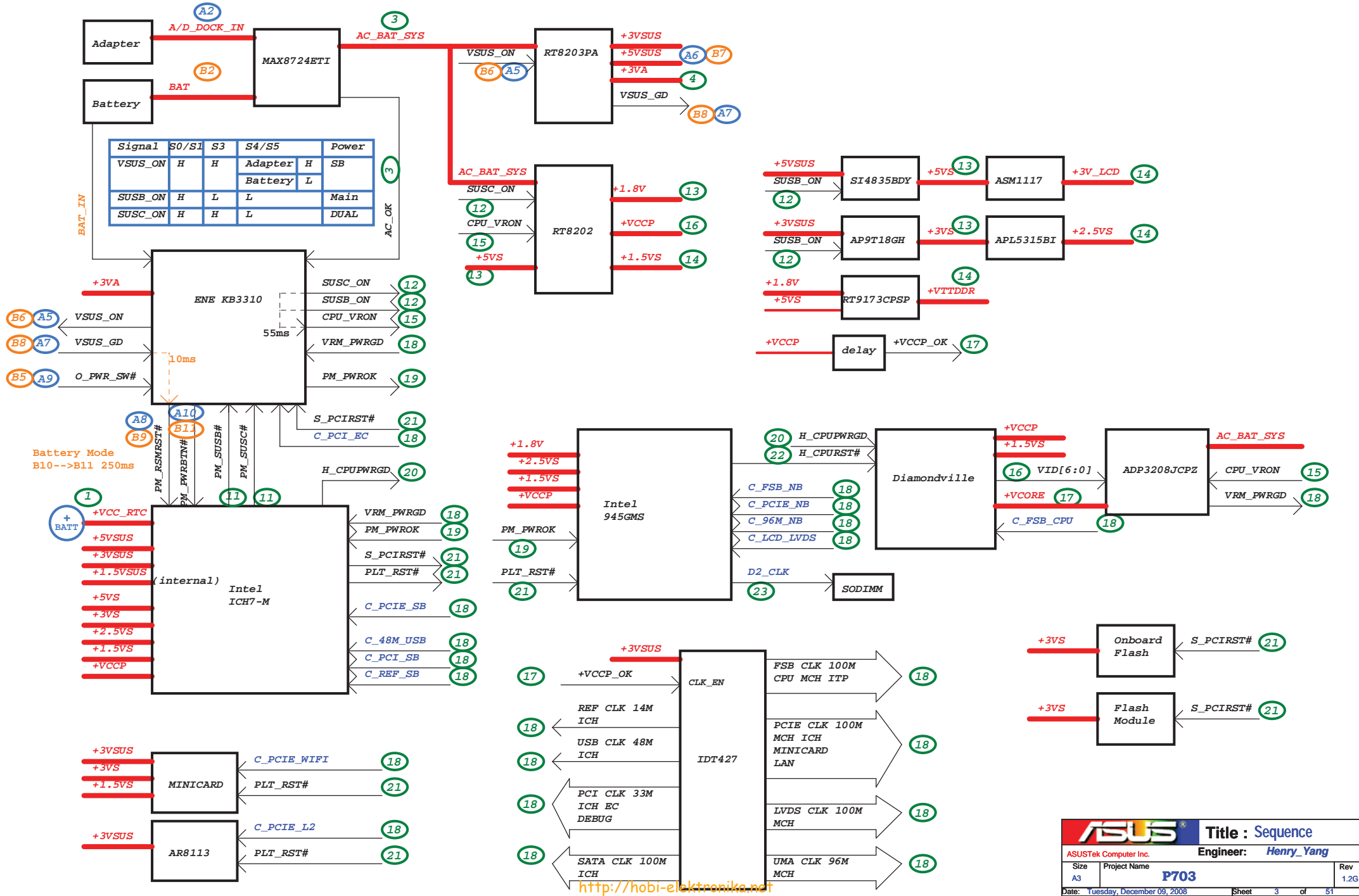


ICH7M GPIO DEFAULT&NOW SETTING

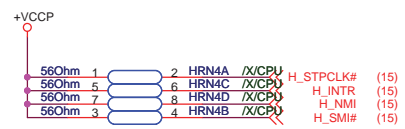
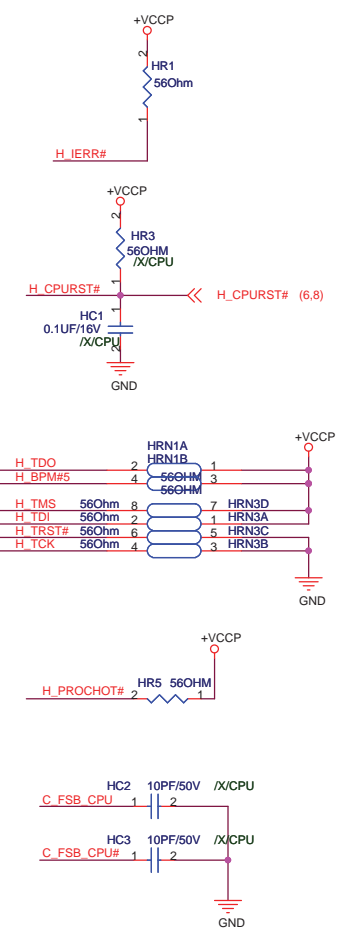
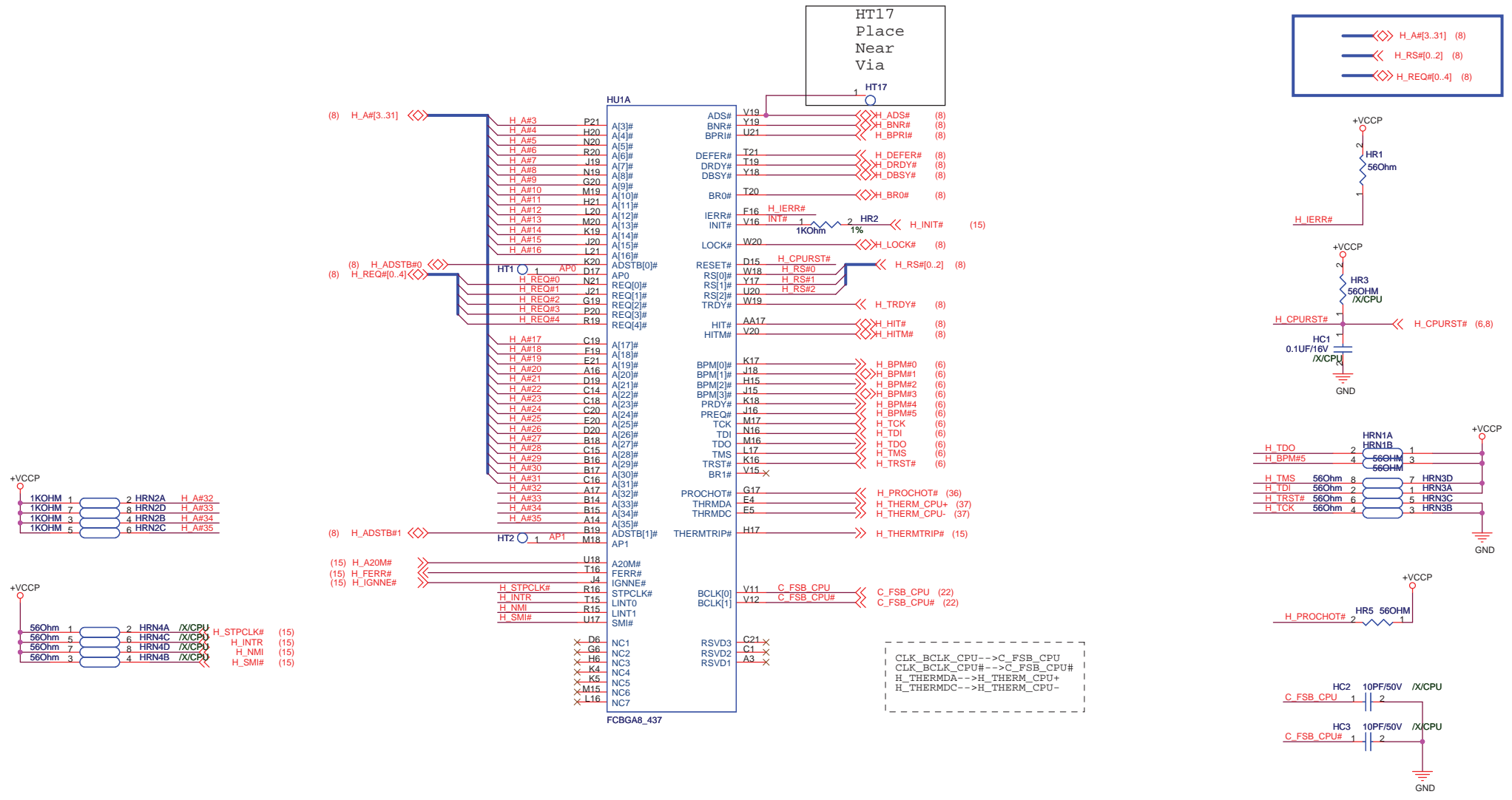
Pin	Pin Name	Type	Tolerance	Powe Well	Default	Now Setting
AB18	GPIO0/BM_BUSY#	I/O	3.3V	CORE	GPI	BM_BUSY#
C8	GPIO1/REQ5#	I/O	5V	CORE	GPI	REQ5#
G8	GPIO2/PIRQE#	I/OD	5V	CORE	GPI	PIRQE#
F7	GPIO3/PIRQF#	I/OD	5V	CORE	GPI	PIRQF#
F8	GPIO4/PIRQG#	I/OD	5V	CORE	GPI	PIRQG#
G7	GPIO5/PIRQH#	I/OD	5V	CORE	GPI	PIRQH#
AC21	GPIO6	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AC18	GPIO7	I/O	3.3V	CORE	GPI	GPO,WLAN_LED
E21	GPIO8	I/O	3.3V	Resume	GPI	GPI,EXTSMI#
E20	GPIO9	I/O	3.3V	Resume	GPI	GPI,No Function,10K Pull +3VS
A20	GPIO10	I/O	3.3V	Resume	GPI	GPO,WLAN_ON#
B23	GPIO11/SMBALERT#	I/O	3.3V	Resume	Native	SMBALERT#
F19	GPIO12	I/O	3.3V	Resume	GPI	GPI,KBC_SCI#
E19	GPIO13	I/O	3.3V	Resume	GPI	GPO,VCCP_DOWN
R4	GPIO14	I/O	3.3V	Resume	GPI	GPO,1.5VS_DOWN
E22	GPIO15	I/O	3.3V	Resume	GPI	GPI,No Function,10K Pull +3VSUS
AC22	GPIO16/DPRSLVR	I/O	3.3V	CORE	Native	DPRSLVR
D8	GPIO17/GNT5#	I/O	3.3V	CORE	GPO	BIOS_SEL1
AC20	GPIO18/STPPC#	I/O	3.3V	CORE	GPO	STP_PC#
AH18	GPIO19/SATA1GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AF21	GPIO20/STPCPU#	I/O	3.3V	CORE	GPO	STP_CPU#
AF19	GPIO21/SATA0GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
A13	GPIO22/REQ4#	I/O	3.3V	CORE	Native	REQ4#
AA5	GPIO23/LDRQ1#	I/O	3.3V	CORE	Native	LDRQ1#
R3	GPIO24	I/O	3.3V	Resume	GPO	GPO,MINICARD1_EN#
D20	GPIO25	I/O	3.3V	Resume	GPO	GPO,DUAL_DOWN

Pin	Pin Name	Type	Tolerance	Powe Well	Default	Now Setting
A21	GPIO26	I/O	3.3V	Resume	GPO	GPO,VCORE_DOWN
B21	GPIO27	I/O	3.3V	Resume	GPO	GPO,CARD_READER_EN#
E23	GPIO28	I/O	3.3V	Resume	GPO	GPO,MODEM_EN#
C3	GPIO29/OC5#	I/O	3.3V	Resume	Native	OC5#
A2	GPIO30/OC6#	I/O	3.3V	Resume	Native	OC6#
B3	GPIO31/OC7#	I/O	3.3V	Resume	Native	OC7#
AG18	GPIO32/CLKRUN#	I/O	3.3V	CORE	GPO	CLKRUN#
AC19	GPIO33/AZ_DOCK_EN#	I/O	3.3V	CORE	GPO	GPO,No Function,NC
U2	GPIO34/AZ_DOCK_RST#	I/O	3.3V	CORE	GPO	GPO,No Function,NC
AD21	GPIO35	I/O	3.3V	CORE	GPO	GPO,CAMERA_EN
AH19	GPIO36/SATA2GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AE19	GPIO37/SATA3GP	I/O	3.3V	CORE	GPI	GPI,PCB_ID0
AE20	GPIO38	I/O	3.3V	CORE	GPI	GPI,PCB_ID1
AD20	GPIO39	I/O	3.3V	CORE	GPI	GPI,PCB_ID2
NA	GPIO40	NA	NA	NA	NA	NA
NA	GPIO41	NA	NA	NA	NA	NA
NA	GPIO42	NA	NA	NA	NA	NA
NA	GPIO43	NA	NA	NA	NA	NA
NA	GPIO44	NA	NA	NA	NA	NA
NA	GPIO45	NA	NA	NA	NA	NA
NA	GPIO46	NA	NA	NA	NA	NA
NA	GPIO47	NA	NA	NA	NA	NA
A14	GPIO48/GNT4#	I/O	3.3V	CORE	Native	BIOS_SEL0
AG24	GPIO49/CPUPWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	CPUPWRGD

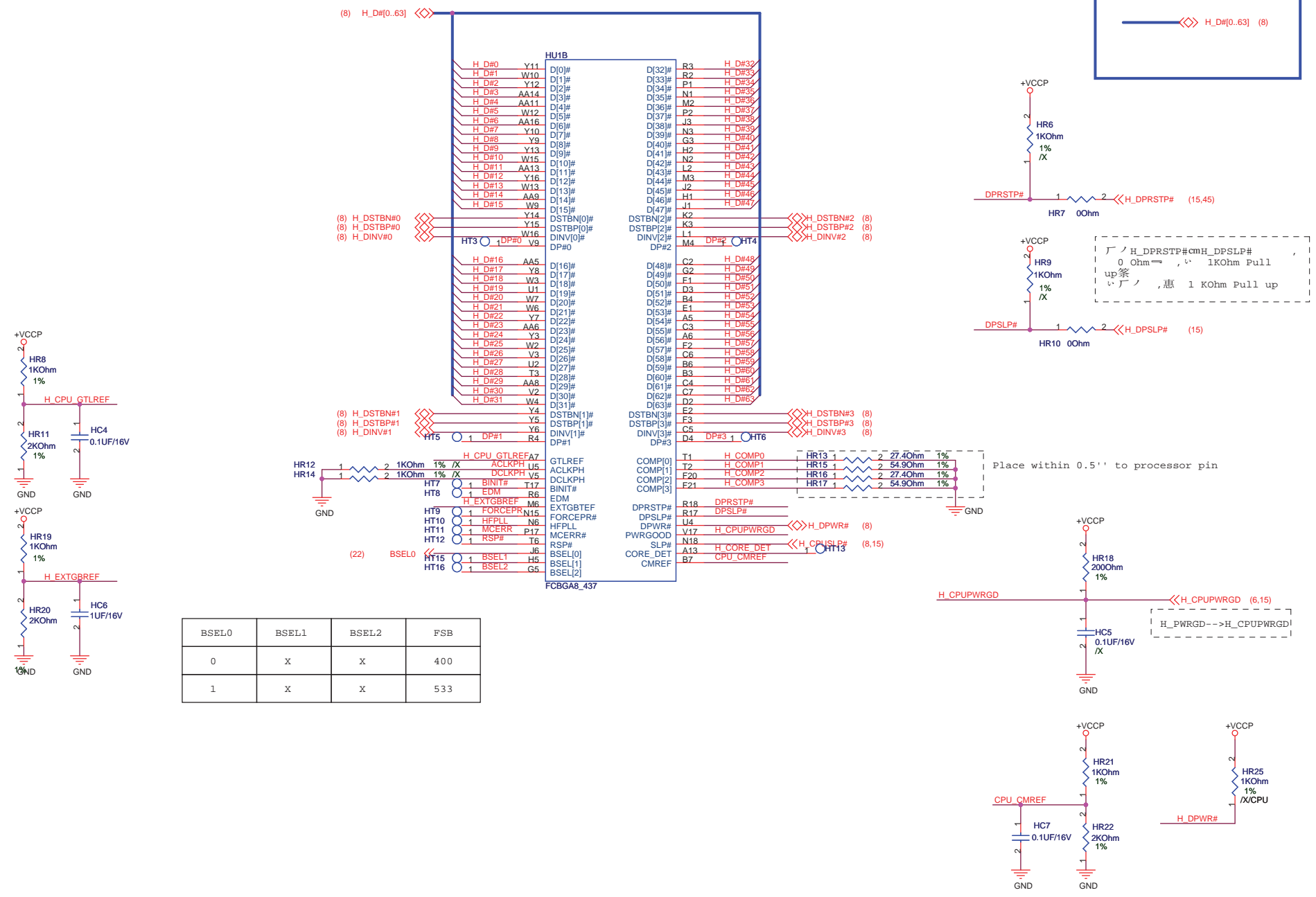
BLUE Anum FOR ADAPTER
 YELLOW Bnum FOR BATTERY ONLY
 GREEN FOR BOTH ADAPTER AND BATTERY



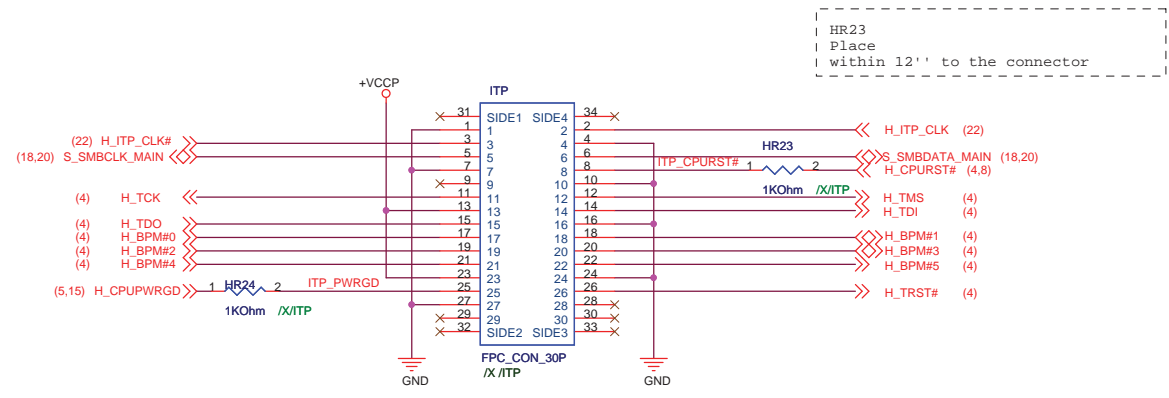
<http://hobi-elektronika.net>



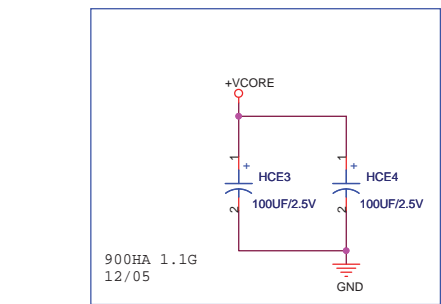
CLK_BCLK_CPU-->C_FSB_CPU
 CLK_BCLK_CPU#-->C_FSB_CPU#
 H_THERMDA-->H_THERM_CPU+
 H_THERMDC-->H_THERM_CPU-



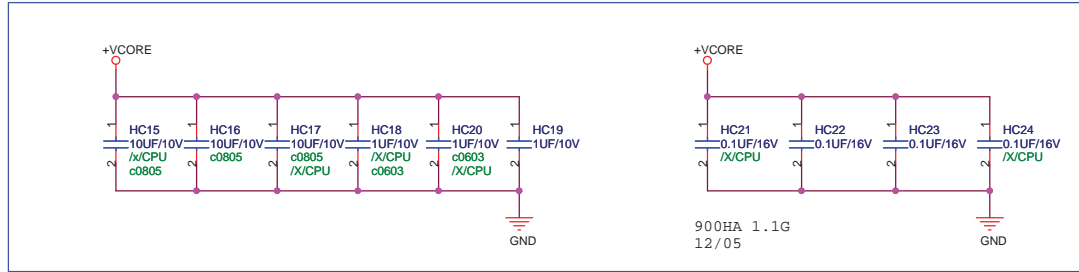
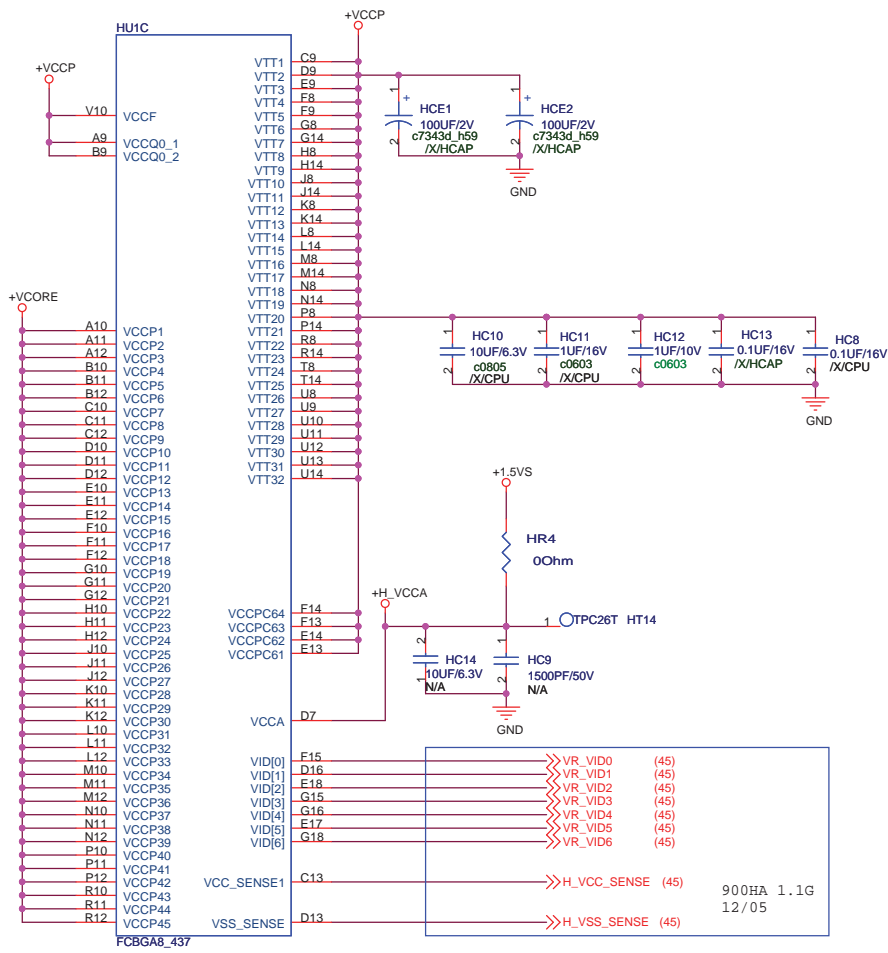
BSEL0	BSEL1	BSEL2	FSB
0	X	X	400
1	X	X	533



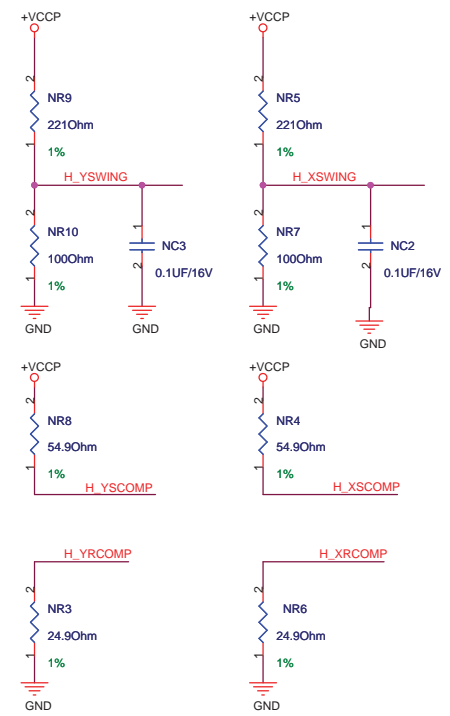
ASUS		Title : ITP	
ASUSTek Computer Inc.		Engineer: <i>Henry_Yang</i>	
Size A3	Project Name P703	Rev 1.2G	
Date: Tuesday, December 09, 2008		Sheet	6 of 51



锁+V CORE 箝背叫把+V CORE 箝隔场



HU1D		
A2	VSS1	N5
A4	VSS2	N7
A8	VSS4	N9
A15	VSS5	N13
A18	VSS6	N17
A19	VSS7	P3
A20	VSS8	P5
B1	VSS9	P6
B2	VSS10	P7
B5	VSS11	P8
B8	VSS12	P9
B13	VSS13	P13
B20	VSS14	P15
B21	VSS15	P18
C3	VSS16	P19
C17	VSS17	R1
D1	VSS18	R13
D5	VSS19	R5
D8	VSS20	R7
D14	VSS21	R9
D18	VSS22	R13
D21	VSS23	R21
E3	VSS24	T4
E6	VSS25	T5
E7	VSS26	T7
E8	VSS27	T9
E15	VSS28	T10
E16	VSS29	T11
E19	VSS30	T12
F4	VSS31	T13
F5	VSS32	T18
F6	VSS33	U3
F7	VSS34	U6
F17	VSS35	U7
G1	VSS36	U15
G4	VSS37	U16
G7	VSS38	U19
G9	VSS39	V1
G13	VSS41	V4
G21	VSS42	V7
H3	VSS45	V8
H4	VSS46	V13
H7	VSS49	V14
H9	VSS51	V18
H13	VSS52	V21
H16	VSS53	W1
H18	VSS54	W6
H19	VSS55	W8
J5	VSS56	W11
J7	VSS57	W14
J9	VSS58	W17
J13	VSS59	W21
J17	VSS60	Y1
K1	VSS61	Y2
K6	VSS62	Y20
K7	VSS63	Y21
K9	VSS64	AA2
K13	VSS65	AA3
K15	VSS66	AA4
K21	VSS67	AA7
L3	VSS68	AA10
L4	VSS69	AA12
L5	VSS70	AA15
L6	VSS71	AA18
L7	VSS72	AA19
L9	VSS73	AA20
L13	VSS74	
L15	VSS75	
L18	VSS76	
L19	VSS77	
M1	VSS78	
M5	VSS79	
M7	VSS80	
M9	VSS81	
M13	VSS82	
M21	VSS83	
N4	VSS84	
		GND



Voltage Swing

For Providing a Reference Voltage to the FSB RCOMP circuit

Signal voltage level = $0.3125 * V_{CCP}$

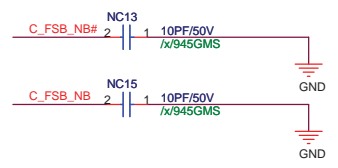
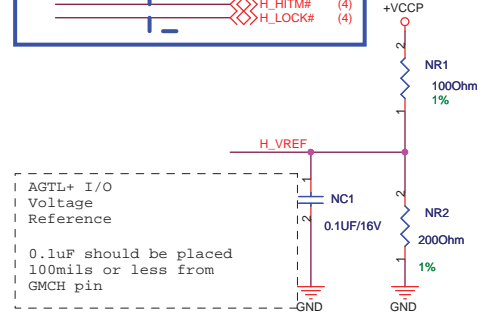
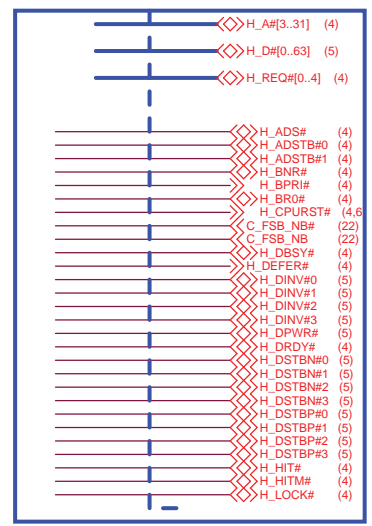
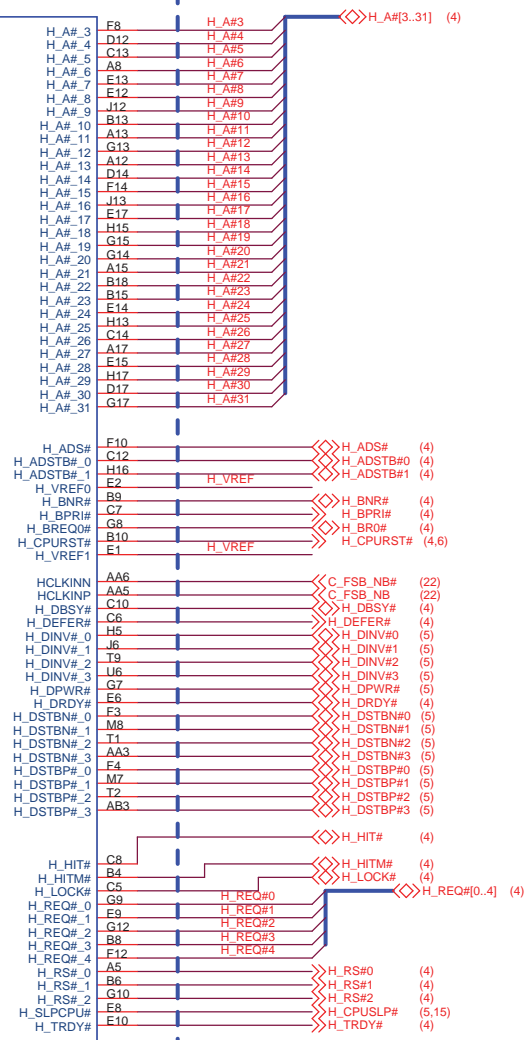
Trace should be 10 mil wide with 20 mil spacing

For Slow Rate Compensation on the FSB

For Calibrating the FSB I/O Buffer

H_D#0	C4	H_D#_0	H_A#_3
H_D#1	F6	H_D#_1	H_A#_4
H_D#2	H9	H_D#_2	H_A#_5
H_D#3	H6	H_D#_3	H_A#_6
H_D#4	F7	H_D#_4	H_A#_7
H_D#5	E3	H_D#_5	H_A#_8
H_D#6	C2	H_D#_6	H_A#_9
H_D#7	C3	H_D#_7	H_A#_10
H_D#8	K9	H_D#_8	H_A#_11
H_D#9	F5	H_D#_9	H_A#_12
H_D#10	J7	H_D#_10	H_A#_13
H_D#11	K7	H_D#_11	H_A#_14
H_D#12	H8	H_D#_12	H_A#_15
H_D#13	E5	H_D#_13	H_A#_16
H_D#14	K8	H_D#_14	H_A#_17
H_D#15	J8	H_D#_15	H_A#_18
H_D#16	J2	H_D#_16	H_A#_19
H_D#17	J3	H_D#_17	H_A#_20
H_D#18	N1	H_D#_18	H_A#_21
H_D#19	M5	H_D#_19	H_A#_22
H_D#20	K5	H_D#_20	H_A#_23
H_D#21	J5	H_D#_21	H_A#_24
H_D#22	H3	H_D#_22	H_A#_25
H_D#23	J4	H_D#_23	H_A#_26
H_D#24	N3	H_D#_24	H_A#_27
H_D#25	M4	H_D#_25	H_A#_28
H_D#26	M3	H_D#_26	H_A#_29
H_D#27	N8	H_D#_27	H_A#_30
H_D#28	N6	H_D#_28	H_A#_31
H_D#29	K9	H_D#_29	
H_D#30	N9	H_D#_30	
H_D#31	M1	H_D#_31	
H_D#32	V8	H_D#_32	
H_D#33	V9	H_D#_33	
H_D#34	R6	H_D#_34	
H_D#35	T8	H_D#_35	
H_D#36	R2	H_D#_36	
H_D#37	N5	H_D#_37	
H_D#38	N2	H_D#_38	
H_D#39	R5	H_D#_39	
H_D#40	U7	H_D#_40	
H_D#41	R8	H_D#_41	
H_D#42	T4	H_D#_42	
H_D#43	T7	H_D#_43	
H_D#44	R3	H_D#_44	
H_D#45	T5	H_D#_45	
H_D#46	V6	H_D#_46	
H_D#47	V3	H_D#_47	
H_D#48	W2	H_D#_48	
H_D#49	Y2	H_D#_49	
H_D#50	W1	H_D#_50	
H_D#51	W4	H_D#_51	
H_D#52	W7	H_D#_52	
H_D#53	W5	H_D#_53	
H_D#54	V5	H_D#_54	
H_D#55	AB8	H_D#_55	
H_D#56	AB4	H_D#_56	
H_D#57	W8	H_D#_57	
H_D#58	AA9	H_D#_58	
H_D#59	AA8	H_D#_59	
H_D#60	AB1	H_D#_60	
H_D#61	AB7	H_D#_61	
H_D#62	AA2	H_D#_62	
H_D#63	AB5	H_D#_63	

HOST



H_XRCOMP	A10	H_XRCOMP
H_XSCOMP	A6	H_XSCOMP
H_XSWING	C15	H_XSWING
H_YRCOMP	J1	H_YRCOMP
H_YSCOMP	K1	H_YSCOMP
H_YSWING	H1	H_YSWING

945GMS

<-Variant Name>

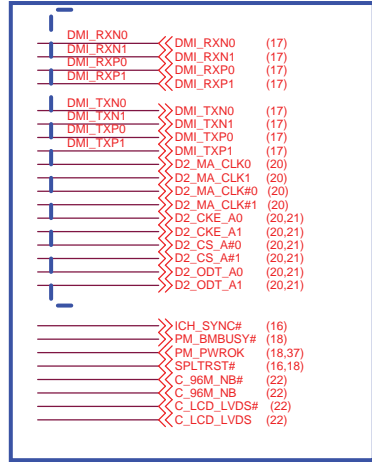
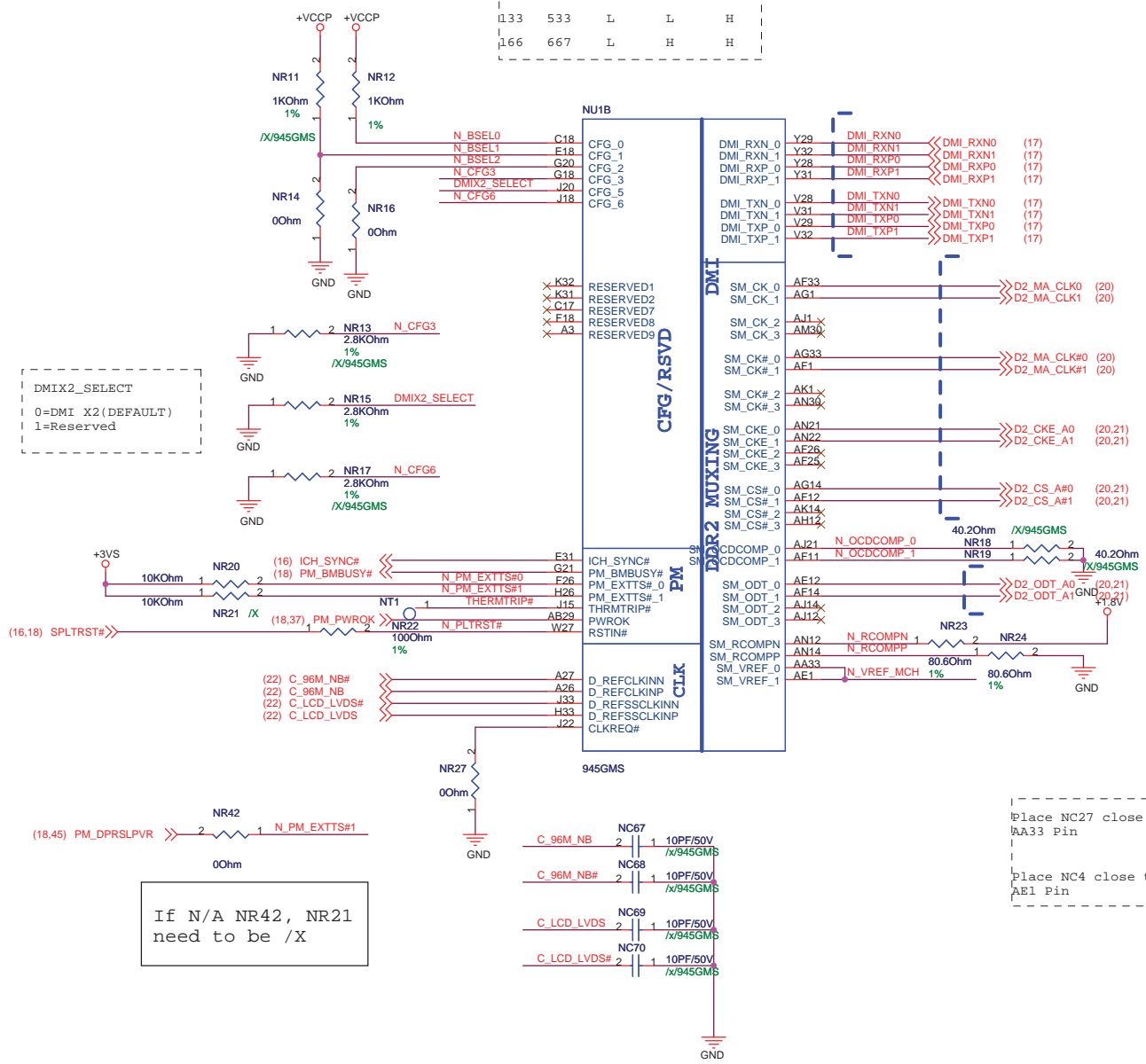
ASUS Title : 945GMS(HOST)

ASUSTeK COMPUTER INC. Engineer: Henry_Yang

Size	Project Name	Rev
A3	P703	1.2G

Date: Tuesday, December 09, 2008 Sheet 8 of 51

BCLK	FSB	BSEL2	BSEL1	BSEL0
L33	533	L	L	H
L66	667	L	H	H



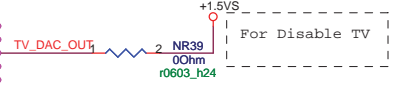
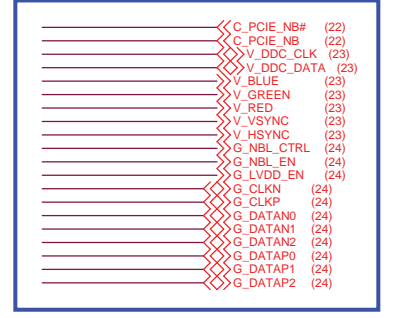
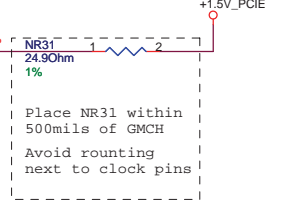
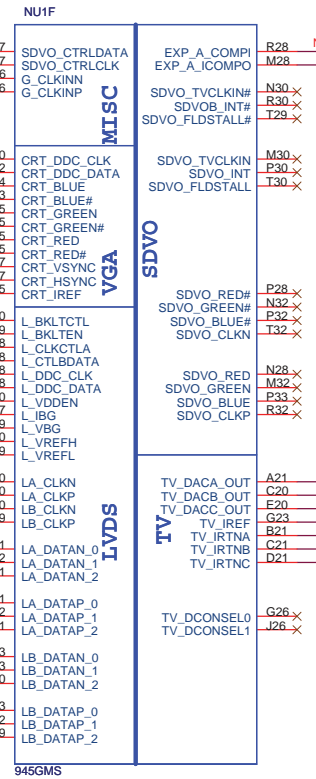
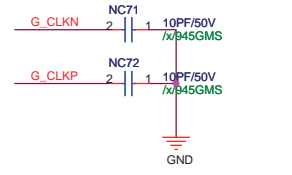
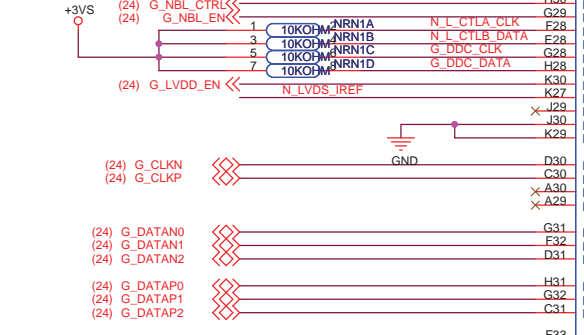
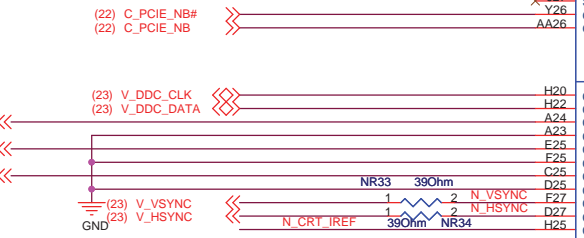
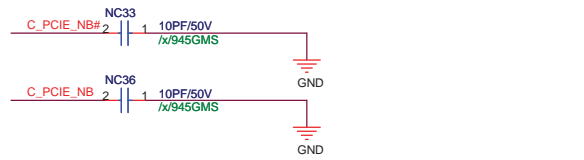
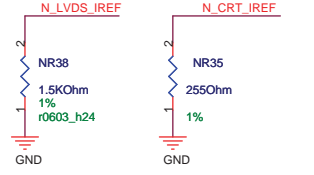
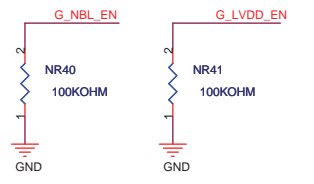
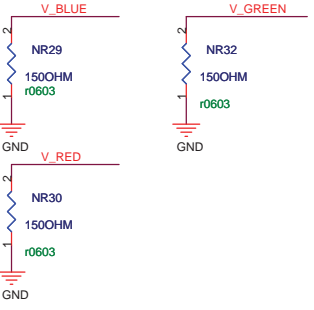
DMIX2_SELECT
0=DMI X2 (DEFAULT)
1=Reserved

If N/A NR42, NR21 need to be /X

Place NC27 close to A33 Pin
Place NC4 close to A61 Pin

ASUS		Title : 945GSE(DMI)	
ASUSTek Computer Inc.		Engineer: Henry_Yang	
Size A3	Project Name P703	Date: Tuesday, December 09, 2008	Rev 1.2G
Sheet 9 of 51			

NR29
NR30
NR32
Close to
GMCH



(20) D2_DQ_A[0..63] <>

NU1C

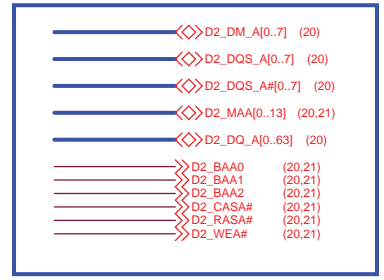
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D2_DQ_A1	AB28	SA_DQ_1
D2_DQ_A2	AE33	SA_DQ_2
D2_DQ_A3	AC33	SA_DQ_3
D2_DQ_A4	AF32	SA_DQ_4
D2_DQ_A5	AB32	SA_DQ_5
D2_DQ_A6	AB31	SA_DQ_6
D2_DQ_A7	AE31	SA_DQ_7
D2_DQ_A8	AH31	SA_DQ_8
D2_DQ_A9	AK31	SA_DQ_9
D2_DQ_A10	AL28	SA_DQ_10
D2_DQ_A11	AK27	SA_DQ_11
D2_DQ_A12	AH30	SA_DQ_12
D2_DQ_A13	AL32	SA_DQ_13
D2_DQ_A14	AJ28	SA_DQ_14
D2_DQ_A15	AJ27	SA_DQ_15
D2_DQ_A16	AH32	SA_DQ_16
D2_DQ_A17	AF31	SA_DQ_17
D2_DQ_A18	AH27	SA_DQ_18
D2_DQ_A19	AF28	SA_DQ_19
D2_DQ_A20	AJ32	SA_DQ_20
D2_DQ_A21	AG31	SA_DQ_21
D2_DQ_A22	AG28	SA_DQ_22
D2_DQ_A23	AG27	SA_DQ_23
D2_DQ_A24	AN27	SA_DQ_24
D2_DQ_A25	AM26	SA_DQ_25
D2_DQ_A26	AJ26	SA_DQ_26
D2_DQ_A27	AJ25	SA_DQ_27
D2_DQ_A28	AL27	SA_DQ_28
D2_DQ_A29	AN26	SA_DQ_29
D2_DQ_A30	AH25	SA_DQ_30
D2_DQ_A31	AG26	SA_DQ_31
D2_DQ_A32	AM12	SA_DQ_32
D2_DQ_A33	AL11	SA_DQ_33
D2_DQ_A34	AH9	SA_DQ_34
D2_DQ_A35	AK9	SA_DQ_35
D2_DQ_A36	AM11	SA_DQ_36
D2_DQ_A37	AK11	SA_DQ_37
D2_DQ_A38	AM8	SA_DQ_38
D2_DQ_A39	AK8	SA_DQ_39
D2_DQ_A40	AG9	SA_DQ_40
D2_DQ_A41	AF9	SA_DQ_41
D2_DQ_A42	AF8	SA_DQ_42
D2_DQ_A43	AK6	SA_DQ_43
D2_DQ_A44	AE7	SA_DQ_44
D2_DQ_A45	AG11	SA_DQ_45
D2_DQ_A46	AJ6	SA_DQ_46
D2_DQ_A47	AH6	SA_DQ_47
D2_DQ_A48	AN6	SA_DQ_48
D2_DQ_A49	AM6	SA_DQ_49
D2_DQ_A50	AK3	SA_DQ_50
D2_DQ_A51	AL2	SA_DQ_51
D2_DQ_A52	AM5	SA_DQ_52
D2_DQ_A53	AL5	SA_DQ_53
D2_DQ_A54	AJ3	SA_DQ_54
D2_DQ_A55	AJ2	SA_DQ_55
D2_DQ_A56	AG2	SA_DQ_56
D2_DQ_A57	AE3	SA_DQ_57
D2_DQ_A58	AE7	SA_DQ_58
D2_DQ_A59	AF6	SA_DQ_59
D2_DQ_A60	AH5	SA_DQ_60
D2_DQ_A61	AG3	SA_DQ_61
D2_DQ_A62	AG8	SA_DQ_62
D2_DQ_A63	AF9	SA_DQ_63

DDR2 SYSTEM MEMORY

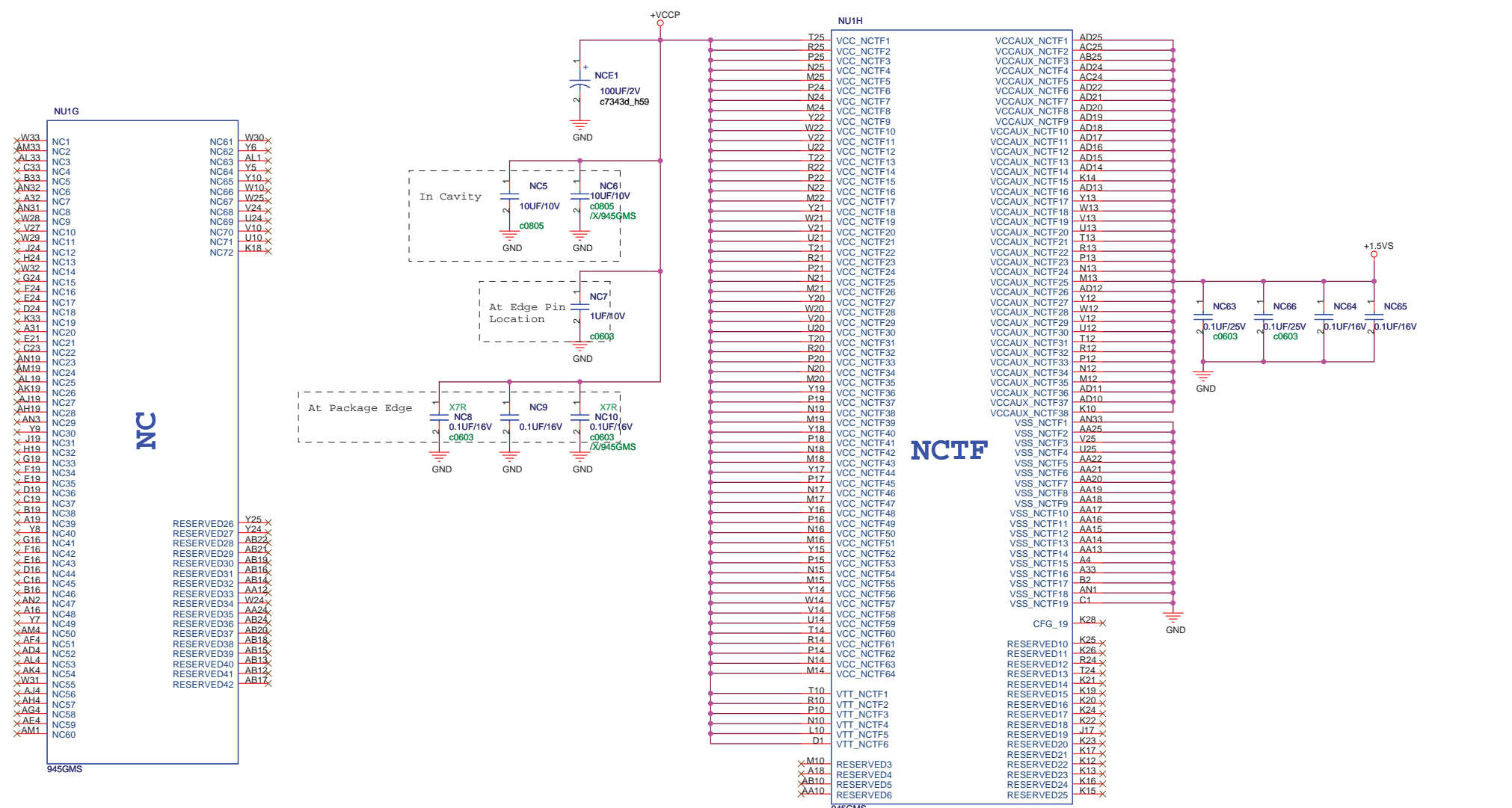
SA_BS_0	AK12	D2_BAA0	(20,21)
SA_BS_1	AH11	D2_BAA1	(20,21)
SA_BS_2	AG17	D2_BAA2	(20,21)
		D2_DM_A[0..7]	(20)
SA_DM_0	AB30	D2_DM_A0	
SA_DM_1	AL31	D2_DM_A1	
SA_DM_2	AF30	D2_DM_A2	
SA_DM_3	AK26	D2_DM_A3	
SA_DM_4	AL9	D2_DM_A4	
SA_DM_5	AG7	D2_DM_A5	
SA_DM_6	AK5	D2_DM_A6	
SA_DM_7	AH3	D2_DM_A7	
		D2_DQS_A[0..7]	(20)
SA_DQS_0	AC28	D2_DQS_A0	
SA_DQS_1	AJ30	D2_DQS_A1	
SA_DQS_2	AK33	D2_DQS_A2	
SA_DQS_3	AL25	D2_DQS_A3	
SA_DQS_4	AN9	D2_DQS_A4	
SA_DQS_5	AH8	D2_DQS_A5	
SA_DQS_6	AM2	D2_DQS_A6	
SA_DQS_7	AE3	D2_DQS_A7	
		D2_DQS_A#[0..7]	(20)
SA_DQS#_0	AC29	D2_DQS_A#0	
SA_DQS#_1	AK30	D2_DQS_A#1	
SA_DQS#_2	AJ33	D2_DQS_A#2	
SA_DQS#_3	AM25	D2_DQS_A#3	
SA_DQS#_4	AN8	D2_DQS_A#4	
SA_DQS#_5	AJ8	D2_DQS_A#5	
SA_DQS#_6	AM3	D2_DQS_A#6	
SA_DQS#_7	AE2	D2_DQS_A#7	
		D2_MAA[0..13]	(20,21)
SA_MA_0	AJ15	D2_MAA0	
SA_MA_1	AM17	D2_MAA1	
SA_MA_2	AM15	D2_MAA2	
SA_MA_3	AH15	D2_MAA3	
SA_MA_4	AK15	D2_MAA4	
SA_MA_5	AM15	D2_MAA5	
SA_MA_6	AJ19	D2_MAA6	
SA_MA_7	AF19	D2_MAA7	
SA_MA_8	AN17	D2_MAA8	
SA_MA_9	AL17	D2_MAA9	
SA_MA_10	AG16	D2_MAA10	
SA_MA_11	AL18	D2_MAA11	
SA_MA_12	AG18	D2_MAA12	
SA_MA_13	AL14	D2_MAA13	
		D2_CASA#	(20,21)
SA_CASA#	AJ17		
		D2_RASA#	(20,21)
SA_RASA#	AK18		
SA_RCVENIN#	AN28		
SA_RCVENOUT#	AM28		
		D2_WEA#	(20,21)
SA_WEA#	AH17		
SB_BS_0	AH21		
SB_BS_1	AJ20		
SB_BS_2	AE23		
SB_MA_0	AN20		
SB_MA_1	AL21		
SB_MA_2	AK21		
SB_MA_3	AK23		
SB_MA_4	AL22		
SB_MA_5	AH22		
SB_MA_6	AG22		
SB_MA_7	AE21		
SB_MA_8	AM21		
SB_MA_9	AE21		
SB_MA_10	AL20		
SB_MA_11	AE22		
SB_MA_12	AE26		
SB_MA_13	AE26		

AG19 SB_CAS#
AG21 SB_RAS#
AG20 SB_WE#

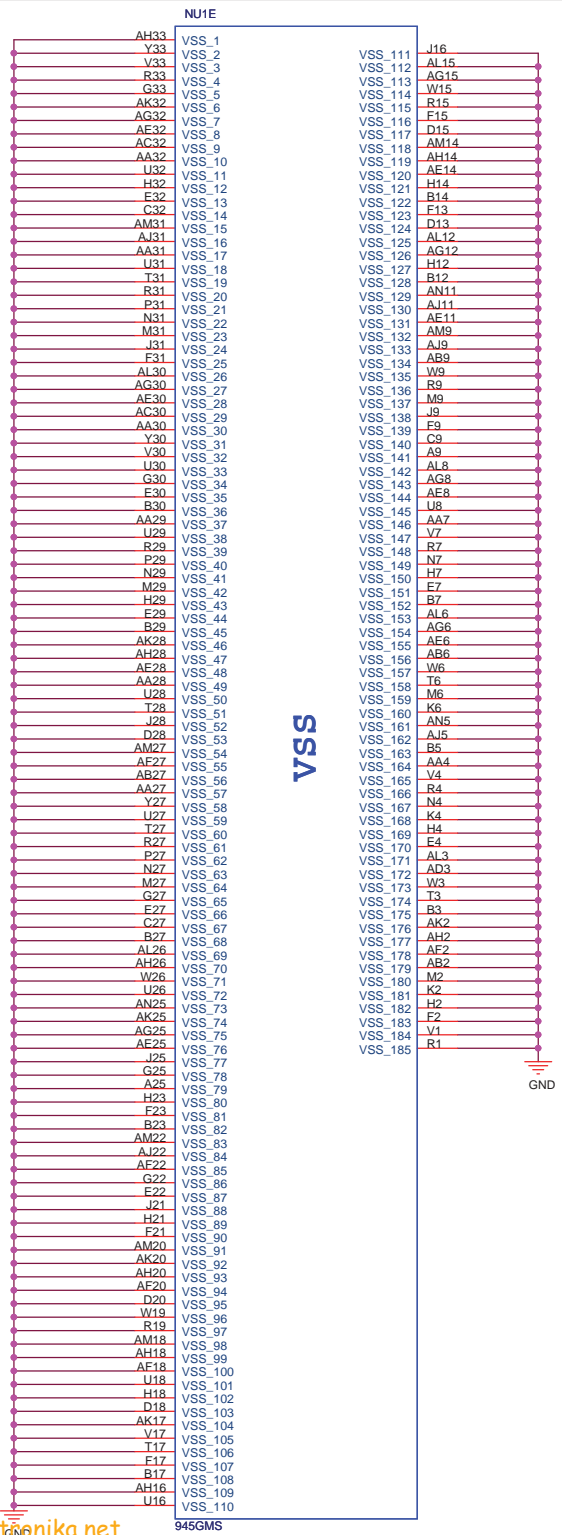
945GMS



ASUS		Title : 945GSE(DDR)	
ASUSTek Computer Inc.		Engineer: Henry_Yang	
Size A3	Project Name P703	Date: Tuesday, December 09, 2008	Rev 1.2G
Date: Tuesday, December 09, 2008		Sheet 11	of 51

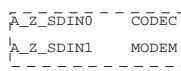
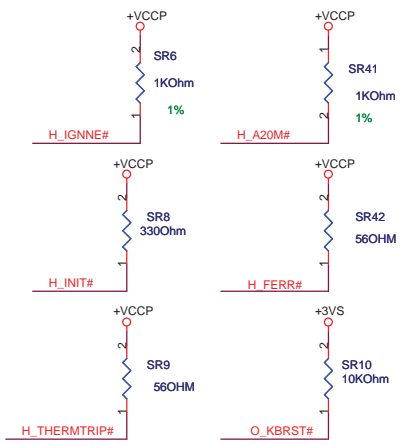
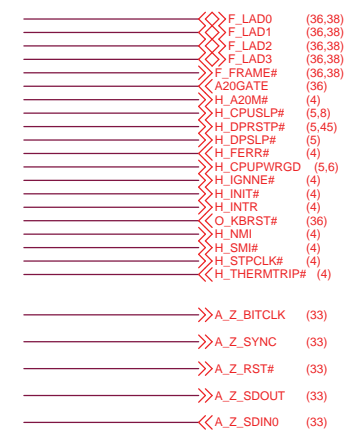
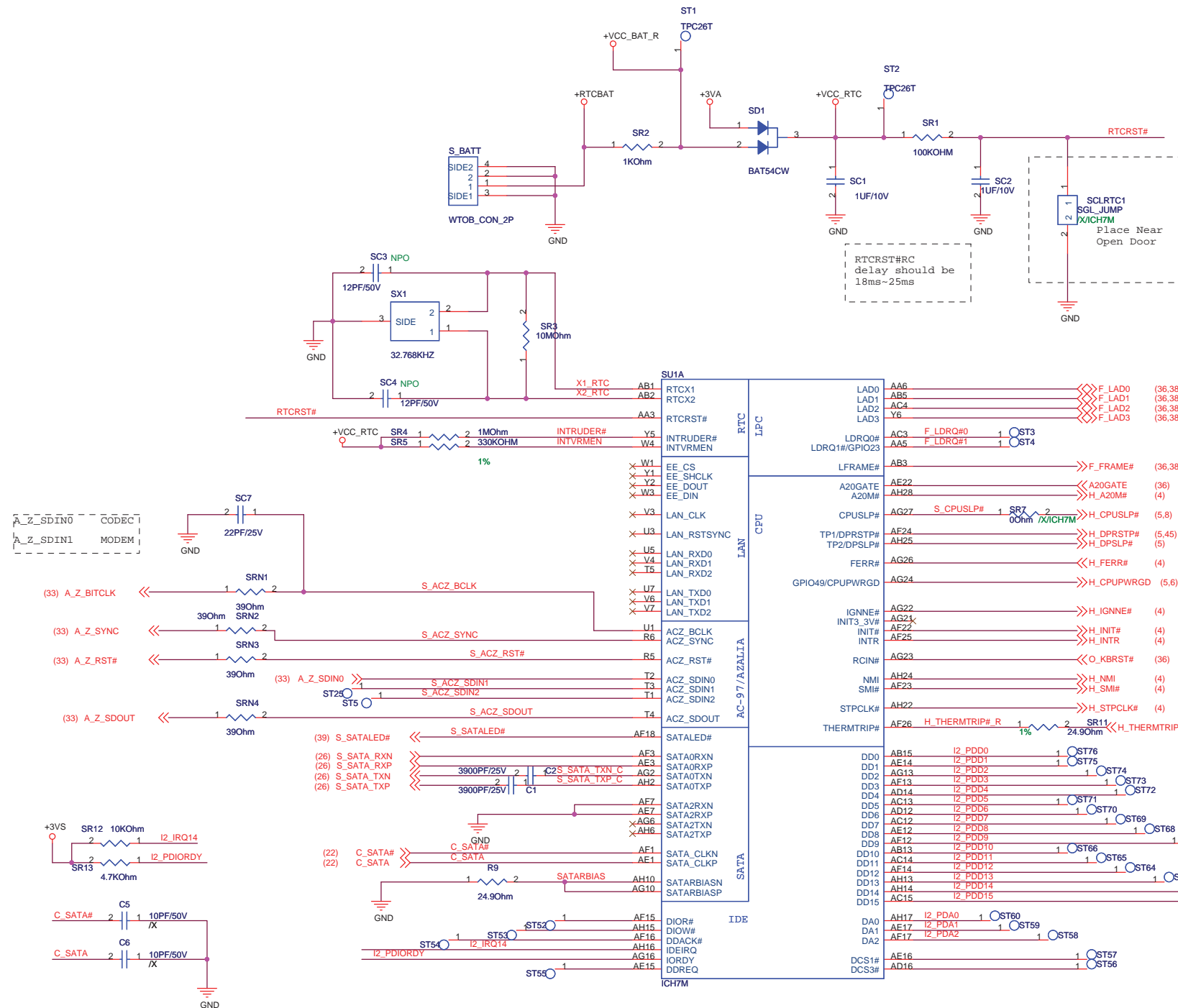


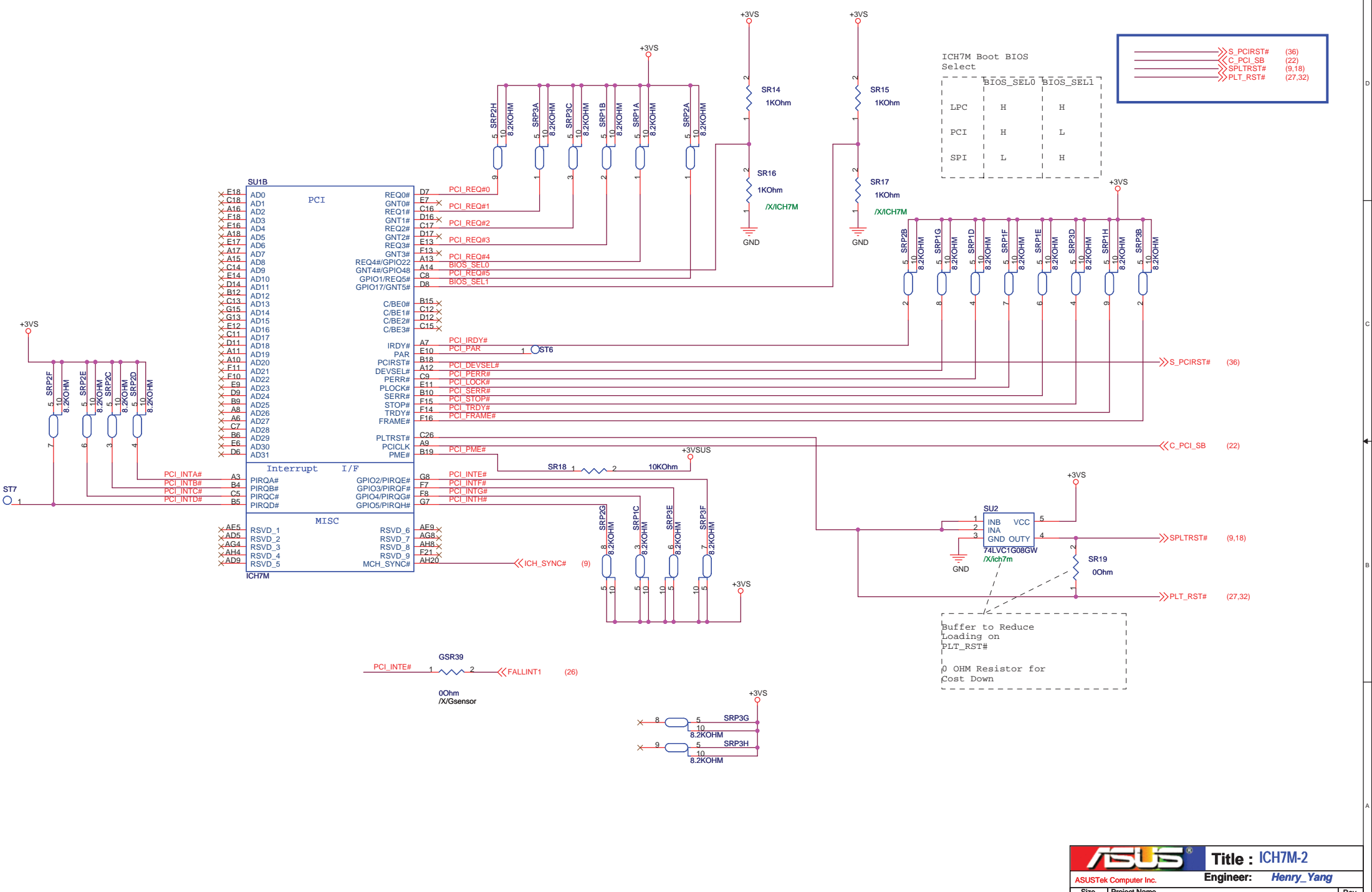
ASUS Title : 945GSE(NC,PWR)
 ASUSTek Computer Inc. Engineer: Henry_Yang
 Size A3 Project Name P703 Rev 1.2G
 Date: Tuesday, December 09, 2008 Sheet 12 of 51



VSS

		Title : 945GSE(GND)	
ASUSTek Computer Inc.		Engineer: Henry_Yang	
Size A3	Project Name P703	Date Tuesday, December 09, 2008	Rev 1.2G
Date: Tuesday, December 09, 2008		Sheet 14 of 51	

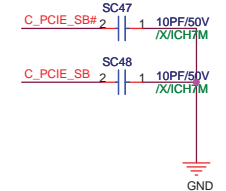
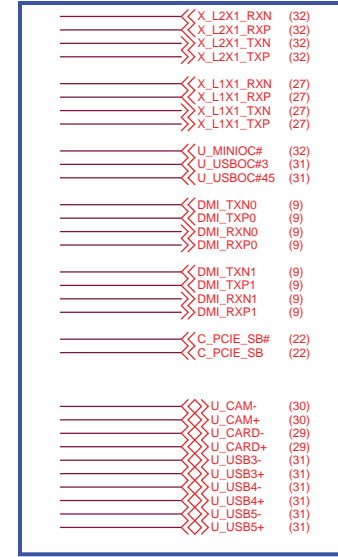
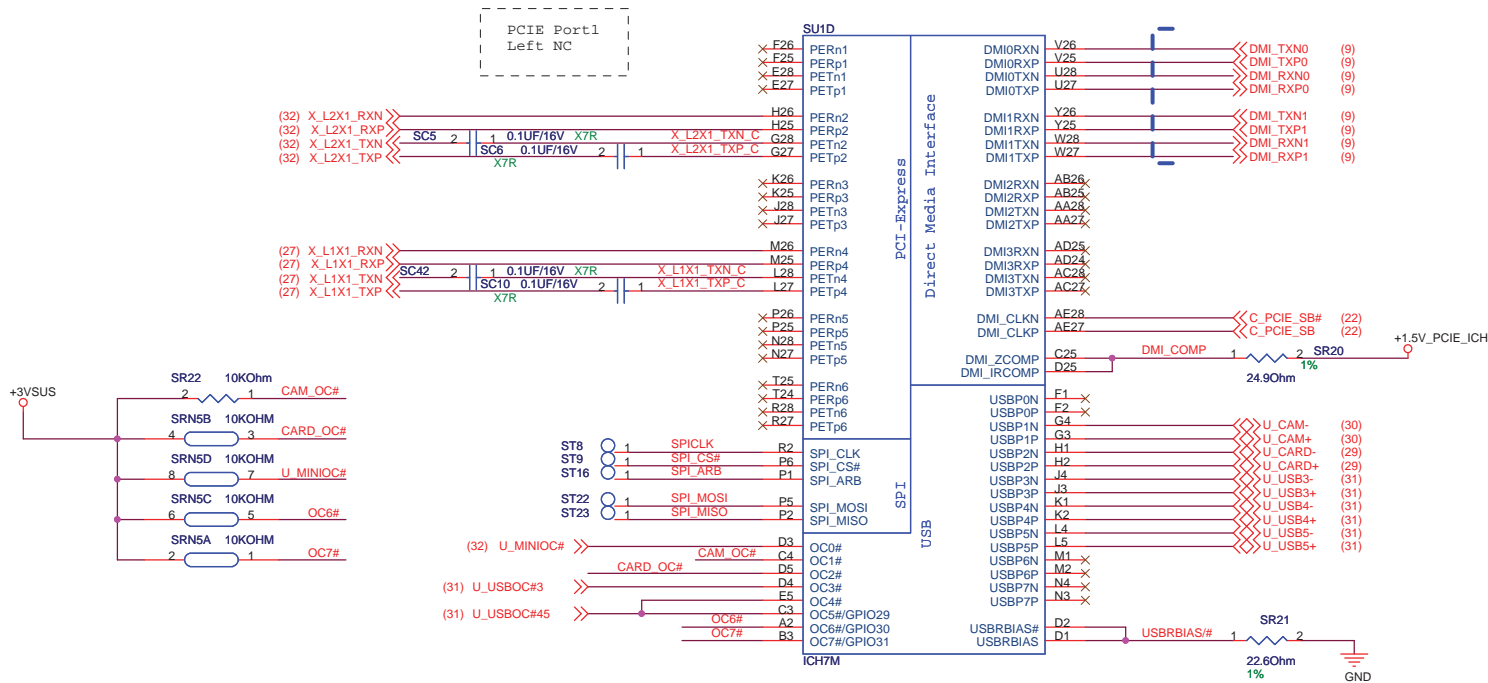




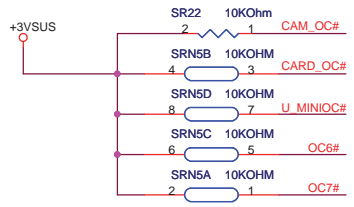
ICH7M Boot BIOS Select		
	BIOS_SEL0	BIOS_SEL1
LPC	H	H
PCI	H	L
SPI	L	H

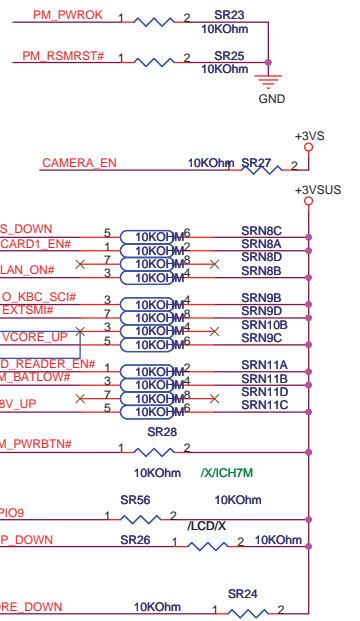
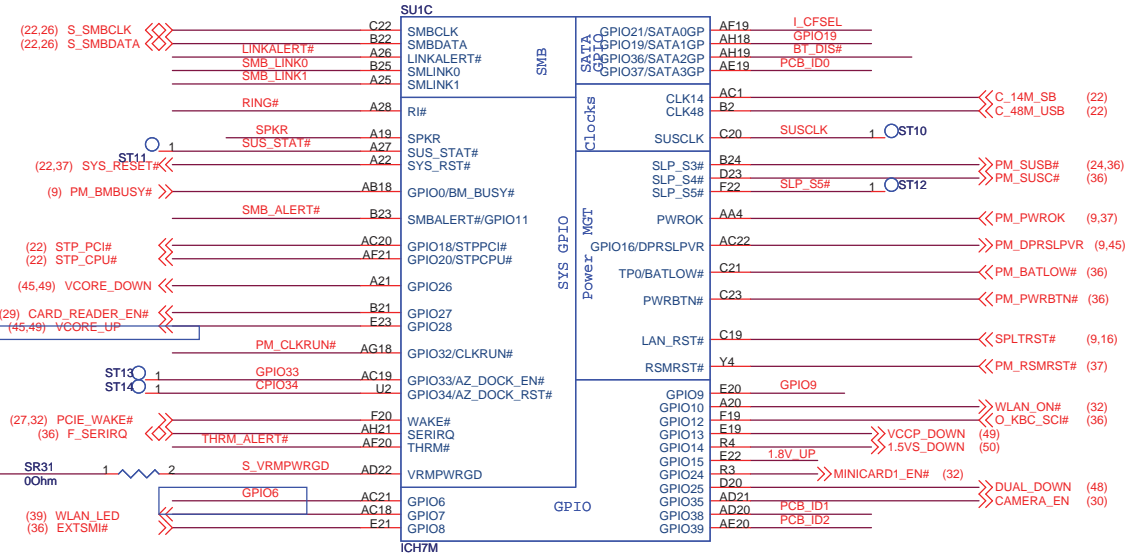
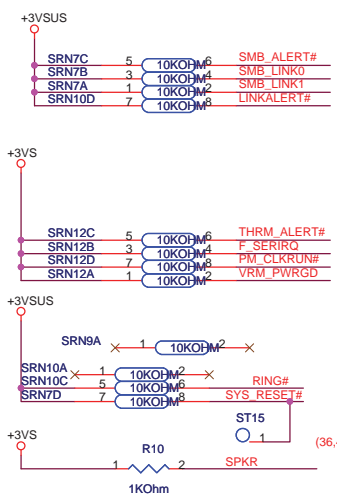
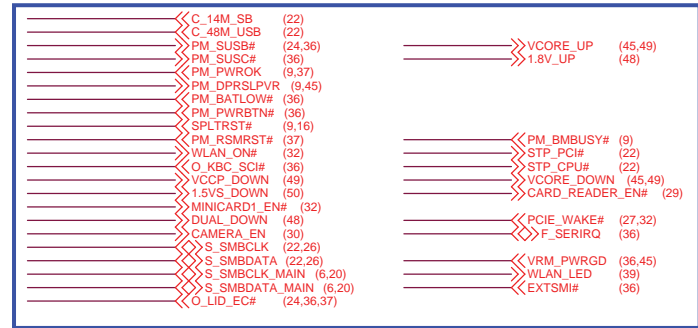
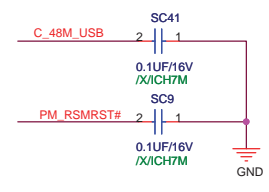
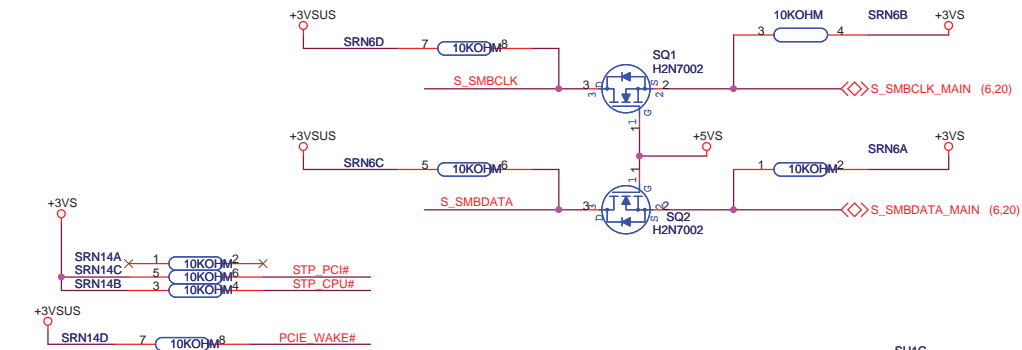
→ S_PCIRST#	(36)
→ C_PCI_SB	(22)
→ SPLTRST#	(9,18)
→ PLT_RST#	(27,32)

Buffer to Reduce Loading on PLT_RST#
0 OHM Resistor for Cost Down



USB0	Minicard
USB1	Camera
USB2	Card Reader
USB3	USB CONN
USB4	USB CONN
USB5	USB CONN
USB6	NC
USB7	NC

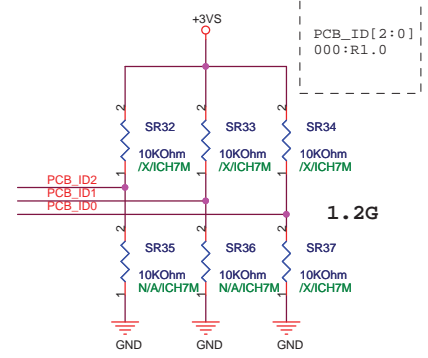
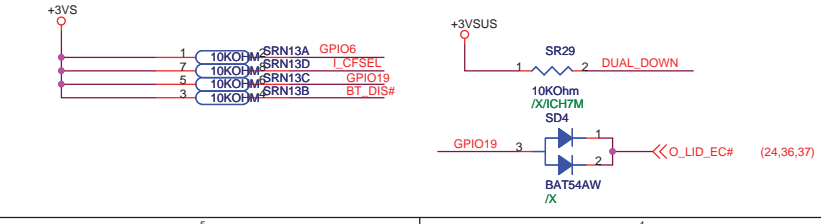


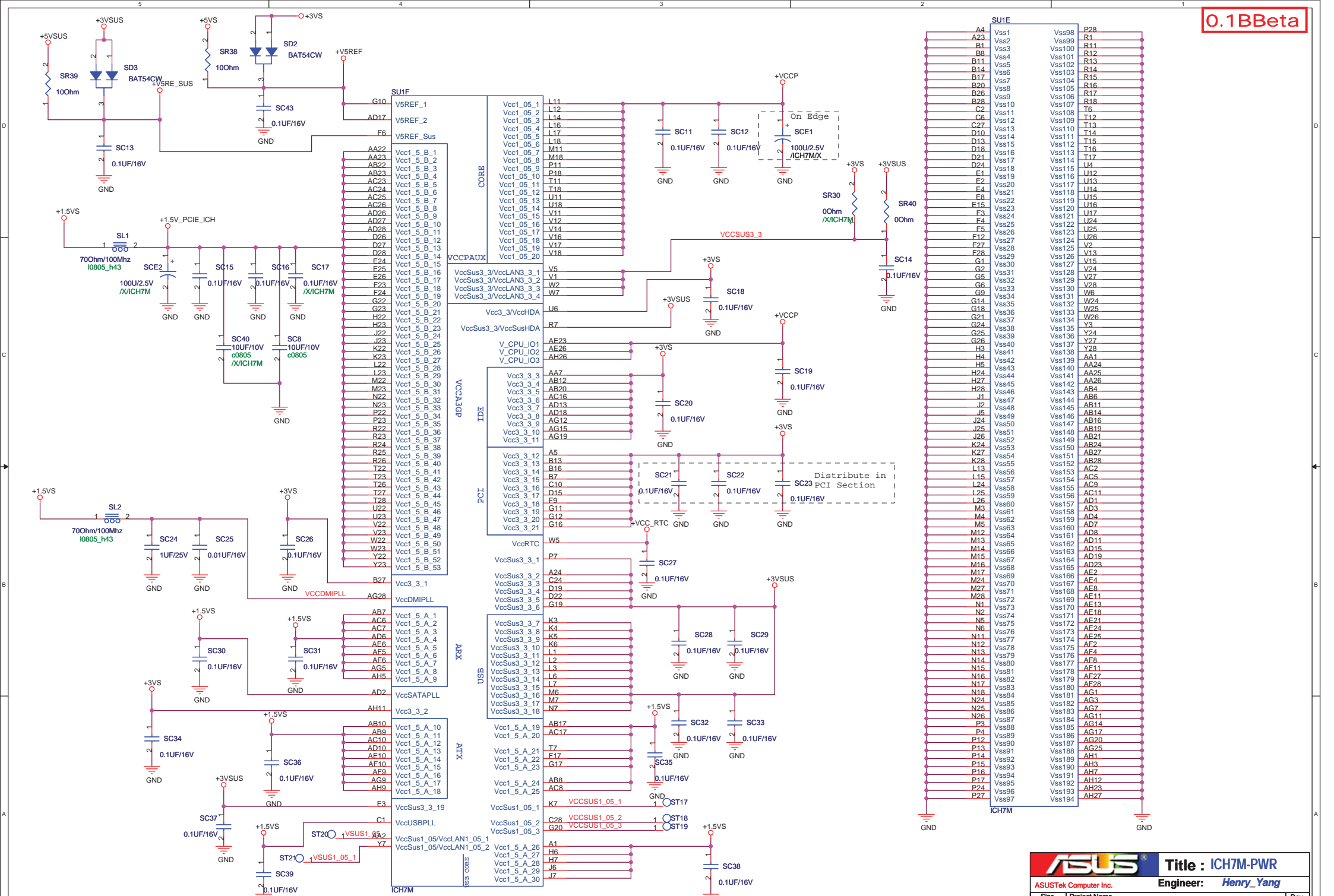


WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

programme GPIO28 as Vcore_Up
9000HA 1.1G
12/05

PCBID[1,2]=00
== 1.3G PCB

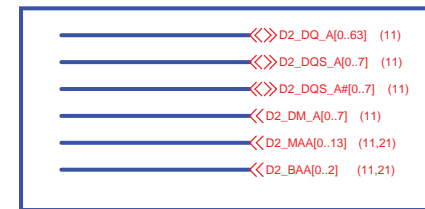




ASUS Title : ICH7M-PWR
 ASUSTek Computer Inc. Engineer: Henry_Yang

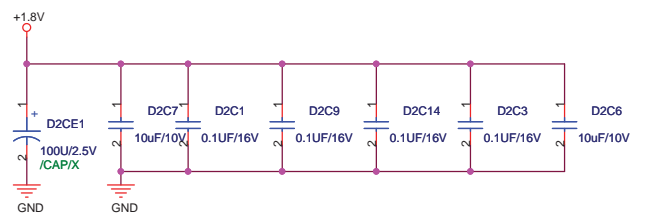
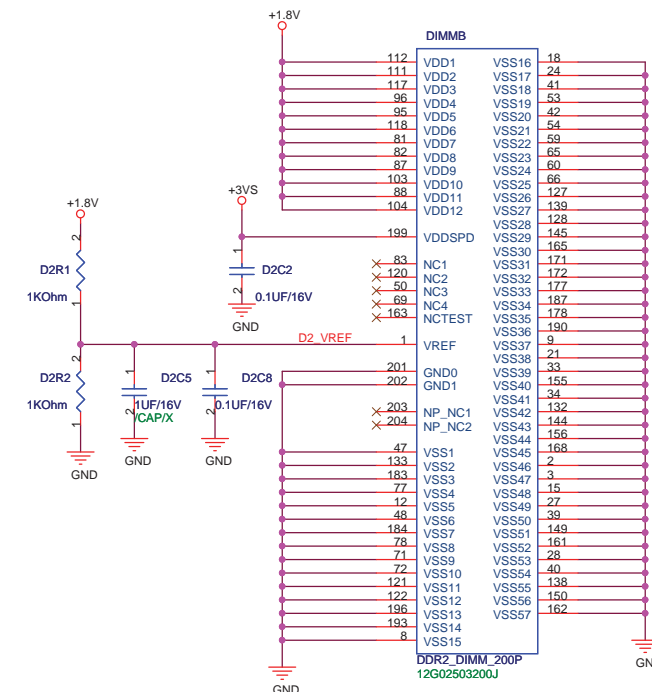
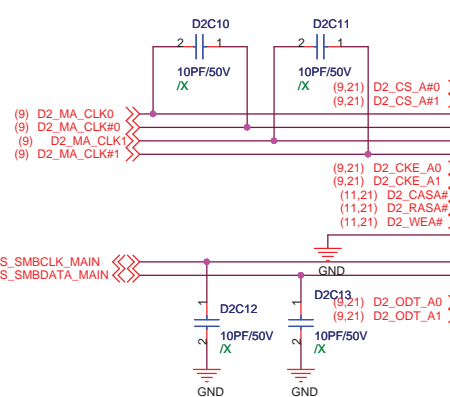
Size	Project Name	Rev
A3	P703	1.2G
Date: Tuesday, December 09, 2008	Sheet	19 of 51

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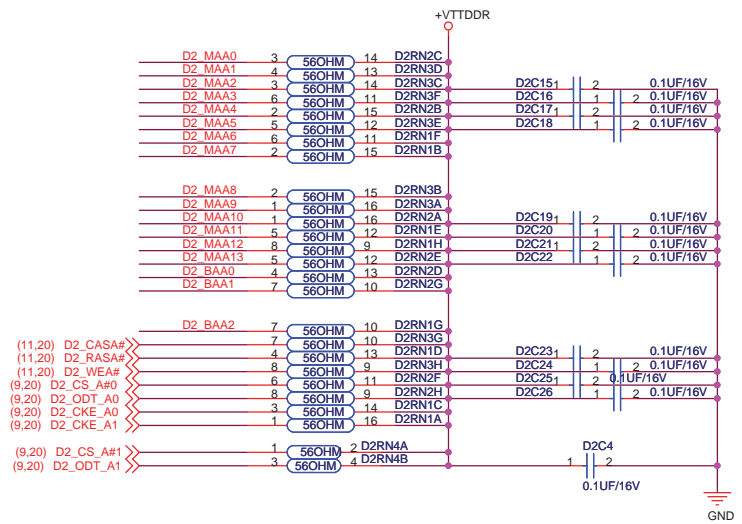
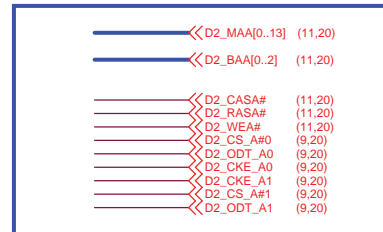


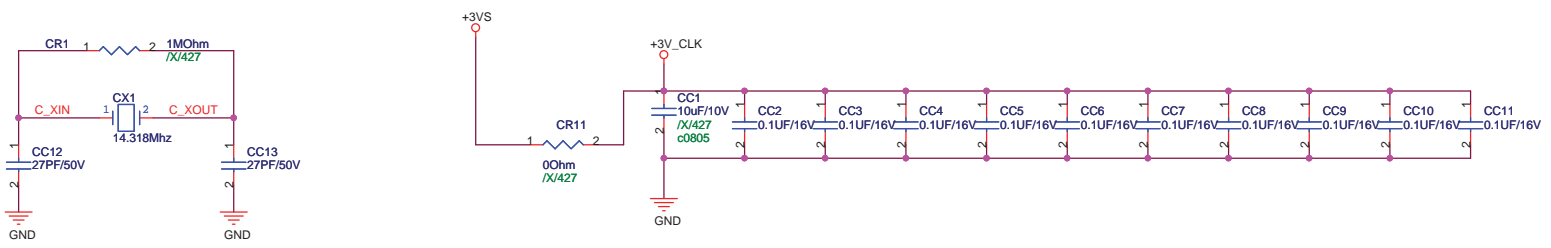
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D2_MAA0	102	A0	DQ0	5	D2_DQ_A0
D2_MAA1	101	A1	DQ1	7	D2_DQ_A1
D2_MAA2	100	A2	DQ2	17	D2_DQ_A2
D2_MAA3	99	A3	DQ3	19	D2_DQ_A3
D2_MAA4	98	A4	DQ4	4	D2_DQ_A4
D2_MAA5	97	A5	DQ5	6	D2_DQ_A5
D2_MAA6	94	A6	DQ6	14	D2_DQ_A6
D2_MAA7	92	A7	DQ7	23	D2_DQ_A7
D2_MAA8	93	A8	DQ8	25	D2_DQ_A16
D2_MAA9	91	A9	DQ9	35	D2_DQ_A17
D2_MAA10	105	A10/AP	DQ10	37	D2_DQ_A18
D2_MAA11	90	A11	DQ11	20	D2_DQ_A19
D2_MAA12	89	A12	DQ12	22	D2_DQ_A20
D2_MAA13	116	A13	DQ13	36	D2_DQ_A21
D2_BAA2	85	A14	DQ14	38	D2_DQ_A22
D2_BAA2	85	A15	DQ15	43	D2_DQ_A23
D2_BAA2	85	A16_BA2	DQ16	45	D2_DQ_A8
D2_BAA0	107	BA0	DQ17	45	D2_DQ_A9
D2_BAA1	106	BA1	DQ18	55	D2_DQ_A10
D2_BAA1	106	BA1	DQ19	57	D2_DQ_A11
D2_CS_A#0	110	S0#	DQ20	44	D2_DQ_A12
D2_CS_A#1	115	S1#	DQ21	46	D2_DQ_A13
D2_CS_A#1	115	S1#	DQ22	56	D2_DQ_A14
D2_CS_A#1	115	S1#	DQ23	58	D2_DQ_A15
D2_CKE_A0	32	CK0	DQ24	61	D2_DQ_A24
D2_CKE_A1	164	CK0#	DQ25	63	D2_DQ_A25
D2_CKE_A1	166	CK1#	DQ26	73	D2_DQ_A26
D2_CAS_A#	80	CKE1	DQ27	75	D2_DQ_A27
D2_CAS_A#	113	CKE1	DQ28	62	D2_DQ_A28
D2_RAS_A#	108	CAS#	DQ29	64	D2_DQ_A29
D2_WEA#	109	RAS#	DQ30	74	D2_DQ_A30
D2_ODT_A0	198	WE#	DQ31	76	D2_DQ_A31
D2_ODT_A1	200	SA0	DQ32	123	D2_DQ_A32
D2_ODT_A1	197	SA1	DQ33	125	D2_DQ_A33
D2_ODT_A1	195	SCL	DQ34	135	D2_DQ_A34
D2_ODT_A1	195	SDA	DQ35	137	D2_DQ_A35
D2_DM_A0	114	DM0	DQ36	124	D2_DQ_A36
D2_DM_A2	119	DM1	DQ37	126	D2_DQ_A37
D2_DM_A1	119	DM1	DQ38	134	D2_DQ_A38
D2_DM_A3	10	DM2	DQ39	136	D2_DQ_A39
D2_DM_A4	26	DM3	DQ40	147	D2_DQ_A40
D2_DM_A5	52	DM4	DQ41	143	D2_DQ_A41
D2_DM_A6	67	DM5	DQ42	151	D2_DQ_A42
D2_DM_A7	130	DM6	DQ43	153	D2_DQ_A43
D2_DM_A7	147	DM7	DQ44	140	D2_DQ_A44
D2_DM_A7	170	DM7	DQ45	142	D2_DQ_A45
D2_DM_A7	185	DM7	DQ46	152	D2_DQ_A46
D2_DM_A7	185	DM7	DQ47	154	D2_DQ_A47
D2_DM_A7	185	DM7	DQ48	157	D2_DQ_A48
D2_DM_A7	185	DM7	DQ49	159	D2_DQ_A49
D2_DM_A7	185	DM7	DQ50	173	D2_DQ_A50
D2_DM_A7	185	DM7	DQ51	175	D2_DQ_A51
D2_DM_A7	185	DM7	DQ52	158	D2_DQ_A52
D2_DM_A7	185	DM7	DQ53	160	D2_DQ_A53
D2_DM_A7	185	DM7	DQ54	174	D2_DQ_A54
D2_DM_A7	185	DM7	DQ55	176	D2_DQ_A55
D2_DM_A7	185	DM7	DQ56	179	D2_DQ_A56
D2_DM_A7	185	DM7	DQ57	181	D2_DQ_A57
D2_DM_A7	185	DM7	DQ58	189	D2_DQ_A58
D2_DM_A7	185	DM7	DQ59	181	D2_DQ_A59
D2_DM_A7	185	DM7	DQ60	180	D2_DQ_A60
D2_DM_A7	185	DM7	DQ61	182	D2_DQ_A61
D2_DM_A7	185	DM7	DQ62	192	D2_DQ_A62
D2_DM_A7	185	DM7	DQ63	194	D2_DQ_A63

DDR2_DIMM_200P
12G02503200J



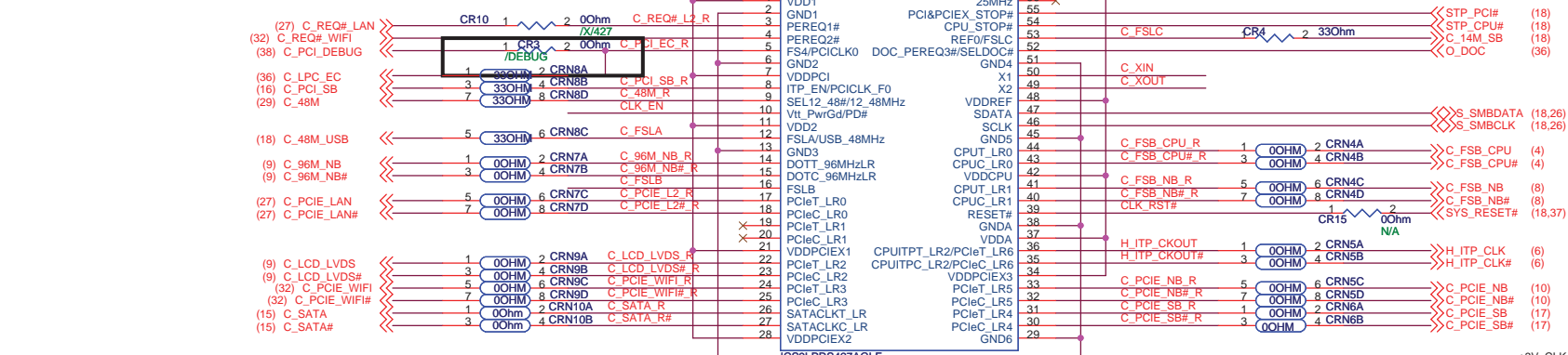
ASUS Title : SO-DIMM
 ASUSTek Computer Inc. Engineer: Henry_Yang
 Size A3 Project Name P703 Rev 1.2G
 Date: Tuesday, December 09, 2008 Sheet 20 of 51



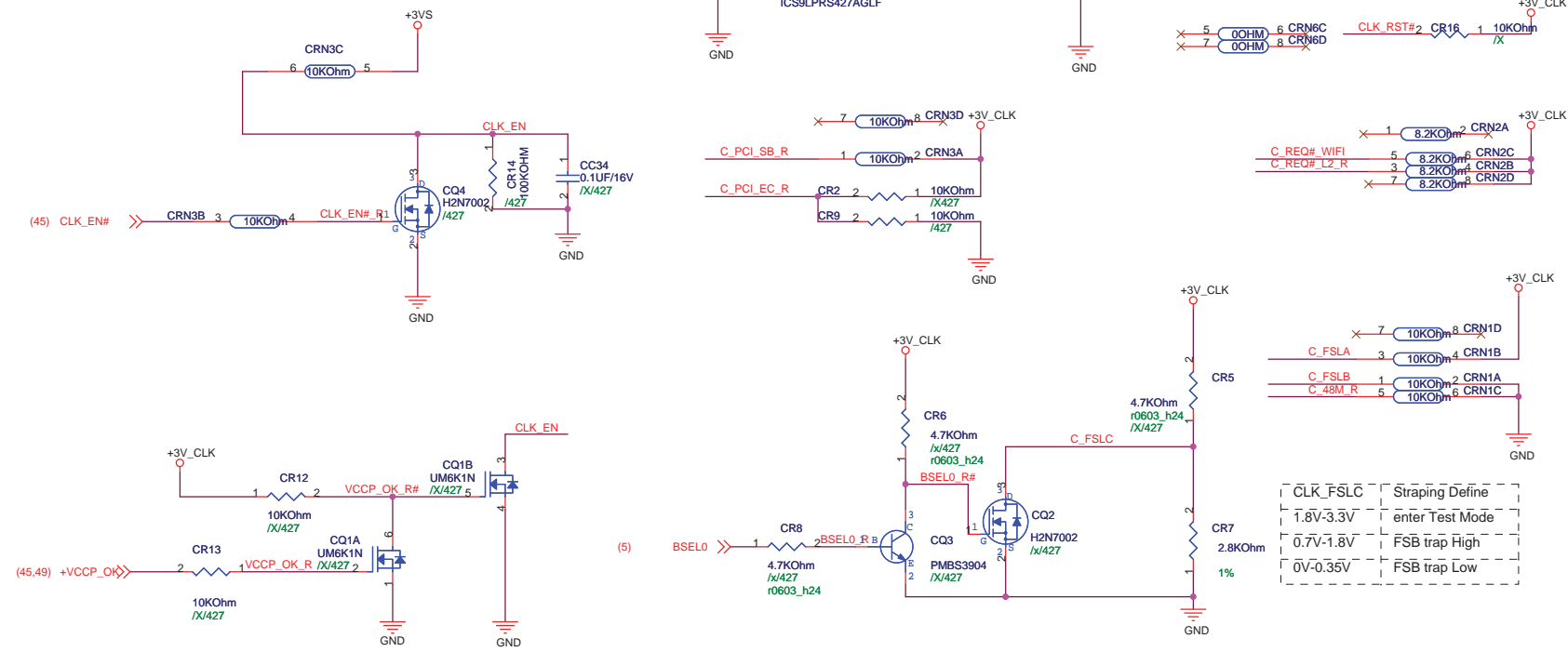


STP_PCI#	(18)	C_REQ#_LAN	(27)
STP_CPU#	(18)	C_REQ#_WIFI	(32)
C_14M_SB	(18)	C_PCI_DEBUG	(38)
S_SMBDATA	(18,26)	C_LPC_EC	(38)
S_SMBCLK	(18,26)	C_PCI_SB	(16)
C_FSB_CPU	(4)	C_48M	(29)
C_FSB_CPU#	(4)	C_48M_USB	(18)
C_FSB_NB	(8)	C_96M_NB	(9)
C_FSB_NB#	(8)	C_96M_NB#	(9)
H_ITP_CLK#	(6)	C_LCD_LVDS	(9)
H_ITP_CLK#	(6)	C_LCD_LVDS#	(9)
C_PCIE_WIFI	(32)	C_PCIE_NB#	(10)
C_PCIE_WIFI#	(32)	C_PCIE_NB	(10)
		C_PCIE_SB	(17)
		C_PCIE_SB#	(17)
		C_PCIE_LAN	(27)
		C_PCIE_LAN#	(27)

N/A for Debug,pR will /X

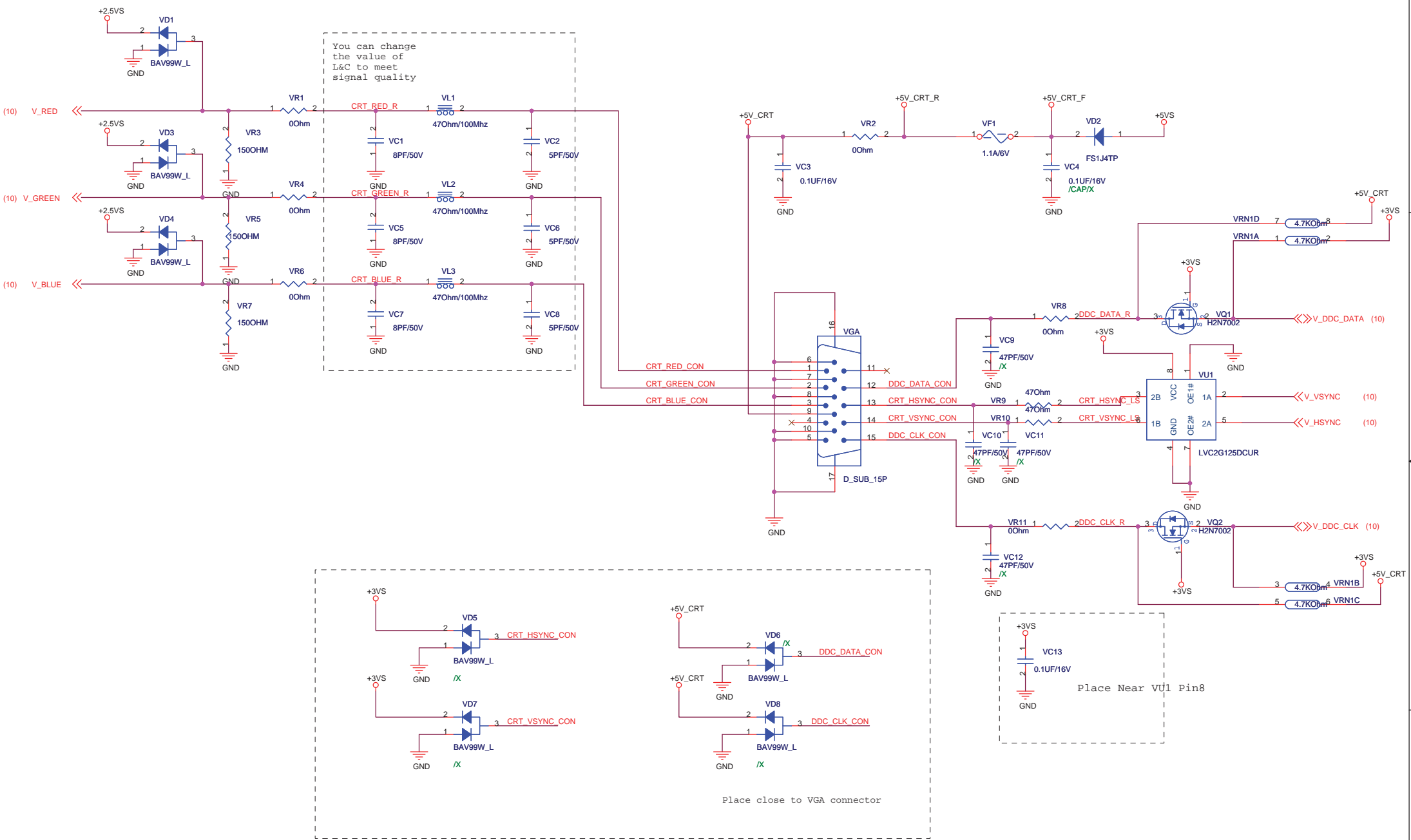


C_FSB_CPU	CC16	2	1	10PF/50V
C_FSB_CPU#	CC17	2	1	10PF/50V
C_FSB_NB	CC18	2	1	10PF/50V
C_FSB_NB#	CC19	2	1	10PF/50V
H_ITP_CLK	CC20	2	1	10PF/50V
H_ITP_CLK#	CC21	2	1	10PF/50V
C_PCIE_NB	CC22	2	1	10PF/50V
C_PCIE_NB#	CC23	2	1	10PF/50V
C_PCIE_SB	CC24	1	2	5PF/50V
C_PCIE_SB#	CC25	1	2	5PF/50V
C_PCIE_WIFI	CC26	1	2	5PF/50V
C_PCIE_WIFI#	CC27	1	2	5PF/50V
C_PCIE_LAN	CC28	1	2	5PF/50V
C_PCIE_LAN#	CC29	1	2	5PF/50V
C_96M_NB	CC30	2	1	10PF/50V
C_96M_NB#	CC31	2	1	10PF/50V
C_LCD_LVDS	CC32	2	1	10PF/50V
C_LCD_LVDS#	CC33	2	1	10PF/50V
C_PCI_SB	CC36	2	1	10PF/50V
C_LPC_EC	CC37	2	1	10PF/50V
C_PCI_DEBUG	CC38	2	1	10PF/50V
C_14M_SB	CC39	2	1	10PF/50V
C_48M_USB	CC40	2	1	10PF/50V
C_48M	CC35	2	1	10PF/50V

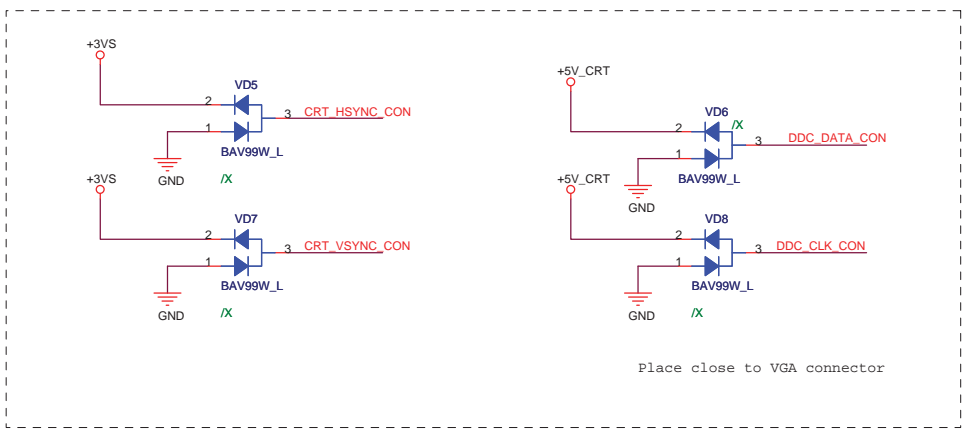


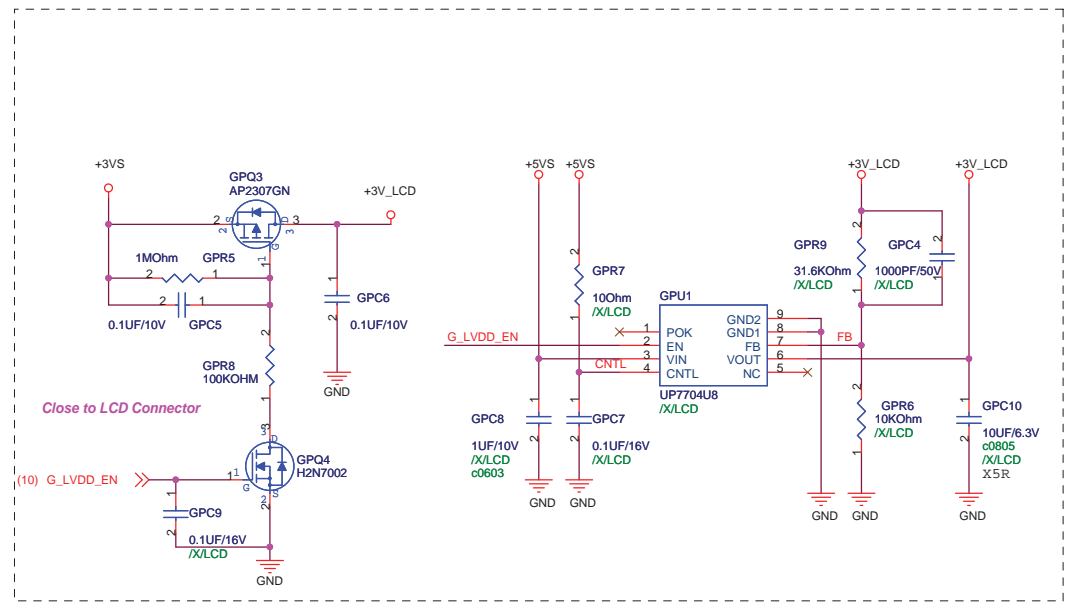
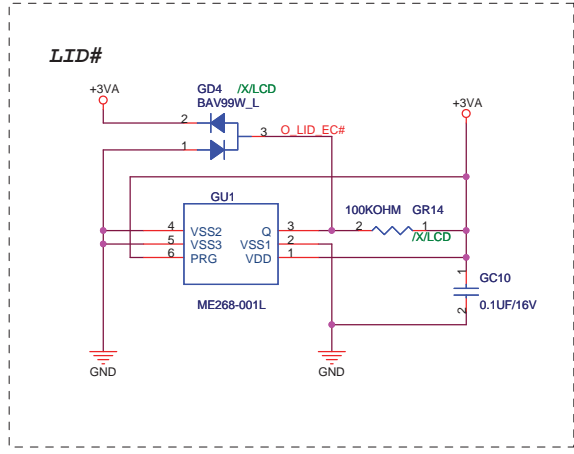
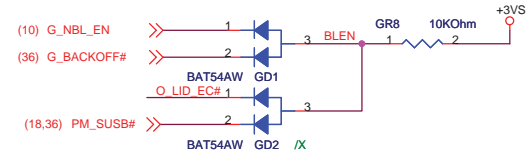
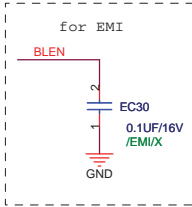
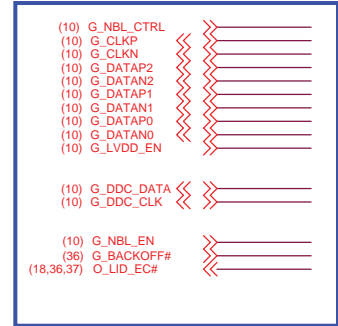
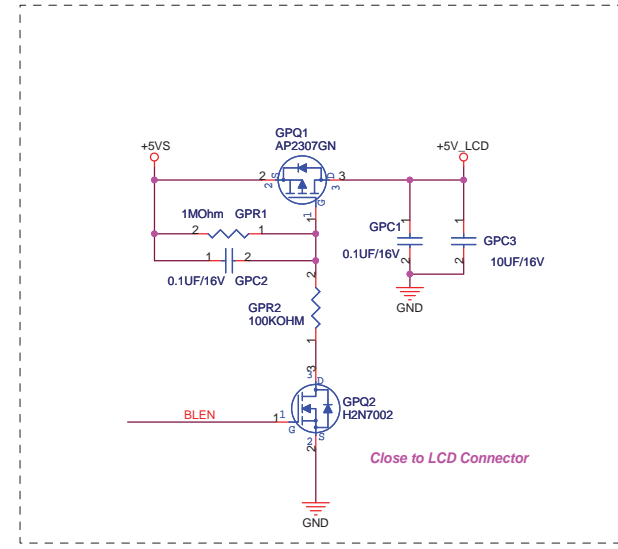
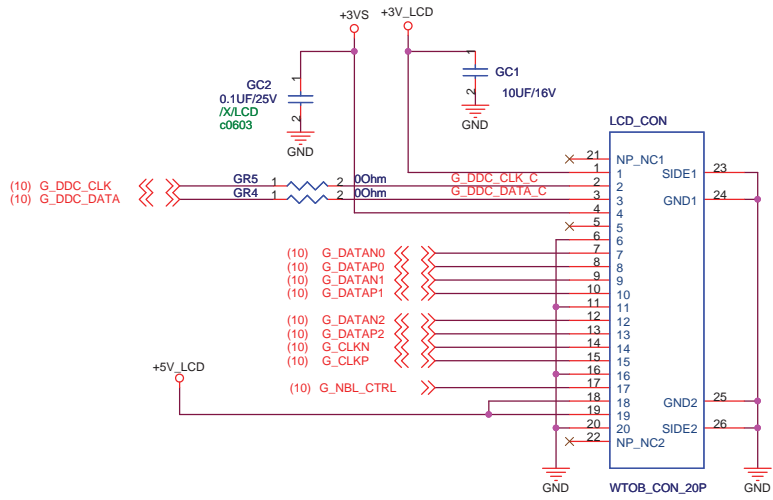
FSLC	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
1	0	1	100

CLK_FSLC	Strapping Define
1.8V-3.3V	enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low




You can change the value of L&C to meet signal quality

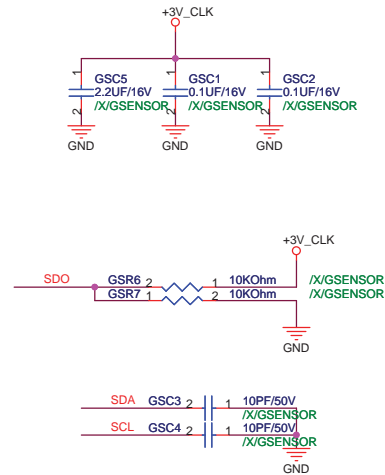
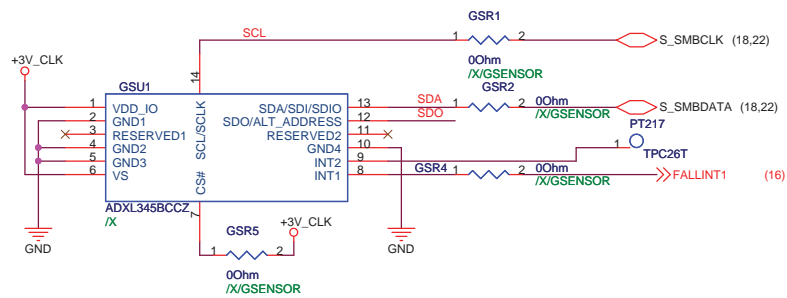
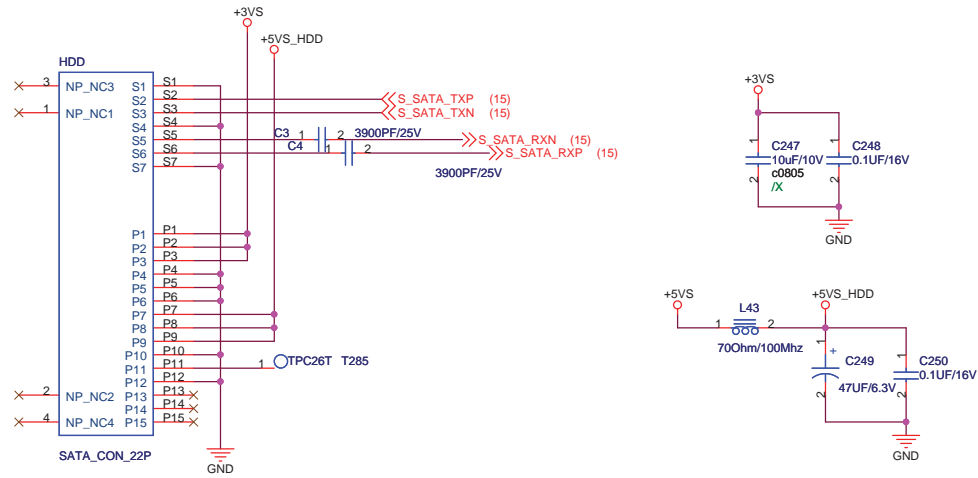


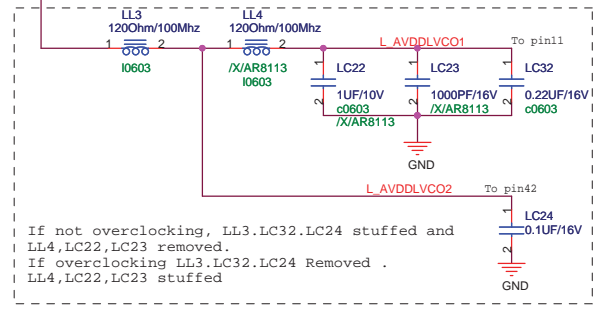
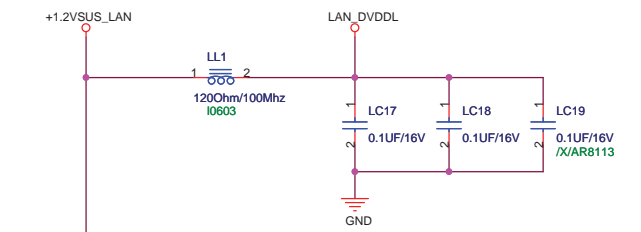
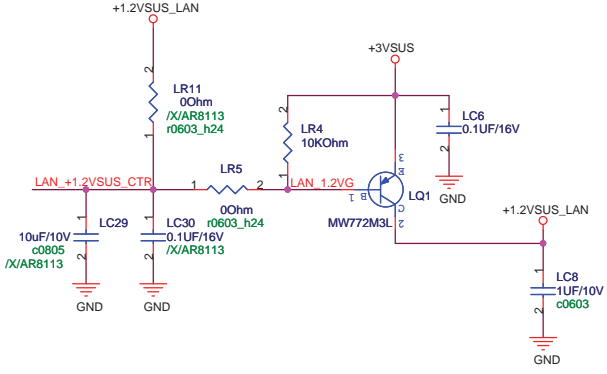
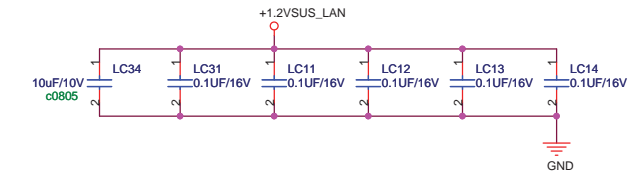
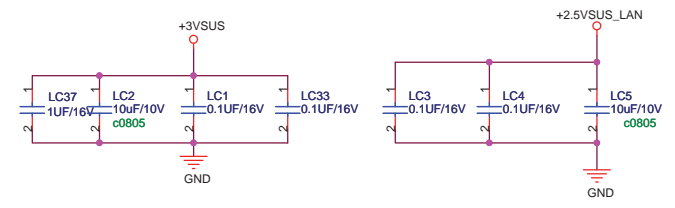




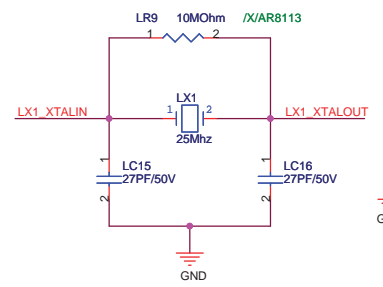
		Title : onboard flash	
ASUSTek Computer Inc.		Engineer: <i>SUSAN_SHI</i>	
Size A3	Project Name Standard Circuit	Date: Tuesday, December 09, 2008	Rev 0.1B
Date: Tuesday, December 09, 2008		Sheet 25 of 51	

SATA HDD Connector

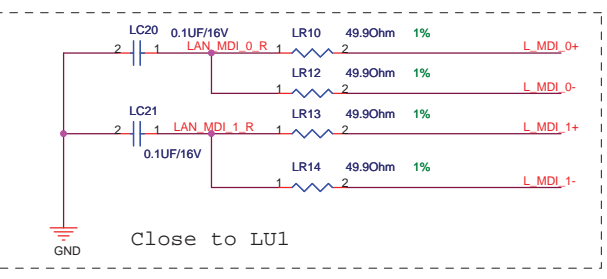
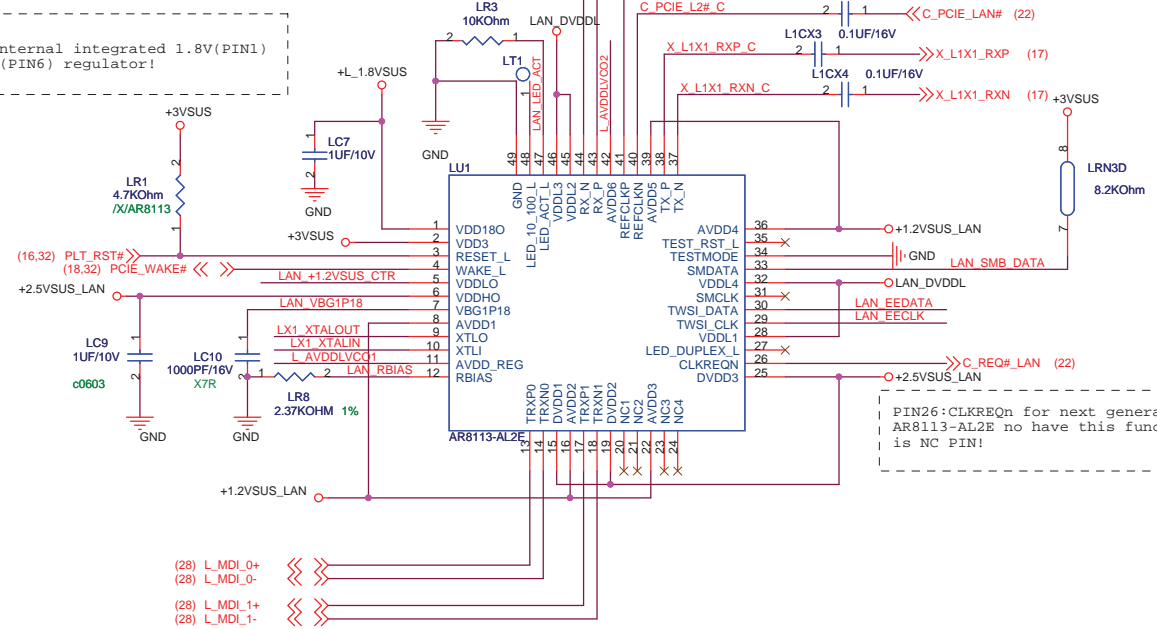




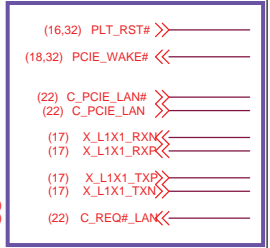
If not overclocking, LL3,LC32,LC24 stuffed and LL4,LC22,LC23 removed.
 IF overclocking LL3,LC32,LC24 Removed .
 LL4,LC22,LC23 stuffed



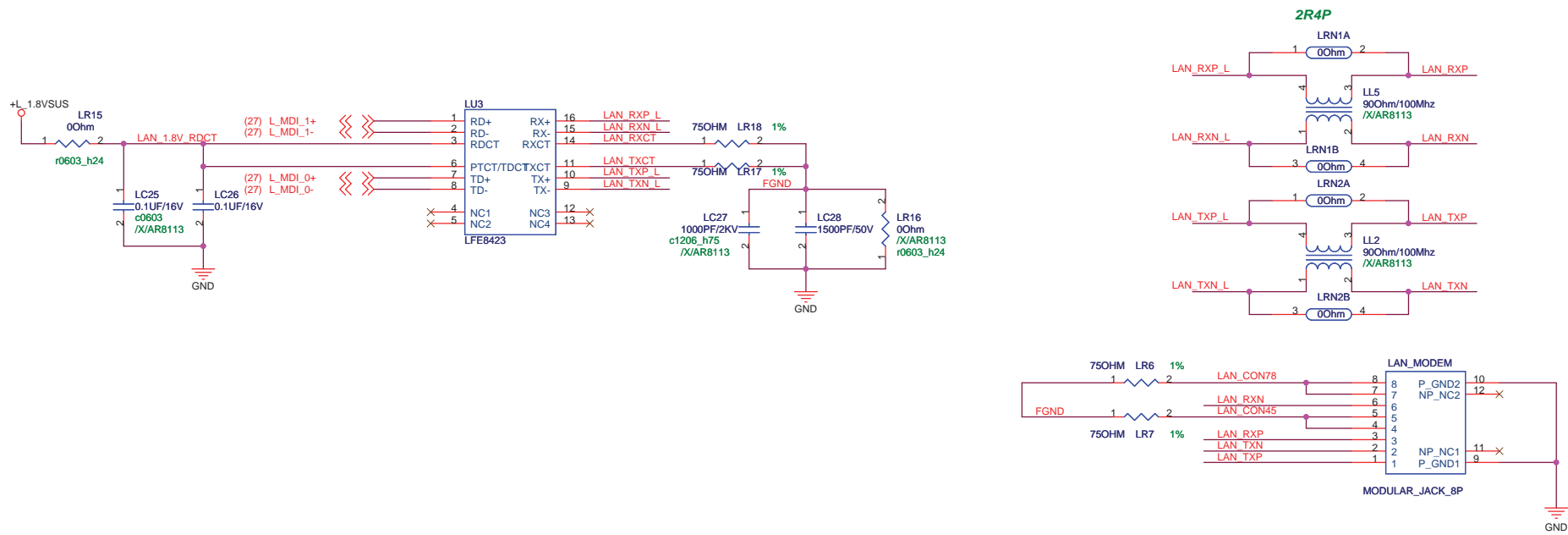
AR8113 internal integrated 1.8V(PIN1) and 2.5V(PIN6) regulator!

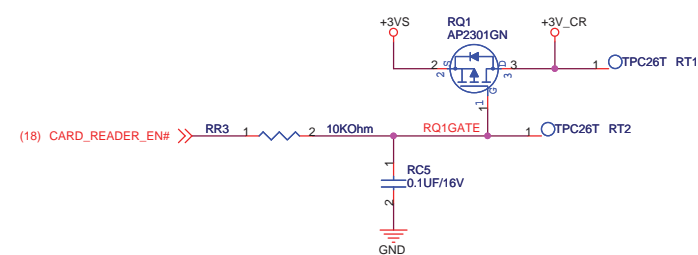
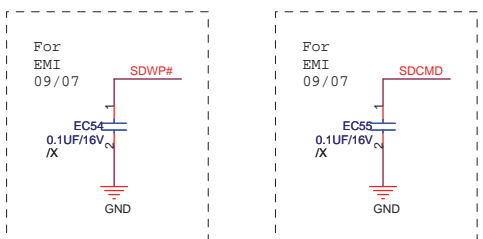
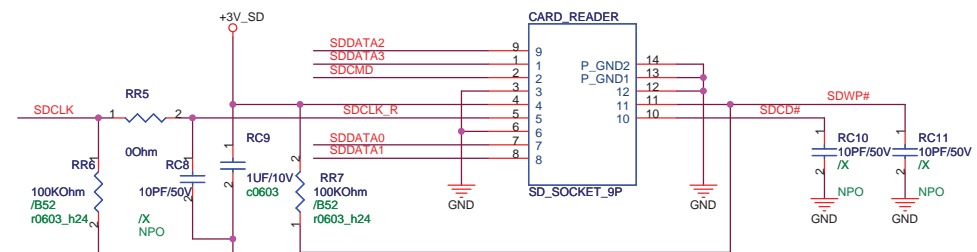
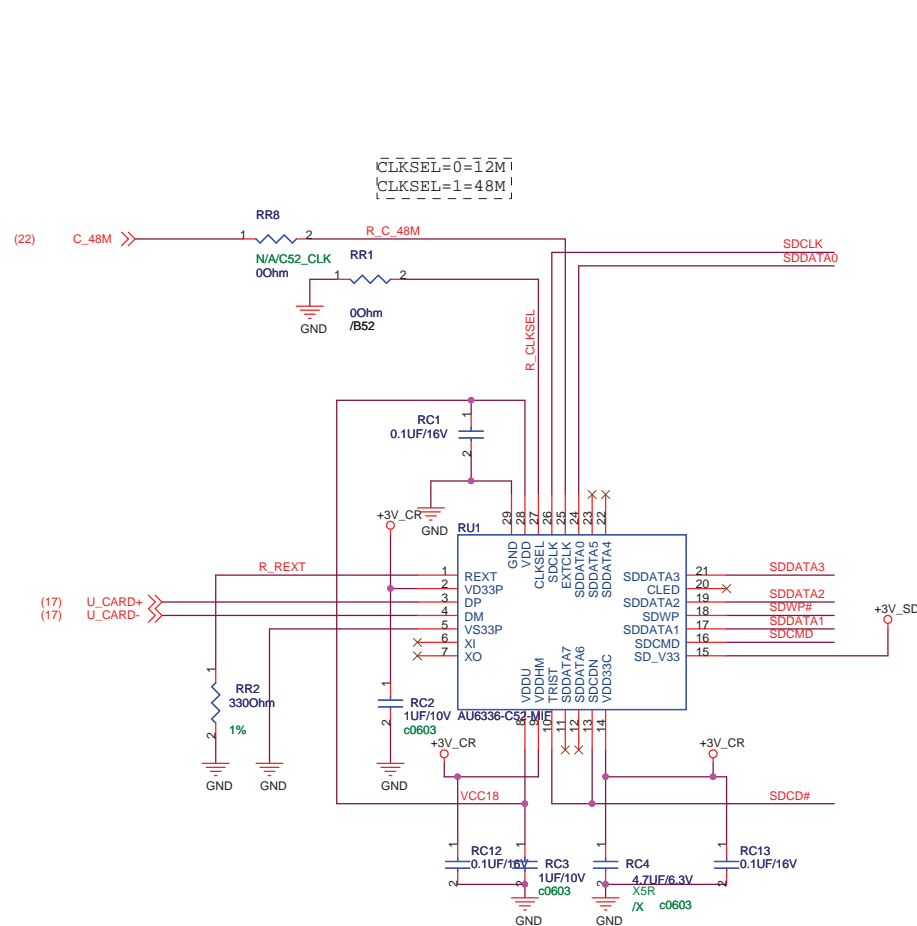


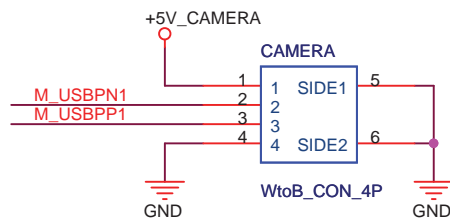
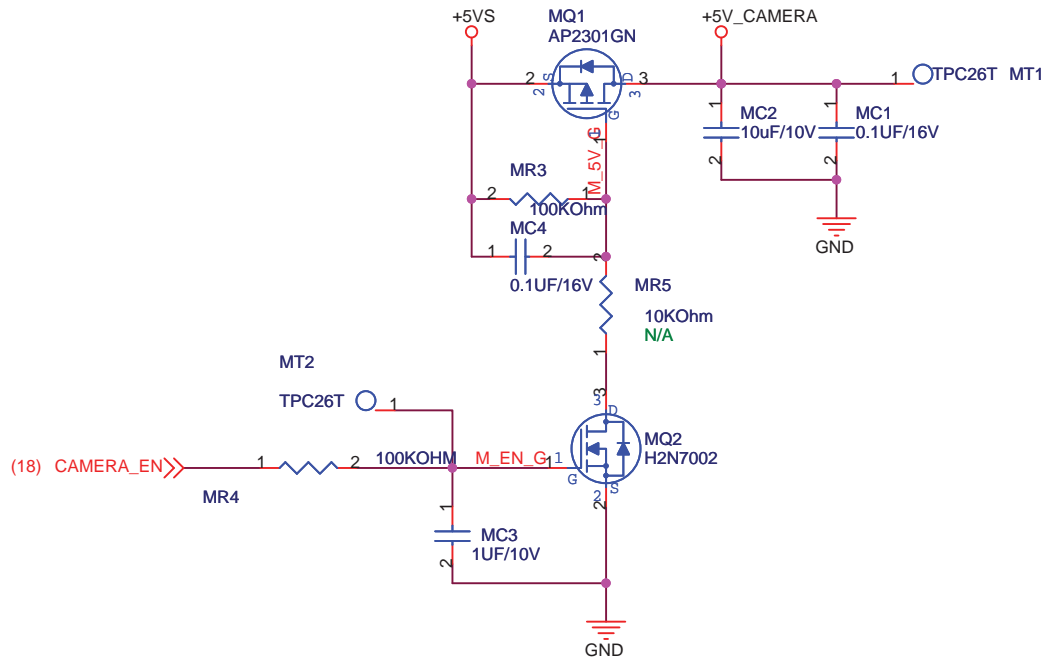
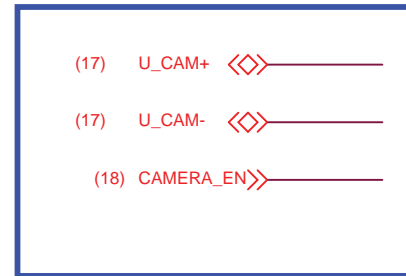
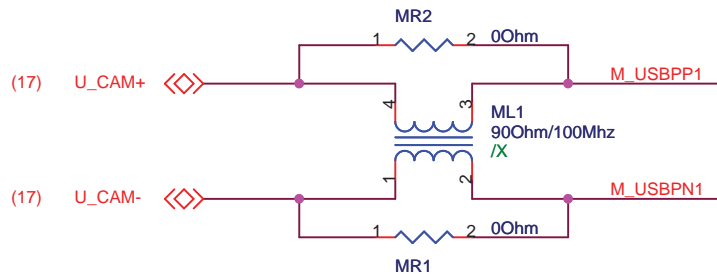
Close to LU1



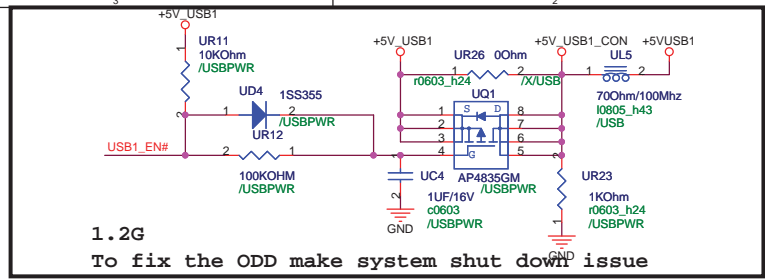
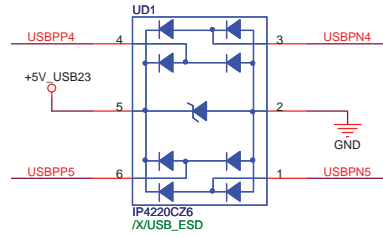
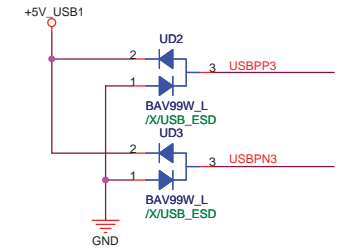
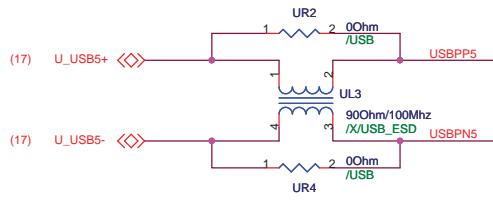
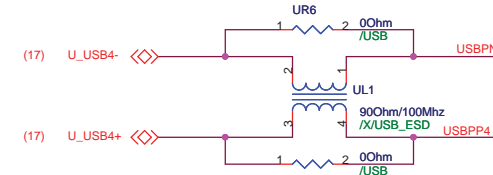
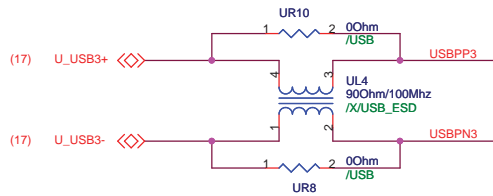
PIN26:CLKREQn for next generation. AR8113-AL2E no have this function . is NC PIN!





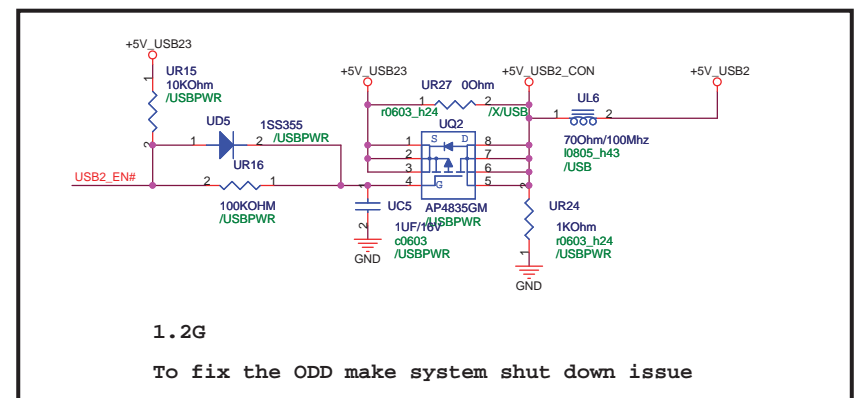
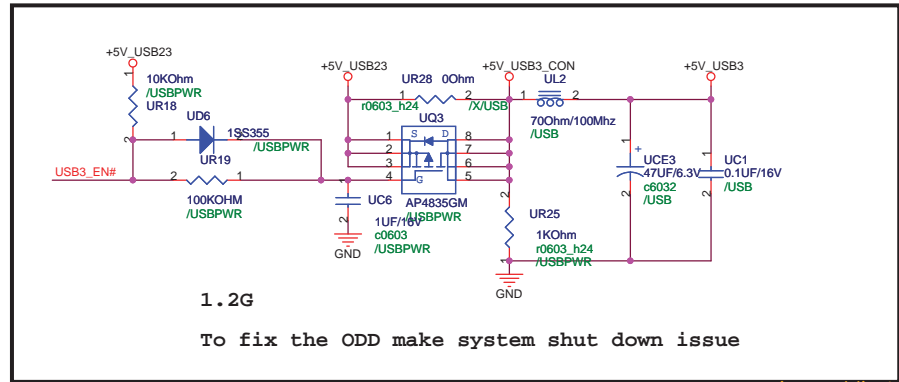
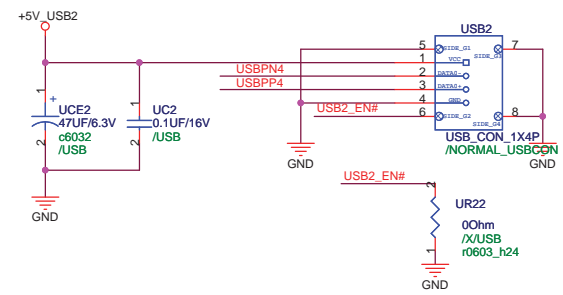
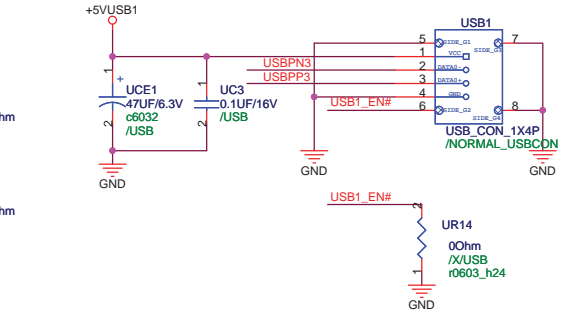
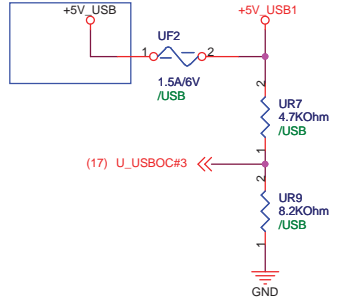
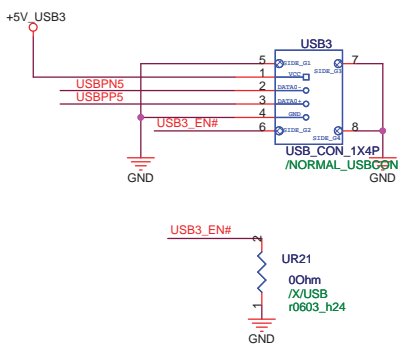
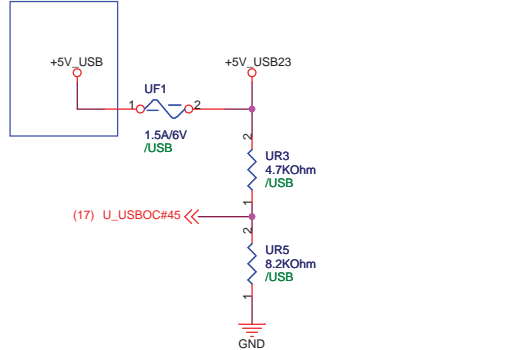


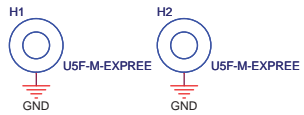
		Title : Camera CONN	
ASUSTek Computer Inc.		Engineer: <i>Henry_Yang</i>	
Size A4	Project Name P703		Rev 1.2G
Date: Tuesday, December 09, 2008		Sheet	30 of 51



- (17) U_USB3+ <<>>
- (17) U_USB3- <<>>
- (17) U_USB4- <<>>
- (17) U_USB4+ <<>>
- (17) U_USB5+ <<>>
- (17) U_USB5- <<>>
- (17) U_USBOC#45 <<>>

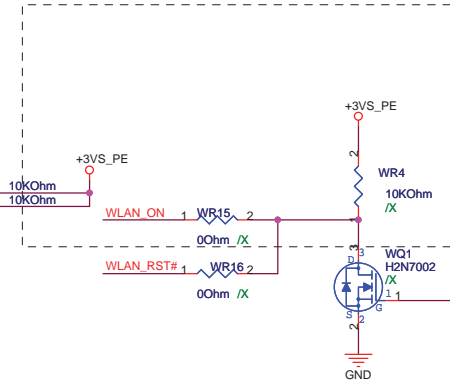
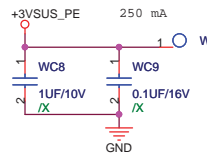
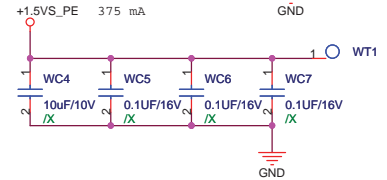
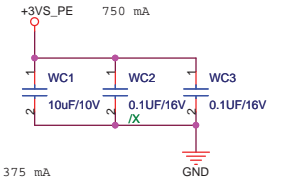
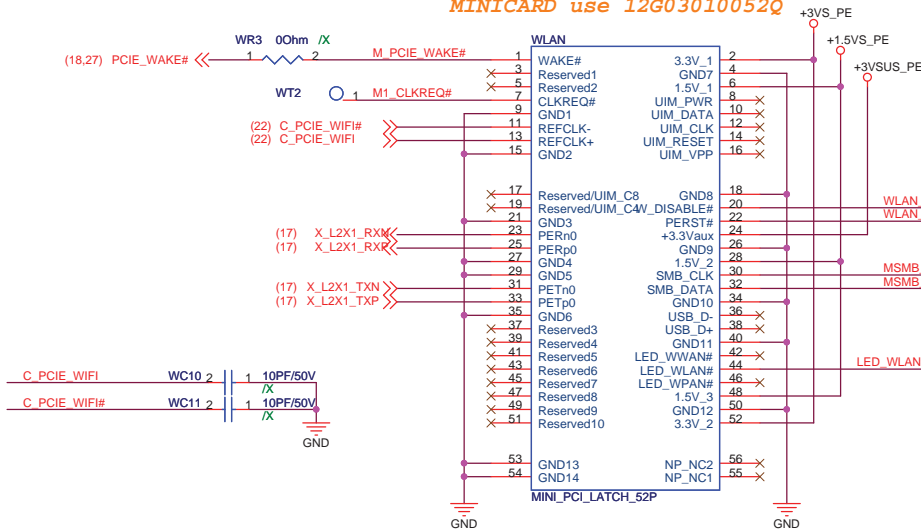
+5VSUS change to
+5V_USB
900HA 1.1G
12/05



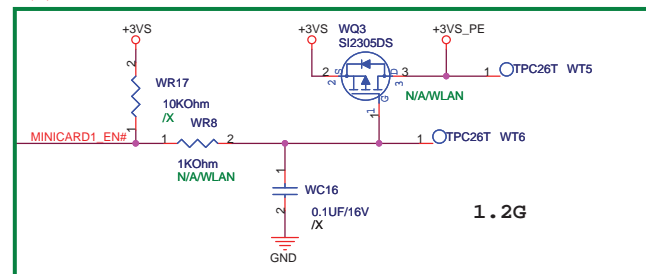
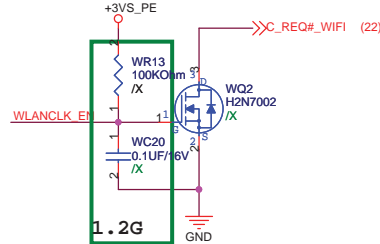
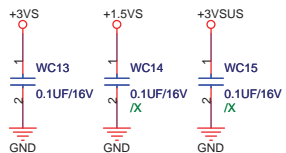
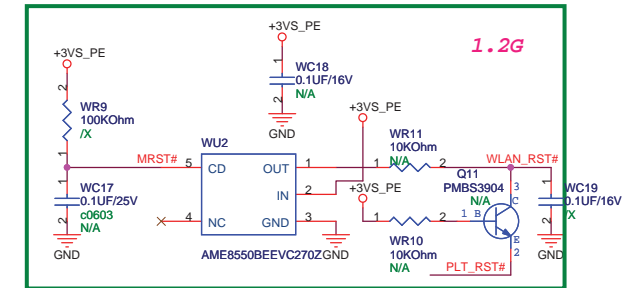
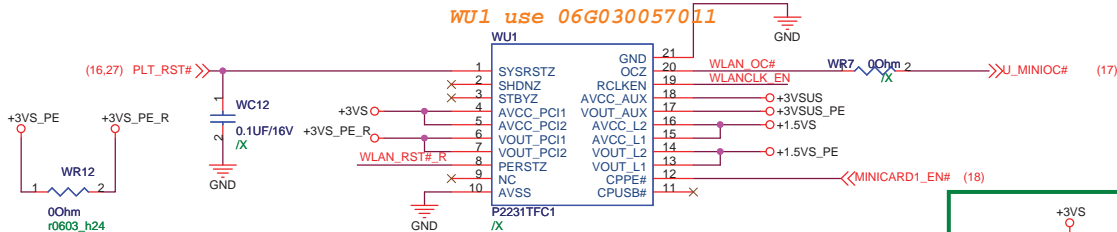


MINI CARD NUT(1.6mm) *2

MINICARD use 12G03010052Q



WU1 use 06G030057011

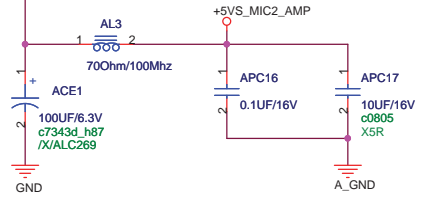
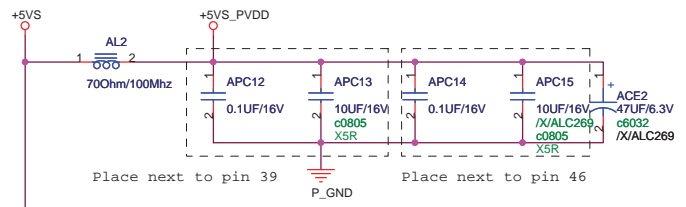
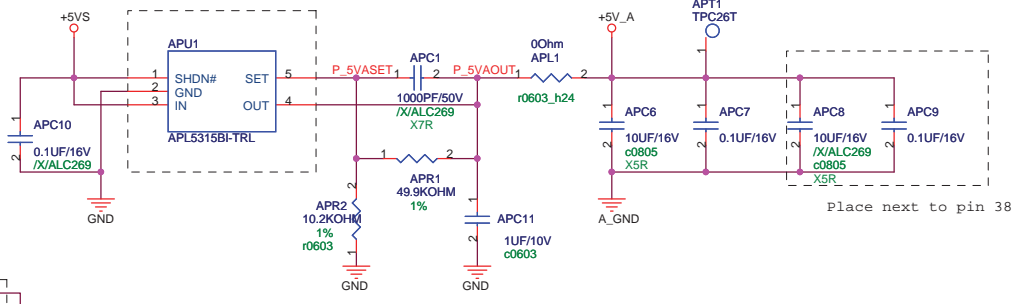
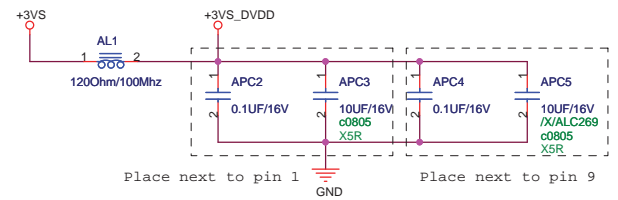


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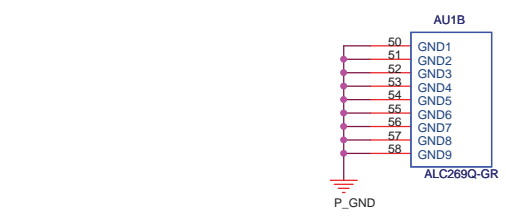
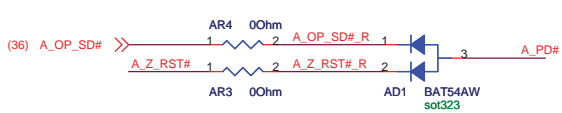
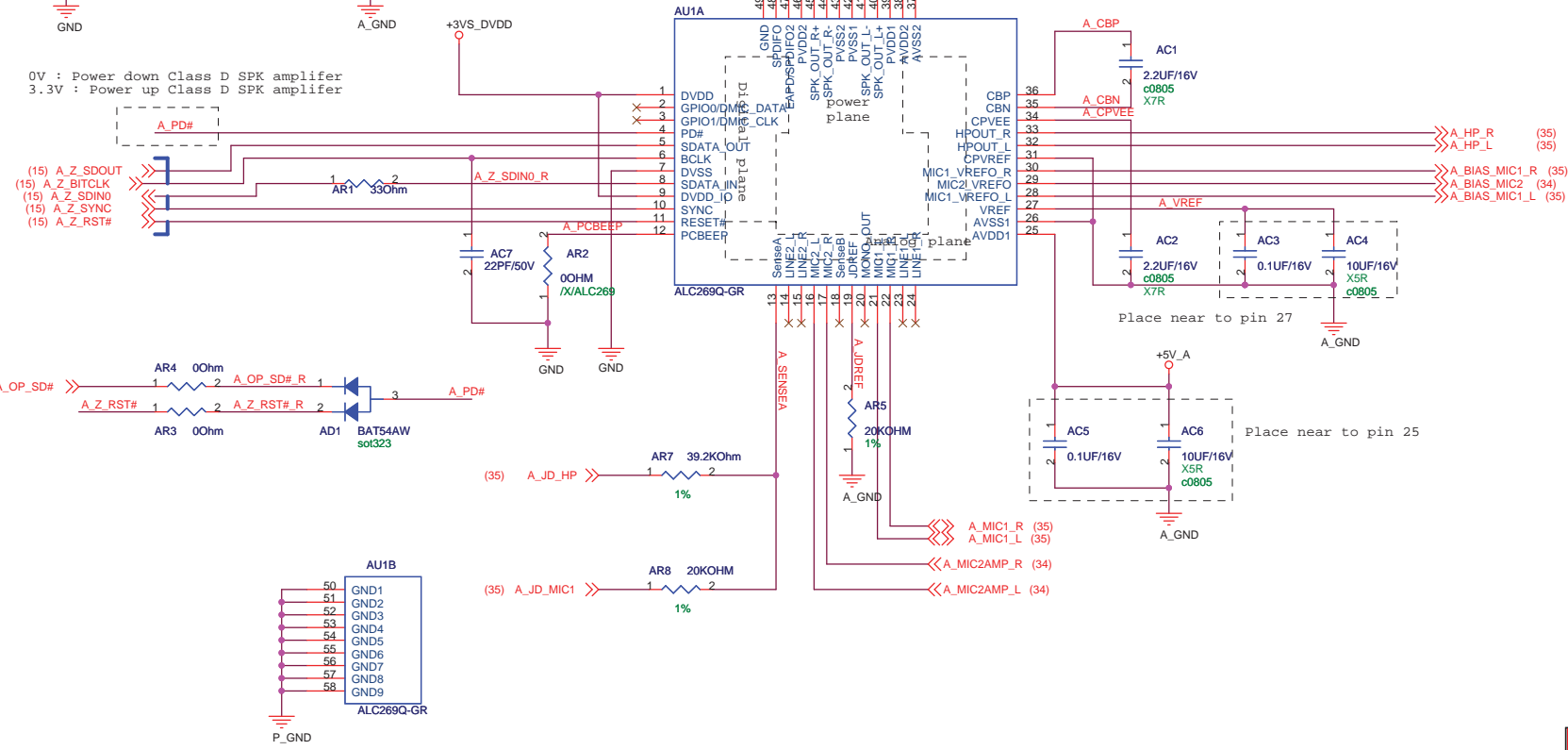
ASUS		Title : WLAN	
ASUSTek Computer INC.		Engineer: Henry_Yang	
Size	Project Name	Rev	
A3	P703	1.2G	
Date: Tuesday, December 09, 2008	Sheet	32	of 51

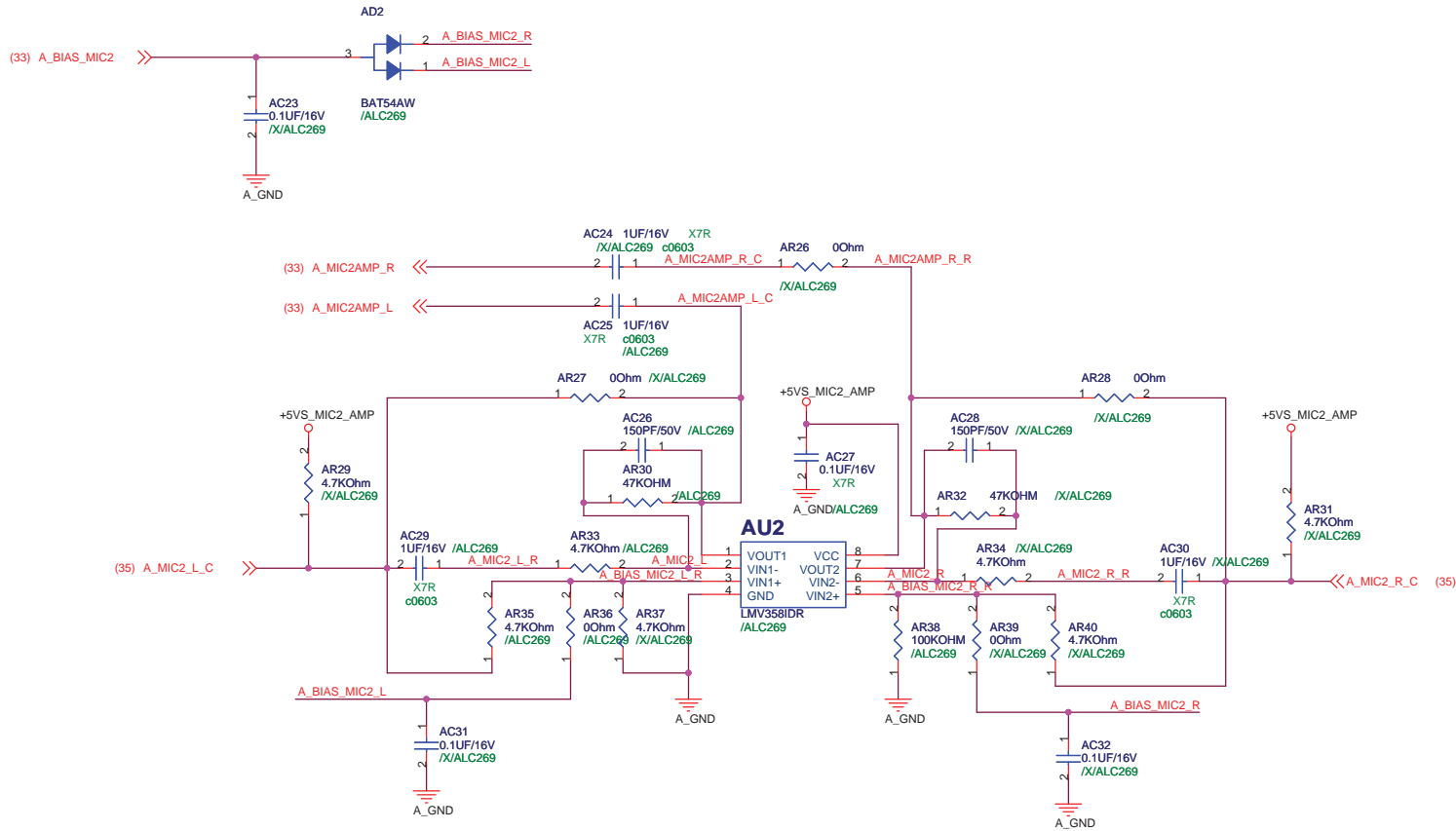
$$V_{out} = 0.8 * (1 + (49.9K / 10.2K))$$

- ⌋ A_Z_SDOUT (15)
- ⌋ A_Z_BITCLK (15)
- ⌋ A_Z_SDI0 (15)
- ⌋ A_Z_SYNC (15)
- ⌋ A_Z_RST# (15)
- ⌋ A_OP_SD# (36)



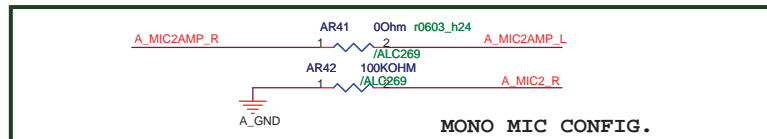
0V : Power down Class D SPK amplifier
 3.3V : Power up Class D SPK amplifier



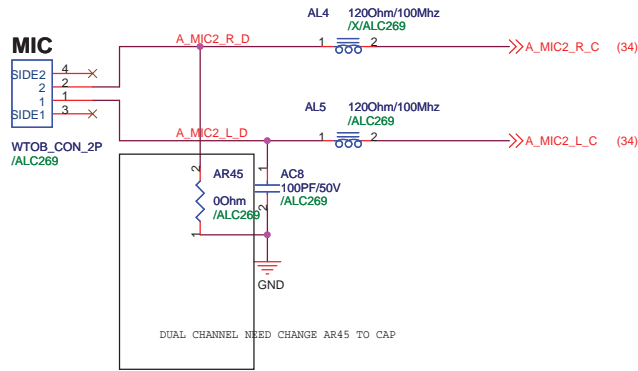


Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz



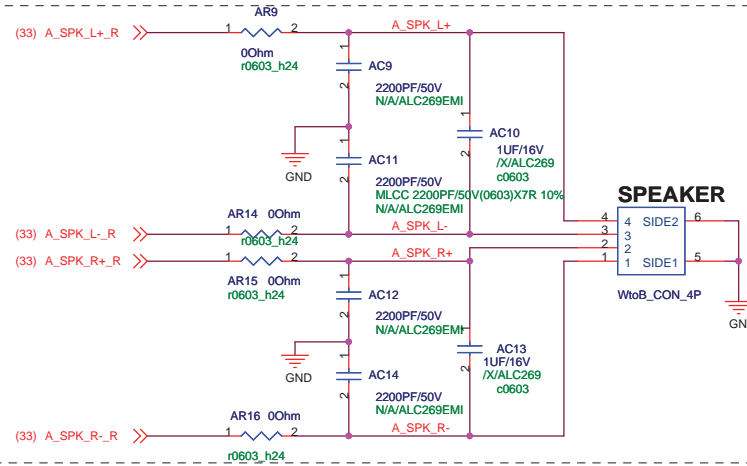
Internal MIC



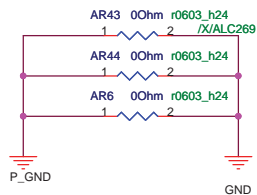
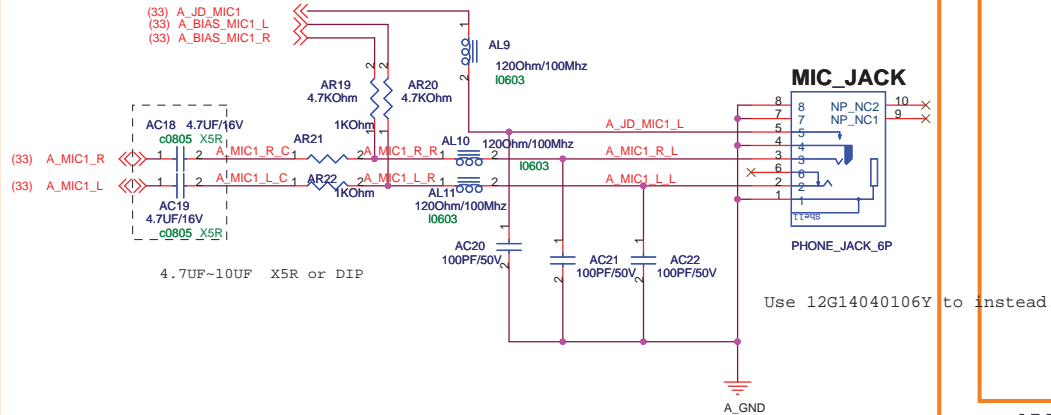
SPEAKER

<<Attention>>
 you can use LC filter(AR9,AR14,AR15,AR16 mount 8.2uH L ;and mount AC10,AC13) to eliminate the EMI(please don't use general beads,because they may influence the THD+N quality) ; AC9/AC11/AC12/AC14 are reserved for EMI fine-tune ; For EMI issue, All L and C should near to codec

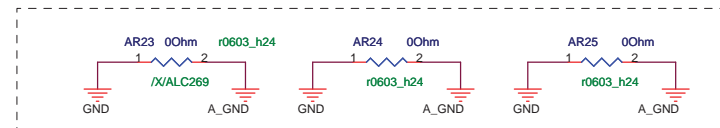
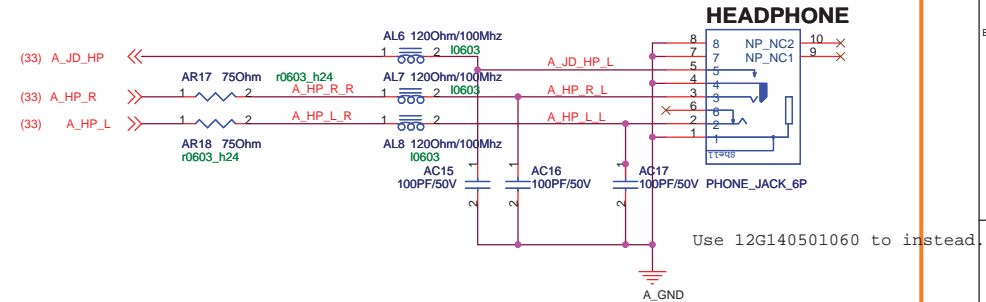
Demodulation Filter Placement near Audio Codec



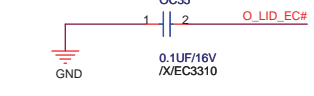
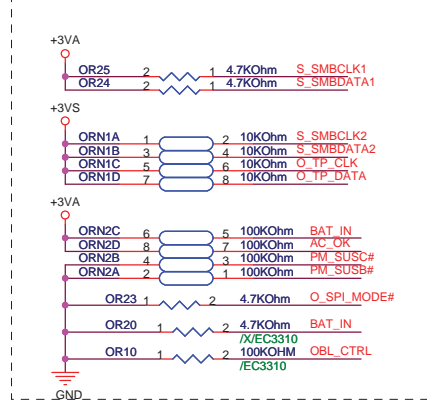
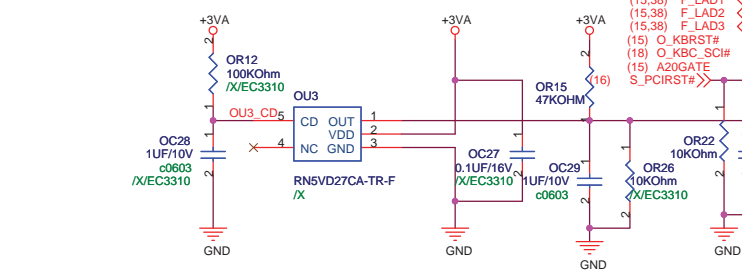
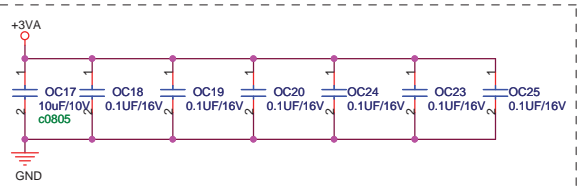
MIC JACK



HEADPHONE

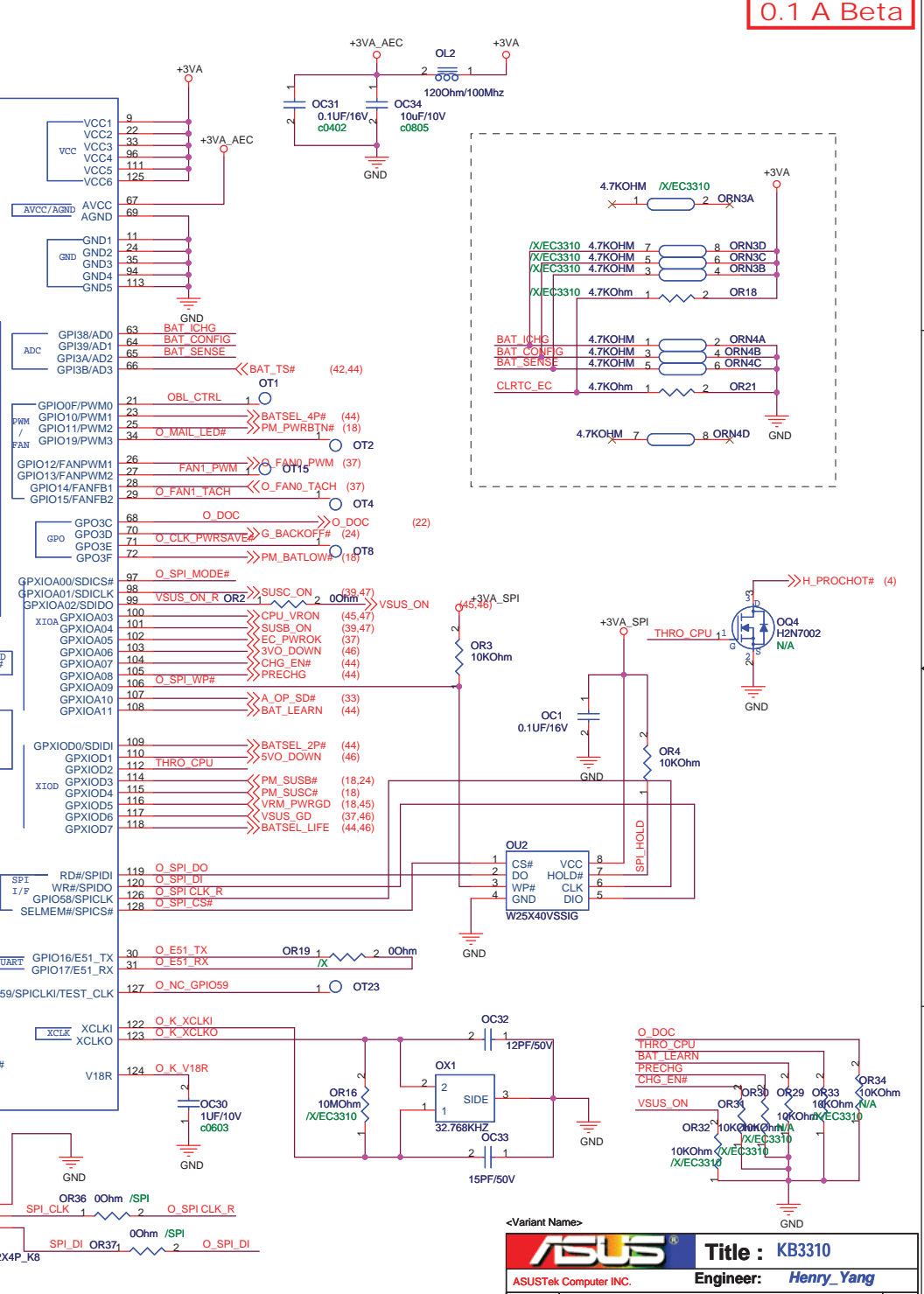
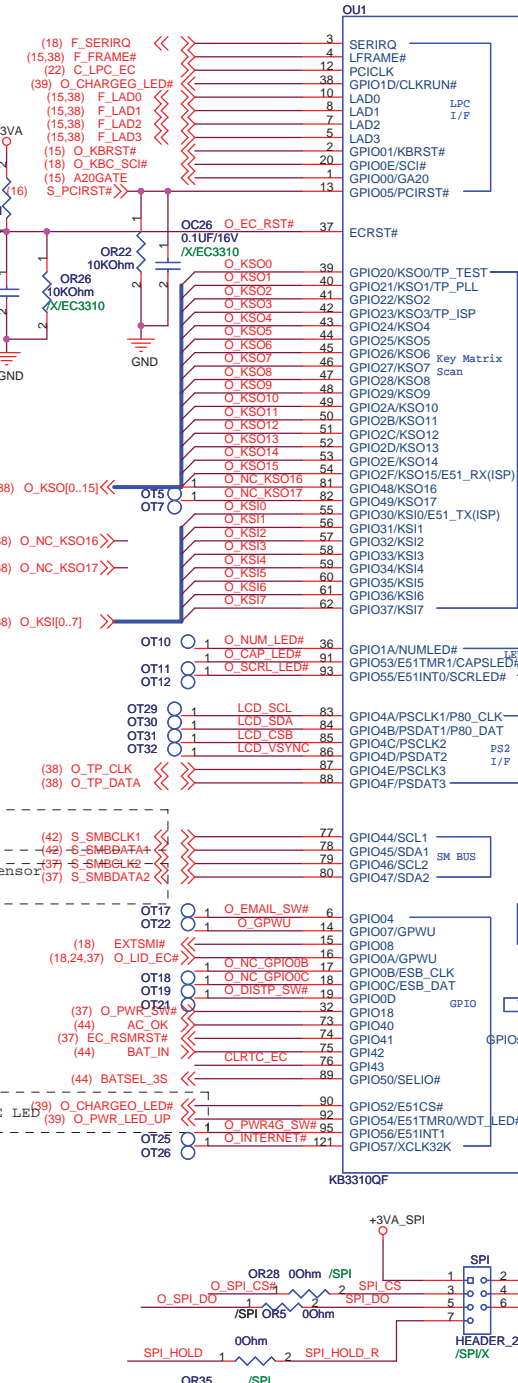
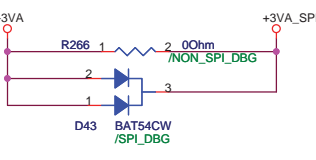


AR24, AR25 can use 0.1UF 11G233310432320 for EMI

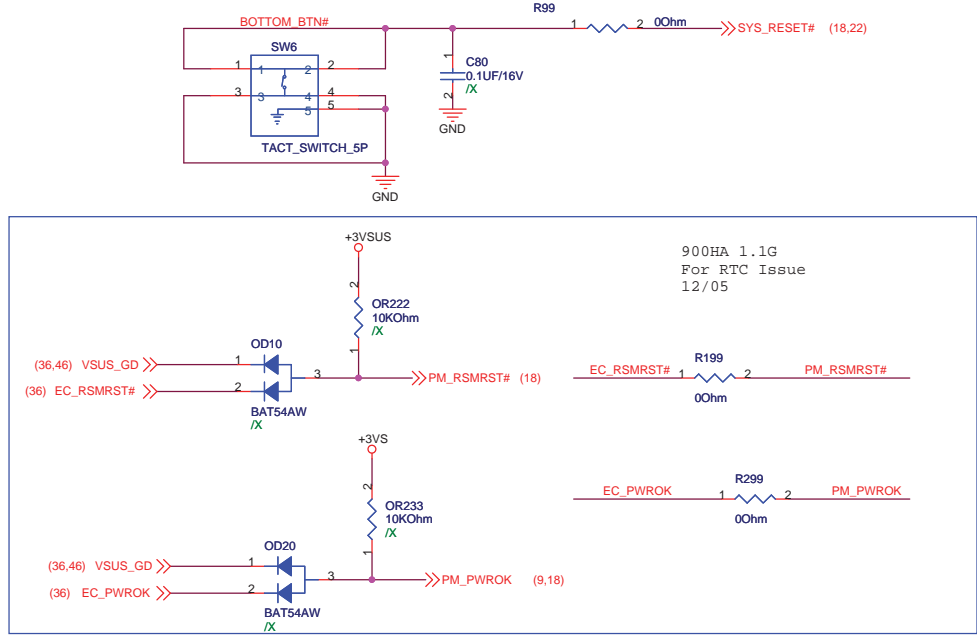
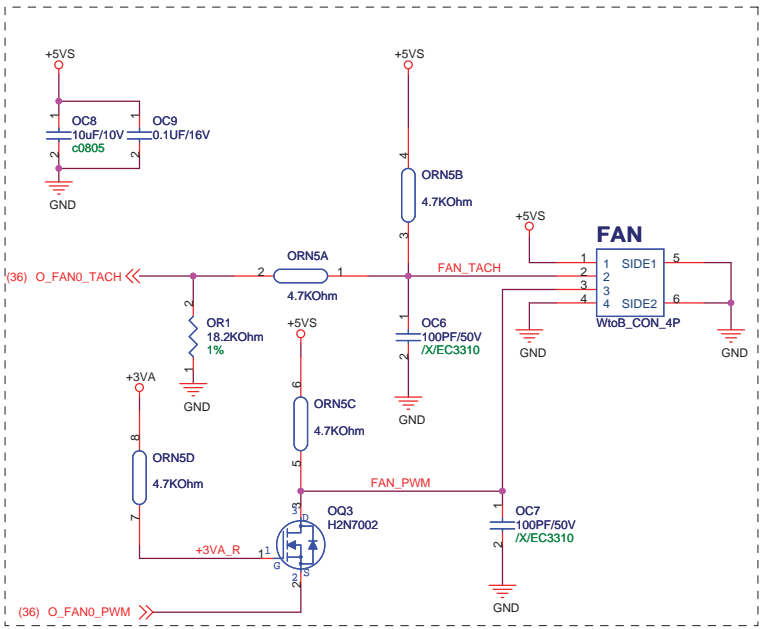
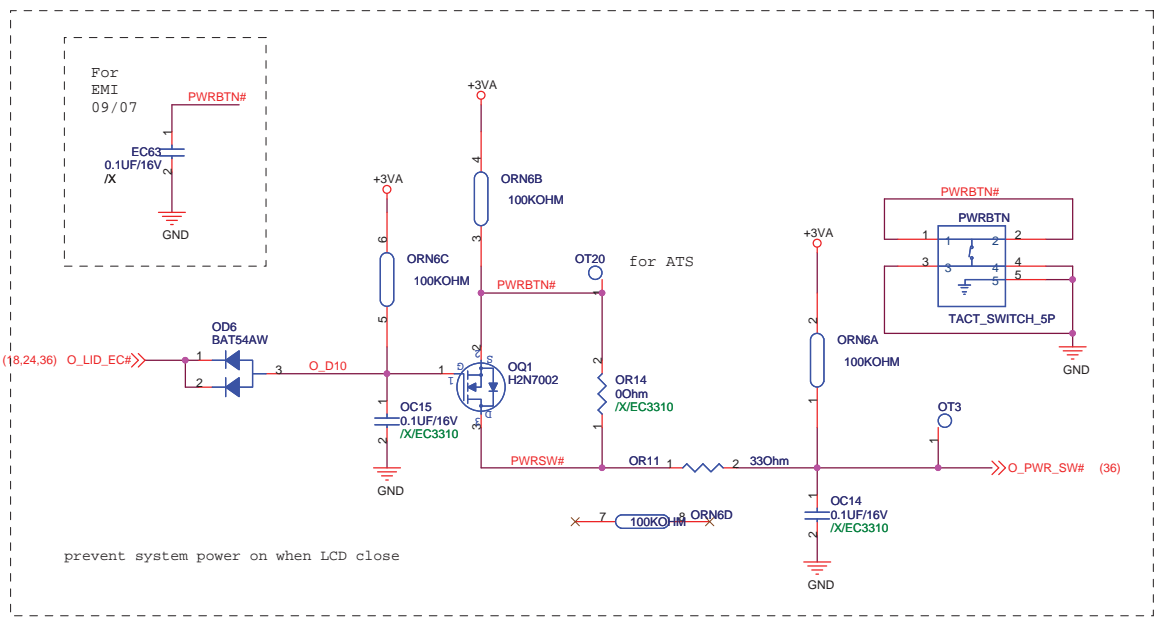
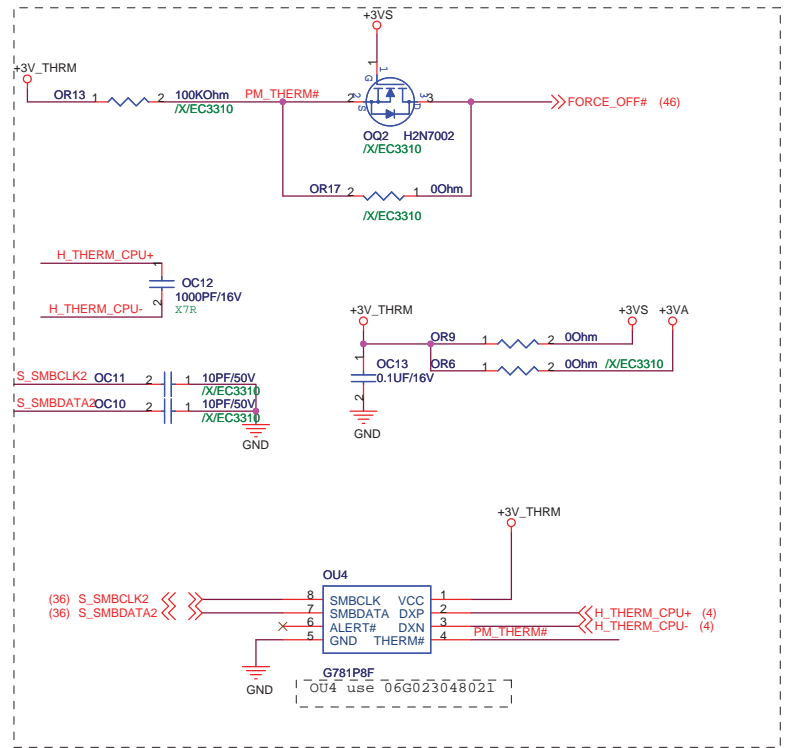


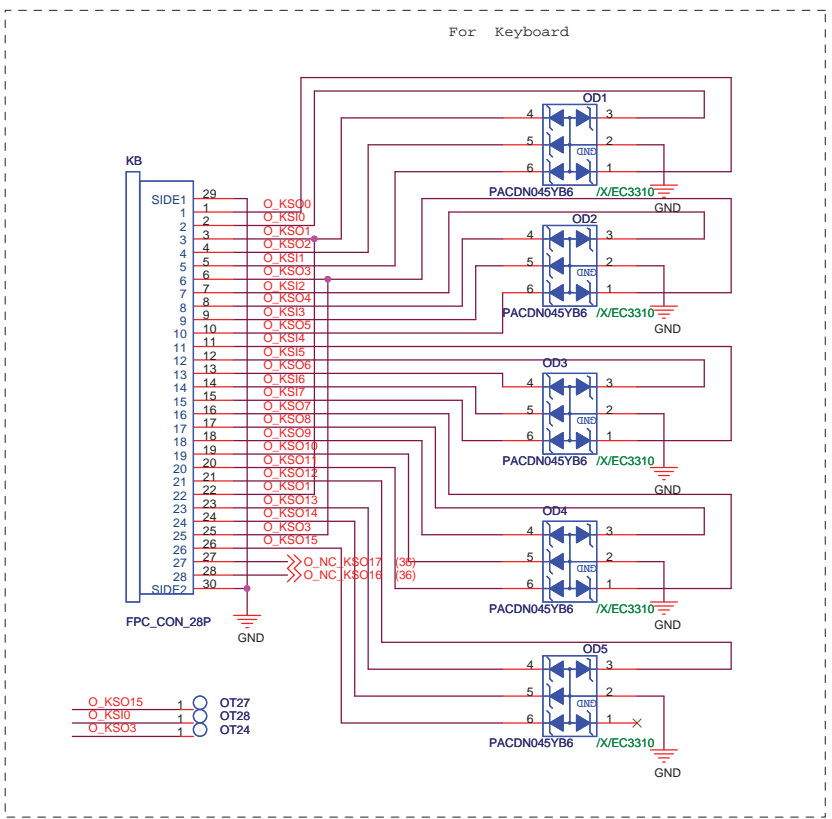
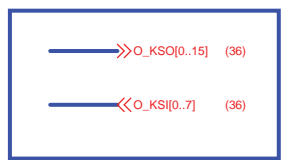
FOR BAT
Thermal sensor

FOR POWER & CHARGE LED

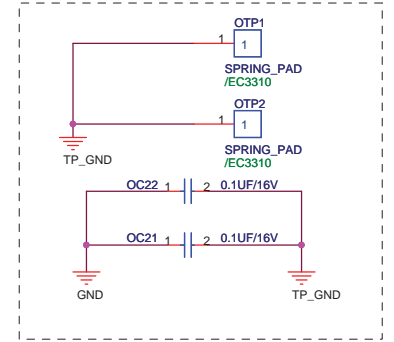
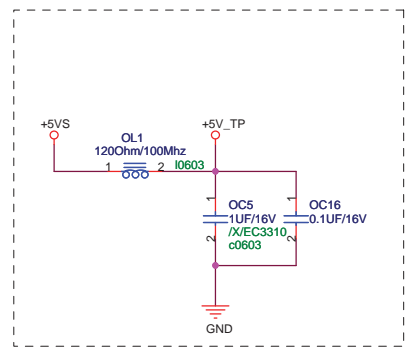
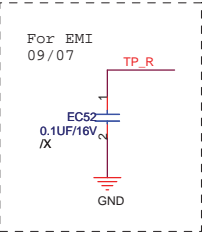
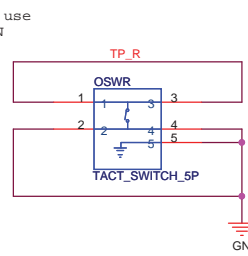
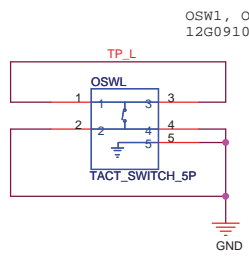
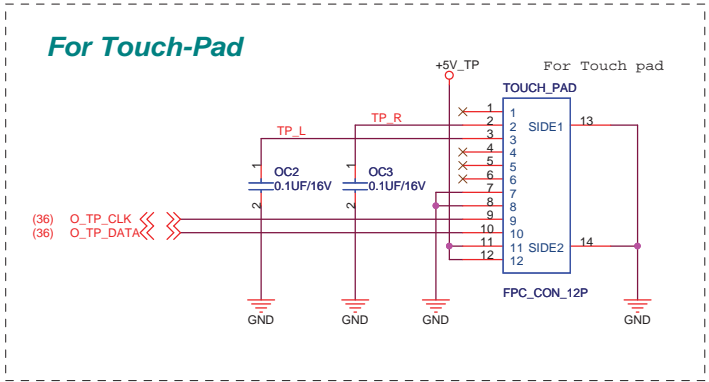
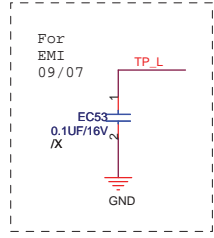
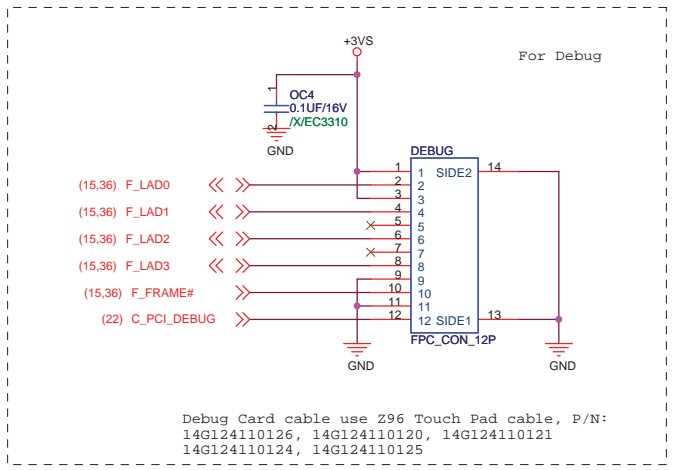
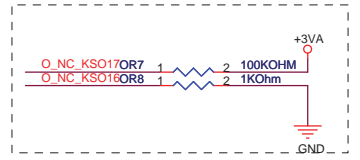


ASUS Title: KB3310
 ASUSTek Computer INC. Engineer: Henry_Yang
 Size Project Name
 A3 P703
 Date: Tuesday, December 09, 2008 Sheet 36 of 51
 Rev 1.2G





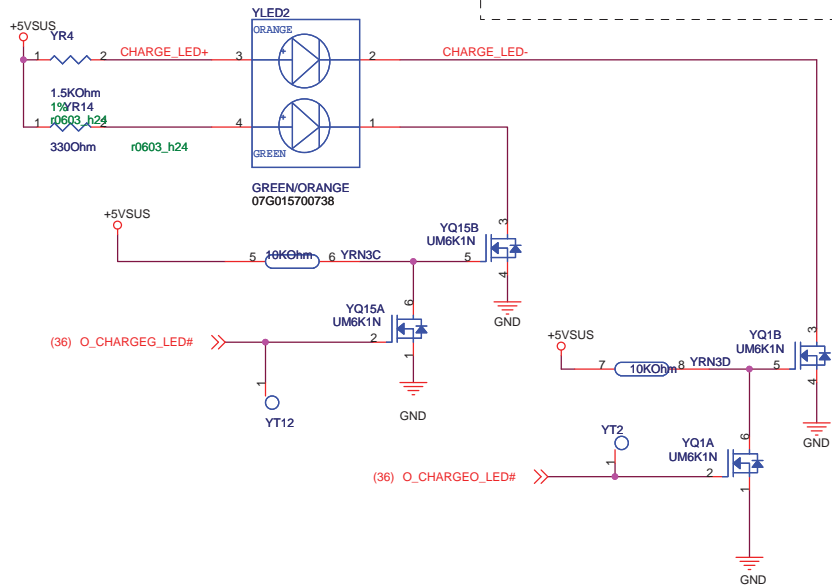
- O_KSO15 1 OT27
- O_KSI0 1 OT28
- O_KSO3 1 OT24



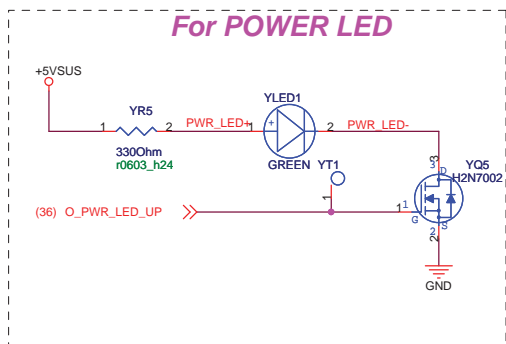
<Variant Name>

ASUS		Title : KB&TP	
ASUSTek Computer INC.		Engineer: Henry_Yang	
Size A3	Project Name P703	Rev 1.2G	
Date: Tuesday, December 09, 2008	Sheet 38	of 51	

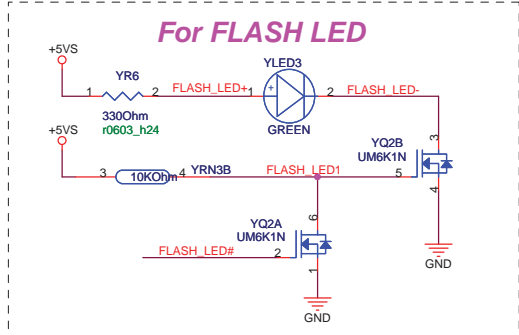
For CHARGE LED



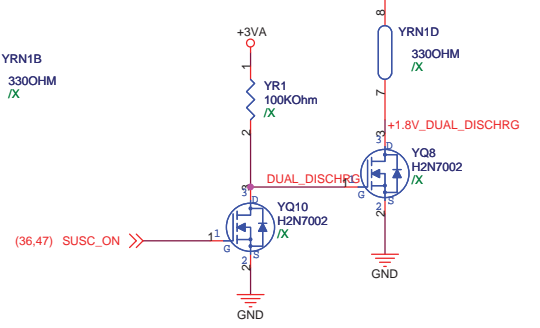
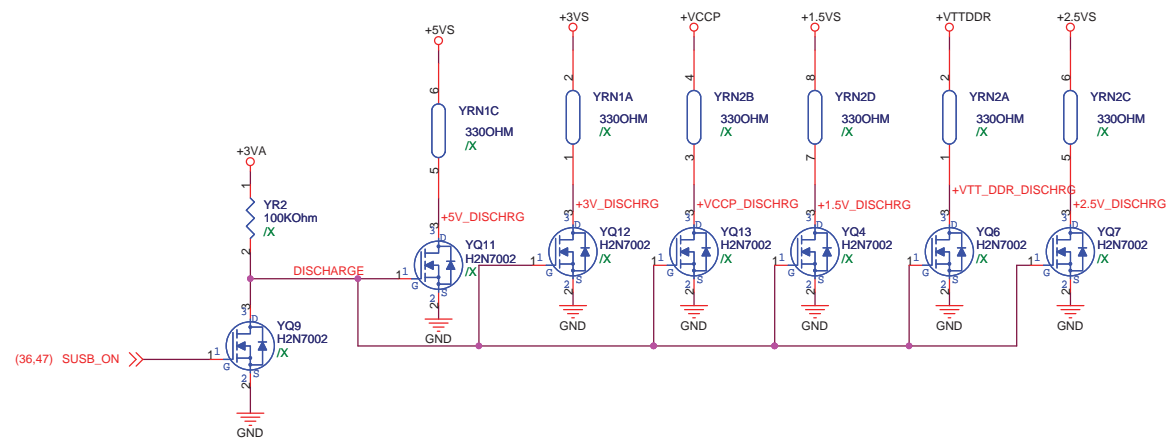
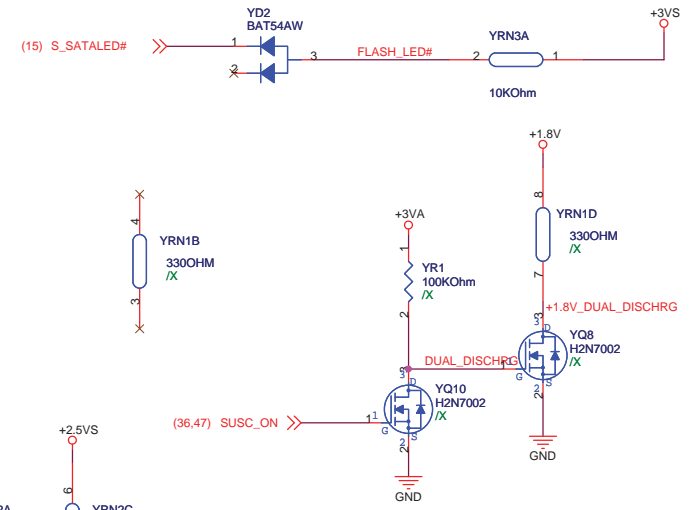
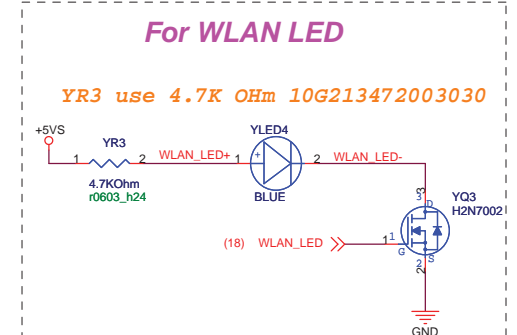
For POWER LED



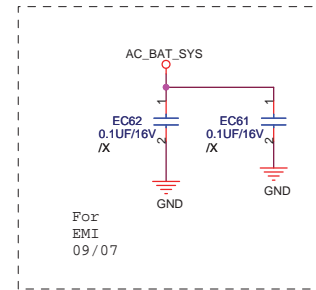
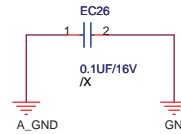
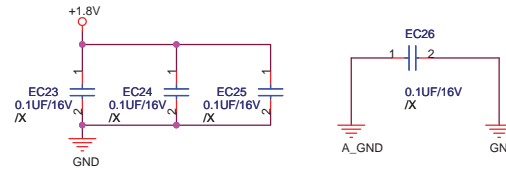
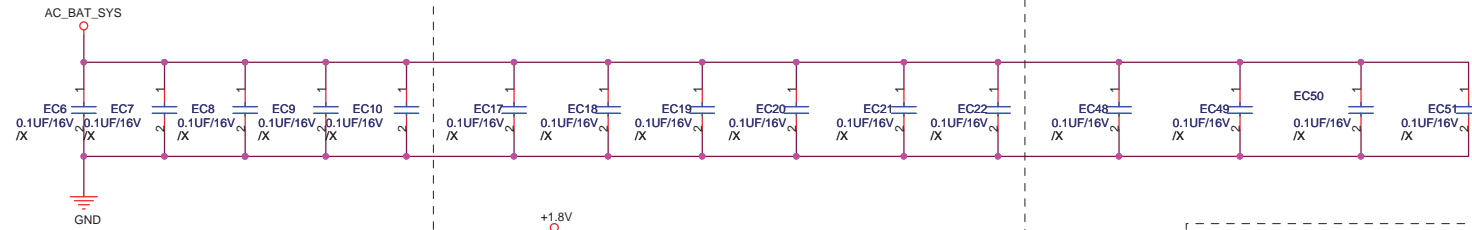
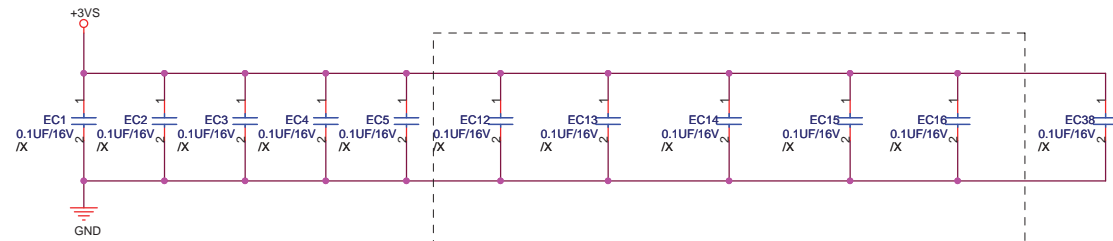
For FLASH LED



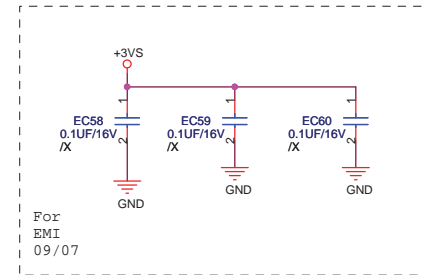
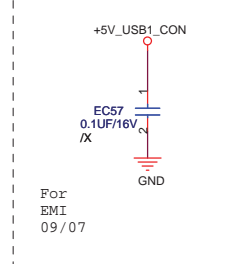
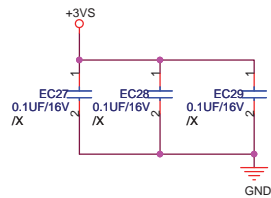
For WLAN LED

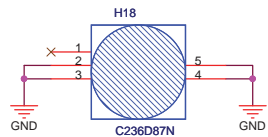
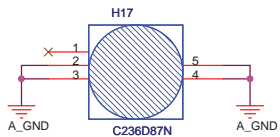
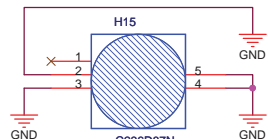
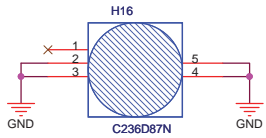
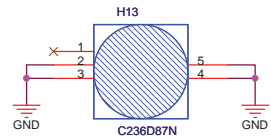
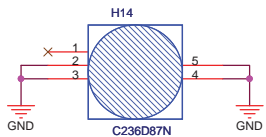
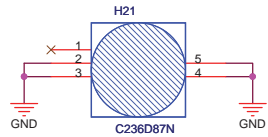
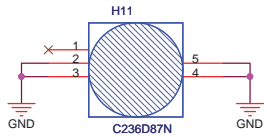
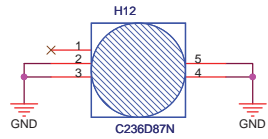
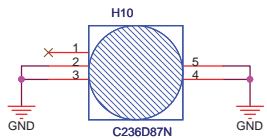
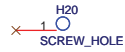
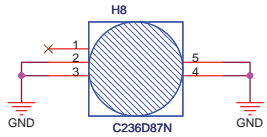
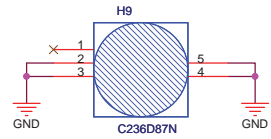
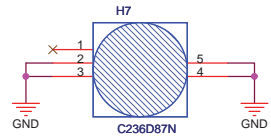


ASUS			Title : LED&Discharge	
ASUSTek Computer INC.			Engineer: Henry_Yang	
Size	Project Name		Rev	
A3	P703		1.2G	
Date:	Tuesday, December 09, 2008	Sheet	39	of 51



1/23 EMI

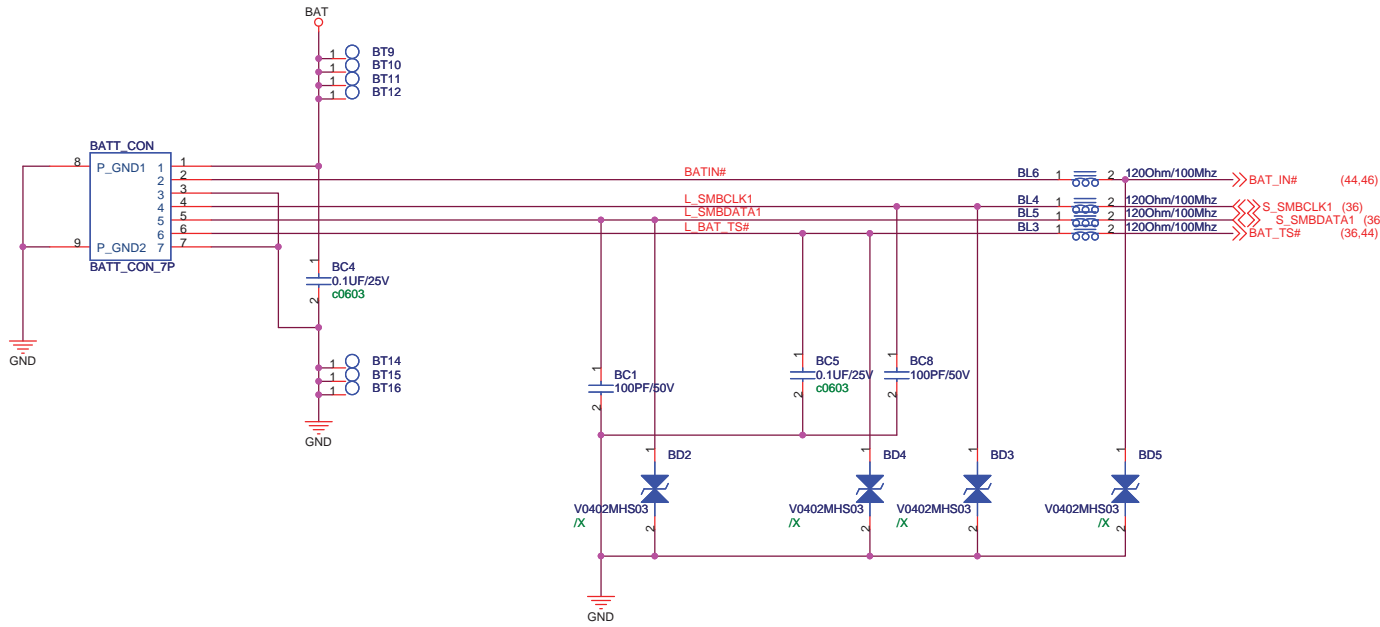
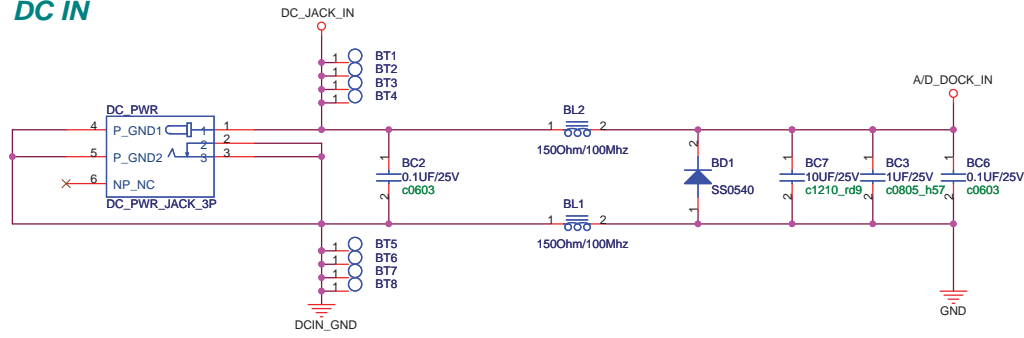




<Variant Name>

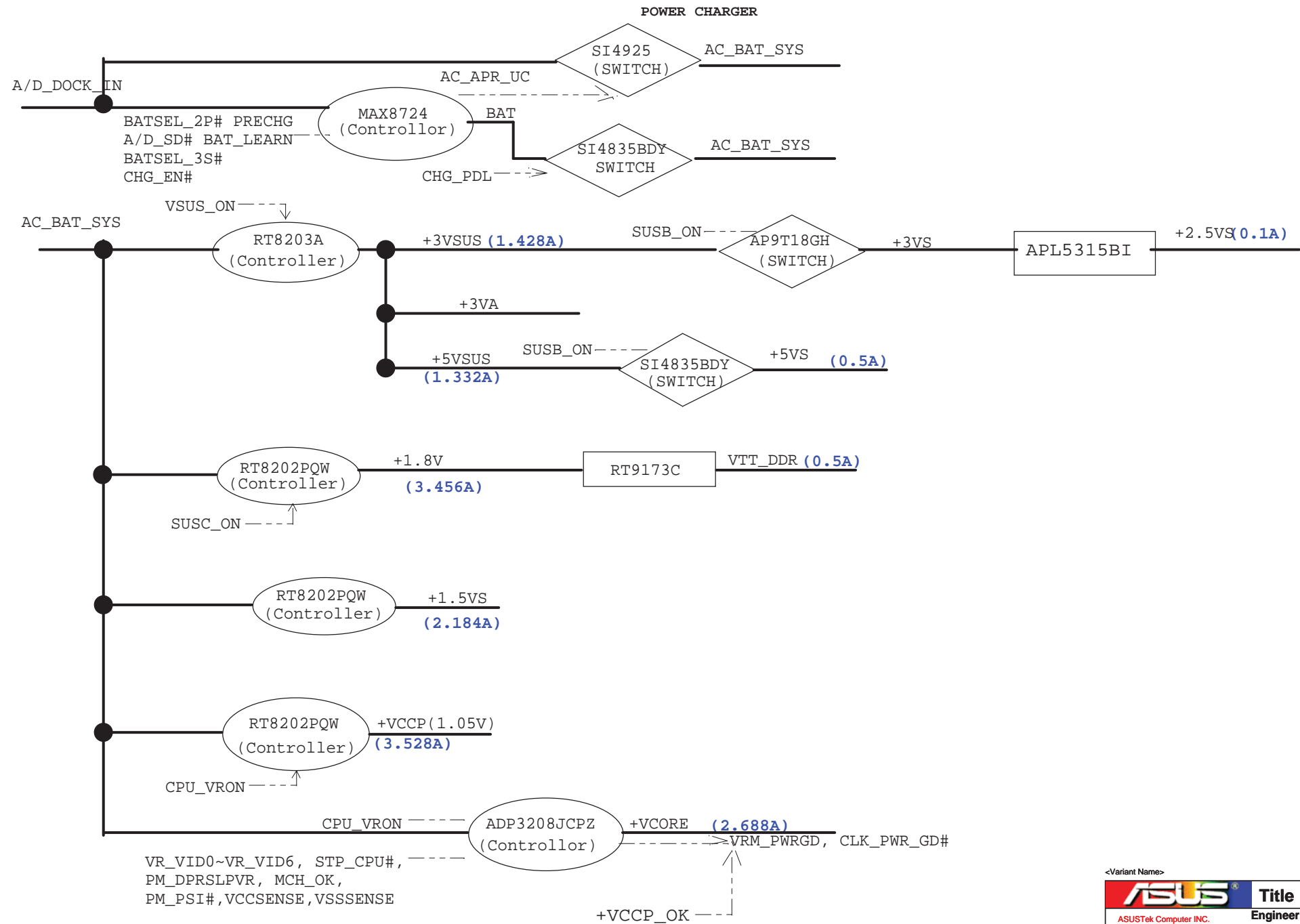
ASUS		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: <i>Henry_Yang</i>	
Size	Project Name		Rev
A3	P703		1.2G
Date: Tuesday, December 09, 2008		Sheet	41 of 51

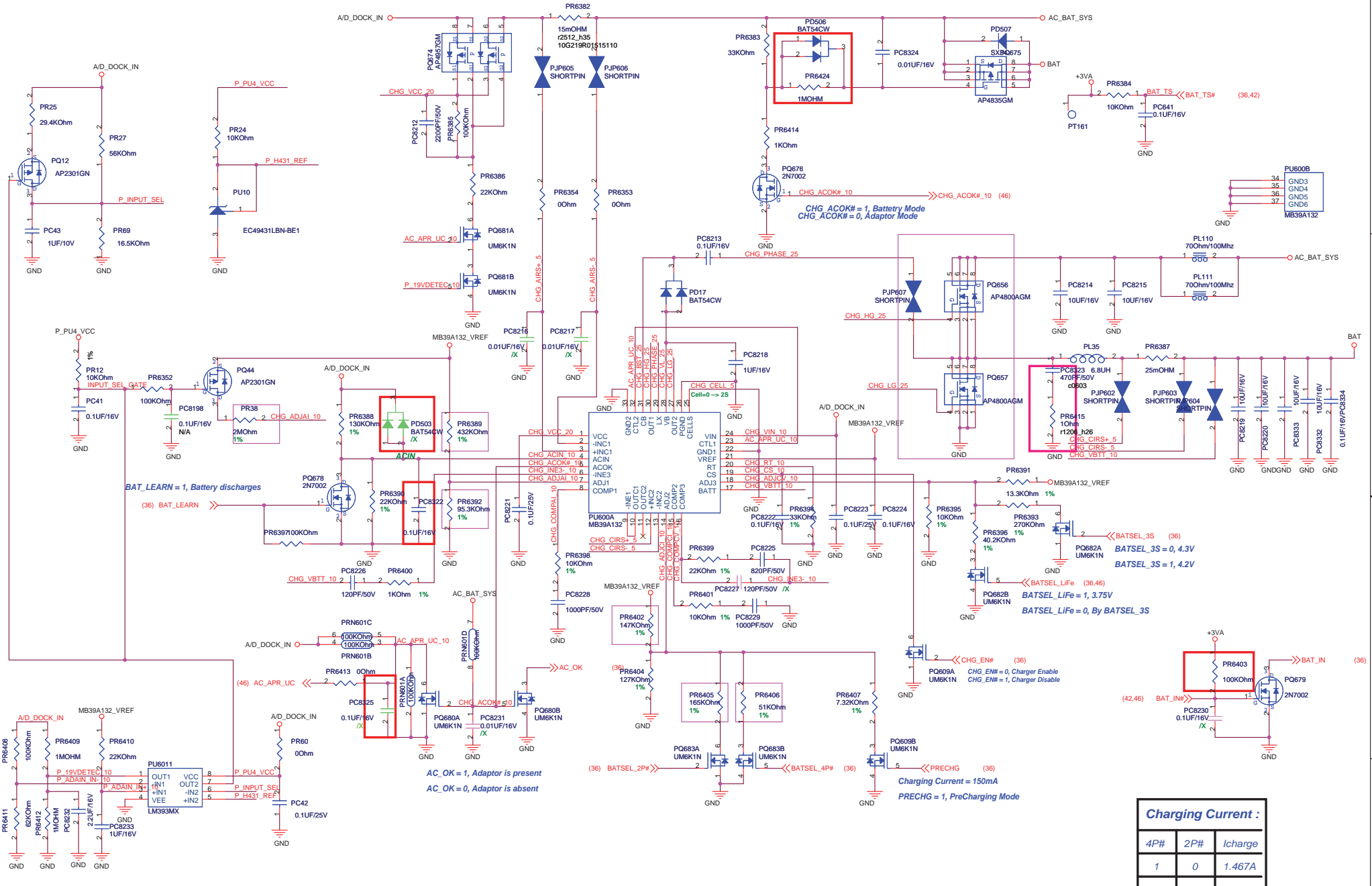
DC IN



<Variant Name>

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: <i>Henry_Yang</i>	
Size A3	Project Name P703	Rev 1.2G	
Date: Tuesday, December 09, 2008	Sheet	42	of 51





Battery Charging Voltage :
 $V_{adj3} > 4.1V \implies V_{bat} = 4.2V / cell$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3} / cell$

Battery Charging Current :
 $4.4V > V_{adj2} > 0V \implies I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s)$

Pre-Charging Mode :
 Precharging current = 150mA
 $V_{adj2} = 168.75mV$

Adaptor Max. Current :
 $PR600 = 235.8k; I_{limit} = 2.170A; 20.615W (9.5V/22V)$
 $PR600 = 185.3k; I_{limit} = 2.677A; 32.124W (12V/36W)$

ACIN Threshold = 1.25V
 Adaptor > 8.63V, System Powered by Adaptor
 Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
 Adaptor > 13.06V, PQ603B Turn-off
 Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
 $BAT_ID = 1, 2 \text{ Cells}; V_{adj2} = 0.998V \implies I_{charge} = 1.477A$
 $BAT_ID = 0, 4/6 \text{ Cells}; V_{adj2} = 1.648V \implies I_{charge} = 2.517A$

Charging Current :

4P#	2P#	I _{charge}
1	0	1.467A
0	1	2.502A
0	0	3.589A

$V_{REF} = 5.0V$
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.23 * CS (\mu F)$

VTH of -IN1: $5V / 62 * (100+62) = 13.06V$
 VTH of ACIN: $1.25V / 25 * (185+25) = 10.5V$
 Change PR607 and PR608 value

ASUS
Title : CHARGER
 ASUSTek Computer INC. Engineer: **Joy_Zhou**

Size: Project Name
 Custom: **P903** Rev: 1.2G

Date: Tuesday, December 09, 2008 Sheet: 44 of 51

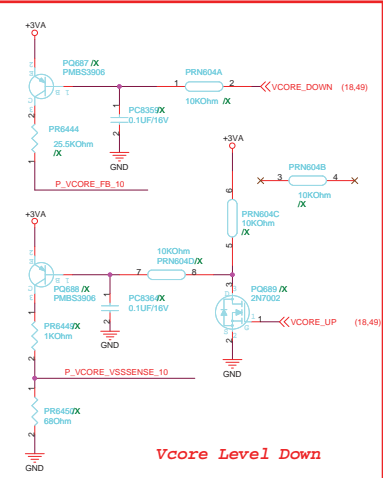
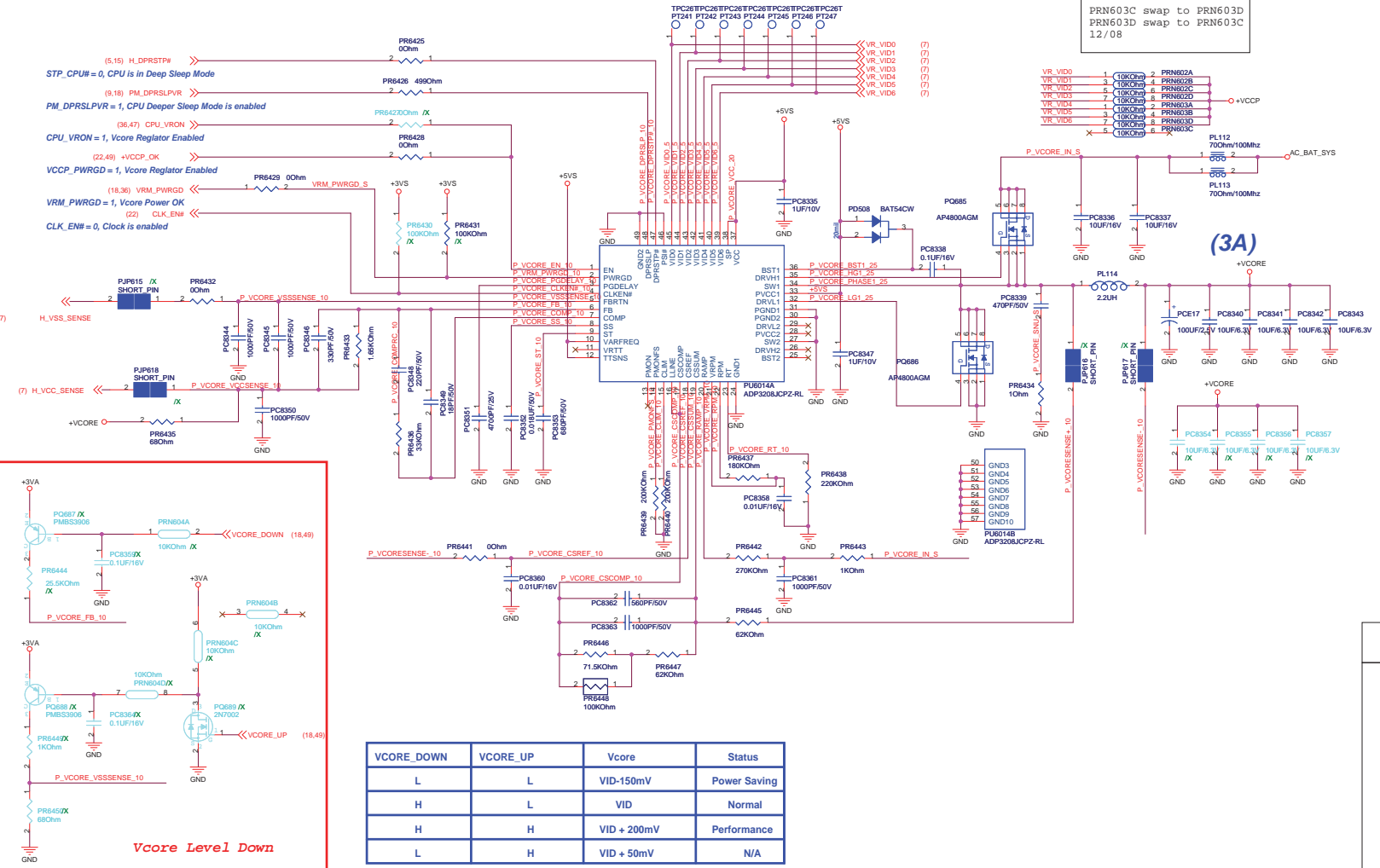
PRN603C swap to PRN603D
 PRN603D swap to PRN603C
 12/08

Power Stage

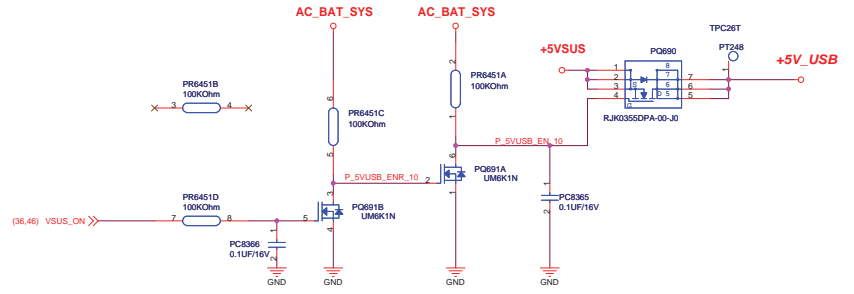
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.95A$
- Ripple Current:**
 $I_{rip} = 3.29A$
 $I_{spec} = 2.5A \text{ } \odot 2 \text{ pcs}$
- Dynamic:**
 $I_{peak} = 8.5A$
 $ESR/2PCS = 9 \text{ mohm}$
 $V = 76.5mV$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18 \text{ mohm}$
- MOSFET Spec:**
H-side MOSFET: RJK0355DPA-00-J0 WPAK
 $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25$)
 $I_{peak} = 120A$ (Pause $\leq 10us$)
L-side MOSFET: RJK0355DPA-00-J0 WPAK
 $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25$)
 $I_{peak} = 120A$ (Pause $\leq 10us$)

Controller

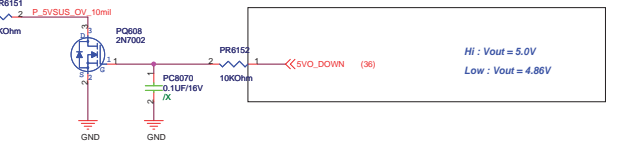
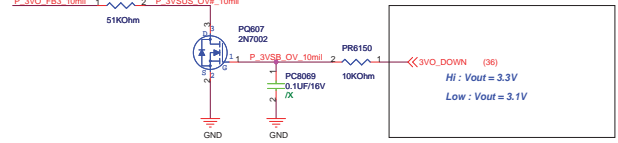
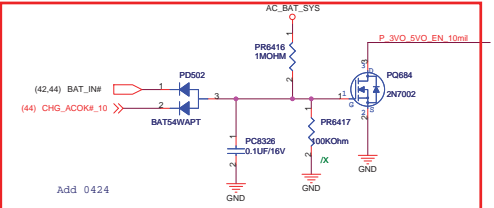
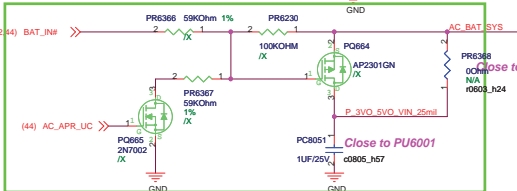
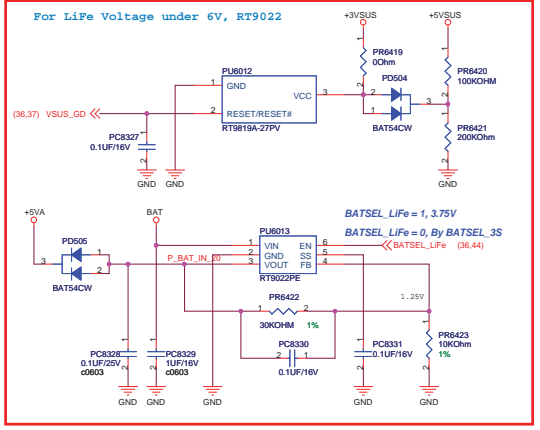
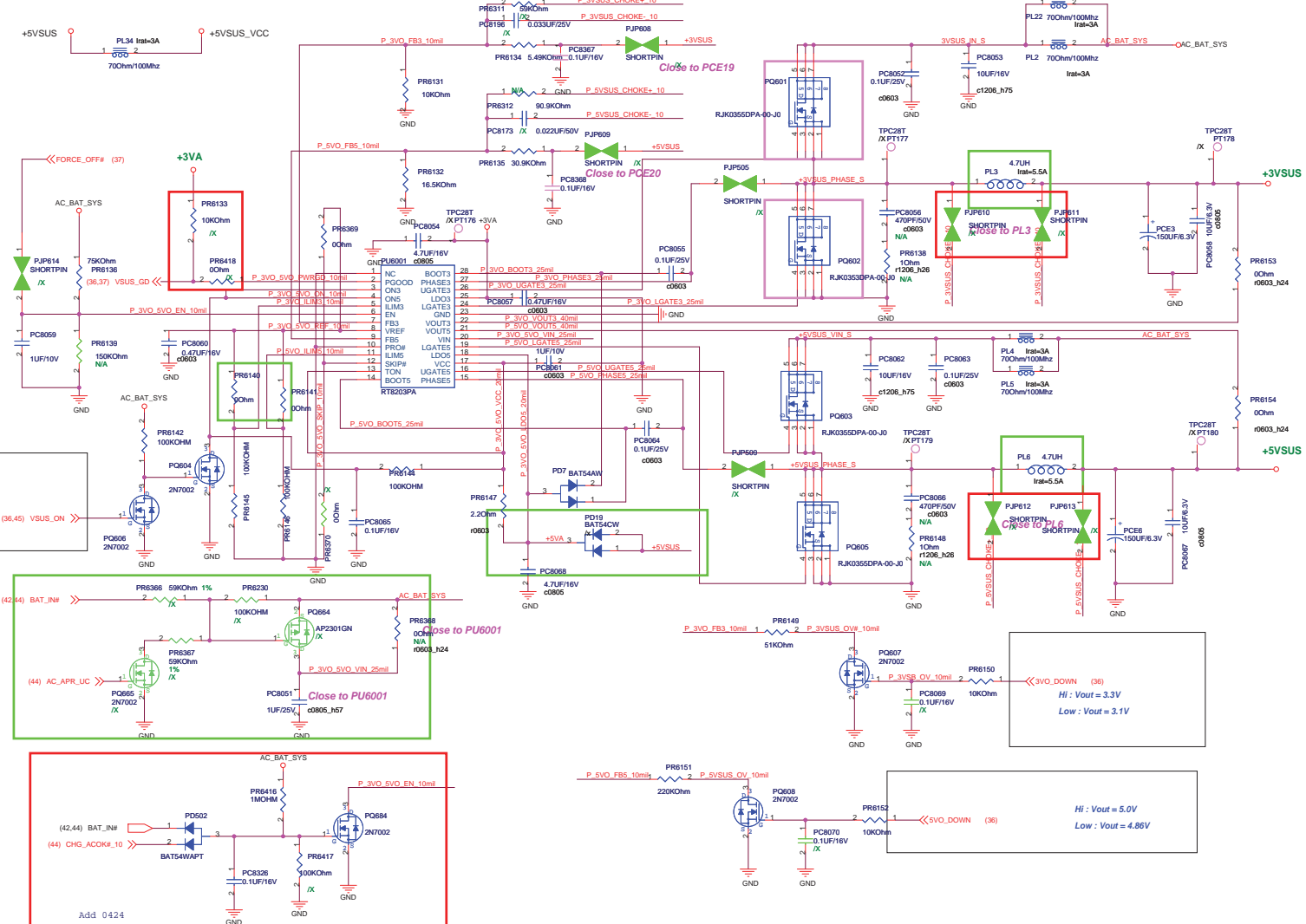
- Voltage & Current:**
 $V_{CORE} = 0.6 - 1.2V @ 8.5A$
- Frequency:**
 Set PR58=220Kohm
 $F_{osc} = 204KHz$ for RPM
 Set PR57=180Kohm
 $F_{osc} = 333KHz$ for CCM
- OCP:**
 Set PR60=1MKOHM
 $I_{ocp} = 33A$
- POR:**
 $POR \text{ Hysteresis} = 0.15V$
 $V_{on} = 4.4 - 4.5V$
 $V_{off} = 4.0 - 4.2V$
- UVP:**
 $VID = 300mV$
- OVP:**
 $VID = 200mV$
- Enable Voltage:**
 $V \text{ rising} = 4.4V$
 $V \text{ falling} = 4.2V$
- Soft start time:**
 $2.7ms$
- Phase selection:**
 $SP = VCC$
 single phase
- Inrush Current:**
 $C \text{ total} = 140uF$
 $I \text{ inrush} = 0.056A$
- Loadline:**
 $30mOhm$

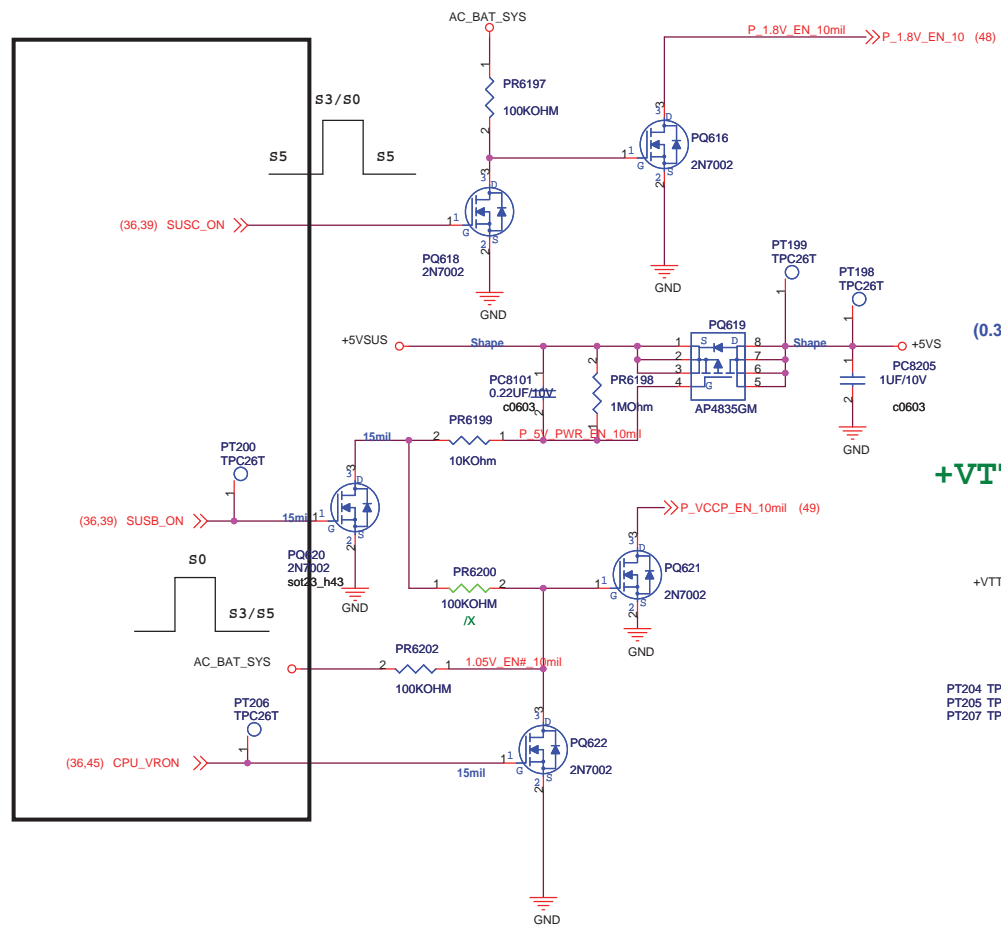
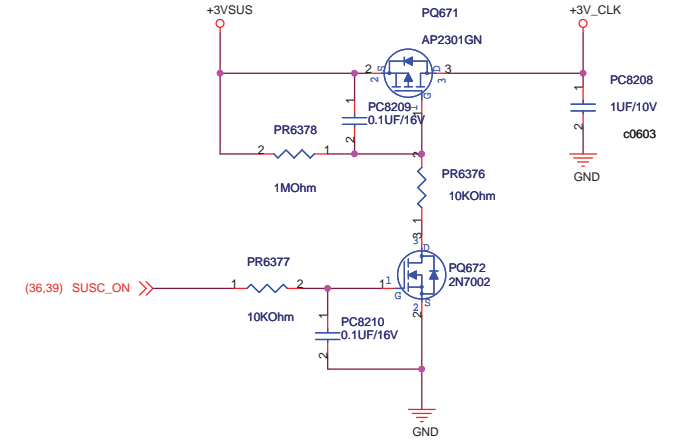
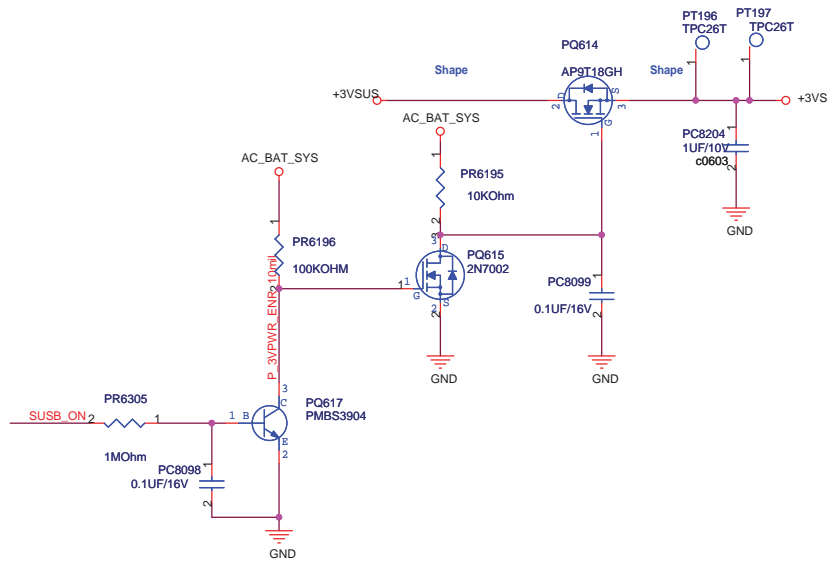


VCORE_DOWN	VCORE_UP	Vcore	Status
L	L	VID-150mV	Power Saving
H	L	VID	Normal
H	H	VID + 200mV	Performance
L	H	VID + 50mV	N/A

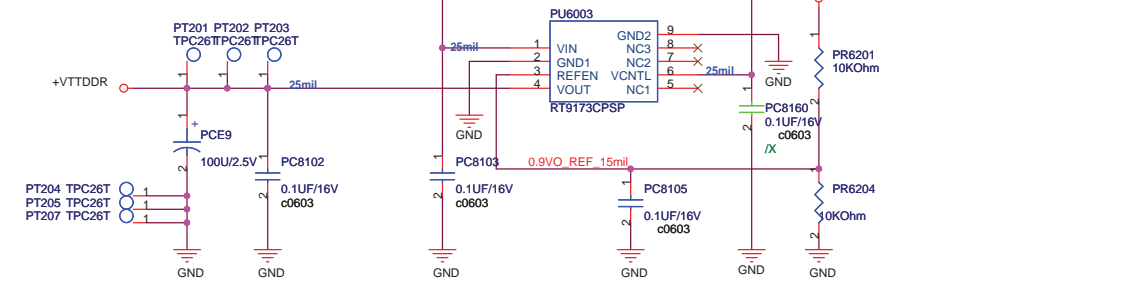


For USB Insert And Remove Protection
<http://hobi-elektronika.net>

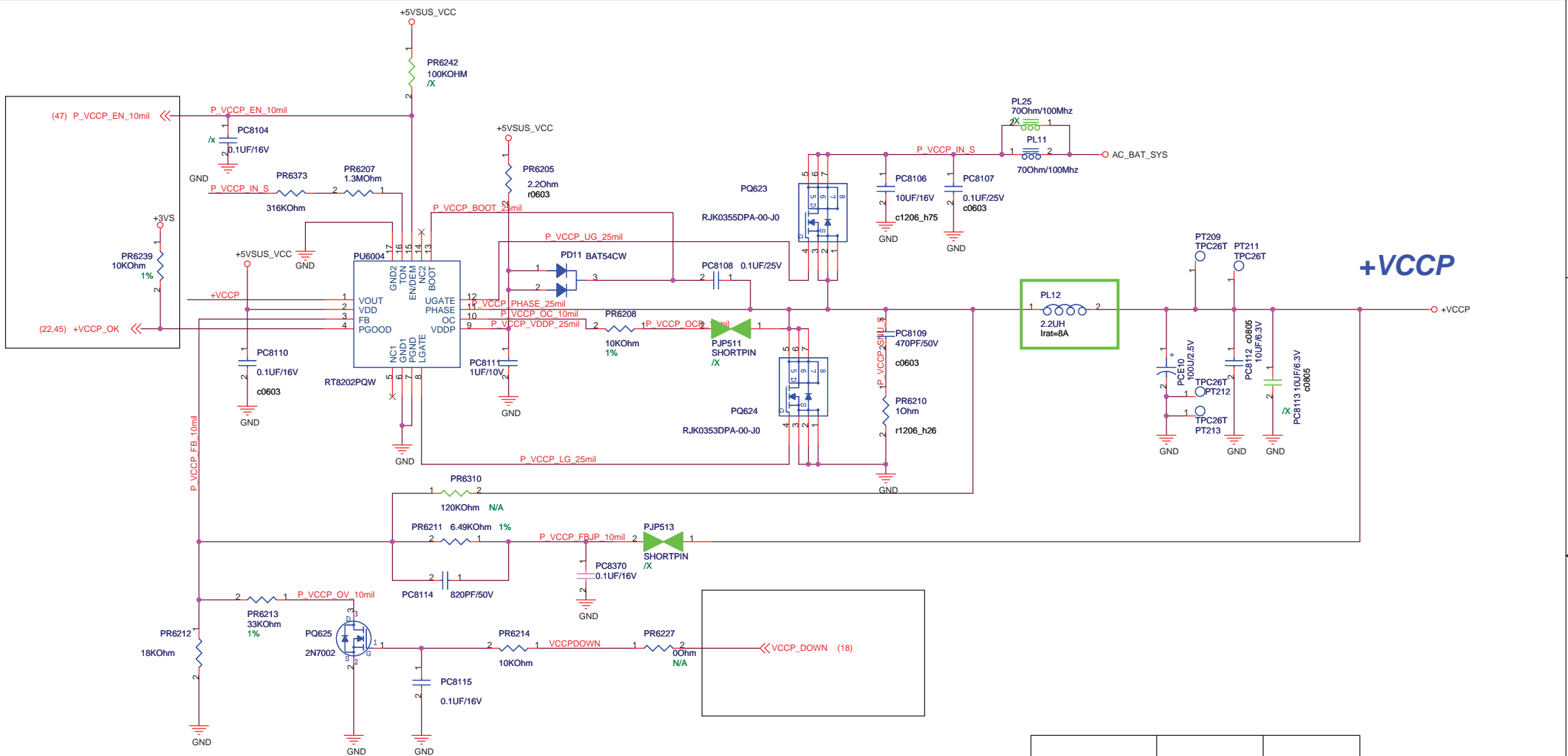




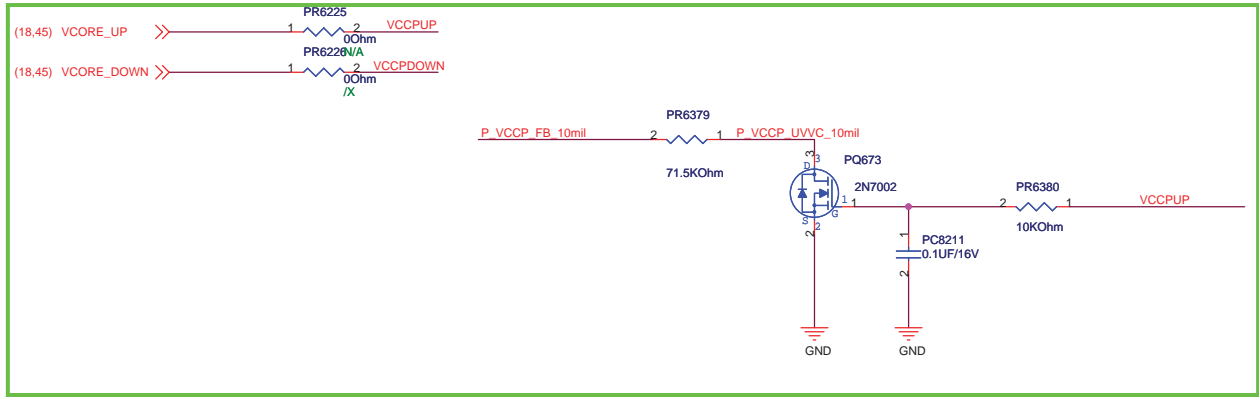
(0.3A)
+VTT_DDR (0.5A)



<Variant Name>		ASUS Title: 3V_5V_VTT_DDR	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name P903	Date: Tuesday, December 09, 2008	Rev 1.1G
Date:		Sheet	47 of 51



+VCCP



VCCP_DOWN	VCCPUP	+VCCP
0	0	+0.95V
0	1	+1V
1	0	+1.05V
1	1	+1.1V

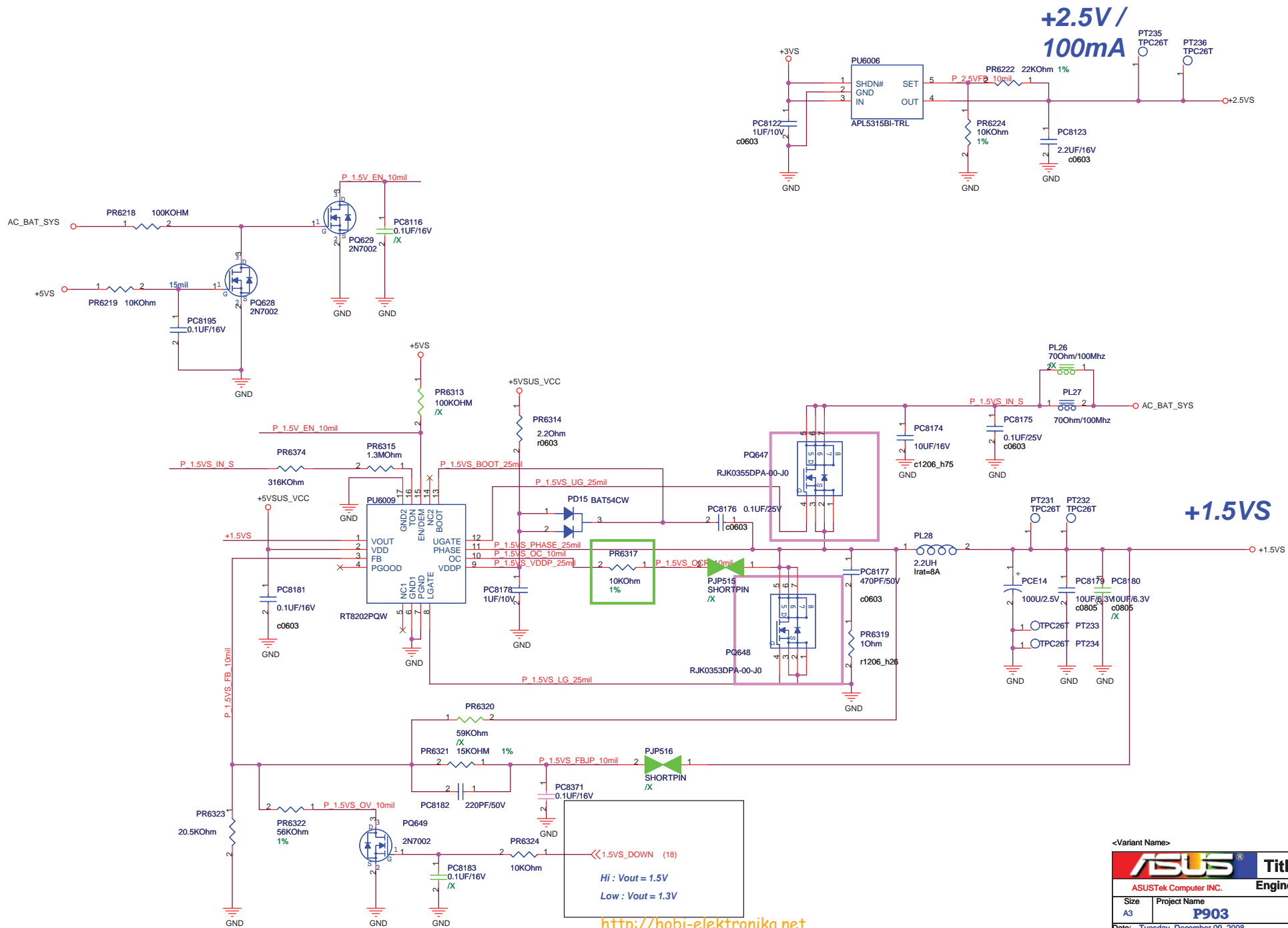
<Variant Name>

ASUS Title : **VCCP**

ASUSTek Computer INC. Engineer: **Joy_Zhou**

Size A3	Project Name P703	Rev 1.1G
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Date: Tuesday, December 09, 2008 Sheet 49 of 51



+2.5V / 100mA

+1.5VS

Hi : Vout = 1.5V
 Low : Vout = 1.3V

<http://hobi-elektronika.net>

<Variant Name>

		Title : 1.05V_1.5V_2.5V	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name P903	Rev 1.1G	
Date: Tuesday, December 09, 2008	Sheet 50	of 51	

- 1.Change the Audio Jack.
- 2.Add BD5 for BAT_IN# ESD, modify the BATIN to BATIN#.
- 3.Add PM_DPRS LPVR to 945GSE,
if use this signal you need /X NR21
- 4.Change PR6406 to 51K
- 5.Change YLED4 to BLUE and change yr6 to 4.7K
- 6.Change YLED2 to orange&green and add a circuit to support it.
- 7.Add the circuit of blue tooth on page32
- 8.Add the circuit to support sata flash module.(sata signal,sata
clock and satarbias.)
- 9.remove modem and change the lan&modem connector.
- 10.change HC14 to 10uf and modify HC9 to /X
- 11.add a dip spi and correlative circuit for RD debug on page36.
- 12.add a 24pin KB connector on page 38 to compatible with 906
- 13.change HR4 from 0 ohm to 300 ohm/100MHZ
- 14.REMOVE 24PIN KB CIRCUIT
- 15.update power p44-p50
- 16.add test point pt235 pt236 for 2.5v
- 17.add gr19 for lcd sense on P24
- 18.add sys_reset on p37
- 19.ADD EMI C P40
- 20.touch pad update