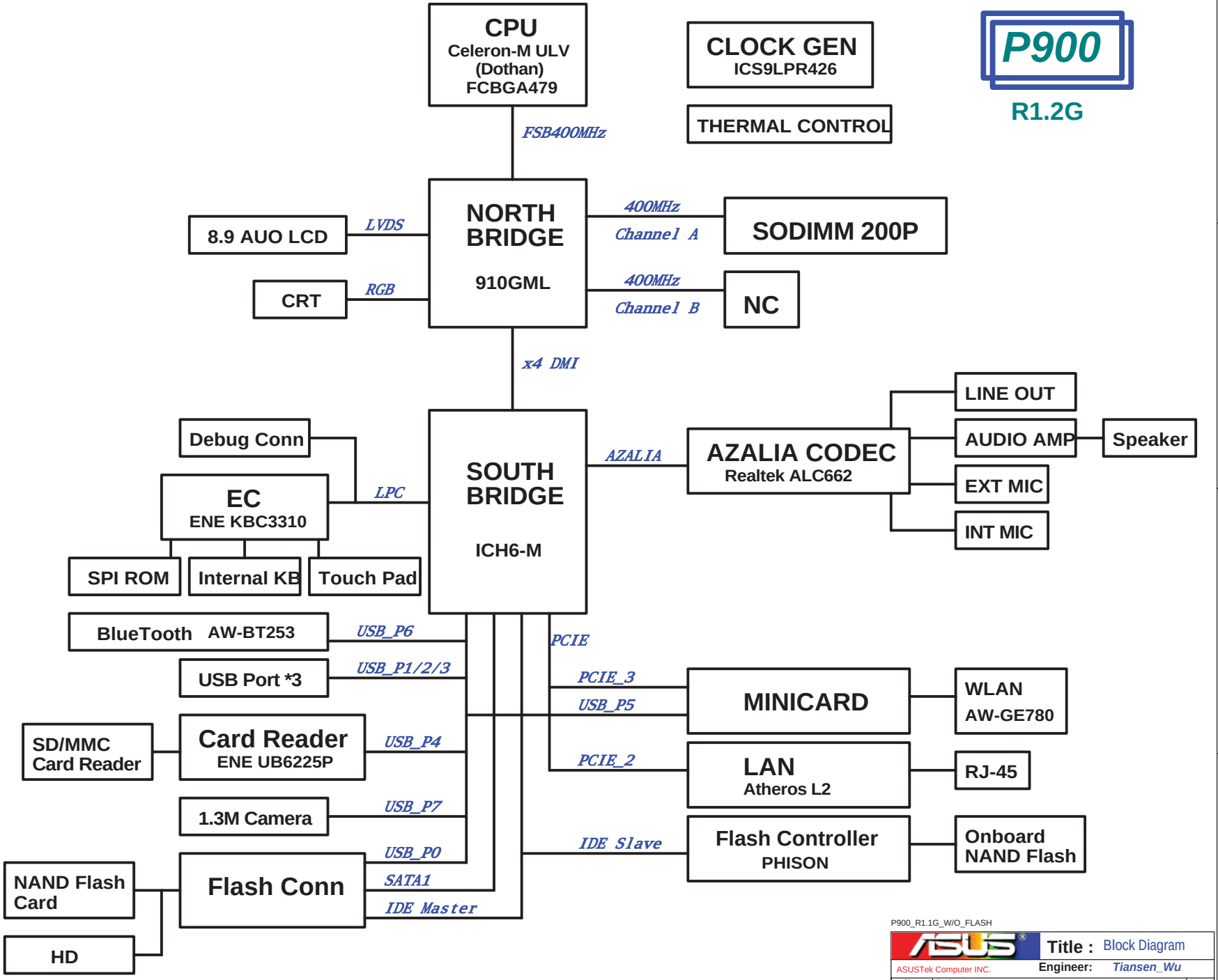


P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 1 of 47	

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	S_SMBALERT#	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PCI#	Clock GEN STP_PCI#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	CAMERA_EN	GPO	fixed as Output only
NA	GPIO22	NC	NA	NA
AD21	GPO23	SPEAKER_EN#	GPO	fixed as Output only
V3	GPIO24	MINICARD_EN#	I/O	Output
P5	GPIO25	WLAN_ON#	I/O	Output

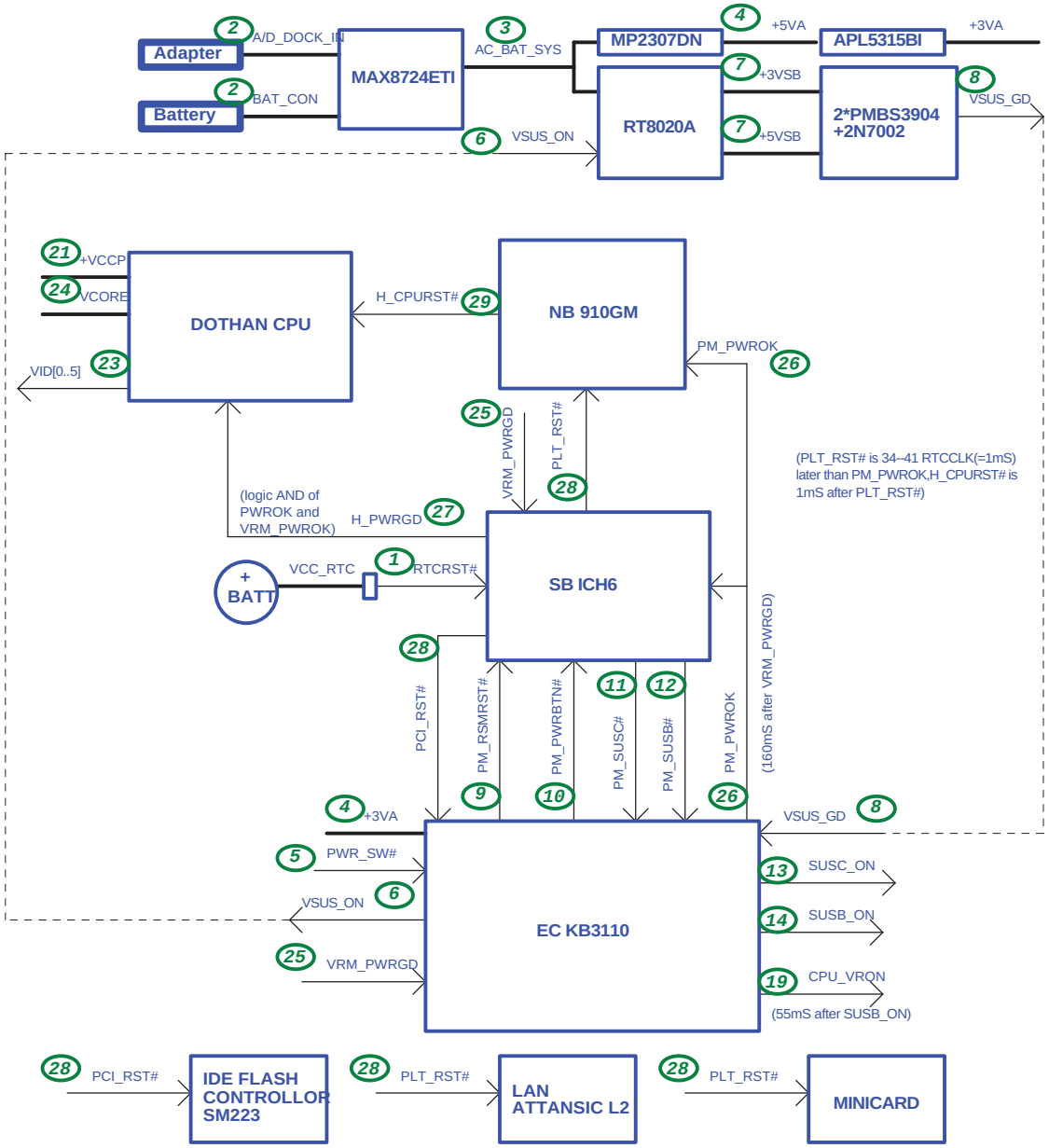
Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	CARD_READER_EN#	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	PM_VCOREL1	I/O	Output
AC18	GPIO34	PM_VCOREL2	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

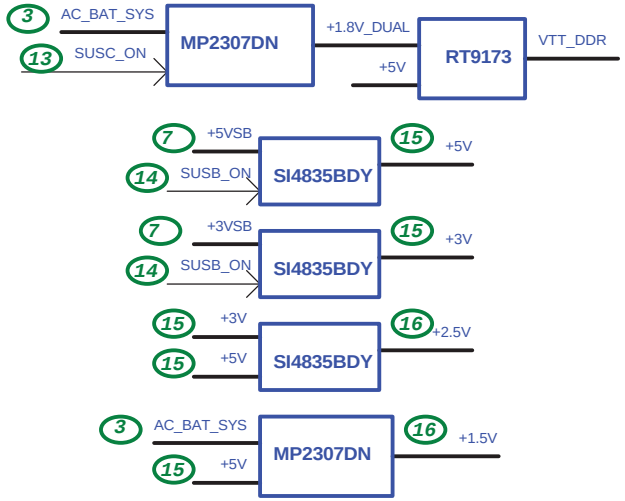
P900_R1.1G_W/O_FLASH

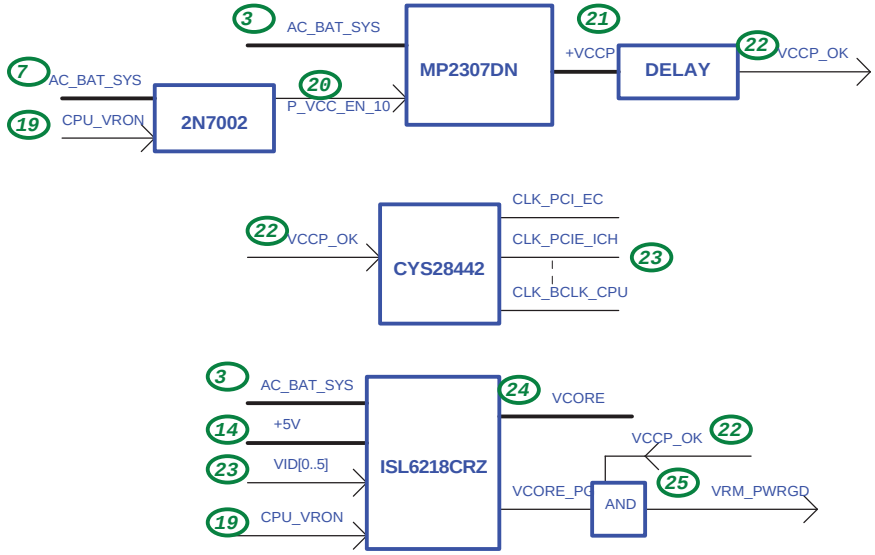
ASUSTek Computer INC.	Title : System Setting	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 2 of 47	

*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in,the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#

	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL







P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Power Sequence	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 3 of 47	

EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	EMAIL_SW#	I	EMAIL_SW# , *
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	BAT_EXT	O	Reserved
15	GPIO08	EXTSMI#	O	EXTSMI#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	NC	O	LCD chip select
18	GPIO0C	NC	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SCI#	KBC_SCI#	O	KBC_SCI#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	BAT_CRITICAL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	E51_RX	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	NUM_LED#	O	EC H/W controls(Unused)
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	BAT_ICHG	I	Sense Power Loading
64	AD1	BAT_CONFIG	I	sense Battery
65	AD2	BAT_SENT	I	Reserved
66	AD3	BAT_TS	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSAVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	PM_BATLOW#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB1_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB1_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB2_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB2_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	LCD_SCL	O	Reserved
84	PSDAT1	LCD_SDA	O	Reserved
85	PSCLK2	LCD_CSB	O	Reserved
86	PSDAT2	LCD_VSYNC	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CAP_LED#	O	EC H/W controls
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	"HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P~3P
110	GPXID1	CPU_LEVELDOWN#	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is over spec
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	BAT_VOLSEL	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Tiansen_Wu

Size	Project Name	Rev
A3	P900	1.2G

Date: Wednesday, February 27, 2008 Sheet 4 of 47

P701 CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.0G	2007/02/26 ~ 2007/03/16	S701L Schematic 1.0G Beginning S701L 1.0G Gerber Out
1.1G	2007/03/24 ~ 2007/04/19	S701L Schematic 1.1G Beginning S701L 1.1G Gerber Out
1.0G	2007/04/24 ~ 2007/05/22	P701(S701L renamed) Schematic 1.0G Beginning 1. PC8054, PR6075 /X to N/A 2. Attansic L2 change to Atheros L2(pin to pin) 3. LC1, LC33 /CAP/X to N/A 4. C87 change to X5R to cost down 5. L1, L2, L3 change to 56 NH, R5, R6 change to 75 Ohm to pass CRT EA measure 6. PR48 change to 22K Ohm, PC35 change to 4700PF to fix no VCORE issue 7. PR6074 change to 4.7K Ohm to fix +3VSB OCP issue 8. Clock Gen CY28442-2 change to ICS9LPR367 9. Phase in Power Level Reduce solution, mark "Taipei0508" 10. Card Reader Socket change to SD Socket 12G25100091E 11. Add System FAN circuit 12. Camera change to USB port 7, Minicard change to USB port 5 13. Use SB GPIO27 to Enable/Disable Card Reader UB6225P 14. Use SB GPIO28 to Enable/Disable Modem 15. Card Reader UB6225P share 48M clock from CLock Gen with SB USB part 16. Add D29 to fix LCD_CSB leakage current issue 17. LC29, LC30 change to 27PF to pass EA crystal measure 18. Change vaule of PR73, PR74, PC56 and add PC60 to adjust the power sequence timing between Stand By power and RSMRST# 19. Remove USB port 1 20. Add +5V generate +3V_LCD circuit 21. Remove +5V_CHG generate circuit 22. Use SB GPIO33, GPIO34 to controll the level of VCORE 23. U31 use APL5315BI-TRL to replace MAX8863TEUK(pin to pin, but reference voltage level different) 24. PR59 change to 130K Ohm for both 12V Adapter and 9.8V Adapter P701 1.0G Gerber Out
1.1G	2007/05/31 ~ 2007/06/07	P701 Schematic 1.1G Beginning 1. Remove the 48M clock from CLock Gen to Card Reader UB6225P 2. Clock Gen ICS9LPR367 change to ICS9LPR426 3. Flash Connector increase SATA and USB interface 4. Add Onboard Flash(SM223 + NAND Flash x4) 5. BATT_CON pin 5 connect to GND 6. Q34 pin 1 connect to +3V to fix EC reset issue 7. Remove J1, J2 8. KB pin 28 connect to GND for P701-ISP_CARD 9. Use SB GPO23 to Enable/Disable Audio Amplifier 10. Use SB GPO21 to controll Camera Power 11. Use SB GPIO24 to controll Minicard Power 12. Use SB GPIO25 to Enable/Disable WLAN Ratio 13. Atheros L2 and Minicard SMBUS interface directly pull high 14. LCD_CON pin 20 connect to AC_BAT_SYS P701 1.1G Gerber Out

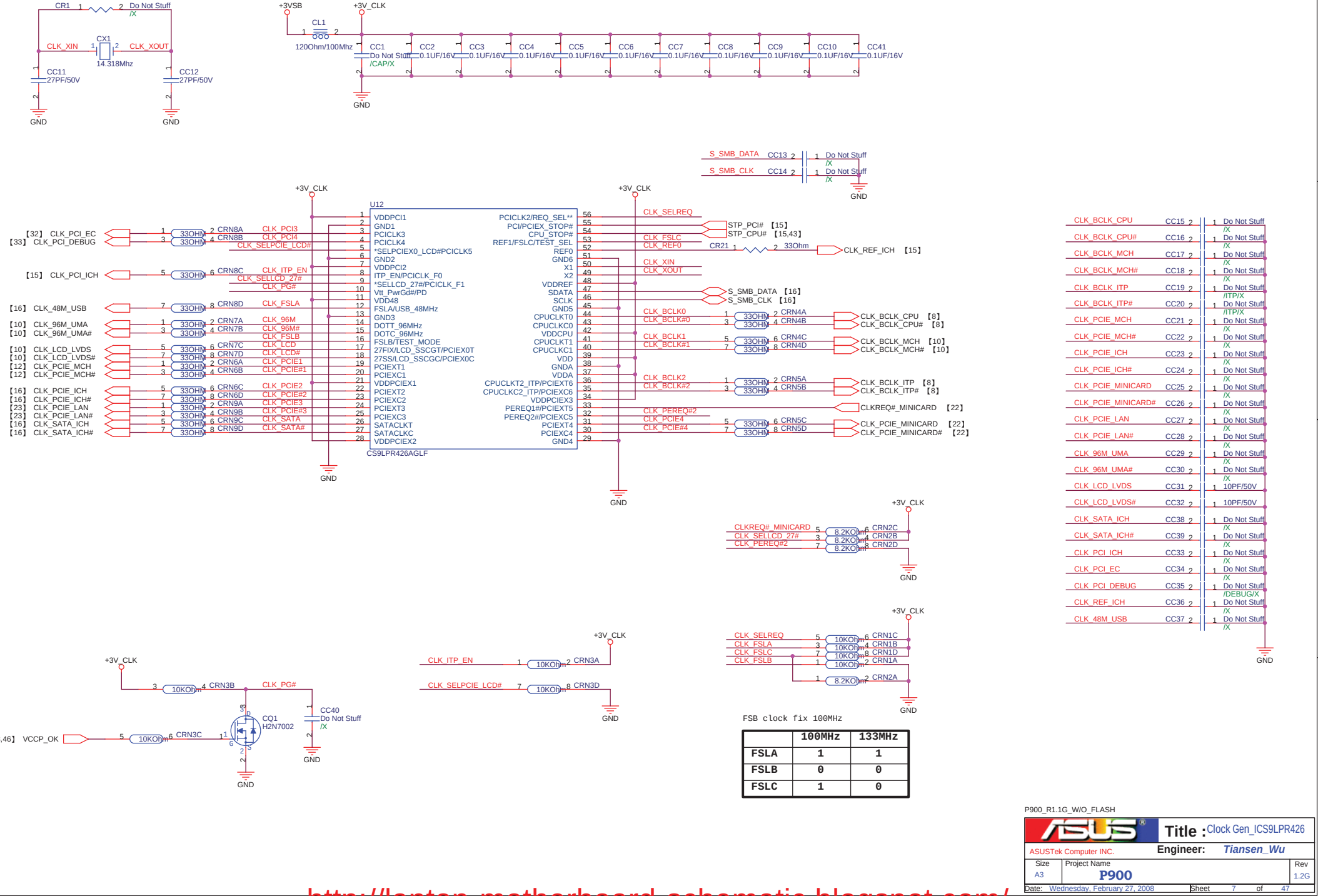
Rev	Date	Description
1.2G	2007/06/30 ~ 2007/07/06	P701 Schematic 1.2G Beginning 1. Add R174 to short DASP pins of Master IDE device and SLave IDE device 2. Use SB GPIO27 to controll Card Reader UB6225P Power 3. PR606084.2 connect to +5V to fix LCD flash issue 4. Adjust SPEAKER pin define 5. Adjust CHARGE LED and WLAN LED lightness 6. Use SB GPI 26, 29, 30, 31 for PCB version 7. Change USB ESD diode for EMI request 8. Add Floating GND TP_GND and Spring TP1 & TP2 for EMI request 9. Change PM_VCOREL1, PM_VCOREL2 default level 10. Add PQ48 to controll +3V_PE to fix WLAN AW-GE780 can't detect issue 11. Power Charger part update circuit for new Adapter 12. Use SB GPI12 to detect LID signal level 13. Add H/W THERMTRIP circuit (page 36) 14. Add U40 to prevent system auto power on after clear CMOS 15. Use SB GPI7 for THRO_CPU 16. Power Charger part update circuit to prevent incorrect Adapter damage boards 17. Q1.1, Q2.1 change to +3V P701 1.2G Gerber Out
1.2G	2007/07/26 ~	P701 Schematic 1.3G Beginning 1. Add R11 for 801

P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : History	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 5 of 47	

P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Blank	
	Engineer: *Tiansen_Wu*	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 6 of 47	

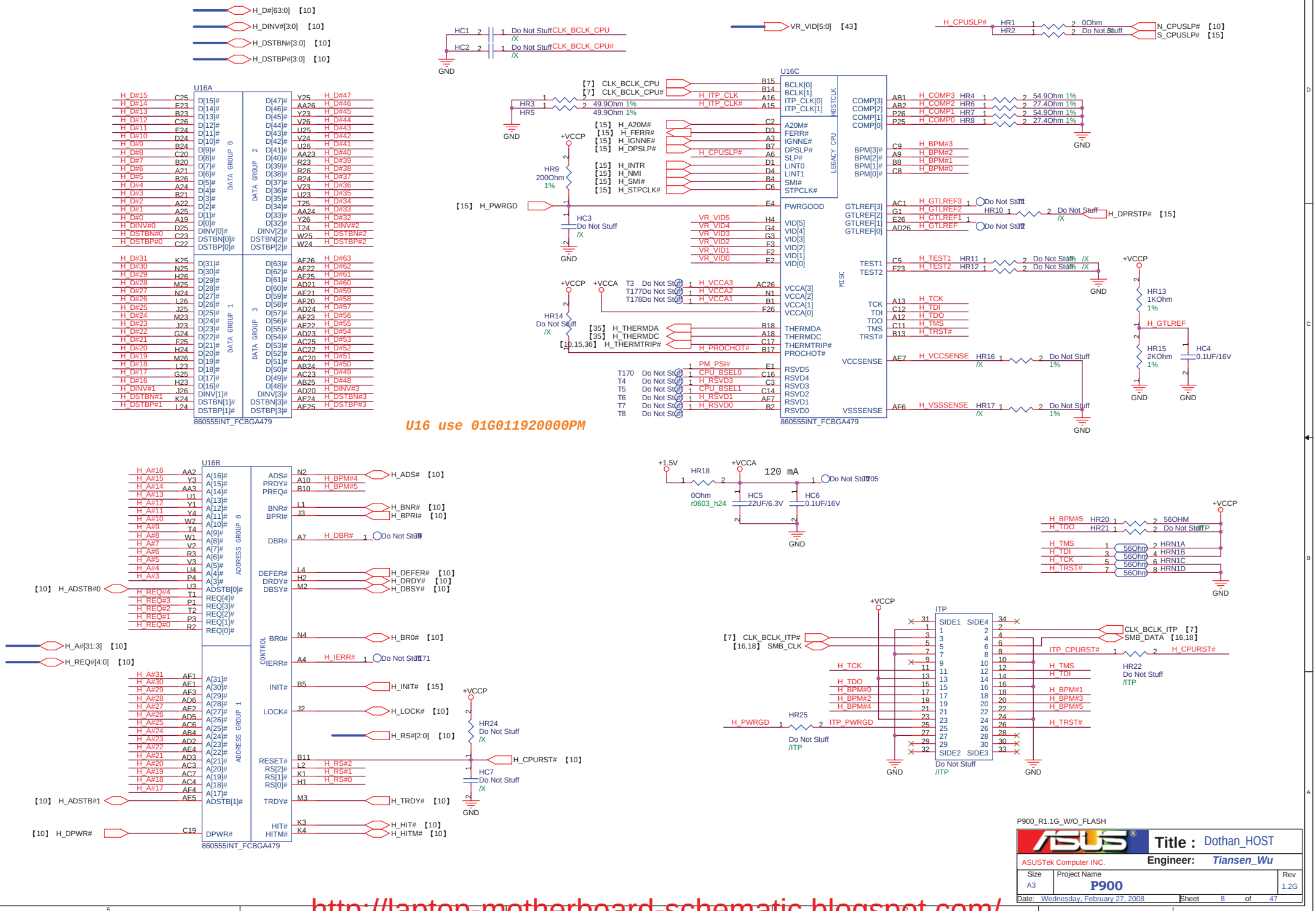


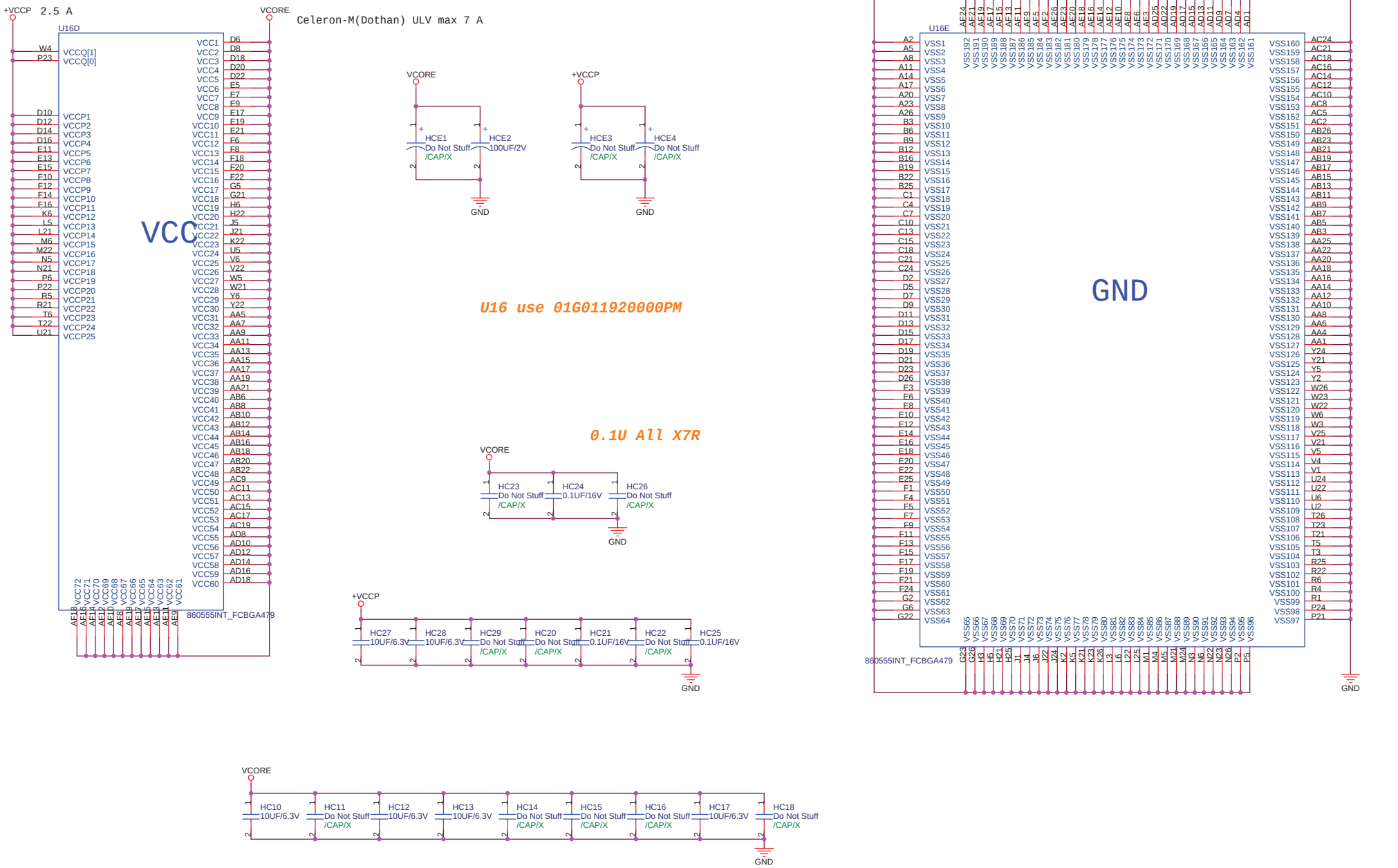
FSB clock fix 100MHz

	100MHz	133MHz
FSLA	1	1
FSLB	0	0
FSLC	1	0

P900_R1.1G_W/O_FLASH

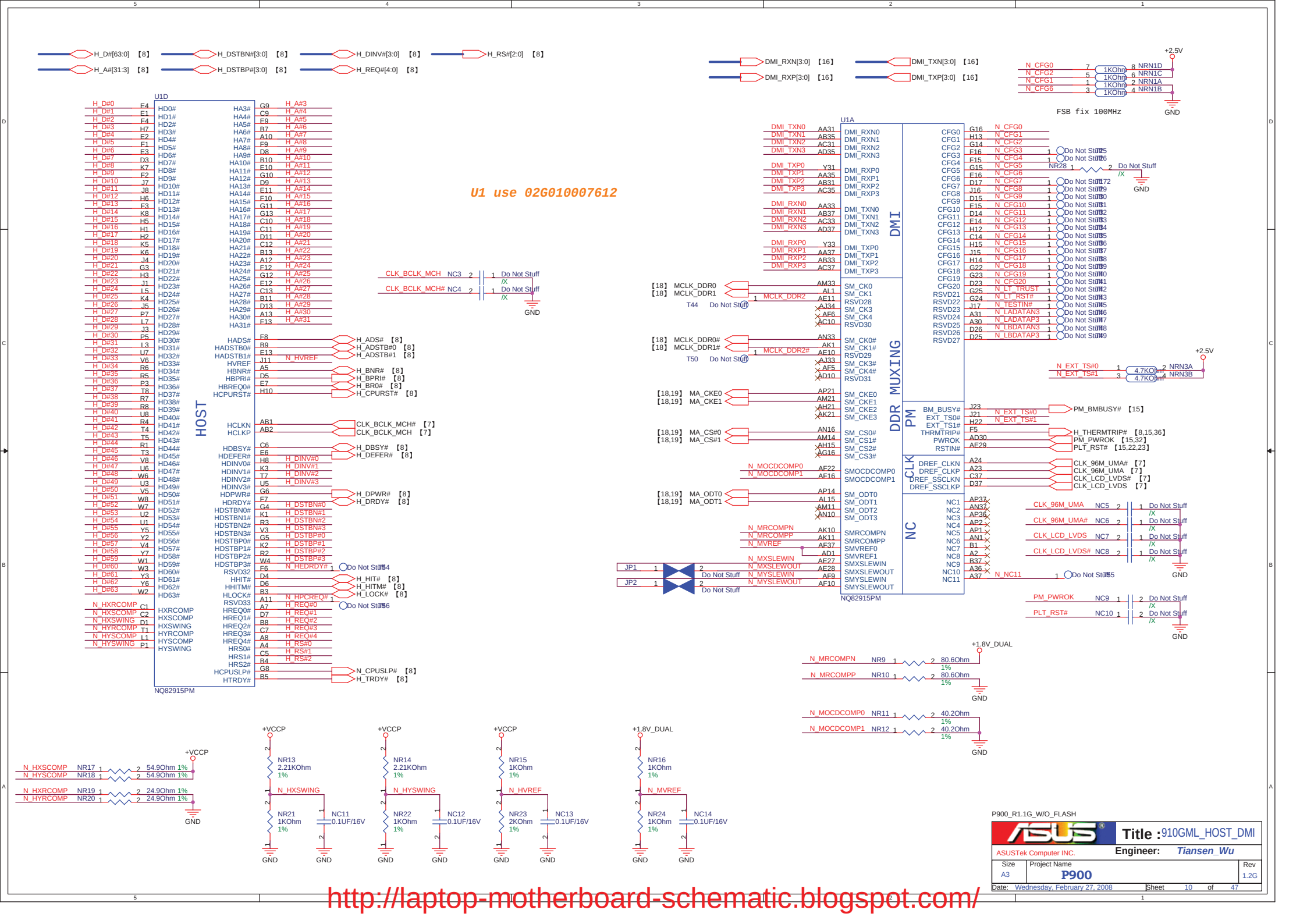
ASUSTek Computer INC.	Title : Clock Gen_ICS9LPR426	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 7 of 47	





P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Dothan_PWR_GND	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 9 of 47	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H_A#[31:3] 【8】
H_DSTBN#[3:0] 【8】
H_DSTBP#[3:0] 【8】
H_DINV#[3:0] 【8】
H_REQ#[4:0] 【8】
H_RS#[2:0] 【8】
U1D
HOST
NQ82915PM
U1 use 02G010007612
DMI_RXN[3:0] 【16】
DMI_RXP[3:0] 【16】
DMI_TXN[3:0] 【16】
DMI_TXP[3:0] 【16】
U1A
DMI
DDR MUXING
PM
CLK
NC
NQ82915PM
FSB fix 100MHz
+2.5V
GND
+1.8V_DUAL
+VCCP
Do Not Stuff
P900_R1.1G_W/O_FLASH
Title :910GML_HOST_DMI
ASUSTek Computer INC.
Engineer: Tiansen_Wu
Size A3
Project Name P900
Rev 1.2G
Date: Wednesday, February 27, 2008
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http://laptop-motherboard-schematic.blogspot.com/

MA_DQ[63:0] 【18】
MA_DQS[7:0] 【18】
MA_DQS#[7:0] 【18】
MA_DM[7:0] 【18】
MA_MA[13:0] 【18,19】
MA_BA[2:0] 【18,19】

U1 use 02G010007612

U1B

DDR SYSTEM MEMORY A

MA_DQ0	AG35	SA_DQ0	SA_BS0	AK15	MA_BA0
MA_DQ1	AH35	SA_DQ1	SA_BS1	AK16	MA_BA1
MA_DQ2	AL35	SA_DQ2	SA_BS2	AL21	MA_BA2
MA_DQ3	AL37	SA_DQ3			
MA_DQ4	AH36	SA_DQ4	SA_DM0	AJ37	MA_DM0
MA_DQ5	AJ35	SA_DQ5	SA_DM1	AP35	MA_DM1
MA_DQ6	AK37	SA_DQ6	SA_DM2	AL29	MA_DM2
MA_DQ7	AL34	SA_DQ7	SA_DM3	AP24	MA_DM3
MA_DQ8	AM36	SA_DQ8	SA_DM4	AP9	MA_DM4
MA_DQ9	AN35	SA_DQ9	SA_DM5	AP4	MA_DM5
MA_DQ10	AP32	SA_DQ10	SA_DM6	AJ2	MA_DM6
MA_DQ11	AM31	SA_DQ11	SA_DM7	AD3	MA_DM7
MA_DQ12	AM34	SA_DQ12			
MA_DQ13	AM35	SA_DQ13	SA_DQS0	AK36	MA_DQS0
MA_DQ14	AL32	SA_DQ14	SA_DQS1	AP33	MA_DQS1
MA_DQ15	AM32	SA_DQ15	SA_DQS2	AN29	MA_DQS2
MA_DQ16	AN31	SA_DQ16	SA_DQS3	AP23	MA_DQS3
MA_DQ17	AP31	SA_DQ17	SA_DQS4	AM8	MA_DQS4
MA_DQ18	AN28	SA_DQ18	SA_DQS5	AM4	MA_DQS5
MA_DQ19	AP28	SA_DQ19	SA_DQS6	AJ1	MA_DQS6
MA_DQ20	AL30	SA_DQ20	SA_DQS7	AE5	MA_DQS7
MA_DQ21	AM30	SA_DQ21			
MA_DQ22	AM28	SA_DQ22	SA_DQS0#	AK35	MA_DQS#0
MA_DQ23	AL28	SA_DQ23	SA_DQS1#	AP34	MA_DQS#1
MA_DQ24	AP27	SA_DQ24	SA_DQS2#	AN30	MA_DQS#2
MA_DQ25	AM27	SA_DQ25	SA_DQS3#	AN23	MA_DQS#3
MA_DQ26	AM23	SA_DQ26	SA_DQS4#	AN8	MA_DQS#4
MA_DQ27	AM22	SA_DQ27	SA_DQS5#	AM5	MA_DQS#5
MA_DQ28	AL23	SA_DQ28	SA_DQS6#	AH1	MA_DQS#6
MA_DQ29	AM24	SA_DQ29	SA_DQS7#	AE4	MA_DQS#7
MA_DQ30	AN22	SA_DQ30			
MA_DQ31	AP22	SA_DQ31	SA_MA0	AL17	MA_MA0
MA_DQ32	AM9	SA_DQ32	SA_MA1	AP17	MA_MA1
MA_DQ33	AL9	SA_DQ33	SA_MA2	AP18	MA_MA2
MA_DQ34	AL6	SA_DQ34	SA_MA3	AM17	MA_MA3
MA_DQ35	AP7	SA_DQ35	SA_MA4	AN18	MA_MA4
MA_DQ36	AP11	SA_DQ36	SA_MA5	AM18	MA_MA5
MA_DQ37	AP10	SA_DQ37	SA_MA6	AL19	MA_MA6
MA_DQ38	AL7	SA_DQ38	SA_MA7	AP20	MA_MA7
MA_DQ39	AM7	SA_DQ39	SA_MA8	AM19	MA_MA8
MA_DQ40	AN5	SA_DQ40	SA_MA9	AL20	MA_MA9
MA_DQ41	AN6	SA_DQ41	SA_MA10	AM16	MA_MA10
MA_DQ42	AN3	SA_DQ42	SA_MA11	AN20	MA_MA11
MA_DQ43	AP3	SA_DQ43	SA_MA12	AM20	MA_MA12
MA_DQ44	AP6	SA_DQ44	SA_MA13	AM15	MA_MA13
MA_DQ45	AM6	SA_DQ45			
MA_DQ46	AL4	SA_DQ46	SA_CAS#	AN15	MA_CAS# 【18,19】
MA_DQ47	AM3	SA_DQ47	SA_RAS#	AP16	MA_RAS# 【18,19】
MA_DQ48	AK2	SA_DQ48	SA_RCVENIN#	AF29	MA_RCVENIN# 1 Do Not Stuff 157
MA_DQ49	AK3	SA_DQ49	SA_RCVENOUT#	AF28	MA_RCVENOUT# 1 Do Not Stuff 158
MA_DQ50	AG2	SA_DQ50	SA_WE#	AP15	MA_WE# 【18,19】
MA_DQ51	AG1	SA_DQ51			
MA_DQ52	AL3	SA_DQ52			
MA_DQ53	AM2	SA_DQ53			
MA_DQ54	AH3	SA_DQ54			
MA_DQ55	AG3	SA_DQ55			
MA_DQ56	AF3	SA_DQ56			
MA_DQ57	AE3	SA_DQ57			
MA_DQ58	AD6	SA_DQ58			
MA_DQ59	AC4	SA_DQ59			
MA_DQ60	AF2	SA_DQ60			
MA_DQ61	AF1	SA_DQ61			
MA_DQ62	AD4	SA_DQ62			
MA_DQ63	AD5	SA_DQ63			

NQ82915PM

U1C

DDR SYSTEM MEMORY B

AE31	SB_DQ0	SB_BS0	AJ15	
AE32	SB_DQ1	SB_BS1	AG17	
AG32	SB_DQ2	SB_BS2	AG21	
AG36	SB_DQ3			
AE34	SB_DQ4	SB_DM0	AF32	
AE33	SB_DQ5	SB_DM1	AK34	
AF31	SB_DQ6	SB_DM2	AK27	
AF30	SB_DQ7	SB_DM3	AK24	
AH33	SB_DQ8	SB_DM4	AJ10	
AH32	SB_DQ9	SB_DM5	AK5	
AK31	SB_DQ10	SB_DM6	AE7	
AG30	SB_DQ11	SB_DM7	AB7	
AG34	SB_DQ12			
AG33	SB_DQ13	SB_DQS0	AF34	
AH31	SB_DQ14	SB_DQS1	AK32	
AJ31	SB_DQ15	SB_DQS2	AJ28	
AK30	SB_DQ16	SB_DQS3	AK23	
AJ30	SB_DQ17	SB_DQS4	AM10	
AH29	SB_DQ18	SB_DQS5	AH6	
AH28	SB_DQ19	SB_DQS6	AF8	
AK29	SB_DQ20	SB_DQS7	AB4	
AH30	SB_DQ21			
AH27	SB_DQ22	SB_DQS0#	AF35	
AG28	SB_DQ23	SB_DQS1#	AK33	
AF24	SB_DQ24	SB_DQS2#	AK28	
AG23	SB_DQ25	SB_DQS3#	AJ23	
AJ22	SB_DQ26	SB_DQS4#	AL10	
AK22	SB_DQ27	SB_DQS5#	AH7	
AH24	SB_DQ28	SB_DQS6#	AF7	
AH23	SB_DQ29	SB_DQS7#	AB5	
AG22	SB_DQ30			
AJ21	SB_DQ31	SB_MA0	AH17	
AG10	SB_DQ32	SB_MA1	AK17	
AG9	SB_DQ33	SB_MA2	AH18	
AG8	SB_DQ34	SB_MA3	AJ18	
AH8	SB_DQ35	SB_MA4	AK18	
AH11	SB_DQ36	SB_MA5	AJ19	
AH10	SB_DQ37	SB_MA6	AK19	
AJ9	SB_DQ38	SB_MA7	AH19	
AK9	SB_DQ39	SB_MA8	AJ20	
AJ7	SB_DQ40	SB_MA9	AH20	
AK6	SB_DQ41	SB_MA10	AJ16	
AJ4	SB_DQ42	SB_MA11	AG18	
AH5	SB_DQ43	SB_MA12	AG20	
AK8	SB_DQ44	SB_MA13	AG15	
AJ8	SB_DQ45			
AJ5	SB_DQ46	SB_CAS#	AH14	
AK4	SB_DQ47	SB_RAS#	AK14	
AG5	SB_DQ48	SB_RCVENIN#	AF15	
AG4	SB_DQ49	SB_RCVENOUT#	AF14	
AD8	SB_DQ50	SB_WE#	AH16	
AD9	SB_DQ51			
AH4	SB_DQ52			
AG6	SB_DQ53			
AF8	SB_DQ54			
AD7	SB_DQ55			
AC5	SB_DQ56			
AB8	SB_DQ57			
AB6	SB_DQ58			
AA8	SB_DQ59			
AC8	SB_DQ60			
AC7	SB_DQ61			
AA4	SB_DQ62			
AA5	SB_DQ63			

NQ82915PM

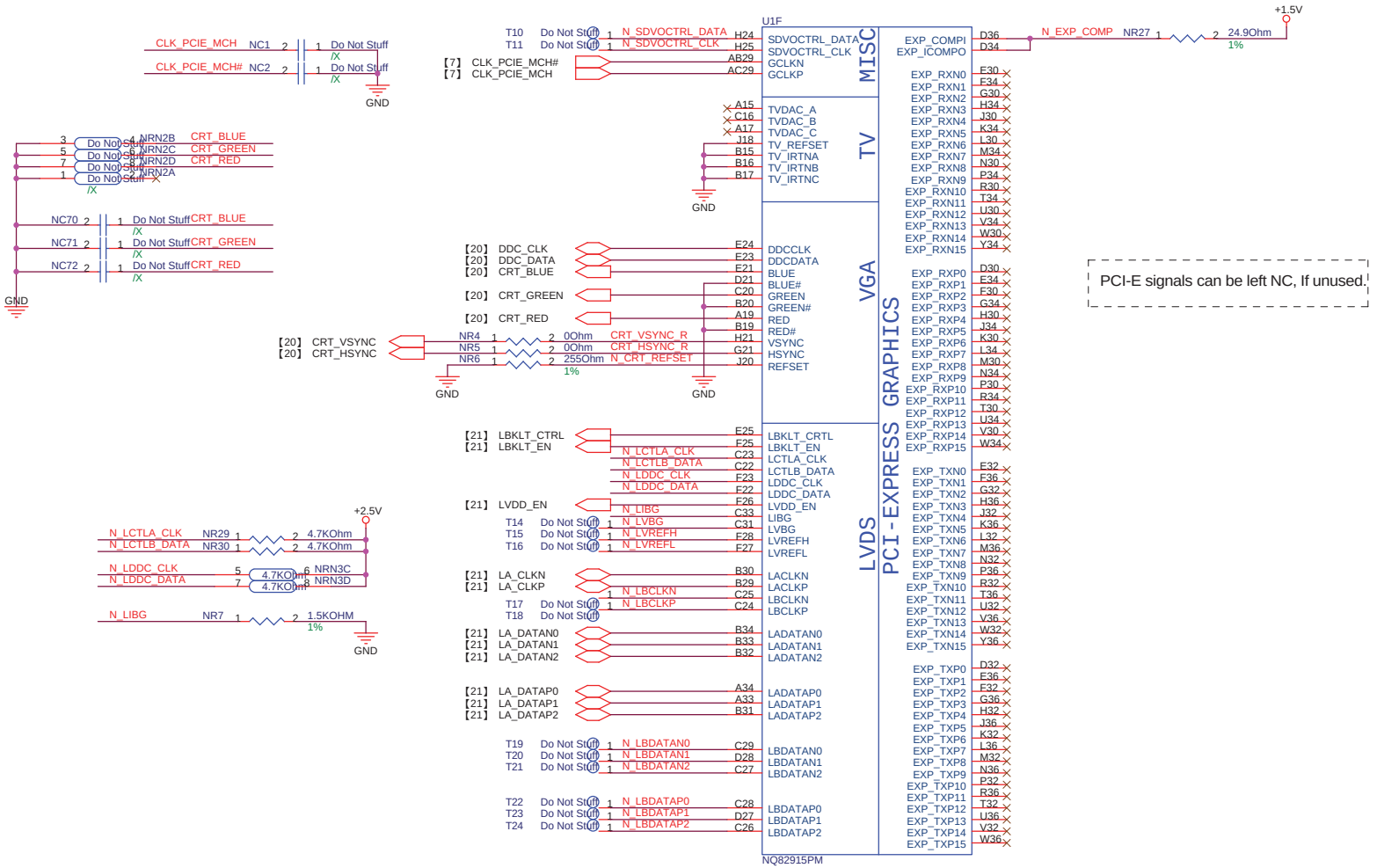
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : 910GML_DRAM	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 11 of 47	

SDVO SMbus have internal pull down

SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

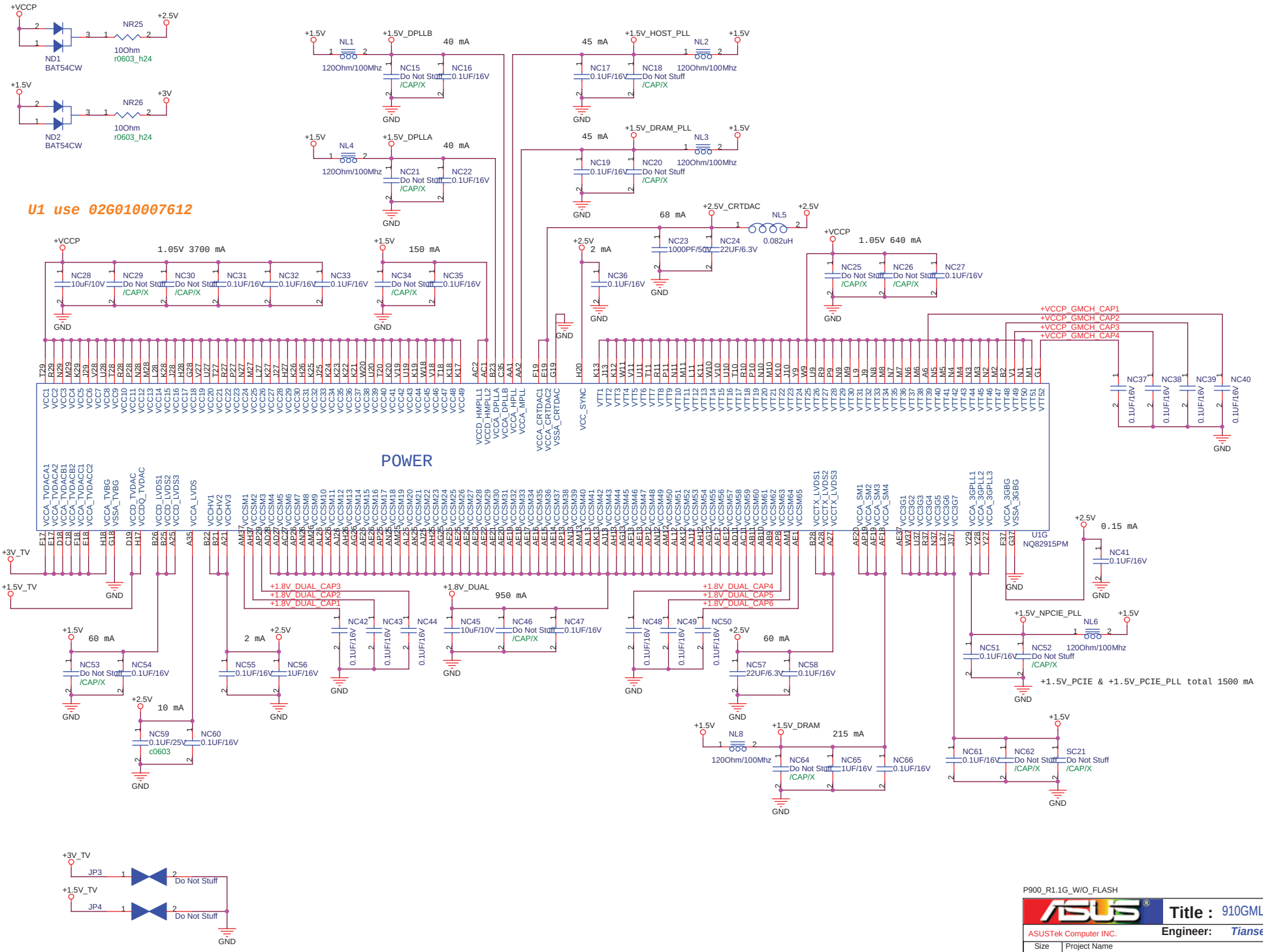
U1 use 02G010007612



PCI-E signals can be left NC, If unused.

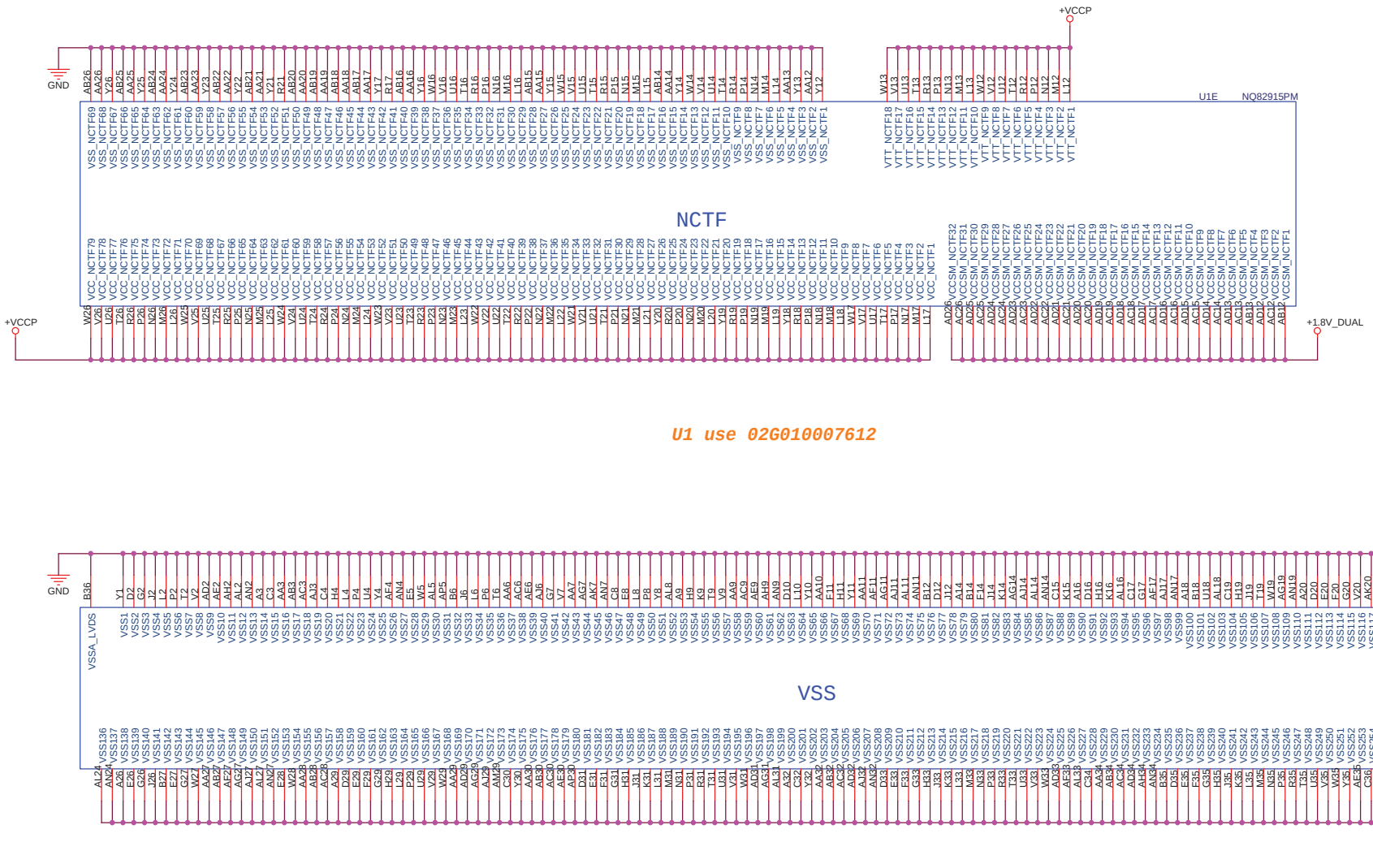
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : 910GML_VGA_LVDS	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 12 of 47	



P900_R1.1G_W/O_FLASH

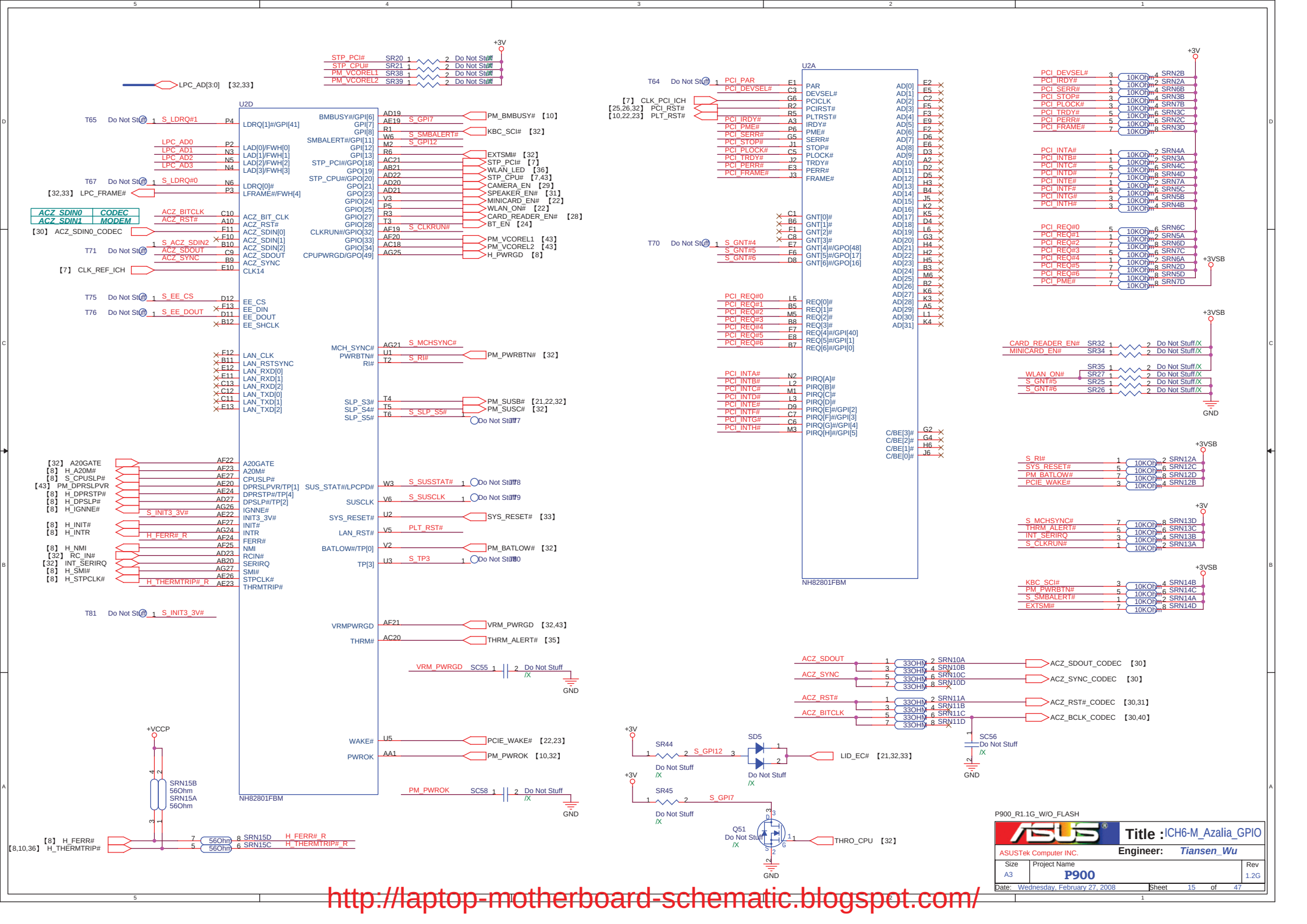
ASUSTek Computer INC.	Title : 910GML_PWR	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 13 of 47	

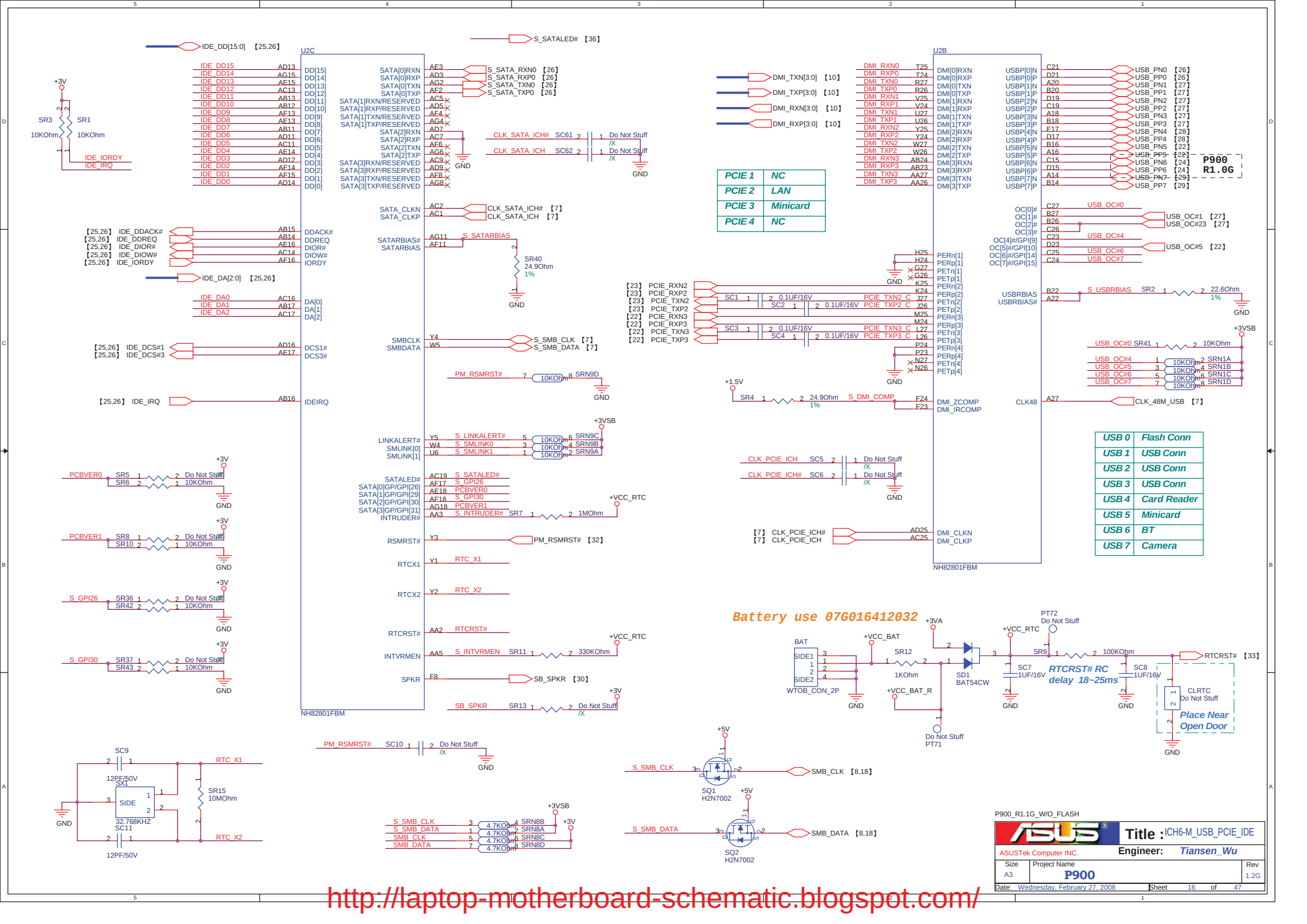


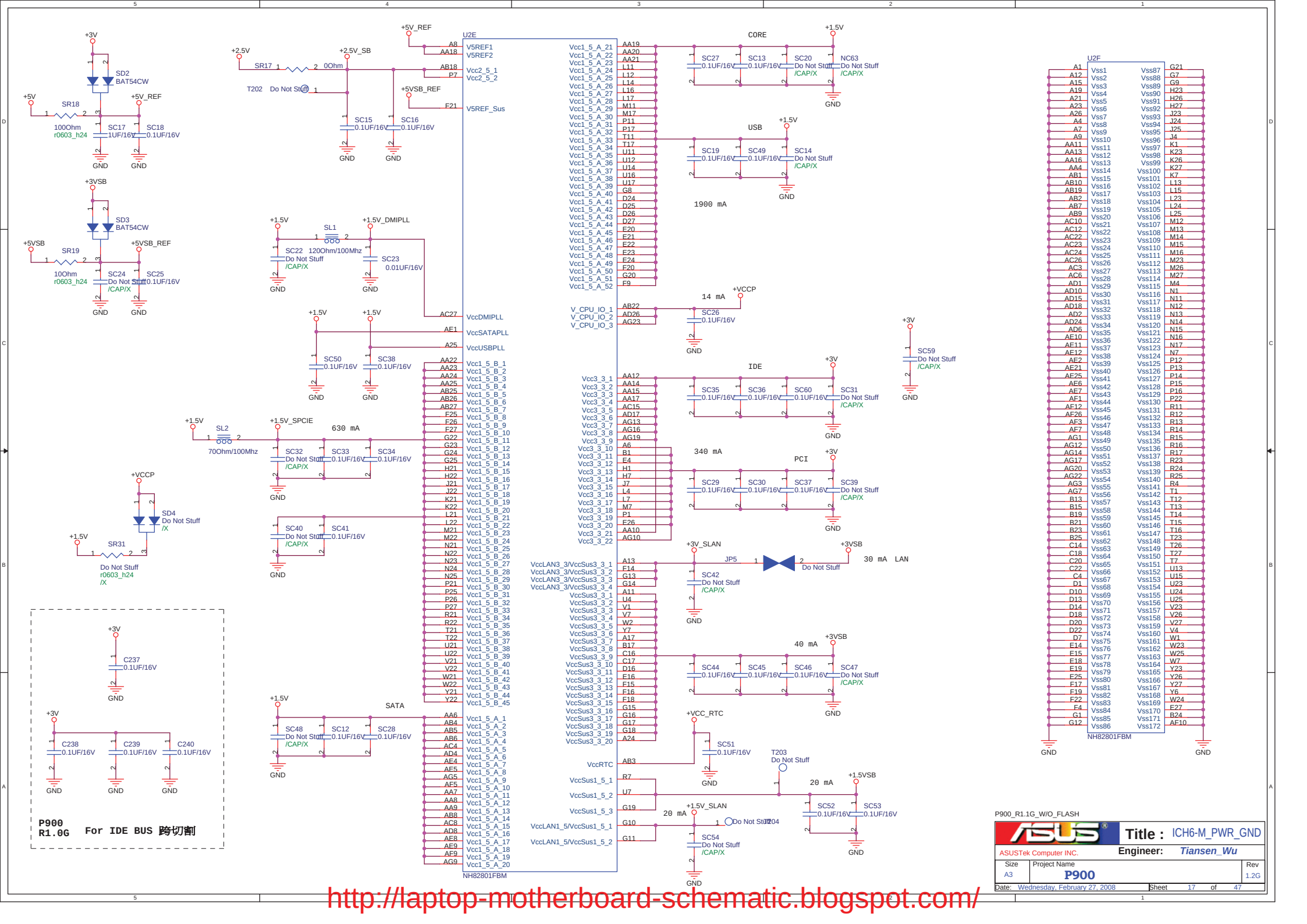
U1 use 02G010007612

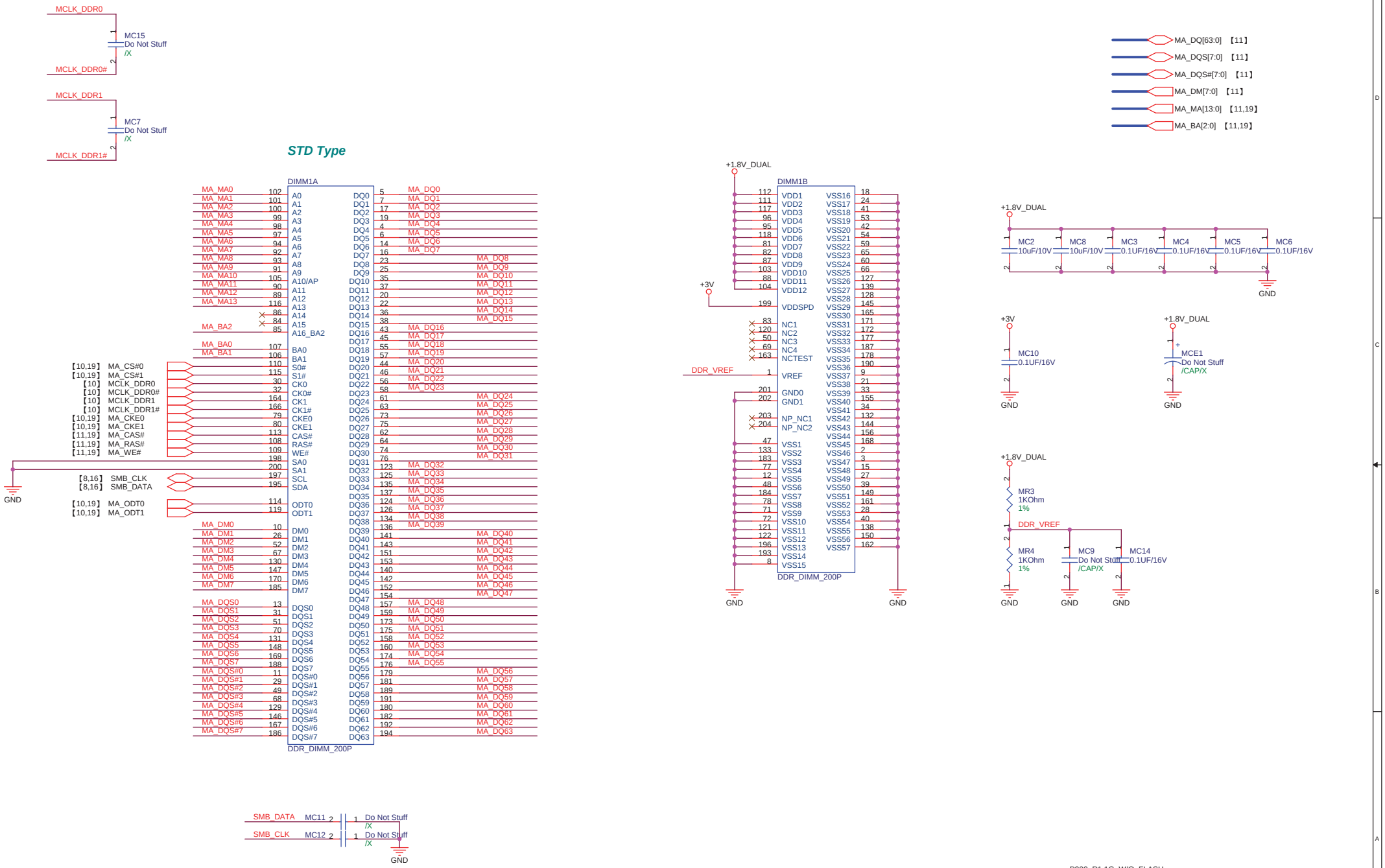
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : 910GML_GND	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 14 of 47	



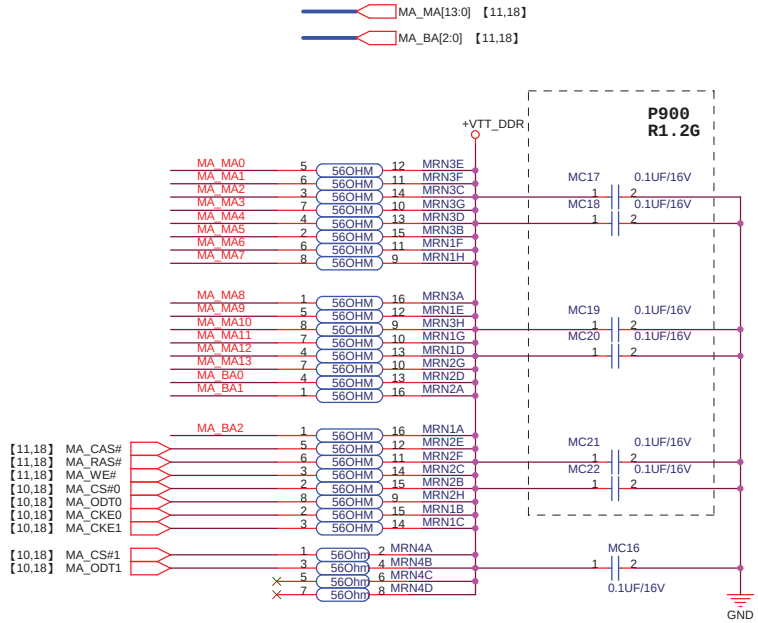

U2C
NH82801FBM
U2B
NH82801FBM
IDE_DD[15:0] 【25,26】
S_SATALED# 【36】
DMI_TXN[3:0] 【10】
DMI_TXP[3:0] 【10】
DMI_RXN[3:0] 【10】
DMI_RXP[3:0] 【10】
PCIE 1 NC
PCIE 2 LAN
PCIE 3 Minicard
PCIE 4 NC
USB 0 Flash Conn
USB 1 USB Conn
USB 2 USB Conn
USB 3 USB Conn
USB 4 Card Reader
USB 5 Minicard
USB 6 BT
USB 7 Camera
P900
R1.0G
Battery use 07G016412032
RTCRST# RC delay 18~25ms
Place Near Open Door
Do Not Stuff
10KOhm
1%
GND
+3V
+3VSB
+1.5V
+3VA
+VCC_RTC
+VCC_BAT
+5V
ASUSTek Computer INC.
Title : ICH6-M_USB_PCIE_IDE
Engineer: Tiansen_Wu
Size A3
Project Name P900
Rev 1.2G
Date: Wednesday, February 27, 2008
Sheet 16 of 47
P900_R1.1G_W/O_FLASH
http://laptop-motherboard-schematic.blogspot.com/





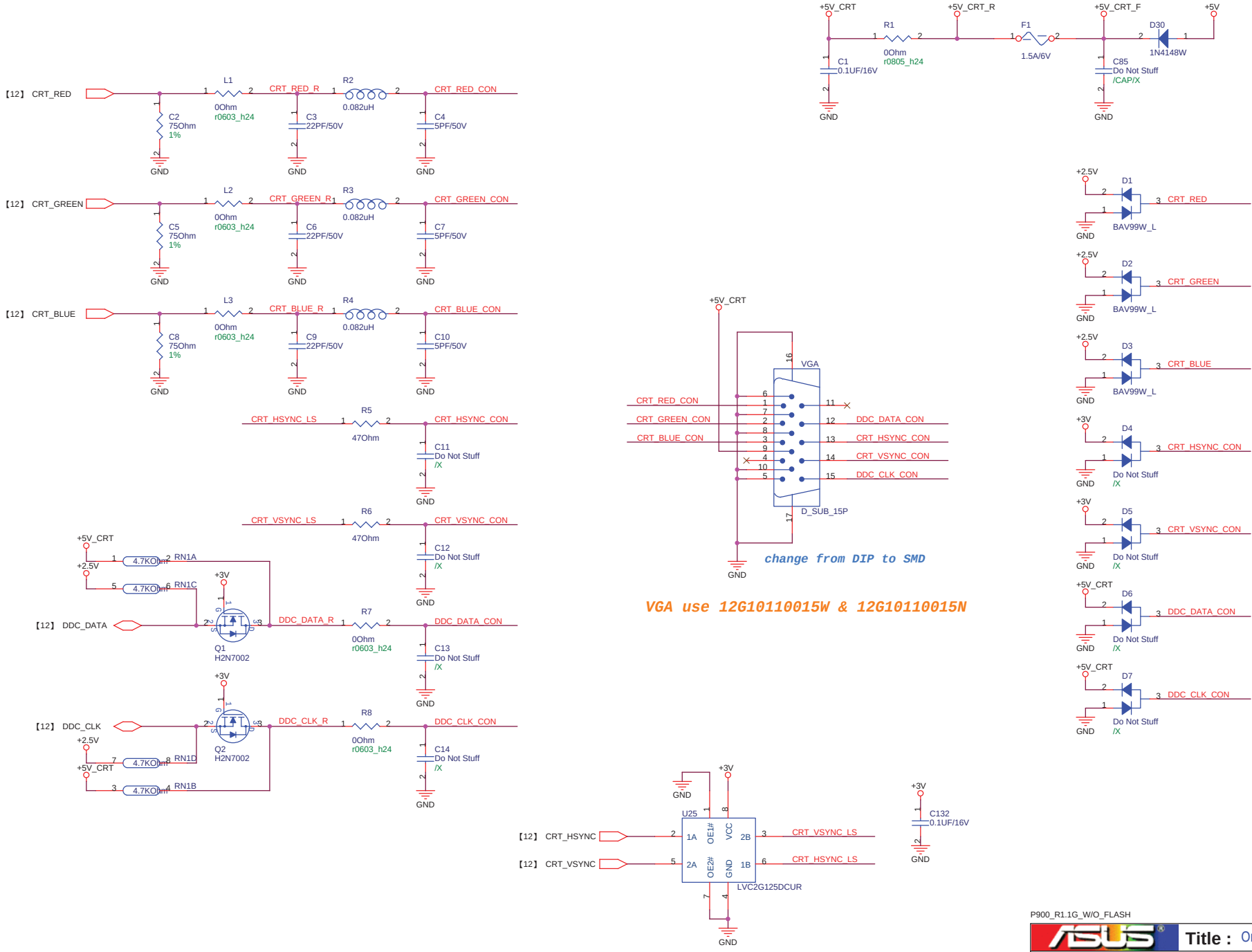
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 18 of 47	



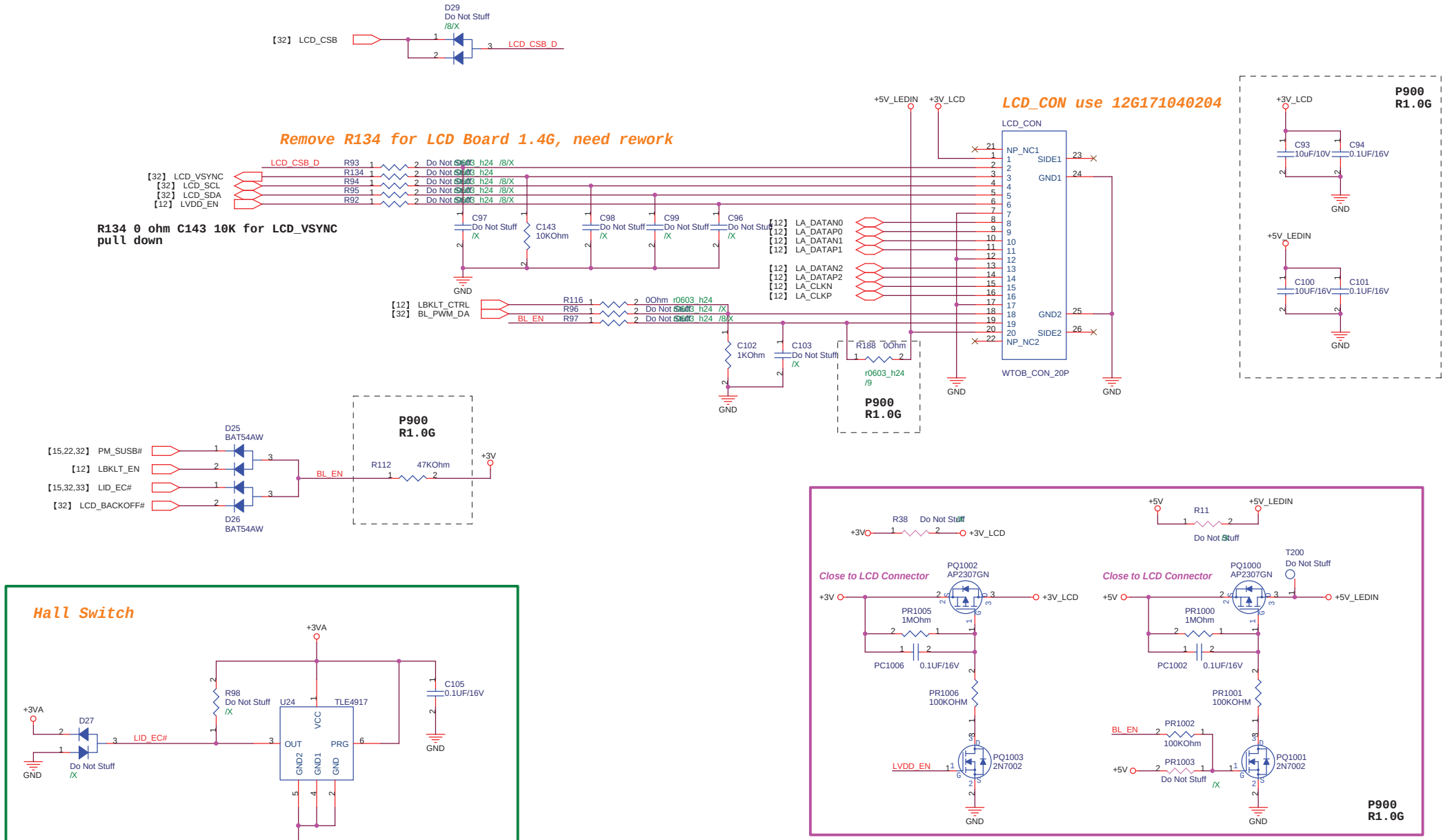
P900_R1.1G_W/O_FLASH

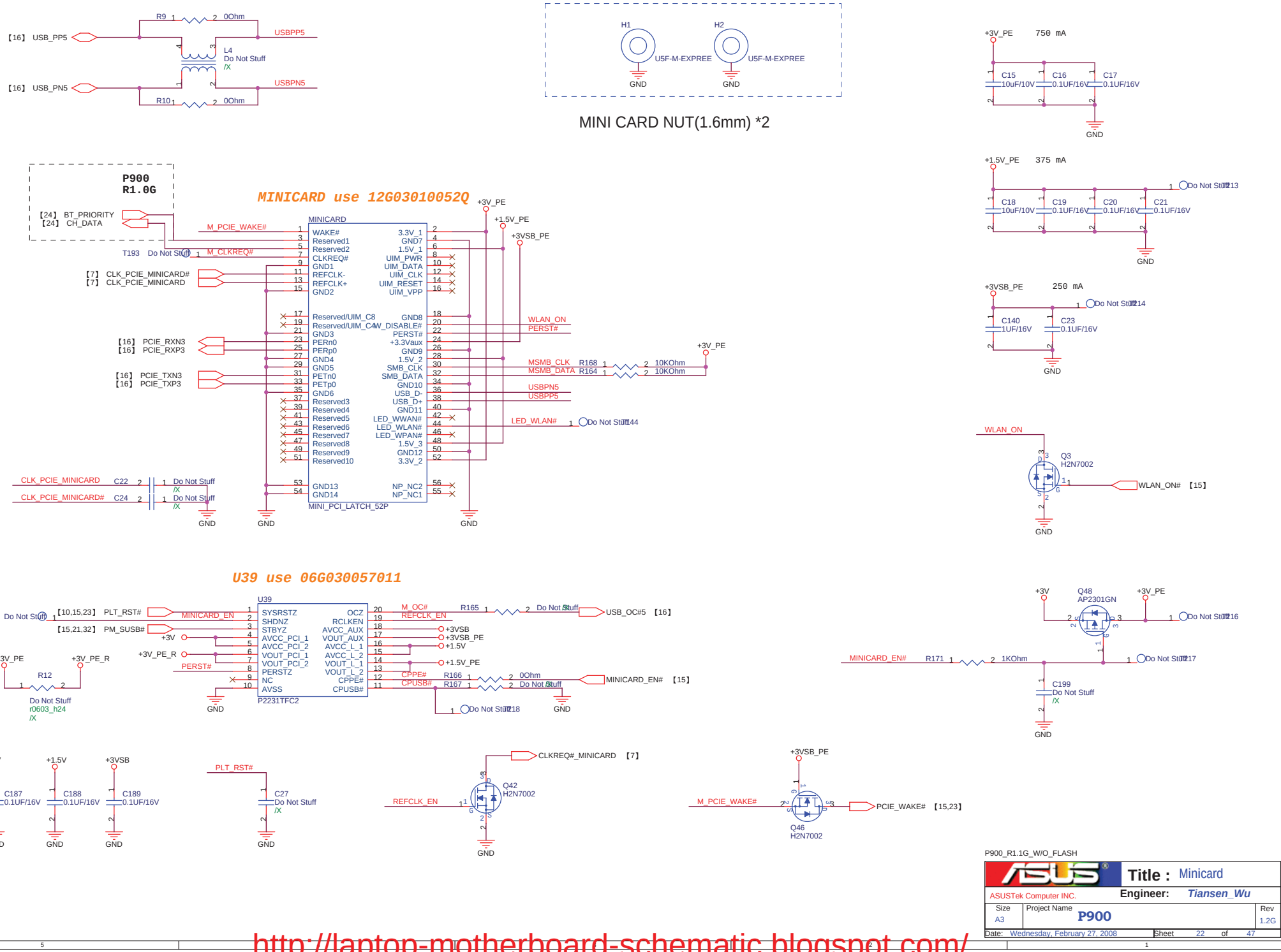
ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Tiansen_Wu*	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 19 of 47	

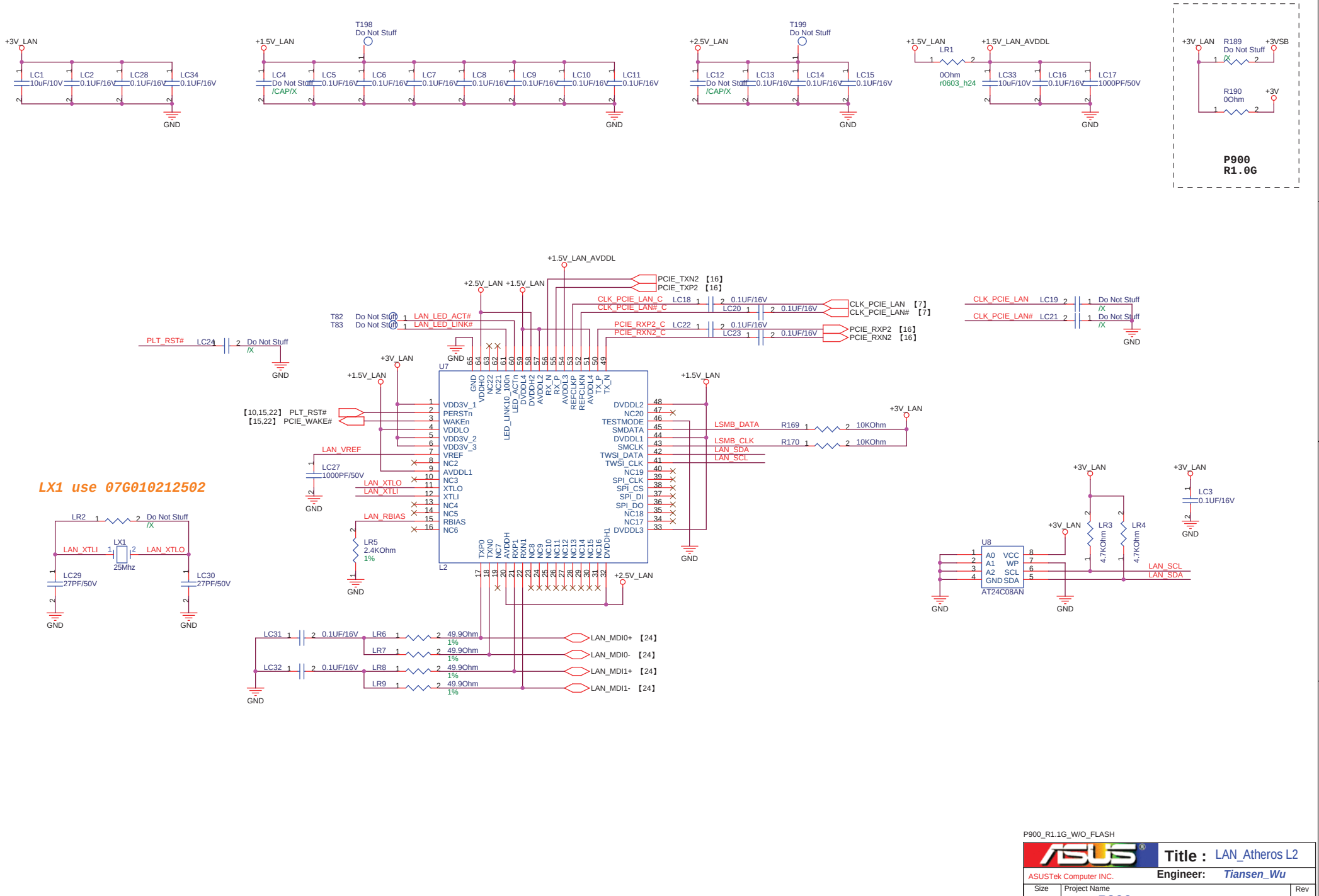


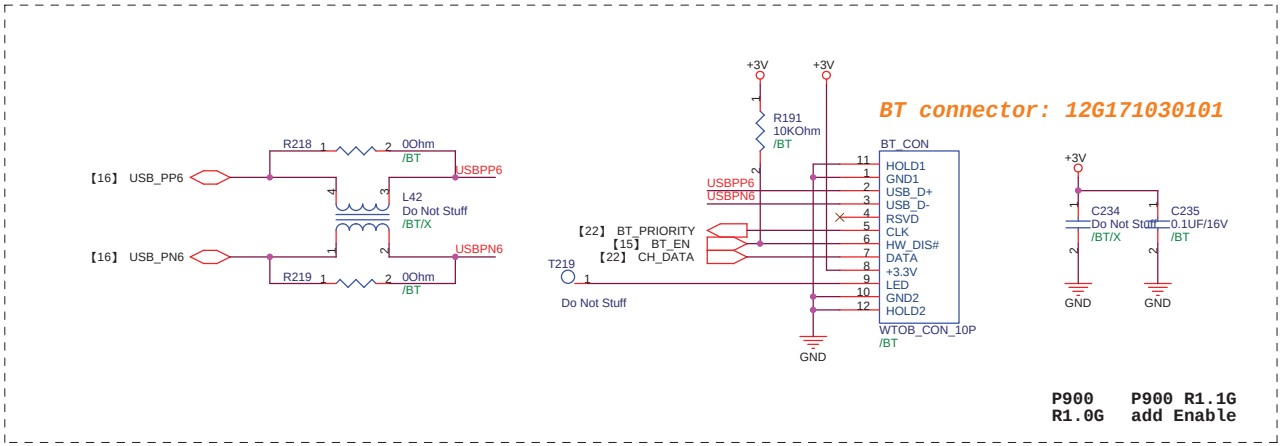
P900_R1.1G_W/O_FLASH

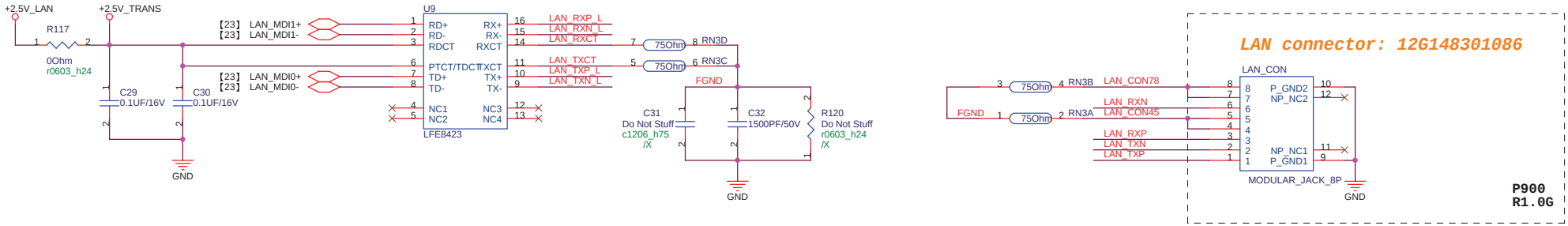
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 20 of 47	

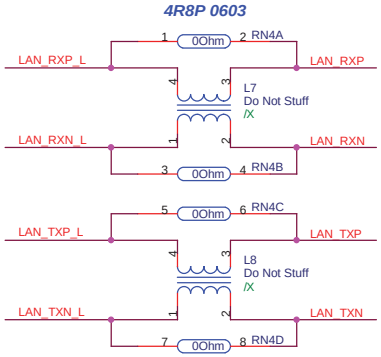












P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : RJ45/BlueTooth	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 24 of 47	

P900
R1.0G

U36: USE 02G113000302

Un-used address Bus

For Toshiba

CSEL#
H: Slave
L: Master

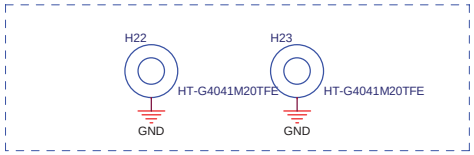
1. 1CE :R203
2. 2CE :R203,R210

Near to Flash VCC1 PIN

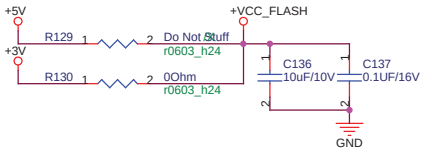
Flash

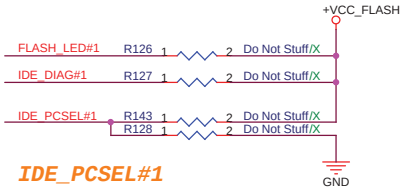
P900_R1.1G_W/O_FLASH

Title : Onboard Flash
ASUSTek Computer INC.
Engineer: Tiansen_Wu
Size: Custom | Project Name: P900 | Rev: 1.2G
Date: Wednesday, February 27, 2008 | Sheet 25 of 47

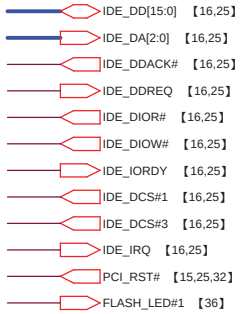


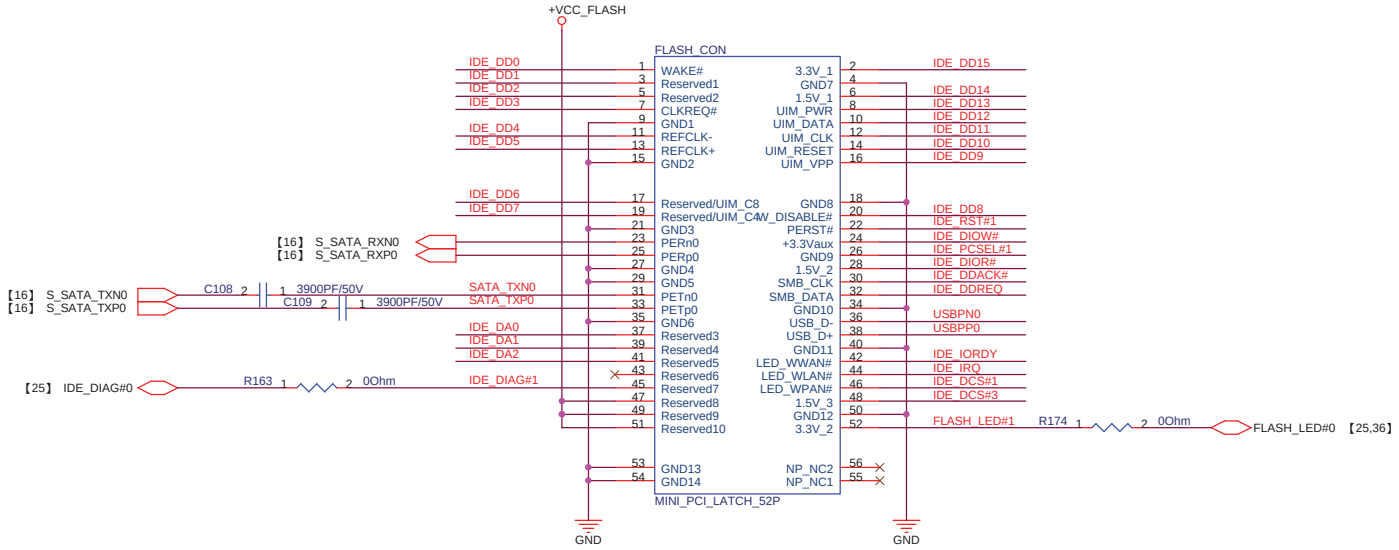
FLASH CARD NUT(3.3mm) *2

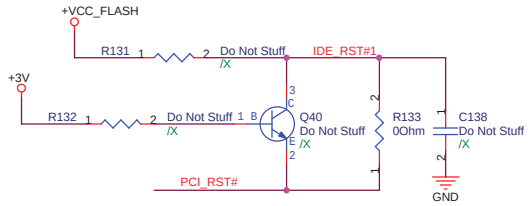


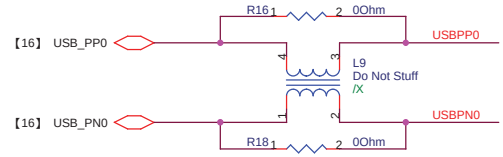


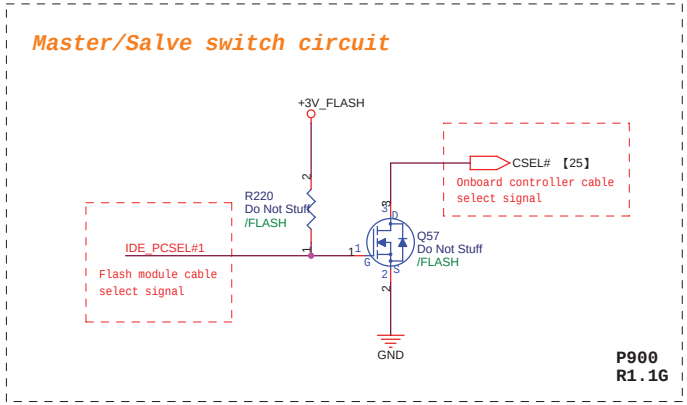
IDE_PCSEL#1
H: Slave
L: Master





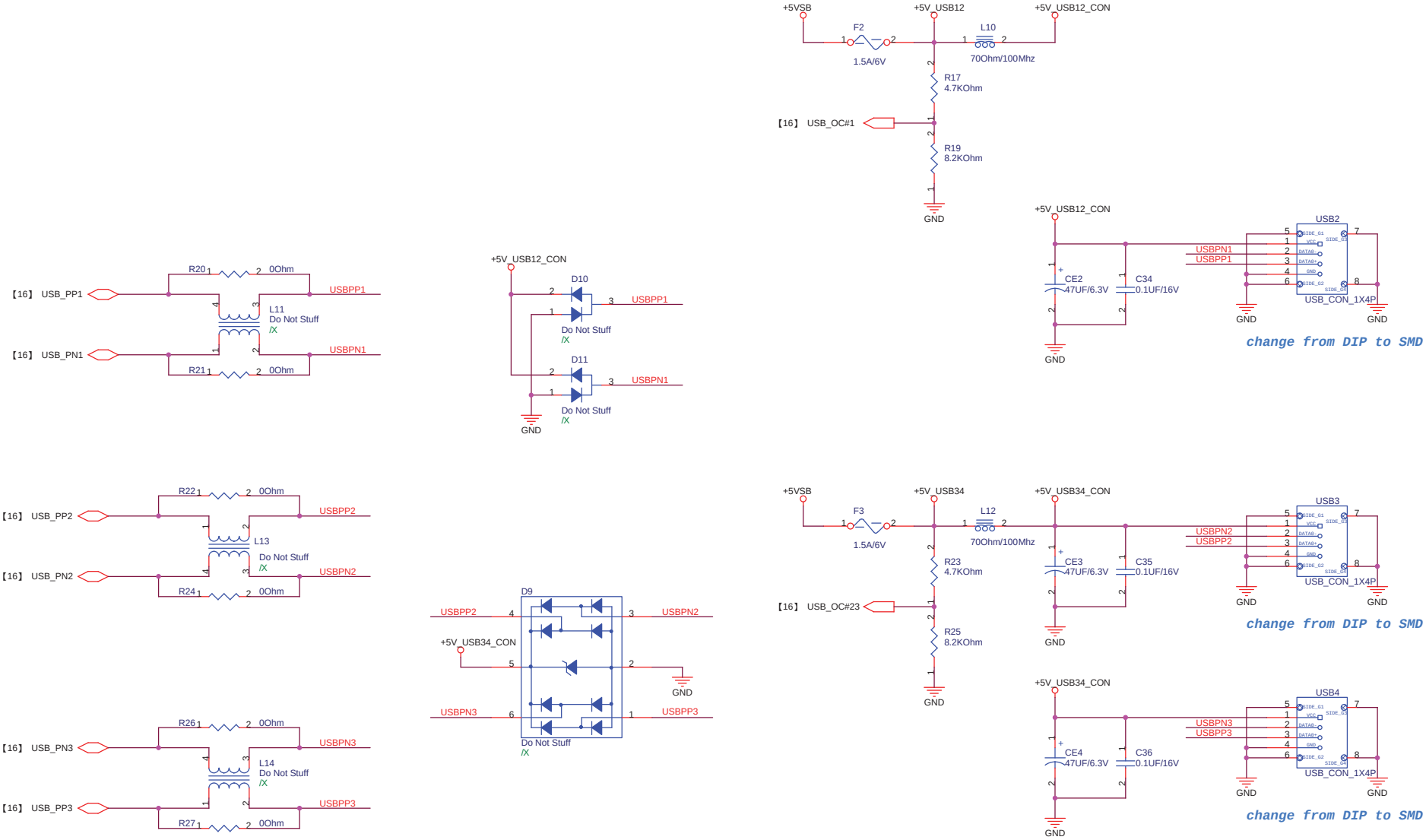






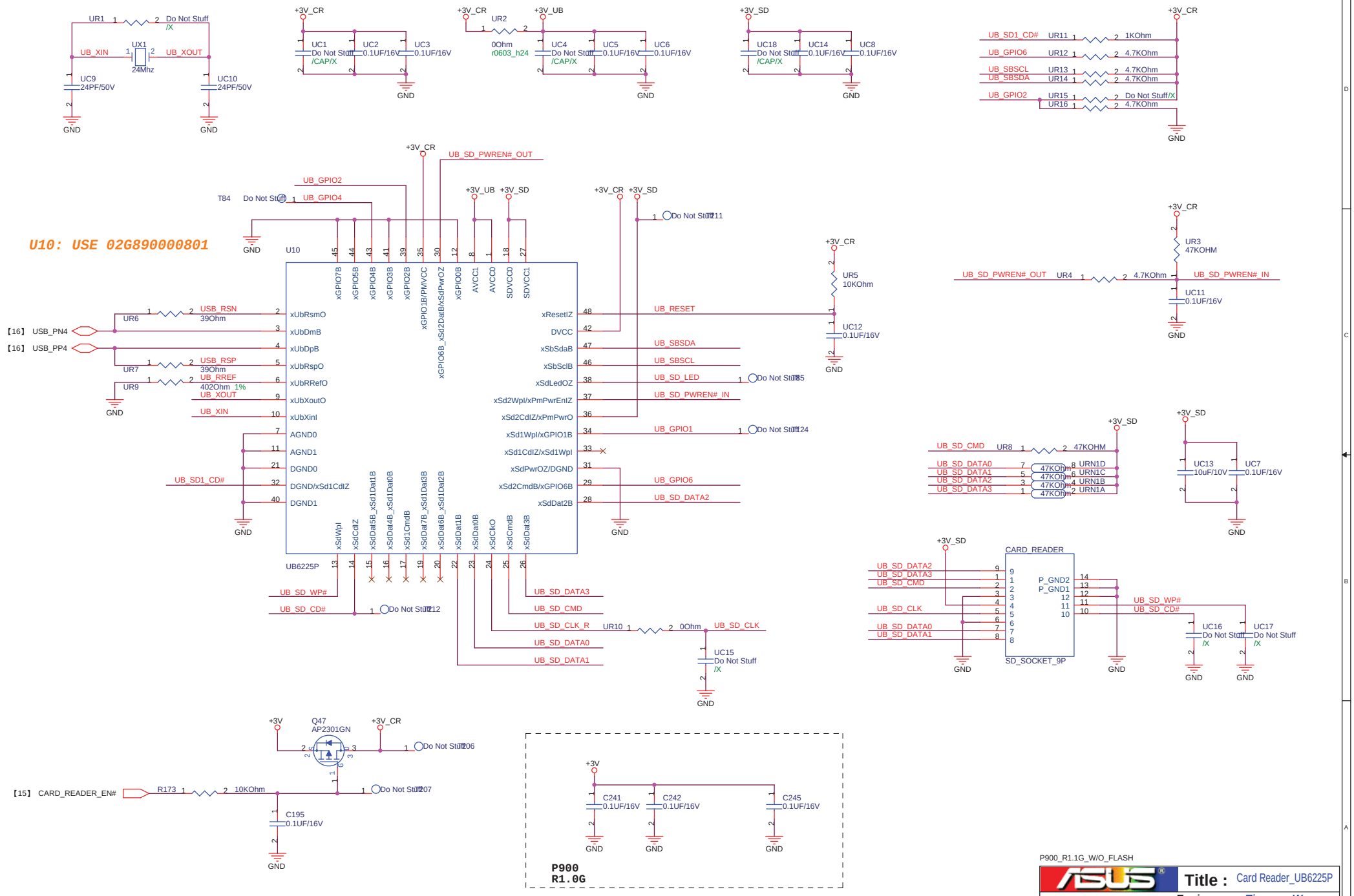
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Flash Conn	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 26 of 47	



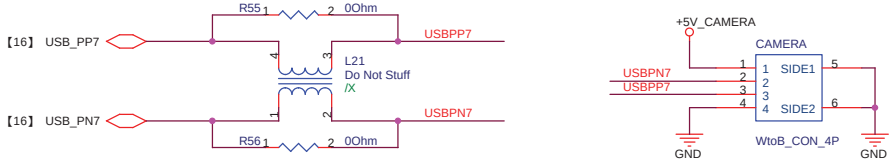
P900_R1.1G_W/O_FLASH

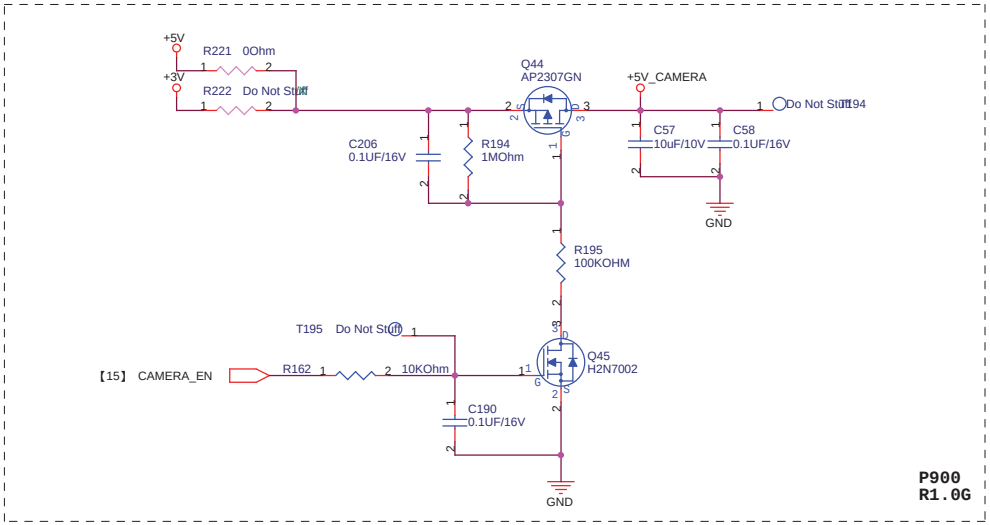
ASUSTek Computer INC.	Title : USB Port	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 27 of 47	



P900_R1.1G_W/O_FLASH

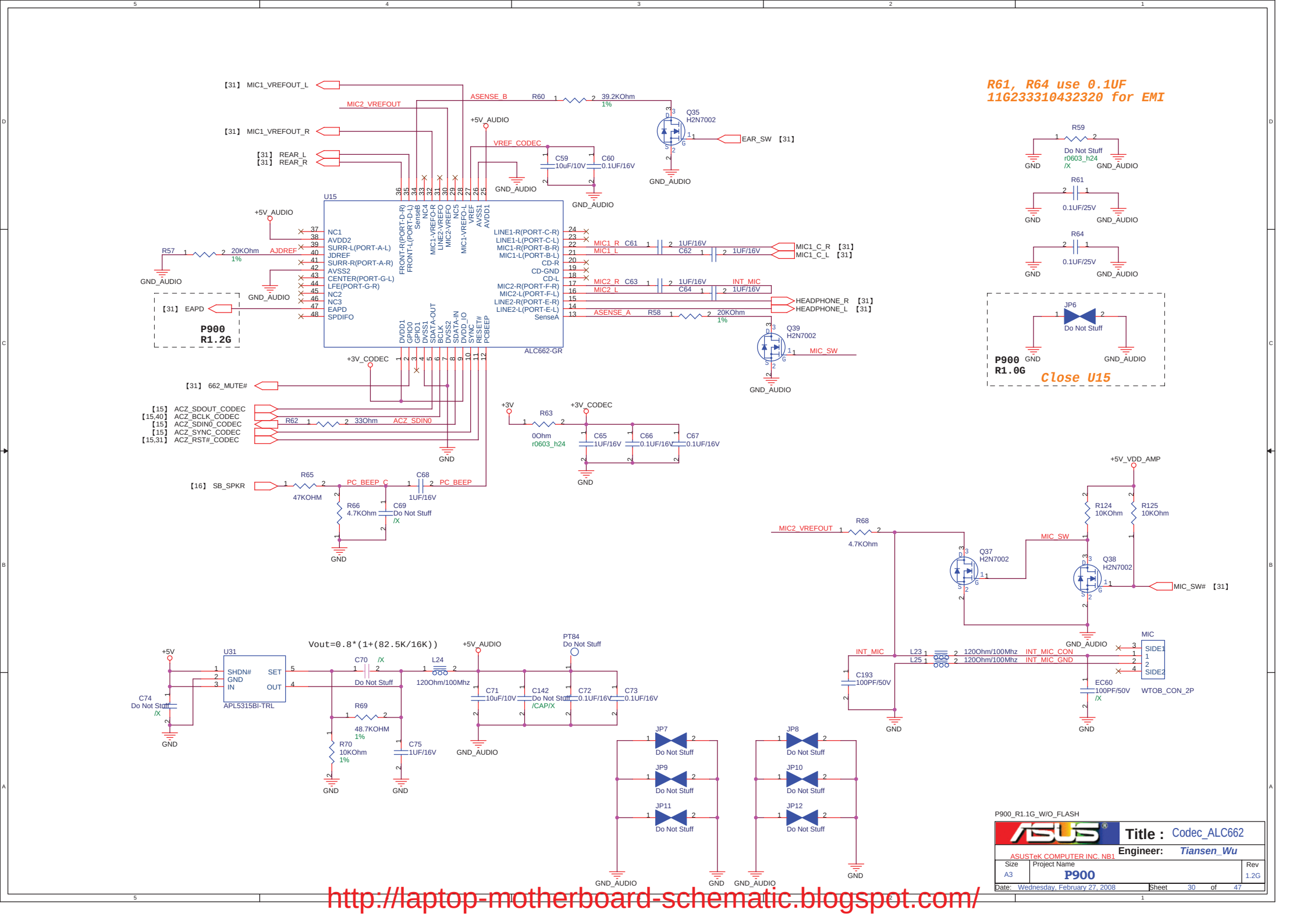
ASUSTek Computer INC.	Title : Card Reader_UB6225P	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 28 of 47	

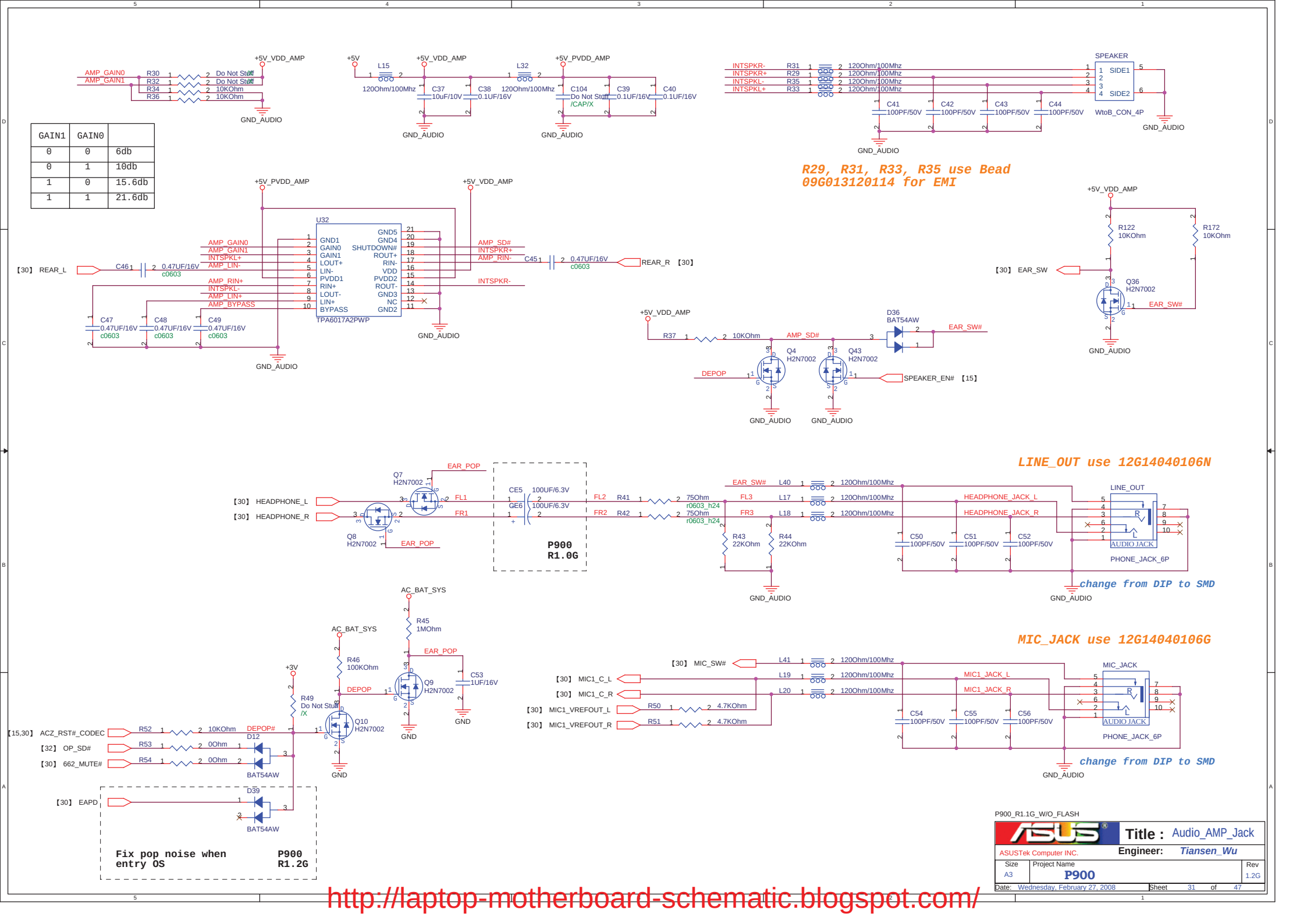


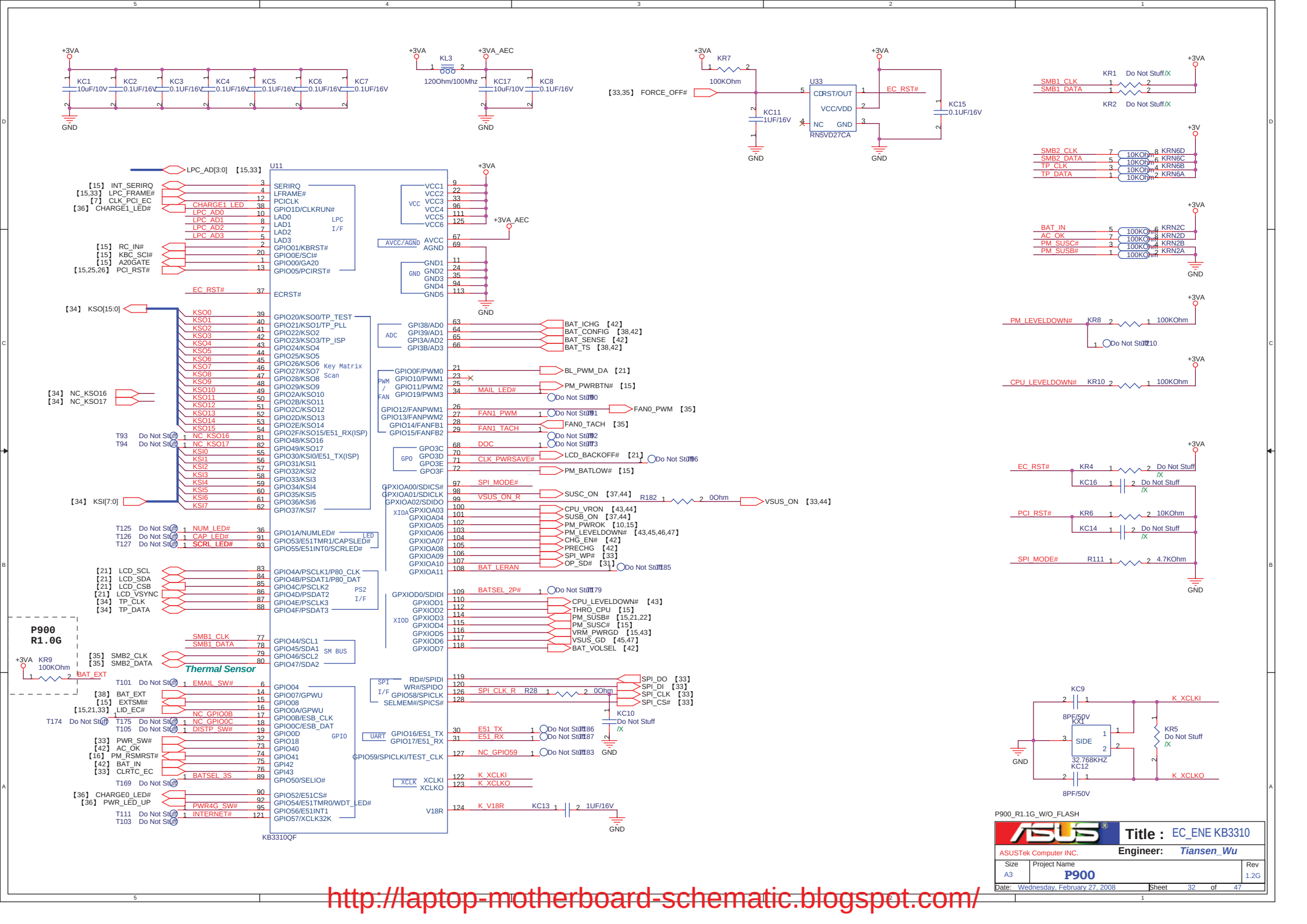


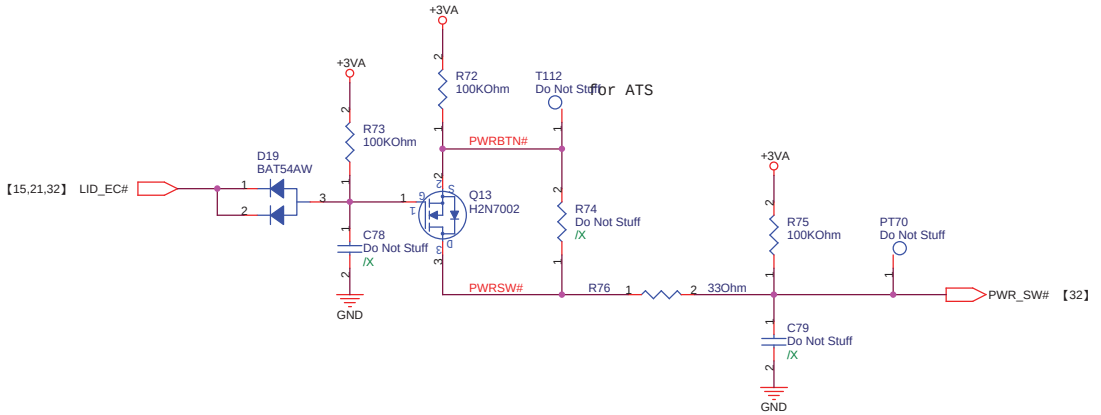
P900_R1.1G_W/O_FLASH

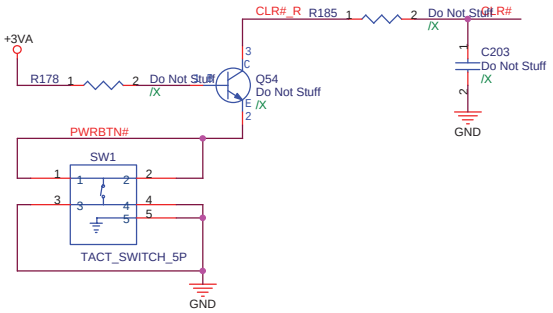
ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 29 of 47	

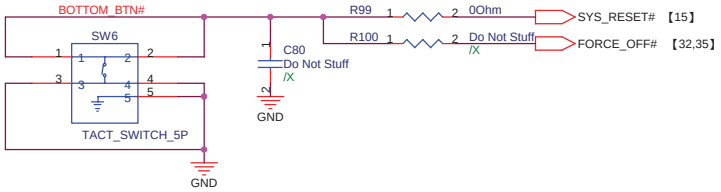


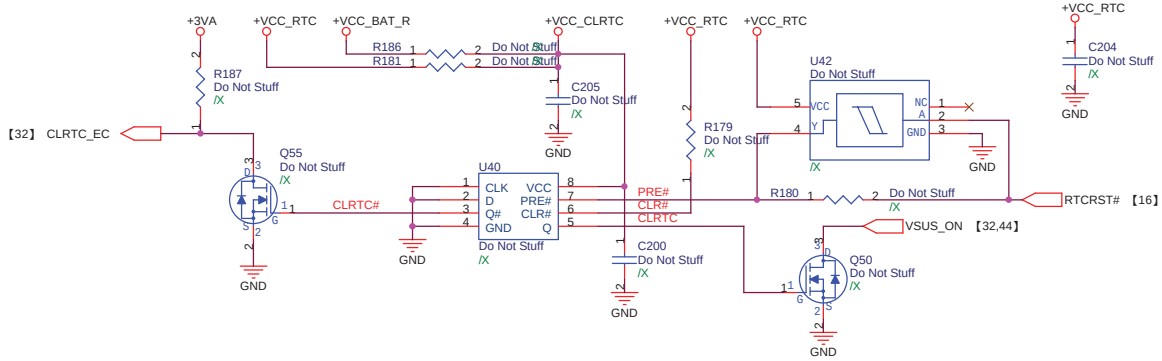


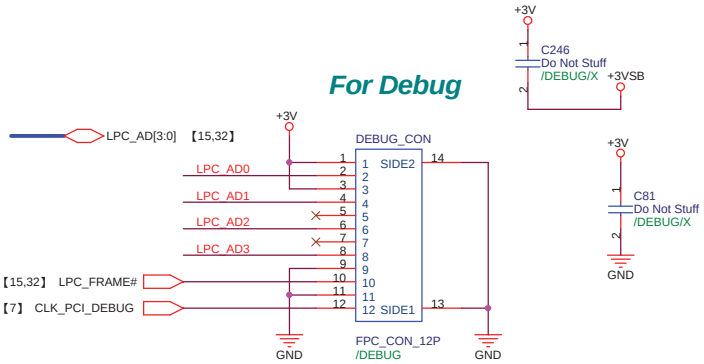


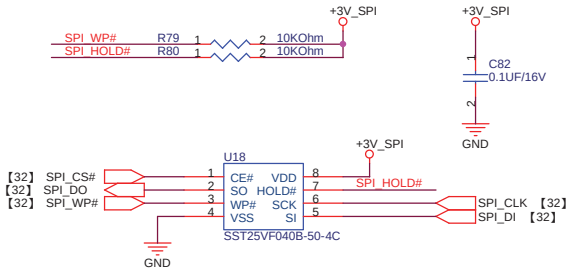


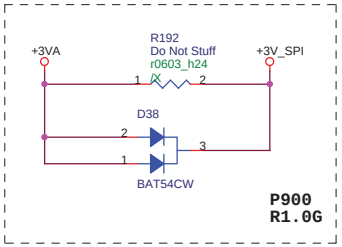












Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125

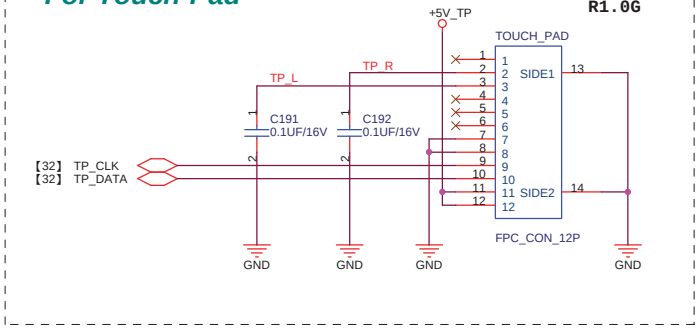
U18 use 05G001002900 & 05G00100F130

P900_R1.1G_W/O_FLASH

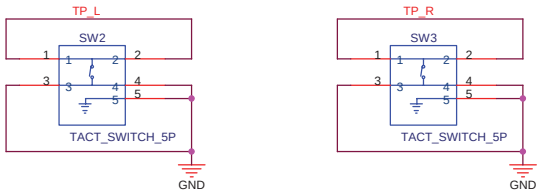
ASUSTek Computer INC.	Title : Switch_SPI ROM_Debug	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 33 of 47	

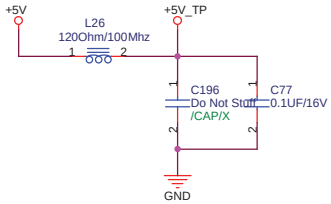
For Touch-Pad

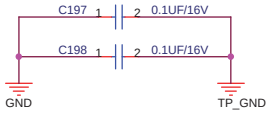
P900
R1.0G

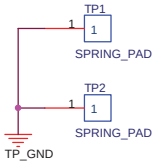


SW2, SW3 use 12G09103305N

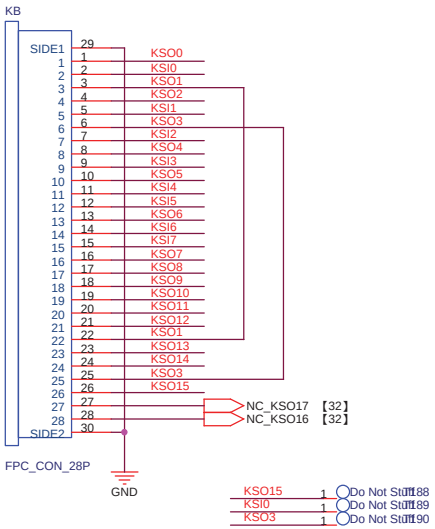


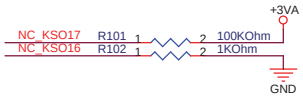


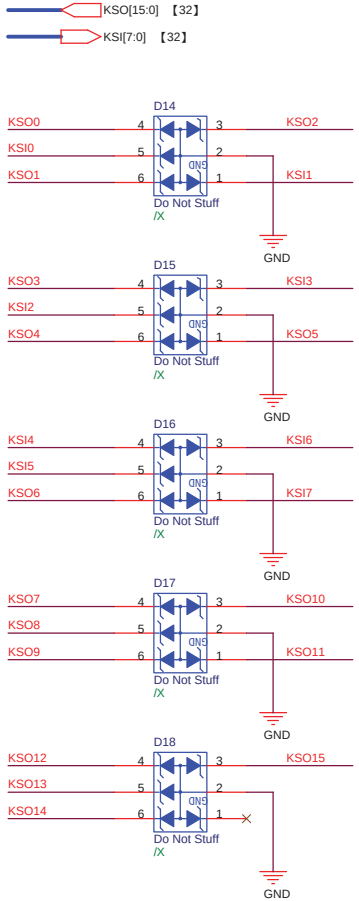




For Keyboard

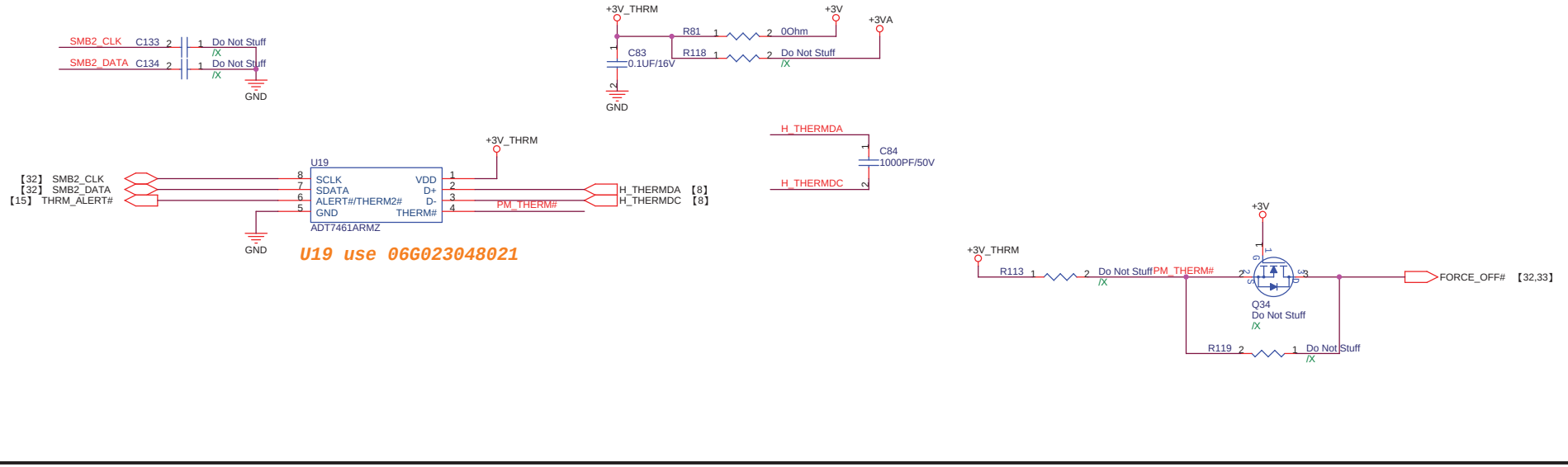


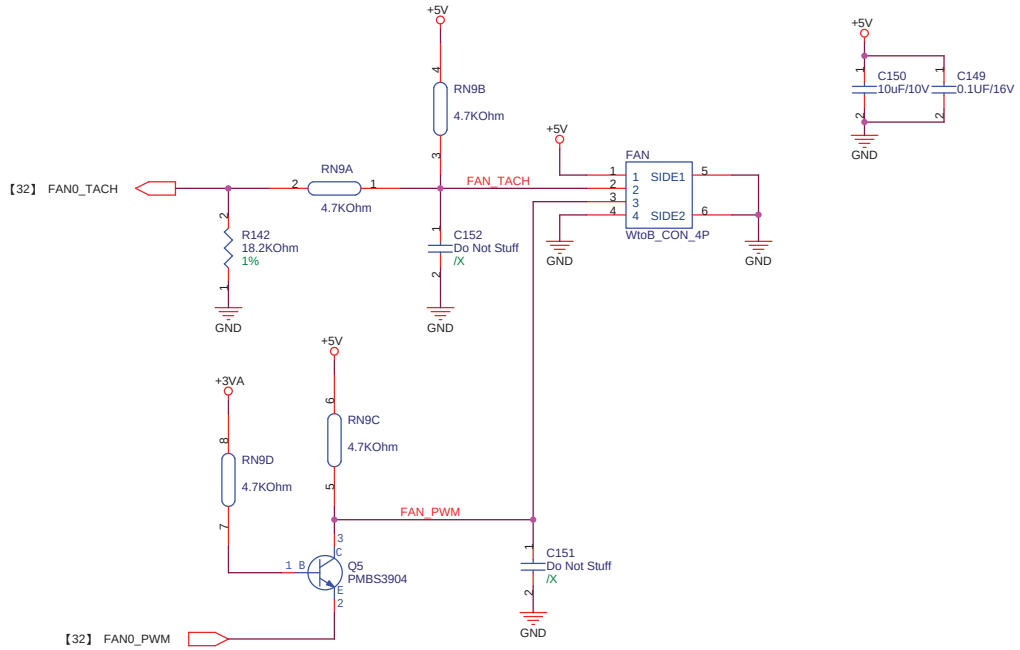




P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 34 of 47	

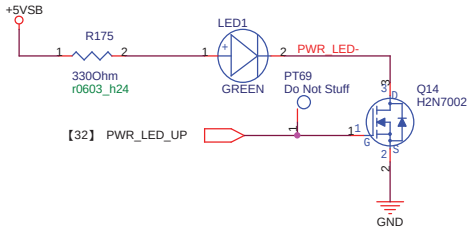




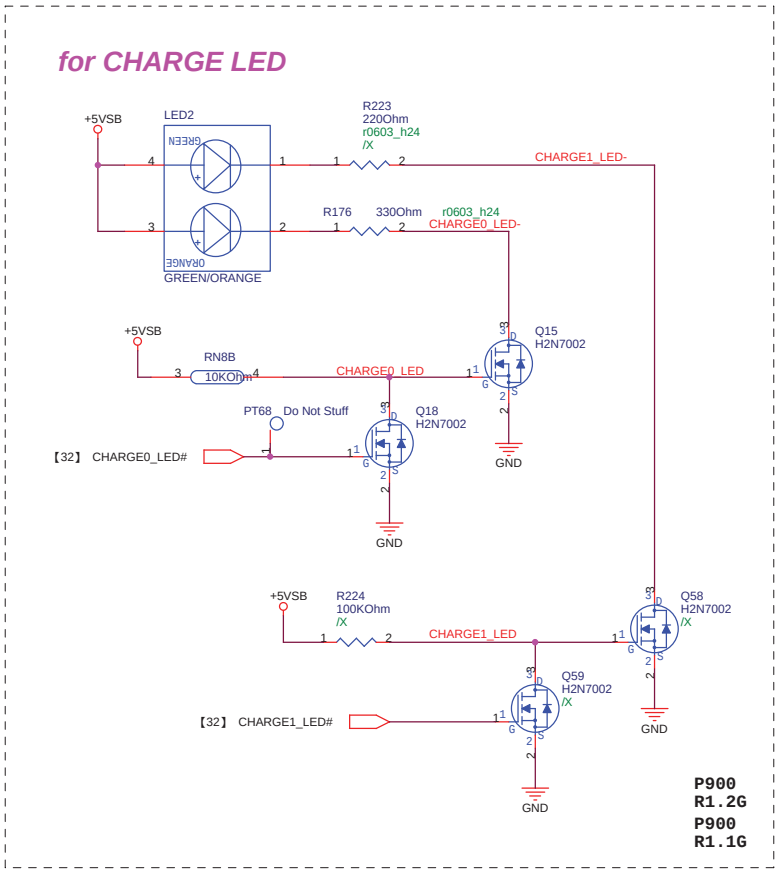
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 35 of 47	

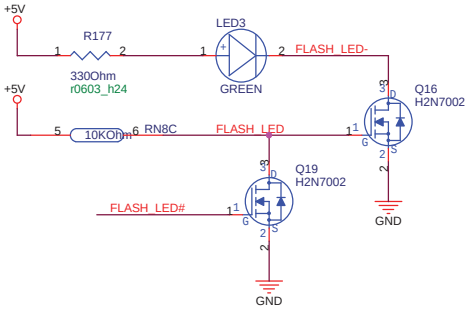
for POWER LED



for CHARGE LED

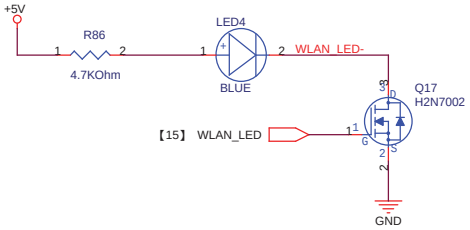


for FLASH LED

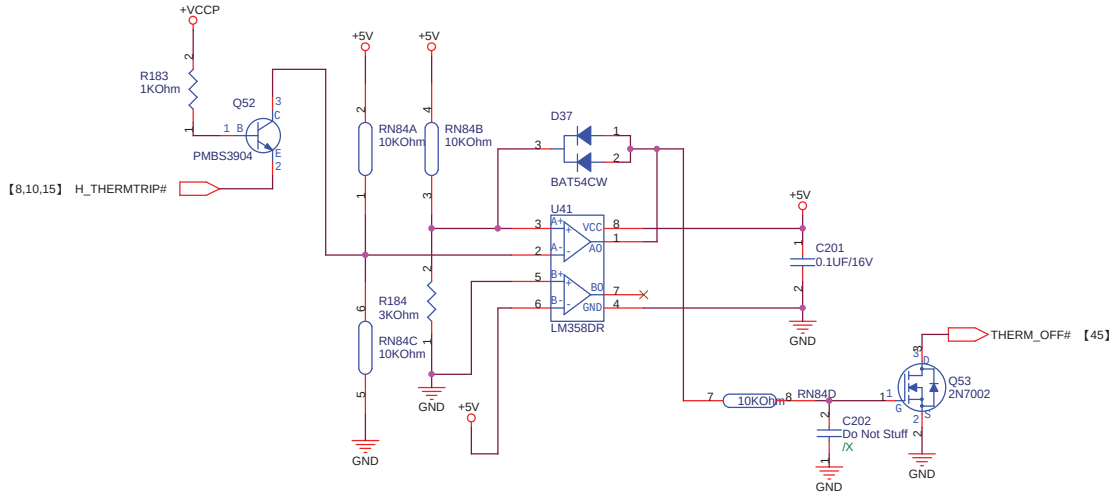


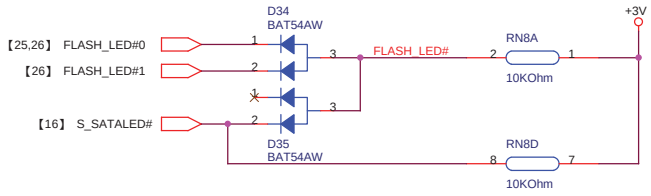
for WLAN LED

R86 use 4.7K OHm 10G213472003030



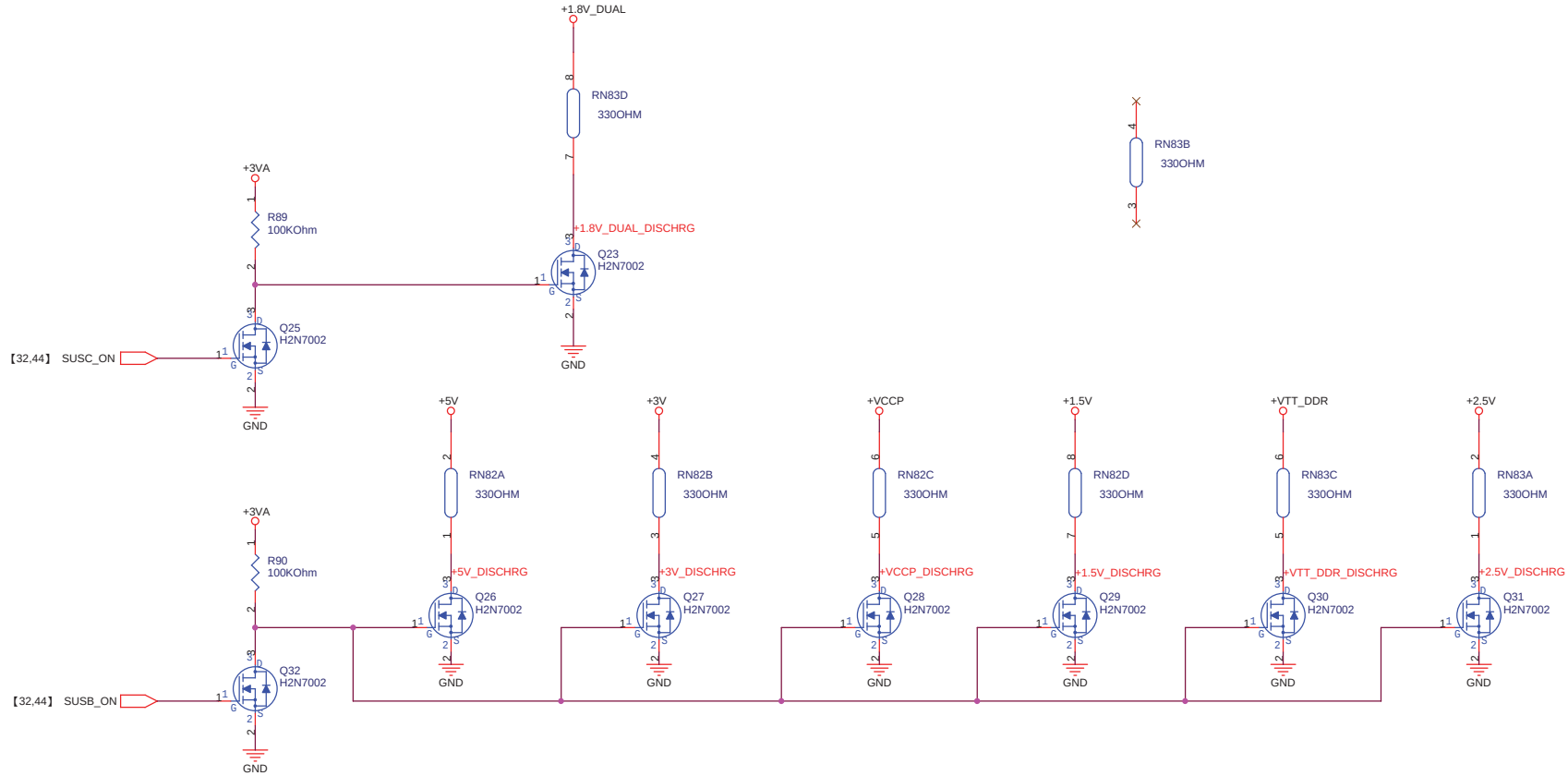
For THERMTRIP





P900_R1.1G_W/O_FLASH

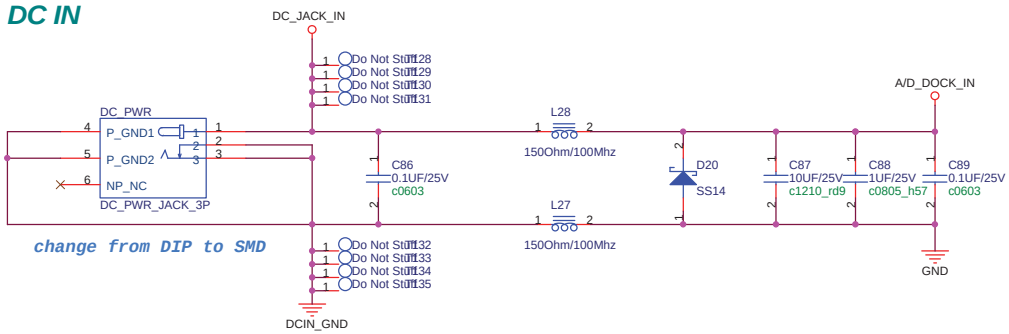
ASUSTek Computer INC.	Title : LED_THERMTRIP	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 36 of 47	



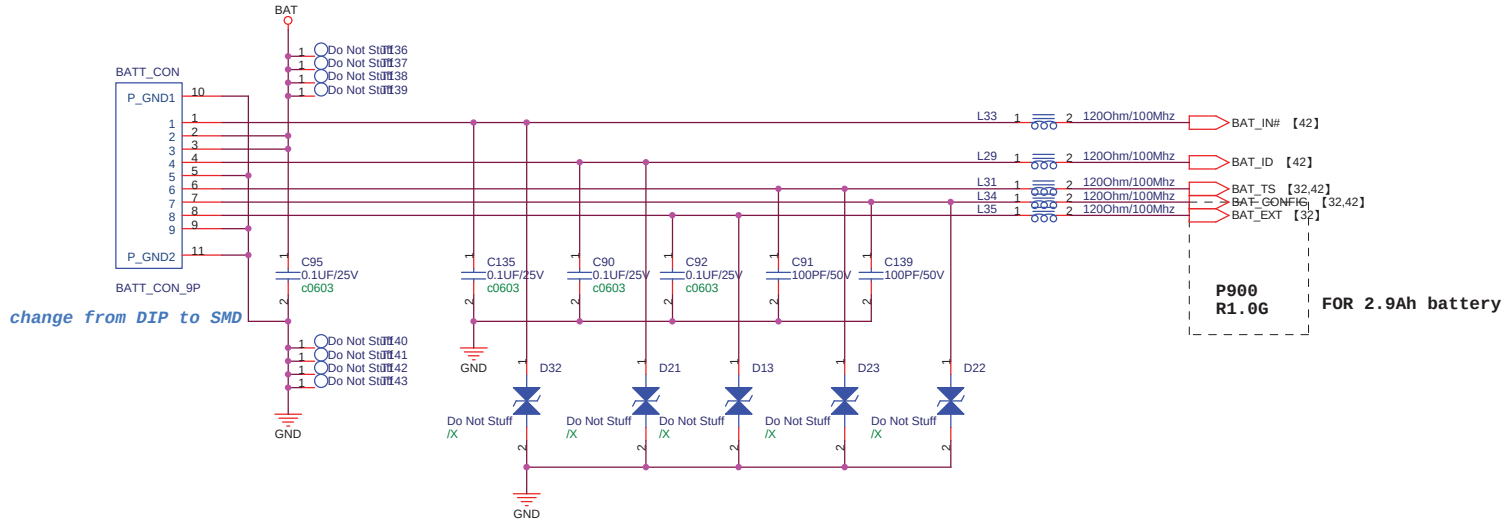
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Discharge	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 37 of 47	

DC IN

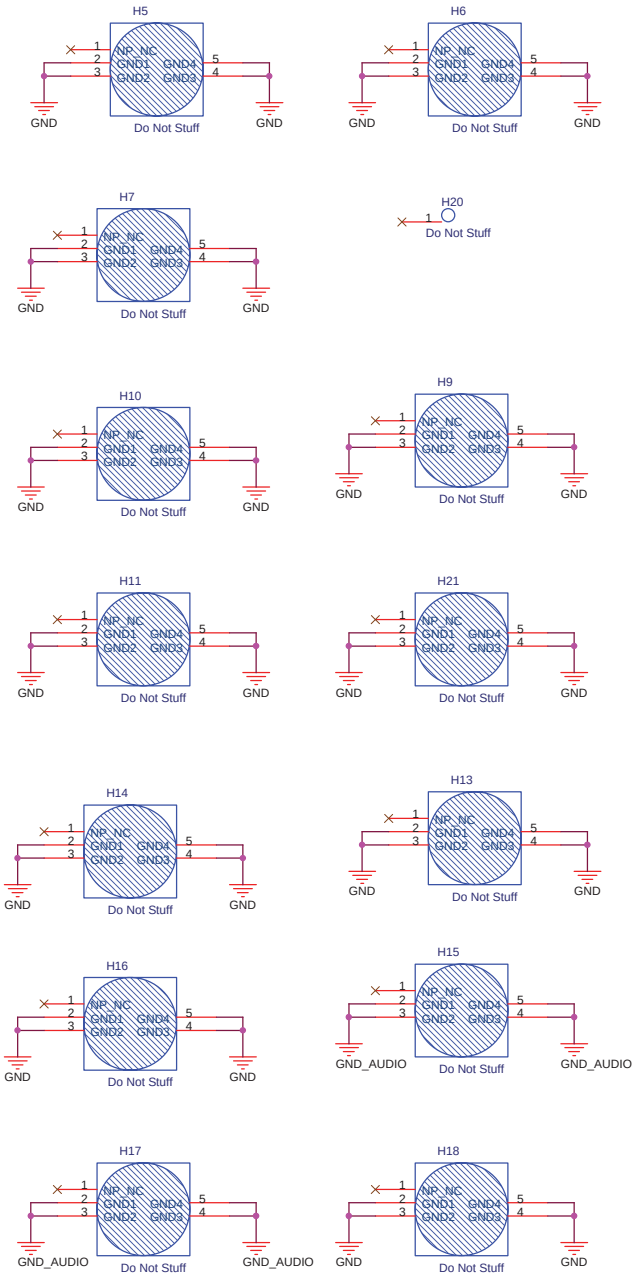


BAT IN



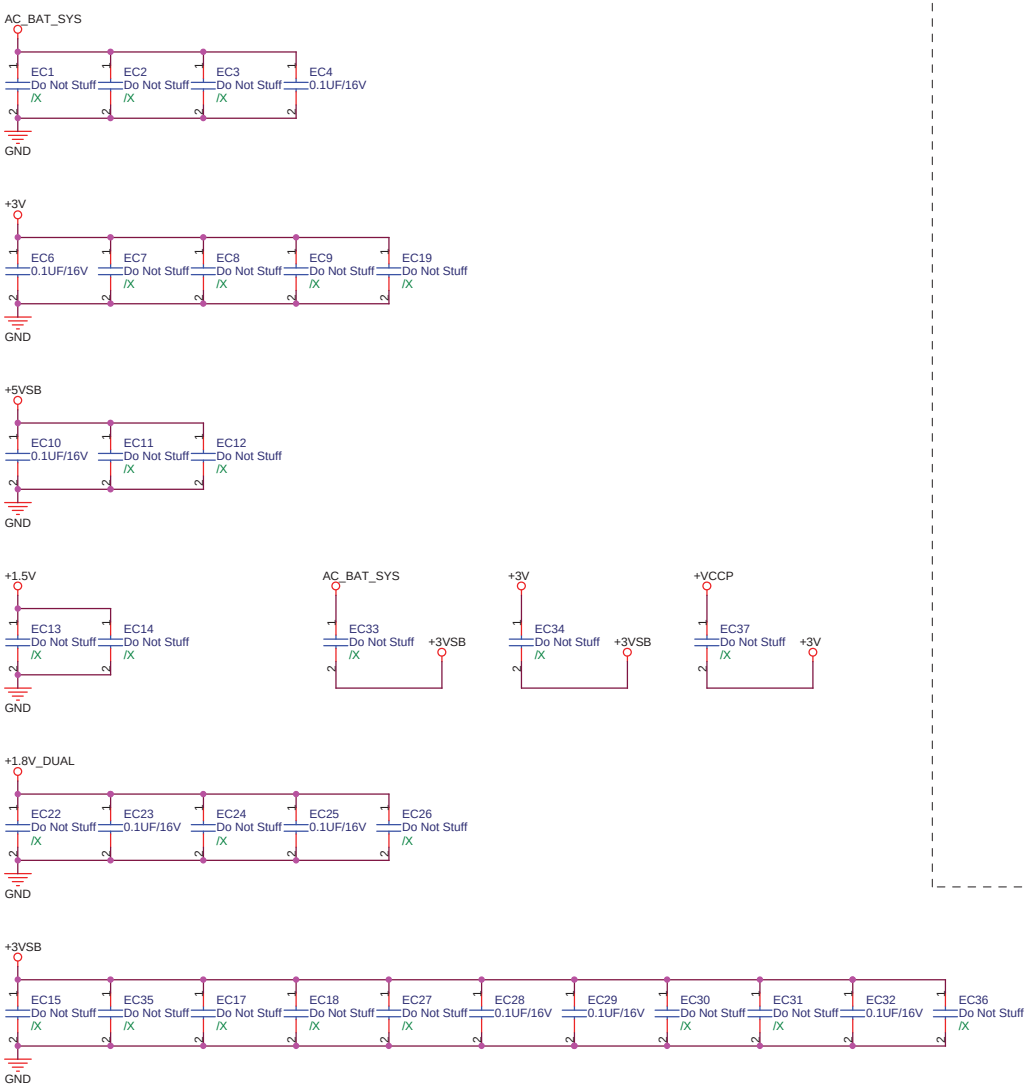
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: *Tiansen_Wu*	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 38 of 47	



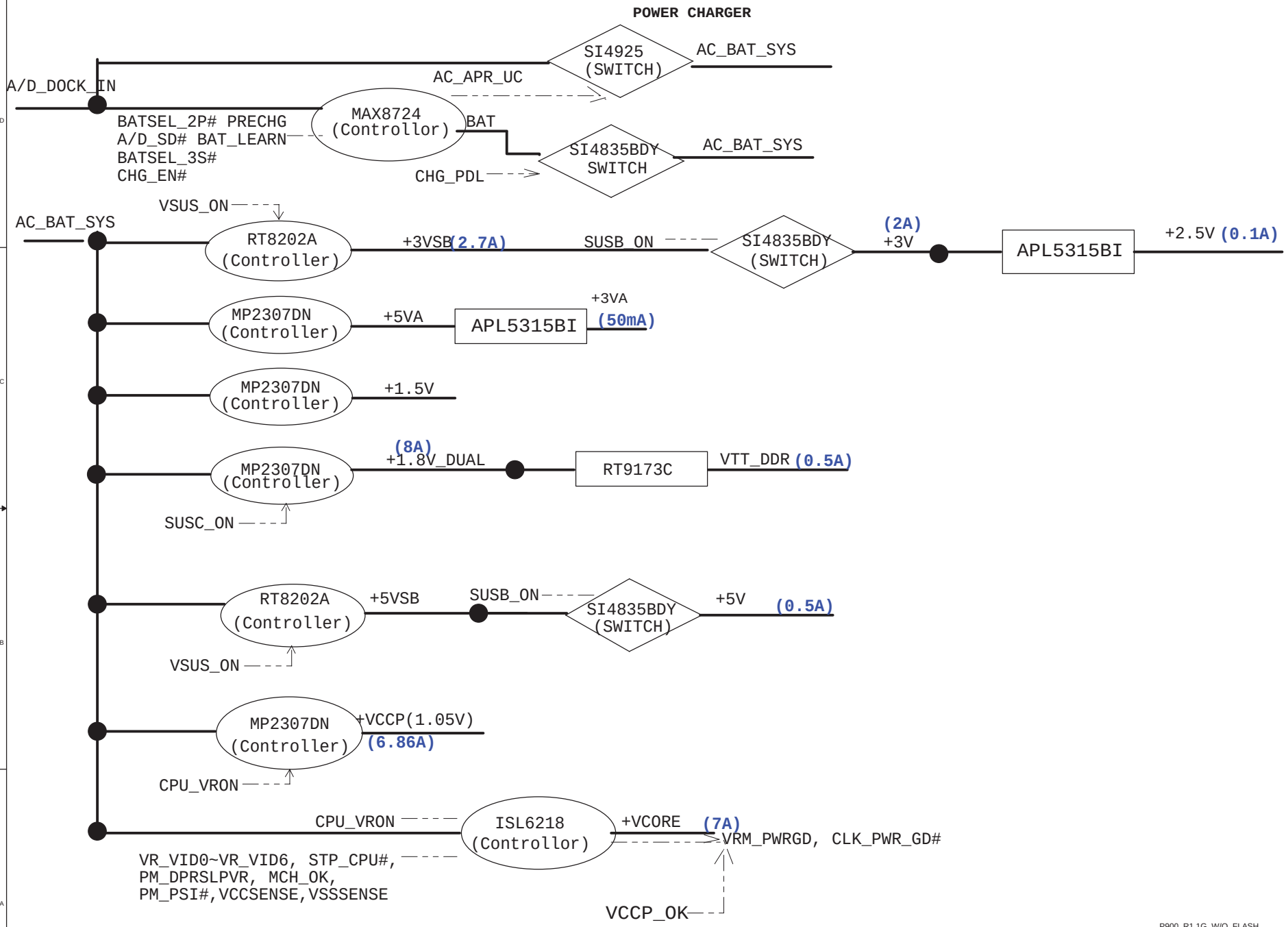
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 39 of 47	



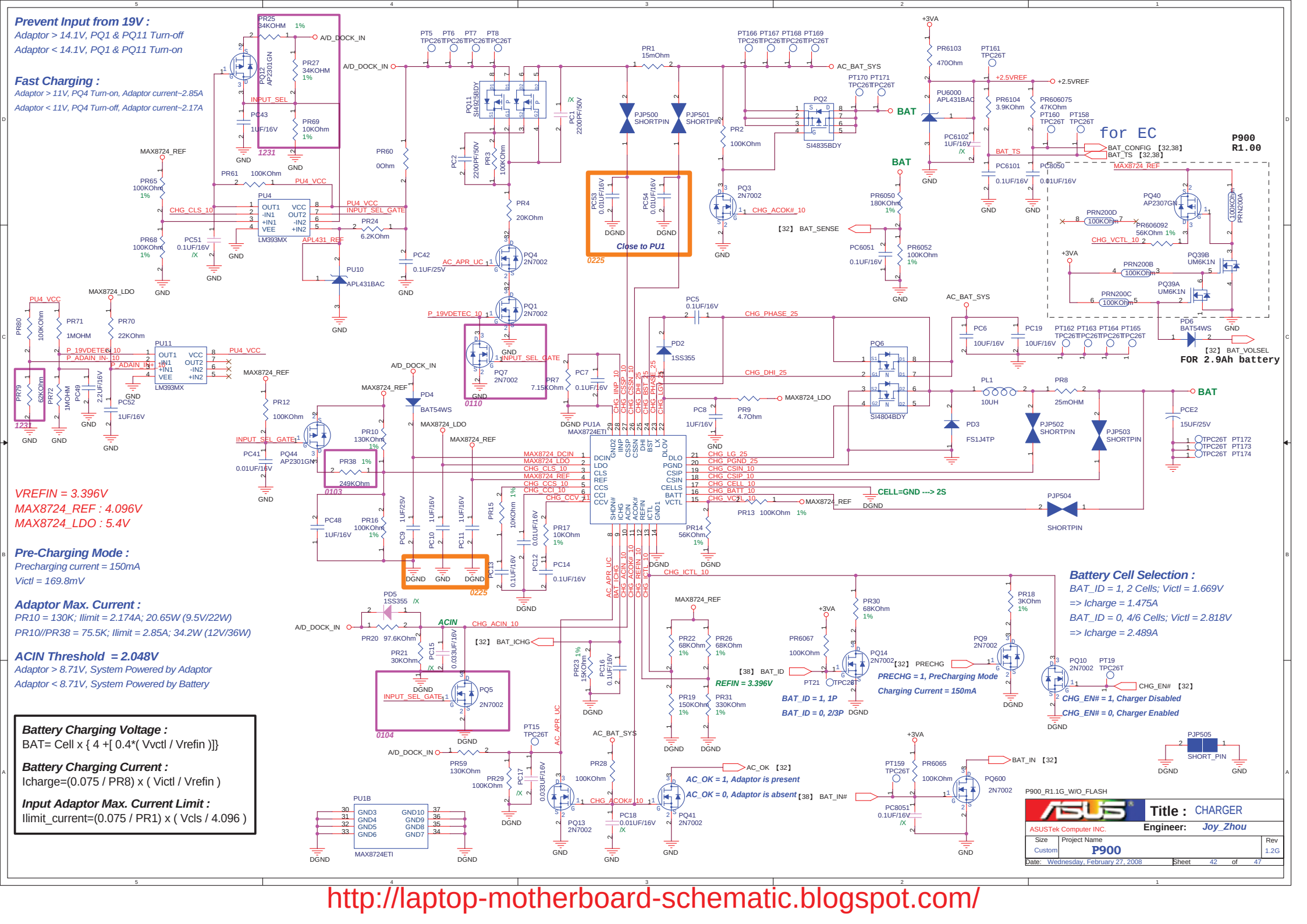
P900_R1.1G_W/O_FLASH

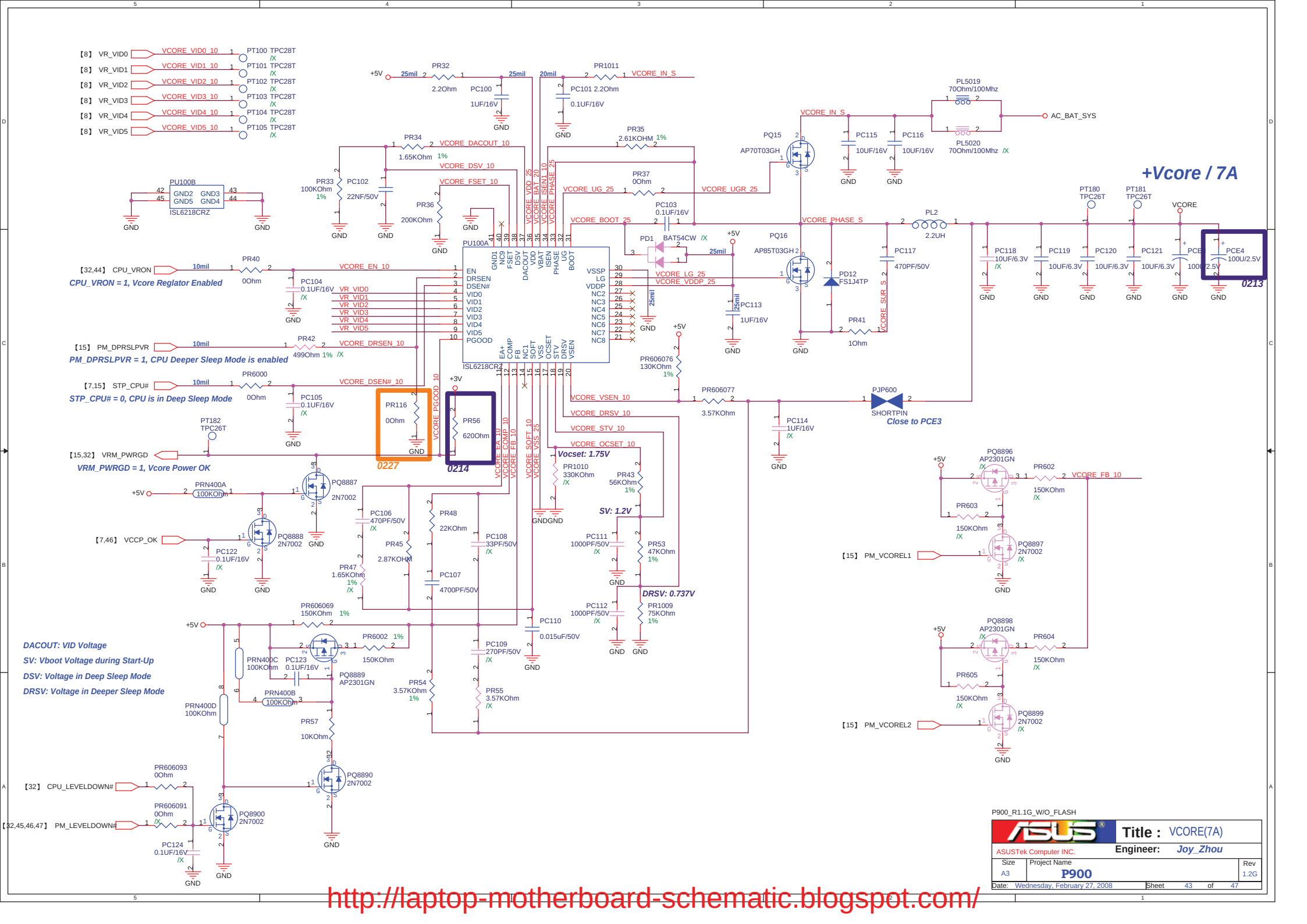
ASUSTek Computer INC.	Title : EMI	
	Engineer: Tiansen_Wu	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 40 of 47	

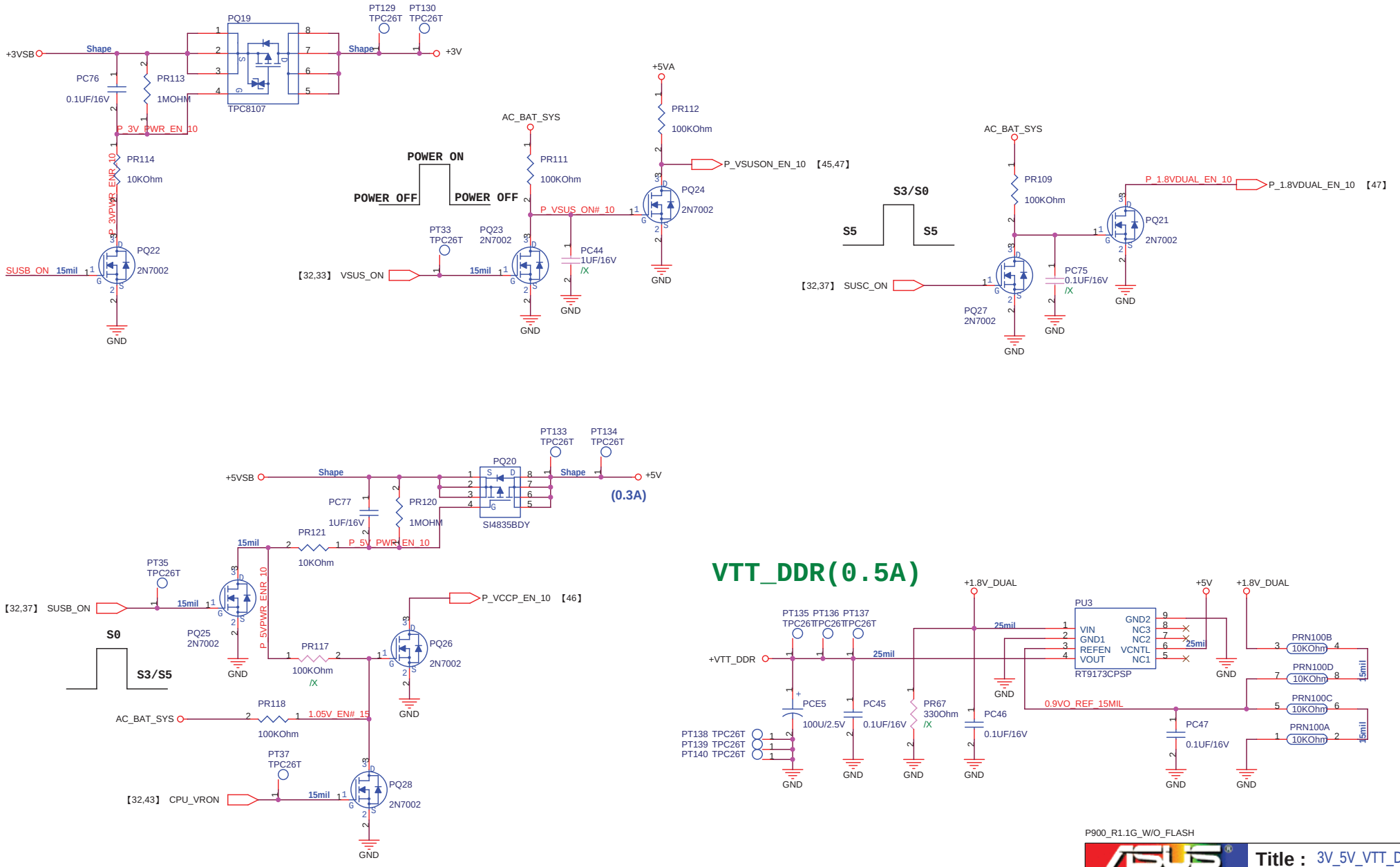


P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: Joy_Zhou	
Size: A3	Project Name: P701	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 41 of 47	

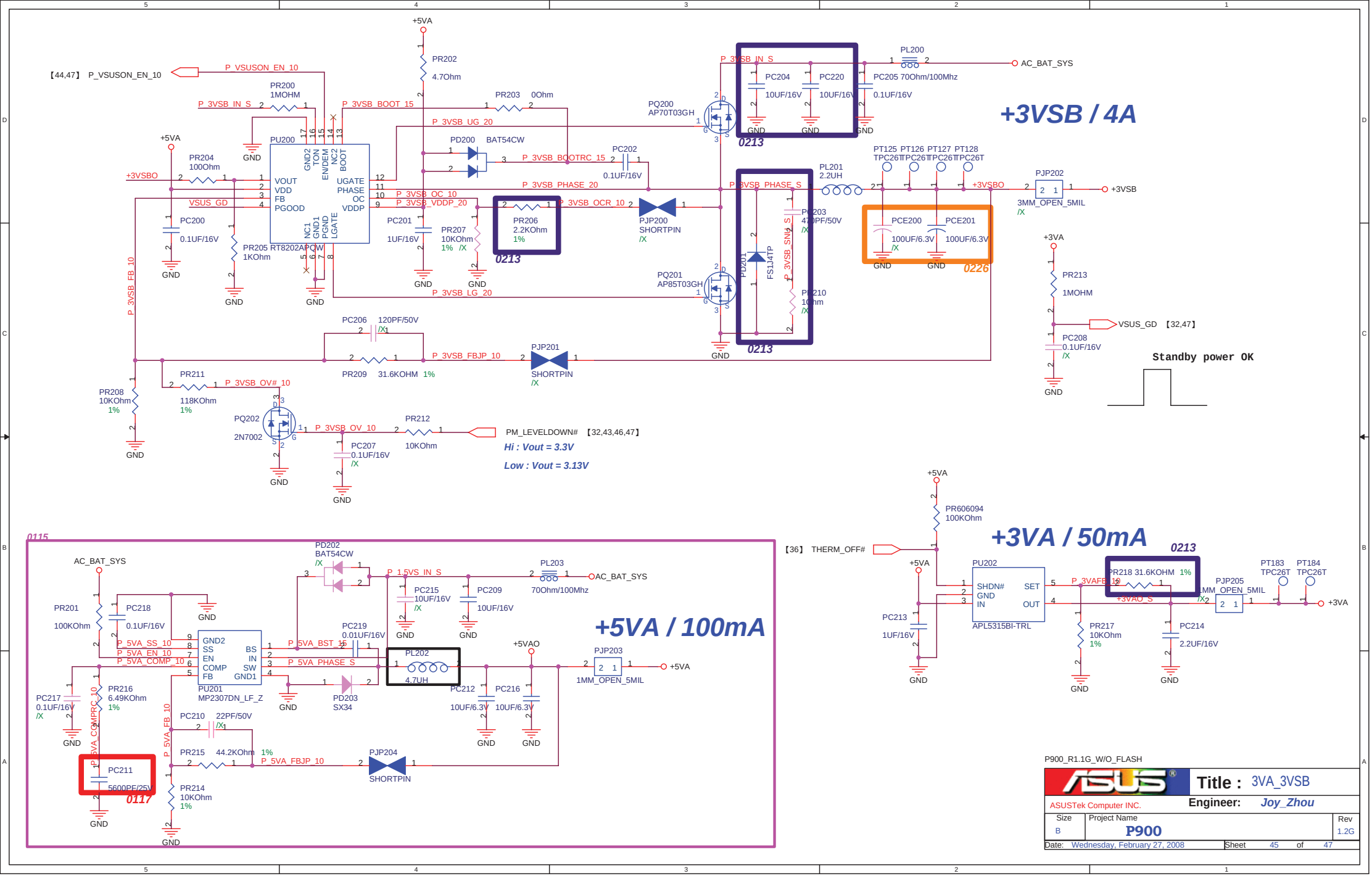


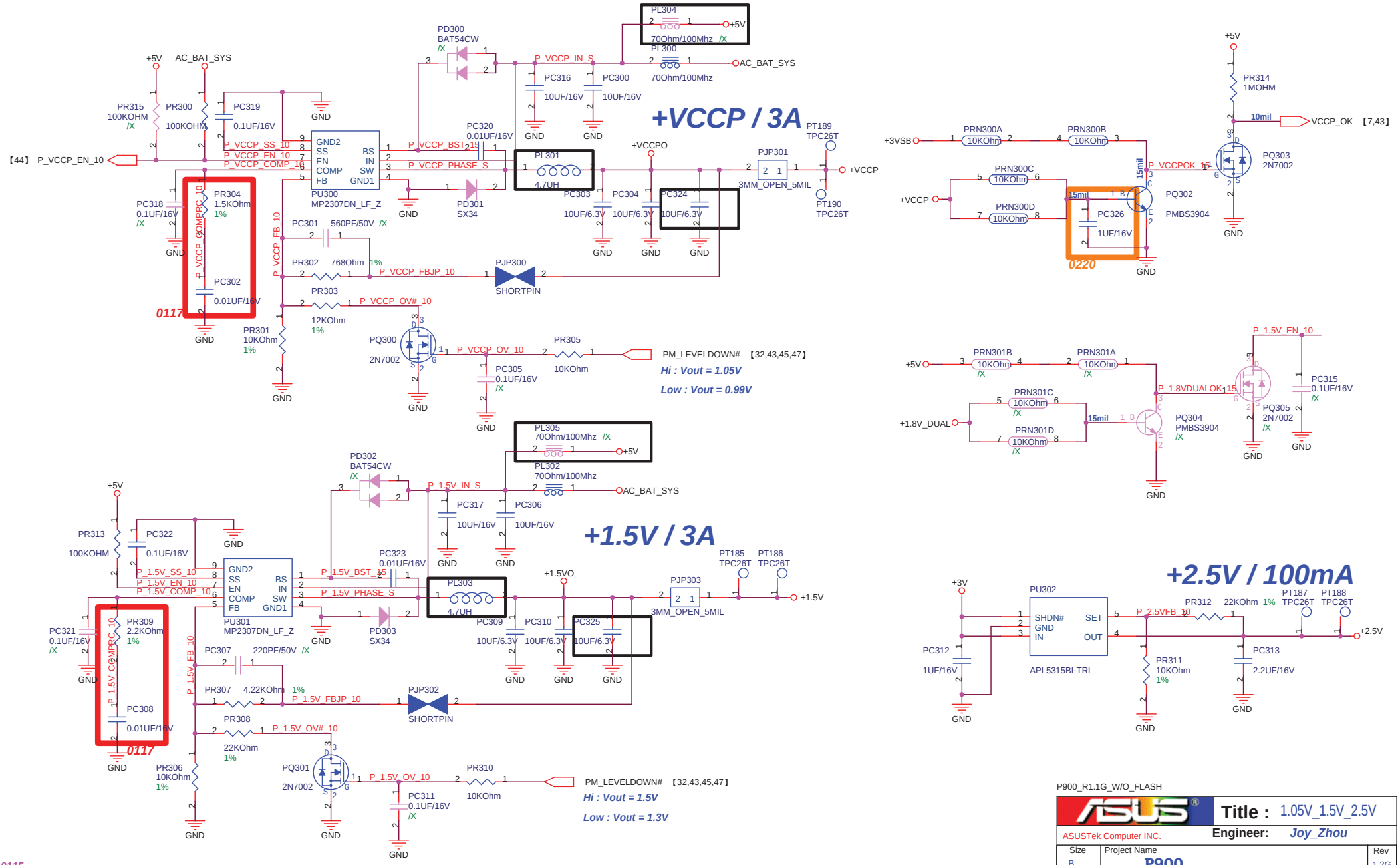


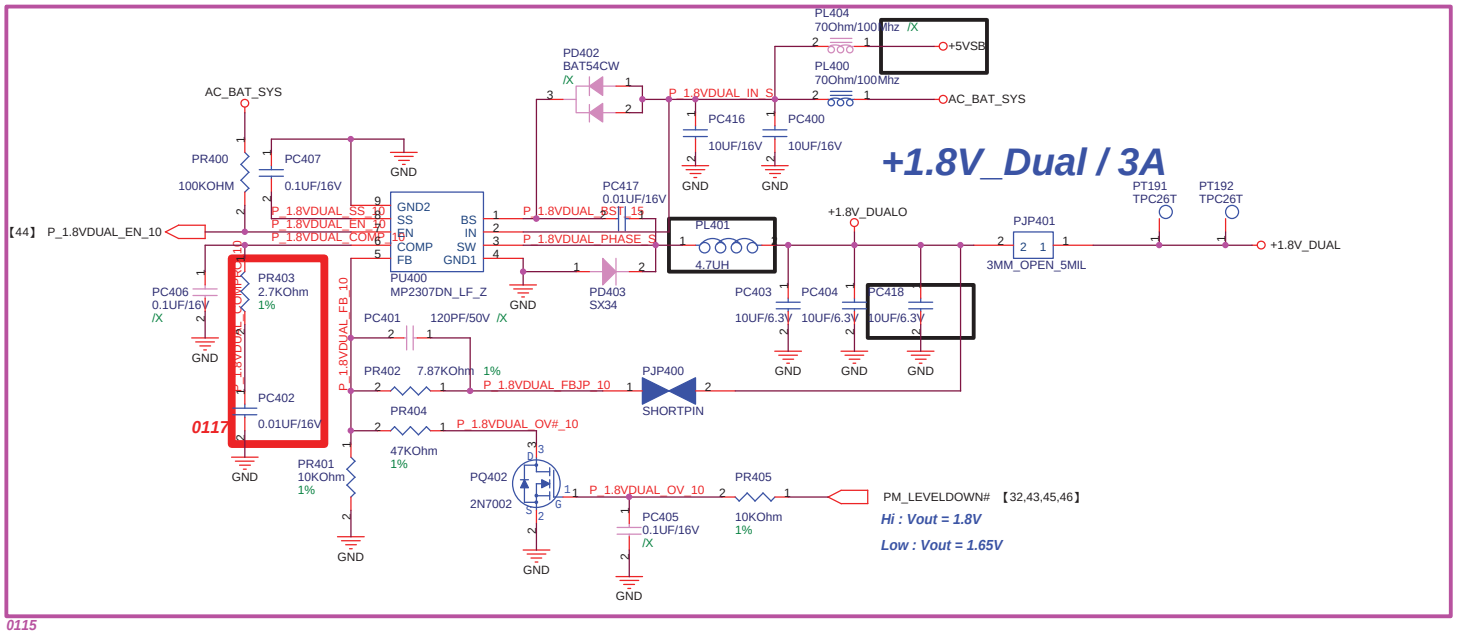


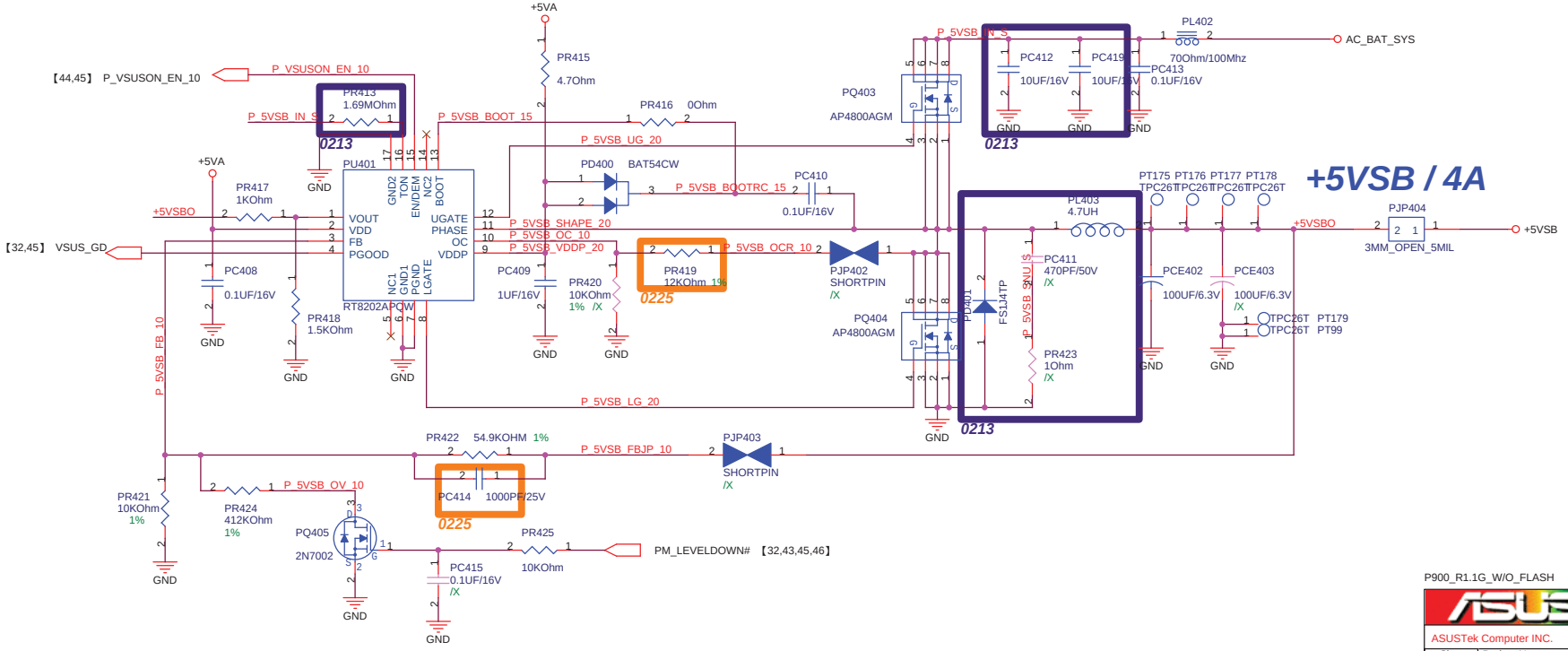
P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : 3V_5V_VTT_DDR	
	Engineer: Joy_Zhou	
Size: B	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 44 of 47	









P900_R1.1G_W/O_FLASH

ASUSTek Computer INC.	Title : 1.8V_DUAL_5VSB	
	Engineer: Joy_Zhou	
Size: A3	Project Name: P900	Rev: 1.2G
Date: Wednesday, February 27, 2008	Sheet 47 of 47	