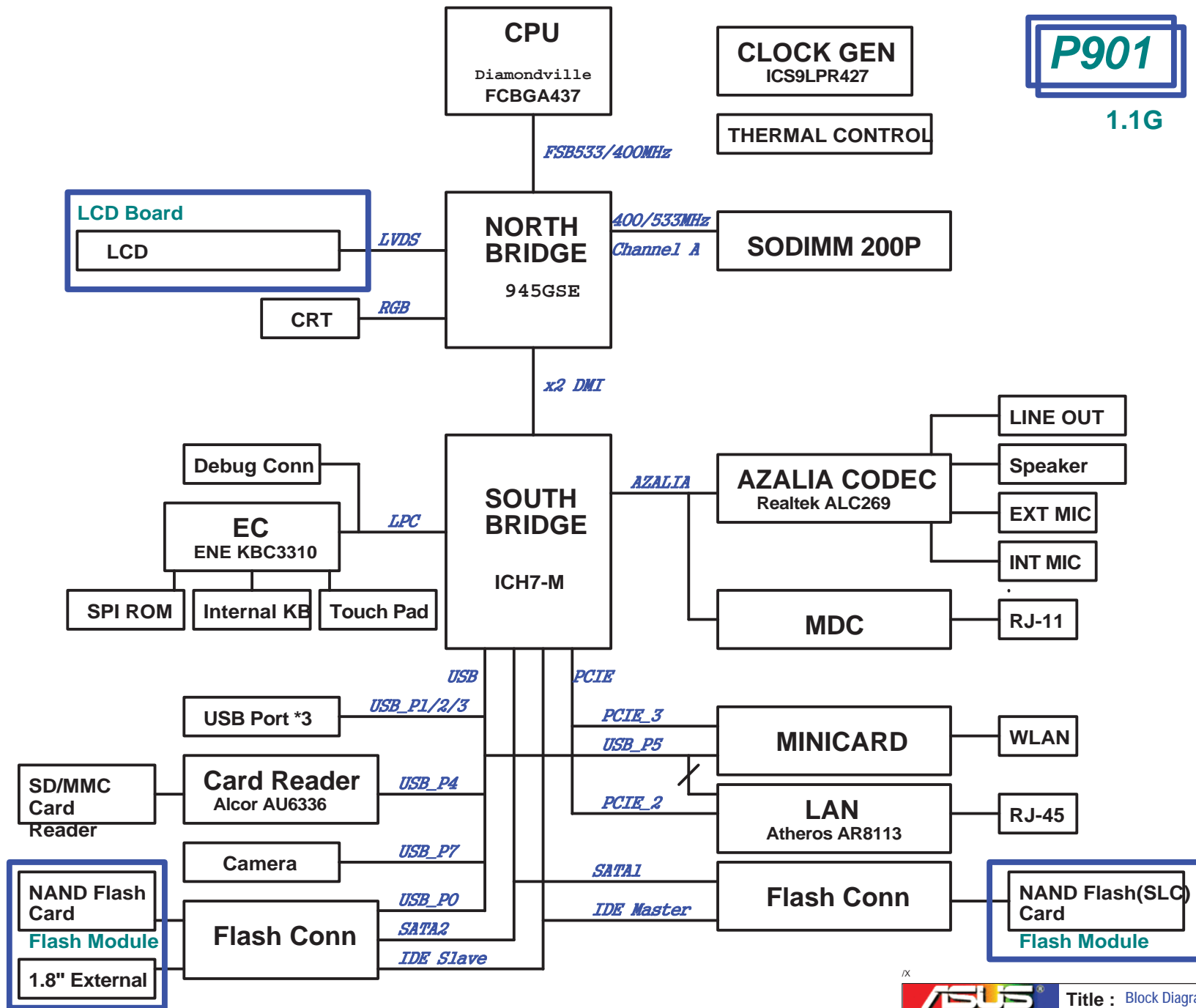


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_Clock Gen_ICS9LPR426
- 05_Diamondville_BUS
- 06_Diamondville_PWR
- 07_NB-945GMS(HOST)
- 08_NB-945GMS(DMI)
- 09_NB-945GMS(GRAPHIC)
- 10_NB-945GMS(DDR2)
- 11_NB-945GMS(PWR)
- 12_NB-945GMS(PWR2)
- 13_NB-945GMS(GND)
- 14_SB-ICH7M(PWR)
- 15_SB-ICH7M(1)
- 16_SB-ICH7M(2)
- 17_SB-ICH7M(3)
- 18_DDR2 SODIMM
- 19_DDR2 Termination
- 20_Onboard VGA
- 21_LCD Conn_LID
- 22_PCIEx 3.5G & Ext. Antenna
- 23_Mini WIFI+ BT
- 24_LAN_Atheros AR8113
- 25_MDC_RJ11_RJ45
- 26_HD + Flash Conn
- 27_USB Port
- 28_Camera Conn
- 29_Card Reader_AU6336C52
- 30_Codec_ALC269
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_EC_UART controller
- 34_Switch_SPI ROM_Debug Conn
- 35_Thermal Sensor_FAN
- 36_KB_Touch Pad
- 37_LED_THERMTRIP
- 38_Discharge
- 39_PWR Jack
- 40_Srew Hole
- 41_EMI
- 42_POWER FLOW
- 43_Vcore
- 44_Power System
- 45_Power_+1.8V & VTTDDR
- 46_Power_VCCP
- 47_Power_+1.5VS & +2.5VS
- 48_Power_Charger
- 49_EC Pin Define
- 49_History



<http://hobi-elektronika.net>

ASUS		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Regin Chiang	
Size	Project Name	Date	Rev
A3	P901	Monday, May 19, 2008	1.1G
Date: Monday, May 19, 2008		Sheet	1 of 50

EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

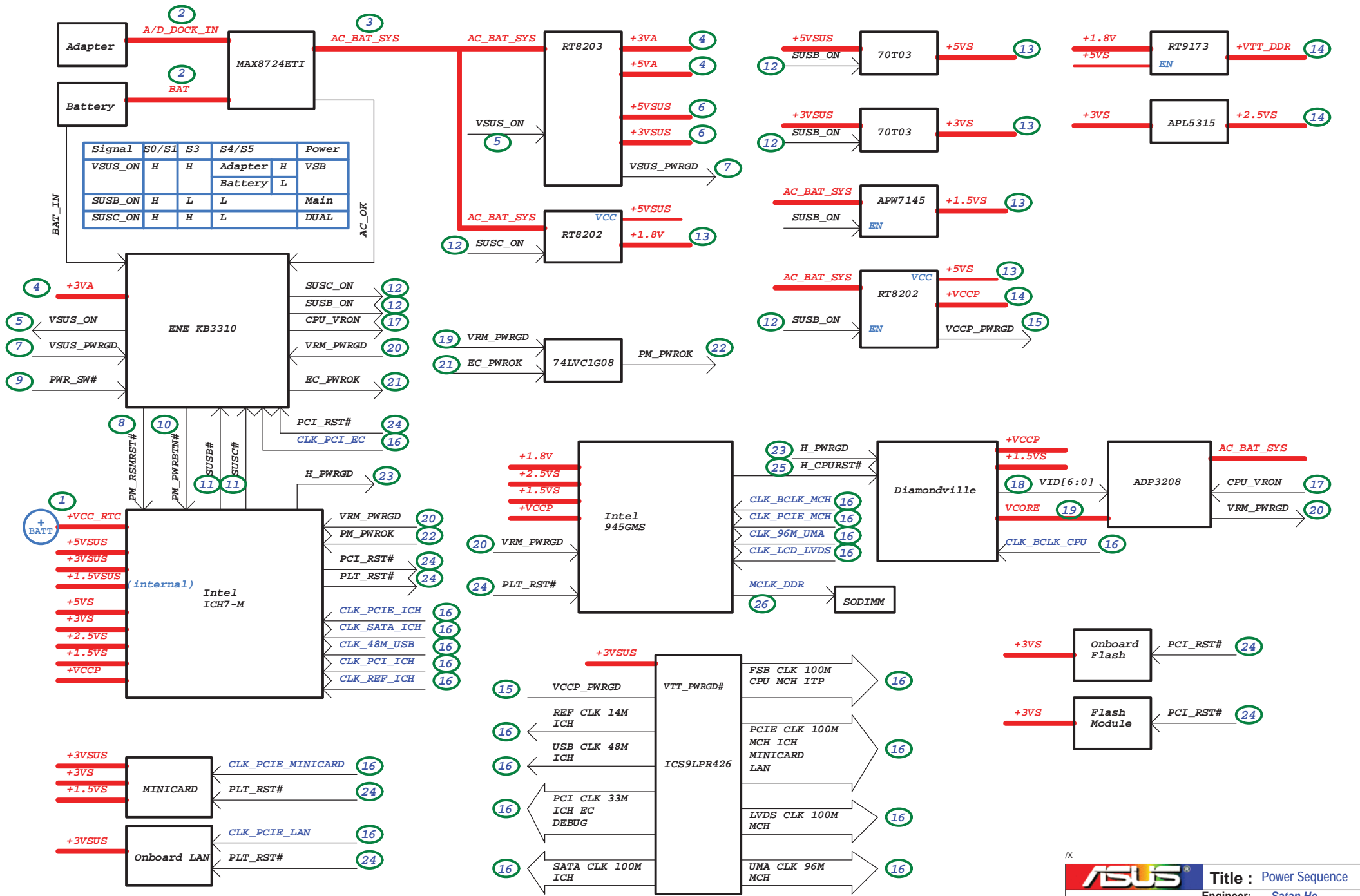
USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

PCIE

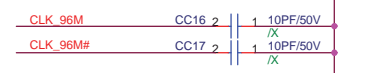
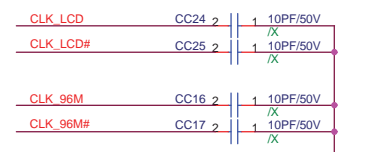
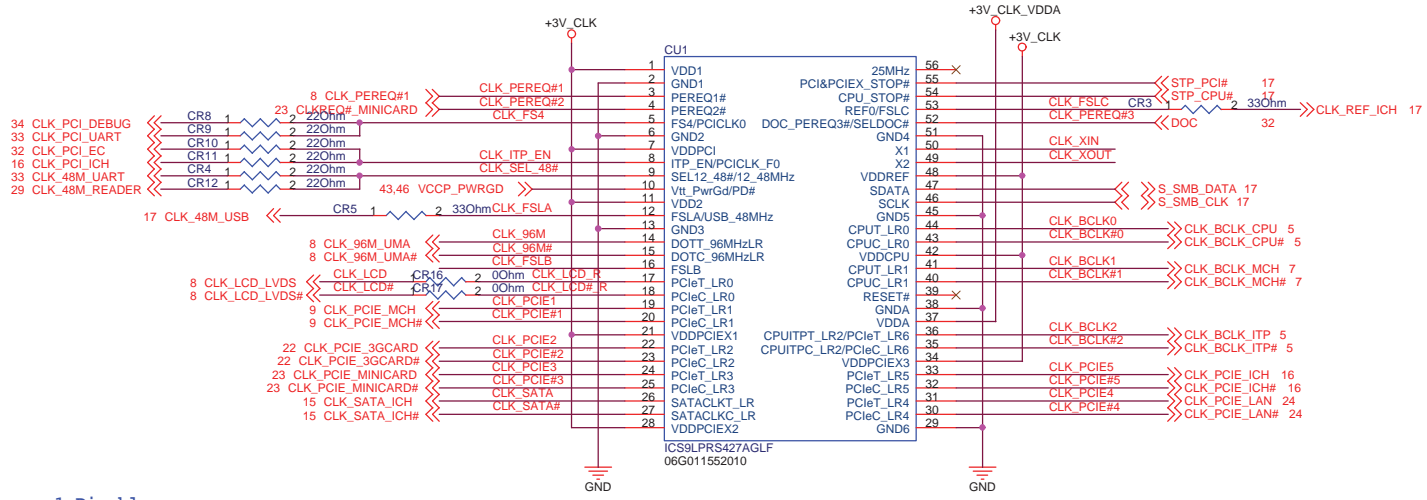
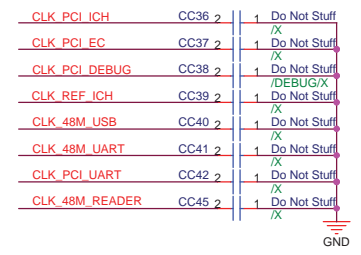
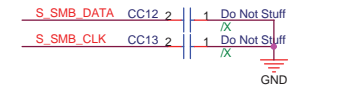
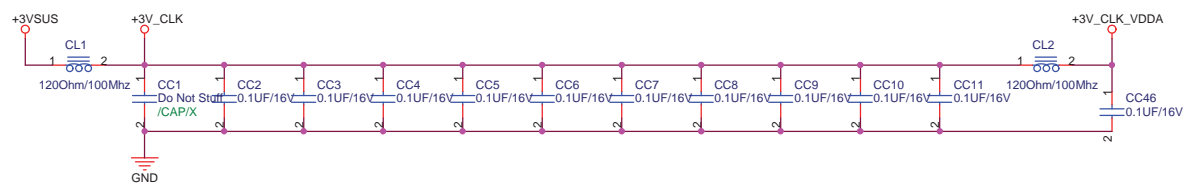
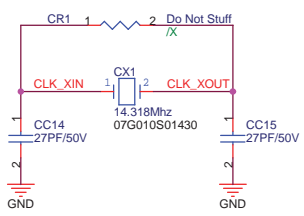
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM
ACZ_SDIN2	NC



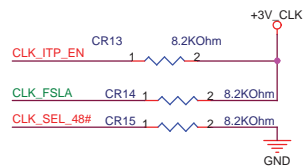
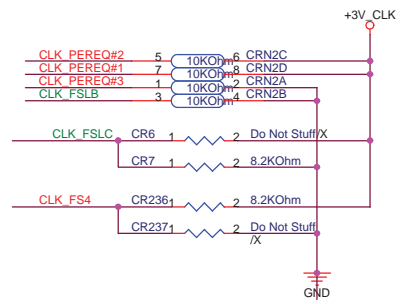
<http://hobi-elektronika.net>



1:Disable
0:Enable

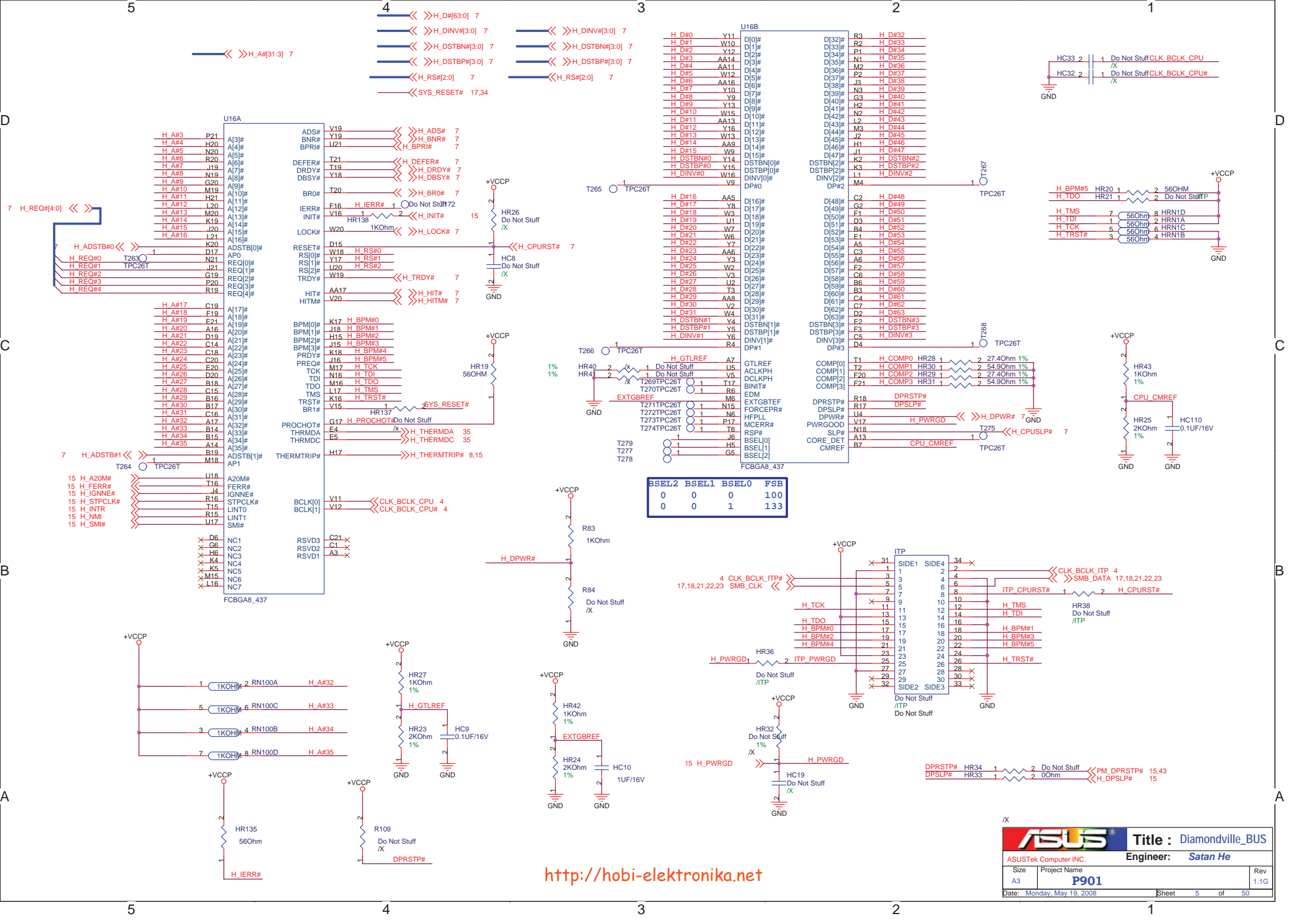
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100



<http://hobi-elektronika.net>

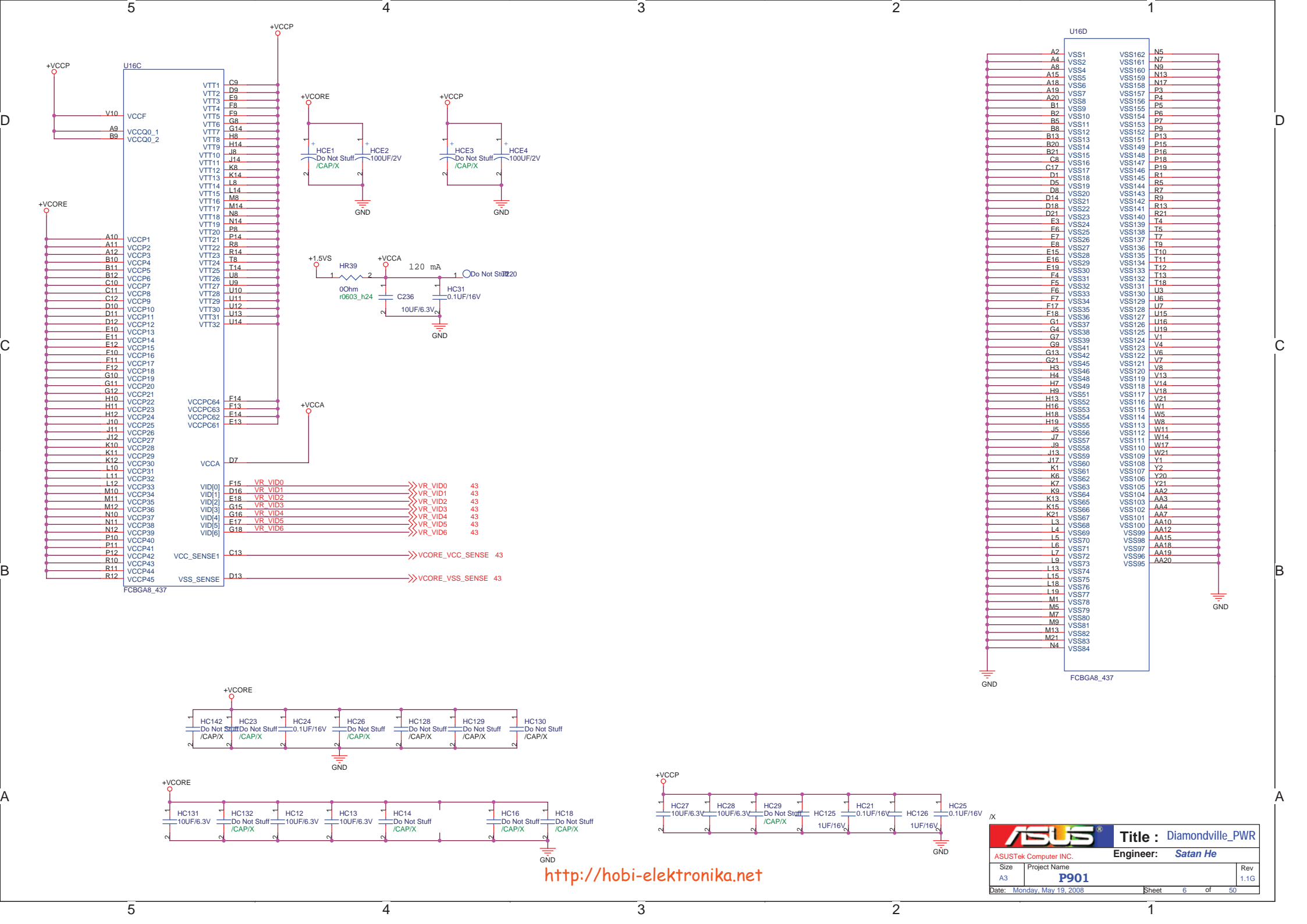
ASUS® Title : Clock Gen_ICS9LPRS427
ASUSTek Computer INC. Engineer: **Satan He**
Size Project Name
A3 **P901** Rev 1.1G
Date: Monday, May 19, 2008 Sheet 4 of 50



BSEL2	BSEL1	BSEL0	FSB
0	0	0	1.00
0	0	1	1.33

ASUS Title : Diamondville_BUS
 ASUSTek Computer INC. Engineer: Satan He
 Size: A3 Project Name: P901 Rev: 1.1G
 Date: Monday, May 19, 2008 Sheet 5 of 50

<http://hobi-elektronika.net>



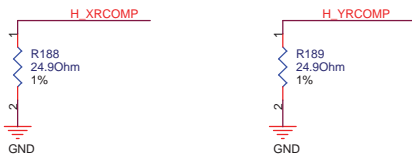
<http://hobi-elektronika.net>

ASUS		Title : Diamondville_PWR	
ASUSTek Computer INC.		Engineer: Satan He	
Size	Project Name		Rev
A3	P901		1.1G
Date:	Monday, May 19, 2008	Sheet	6 of 50

**Power :
+VCCP**

RCOMP

For Calibrating the FSB I/O Buffer



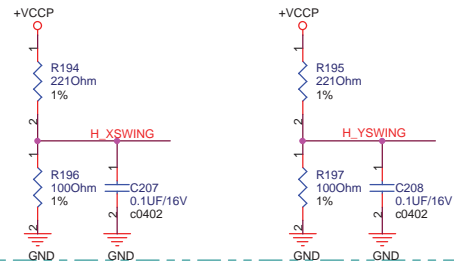
SCOMP

For Slew Rate Compensation on the FSB

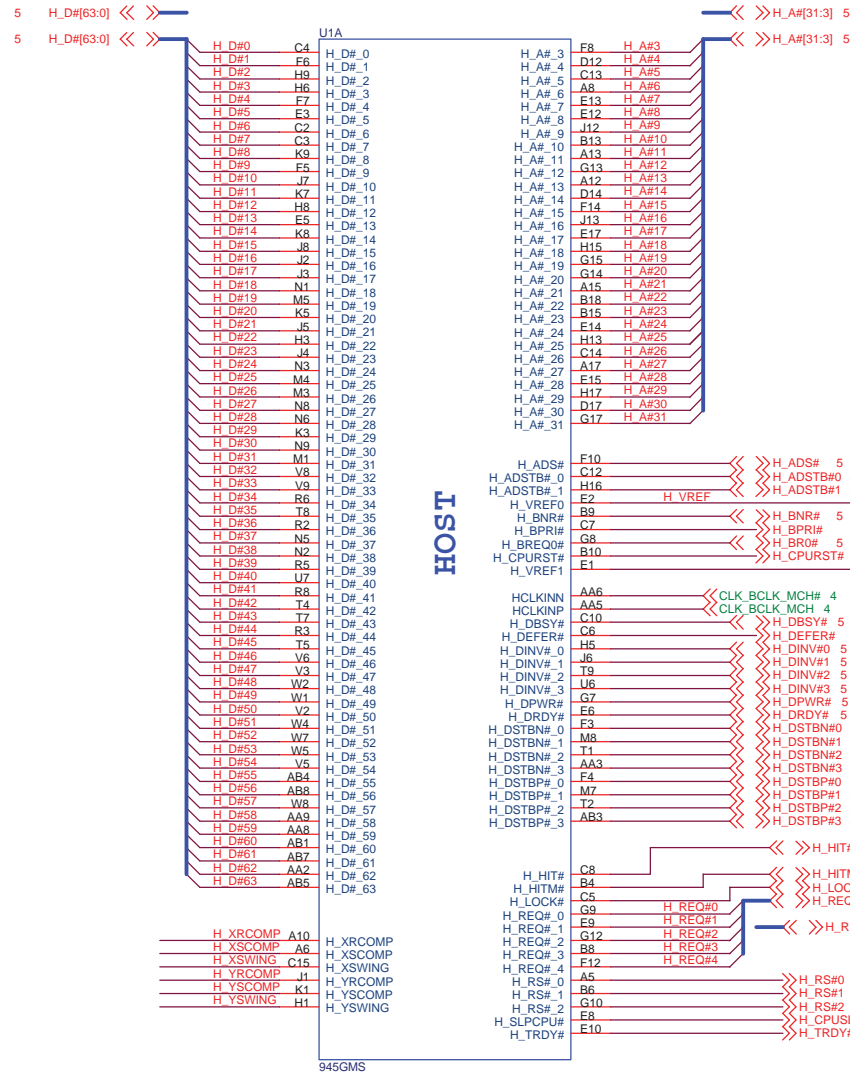


Voltage Swing

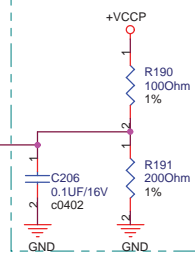
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing

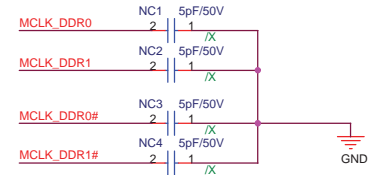
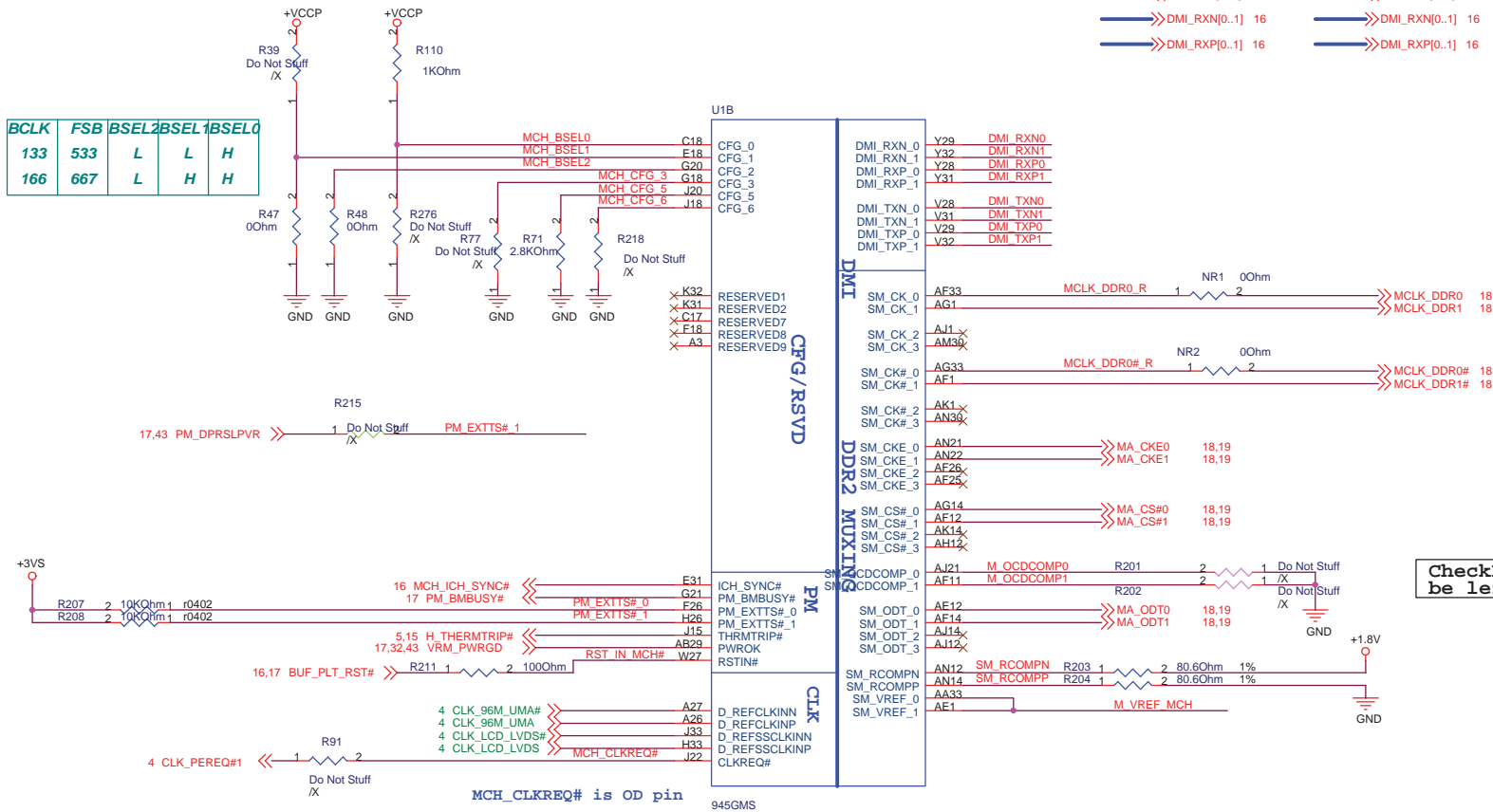


AGTL+ I/O Voltage Reference

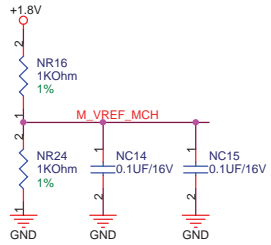


Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

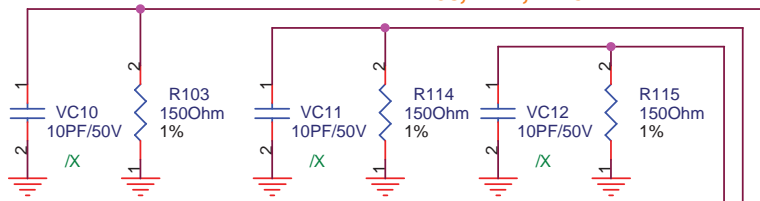


CheckList notes :Can be left as NC

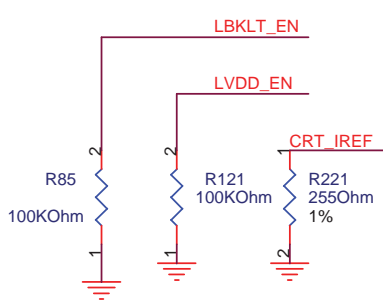
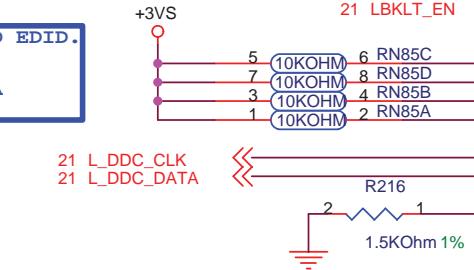


ASUS		Title : NB-945GMS(DMI & CFG)	
ASUSTeK COMPUTER INC.		Engineer: Satan He	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008	Sheet	8	of 50

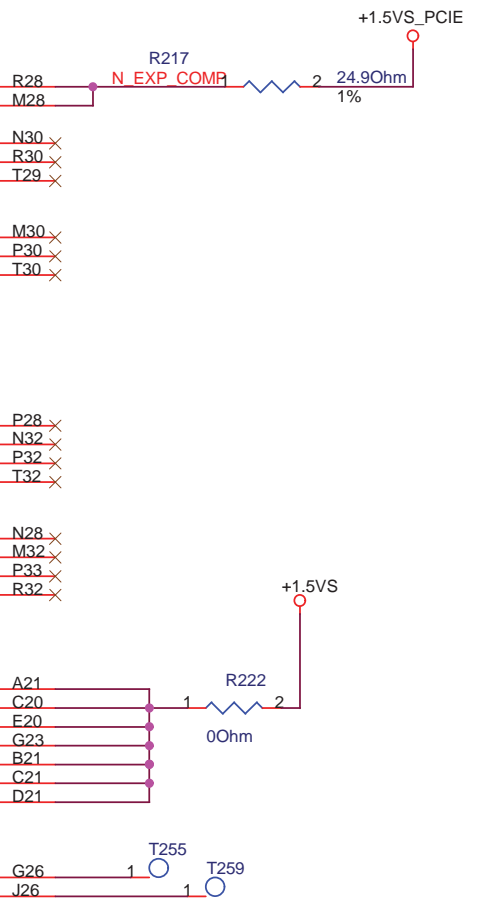
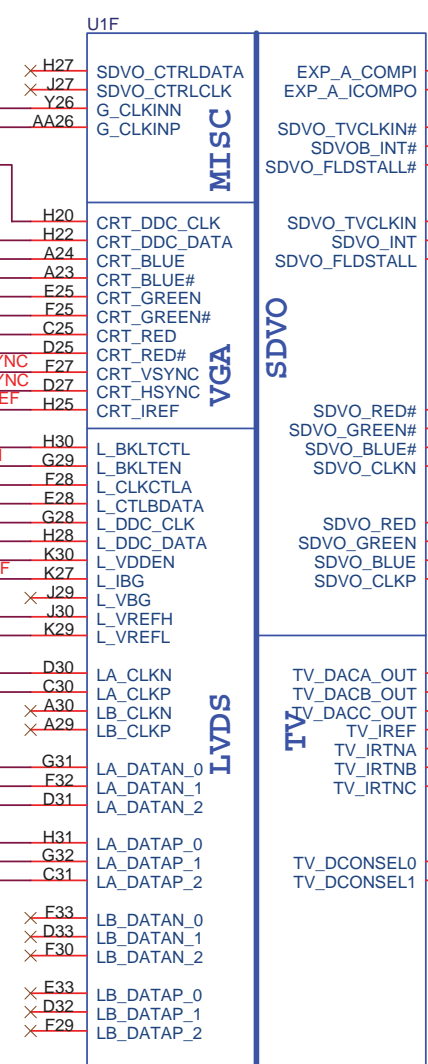
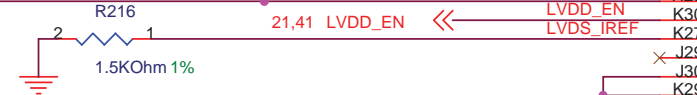
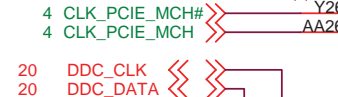
Close to GMCH
R103,R114,R115



IF USE NB READ EDID.
MUST CONNECT
L_DDC_CLK&DATA



Close to GMCH



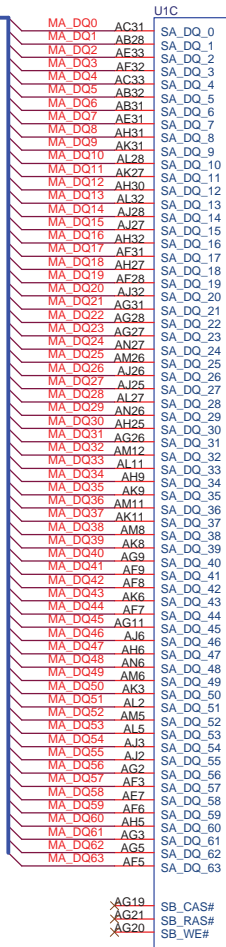
945GMS

/X

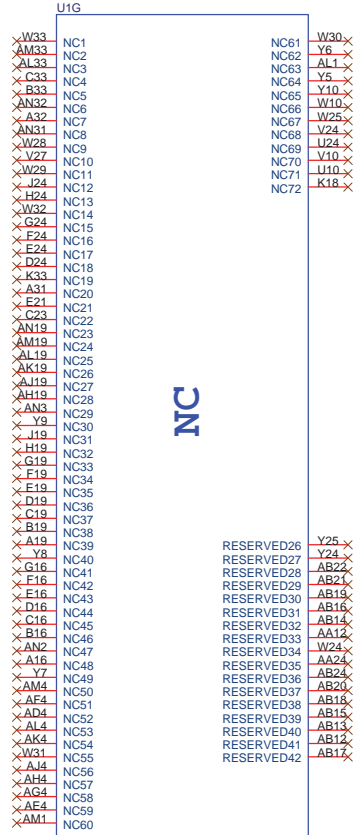
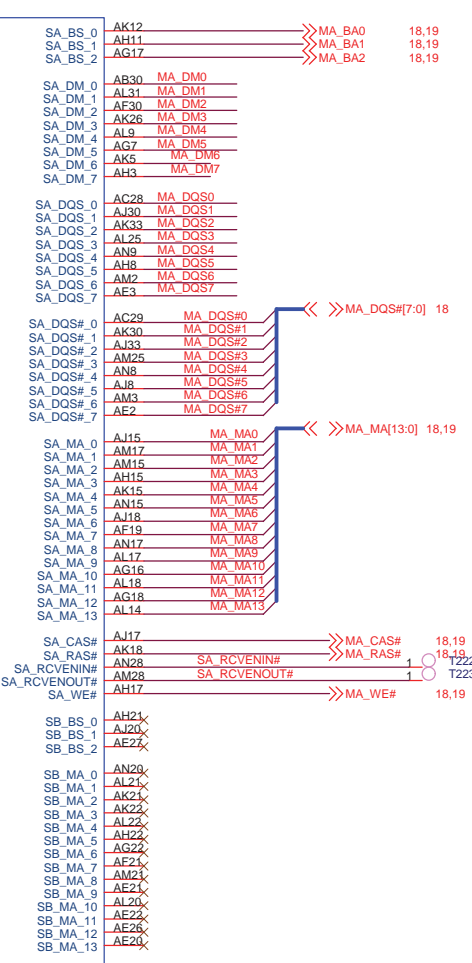
		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: Satan_He	
Size A4	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008	Sheet 9 of 50		

18 MA_DQ[63:0] << >>
 18 MA_DQ[63:0] << >>

<< >> MA_DQS[7:0] 18
 << >> MA_DM[7:0] 18



DDR2 SYSTEM MEMORY

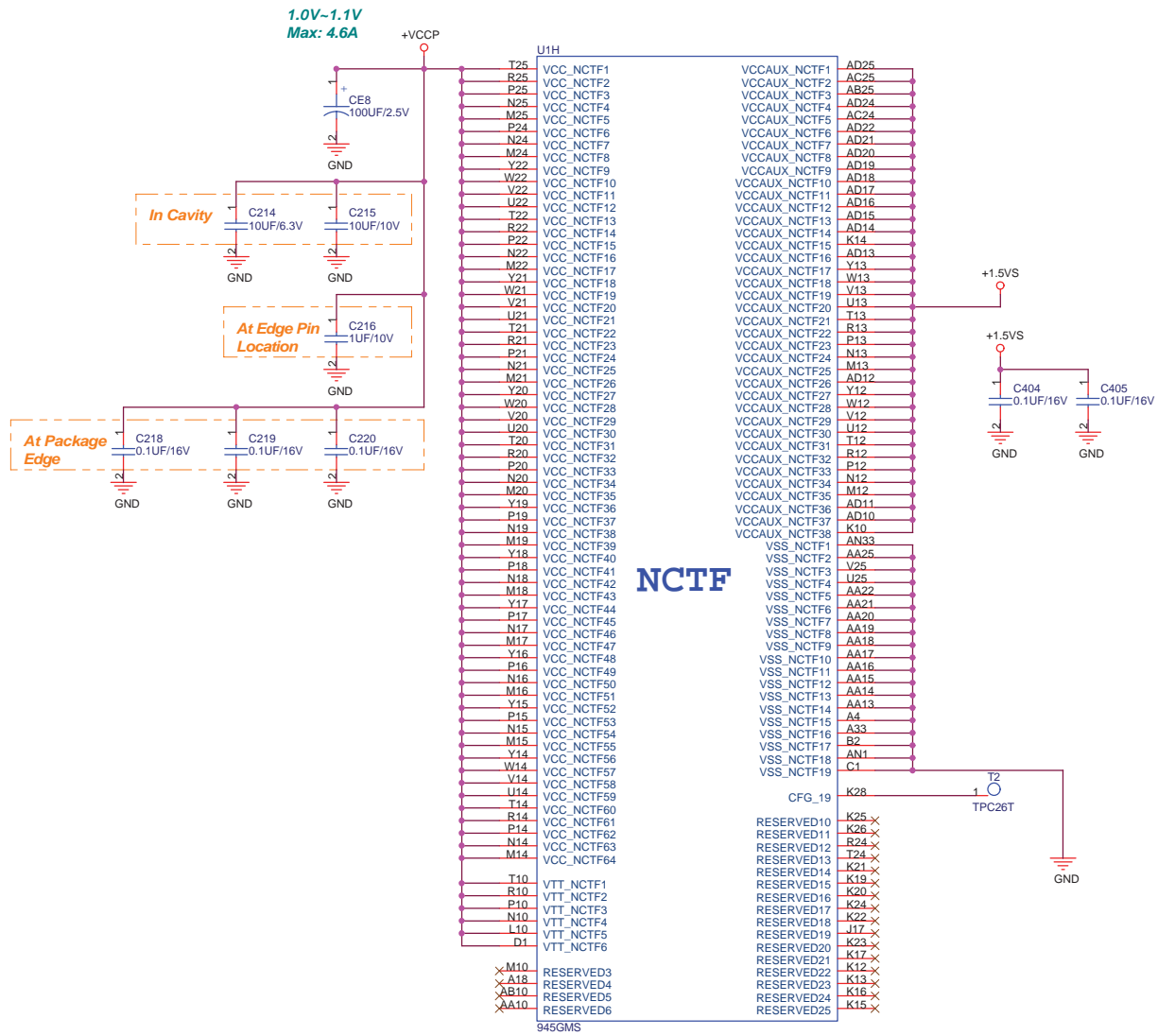


NC

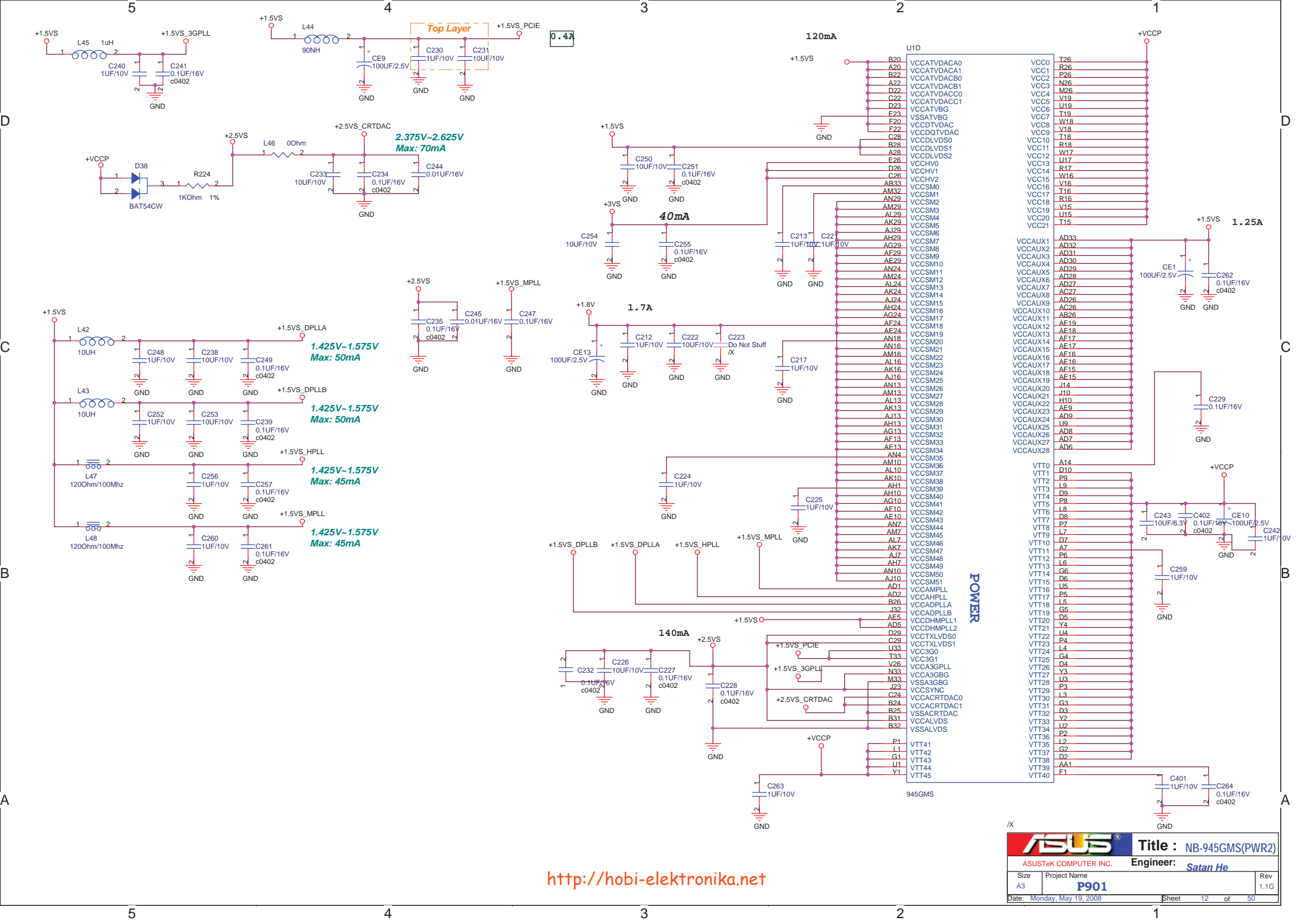
945GMS

945GMS

ASUS		Title : NB-945GMS(DDR2)	
ASUSTek COMPUTER INC.		Engineer: Satan He	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008		Sheet	10 of 50

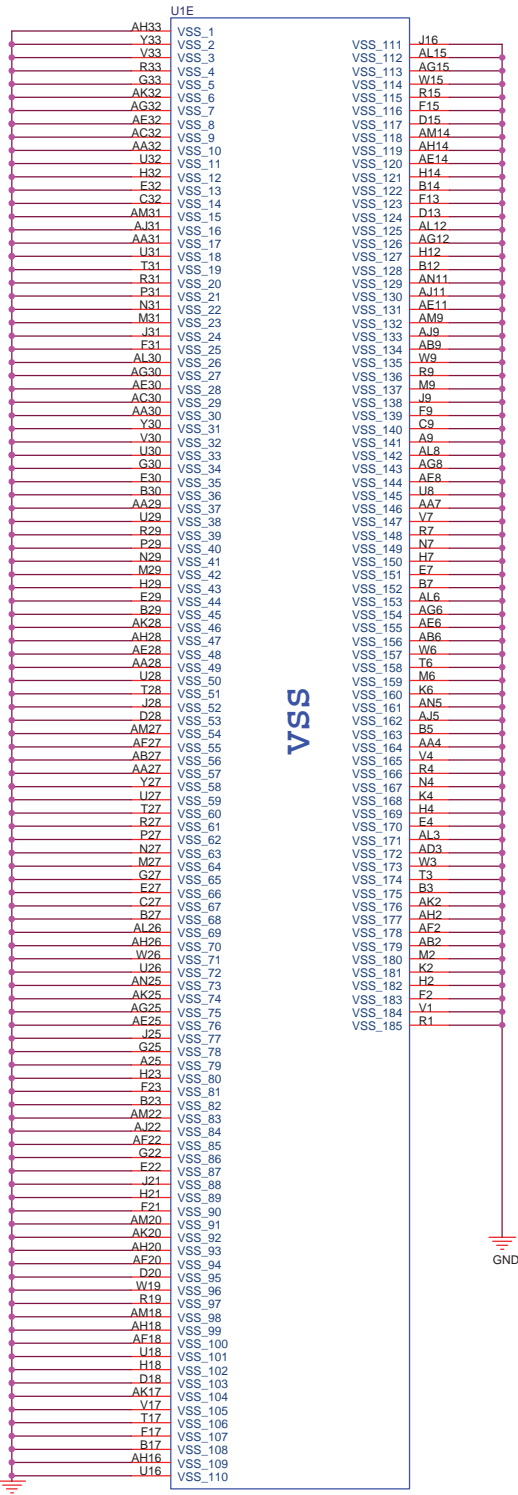


CFG_19(K28) Strapping :
DMI LANE Reversal:
 0:Normal Operation (Default)
 1.:Reversal Lanes, 3->0,2->1..etc
 Note:945GMS doesn't support DMI Lane Reversal



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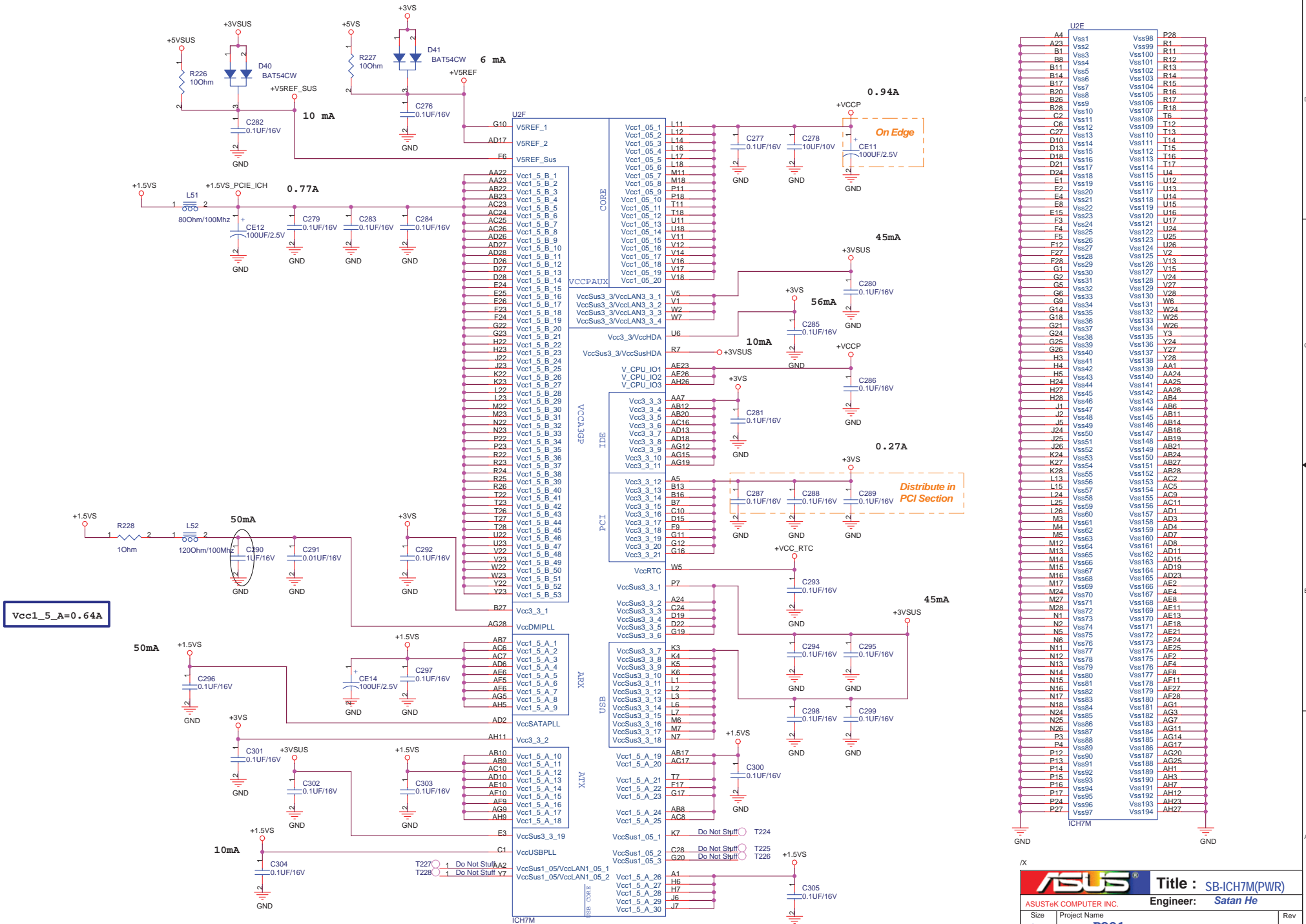
ASUS		Title : NB-945GMS(PWR2)	
ASUSTeK COMPUTER INC.		Engineer: Satan He	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008		Sheet 12 of 50	



VSS

<http://hobi-elektronika.net>

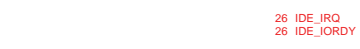
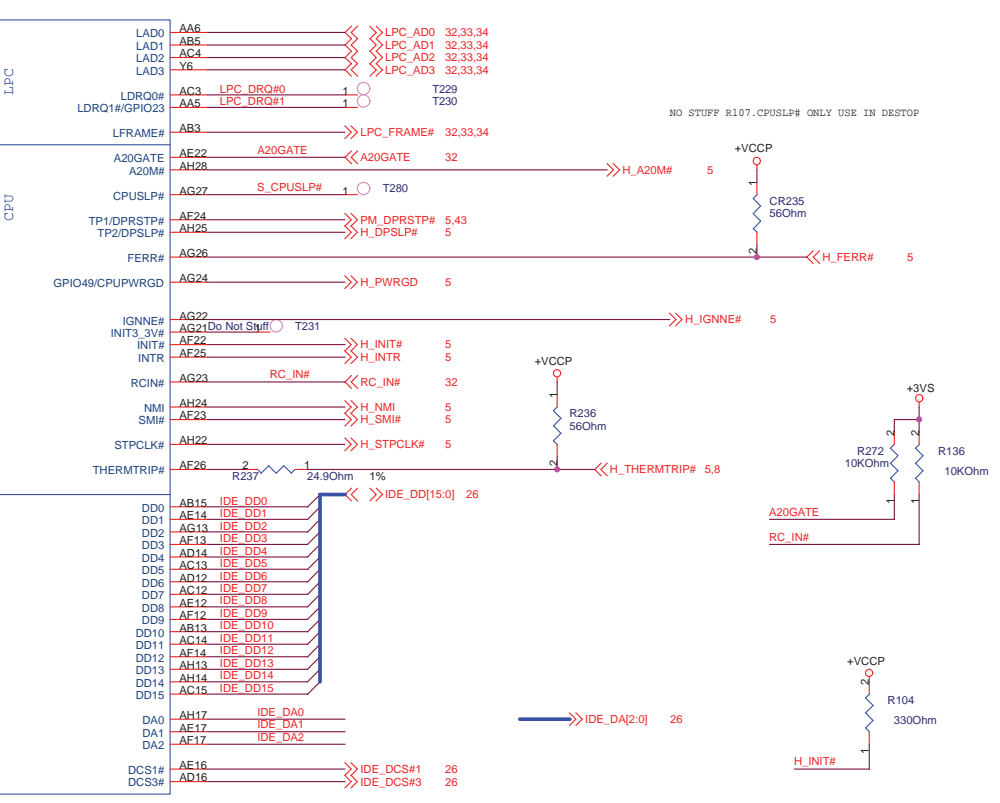
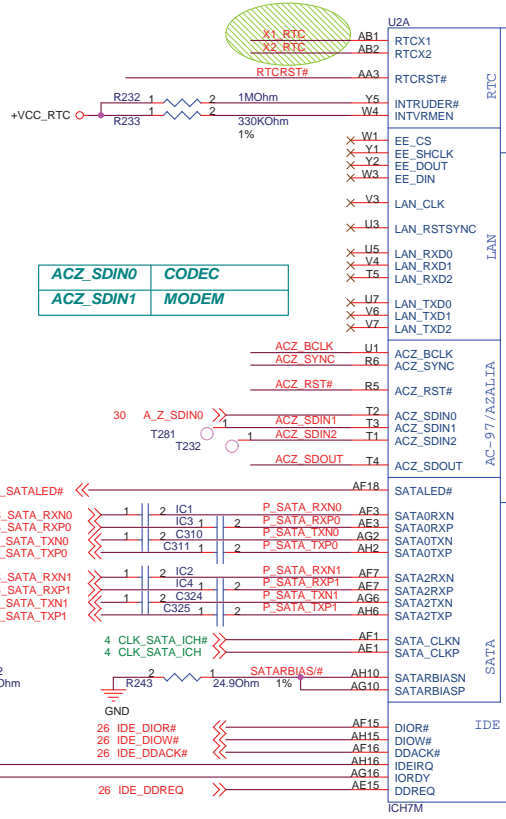
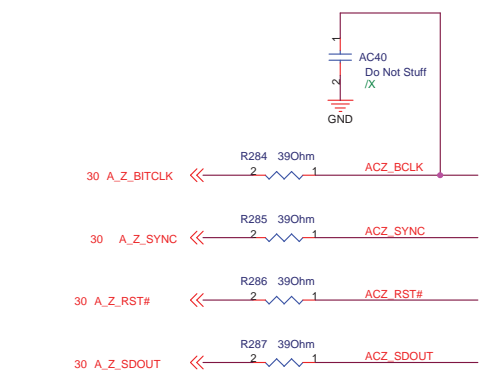
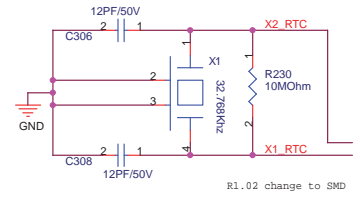
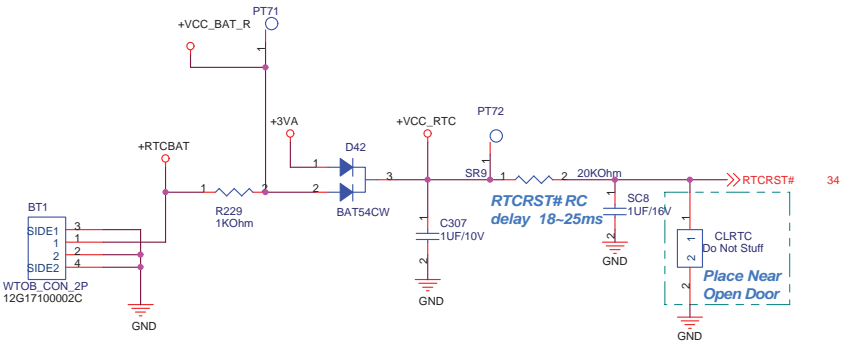
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ASUSTeK COMPUTER INC.		Engineer: Satan_He	
Size	Project Name	Rev	
A3	P901	1.1G	
Date:	Monday, May 19, 2008	Sheet	13 of 50



U2E		P28	
A4	Vss1	Vss89	R1
A23	Vss2	Vss99	R11
B1	Vss3	Vss100	R12
B8	Vss4	Vss101	R13
B11	Vss5	Vss102	R14
B14	Vss6	Vss103	R15
B17	Vss7	Vss104	R16
B20	Vss8	Vss105	R17
B26	Vss9	Vss106	R18
B28	Vss10	Vss107	T6
C2	Vss11	Vss108	T12
C6	Vss12	Vss109	T16
C27	Vss13	Vss110	T13
D10	Vss14	Vss111	T14
D18	Vss15	Vss112	T15
D21	Vss16	Vss113	T17
D24	Vss17	Vss114	T17
E1	Vss18	Vss115	U4
E2	Vss19	Vss116	U13
E4	Vss20	Vss117	U12
E8	Vss21	Vss118	U14
F15	Vss22	Vss119	U15
F3	Vss23	Vss120	U16
F4	Vss24	Vss121	U24
F5	Vss25	Vss122	U25
F12	Vss26	Vss123	U25
F26	Vss27	Vss124	U26
G1	Vss28	Vss125	V13
G2	Vss29	Vss126	V15
G5	Vss30	Vss127	V27
G6	Vss31	Vss128	V24
G9	Vss32	Vss129	V28
G14	Vss33	Vss130	W6
G18	Vss34	Vss131	W24
G21	Vss35	Vss132	W25
G24	Vss36	Vss133	W26
G25	Vss37	Vss134	Y3
G26	Vss38	Vss135	Y24
H3	Vss39	Vss136	Y27
H4	Vss40	Vss137	Y28
H5	Vss41	Vss138	AA1
H24	Vss42	Vss139	AA24
H27	Vss43	Vss140	AA25
H28	Vss44	Vss141	AA26
J2	Vss45	Vss142	AB4
J5	Vss46	Vss143	AB6
J24	Vss47	Vss144	AB11
J25	Vss48	Vss145	AB4
J26	Vss49	Vss146	AB16
K24	Vss50	Vss147	AB19
K27	Vss51	Vss148	AB21
K28	Vss52	Vss149	AB24
L13	Vss53	Vss150	AB27
L15	Vss54	Vss151	AB28
L24	Vss55	Vss152	AC2
L25	Vss56	Vss153	AC5
L26	Vss57	Vss154	AC9
M3	Vss58	Vss155	AC11
M4	Vss59	Vss156	AD1
M5	Vss60	Vss157	AD3
M12	Vss61	Vss158	AD4
M13	Vss62	Vss159	AD7
M14	Vss63	Vss160	AD8
M15	Vss64	Vss161	AD11
M16	Vss65	Vss162	AD15
M17	Vss66	Vss163	AD19
M24	Vss67	Vss164	AD23
M27	Vss68	Vss165	AE2
M28	Vss69	Vss166	AE4
M29	Vss70	Vss167	AE8
M28	Vss71	Vss168	AE11
N1	Vss72	Vss169	AE13
N2	Vss73	Vss170	AE18
N5	Vss74	Vss171	AE21
N6	Vss75	Vss172	AE24
N11	Vss76	Vss173	AE25
N12	Vss77	Vss174	AF4
N13	Vss78	Vss175	AF4
N14	Vss79	Vss176	AF4
N15	Vss80	Vss177	AF11
N16	Vss81	Vss178	AF27
N17	Vss82	Vss179	AF28
N18	Vss83	Vss180	AG1
N24	Vss84	Vss181	AG7
N25	Vss85	Vss182	AG3
N26	Vss86	Vss183	AG11
P3	Vss87	Vss184	AG14
P4	Vss88	Vss185	AG17
P12	Vss89	Vss186	AG20
P13	Vss90	Vss187	AG25
P14	Vss91	Vss188	AH1
P15	Vss92	Vss189	AH3
P16	Vss93	Vss190	AH7
P17	Vss94	Vss191	AH12
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P27	Vss96	Vss193	AH23
P27	Vss97	Vss194	AH27

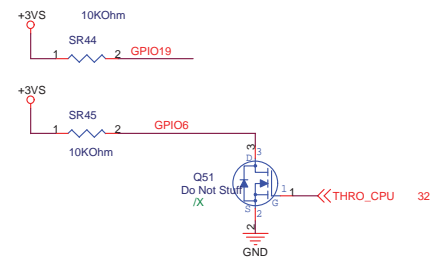
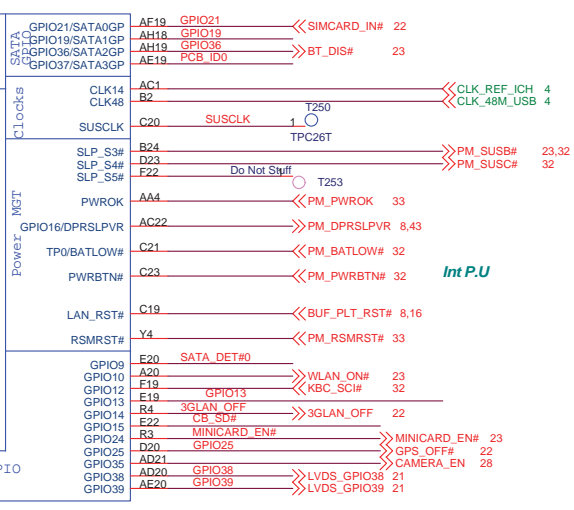
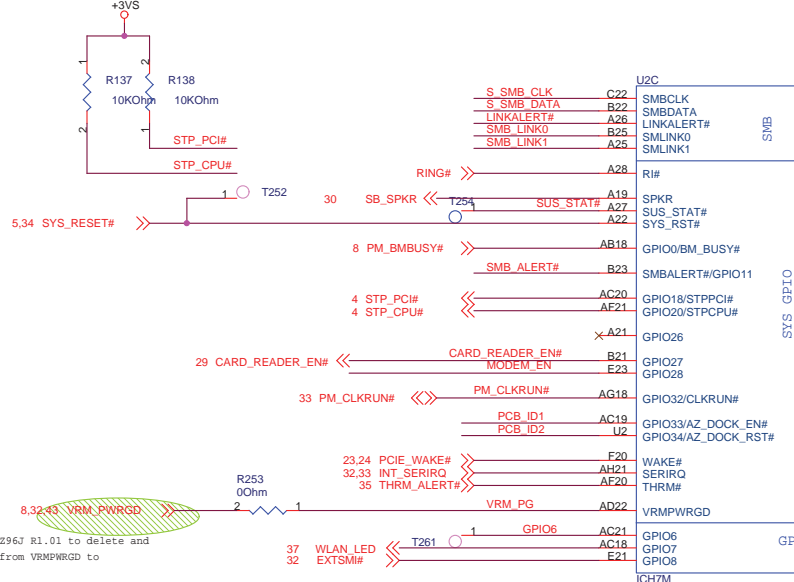
ASUS Title : SB-ICH7M(PWR)
 ASUSTek COMPUTER INC. Engineer: Satan He
 Size Project Name
 Custom P901
 Date: Monday, May 19, 2008 Sheet 14 of 50
 Rev 1.1G

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<http://hobi-elektronika.net>

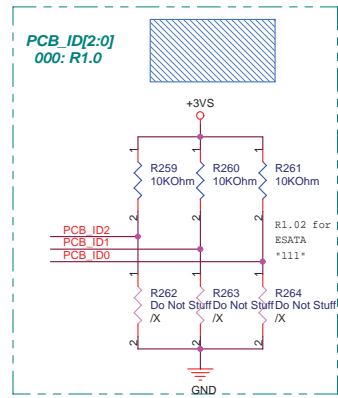
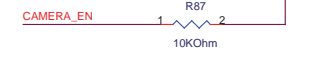
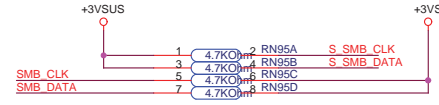
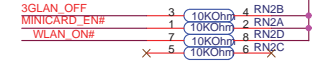
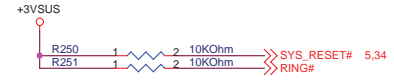
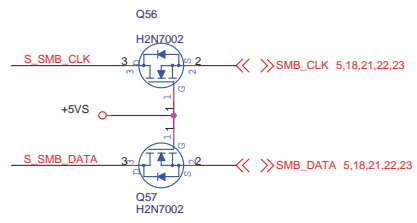
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ASUSTek COMPUTER INC.		Engineer: Satan He	
Size	Project Name	Rev	
Custom	P901	1.1G	
Date: Monday, May 19, 2008	Sheet	15	of 50



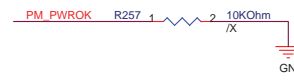
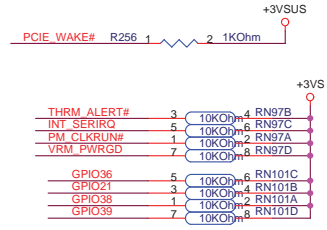
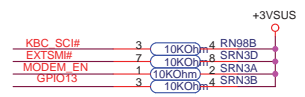
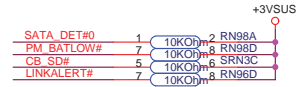
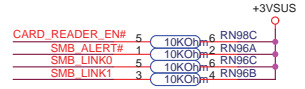
05/12/30, refer Z967 R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.



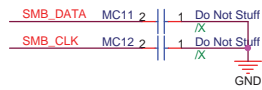
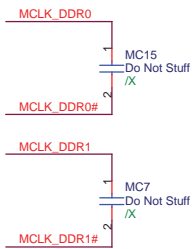
	WLAN_LED	WLAN	BT
High	v	v	v
High	v	v	x
High	x	v	v
Low	x	x	x



PCB_VID3 : PROJECT CODE

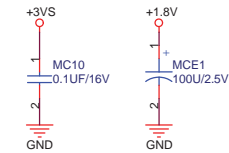
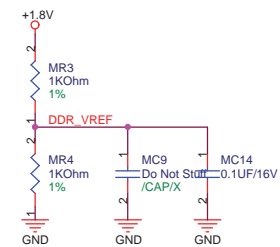
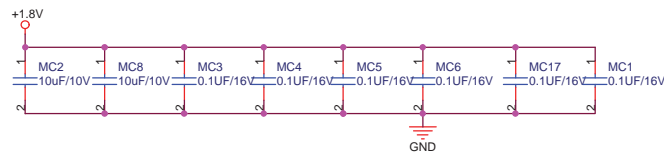


ASUS Title : SB-ICH7M(3)
 ASUSTek COMPUTER INC Engineer: Satan He
 Size Project Name
 Custom P901
 Date: Monday, May 19, 2008 Sheet 17 of 50



STD Type

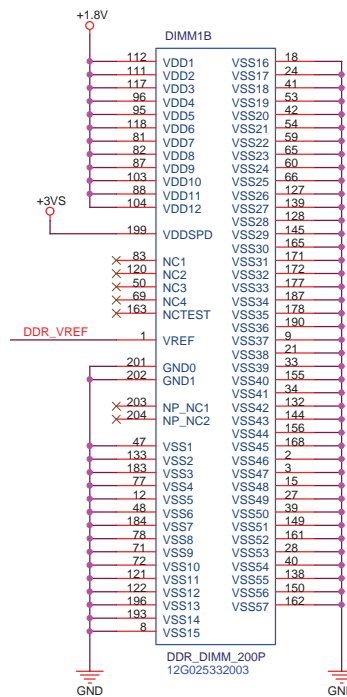
- << >>MA_DQ[63:0] 10
- << >>MA_DQS[7:0] 10
- << >>MA_DQS#[7:0] 10
- << >>MA_DM[7:0] 10
- << >>MA_MA[13:0] 10,19
- << >>MA_BA[2:0] 10,19



DIMM1A			
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	X 86	A14	DQ14
	X 85	A15	DQ15
MA_BA2	X 84	A16_BA2	DQ16
MA_BA0	107	BA0	DQ17
MA_BA1	106	BA1	DQ18
	110	BA2	DQ19
8,19 MA_CS#0	X 115	S0#	DQ20
8,19 MA_CS#1	X 114	S1#	DQ21
8 MCLK_DDR0	30	CK0	DQ22
8 MCLK_DDR0#	32	CK0#	DQ23
8 MCLK_DDR1	164	CK1	DQ24
8 MCLK_DDR1#	166	CK1#	DQ25
8,19 MA_KE0	79	CKE0	DQ26
8,19 MA_KE1	80	CKE1	DQ27
10,19 MA_CAS#	113	CAS#	DQ28
10,19 MA_RAS#	108	RAS#	DQ29
10,19 MA_WE#	109	WE#	DQ30
	198	SA0	DQ31
	200	SA1	DQ32
5,17,21,22,23 SMB_CLK	X 197	SCL	DQ33
5,17,21,22,23 SMB_DATA	X 195	SDA	DQ34
		DQ35	DQ35
8,19 MA_ODT0	X 114	ODT0	DQ36
8,19 MA_ODT1	X 119	ODT1	DQ37
		DQ38	DQ38
MA_DM0	10	DM0	DQ39
MA_DM2	26	DM1	DQ40
MA_DM1	52	DM2	DQ41
MA_DM3	67	DM3	DQ42
MA_DM4	140	DM4	DQ43
MA_DM5	147	DM5	DQ44
MA_DM6	170	DM6	DQ45
MA_DM7	185	DM7	DQ46
		DQ47	DQ47
MA_DQS0	13	DQS0	DQ48
MA_DQS2	31	DQS1	DQ49
MA_DQS1	51	DQS2	DQ50
MA_DQS3	70	DQS3	DQ51
MA_DQS4	131	DQS4	DQ52
MA_DQS5	148	DQS5	DQ53
MA_DQS6	169	DQS6	DQ54
MA_DQS7	188	DQS7	DQ55
MA_DQS#0	11	DQS#0	DQ56
MA_DQS#2	29	DQS#1	DQ57
MA_DQS#1	49	DQS#2	DQ58
MA_DQS#3	68	DQS#3	DQ59
MA_DQS#4	129	DQS#4	DQ60
MA_DQS#5	146	DQS#5	DQ61
MA_DQS#6	167	DQS#6	DQ62
MA_DQS#7	186	DQS#7	DQ63

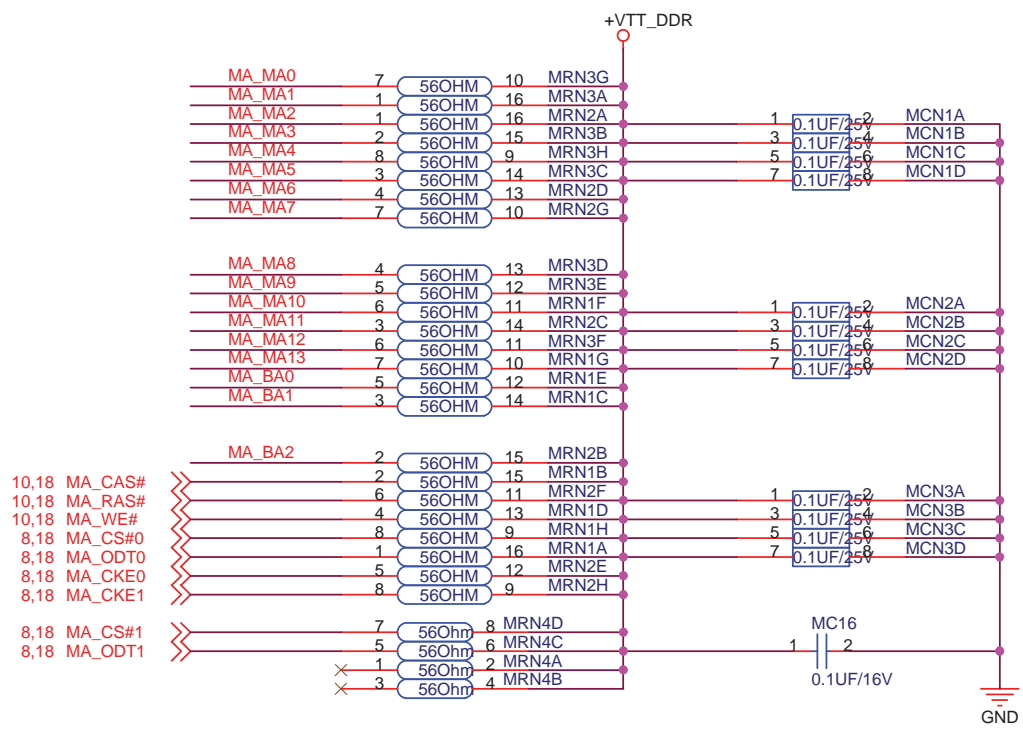
DDR_DIMM_200P
12G025332003

GROUP1
GROUP2
SWAP



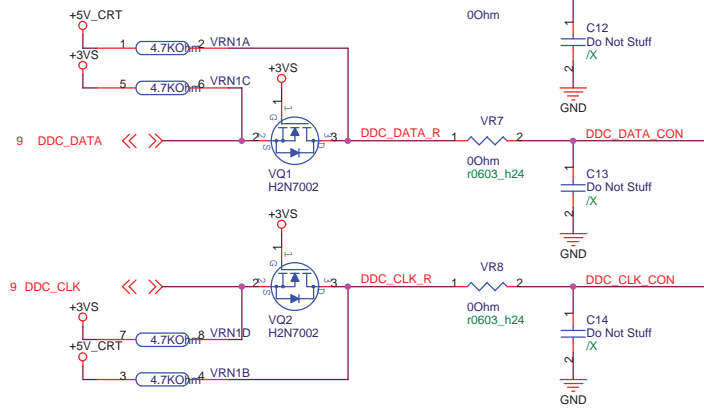
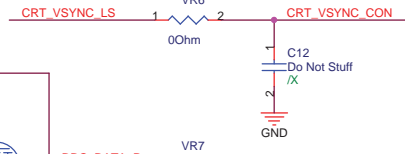
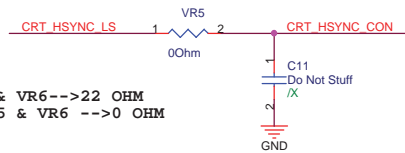
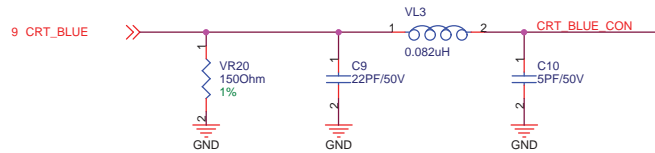
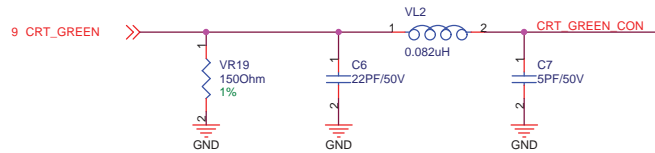
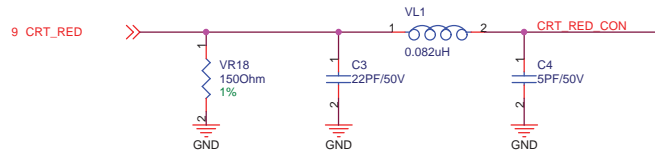
DDR_DIMM_200P
12G025332003

<< MA_MA[13:0] 10,18
<< MA_BA[2:0] 10,18

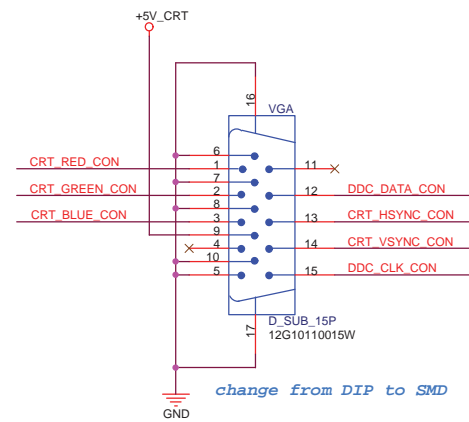


<http://hobi-elektronika.net>

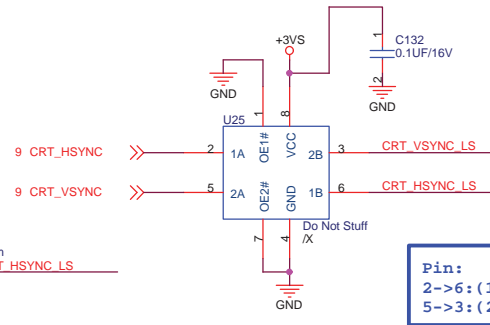
ASUS		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A4	Project Name P901		Rev 1.1G
Date: Monday, May 19, 2008		Sheet 19 of 47	



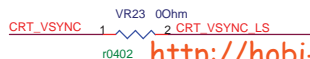
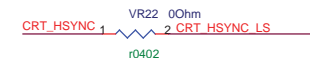
U25上:VR5 & VR6-->22 OHM
U25 /X :VR5 & VR6 -->0 OHM



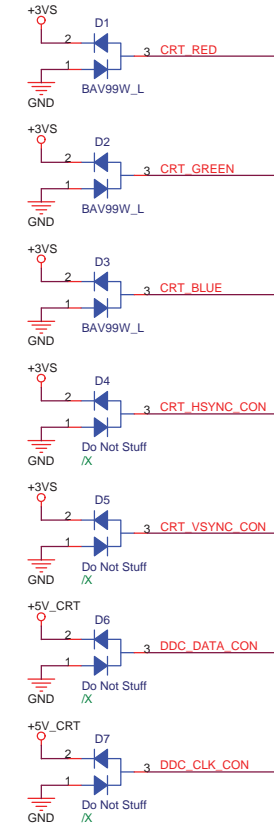
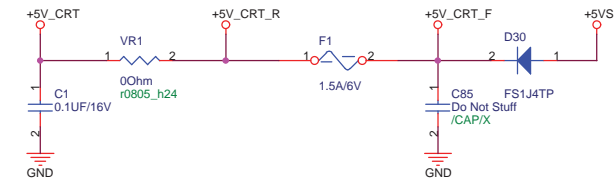
VGA use 12G10110015W & 12G10110015N



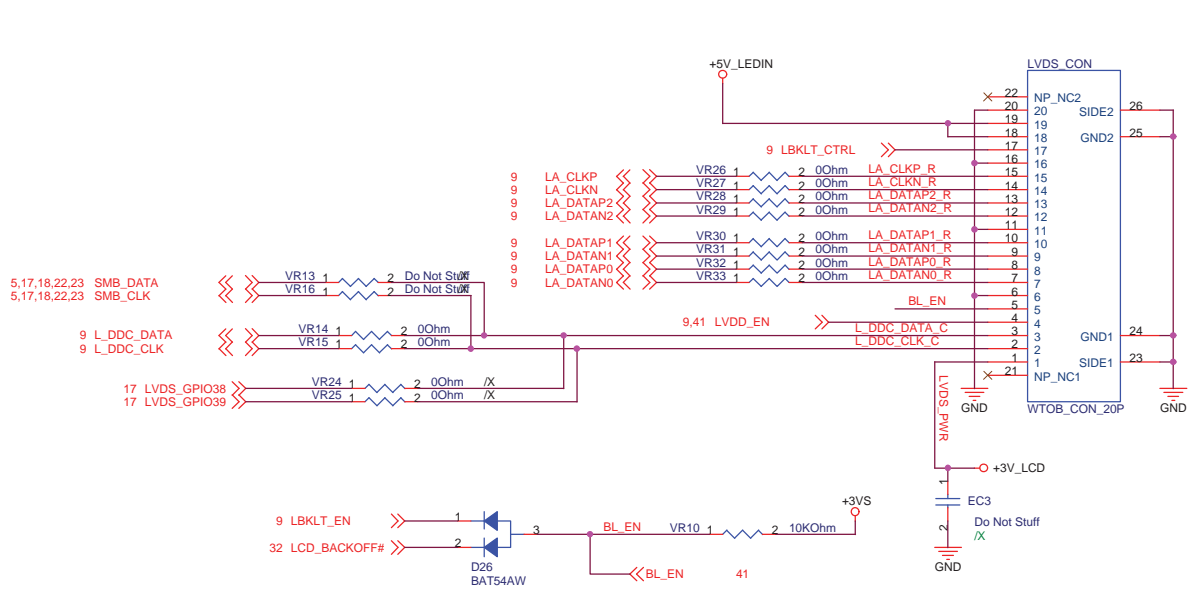
Pin:
2->6: (1A->1B)
5->3: (2A->2B)



<http://hobi-elektronika.net>

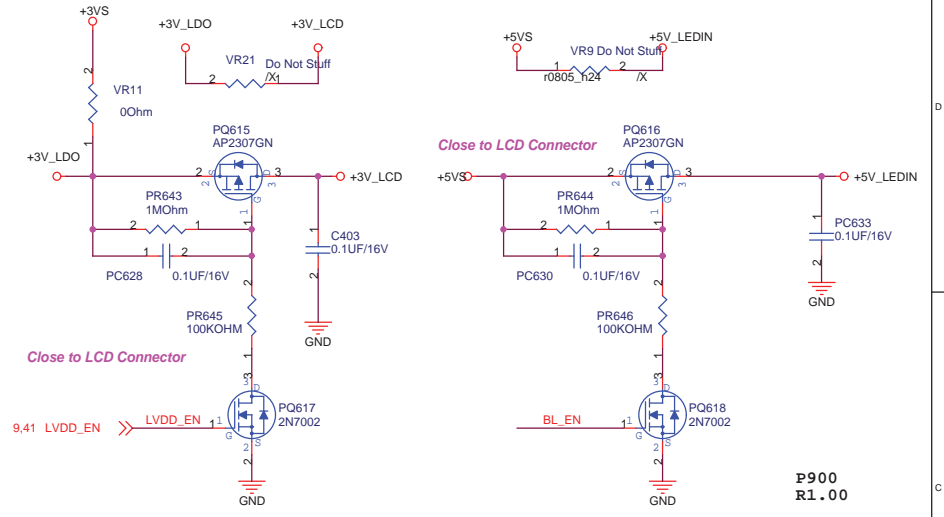
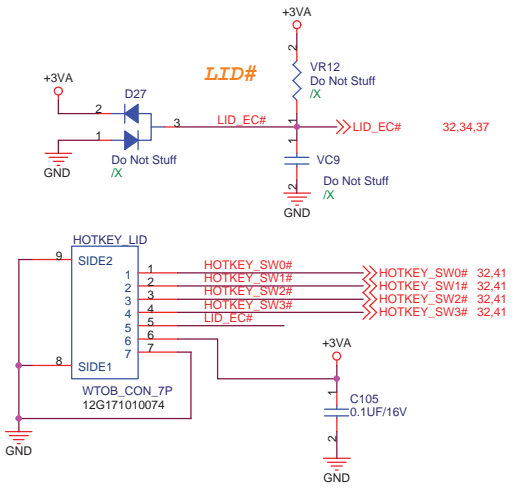


ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008	Sheet	20 of 47	

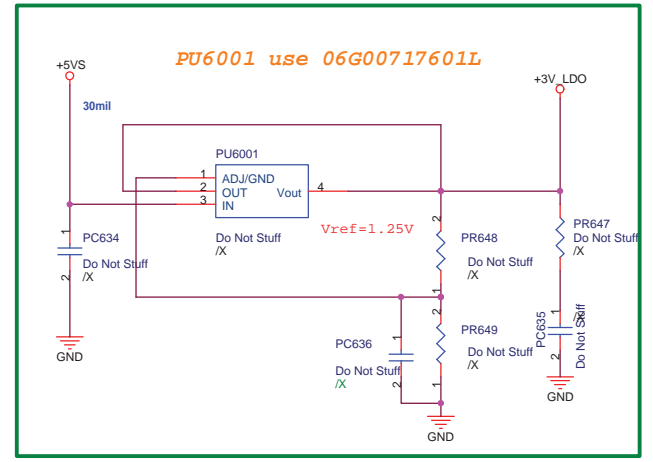


5,17,18,22,23 SMB_DATA
5,17,18,22,23 SMB_CLK
9 L_DDC_DATA
9 L_DDC_CLK
17 LVDS_GPIO38
17 LVDS_GPIO39

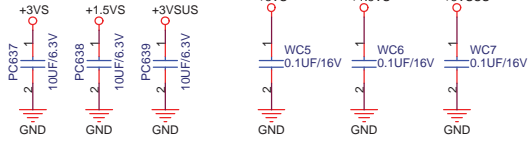
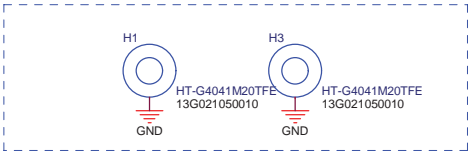
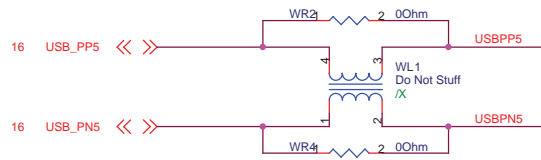
L_DDC_CLK_C	EC1	2	1	Do Not Stuff	/X
L_DDC_DATA_C	EC2	2	1	Do Not Stuff	/X
LA_CLKP_R	VC1	2	1	Do Not Stuff	/X
LA_CLKN_R	VC2	2	1	Do Not Stuff	/X
LA_DATAP2_R	VC3	2	1	Do Not Stuff	/X
LA_DATAN2_R	VC4	2	1	Do Not Stuff	/X
LA_DATAP1_R	VC5	2	1	Do Not Stuff	/X
LA_DATAN1_R	VC6	2	1	Do Not Stuff	/X
LA_DATAP0_R	VC7	2	1	Do Not Stuff	/X
LA_DATAN0_R	VC8	2	1	Do Not Stuff	/X



P900
R1.00

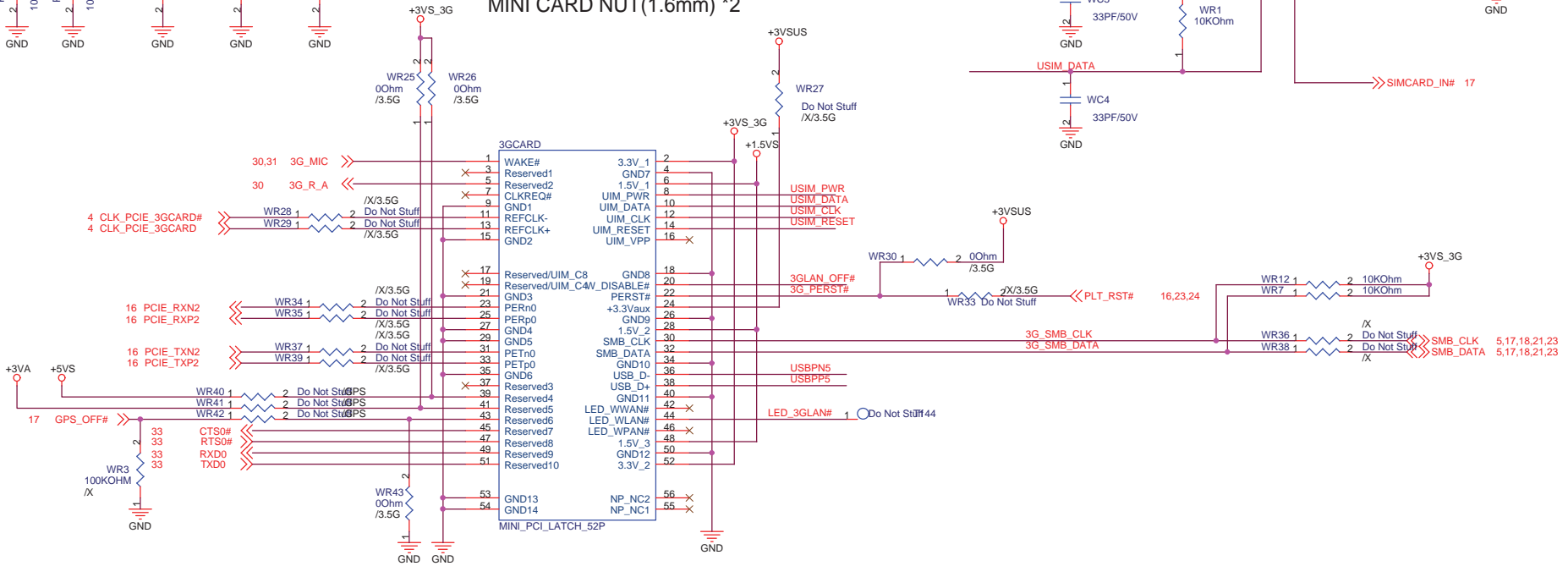
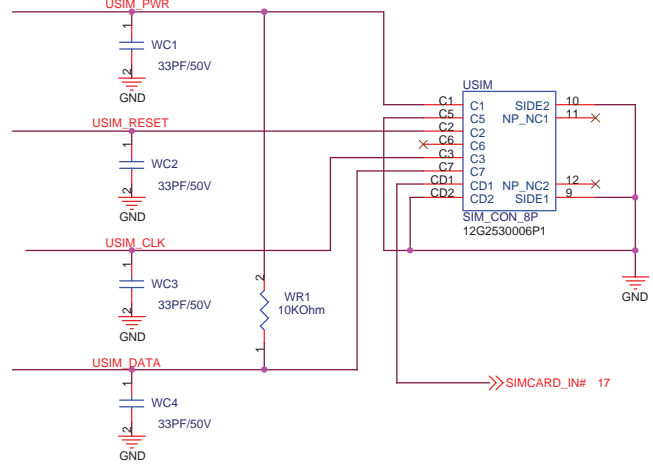


<http://hobi-elektronika.net>



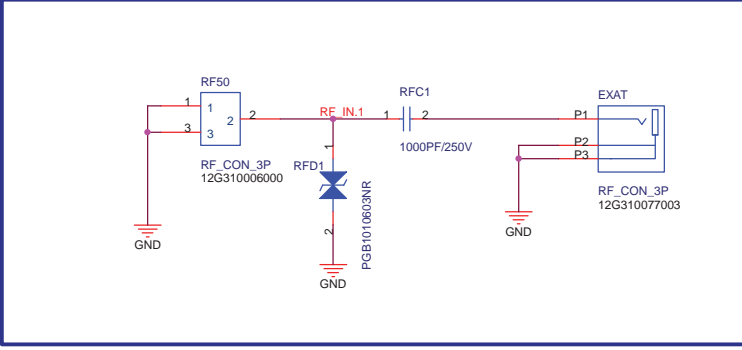
MINI CARD NUT(1.6mm) *2

CAP
Near
SIM
Socket

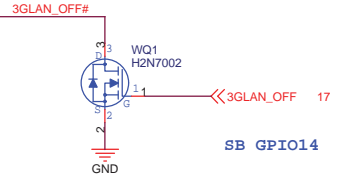
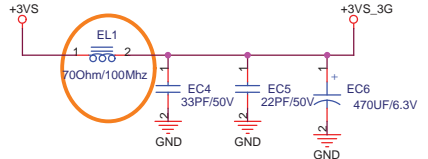


MINICARD use 12G03010052Q

External Antenna



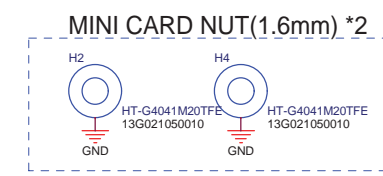
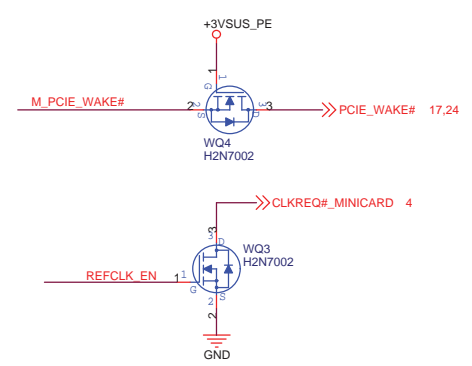
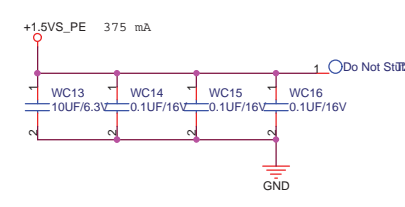
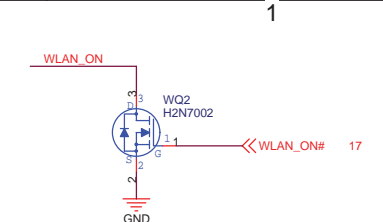
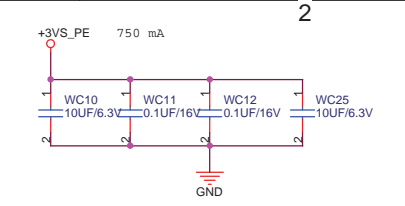
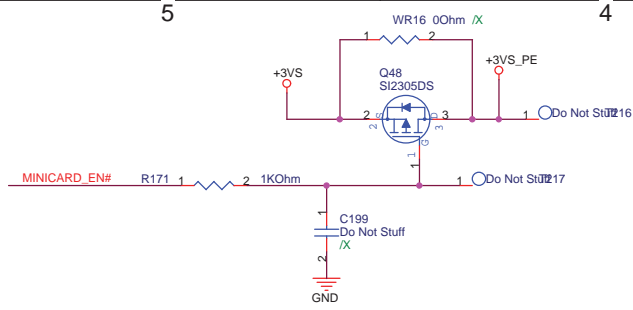
2008/03/11 change



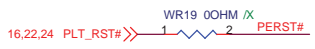
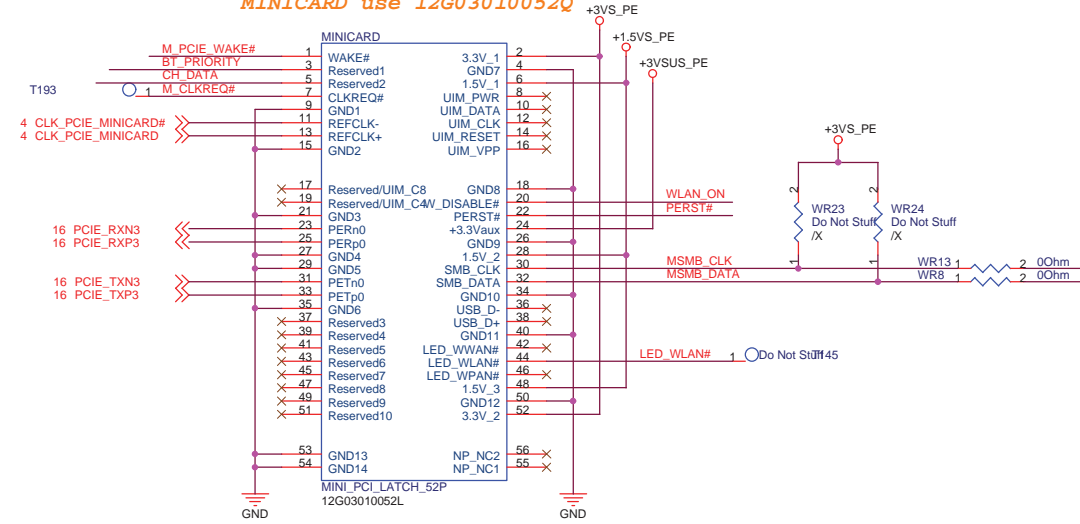
SB GPIO14

<http://hobi-elektronika.net>

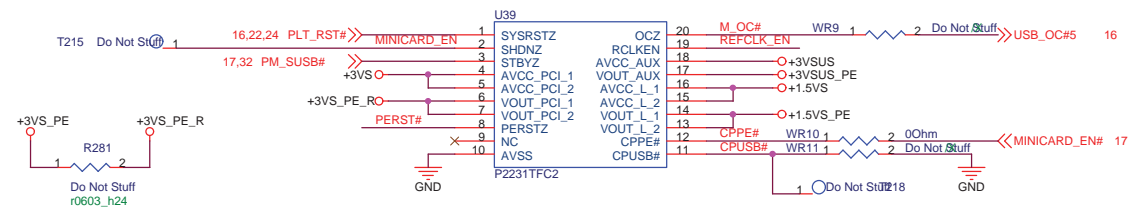
ASUS 3.5G Module & External Antenna
Title :
 ASUSTek Computer INC. **Engineer: Kell Huang**
 Size A3 Project Name **P901** Rev 1.1G
 Date: Monday, May 19, 2008 Sheet 22 of 47



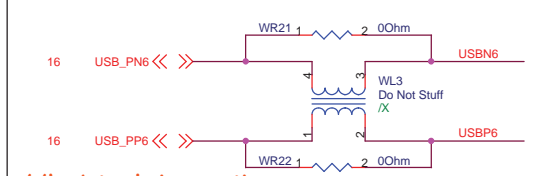
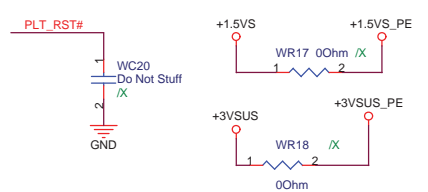
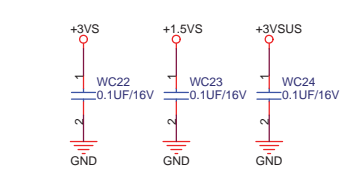
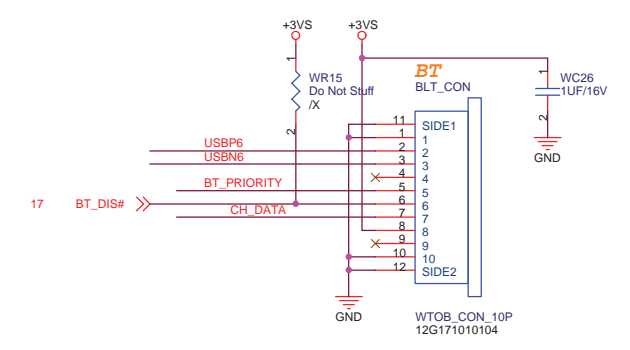
MINICARD use 12G03010052Q



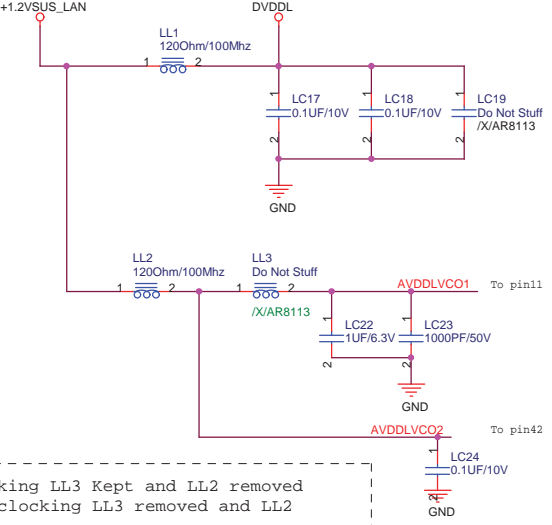
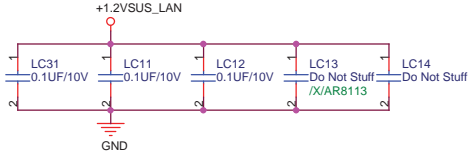
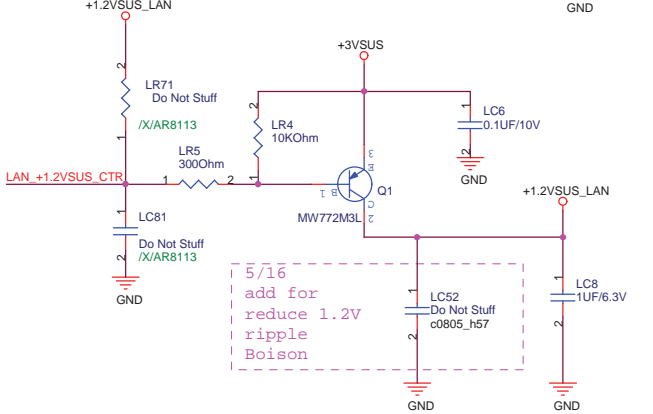
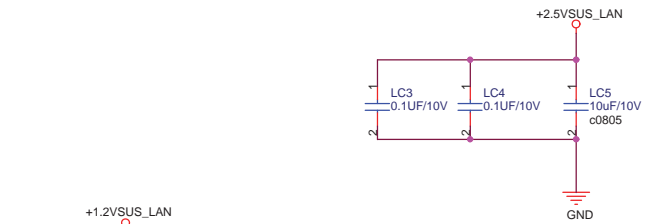
U39 use 06G030057011



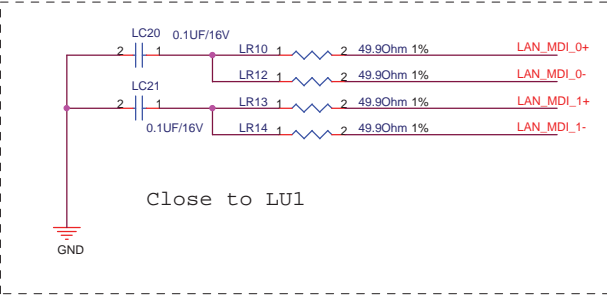
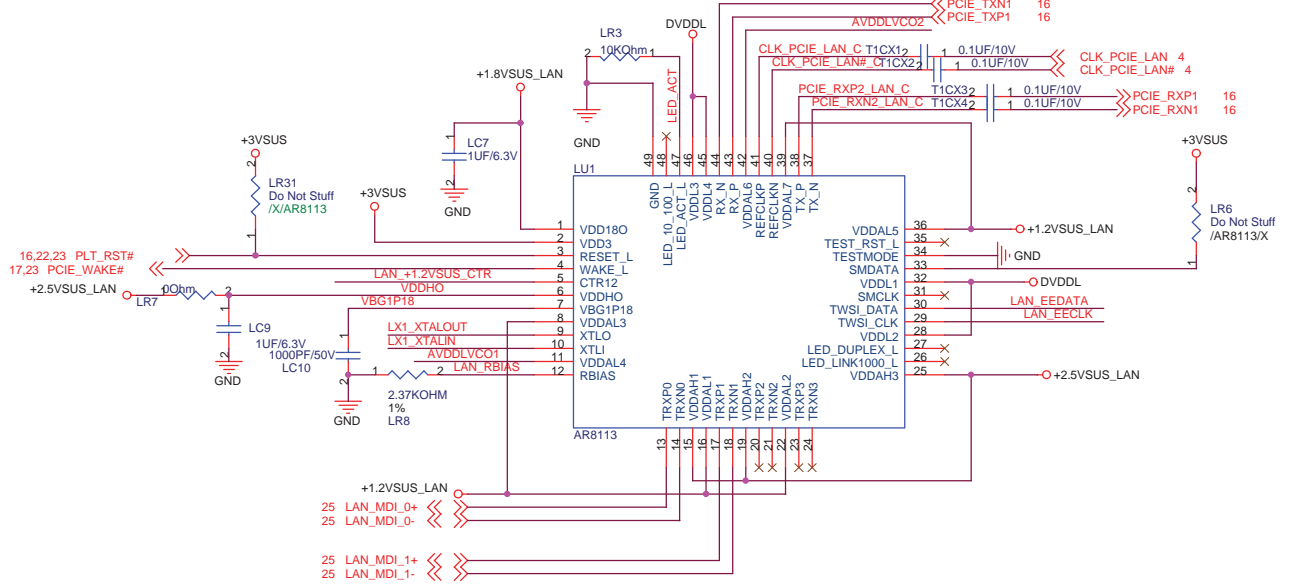
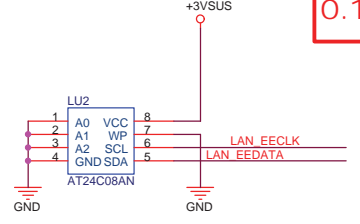
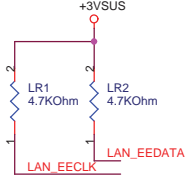
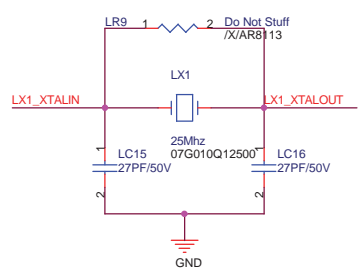
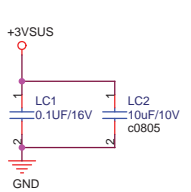
BlueTooth



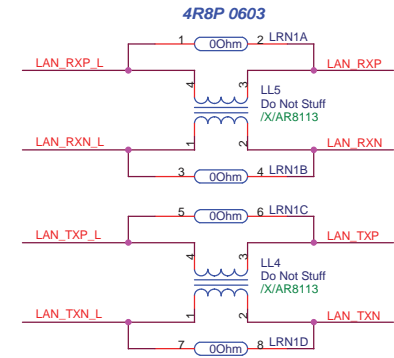
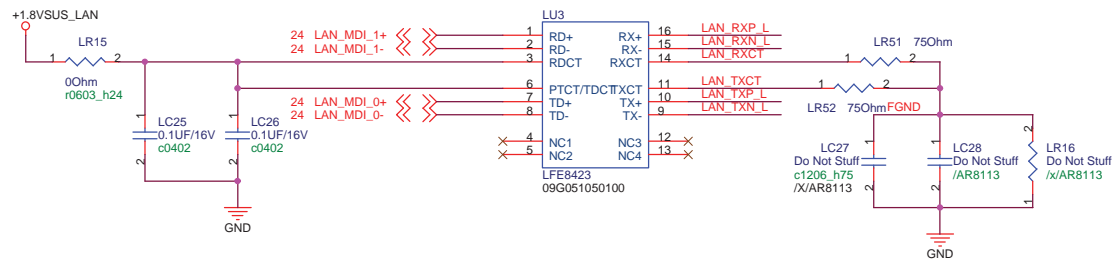
<http://hobi-elektronika.net>



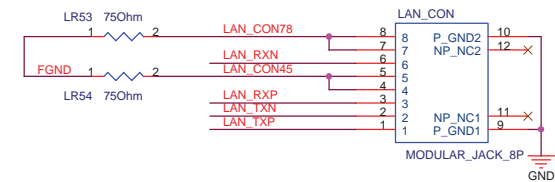
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept

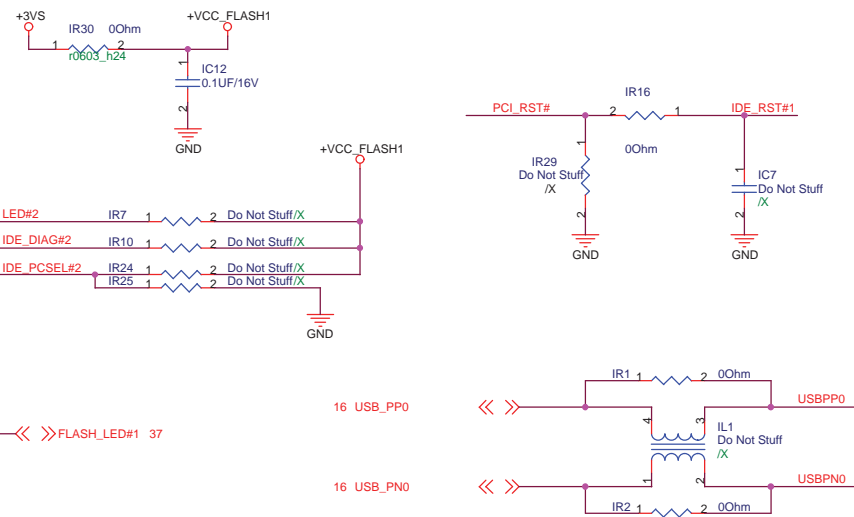
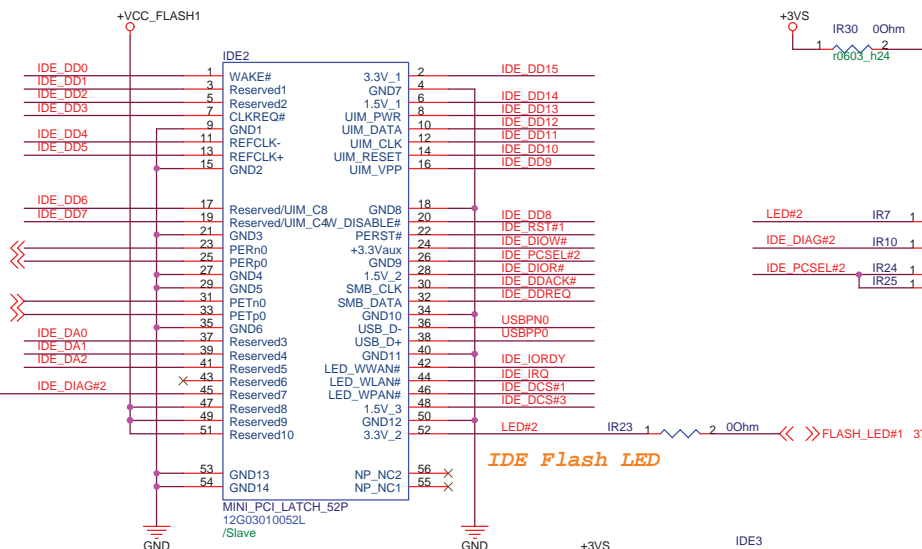
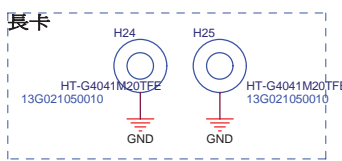
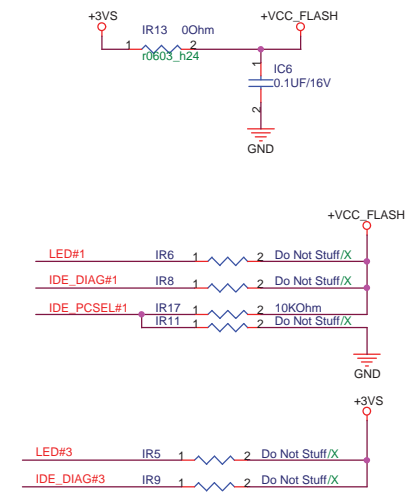
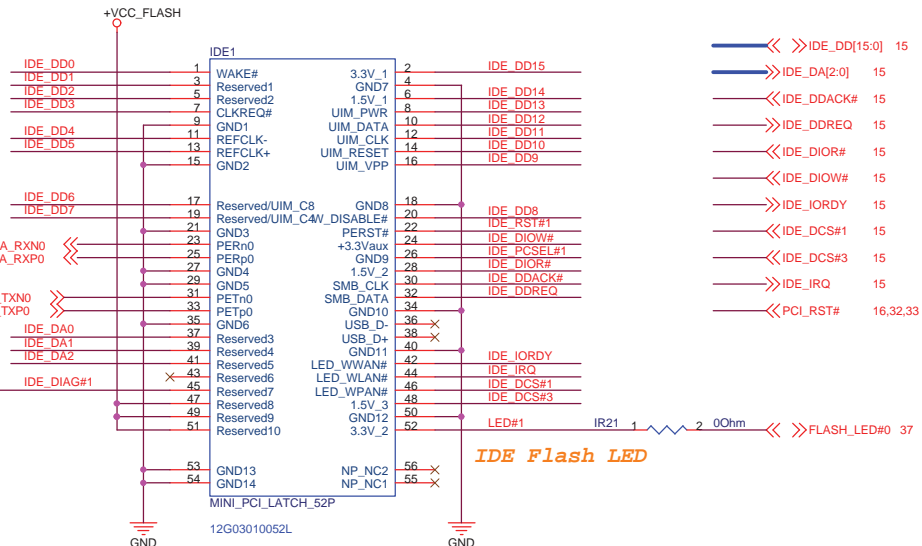
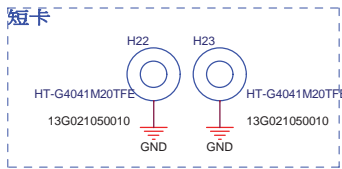


Close to LU1

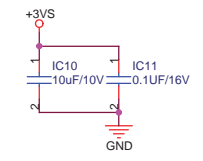
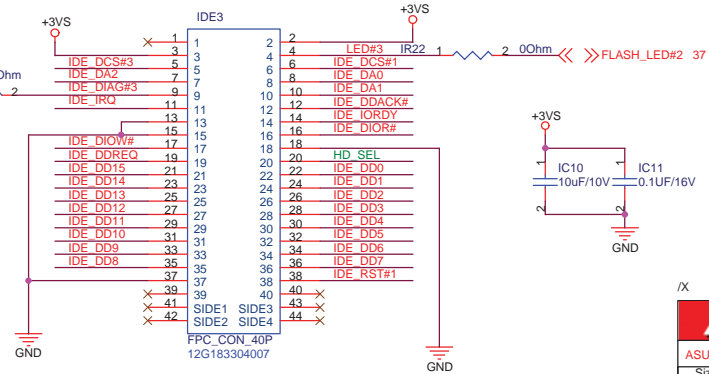
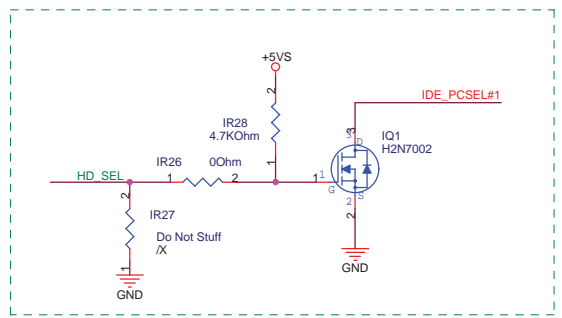


LAN connector: 12G148301086





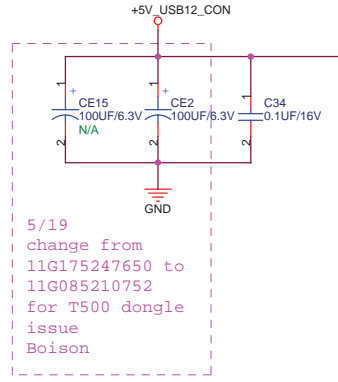
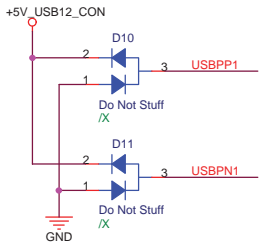
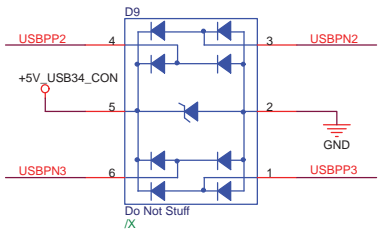
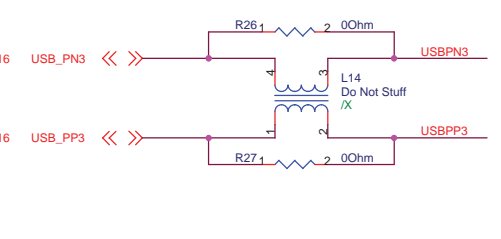
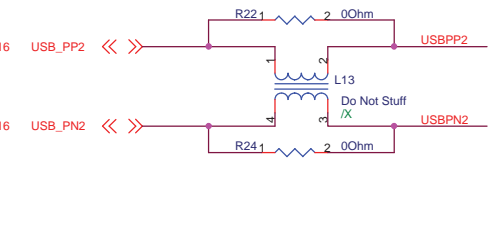
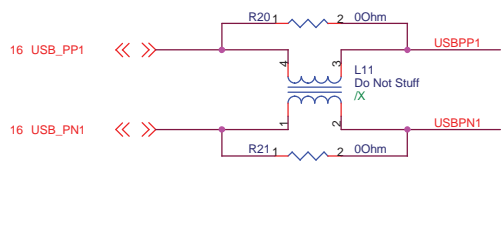
HD Master/Slave:
 Master:Low
 Slave :NC or High
 Default :High



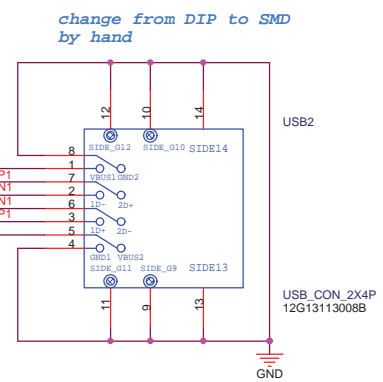
Naming Rule:
 IC: IU?
 R: IR?
 C: IC?
 L: IL?

<http://hobi-elektronika.net>

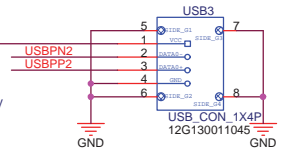
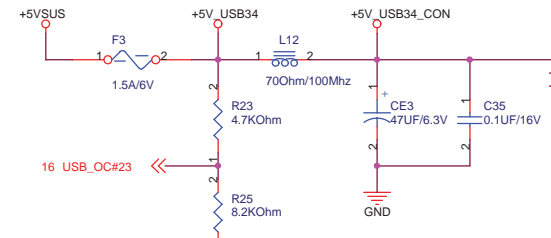
ASUS		Title : HD + Flash Conn	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size A3	Project Name P901	Date: Monday, May 19, 2008	Rev 1.1G
		Sheet	26 of 47



5/19
change from
11G175247650 to
11G085210752
for T500 dongle
issue
Boison



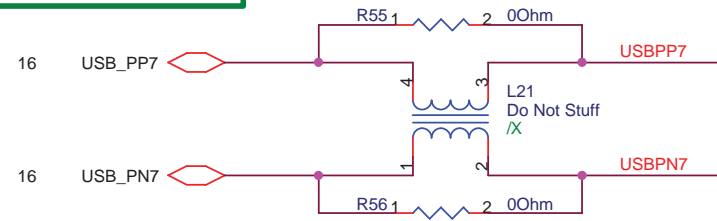
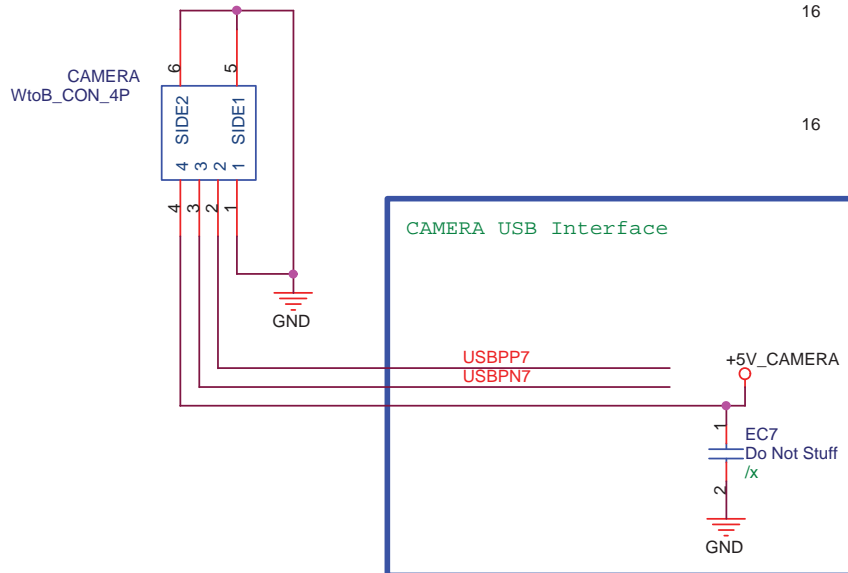
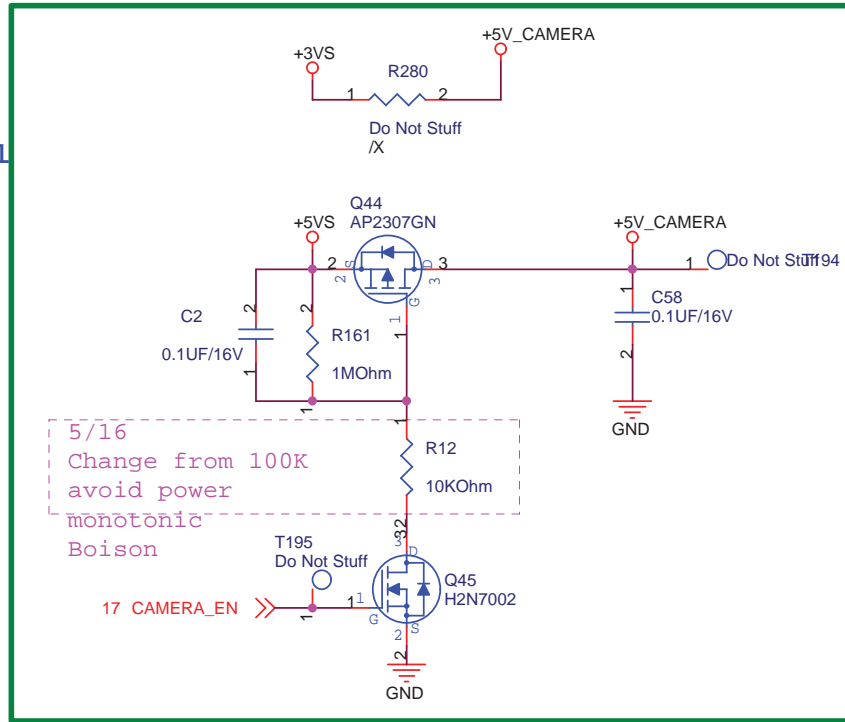
change from DIP to SMD
by hand



change from DIP to SMD

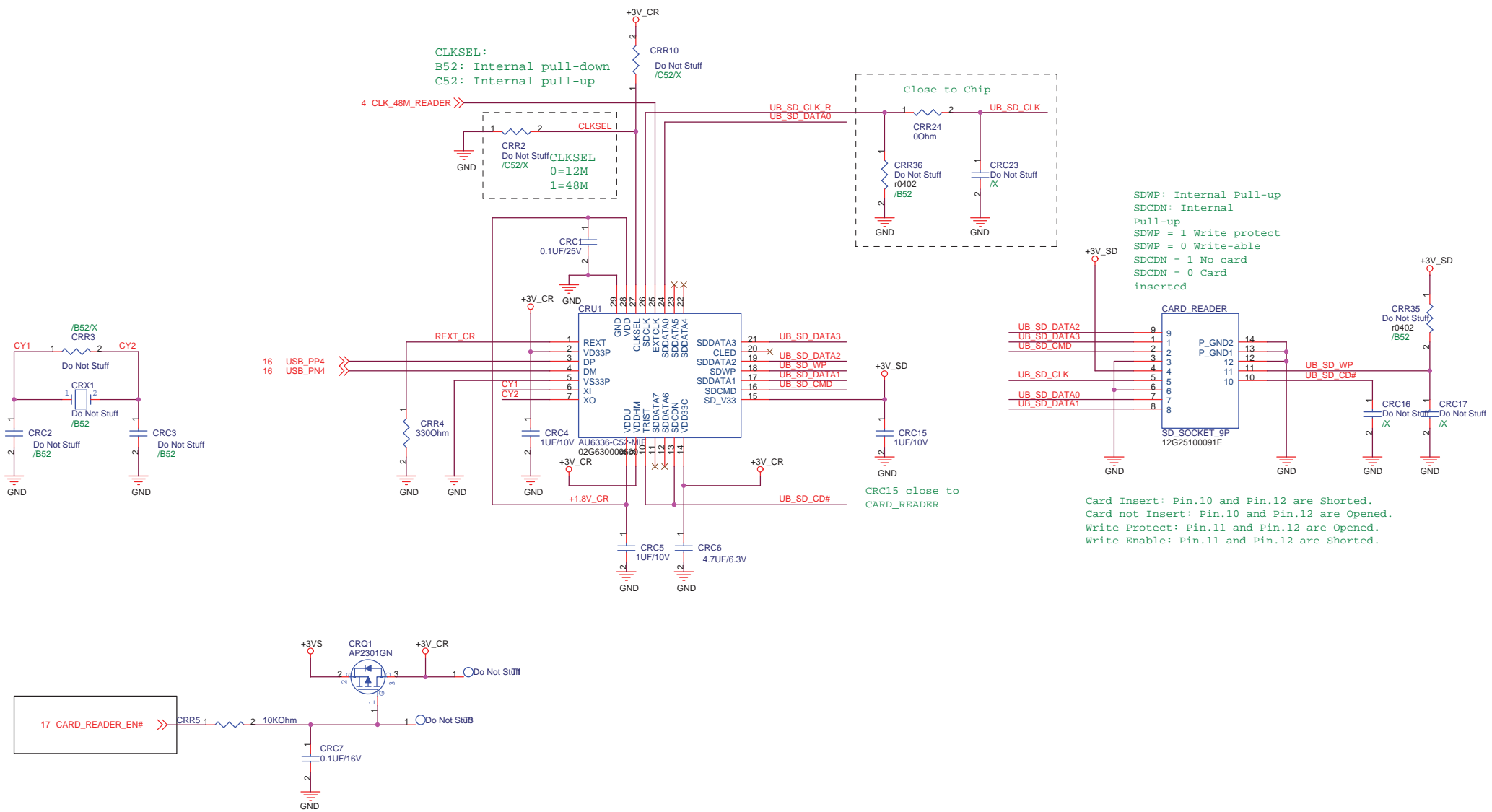
change from DIP to SMD

Power Control



<http://hobi-elektronika.net>

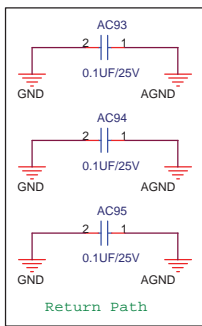
ASUS		Title : Camera Power	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A4	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008		Sheet 28 of 47	



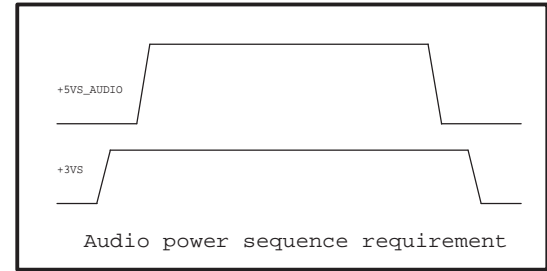
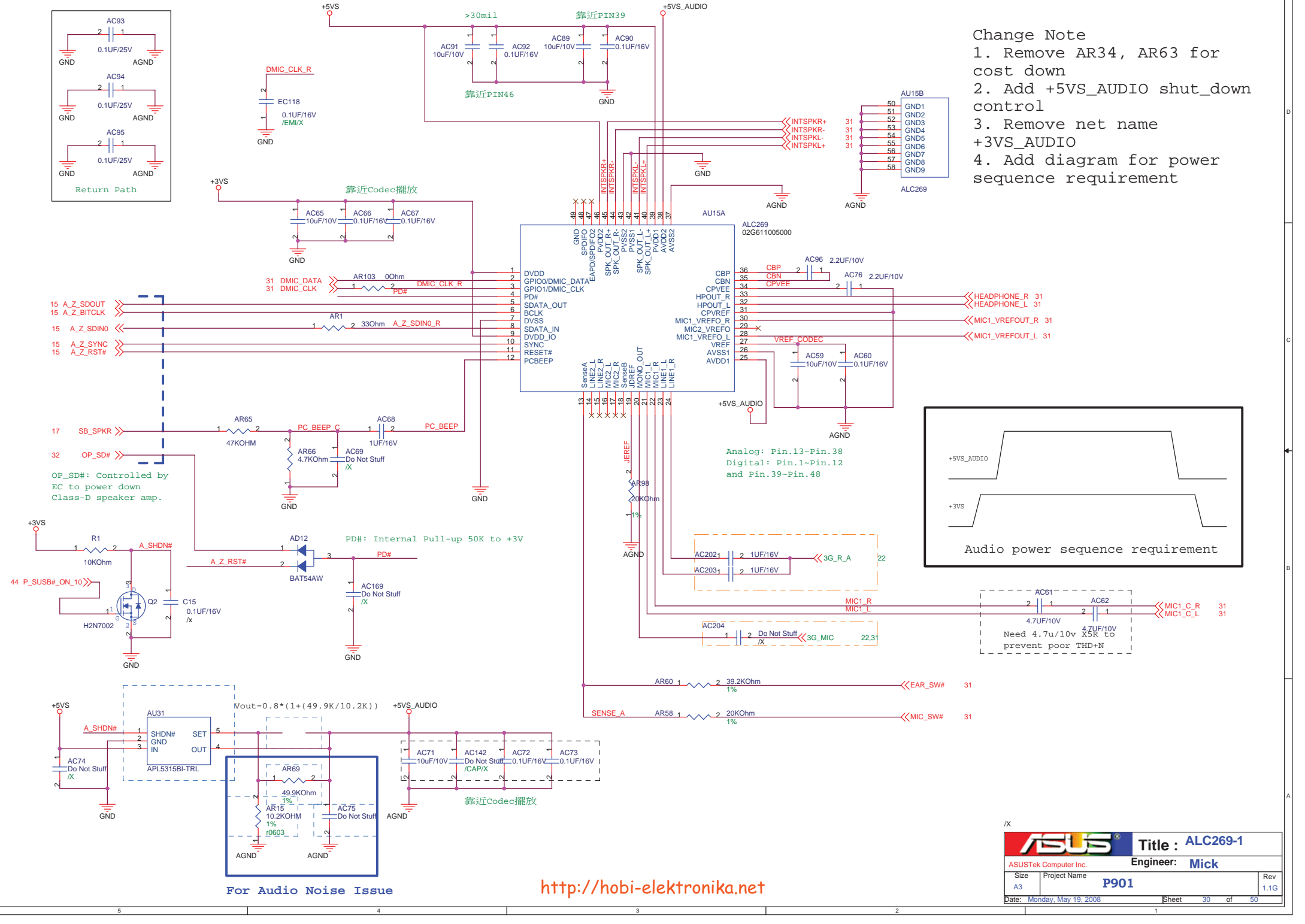
CLKSEL:
 B52: Internal pull-down
 C52: Internal pull-up

SDWP: Internal Pull-up
 SDCDN: Internal
 Pull-up
 SDWP = 1 Write protect
 SDWP = 0 Write-able
 SDCDN = 1 No card
 SDCDN = 0 Card inserted

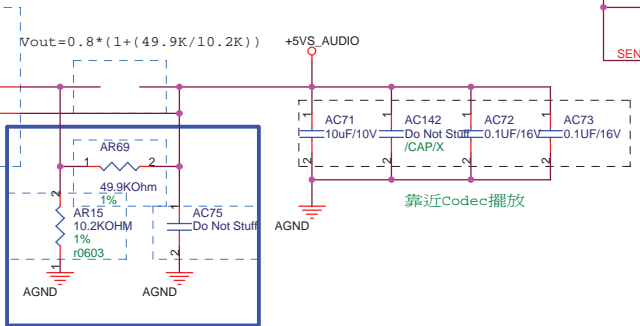
Card Insert: Pin.10 and Pin.12 are Shorted.
 Card not Insert: Pin.10 and Pin.12 are Opened.
 Write Protect: Pin.11 and Pin.12 are Opened.
 Write Enable: Pin.11 and Pin.12 are Shorted.



- Change Note
1. Remove AR34, AR63 for cost down
 2. Add +5VS_AUDIO shut_down control
 3. Remove net name +3VS_AUDIO
 4. Add diagram for power sequence requirement

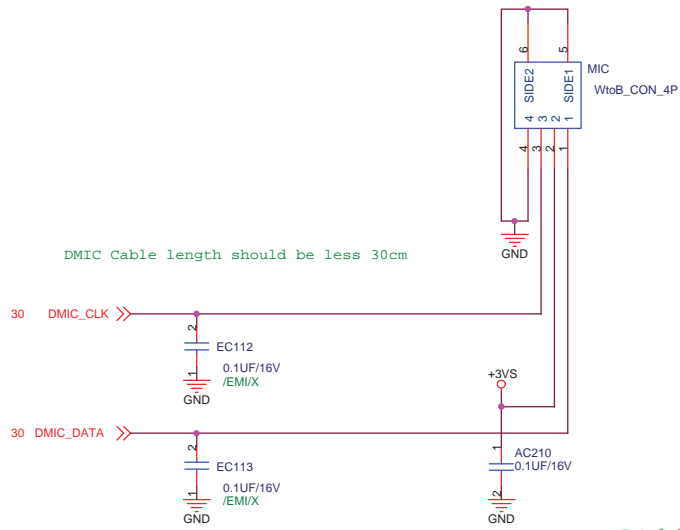


Need 4.7u/10V X5R to prevent poor THD+N

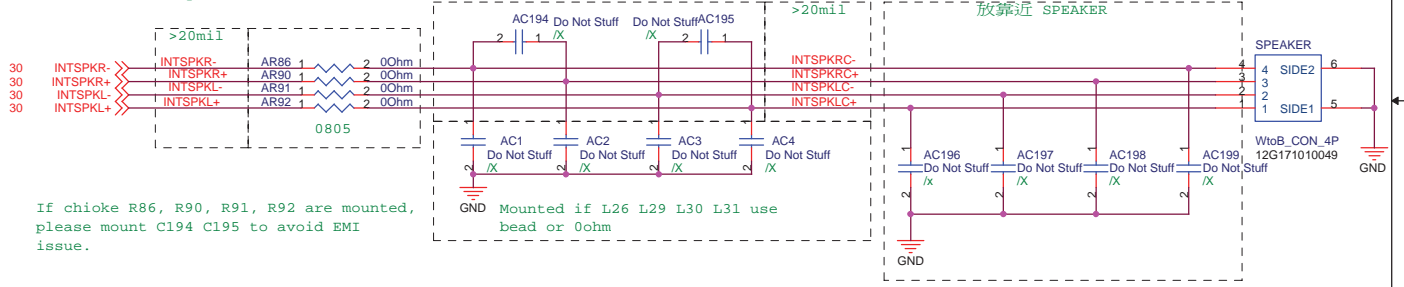


<http://hobi-elektronika.net>

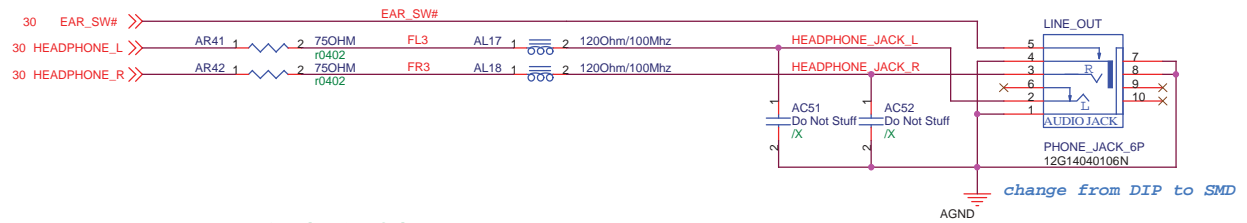
ASUS		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer: Mick	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008	Sheet 30 of 50		



Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)

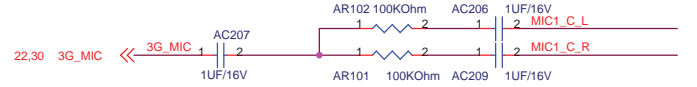
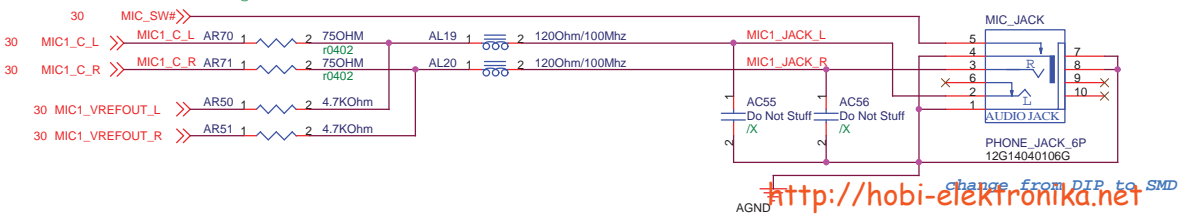


LINE_OUT use 12G14040106N



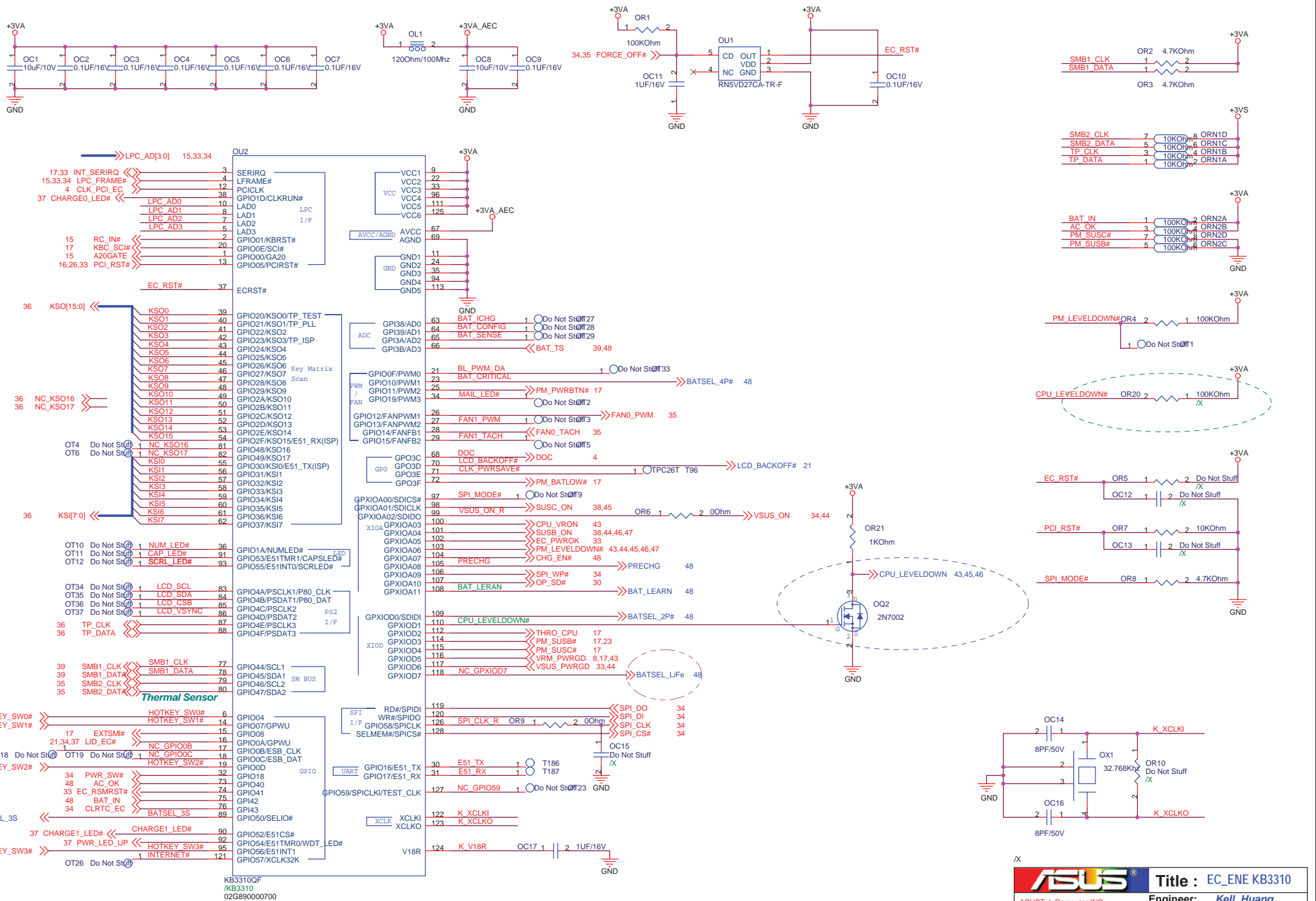
R70 and R71: If don't need retasking function, change to 1K.

MIC_JACK use 12G14040106G



<http://hobi-elektronika.net>

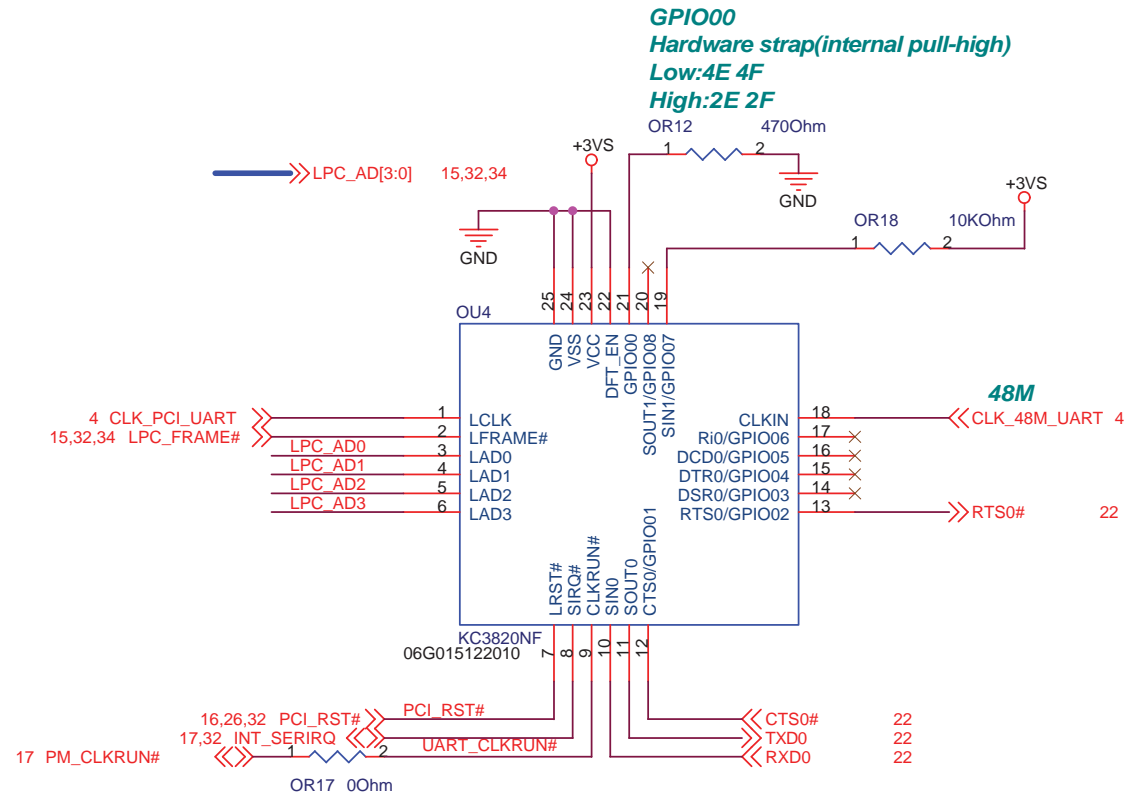
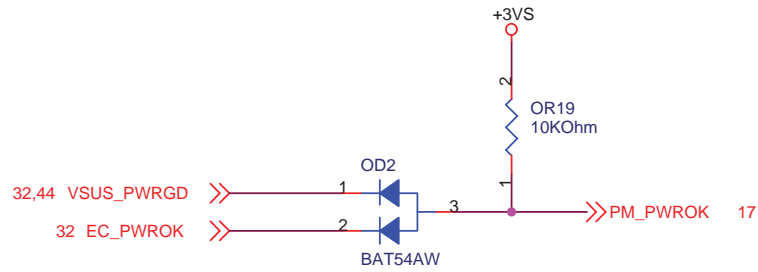
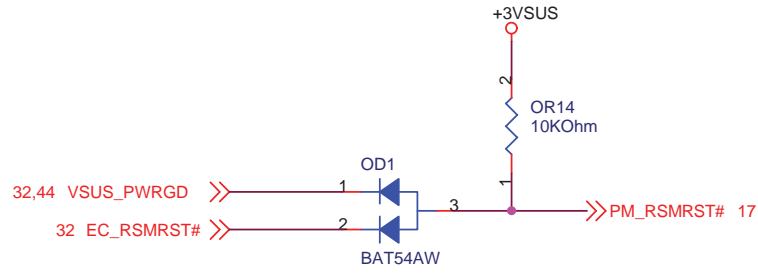
ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008	Sheet	31	of 50



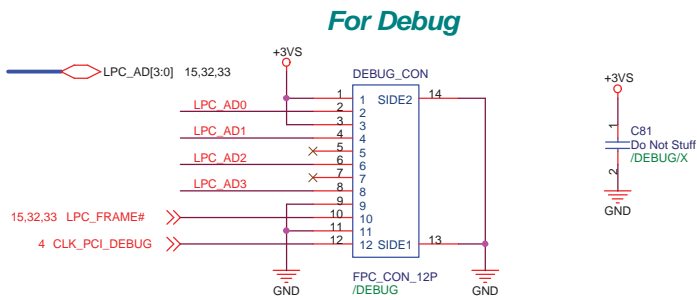
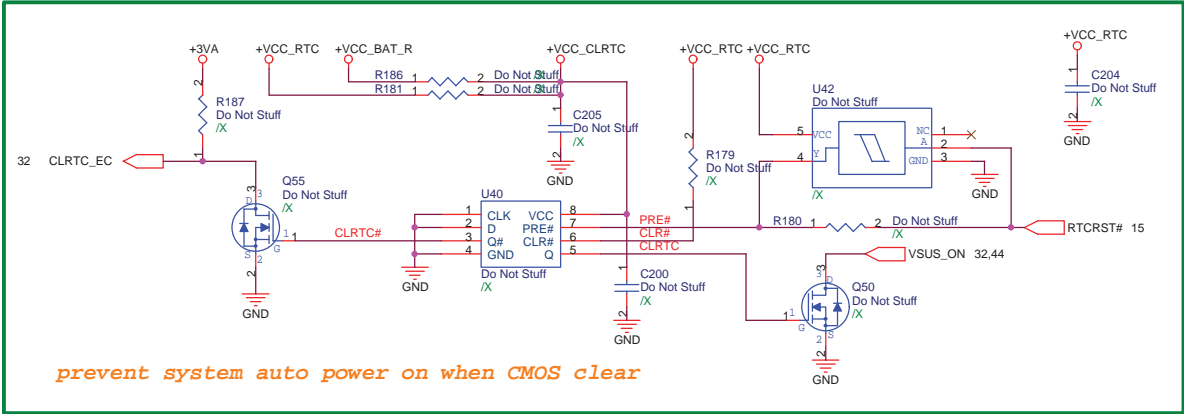
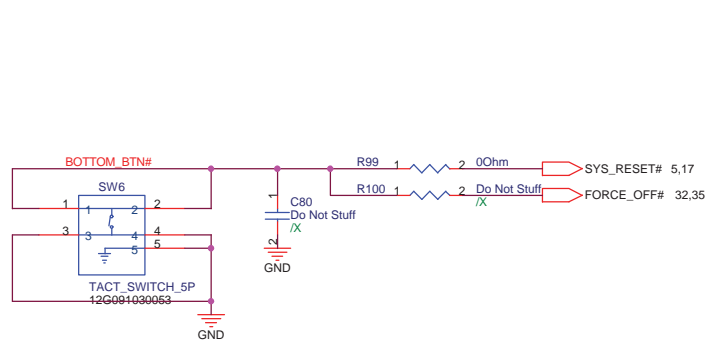
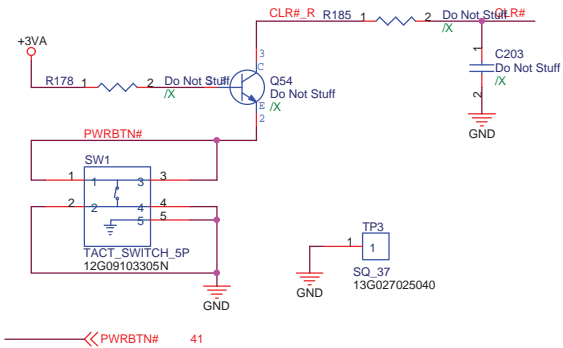
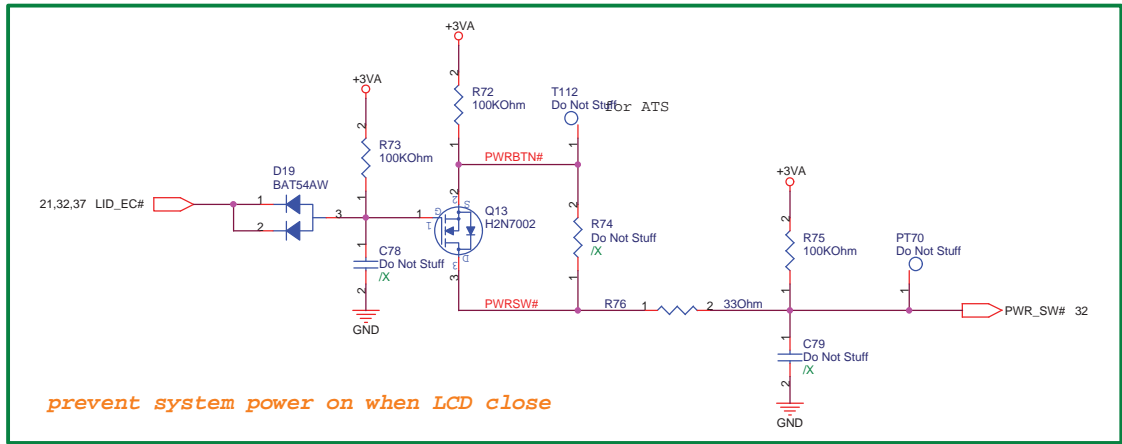
ASUS		Title : EC_ENE KB3310	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size A3	Project Name P901	Date: Monday, May 19, 2008	Rev 1.1G
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<http://hobi-elektronika.net>

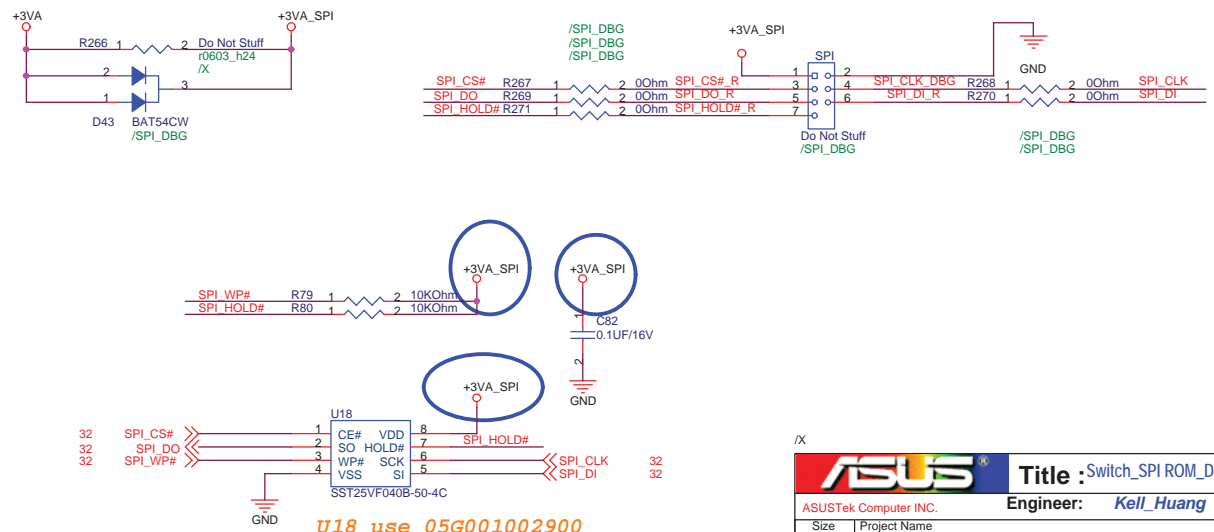
R1.2G to resolve auto-boot issue



UART Control IC for using GPS module due to no UART on ENE EC

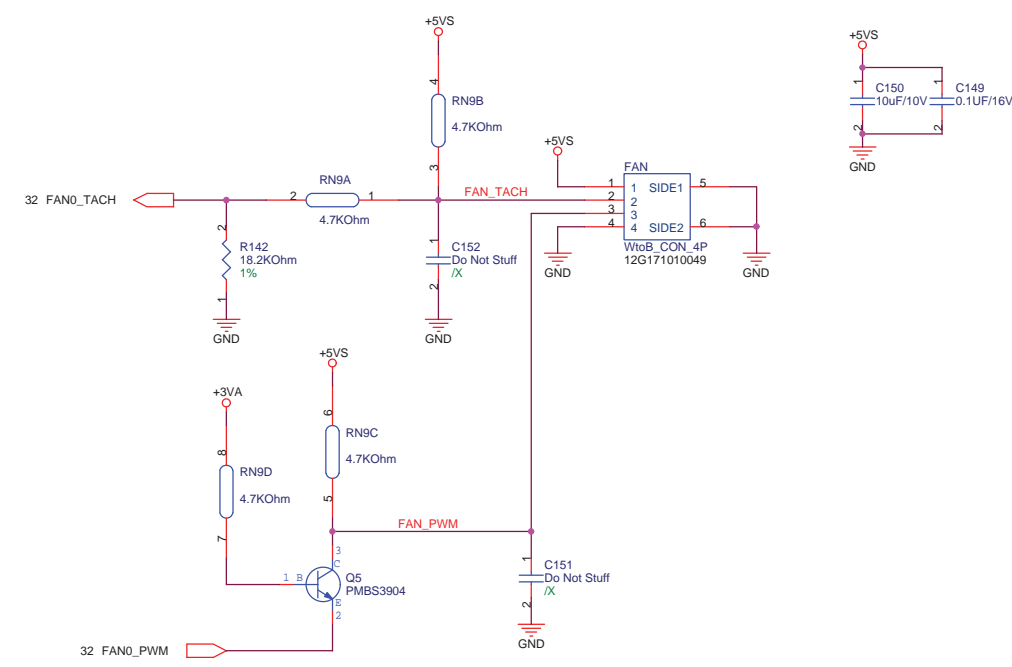
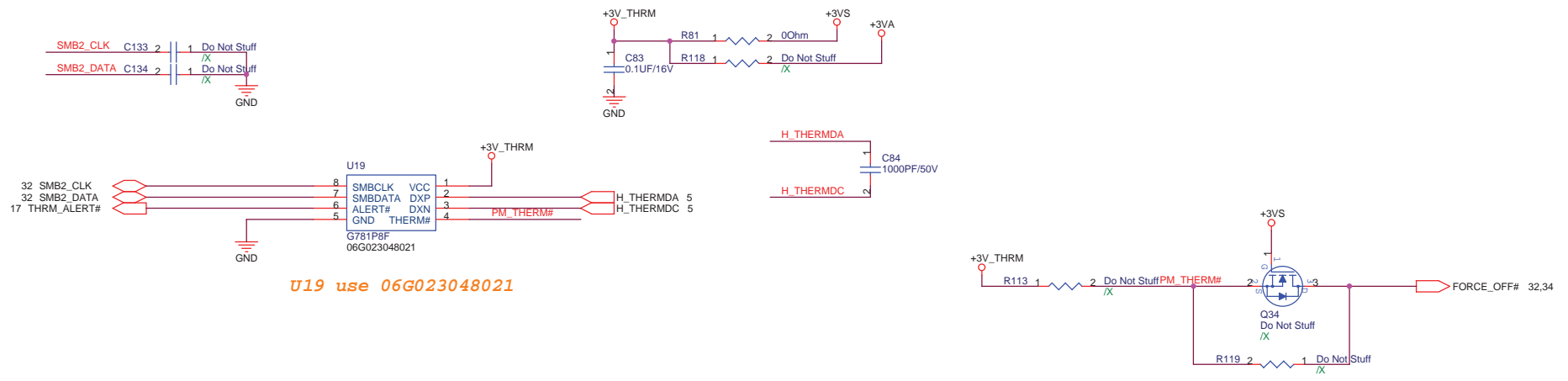


Debug Card cable use Z96 Touch Pad cable, P/N:
 14G124110126, 14G124110120, 14G124110121
 14G124110124, 14G124110125



U18 use 05G00100290
 and 0100F130

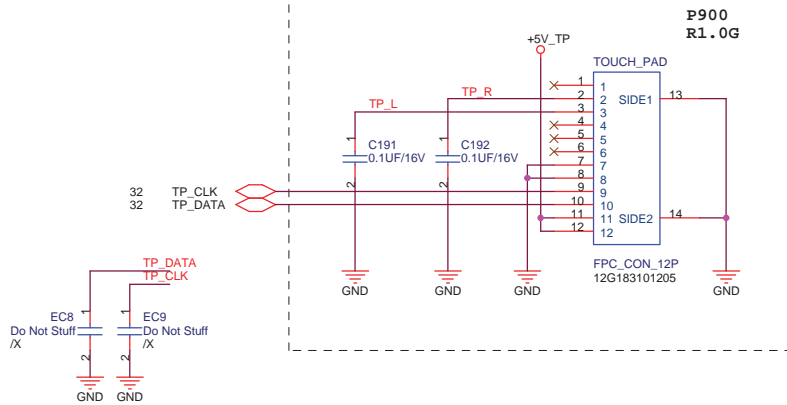
ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Keli Huang	
Size	Project Name		Rev
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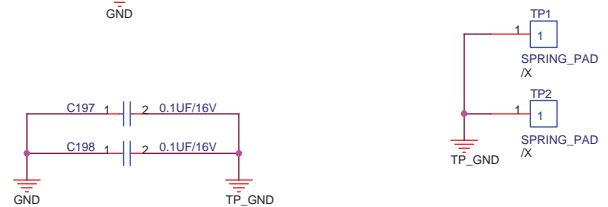
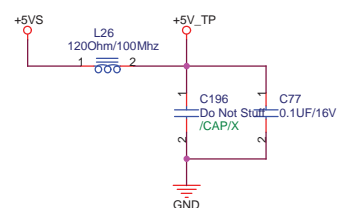
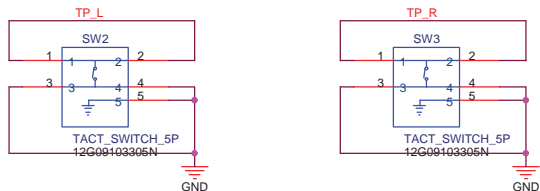
<http://hobi-elektronika.net>

		Title : Thermal Sensor_FAN	
ASUSTek Computer INC.		Engineer: Keli_Huang	
Size	Project Name		Rev
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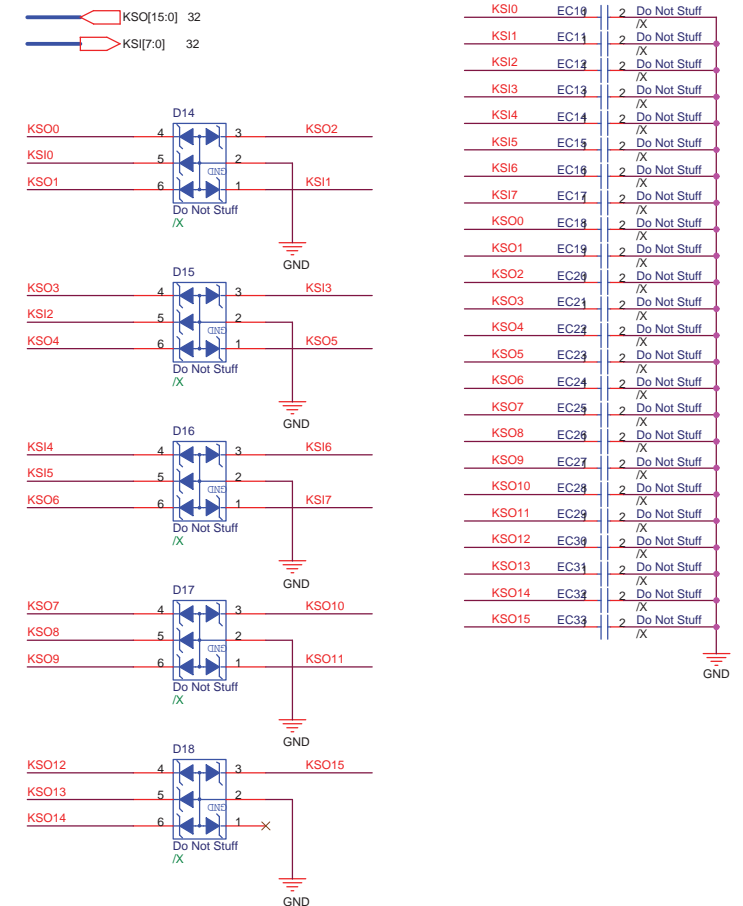
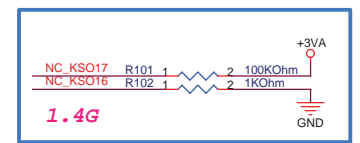
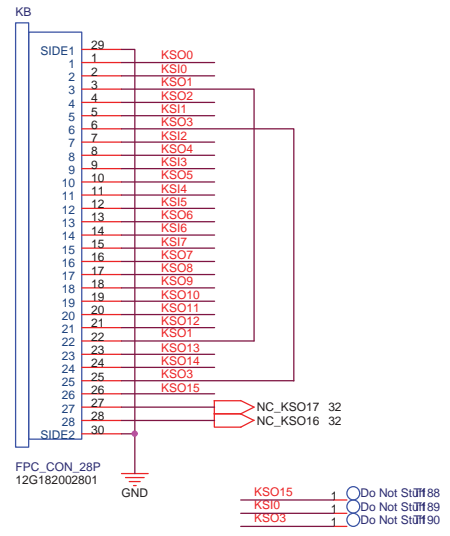
For Touch-Pad



SW2, SW3 use 12G09103305N

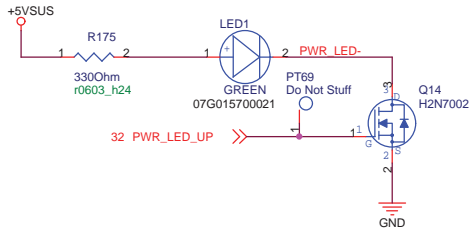


For Keyboard Connector

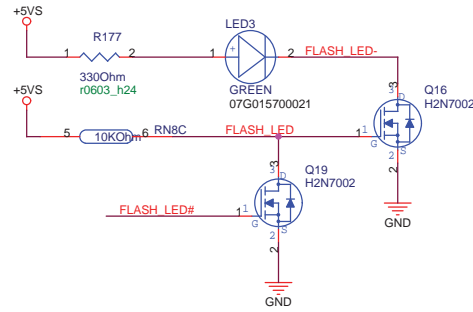


KSI0	EC19	2	Do Not Stuff
KSI1	EC11	2	Do Not Stuff
KSI2	EC12	2	Do Not Stuff
KSI3	EC13	2	Do Not Stuff
KSI4	EC14	2	Do Not Stuff
KSI5	EC15	2	Do Not Stuff
KSI6	EC16	2	Do Not Stuff
KSI7	EC17	2	Do Not Stuff
KSO0	EC18	2	Do Not Stuff
KSO1	EC19	2	Do Not Stuff
KSO2	EC20	2	Do Not Stuff
KSO3	EC21	2	Do Not Stuff
KSO4	EC22	2	Do Not Stuff
KSO5	EC23	2	Do Not Stuff
KSO6	EC24	2	Do Not Stuff
KSO7	EC25	2	Do Not Stuff
KSO8	EC26	2	Do Not Stuff
KSO9	EC27	2	Do Not Stuff
KSO10	EC28	2	Do Not Stuff
KSO11	EC29	2	Do Not Stuff
KSO12	EC30	2	Do Not Stuff
KSO13	EC31	2	Do Not Stuff
KSO14	EC32	2	Do Not Stuff
KSO15	EC33	2	Do Not Stuff

for POWER LED

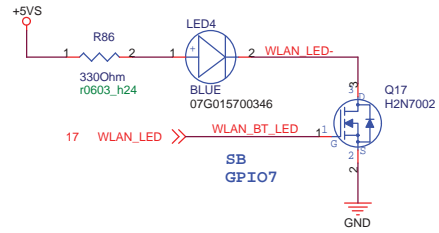


for FLASH LED

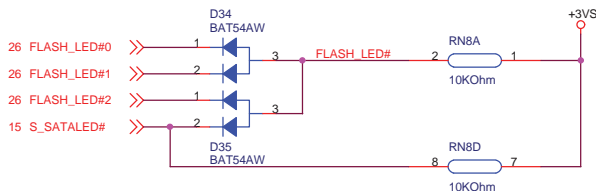
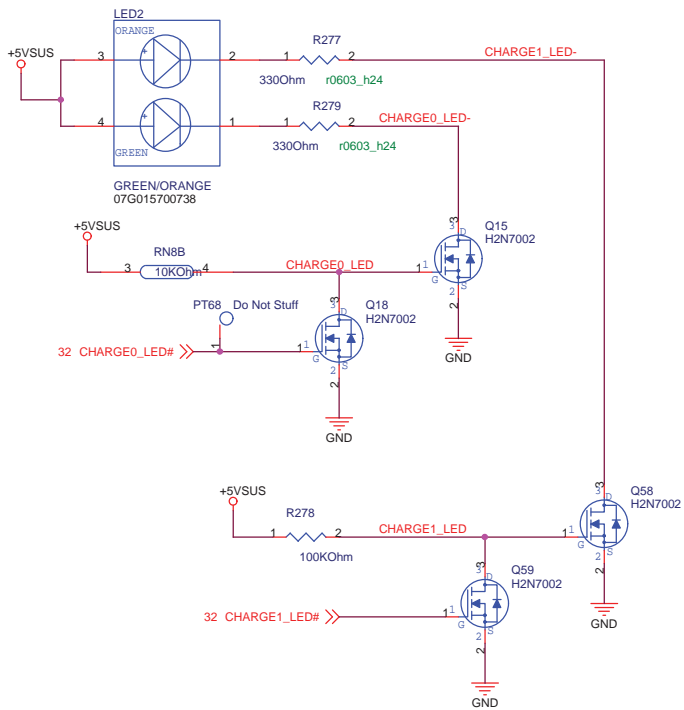


for WLAN/BlueTooth LED

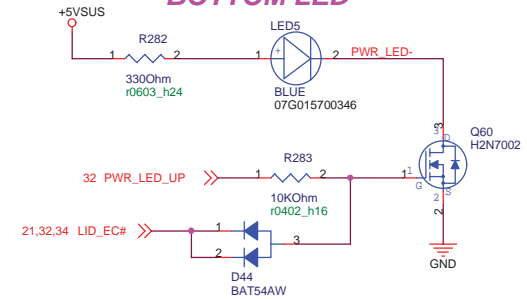
R86 use 4.7K OHm 10G213472003030

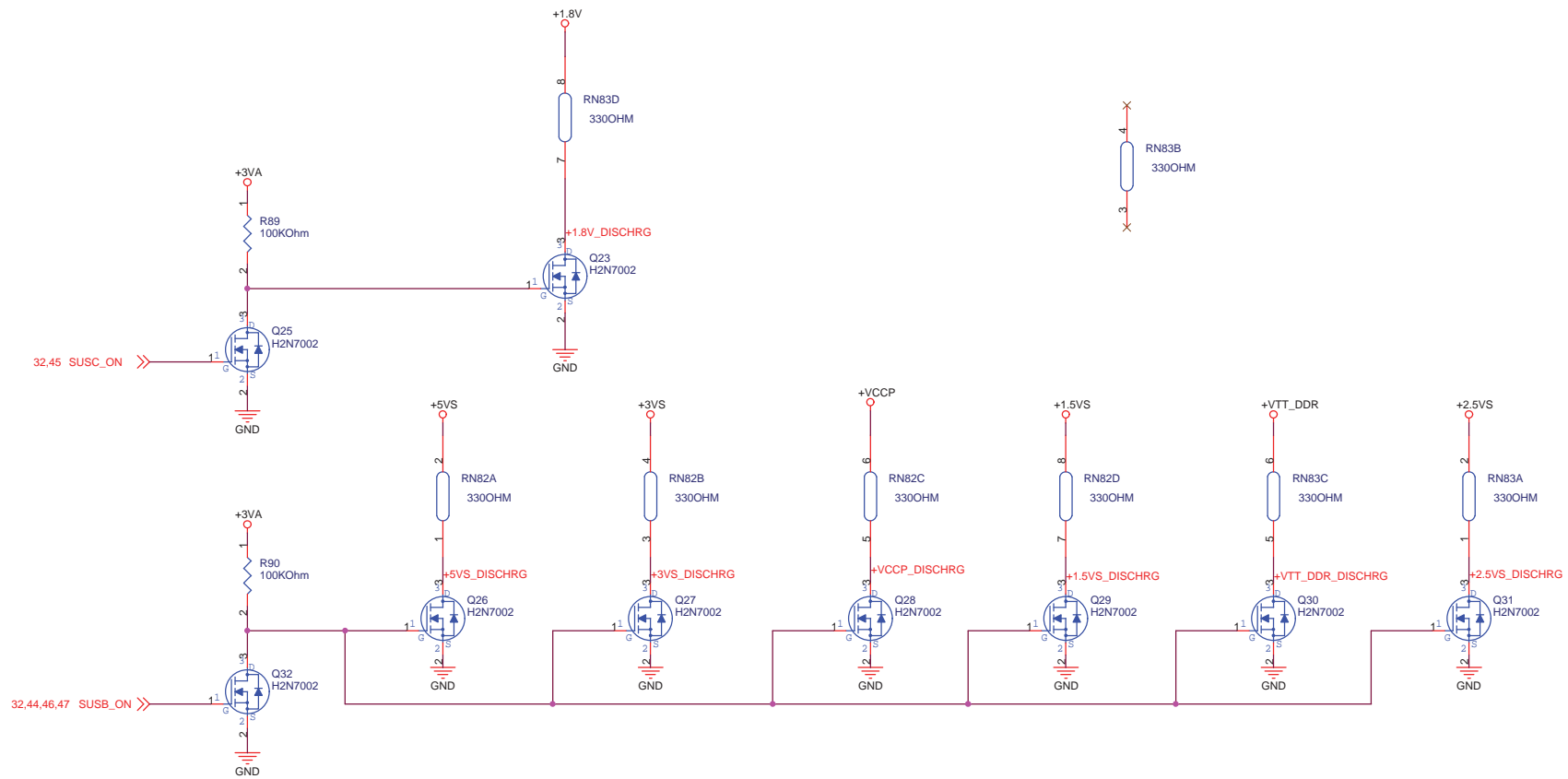


for CHARGE LED



for POWER BOTTOM LED

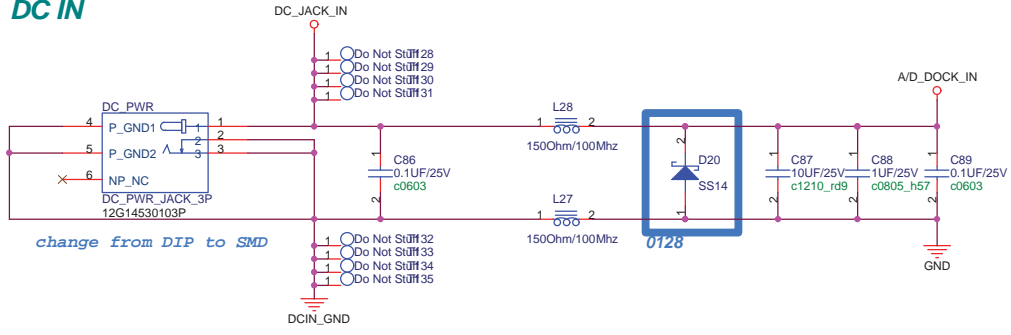




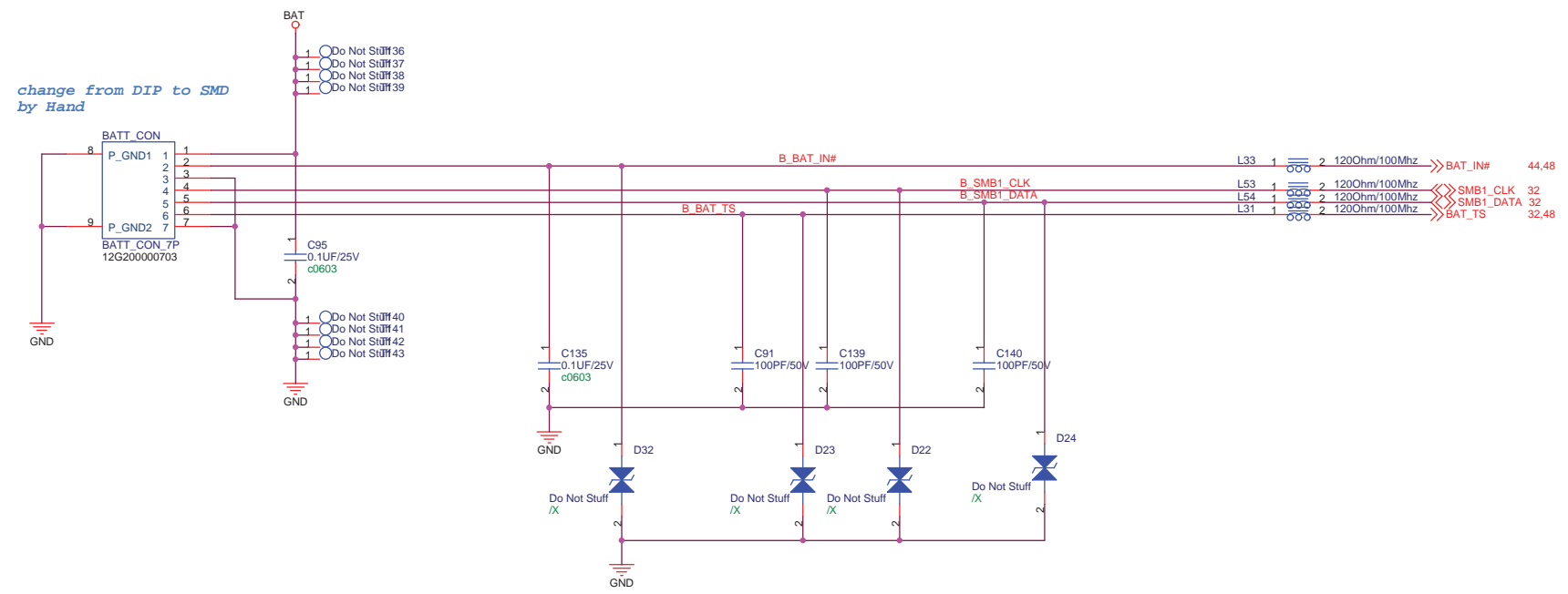
<http://hobi-elektronika.net>

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Date	Rev
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DC IN

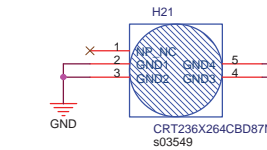
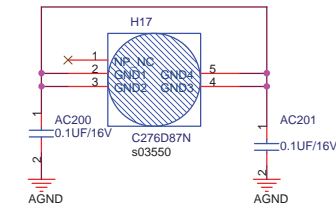
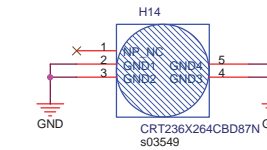
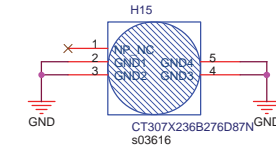
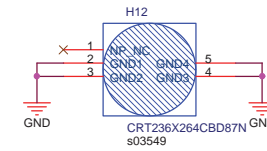
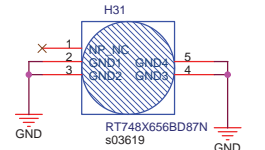
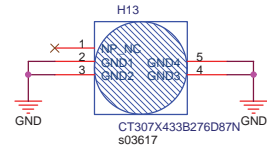
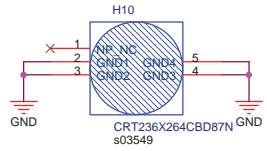
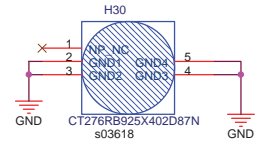
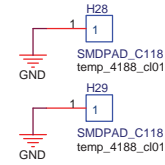
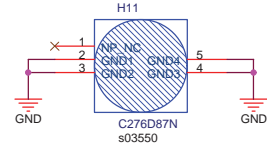
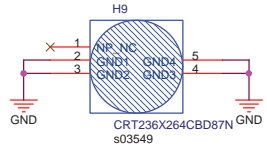
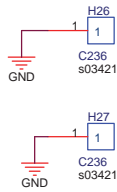
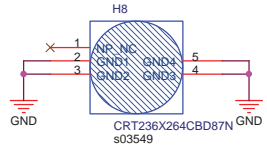
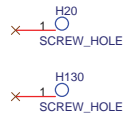
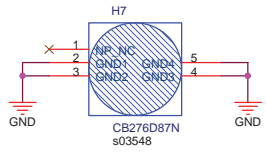


BAT IN



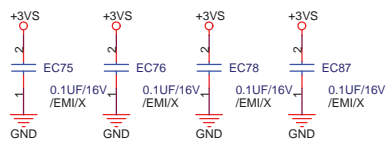
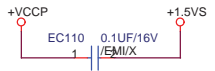
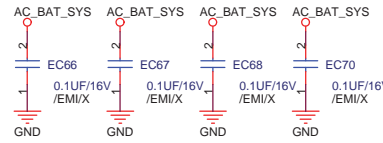
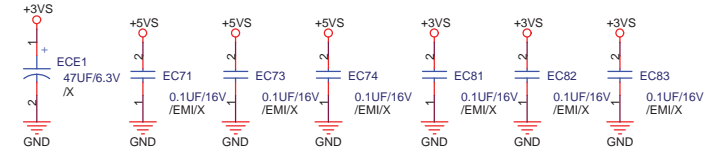
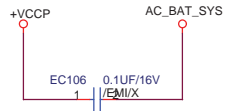
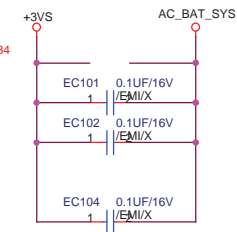
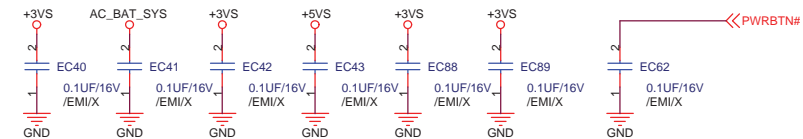
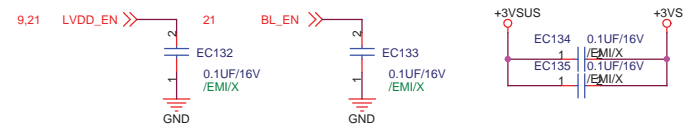
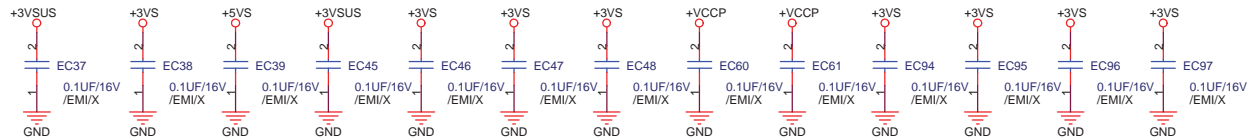
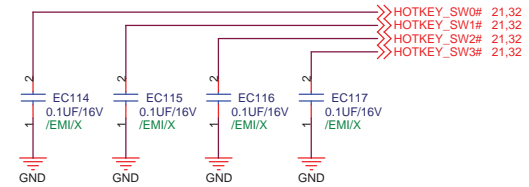
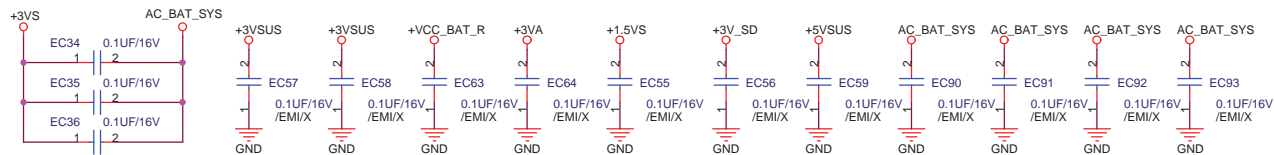
<http://hobi-elektronika.net>

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
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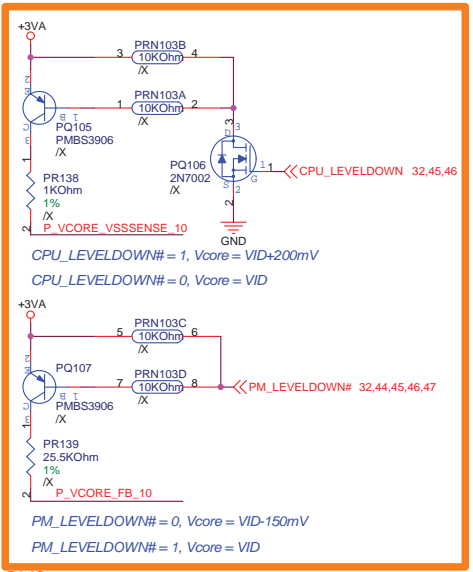
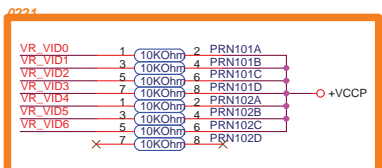
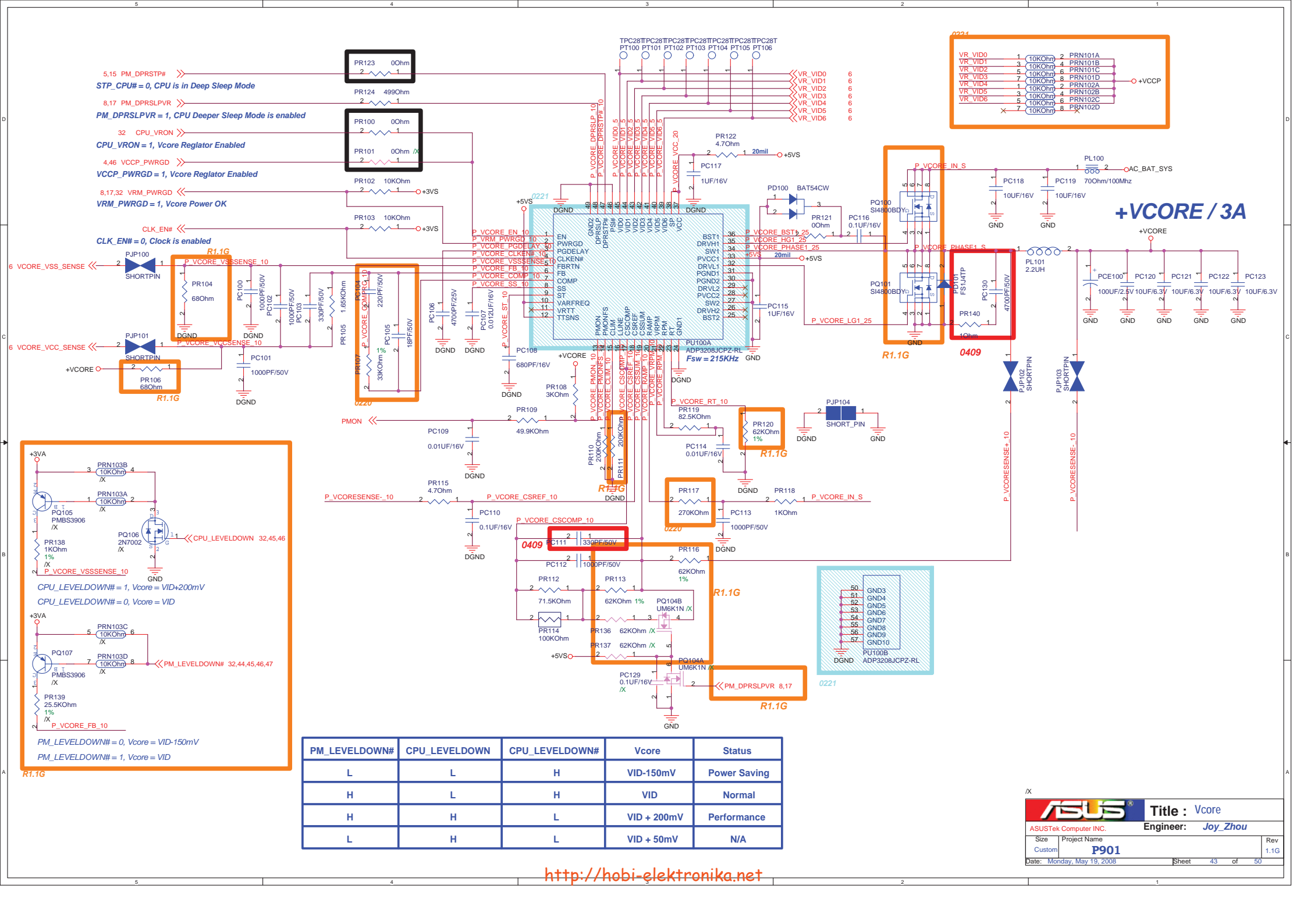


<http://hobi-elektronika.net>

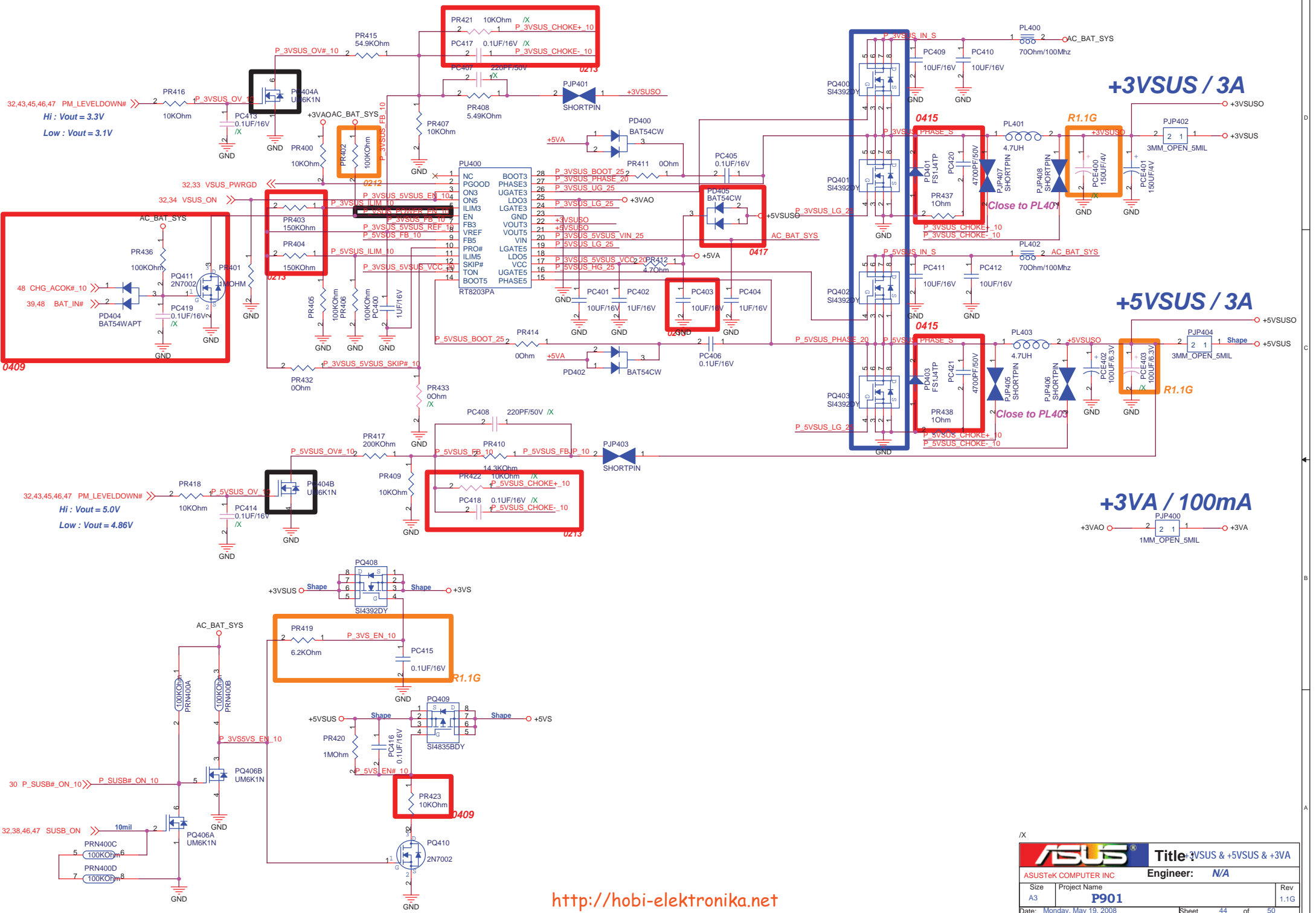
ASUS		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
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Date: Monday, May 19, 2008		Sheet	40 of 47



ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
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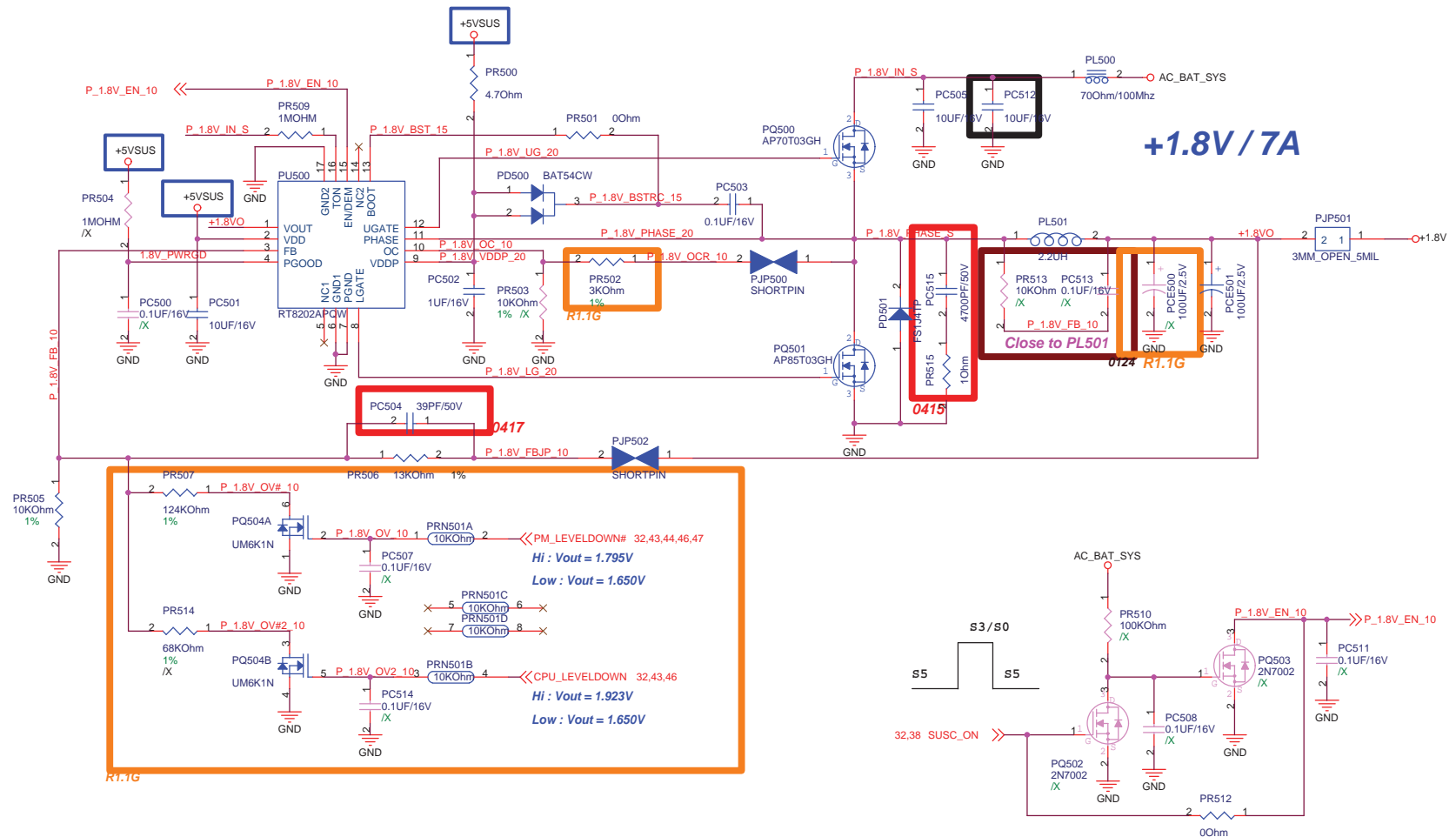


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

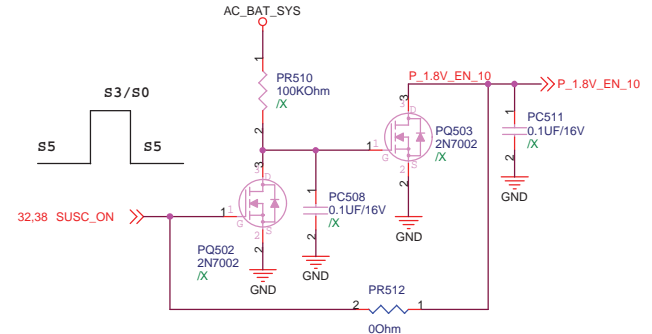
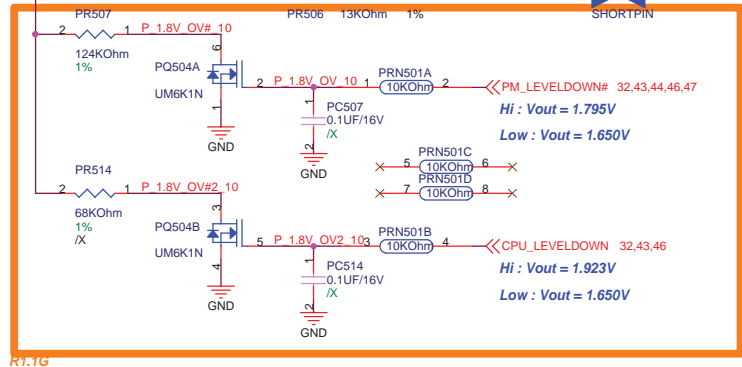


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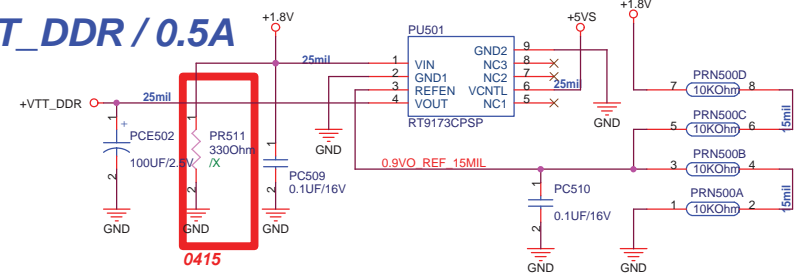
ASUS		Title: 3VSUS & +5VSUS & +3VA	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
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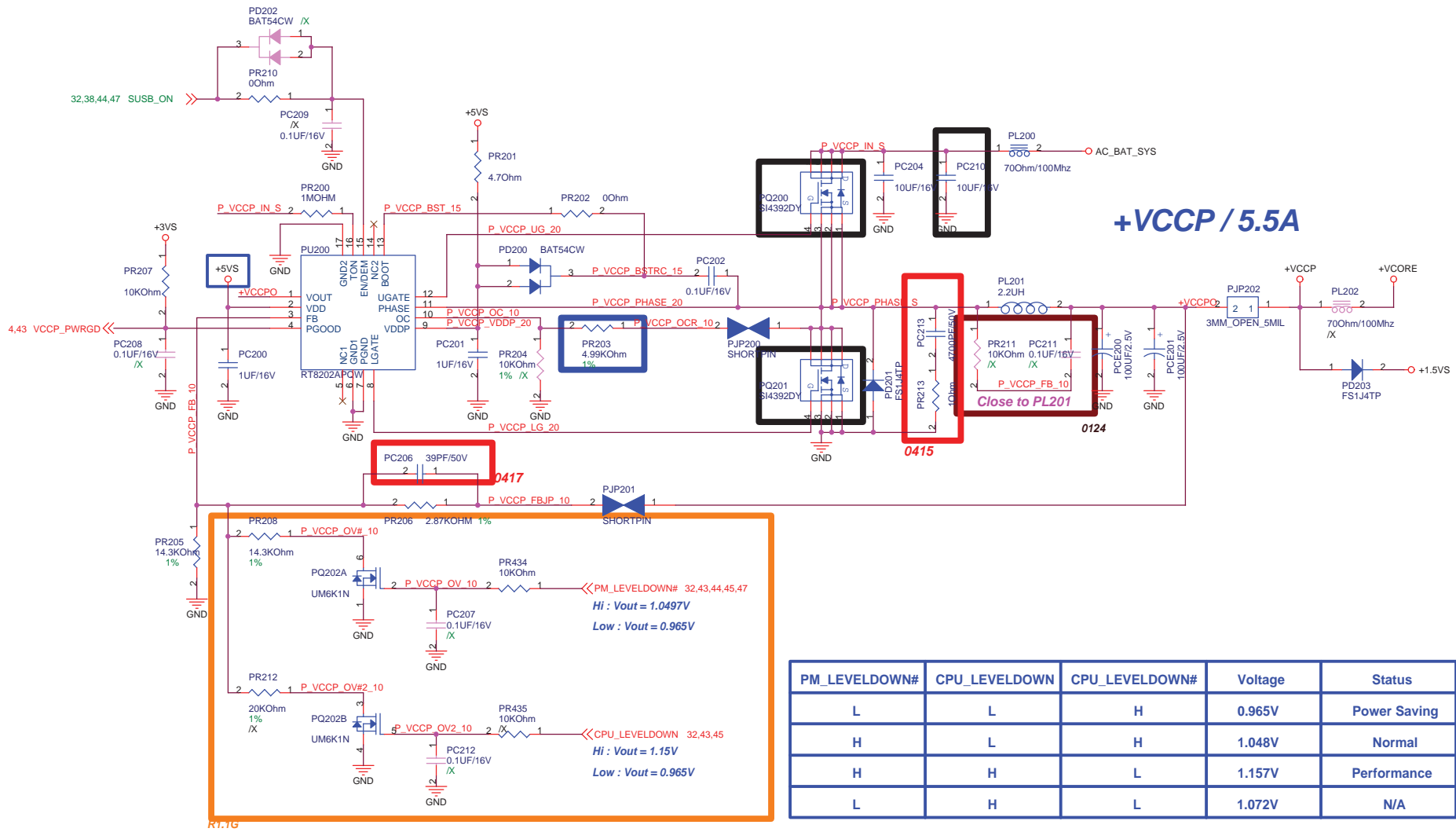
+1.8V / 7A



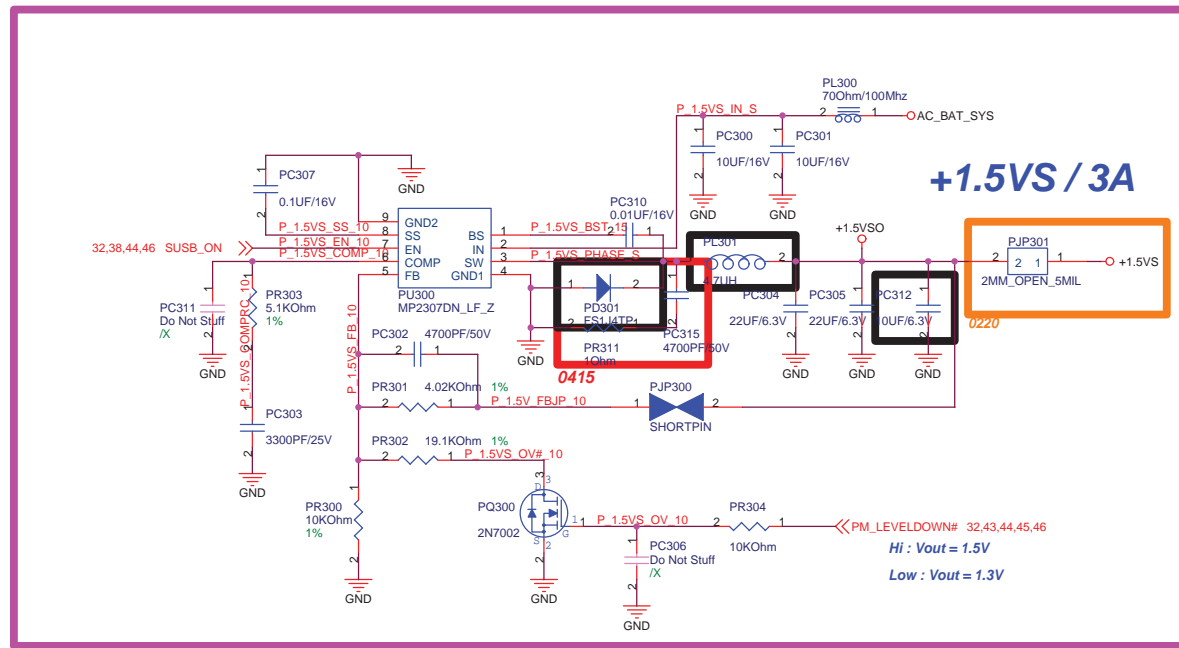
VTT_DDR / 0.5A



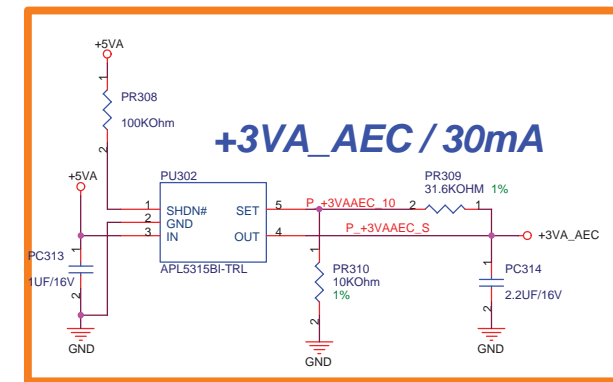
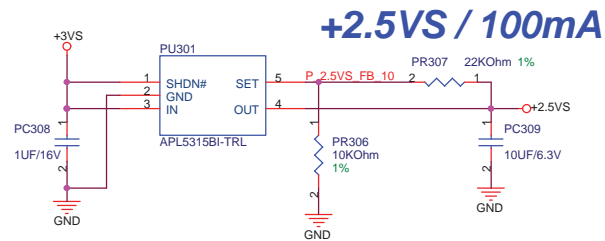
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A



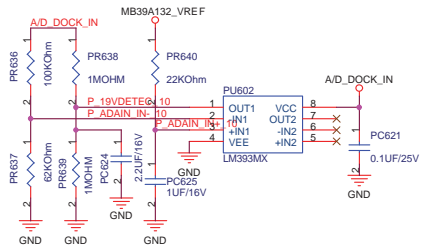
0115



0220

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ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
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VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.13 * CS (\mu F)$

$V_{TH} \text{ of } -IN1: 5V / 62 * (100+62) = 13.06V$

$V_{TH} \text{ of } ACIN: 1.25V / 25 * (185+25) = 10.5V$
 Change PR607 and PR608 value

Prevent Input from 19V :

Adaptor > 13.06V, PQ603B Turn-off
 Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :

$BAT_ID = 1, 2 \text{ Cells; } Vadj2 = 0.998V$
 $\Rightarrow I_{charge} = 1.477A$
 $BAT_ID = 0, 4/6 \text{ Cells; } Vadj2 = 1.648V$
 $\Rightarrow I_{charge} = 2.517A$

Pre-Charging Mode :

Precharging current = 150mA
 $Vadj2 = 168.75mV$

Adaptor Max. Current :

PR600=235.8K; $I_{limit} = 2.170A$; 20.615W (9.5V/22W)
 PR600=185.3K; $I_{limit} = 2.677A$; 32.124W (12V/36W)

ACIN Threshold = 1.25V

Adaptor > 10.5V, System Powered by Adaptor
 Adaptor < 10.5V, System Powered by Battery

Battery Charging Voltage :

$Vadj3 > 4.1V \Rightarrow V_{bat} = 4.2V / \text{cell}$
 $2.2V > Vadj3 > 1.1V \Rightarrow V_{bat} = 2 * Vadj3$

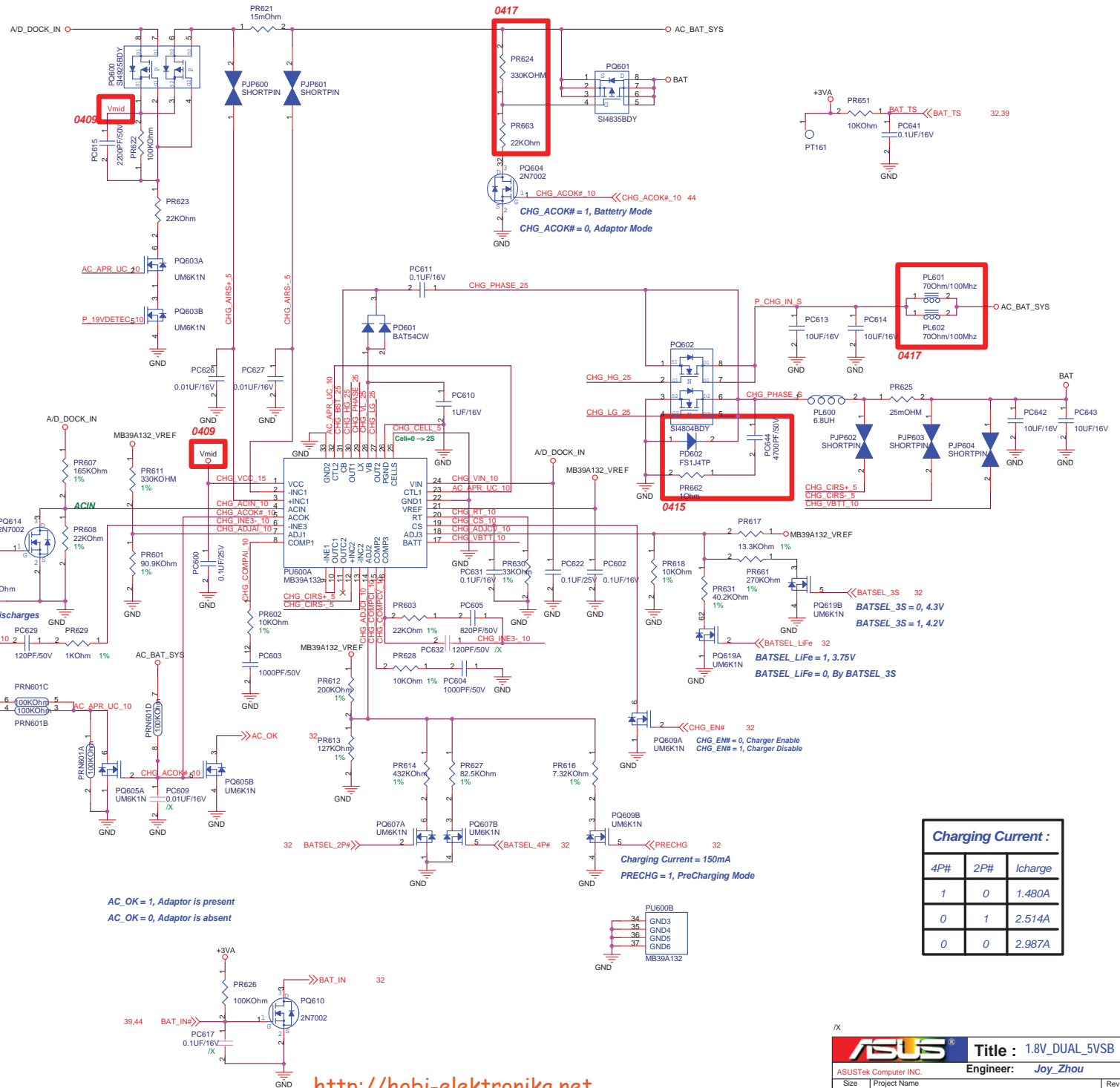
Battery Charging Current :

$4.4V > Vadj2 \geq 0V \Rightarrow$

$I_{chg} =$

$Vadj2 = 0.075V / (25 * R_s)$

$I_{limit} \text{ current} = (Vadj1 - 0.075) / (25 * R_s)$



AC_OK = 1, Adaptor is present
 AC_OK = 0, Adaptor is absent

CHG_EN# = 0, Charger Enable
 CHG_EN# = 1, Charger Disable

Charging Current = 150mA
 PRECHG = 1, PreCharging Mode

Charging Current :

4P#	2P#	Icharge
1	0	1.480A
0	1	2.514A
0	0	2.987A

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO0/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO4	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMIH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING


Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCL_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

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		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Satan He	
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IX

		Title : History	
ASUSTek Computer INC.		Engineer: <i>Satan He</i>	
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