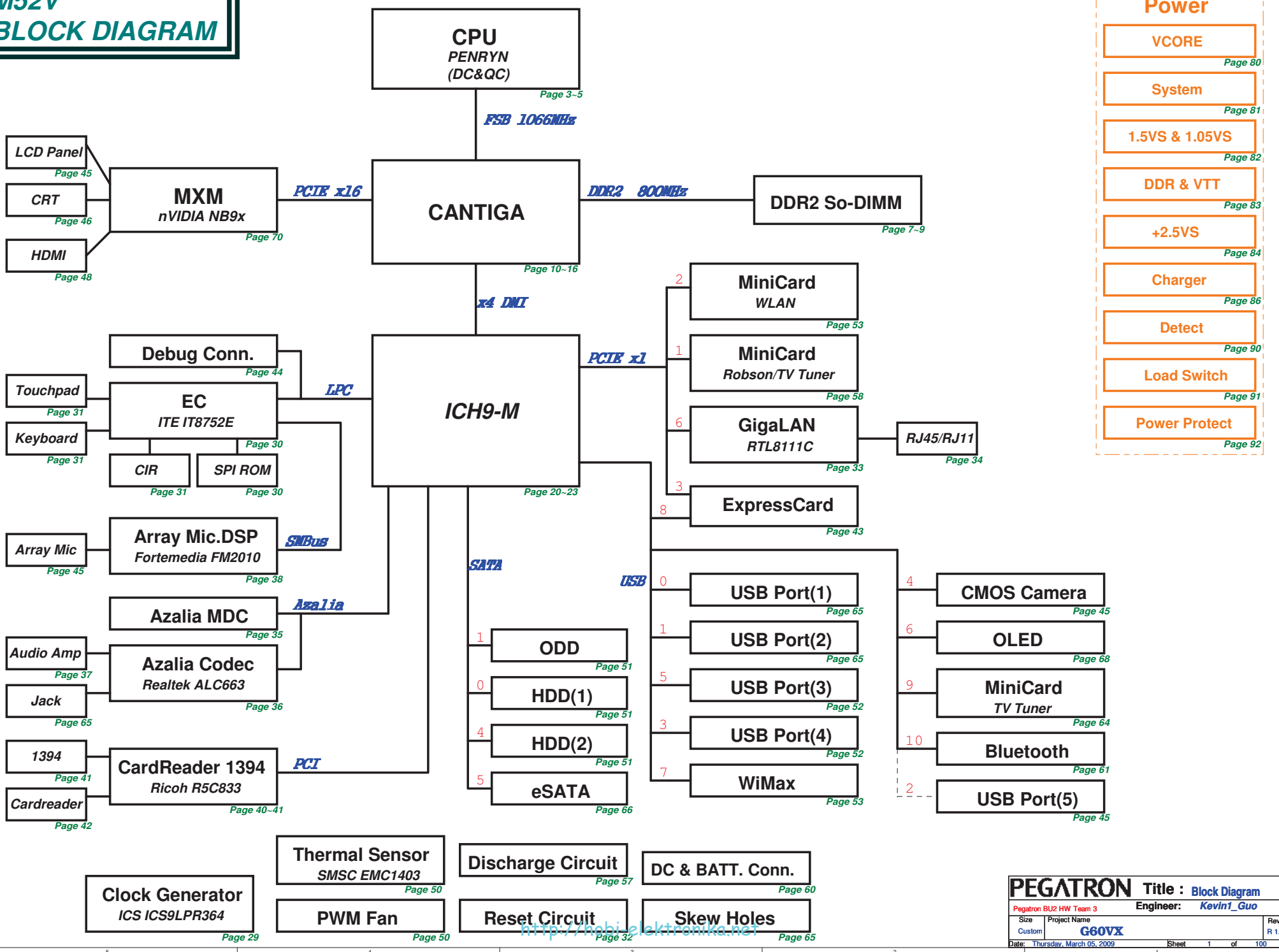


M52V BLOCK DIAGRAM



Power

- VCore Page 80
- System Page 81
- 1.5VS & 1.05VS Page 82
- DDR & VTT Page 83
- +2.5VS Page 84
- Charger Page 86
- Detect Page 90
- Load Switch Page 91
- Power Protect Page 92

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ICH9-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPIO2/GPIO14		
AE20	STP_PC#/GPIO15	STP_PC#	I/O
AJ14	DPRSPLVR/GPIO16	PM DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8512E GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O	105	CLKRUN#/GPH0	PM_CLKRUN#	I/O
29	PWM1/GPA1	CHG_LED_UP#	O	106	CRX1/GPH1	3G_ON#	O
32	PWM2/GPA2			107	CTX1/GPH2	3G_LED_ON#	O
33	PWM3/GPA3			108	GPH3	BAT_LEARN	I/O
34	PWM4/GPA4	LCD_BL_PWM	O	109	GPH4		
35	PWM5/GPA5	FAN_PWM	O	110	GPH5	NUM_LED	O
36	PWM6/GPA6			111	GPH6	CAP_LED	O
38	PWM7/GPA7			74	ADC0/GPI0	NV_OVERT#	I
122	RXD/GPB0	CHG_EN#	O	75	ADC1/GPI1	SUS_PWRGD	I
123	TXD/GPB1	PRECHG	O	76	ADC2/GPI2	ALL_SYS_PWRGD	I
139	CTX0/GPB2			77	ADC3/GPI3	CPU_PWRGD	I
124	SMCLK0/GPB3	SMB0_CLK	I/O	78	ADC4/GPI4	PWR_MON	I
125	SMDAT0/GPB4	SMB0_DAT	I/O	79	ADC5/GPI5	ALS_DA	I
142	GA20/GPB5	A20GATE	O	80	ADC6/GPI6		
4	KBRST#/GPB6	RC_IN#	O	81	ADC7/GPI7		
126	GPB7	PM_RSMRST#	O	84	DAC0/GPJ0	EC_CLK_EN	
133	CRX0/GPC0	CRX0	I	85	DAC1/GPJ1	PM_PWROK	
129	SMCLK1/GPC1	SMB1_CLK	I/O	86	DAC1/GPJ2		
130	SMDAT1/GPC2	SMB1_DAT	I/O	87	DAC1/GPJ3		
64	GPC3	PM_PWRBTN#	O	88	DAC1/GPJ4		
136	WUI2/GPC4	AC_IN_OC#	I	89	DAC1/GPJ5		
65	GPC5	OP_SD#	O	15	GPK0		
140	WUI3/GPC6	BAT1_IN_OC#	I	16	GPK1		
20	GPC7	RFON_SW#	I	17	GPK2		
22	WUI0/GPD0	PWRLIMIT#	I	18	GPK3		
25	WUI1/GPD1	PM_SUSC#	I	48	GPK4		
26	WUI4/GPD2	BUF_PLT_RST#	I	49	GPK5		
27	ECSC#GPD3	EXT_SCI#	O	62	GPK6		
19	GPD4	EXT_SMI#	O	63	GPK7		
37	GPD5	LCD_BACKOFF#	O	90	GPL0		
53	TACH0 / GPD6	FAN0_TACH	I	91	GPL1		
54	GPD7			92	GPL2		
23	GPE0	VSUS_ON	O	93	GPL3		
94	GPE1	SUSC_EC#	O	119	GPL4		
95	GPE2	SUSB_EC#	O	120	GPL5		
96	GPE3	CPU_VRON	O	134	GPL6		
141	PWRSW/GPE4	PWR_SW#	I	135	GPL7		
39	WUI5/GPE5	BAT2_IN_OC#	I				
21	GPE6	LID_SW#	I				
24	GPE7	INSTANT_ON#	I				
97	PS2CLK0/GPF0						
98	PS2DAT0/GPF1	COLOREN#	I				
99	PS2CLK1/GPF2	MARATHON#	I				
100	PS2DAT1/GPF3	DISTP#	I				
101	PS2CLK2/GPF4	TP_CLK	I/O				
102	PS2DAT2/GPF5	TP_DAT	I/O				
131	SMCLK2/GPF6	THRO_CPU	O				
132	SMDAT2/GPF7	TP_LED	O				
118	WUI7/GPG0						
121	GPG1	PM_SUSB#	I				
112	GPG2						
116	GPG6						

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PEGATRON		Title : System Setting	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Thursday, March 05, 2009	Sheet	2	of 100

10 H_D#(63:0) H_D#(63:0)
 10 H_A#(35:3) H_A#(35:3)
 10 H_REQ#(4:0) H_REQ#(4:0)

DC:
 56 ohm pull-up resistor and
 56 ohm terminated resistor
 QC:
 50 ohm pull-up resistor and
 50 ohm terminated resistor
 200811182107

BPM[3:0]:
 DC: point to debug connector if debug enabled; left unconnected if debug disabled;
 QC: 51 ohm termination needed, p-t-p to debug connector if debug enabled; left unconnected if debug disabled;
 200811191553

DC:
 COMP 0, 2: 27 ohm pull down;
 COMP 1, 3: 55 ohm pull down;
 QC:
 COMP 0, 2: 25 ohm pull down;
 COMP 1, 3: 50 ohm pull down
 200811191401

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
 Comp 1,3: Zo=55 Ohm, trace length < 0.5"

Pin M4, N5, B2:
 DC: Reserved
 unconnected;
 QC:
 BPM_2[1,0,2]
 left unconnected
 200811191521

DC: unused

DC: no termination needed;
 QC: 100 ohm resistor needed
 200811191321

Default Strapping When Not Used
 XDP_BPM#1: DC/QC: Can be left unconnected
 200811-19-14-44

R0302->RN0302A
 R0305->RN0302B
 R0307->RN0307A
 R0308->RN0307B
 G60VX R2.0 costdown
 20090328

Place R0304 & R0306 for XDP function

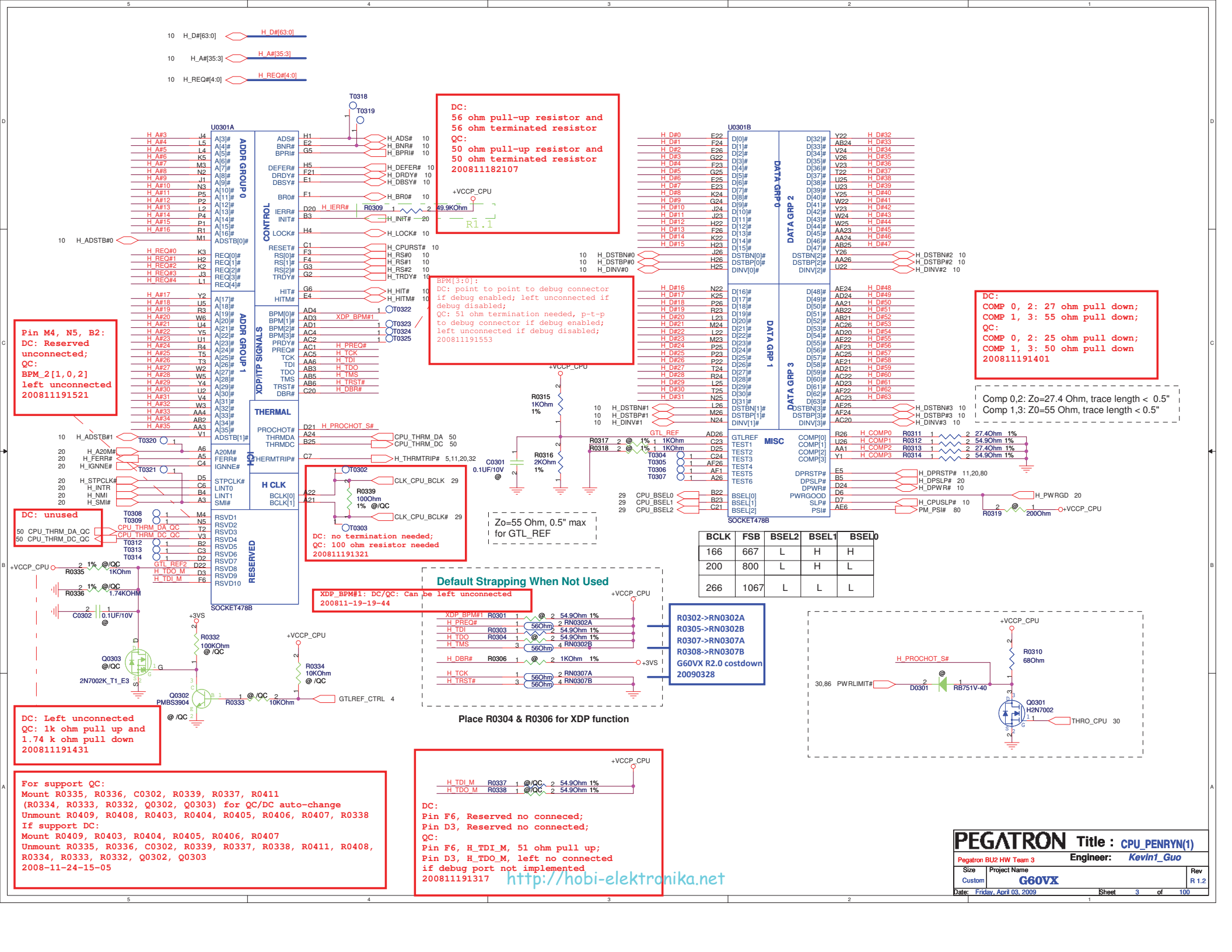
DC:
 Pin F6, Reserved no connected;
 Pin D3, Reserved no connected;
 QC:
 Pin F6, H_TDI_M, 51 ohm pull up;
 Pin D3, H_TDO_M, left no connected
 if debug port not implemented
 200811191317

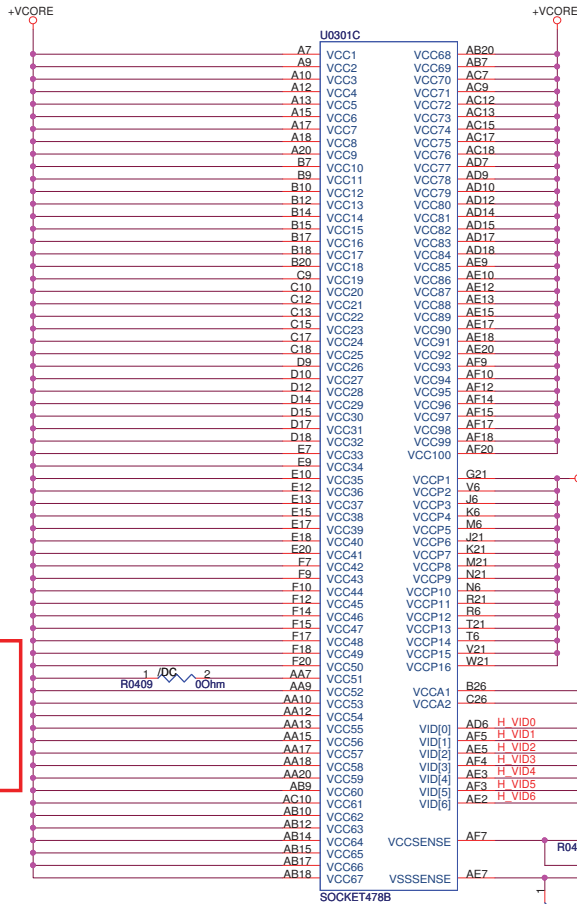
DC: Left unconnected
 QC: 1k ohm pull up and
 1.74 k ohm pull down
 200811191431

For support QC:
 Mount R0335, R0336, C0302, R0339, R0337, R0411
 (R0334, R0333, R0332, Q0302, Q0303) for QC/DC auto-change
 Unmount R0409, R0408, R0403, R0403, R0404, R0405, R0406, R0407, R0338
 If support DC:
 Mount R0409, R0403, R0404, R0405, R0406, R0407
 Unmount R0335, R0336, C0302, R0339, R0337, R0338, R0411, R0408,
 R0334, R0333, R0332, Q0302, Q0303
 2008-11-24-15-05

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

PEGATRON Title : CPU_PENRYN(1)
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
 Size Project Name
 Custom G60VX
 Date: Friday, April 03, 2009 Sheet 3 of 100





Pin AC8/AA8/D8:
 DC: VSS to GND;
 QC: Reserved and should be left unconnected,
 but can be rout open for future use
 2008-11-19-21-00

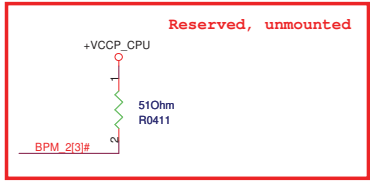
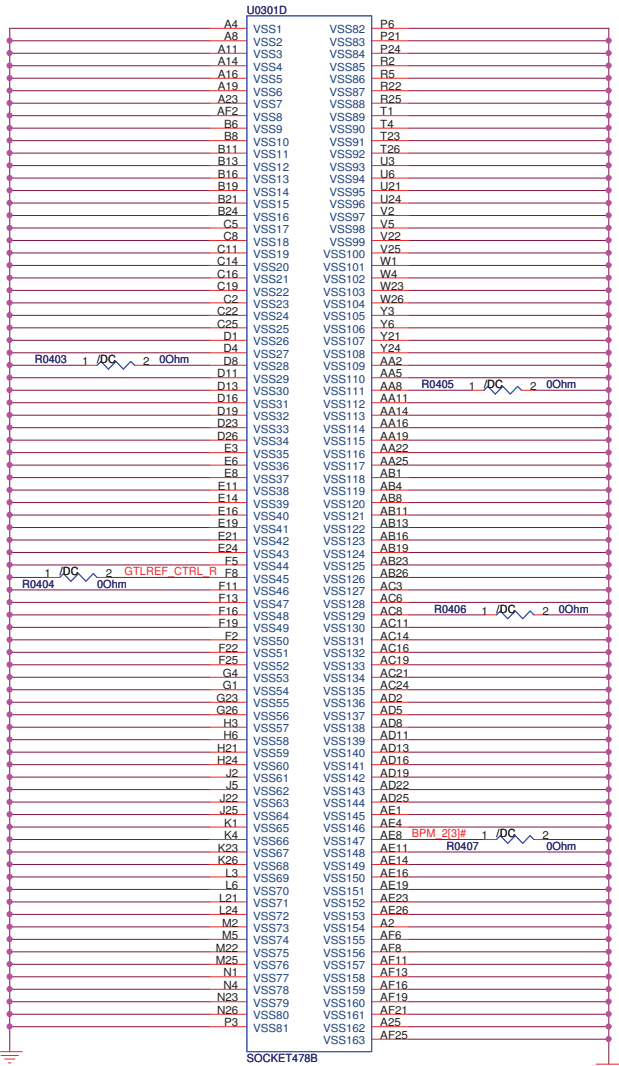
Pin F8:
 DC: VSS;
 QC: GTLREF_CONTROL, control signal to
 connect or disconnect GTLREF_2 circuit
 to switch between QC and DC.
 Use this signal to control GTLREF_2 circuit
 or Use R0335/R0334 voltage divider
 (with the later method, DC and QC will has
 a BOM change)
 2008-11-19-20-55

unmount C0401
 change RNX0401 RNX0402 to short land
 G60VX R2.0 costdown 20090328

Pin AE8:
 DC: VSS to GND;
 QC: BPM_2[3]#, left
 unconnected

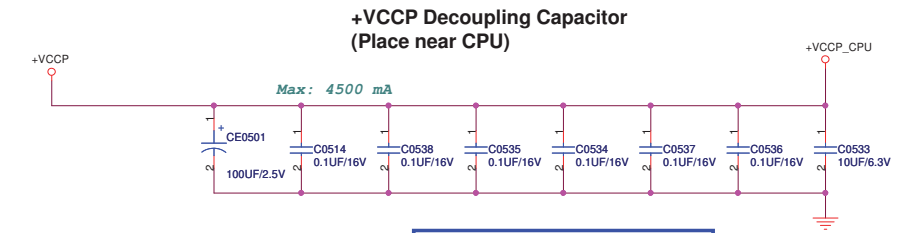
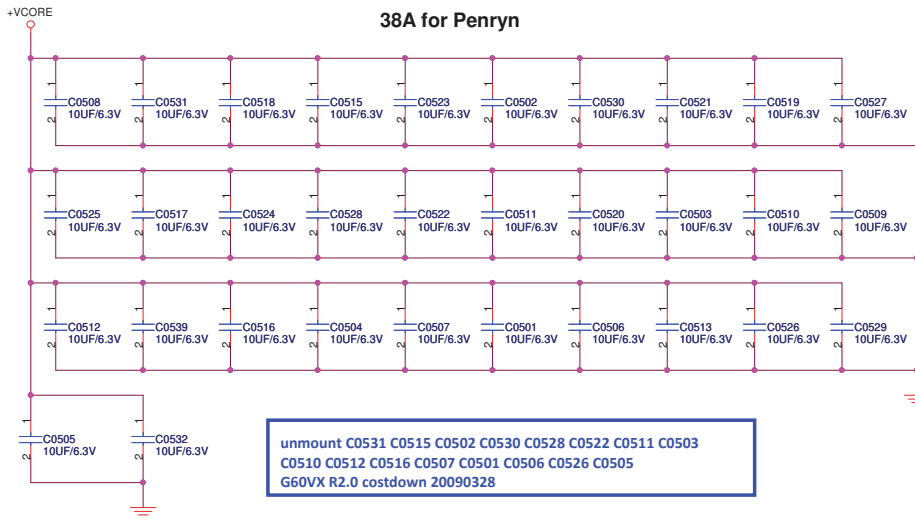
VCCSENSE and VSSSENSE are wide trace
 can't use a RES A to costdown

Pin AA7:
 DC: Power pin
 to VCCP;
 QC: BR1#, for
 debug, should
 left as NC



If support DC:
 Mount R0409, R0403, R0404, R0405, R0406, R0407
 Unmount R0335, R0336, C0302, R0339, R0337, R0338, R0411, R0408
 For support QC:
 Mount R0335, R0336, C0302, R0339, R0337, R0338, R0411
 Unmount R0409, R0408, R0403, R0404, R0405, R0406, R0407 ??
 200811122108

??
<http://hobi-elektronika.net>

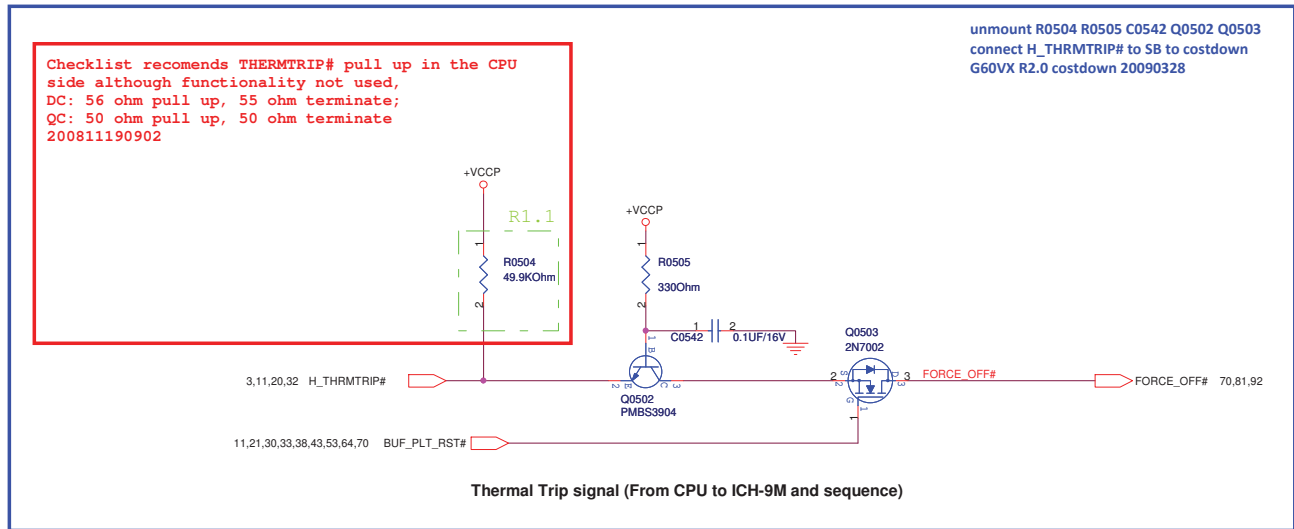


Decoupling guide from Intel

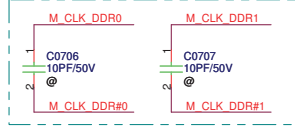
V_CORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+V_CORE Mid-Frequency Capacitor
Intel: 22UF *32
F3S: 10UF *16
A7S: 10UF *1011/17
V1V: ?

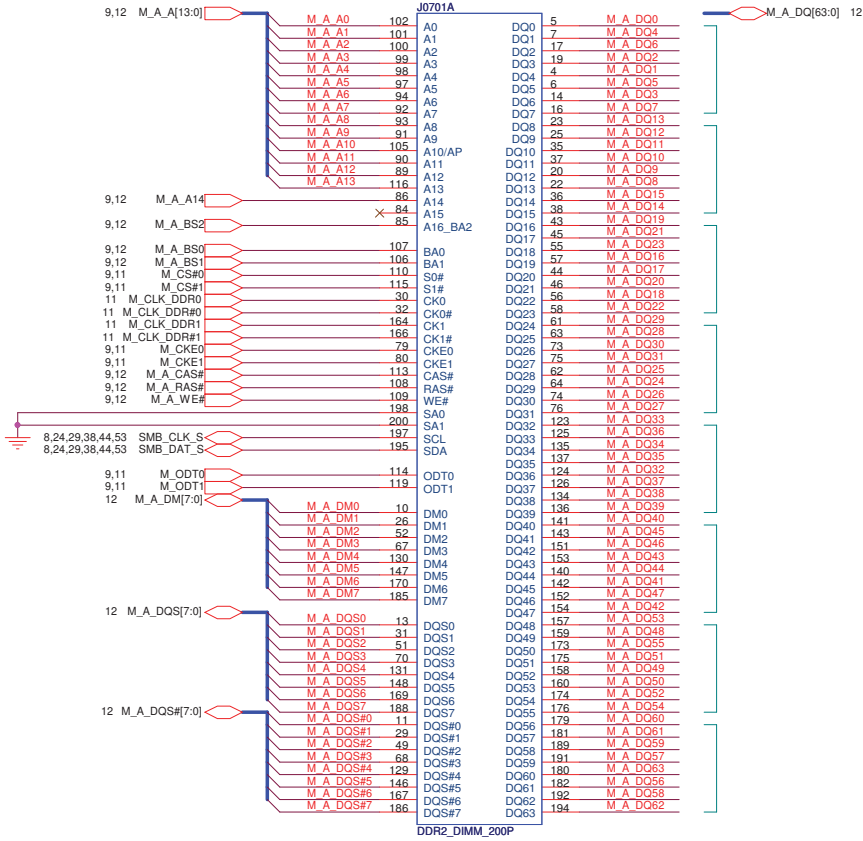
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4
V1V: ?



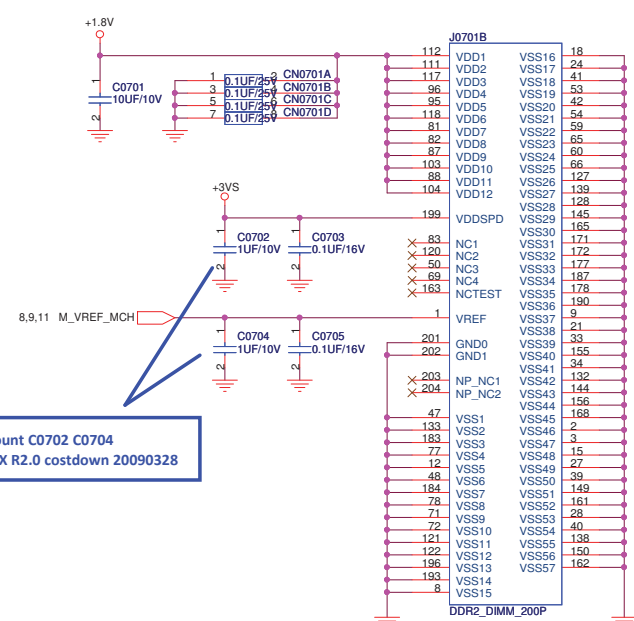
Reserved for 3G



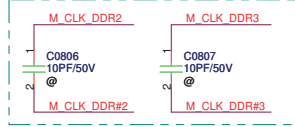
Reverse Type
H = 9.2 mm



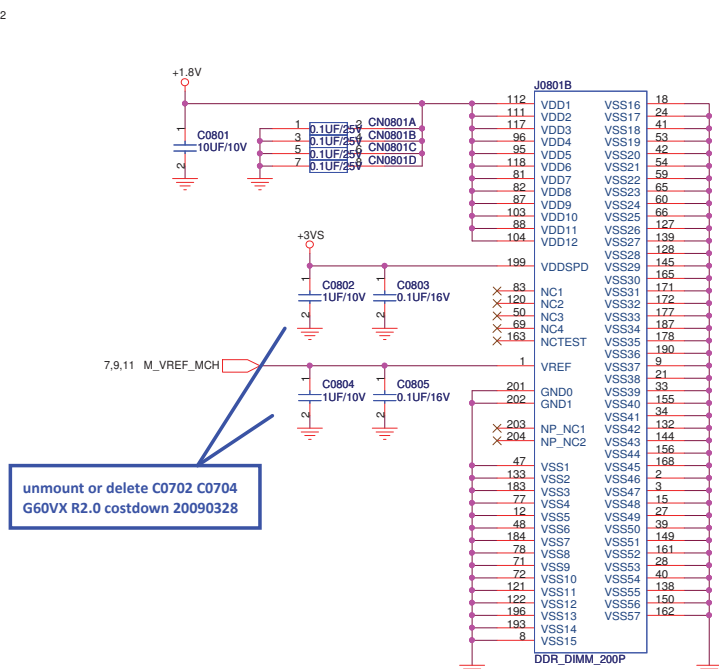
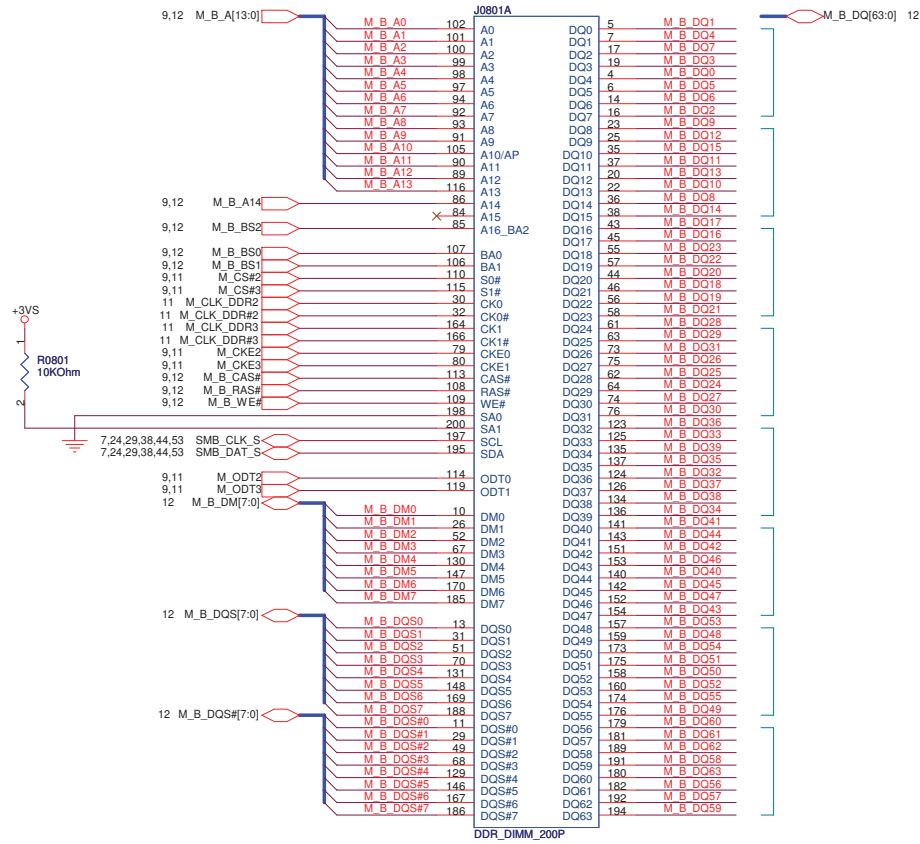
unmount C0702 C0704
G60VX R2.0 costdown 20090328



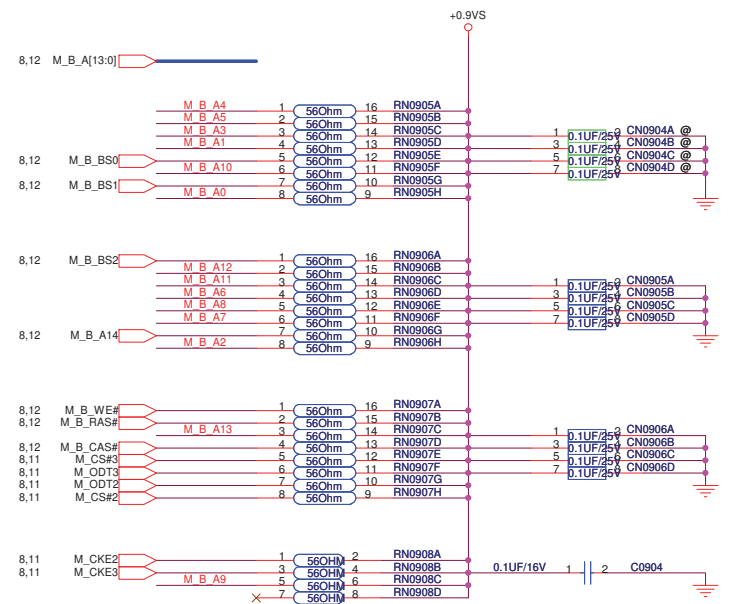
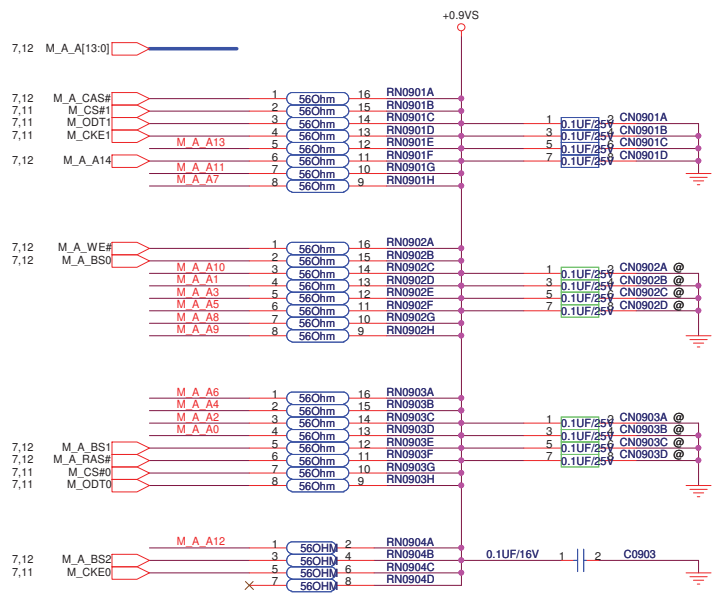
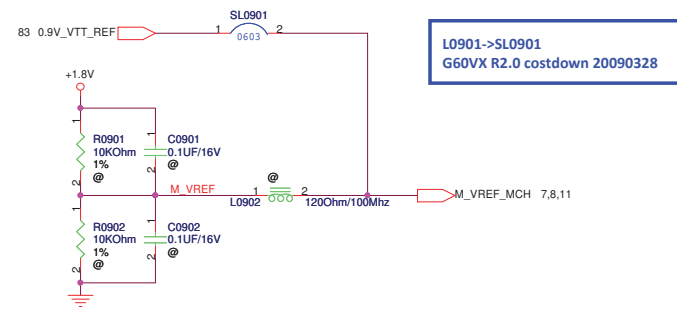
Reserved for 3G



Reverse Type
H = 4.0 mm



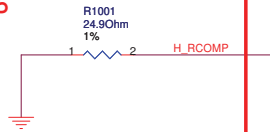
unmount or delete C0702 C0704
G60VX R2.0 costdown 20090328



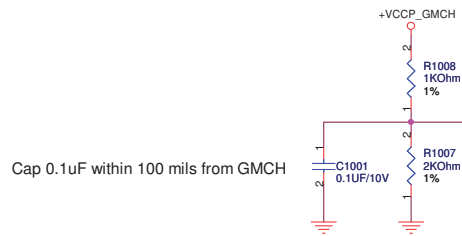
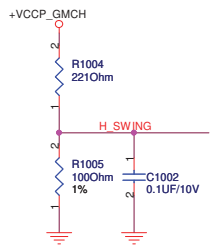
<http://hobi-elektronika.net>

PEGATRON Title : DIM_DDR2 Termination
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
 Size Custom Project Name G60VX Rev R 1.2
 Date: Wednesday, April 08, 2009 Sheet 9 of 100

H_RCOMP:
 DC: 25 ohm pull down;
 QC: 17 ohm pull down
 2008-11-19-20-25



H_SWING:
 DC: 221 ohm pull up,
 100 ohm pull down;
 QC: 221 ohm pull up,
 75 ohm pull down
 2008-11-19-20-27

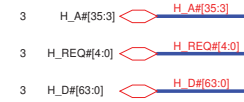


Cap 0.1uF within 100 mils from GMCH

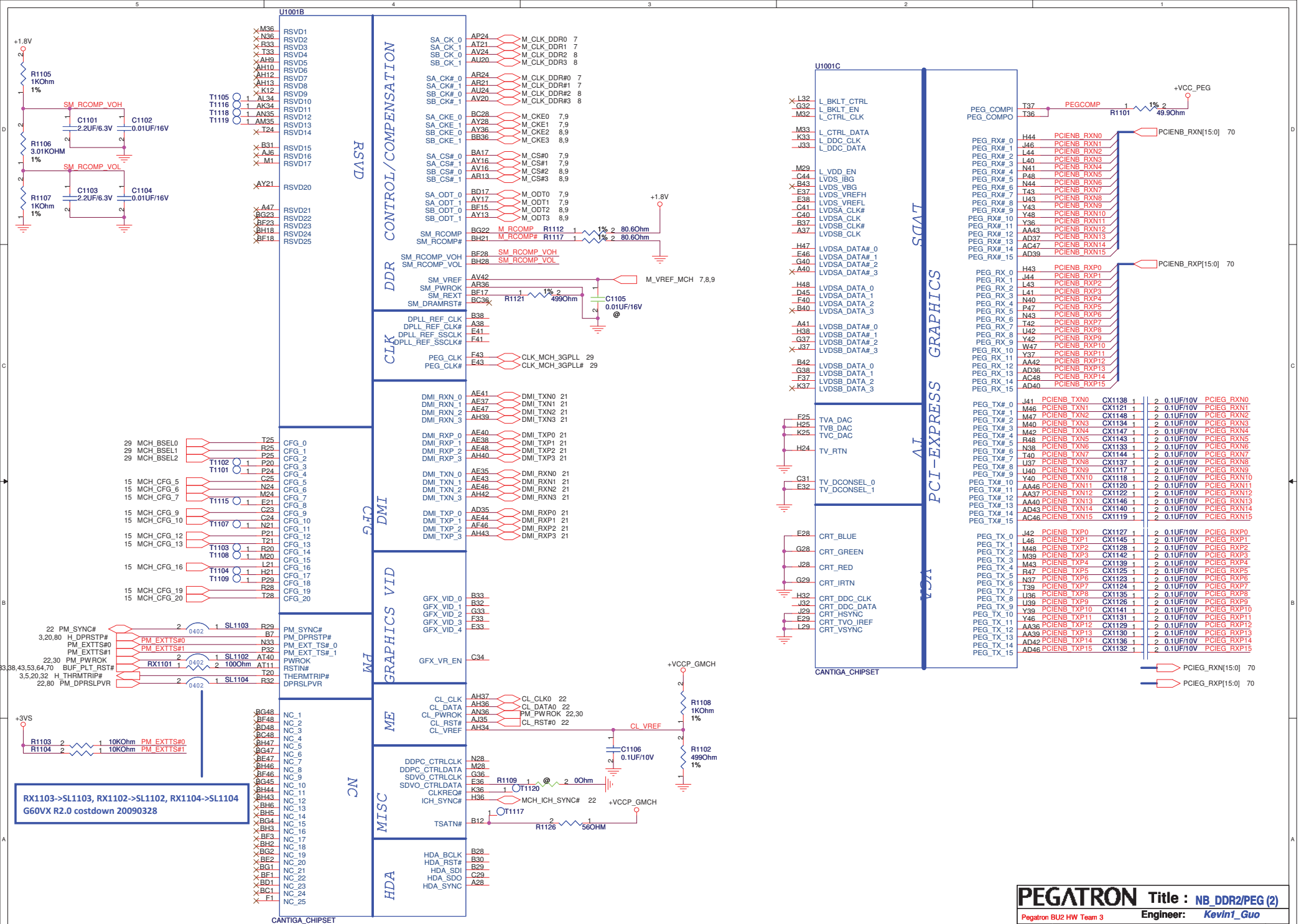
RX1006->SL1006;
 G60VX R2.0 costdown 20090405

H_D#0	F2	H_D#_0	A14	H_A#3
H_D#1	G8	H_D#_1	C15	H_A#4
H_D#2	F8	H_D#_2	F16	H_A#5
H_D#3	E6	H_D#_3	H13	H_A#6
H_D#4	G2	H_D#_4	C18	H_A#7
H_D#5	H6	H_D#_5	M16	H_A#8
H_D#6	H2	H_D#_6	J13	H_A#9
H_D#7	F6	H_D#_7	P16	H_A#10
H_D#8	D4	H_D#_8	R16	H_A#11
H_D#9	H3	H_D#_9	N17	H_A#12
H_D#10	M9	H_D#_10	M13	H_A#13
H_D#11	M11	H_D#_11	E17	H_A#14
H_D#12	J2	H_D#_12	P17	H_A#15
H_D#13	N12	H_D#_13	F17	H_A#16
H_D#14	J6	H_D#_14	G20	H_A#17
H_D#15	R2	H_D#_15	B19	H_A#18
H_D#16	L2	H_D#_16	R16	H_A#19
H_D#17	R2	H_D#_17	E20	H_A#20
H_D#18	N9	H_D#_18	H16	H_A#21
H_D#19	L6	H_D#_19	J20	H_A#22
H_D#20	M5	H_D#_20	L17	H_A#23
H_D#21	J3	H_D#_21	A17	H_A#24
H_D#22	N2	H_D#_22	B17	H_A#25
H_D#23	R1	H_D#_23	L16	H_A#26
H_D#24	N2	H_D#_24	C21	H_A#27
H_D#25	N5	H_D#_25	J17	H_A#28
H_D#26	N6	H_D#_26	H20	H_A#29
H_D#27	P13	H_D#_27	B18	H_A#30
H_D#28	N8	H_D#_28	K17	H_A#31
H_D#29	L7	H_D#_29	B20	H_A#32
H_D#30	N10	H_D#_30	F21	H_A#33
H_D#31	M3	H_D#_31	K21	H_A#34
H_D#32	Y3	H_D#_32	L20	H_A#35
H_D#33	AD14	H_D#_33		
H_D#34	Y6	H_D#_34		
H_D#35	Y10	H_D#_35		
H_D#36	Y12	H_D#_36		
H_D#37	Y14	H_D#_37		
H_D#38	Y7	H_D#_38		
H_D#39	W2	H_D#_39		
H_D#40	AA8	H_D#_40		
H_D#41	Y9	H_D#_41		
H_D#42	AA13	H_D#_42		
H_D#43	AA9	H_D#_43		
H_D#44	AA11	H_D#_44		
H_D#45	AD11	H_D#_45		
H_D#46	AD10	H_D#_46		
H_D#47	AD13	H_D#_47		
H_D#48	AE12	H_D#_48		
H_D#49	AE9	H_D#_49		
H_D#50	AA2	H_D#_50		
H_D#51	AD8	H_D#_51		
H_D#52	AA3	H_D#_52		
H_D#53	AD3	H_D#_53		
H_D#54	AD7	H_D#_54		
H_D#55	AE14	H_D#_55		
H_D#56	AE4	H_D#_56		
H_D#57	AC1	H_D#_57		
H_D#58	AE3	H_D#_58		
H_D#59	AC3	H_D#_59		
H_D#60	AE11	H_D#_60		
H_D#61	AE8	H_D#_61		
H_D#62	AG2	H_D#_62		
H_D#63	AD6	H_D#_63		
H_SWING	C5	H_SWING		
H_RCOMP	E3	H_RCOMP		

HOST



H_ADS#	H12	H_ADS#	3
H_ADSTB#_0	B16	H_ADSTB#_0	3
H_ADSTB#_1	G17	H_ADSTB#_1	3
H_BNR#	A9	H_BNR#	3
H_BPRI#	E11	H_BPRI#	3
H_BREQ#	G12	H_BREQ#	3
H_DEFER#	B10	H_DEFER#	3
H_DBSY#	AH7	H_DBSY#	3
HPLL_CLK	AH6	CLK_MCH_BCLK#	29
HPWR#	J11	H_DPWR#	3
H_DRDY#	E9	H_DRDY#	3
H_HIT#	H9	H_HIT#	3
H_HITM#	E12	H_HITM#	3
H_LOCK#	H11	H_LOCK#	3
H_TRDY#	C8	H_TRDY#	3
H_DINV#_0	J8	H_DINV#_0	3
H_DINV#_1	L3	H_DINV#_1	3
H_DINV#_2	Y13	H_DINV#_2	3
H_DINV#_3	Y1	H_DINV#_3	3
H_DSTBN#_0	L10	H_DSTBN#_0	3
H_DSTBN#_1	M7	H_DSTBN#_1	3
H_DSTBN#_2	AA5	H_DSTBN#_2	3
H_DSTBN#_3	AE6	H_DSTBN#_3	3
H_DSTBP#_0	L9	H_DSTBP#_0	3
H_DSTBP#_1	M8	H_DSTBP#_1	3
H_DSTBP#_2	AA6	H_DSTBP#_2	3
H_DSTBP#_3	AE5	H_DSTBP#_3	3
H_REQ#_0	B15	H_REQ#_0	3
H_REQ#_1	K13	H_REQ#_1	3
H_REQ#_2	F13	H_REQ#_2	3
H_REQ#_3	B13	H_REQ#_3	3
H_REQ#_4	B14	H_REQ#_4	3
H_RS#_0	B6	H_RS#_0	3
H_RS#_1	F12	H_RS#_1	3
H_RS#_2	C8	H_RS#_2	3



RX1103->SL1103, RX1102->SL1102, RX1104->SL1104
G60VX R2.0 costdown 20090328

<http://hobi-elektronika.net>

PEGATRON Title : NB_DDR2/PEG (2)
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
 Size Custom Project Name G60VX Rev R 1.2
 Date: Wednesday, April 08, 2009 Sheet 11 of 100

7 M_A_DQ[0:63]

M A DQ0	AJ36	SA_DO_0
M A DQ1	AJ41	SA_DO_1
M A DQ2	AN38	SA_DO_2
M A DQ3	AM38	SA_DO_3
M A DQ4	AJ36	SA_DO_4
M A DQ5	AJ40	SA_DO_5
M A DQ6	AM44	SA_DO_6
M A DQ7	AM42	SA_DO_7
M A DQ8	AN43	SA_DO_8
M A DQ9	AN44	SA_DO_9
M A DQ10	AL40	SA_DO_10
M A DQ11	AT38	SA_DO_11
M A DQ12	AN41	SA_DO_12
M A DQ13	AN39	SA_DO_13
M A DQ14	AJ44	SA_DO_14
M A DQ15	AL42	SA_DO_15
M A DQ16	AV39	SA_DO_16
M A DQ17	AY44	SA_DO_17
M A DQ18	BA40	SA_DO_18
M A DQ19	BD43	SA_DO_19
M A DQ20	AV41	SA_DO_20
M A DQ21	AY43	SA_DO_21
M A DQ22	BB41	SA_DO_22
M A DQ23	BC40	SA_DO_23
M A DQ24	AY37	SA_DO_24
M A DQ25	BD38	SA_DO_25
M A DQ26	AV37	SA_DO_26
M A DQ27	AT36	SA_DO_27
M A DQ28	AY38	SA_DO_28
M A DQ29	BB38	SA_DO_29
M A DQ30	AV36	SA_DO_30
M A DQ31	AW36	SA_DO_31
M A DQ32	BD13	SA_DO_32
M A DQ33	AU11	SA_DO_33
M A DQ34	BC11	SA_DO_34
M A DQ35	BA12	SA_DO_35
M A DQ36	AU13	SA_DO_36
M A DQ37	AV13	SA_DO_37
M A DQ38	BD12	SA_DO_38
M A DQ39	BC12	SA_DO_39
M A DQ40	BB9	SA_DO_40
M A DQ41	BA9	SA_DO_41
M A DQ42	AU10	SA_DO_42
M A DQ43	AV9	SA_DO_43
M A DQ44	BA11	SA_DO_44
M A DQ45	BD9	SA_DO_45
M A DQ46	AY8	SA_DO_46
M A DQ47	BA6	SA_DO_47
M A DQ48	AV5	SA_DO_48
M A DQ49	AV7	SA_DO_49
M A DQ50	AT9	SA_DO_50
M A DQ51	AN8	SA_DO_51
M A DQ52	AU5	SA_DO_52
M A DQ53	AU6	SA_DO_53
M A DQ54	AT5	SA_DO_54
M A DQ55	AN10	SA_DO_55
M A DQ56	AM11	SA_DO_56
M A DQ57	AM5	SA_DO_57
M A DQ58	AJ9	SA_DO_58
M A DQ59	AJ8	SA_DO_59
M A DQ60	AN12	SA_DO_60
M A DQ61	AM13	SA_DO_61
M A DQ62	AJ11	SA_DO_62
M A DQ63	AJ12	SA_DO_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2

BD21	M A_BS0	7,9
BG18	M A_BS1	7,9
AT25	M A_BS2	7,9
BB20	M A_RAS#	7,9
BD20	M A_CAS#	7,9
AY20	M A_WE#	7,9

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

AM37	M A_DM0	M_A_DM[0:7]	7
AT41	M A_DM1		
AY41	M A_DM2		
AU39	M A_DM3		
BB12	M A_DM4		
AY6	M A_DM5		
AT7	M A_DM6		
AJ5	M A_DM7		

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

AJ44	M A_DQS0	M_A_DQS[0:7]	7
AT44	M A_DQS1		
BA43	M A_DQS2		
BC37	M A_DQS3		
AW12	M A_DQS4		
BC8	M A_DQS5		
AU8	M A_DQS6		
AM7	M A_DQS7		

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

AJ43	M A_DQS#0	M_A_DQS#[0:7]	7
AT43	M A_DQS#1		
BA44	M A_DQS#2		
BD37	M A_DQS#3		
AY12	M A_DQS#4		
BD8	M A_DQS#5		
AU9	M A_DQS#6		
AM8	M A_DQS#7		

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BA21	M A_A0	M_A_A[0:14]	7,9
BC24	M A_A1		
BG24	M A_A2		
BH24	M A_A3		
BG25	M A_A4		
BA24	M A_A5		
BD24	M A_A6		
BG27	M A_A7		
RF25	M A_A8		
AW24	M A_A9		
BC21	M A_A10		
BG26	M A_A11		
BH26	M A_A12		
BH17	M A_A13		
AY25	M A_A14		

8 M_B_DQ[0:63]

M B DQ0	AK47	SB_DO_0
M B DQ1	AH46	SB_DO_1
M B DQ2	AP47	SB_DO_2
M B DQ3	AP46	SB_DO_3
M B DQ4	AJ46	SB_DO_4
M B DQ5	AH46	SB_DO_5
M B DQ6	AM48	SB_DO_6
M B DQ7	AP48	SB_DO_7
M B DQ8	AU47	SB_DO_8
M B DQ9	AU46	SB_DO_9
M B DQ10	BA48	SB_DO_10
M B DQ11	AY48	SB_DO_11
M B DQ12	AT47	SB_DO_12
M B DQ13	AR47	SB_DO_13
M B DQ14	PA47	SB_DO_14
M B DQ15	BC47	SB_DO_15
M B DQ16	BC46	SB_DO_16
M B DQ17	BC44	SB_DO_17
M B DQ18	BG43	SB_DO_18
M B DQ19	BF43	SB_DO_19
M B DQ20	BE45	SB_DO_20
M B DQ21	BC41	SB_DO_21
M B DQ22	BF41	SB_DO_22
M B DQ23	BF41	SB_DO_23
M B DQ24	BG38	SB_DO_24
M B DQ25	BF38	SB_DO_25
M B DQ26	BH35	SB_DO_26
M B DQ27	BG35	SB_DO_27
M B DQ28	BH40	SB_DO_28
M B DQ29	BG39	SB_DO_29
M B DQ30	BG34	SB_DO_30
M B DQ31	BH34	SB_DO_31
M B DQ32	BH14	SB_DO_32
M B DQ33	BG14	SB_DO_33
M B DQ34	BH11	SB_DO_34
M B DQ35	BG8	SB_DO_35
M B DQ36	BH12	SB_DO_36
M B DQ37	BF11	SB_DO_37
M B DQ38	BF8	SB_DO_38
M B DQ39	BG7	SB_DO_39
M B DQ40	BC5	SB_DO_40
M B DQ41	BC6	SB_DO_41
M B DQ42	AV3	SB_DO_42
M B DQ43	AY1	SB_DO_43
M B DQ44	BF6	SB_DO_44
M B DQ45	BF5	SB_DO_45
M B DQ46	BA1	SB_DO_46
M B DQ47	B03	SB_DO_47
M B DQ48	AV2	SB_DO_48
M B DQ49	AU3	SB_DO_49
M B DQ50	AR3	SB_DO_50
M B DQ51	AN2	SB_DO_51
M B DQ52	AY2	SB_DO_52
M B DQ53	AV1	SB_DO_53
M B DQ54	AP3	SB_DO_54
M B DQ55	AP1	SB_DO_55
M B DQ56	AL1	SB_DO_56
M B DQ57	AL2	SB_DO_57
M B DQ58	AJ1	SB_DO_58
M B DQ59	AH1	SB_DO_59
M B DQ60	AM2	SB_DO_60
M B DQ61	AM3	SB_DO_61
M B DQ62	AH3	SB_DO_62
M B DQ63	AJ3	SB_DO_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2

BC16	M_B_BS0	8,9
BB17	M_B_BS1	8,9
BB33	M_B_BS2	8,9
AU17	M_B_RAS#	8,9
BG16	M_B_CAS#	8,9
BF14	M_B_WE#	8,9

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

AM47	M_B_DM0	M_B_DM[0:7]	8
AY47	M_B_DM1		
BD40	M_B_DM2		
BF35	M_B_DM3		
BG11	M_B_DM4		
BA3	M_B_DM5		
AP1	M_B_DM6		
AK2	M_B_DM7		

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

AL47	M_B_DQS0	M_B_DQS[0:7]	8
AV48	M_B_DQS1		
BG41	M_B_DQS2		
BG37	M_B_DQS3		
BH9	M_B_DQS4		
BB2	M_B_DQS5		
AU1	M_B_DQS6		
AN6	M_B_DQS7		

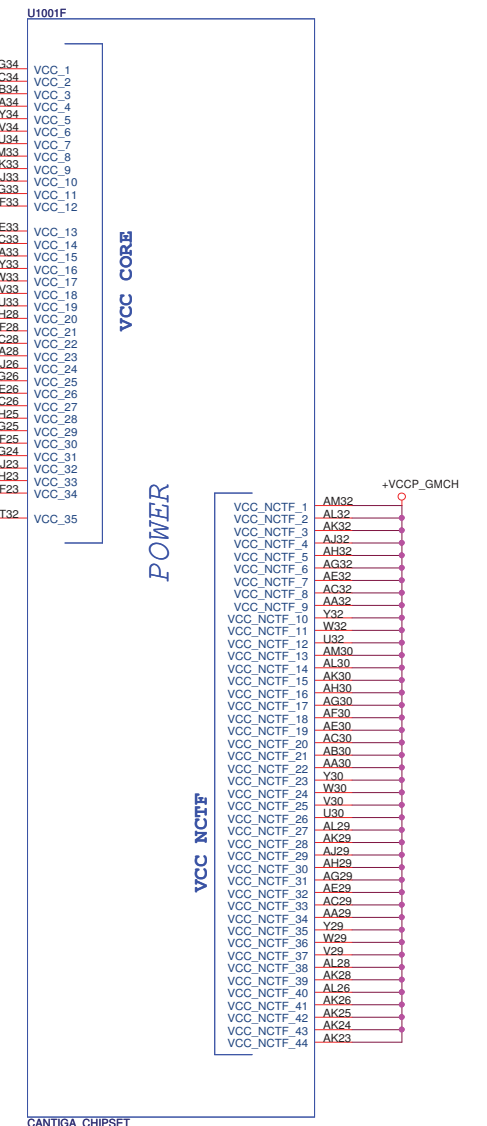
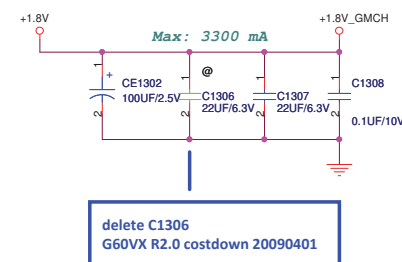
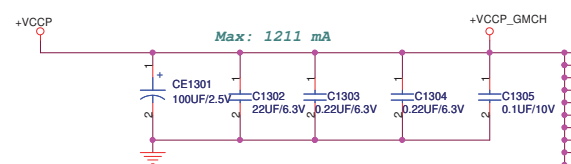
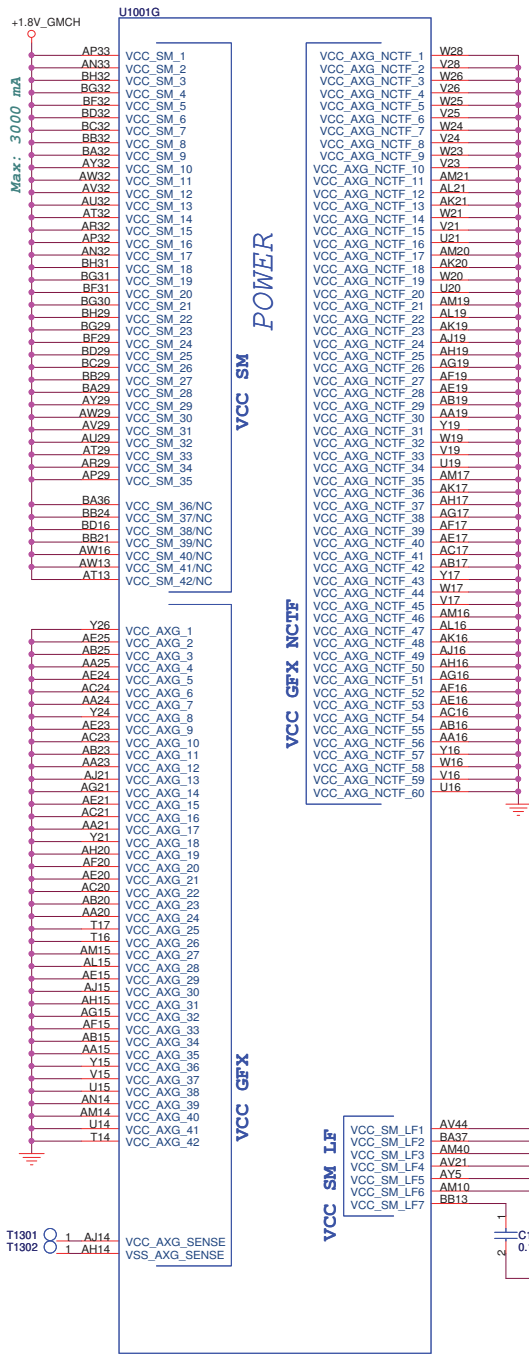
SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

AL46	M_B_DQS#0	M_B_DQS#[0:7]	8
AV47	M_B_DQS#1		
BH41	M_B_DQS#2		
BH37	M_B_DQS#3		
BG9	M_B_DQS#4		
BC2	M_B_DQS#5		
AT2	M_B_DQS#6		
AN5	M_B_DQS#7		

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

AV17	M_B_A0	M_B_A[0:14]	8,9
BA25	M_B_A1		
BC25	M_B_A2		
AU25	M_B_A3		
AW25	M_B_A4		
BB28	M_B_A5		
AU28	M_B_A6		
AT33	M_B_A7		
BD33	M_B_A8		
BB16	M_B_A9		
AW33	M_B_A10		
AY33	M_B_A11		
BH15	M_B_A12		
AU33	M_B_A13		
AU33	M_B_A14		

PEGATRON Title : NB_DDR2 bus (3)
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
 Size Custom Project Name G60VX Rev R 1.2
 Date: Wednesday, April 08, 2009 Sheet 12 of 100



CANTIGA_CHIPSET

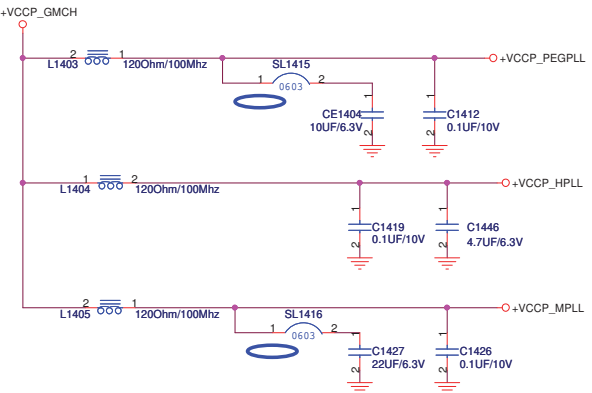
PEGATRON Title : **NB_POWER (4)**

Pegatron BU2 HW Team 3 Engineer: **Kevin1_Guo**

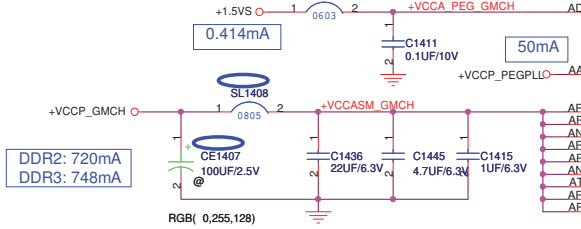
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Sunday, April 05, 2009 Sheet 13 of 100

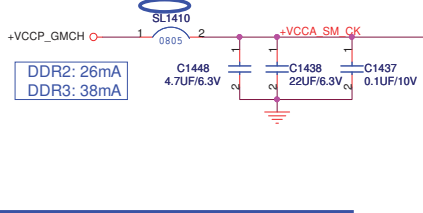
R1415->SL1415;R1416->SL1416
 R1406->SL1406;R1408->SL1408
 R1410->SL1410; delete R1414
 delete CE1407 C1442 C1449
 R1405->SL1405->delete SL1405 Height limit;
 R1401->SL1401;R1409->SL1409
 R1404->SL1404;R1403->SL1403
 Delete C1404
 G60VX R2.0 costdown 20090401



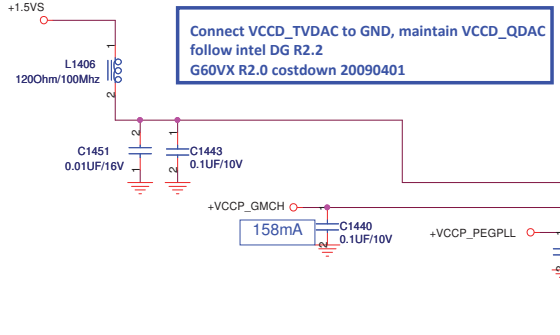
24mA
140mA



DDR2: 720mA
DDR3: 748mA

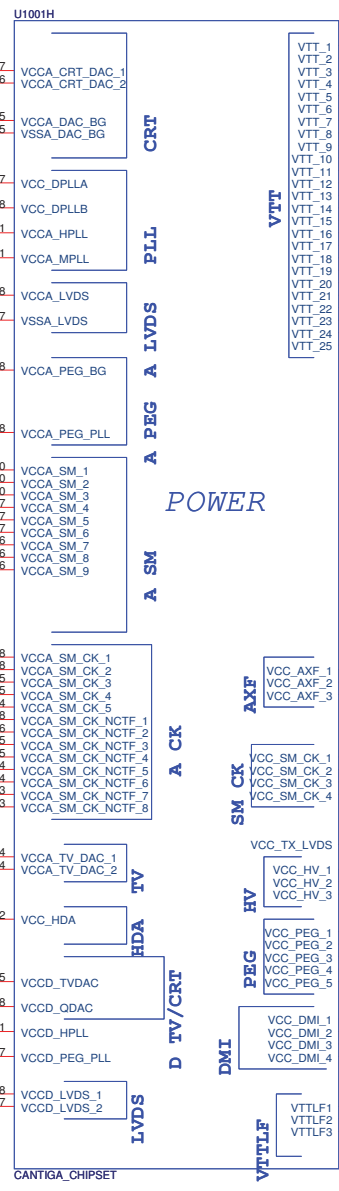


DDR2: 26mA
DDR3: 38mA



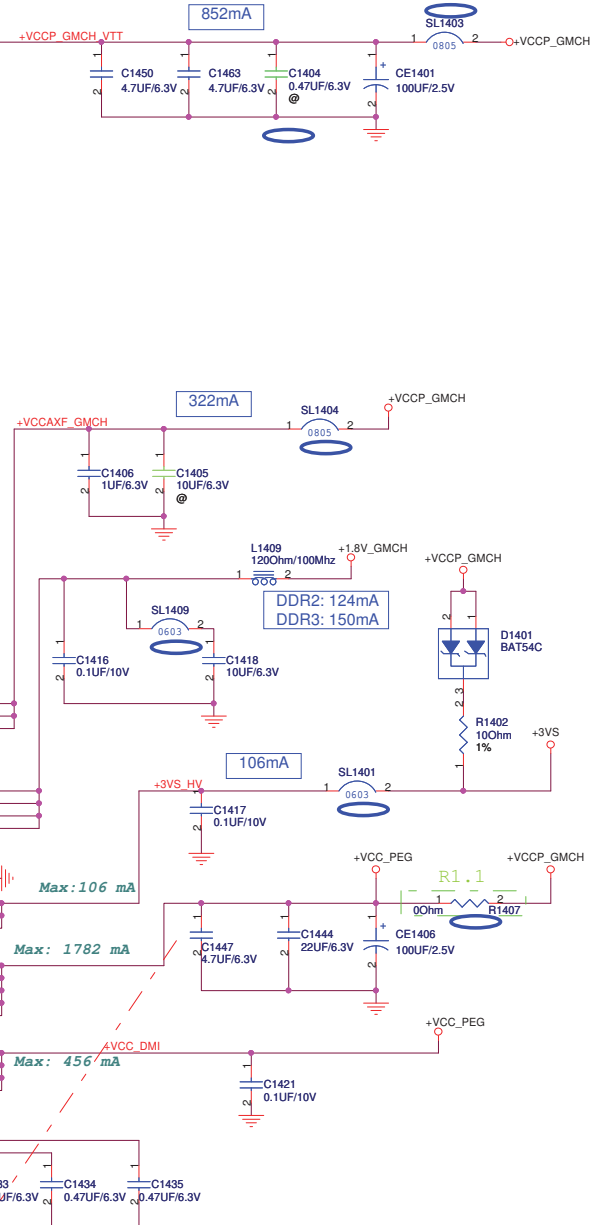
Connect VCCD_TV_DAC to GND, maintain VCCD_QDAC follow intel DG R2.2
 G60VX R2.0 costdown 20090401

158mA

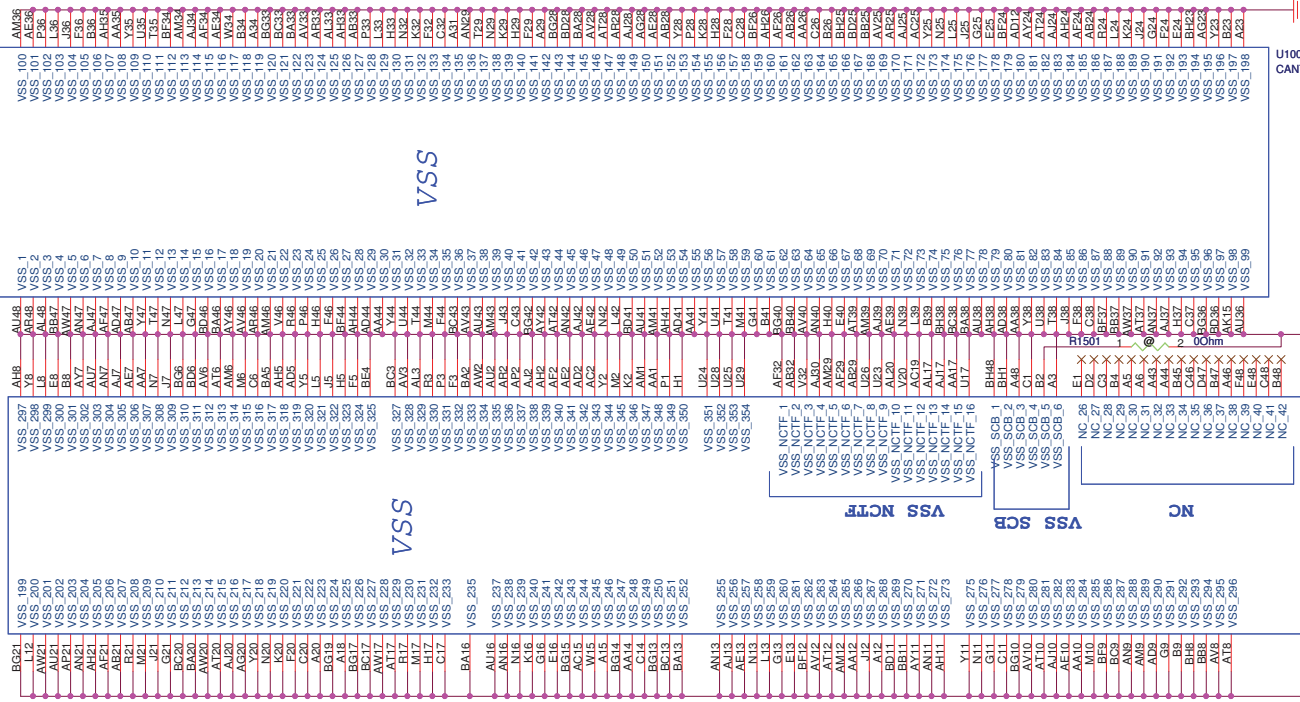


POWER

Change C1447 from 4.7UF/6.3V 0805 to 4.7UF/6.3V 0603 to satisfy the mechinal height strain
 2008-11-26-14-22



PEGATRON		Title : NB_POWER (5)	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	R 1.2
Custom	G60VX	Date:	Wednesday, April 08, 2009
Date: Wednesday, April 08, 2009		Sheet	14 of 100



- 11 MCH_CFG_5
- 11 MCH_CFG_6
- 11 MCH_CFG_7
- 11 MCH_CFG_9
- 11 MCH_CFG_10
- 11 MCH_CFG_12
- 11 MCH_CFG_13
- 11 MCH_CFG_16
- 11 MCH_CFG_19
- 11 MCH_CFG_20

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

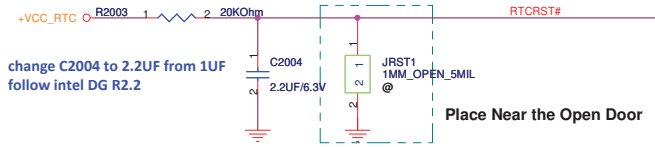
CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

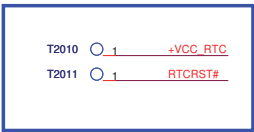
CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

<http://hobi-elektronika.net>

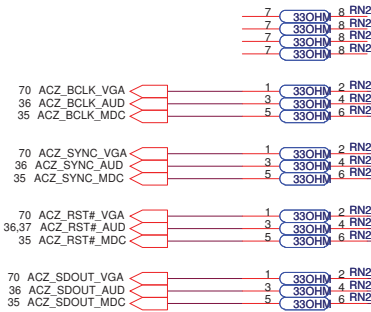
PEGATRON		Title : NB_GND/Strapping (6)	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Wednesday, April 08, 2009		Sheet 15 of 100	



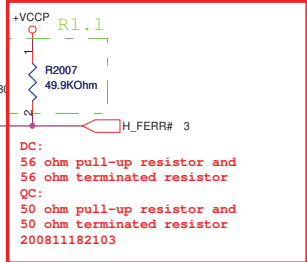
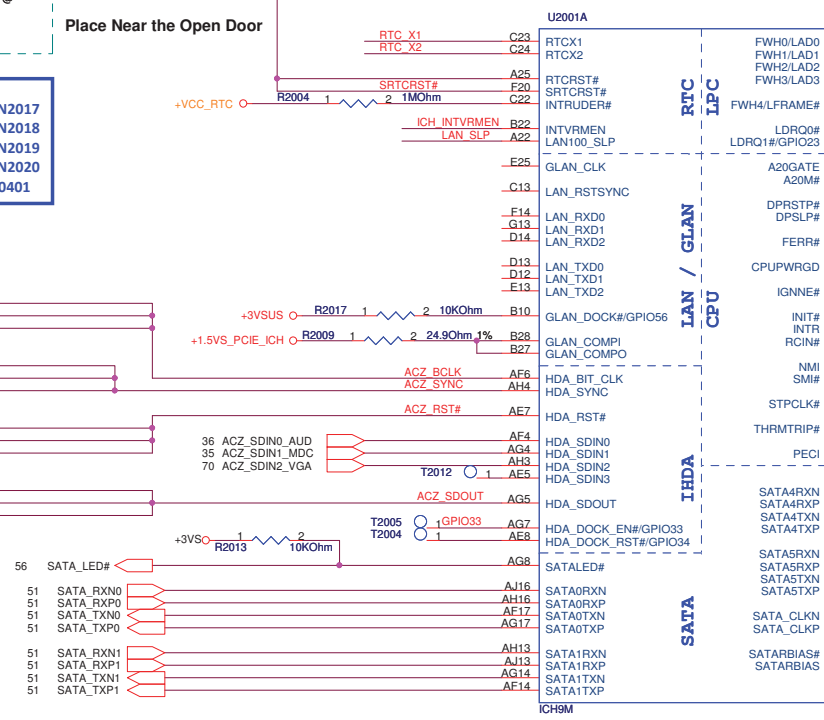
change RX2001,RX2002,RX2003,RX2004
RX2007,RX2008 to short land
change reserved RX2005 to SL2005
G60VX R2.0 costdown 20090401



delete R2008 C2005
RX2017,RX2010,RX2009->RN2017
RX2018,RX2011,RX2012->RN2018
RX2019,RX2013,RX2014->RN2019
RX2020,RX2015,RX2016->RN2020
G60VX R2.0 costdown 20090401



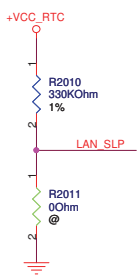
Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
May need change J3402
For Modem Delete
20081107



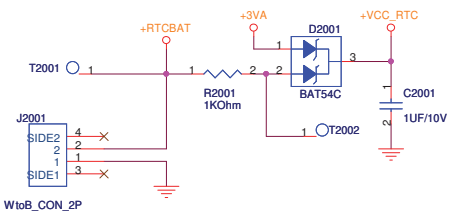
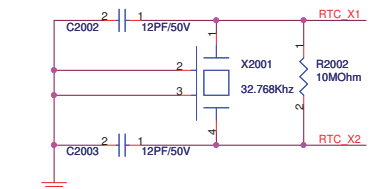
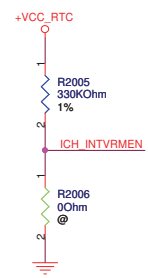
SATA1 HDD 1
SATA2 ODD
SATA4 HDD 2
SATA5 ESATA



VccLAN1_05 & VccCL1_05
Internal VR
High = Enable (Default)
Low = Disable



VccSus1_05, VccSus1_5, &
VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable

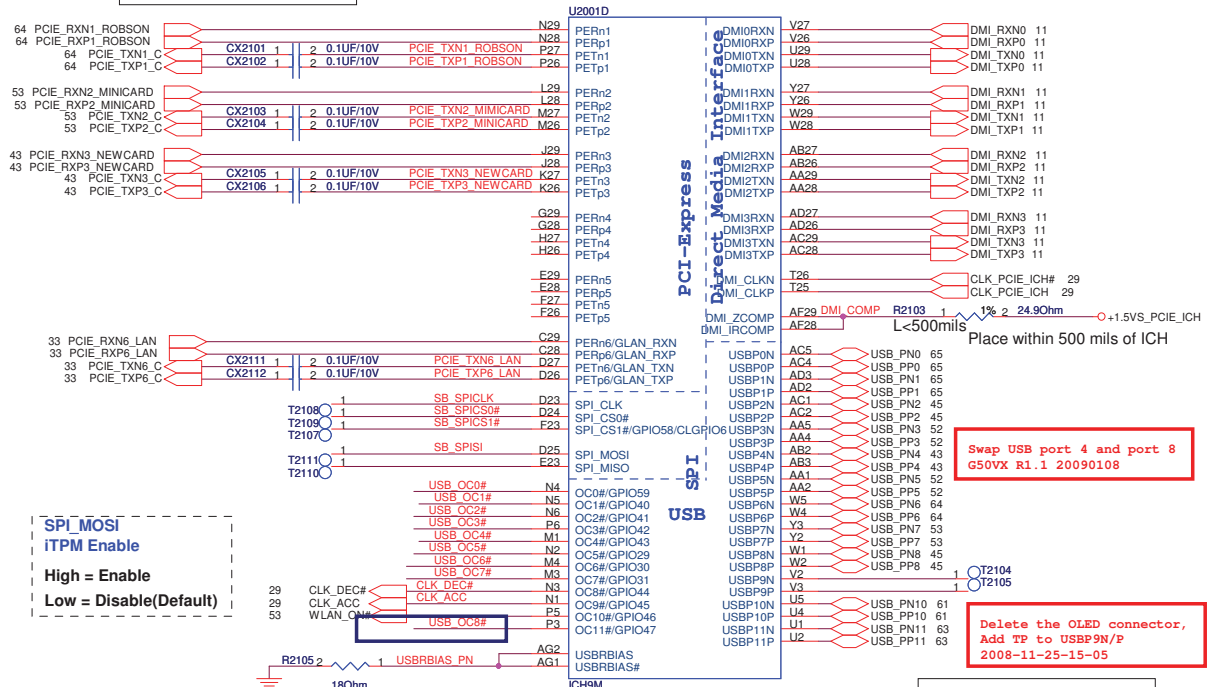
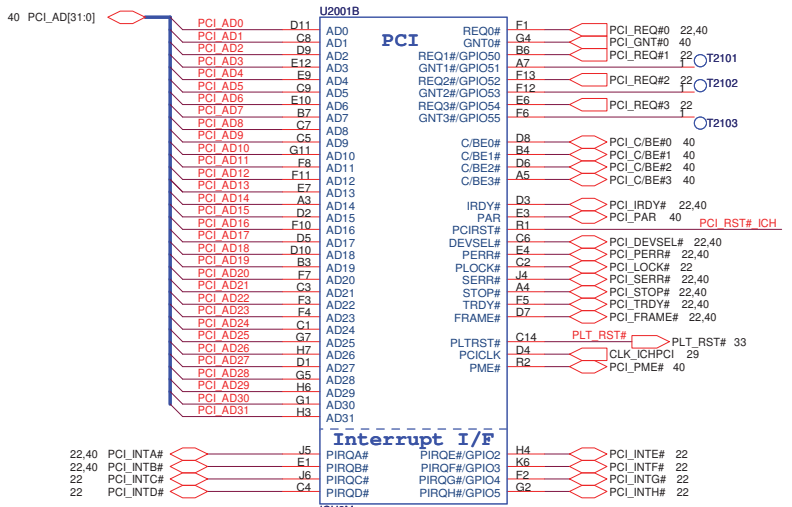


[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

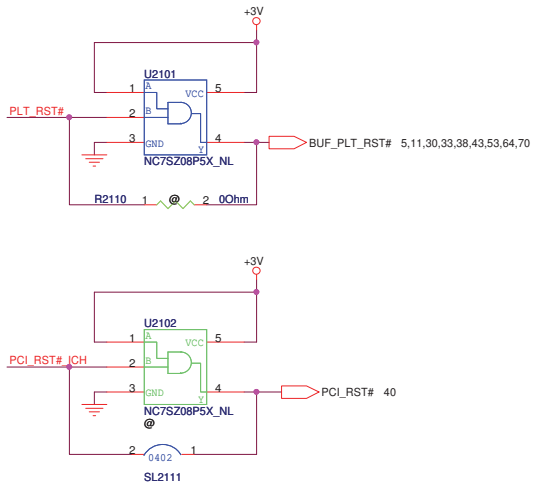
Checklist recommends pull up in the ICH9 side
although functionality not used
DC:
56 ohm pull-up resistor and
55 ohm terminated resistor
QC:
50 ohm pull-up resistor and
50 ohm terminated resistor
20081190906



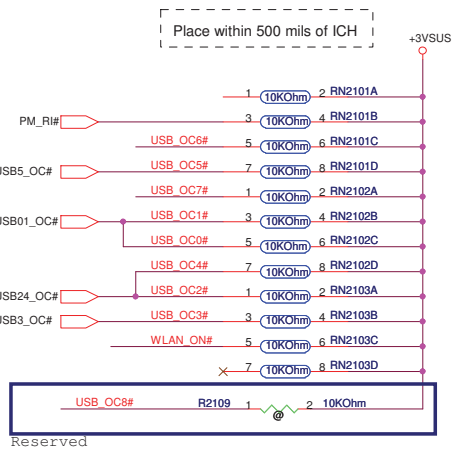
- PCIE1 Robson/TV Tuner
- PCIE2 MiniCard
- PCIE3 NewCard
- PCIE4 NC
- PCIE5 SATA RAID
- PCIE6 LAN



SPI_MOSI
ITPM Enable
High = Enable
Low = Disable(Default)



change R2111 to short land
G60VX R2.0 costdown 20090401



ICH9 Boot BIOS select

	GNT#0	CS#1	
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

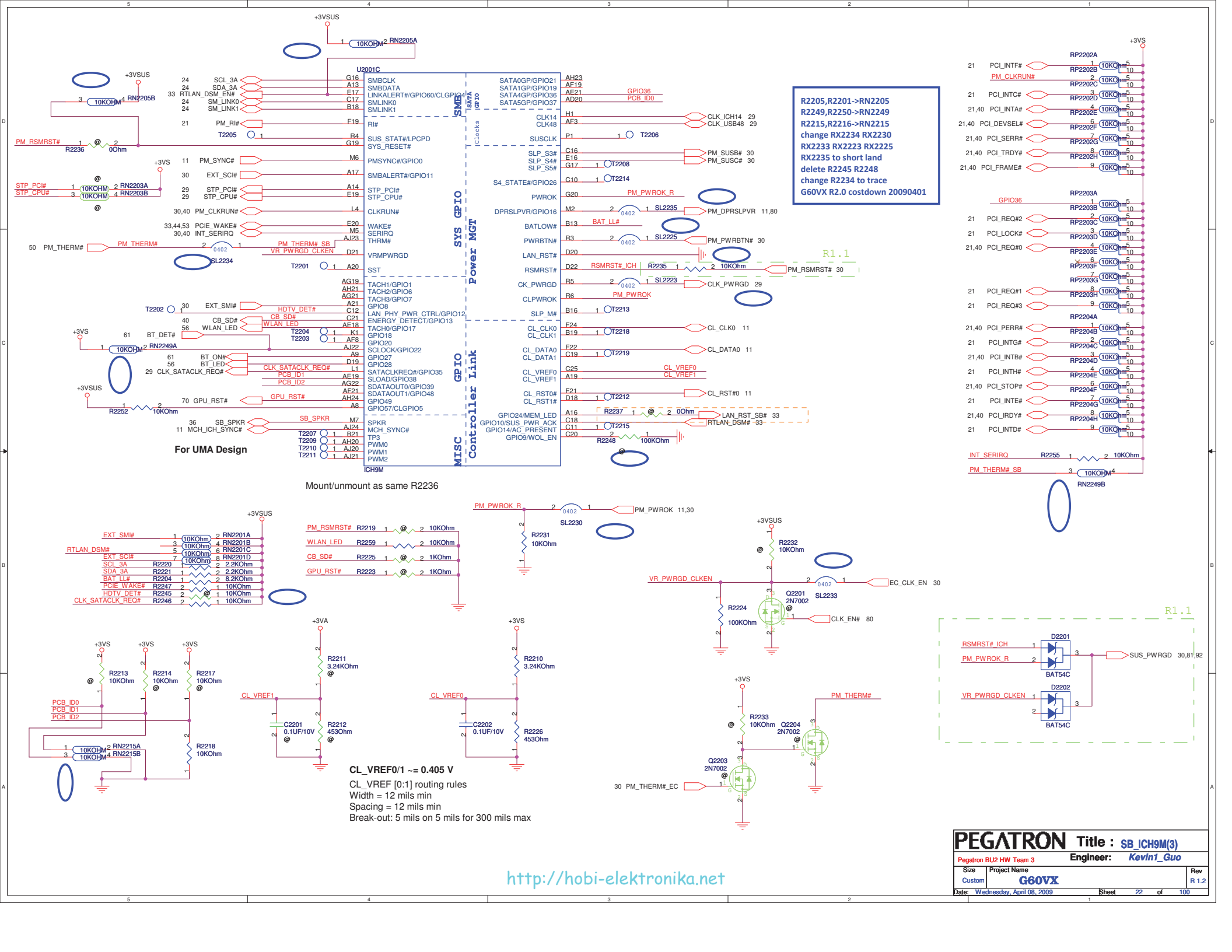
(default)

- USB0 External Port 1
- USB1 External Port 2
- USB2 External Port 3
- USB3 External Port 4
- USB4 CMOS Camera
- USB5 External Port 5
- USB6 OLED
- USB7 WiMax
- USB8 NewCard
- USB9 TV-Tuner
- USB10 Blue-Tooth
- USB11 Finger Printer

When supporting CLK GEN Turbo PIN, UNI R2107.



PEGATRON Title : SB_ICH9M(2)
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
 Size Custom Project Name G60VX Rev R.1.2
 Date: Wednesday, April 08, 2009 Sheet 21 of 100



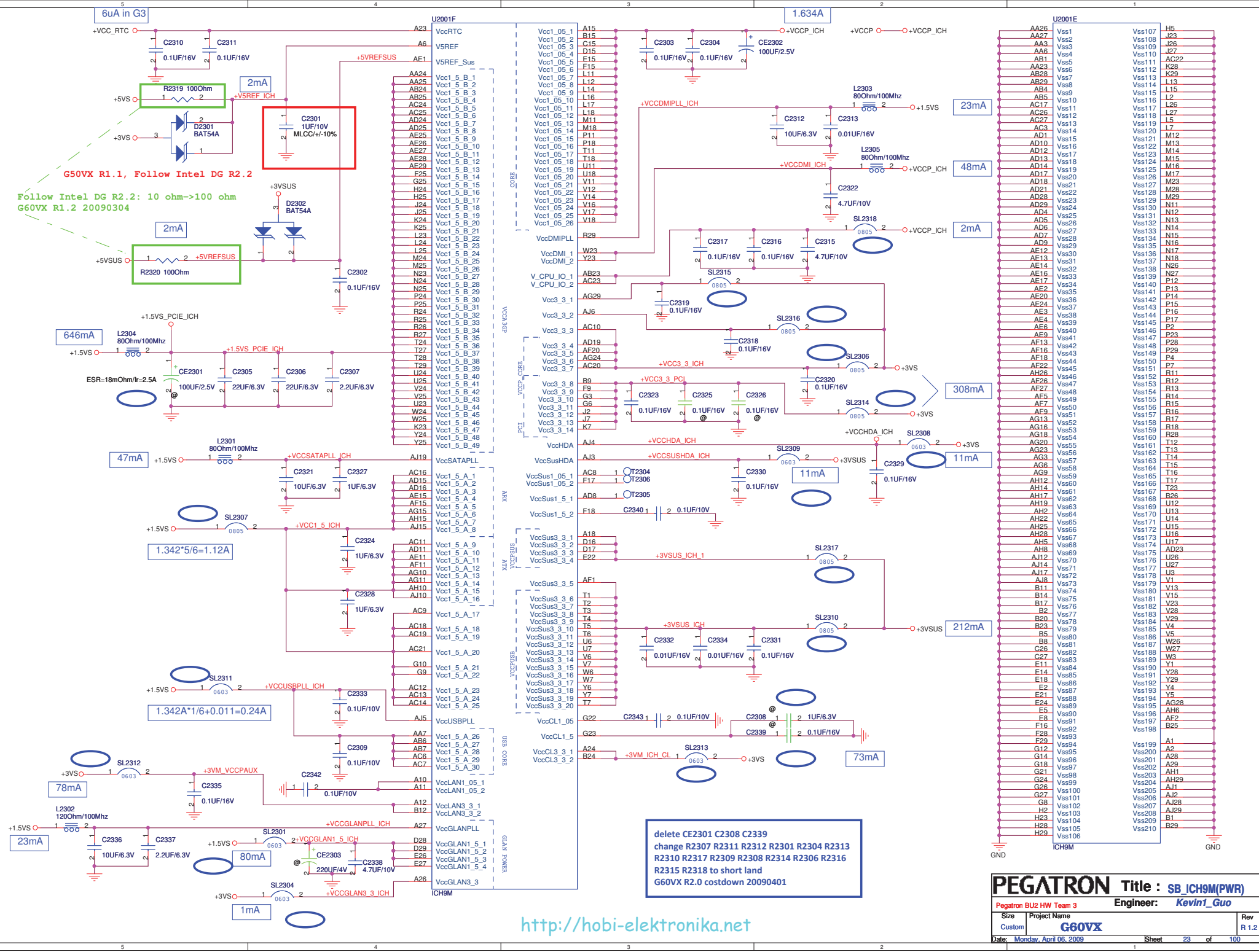
R2205,R2201->RN2205
R2249,R2250->RN2249
R2215,R2216->RN2215
change RX2234 RX2230
RX2233 RX2223 RX2225
RX2235 to short land
delete R2245 R2248
change R2234 to trace
G60VX R2.0 costdown 20090401

For UMA Design

Mount/unmount as same R2236

CL_VREF0/1 ≈ 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max

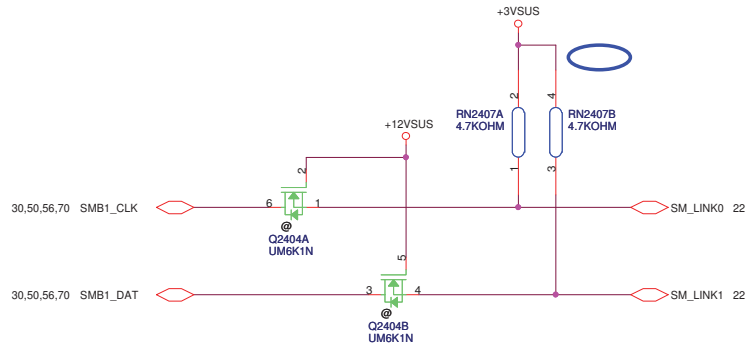
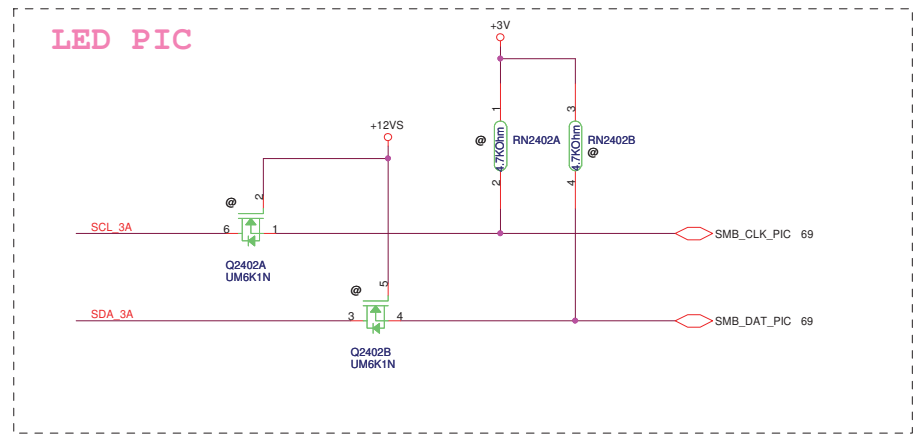
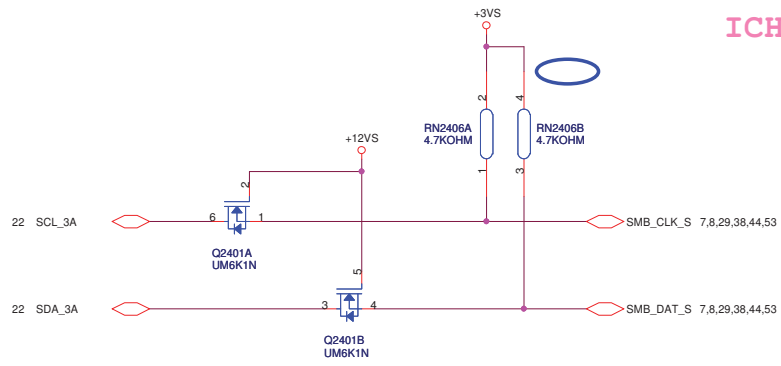
PEGATRON		Title : SB ICH9M(3)	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	R 1.2
Custom	G60VX	Date:	Wednesday, April 08, 2009
Sheet	22	of	100



G50VX R1.1, Follow Intel DG R2.2
 Follow Intel DG R2.2: 10 ohm -> 100 ohm
 G60VX R1.2 20090304

delete CE2301 C2308 C2339
 change R2307 R2311 R2312 R301 R2304 R2313
 R2310 R2317 R2309 R2308 R2314 R2306 R2316
 R2315 R2318 to short land
 G60VX R2.0 costdown 20090401

PEGATRON Title: **SB_ICh9M(PWR)**
 Pegatron BU2 HW Team 3 Engineer: **Kevin1_Guo**
 Size Custom **G60VX** Rev R 1.2
 Date: **Monday, April 06, 2009** Sheet 23 of 100

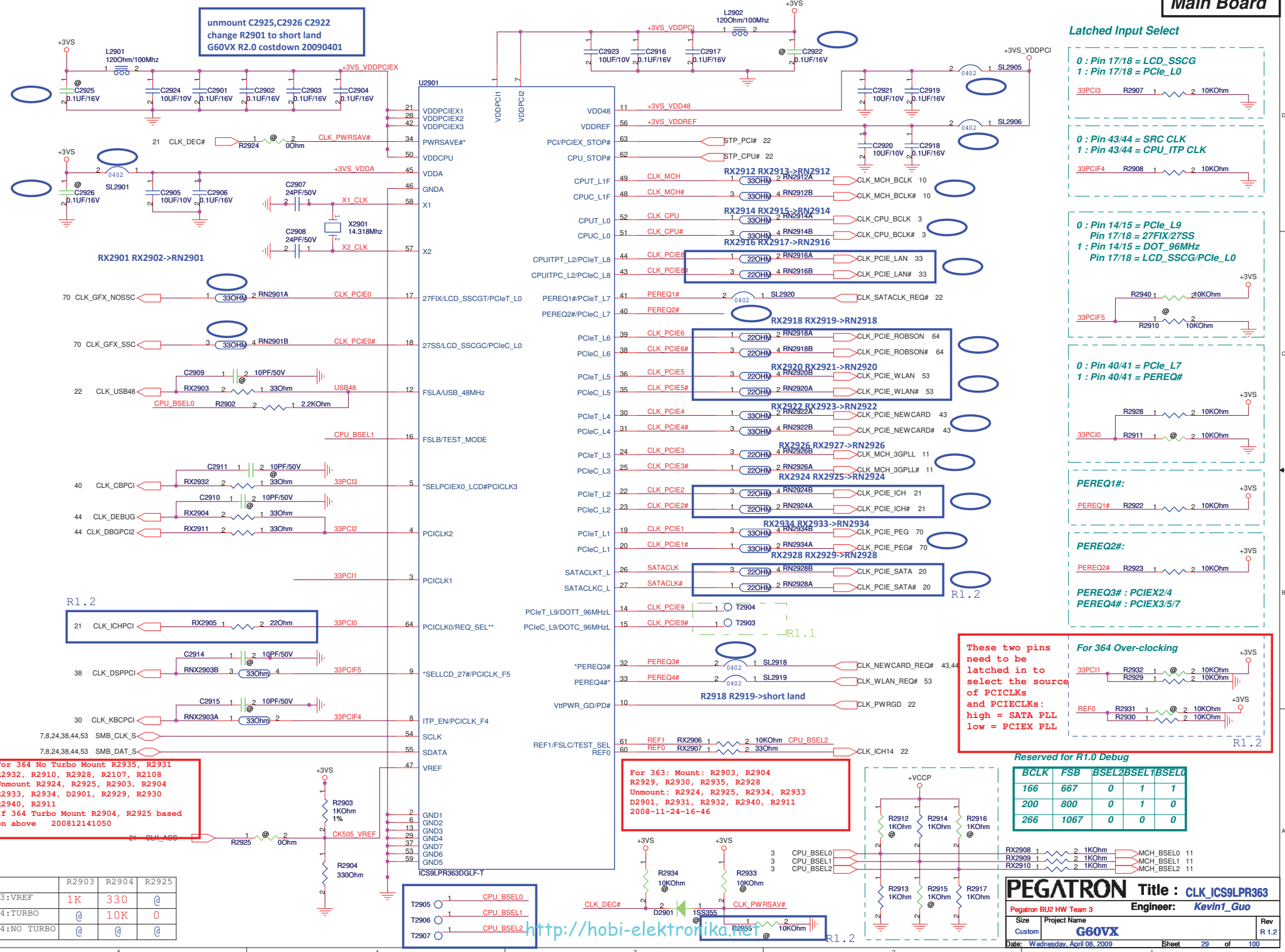


delete R2406 R2405; add RN2406
 delete R2407 R2408; add RN2407
 G60VX R2.0 costdown 20090401

<http://hobi-elektronika.net>

PEGATRON		Title : SB_ICH9M-Other	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX	Date: Thursday, April 02, 2009	Rev R 1.2
		Sheet 24	of 100

unmount C2925, C2926 C2922
change R2901 to short land
G60VX R2.0 costdown 20090401



Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0

0 : Pin 43/44 = SRC_CLK
1 : Pin 43/44 = CPU_ITP_CLK

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0

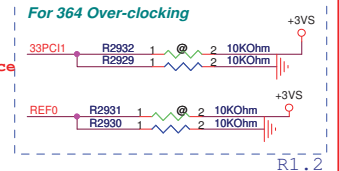
0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#

PEREQ1#:
PEREQ1# R2922 1 2 10KOhm

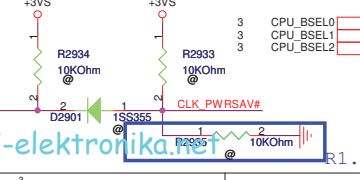
PEREQ2#:
PEREQ2# R2923 1 2 10KOhm

PEREQ3# : PCIe2/4
PEREQ4# : PCIe3/5/7

These two pins need to be latched in to select the source of PCIECLKs: high = SATA PLL low = PCIEX PLL



For 363: Mount: R2903, R2904
R2929, R2930, R2935, R2928
Unmount: R2924, R2925, R2934, R2933
D2901, R2931, R2932, R2940, R2911
2008-11-24-16-46



Reserved for R1.0 Debug

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

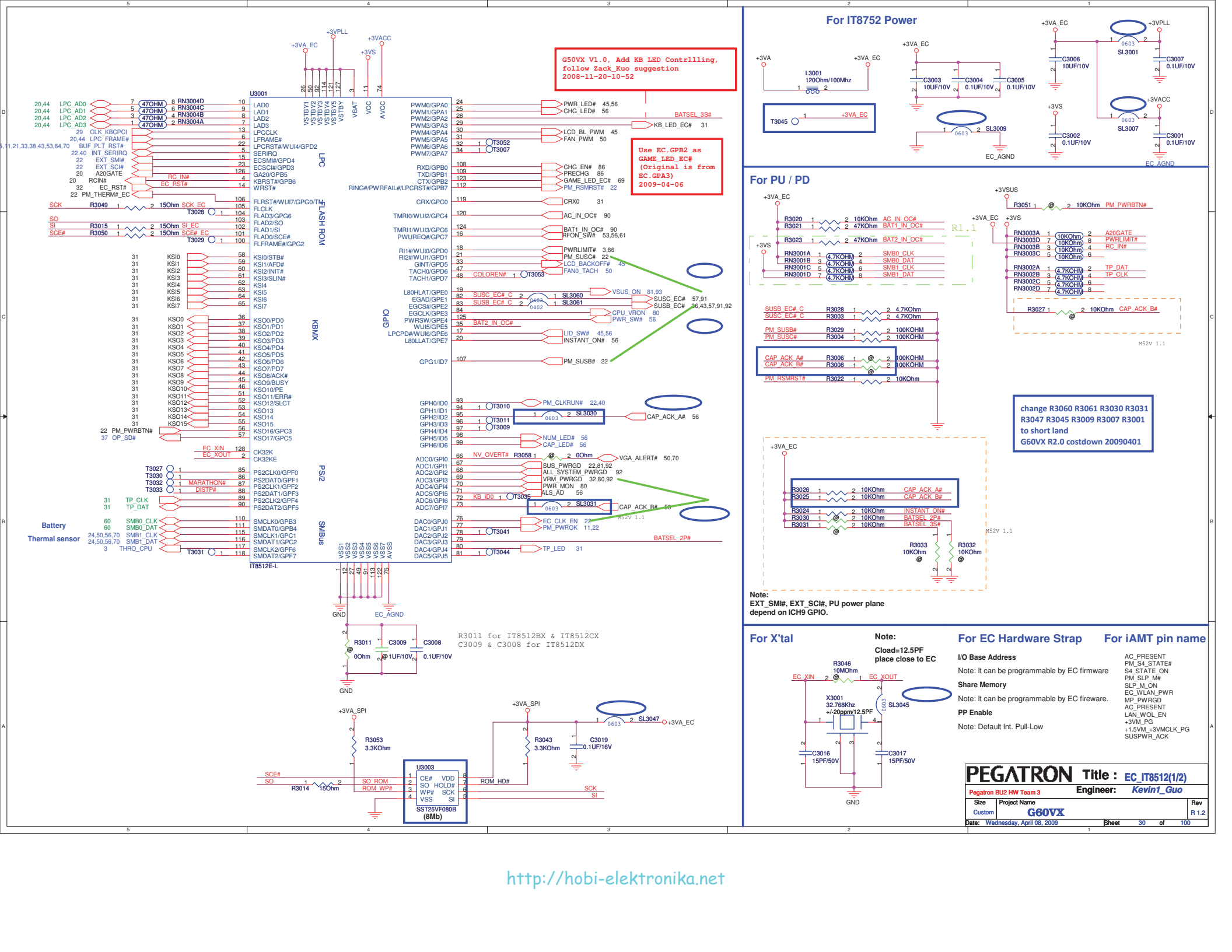
PEGATRON Title : CLK_ICS9LPR363
Engineer: Kevin1_Guo

Size Custom Project Name G60VX

Date: Wednesday, April 08, 2009 Sheet 29 of 100

For 364 No Turbo Mount R2935, R2931
R2932, R2910, R2928, R2107, R2108
Unmount R2924, R2925, R2903, R2904
R2933, R2934, D2901, R2929, R2930
R2940, R2911
If 364 Turbo Mount R2904, R2925 based
on above 200812141050

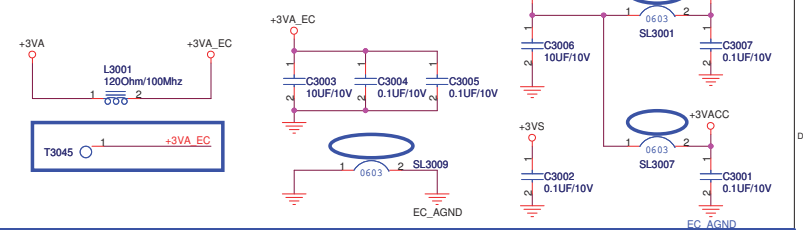
	R2903	R2904	R2925
363:VREF	1K	330	@
364:TURBO	@	10K	0
364:NO TURBO	@	@	@



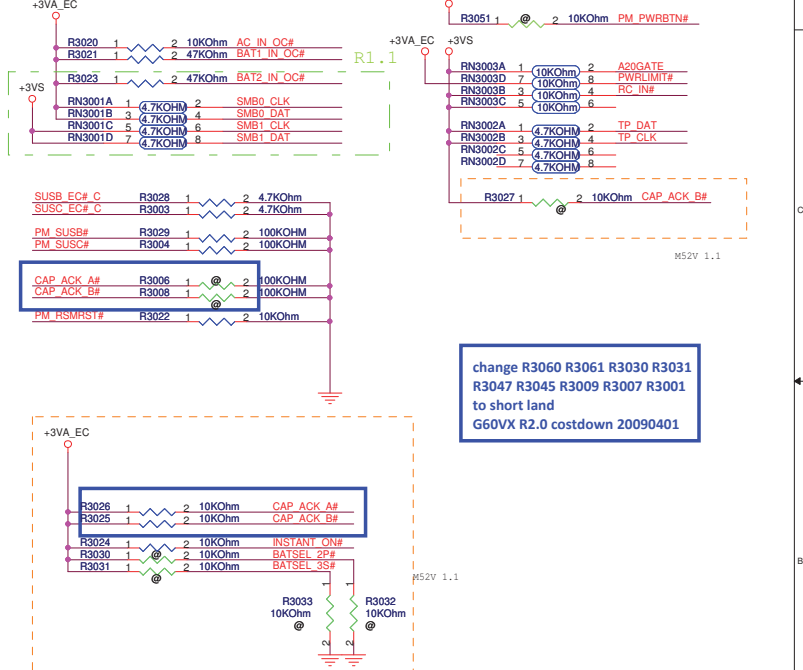
G50VX V1.0, Add KB LED Contrlling, follow Zack Kuo suggestion 2008-11-20-10-52

Use EC.GPB2 as GAME_LED_EC# (Original is from EC.GPA3) 2009-04-06

For IT8752 Power



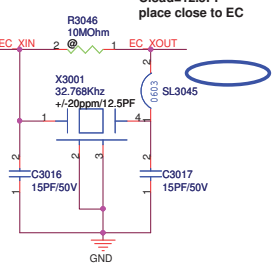
For PU / PD



change R3060 R3061 R3030 R3031 R3047 R3045 R3009 R3007 R3001 to short land G60VX R2.0 costdown 20090401

Note: EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal



Note: Cload=12.5PF place close to EC

For EC Hardware Strap

I/O Base Address
 Note: It can be programmable by EC firmware
 Share Memory
 Note: It can be programmable by EC firmware.
 PP Enable
 Note: Default Int. Pull-Low

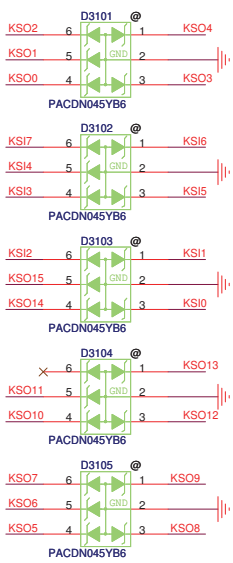
For iAMT pin name

AC_PRESENT
 PM_S4_STATE#
 S4_STATE_ON
 PM_SLP_#
 SLP_M_ON
 EC_WLAN_PWR
 MP_PWRGD
 AC_PRESENT
 LAN_WOL_EN
 +3VM_PG
 +3VM_-3VMCLK_PG
 SUSPWR_ACK

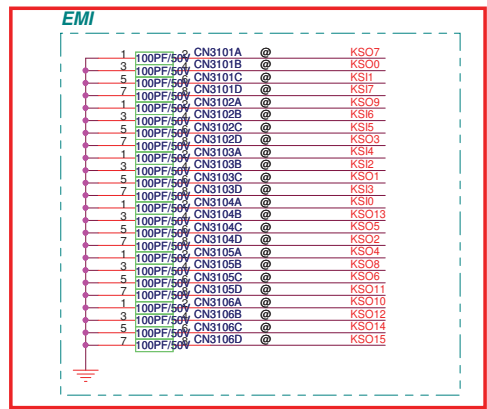
PEGATRON Title : EC_IT8512(1/2)
 Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R1.2

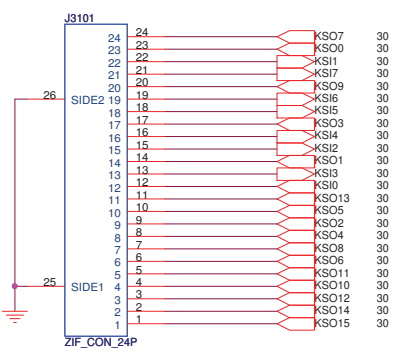
 Date: Wednesday, April 08, 2009 Sheet 30 of 100



G50VX R1.1 Change back
20090113

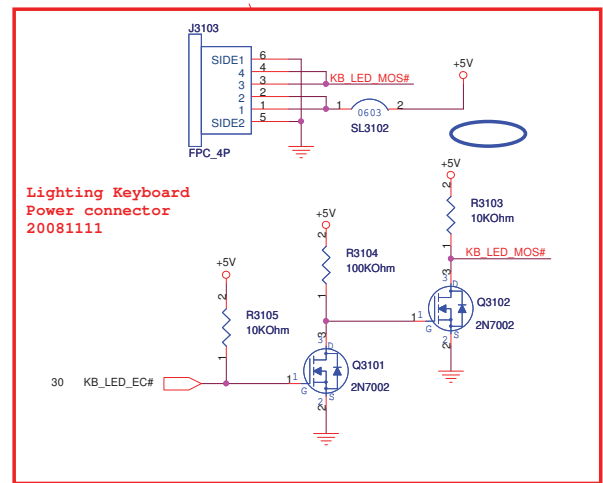


Keyboard

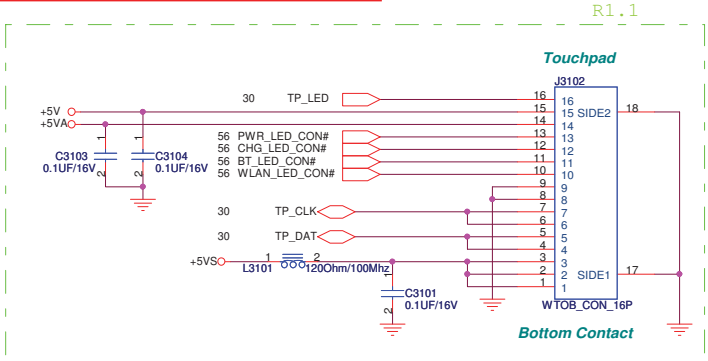


FPC_4P Reference P/N
12G183100402

change R3102 to 0603 short land
G60VX R2.0 costdown 20090401



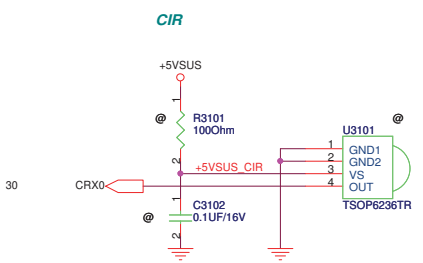
Lighting Keyboard
Power connector
20081111



R1.1

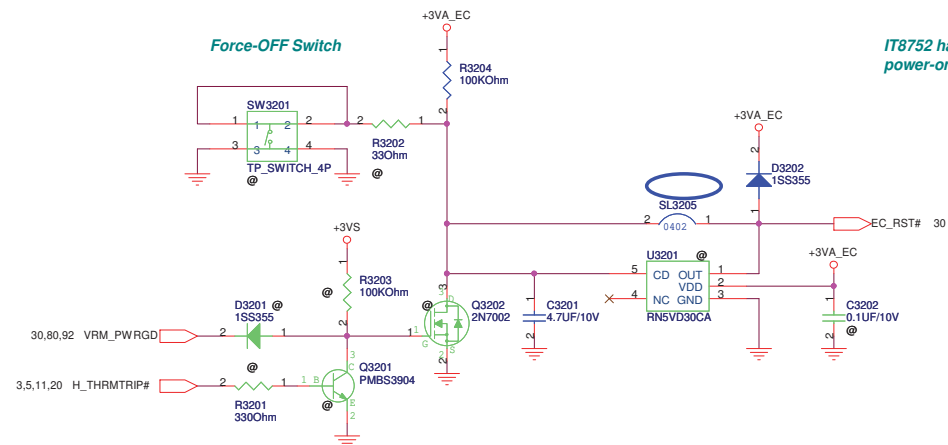
Touchpad

Bottom Contact



Unmount U3101
R3101, C3102 For
delete CIR
20081107

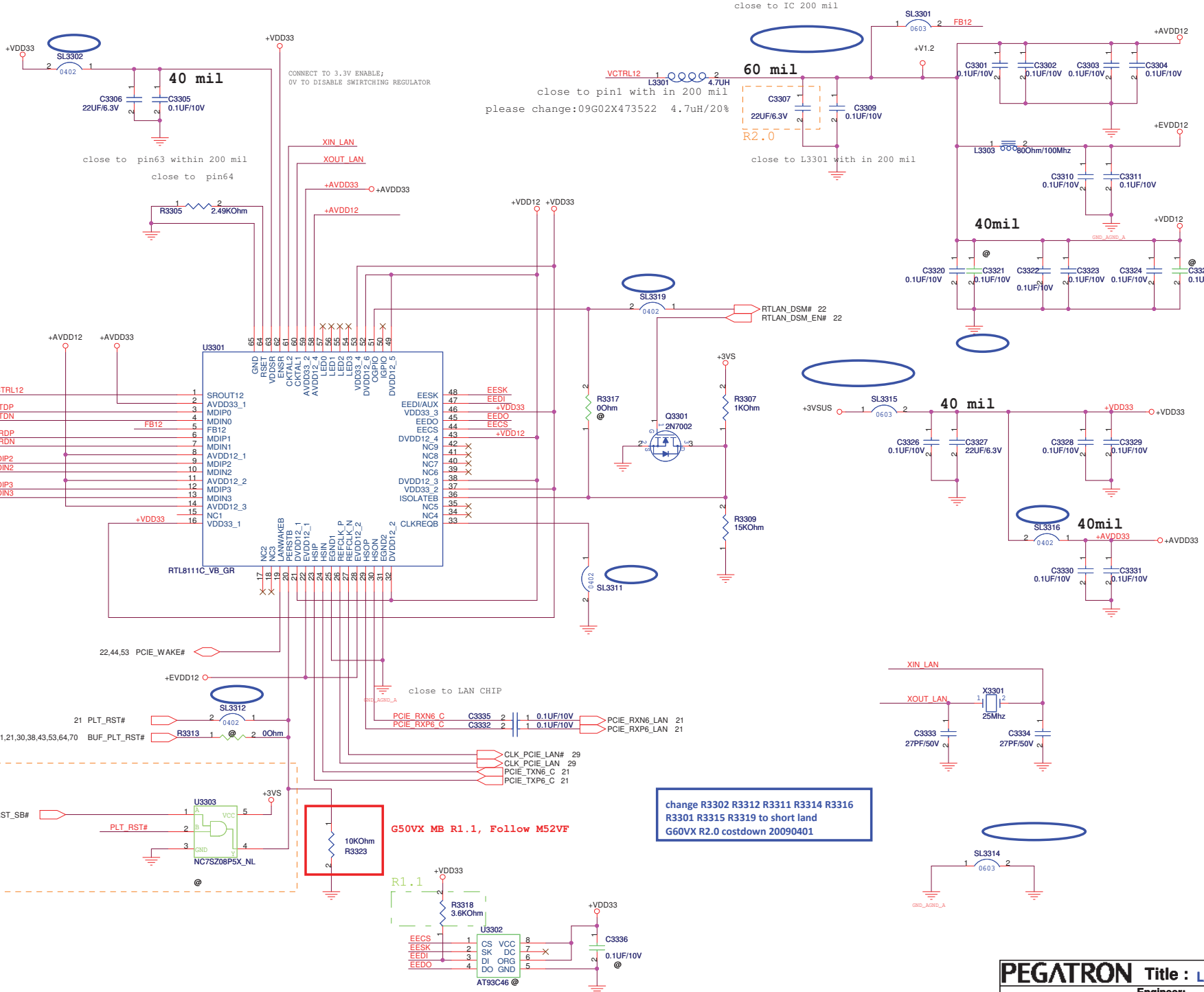
unmount SW3201 D3201 R3201 R3202 R3203 Q3201 Q3202
 change R3205 to short land
 G60VX R2.0 costdown 20090401



IT8752 has built-in level detection for power-on reset circuit



Reserve this part for protection
 G60VX R1.2 20090305



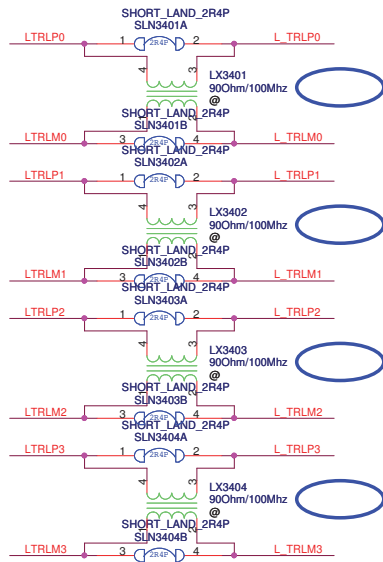
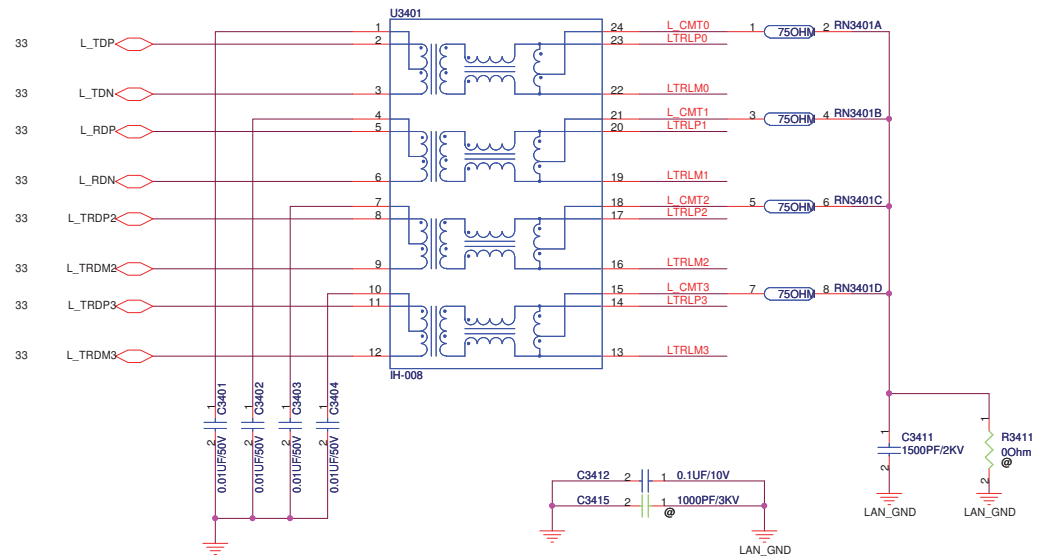
close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%

change R3302 R3312 R3311 R3314 R3316
R3301 R3315 R3319 to short land
G60VX R2.0 costdown 20090401

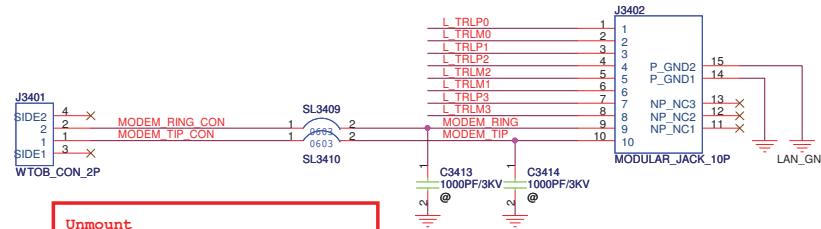
G50VX MB R1.1, Follow M52VF

<http://hobi-elektronika.net>

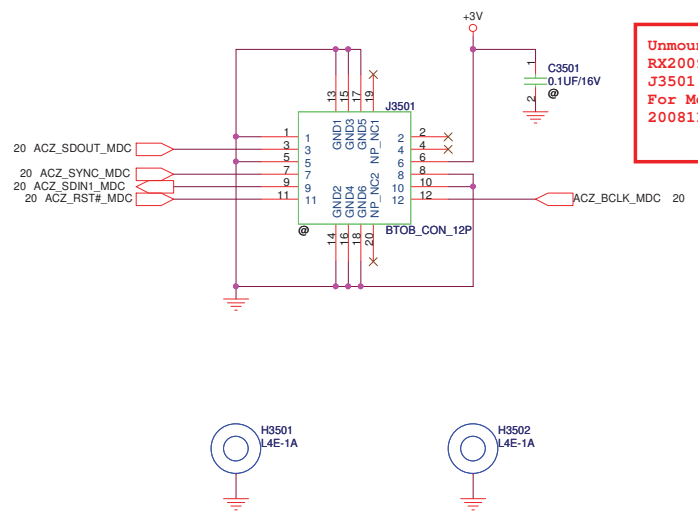
PEGATRON		Title : LAN-RTL811C	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX		Rev R 1.2
Date: Wednesday, April 08, 2009	Sheet 33 of 100		



change RNX3401 RNX3402 RNX3403 RNX3404 to integrated short land;
change R3409 R3410 to short land G60VX R2.0 costdown 20090402



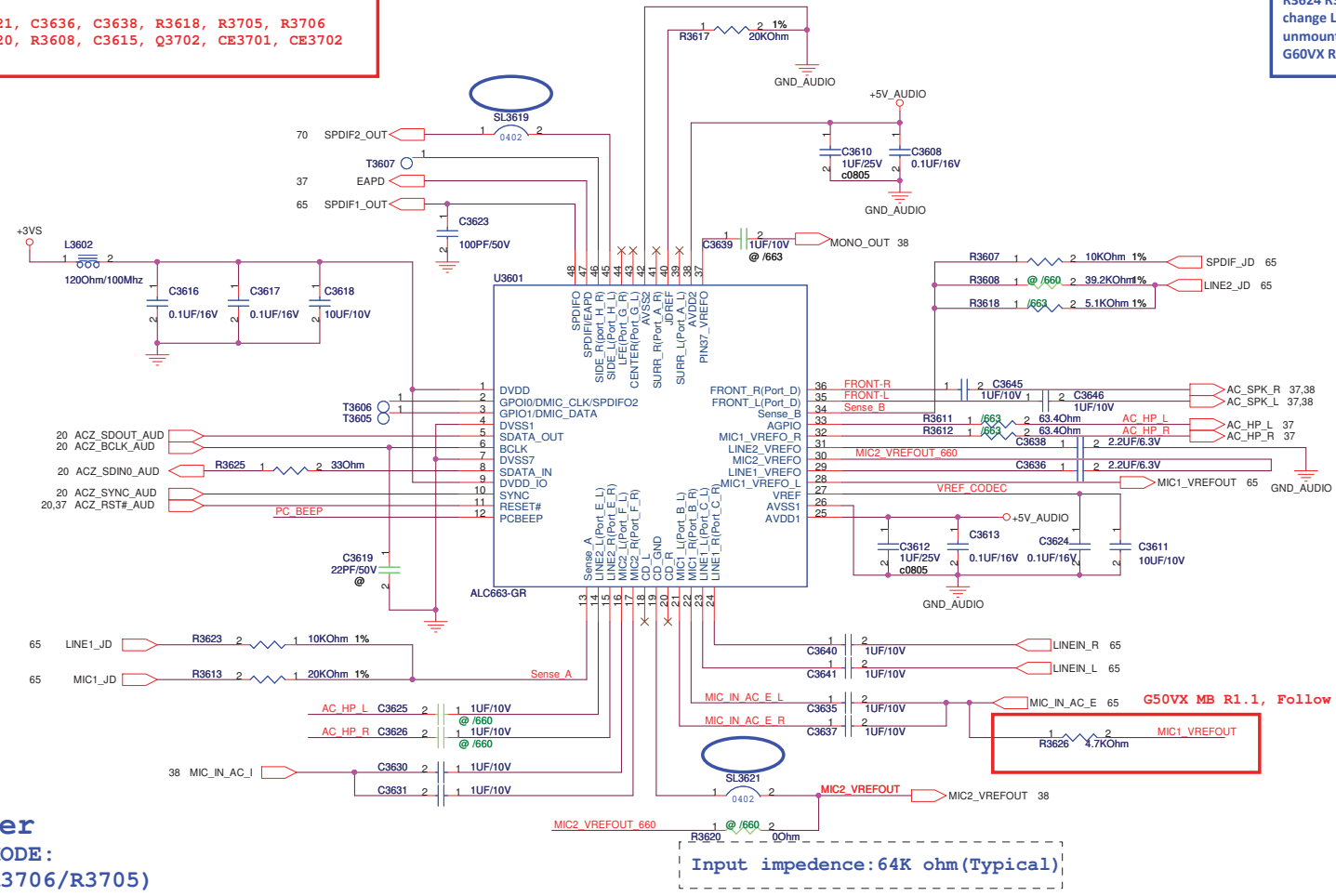
Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
20081107



Unmount
 RX2009, RX2012, RX2014, RX2016
 J3501, R3409, R3410, J3401,
 For Modem Delete
 20081107

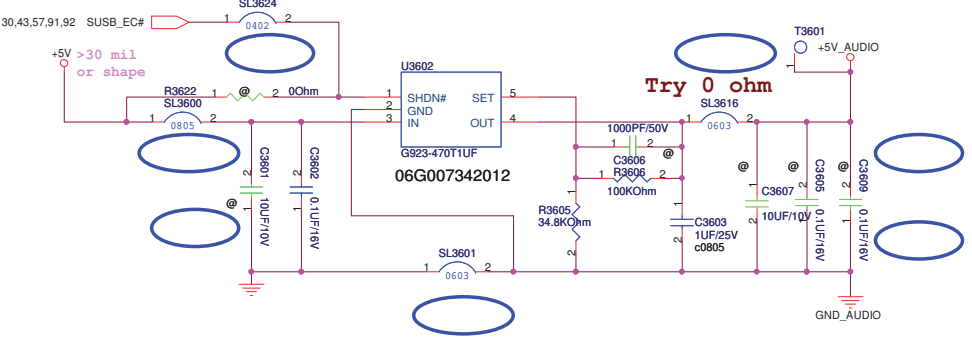
IF ALC662L
 Mount **L** C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702
 Unmount **L** R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
IF ALC663L
 Mount **L** R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
 Unmount **L** C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702

change R3619 R3621 R3602
 R3624 R3601 R3616 to short land;
 change L3601 to short land;
 unmount C3601 C3605 C3609;
 G60VX R2.0 costdown 20090402

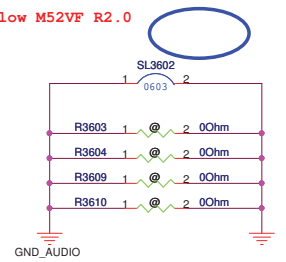


Audio Power
FOR ADJUST MODE:
 $V_o = 1.25 * (1 + R3706/R3705)$
 $= 1.25 * (1 + 100K/34.8K) = 4.84$

Input impedance: 64k ohm (Typical)



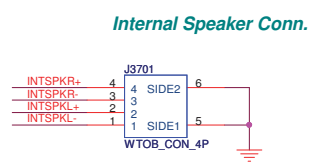
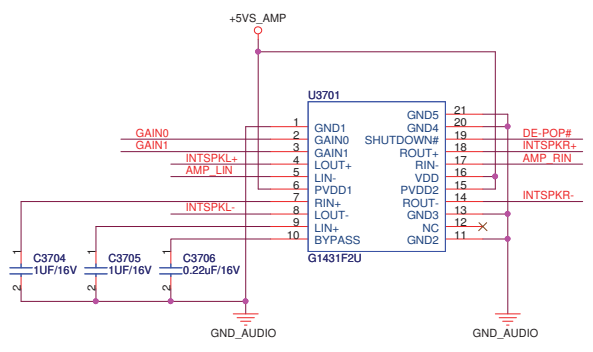
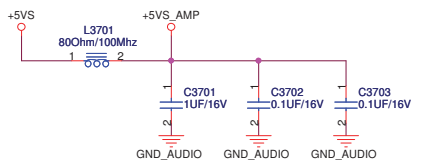
T3602
 SB_SPKR



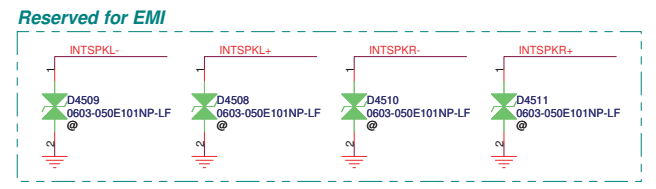
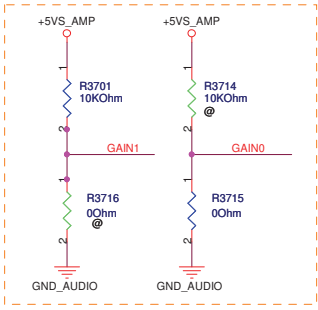
PC BEEP

<http://hobi-elektronika.net>

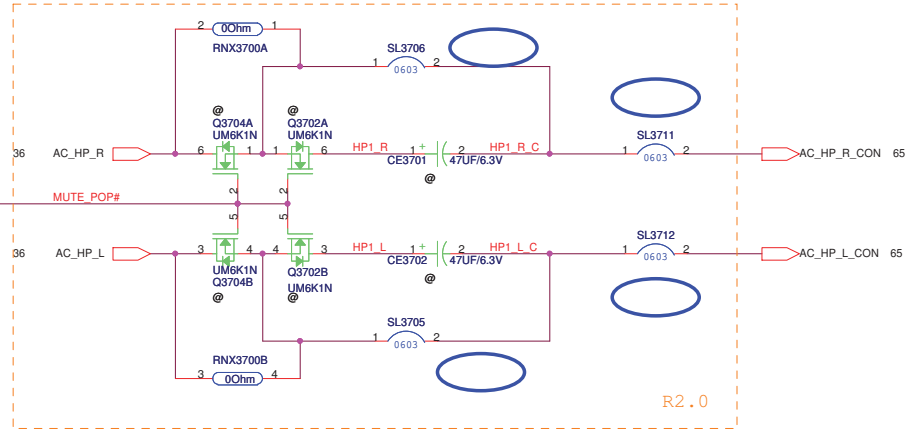
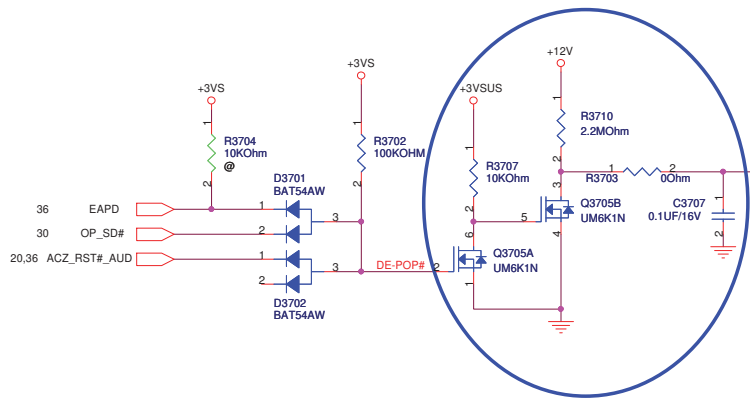
PEGATRON		Title : CODEC-ALC663	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet 36	of 100	



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

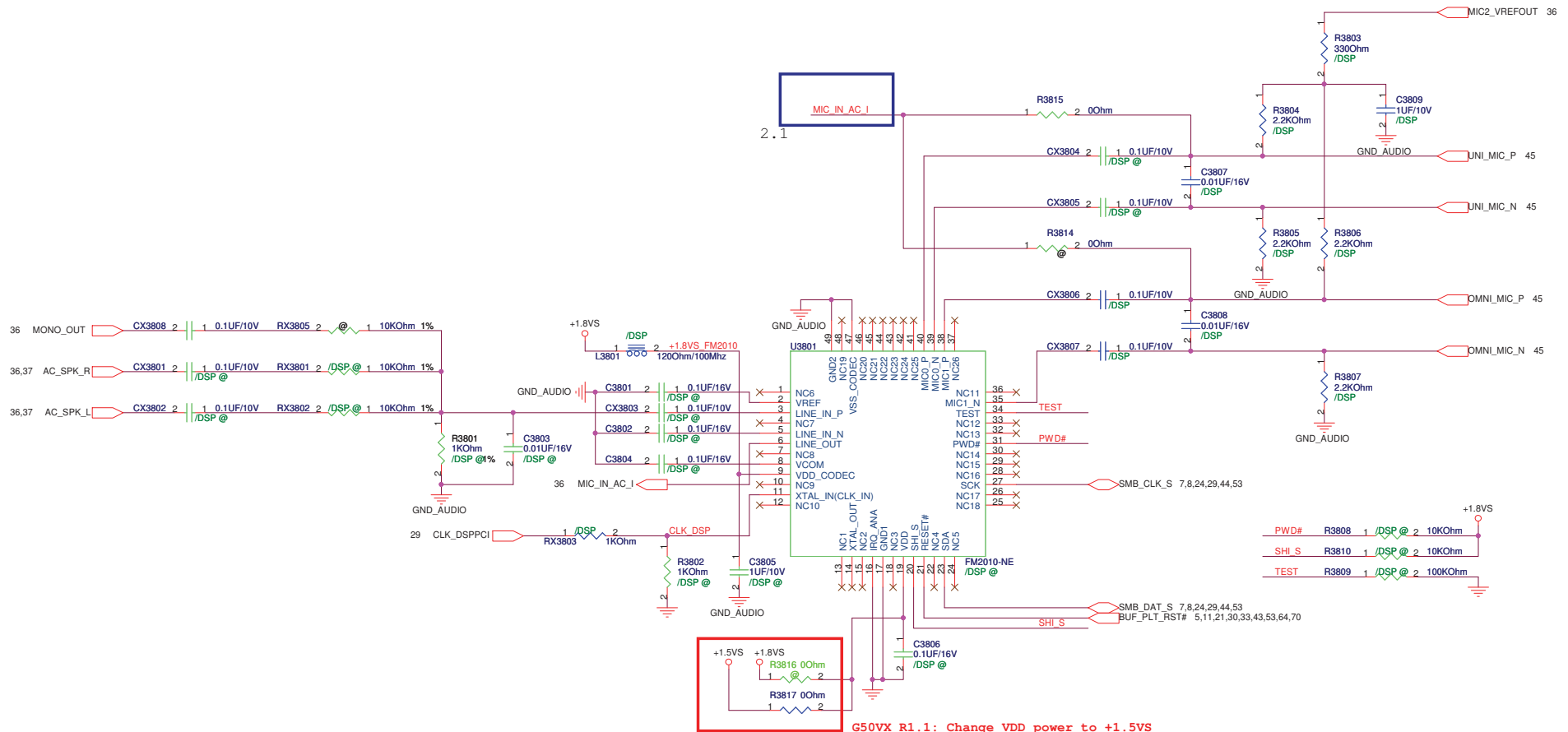


R2.0



unmount R3707 Q3705 R3710 R3703 C3707
change R3706 R3705 R3711 R3712 to short land
add SL3700 SL3701
G60VX R2.0 costdown 20090402

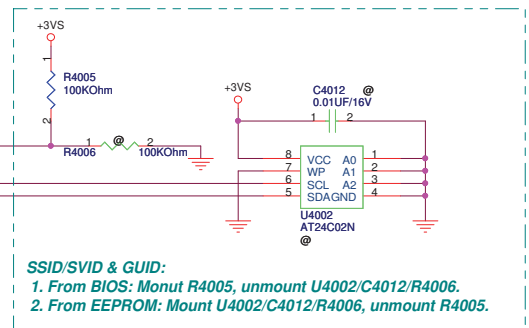
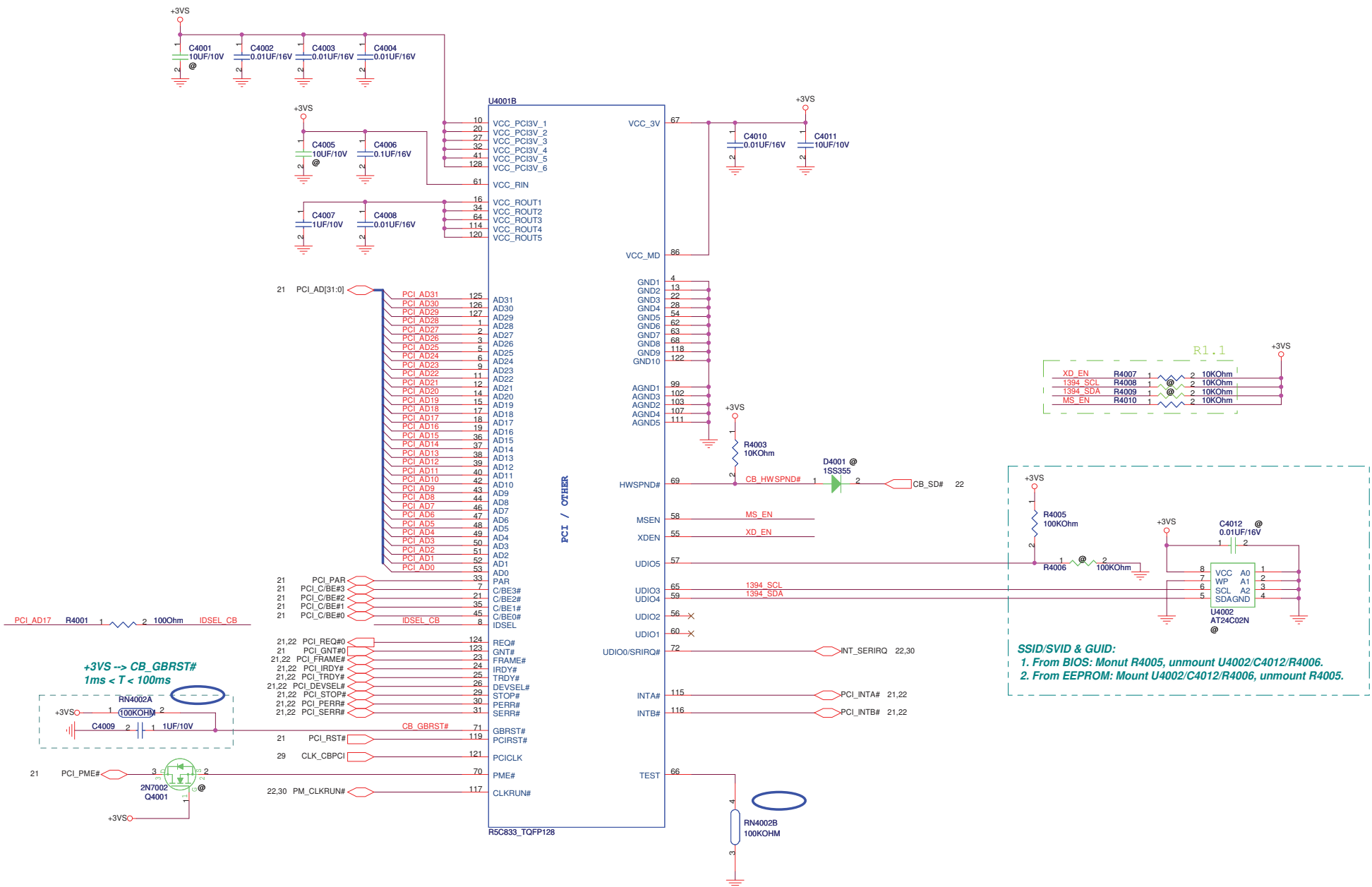
R2.0



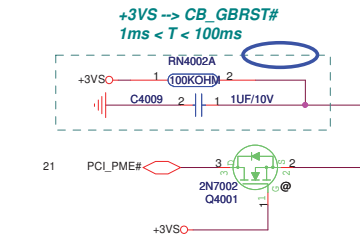
Mount R4507, R508, R4509, R4510
 U3801, R3803, C3809, R3804, CX3804, C3807, CX3805,
 R3805, R3806, CX3806, CX3807, C3808, R3807
 R3808, R3810, R3809, C3806, C3805, R3802, RX3803
 C3804, C3802, CX3803, C3801, L3801, C3803, R3801
 RX3801, RX3802, CX3801, CX3802

Unmount R3815, R3814, CX3808, RX3805
 For supporting Array Mic
 20081107

G50VX R1.1: Change VDD power to +1.5VS
 to decrease the digital noise and for
 less power consumption



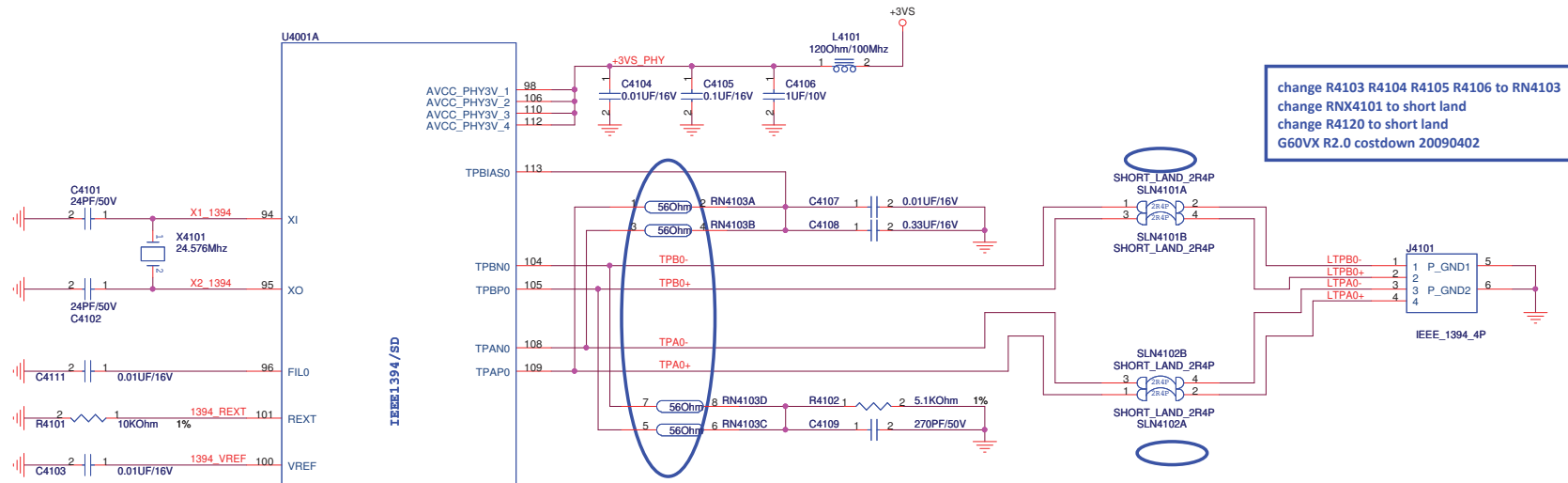
SSD/SVID & GUID:
 1. From BIOS: Mount R4005, unmount U4002/C4012/R4006.
 2. From EEPROM: Mount U4002/C4012/R4006, unmount R4005.



change R4002 R4004 to RN4002
 10G302104004050
 G60VX R2.0 costdown 20090402

<http://hobi-elektronika.net>

PEGATRON		Title : CB_R5C833	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	40	of 100



change R4103 R4104 R4105 R4106 to RN4103
change RNX4101 to short land
change R4120 to short land
G60VX R2.0 costdown 20090402

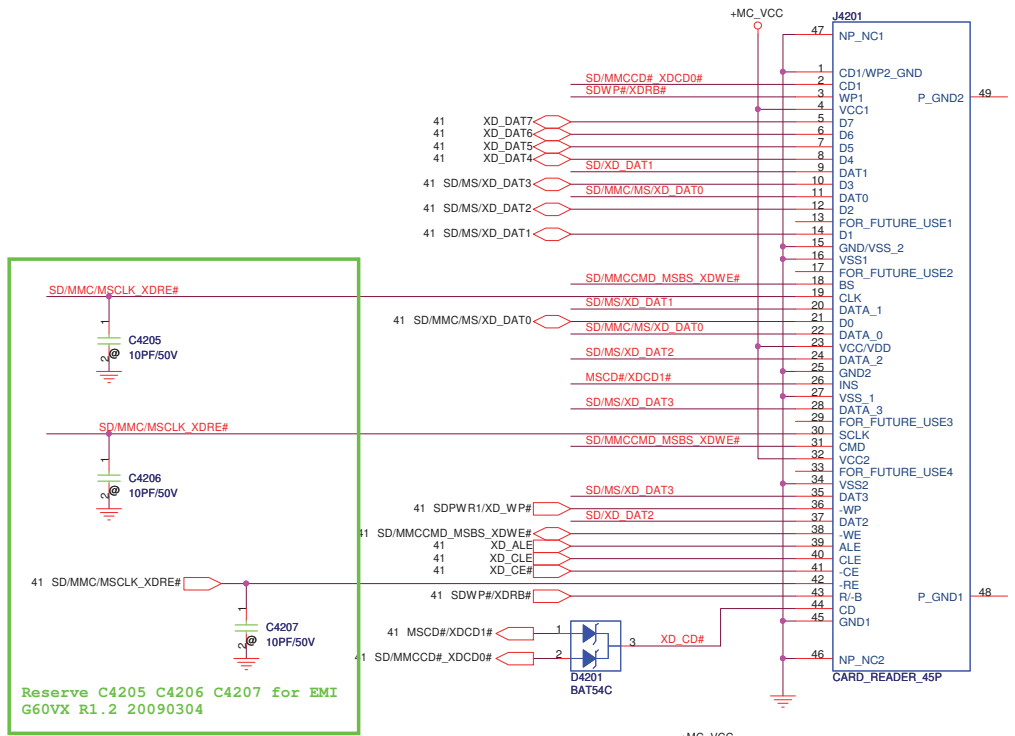
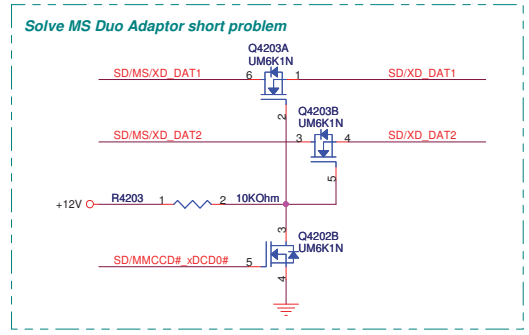
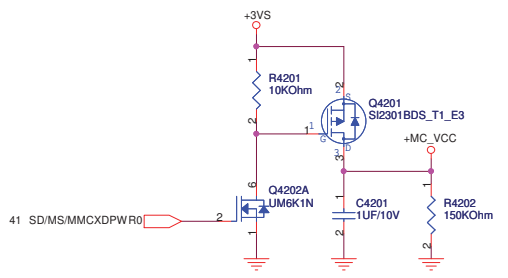
Add R4120 and C4110 for EMI
G60VX R1.2 20090304

Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLEd#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDR#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLE
MDIO19	-	-	-	XDALE

- MDIO17 87 XD_DAT7 42
- MDIO16 92 XD_DAT6 42
- MDIO15 89 XD_DAT5 42
- MDIO14 91 XD_DAT4 42
- MDIO13 90 SD/MS/XD_DAT3 42
- MDIO12 93 SD/MS/XD_DAT2 42
- MDIO11 81 SD/MS/XD_DAT1 42
- MDIO10 82 SD/MMC/MS/XD_DAT0 42
- MDIO05 75 SDPWR1/XD_WP# 42
- MDIO08 88 SD/MMCCMD_MSBS_XDWE# 42
- MDIO19 83 XD_ALE 42
- MDIO18 85 XD_CLE 42
- MDIO02 78 XD_CE# 42
- MDIO03 77 SDWP#/XDRB# 42
- MDIO00 80 SD/MMCCD#_XDCD0# 42
- MDIO01 79 MSCD#/XDCD1# 42
- MDIO09 84 SD/MMC/MCLK_XDRE# 42
- MDIO04 76 SD/MS/MMCXPWR0 42
- MDIO06 74 X
- MDIO07 73

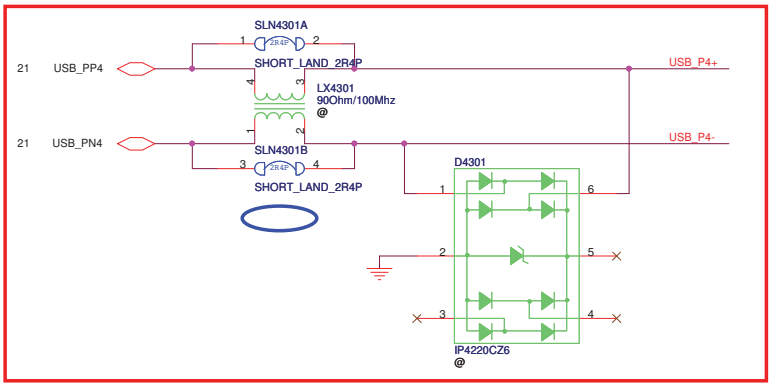
PEGATRON Title : **CB_R5C833**
 Pegatron BU2 HW Team 3 Engineer: **Kevin1_Guo**

Size	Project Name	Rev
Custom	G60VX	R 1.2
Date: Wednesday, April 08, 2009	Sheet 41 of 100	



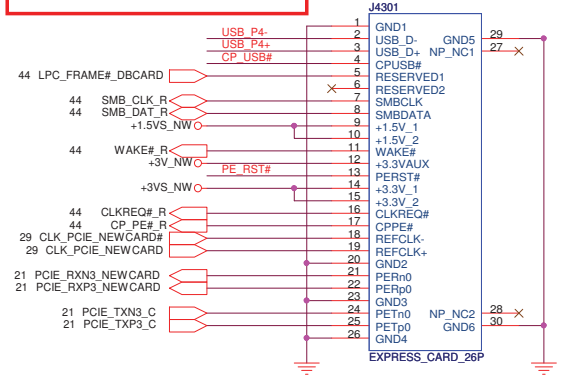
<http://hobi-elektronika.net>

PEGATRON		Title : CB_4in1 CardReader	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	42	of 100

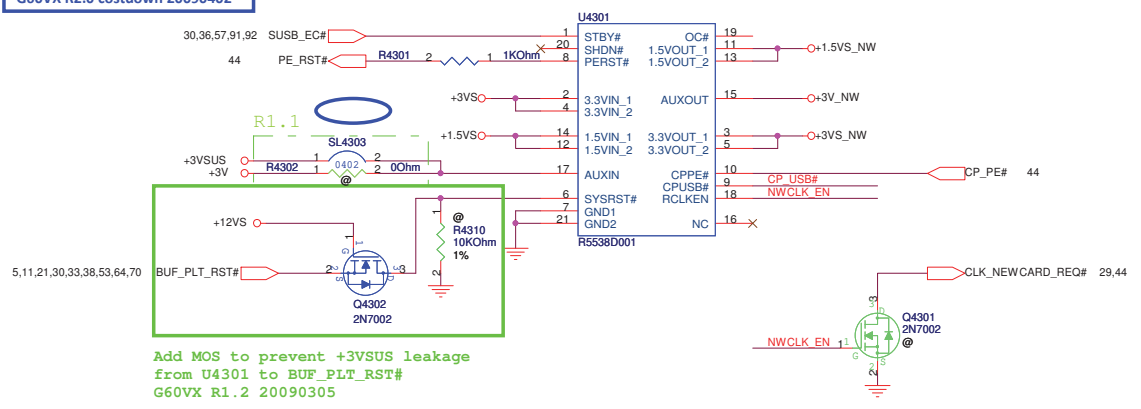


Change Newcard to USB port 4
G50VX R1.1 20090108

NewCard Header

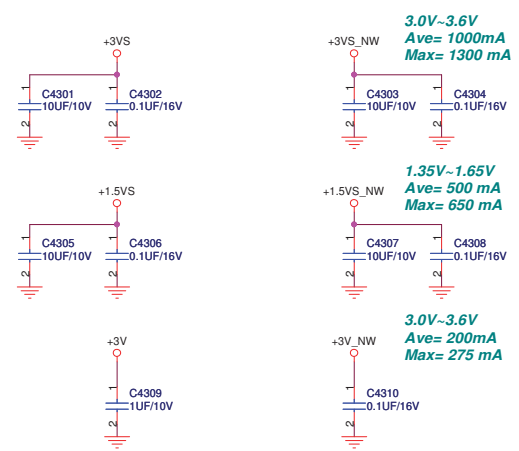
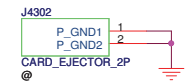


change RNX4301 to short land
chang R4303 to short land
G60VX R2.0 costdown 20090402



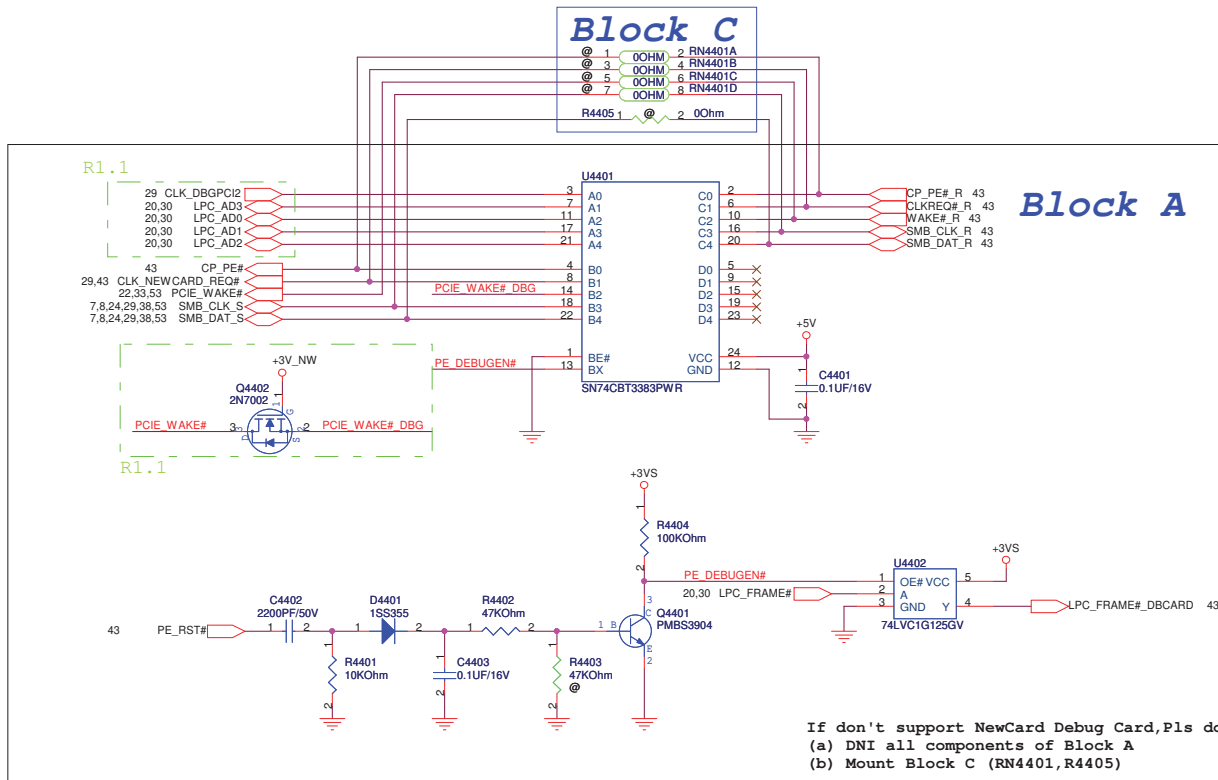
Add MOS to prevent +3VSUS leakage
from U4301 to BUF_PLT_RST#
G60VX R1.2 20090305

NewCard Ejector

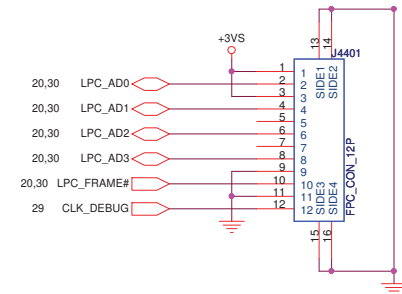


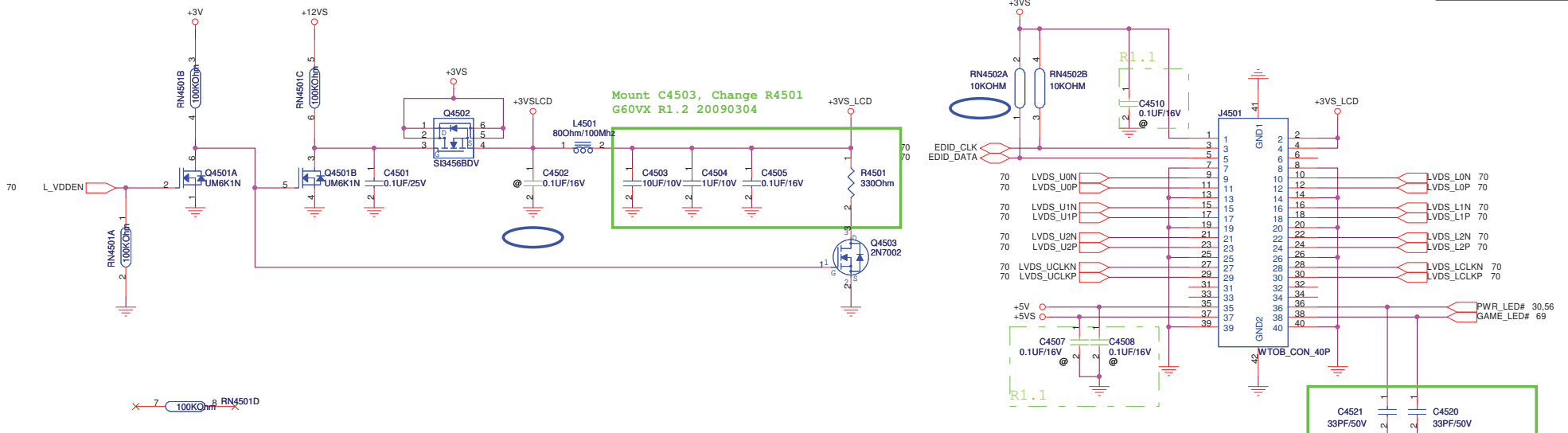
For NewCard Debug Card

LPC Debug Port



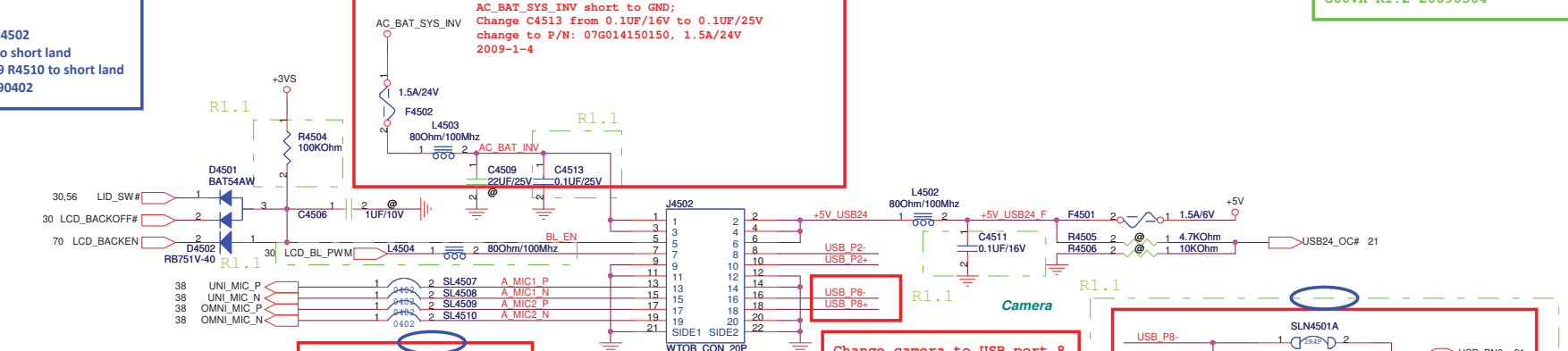
Mount Block A and LPC Debug Port in early stage
200811170917





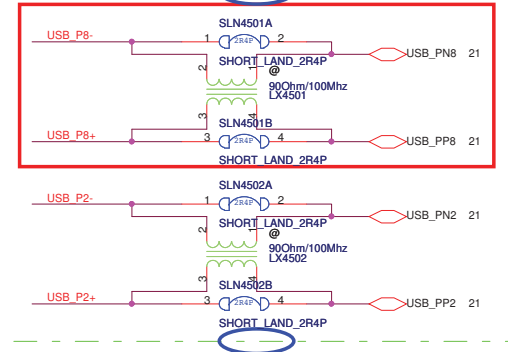
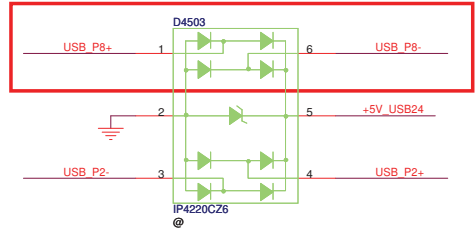
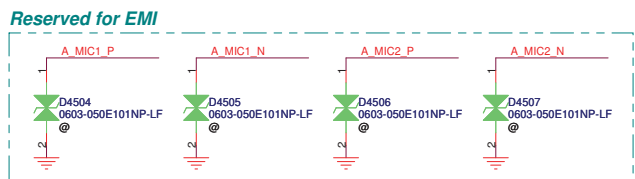
unmount C4502
 change R4502 R4503 to RN4502
 change RNX4501 RNX4502 to short land
 change R4507 R4508 R4509 R4510 to short land
 G60VX R2.0 costdown 20090402

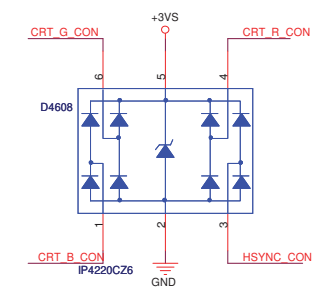
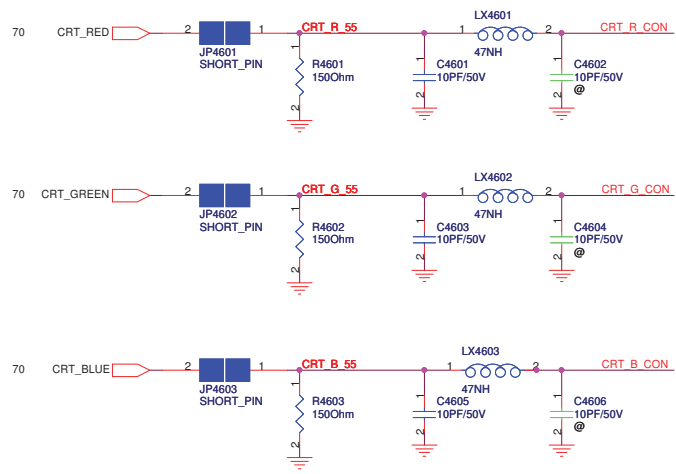
Add F4502 to protect the M/B from damaging by AC_BAT_SYS_INV short to GND;
 Change C4513 from 0.1uF/16V to 0.1uF/25V
 change to P/N: 07G014150150, 1.5A/24V
 2009-1-4



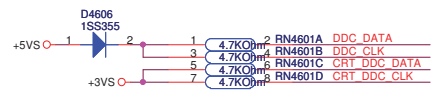
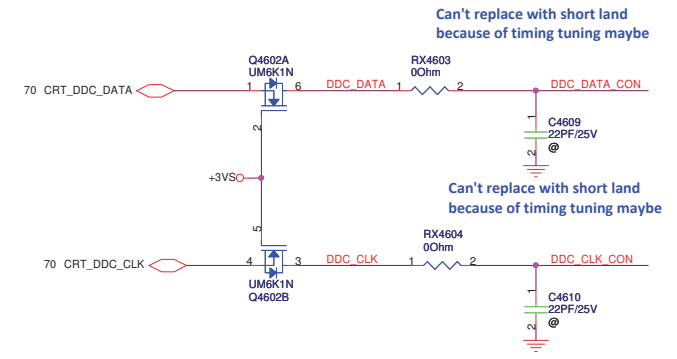
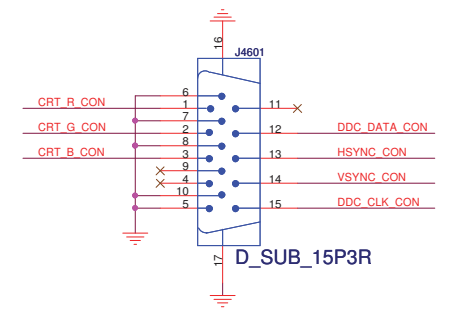
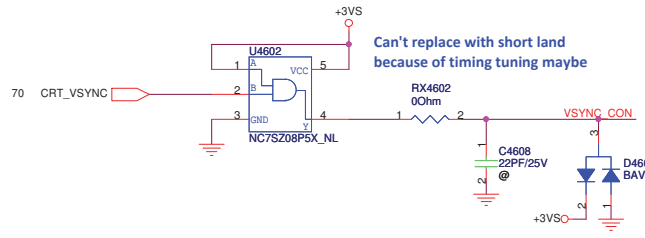
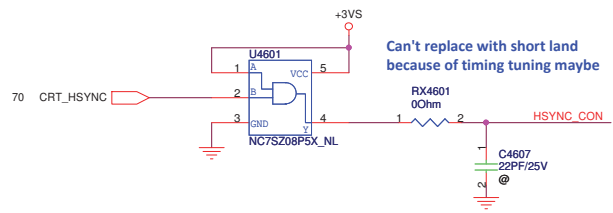
Mount R4507, R508
 R4509, R4510
 For supporting Array Mic
 20081107

Change camera to USB port 8
 G50VX R1.1 20090108



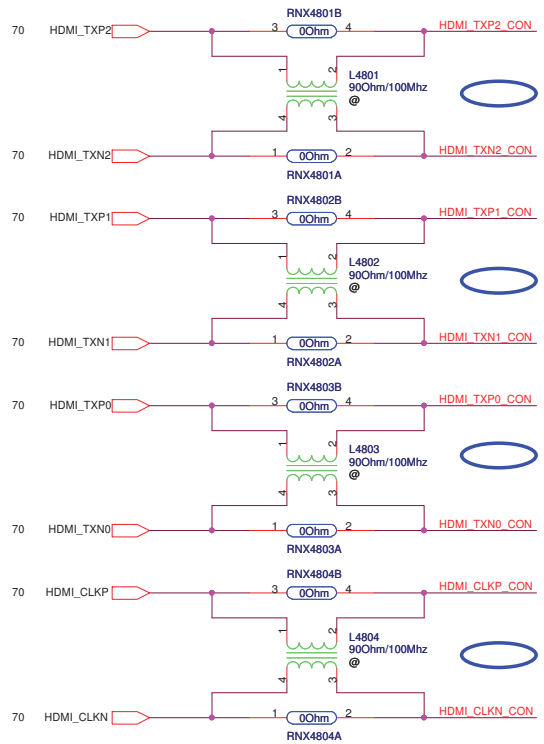


delete RX4605 RX4606 RX4607
 delete D4601 D4602 D4603 D4604
 add D4608
 change RN4601 to 4R8P
 delete RN4602
 G60VX R2.0 costdown 20090402

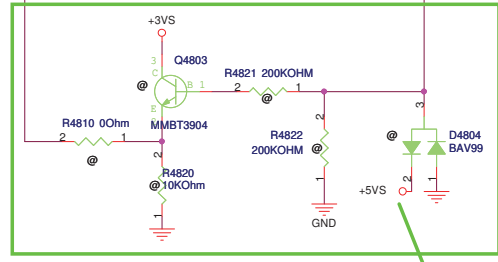
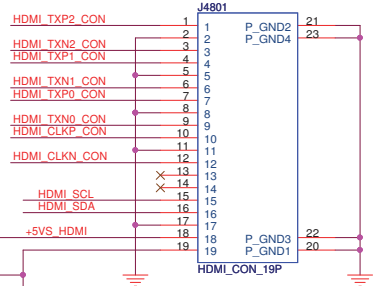
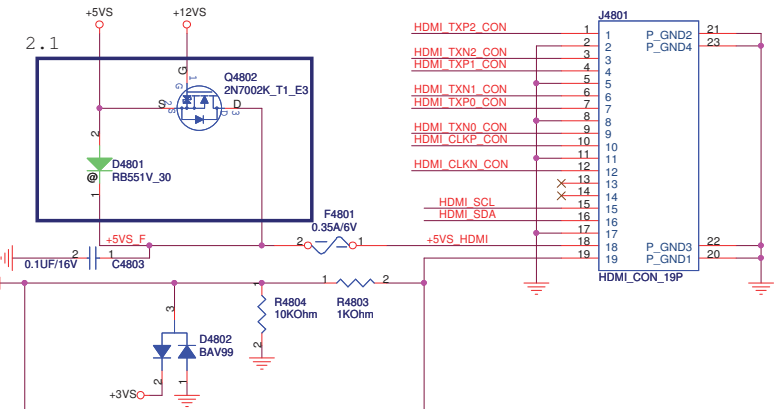


<http://hobi-elektronika.net>

PEGATRON		Title : CRT_D-Sub	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R	1.2
Date: Thursday, April 02, 2009	Sheet	46	of 100

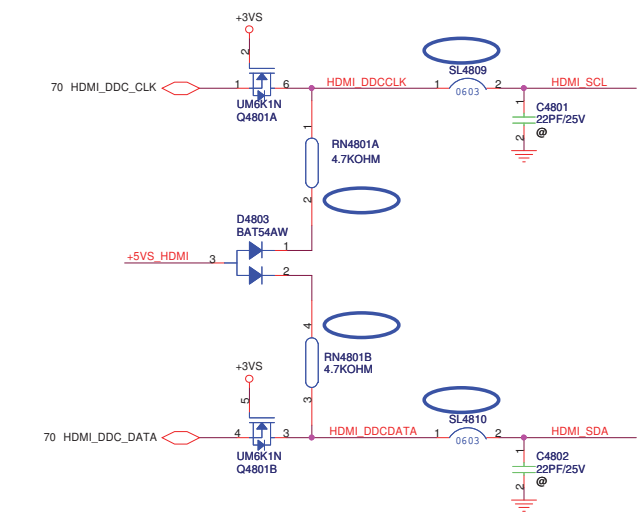


Reserve RNX4801 RNX4802 RNX4803 RNX4804
 delete RX4809 RX4810 / use short land;
 delete R4801 R4802 / add RN4801
 G60VX R2.0 costdown 20090402



Reserve schematic to prevent the
 3.6-3.7V voltage to damage the GPU
 NO STUFF! G60VX R1.2 20090304

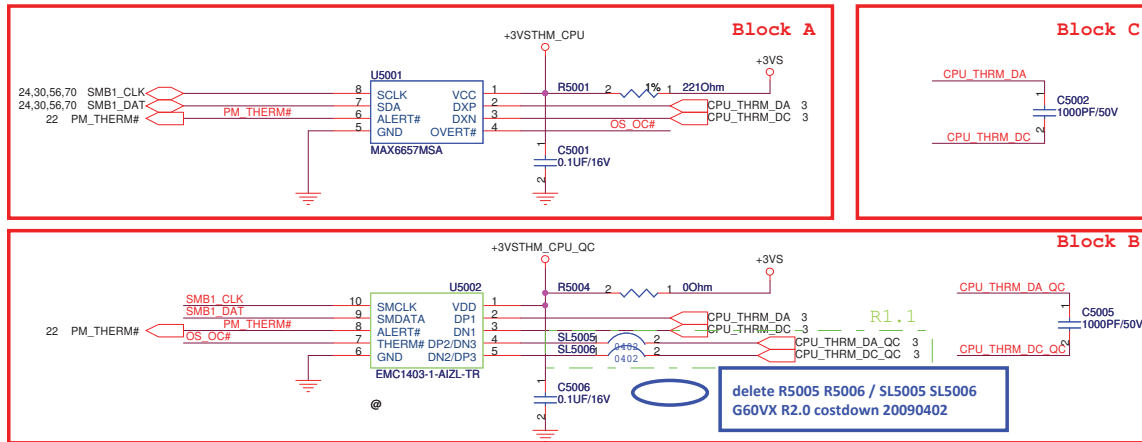
Change +5VS from +3VS
 G60VX R1.2 20090306



PEGATRON		Title : TV_HDMI	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX		Rev R 1.2
Date: Wednesday, April 08, 2009	Sheet	48	of 100

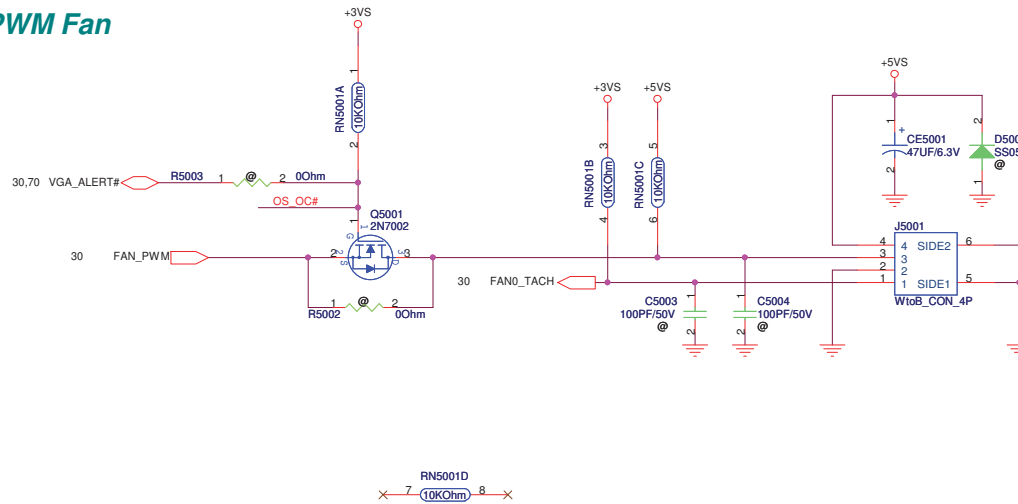
CPU Thermal Sensor

If support DC, Mount Block A and C, Unmount Block B;
 If support QC, Mount Block B and C, Unmount Block A
 200811121042



G50V and M52VF Mount R5004, R5005, R5006
 C5005, C5006 although only support DC,
 They can be cost down if only support DC

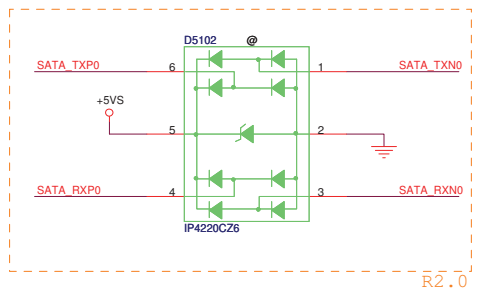
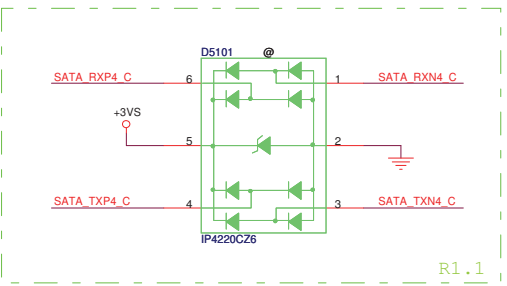
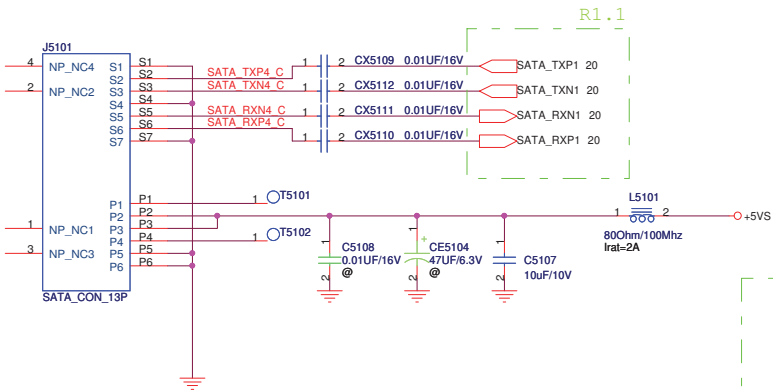
PWM Fan



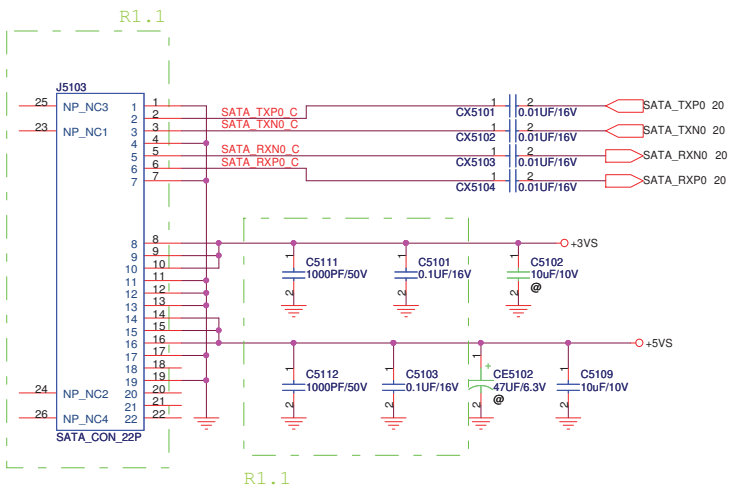
<http://hobi-elektronika.net>

PEGATRON		Title : FAN_Fan & Sensor	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	50	of 100

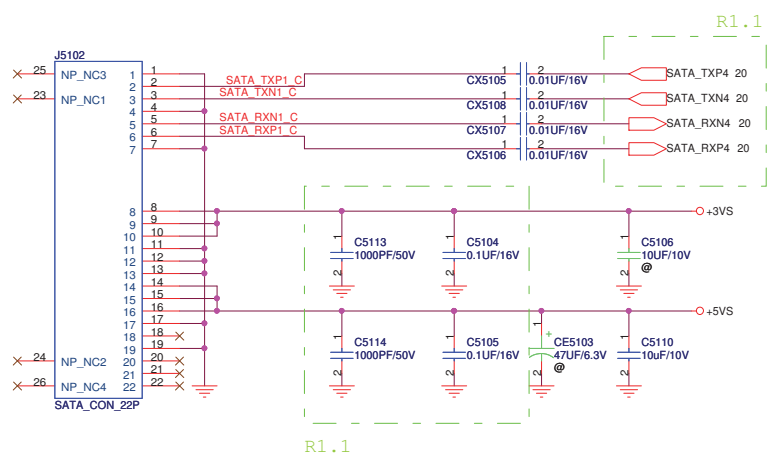
ODD



HDD



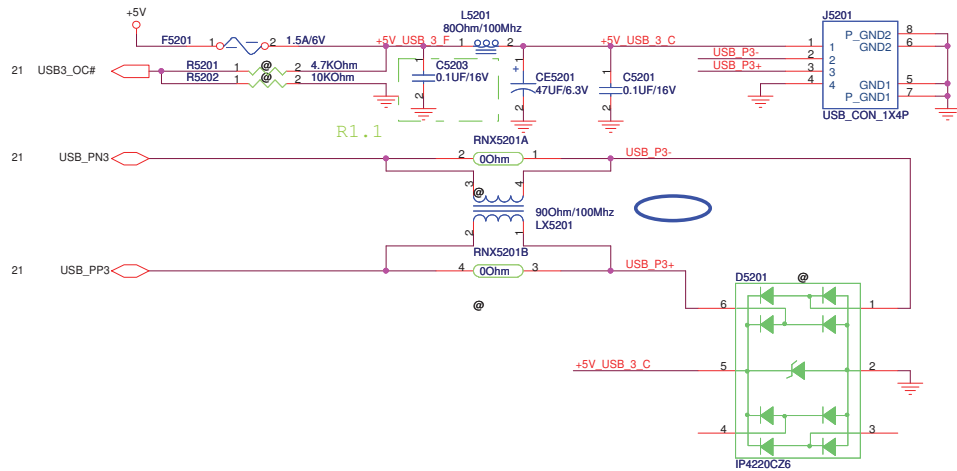
mount CE5102 C5103, unmount C5111
C5101 C5112 C5109
G60VX R2.0 costdown 20090402



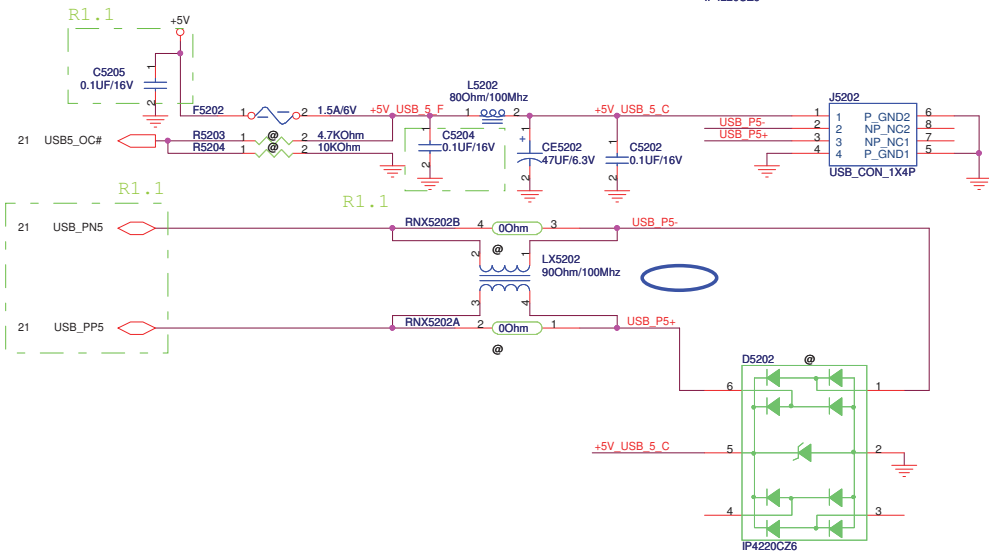
mount CE5103 C5105, unmount C5113
C5104 C5114 C5110
G60VX R2.0 costdown 20090402

<http://hobi-elektronika.net>

PEGATRON		Title : XDD_HDD & ODD	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R	1.2
Date: Wednesday, April 08, 2009	Sheet	51	of 100



need Verification !
G60VX R2.0 costdown 20090402

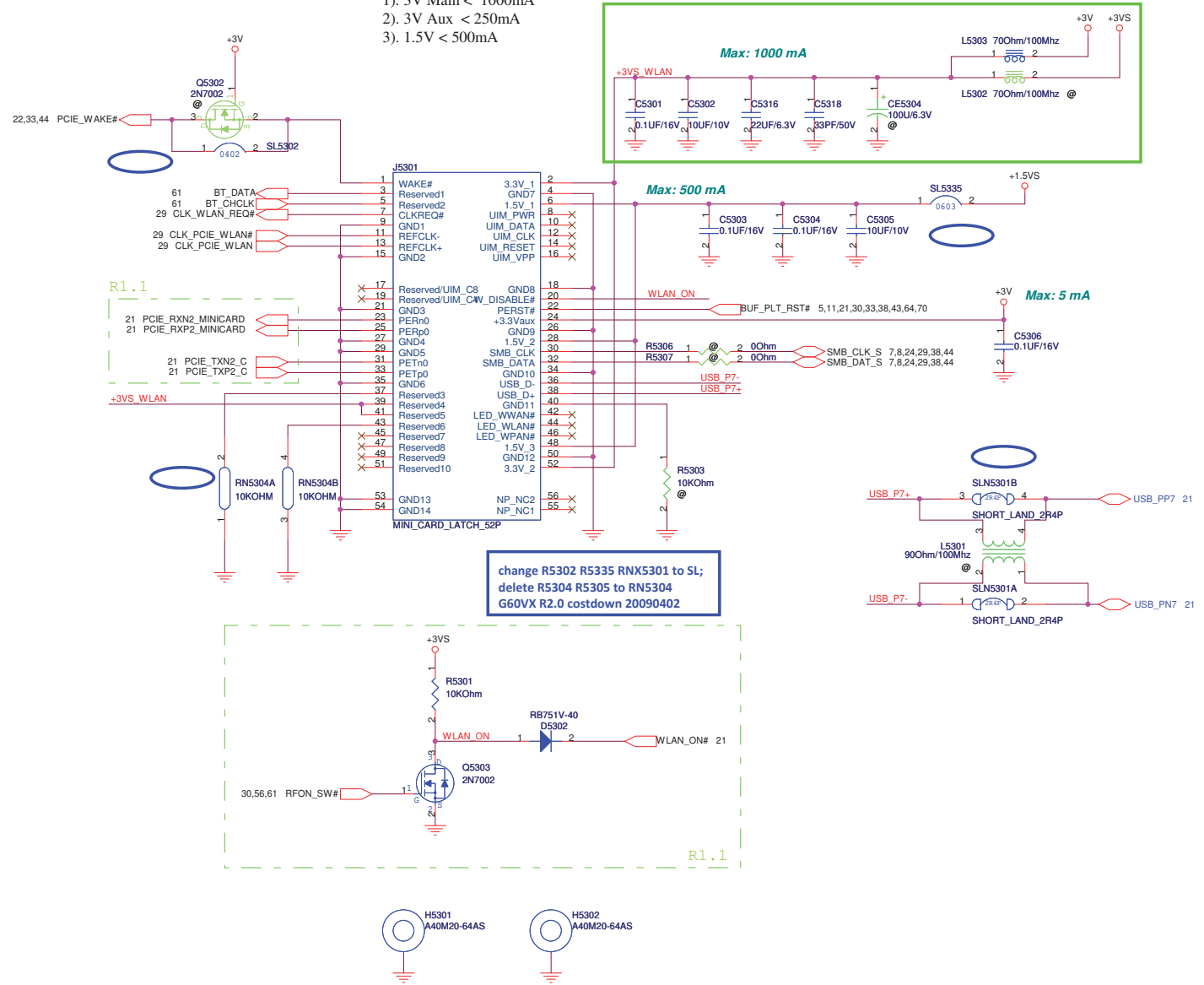


<http://hobi-elektronika.net>

PEGATRON		Title : USB_USB Port *2	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Wednesday, April 08, 2009		Sheet	52 of 100

Follow H15HV R2.1 to accommodate large current for Intel WiFi link 5300/5100 WLAN card
G60VX R1.2 20090305

- POWER CONSUMPTION:
- 1). 3V Main < 1000mA
 - 2). 3V Aux < 250mA
 - 3). 1.5V < 500mA

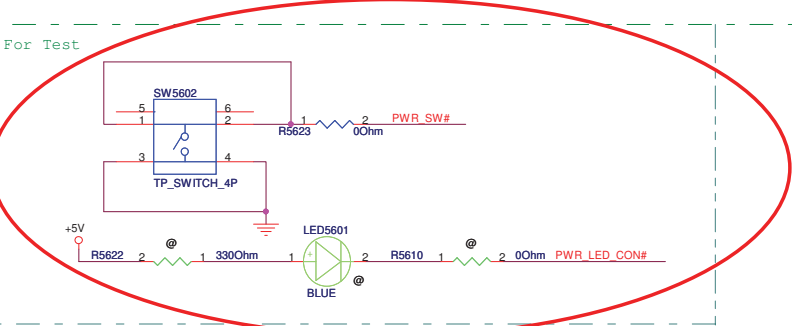
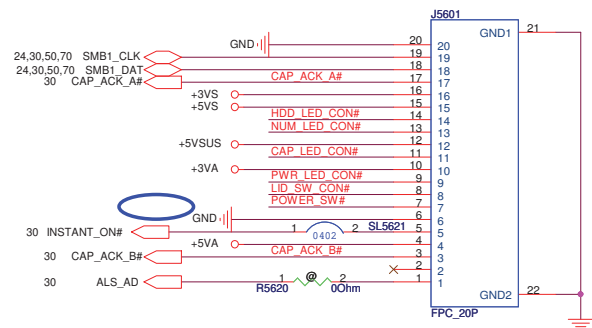
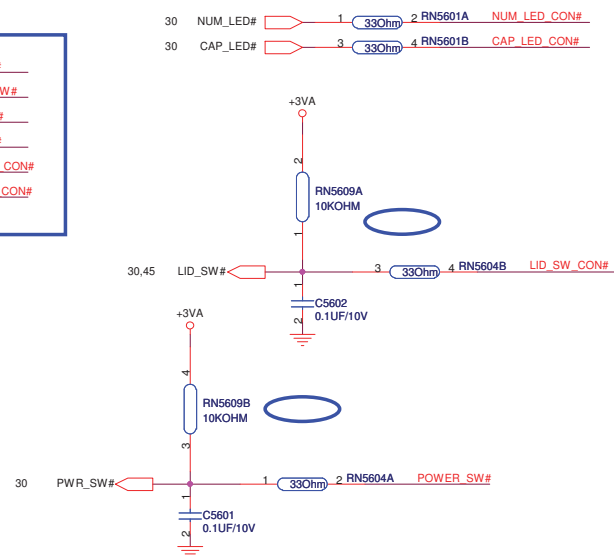


change R5302 R5335 RNX5301 to SL;
delete R5304 R5305 to RN5304
G60VX R2.0 costdown 20090402

<http://hobi-elektronika.net>

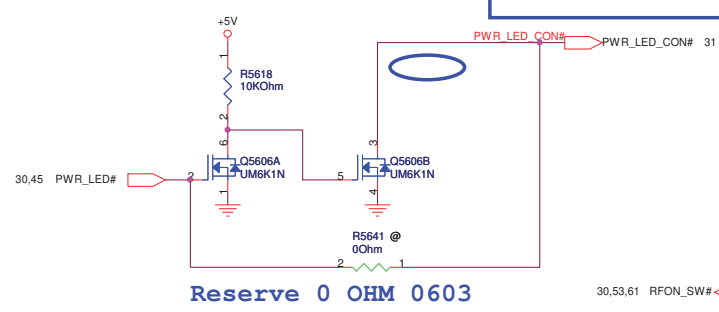
PEGATRON		Title : PCI WLAN	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX	Date: Wednesday, April 08, 2009	Rev R 1.2
		Sheet 53	of 100

- T5601 ○ 1 PWR_SW#
- T5602 ○ 1 POWER_SW#
- T5603 ○ 1 PWR_LED#
- T5604 ○ 1 CHG_LED#
- T5605 ○ 1 PWR_LED_CON#
- T5606 ○ 1 CHG_LED_CON#

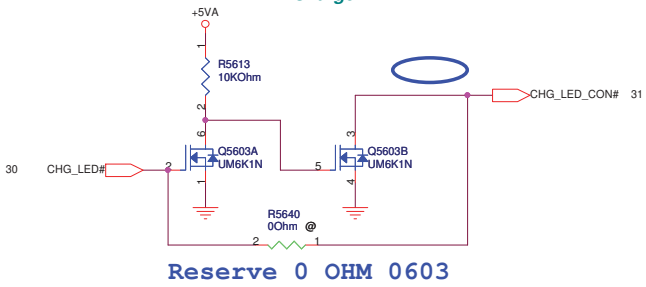


delete R5609 R5607, add RN5609
 delete R5621
 delete R5619
 delete R5614
 delete R5617 R5616
 G60VX R2.0 costdown 20090402

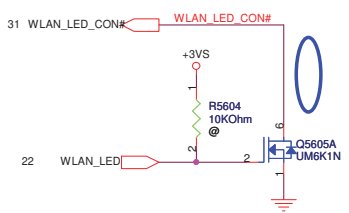
Power LED



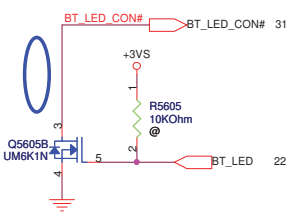
Charger LED



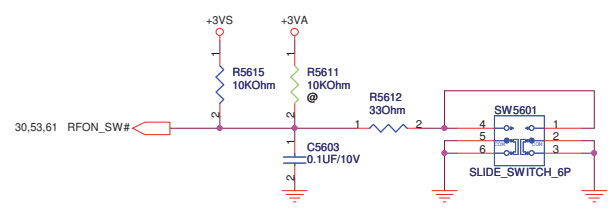
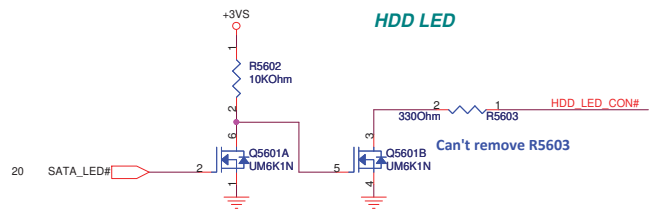
WLAN LED



BT LED



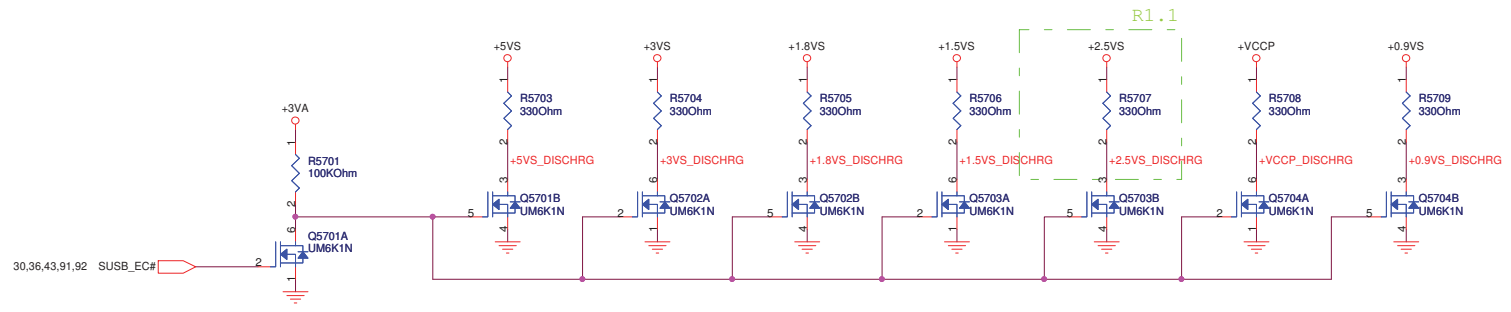
HDD LED



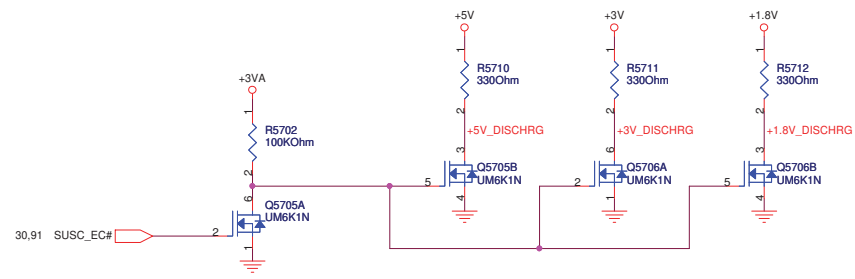
U80V doesn't costdown this MOS

<http://hobi-elektronika.net>

PEGATRON		Title : LED Indicator	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet 56 of 100		



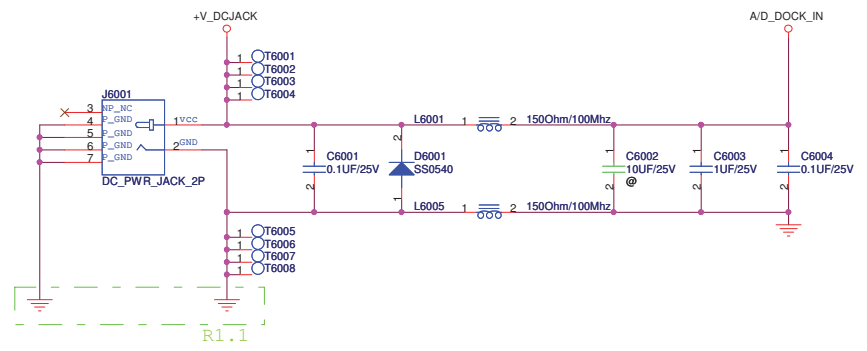
Need to verification!
G60VX R2.0 costdown 20090402



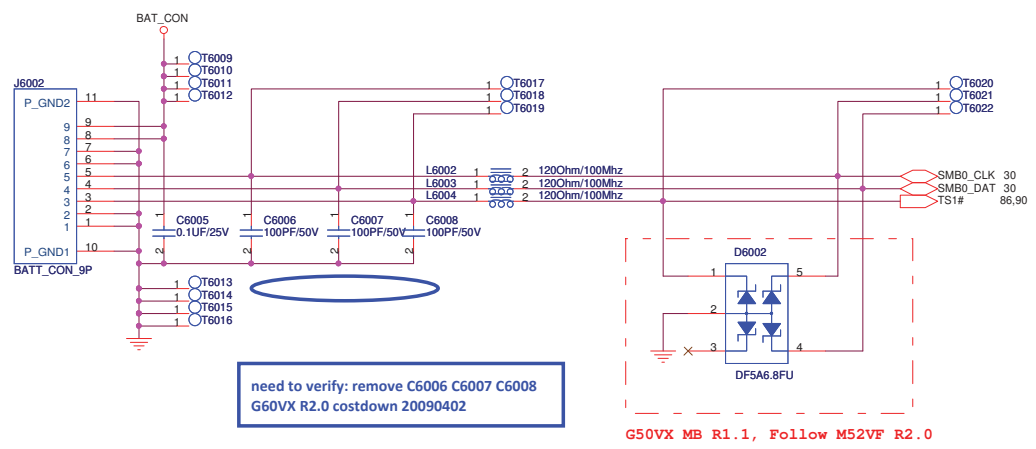
<http://hobi-elektronika.net>

PEGATRON		Title : DSG_Discharge	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX		Rev R 1.2
Date: Wednesday, April 08, 2009		Sheet	57 of 100

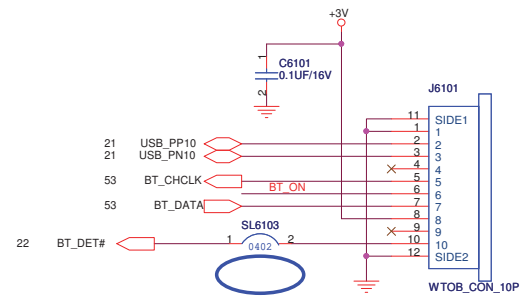
DC Jack



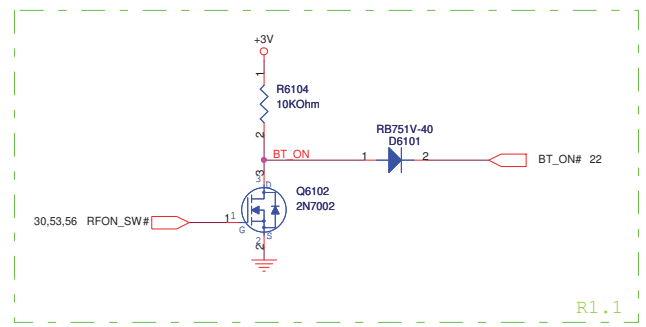
Battery Connector



PEGATRON		Title : DC_DC & BAT Conn	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Sunday, April 05, 2009	Sheet	60	of 100

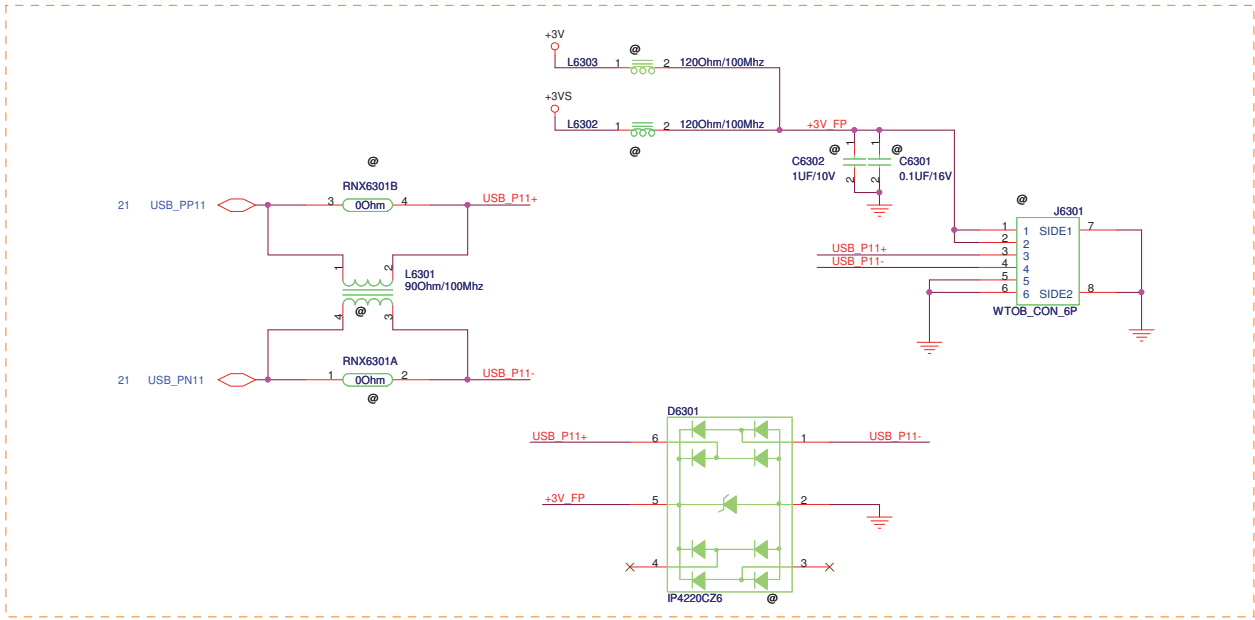


delete R6103
G60VX R2.0 costdown 20090402



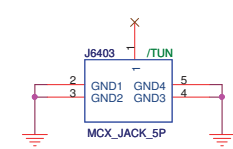
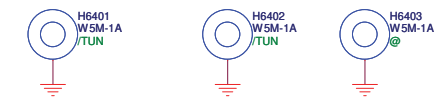
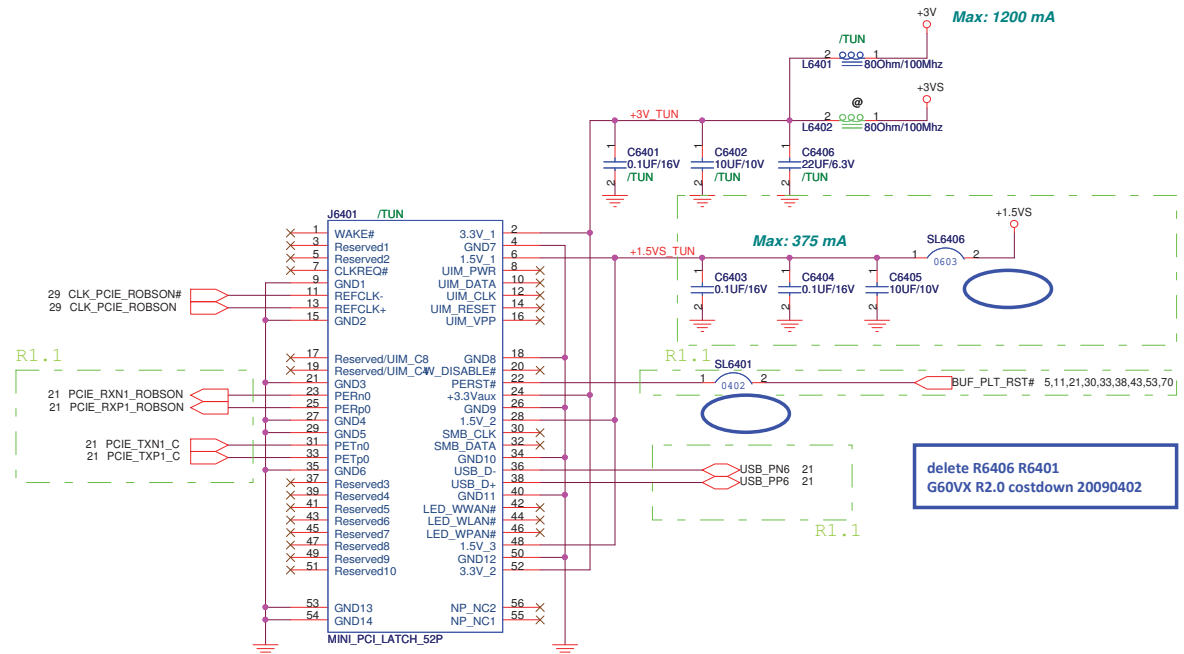
R1.1

PEGATRON		Title : BT Bluetooth	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX		Rev R 1.2
Date: Wednesday, April 08, 2009		Sheet 61 of 100	

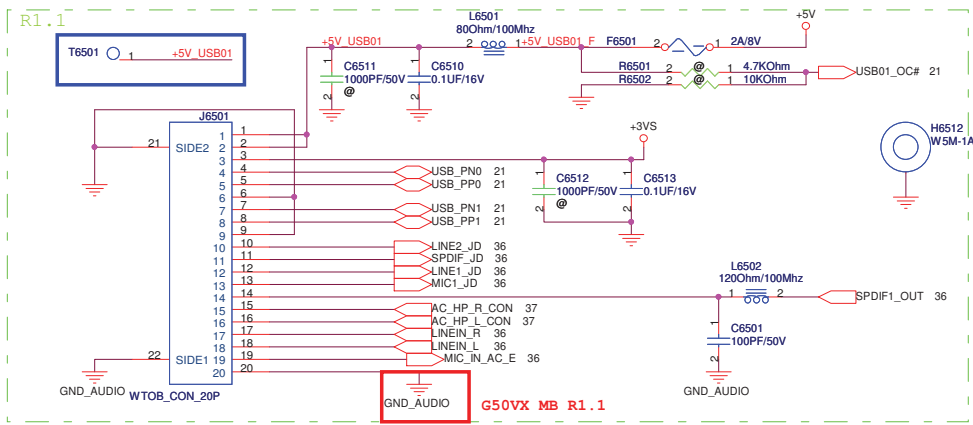


R2.0

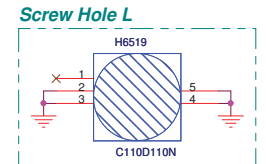
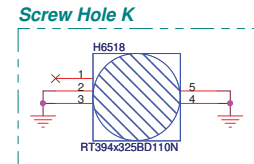
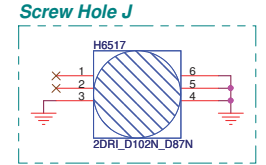
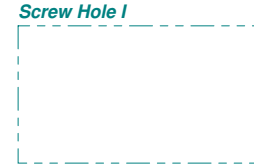
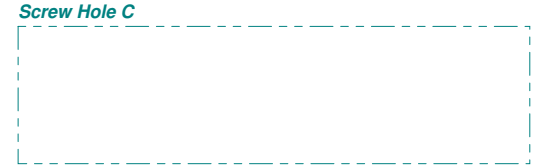
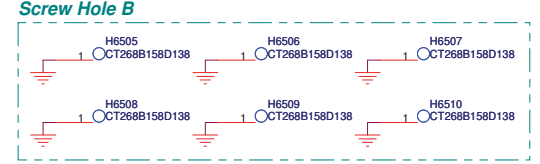
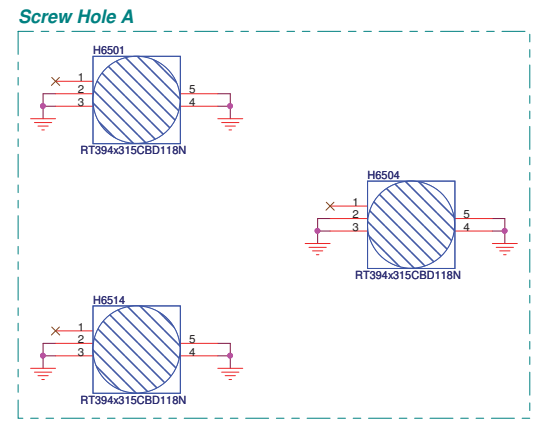
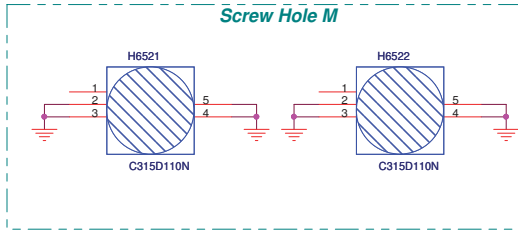
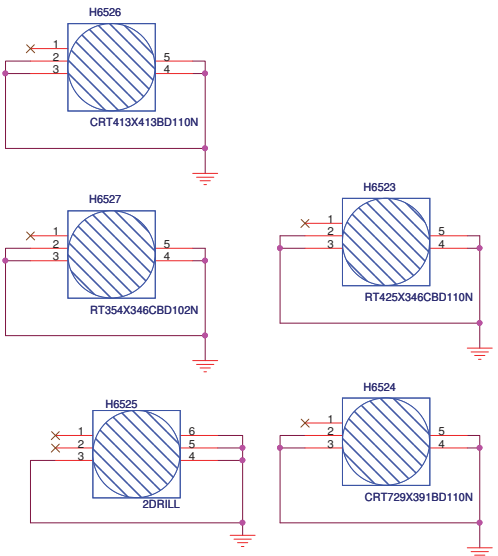
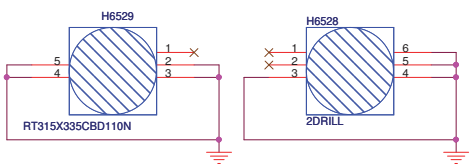
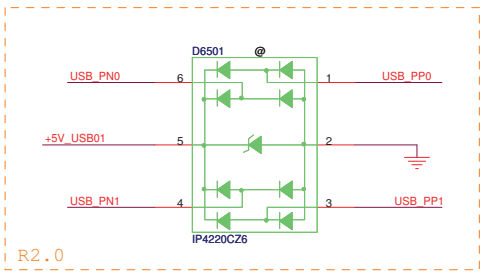
Unmount J6301, C6301, C6302, L6302
 RNX6301 for delete FP connector
 L6303, L6301, D6301 is reserved
 200811102025

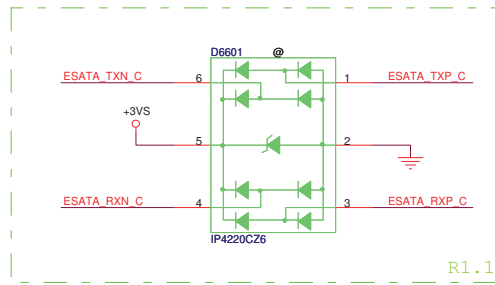
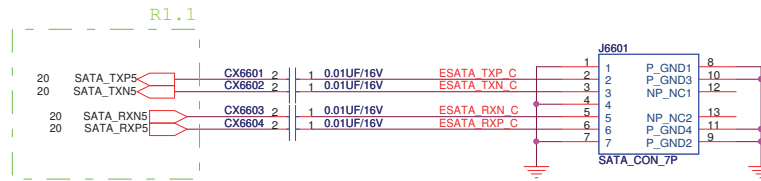


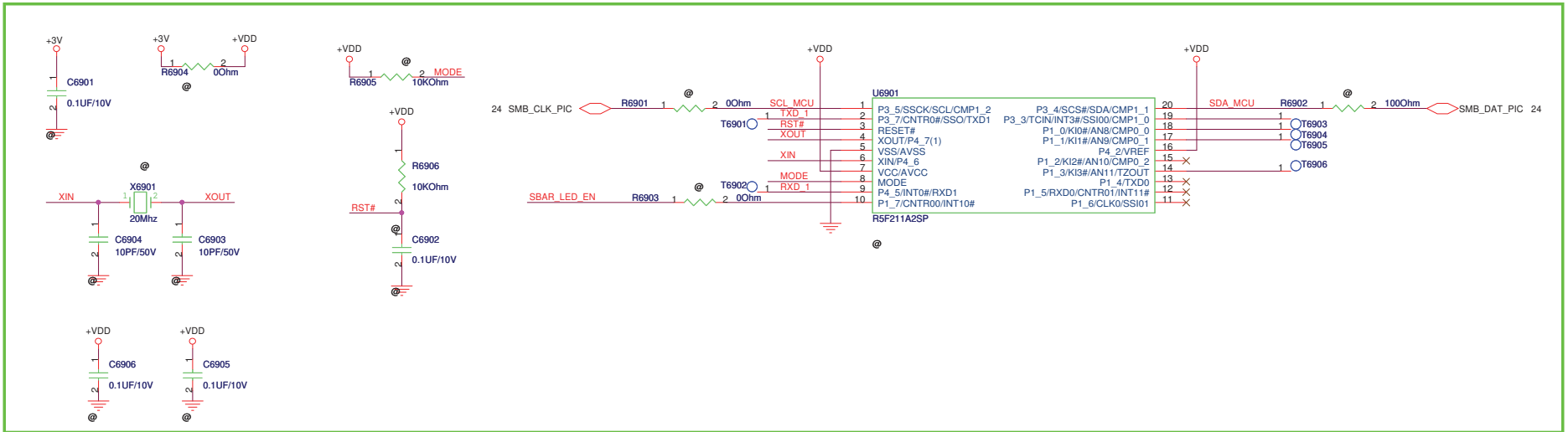
delete R6406 R6401
G60VX R2.0 costdown 20090402



LINE2_JD	C6502	1	2	100PF/50V
LINE1_JD	C6503	1	2	100PF/50V
LINEIN_R	C6504	1	2	100PF/50V
LINEIN_L	C6505	1	2	100PF/50V
MIC_IN_AC_E	C6506	1	2	100PF/50V
MIC1_JD	C6507	1	2	100PF/50V
AC_HP_L_CON	C6508	1	2	100PF/50V
AC_HP_R_CON	C6509	1	2	100PF/50V

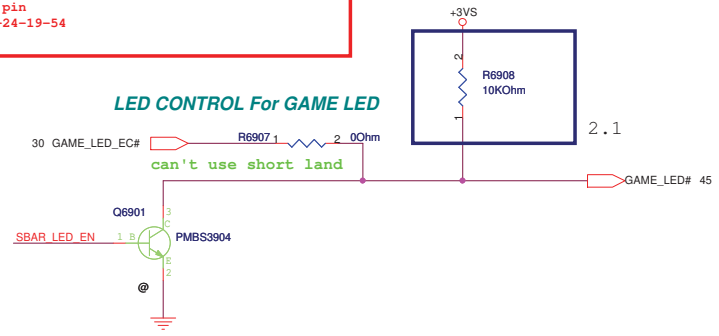


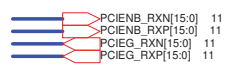




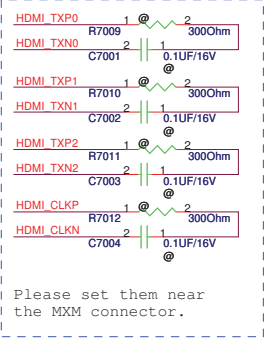
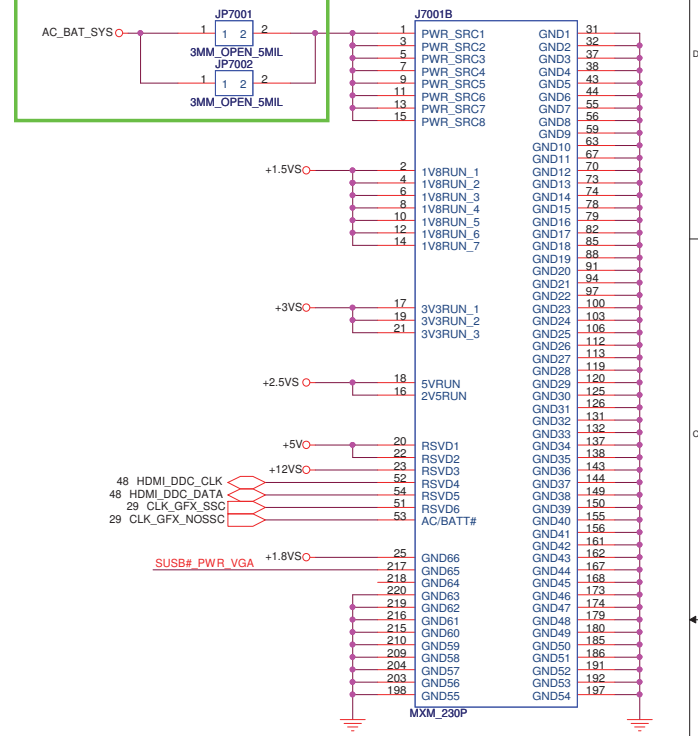
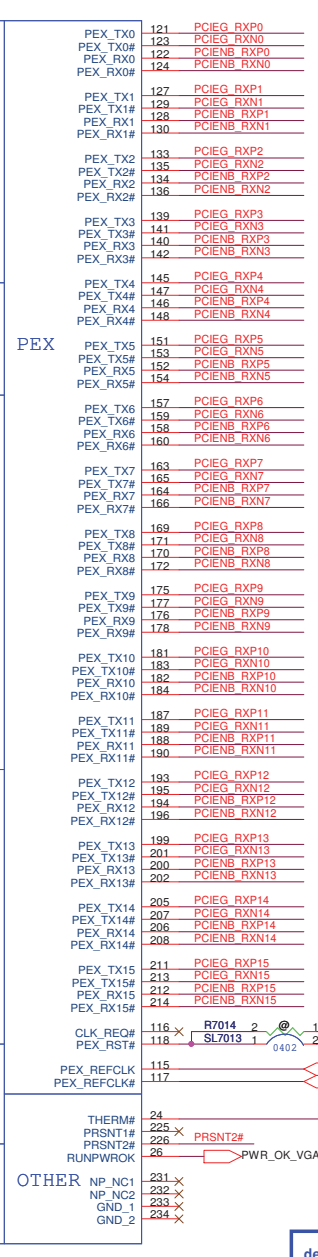
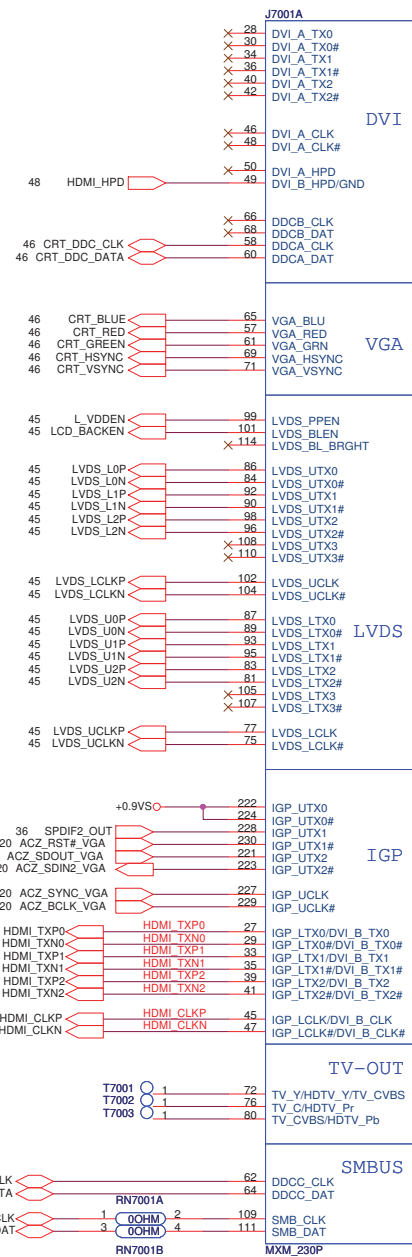
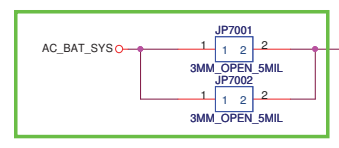
Cause EC will control GAME_LED#
Mount R6907 R6908, unmount
all others and Q2402 RN2402
G60VX R1.2 20090305

G50VX V1.0, Change net GAME_LED_EC# from
connecting with EC.GPA3 pin to connecting with
EC.GPA6 pin
2008-11-24-19-54

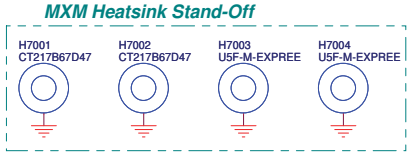




delete co-lay, reserved bead for EMI, G60VX R2.0 20090408

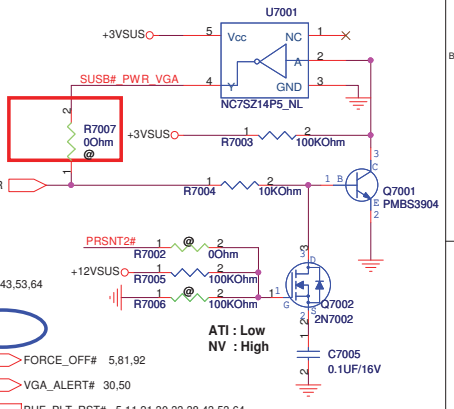


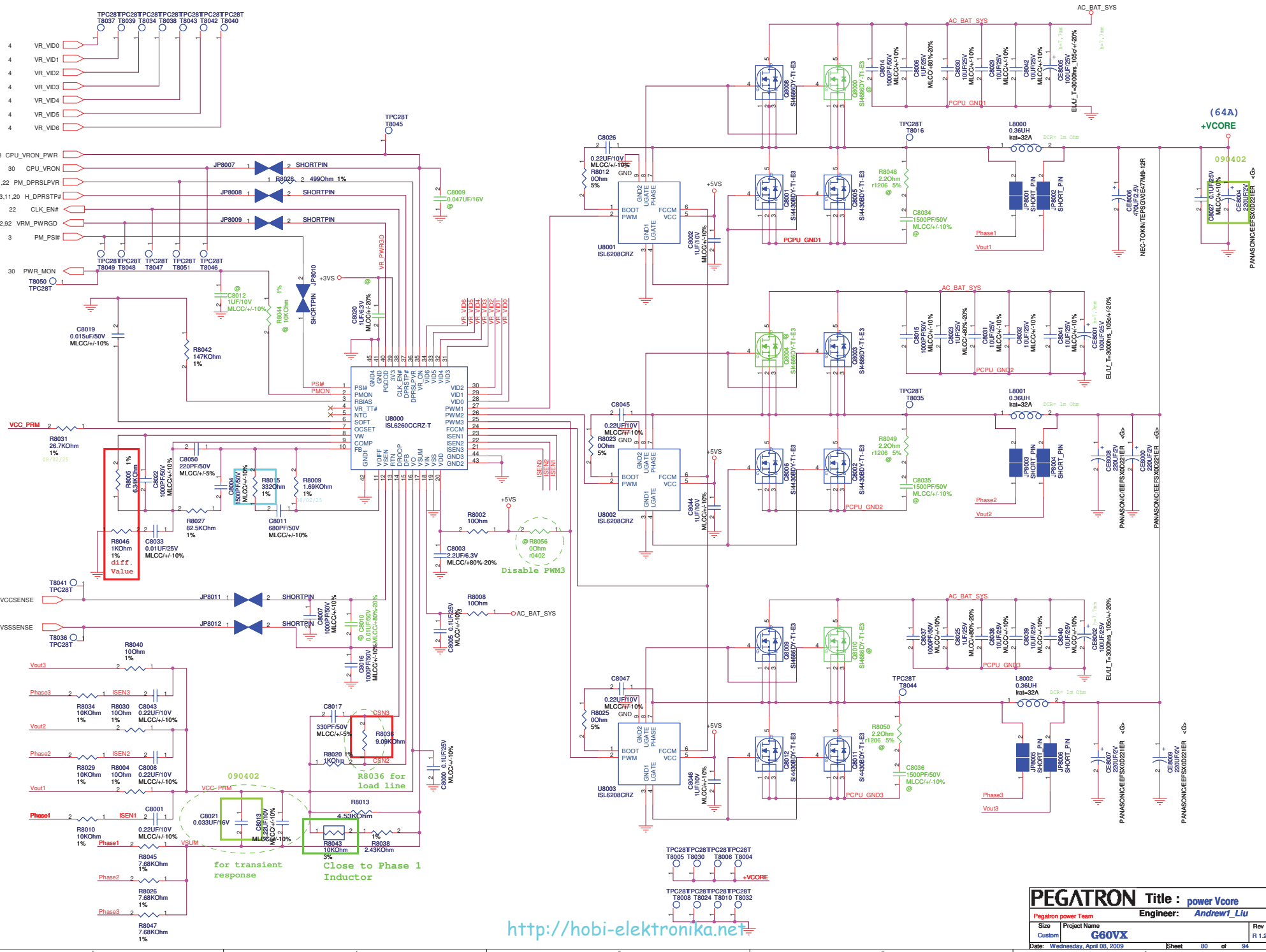
Please set them near the MXM connector.



no change

delete R7001 R7013 G60VX R2.0 costdown 20090402

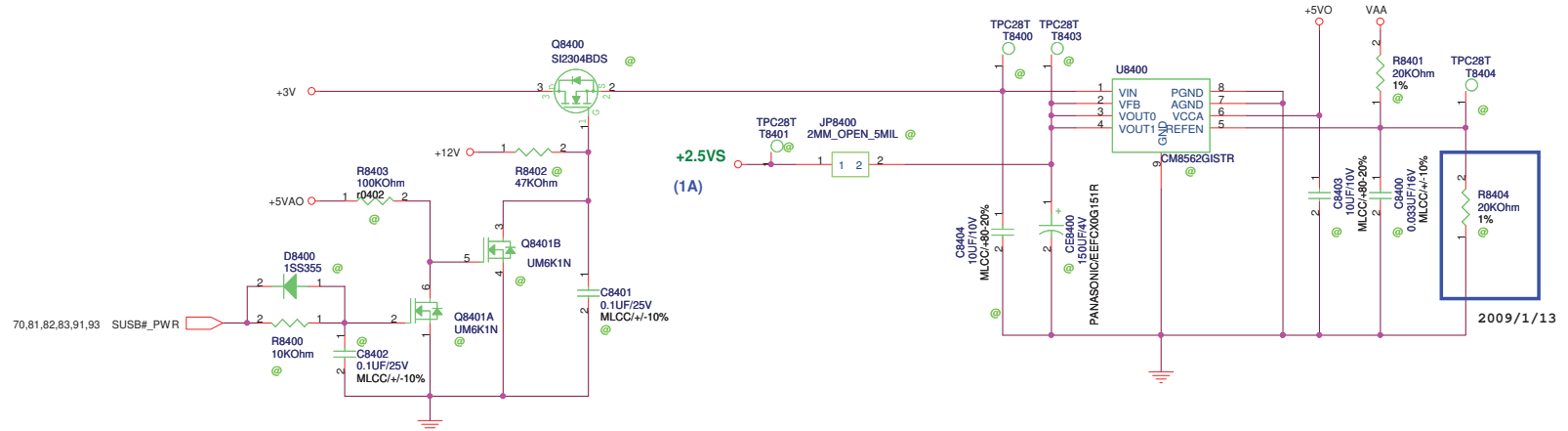




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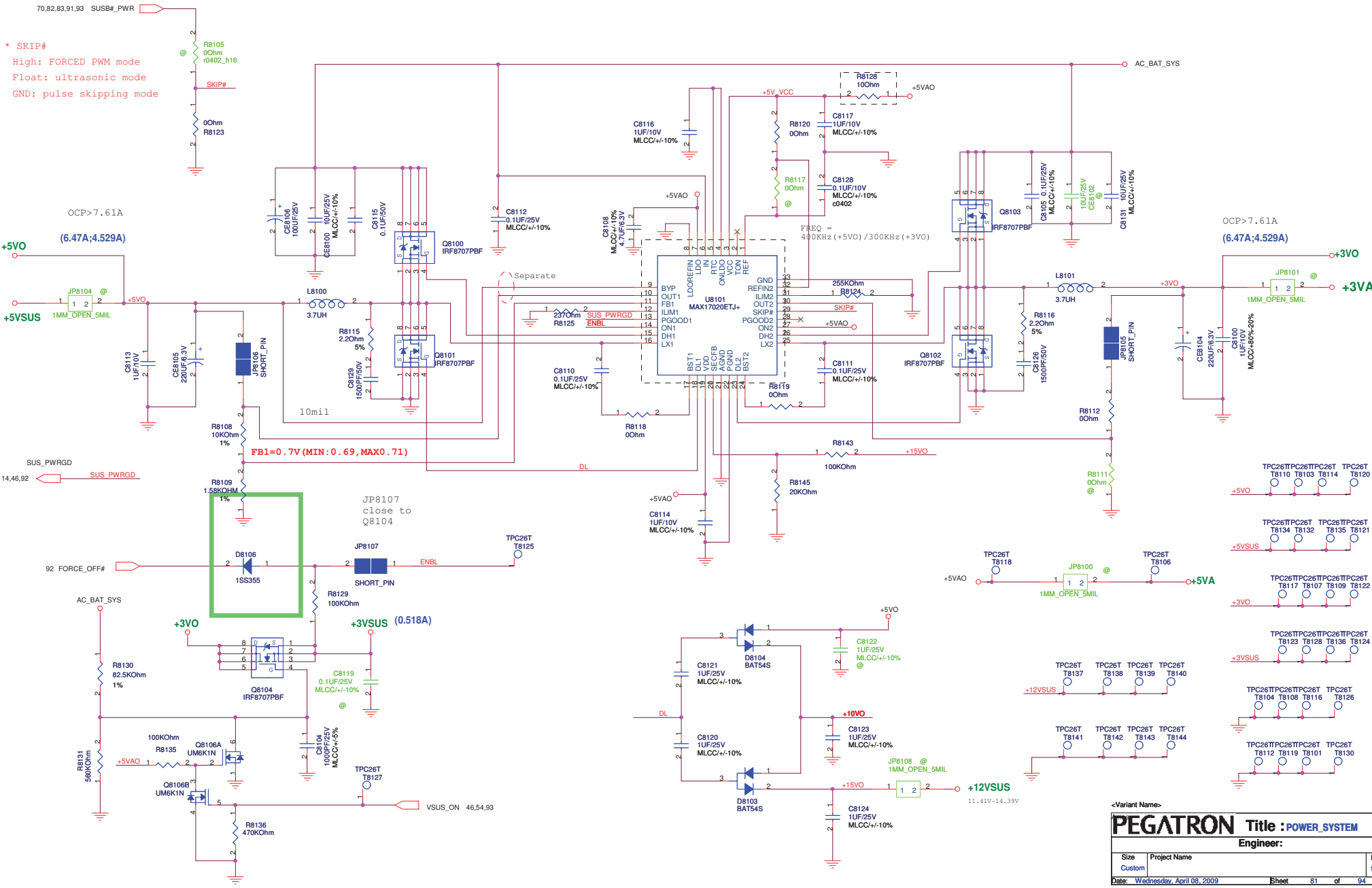
PEGATRON Title : power Vcore	
Pegatron power Team Engineer: Andrew_Liu	
Size	Project Name
Custom	G60VX
Date: Wednesday, April 08, 2009	Sheet 80 of 94
Rev R.1.2	

+2.5VS



<http://hobi-elektronika.net>

PEGATRON		Title : POWER_IO_+2.5VS	
Pegatron power Team		Engineer: Andrew1_Liu	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	80	of 94



<Variant Name>

PEGATRON		Title : POWER_SYSTEM	
Engineer:			
Size	Project Name		Rev
Custom			1.0
Date: Wednesday, April 08, 2009	Sheet	81	of 94

* Rocset = Ioc * DRC / 10uA

+1.5VO: ROCSET = R8213 ; R8215 = R8213=10KOhm

+1.05VO: ROCSET = R8212 ; R8212=R8211=10KOhm

* VREF = 0.6V+-1%

+1.5VO = VREF * (R8206 + R8214) / R8214 =1.52V+-2.26%

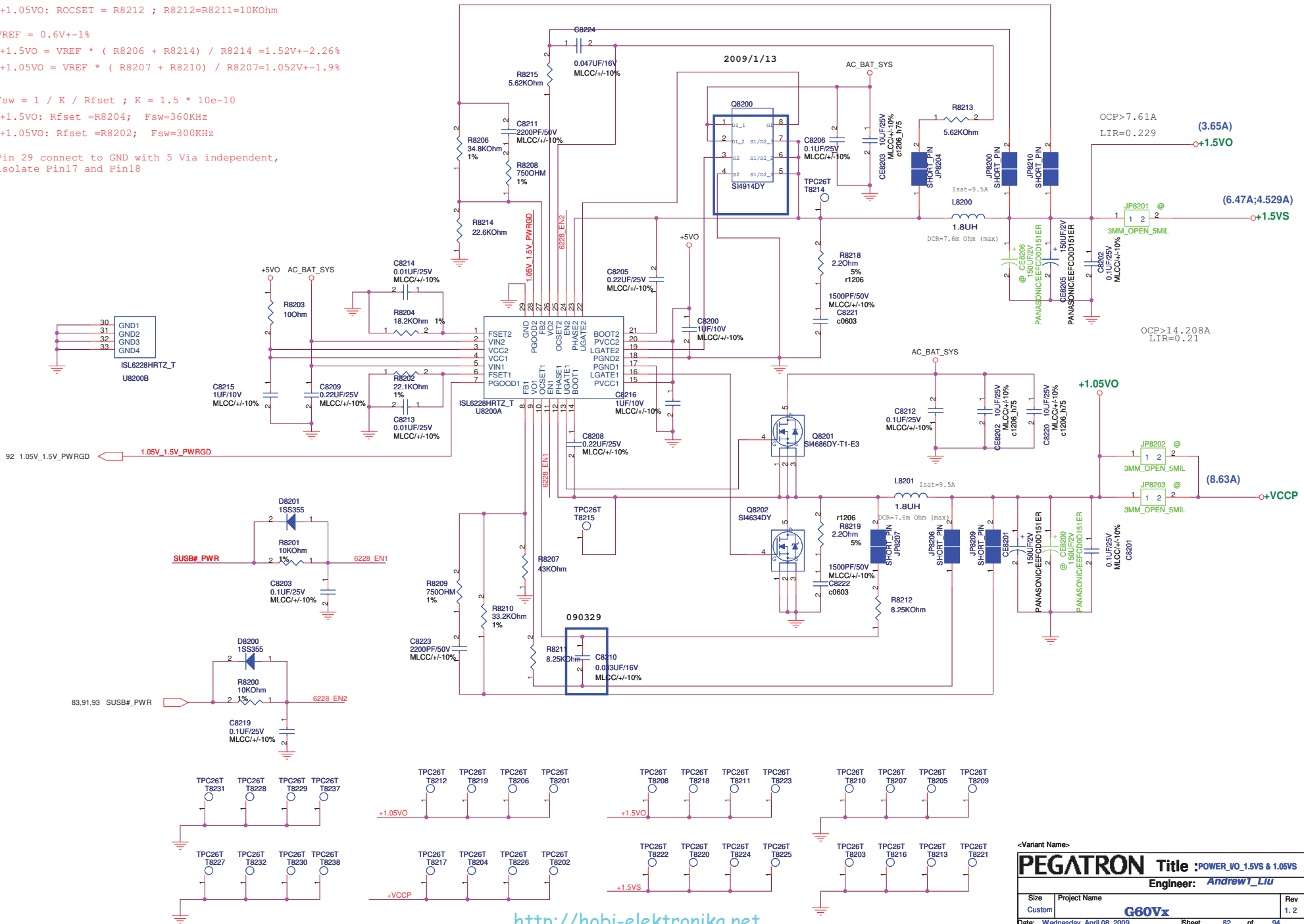
+1.05VO = VREF * (R8207 + R8210) / R8207=1.052V+-1.9%

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

+1.5VO: Rfset =R8204; Fsw=360KHz

+1.05VO: Rfset =R8202; Fsw=300KHz

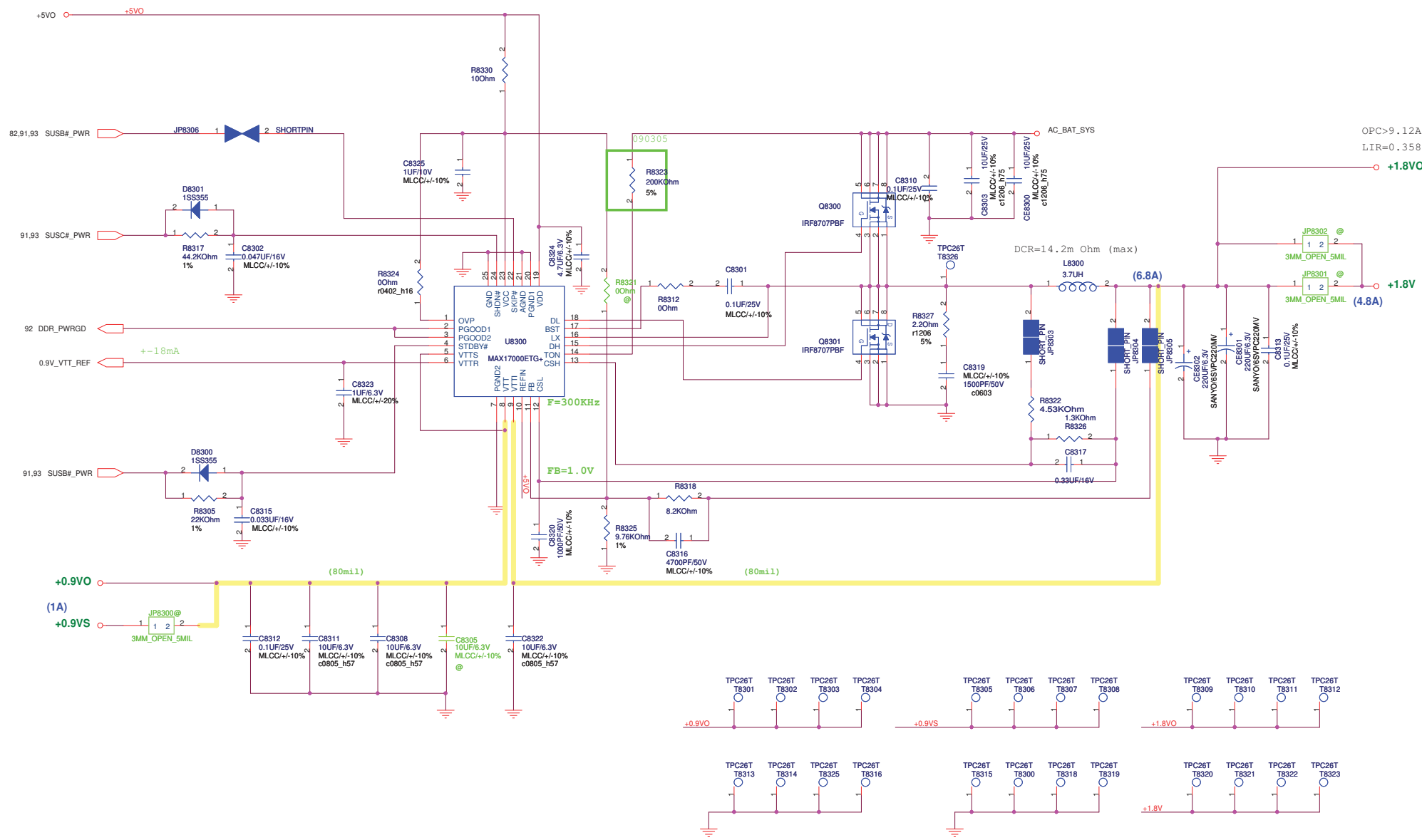
* Pin 29 connect to GND with 5 Via independent, isolate Pin17 and Pin18



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<Variant Name>

PEGATRON Title :POWER_VO_1.5VS & 1.05VS	
Engineer: <i>Andrew T. Liu</i>	
Size Custom	Project Name G60Vx
Date: Wednesday, April 08, 2009	Sheet 82 of 94
	Rev 1.2

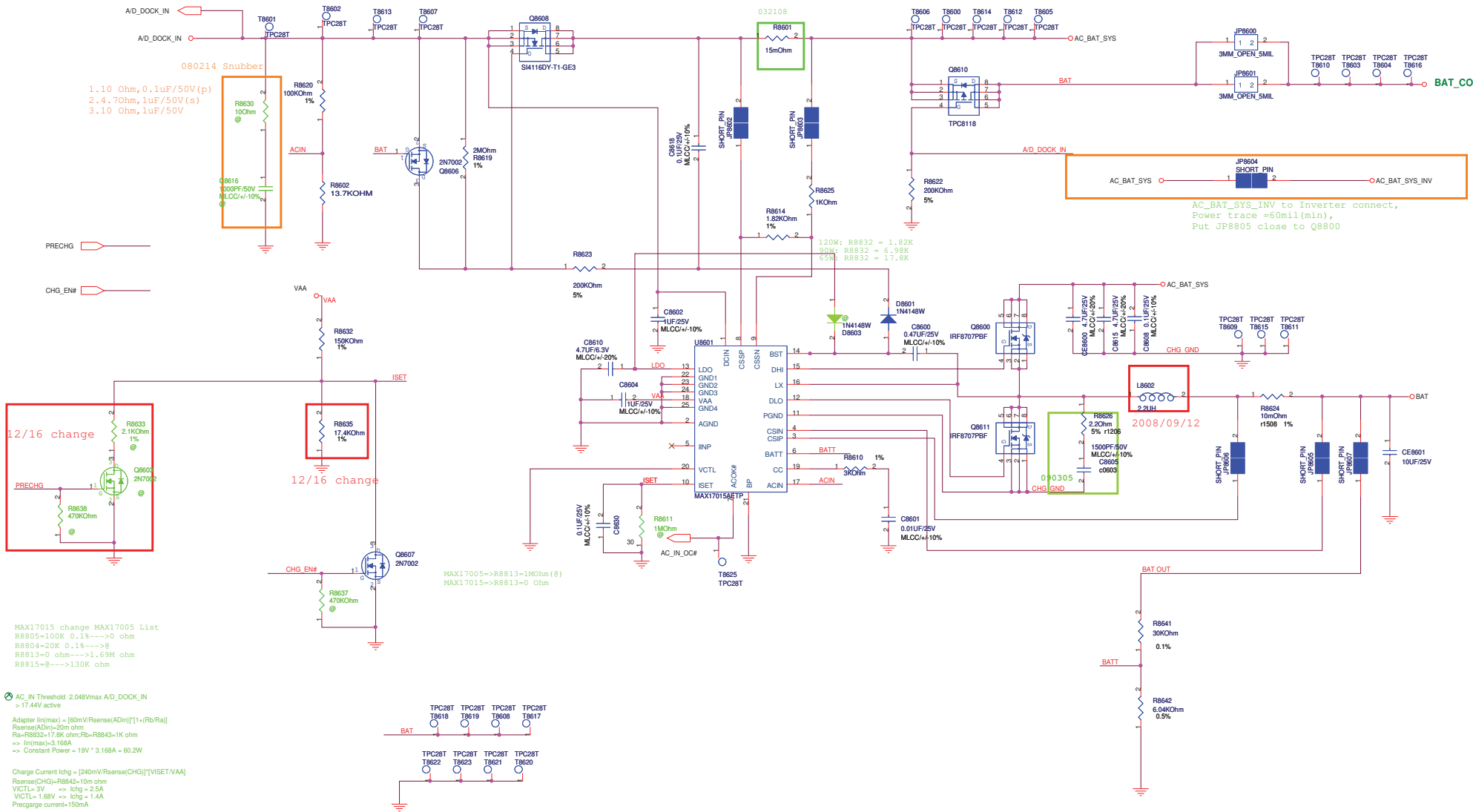


-Variant Name-		
PEGATRON Title : POWER_IO_DDR & VTT		
Engineer: Andrew_Liu		
Size Custom	Project Name G60Vx	Rev 1.2
Date: Wednesday, April 08, 2009 Sheet 63 of 94		

POWER PATH & BAT_LEARN

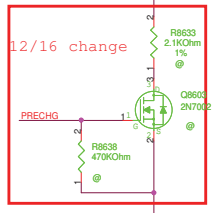
120W: R8801=15mOhm(10G21DR01515110)

65M: R8801=20mOhm(10G21DR02015110)



080214 Snubber
 1.10 Ohm, 0.1uF/50V(p)
 2.4, 70hm, 1uF/50V(s)
 3.10 Ohm, 1uF/50V

AC_BAT_SYS_INV to Inverter connect,
 Power Trace =60mil(min),
 Put JP8805 close to Q8800



12/16 change

MAX17015 change MAX17005 List
 R8805=100K 0.1k---->0 ohm
 R8804=20K 0.1k---->8
 R8813=0 ohm---->1.69M ohm
 R8815=@---->130K ohm

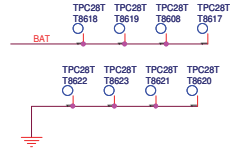
AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter Iin(max) = [50mV/Rsense(ADIN)]*[1+(Rb/Ra)]
 Rsense(ADin)=20m ohm
 Ra=R8832=17.8K ohm;Rb=R8843=1K ohm
 => Iin(max)=3.168A
 => Constant Power = 19V * 3.168A = 60.2W

Charge Current Ichg = [240mV/Rsense(CHG)]*[VSET/VAA]
 Rsense(CHG)=R8842=10m ohm
 VCTL=3V => Ichg = 2.5A
 VCTL=1.88V => Ichg = 1.4A
 Precharge current=150mA
 2.4V-VCTL<4.2V->3cell->Vcell =4.2V+(4.2V-VCTL)/6
 3 cell->VCTL= 3.9V => Vcell = 4.635V
 0V-VCTL=1.8V->4cell->Vcell =4.2V+(VCTL/6)
 4 cell->VCTL= 0.3V => Vcell = 4.635V

Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells
 0.8 > Vmode (try to GND) ----> Learning mode

VCTL= 0.8V or DCIN < 7V -->Charger Disable

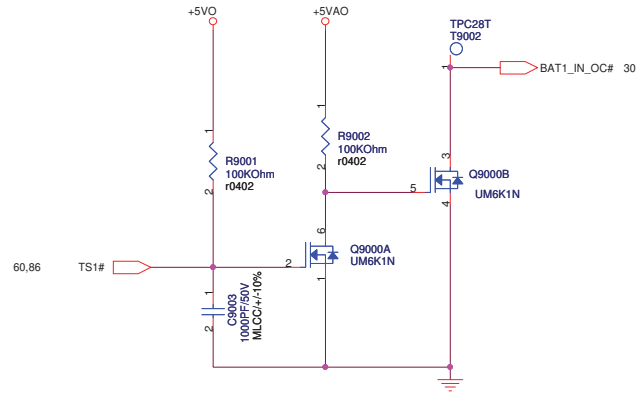
VCTL = 3.9V; CHG VOLTAGE = 4.25/CELL(3 CELL)



MAX17005->R8813=1Mohm(8)
 MAX17015->R8813=0 Ohm

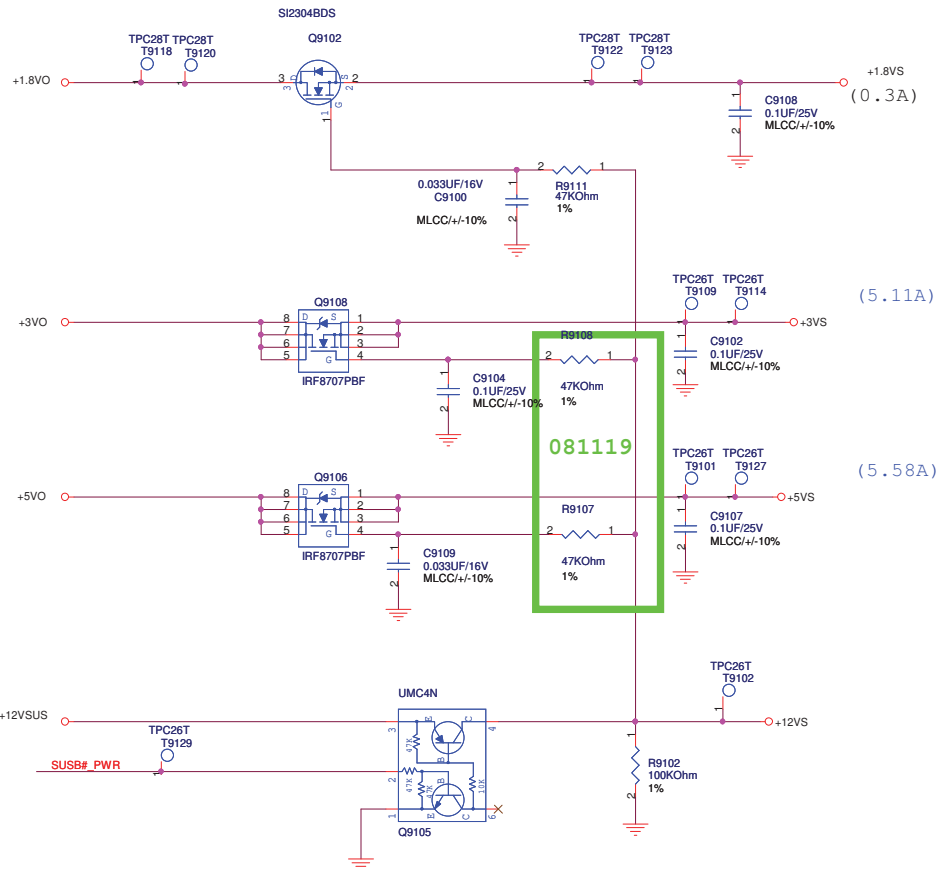
2008/09/12

BATTERY IN DETECT

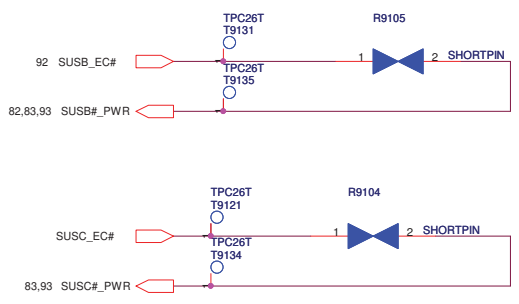
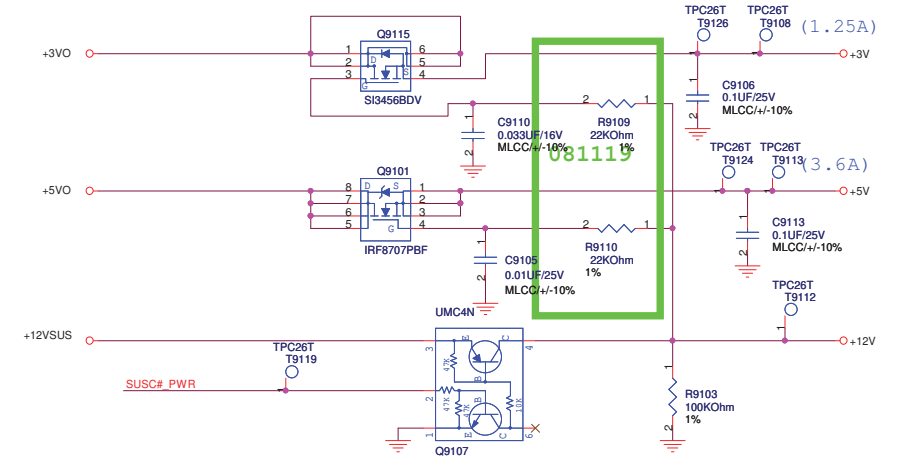


PEGATRON		Title : POWER_DETECT	
Pegatron power Team		Engineer: <i>Andrew Liu</i>	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Wednesday, April 08, 2009	Sheet	90	of 94

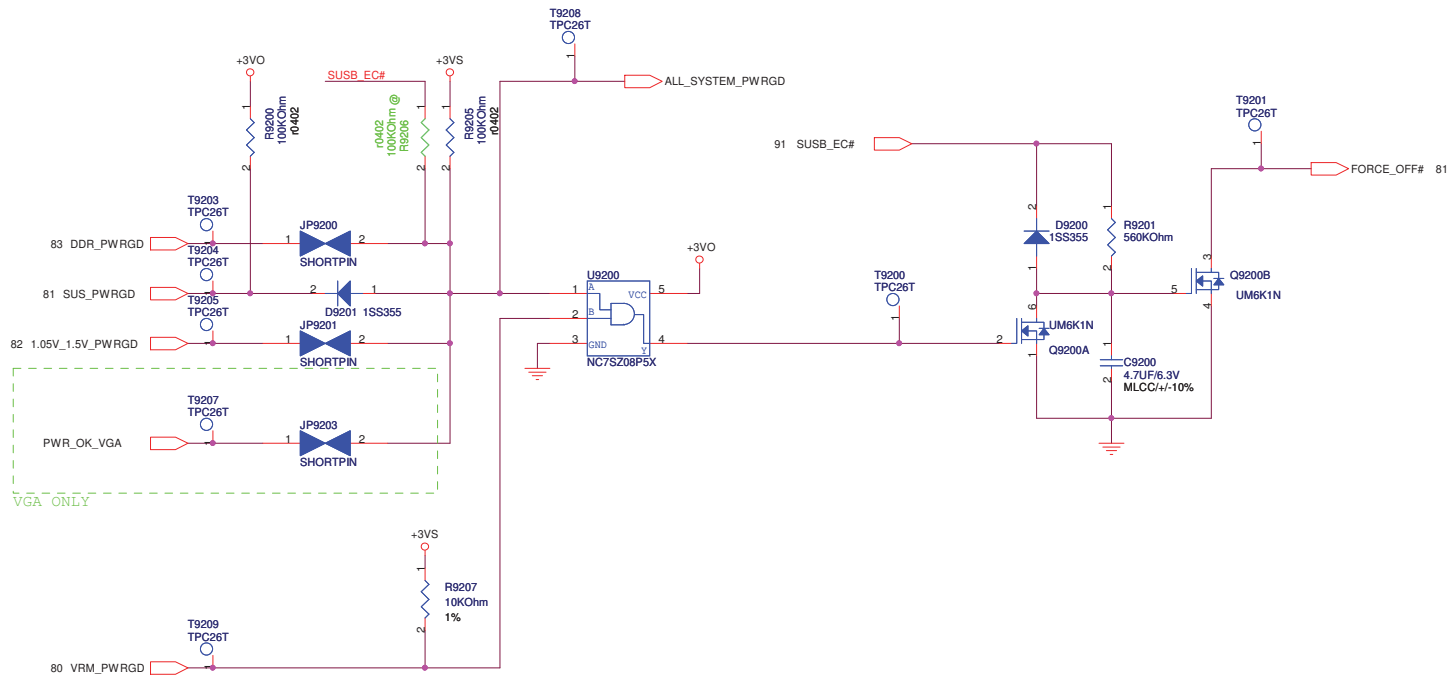
SUSB#_PWR POWER



SUSC#_PWR POWER

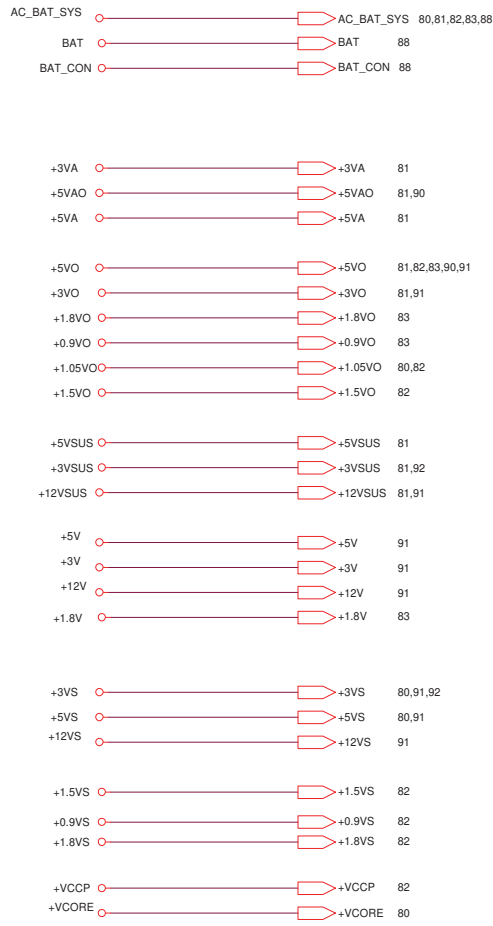


POWER GOOD DETECTOR

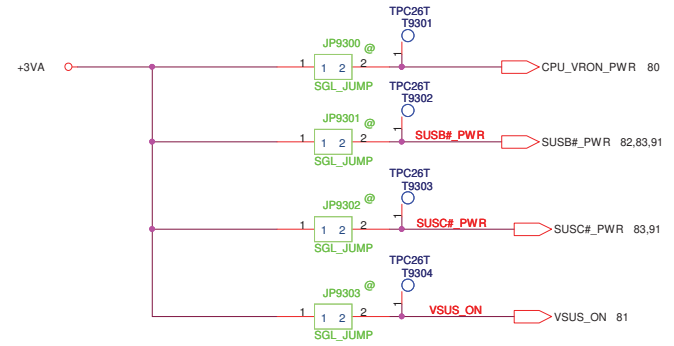


<http://hobi-elektronika.net>

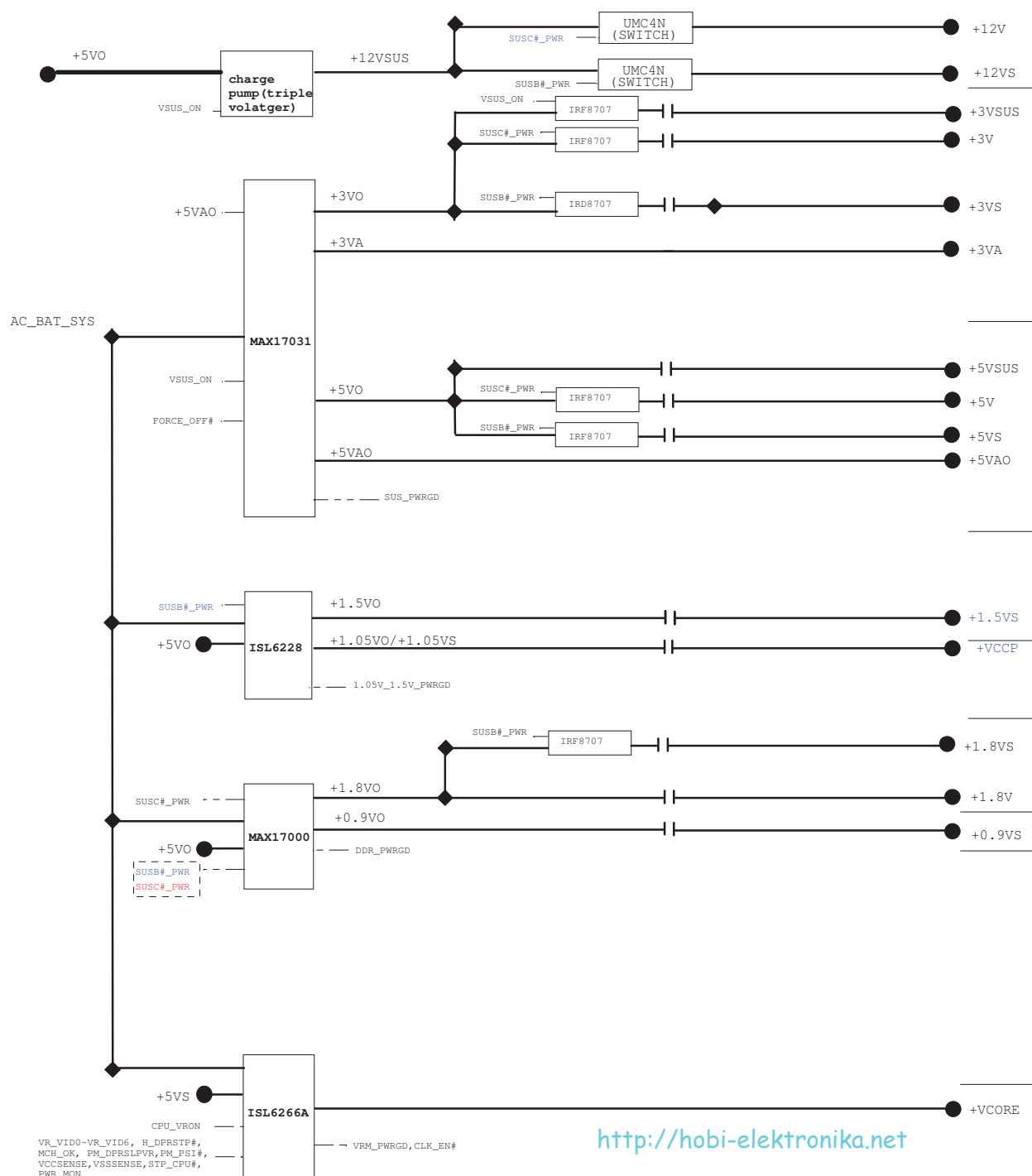
<Variant Name>		
PEGATRON Title :POWER_PROTECT		Rev
Engineer: Andrew1_Liu		1.2
Size Custom	Project Name G60Vx	Date: Wednesday, April 08, 2009
Sheet 92 of 94		



FOR POWER TEST



<Variant Name>			
PEGATRON		Title :POWER SIGNAL	
Engineer: <i>Andrew1_Liu</i>			
Size	Project Name		Rev
Custom	G60Vx		1.2
Date:	Wednesday, April 08, 2009	Sheet	93 of 94



		Design rating
	+12V	(10mA)
	+12VS	(10mA)
	+3VSUS	(0.74A)
	+3V	(1.29A)
	+3VS	(8.62A)
	+3VA	(0.133A)
	+5VSUS	(0.01A)
	+5V	(3.61A)
	+5VS	(3.875A)
	+5VAO	(0.01A)
	+1.5VS	(3.77A)
	+VCCP	(12.816A)
	+1.8VS	
	+1.8V	(11.96A)
	+0.9VS	(2A)
	+V CORE	(47A)
		(47A)

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VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON

<Variant Name>
PEGATRON Title :POWER_FLOWCHART
 Engineer: Andrew Li
 Size Project Name Rev
 Custom G60Vx 1.2
 Date: Wednesday, April 08, 2009 Sheet 04 of 04

Rev	Date	Description
R1.0		First Release!
R1.1		

Rev	Date	Description

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PEGATRON		Title : Revision History	
Pegatron BU2 HW Team 3		Engineer:	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Thursday, March 05, 2009		Sheet	96 of 100

R1.0

Item	Before	After	Reason	Owner	Date
	R8036:10.5k	R8036 change to 8.87k	To change VCORE load line to meet Intel spec.	Eve Kuo	2008/02/25
	R8015:0805	R8015 from 0805 --> 0603	0805 is common component to use.	Eve Kuo	2008/02/25
	Q8612, R8628, R8629	De-pop Q8612, R8628, R8629	G50V support 3S battery	Eve Kuo	2008/02/25

R1.1

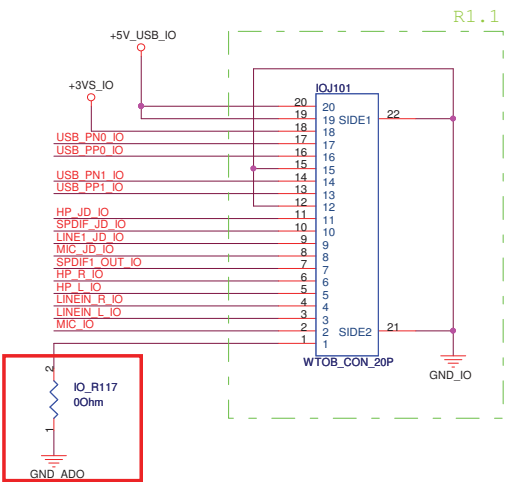
Item	Before	After	Reason	Owner	Date
	JP8601,JP8606	Delete JP8601,JP8606	Due to the factory's requirement, the bead and jump won't be co-lay.		

R2.0

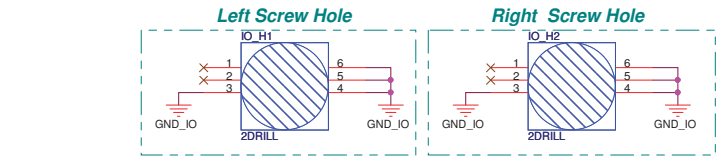
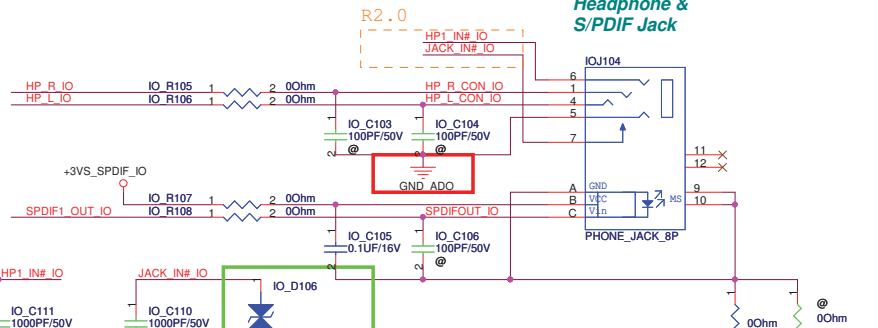
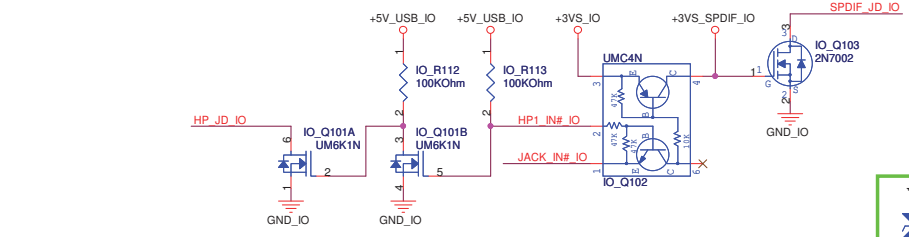
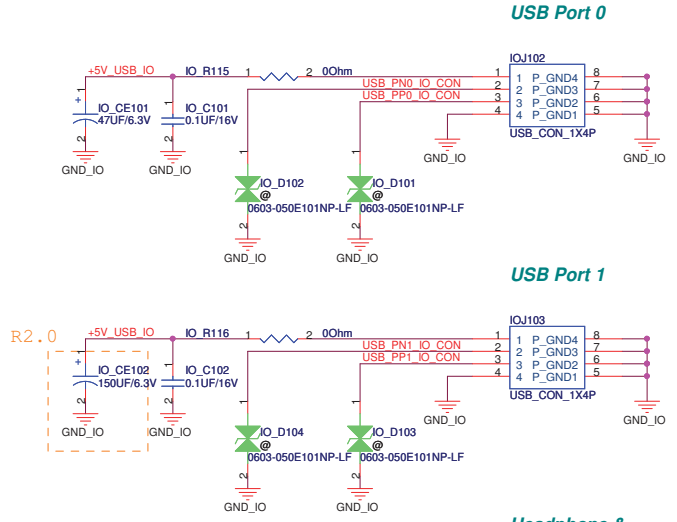
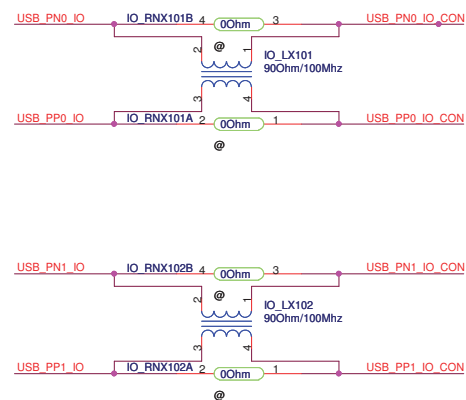
Item	Before	After	Reason	Owner	Date

<http://hobi-elektronika.net>

PEGATRON		Title : POWER_HISTORY	
Pegatron BU2 HW Team 3		Engineer:	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Thursday, March 05, 2009		Sheet	97 of 100

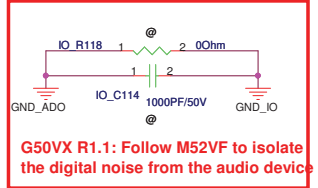


G50VX R1.1: Follow M52VF

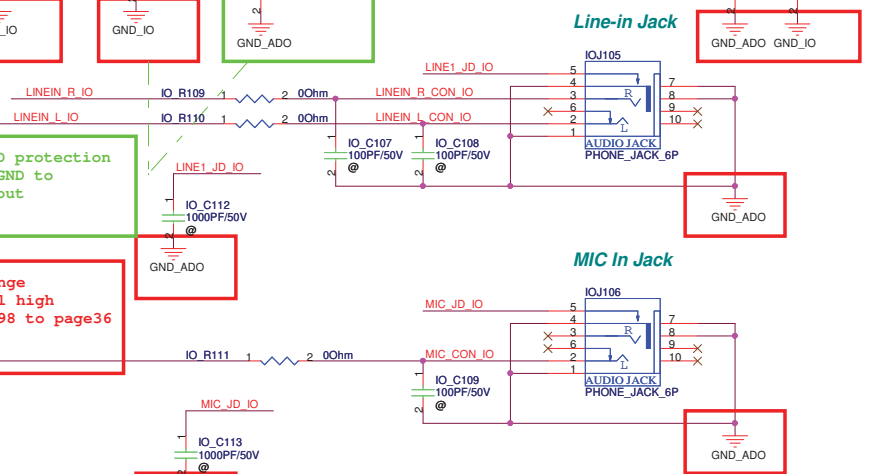


Add IO_D105, IO_D106 for ESD protection
Change IO_C111 and IO_C110 GND to GND_IO from GND_ADO for layout
G60VX R1.2 20090304

G50VX MB R1.1: change MIC_VREFOUT and pull high resistor form page98 to page36



G50VX R1.1: Follow M52VF to isolate the digital noise from the audio device



2008/02/18	<p>1. Change the port of SATA ODD and SATA HDD to meet design IP. (Page 51)</p> <p>2. Change SMBus of the Cap-sense Touch key from SMB0 to SMB1. (Page 56)</p> <p>3. Correct the signals of ESATA. (Page 66)</p> <p>4. Set R3318 as mount. (Page 33)</p> <p>5. Correct the signals of PCIE of WLAN. (Page 53)</p> <p>6. Correct the signals of PCIE of TV Tuner and add the reset signal for PCIE TV Tuner. Set the 1.5V power rail as mount. (Page 64)</p> <p>7. Unmount pull up resistors of 1394_SCL and 1394_SDA. (Page 40)</p> <p>8. Add common choke on CMOS for EMI requirement. (Page 45)</p> <p>9. Correct the signals of Newcard Debug Card. (Page 44)</p> <p>10. Change the R1407 to 1206 size. (Page 14)</p>
2008/02/20	<p>11. Change EC to 8512. (Page 30)</p> <p>12. Pull BAT2_IN_OC# up to fix CHARGER_LED bug. (Page 30)</p>
2008/02/21	<p>13. Delete the LCD_BL_DA signal which is designed for Light Sensor. (Page 45)</p> <p>14. Change the R4504 to 100K to fix LCD will display white screen when system boots. (Page 45)</p> <p>15. Add uP schematic to control the Game LED for FM request. (Page 69 & 24)</p>
2008/03/05	<p>16. Add discharge circuit for 2.5VS (Page 57)</p> <p>17. Change BT and WLAN ON/OFF control method (Page 53 and 61)</p> <p>18. Add ESD Protected Diode on SATA ODD and E-SATA(Page 51 and 66)</p>
2008/03/11	<p>19. Change PEG CLK Source on Clock Gen(Page 29)</p>
2008/03/14	<p>20. Change TouchPad Connector. (Page 31)</p>
2008/03/18	<p>21. Add 2 diodes to follow EC suggestion. (Page 22)</p> <p>22. Change the IO Connector. (Page 65, 98)</p> <p>23. Change Power Circuit. (Page 80-94)</p> <p>24. Exchange CLK_ICHPCI and CLK_KBCPCI to follow Design IP setting. (Page 30)</p> <p>25. Swap USB Ports to follow Design IP. (Page 45, 52, 64, 68,)</p>
2008/03/19	<p>26. Add 00HM resistor between thermal sensor and CPU to follow Intel Design Guide. (Page 50)</p> <p>27. Add a N-MOS between U4401 and PCI_WAKE# to prevent system can't enter S4 which is waked by U4401. (Page 44)</p>
2008/03/24	<p>28. Add +3VSUS to NewCard Power Switch. (Page 43)</p> <p>29. Change the pull-up power source of SMB1 to +3VS. (Page 30)</p>
2008/03/26	<p>30. Change HDD Connector. (Page 51)</p> <p>31. Add EMI Solution on LVDS connector. (Page 45)</p> <p>32. Change the Ground of DC Jack for EMI. (Page 60)</p> <p>33. Add EMI Solution on USB connector. (Page 52)</p> <p>34. Add EMI Solution on HDMI connector. (Page 48)</p> <p>35. Add EMI Solution on IO connector. (Page 65)</p> <p>36. Add EMI Solution on HDD connector. (Page 51)</p> <p>37. Add EMI Solution on T/P connector. (Page 31)</p>
2008/05/02	<p>38. Correct the Headphone Jack Detect schematic. (Page 98)</p> <p>39. Change capacitor to MLCC. (Page 33)</p>
2008/05/04	<p>40. Add over-clock strapping. (Page 29)</p>
2008/05/06	<p>41. Reserve Finger Printer Schematic. (Page 63)</p> <p>42. Add Amplifer strapping. (Page 37)</p> <p>43. Remove the Capacitor of headphone. (Page 37)</p>

2008/11/17	<p>3. Add comment for supporting Quad Core CPU. (Page 3)</p> <p>4. Reserve R0411 for support Quad Core, Add BOM option for DC/QC. (Page 4)</p> <p>5. Add comment for DC/QC. (Page 5)</p> <p>10. Add comment for DC/QC. (Page 10)</p> <p>20. Add comment for delete Modem function. (Page 20)</p> <p>21. Add comment for BOM option. (Page 21)</p> <p>29. Add comment for CLK Gen BOM option. (Page 29)</p> <p>30. Change: add Keyboard_LED control signal. (Page 30)</p> <p>31. Add keyboard LED Power connector, Add comment for delete CIR BOM option (31)</p> <p>34. Add BOM option for delete RJ11 (34)</p> <p>35. Add BOM option for delete Modem function (35)</p> <p>36. Add BOM option for ALC662 and ALC663 co-lay (36)</p> <p>38. Add BOM option for supporting Array MIC (38)</p> <p>44. Add BOM option for supporting Debug Connector (44)</p> <p>45. Add BOM option for supporting Array MIC (45)</p> <p>50. Add BOM option for Thermal Sensor for QC and DC (50)</p> <p>63. Add BOM option for deleting FP function. (63)</p> <p>68. Add BOM option for deleting OLED connector. (68)</p> <p>69. Co-using of EC.GPA3 pin, for G50V reserved for controlling GAME_LED#. (69)</p>
2008/11/24	<p>31. Change J3103 Pin5, 6 GND name from GND_POWER to GND. (31)</p> <p>30. Change net GAME_LED_EC# from connecting with EC.GPA3 to EC.GPA6.(30)</p> <p>68. Delete all the content of page 68: OLED Connector.(68)</p>
2008/11/25	<p>21.Add TP to USBP9N/P.(21)</p> <p>45.Add F4502 to protect the M/B from damaging by AC_BAT_SYS_INV short to GND; Change C4513 from 0.1UF/16V to 0.1UF/25V.(45) 2008-11-25-21-06</p>
2008/11/26	<p>14.Change C1447 from 0805 to 0603 to satisfy the mechanical height constrain.(14)</p>
2008/12/31	<p>80.Change power solution, related page is 80-84, 86, 90-94</p>
2009/1/2	<p>60.Replace D6002,D6003,D6004 with integrated D6002 for improving the rise time</p> <p>70.Reserve R7007 for AMD M96 VGA card</p> <p>33.Add R3323 to reduce the LAN power consumption ?</p>
2009/1/4	<p>36.Change MIC_VREFOUT and 4.7k ohm pull high resistor from page98 to page36, related page is 98, 65, 36</p> <p>98.isolate the GND_AUDIO and GND_IO</p> <p>23.Follow Intel DG R2.2, change C2301 from 0.1UF/16V X7R-->1UF/10V X5R</p> <p>38.change the DSP VDD power to +1.5VS for better immunity of noise and less power</p> <p>31.change the keyboard connector pin define for chocolate keyboard</p>
2009/1/8	<p>21.Swap USB port 4 and 8, Camera use port 8, newcard use port 4, to decrease the EMI of camera when USB HDD is also used</p> <p>80.power team update the schematic</p>
2009/1/13	<p>31.Keyboard signal swap for capacitor layout</p> <p>30.Change EC pin GPH3/ID3 from BAT_LEARN to T3011, delete BAT_LEARN signal</p> <p>80,81,84. Add net CLK_EN#; Change U8101 symbol; Add R8404</p> <p>31.Keyboard connector signal change back</p>

G60VX R1.2

2009/03/05 Page 23: R2319, R2320 change to 100 ohm (Follow Intel DG R2.2)
Page 32: Reserve Force_off# connect to EC_RST#
page 41/42: Reserve 10pf capacitor for SD card CLK for EMI
Page 43: Add MOS to prevent the leakage current from +3VSUS (U4301 pin 17) to BUF_PLT_RST#
page 45: Reserve 33pf capacitor for PWR_LED#, GAME_LED# for EMI
Page 45: Change R4501, mount C4503 to tune the falling time of +3VS_LCD
Page 46: Follow M52V to change the schematic of RGB to tune the rise/fall time
Page 46: Add schematic to protect the HSYNC/VSYNC from pulling low by CRT connector for M52VP
Page 48: Reserve schematic for G50VX HDMI HPD signal level shift
Page 48: Reserve pull high resistor and decoupling capacitor for TMDS signals
Page 53: change WLAN pin 39,41 from NC to 3.3V power for full support Intel WiFi Link
Page 69: Change GAME_LED# control from PIC MCU to EC
Page 70: Reserve bead for MXM card for EMI
Page 81: Reserve D8107 to prevent leakage from +3V, +3VS to +3VSUS and ENBL when VSUS_ON accidentally pulled low
Page 98: Reserve VPORT (varistor) on signal HP1_IN#_IO and JACK_IN#_IO for ESD protection

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PEGATRON		Title : System History 2	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Thursday, March 12, 2009		Sheet	100 of 100