

# ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

## Lanai Discrete VGA nVidia NB8M Schematics Document

uFCPGA Mobile Merom  
Intel Crestline-PM + ICH8M

2007-03-19

REV : 1.2(DELL: X02)

MB PCB	
Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

*BOM NO. ???*  
*PCB P/N: ???*

<Variant Name>



PROJECT: **Lanai**

REVISION  
**1.2**

DATE: *Monday, March 19, 2007*  
SHEET **1** OF **69**

DESCRIPTION: *Cover Page*

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
**Terry Lin**

# LANAI: DISCRETE

**CLOCK**  
CK410M+LP  
PG 21

**POWER**

POWER SEQUENCE LOGIC	PG 51
POWER CHARGER	PG 57
POWER CONTROL SWITCH	PG 49
DISCHARGE PATH	PG 49
+3.3V_SUS/+5V_SUS/+3.3V_RUN +5V/+3.3V/+1.8V/+1.25V_RUN	

POWER CON. PG 59

**Merom**  
(478 Micro-FCPGA)  
PG 7,8  
(Symbol Rev.09)

**POWER**

POWER I/O	PG 55
+1.5V_RUN/+1.05V_VCCP	
REGULATOR	PG 58
+VCC_GFX_CORE/+1.25V_RUN	
POWER VCORE	PG 53
POWER SYSTEM	PG 54
5V_ALW & 3.3V_ALW	
REGULATOR	PG 56
+1.8V_SUS/+0.9V_DDR_VTT	

Panel Connector PG 28

**nVIDIA G86M**  
PCI EXPRESS GFX  
PG 22,23,24,25,26,27

**Crestline**  
1299 uFCBGA  
PG 9,10,11,12,13,14  
(Symbol Rev.09)

**IO Board**

CRT CONN. VGA

TV CONN. TVOUT

USB CONN. x2 USB2.0 (P2,3)

MINI-CARD WLAN PCIEx1 (Lane2)

MINI-CARD WWAN USB2.0 (P9)

D.B CON PG 50

**ICH8-M**  
676 BGA  
PG 15,16,17,18  
(Symbol Rev.09)

SIM CARD Board

AUDIO/AMP PG 44,45,46

MDC PG 36

S/PDIF TO TV CONN. PG 30

DIGITAL MIC. PG 28

Speaker CON PG 46

WtoB CON PG 46

Audio Jacks \*3

JACK Board

RJ11 Board

DDR2-SODIMM1 PG 19

DDR2-SODIMM2 PG 19

USB CONN. PG 39

USB Board

PCIE (Lane6)

PCI

PCIE (Lane4)

USB2.0 (P6)

USB2.0 (P7)

CARD READER 1394/R5C833 PG 32,33,34

BCM5906KMLG QFN-68 PG 47

RJ45/Magnetic PG 48

EXPRESS-CARD R5538 PG 35

USB2.0 (P5)

CAMERA PG 28

SATA

SATA-HDD PG 31

IDE

CD-ROM PG 31

Bluetooth PG 41

SIO MEC5025 128KB Flash TMKBC 128 Pins VTQFP PG 37

SIO ECE5011 Expander USB 2.0 Hub (4) 128 Pins VTQFP PG 38

CIR PG 41

FLASH PG 40

Touchpad CON. PG 41

FAN & THERMAL EMC4001 PG 43

USER INTERFACE PG 42

SNIFFER PG 42

CAPBTN CON. PG 40

**INDEX**

Pg#	Description	DNI LIST
01	Cover Page	
02	Schematic Block Diagram	
03	INDEX	
04	Bus connection	
05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU ( Merom 、 Penryn )	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM( 533MHz 、 667MHz )	
21	Clock Generator ( CK410M+LP )	
22-27	VGA ( nVIADA - G86M & GDDR3)	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 ( R5C833 )	
35	PCI-Express Card	
36	MDC CONN	
37	EC ( MEC5025 )	
38	SIO ( ECE5011 )	
39	USB PORT x 2	
40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
43	HARDWARE MONITOR ( EMC4001 )	
44-46	AUDIO CODEC & AMP	
47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
50	BtoB CON	
51	Power Sequence Logic	
52	XDP	
53-59	Power Circuit	
60	SCREW PAD	
61	Change list (1)	
62	Change list (2)	
63	Change list (3)	

Pg#	Description	DNI LIST
64	Power circuit Change list	
R01	Modem board cover page	
R02	RJ-11 CONN	
R03	Modem board Change list	
U01	USB board cover page	
U02	USB PORT ( SINGLE * 2 )	

<Variant Name>



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DESCRIPTION: **INDEX**

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RELEASE DATE :

DESIGN ENGINEER :  
**Terry Lin**

Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

**Layout Note**

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE	
Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

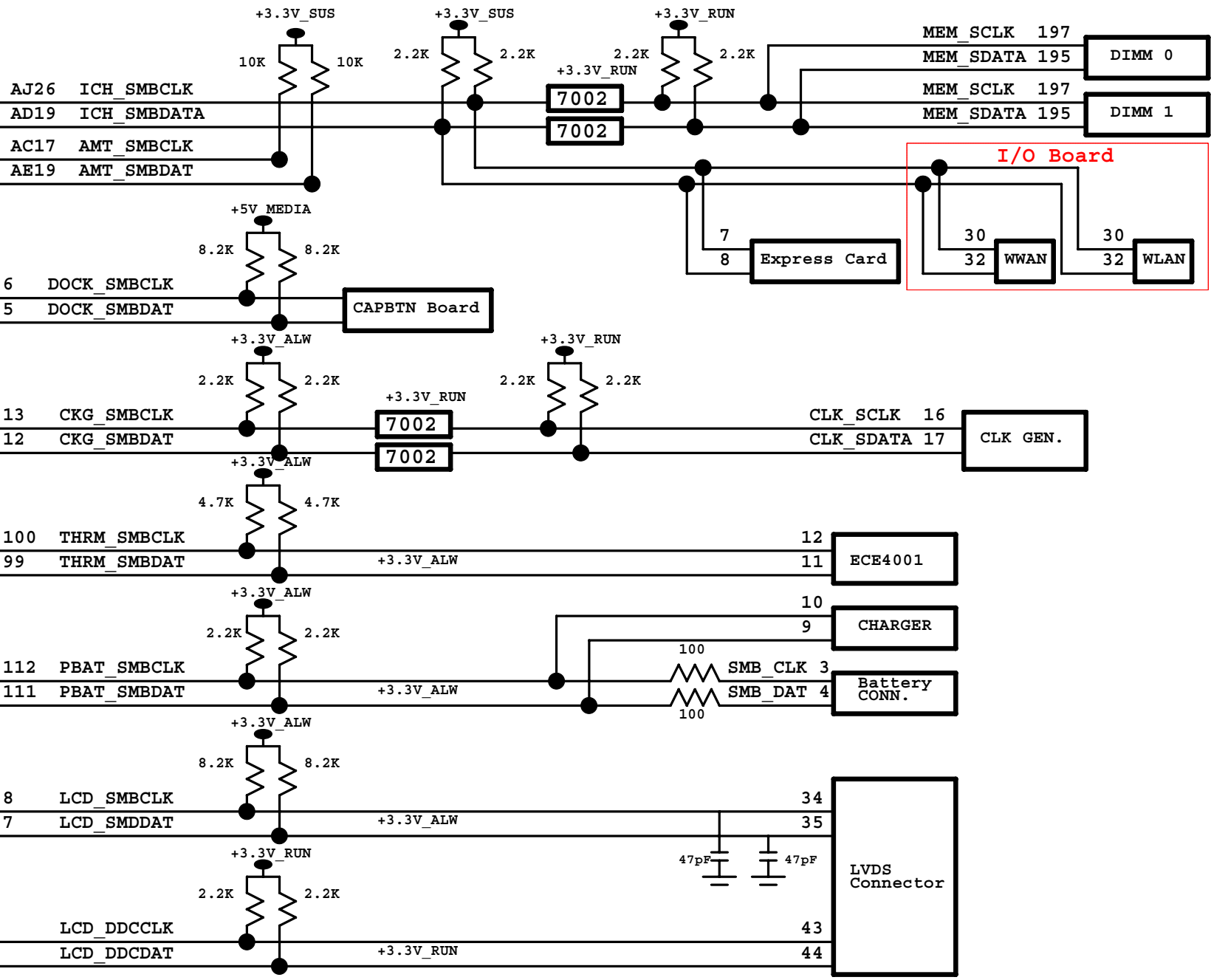
USB TABLE	
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

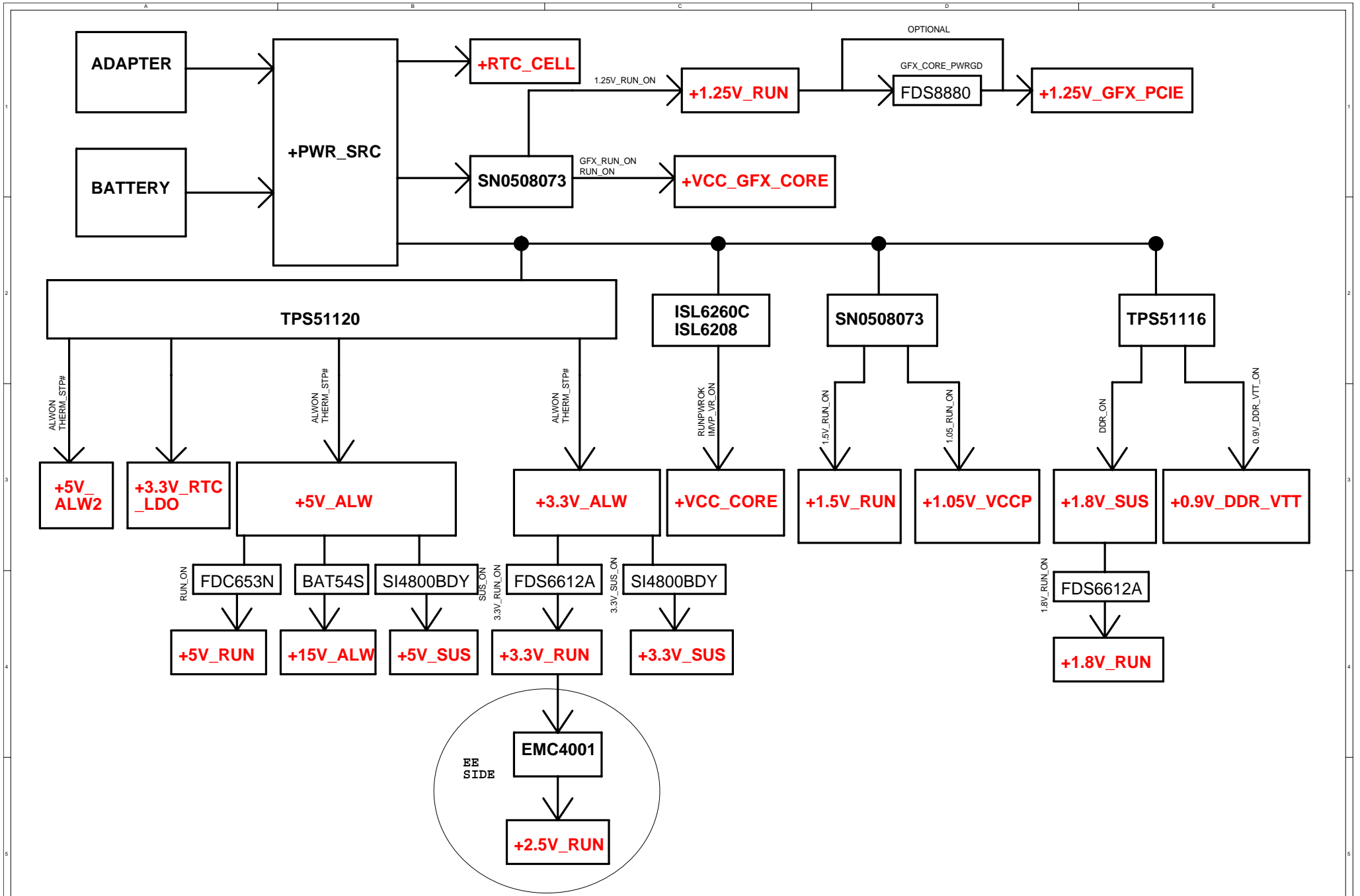
Note : No USB for WLAN

**ICH8-M**

**SIO  
MEC5025**

**VGA**





<Variant Name>



PROJECT: Lanai

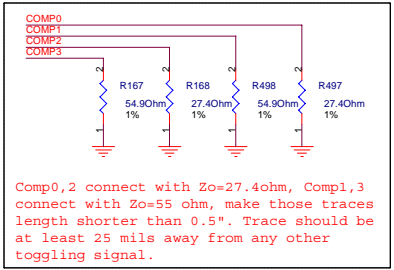
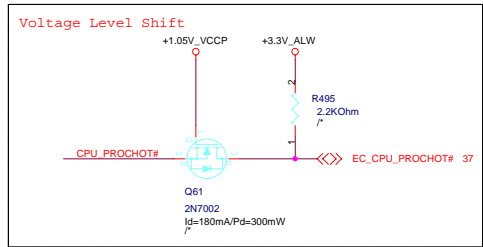
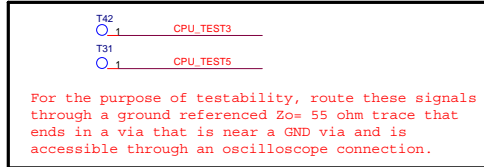
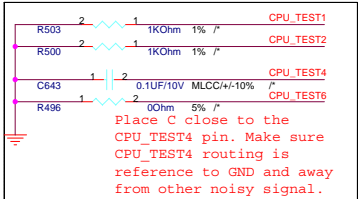
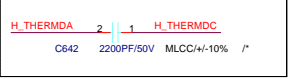
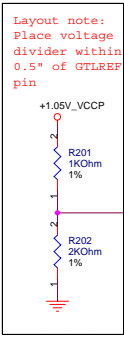
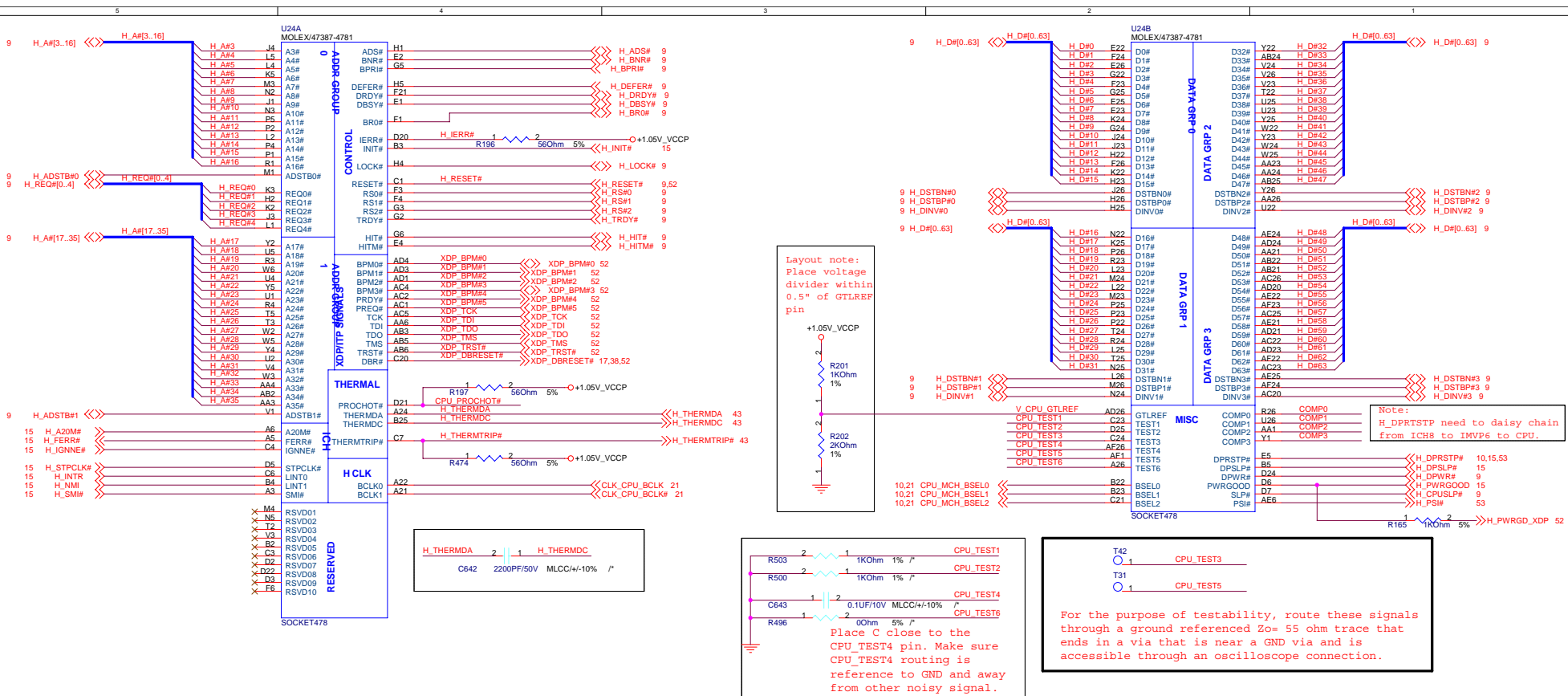
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DESCRIPTION: Power Rail

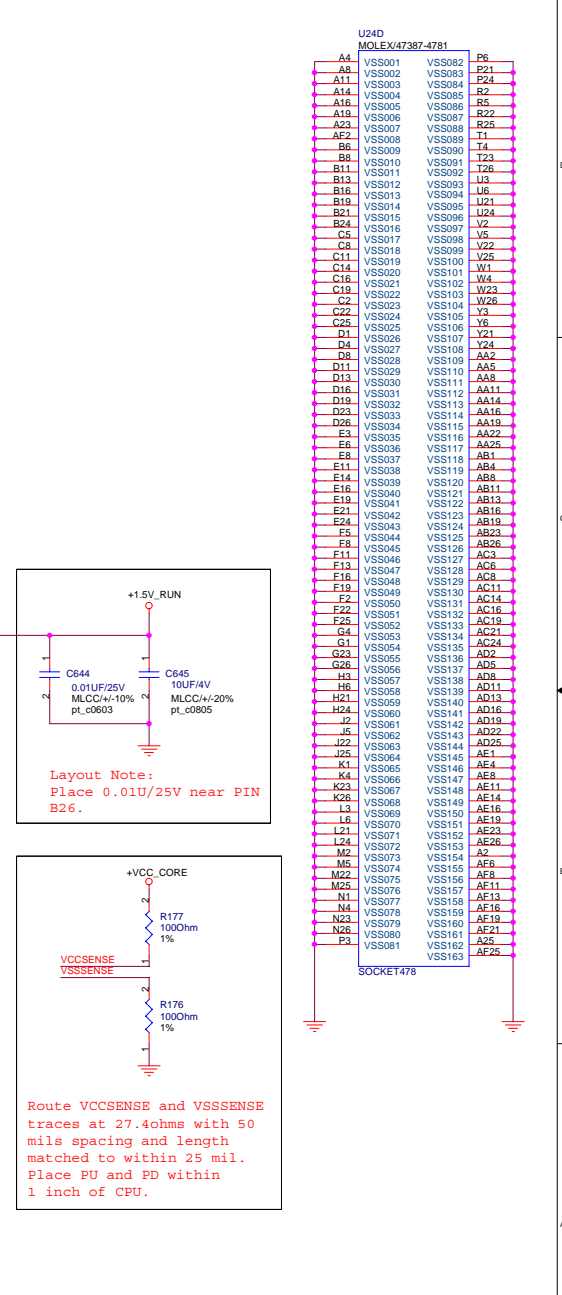
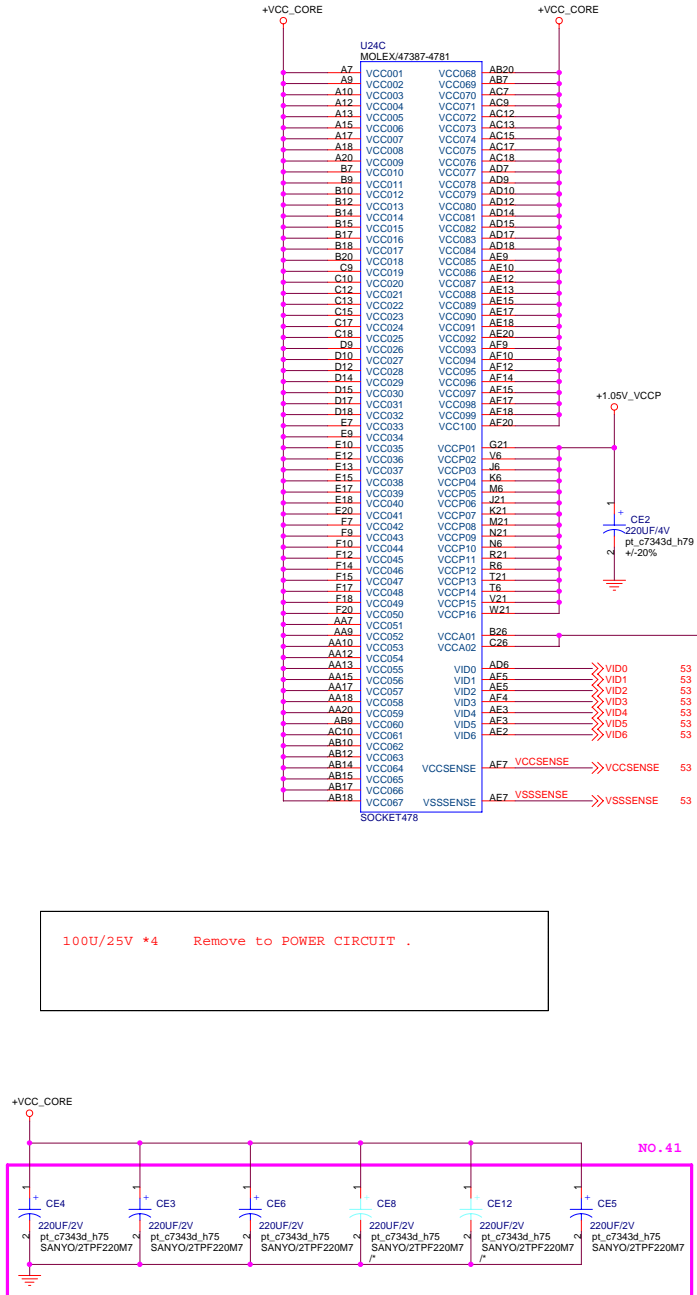
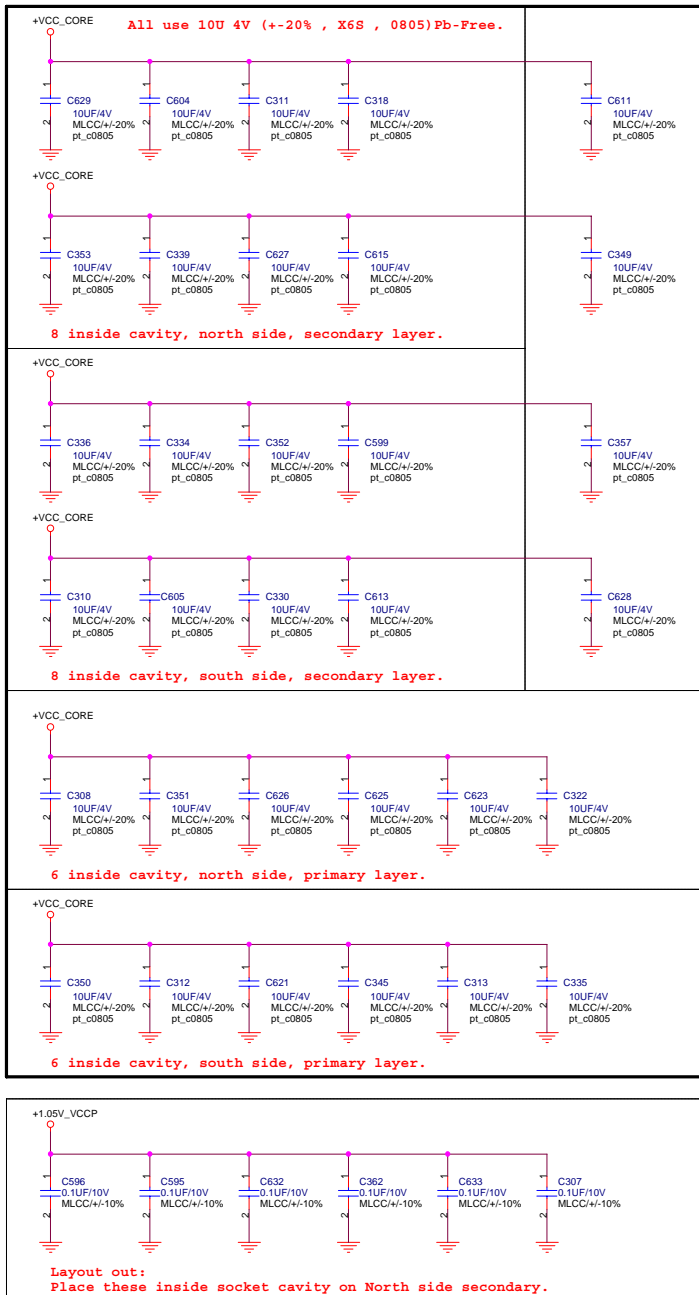
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RELEASE DATE :

DESIGN ENGINEER :  
Eric Ko



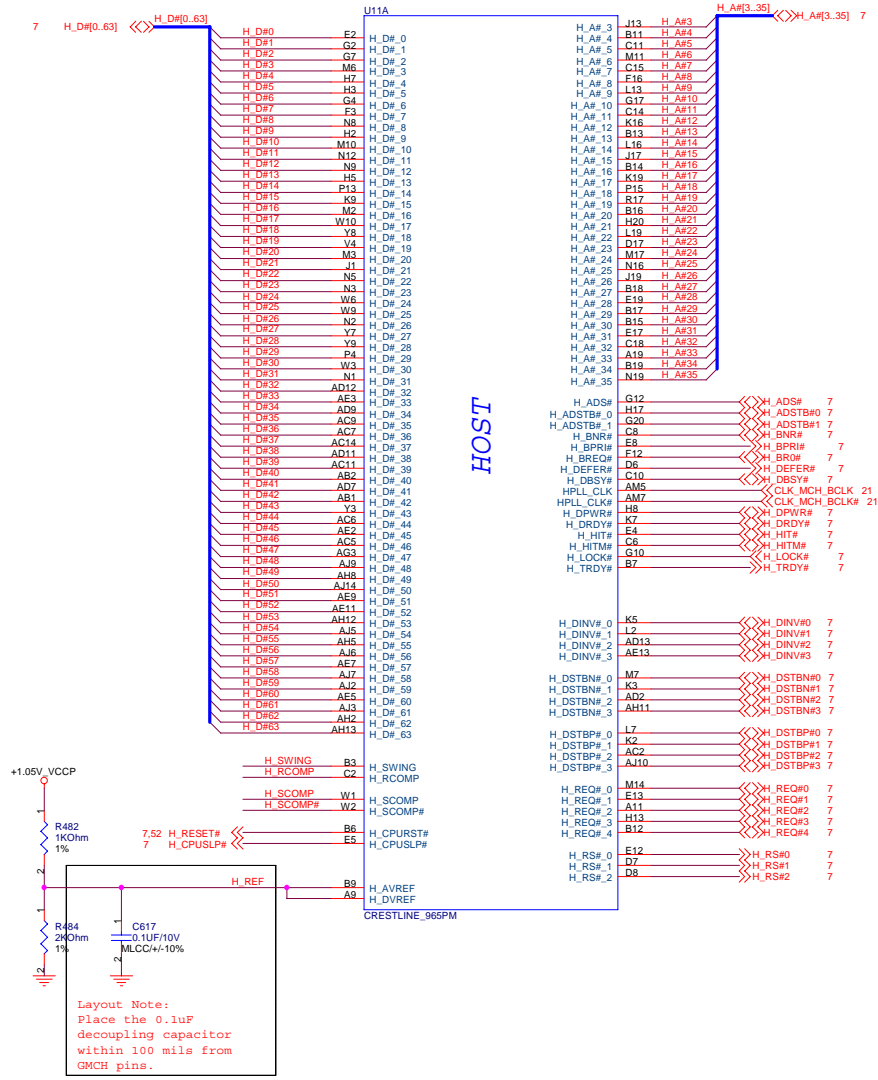
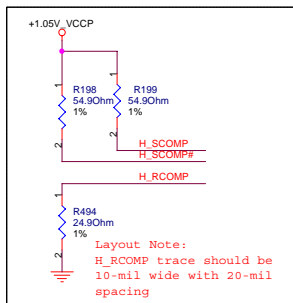
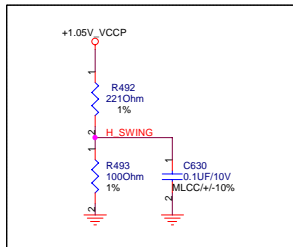
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

<Variant Name>



<Variant Name>





«Variant Name»



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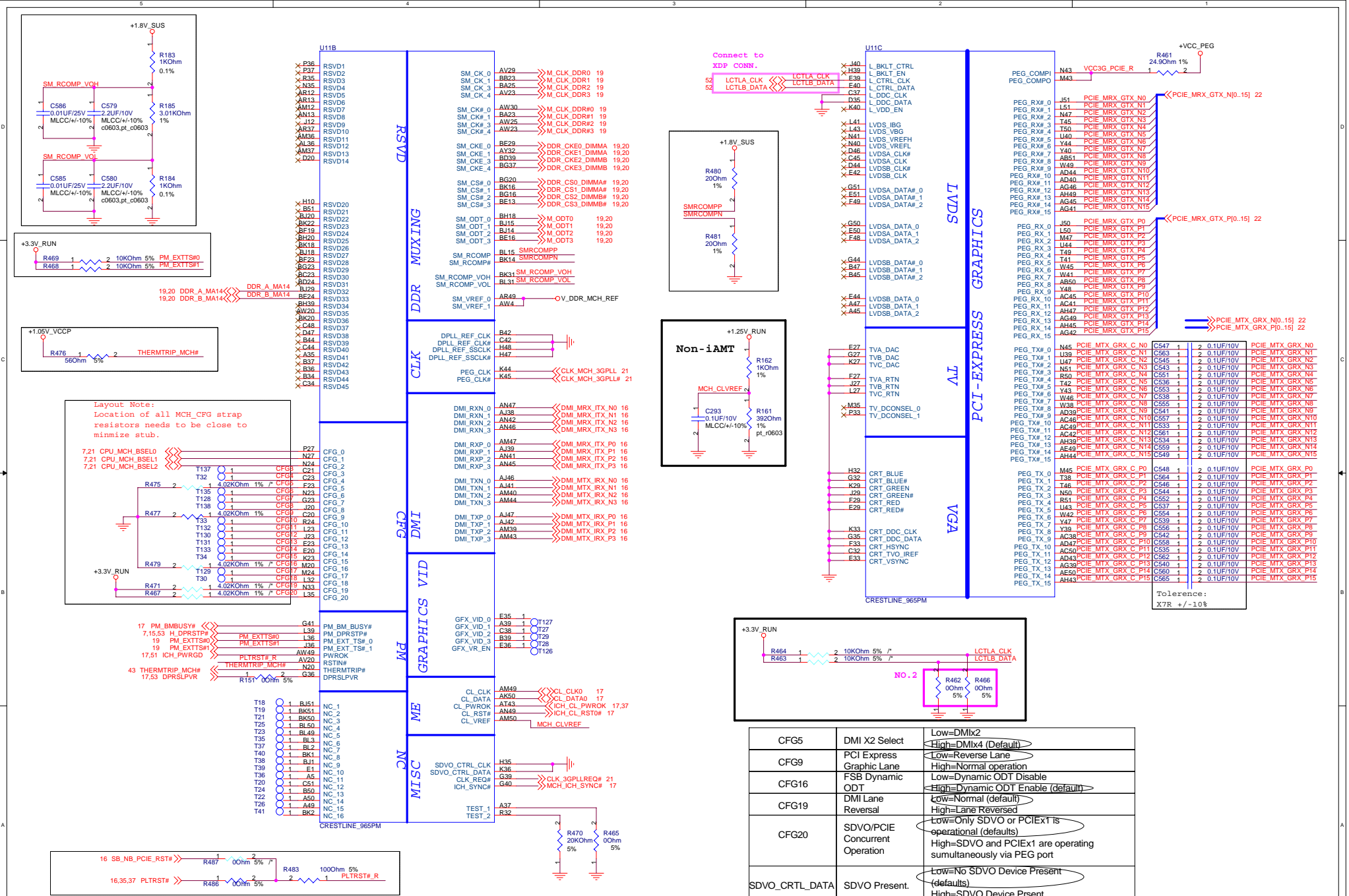
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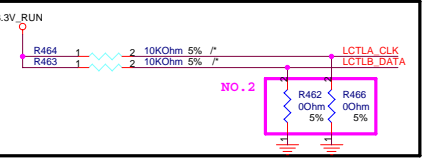
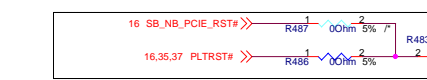
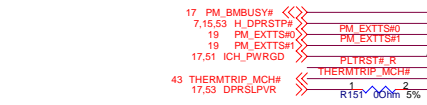
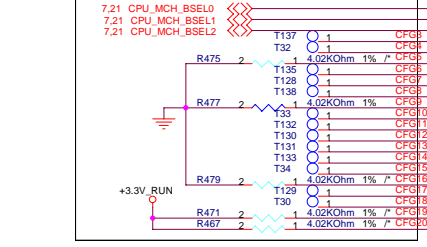
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Crestline (HOST)

SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

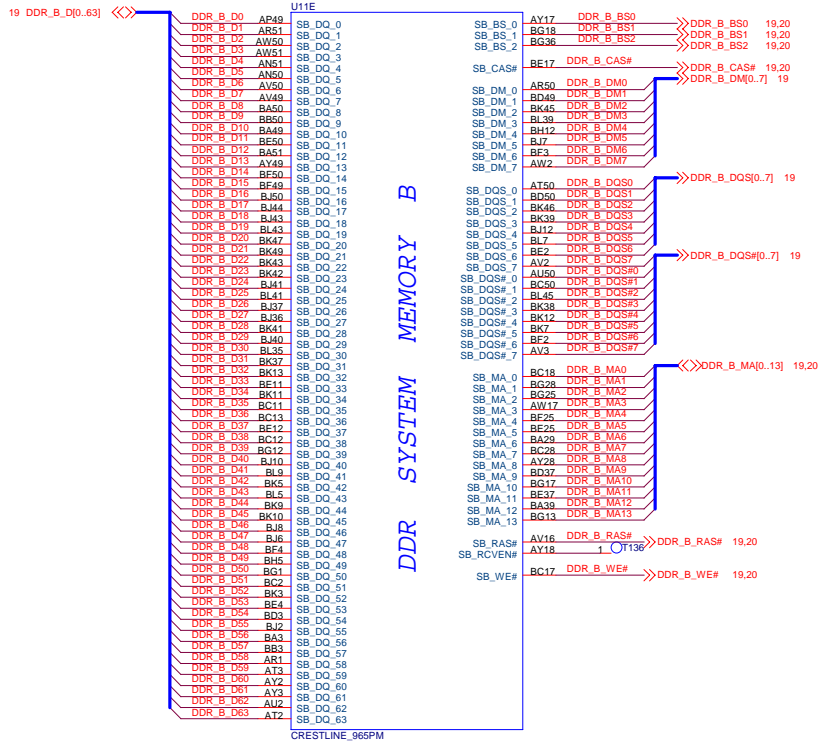
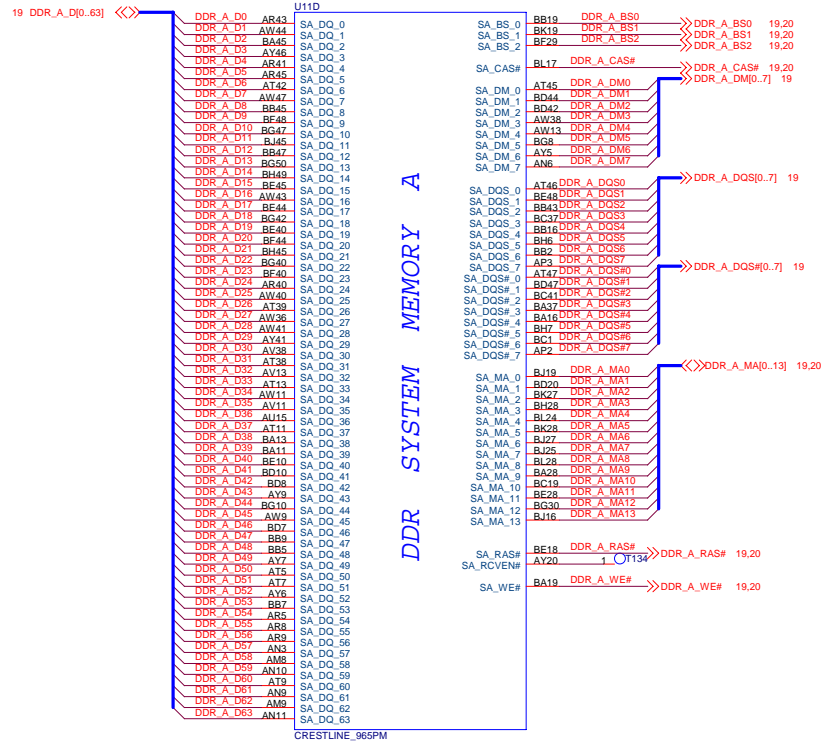
DESIGN ENGINEER:  
Ivan Chou



**Layout Note:**  
Location of all MCH\_CFG strap resistors needs to be close to minimize stub.



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIE1 is operational (defaults) High=SDVO and PCIE1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (defaults) High=SDVO Device Present



Variant Name:



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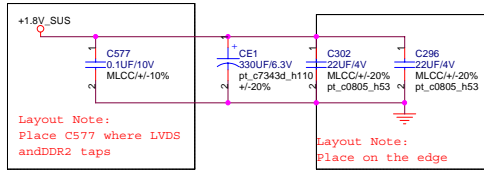
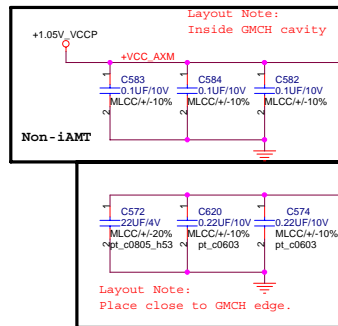
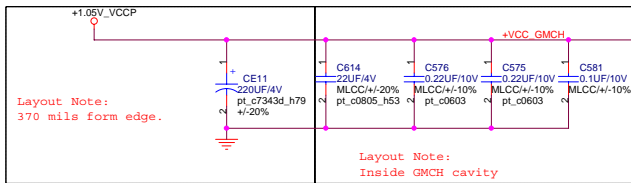
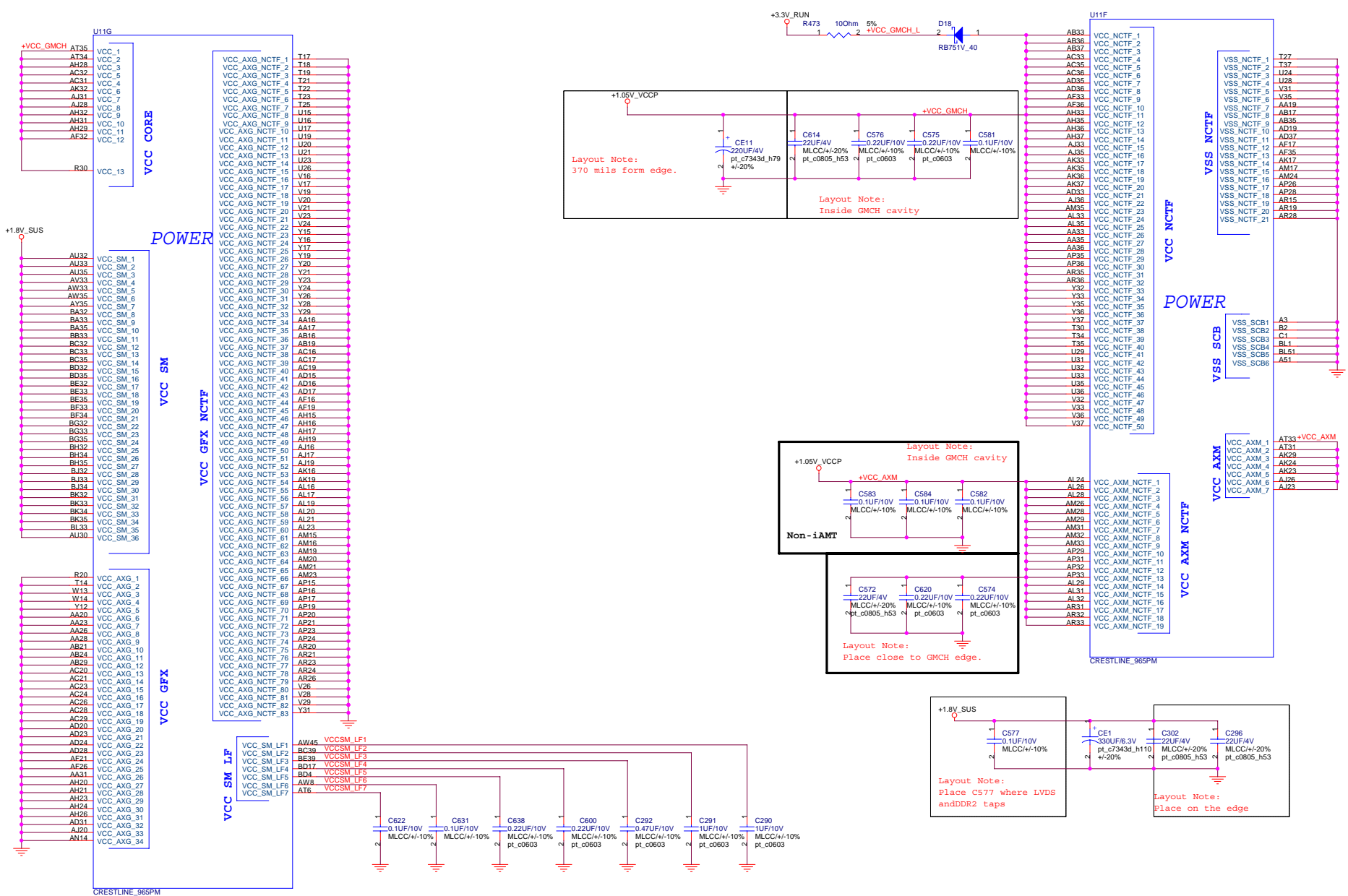
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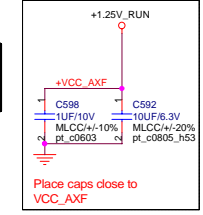
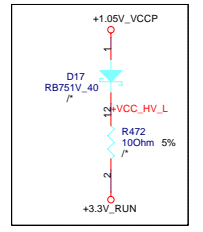
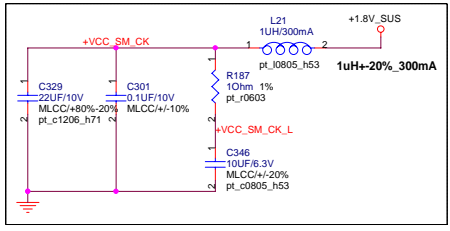
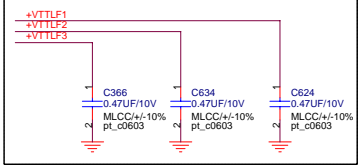
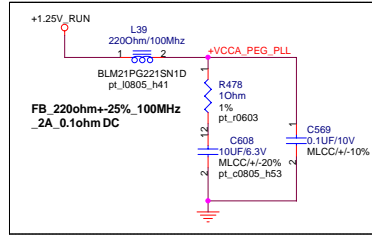
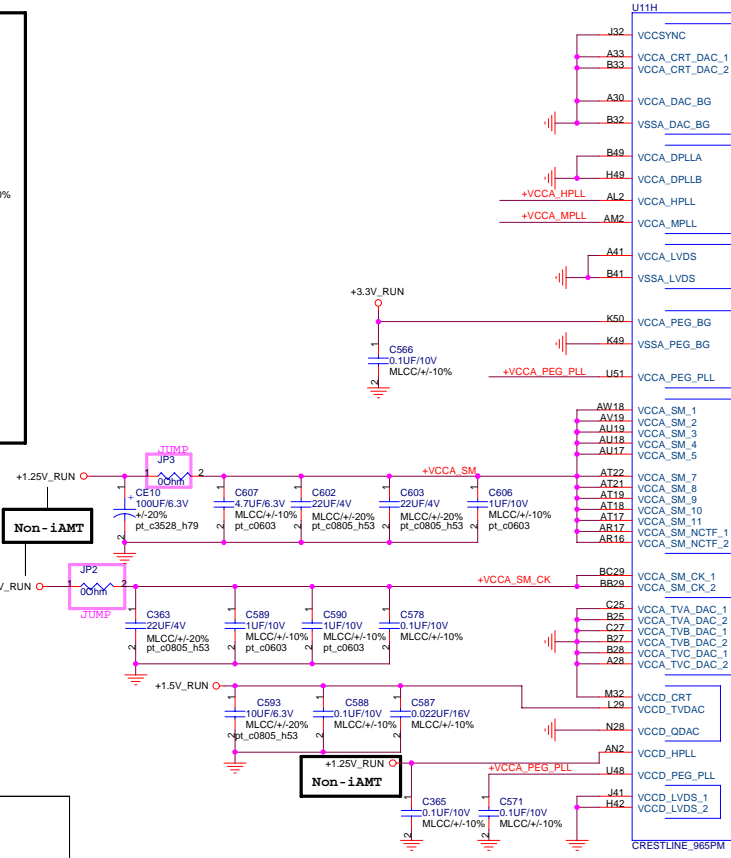
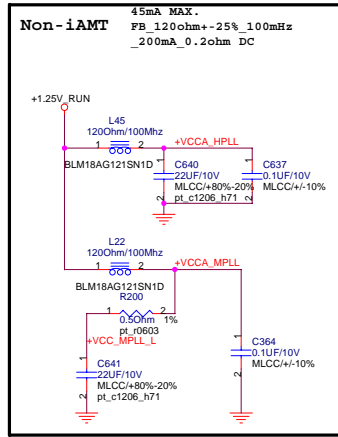
DATE: Monday, March 19, 2007  
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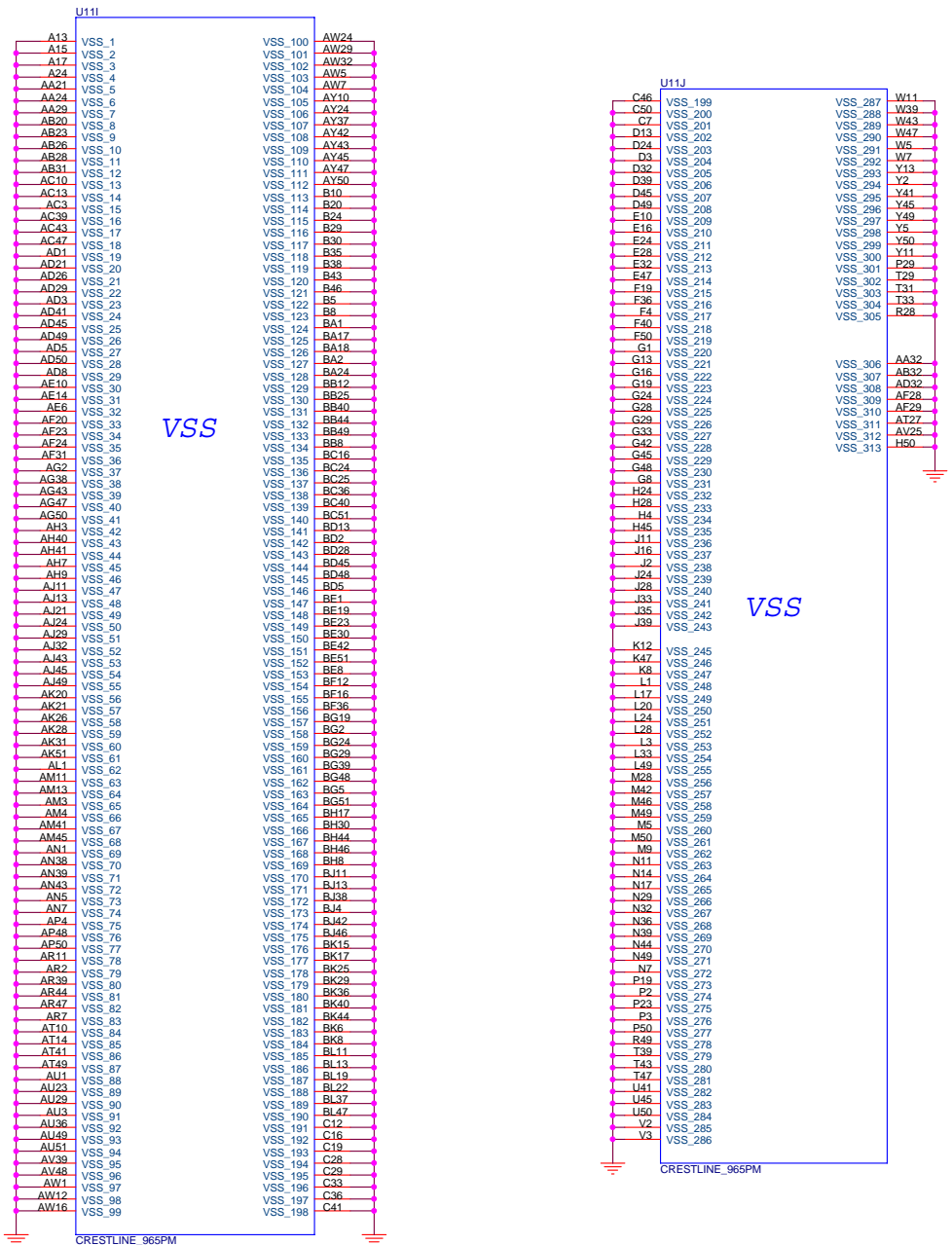
DESCRIPTION: Crestline (DDR2)

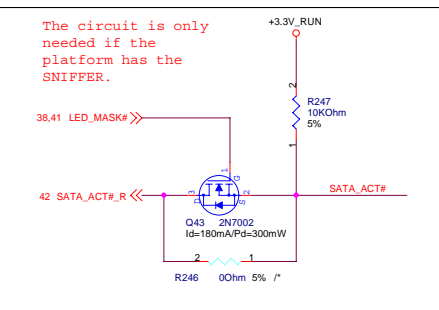
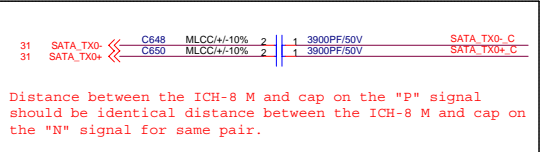
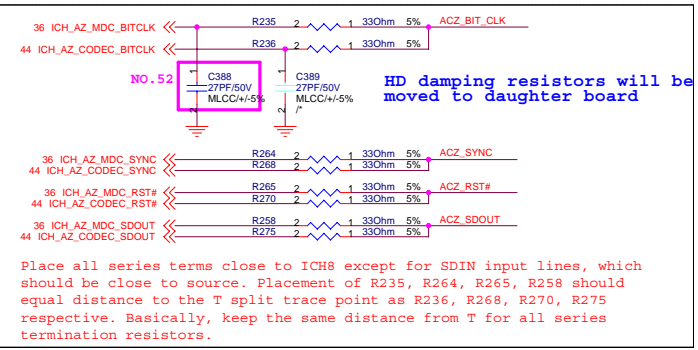
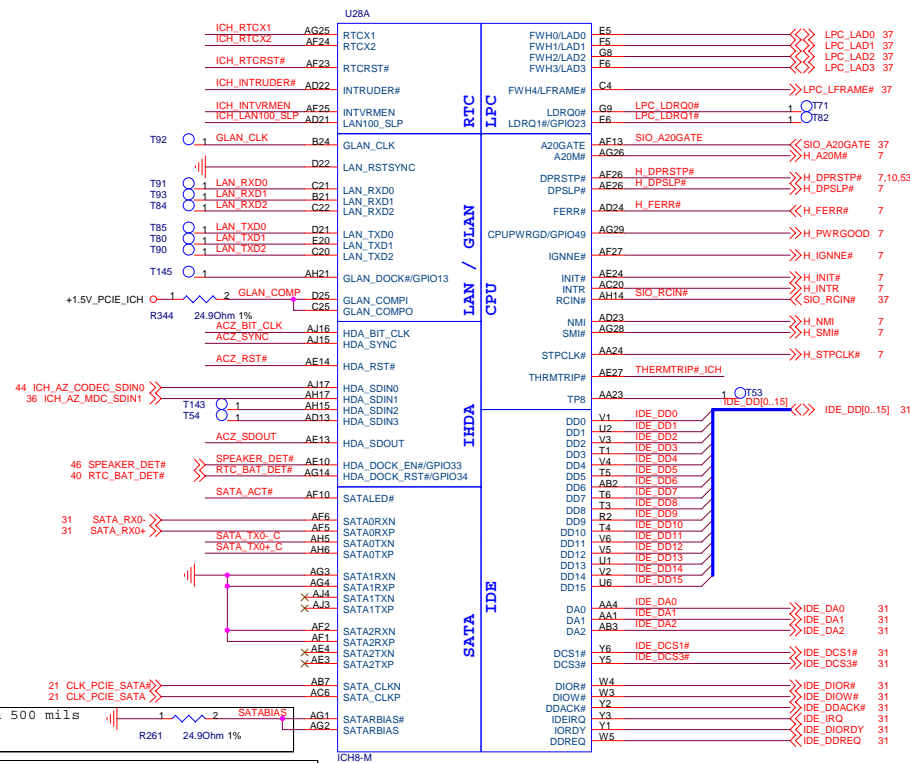
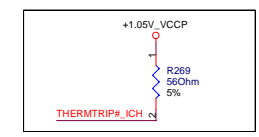
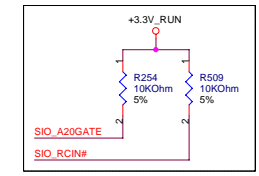
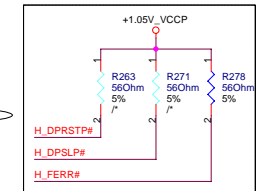
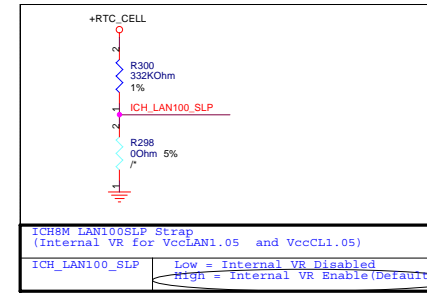
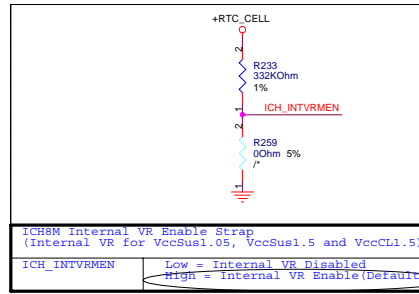
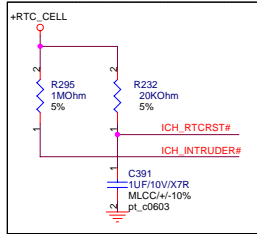
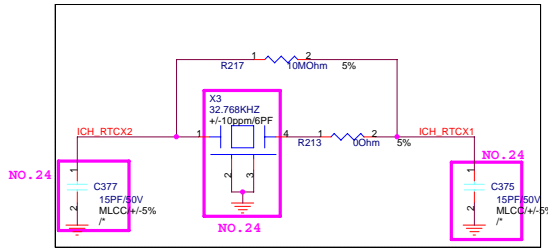
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 RELEASE DATE:

DESIGN ENGINEER: Ivan Chou





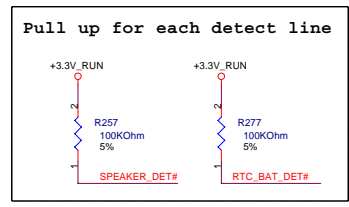


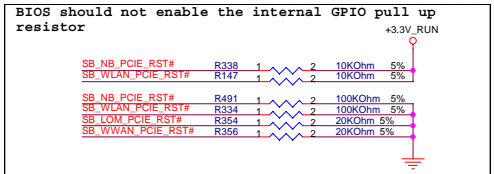
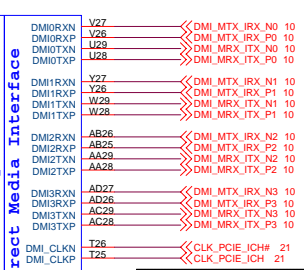
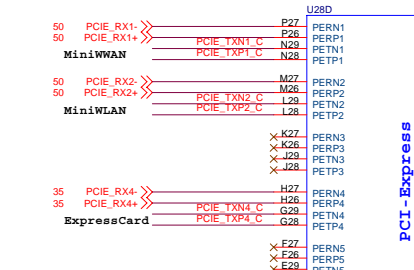
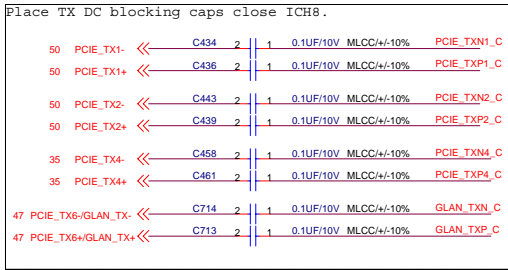


Place within 500 mils of ICH8 ball

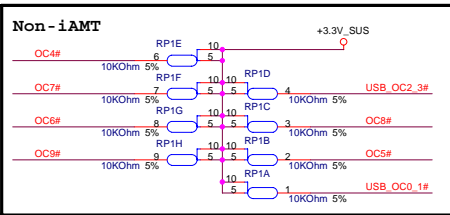
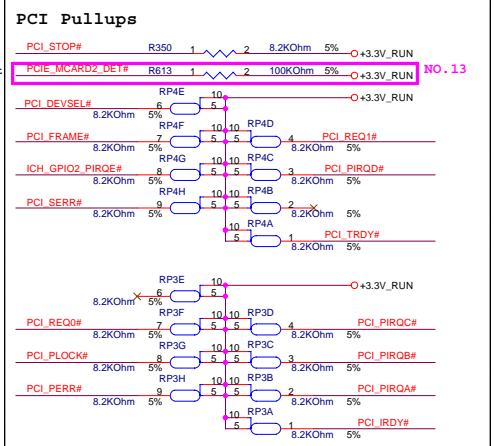
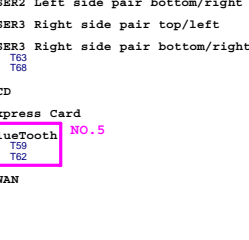
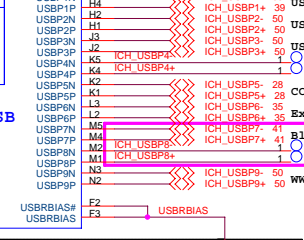
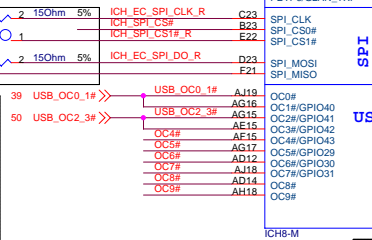
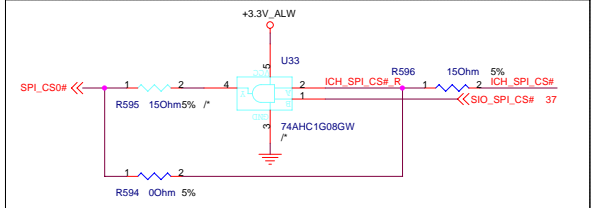
XOR Chain Entrance strap

ICH_RSVD	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR chain
1	0	Normal operation (Default)
1	1	Set PCIE port config bit 1

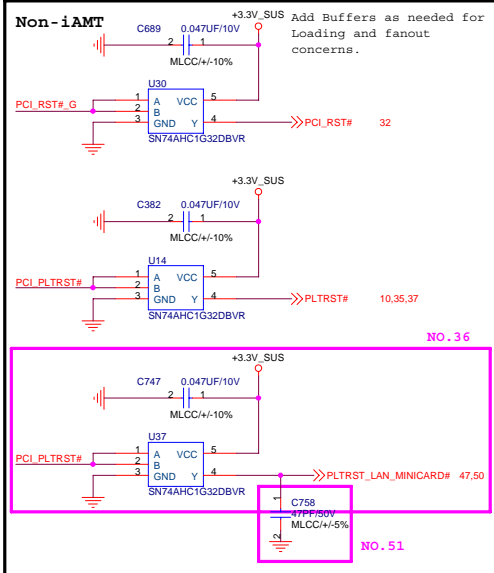
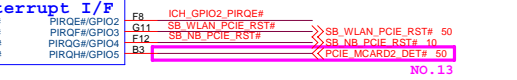
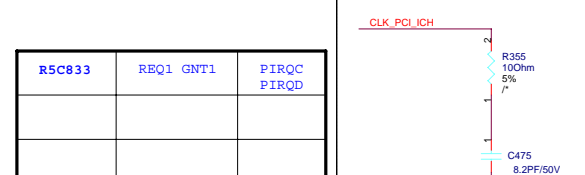
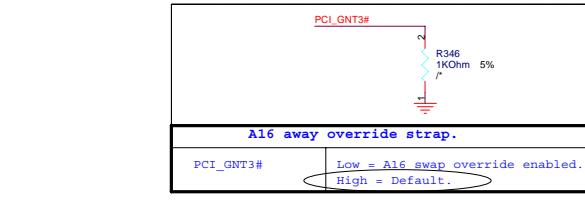
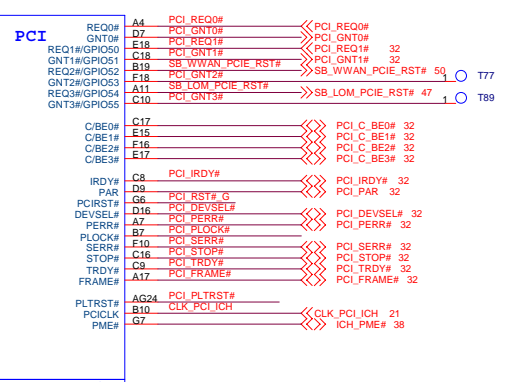
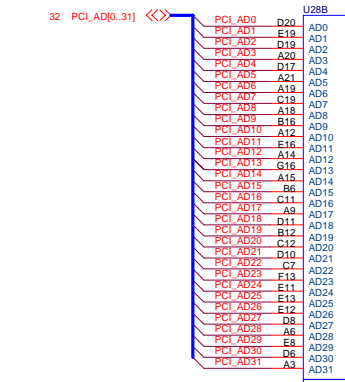
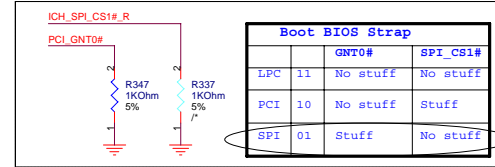




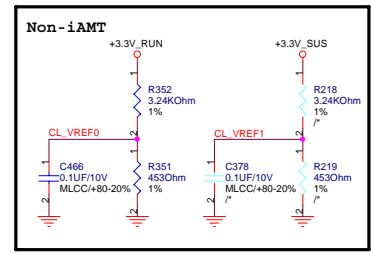
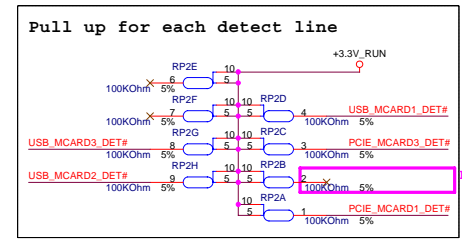
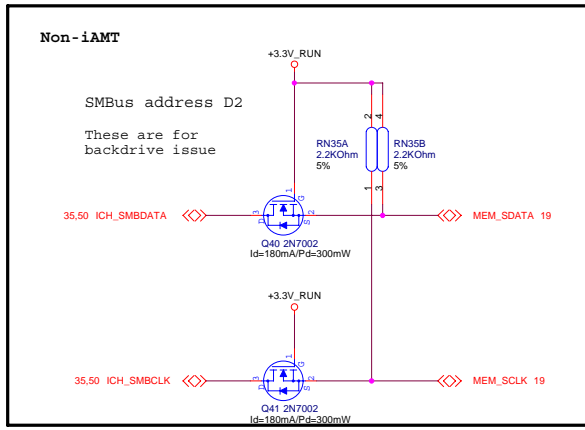
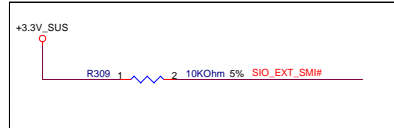
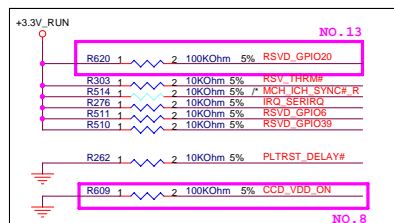
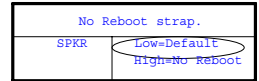
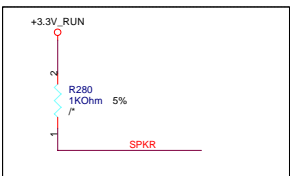
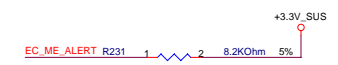
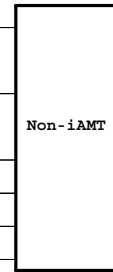
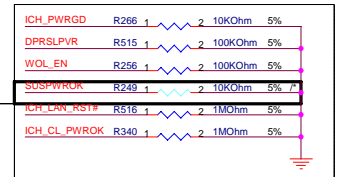
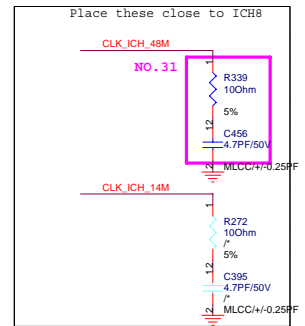
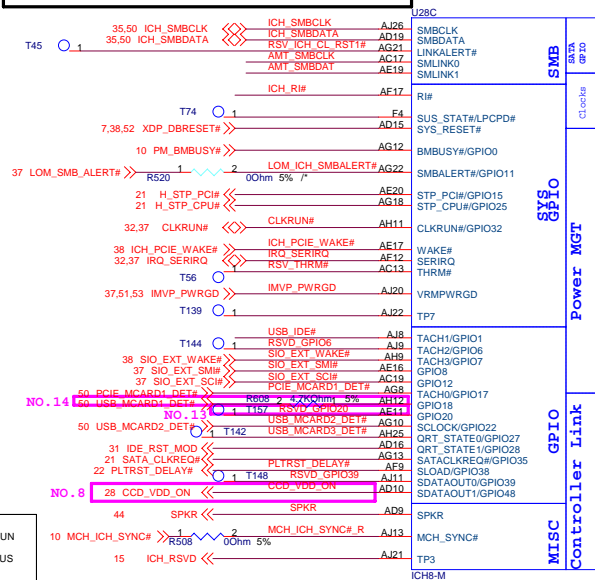
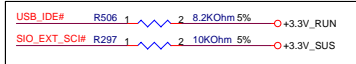
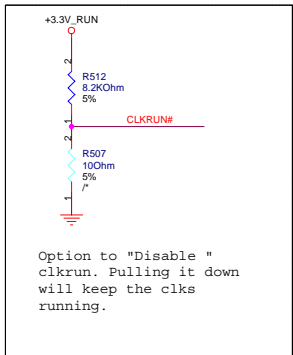
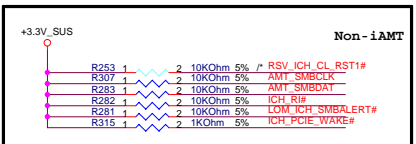
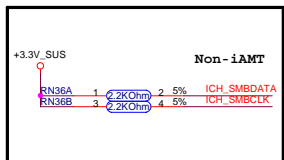
Layout Note:  
Place 15 ohm within  
500 mils from ICH.

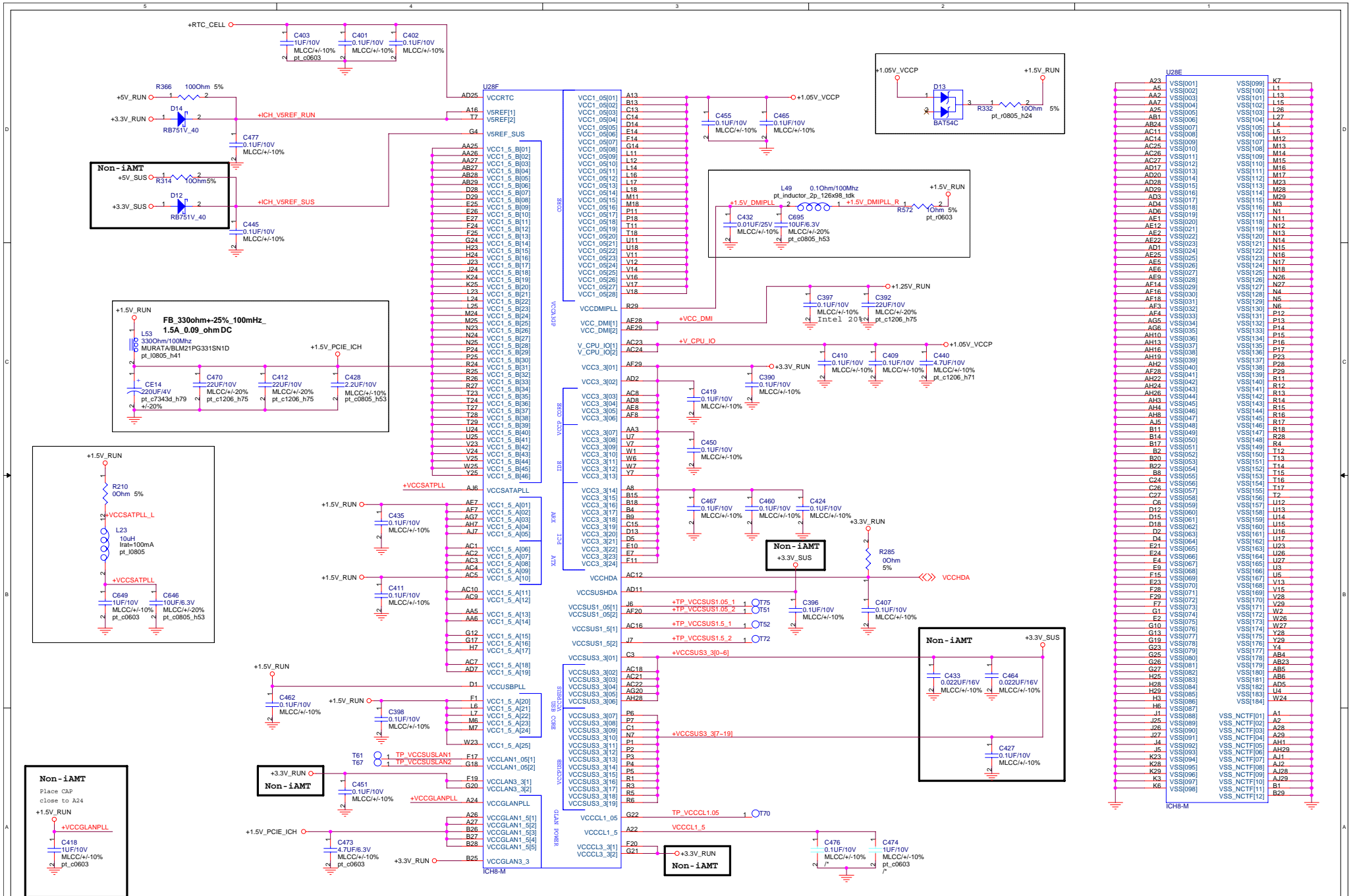


Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.



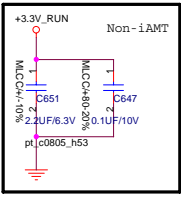
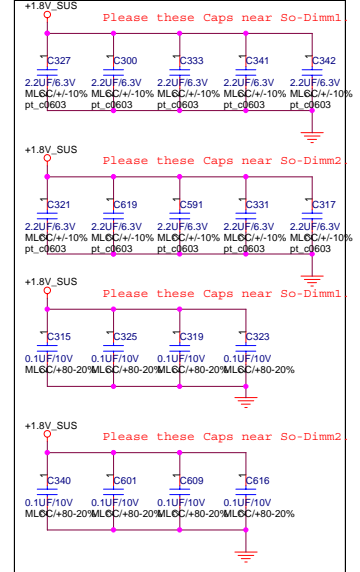
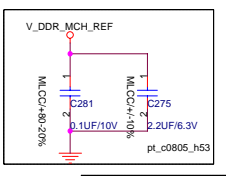
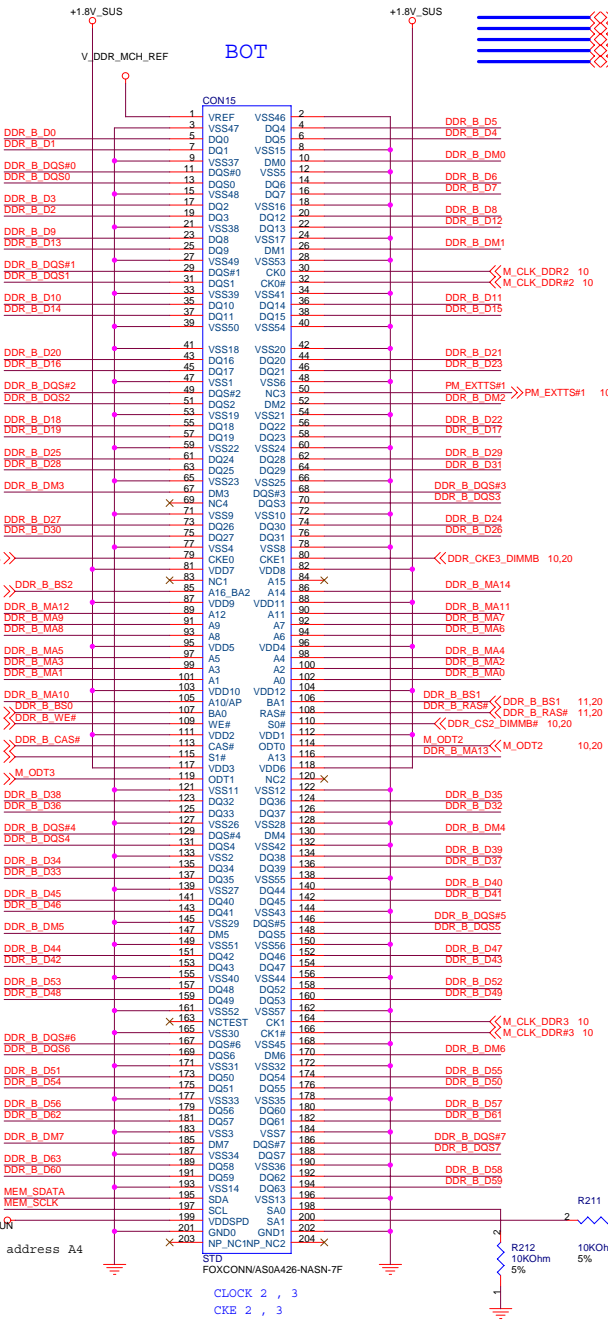
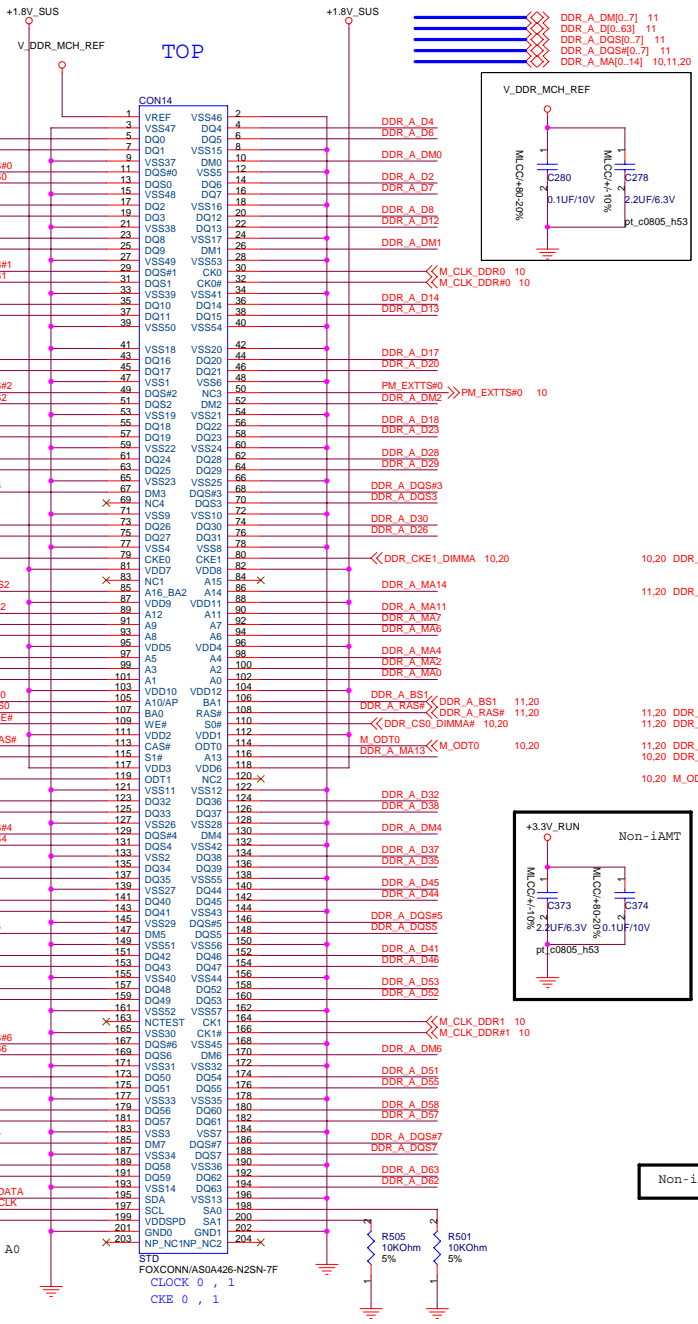


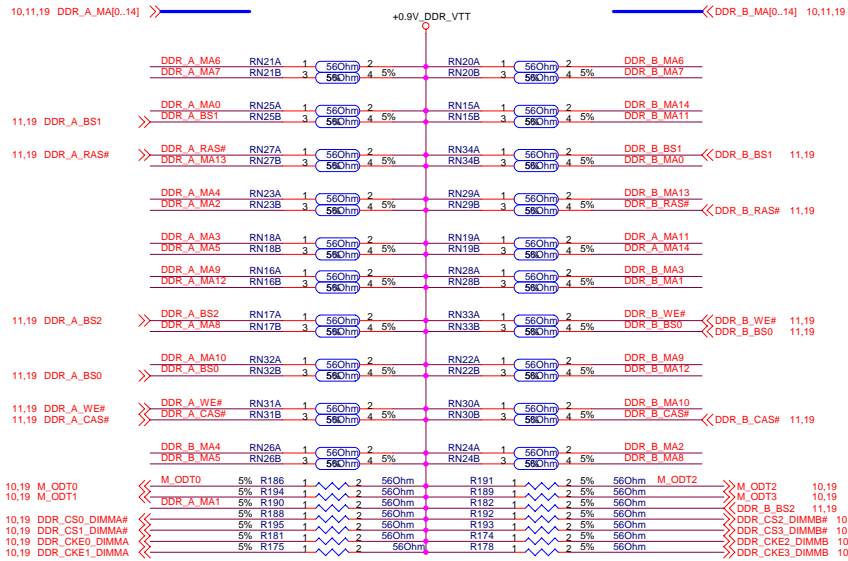
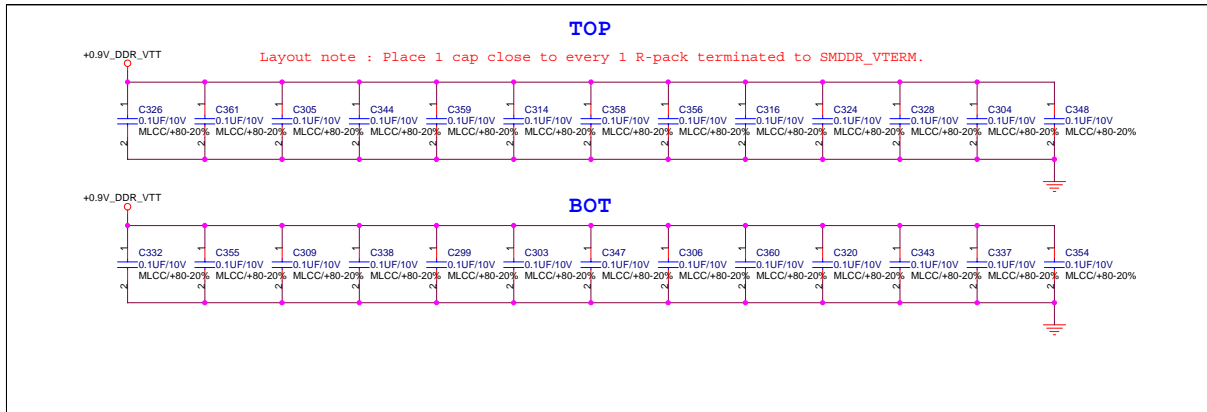




ICH8-M		
A23	VSS0001	VSS0001
A5	VSS0002	VSS0002
A27	VSS0003	VSS0003
A25	VSS0004	VSS0004
A21	VSS0005	VSS0005
AB1	VSS0006	VSS0006
AB24	VSS0007	VSS0007
AC11	VSS0008	VSS0008
AC14	VSS0009	VSS0009
AC25	VSS0010	VSS0010
AC26	VSS0011	VSS0011
AC27	VSS0012	VSS0012
AD17	VSS0013	VSS0013
AD28	VSS0014	VSS0014
AD33	VSS0015	VSS0015
AD29	VSS0016	VSS0016
AD3	VSS0017	VSS0017
AD4	VSS0018	VSS0018
AD6	VSS0019	VSS0019
AE1	VSS0020	VSS0020
AE12	VSS0021	VSS0021
AE22	VSS0022	VSS0022
AD1	VSS0023	VSS0023
AE25	VSS0024	VSS0024
AE5	VSS0025	VSS0025
AE6	VSS0026	VSS0026
AE9	VSS0027	VSS0027
AE14	VSS0028	VSS0028
AE16	VSS0029	VSS0029
AE18	VSS0030	VSS0030
AE13	VSS0031	VSS0031
AE4	VSS0032	VSS0032
AE5	VSS0033	VSS0033
AG6	VSS0034	VSS0034
AH10	VSS0035	VSS0035
AH13	VSS0036	VSS0036
AH19	VSS0037	VSS0037
AH2	VSS0038	VSS0038
AE28	VSS0039	VSS0039
AH22	VSS0040	VSS0040
AH24	VSS0041	VSS0041
AH26	VSS0042	VSS0042
AH3	VSS0043	VSS0043
AH4	VSS0044	VSS0044
AH5	VSS0045	VSS0045
AH6	VSS0046	VSS0046
AH7	VSS0047	VSS0047
AH8	VSS0048	VSS0048
AH9	VSS0049	VSS0049
B14	VSS0050	VSS0050
B17	VSS0051	VSS0051
B2	VSS0052	VSS0052
B20	VSS0053	VSS0053
B22	VSS0054	VSS0054
B23	VSS0055	VSS0055
B24	VSS0056	VSS0056
C27	VSS0057	VSS0057
CB	VSS0058	VSS0058
D12	VSS0059	VSS0059
D18	VSS0060	VSS0060
D4	VSS0061	VSS0061
D2	VSS0062	VSS0062
E21	VSS0063	VSS0063
E24	VSS0064	VSS0064
E4	VSS0065	VSS0065
E9	VSS0066	VSS0066
F15	VSS0067	VSS0067
F23	VSS0068	VSS0068
F28	VSS0069	VSS0069
F29	VSS0070	VSS0070
F7	VSS0071	VSS0071
G1	VSS0072	VSS0072
E2	VSS0073	VSS0073
G10	VSS0074	VSS0074
G13	VSS0075	VSS0075
G19	VSS0076	VSS0076
G23	VSS0077	VSS0077
G25	VSS0078	VSS0078
G26	VSS0079	VSS0079
G27	VSS0080	VSS0080
H25	VSS0081	VSS0081
H28	VSS0082	VSS0082
H3	VSS0083	VSS0083
H6	VSS0084	VSS0084
H9	VSS0085	VSS0085
H2	VSS0086	VSS0086
J1	VSS0087	VSS0087
J2	VSS0088	VSS0088
J5	VSS0089	VSS0089
J7	VSS0090	VSS0090
J27	VSS0091	VSS0091
J4	VSS0092	VSS0092
J5	VSS0093	VSS0093
K23	VSS0094	VSS0094
K28	VSS0095	VSS0095
K29	VSS0096	VSS0096
K3	VSS0097	VSS0097
K6	VSS0098	VSS0098
K7	VSS0099	VSS0099
L1	VSS0100	VSS0100
L16	VSS0101	VSS0101
L26	VSS0102	VSS0102
L4	VSS0103	VSS0103
L7	VSS0104	VSS0104
L5	VSS0105	VSS0105
M12	VSS0106	VSS0106
M13	VSS0107	VSS0107
M14	VSS0108	VSS0108
M15	VSS0109	VSS0109
M16	VSS0110	VSS0110
M17	VSS0111	VSS0111
M23	VSS0112	VSS0112
M28	VSS0113	VSS0113
M29	VSS0114	VSS0114
M3	VSS0115	VSS0115
N1	VSS0116	VSS0116
N11	VSS0117	VSS0117
N12	VSS0118	VSS0118
N13	VSS0119	VSS0119
N14	VSS0120	VSS0120
N15	VSS0121	VSS0121
N16	VSS0122	VSS0122
N17	VSS0123	VSS0123
N18	VSS0124	VSS0124
N26	VSS0125	VSS0125
N27	VSS0126	VSS0126
N4	VSS0127	VSS0127
N5	VSS0128	VSS0128
N6	VSS0129	VSS0129
N6	VSS0130	VSS0130
P12	VSS0131	VSS0131
P13	VSS0132	VSS0132
P14	VSS0133	VSS0133
P15	VSS0134	VSS0134
P16	VSS0135	VSS0135
P17	VSS0136	VSS0136
P23	VSS0137	VSS0137
P28	VSS0138	VSS0138
P29	VSS0139	VSS0139
R11	VSS0140	VSS0140
R13	VSS0141	VSS0141
R14	VSS0142	VSS0142
R15	VSS0143	VSS0143
R16	VSS0144	VSS0144
R17	VSS0145	VSS0145
R18	VSS0146	VSS0146
R2	VSS0147	VSS0147
R4	VSS0148	VSS0148
R12	VSS0149	VSS0149
T12	VSS0150	VSS0150
T14	VSS0151	VSS0151
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T2	VSS0193	VSS0193
T2	VSS0194	VSS0194
T2	VSS0195	VSS0195
T2	VSS0196	VSS0196
T2	VSS0197	VSS0197
T2	VSS0198	VSS0198
T2	VSS0199	VSS0199
T2	VSS0200	VSS0200

A is required to route to Top SODIMM for AMT to function Ch.A SODIMM needs to be populated for Intel AMT support.

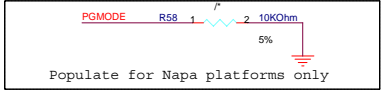
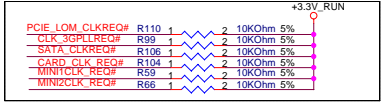
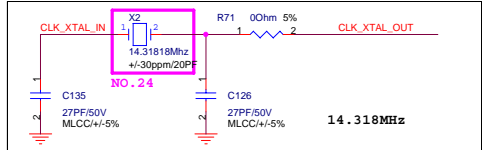
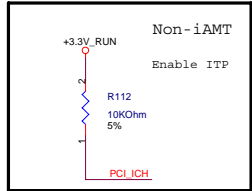
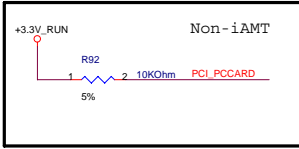
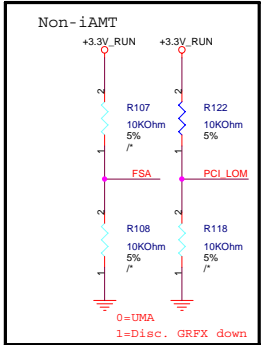




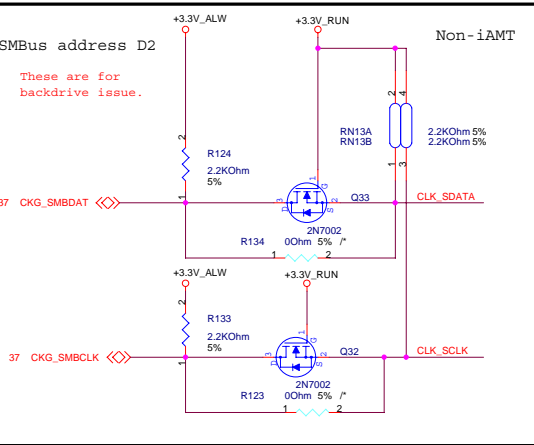
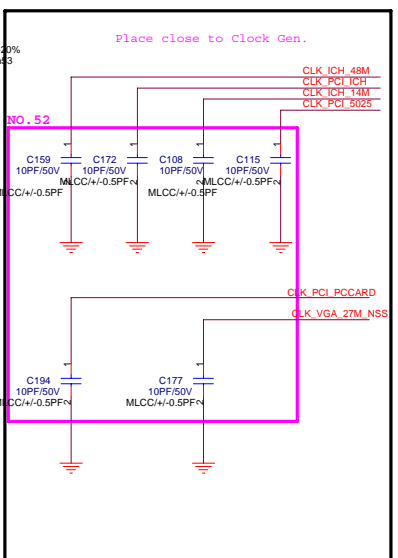
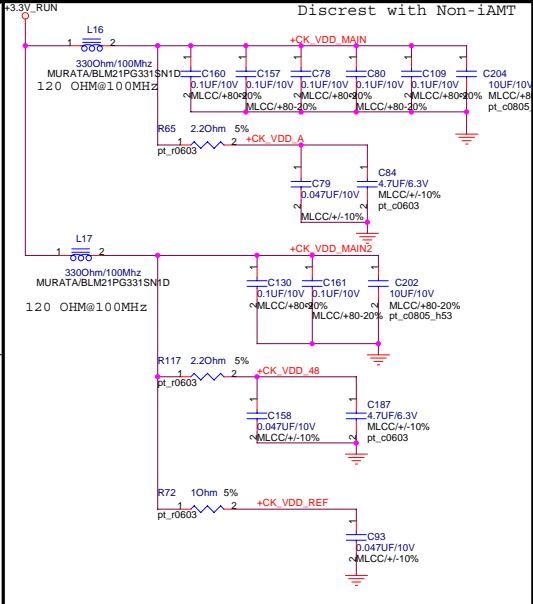
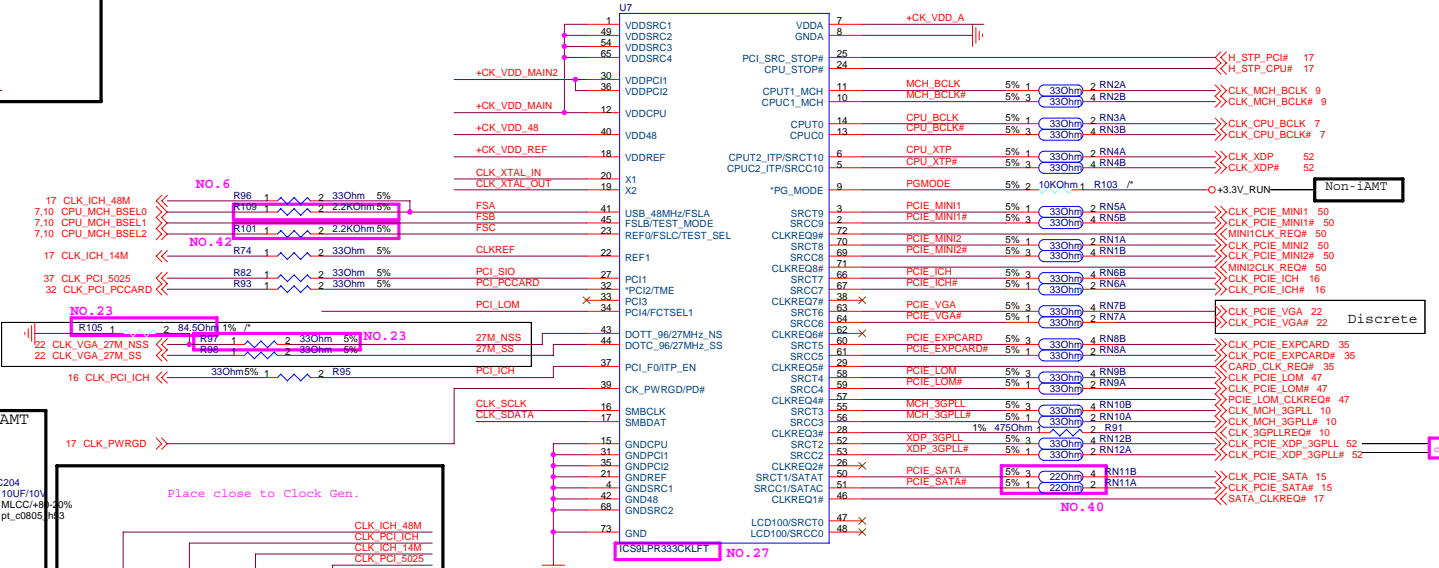
Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

<Variant Name>

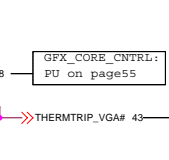
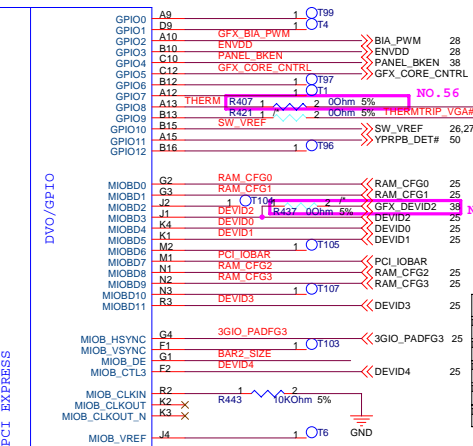
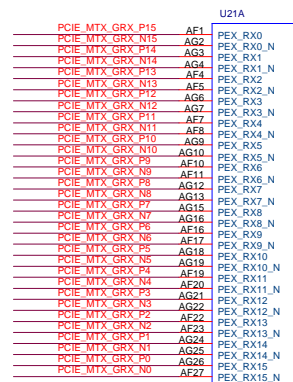
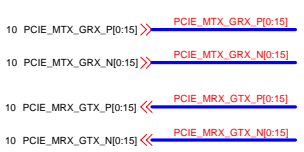


CLK_VGA_27M_NSS (VGA XTALIN) OPTION		
	G7X	NB8X
R97	147ohm	33 ohm
R105	84.5 ohm	no-stuf
clk. voltage	1.2V	3.3V



FSC	F5B	F5A	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM=FCTSEL1				
FCTSEL1 (PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M T	96/100M C
1 = Disc.	27Mout	27M SSout	SRCT0	SRCC0
GRFX down				

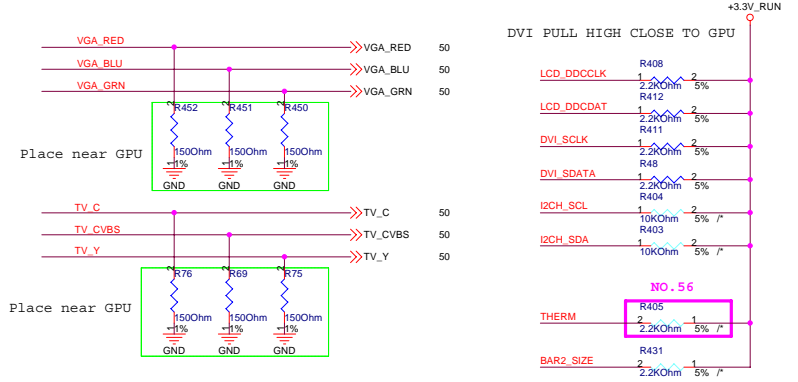
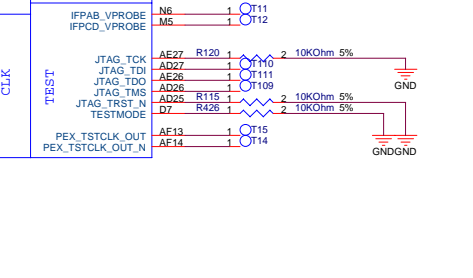
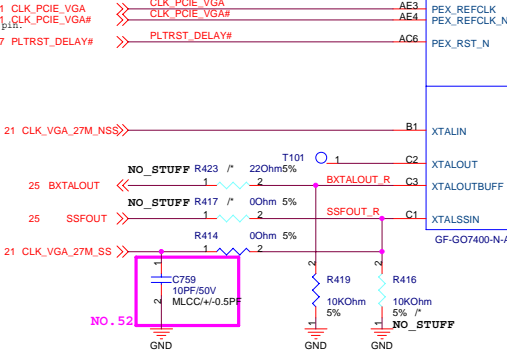
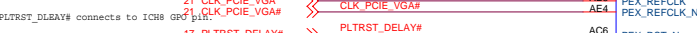
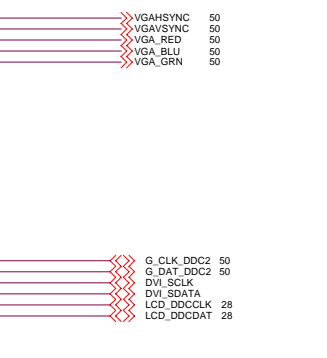
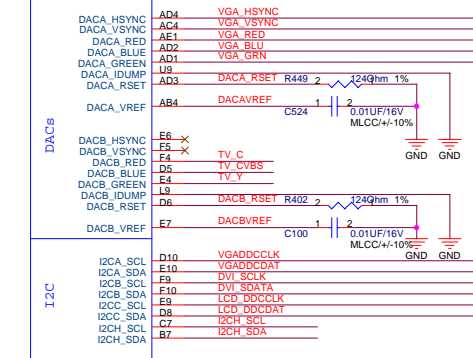
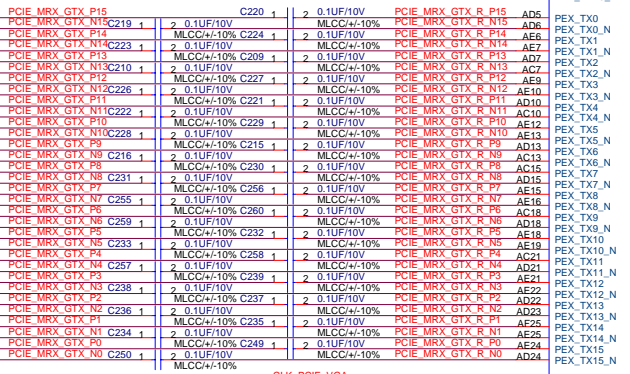
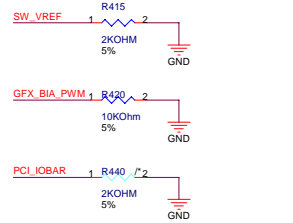


Pop	R421,R405	R407
De-pop	R407	R421,R405

Note: Populate R421 for the platform that use internal G72 Thermal Sensor

	G72M	G8XM	DEFAULT	STRAP
MI0B2	CRYSTAL0	CRYSTAL	0	NOT REQUIRED
MI0B6	CRYSTAL1	TVMODE2	0	NOT REQUIRED
MI0B_HS_SYNC	-	3GIO_PADFG3	0	NOT REQUIRED
MI0BD7	MI0BLE_GPIO	PC_I0BAR	1	NOT REQUIRED
MI0B_DE	-	BAR2_SIZE	0	NOT REQUIRED

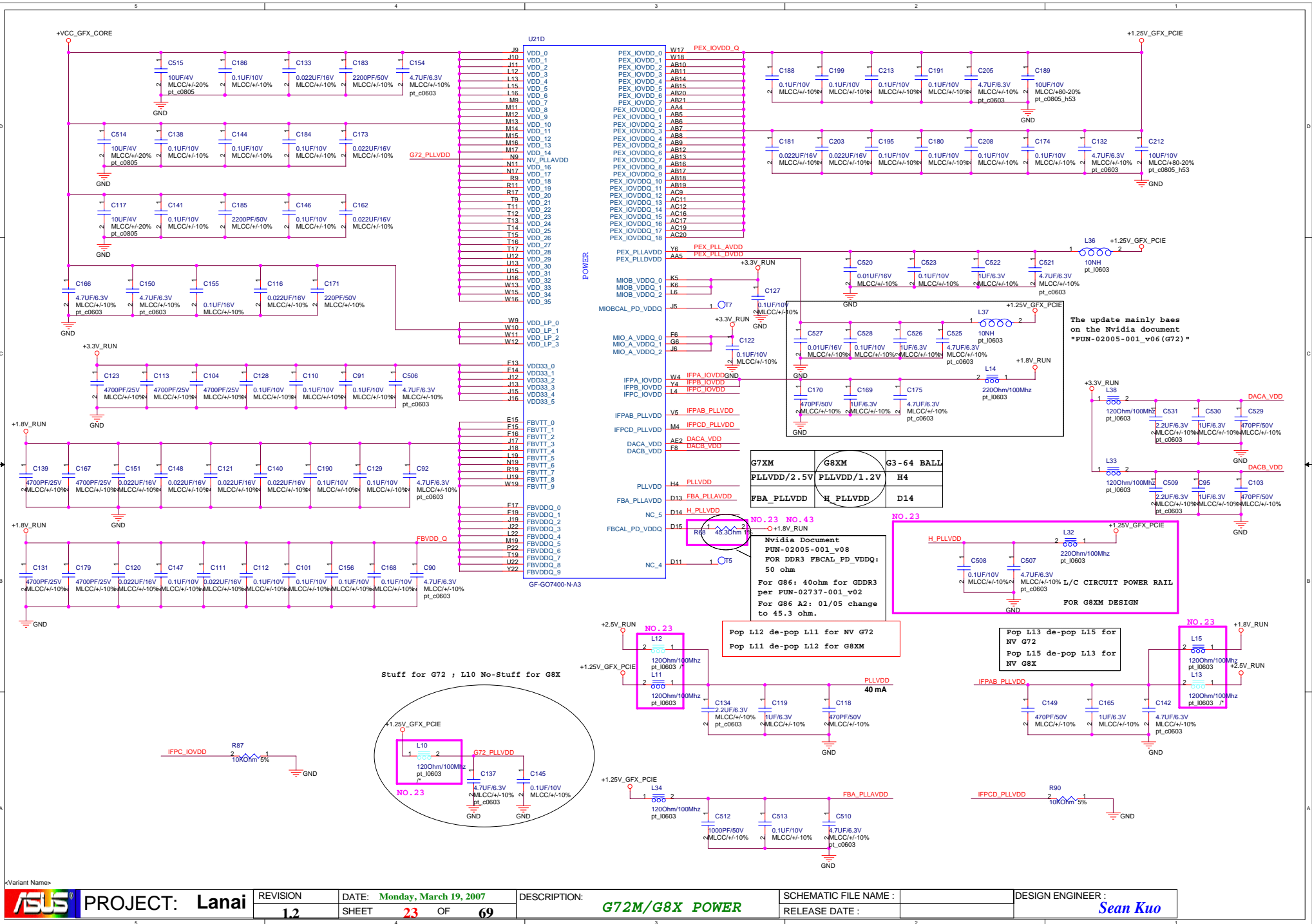
	MI0BD11	MI0BD3	MI0BD5	MI0BD4
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86M	0	1	1	1



	CY28547+SS	CY28547+U5	CY28547 wo/SS
Pop	R414, R419, R98	R423, R417, U5	R416, R419
De-pop	U5, R423, R417, R416	R414, R416, R419, R98	U5, R98, R414, R417, R423

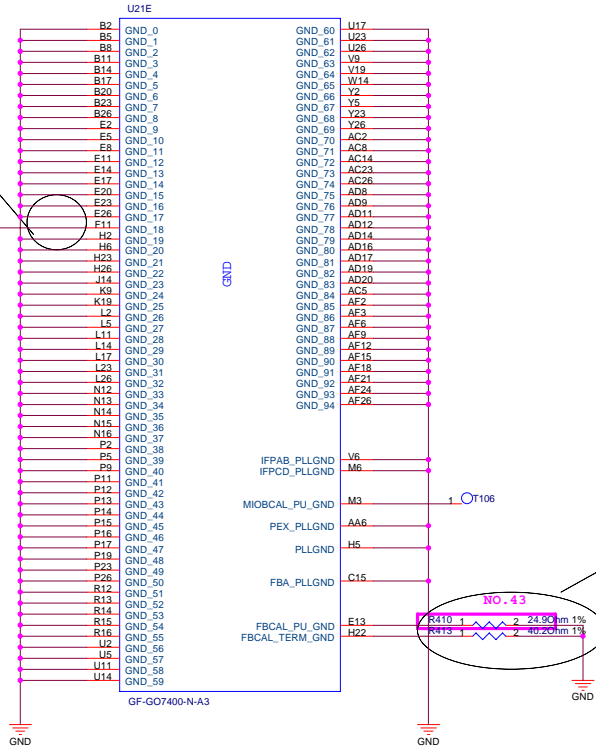
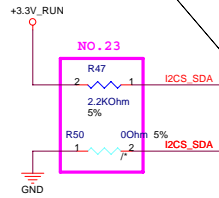
'U5' indicate all ockt.related to U5 in Page.25

Layout comments: Place R423,R419 as close as possible to C3. . Place R414,R416and R417 as close as possible to pin C1.



<Variant Name>

G7XM	G8XM	G3-64 BALL
GND	I2SC_SDA	F11



UPDATE FROM NVIDIA UPDATED NOTIFICATION  
 PUN-02005-001\_v08 (G72)  
 FBCAL\_PU\_GND: 30 OHM  
 FBCAL\_TERM\_GND: 40 OHM  
 01/05 for G86 A2: change R410 to 24.9  
 ohm from 30 ohm

<Variant Name>



PROJECT: Lanai

REVISION  
1.2

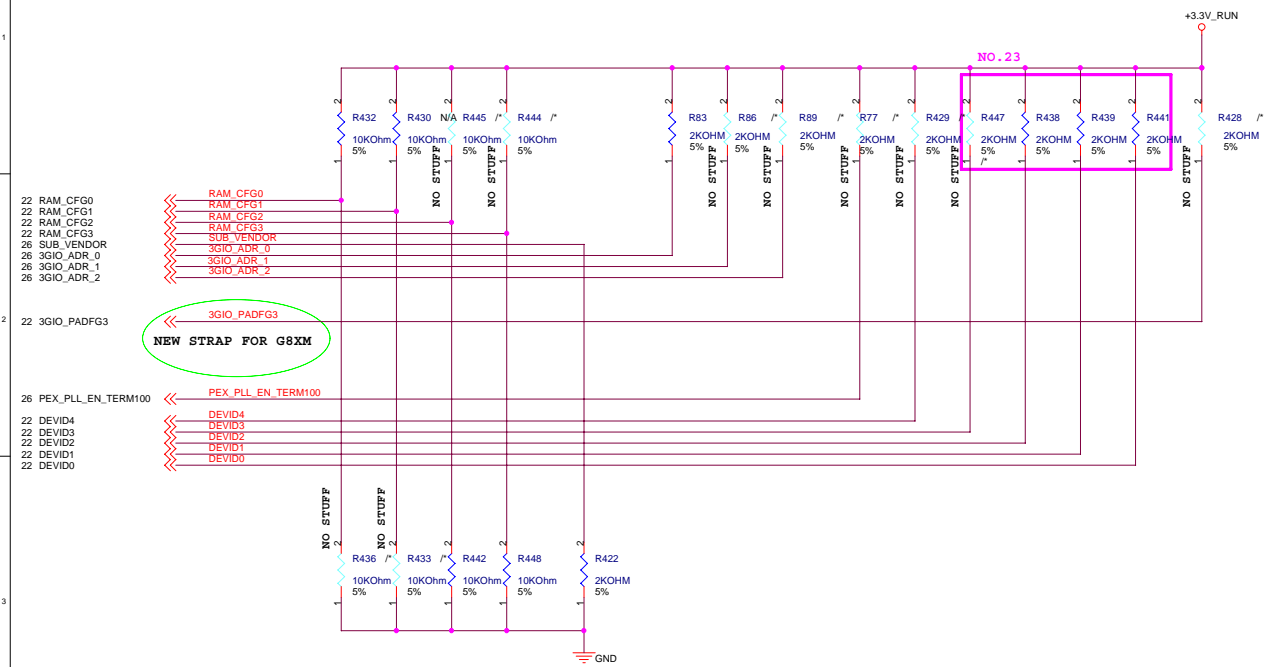
DATE: Monday, March 19, 2007  
 SHEET 24 OF 69

DESCRIPTION:  
G7XM/G8X CORE GND

SCHEMATIC FILE NAME : <OrgName>  
 RELEASE DATE :

DESIGN ENGINEER :  
Sean Kuo



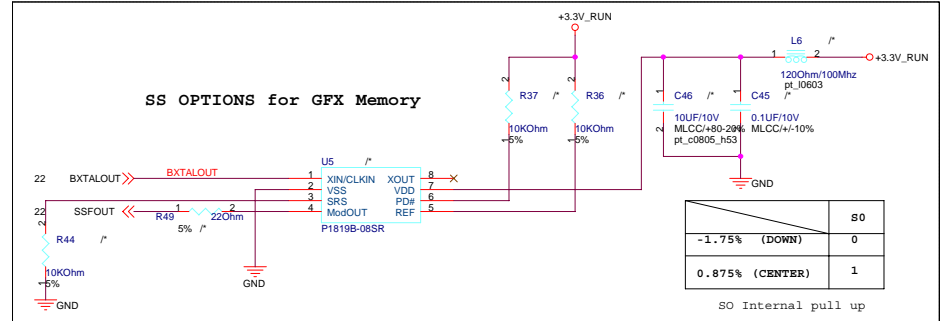


STRAPS	PIN	DESCRIPTION	Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT,Serial SST45VF=10, LPC=11	01
SUB_VENDOR	MIOAD1		0
PEX_PLL_TERM	MIOAD0		0
RAM_CFG[3:0]	FOR GDDR1	8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
		4Mx32 DDR generic (64bit) 1.8V I/O	0100
		4Mx32 DDR generic (32bit) 1.8V I/O	1100
	MIOBD0 MIOBD1 MIOBD8 MIOBD9 FOR GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
		Hynix 8Mx32 500MHz, 1.8V	0111
		Samsung 8Mx32 500MHz, 1.8V	0110
		Infineon 16Mx32 GDDR3 ,1.8V	0001
		Hynix 16Mx32 GDDR3 1.8V	0010
		Samsung 16Mx32 GDDR3 1.8V	0011

**Internal Pull-down**

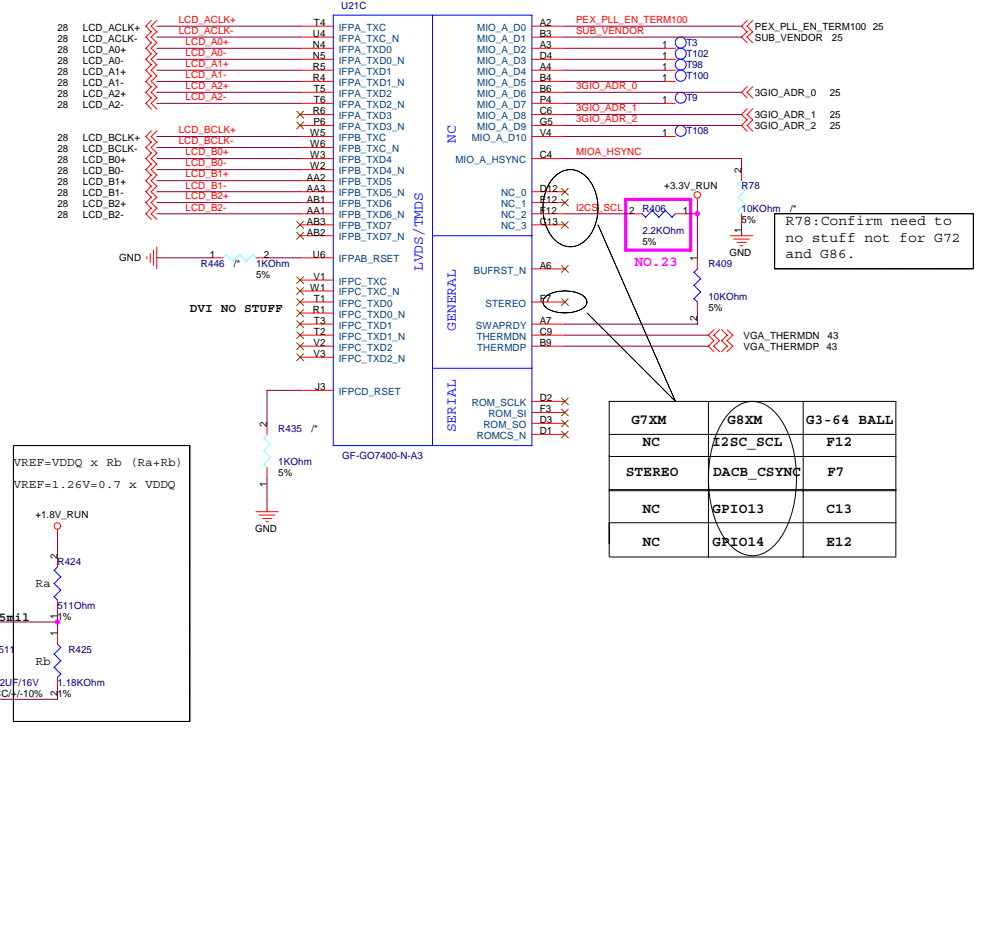
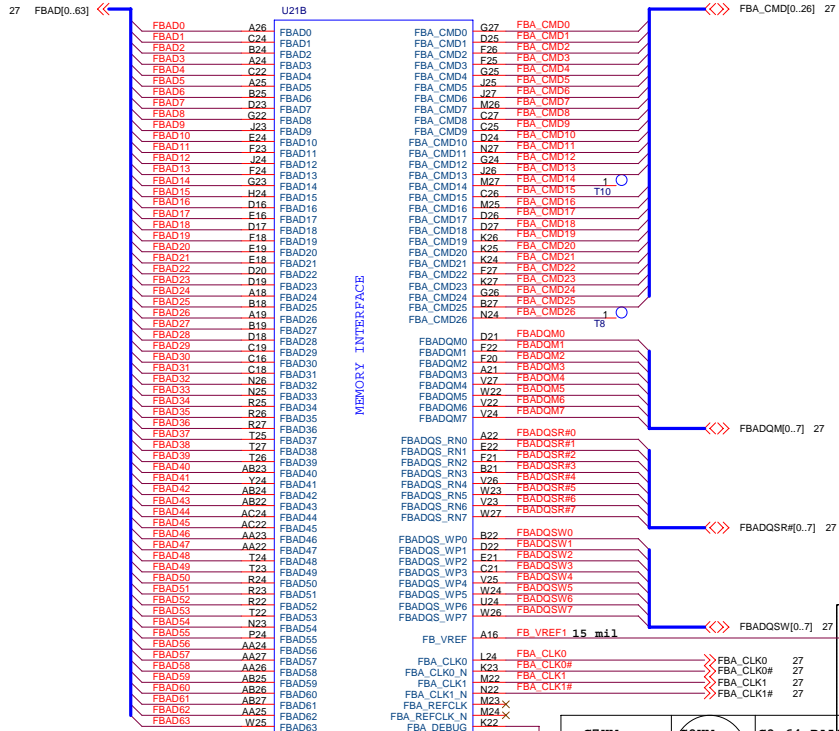
MIOAD0, MIOAD6, MIOAD8, MIOAD9  
MIOAD1----SUB\_VENDOR 0, SYSTEM BIOS  
MIOAD0----PEX\_PLL\_EN\_TERM 0111, G72M  
MIOAD6----3GIO\_ADR\_0 [2:0] 001 for NV43/NV44  
MIOAD8----3GIO\_ADR\_1 010 for G7x, NV42  
MIOAD9----3GIO\_ADR\_2

MIOBD4----PCI\_DEVID0 1000, G72M  
MIOBD5----PCI\_DEVID1 0111, G72MV  
MIOBD3----PCI\_DEVID2  
MIOBD11----PCI\_DEVID3



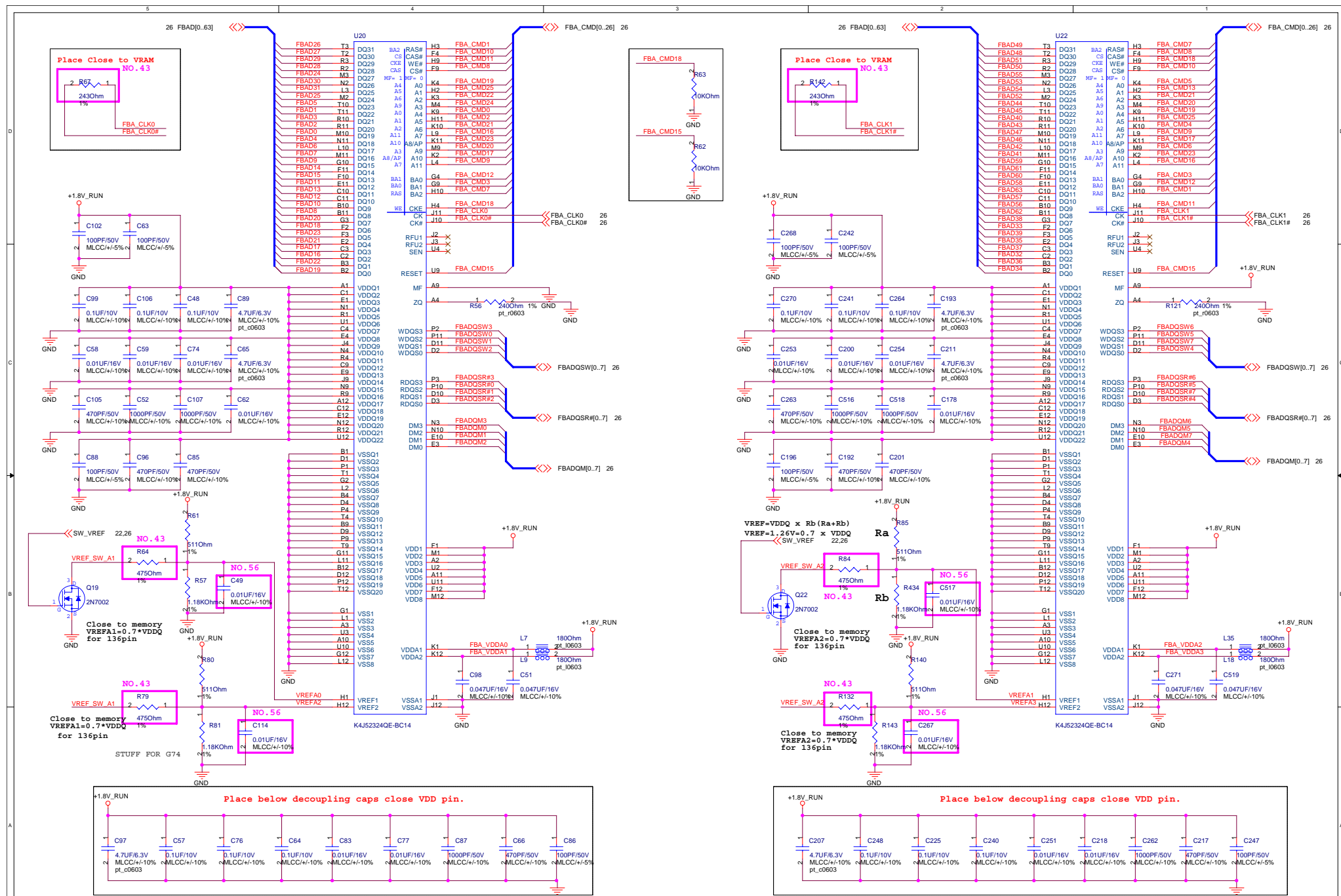
M08 HAS REMOVED THIS PORTION  
INSTALL OR NOT?

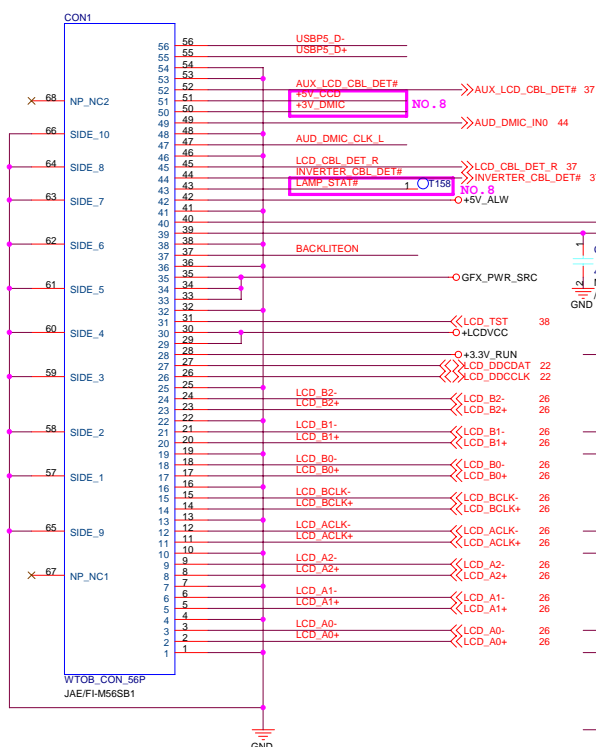
<Variant Name>



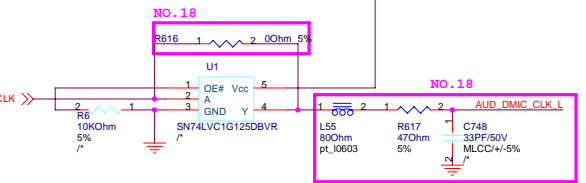
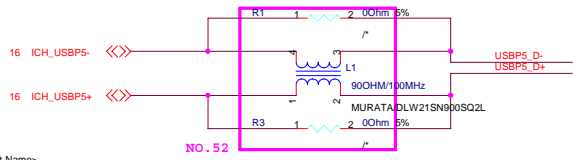
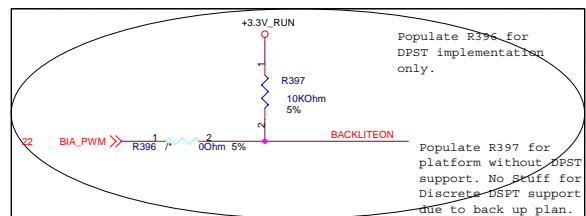
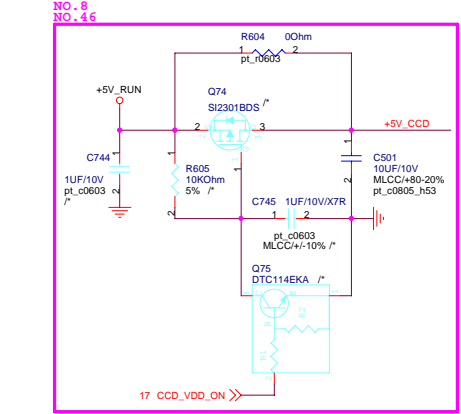
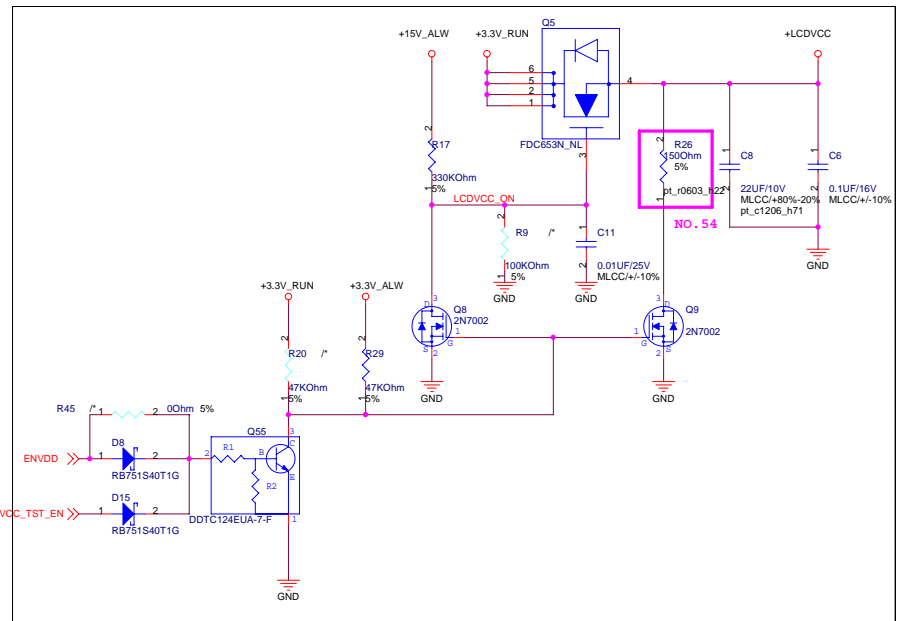
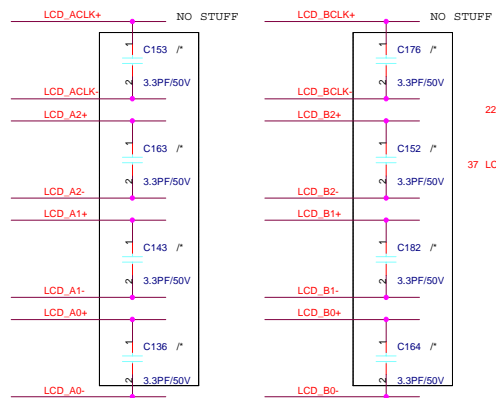
$V_{REF} = V_{DDQ} \times R_b / (R_a + R_b)$   
 $V_{REF} = 1.26V = 0.7 \times V_{DDQ}$

R78: Confirm need to no stuff not for G72 and G86.

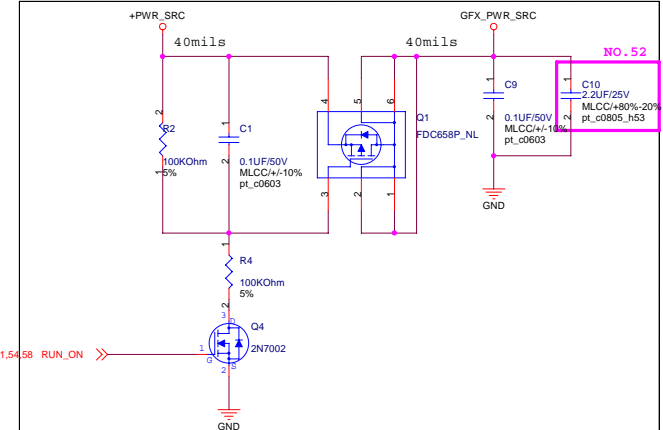
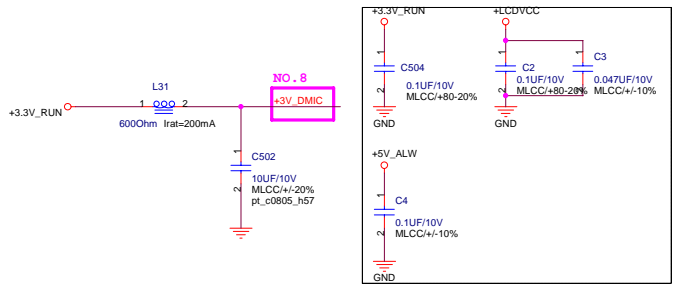




Address: A9H --Contrast  
AAH --Backlight



V\_DMIC IS DEPENDENT ON MIC SELECTION (1.8V - 3.3V TYP)  
Verify to ensure operability with chosen mic supplier.  
Notel: If only 1 digital mic, use AUD\_DMIC\_IN0.  
Note2: If using 2 dig mics, also use AUD\_DMIC\_IN0.  
This input supports 2 digmics. AUD\_DMIC\_IN1 is only used to support 4 dig mics.



<Variant Name>



<Variant Name>



PROJECT: **Lanai**

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**12**

DATE: **Monday, March 19, 2007**  
SHEET **29** OF **69**

DESCRIPTION: **VGA CRT CON**

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
*Sean Kuo*



<Variant Name>



PROJECT: **Lanai**

REVISION  
**1.2**

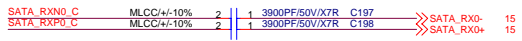
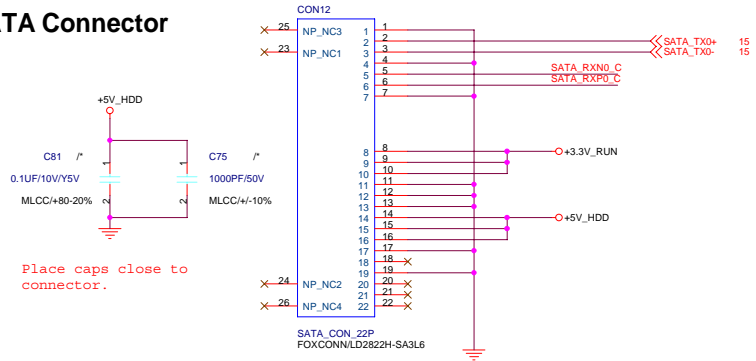
DATE: *Monday, March 19, 2007*  
SHEET **30** OF **69**

DESCRIPTION: *TV OUT CON*

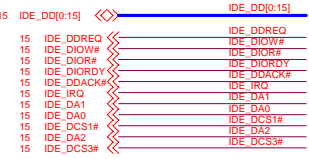
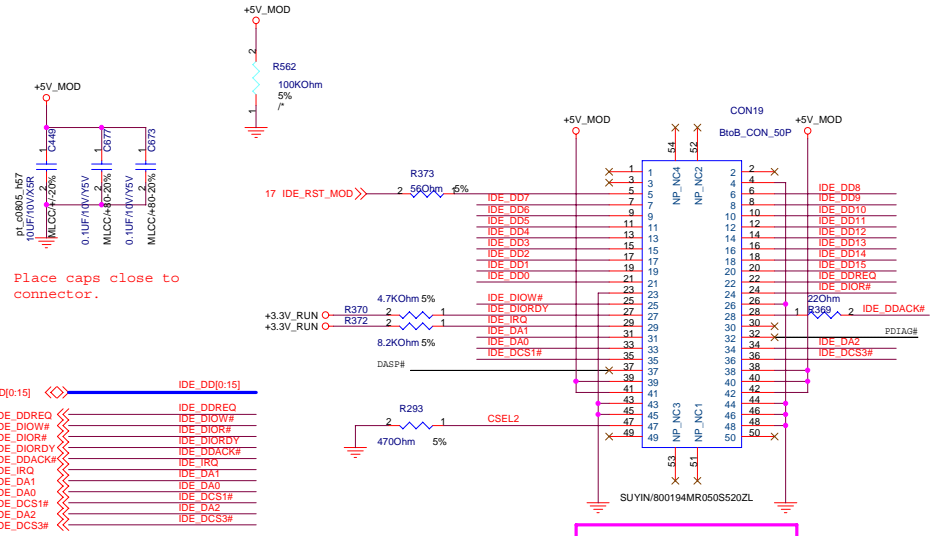
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER : *Sean Kuo*

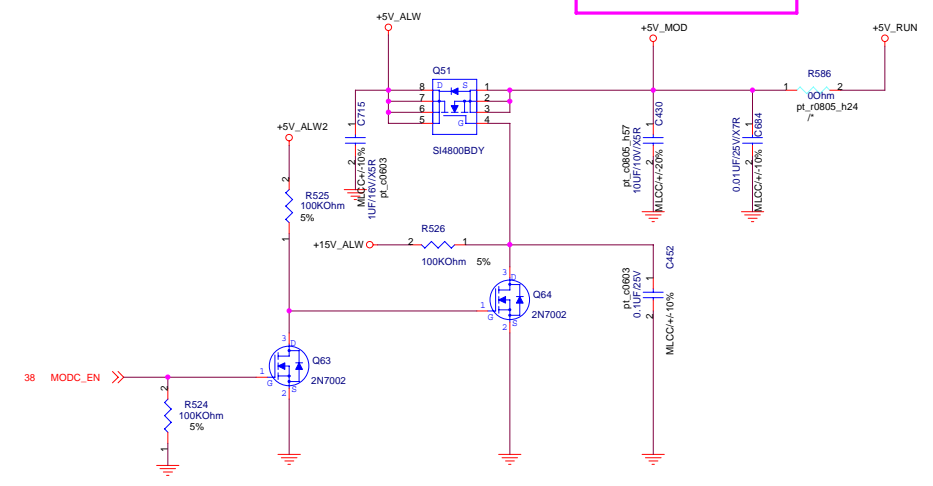
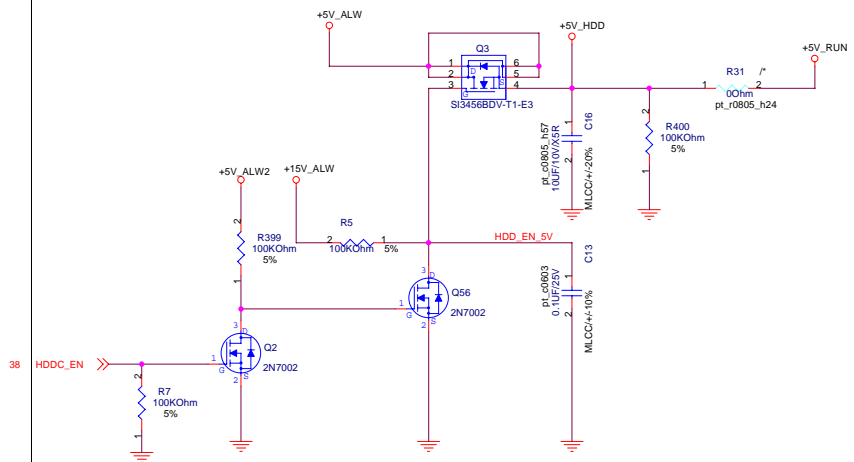
### SATA Connector

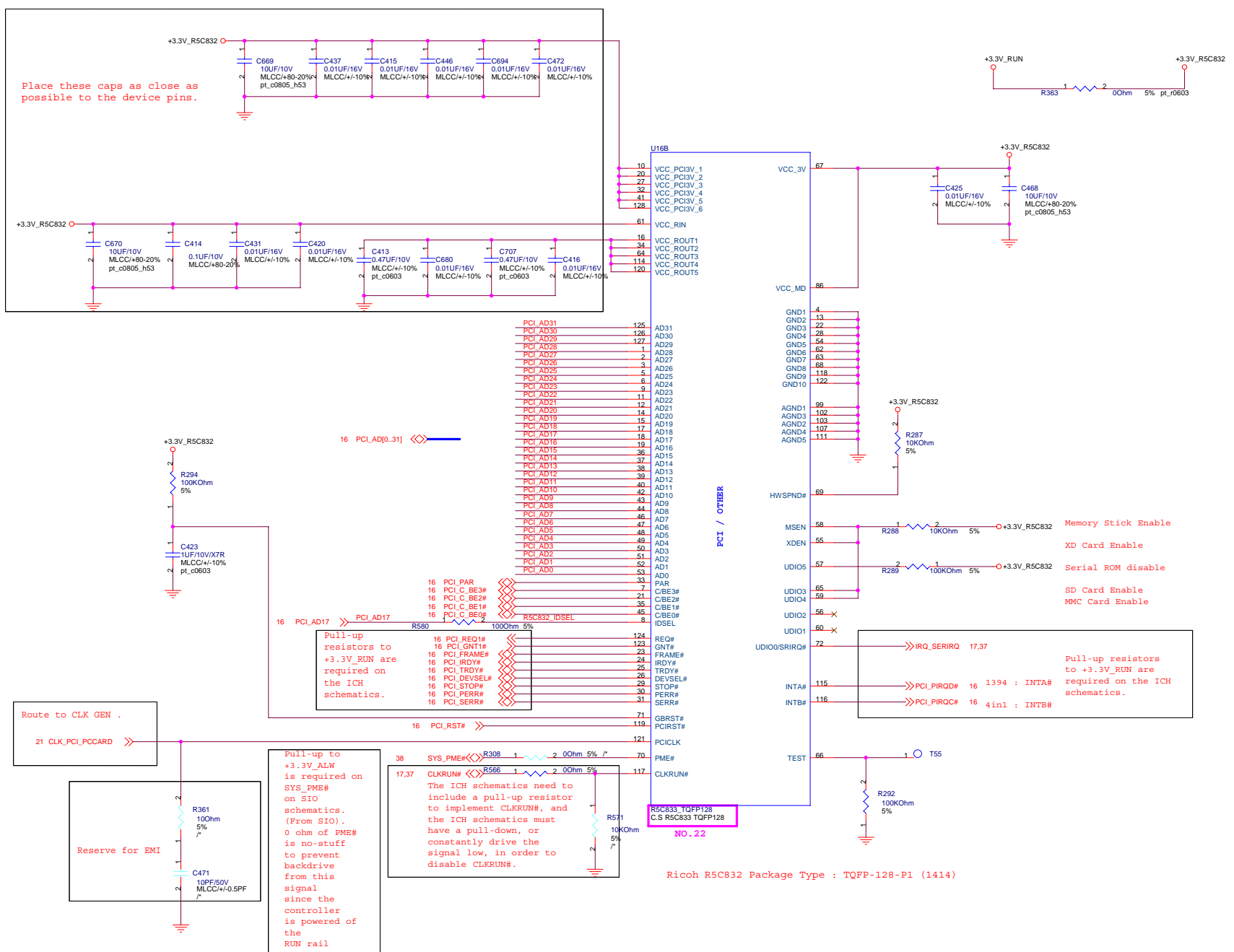


### ODD Connector



MODPRES# and USB\_IDE# are removed.





Place these caps as close as possible to the device pins.

Route to CLK GEN .

Reserve for EMI

Pull-up to +3.3V\_ALW is required on SYS\_PME# on SIO schematics. (From SIO). 0 ohm of PME# is no-stuff to prevent backdrive from this signal since the controller is powered of the RUN rail

17.37 CLKRUN# R566 1 2 0Ohm 5%  
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

IRQ\_SERIRQ 17.37  
PCI\_PIRQ# 16 1394 : INTA#  
PCI\_PIROC# 16 4in1 : INTB#

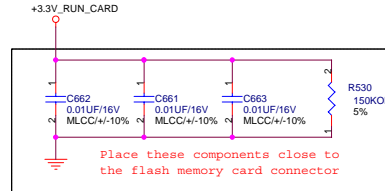
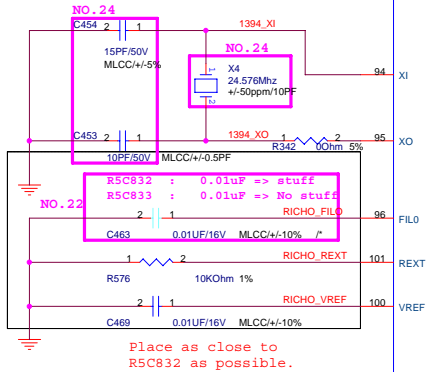
R5C833 TQFP128  
C.S R5C833 TQFP128  
NO.22

Ricoh R5C832 Package Type : TQFP-128-P1 (1414)

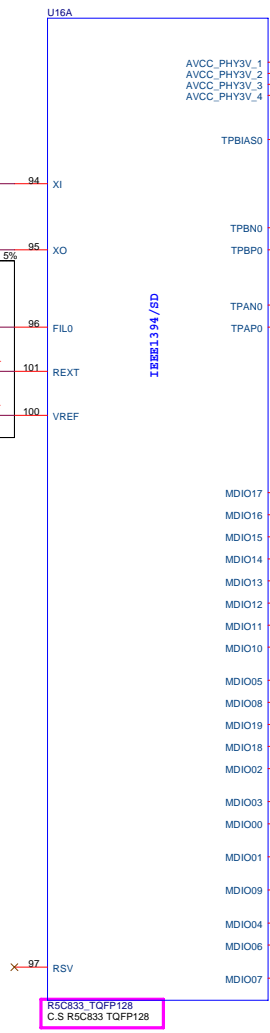
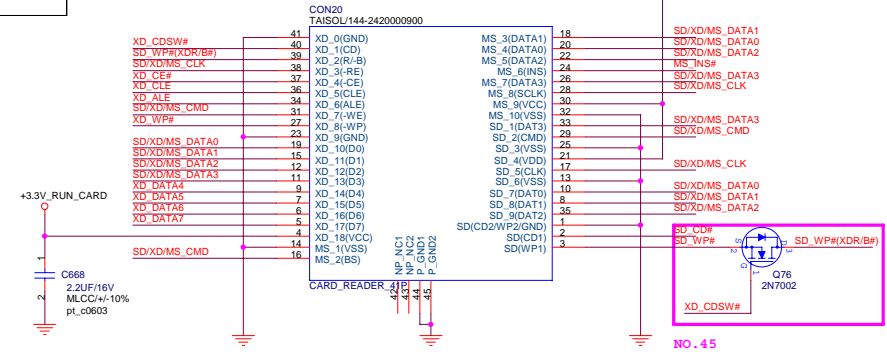
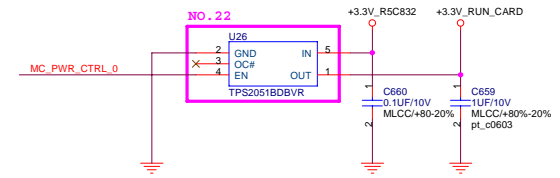


**Recommended Crystal Specs from Data Sheet:**

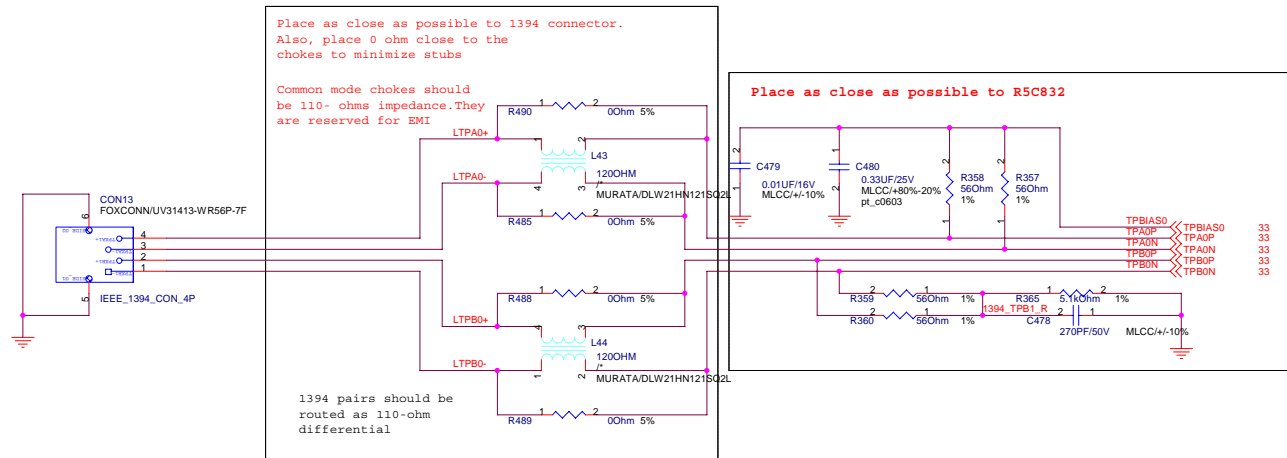
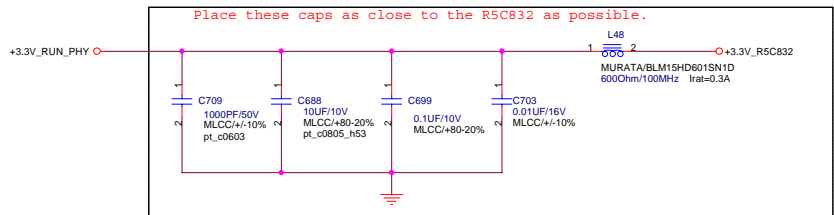
Normal Frequency : 24.576 Mhz  
 Frequency Tolerance : +/- 50ppm @ 25C  
 Driver Level : .1 mW  
 Load capacitance : 10pF  
 Equ. Resistance : 50 Ohm Max  
 Shunt Capacitance : 7.0pF Max



**For SD/MS Card Power**



Variant Name:



<Variant Name>



PROJECT: Lanai

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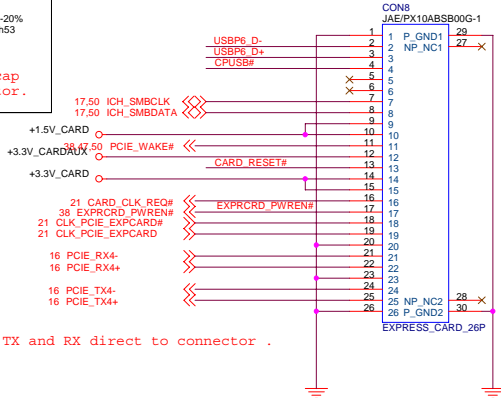
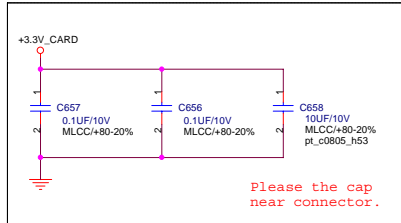
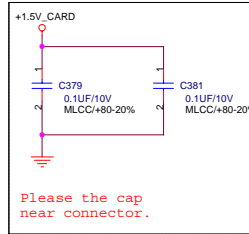
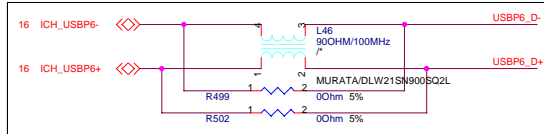
DATE: Monday, March 19, 2007  
SHEET 34 OF 69

DESCRIPTION:  
R5C833 - IEEE1394 PART

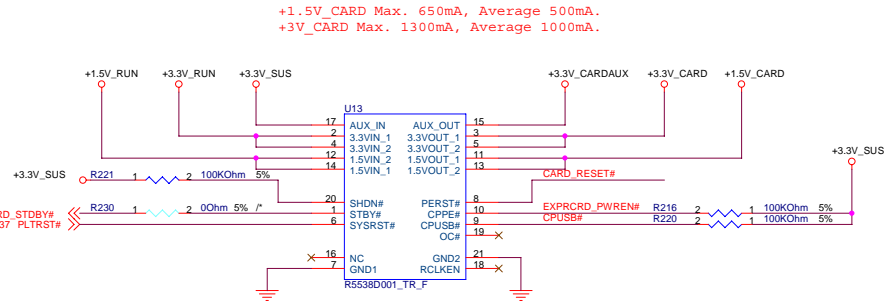
SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :  
Terry Lin

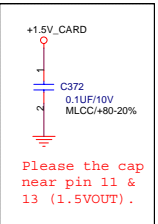
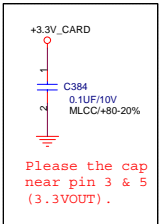
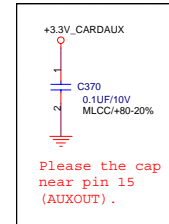
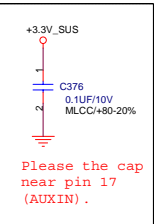
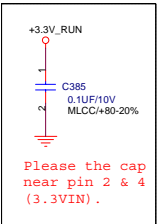
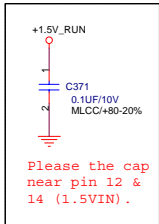
# Express Card



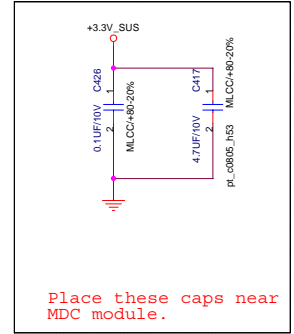
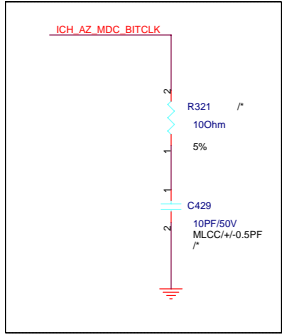
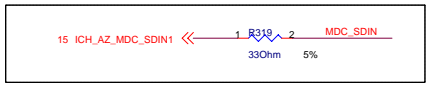
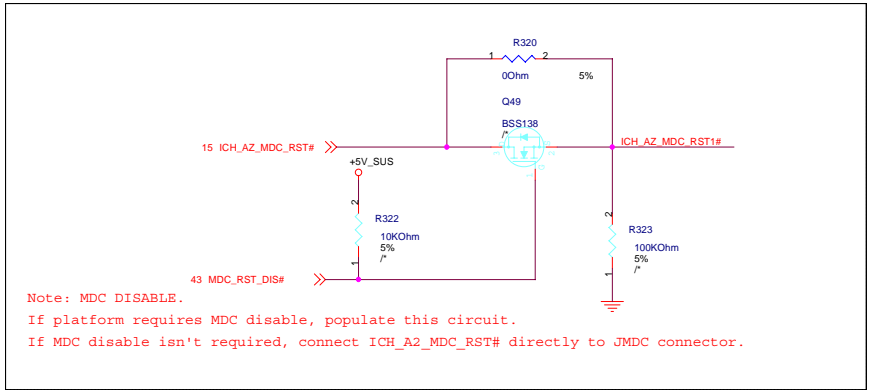
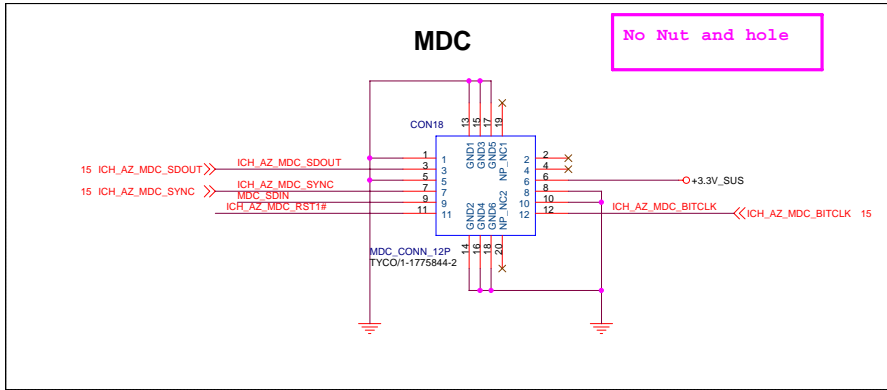
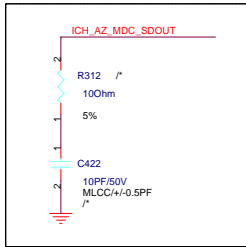
PCI-Express TX and RX direct to connector .

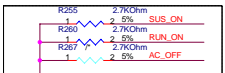
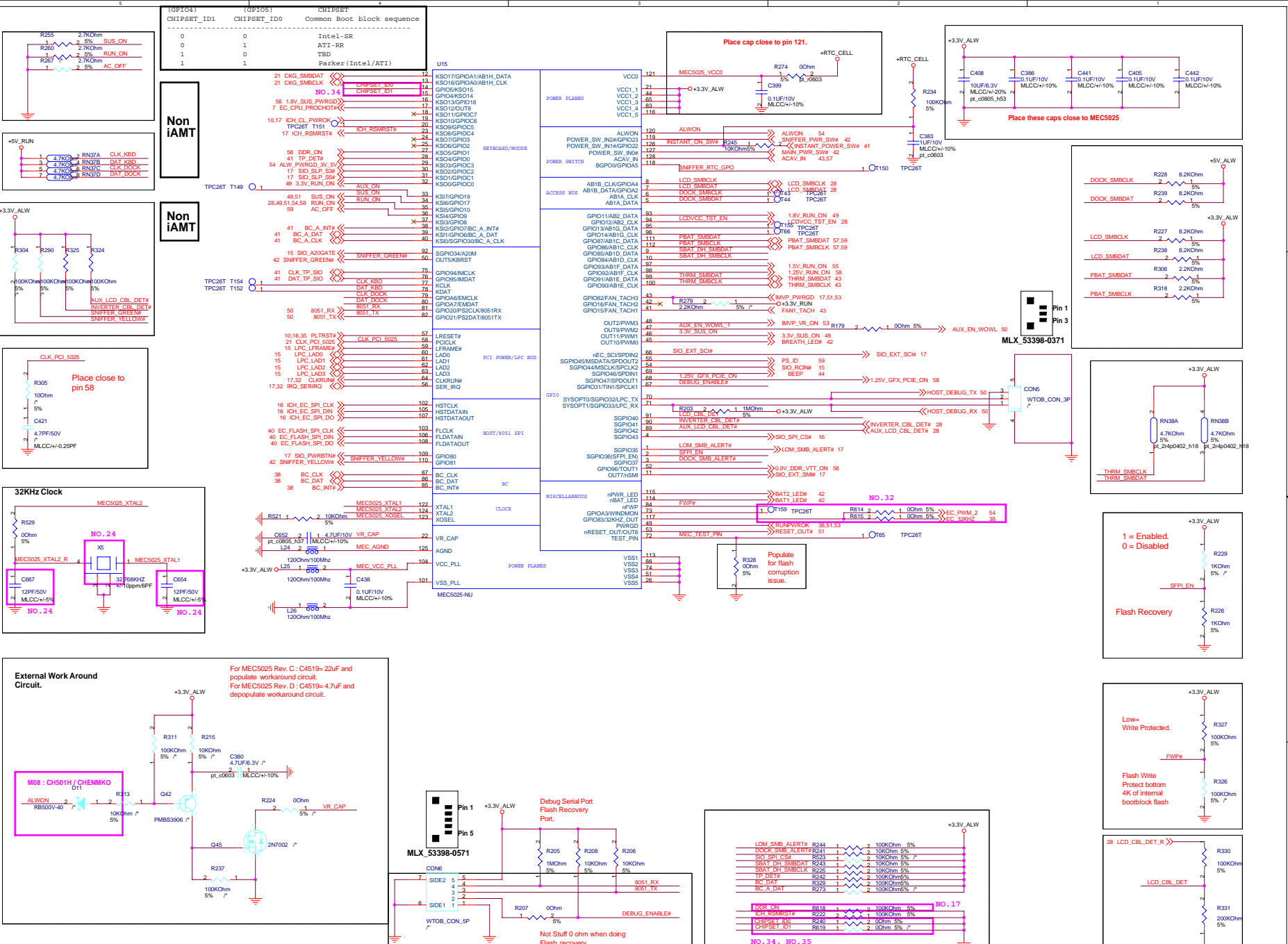


+1.5V\_CARD Max. 650mA, Average 500mA.  
+3V\_CARD Max. 1300mA, Average 1000mA.



<Variant Name>

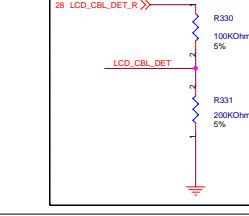
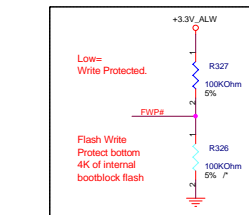
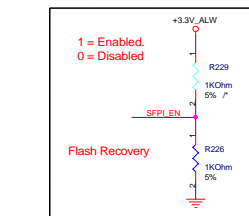
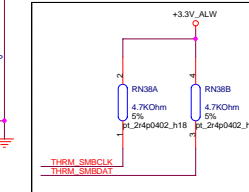
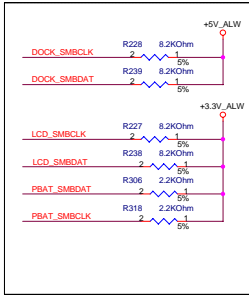
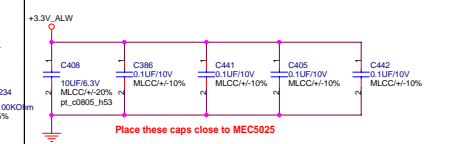
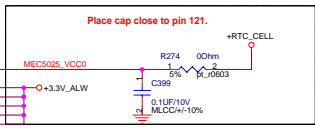
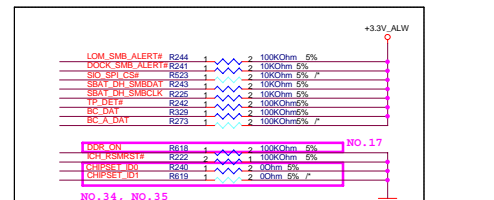
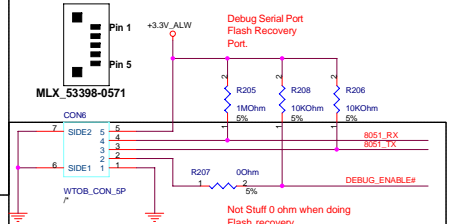
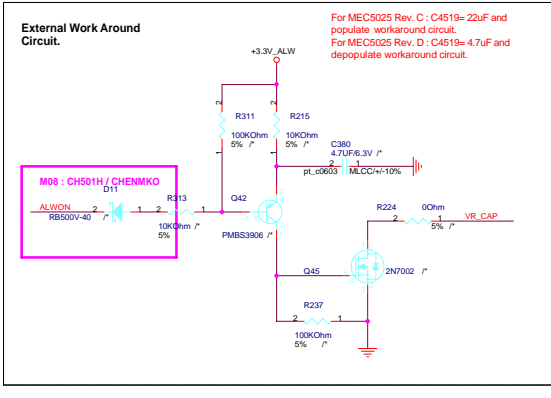
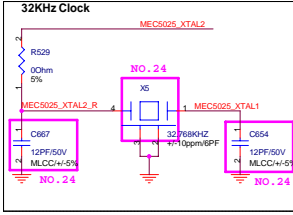
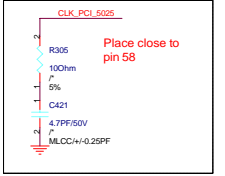
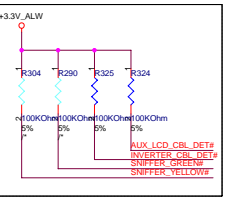


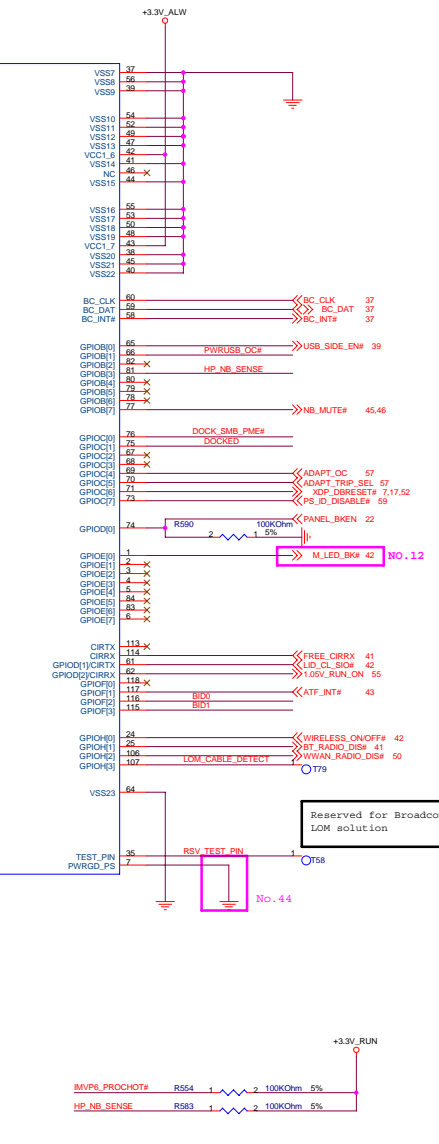
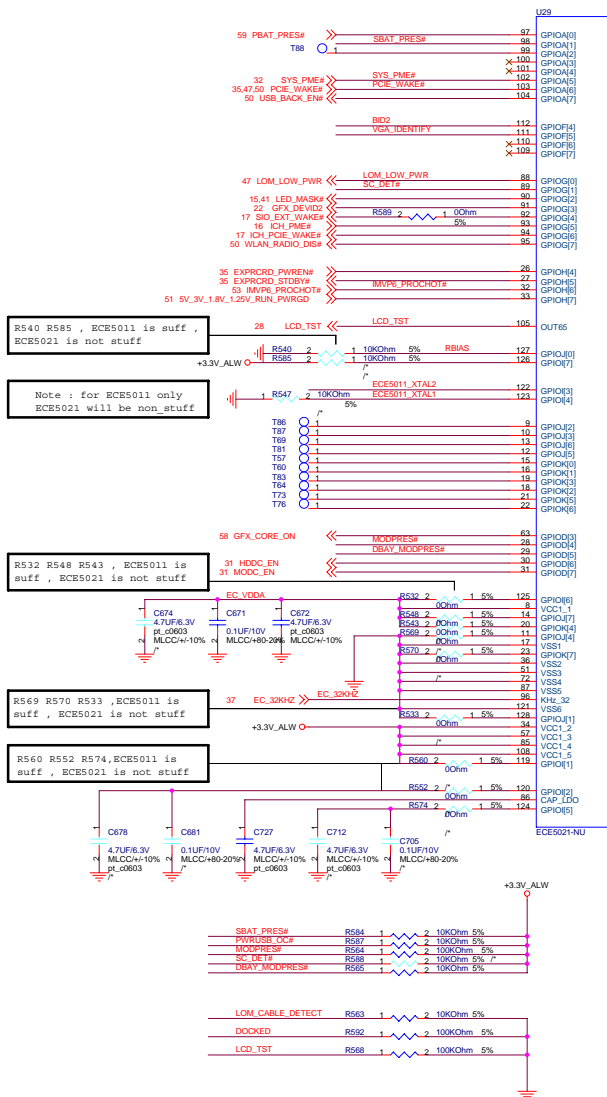
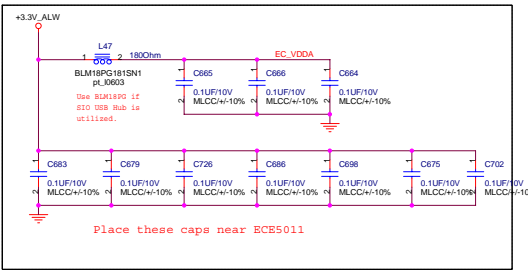
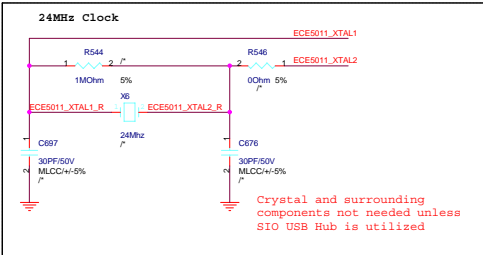
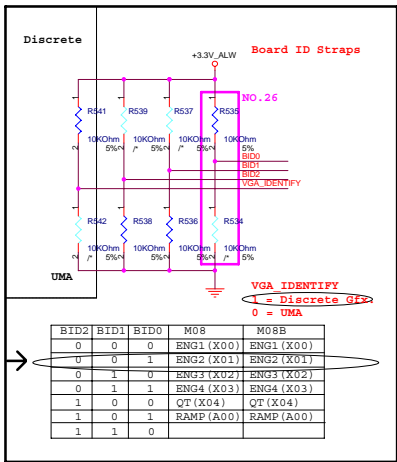
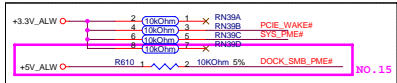


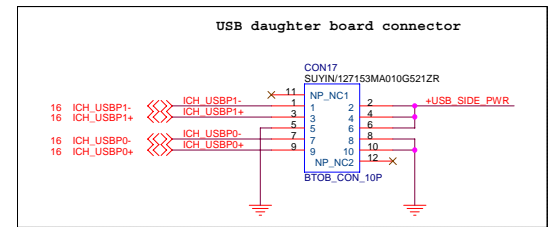
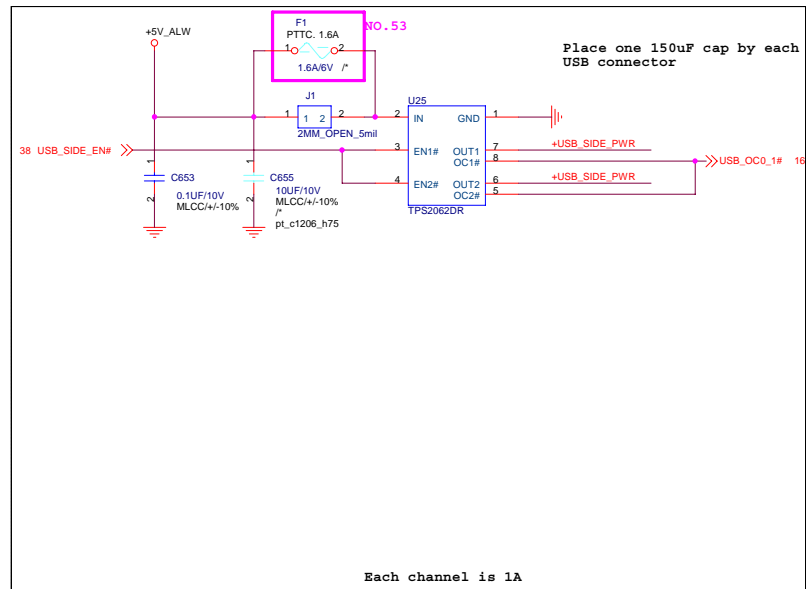
Non iAMT



Non iAMT







<Variant Name>



PROJECT: Lanai

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1.2

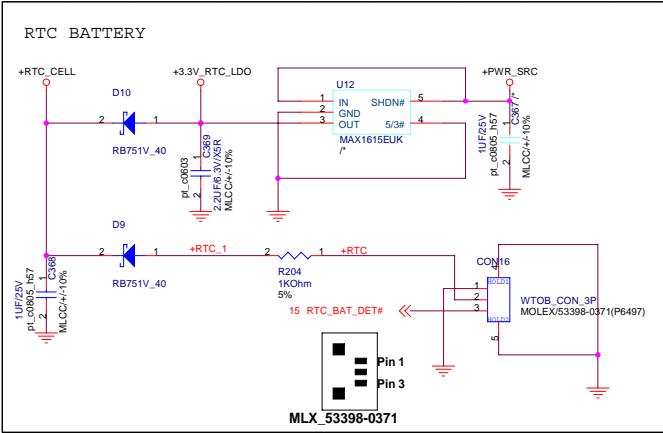
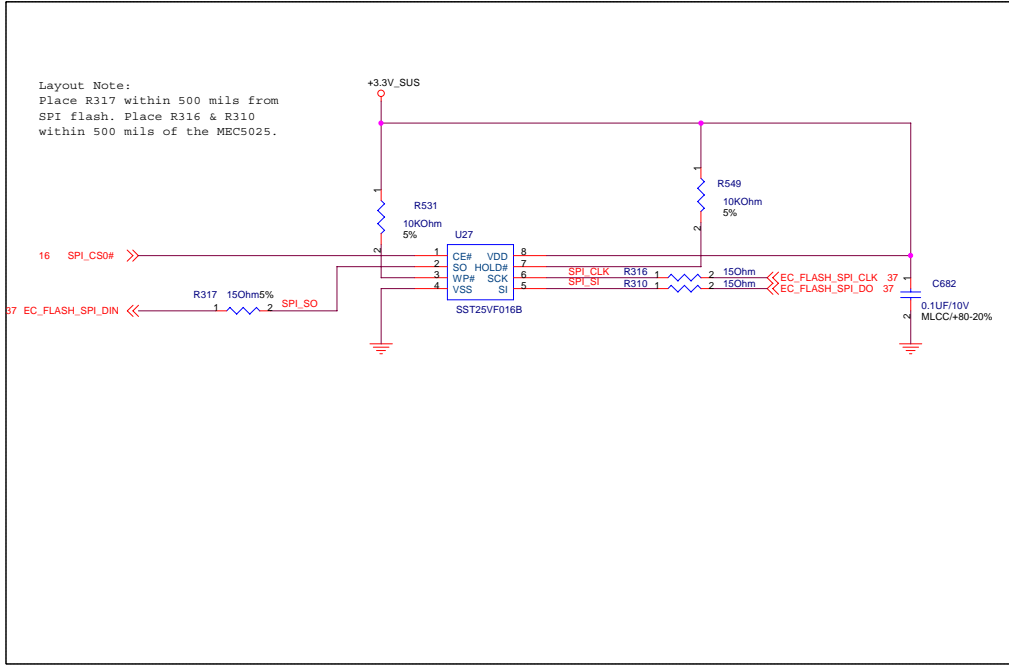
DATE: Monday, March 19, 2007  
SHEET 39 OF 69

DESCRIPTION: USB PORT x 2

SCHEMATIC FILE NAME :  
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :  
Terry Lin



<Variant Name>



PROJECT: Lanai

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1.2

DATE: Monday, March 19, 2007  
SHEET 40 OF 69

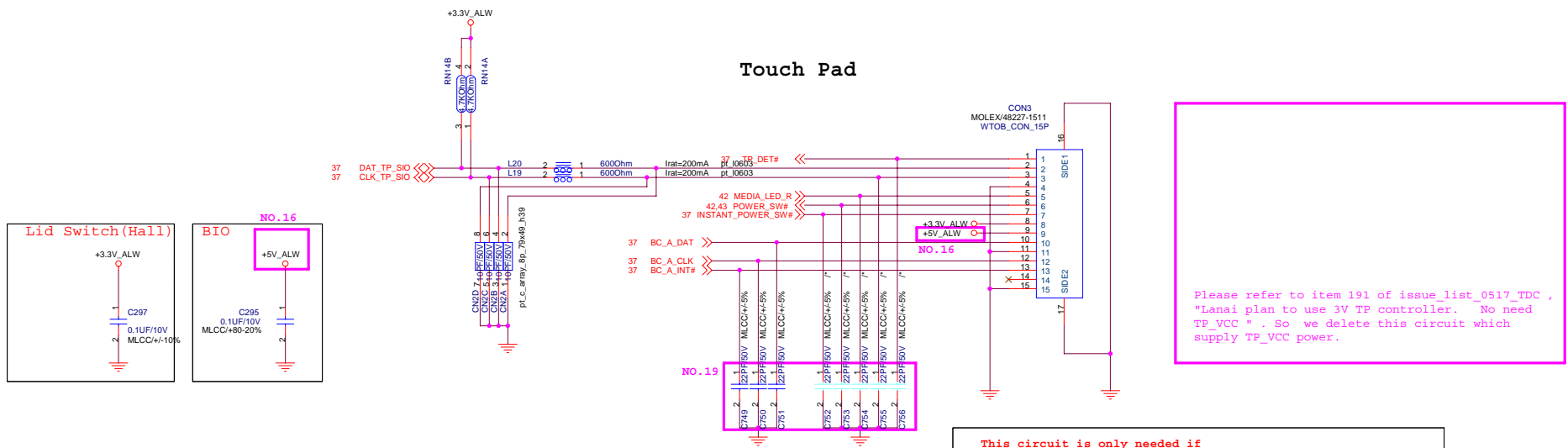
DESCRIPTION:  
FLASH & RTC

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :  
C.L. Ho

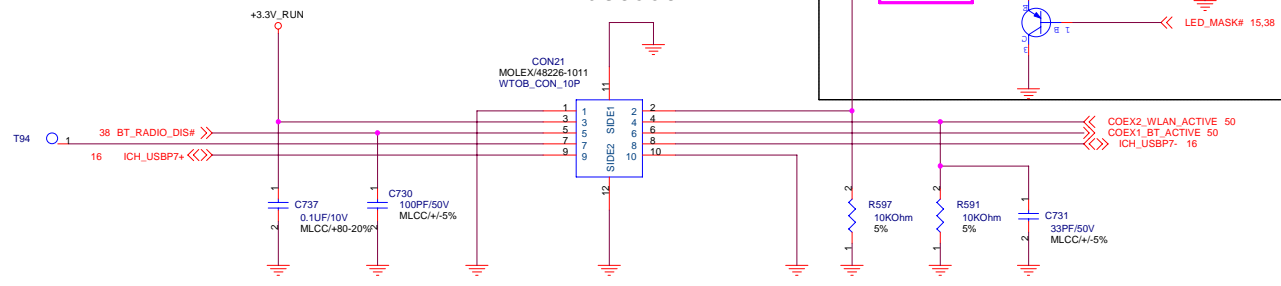


### Touch Pad

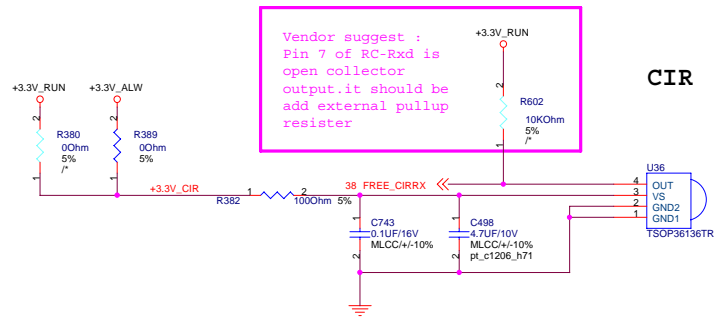


Please refer to item 191 of issue\_list\_0517\_TDC , "Lanai plan to use 3V TP controller. No need TP\_VCC ". So we delete this circuit which supply TP\_VCC power.

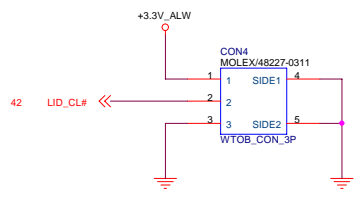
### Bluetooth



### CIR



### HALL SENSOR



<Variant Name>



PROJECT: Lanai

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DATE: Monday, March 19, 2007  
SHEET 41 OF 69

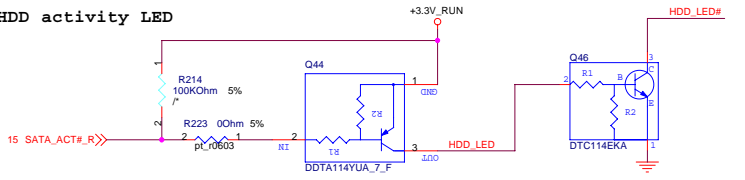
DESCRIPTION:  
TOUCH PAD & BT & CIR & LID

SCHEMATIC FILE NAME :  
RELEASE DATE :

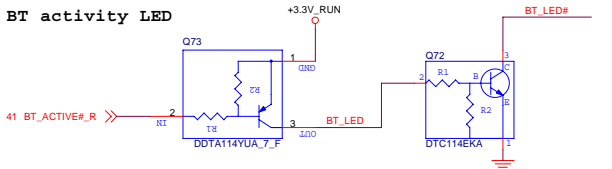
<OrgName>

DESIGN ENGINEER :  
Terry Lin

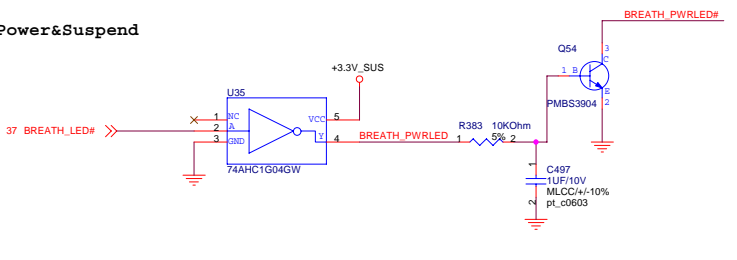
### HDD activity LED



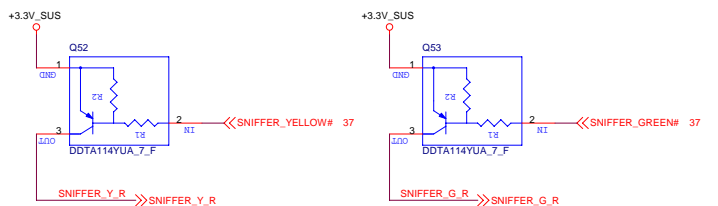
### BT activity LED



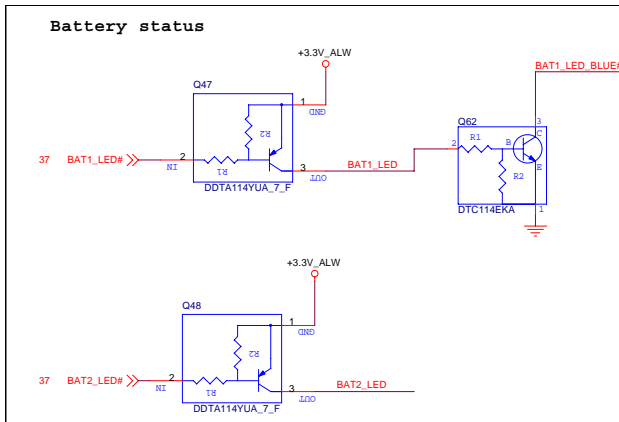
### Power&Suspend



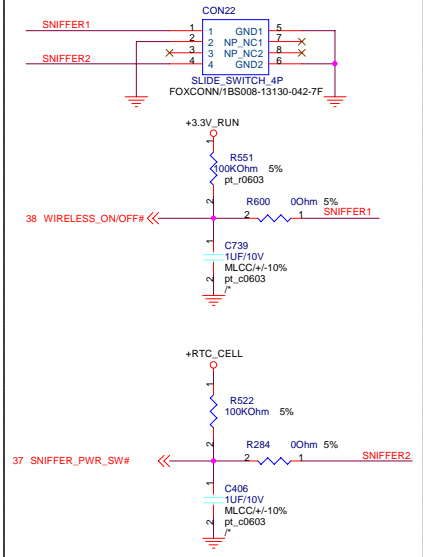
### Sniffer LED driver circuit



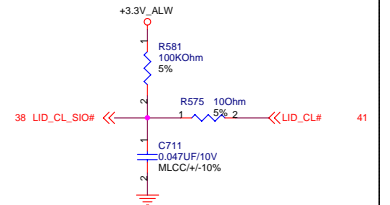
### Battery status



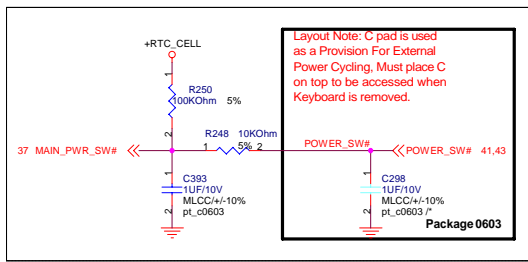
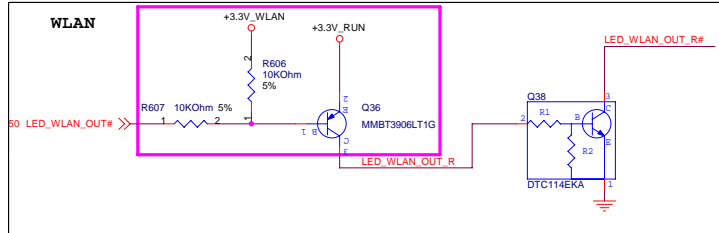
### Sniffer Switch



### Hall Switch



### NO.7 WLAN

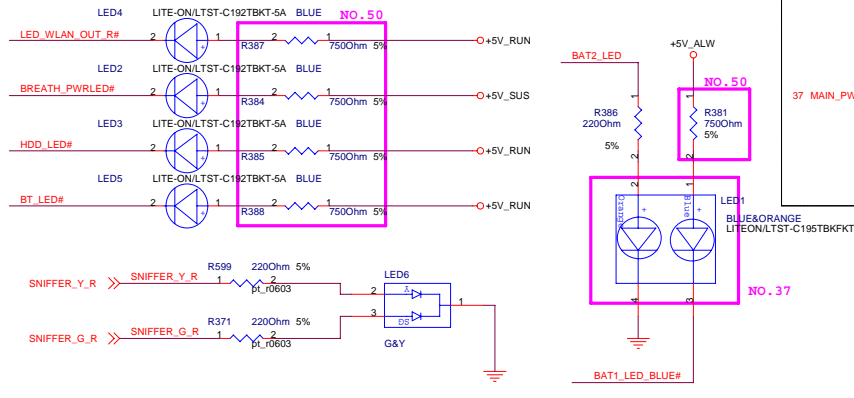
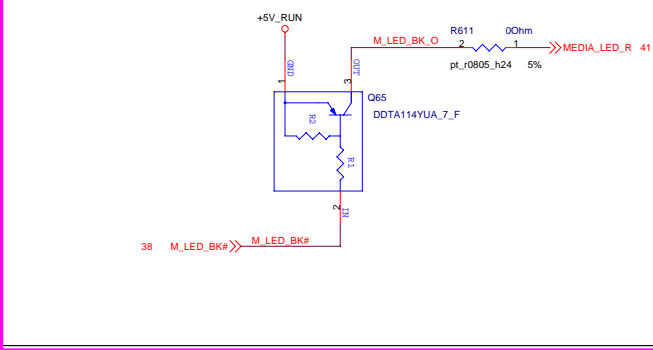


Layout Note: C pad is used as a Provision For External Power Cycling. Must place C on top to be accessed when Keyboard is removed.

Package 0603

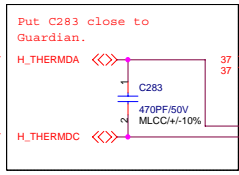
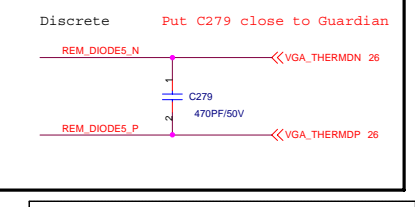
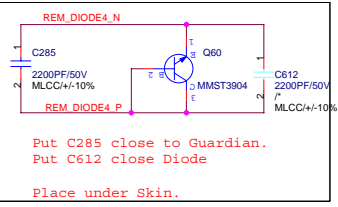
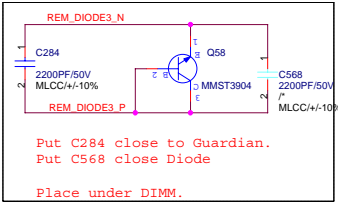
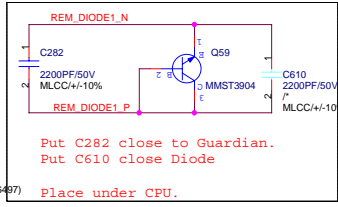
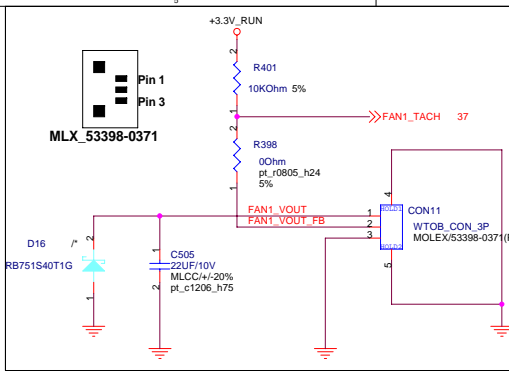
### NO.12 NO.33

### Media Bottom Board LED drive circuit



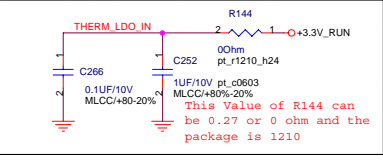
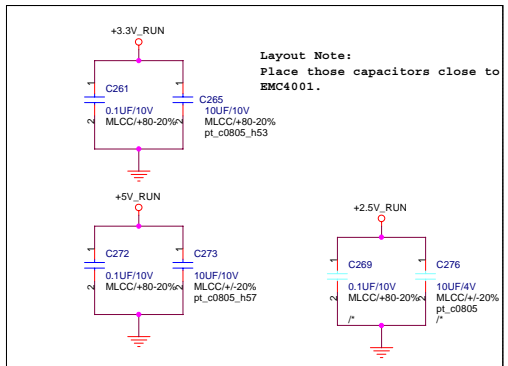
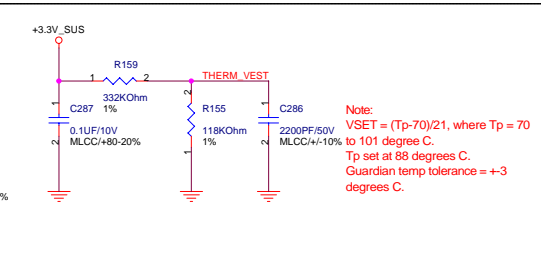
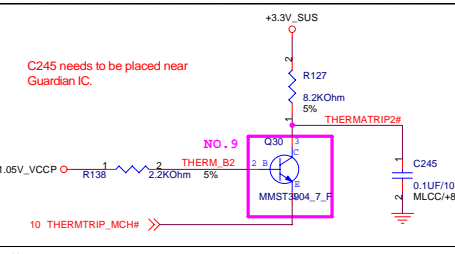
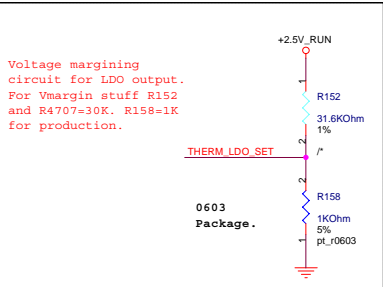
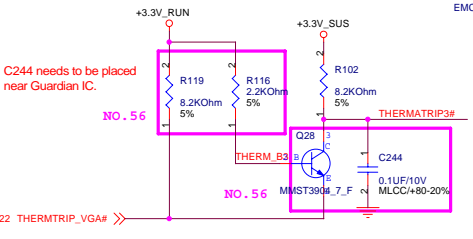
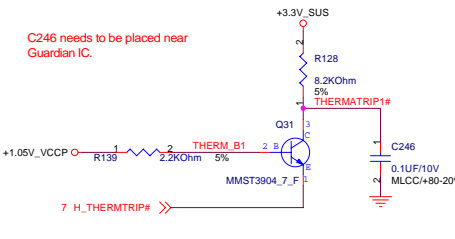
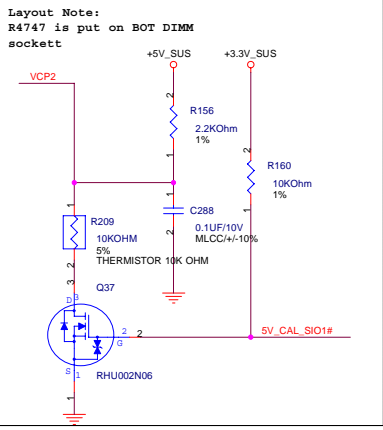
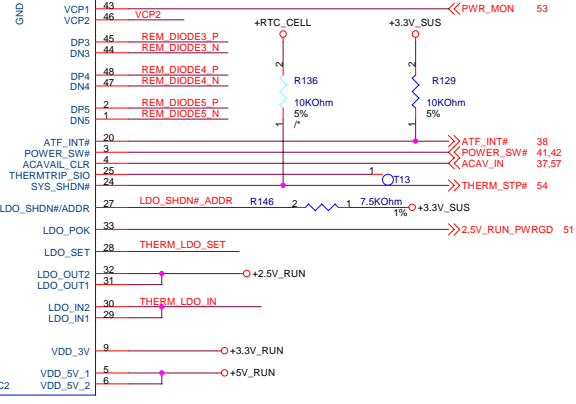
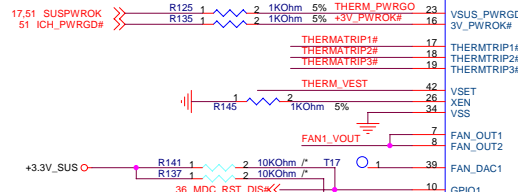
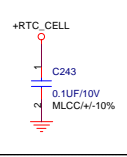
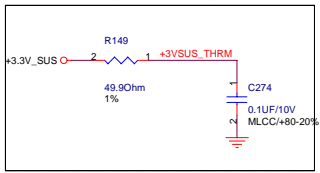
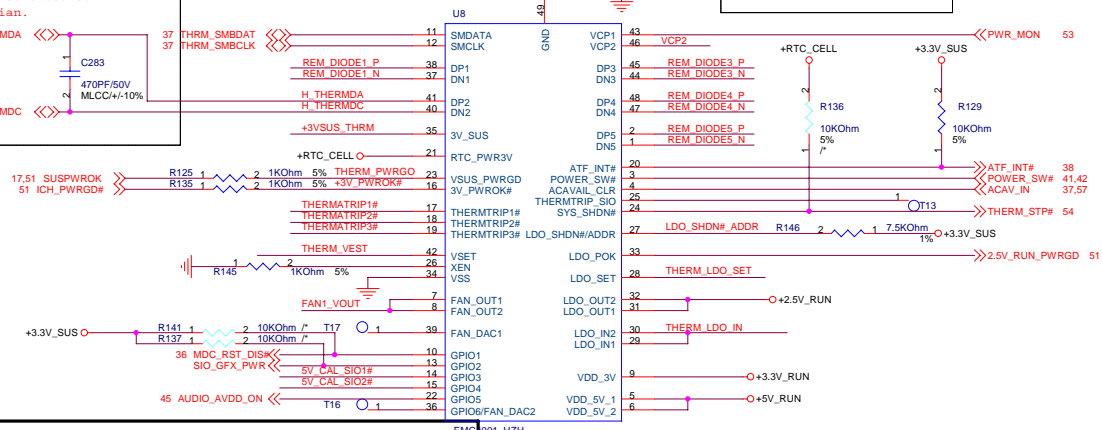
Variant Name:

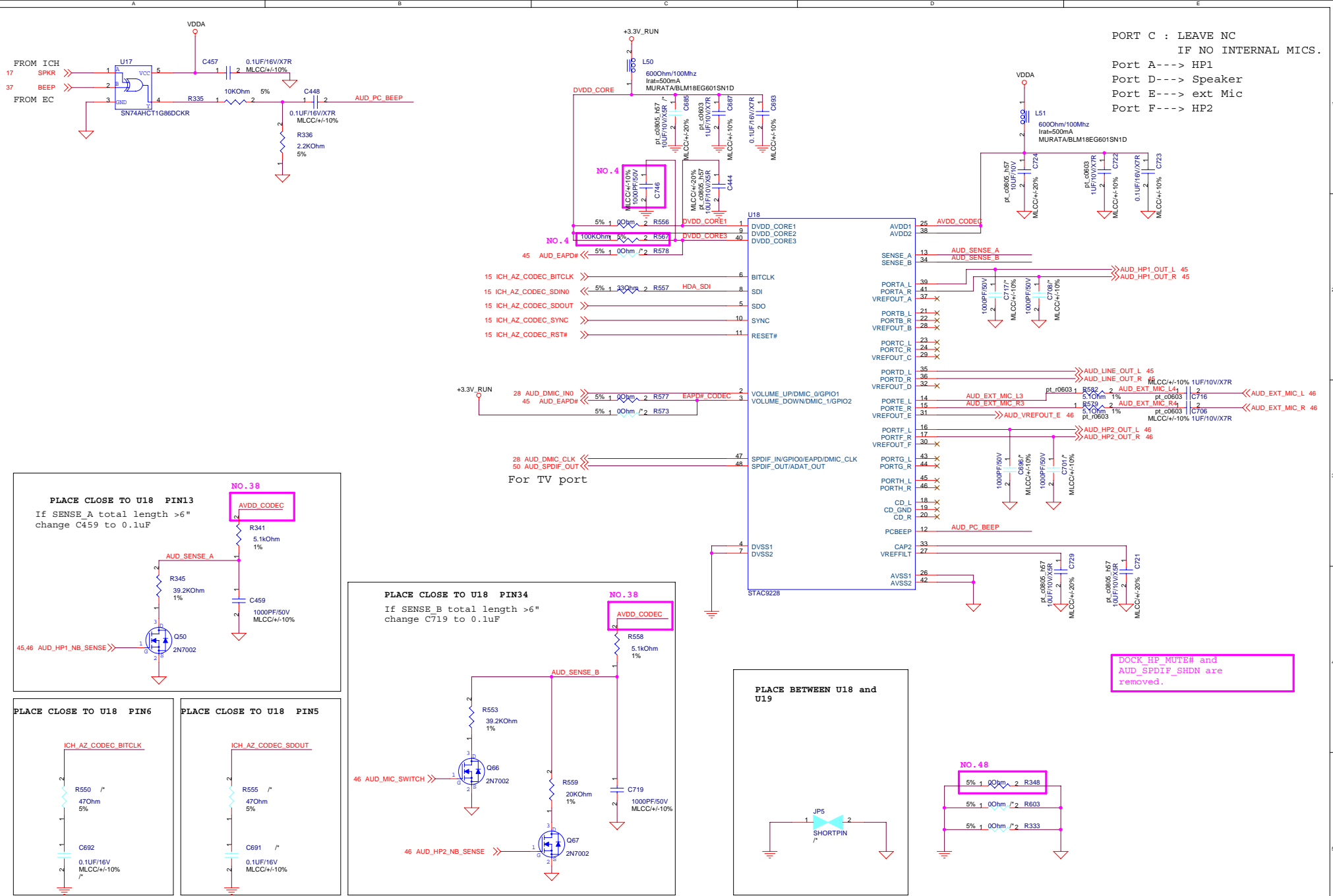
ASUS PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	<OrgName>	DESIGN ENGINEER:
	1.2	SHEET 42 OF 69	SWITCH & LED	RELEASE DATE:		Ivan Chou



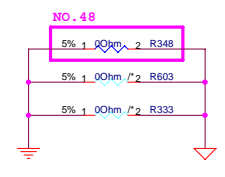
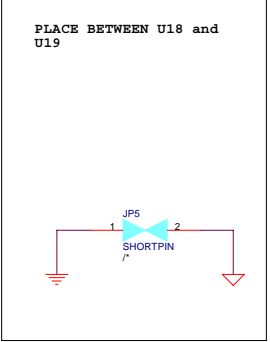
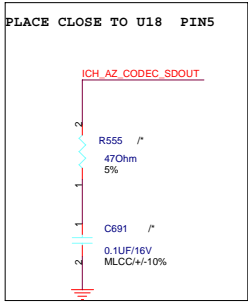
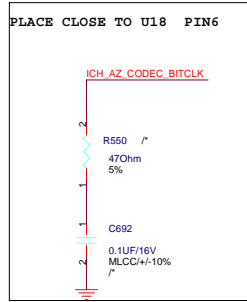
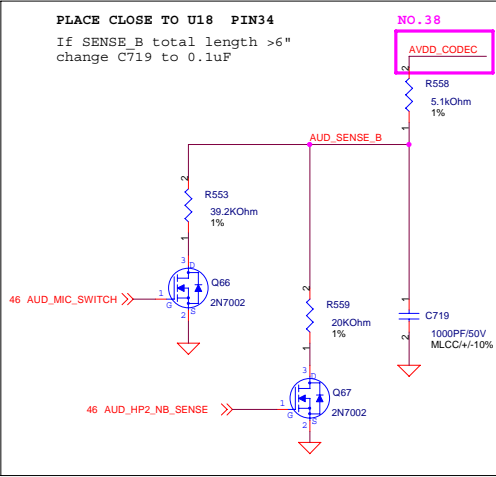
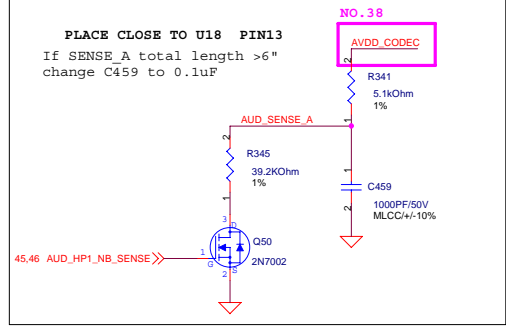
### Guardian

Note:  
150K input impedance on VCP1 (Pin 43)

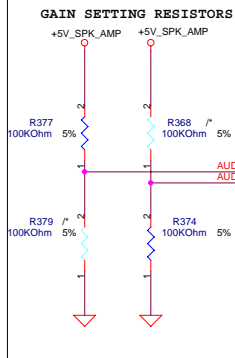
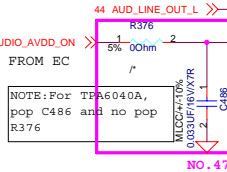
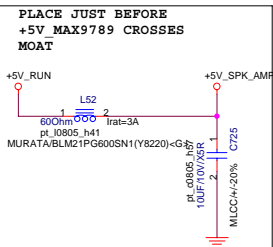
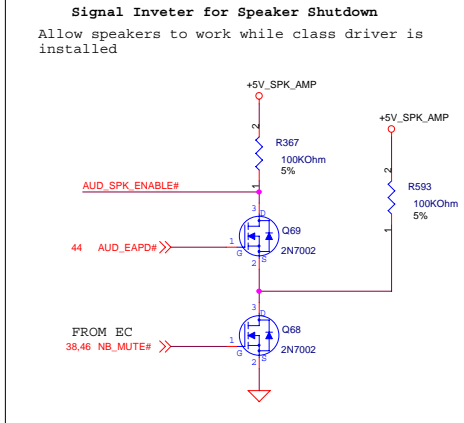




PORT C : LEAVE NC  
 IF NO INTERNAL MICS.  
 Port A----> HP1  
 Port D----> Speaker  
 Port E----> ext Mic  
 Port F----> HP2



DOCK\_HP\_MUTE# and  
 AUD\_SPDIF\_SHDN are  
 removed.

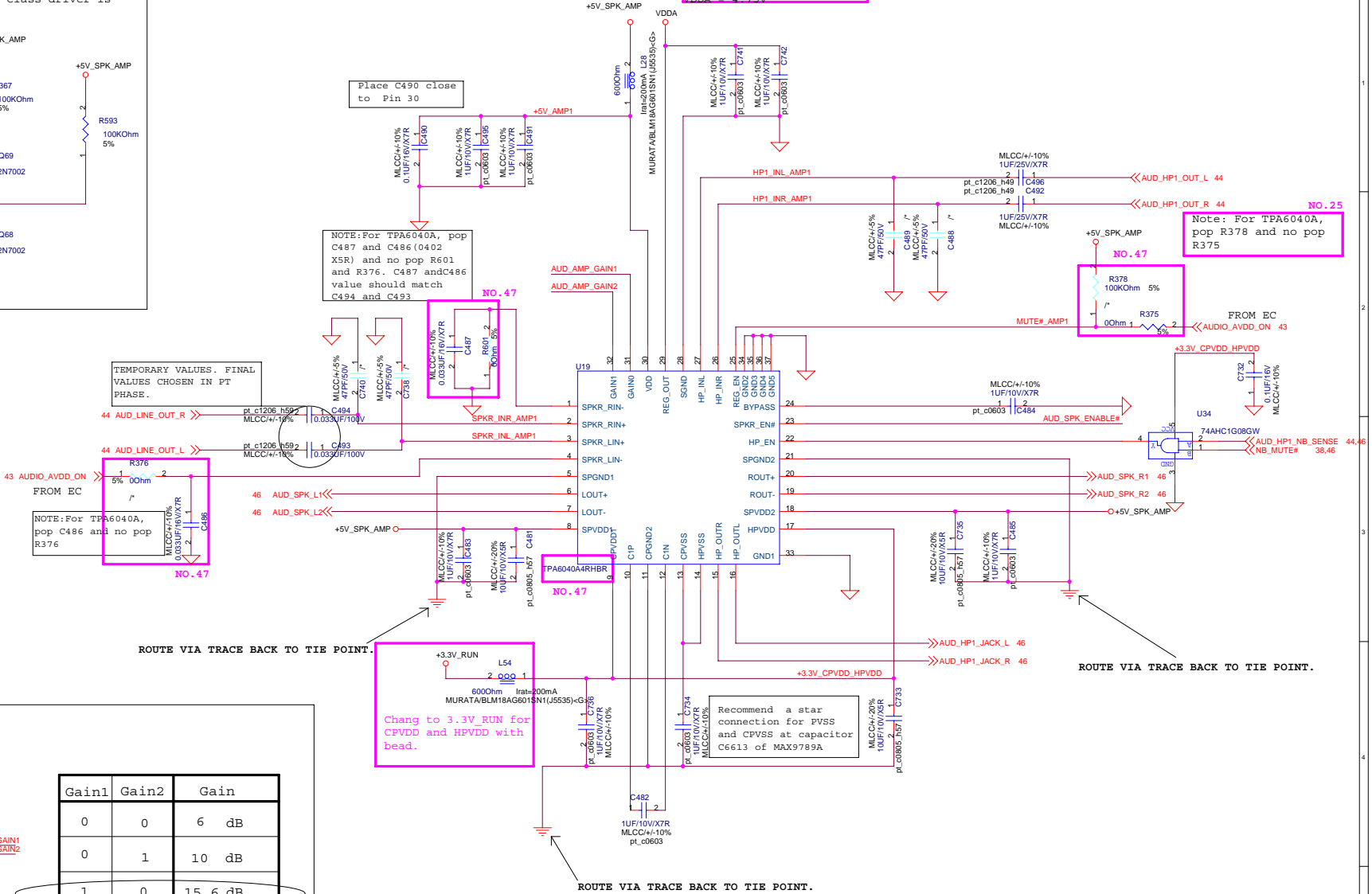


Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

NOTE: For TPA6040A, pop C487 and C486 (0402 X5R) and no pop R601 and R376. C487 and C486 value should match C494 and C493

Change to 3.3V RUN for CPVDD and HPVDD with bead.

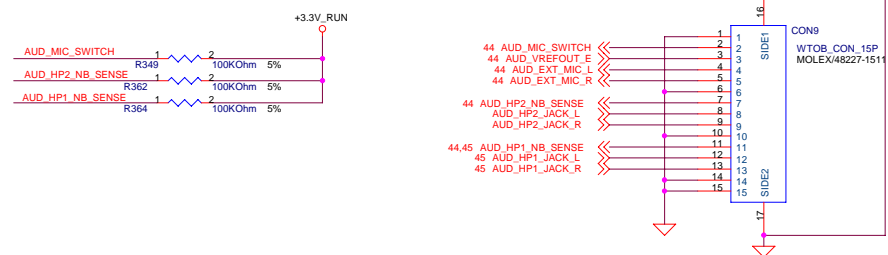
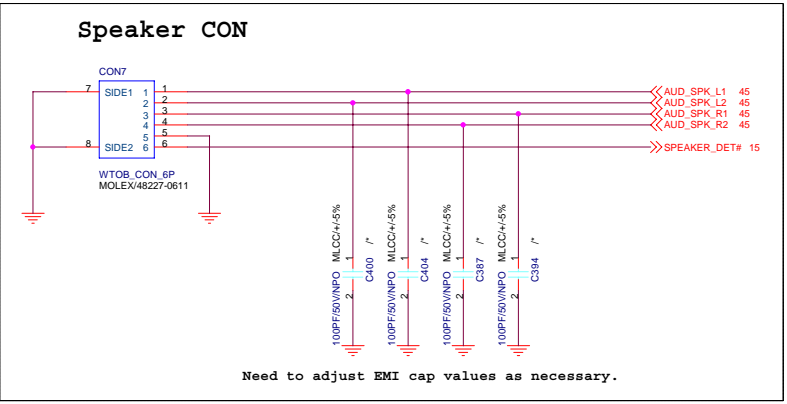
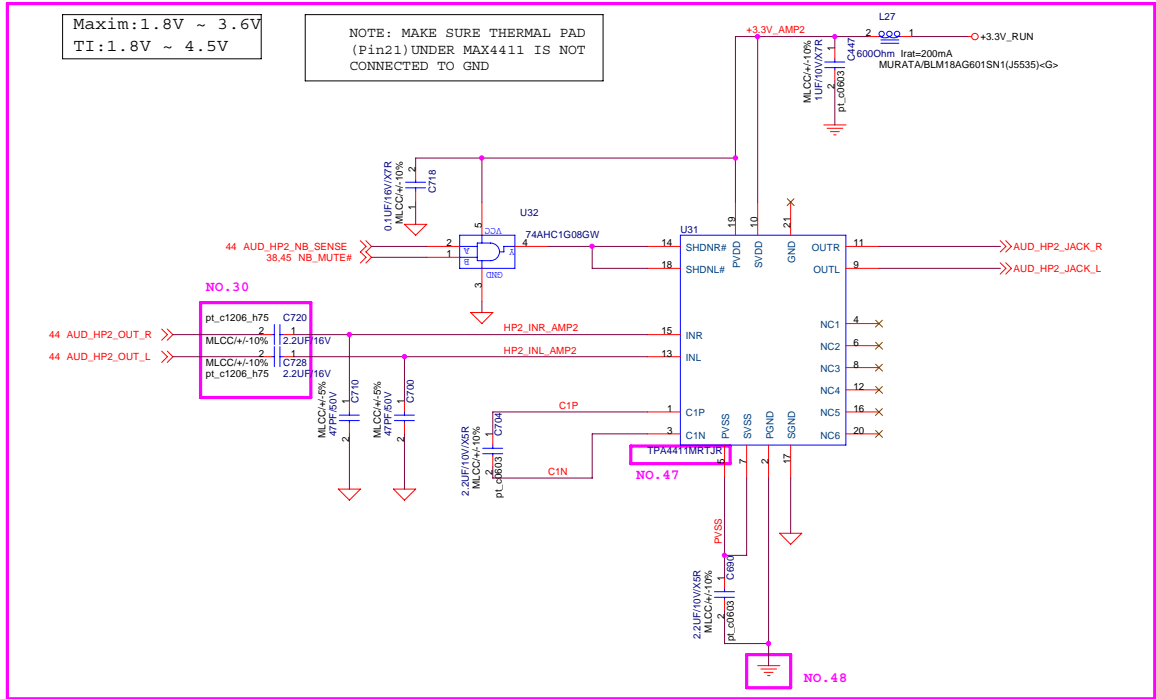
VDDA Range = 1.21V ~ 4.85V (SET = 1.23V). If SET = 0 V, VDDA = 4.75V

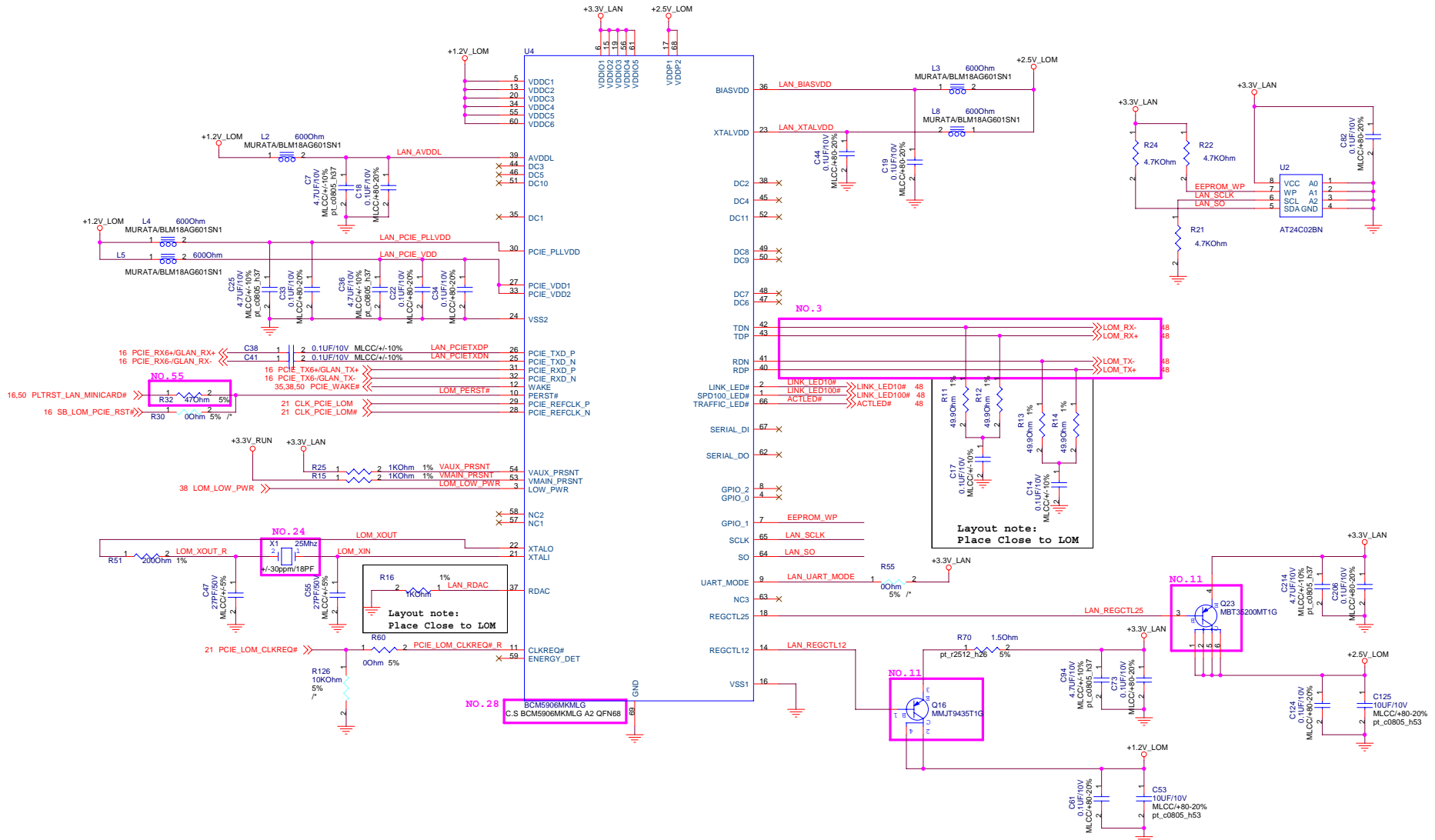
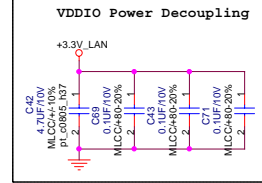
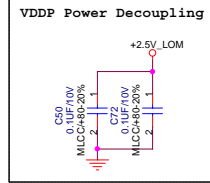
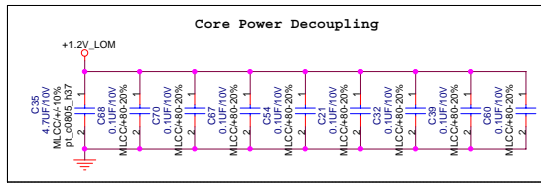


<Variant Name>

Maxim: 1.8V ~ 3.6V  
 TI: 1.8V ~ 4.5V

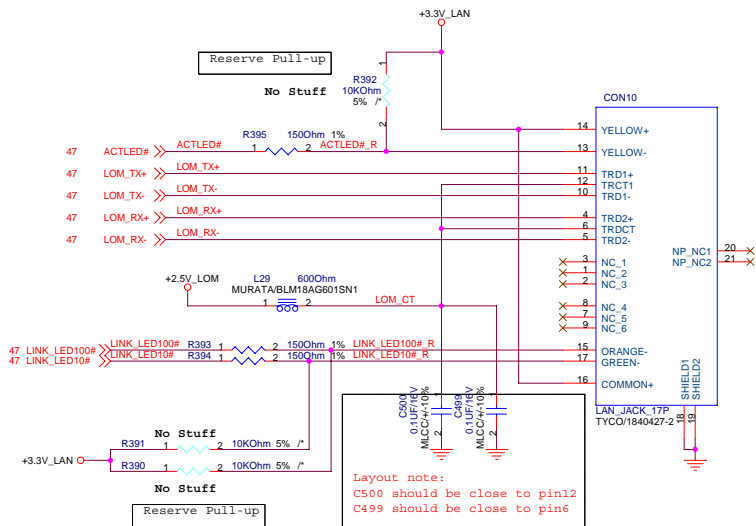
NOTE: MAKE SURE THERMAL PAD (Pin21) UNDER MAX4411 IS NOT CONNECTED TO GND





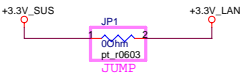
<Variant Name>

	PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: LAN BCM5906MKMLG(QFN-68)	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER:
			SHEET 47 OF 69		RELEASE DATE:	Ivan Chou



**+3.3V LAN Source Guideline:**

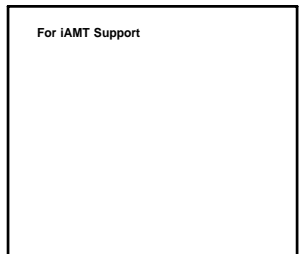
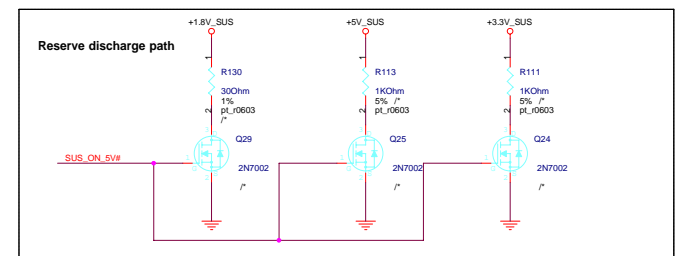
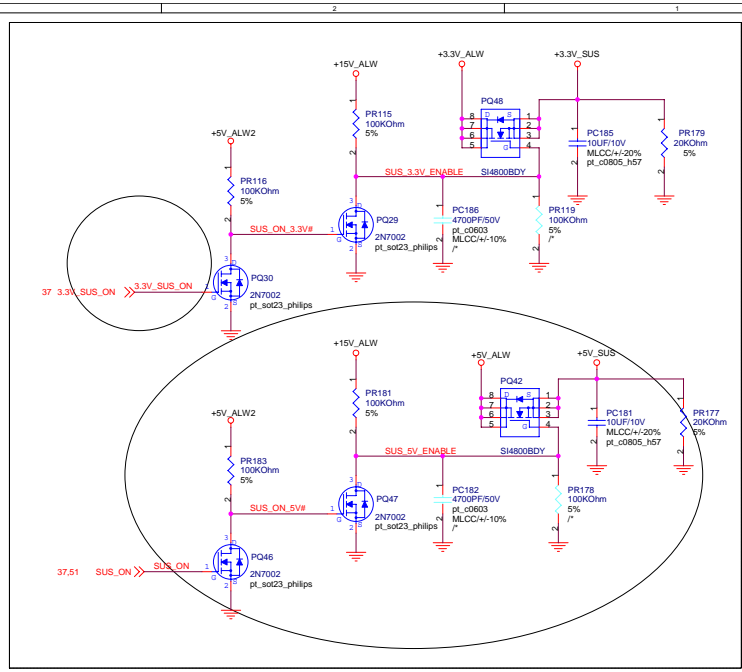
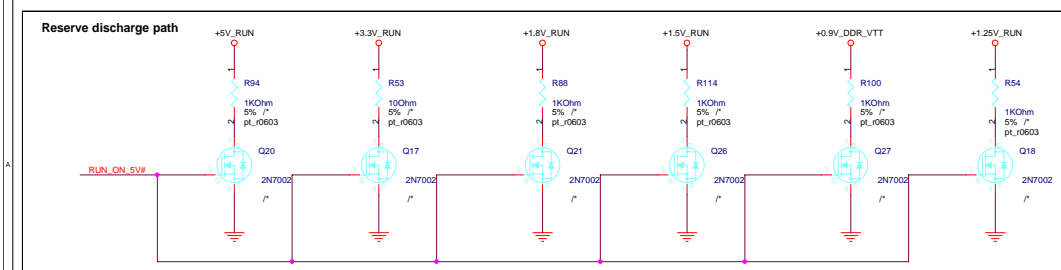
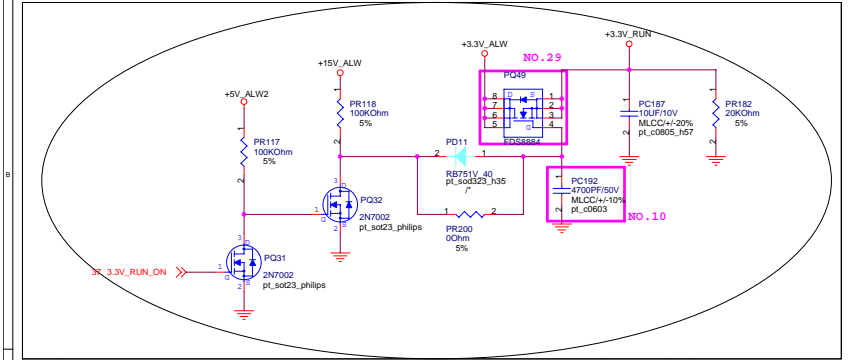
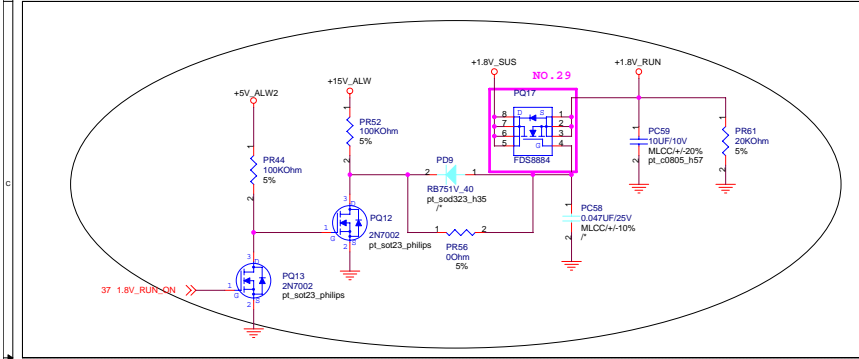
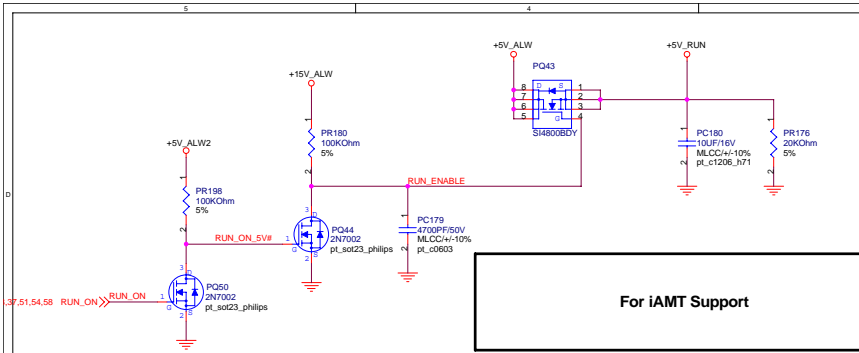
1. Use +3.3V\_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V\_SRC if Wake-on-LAN is required out of S4, S5



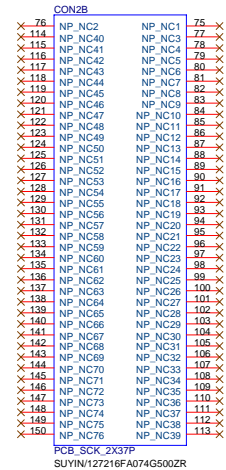
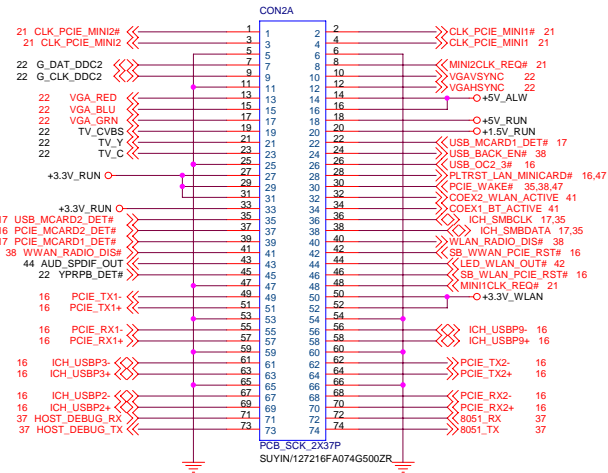
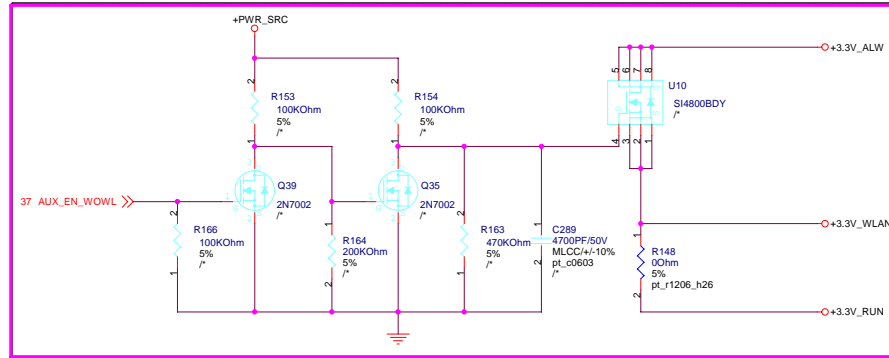
Layout note:  
 C500 should be close to pin12  
 C499 should be close to pin6

Per EE schematic checklist item.87: Only support wake up from S3



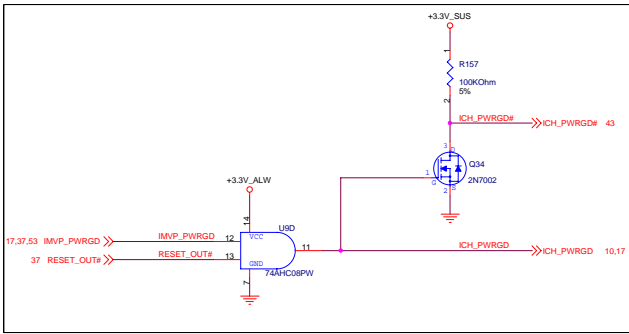
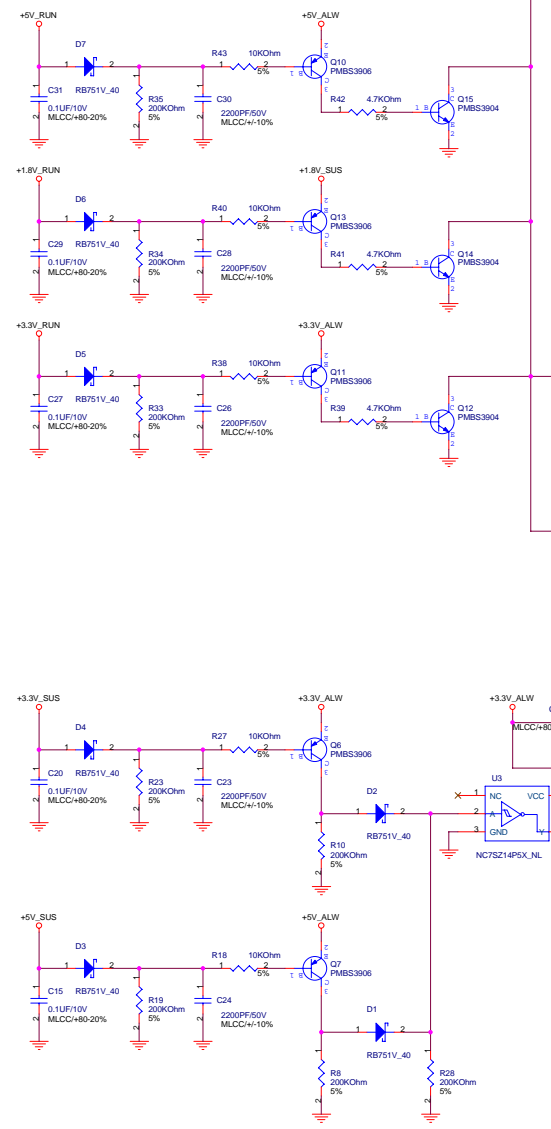


NO. 20

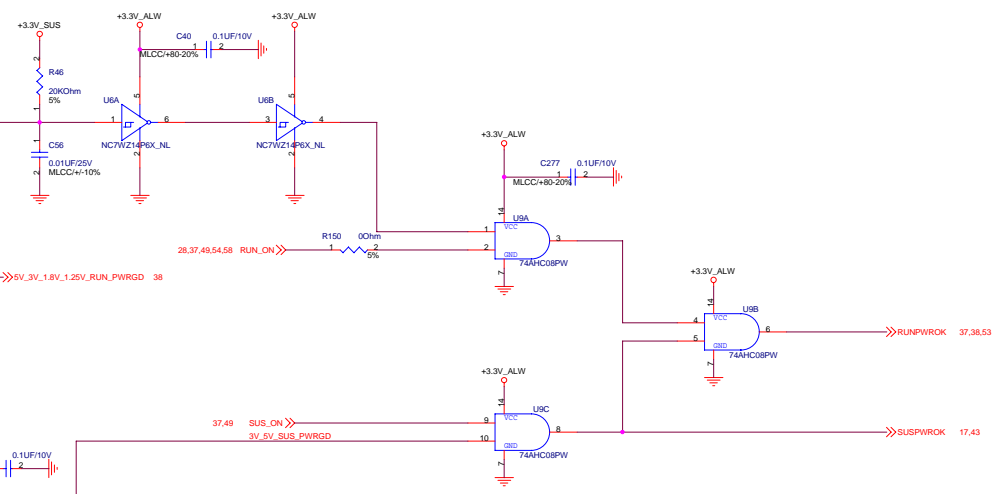


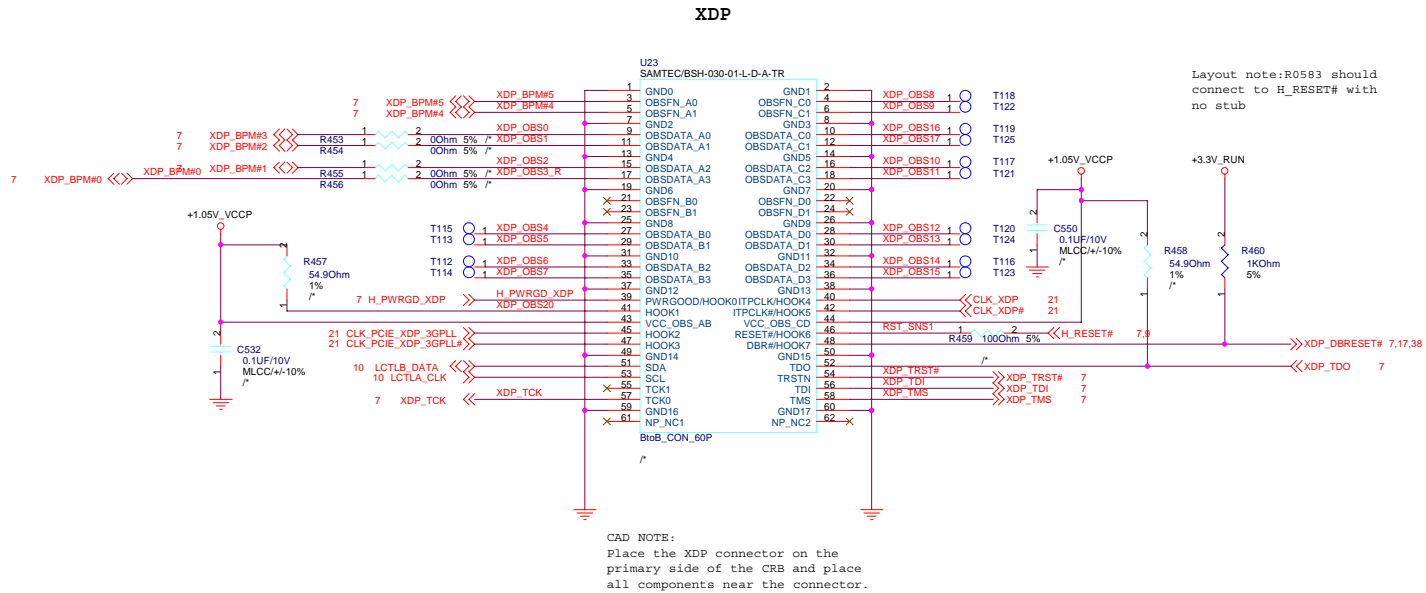
<Variant Name>

Discrete



Keep Away from high speed buses





<Variant Name>



**PROJECT: Lanai**

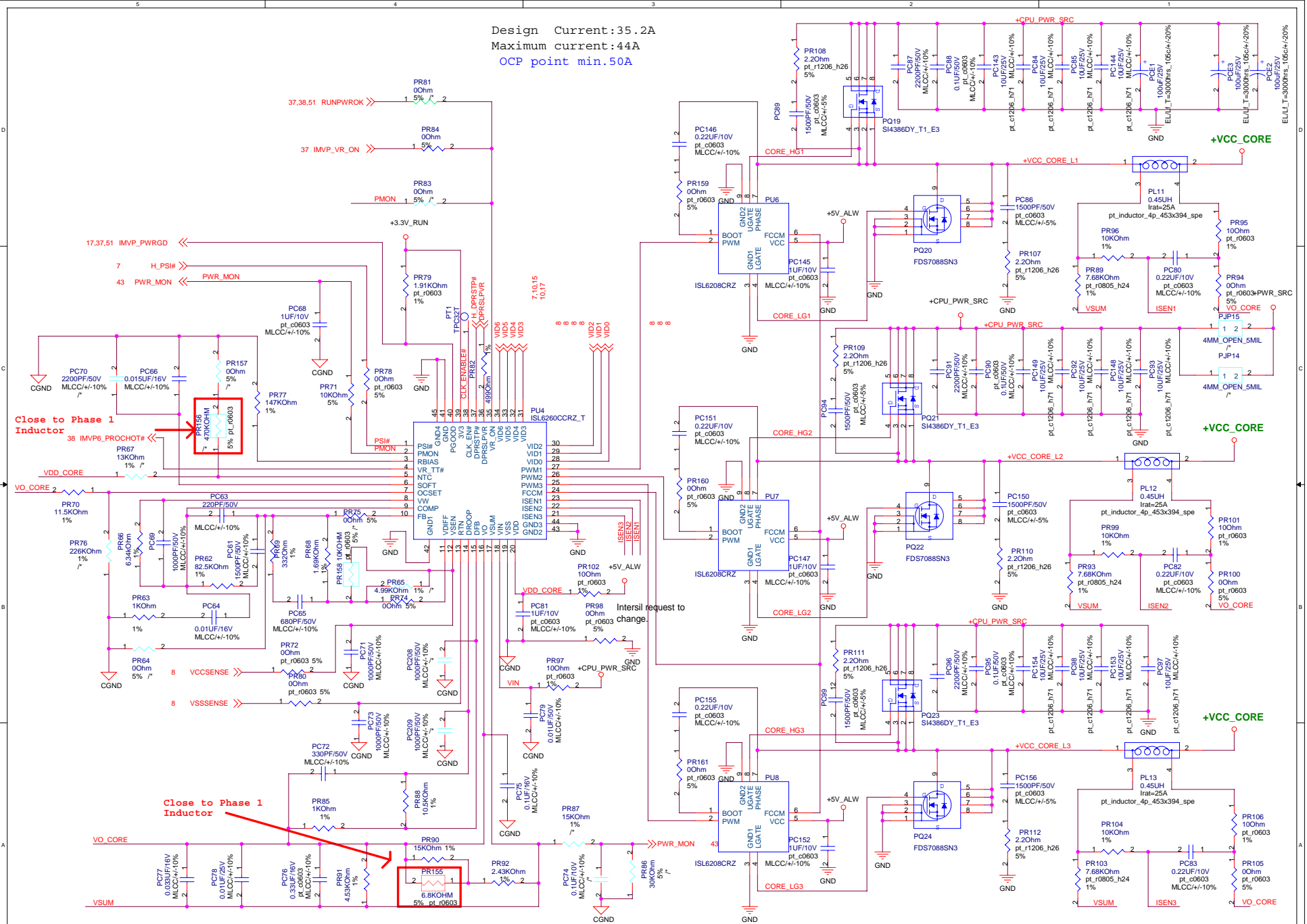
REVISION	DATE: <b>Monday, March 19, 2007</b>
<b>1.2</b>	SHEET <b>52</b> OF <b>69</b>

DESCRIPTION: **XDP**

SCHEMATIC FILE NAME: **<OrgName>**  
RELEASE DATE:

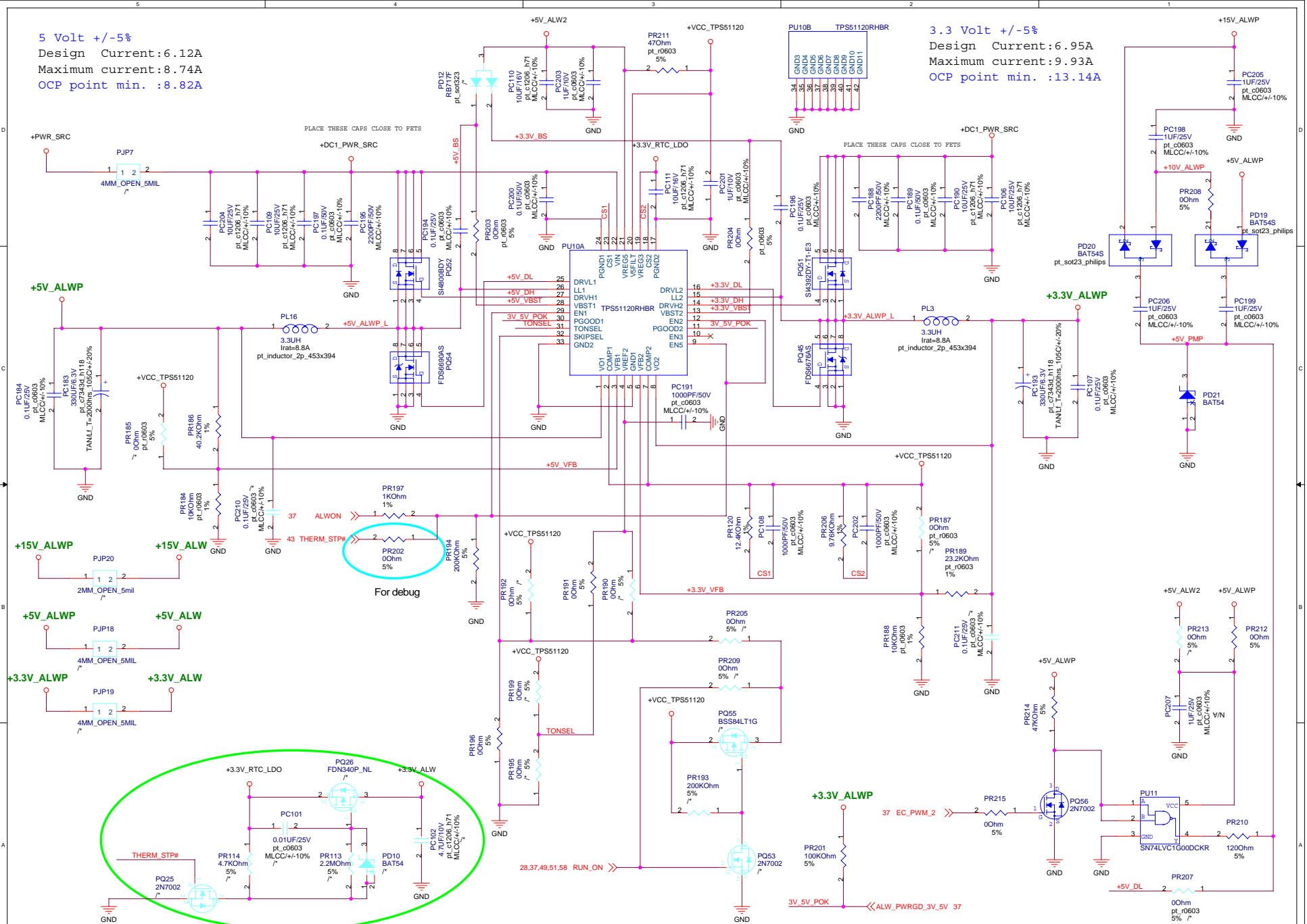
DESIGN ENGINEER:  
**Terry Lin**

Design Current:35.2A  
 Maximum current:44A  
 OCP point min.50A



5 Volt +/-5%  
 Design Current:6.12A  
 Maximum current:8.74A  
 OCP point min. :8.82A

3.3 Volt +/-5%  
 Design Current:6.95A  
 Maximum current:9.93A  
 OCP point min. :13.14A



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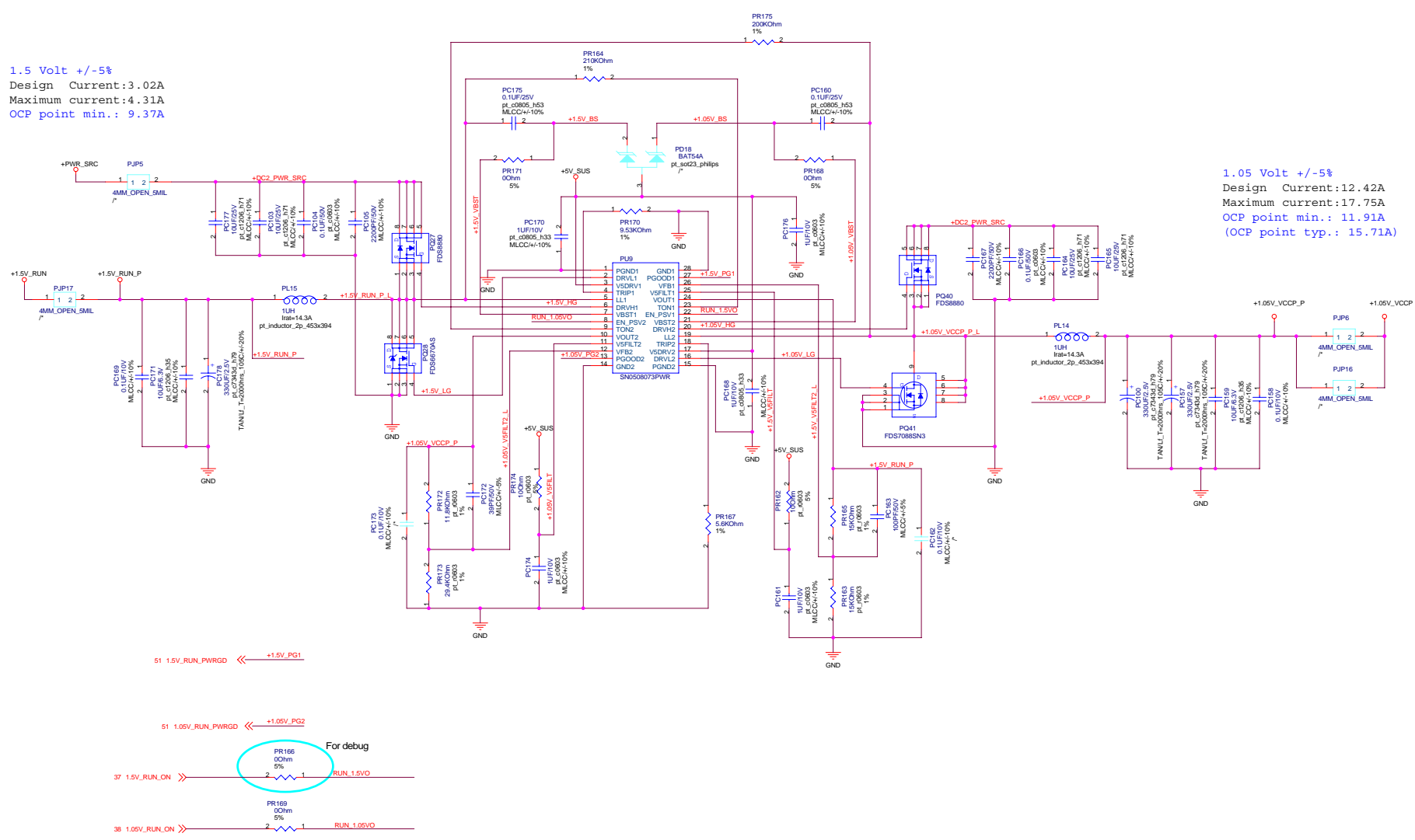
DESCRIPTION: POWER\_SYSTEM 5V\_ALW&3.3V\_ALW

SCHEMATIC FILE NAME: <OrgName>  
 RELEASE DATE:

DESIGN ENGINEER: JEFF

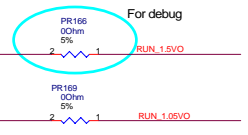
1.5 Volt +/-5%  
 Design Current:3.02A  
 Maximum current:4.31A  
 OCP point min.: 9.37A

1.05 Volt +/-5%  
 Design Current:12.42A  
 Maximum current:17.75A  
 OCP point min.: 11.91A  
 (OCP point typ.: 15.71A)



51 1.5V\_RUN\_PWRGD << +1.5V\_PG1

51 1.05V\_RUN\_PWRGD << +1.05V\_PG2



PROJECT: Lanai

REVISION 1.1 DATE: Monday, March 19, 2007 SHEET 55 OF 69

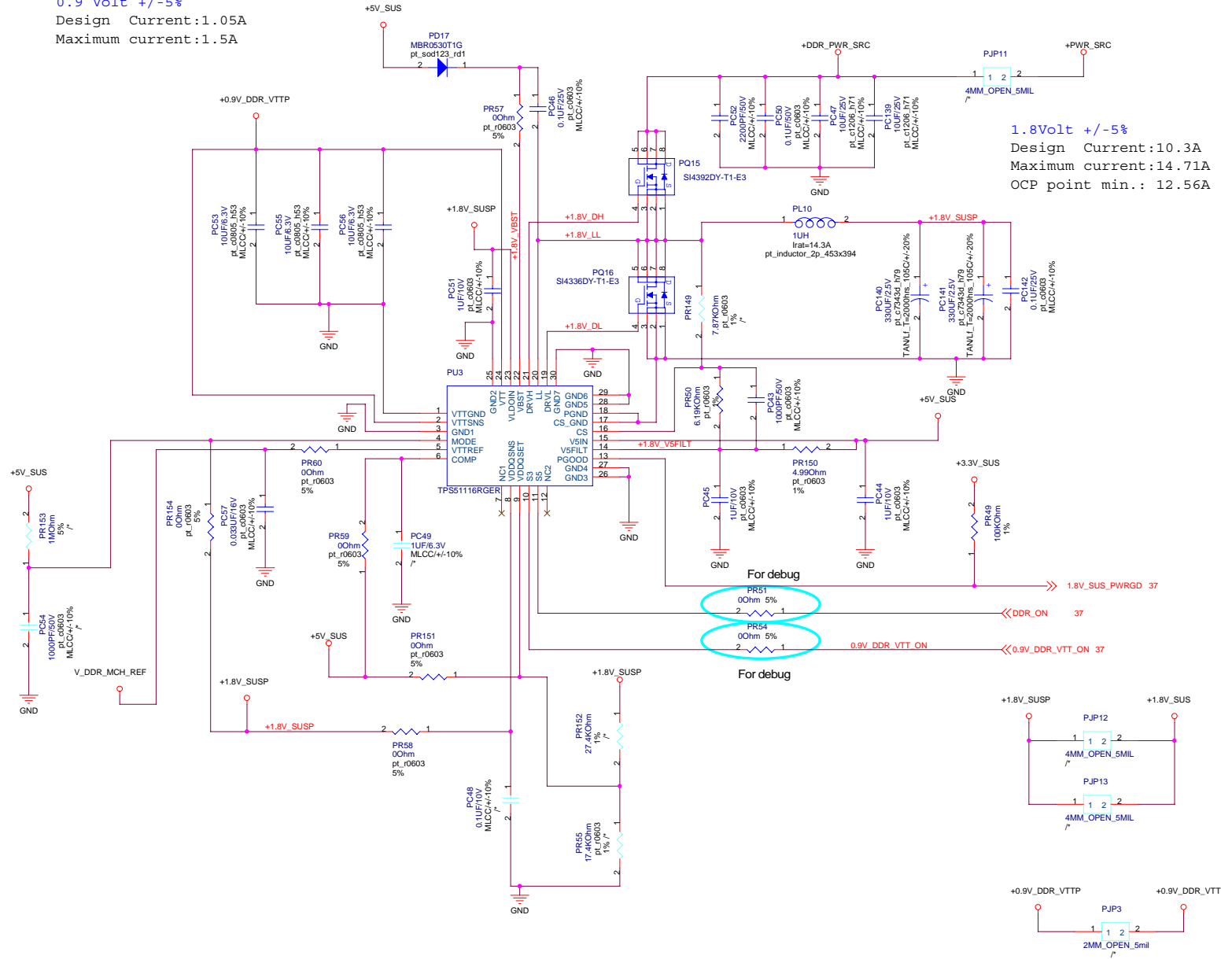
DESCRIPTION: POWER I/O 1.5VS & 1.05VS

SCHEMATIC FILE NAME: <OrgName> RELEASE DATE:

DESIGN ENGINEER: JEFF

0.9 Volt +/-5%  
 Design Current:1.05A  
 Maximum current:1.5A

1.8Volt +/-5%  
 Design Current:10.3A  
 Maximum current:14.71A  
 OCP point min.: 12.56A



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 DATE: Monday, March 19, 2007  
 SHEET: 56 OF 69

DESCRIPTION: POWER\_I/O\_DDR & VTT

SCHEMATIC FILE NAME: <OrgName>  
 RELEASE DATE:

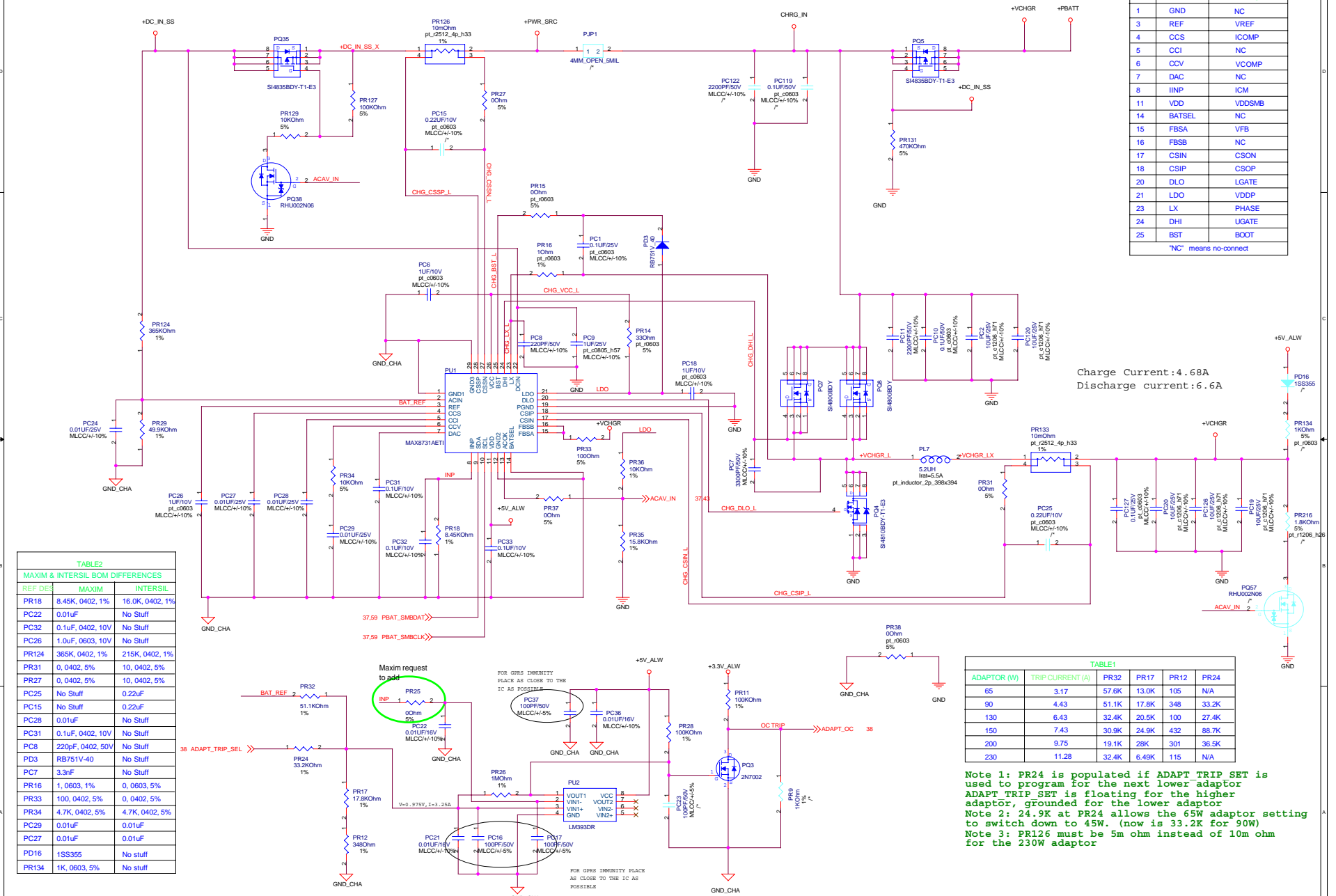
DESIGN ENGINEER: JEFF



TOTAL POWER=90W  
-->4.62A

TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	LGATE
25	BST	BOOT

"NC" means no-connect



Charge Current:4.68A  
Discharge current:6.6A

TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR18	8.45K, 0402, 1%	16.0K, 0402, 1%
PC22	0.01uF	No Stuff
PC32	0.1uF, 0402, 10V	No Stuff
PC26	1.0uF, 0603, 10V	No Stuff
PR124	365K, 0402, 1%	215K, 0402, 1%
PR31	0, 0402, 5%	10, 0402, 5%
PR27	0, 0402, 5%	10, 0402, 5%
PC25	No Stuff	0.22uF
PC15	No Stuff	0.22uF
PC28	0.01uF	No Stuff
PC31	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD3	RB751V-40	No Stuff
PC7	3.3nF	No Stuff
PR16	1, 0603, 1%	0, 0603, 5%
PR33	100, 0402, 5%	0, 0402, 5%
PR24	4.7K, 0402, 5%	4.7K, 0402, 5%
PC29	0.01uF	0.01uF
PC27	0.01uF	0.01uF
PD16	1SS355	No stuff
PR134	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR32	PR17	PR12	PR24
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR24 is populated if ADAPT TRIP SET is used to program for the next lower adaptor  
ADAPT TRIP SET is floating for the higher adaptor, grounded for the lower adaptor  
Note 2: 24.9K at PR24 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)  
Note 3: PR126 must be 5m ohm instead of 10m ohm for the 230W adaptor



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REVISION: 1.1  
DATE: Monday, March 19, 2007  
SHEET: 57 OF 69

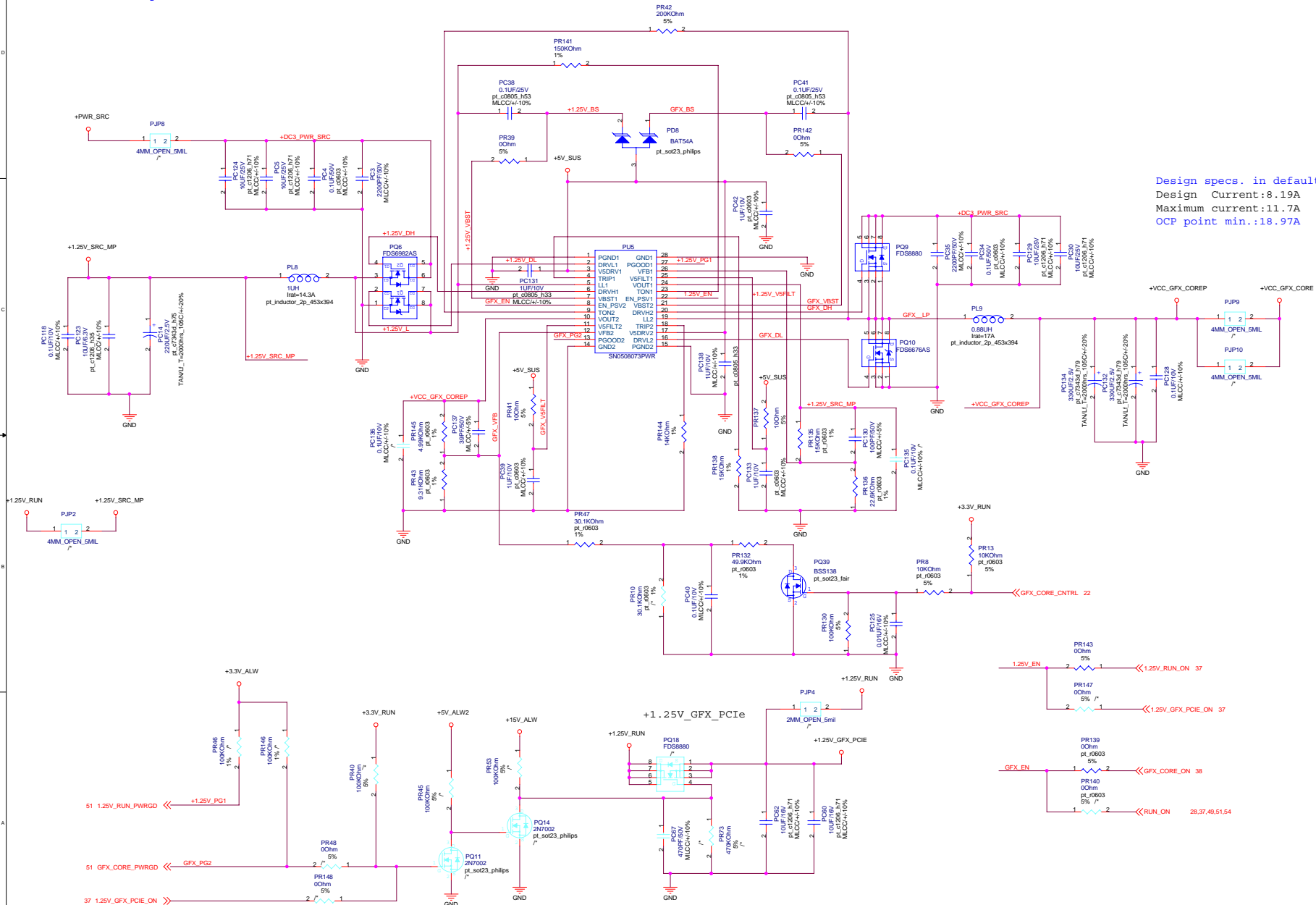
DESCRIPTION: POWER CHARGER

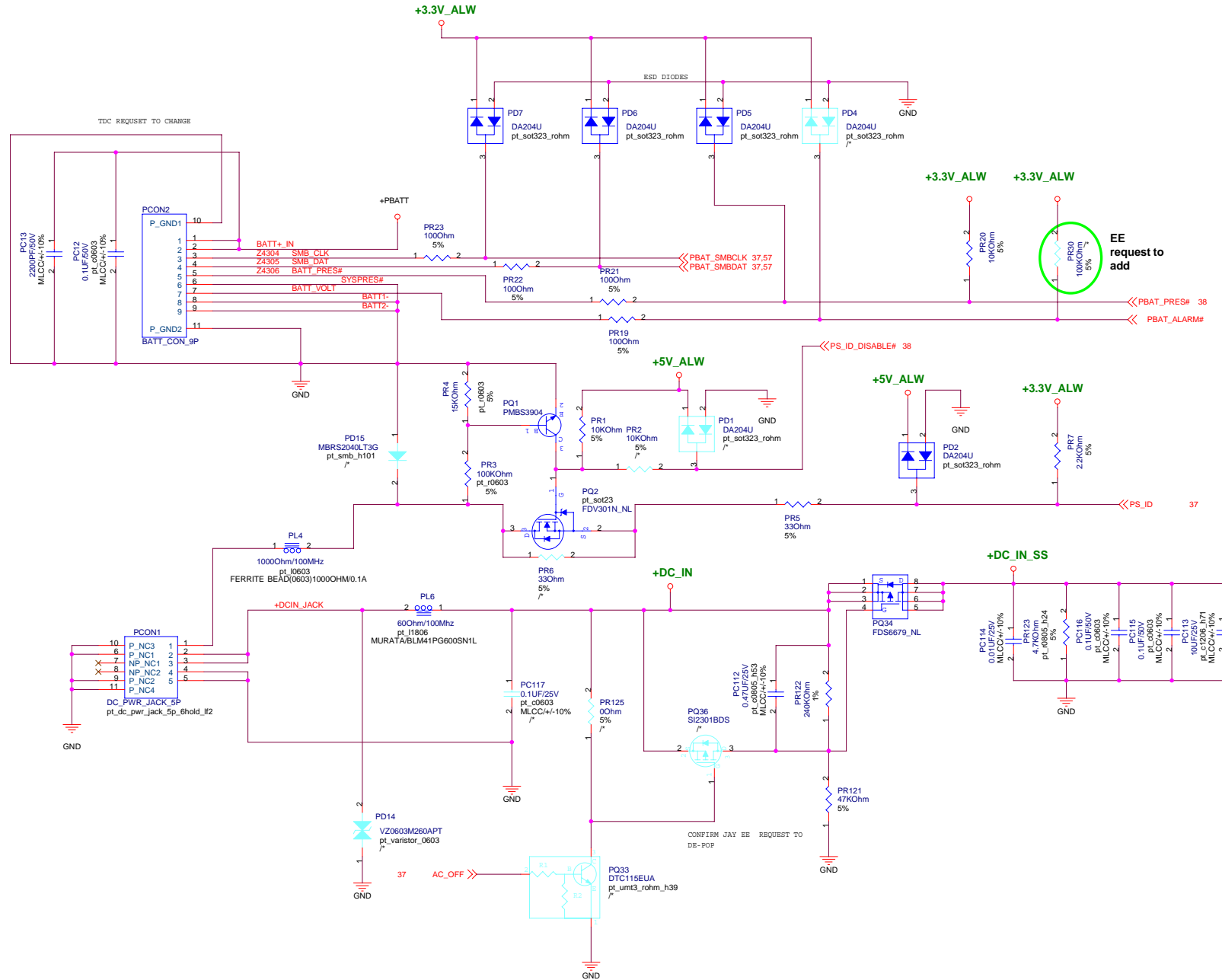
SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

DESIGN ENGINEER: JEFF

1.25Volt +/-5%  
 Design Current:2.26A  
 Maximum current:3.23A  
 OCP point min. : 9.59A

Design specs. in default:  
 Design Current:8.19A  
 Maximum current:11.7A  
 OCP point min.:18.97A





PROJECT: Lanai

REVISION  
1.1

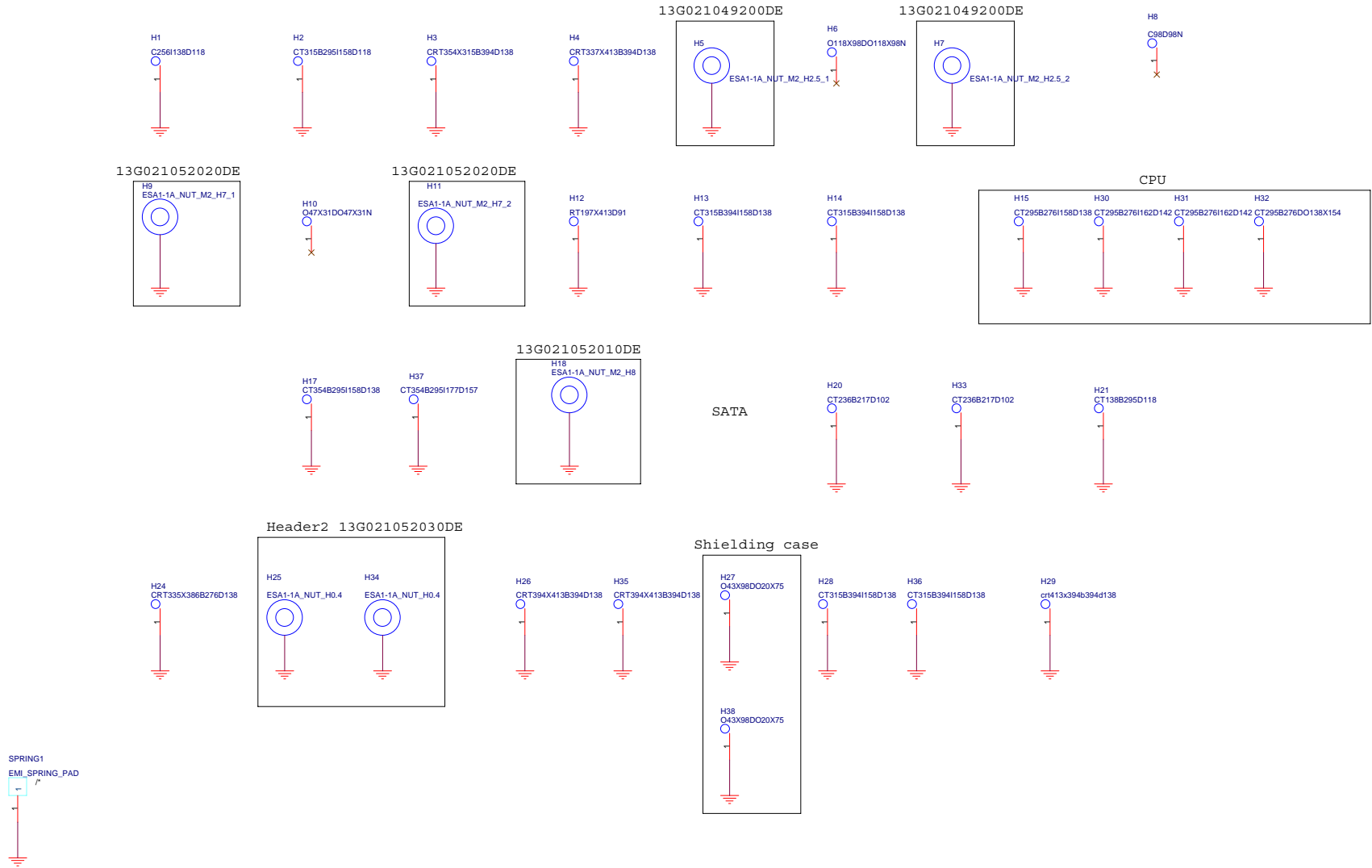
DATE: Monday, March 19, 2007  
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DESCRIPTION: POWER\_CONNECTOR

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :  
JEFF

PM screw pad



PROJECT: Lanai

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DATE: Monday, March 19, 2007  
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DESCRIPTION: SCREW PAD

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER : Sean Kuo

# ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

## Lanai USB Board

REV :1.1(DELL: X01)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

*BOM NO. ???*

*PCB P/N: ???*



PROJECT: **Lanai**

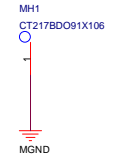
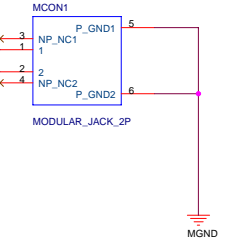
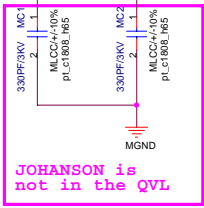
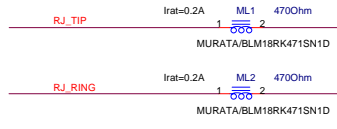
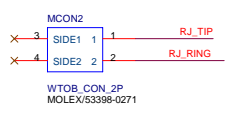
REVISION  
**1.2**

DATE: **Monday, March 19, 2007**  
SHEET **65** OF **69**

DESCRIPTION: **Cover Page**

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
**Terry Lin**



PROJECT: Lanai

REVISION 1.2  
DATE: Monday, March 19, 2007  
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DESCRIPTION: RJ-11 CONN

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

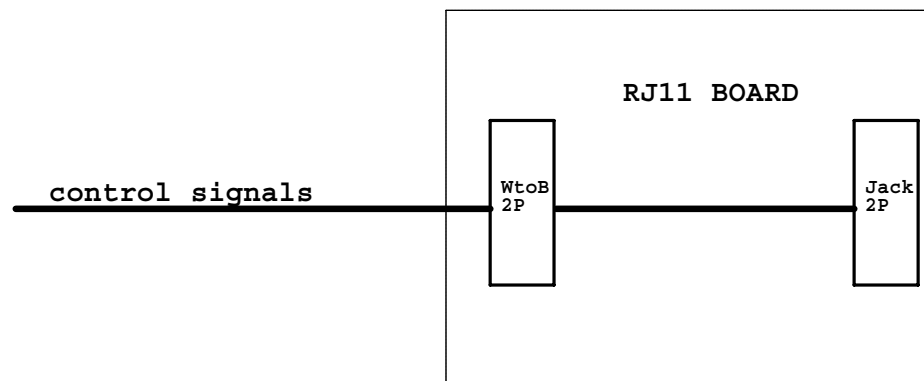
DESIGN ENGINEER : Stanly Hsu

**ASUS CONFIDENTIAL**

MODEL NAME : *Elsa*

## *Lanai Modem Board*

**REV :1.1(DELL: X01)**



PROJECT: Lanai

REVISION  
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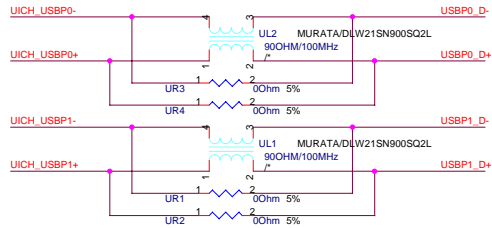
DATE: Monday, March 19, 2007  
SHEET 68 OF 69

DESCRIPTION:  
BLOCK DIAGRAM

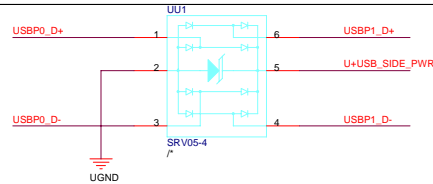
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
Stanly Hsu

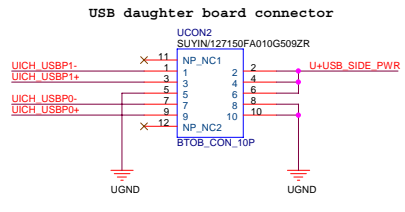
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .



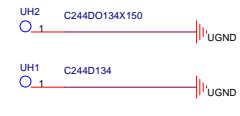
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



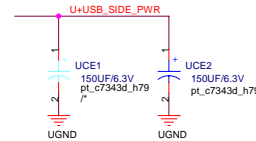
Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C ( 1pf vs 3pf ) .



**Screw hole**

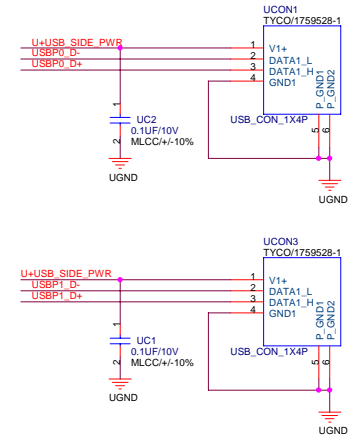


Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.



PROJECT: Lanai

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DATE: Monday, March 19, 2007  
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DESCRIPTION:

USB PORT ( SINGLE 2 )

SCHEMATIC FILE NAME :  
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :

Terry Lin