

# COMPAL CONFIDENTIAL

MODEL NAME : **IBQ00**

PCB NO : **LA-3302P ( DAA00000K0L)**

BOM P/N : **45144731L01**

## M08 (DIS) Briscoe

### uFCPGA Mobile Merom Intel Crestline + ICH8M

2007-03-07

**REV : 0.4 (X03)**

**@ : Nopop Component**  
**1@ : Populate for G72MV**  
**2@ : Populate for G86MV**  
**45144731L01 pop for G86MV**  
**45144XXXXX pop for G72MV**

#### MB PCB

Part Number	Description
DAA00000K0L	PCB 2GX LA-3302P REV0 M/B DIS

hexainf@hotmail.com  
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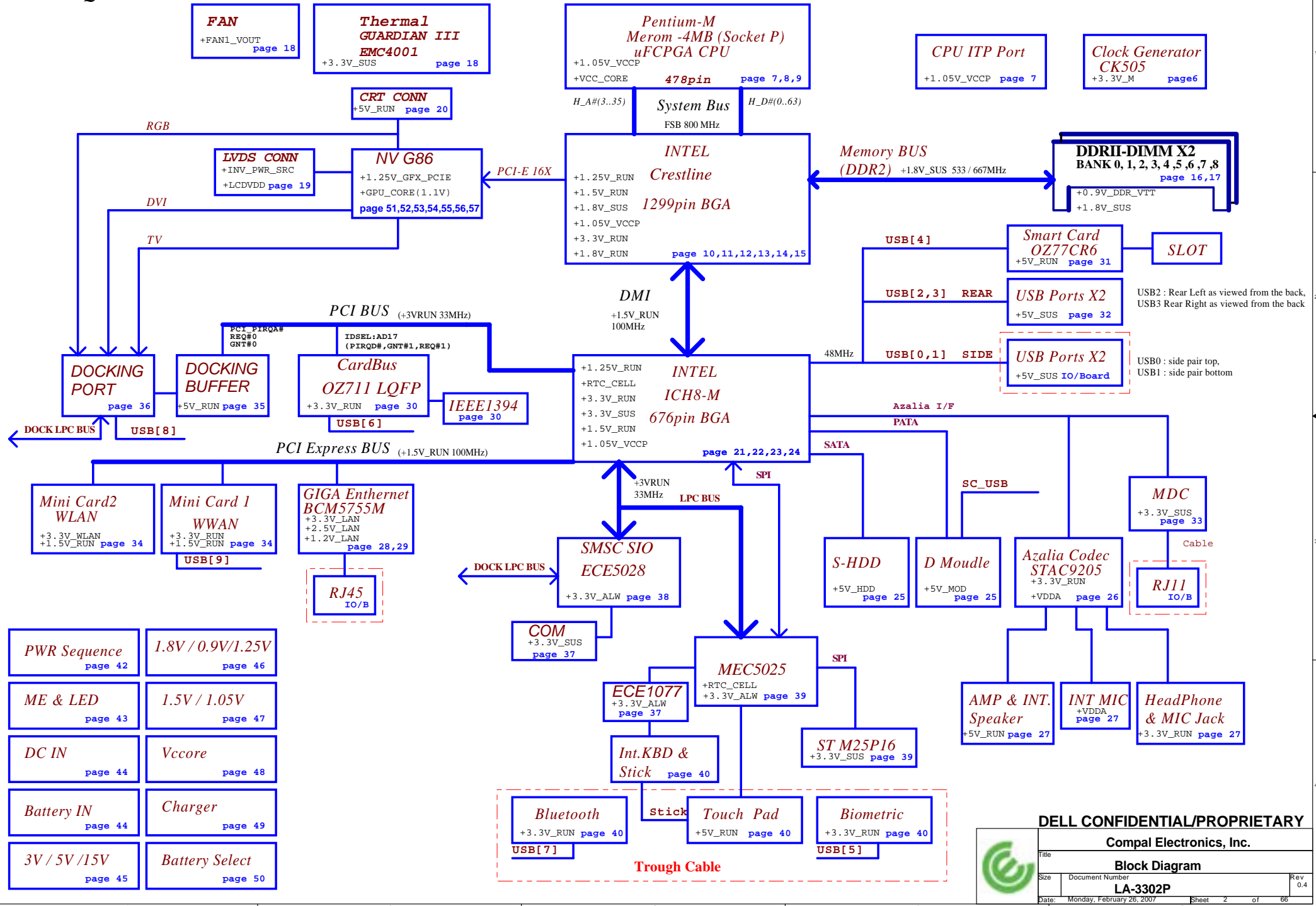


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Cover Sheet		
Title		
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**Block Diagram**  
**Compal confidential**  
**Model : IBQ01**



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Title		
Block Diagram		
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**POWER STATES**

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

**PM TABLE**

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +VCC_+1P2V_GPU_CORE +0.9V_DDR_VTT +GPU_CORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.25V_M +1.05V_M	+1.25V_M +3.3V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

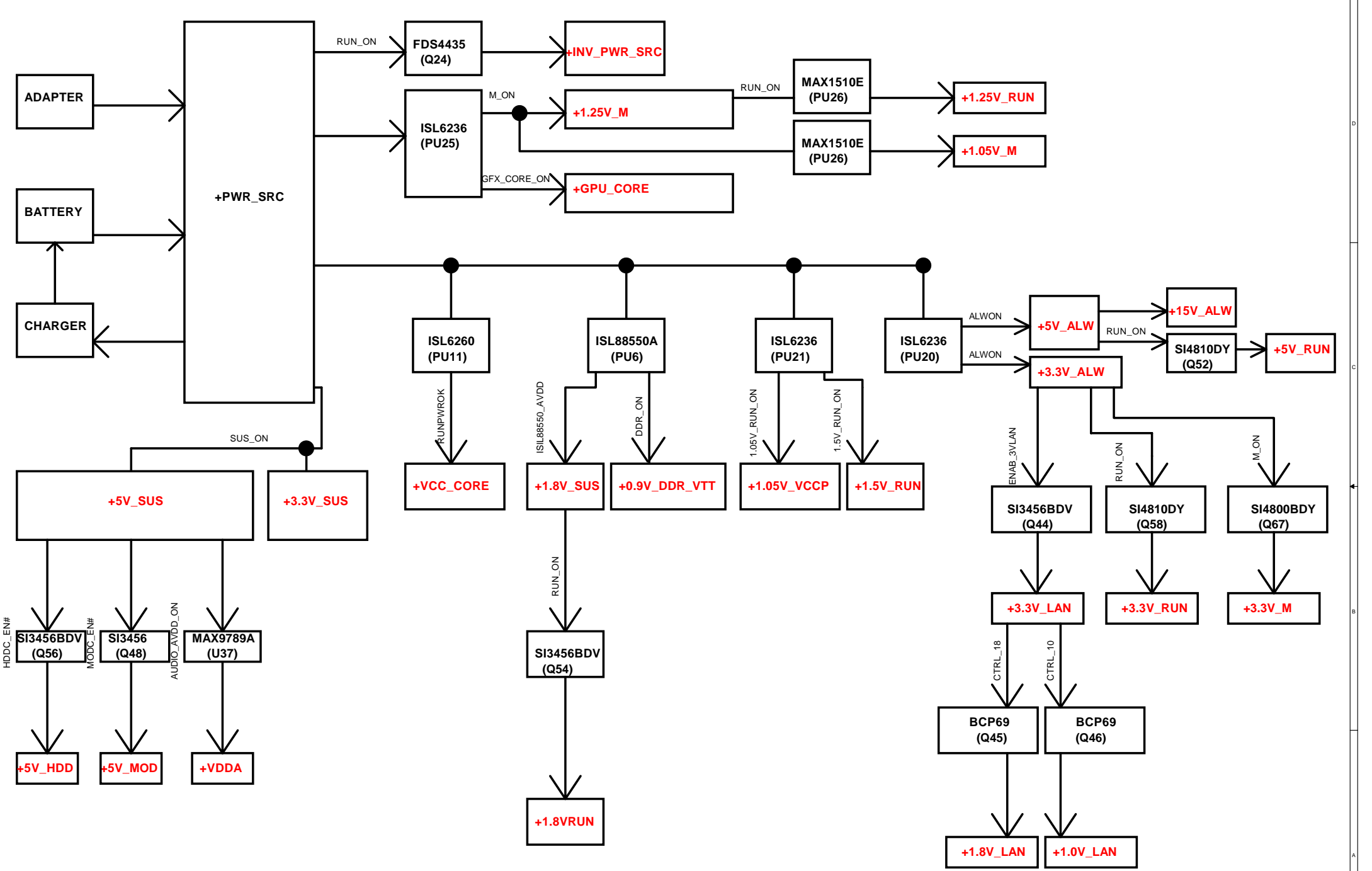
**PCI TABLE**

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
OZ711	AD17	REQ#1 / GNT#1	PIRQD
Docking	AD24	REQ#0 / GNT#0	PIRQA

	USB PORT#	DESTINATION
<b>ICH8-M</b>	0	Side Top
	1	Side Bottom
	2	Rear Left
	3	Rear Right
	4	Smart Card
	5	Biometric
	6	Card Bus
	7	Bluetooth
	8	Docking
	9	WWAN
<b>ECE 5028</b>	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	GIGA LAN



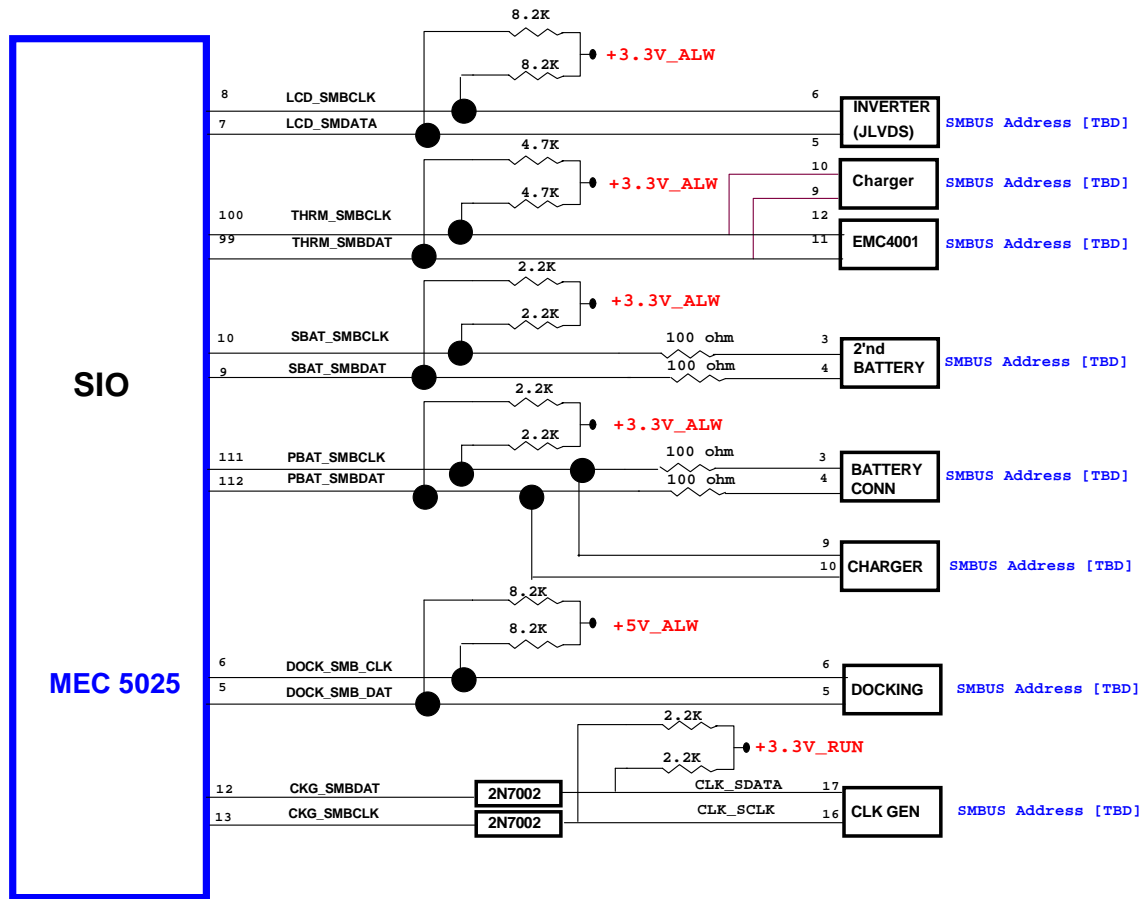
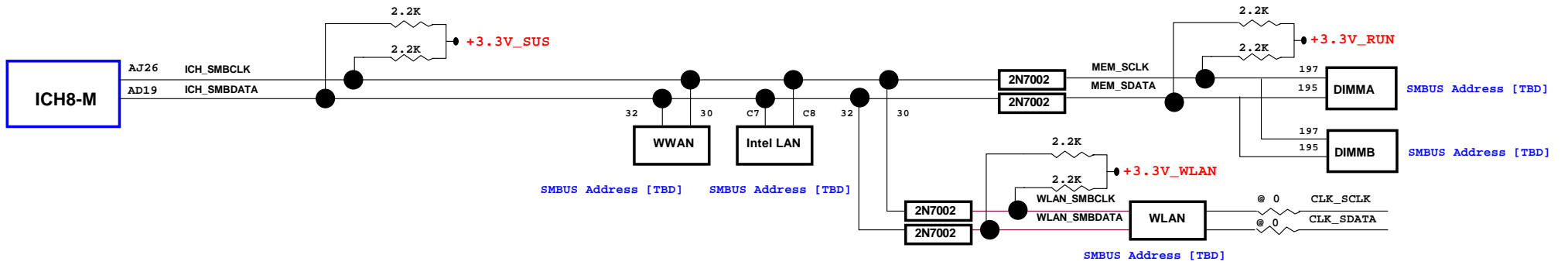


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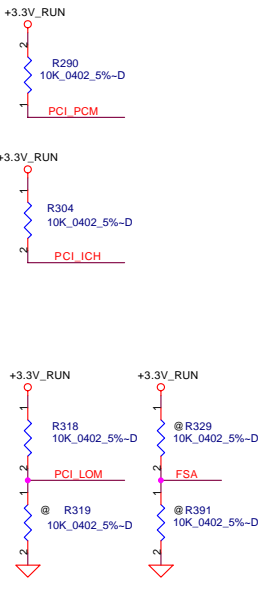
<b>Compal Electronics, Inc.</b>		
<b>Power Rail</b>		
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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSELO	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	200	100	33.3

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1



Populate R697,R833 for G72MV  
Populate R286 for G86MV.  
R833,R286 place overlap

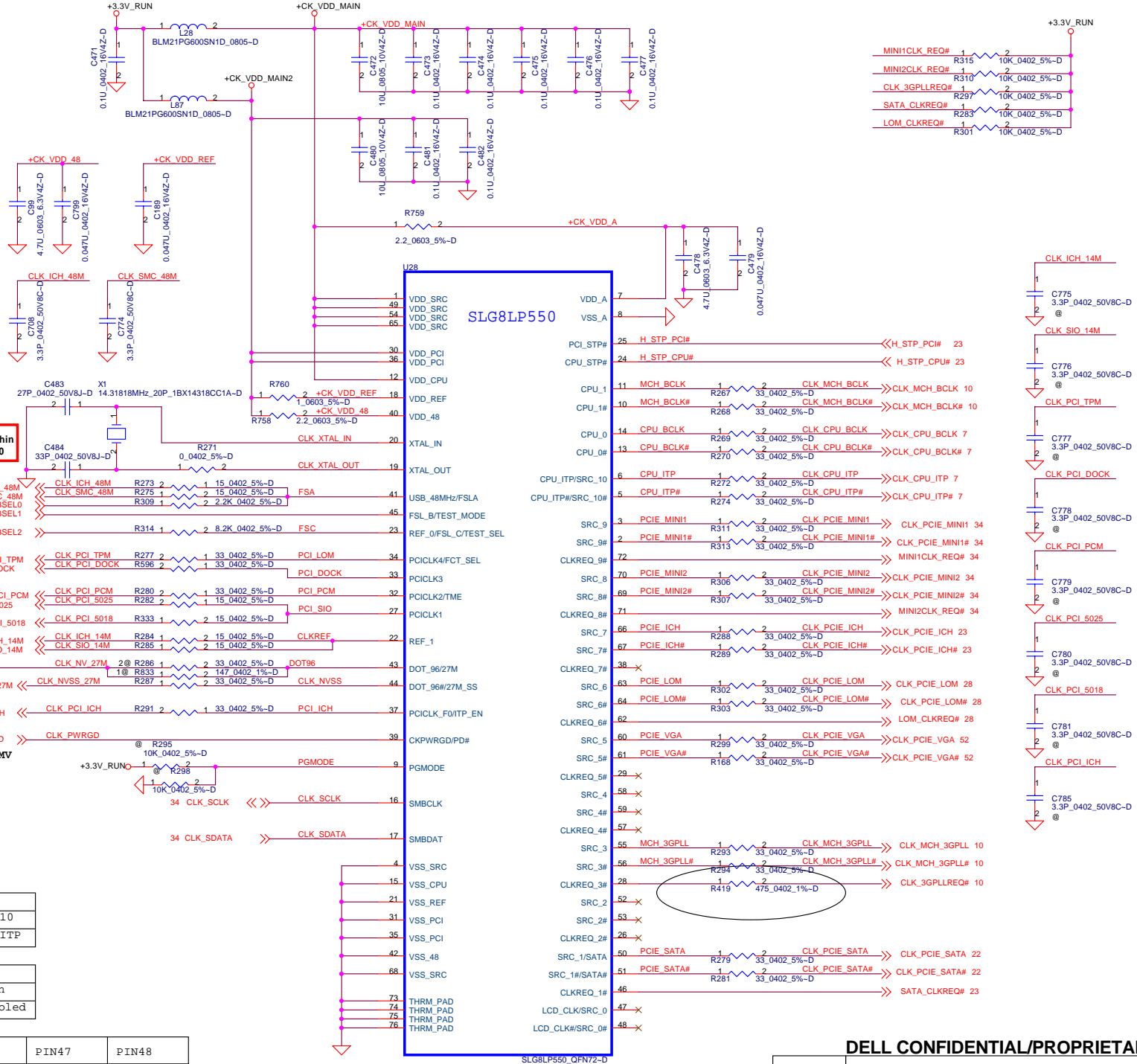
PGMODE	PIN 9
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

TME	PIN 32
0	Normal Operation
1	Trusted Mode Enabled

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

Place crystal within 500 mils of CK410

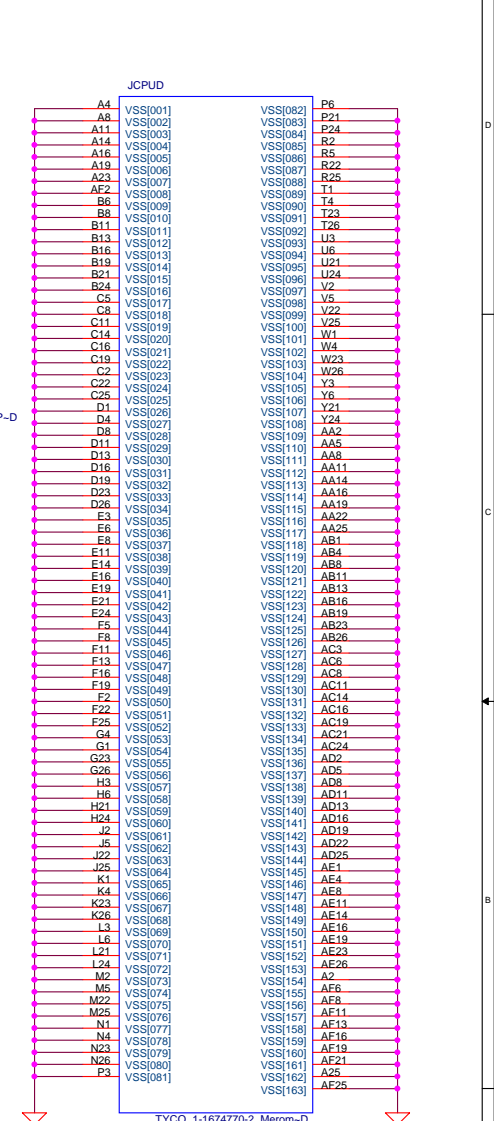
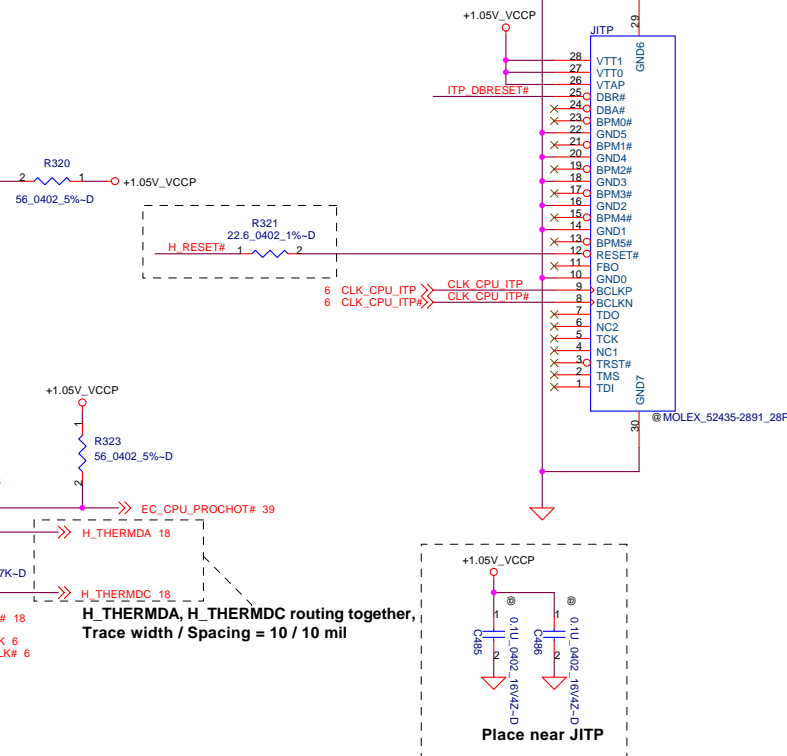
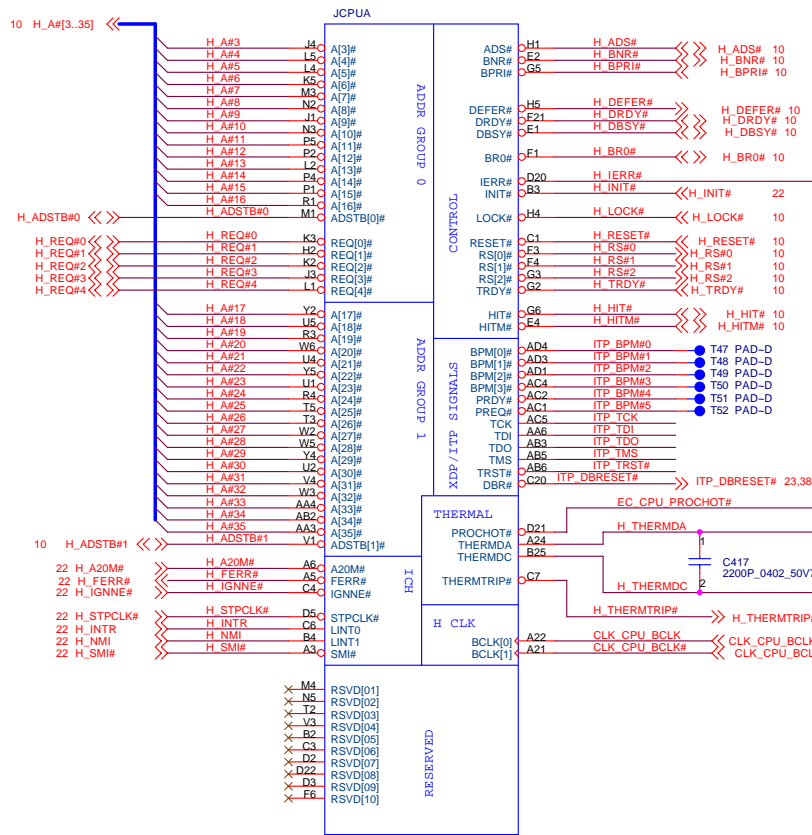


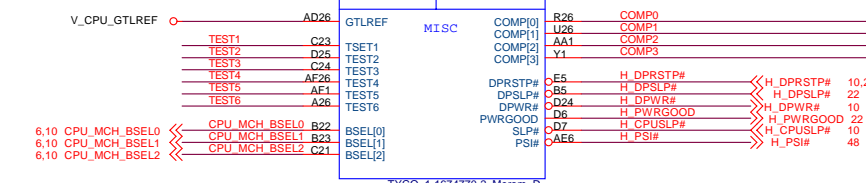
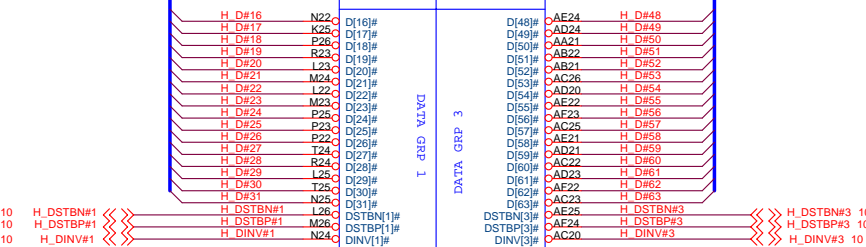
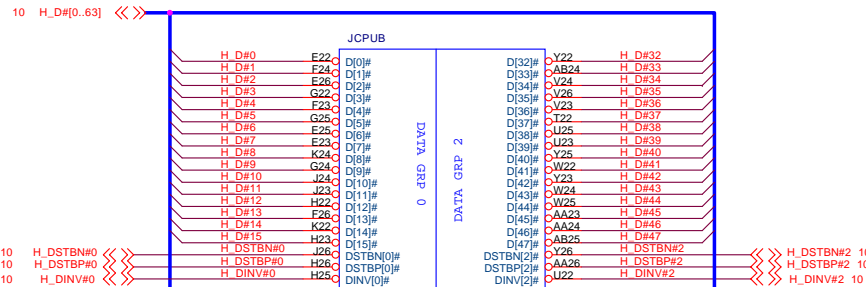
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Compal Electronics, Inc.			
Clock Generator			
LA-3302P			
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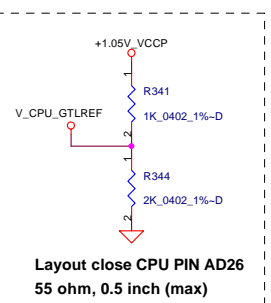




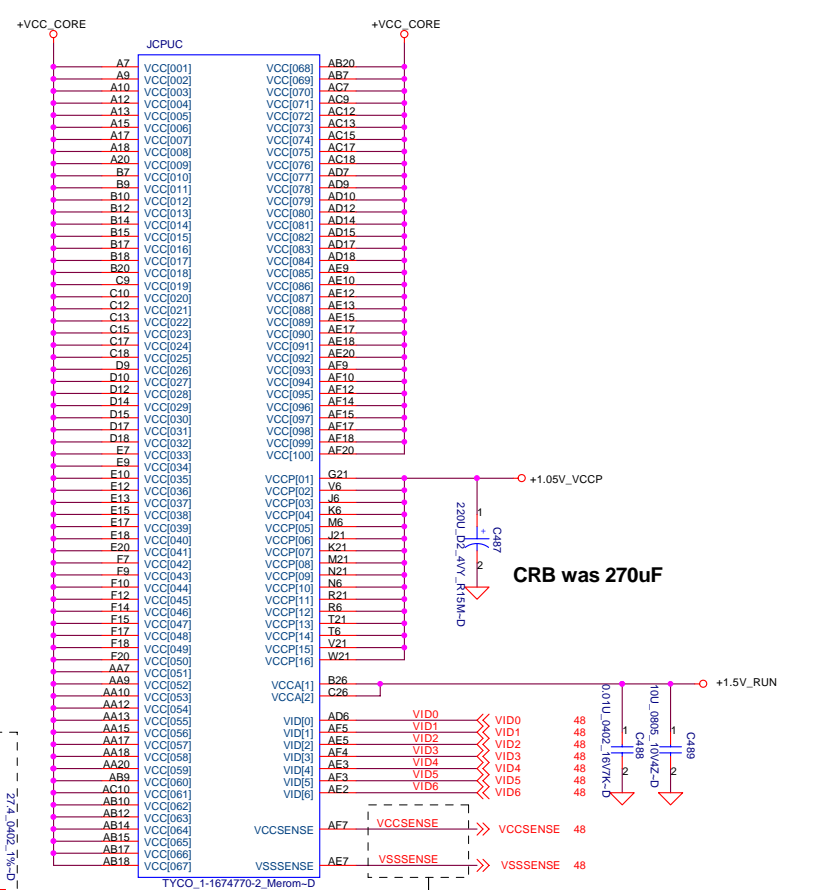
**Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.**

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

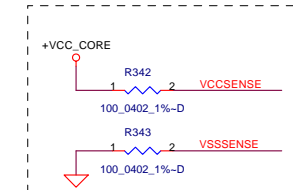


Layout close CPU PIN AD26  
55 ohm, 0.5 inch (max)



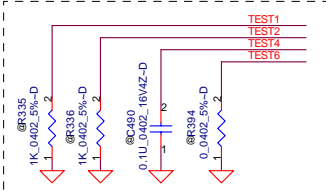
Length match within 25 mils, Z0=27.4 ohm

Place R342 and R343 near CPU



Route VCCSSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing and 1 inch (max)

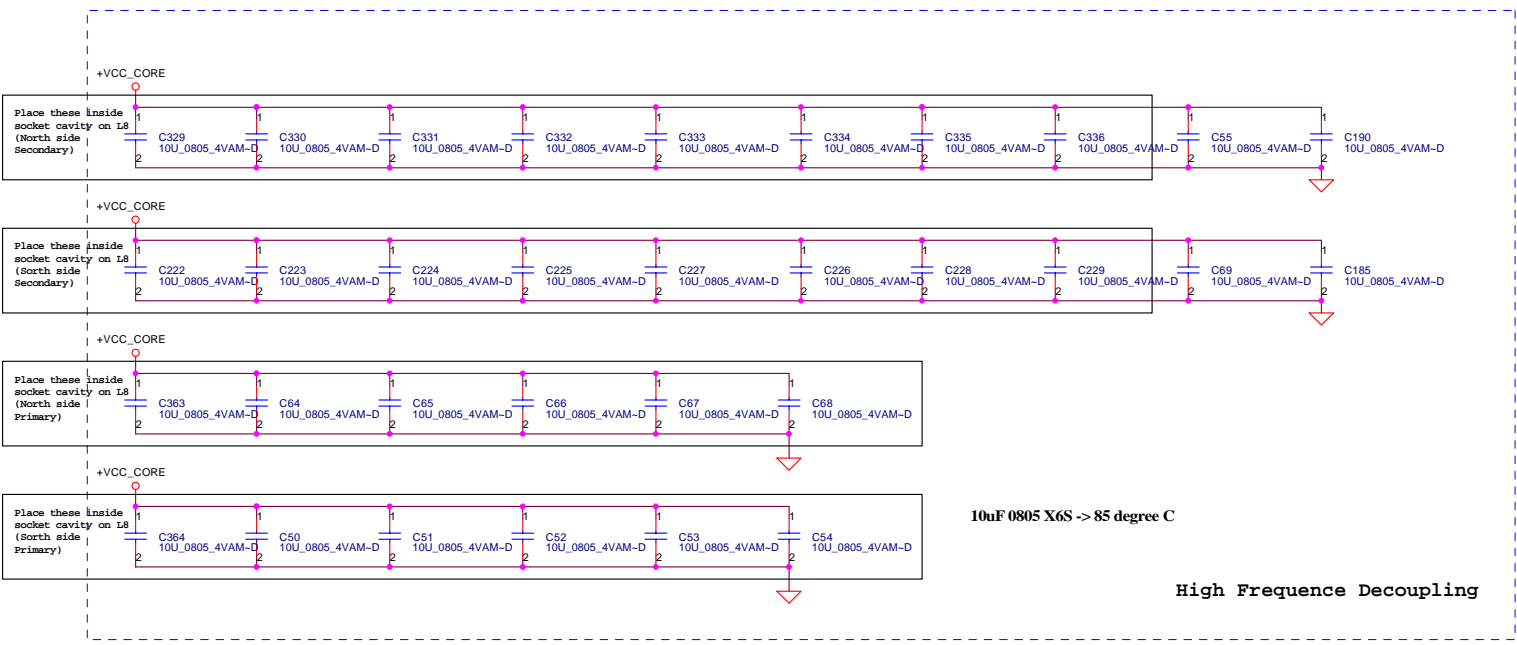
Place C490 close to the CPU TEST4 pin. Make sure CPU\_TEST4 routing is reference to GND and away from other noisy signal.



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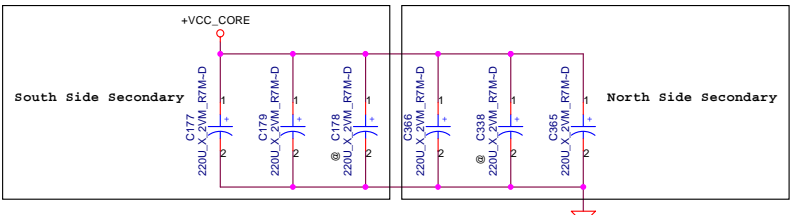




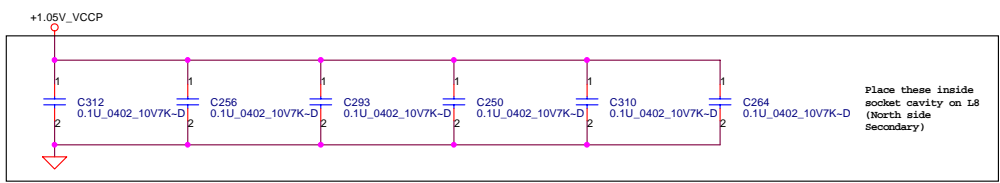
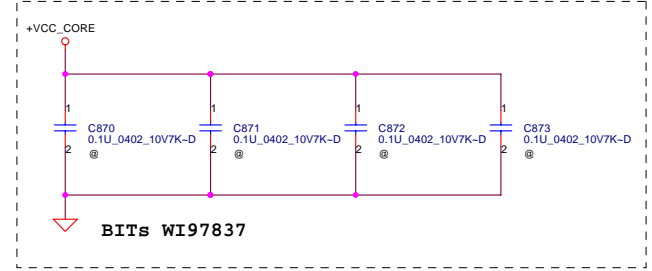
10uF 0805 X6S -> 85 degree C

High Frequency Decoupling

Near VCORE regulator.



ESR <= 1.5m ohm  
Capacitor > 1980uF



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8 H\_D#0[0.63] <<>

H_D#0	E2	H_D#_0
H_D#1	C2	H_D#_1
H_D#2	G2	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	V8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AC3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AH6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ2	H_D#_58
H_D#59	AE5	H_D#_59
H_D#60	AJ3	H_D#_60
H_D#61	AH2	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

J13	H_A#3	H_A#3
C11	H_A#5	H_A#5
M11	H_A#6	H_A#6
C15	H_A#7	H_A#7
F16	H_A#8	H_A#8
L13	H_A#9	H_A#9
G17	H_A#10	H_A#10
C14	H_A#11	H_A#11
K16	H_A#12	H_A#12
B13	H_A#13	H_A#13
L16	H_A#14	H_A#14
J17	H_A#15	H_A#15
B14	H_A#16	H_A#16
K18	H_A#17	H_A#17
P15	H_A#18	H_A#18
R17	H_A#19	H_A#19
B16	H_A#20	H_A#20
H20	H_A#21	H_A#21
L19	H_A#22	H_A#22
D17	H_A#23	H_A#23
M17	H_A#24	H_A#24
N16	H_A#25	H_A#25
J19	H_A#26	H_A#26
B18	H_A#27	H_A#27
E19	H_A#28	H_A#28
B17	H_A#29	H_A#29
B15	H_A#30	H_A#30
E17	H_A#31	H_A#31
C18	H_A#32	H_A#32
A19	H_A#33	H_A#33
B18	H_A#34	H_A#34
N19	H_A#35	H_A#35

H_ADS#	H_ADS#	H_ADS#	7
H_ADSTB#_0	G12	H_ADSTB#0	7
H_ADSTB#_1	G20	H_ADSTB#1	7
H_BNR#	C8	H_BNR#	7
H_BPR#	E8	H_BPR#	7
H_BRD#	E12	H_BRD#	7
H_DEFER#	C10	H_DEFER#	7
H_DBSY#	D16	H_DBSY#	7
CLK_MCH_BCLK_6	AM5	CLK_MCH_BCLK_6	6
CLK_MCH_BCLK#_6	AM7	CLK_MCH_BCLK#_6	6
H_DRDY#	K7	H_DRDY#	7
H_HIT#	E4	H_HIT#	7
H_HITM#	C6	H_HITM#	7
H_LOCK#	G10	H_LOCK#	7
H_TRDY#	B7	H_TRDY#	7

H_DIN#0	K5	H_DIN#0	8
H_DIN#1	L2	H_DIN#1	8
H_DIN#2	AD13	H_DIN#2	8
H_DIN#3	AE13	H_DIN#3	8

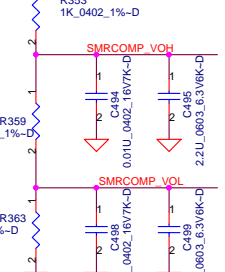
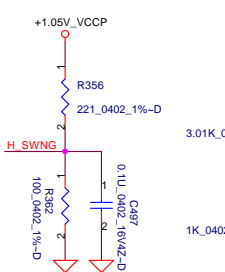
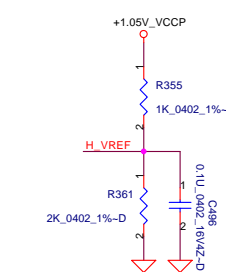
H_DSTB#_0	M7	H_DSTB#0	8
H_DSTB#_1	K3	H_DSTB#1	8
H_DSTB#_2	AD2	H_DSTB#2	8
H_DSTB#_3	AH11	H_DSTB#3	8

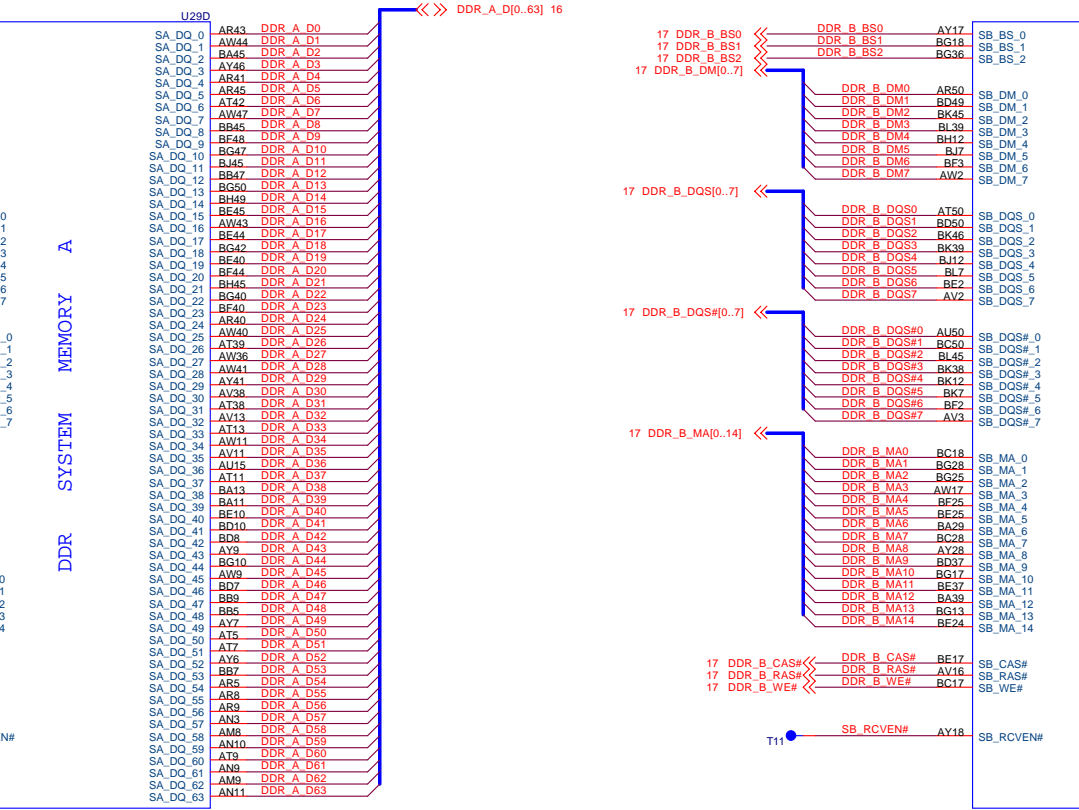
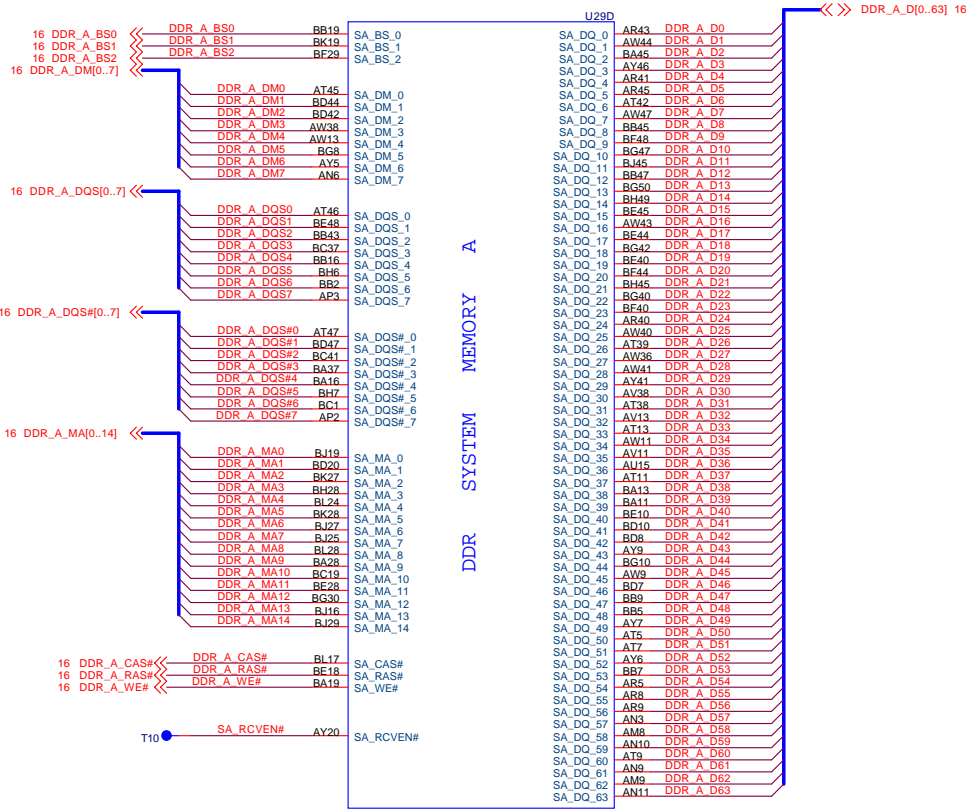
H_REQ#_0	M14	H_REQ#0	7
H_REQ#_1	E13	H_REQ#1	7
H_REQ#_2	A11	H_REQ#2	7
H_REQ#_3	B13	H_REQ#3	7
H_REQ#_4	B12	H_REQ#4	7

H_RS#_0	E12	H_RS#0	7
H_RS#_1	D7	H_RS#1	7
H_RS#_2	D8	H_RS#2	7

CL_CLK0	AM49	CL_CLK0	7
ICH_CL_PWROK	AK50	ICH_CL_PWROK	7
CL_RSTOK	AM49	CL_RSTOK	7
CL_VREF	AM50	CL_VREF	7

Layout Note: H\_RCOMP trace width and spacing is 10/20

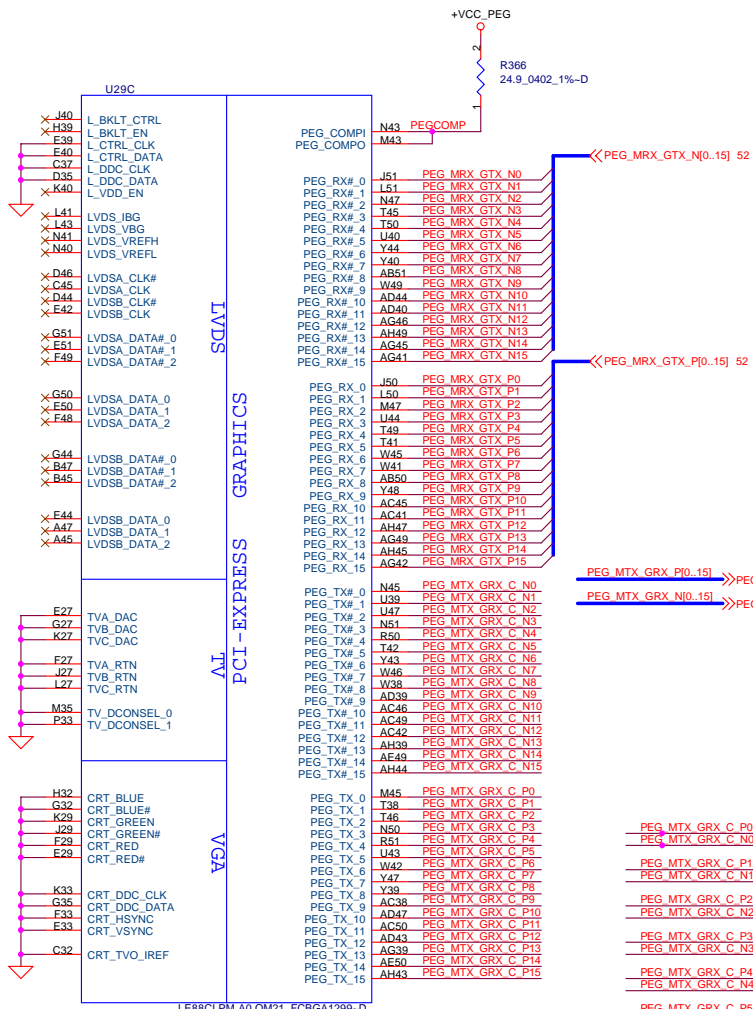




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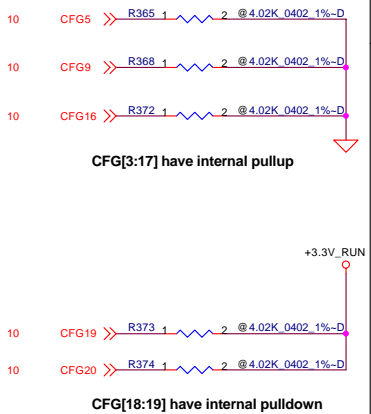
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### Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation (Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present



PEG_MTX_GRX_C_P0	C500	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P0
PEG_MTX_GRX_C_N0	C501	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N0
PEG_MTX_GRX_C_P1	C502	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P1
PEG_MTX_GRX_C_N1	C503	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N1
PEG_MTX_GRX_C_P2	C504	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P2
PEG_MTX_GRX_C_N2	C505	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N2
PEG_MTX_GRX_C_P3	C506	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P3
PEG_MTX_GRX_C_N3	C507	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N3
PEG_MTX_GRX_C_P4	C508	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P4
PEG_MTX_GRX_C_N4	C509	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N4
PEG_MTX_GRX_C_P5	C510	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P5
PEG_MTX_GRX_C_N5	C511	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N5
PEG_MTX_GRX_C_P6	C512	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P6
PEG_MTX_GRX_C_N6	C513	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N6
PEG_MTX_GRX_C_P7	C514	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P7
PEG_MTX_GRX_C_N7	C515	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N7
PEG_MTX_GRX_C_P8	C516	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P8
PEG_MTX_GRX_C_N8	C517	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N8
PEG_MTX_GRX_C_P9	C518	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P9
PEG_MTX_GRX_C_N9	C519	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N9
PEG_MTX_GRX_C_P10	C520	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P10
PEG_MTX_GRX_C_N10	C521	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N10
PEG_MTX_GRX_C_P11	C522	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P11
PEG_MTX_GRX_C_N11	C523	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N11
PEG_MTX_GRX_C_P12	C524	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P12
PEG_MTX_GRX_C_N12	C525	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N12
PEG_MTX_GRX_C_P13	C526	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P13
PEG_MTX_GRX_C_N13	C527	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N13
PEG_MTX_GRX_C_P14	C528	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P14
PEG_MTX_GRX_C_N14	C529	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N14
PEG_MTX_GRX_C_P15	C530	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_P15
PEG_MTX_GRX_C_N15	C531	1	2	0.1U	0402	10V7K-D	PEG_MTX_GRX_N15

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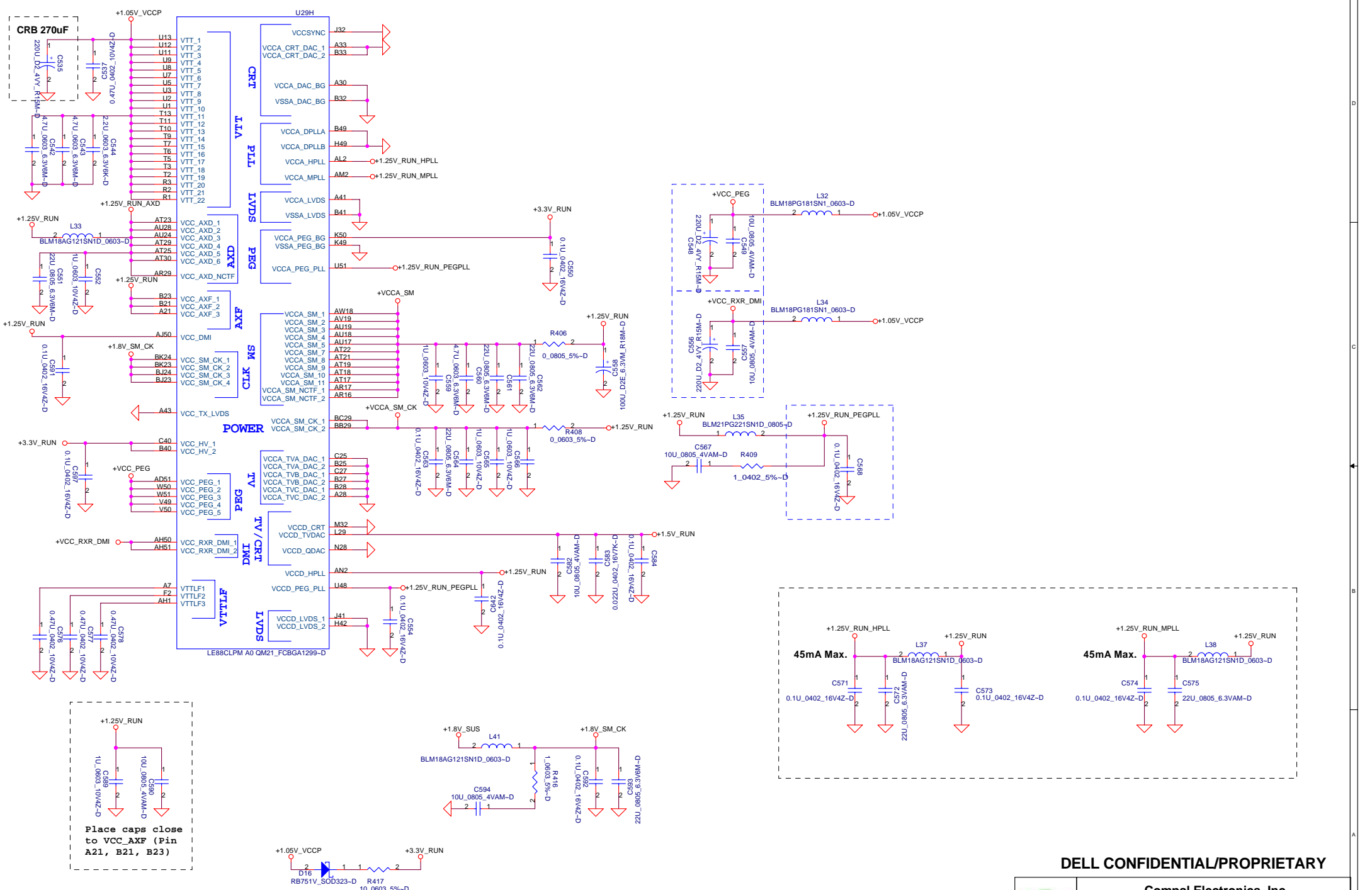
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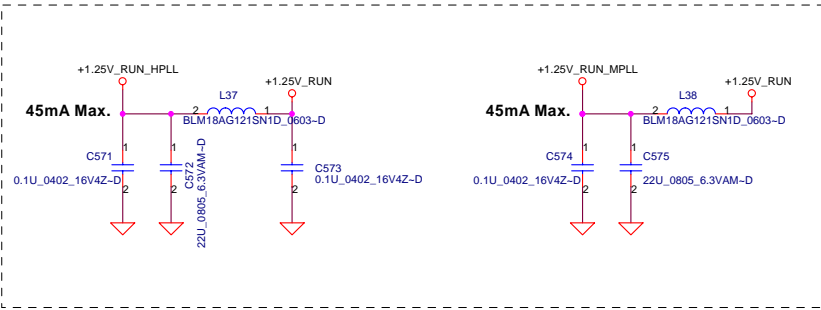
Title: **Crestline(3 of 6)**

Size: Document Number **LA-3302P** Rev: 0.4

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Place caps close to VCC\_AXF (Pin A21, B21, B23)



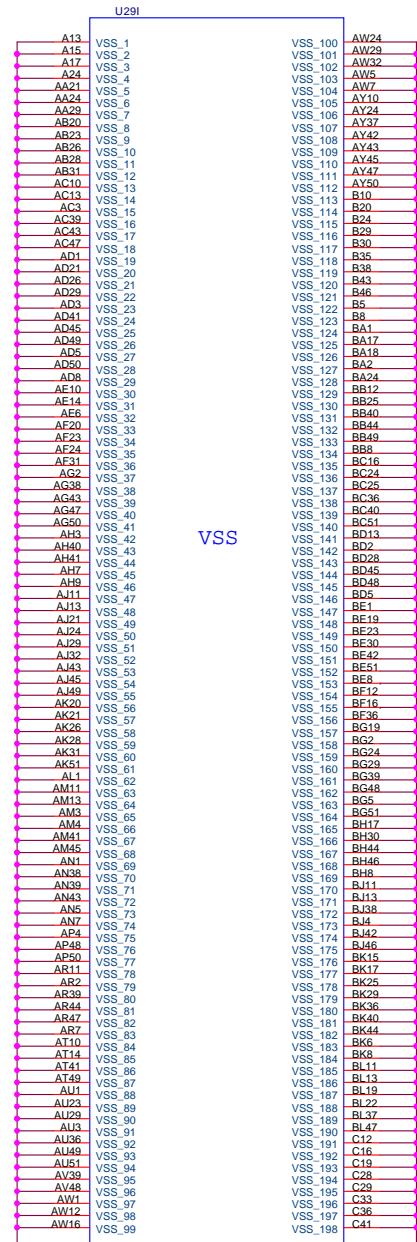
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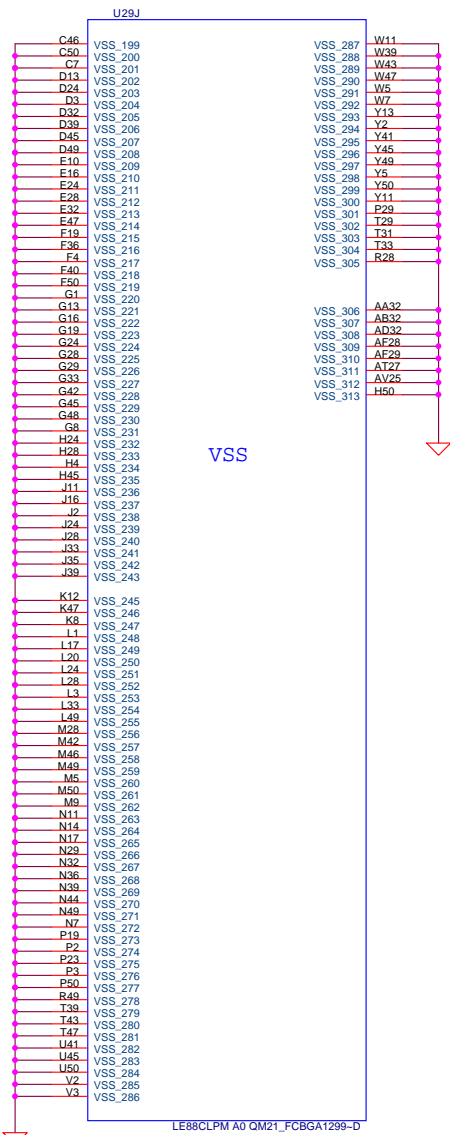
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<b>Crestline(4 of 6)</b>			
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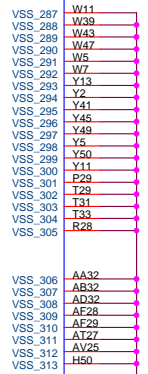




LE88CLPM A0 QM21\_FCBGA1299-D



LE88CLPM A0 QM21\_FCBGA1299-D



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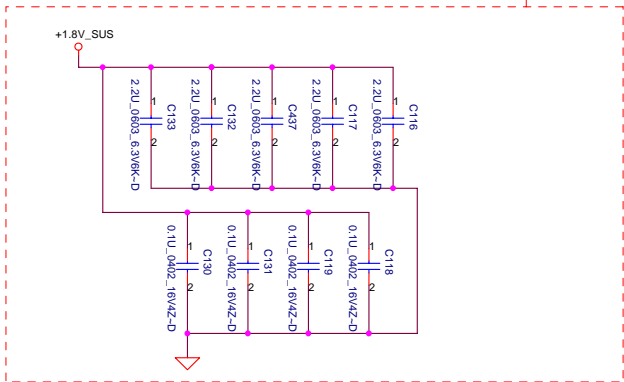
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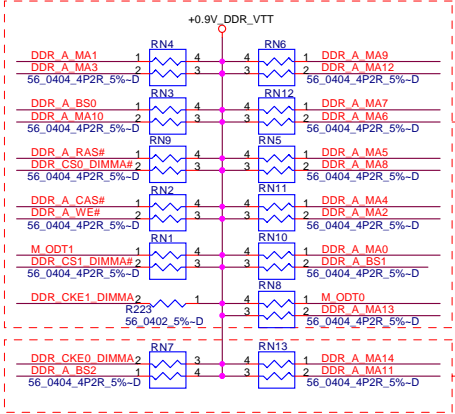
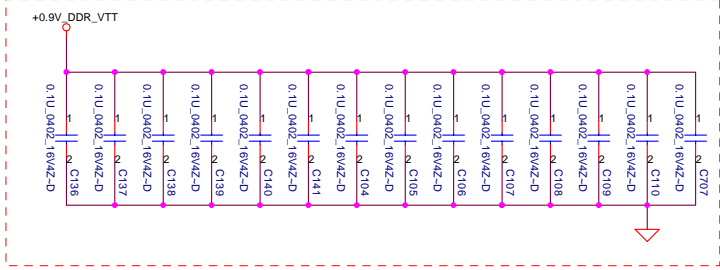
Title		
<b>Crestline(6 of 6)</b>		
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11 DDR\_A\_DQS#[0..7] <<>>  
 11 DDR\_A\_D[0..63] <<>>  
 11 DDR\_A\_DM[0..7] <<>>  
 11 DDR\_A\_DQS#[0..7K] <<>>  
 11 DDR\_A\_MA[0..14] <<>>

**Layout Note:**  
Place near JDIM1



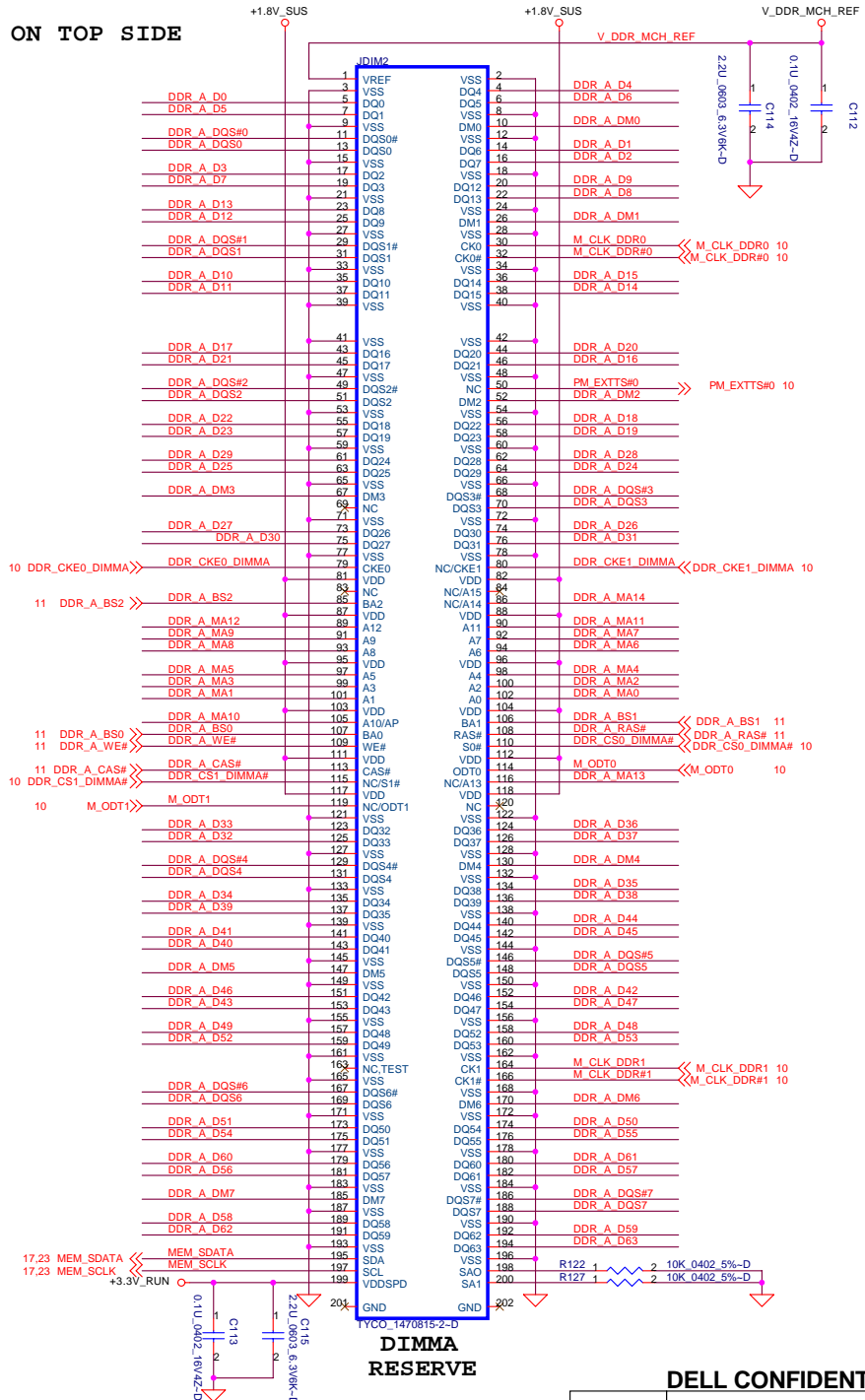
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor closely DIMM0, all trace length < 750 mil

**Layout Note:**  
Place these resistor closely DIMM0, all trace length Max=1.3"

**ON TOP SIDE**



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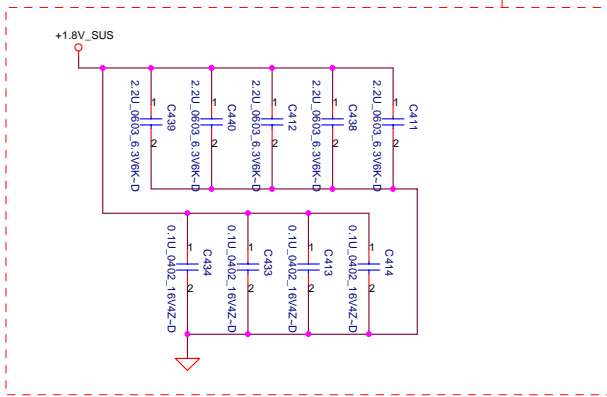
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<b>DDR11-SODIMM SLOT1</b>		
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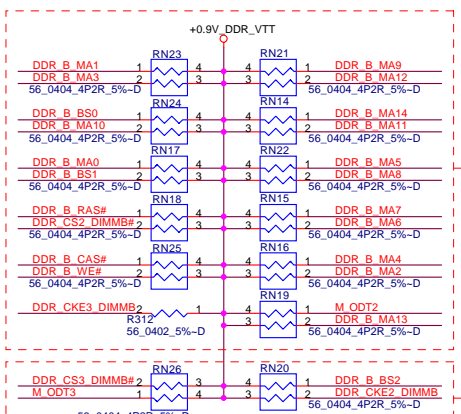
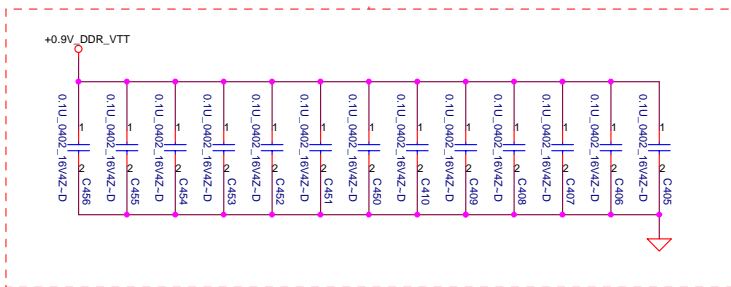


- 11 DDR\_B\_DQS#0[0..7] <<>>
- 11 DDR\_B\_DQ[0..63] <<>>
- 11 DDR\_B\_DM[0..7] <<>>
- 11 DDR\_B\_DQS[0..7] <<>>
- 11 DDR\_B\_MA[0..14] <<>>

**Layout Note:**  
Place near JDIM2



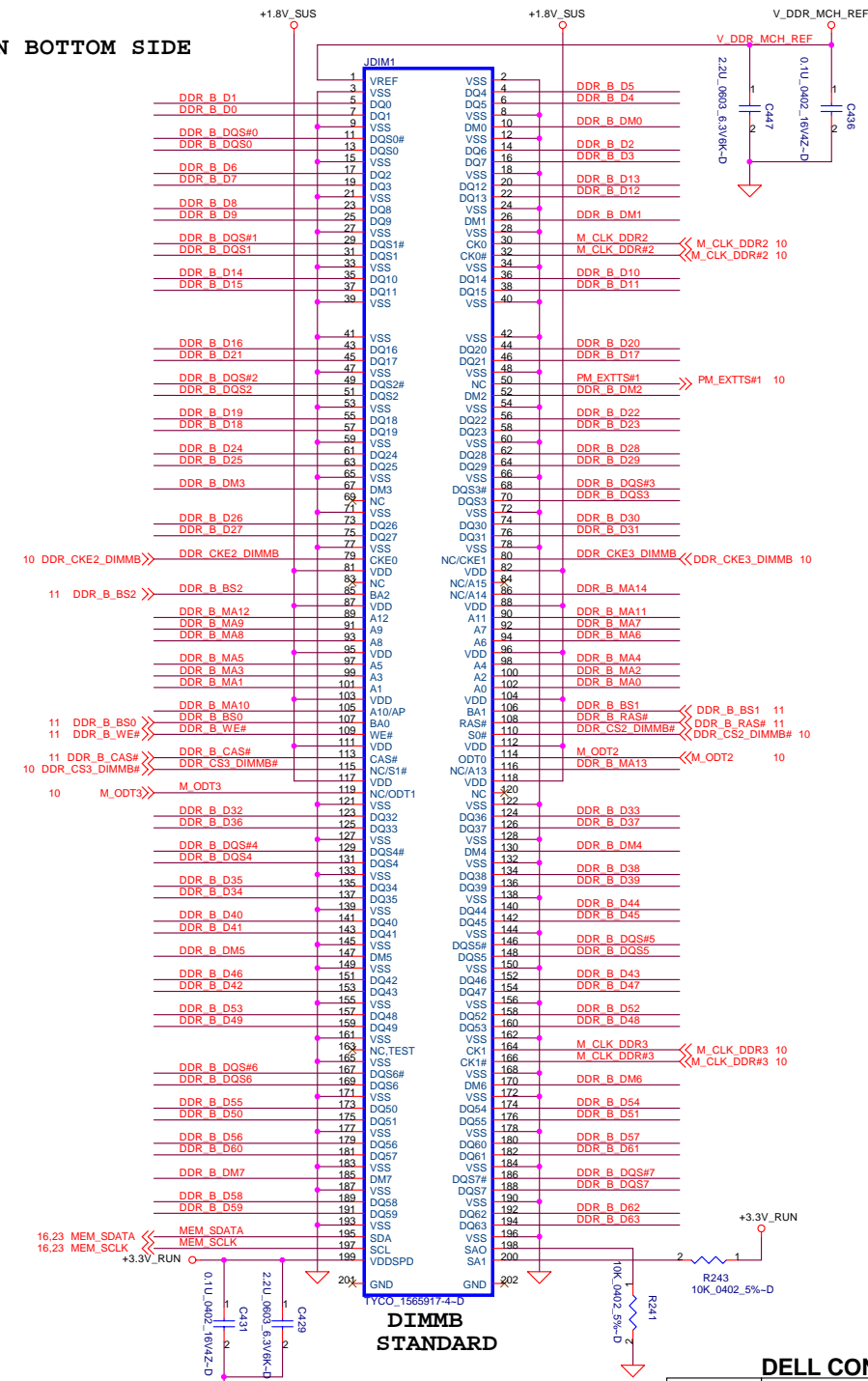
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor closely DIMM0, all trace length < 750 mil

**Layout Note:**  
Place these resistor closely DIMM0, all trace length Max=1.3"

**ON BOTTOM SIDE**



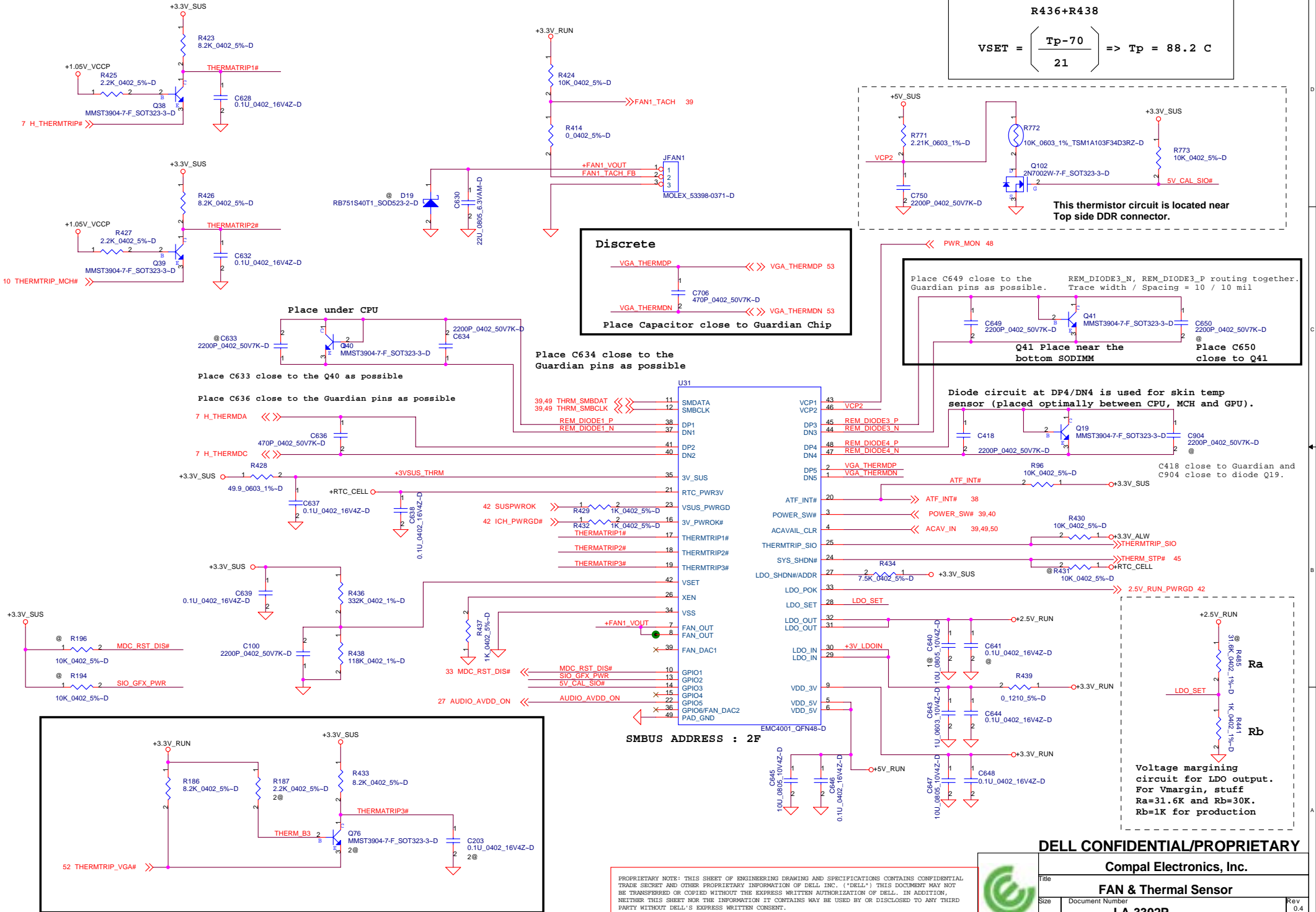
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## FAN1 Control and Tachometer



$$VSET = \frac{R438}{R436+R438} \times 3.3V = 0.865V$$

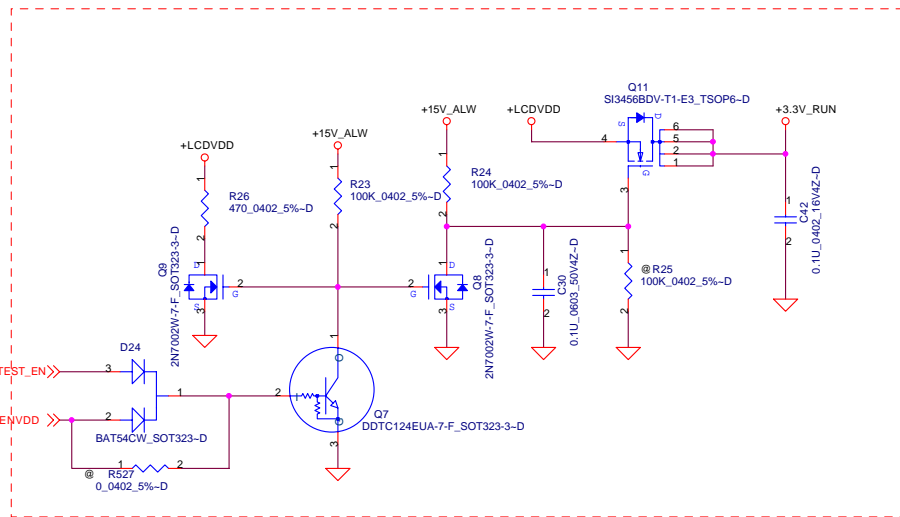
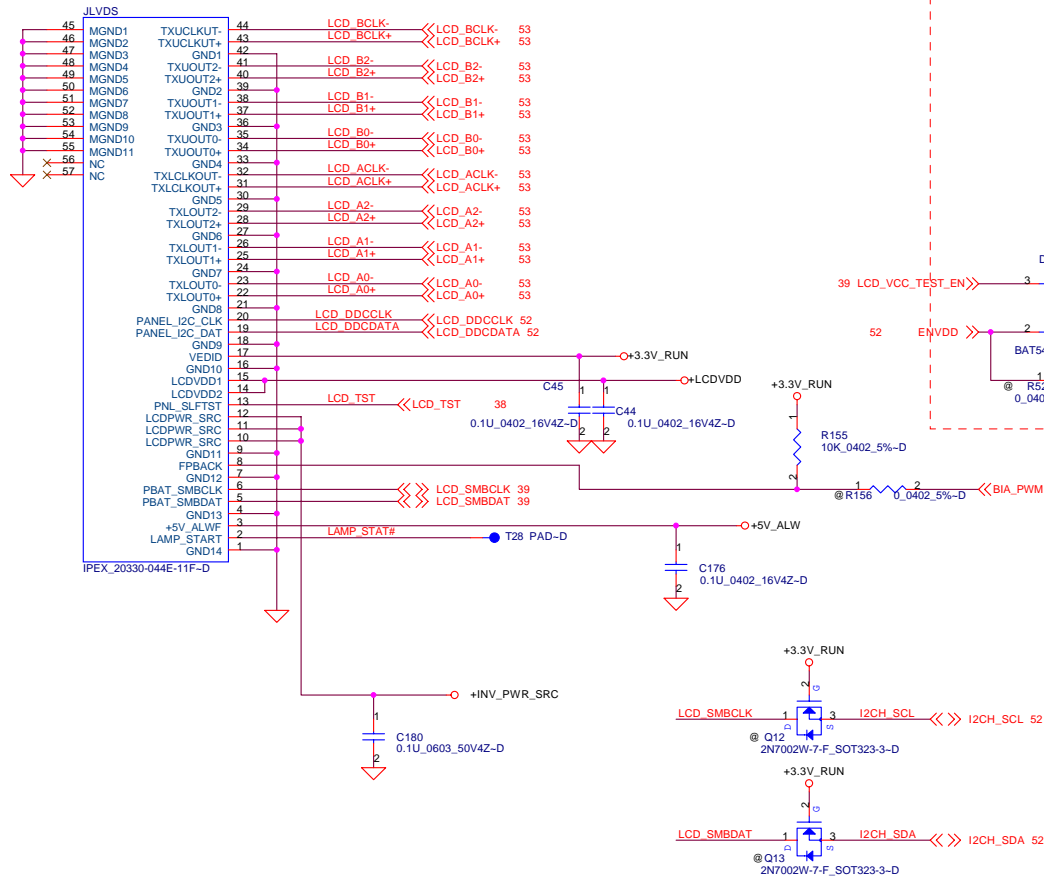
$$VSET = \left( \frac{T_p - 70}{21} \right) \Rightarrow T_p = 88.2 \text{ C}$$

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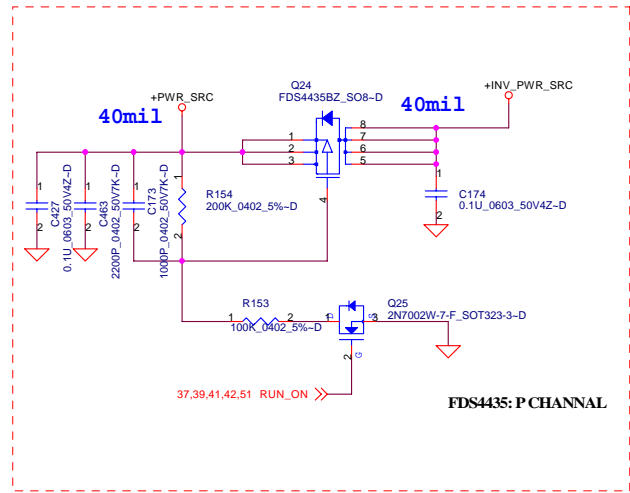


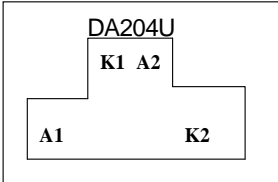
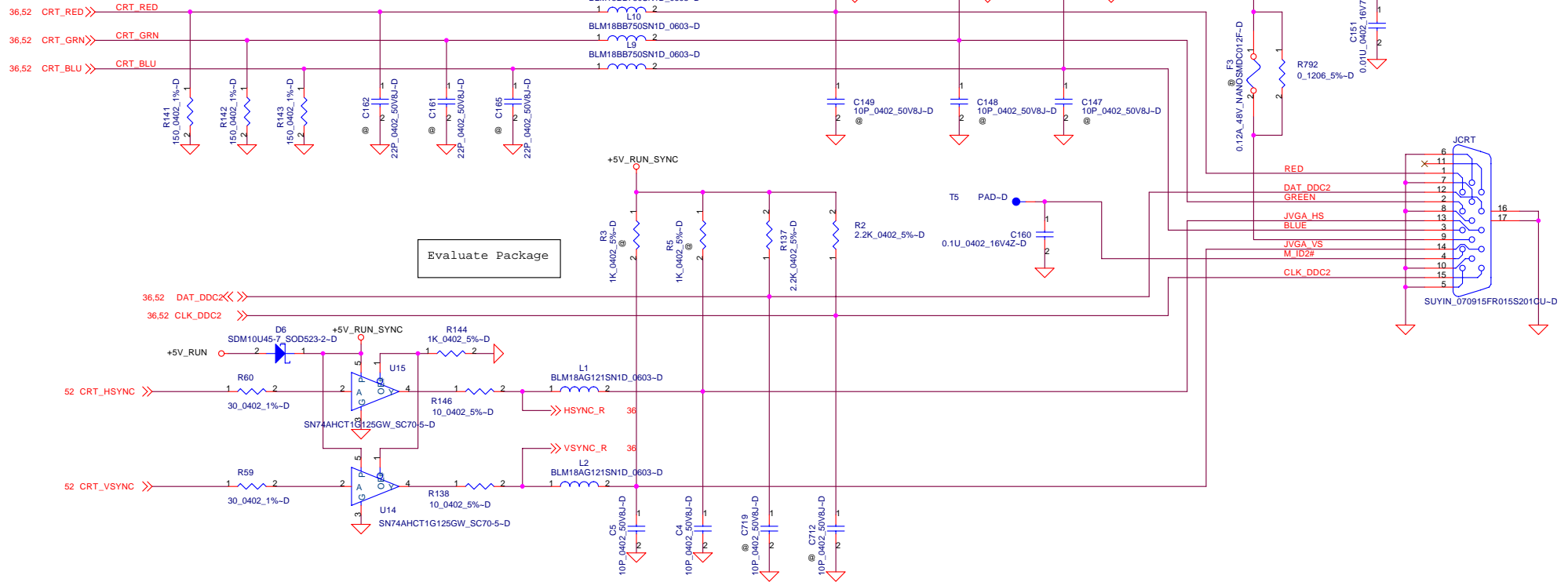
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Populate R155 and de-pop R156 for discrete because it doesn't support DPST

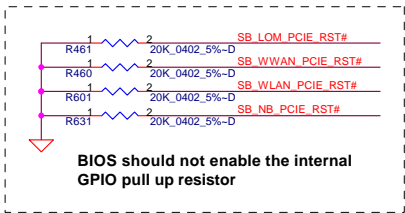
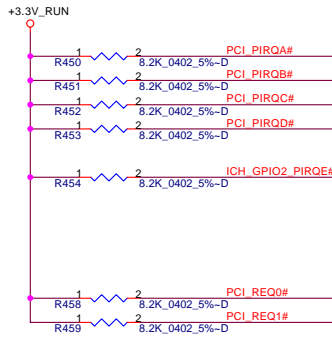
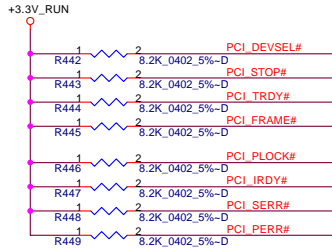




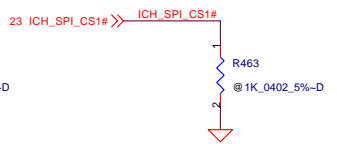
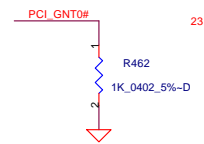
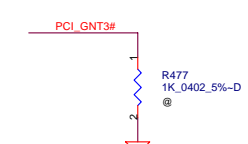
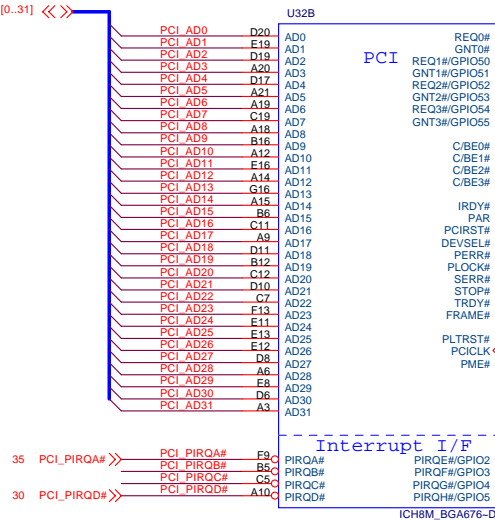
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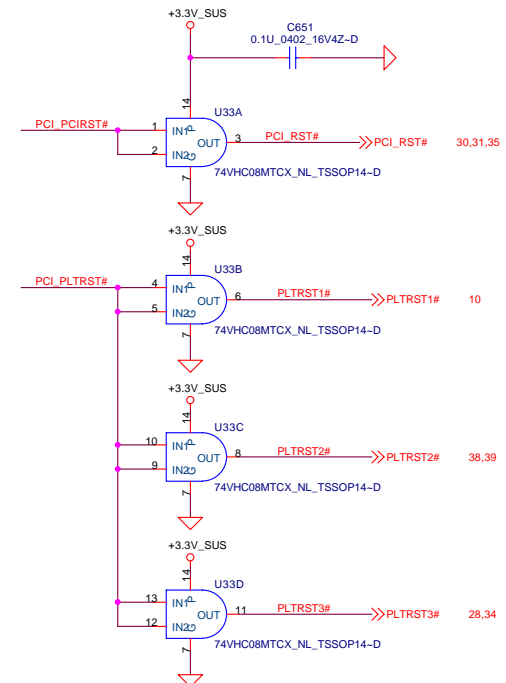
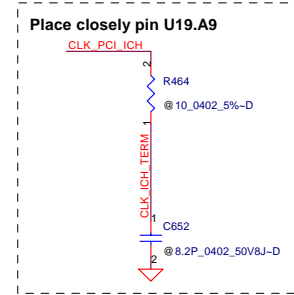


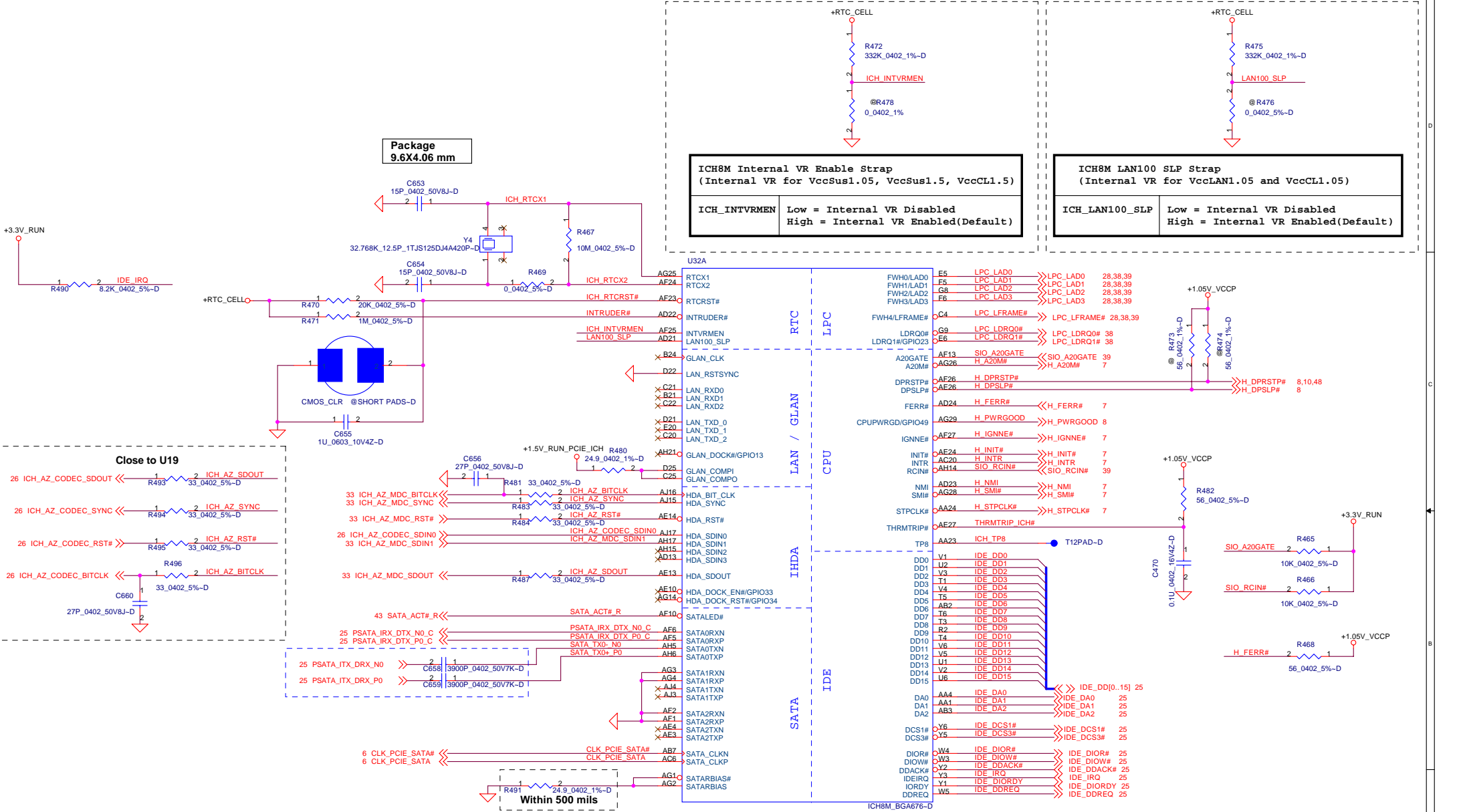
30,35 PCI\_AD[0..31] <<>



A16 away override strap.	
PCI_GNT3#	Low = A16 swap override enabled. High = Default.

Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC





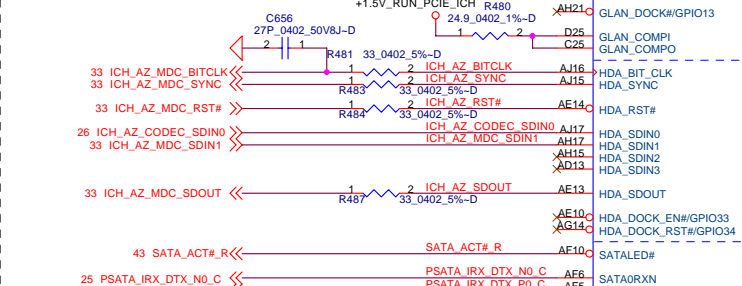
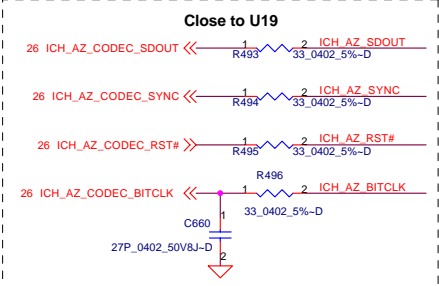
Package  
9.6X4.06 mm

**ICH8M Internal VR Enable Strap**  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)

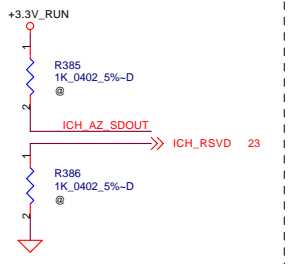
**ICH8M LAN100 SLP Strap**  
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)



**XOR Chain Entrance Strap**

ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



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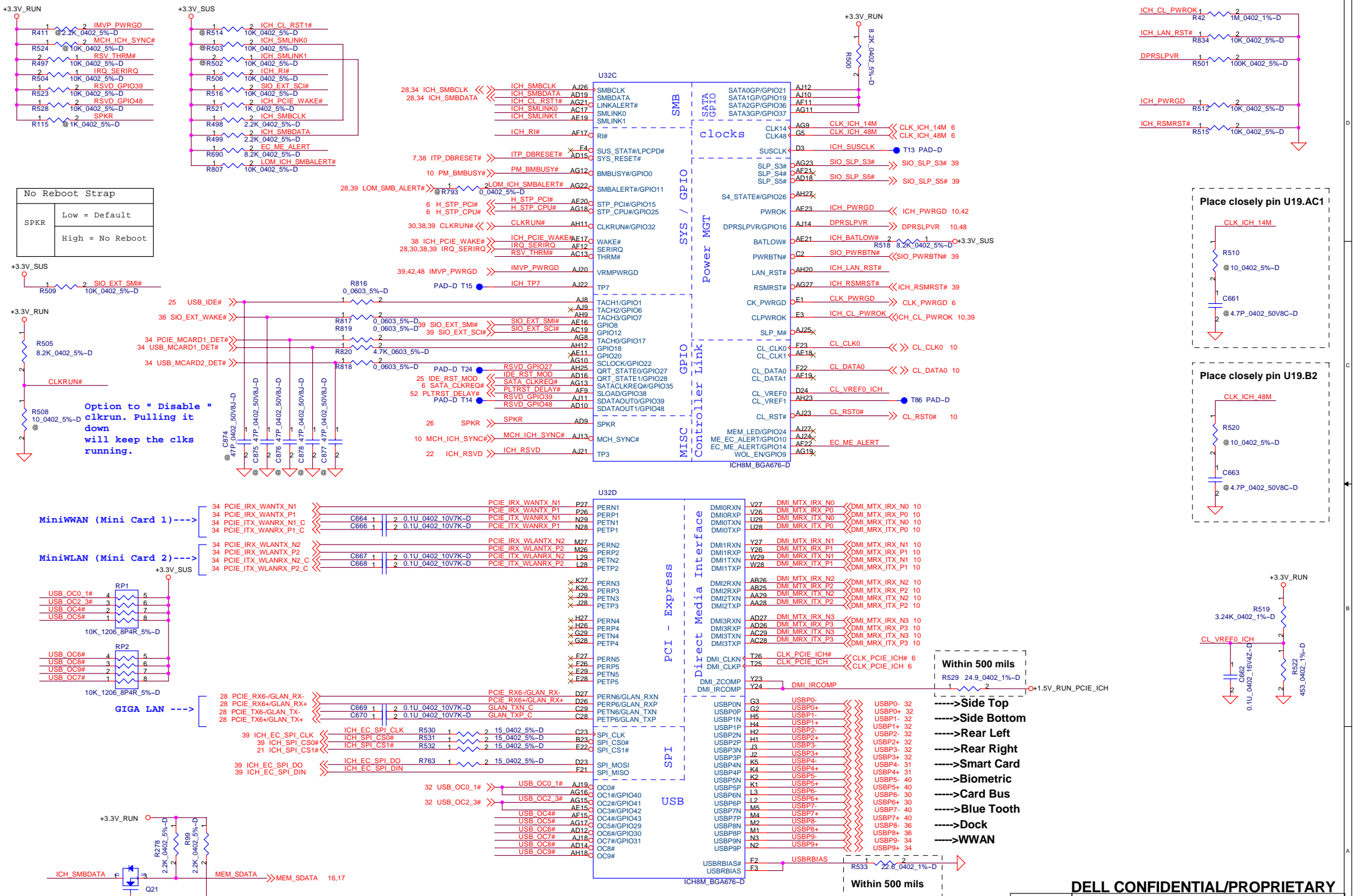
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No Reboot Strap

SPKR	Low = Default
	High = No Reboot

Option to "Disable" clkrun. Pulling it down will keep the clks running.

MiniWWAN (Mini Card 1) ---->

MiniWLAN (Mini Card 2) ---->

GIGA LAN ---->

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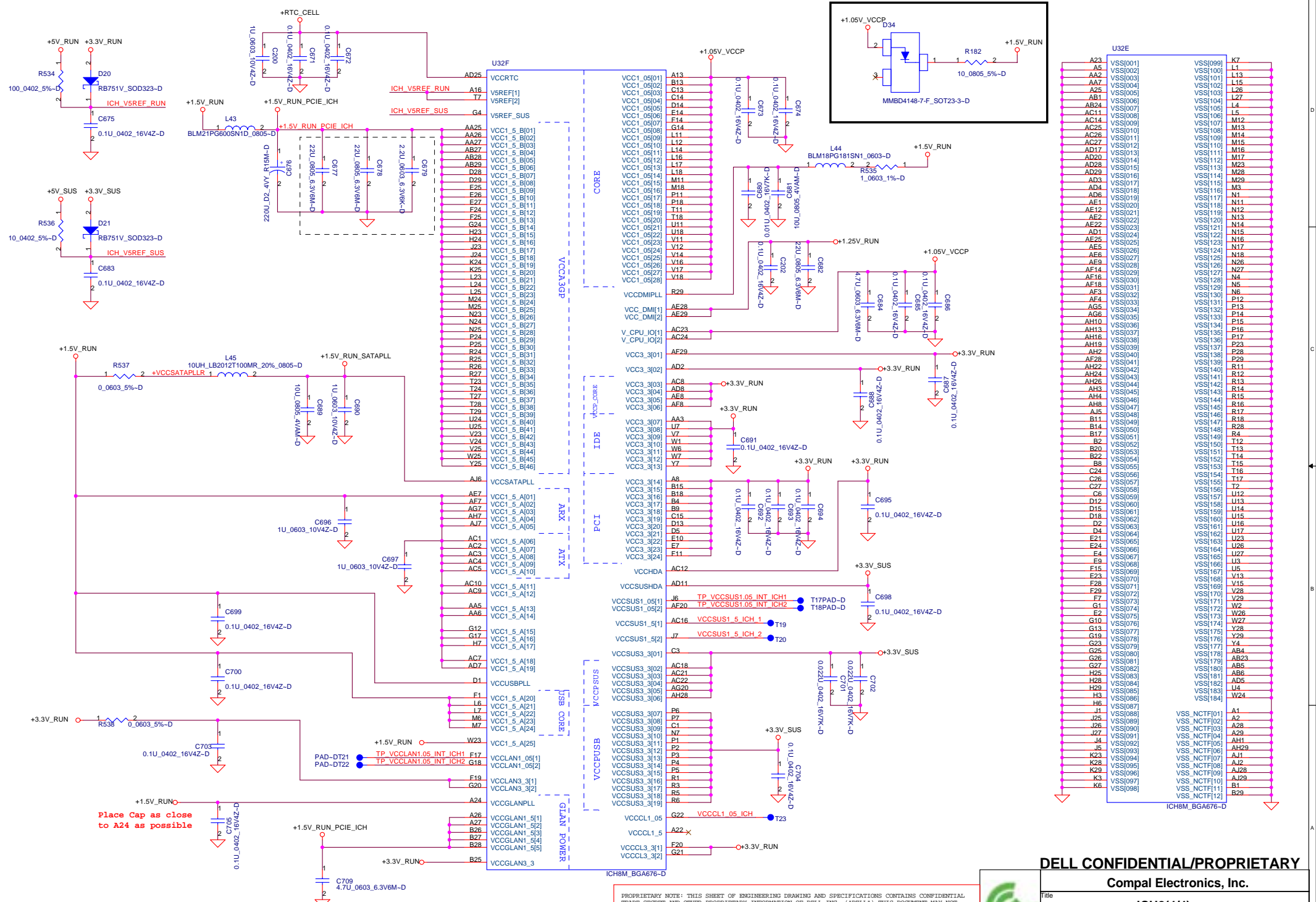
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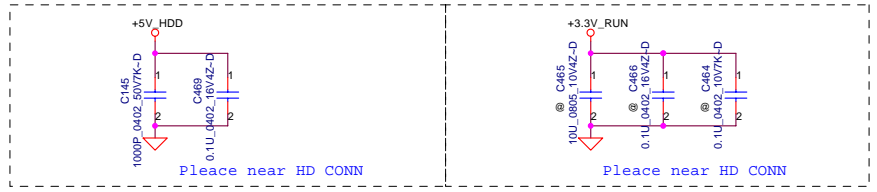
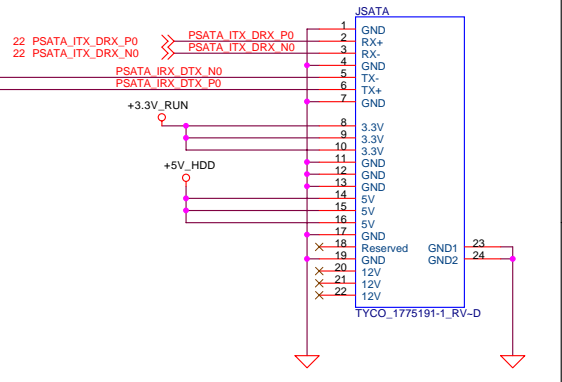
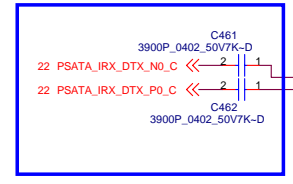
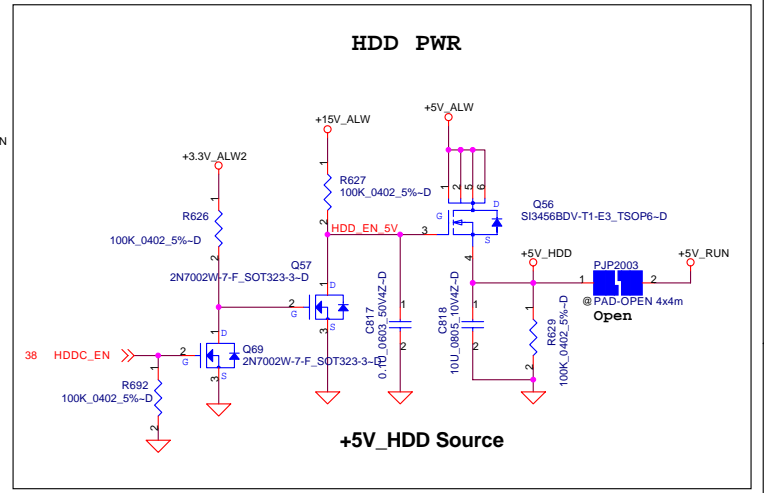
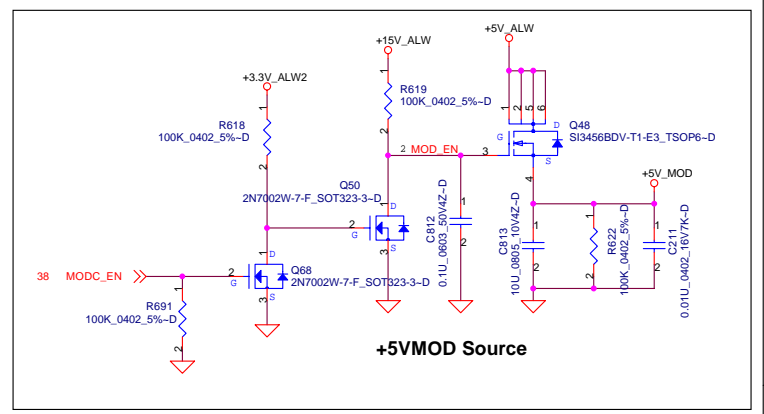
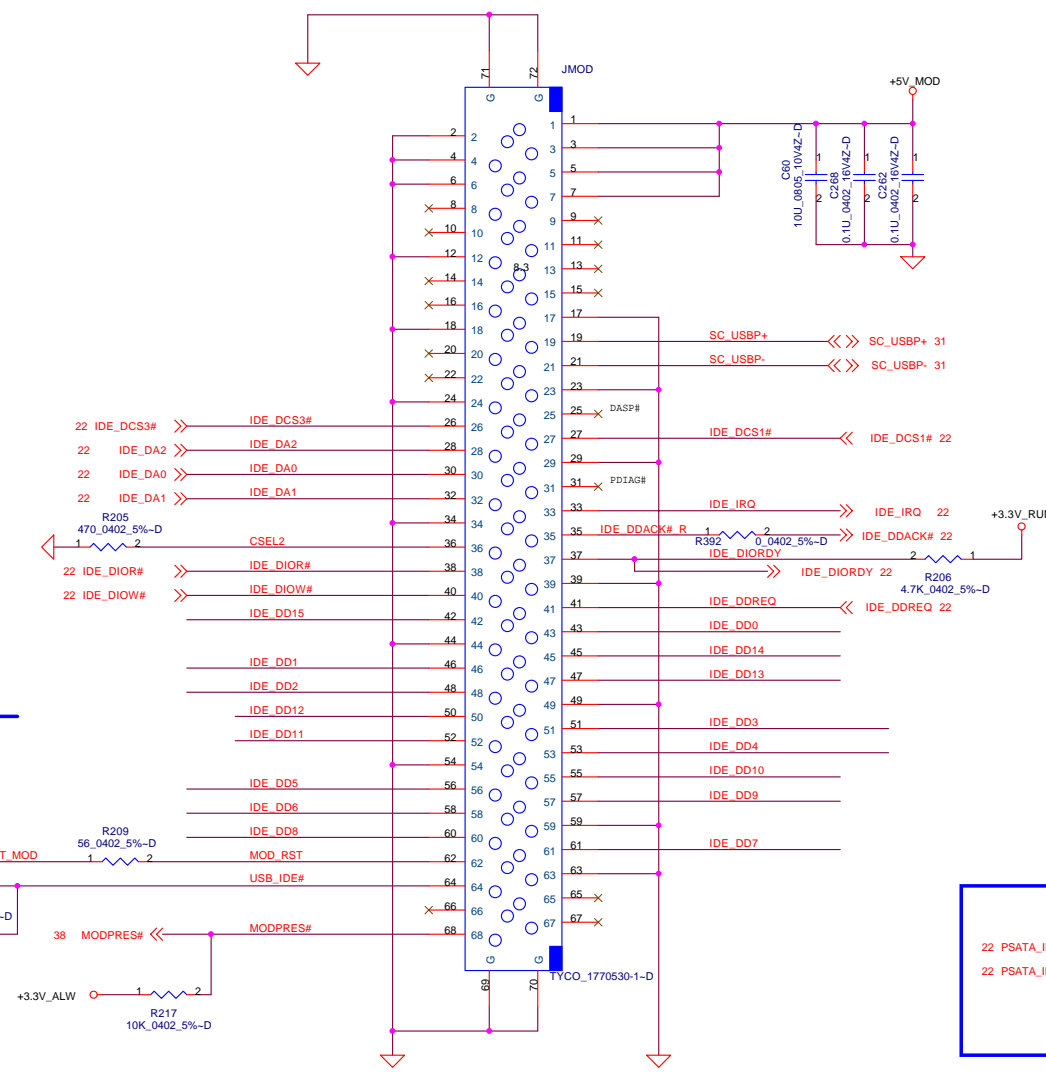
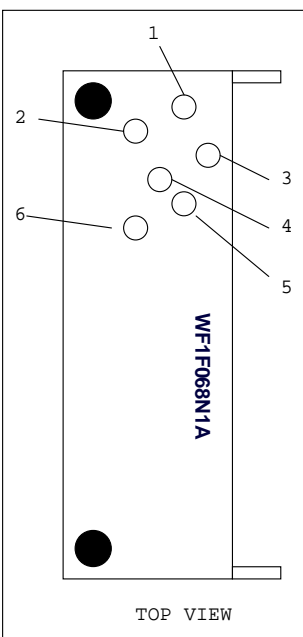
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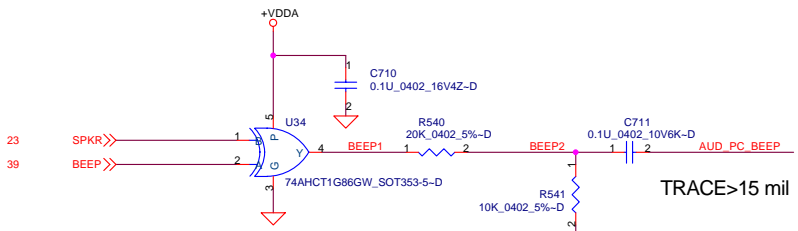
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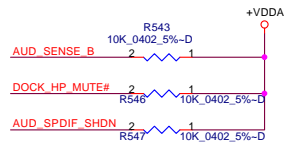
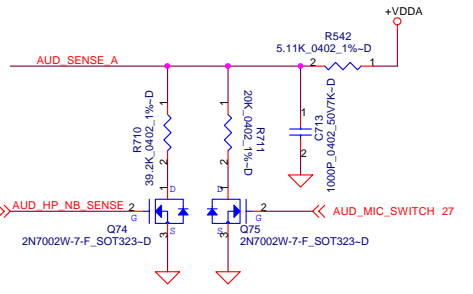
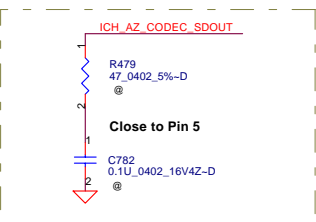
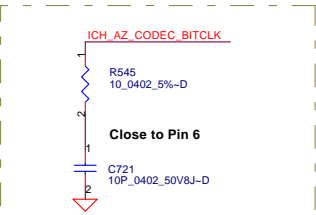
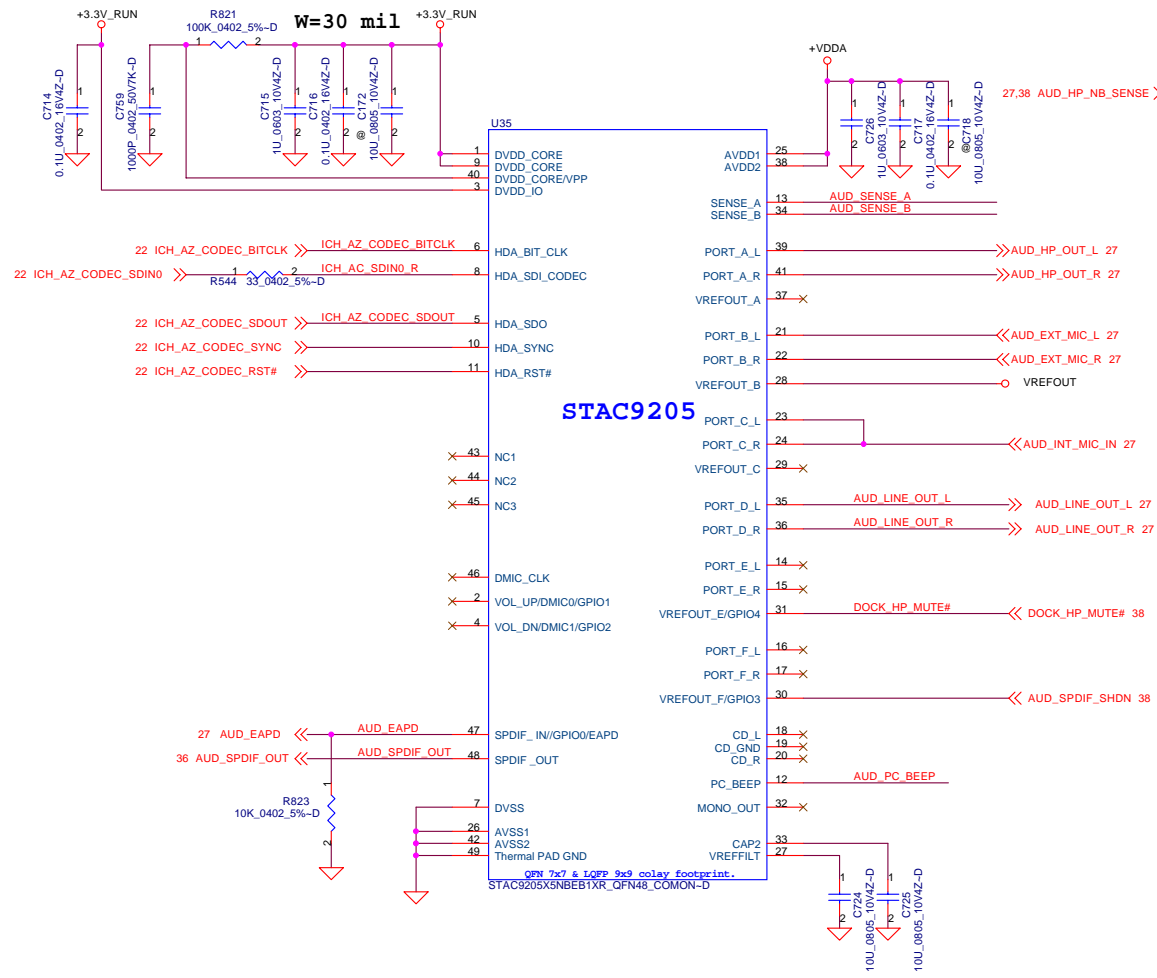
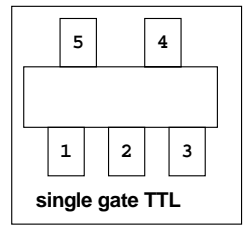
**DVD MODULE**

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U34 place as close to CODEC as possible



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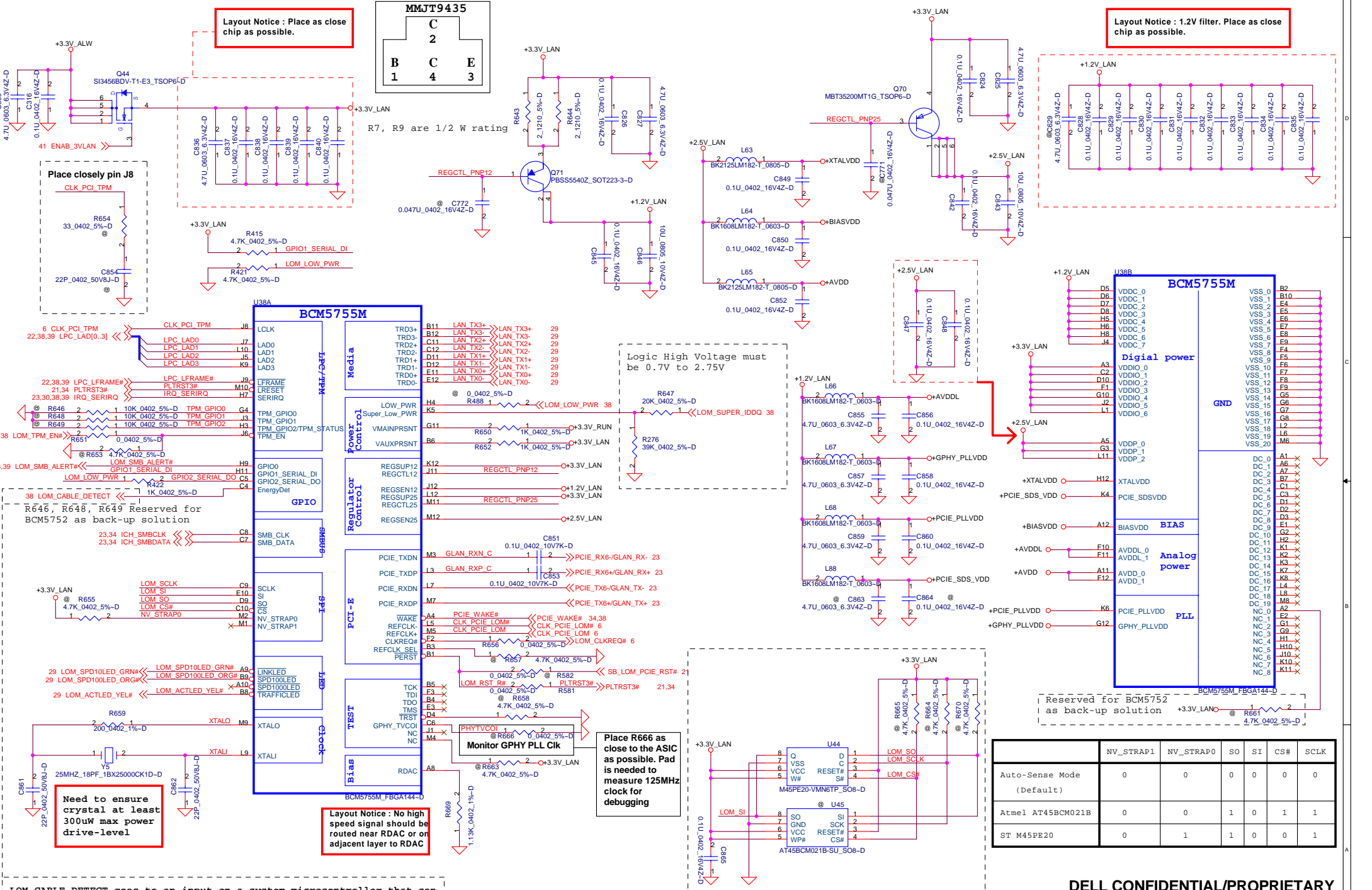
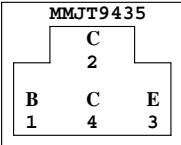
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Title			Azalia (HD) Codec		
Size	Document Number	Rev			
	LA-3302P	0.4			
Date:	Thursday, March 01, 2007	Sheet	26	of	66



Layout Notice : Place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.

Logic High Voltage must be 0.7V to 2.75V

Place R666 as close to the ASIC as possible. Pad is needed to measure 125MHz clock for debugging

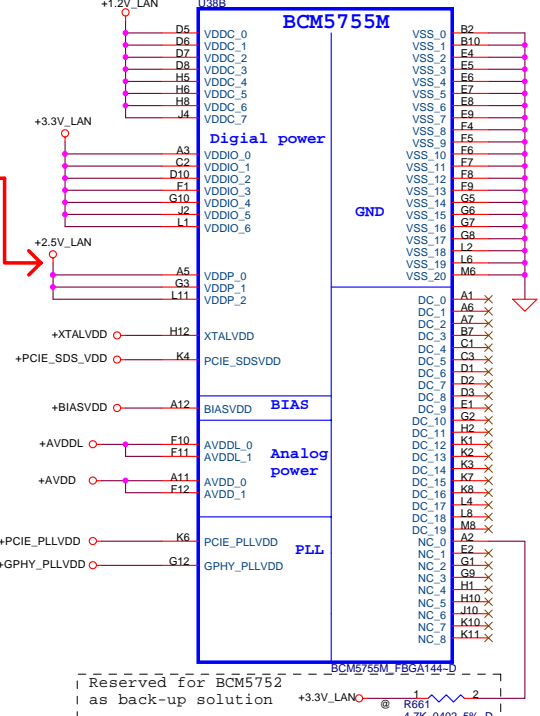
Need to ensure crystal at least 300uW max power drive-level

Layout Notice : No high speed signal should be routed near RDAC or adjacent layer to RDAC

LOM\_CABLE\_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM\_LOW\_PWR when LOM\_CABLE\_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping.

R663 Reserved for BCM5752 as back-up solution

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	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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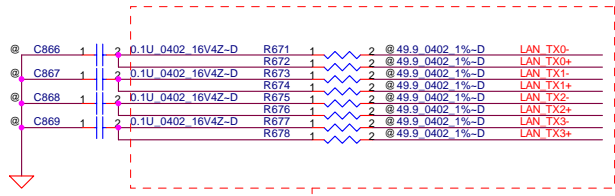
Compal Electronics, Inc.

BCM5755M

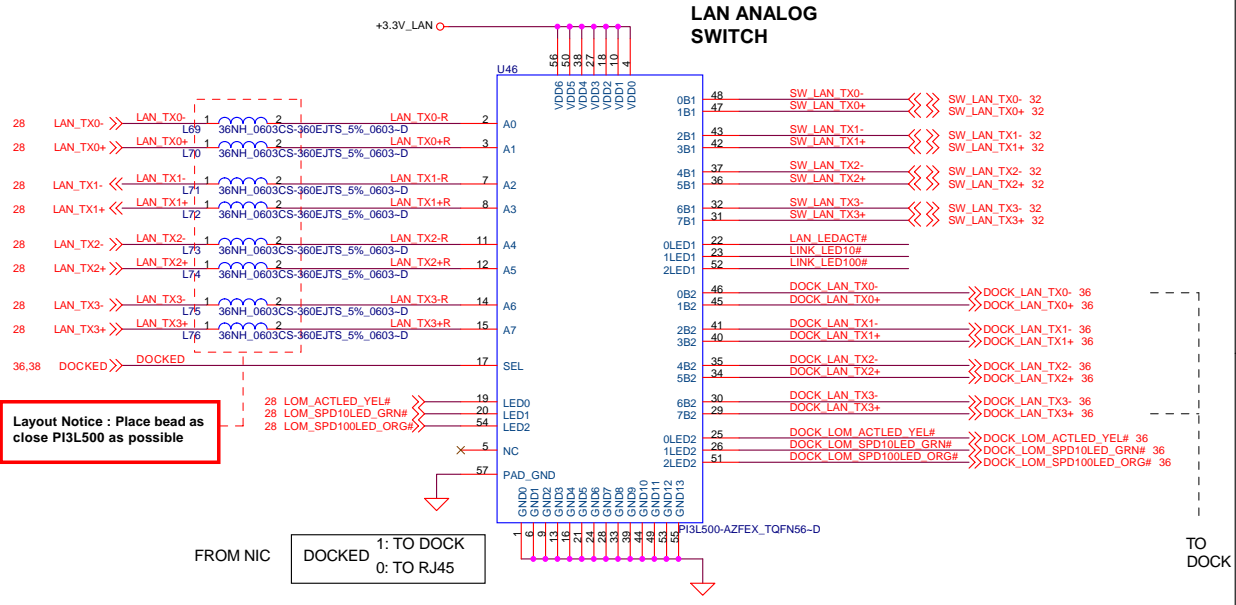
LA-3302P



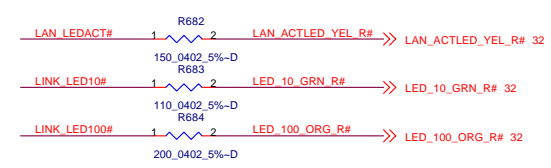
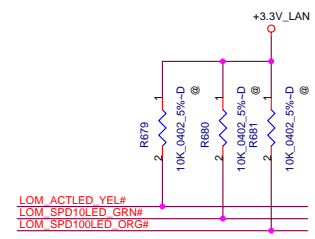
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Size	Document Number	Sheet	28	of	66
Date:	Thursday, March 01, 2007				

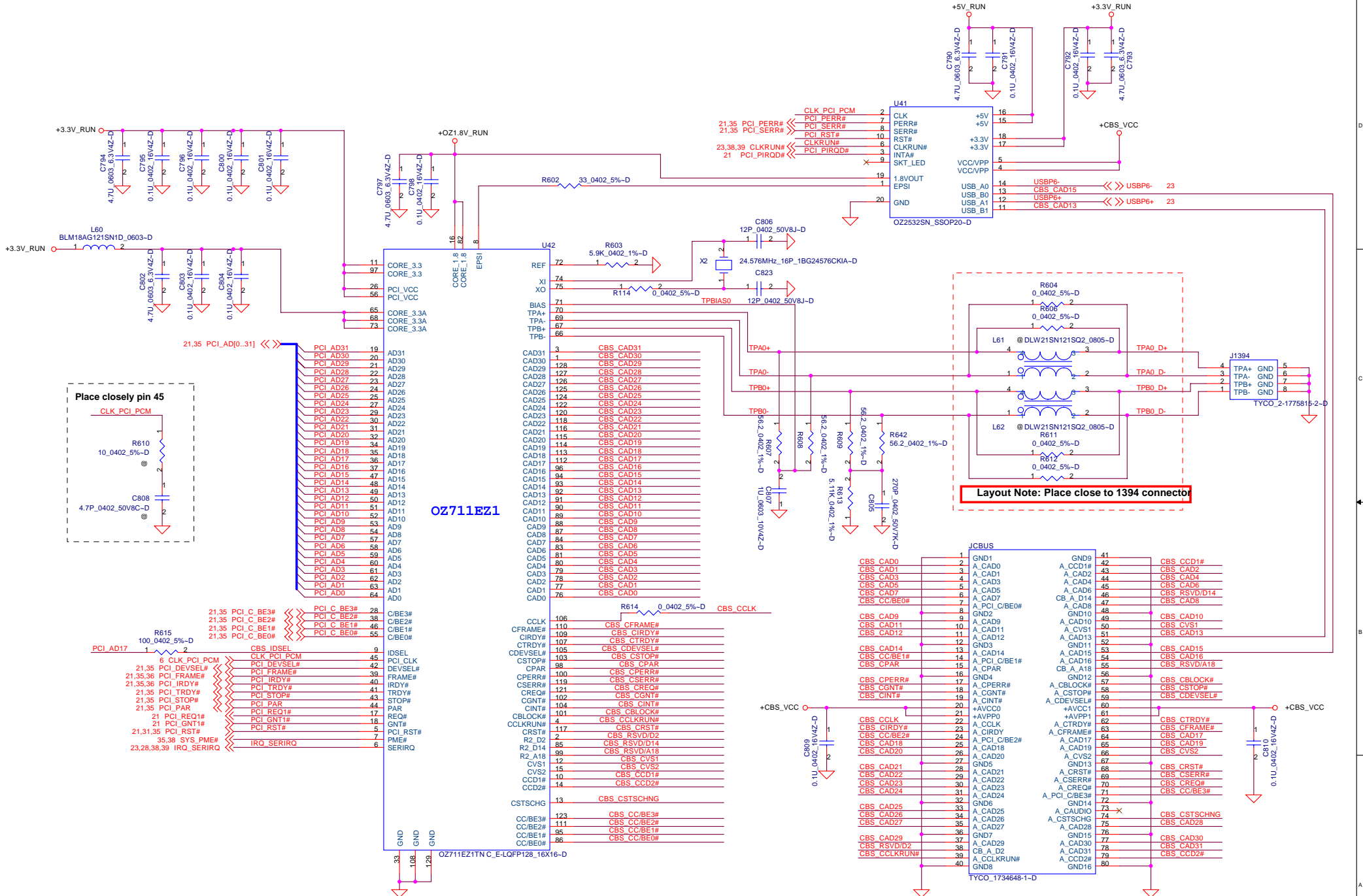


**Layout Notice : Place termination as close as ASIC as possible**  
The resistors need at least 1/16W



**Layout Notice : Place bead as close PI3L500 as possible**





Ground pin 129 exposed die pad, dimension 5.72mm x 5.72mm, should connect to PCB solder pad of same dimension

Layout Note: Place close to 1394 connector

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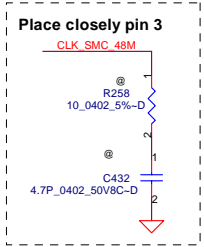
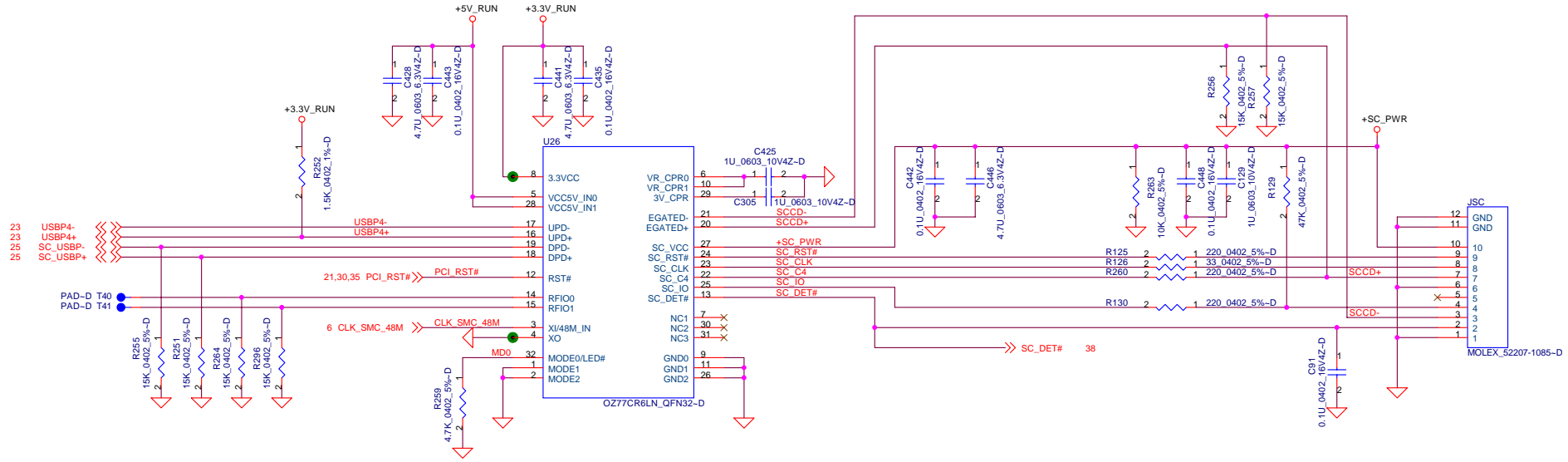
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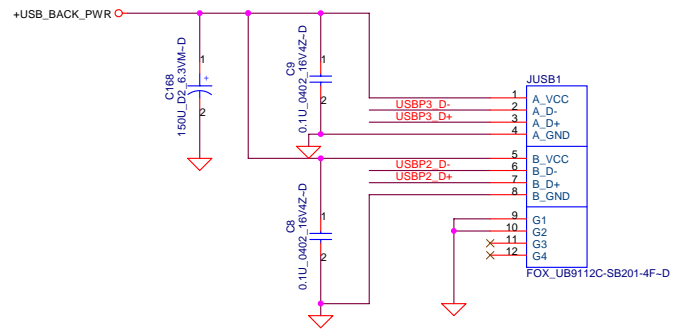
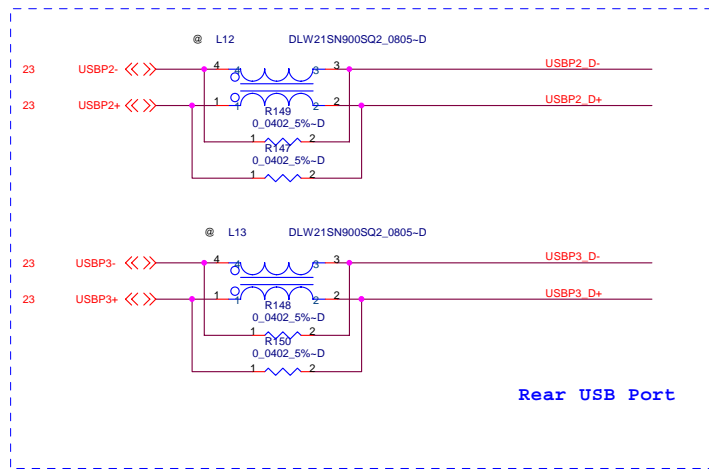
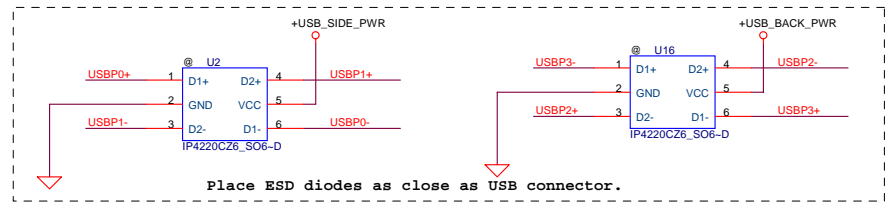
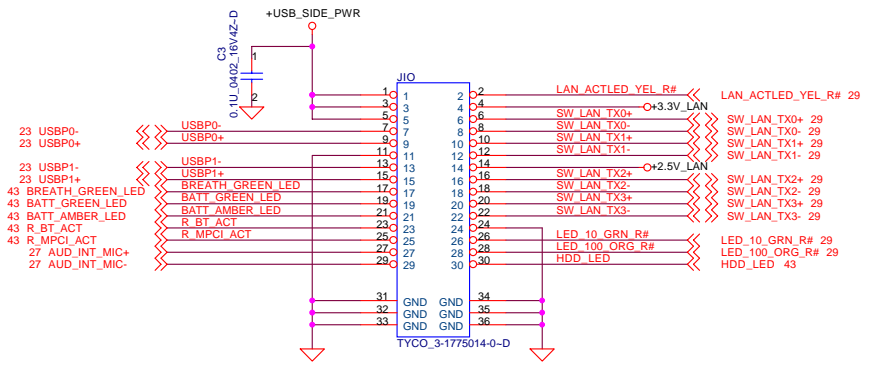
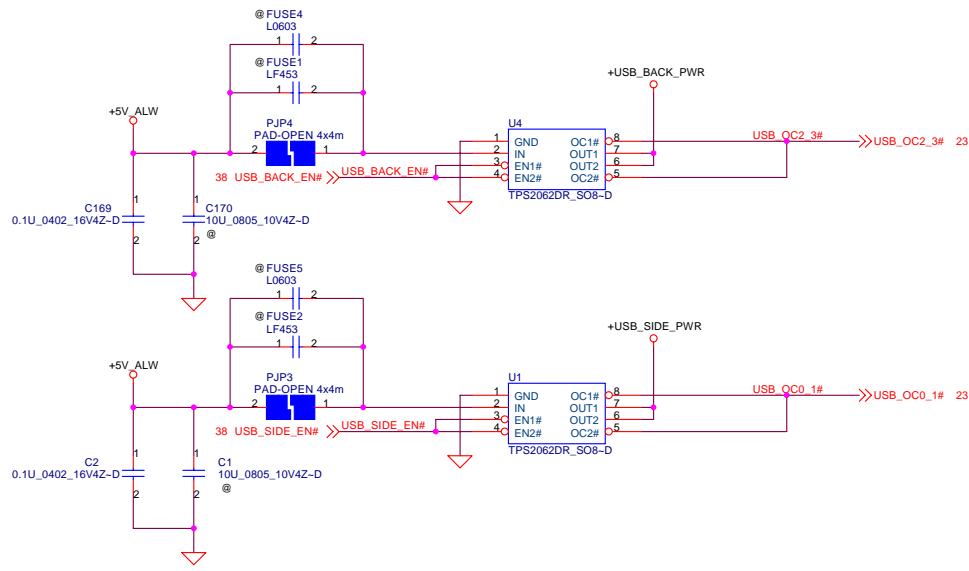
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Cardbus and 1394 OZ711EZ1 Controller

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USB SMARTCARD READER.  
 TYPE A (5V), B (3V), AB (5V/3V)  
 & USB SMARTCARDS ARE SUPPORTED.





Rear USB Ports

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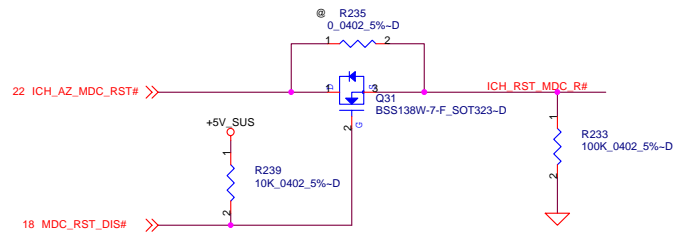
Compal Electronics, Inc.

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USB 2.0 Port		0.4	
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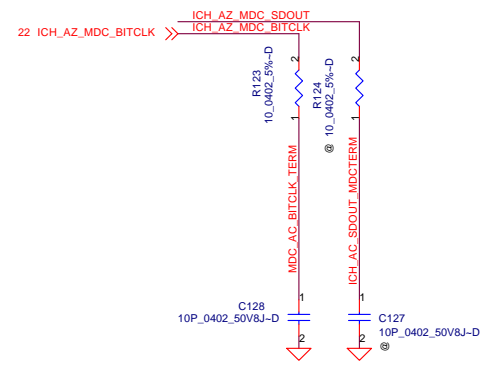
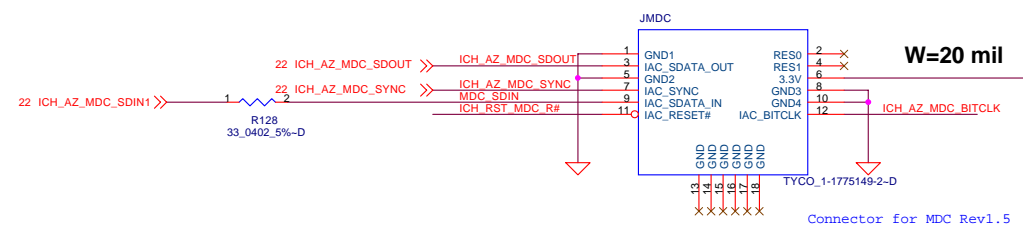






New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12



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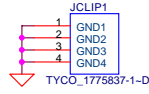
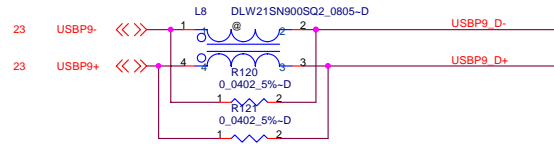
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BT PORT and MDC

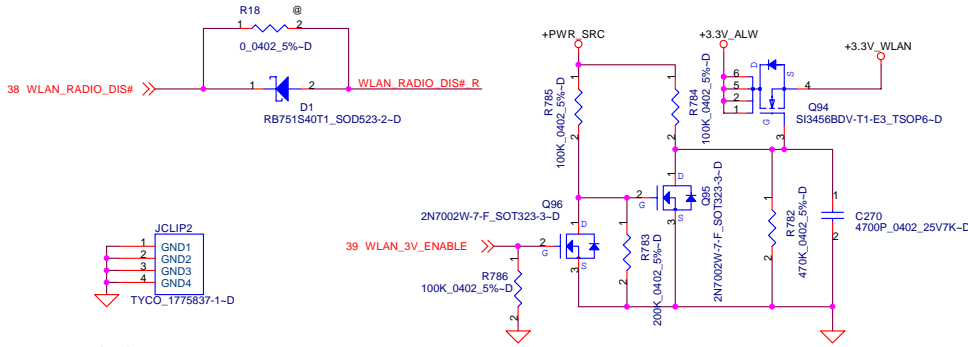
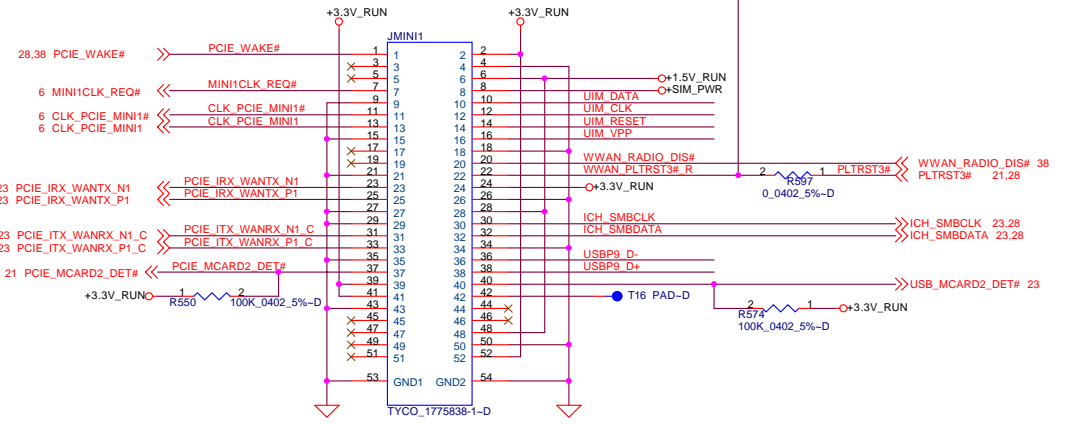
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Date:	Thursday, March 01, 2007	Sheet	33 of 66

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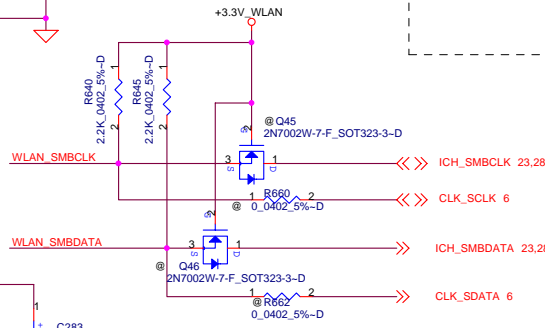
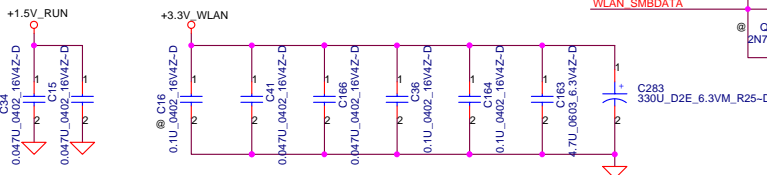
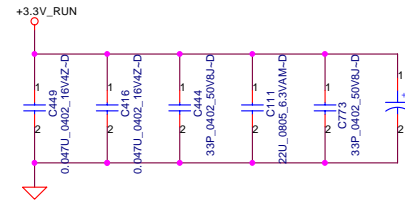
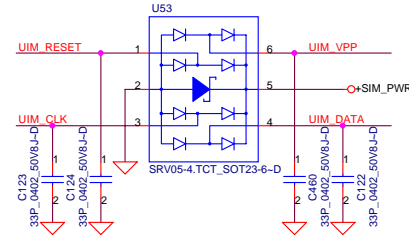
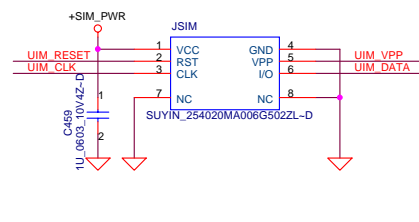
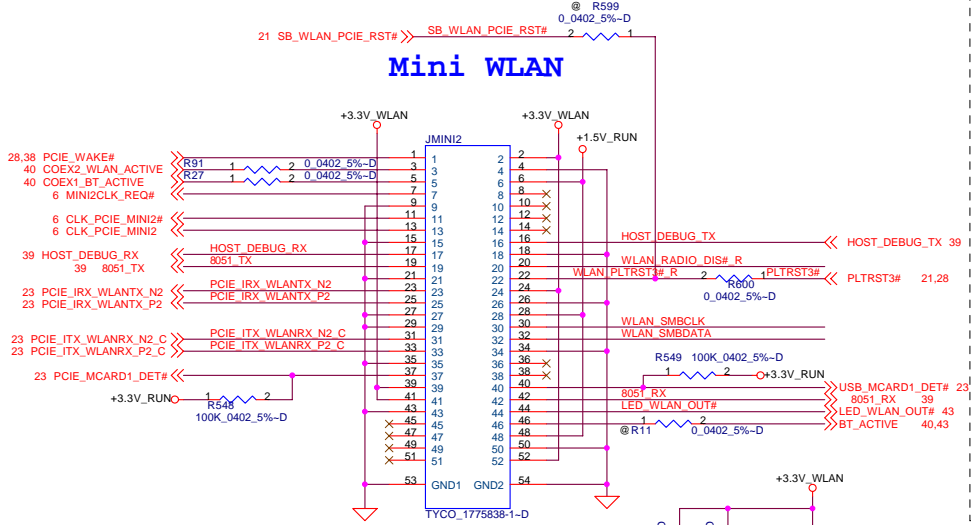
**Mini-Card Latch**

**Mini WWAN**



**Mini-Card Latch**

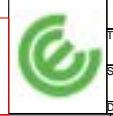
**Mini WLAN**



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA

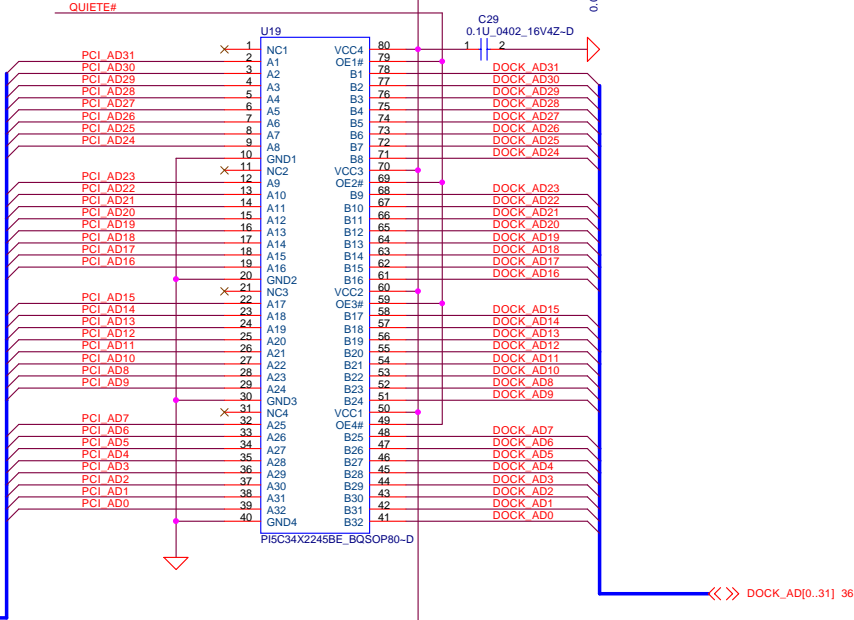
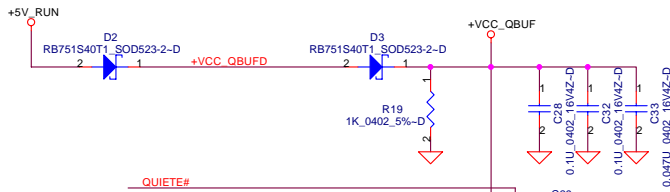
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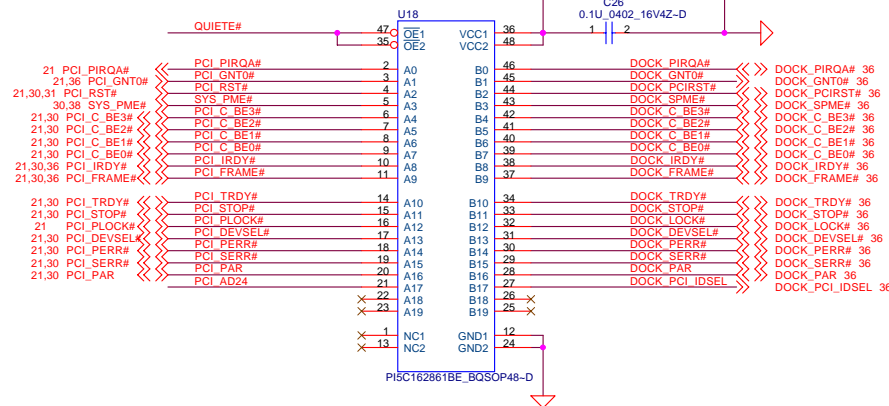
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Title			
Mini Card			
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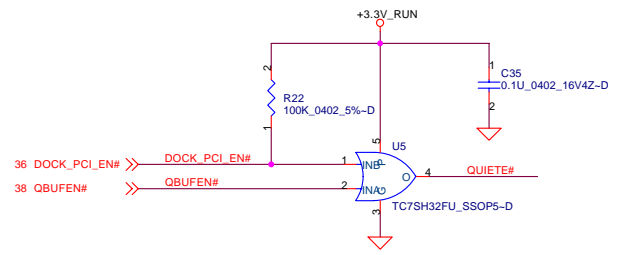
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>>> DOCK\_AD[0..31] 36



21 PCI\_PIRQA# <<>> PCI\_PIRQA#  
 21,36 PCI\_GNT0# <<>> PCI\_GNT0#  
 21,30,31 PCI\_RST# <<>> PCI\_RST#  
 30,38 SYS\_PME# <<>> SYS\_PME#  
 21,30 PCI\_C\_BE3# <<>> PCI\_C\_BE3#  
 21,30 PCI\_C\_BE2# <<>> PCI\_C\_BE2#  
 21,30 PCI\_C\_BE1# <<>> PCI\_C\_BE1#  
 21,30 PCI\_C\_BE0# <<>> PCI\_C\_BE0#  
 21,30,36 PCI\_IRDY# <<>> PCI\_IRDY#  
 21,30,36 PCI\_FRAME# <<>> PCI\_FRAME#  
 21,30 PCI\_TRDY# <<>> PCI\_TRDY#  
 21,30 PCI\_STOP# <<>> PCI\_STOP#  
 21 PCI\_PLOCK# <<>> PCI\_PLOCK#  
 21,30 PCI\_DEVSEL# <<>> PCI\_DEVSEL#  
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 21,30 PCI\_SERR# <<>> PCI\_SERR#  
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 21,30 PCI\_PAR# <<>> PCI\_AD24

DOCK\_PIRQA# <<>> DOCK\_PIRQA# 36  
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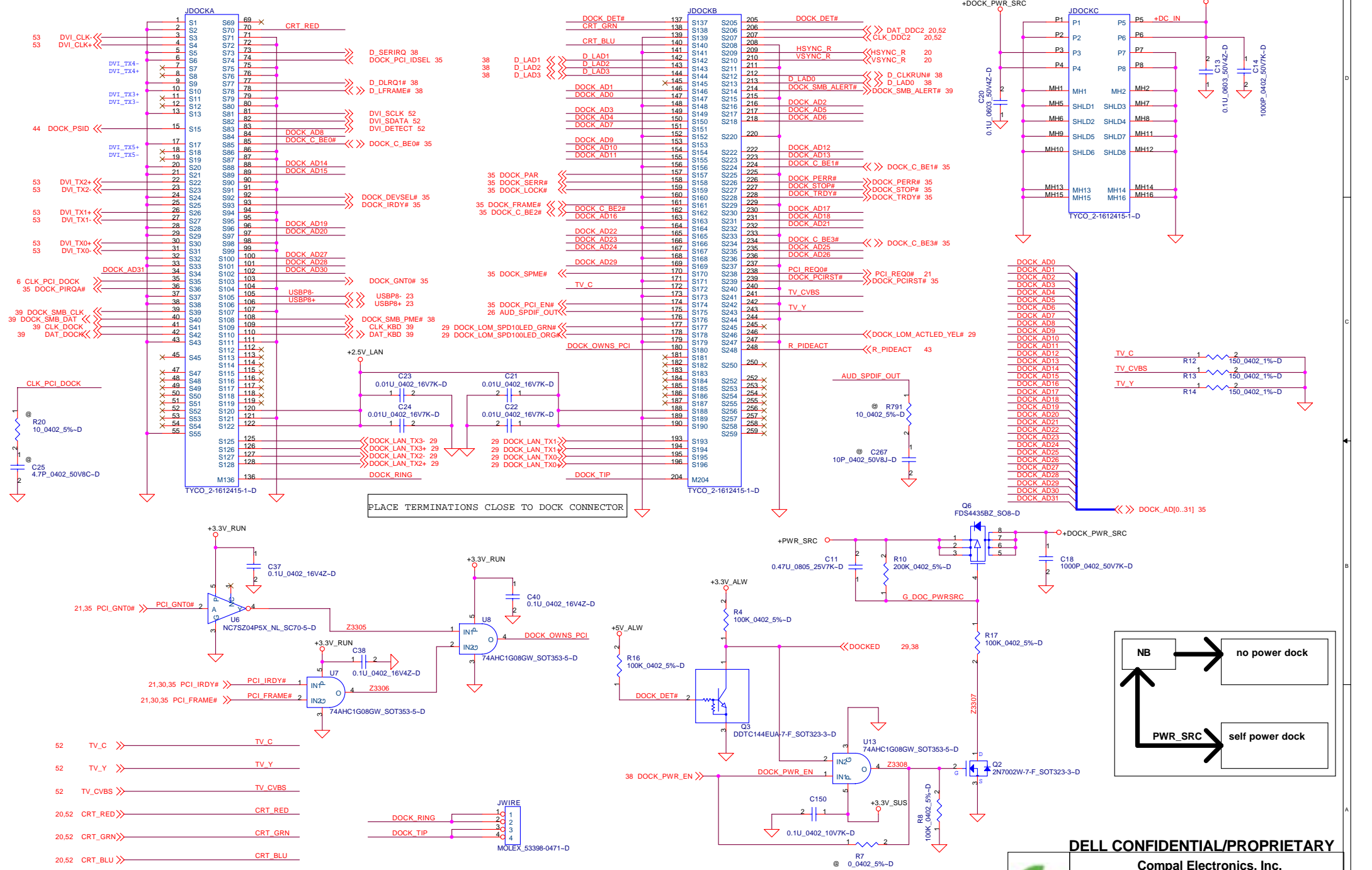


36 DOCK\_PCI\_EN# <<>> DOCK\_PCI\_EN#

38 QBUFEN# <<>> QBUFEN#

QUIETE#





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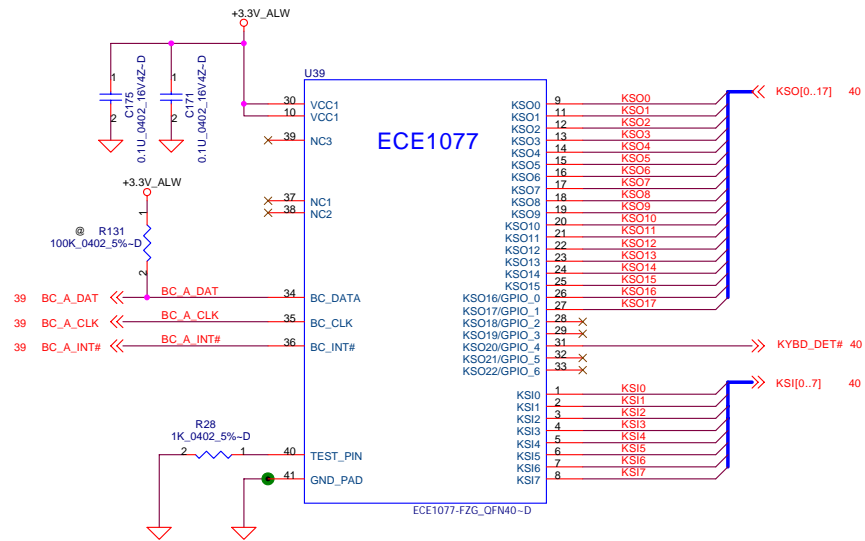
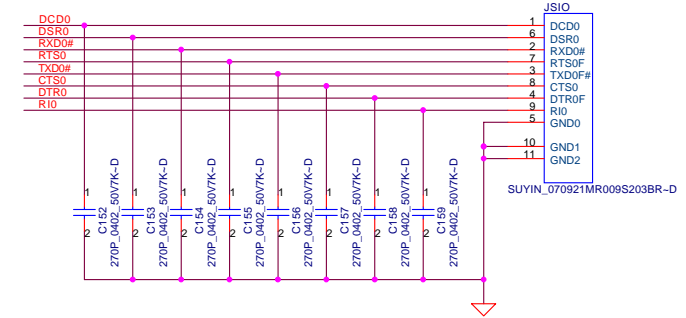
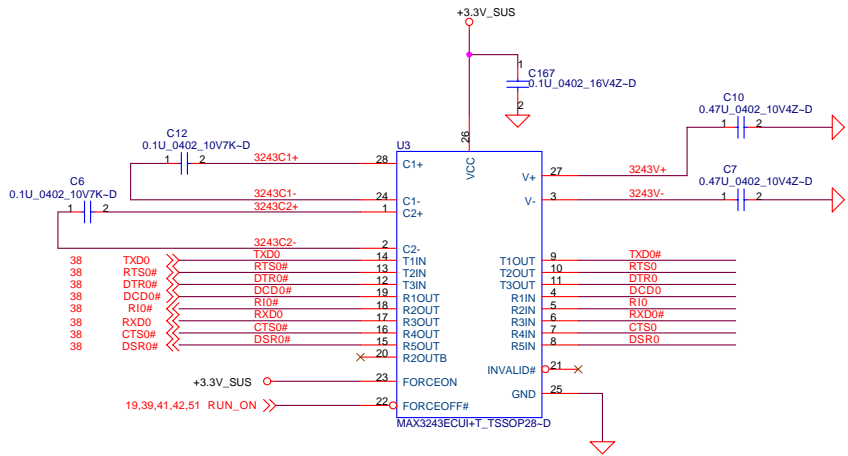
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**DOCKING CONN**

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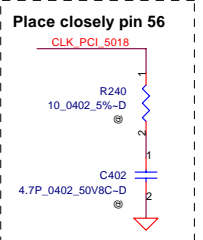
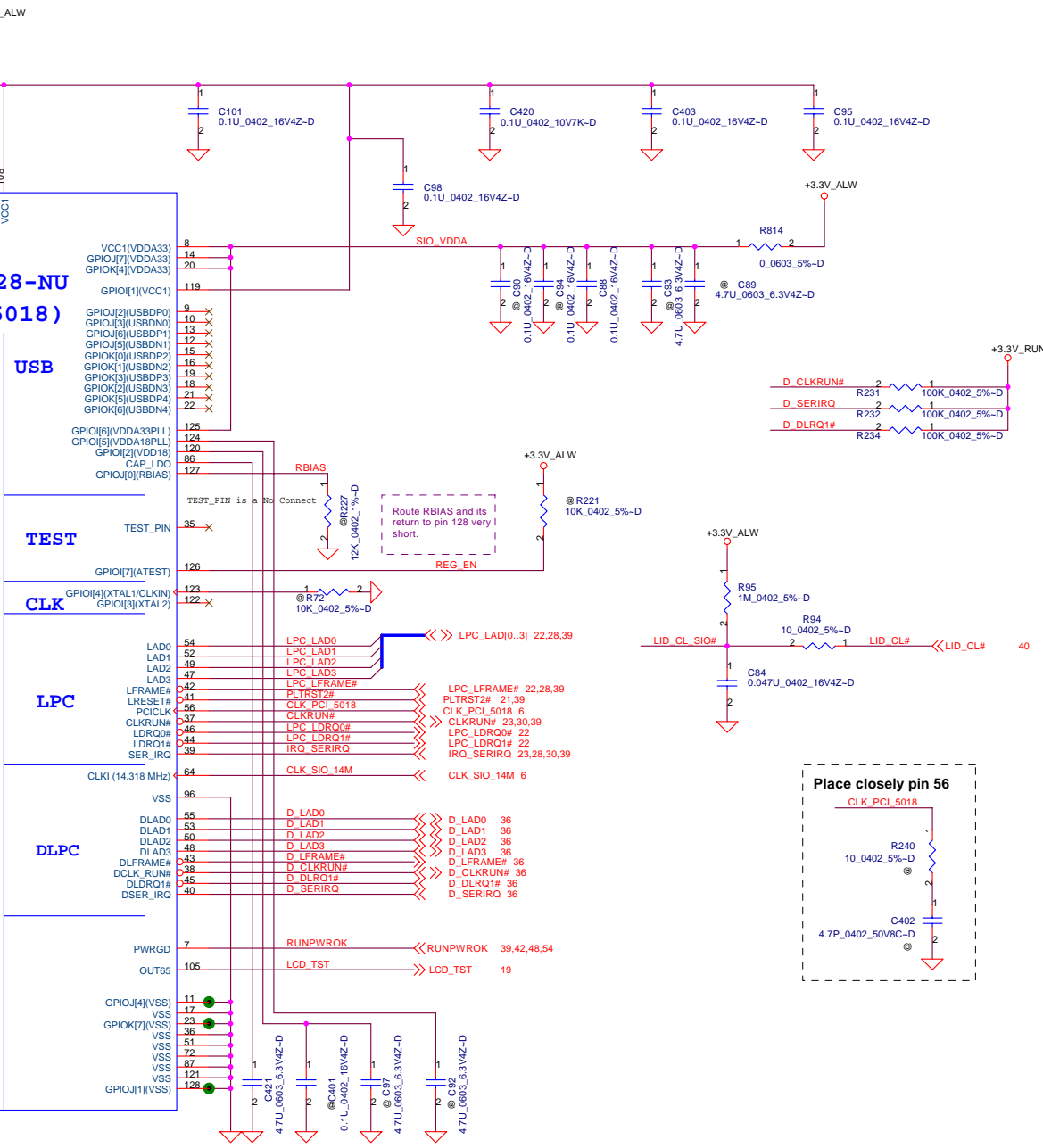
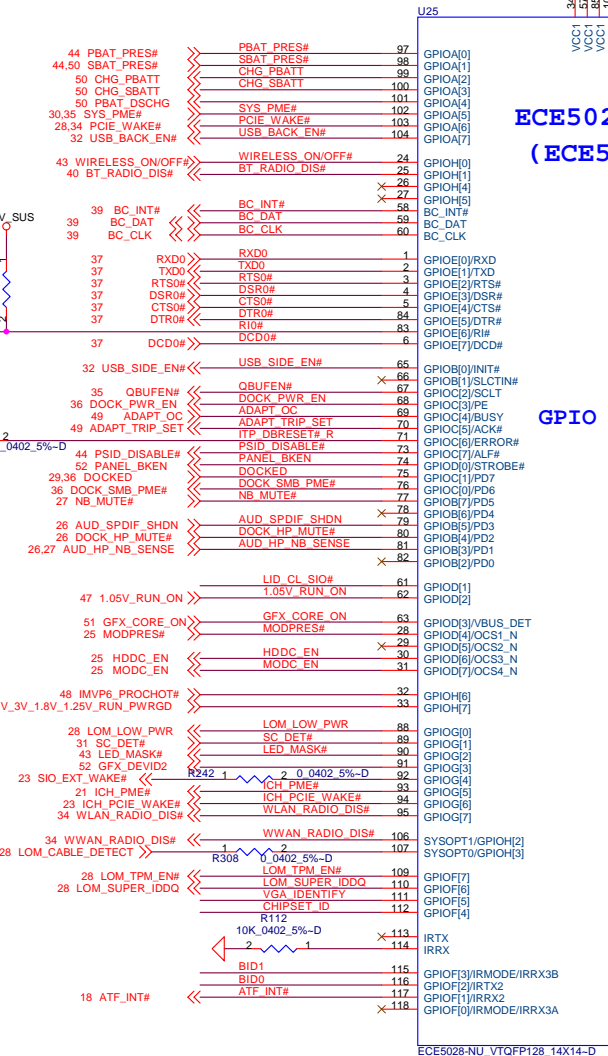
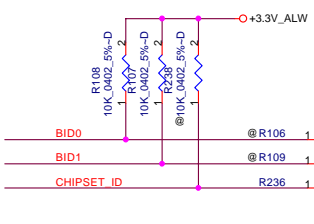
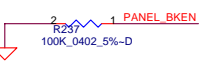
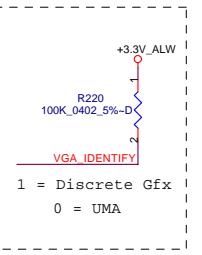
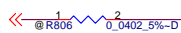
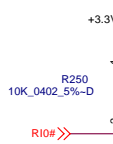
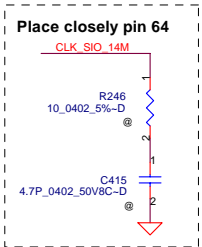
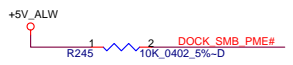
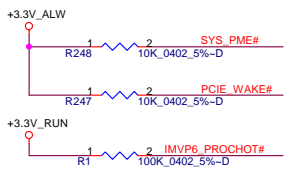


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REV	BID1	BID0
X00	0	0
X01	0	1
X02	1	0
X03	1	1

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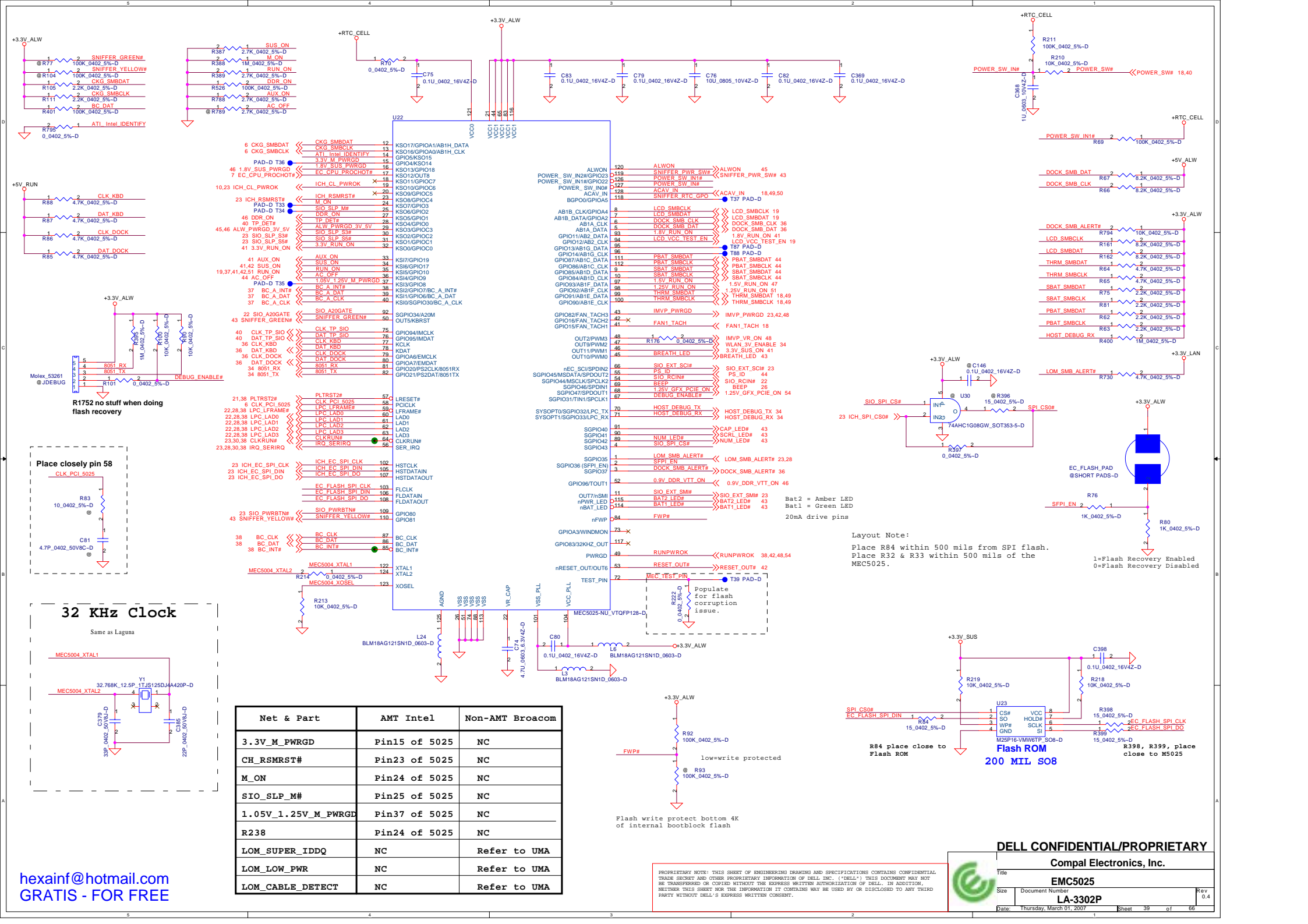
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Title: **ECE5028**

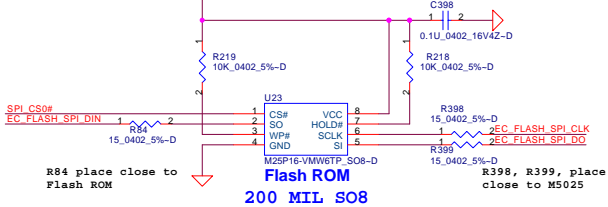
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Net & Part	AMT Intel	Non-AMT Broacom
3.3V_M_PWRGD	Pin15 of 5025	NC
CH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA
LOM_LOW_PWR	NC	Refer to UMA
LOM_CABLE_DETECT	NC	Refer to UMA

Layout Note:  
Place R84 within 500 mils from SPI flash.  
Place R32 & R33 within 500 mils of the MEC5025.



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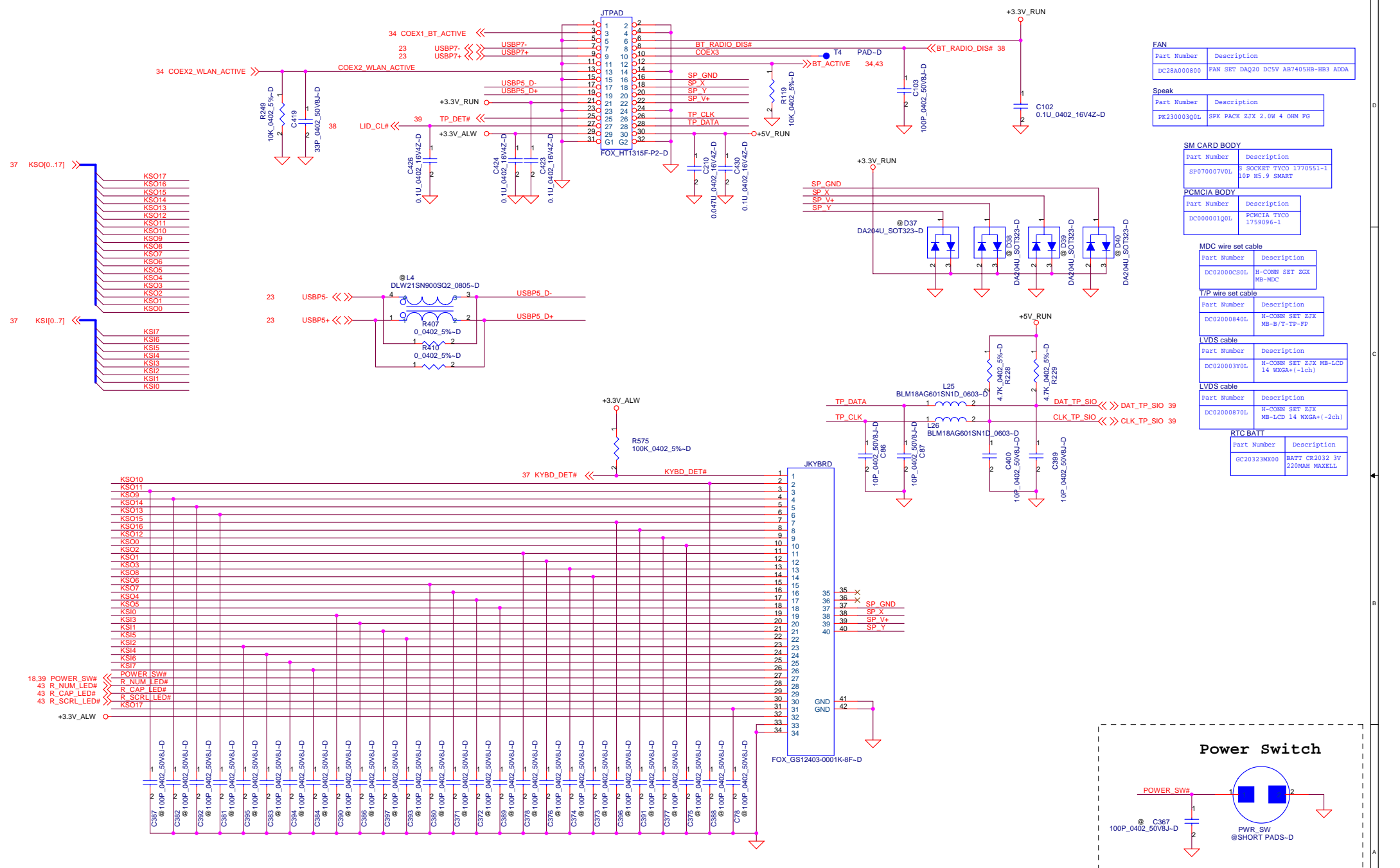
EMC5025

LA-3302P

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### Touch PAD



FAN	
Part Number	Description
DC28A00800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Speak	
Part Number	Description
PK23003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

SM CARD BODY	
Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P HS.9 SMART

PCMCIA BODY	
Part Number	Description
DC00001Q0L	PCMCIA TYCO 1759096-1

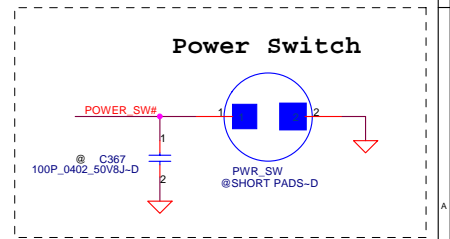
MDC wire set cable	
Part Number	Description
DC02000CS0L	H-CONN SET 2GX MB-MDC

T/P wire set cable	
Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

LVDS cable	
Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

LVDS cable	
Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

RTC BATT	
Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL



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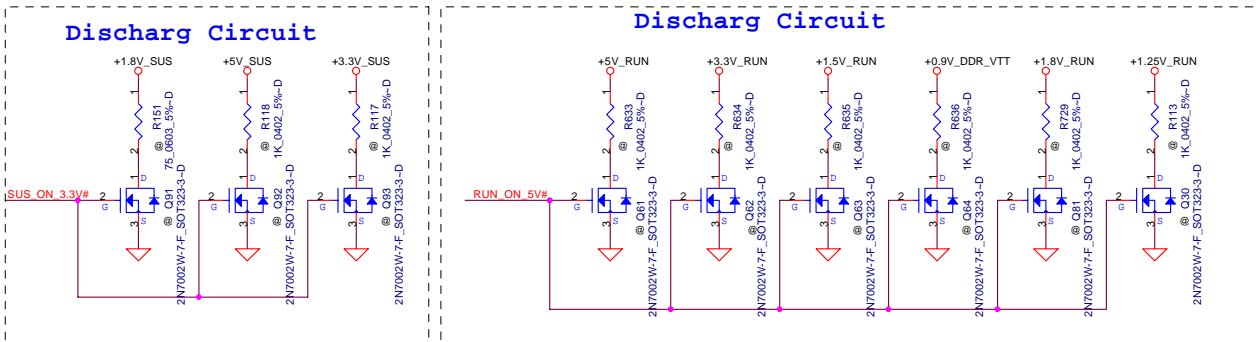
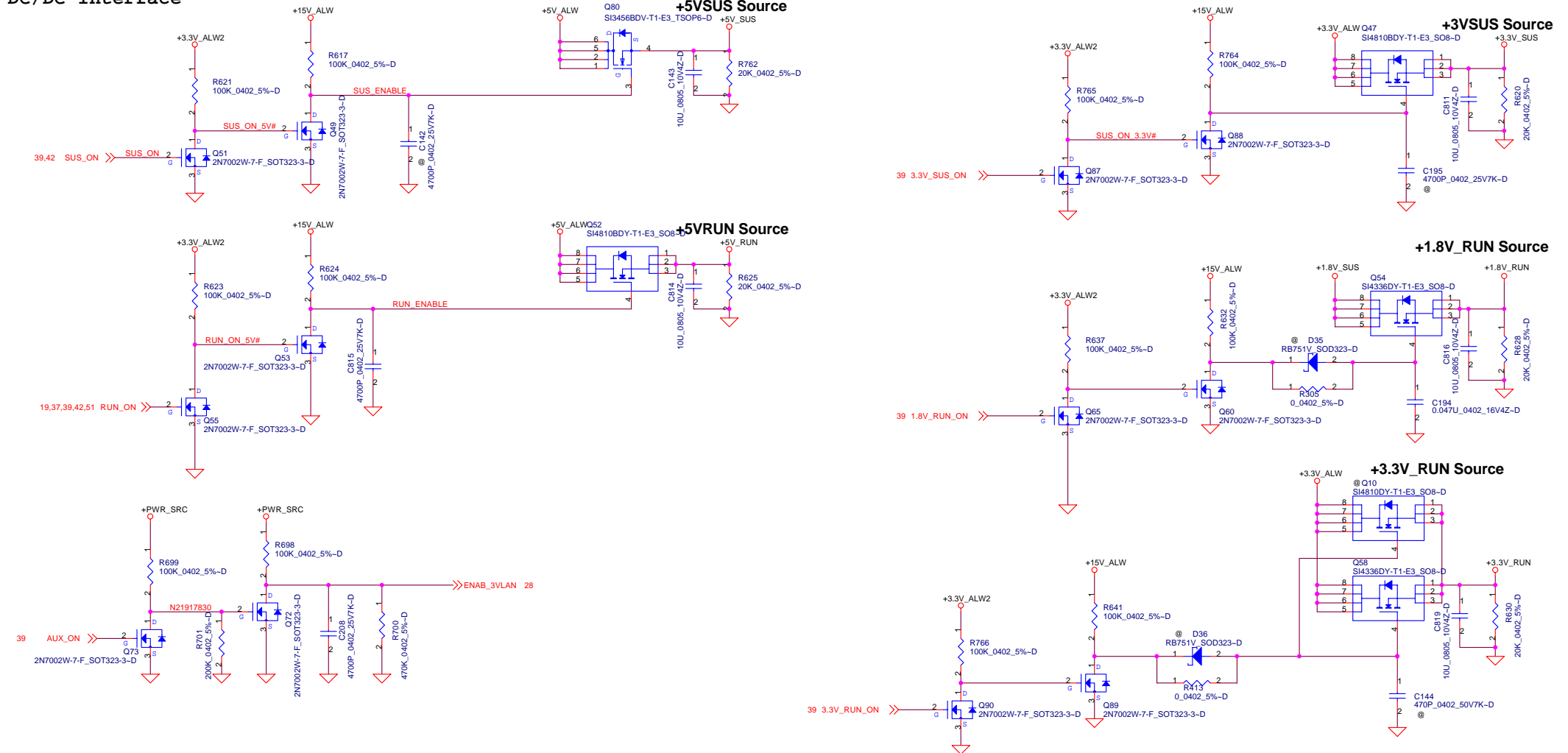


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# DC/DC Interface



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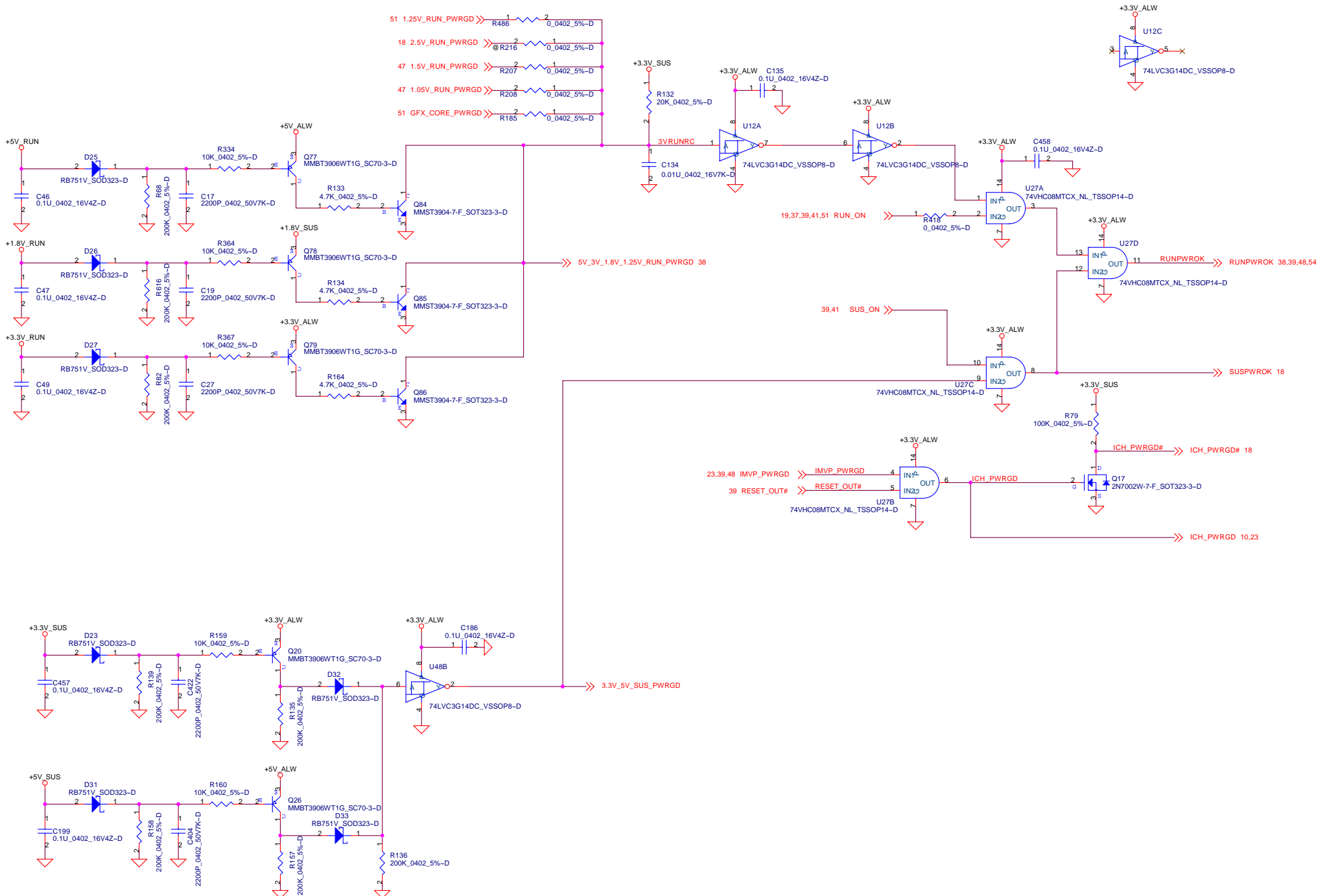
POWER CONTROL

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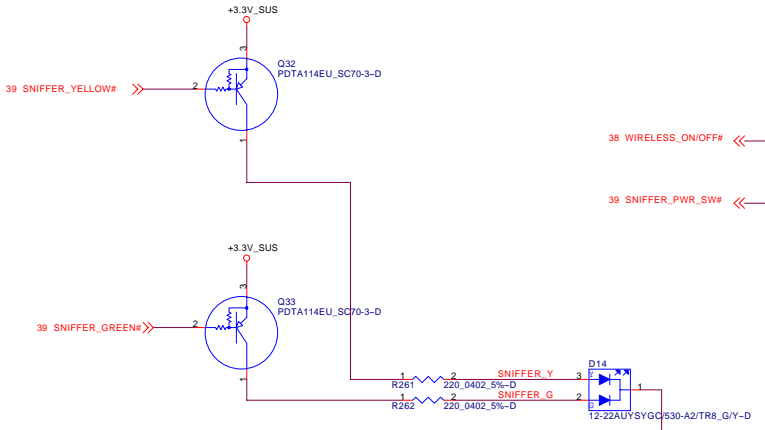
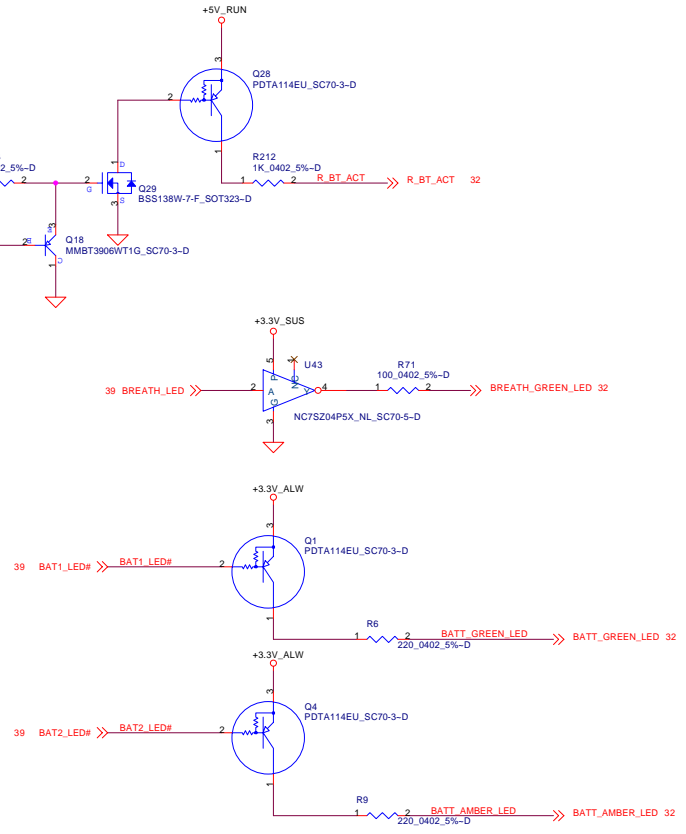
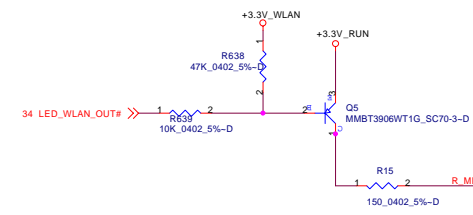
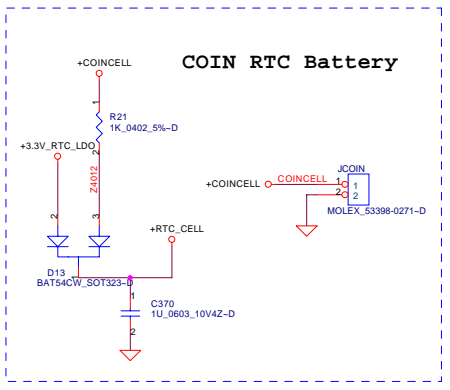
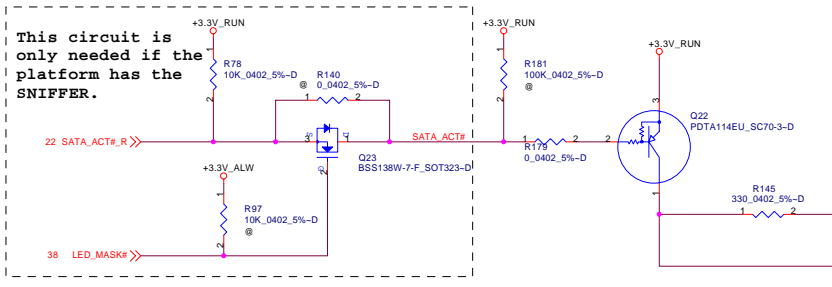
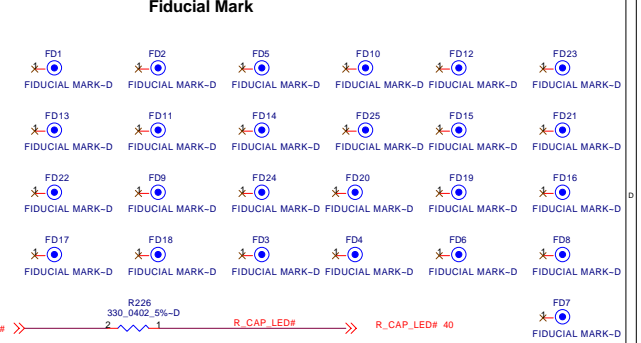
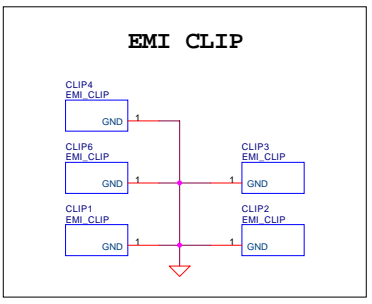
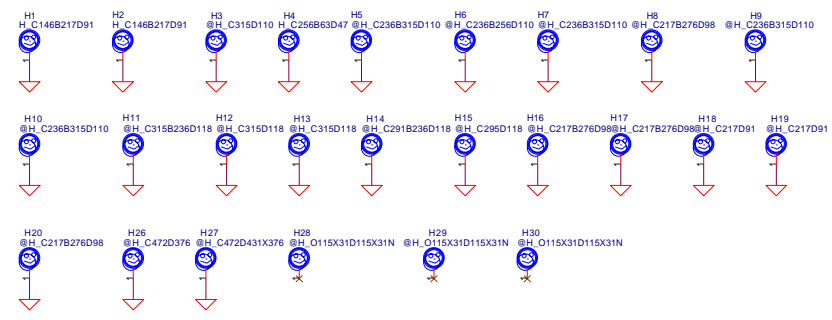
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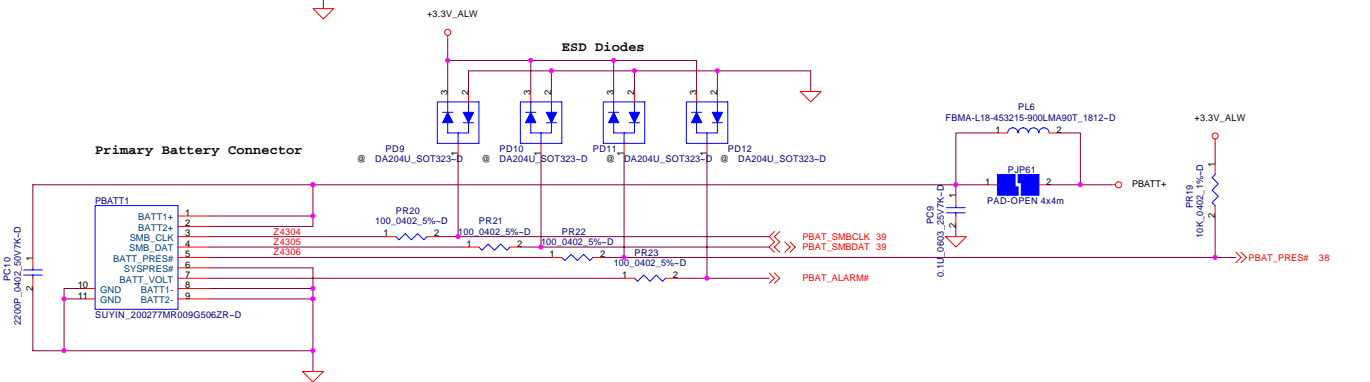
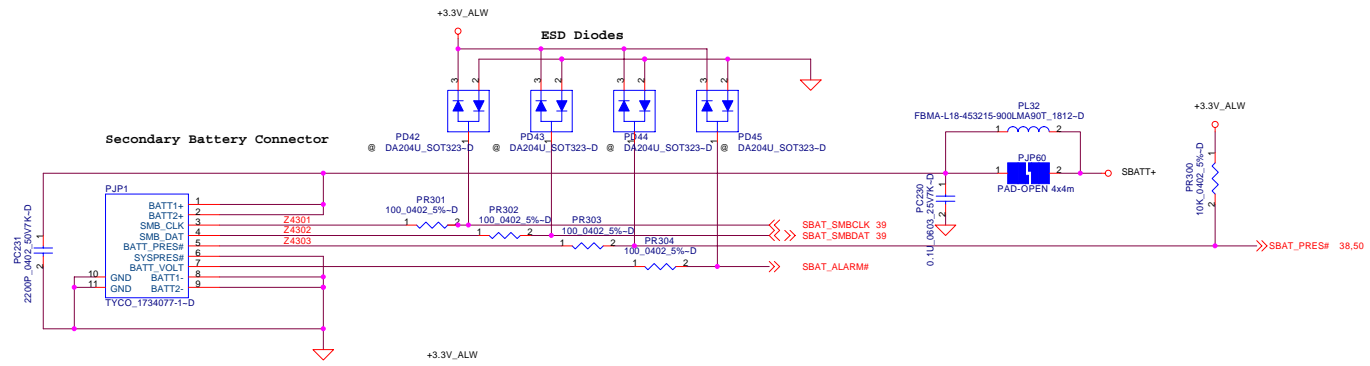
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Title: **PAD and Standoff**

Size: Document Number: **LA-3302P**

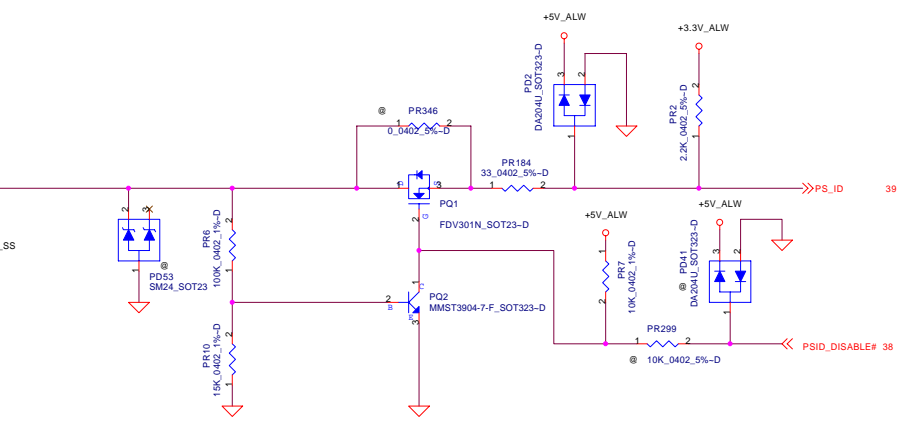
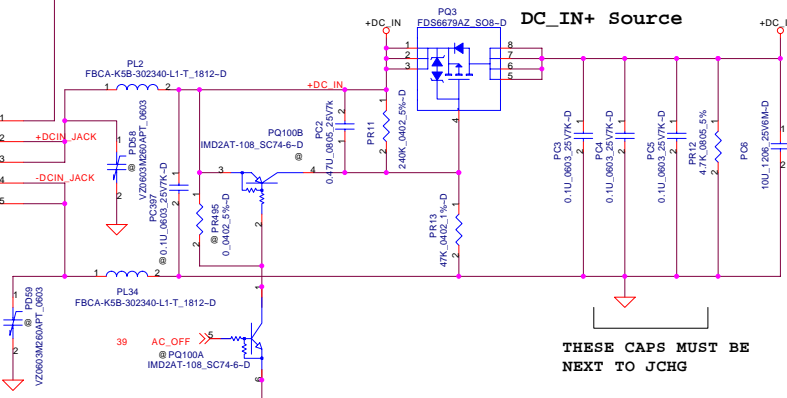
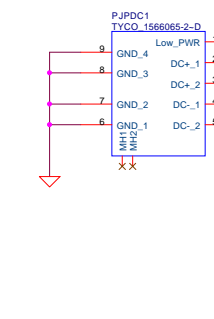
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GPIO Input from EC



Z-series AC Adaptor Connector



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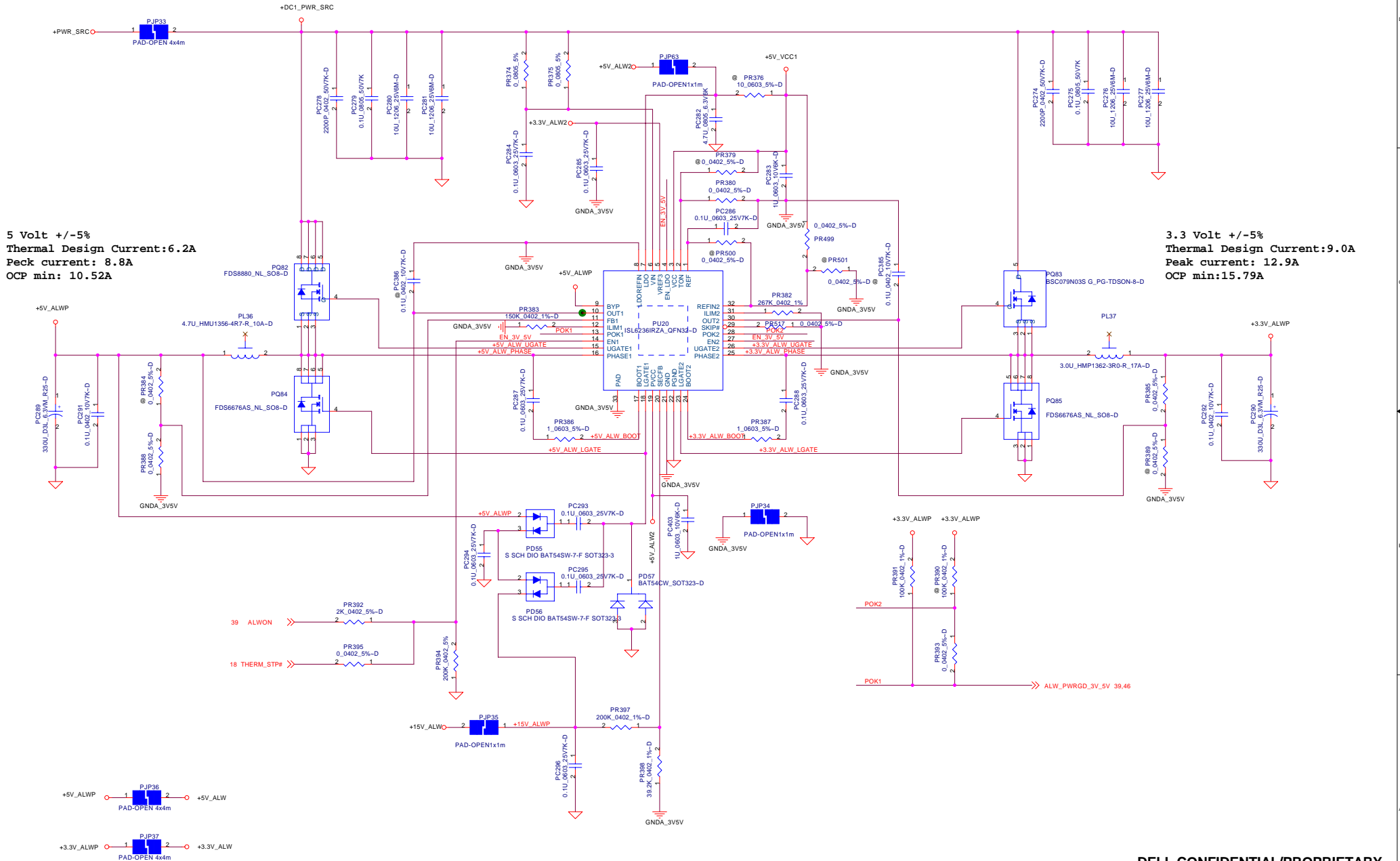
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**+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP**



**5 Volt +/-5%**  
**Thermal Design Current: 6.2A**  
**Peak current: 8.8A**  
**OCp min: 10.52A**

**3.3 Volt +/-5%**  
**Thermal Design Current: 9.0A**  
**Peak current: 12.9A**  
**OCp min: 15.79A**

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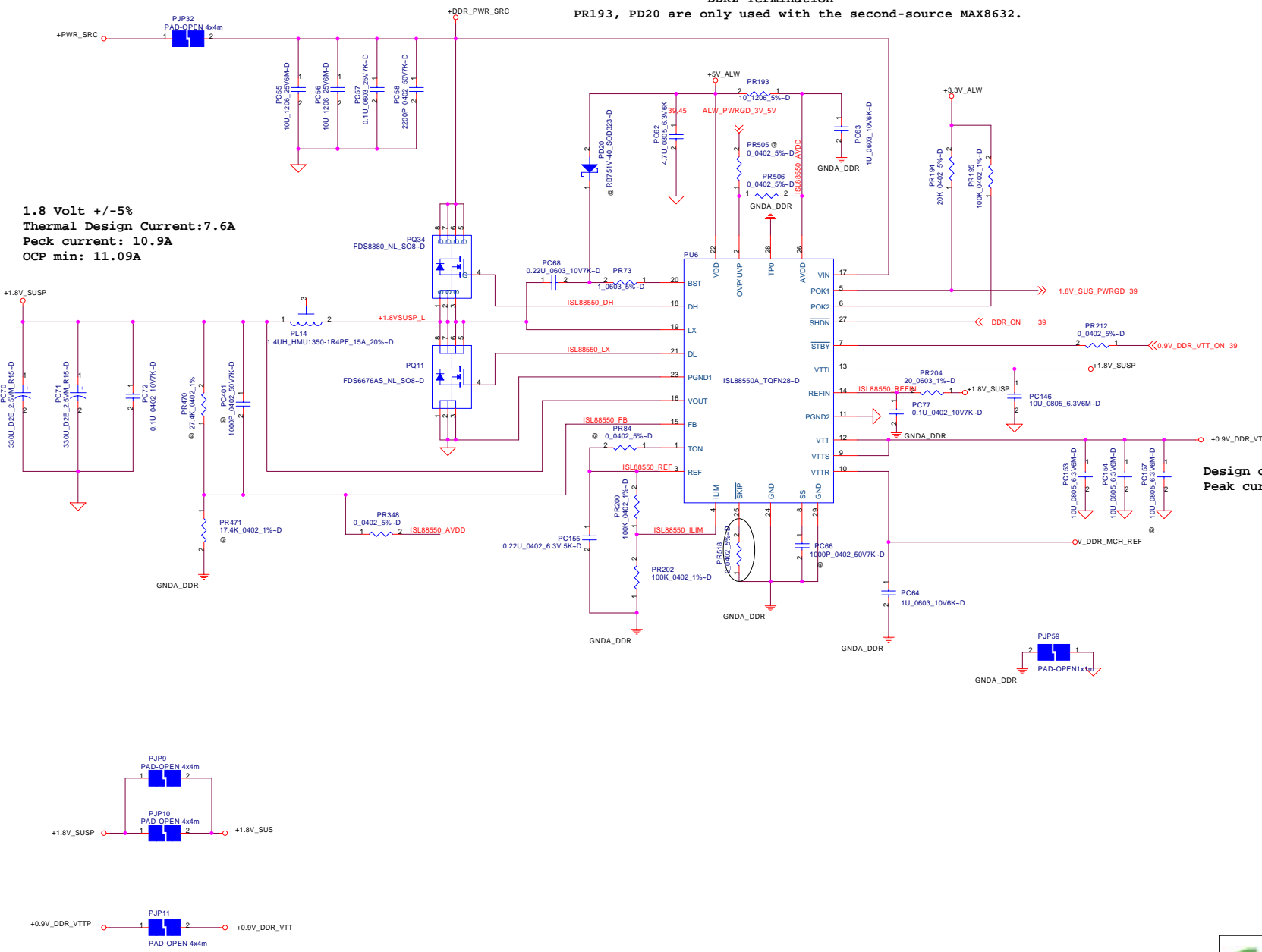
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File	DC/DC +3V/ +5V		
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# +1.8VSUSP/ +0.9V\_DDR\_VTT

## DDR2 Termination

PR193, PD20 are only used with the second-source MAX8632.



1.8 Volt +/-5%  
 Thermal Design Current: 7.6A  
 Peck current: 10.9A  
 OCP min: 11.09A

Design current 0.7A for +0.9V\_DDR\_VTTP  
 Peak current 1A for +0.9V\_DDR\_VTTP

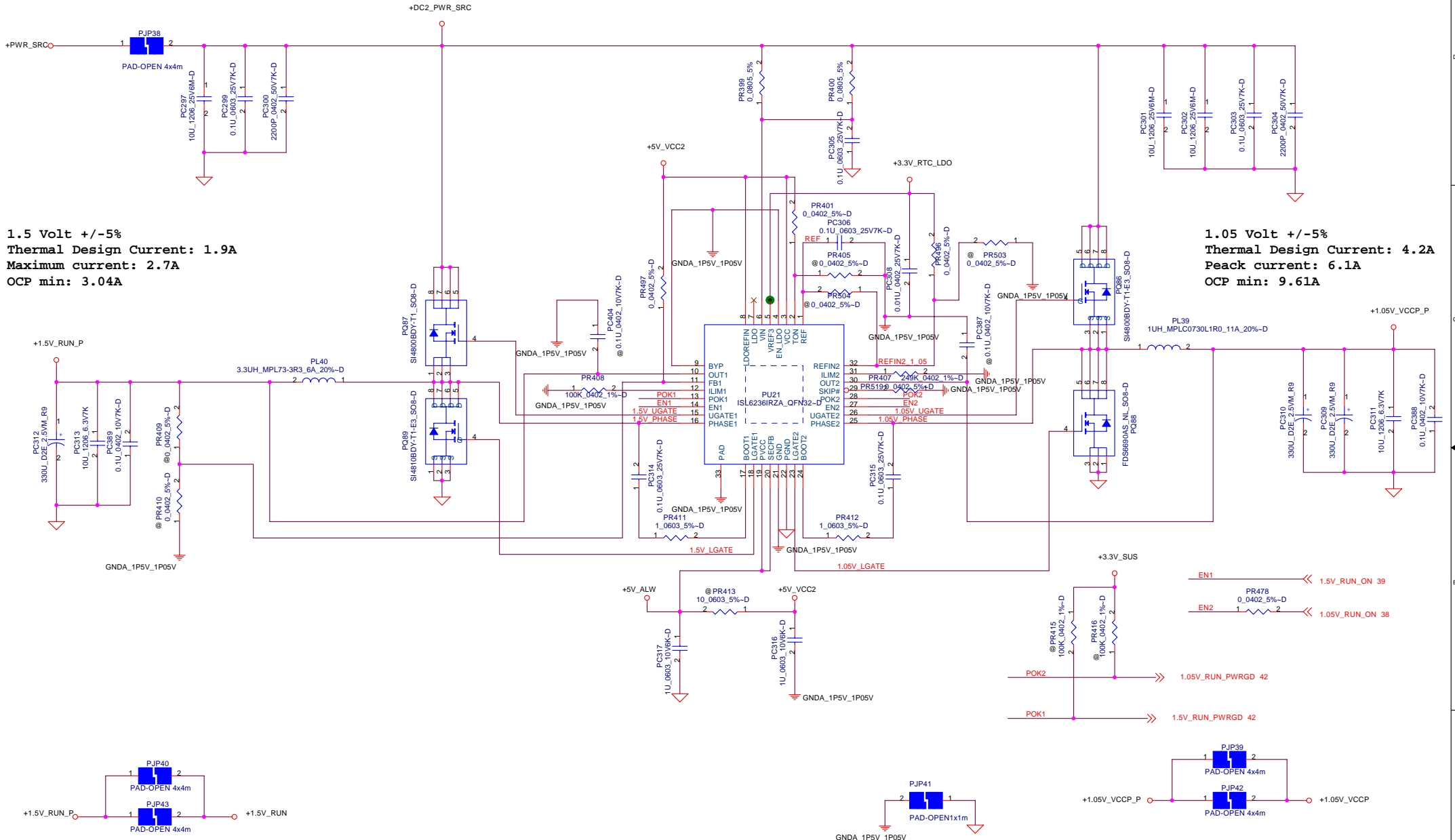
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<b>+1.8VSUSP/ +0.9V_DDR_VT</b>	
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**+1.5V\_RUN / +1.05V\_VCCP / +3.3V\_ALW / +3.3V\_RTC\_LDO**

**1.5 Volt +/-5%**  
**Thermal Design Current: 1.9A**  
**Maximum current: 2.7A**  
**OCP min: 3.04A**

**1.05 Volt +/-5%**  
**Thermal Design Current: 4.2A**  
**Peak current: 6.1A**  
**OCP min: 9.61A**



OK to Short if CAD System can Support

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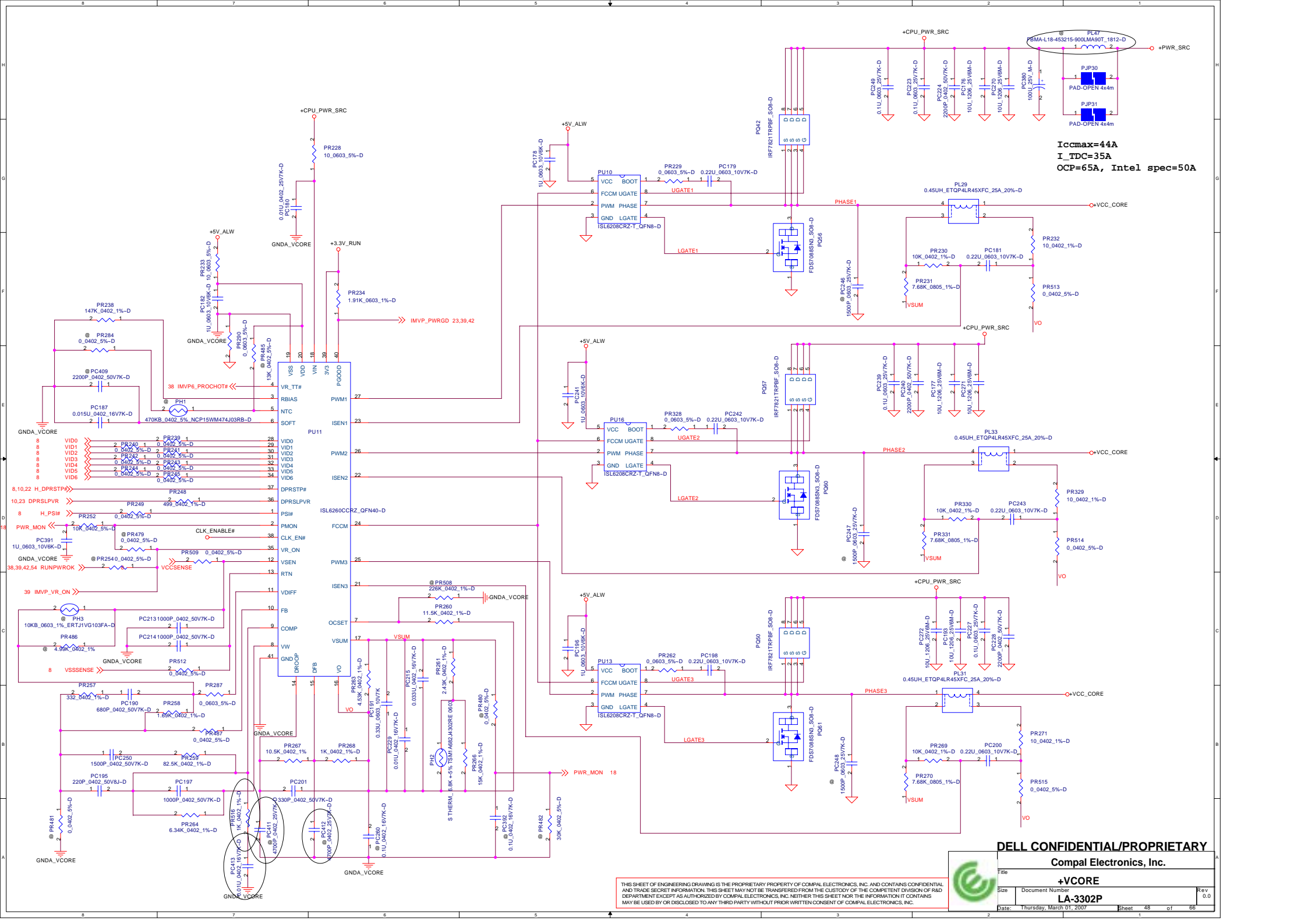
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Title: **+1.5V\_RUN / +1.05V\_VCCP**

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Iccmax=44A  
I\_TDC=35A  
OCP=65A, Intel spec=50A

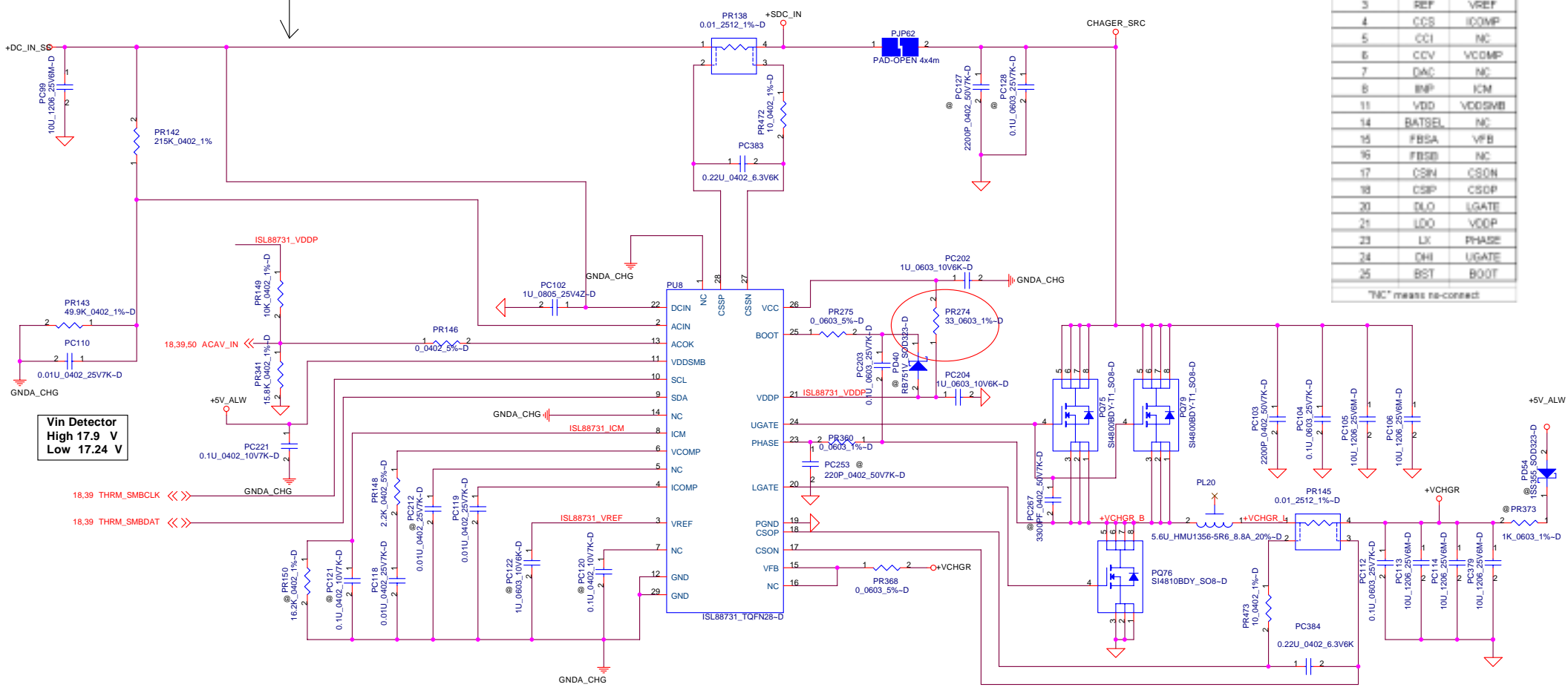
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+VCCORE	
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+DC\_IN discharge path

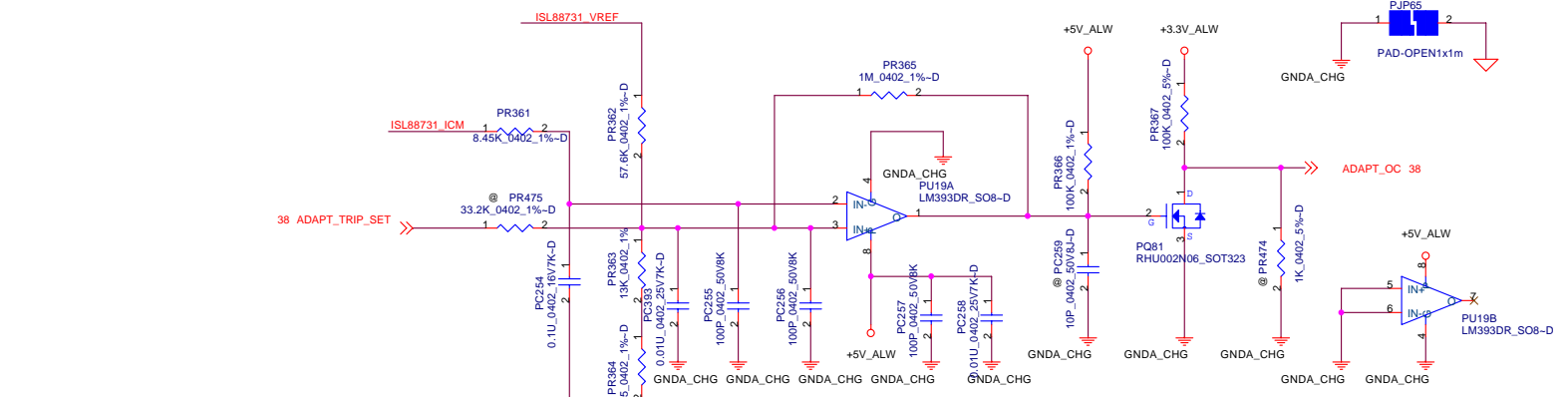


Vin Detector  
High 17.9 V  
Low 17.24 V

PIN	MAXIM	INTERSIL
1	GN0	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IMP	ICM
11	VDD	VDD5MB
14	BATSEL	NC
15	FB5A	VFB
16	FB5B	NC
17	CSIN	CS0N
18	CSP	CSDP
20	DLO	LGATE
21	LOO	VPOE
23	LX	PHASE
24	DH	UGATE
25	BST	BOOT

"NC" means no-connect

Maximum charging current is 6.24A



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Charger

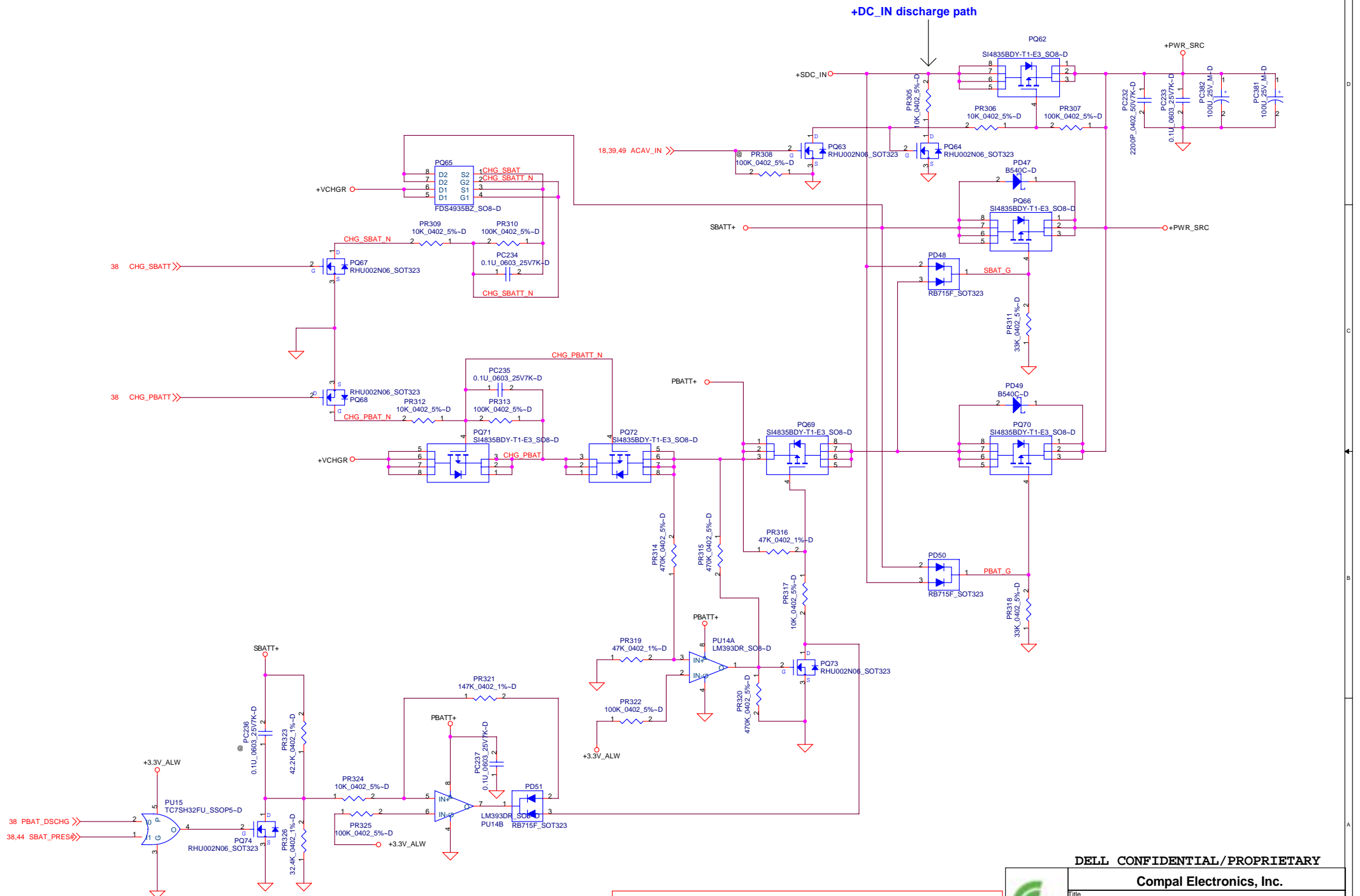
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GPU\_COREP/ +1.25V\_RUN

1.25 Volt +/-5%  
 Thermal Design Current:2.1A  
 Peak current: 3A  
 OCP min: 6.31A

GPU\_CORE  
 Thermal Design Current:7.7A  
 Peak current: 11A  
 OCP min: 12.23A

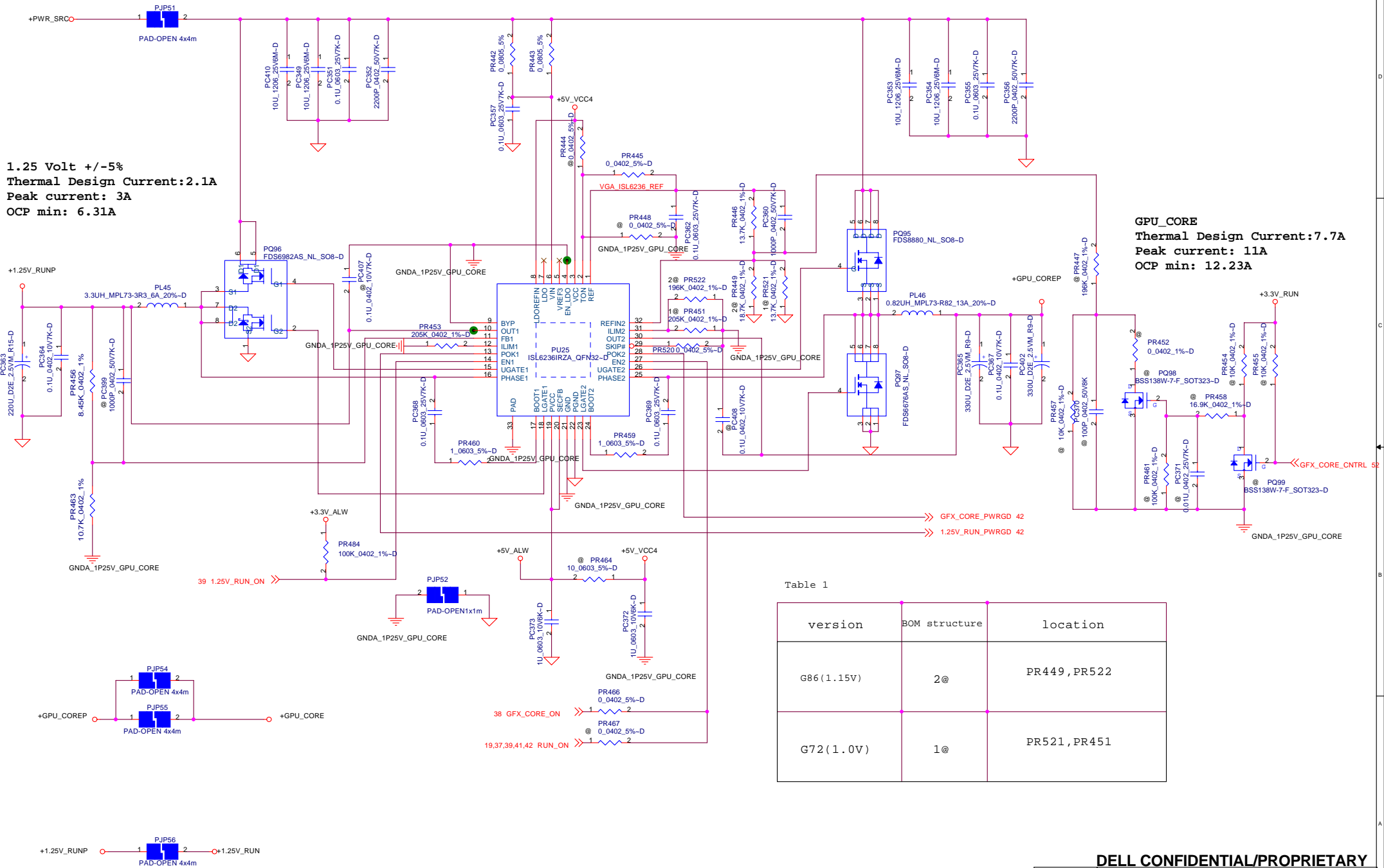


Table 1

version	BOM structure	location
G86(1.15V)	2@	PR449, PR522
G72(1.0V)	1@	PR521, PR451

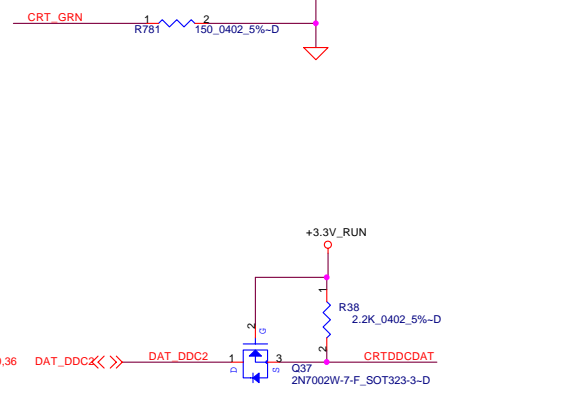
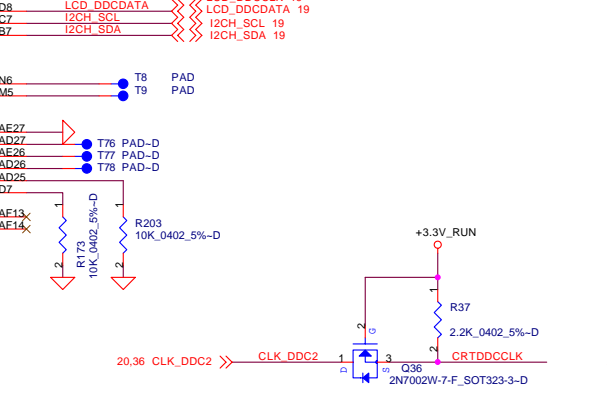
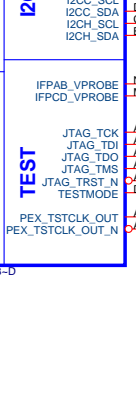
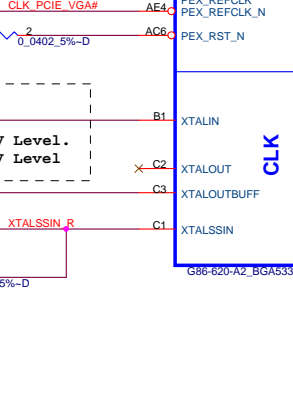
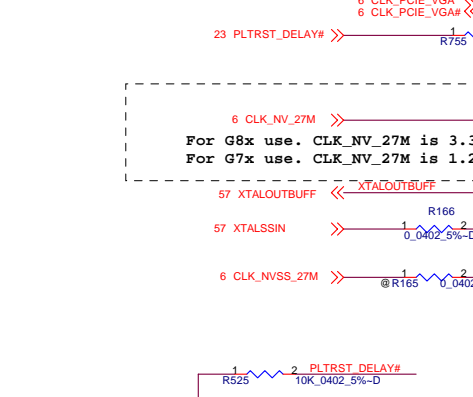
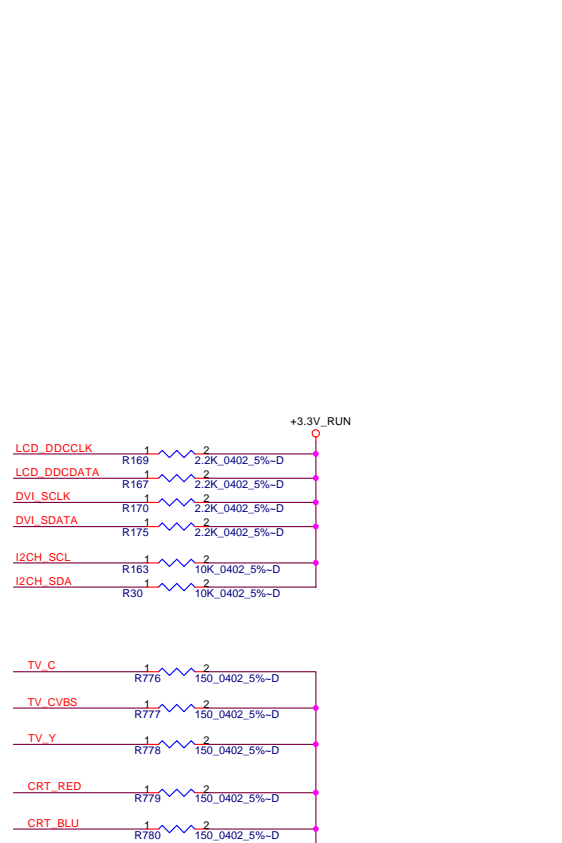
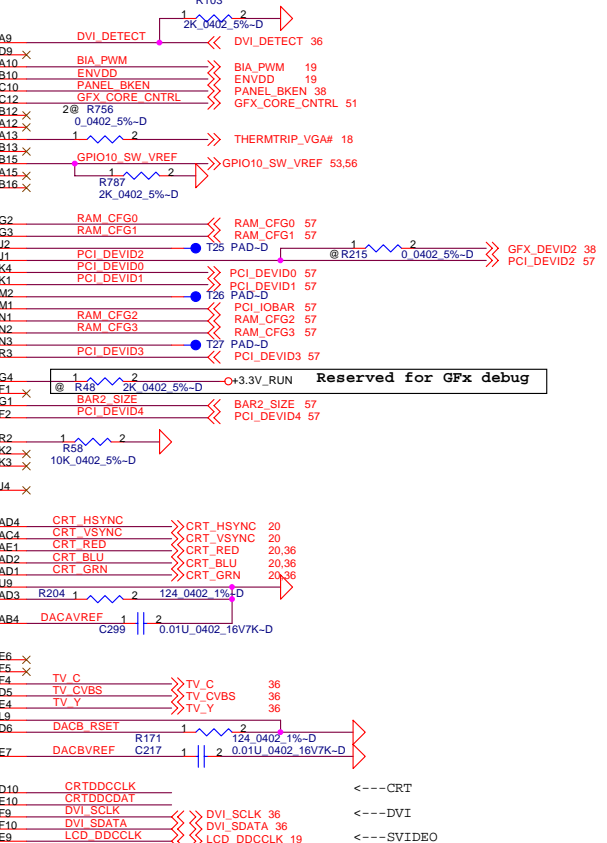
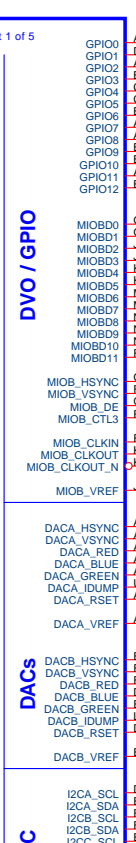
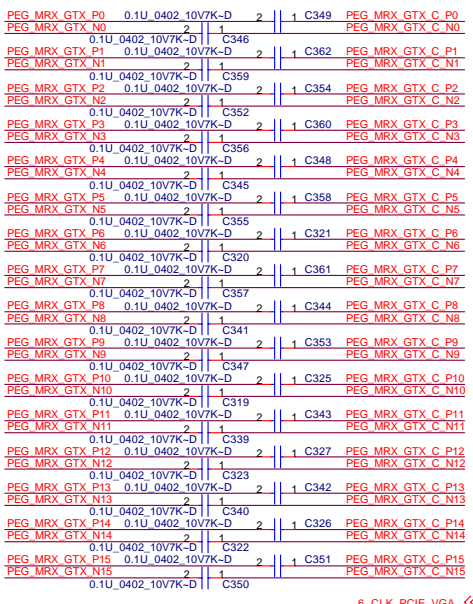
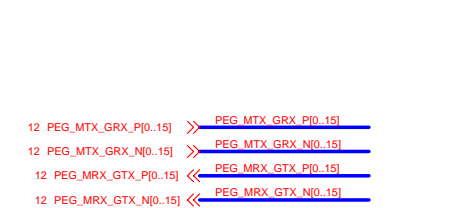
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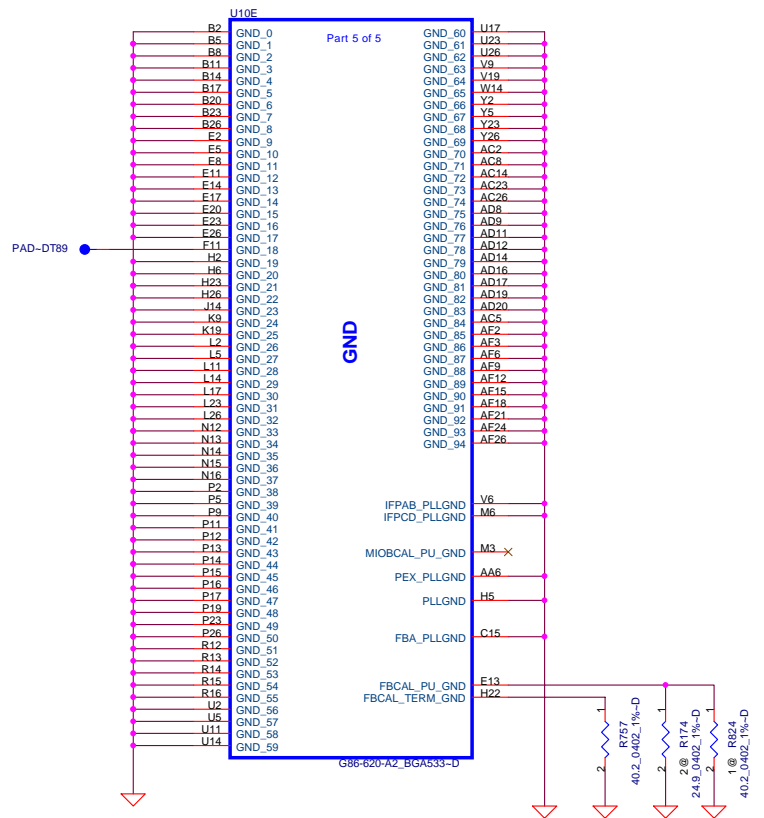
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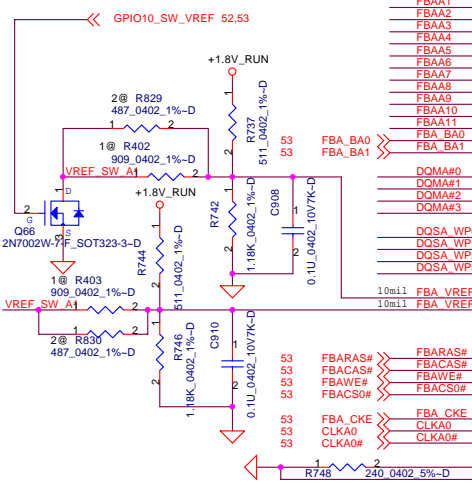
Populate R824 for G72MV  
 Populate R174 for G86.  
 R174,R824 place overlap

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<b>NVG86 Ground</b>		
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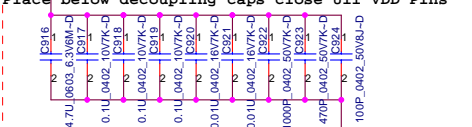
R829,R830 for G86  
R402,R403 for G72MV.  
R829,R402 and R830,R403 place overlap



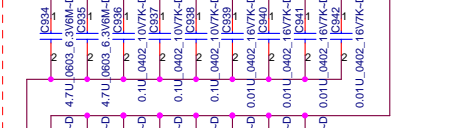
Populate R827 for G86  
Populate R172 for G72MV.  
R172,R827 place overlap  
and close to U49



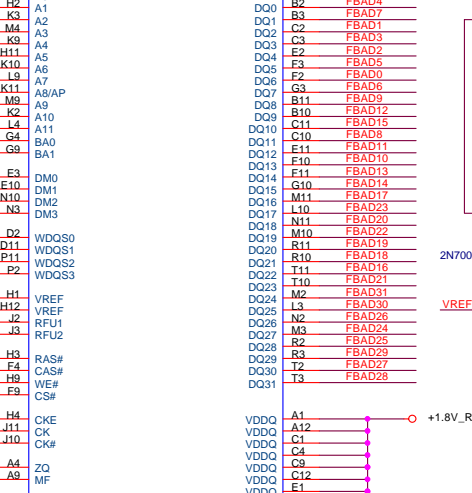
Place below decoupling caps close U11 VDD Pins



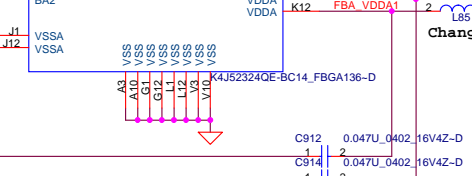
Place below decoupling caps close U11 VDDQ Pins



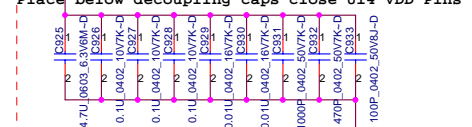
R831,R832 for G86  
R404,R405 for G72MV.  
R831,R404 and R832,R405 place overlap



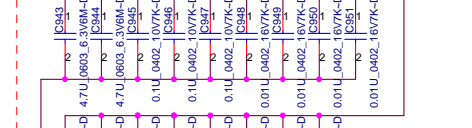
Populate R826 for G86  
Populate R177 for G72MV.  
R177,R826 place overlap  
and close to U50



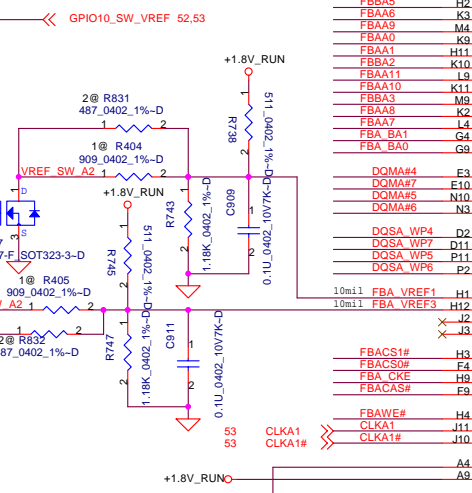
Place below decoupling caps close U14 VDD Pins



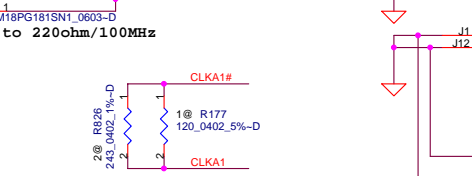
Place below decoupling caps close U14 VDDQ Pins



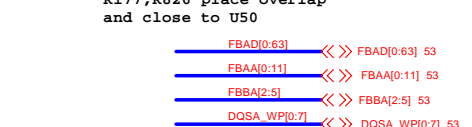
VREF=VDDQ x Rb/(Ra+Rb)  
VREF=0.7 x VDDQ for G86 trun on, 0.4x VDDQ when trun off  
VREF=0.7 x VDDQ for G72MV trun on, 0.5x VDDQ when trun off



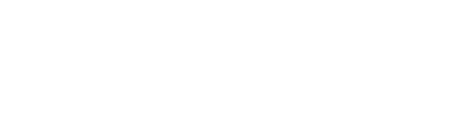
Populate R826 for G86  
Populate R177 for G72MV.  
R177,R826 place overlap  
and close to U50



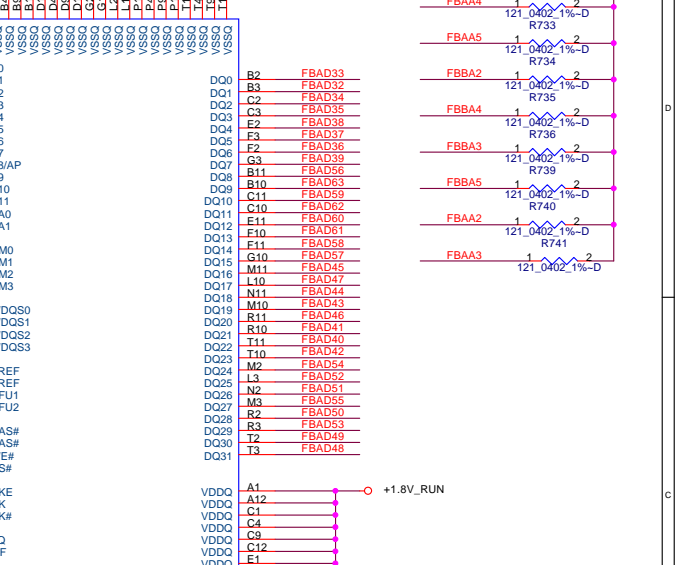
Place below decoupling caps close U14 VDD Pins



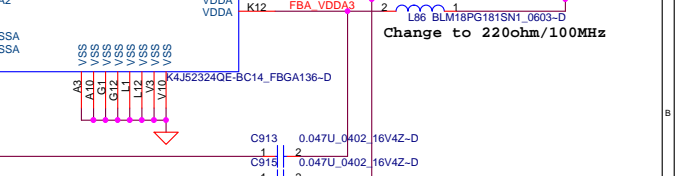
Place below decoupling caps close U14 VDDQ Pins



VREF=VDDQ x Rb/(Ra+Rb)  
VREF=0.7 x VDDQ for G86 trun on, 0.4x VDDQ when trun off  
VREF=0.7 x VDDQ for G72MV trun on, 0.5x VDDQ when trun off

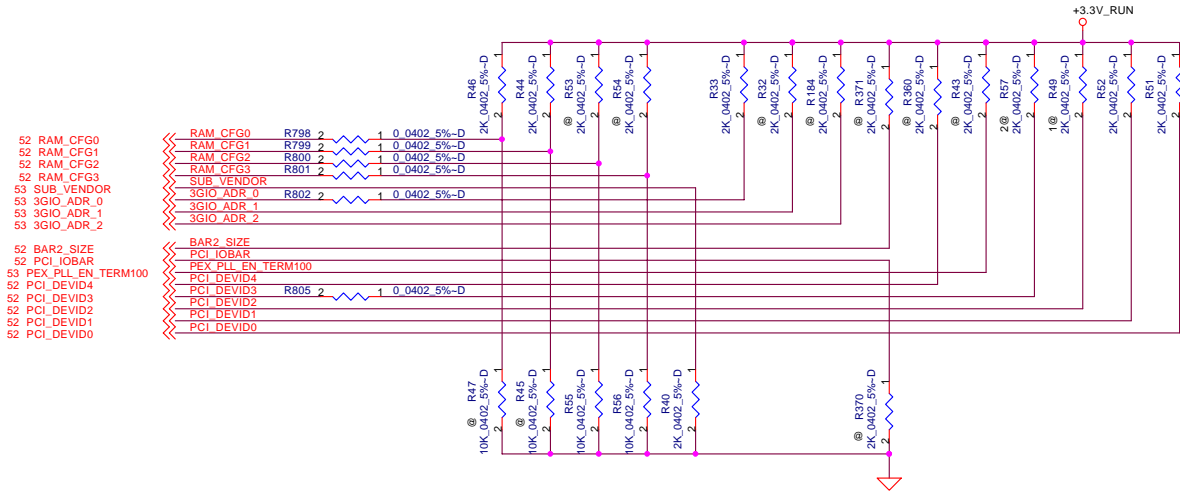


Populate R826 for G86  
Populate R177 for G72MV.  
R177,R826 place overlap  
and close to U50



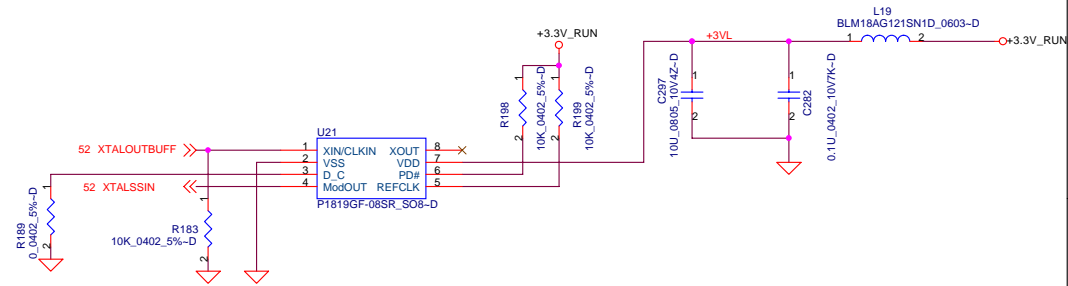


G72MV STRAPS



Device ID strapping				
	DEVID3	DEVID2	DEVID1	DEVID0
<b>G72GLM</b>	1	1	0	0
<b>G72M</b>	1	0	0	0
<b>G72MV</b>	0	1	1	1
<b>G86MV</b>	1	0	1	1

STRAPS	PIN	DESCRIPTION	Value	
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT, Serial SST45VF=10, LPC=11	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	For GDDR1	8Mx32 DDR monolithic (64bit) 300MHz, 1.8V	0001
			8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
			8Mx32 DDR (Samsung K4D5323QF-GC) 300MHz, 1.8V	0010
		For GDDR3	4Mx32 DDR generic (64bit) 1.8V I/O	0100
			4Mx32 DDR generic (32bit) 1.8V I/O	1100
			Infinion 16Mx32 500MHz, 1.8V	0001
			Hynix 16Mx32 500MHz, 1.8V	0010
			Samsung 16Mx32 500MHz, 1.8V	0011



	S0
-1.75% (DOWN)	0
±0.875% (CENTER)	1

S0 Internal pull up

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hexainf@hotmail.com  
GRATIS - FOR FREE

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	38	HW	08/2/2006	Compal	BID change to X01	Pop R108, depop R106	X01
2	18	HW	08/10/2006	Compal	Change SOT23 package to SOT323 package	Change Q102, Q59 to SOT323 package	X01
3	7	HW	08/21/2006	Compal	BITS issue WI86517 (S5 state back driver issue)	Change R324 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
4	41	HW	08/21/2006	Compal	Bits issue WI84312 (Derating issue)	Change R151 from 30 ohm to 75 ohm	X01
5	23	HW	08/21/2006	Compal	Bits issue WI86509	Populate R761 and change value from 100k to 10k. Change R761 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
6	39	HW	08/21/2006	Compal	Bits issue WI86511	Add R401 (100K) for signal BC_DAT pull up to +3.3V_ALW	X01
7	37	HW	08/21/2006	Compal	Bits issue WI86512	Change R131 to no-stuff and from 4.7k to 100k per SMSC	X01
8	23	HW	08/21/2006	Compal	Bits issue WI86516	R509 PU for SIO_EXT_SMI# change from +3.3V_ALW to +3.3V_SUS to prevent backdrive through the ICH in S4/S5	X01
9	38,39	HW	08/21/2006	Compal	Bits issue WI86518	Swap PSID GPIO from ECE5018 pin 71 with MEC5025 ITP_DBRESET# pin 55	X01
10	38,39	HW	08/21/2006	Compal	Bits issue WI86532	Swap BEEP (ECE5018 GPIOB[6]) with PLTRST_DELAY# (MEC5025 SGPIO46)	X01
11	18	HW	08/21/2006	Compal	Bits issue WI86752	Change pull-up rail for R773 from +5V_SUS to +3.3V_SUS	X01
12	21	HW	08/30/2006	Compal	Bits issue WI86530	Move SB_NB_PCIE_RST# to GPIO4/PIRQG# pinF12 per M08 design	X01
13	21	HW	09/7/2006	Compal	Bits issue WI86529	Move SB_WLAN_PCIE_RST# to GPIO3/PIRQF# U32 pin G11 per M08 direction, add test point T1 on pin F18	X01
14	39	HW	09/7/2006	Compal	Bits issue WI86376. Due to increase in number of payloads the BIOS is carrying	Change U23 from ( ST M25P80 8M bit ) to ( MXIC MX25L1605AM2C 16M bit )	X01
15	54	HW	09/7/2006	Compal	Bits issue WI87262. Add depopulated soft start capacitor	Add C85 (470PF_0402) across R244	X01
16	43	HW	09/11/2006	Compal	Bits issue WI90535	Change Q5 to MMBT3906WT1G, R15 to 150 ohm. Add R638 on LED_WLAN_OUT# pull up to +3.3V_WLAN. Add R639 (10K ohm) in series on LED_WLAN_OUT#	X01
17	7	HW	09/14/2006	Compal	Briscoe ESD/EMI Improvement Requests on PT	Remove ITP port and just keep ITP test point	X01
18	34	HW	09/14/2006	Compal	Bits issue WI90713	No stuff C16	X01
19	43	HW	09/14/2006	Compal	Bits issue WI90712	Remove R73, R178, C192, and C193	X01
20	43	HW	09/14/2006	Compal	Bits issue WI90705	Add SMBus isolation circuit for WLAN, R640,R645,R660,R662,Q45,Q46	X01
21	34	HW	09/14/2006	Compal	Bits issue WI90696	JMINI1 connect to +3.3V_RUN. Removed C427	X01
22	12	HW	09/14/2006	Compal	Shunt caps on LVDS for improving WWAN	Add C181,C192,C193,C196,C207,C209 cross LVDS signals	X01
23	27	HW	09/14/2006	Compal	Bits issue WI90516	Remove C759 from mic amp bias circuit	X01
24	26	HW	09/14/2006	Compal	Bits issue WI90487	Populate R541to cut BEEP level in half	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	18,52	HW	09/14/2006	Compal	Bits issue WI90207	Connect THERMTRIP_VGA# from U10 pinB13 to U10 pin A13. Populate R186 for THERMTRIP_VGA# pull up	X01
26	43	HW	09/14/2006	Compal	Bits issue WI89637	Populate EMI Clips Clip1, Clip2, Clip3, Clip4, Clip6	X01
27	23	HW	09/14/2006	Compal	Bits issue WI89409	No stuff R516, add R690 (8.2K ohm) for pull up ICH8 pin AF22 to +3.3V_SUS	X01
28	25	HW	09/14/2006	Compal	Bits issue WI89407	Add Q68, Q69, R691, R692 for HDDC_EN and MODC_EN circuits	X01
29	41	HW	09/14/2006	Compal	Bits issue WI89394	Change connect R765 pin1, R623 pin1, R621 pin1, R766 pin1, R637 pin1, R300 pin1 from +5V_ALW to +5V_ALW2	X01
30	37,39	HW	09/14/2006	Compal	Bits issue WI89379	Change R387,R389 from 1M to 2.7K. Add R778,R779 for AUX_ON,AC_OFF	X01
31	39	HW	09/15/2006	Compal	Bits issue WI92249	Change R730 from 100K to 4.7K ohm	X01
32	57	HW	09/15/2006	Compal	Bits issue WI92188. The MIO_A_D0 signal has an internal pull-down in the GPU	Remove R39	X01
33	53,55	HW	09/18/2006	Compal	Bits issue WI92289	U10 (NV86) pin F11,F12 connect to test point T89,T90 for testing and debug	X01
34	23	HW	09/18/2006	Compal	Bits issue WI92296	PLTRST_DELAY# move from ECE5018 GPOB[6] to ICH8 GPIO38	X01
35	34	HW	09/18/2006	Compal	Bits issue WI92287,WI90716	R660 and R662 connected to CLK_SCLK and CLK_SDATA.	X01
36	57,37,22,33,28,19,20	HW	09/18/2006	Compal	EMI solutions	Populate SSCG U21,R189,R198,R199,L19,C297,C282,R166. depopR165. Populate RS232 C152,153,154,155,156,157,158,159. Resume ICH_AZ_MDC_BITCLK C656,R123,C128. Add R790,R791,C232, C267. Change L63,L65 from 0603size to 0805size. Add C309,C316 for LOM. Add C427,C463 for LVDS. Add fuse F3, R792 for CRT. Populate C660, R545 (10 ohm),C721 (10P)	X01
37	23,36	HW	09/18/2006	Compal	Bits issue WI92298	Move SIO_EXT_SCI# from to ICH8 GPIO11/SMBALERT# pin AG22 to GP012 pin AC19. Remove D22 and R761 and net DOCK_DET#	X01
38	23	HW	09/18/2006	Compal	Bits issue WI92299	ICH8 Pin AG22 tie to LOM_ICH_SMBALERT#. Add R793 (0 ohm) series on LOM_ICH_SMBALERT# and LOM_SMB_ALERT#. Change R730 pull up rail from +3.3V_ALW to +3.3V_LAN. Add R807 pull up to +3.3V_SUS for LOM_ICH_SMBALERT#	X01
39	39	HW	09/18/2006	Compal	Bits issue WI92301	Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to MEC5025 pin 29. Remove 3.3V_5V_SUS_PWRGD from MEC5025 pin 29	X01
40	38,39	HW	09/18/2006	Compal	Bits issue WI92305	Swap DOCK_SMB_PME and DOCK_SMB_ALERT# from MEC5025 pin3 and ECE5028 pin76	X01
41	39,42	HW	09/18/2006	Compal	Bits issue WI92308	Removed 3.3V_LAN_PWRGD from MEC5025 KSO15/GPIO5. Remove U52,Q83,D29,R89,R98,R381,C784,C182,C183,C184	X01
42	39	HW	09/18/2006	Compal	Bits issue WI92312	Add R795 (10K ohm) pull down for MEC5025 pin 14	X01
43	29	HW	09/19/2006	Compal	EMI issue	Populate R671~R678 and C866~C869. Change L69~L76 from 24NH to 36NH inductor	X01
44	27	HW	09/19/2006	Compal	Bits issue WI90510	Add R796,R797 (0ohm) between L47/L48 and C728/C730	X01
45	57	HW	09/20/2006	Compal	EMI request	Add R798~R803 for strap damping	X01

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46	18	HW	09/20/2006	Compal	Bits issue WI92860	Depop Q39 and R427	X01
47	28	HW	09/20/2006	Compal	Bits issue WI92858	Change R669 to from 1.15K to 1.13K. Depop C771 & C772. Change C861 and C862 to 22pF	X01
48	38	HW	09/20/2006	Compal	Bits issue WI92857	Add no-stuff series 0-ohm for ITP_DBRESET# on ECE5028	X01
49	33	HW	09/21/2006	Compal	Bits issue WI93157	Remove R586 and make JMDC pin2 NC	X01
50	34	HW	09/21/2006	Compal	Bits issue WI93158	Depop Q45, Q46	X01
51	6	HW	09/25/2006	Compal	Bits issue WI93403	C484 change to 33pF, C861/C862 change to 22pF	X01
52	29	HW	09/26/2006	Compal	Bits issue DF86424	No Populate C866-C869/R671-R678	X01
53	40	HW	09/26/2006	Compal	EMI request	Add D37-D40 for stick point signals	X01
54	32	HW	09/27/2006	Compal	Bits issue DF94094	Add FUSE4,FUSE5	X01
55	9	HW	09/28/2006	Compal	Bits issue WI94923	C329,C330 chagne back to 10 0805 X6S	X01
56	18	HW	10/05/2006	Compal	Bits issue WI94892	Populate R771, C750, R772, Q102, R773	X01
57	30	HW	10/05/2006	Compal	Bits issue WI95910	Change R603 from 6.2k to 5.9k. Change C805 from 820pF to 270pF	X01
58	38,23 27,6	HW	10/05/2006	Compal	Bits issue WI95932	No stuff R227, R221, C89, C93, C97, c401, C92, r72, C90, C94. No stuff C775-C781, C785. No stuff R514 (no iAMT). Populate R515.	X01
59	36	HW	10/14/2006	Dell	Bits issue WI97539	Added signal DOCK_DET# to JDOCKBpin137, pin205 and Q3pin2	X02
60	9	HW	10/17/2006	Dell	Bits issue WI97837	Add 0.1 uf (0402) caps on +Vcc_Core to Gnd. Four total, bottom of board. (C870 ~ C873)	X02
61	23	HW	10/18/2006	Dell	Bits issue WI98222 (Change for ASF2.0 due to ICH8M errata )	1. No stuff R502, R503 2. Connect the pad of R503.2 to the pad of R498.2 3. Connect the pad of R502.1 to the pad of R499.2	X02
62	38	HW	10/24/2006	Dell	Board ID Changed to X02	Populated R106, R107. Depopulated R108, R109.	X02
62	38	HW	10/24/2006	Dell	Bits issue WI98660	The DevID for G86 on Briscoe needs to be updated to 1011	X02
63	23	HW	11/16/2006	Dell	Bits issue WI104573	Add R816,C874 for USB_IDE#. R817,C875 for SIO_EXT_WAKE#. R819,C876 for PCIE_MCARD1_DET#. R820,C878 for USB_MCARD1_DET#. R818,C877 for USB_MCARD2_DET#. Remove net RSVD_GPIO6 and R513	X02
64	6,23,34	HW	11/16/2006	Dell	Bits issue WI103311	Change R309 from 8.2K to 2.2K. No stuff R820. No stuff R550	X02
65	39	HW	11/18/2006	Dell	Bits issue WI103986	Change C379 from 22pF to 33pF per KDS X'tal report	X02
66	25,41	HW	11/20/2006	Compal	Bits issue WI105207	Change net name from +5V_ALW2 to +3.3V_ALW2 at R618.1, R626.1, R623.1, R621.1, R766.1, R765.1, R637.1, R300.	X03

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67	28	HW	11/21/2006	Dell	Bits issue WI105200	Change L64,L66,L67,L68 from BLM18AG601SN1D to BK1608LM182. Change R668 to L88 BK1608LM182. Change L63, L65 from BLM21AG601SN1D to BK2125LM182.	X02
68	6,54,57	HW	11/21/2006	Dell	Bits issue WI105712	Depop R697, change R286 to 0 ohm. Pop L53, depop L16. Pop L27, C314, C315. Depop L20, L21, pop L54, L55. Depop L17.	X02
69	38,39	HW	11/21/2006	Dell	Bits issue WI105754	Change R794 pin1 from +5V_ALW to +3.3V_ALW. Change R245 pin1 from +3.3V_ALW to +5V_ALW	X02
70	26	HW	11/21/2006	Dell	Bits issue WI105758. Updates for potential Back Drive	Add 100kohm resistor R721 between U35 pin 40 and +3.3V_RUN and 1000pF cap C759	X02
71	21,23,34	HW	12/1/2006	Dell	Bits issue WI106999	Please populate R820 with a 4.7k-ohm resistor. Move signal PCIE_MCARD2_DET# from ICH8m GPIO20 pinAE11 to PIRQH#/GPIO5 pinB3. Delete R457 and net ICH_GPIO5_PIRQH#. Populate R550	X02
72	41	HW	12/1/2006	Dell	Bits issue WI107466. +2.5V_LAN in-rush current test fai.	Populate C208	X02
73	6	HW	12/5/2006	Dell	Bits issue WI107881	Change R286 from 0 ohm to 33 ohms	X02
74	27	HW	12/6/2006	Dell	Bits issue WI107896	Change R554 from 10K to 0 ohm	X02
75	36,38	HW	12/6/2006	Dell	Bits issue WI108259. Per M08 GPIO map rev A15 Change list	Change net DOCK_SMB_PME to DOCK_SMB_PME#	X02
76	9	HW	12/6/2006	Dell	Bits issue WI108223	Change C177,C179,C178,C366,C338,C365 to EEFSX0D221E7 220uF	X02
77	52	HW	12/12/2006	Dell	Bits issue WI109622. Per NB8M PUN document	Change R35 from 60.4 ohm to 40.2 ohm	X02
78	55	HW	12/13/2006	Dell	Bits issue WI109627	Change R174 from 40.2 ohm to 30 ohm	X02
79	39	HW	12/14/2006	Dell	Bits issue WI110179	Add EC_FLASH_PAD pin1 connect to +3.3V_ALW, pin2 connect to R76 pin1 and R80 pin1	X02
80	27	HW	12/15/2006	Dell	Bits issue WI110158	Add R822 (1M_0402) from Pin 10 (C1P) pin of MAX9789A to ground	X02
81	26	HW	12/18/2006	Dell	Bits issue WI110749	Add R823 (10K_0402) to ground on pin 47 of STAC9205 (U37)	X02
82	29	HW	12/20/2006	Dell	Bits issue WI111288	Change R683 from 150ohms to 110 ohms, R684 from 150ohms to 200ohms	X02
83	12,23,28	HW	12/25/2006	Dell	Change AC Coupling Cap SPEC for PCIE	Change C500-C531,C664,C666-C670,C851,C853 from 0.1uF Y5V to 0.1uF X7R	X02
84	54,55	HW	1/5/2007	Dell	Bits issue WI113179	Change R174 to 24.9 ohm for G86, Add R824 40.2 ohm for G72. Change R35 to 45.3 ohm G86, add R825 60.4 ohm for G72MV	X03
85	56	HW	1/5/2007	Dell	Bits issue WI113180	Add R826,R827 243 ohm for G86	X03
86	53,56	HW	1/5/2007	Dell	Bits issue WI113227	Add R828,R829,R830,R831,R832 487 ohm for G86	X03
87	38	HW	1/5/2007	Dell	Chagne Board ID to X03	Populate R108, de-pop R106	X03
88	6	HW	1/8/2007	Dell	Bits issue WI113588	Change U10 value to G86-620-A2. Add R833=147 ohm with R697 use 1@ for G72. R286=33 ohm use 2@ for G86. Change R48 note to "Reserved for GFx debug".	X03

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89	38	HW	1/26/2007	Dell	Bits issue WI115658. M08 GPIO map rev A16 change	Change ECE5028 GPIOF4 from BID2 to CHIPSET_ID.	X03
90	23	HW	2/12/2007	Dell	Bits issue WI121957	Add R834 (1M_0402_1%) for ICH_LAN_RST#	X03
91	27	HW	2/12/2007	Dell	Bits issue WI121438	Change R565 from 10K to 100k ohm	X03
92	41	HW	2/12/2007	Dell	Bits issue DF116813	Depop C194, changed C815 from 4700pF to 2200pF	X03
93	54	HW	2/14/2007	Dell	Modify pop option symbol for G72M/G86M power bead	L53,L27,L55,L54, with 2@, L16,L17,L21, L20, with 1@	X03
94	57	HW	2/14/2007	Dell	Modify NV strap table	Change GDDR3 table from 500 MHz to 700 MHz	X03
95	18	HW	2/26/2007	Dell	Bits issue WI124164	populate C640 = 10uF for G72MV. Add 1@ for C640	X03
96	54 57	HW	2/26/2007	Dell	Bits issue WI124408	Add note "Populate C251, C255 for G86 and G72 solution per Nvidia". Add 2@ for C314, C315, R805 and R57. Add 1@ for R49.	X03
97	54	HW	2/27/2007	Dell	Bits issue WI123608	Change C233 from X5R to X7R	X03
98	23	HW	2/27/2007	Dell	Bits issue WI125173. Per Intel's latest recommendation	Change R834 from 1M to 10K	X03
99	54	HW	2/28/2007	Dell	Bits issue WI123608	Change C233 back to X5R	X03
100	18 52	HW	2/28/2007	Dell	Bits issue WI124613. Need to connect THERMTRIP_VGA to the thermal sensor for G86	Add 2@ for R756, R187, Q76, C203	X03
101	18	HW	3/1/2007	Dell	Bits issue WI125873. Populate circuit for THERMTRIP_MCH#	Populate R427 and Q39	X03
102	27	HW	3/7/2007	Dell	Bits issue WI127300	Change U40 from 74AHC1G08 to 74AHCT1G08	X03

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Compal Electronics, Inc.

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48/50	PWR	9/14	Elick	change the AL CAP to 2000hr	change PC380 from SF10004M08L to SF000000S8L. change PC381 from SF10004M08L to SF000000S8L. change PC382 from SF10004M08L to SF000000S8L.	0.1
2	45	PWR	9/14	DELL	change to correct parts for 15ALW	change PD55 from SCSB717F08L to SCS00001U8L. change PD56 from SCSB717F08L to SCS00001U8L.	0.1
3	48	PWR	9/14	DELL	change to PSL of DELL	change PH2 from SL20000030L to SL200000F8L	0.1
4	44	PWR	9/14	DELL	change to PSL of DELL	change PL1 from SM01001680L to SM010008U0L.	0.1
5	44	PWR	9/14	DELL	change to PSL of DELL	change PL2 from SM01001418L to SM010009C8L. change PL34 from SM01001418L to SM010009C8L.	0.1
6	46	PWR	9/14	DELL	BITS-WI89364 The 0.9V_DDR_VTT_PWRGD net is not used at the MEC5025. The 0.9V_DDR_VTT_PWRGD net should be no connect at the MEC5025 pin 73.	remove PR437, PR438, PR441, PQ93 and PQ94.	0.1
7	45	PWR	9/14	DELL	BITS-WI91011 change to correct current limits	Change PR383 from 124K(SD03412438L) to 150K(SD03415038L). Change PR382 from 187K(SD03418738L) to 226K(SD03422638L).	0.1
8	47	PWR	9/14	DELL	BITS-WI91278 following DELL rule	Depopulate PR415 and PR416 resistors.	0.1
9	49	PWR	9/14	DELL	BITS-WI91289 be compliant with the reference schematic.	Change PR274 from 4.7 ohm(SD000006T8L) to 33 ohm(SD014330A8L). Populate PR373 and PD54.	0.1
10	51	PWR	9/14	DELL	BITS-WI91295 Implement changes to 1.25V_RUN and GPU Core regulators	Add PC410 10uF, 1206, 25V at the input rail (+PWR_SRC) of the 1.25V_RUN regulator. Change PR460 from 0 ohm(SD01300008L) to 1 ohm(SD013100B8L). Change PR459 from 0 ohm (SD01300008L) to 1 ohm(SD013100B8L). Change PR449 ground connection from AGND to PGND.	0.1
11	47	PWR	9/14	DELL	BITS-WI91372 following DELL rule	Change PR408 from 75K(SD03475028L) to 82.5K(SD00000278L).	0.1
12	44	PWR	9/14	DELL	BITS-WI91682 DC IN schematic changes.	Change PL1 from SM01001680L to SM010008U0L. Change PQ100 from SI2301BDS(SB923010020) to PQ100A depopulated IMD2A(SB000009N8L). Change PQ101 from SI2301BDS(SB923010020) to PQ100B depopulated IMD2A(SB000009N8L). Change PR12 from 10K,0603(SD01310028L) to 4.7K,0805(SD00247018L).	0.1
13	45	PWR	9/14	DELL	BITS-WI90985 following DELL rule	Change PC285 pin 2 pad connection from PGND to AGND.	0.1
14	45	PWR	9/14	DELL	BITS-WI90988 Change PQ83 from FDS8880 to BSC079N03SG PPAK	Change PQ83 from SB000004U8L to SB000004D8L.	0.1
15	51	PWR	9/15	DELL	BITS-WI92173 correct the current limit on GPU CORE regulator	Change PR451 from 140K(SD03414038L) to 182K(SD03418238L)	0.1

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	51	PWR	9/15	DELL	BITS-WI92161 correct the current limit on 1.25V_RUN regulator.	Change PR453 from 140K(SD03414038L) to 205K (SD03420538L)	0.1
17	46	PWR	9/15	DELL	BITS-WI91932 correct the current limit on 1.8V output	Change PR202 from 61.9K(SD03461928L) to 100K (SD03410038L)	0.1
18	46	PWR	9/18	DELL	BITS-WI92459 follow BITS of DELL	change PR193 to be populate. change PR506 to be populate. change PR505 to be depopulate.	0.1
19	48	PWR	9/18	DELL	BITS-WI92462 improve transients at load dump. and reduce jittering.	Add depopulate PR516(SD03410018L) and depopulate PC413(SE076103K8L) between pin 9 of PU11 and AGND. Add depopulated PC411(SE075472K8L),4700pF between pin 14 of PU11 and AGND Add depopulated PC412(SE075472K8L),4700pF between pin 15 of PU11 and AGND	0.1
20	51	PWR	9/18	DELL	BITS-WI87245 PWRGD signals are reversed coming from the wrong side of the IC.	Change the node name at pin 13 of PU25 from GFX_CORE_PWRGD to 1.25V_RUN_PWRGD. Change the node name at pin 28 of PU25 from 1.25V_RUN_PWRGD to GFX_CORE_PWRGD . Remove +3.3V_RUN node connected to pin 2 of PR462. Remove +3.3V_ALW node connected to pin 1 of PR483. Remove +3.3V_ALW node connected to pin 1 of PR450. Remove totally PR462 pad, PR483, PR450.	0.1
21	51	PWR	9/20	Elick	change GPU_CORE voltage	change PR446 from 10k to 13.7k(SD03413728L)	0.1
22	44	PWR	9/21	DELL	BITS-WI91682 change PL1 from BK1608HM to BLM18BD102SN1D.	change PL1 from SM010008U0L to SM010007C8L.	0.1
23	48/50	PWR	9/21	DELL	BITS-WI87563 change populate PC380 from 25CE100AX to 25CE100LS change PC381 from 25CE100AX to 25CE100LS change PC382 from 25CE100AX to 25CE100LS	change populate PC380 from SF000000S8L to SF000000T8L. change PC381 from SF000000S8L to SF000000T8L. change PC382 from SF000000S8L to SF000000T8L.	0.1
24	49	PWR	9/29	DELL	match Maxim's response time of ICM input to comparator.	change PR361 from 0 Ohm (SD02800008L) to 8.45K (SD00000068L). change PC254 from 0.01uF 25V (SE068103K8L) to 0.1uF 16V (SE076104K8L).	0.1
25	49	PWR	9/29	DELL	ICM is voltage source and does not need this component.	depopulate PR150.	0.1
26	49	PWR	9/29	DELL	Increase BW from 20kHz to 25kHz while maintaining 80degrees phase margin.	change PR148 from 4.7K (SD03447018L) to 10K (SD03410028L).	0.1
27	49	PWR	9/29	DELL	following DELL rule	depopulate PD54 and PR373	0.1
28	48	PWR	10/27	DELL	Add bead to connect +PWR_SRC to +CPU_PWR_SRC	Add PL47(SM01002078L) to parallel PJP30.	0.2

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	45, 46, 47, 51	PWR	10/27	DELL	BITS-WI99895 This is to add an optional ultrasonic mode in case the regulators experience an audible noise.	Add PR517 0 ohm 0402(SD02800008L) between pin 29 of PU20 and AGND . Add PR519 0 ohm 0402(SD02800008L) between pin 29 of PU21 and AGND . Add PR520 0 ohm 0402(SD02800008L) between pin 29 of PU25 and AGND . Add PR518 0 ohm 0402(SD02800008L) between pin 26 of PU6 and AGND .	0.2
30	49	PWR	10/27	DELL	BITS: WI102600 Change PR148 from 10K_0402_1% to 2.2K_0402_5%	change PR148 from 10k 0402 1%(SD03410028L) to 2.2k 0402 5%(SD02822018L)	0.3
31	45	PWR	11/20	DELL	BITS-WI105406 Add node name +3.3V_ALW2 for the trace connected to the pin 5 (VREF3) of PU20. Populate PC285 with 0.1uF cap.	Add node name +3.3V_ALW2 between pin5 of PU20 and PC285. Populate PC285.	0.3
32	49	PWR	12/06	DELL	BITS-WI106278 make sure that PC113, PC114 and PC379 are X5R/X7R caps, need to stuff PC379.	change PC379 is populated.	0.3
33	48	PWR	12/06	DELL	BITS-WI108229 Change PC187 from 10nF to 15nF. Change PR258 from 2.21K to 1.69K. Populate PR516 with 1K resistor. Populate C413 with 0.01uF.	change PR187 from 10nF(SE076103K8L) to 15nF(SE076153K8L). change PR258 from 2.21K(SD03422118L) to 1.69K(SD00000JB8L). populate PC413. populate PR516.	0.3
34	51	PWR	01/04	ELICK	EMI CLK issue	Add PL3 to parallel PJP54. add PC414 to connect between GPU_CORE to GND. add PC415 to connect between GPU_CORE to GND.	0.3
35	49	PWR	01/25	ELICK	change to new part number for PSL	change PR138 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS) change PR145 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS)	0.4
36	44	PWR	01/26	ELICK	change bead to 9A 1812 in DC-IN.	change PL2 from SM010009C8L(TAIYO FBMJ4516HS720NT 1806) to SM01000BI0L(KC FBCA-K5B-302340-L1-T 1812 ). change PL32 from SM010009C8L(TAIYO FBMJ4516HS720NT 1806) to SM01000BI0L(KC FBCA-K5B-302340-L1-T 1812 ).	0.4
37	45/47/51	PWR	02/05	DELL	BITS-WI119950 Increase current limits for 3.3V, 1.5V and GPU_CORE regulators.	change PR382 from 226K to 267k (SD02822018L). Change PR408 from 82.5K to 100K(SD03410038L). Change PR451 from 182K to 205K(SD03420538L) .	0.4
38	49	PWR	02/06	DELL	additional 1206 resistor on +VCHGR for Maxim solution.	add an unpopulation PR522 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4
39	49	PWR	02/12	DELL	delete 1206 resistor on +VCHGR not to implement for Maxim solution.	delete an unpopulate PR520 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4



