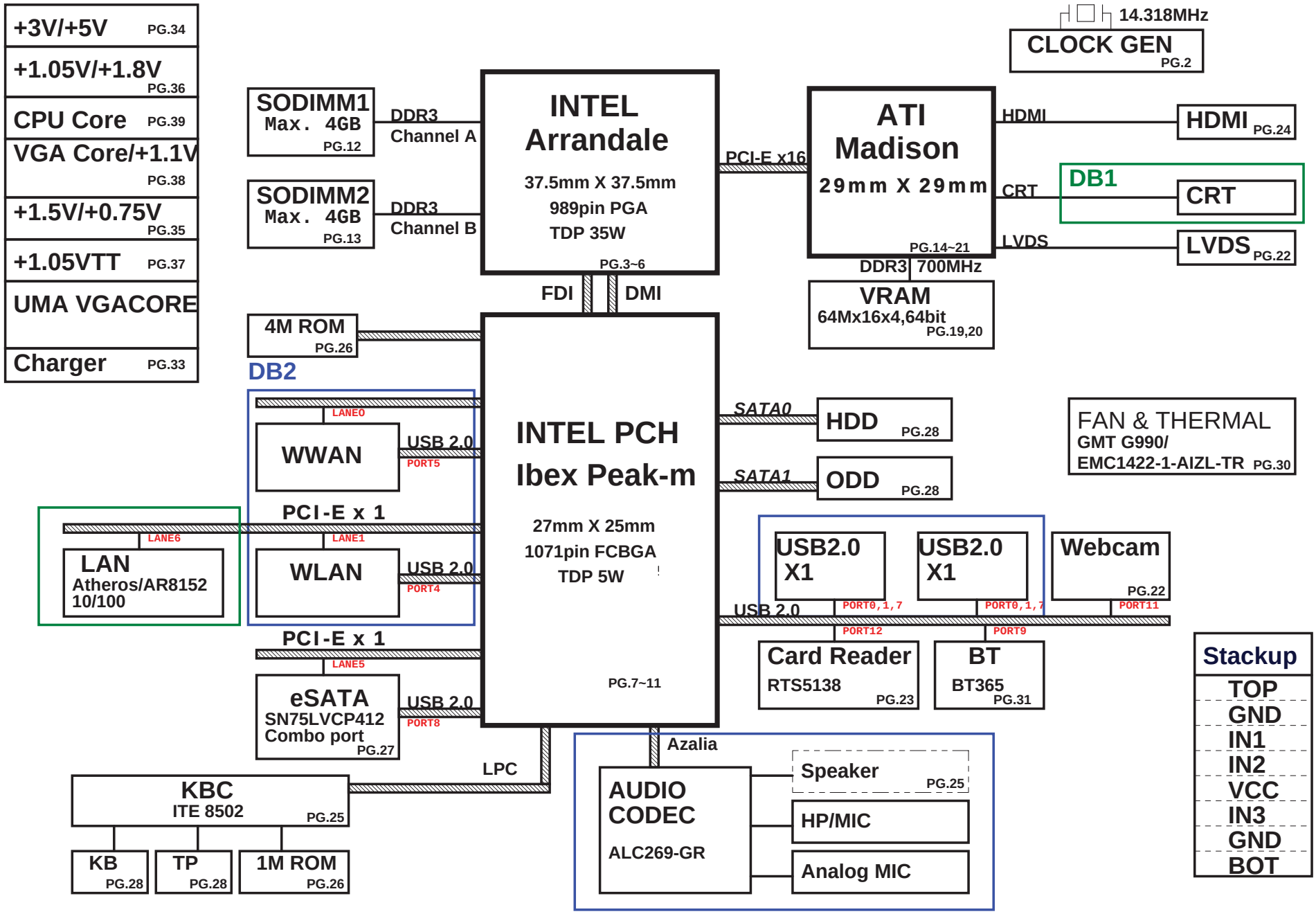
UM8B DIS SYSTEM DIAGRAM



Quanta Computer Inc.
PROJECT : UM8B DIS
Size | Document Number: BLOCK DIAGRAM | Rev 1A
Date: Wednesday, February 10, 2010 | Sheet 1 of 46

25mA

+1.05V_PCH — L25 HCB1608KF-181T15_6 — +VDDIO_CLK

C327 0.1U/ 10V/X7R
C320 0.1U/ 10V/X7R
C323 10U/6.3V 8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L27 HCB1608KF-181T15_6 — +VDDSE_CLK

C352 10U/6.3V 8/X5R
C336 0.1U/ 10V/X7R
C353 0.1U/ 10V/X7R
C354 0.1U/ 10V/X7R
C322 0.1U/ 10V/X7R
C321 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint

U10 — 9LRS3197 — QFN32

+VDDSE_CLK: VDD_LCD, VDD_REF
+VDDIO_CLK: VDD_CPU_IO, VDD_SRC_IO
VDD_USB, VDD_SRC, VDD_CPU
SDATA (18,25,30 SMBDAT2), SCLK (18,25,30 SMBCLK2)
CPU_STOP#, REF_0/CPU_SEL
CK_PWRGD/PD#_3.3
XOUT (XTAL_OUT), XIN (XTAL_IN)
VSS_SATA, VSS_USB, VSS_LCD

CPU-0 / CPU-0# → CLK_BUF_BCLKP_R / CLK_BUF_BCLKN_R → RP5 0X2 → CLK_BUF_BCLKP 8 / CLK_BUF_BCLKN 8
CPU-1 / CPU-1#
DOT96T_LPR / DOT96C_LPR → CLK_BUF_DREFCLKP_R / CLK_BUF_DREFCLKN_R → RP8 0X2 → CLK_BUF_DREFCLKP 8 / CLK_BUF_DREFCLKN 8
SRC-1 / SRC-1# → CLK_BUF_PCIE_3GPLLP_R / CLK_BUF_PCIE_3GPLLN_R → RP6 0X2 → CLK_BUF_PCIE_3GPLLP 8 / CLK_BUF_PCIE_3GPLLN 8
SATA / SATA# → CLK_BUF_DREFSSCLKP_R / CLK_BUF_DREFSSCLKN_R → RP7 0X2 → CLK_BUF_DREFSSCLKP 8 / CLK_BUF_DREFSSCLKN 8
27MHz_nonSS / 27MHz_SS → CLK_VGA_27M_NOSS / CLK_VGA_27M_SS → R217 33/J_4, R216 *33/J_4_NC → EVGA-XTALI 15 / CLK_27M_SS 15
GND, VSS_REF, VSS_CPU, VSS_SRC

Place within 0.5" of C/G

Discrete only

+3.3V_RUN — R196 10K — R213 33/J_4 — CPU_SEL
8 CLK_PCH_14M — CLK_PCH_14M — C338 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

CK_PWRGD_R

XTAL_OUT / XTAL_IN

C351 *10P/50V_4_NC/COG

+3.3V_RUN — R212 *10K_NC — CPU_SEL — R209 10K

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

BOM check

+3.3V_RUN — R199 1K/J_4 — CK_PWRGD_R

39 VR_PWRGD_CLKEN# — Q13 FDN357N — R201 *100K/F_4_NC

Y1 14.318MHZ
XTAL_IN — C330 33P/50V_4/NPO
XTAL_OUT — C328 33P/50V_4/NPO

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

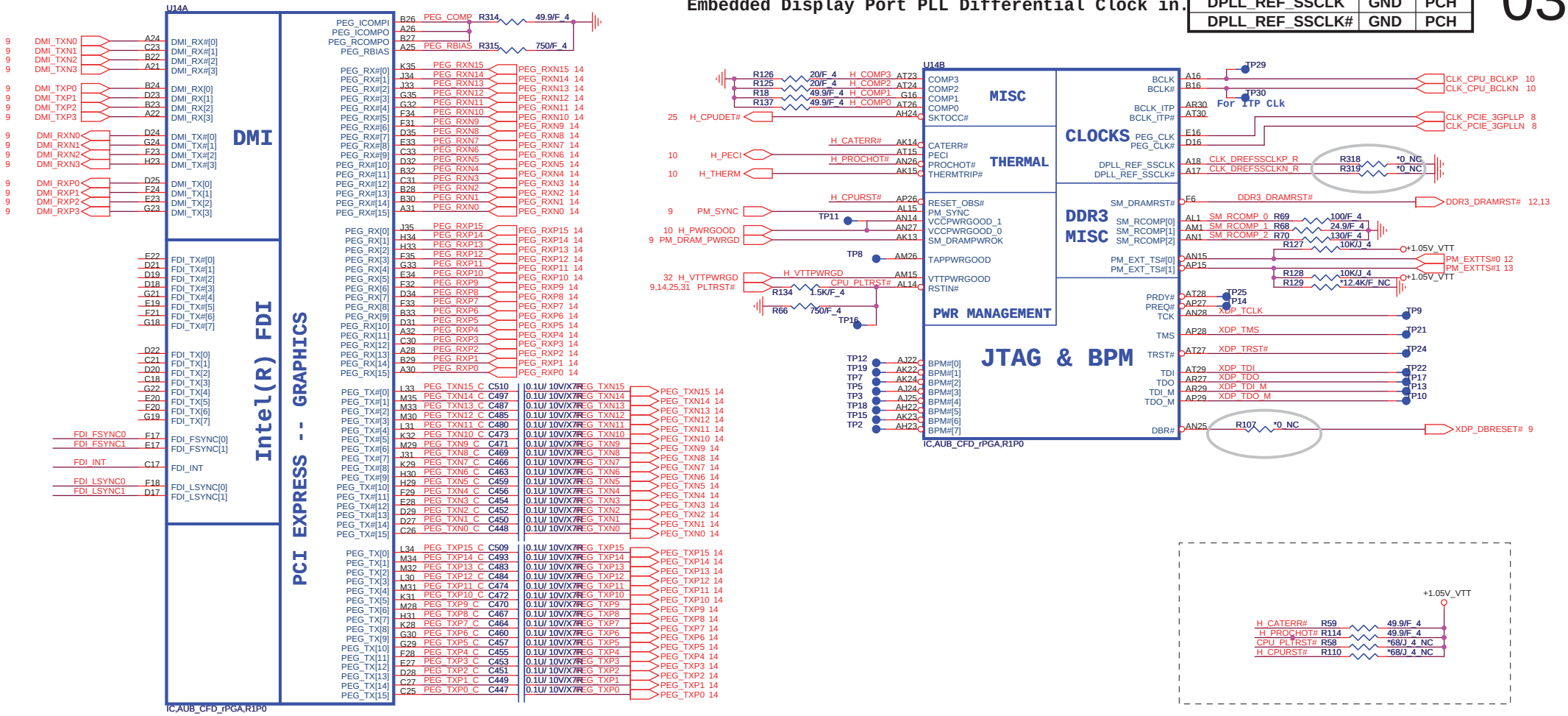
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	1A
Date: Wednesday, February 10, 2010	Sheet 2 of 46	

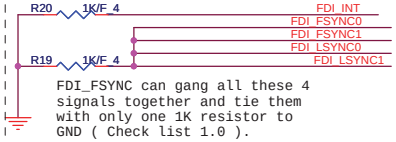
DPLL_REF_SSCLK/DPLL_REF_SSCLK#:
Embedded Display Port PLL Differential Clock in.

	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03



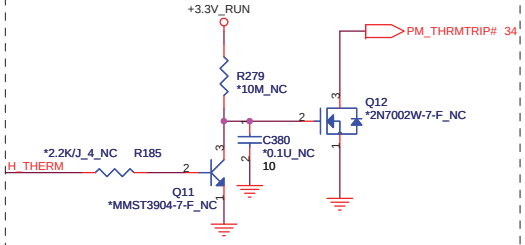
Discrete Only

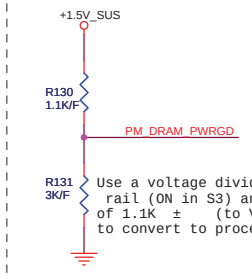


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1],FDI_LSYN[0],FDI_LSYN[1] can be ganged together with one resistor.

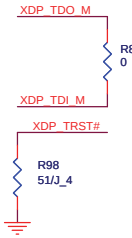
CPU THERMTRIP





Use a voltage divider with VDDQ (1.5 V) rail (ON in S3) and resistor combination of 1.1K ± (to VDDQ)/3K ± (to GND) to convert to processor VTT level.

JTAG MAPPING



Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins. (DS 403777 Page 81)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A

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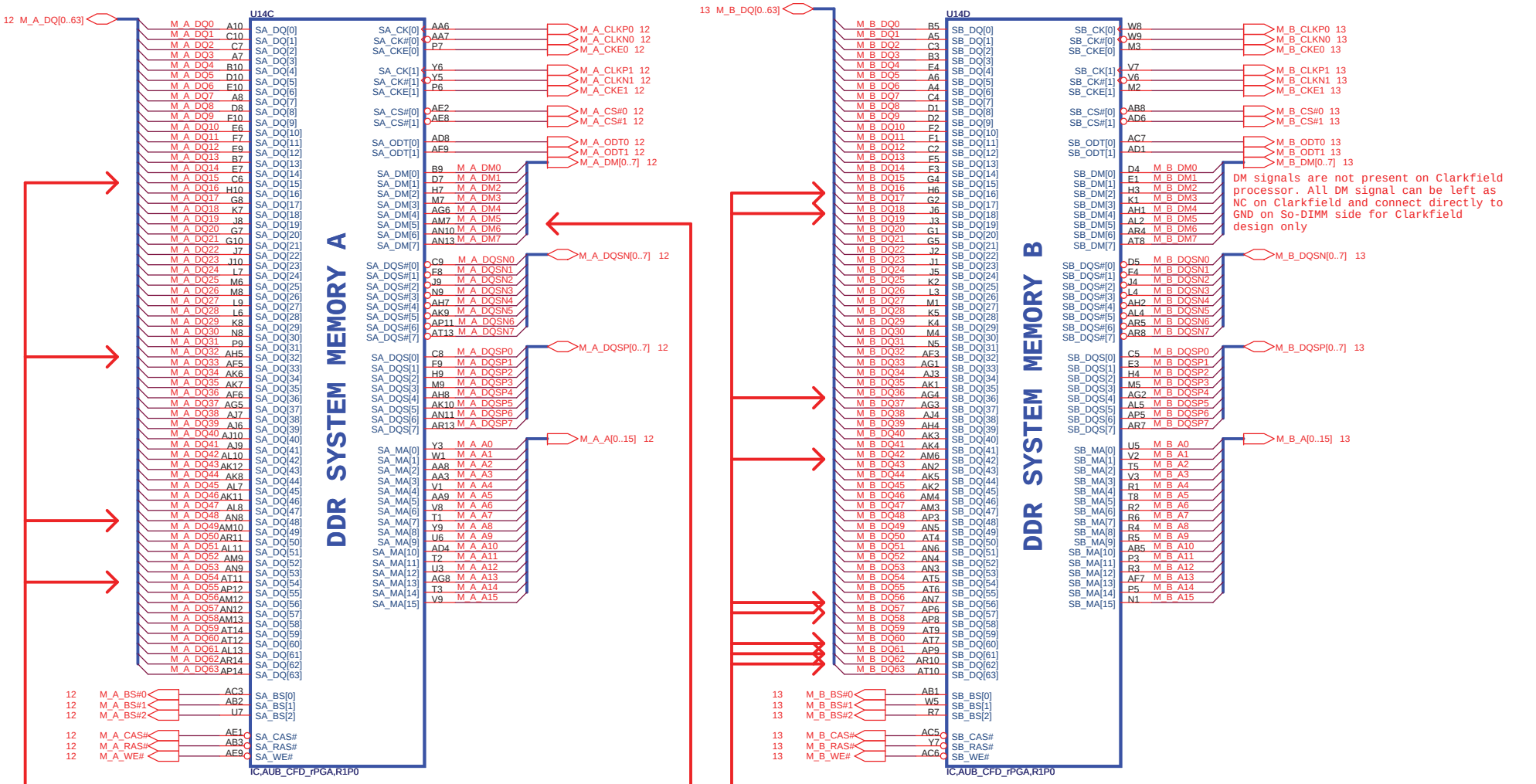
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A
Date: Wednesday, February 10, 2010	Sheet 4 of 46	

Name different with power

+VCC_CORE

C491 *22U/6.3V_8/X5R_NC
C490 *22U/6.3V_8/X5R_NC
C92 *22U/6.3V_8/X5R_NC
C70 *22U/6.3V_8/X5R_NC
C521 *22U/6.3V_8/X5R_NC
C125 22U/6.3V_8/X5R
C103 22U/6.3V_8/X5R
C121 22U/6.3V_8/X5R
C126 22U/6.3V_8/X5R
C77 22U/6.3V_8/X5R
C124 22U/6.3V_8/X5R
C129 22U/6.3V_8/X5R
C78 10U/6.3V_8/X5R
C488 10U/6.3V_8/X5R
C505 10U/6.3V_8/X5R
C445 10U/6.3V_8/X5R
C520 10U/6.3V_8/X5R
C60 10U/6.3V_8/X5R
C516 10U/6.3V_8/X5R
C122 10U/6.3V_8/X5R
C515 *10U/6.3V_8/X5R_NC
C489 *10U/6.3V_8/X5R_NC
C120 10U/6.3V_8/X5R
C117 10U/6.3V_8/X5R
C522 *10U/6.3V_8/X5R_NC
C518 *10U/6.3V_8/X5R_NC
C108 *10U/6.3V_8/X5R_NC
C123 *10U/6.3V_8/X5R_NC

C446 *470U_NC/
C18 *470U_NC

U14F

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AE35 AE34 AE33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

IC,AUB_CFD_rPGA,R1P0

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

18A

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.05V_VTT

C519 10U/6.3V_8/X5R
C503 10U/6.3V_8/X5R
C478 10U/6.3V_8/X5R
C73 10U/6.3V_8/X5R
C46 *10U/6.3V_0805/X5R_NC
C481 *10U/6.3V_0805/X5R_NC
C47 *10U/6.3V_0805/X5R_NC
C119 *10U/6.3V_0805/X5R_NC
C114 *10U/6.3V_0805/X5R_NC
C524 22U/6.3V_8/X5R
C48 22U/6.3V_8/X5R
C514 *22U/6.3V_8/X5R_NC

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C43 22U/6.3V_8/X5R
C84 22U/6.3V_8/X5R

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# AN33 H_PSI# 39

VID[0] AK35 VID0 39
VID[1] AK33 VID1 39
VID[2] AK34 VID2 39
VID[3] AL35 VID3 39
VID[4] AL33 VID4 39
VID[5] AM33 VID5 39
VID[6] AM35 VID6 39
PROC_DPRSLPVR AM34 DPRSLPVR 39

VTT_SELECT G15 TP1

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

SENSE LINES

ISENSE AN35 I_MON 39

VTT_SENSE B15 VTT_SENSE 37
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT T34

VCC_SENSE AJ34 VCCSENSE 39
VSS_SENSE AJ35 VSSSENSE 39

+VCC_CORE
R64 100/F
R61 100/F/

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options
in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors
will depend on the POC configuration of AUB
and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

U14G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

GRAPHICS

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDs

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

Pop it when Arrandale Graphics disable.

R118 1K/J_4

POWER

DDR3 - 1.5V RAILS

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_SUS

C44 1U/6.3V/X5R
C90 1U/6.3V/X5R
C116 1U/6.3V/X5R
C53 1U/6.3V/X5R
C38 1U/6.3V/X5R
C55 22U/6.3V_8/X5R
C61 *22U/6.3V_8/X5R_NC
C20 330U/2V_7343

FDI

+1.05V_VTT

C49 22U/6.3V_8/X5R
C475 *22U/6.3V_8/X5R_NC

VTT1_45 VTT1_46 VTT1_47

J24 J23 H25

PEG & DMI

+1.05V_VTT

C56 22U/6.3V_8/X5R
C62 22U/6.3V_8/X5R
C98 *22U/6.3V_8/X5R_NC
C37 *22U/6.3V_8/X5R_NC

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

+1.05V_VTT

C486 10U/6.3V_8/X5R
C495 *10U/6.3V_0805/X5R_NC
C476 22U/6.3V_8/X5R
C477 *22U/6.3V_8/X5R_NC

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C45 22U/6.3V_8/X5R
C34 4.7U/6.3V/X5R
C42 2.2U/ 6.3V/X5R
C36 1U/6.3V/X5R
C479 1U/6.3V/X5R

IC,AUB_CFD_rPGA,R1P0

VID0 R96 1K/J_4 R313 *1K/J_4_NC
VID1 R84 1K/J_4 R312 *1K/J_4_NC
VID2 R104 1K/J_4 R311 *1K/J_4_NC
VID3 R111 1K/J_4 R310 *1K/J_4_NC
VID4 R115 1K/J_4 R309 *1K/J_4_NC
VID5 R148 1K/J_4 R308 *1K/J_4_NC
VID6 R124 1K/J_4 R307 *1K/J_4_NC
DPRSLPVR R139 1K/J_4 R306 *1K/J_4_NC
H_PSI# R140 1K/J_4 R305 *1K/J_4_NC

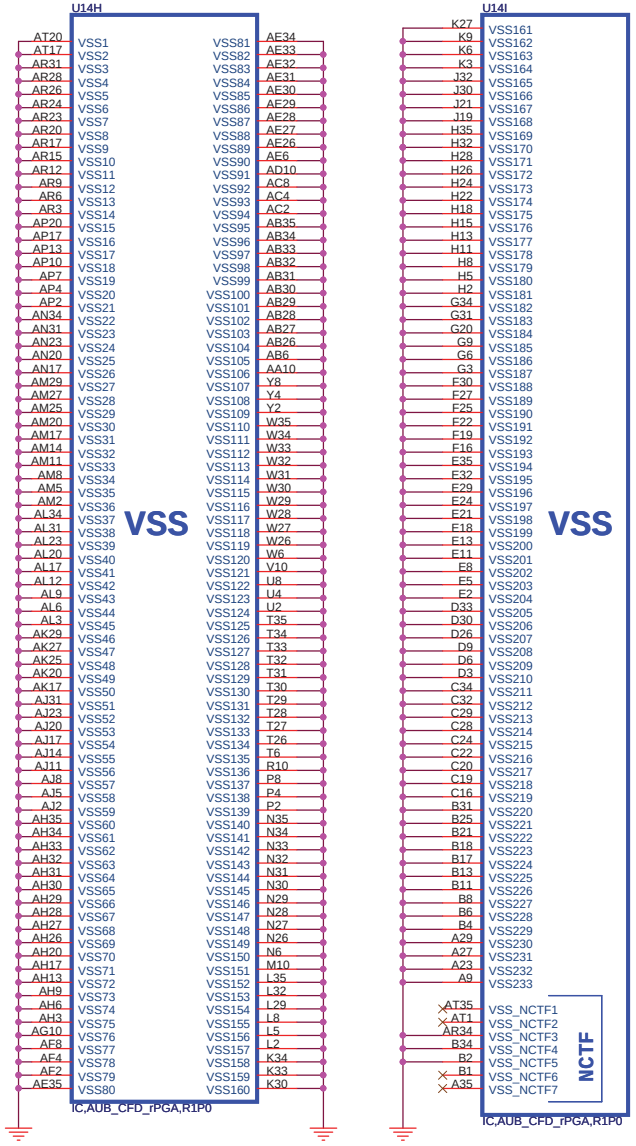
+1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM8B DIS

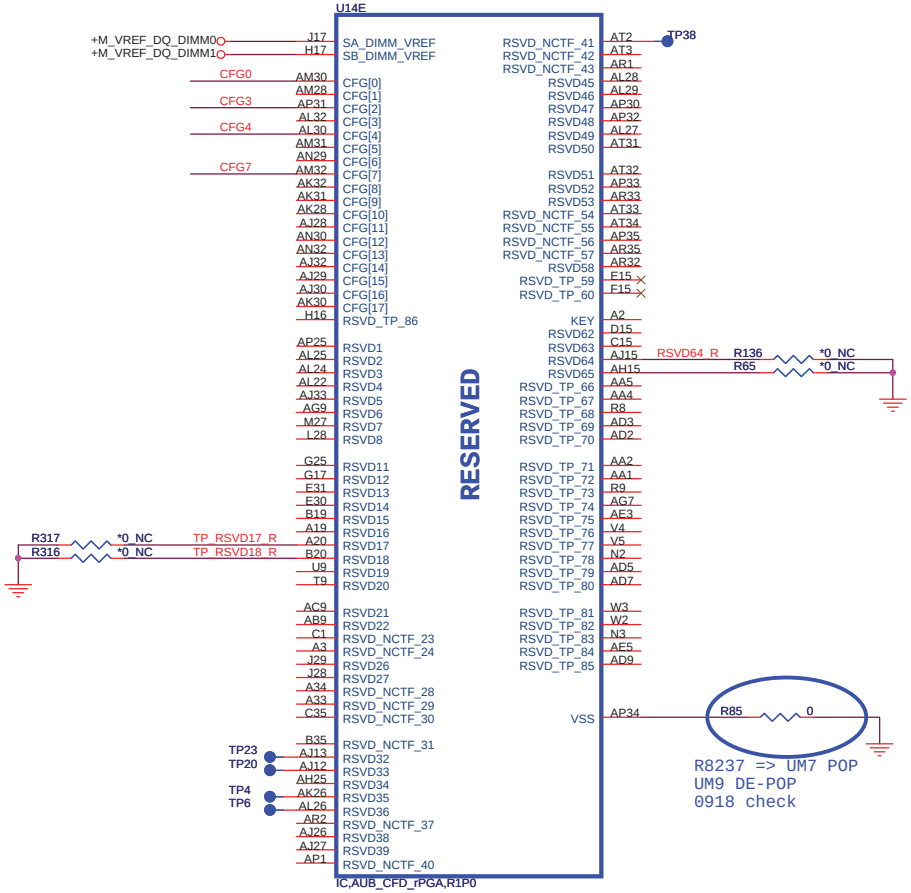
Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A
Date: Wednesday, February 10, 2010	Sheet 5 of 46	

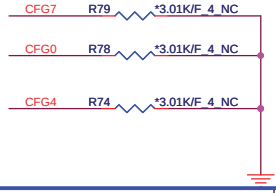
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



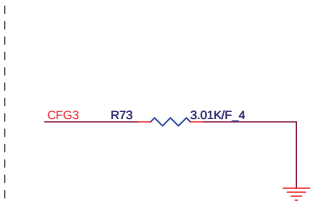
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Wednesday, February 10, 2010 Sheet 6 of 46

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U21A

Ibex-M 1 OF 10

RTC
LPC
IHDA
JTAG
SPI
SATA

HDD
ODD
ESATA

DG: Place TX cap close to connector
SATA port 2/3 are not support in HM55 .
They are only in PM 55

must add test point.

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

ibexPeak-M_Rev1_0

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

iTPM ENABLE/DISABLE

TPM Function	
Enable	Mount
Disable	NC (Default)

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U21D

Ibex-M 4 OF 10

SDVO
LVDS--A
LVDS--B
CRT
Digital Display Interface
DISPLAY PORT B
DISPLAY PORT C
DISPLAY PORT D

UMA 0.5%
DIS 1%

ibexPeak-M_Rev1_0

Res. of TDI near PCH

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For AUDIO

RTC

1mA

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

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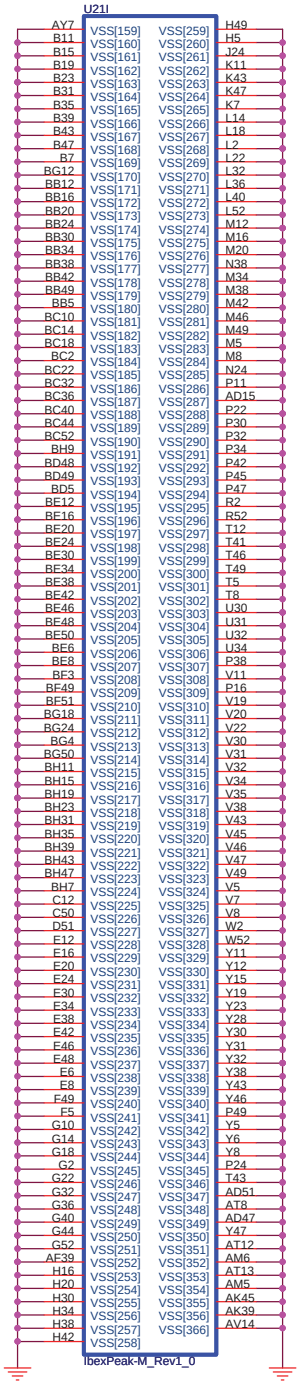
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

08

U21B

Ibex-M 2 OF 10

PCI-E*

[WLAN] 31 PCIE_RXN1 31 PCIE_RXP1 31 PCIE_TXN1 31 PCIE_TXP1 C348 0.1U/ 10V/X7R C349 0.1U/ 10V/X7R PCIE_TXN1_C PCIE_TXP1_C

[LAN] 31 PCIE_RXN6_LAN 31 PCIE_RXP6_LAN 31 PCIE_TXN6_LAN 31 PCIE_TXP6_LAN C334 0.1U/ 10V/X7R C333 0.1U/ 10V/X7R PCIE_TXN6_LAN_C PCIE_TXP6_LAN_C

MiniWLAN 31 CLK_PCIE_WLANN 31 CLK_PCIE_WLANP 31 PCIE_CLK_REQ1#

LAN 31 CLK_PCIE_LANN 31 CLK_PCIE_LANP 31 PCIE_CLK_REQB#_R

SMBus (+3V_S5)
SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

+3.3V_SUS
B9 SMBALERT# 10K/J_4 R438
H14 ICH_SMBCLK 2.2K/J_4 R282
C8 ICH_SMBDATA 2.2K/J_4 R281
J14 SMBL0ALERT# 10K/J_4 R262
C6 SMB_CLK_ME0 2.2K/J_4 R433
G8 SMB_DATA_ME0 2.2K/J_4 R256
M14 SML1ALERT# 10K/J_4 R263
E10 SMB_CLK_ME1 2.2K/J_4 R272
G12 SMB_DATA_ME1 2.2K/J_4 R271

SMB1 Check R value...
(R8283, R8296)

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9
ICH_SMBCLK ICH_SMBCLK 31
ICH_SMBDATA ICH_SMBDATA 31

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
H1 PEG_CLKREQ#
AD43 CLK_PCIE_VGAN 14
AD45 CLK_PCIE_VGAP 14
AN4 CLK_PCIE_3GPLLN 3
AN2 CLK_PCIE_3GPLLP 3

From CLK BUFFER
CLKOUT_DP_N / CLKOUT_BCLK1_N AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3
CLKIN_DMI_N AW24 CLK_BUF_PCIE_3GPLLN 2
CLKIN_DMI_P BA24 CLK_BUF_PCIE_3GPLLP 2
CLKIN_BCLK_N AP3 CLK_BUF_BCLKN 2
CLKIN_BCLK_P AP1 CLK_BUF_BCLKP 2
CLKIN_DOT_96N F18 CLK_BUF_DREFCLKN 2
CLKIN_DOT_96P E18 CLK_BUF_DREFCLKP 2
CLKIN_SATA_N / CKSSCD_N AH13 CLK_BUF_DREFSSCLKN 2
CLKIN_SATA_P / CKSSCD_P AH12 CLK_BUF_DREFSSCLKP 2
REFCLK14IN P41 CLK_PCH_14M 2
CLKIN_PCILOOPBACK J42 CLK_PCI_FB
C384 *5.6P/50V_4_NC/COG
CLK_PCI_FB 9
T33
Intel recommendation
XTAL25_IN AH51
XTAL25_OUT AH53
R227 *0_NC
T56 short0402
67
XCLK_RCOMP AF38
R219 90.9/F_4
+1.05V_PCH

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64 T45 CLK_FLEX0 T30
(+3V) CLKOUTFLEX1 / GPIO65 P43 CLK_FLEX1 T32
(+3V) CLKOUTFLEX2 / GPIO66 T42 CLK_FLEX2 T31
(+3V) CLKOUTFLEX3 / GPIO67 N50 CLK_FLEX3
R243 22/J_4
CLK_48M_CARD 23
77
R8236 => UM7 POP 33ohm
UM9 POP 22ohm
0918 check
C419 10P/50V/COG

PCI-E*
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8
CLKOUT_PCIE0N CLKOUT_PCIE0P
PCIECLKRQ0# / GPIO73 (+3V_S5)
CLKOUT_PCIE1N CLKOUT_PCIE1P
PCIECLKRQ1# / GPIO18 (+3V)
CLKOUT_PCIE2N CLKOUT_PCIE2P
PCIECLKRQ2# / GPIO20 (+3V)
CLKOUT_PCIE3N CLKOUT_PCIE3P
PCIECLKRQ3# / GPIO25 (+3V_S5)
CLKOUT_PCIE4N CLKOUT_PCIE4P
PCIECLKRQ4# / GPIO26 (+3V_S5)
CLKOUT_PCIE5N CLKOUT_PCIE5P
PCIECLKRQ5# / GPIO44 (+3V_S5)
CLKOUT_PEG_B_N CLKOUT_PEG_B_P
PEG_B_CLKRQ# / GPIO56 (+3V_S5)

IbexPeak-M_Rev1_0

66

PCIE Clock Request

+3.3V_RUN
PCIE_CLK_REQ1# R406 10K/J_4
PCIE_CLK_REQ2# R413 10K/J_4

+3.3V_SUS
PCIE_CLK_REQ0# R239 10K/J_4
PCIE_CLK_REQ3# R434 10K/J_4
PCIE_CLK_REQ4# R249 10K/J_4
PCIE_CLK_REQB#_R R265 10K/J_4
PCIE_CLK_REQ5# R253 10K/J_4

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S (DS 401376 Table2-26)

PEG_CLKREQ# R435 10K/J_4

LOW acvite on GPIO47 for GFX CLK output

Q15 FDN357N
SMB_CLK_ME1 1 3 SMBCLK1 25
+3.3V_SUS
SMB_DATA_ME1 1 3 SMBDAT1 25
Q14 FDN357N

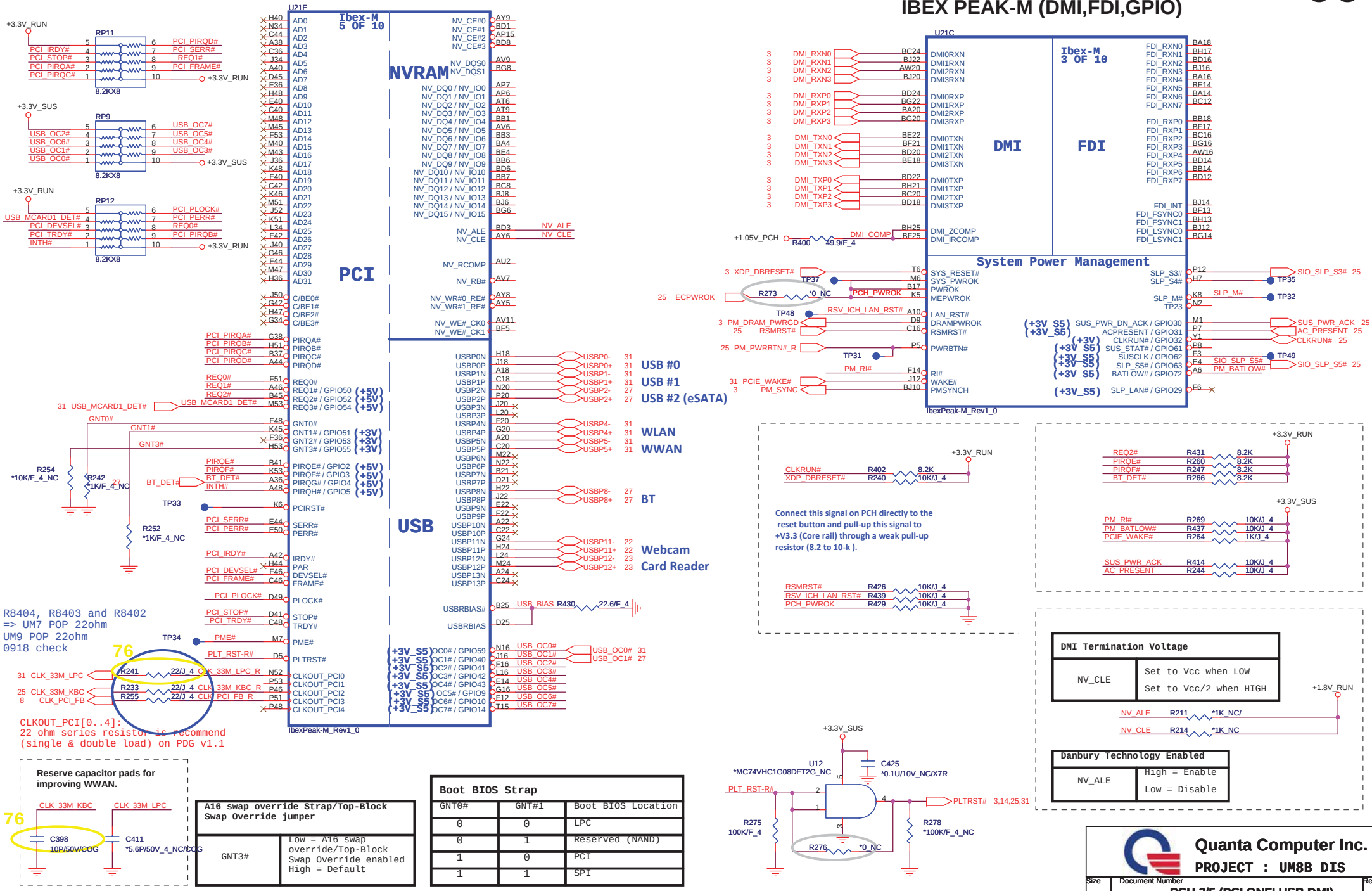
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	1A
Date: Wednesday, February 10, 2010	Sheet 8 of 46	

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

09



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

U21F — Ibex-M 6 OF 10

GPIO MISC

PCH_GPIO0 — Y3 — BMBUSY# / GPIO0 (+3V)
25 SIO_EXT_SMI# — C38 — TACH1 / GPIO1 (+3V)
25 SIO_EXT_SCI# — D37 — TACH2 / GPIO6 (+3V)
25 SIO_EXT_WAKE# — J32 — TACH3 / GPIO7 (+3V)
TP36 — PCH_GPIO8 — F10 — GPIO8 (+3V_S5)
LAN_PHY_PWR_CTRL — K9 — LAN_PHY_PWR_CTRL / GPIO12 (+3V_S5)
T7 — GPIO15 (+3V_S5)
SATA4GP — AA2 — SATA4GP / GPIO16 (+3V)
31 PCIE_MCARD1_DET# — R251 *0_NC — PCIE_MCARD1_DET#_R — F38 — TACH0 / GPIO17 (+3V)
PCIE_MCARD2_DET# — Y7 — SCLOCK / GPIO22 (+3V)
GPIO27 reserve for internal VR. — R224 *10K_NC — GPIO27 — AB12 — GPIO27 (+3V_S5)
TP_PCH_GPIO28 — V13 — GPIO28 (+3V_S5)
SATA2GP — AB7 — SATA2GP / GPIO36 (+3V)
SATA3GP — AB13 — SATA3GP / GPIO37 (+3V)
27 BT_RADIO_DIS# — BT_RADIO_DIS# — P3 — SDATAOUT0 / GPIO39 (+3V)
GPIO46 — F1 — PCIECLKRQ7# / GPIO46 (+3V_S5)
31 WWAN_RADIO_DIS# — WWAN_RADIO_DIS# — AB6 — SDATAOUT1 / GPIO48 (+3V)
25 CRIT_TEMP_REP# — CRIT_TEMP_REP# — AA4 — SATA5GP / GPIO49 (+3V)

GPIO24 register not cleared by CF9h reset event.

H10 — GPIO24 (+3V_S5)
GPIO45 — H3 — PCIECLKRQ6# / GPIO45 (+3V_S5)
VGA_TYPE — F8 — GPIO57 (+3V_S5)
31 USB_MCARD2_DET# — USB_MCARD2_DET# — M11 — STP_PCI# / GPIO34 (+3V)
GPIO35 — V6 — SATACLKREQ# / GPIO35 (+3V)
31 WLAN_RADIO_DIS# — WLAN_RADIO_DIS# — V3 — SLOAD / GPIO38 (+3V)

CPU

CLKOUT_PCIE6N — AH45
CLKOUT_PCIE6P — AH46
CLKOUT_PCIE7N — AF48
CLKOUT_PCIE7P — AF47
A20GATE — U2 — GATEA20 25
CLKOUT_BCLK0_N/CLKOUT_PCIE8N — AM3 — CLK_CPU_BCLKN 3
CLKOUT_BCLK0_P/CLKOUT_PCIE8P — AM1 — CLK_CPU_BCLKP 3
PECI — BG10 — PCH_PECI_R — H_PECI 3
RCIN# — T1 — RCIN# 25
PROCPWRGD — BE10 — H_PWRGOOD 3
THRMTRIP# — BD10 — PCH_THRMTRIP#_R — R210 56/F — H_THERM 3
+1.05V_VTT — R215 56/F

RSVD

TP1 — BA22
TP2 — AW22
TP3 — BB22
TP4 — AY45
TP5 — AY46
TP6 — AV43
TP7 — AV45
TP8 — AF13
TP9 — M18
TP10 — N18
TP11 — AJ24
TP12 — AK41
TP13 — AK42
TP14 — M32
TP15 — N32
TP16 — M30
TP17 — N30
TP18 — H12
TP19 — AA23
NC_1 — AB45
NC_2 — AB38
NC_3 — AB42
NC_4 — AB41
NC_5 — T39
INIT3_3V# — P6
TP24 — C10

NCTF

VSS_NCTF_1 — A4
VSS_NCTF_2 — A49
VSS_NCTF_3 — A5
VSS_NCTF_4 — A50
VSS_NCTF_5 — A52
VSS_NCTF_6 — A53
VSS_NCTF_7 — B2
VSS_NCTF_8 — B4
VSS_NCTF_9 — B52
VSS_NCTF_10 — B53
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE53
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF53
VSS_NCTF_15 — BH1
VSS_NCTF_16 — BH2
VSS_NCTF_17 — BH52
VSS_NCTF_18 — BH53
VSS_NCTF_19 — BJ1
VSS_NCTF_20 — BJ2
VSS_NCTF_21 — BJ4
VSS_NCTF_22 — BJ49
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ50
VSS_NCTF_25 — BJ52
VSS_NCTF_26 — BJ53
VSS_NCTF_27 — D1
VSS_NCTF_28 — D2
VSS_NCTF_29 — D53
VSS_NCTF_30 — E1
VSS_NCTF_31 — E53

IbexPeak-M_Rev1_0

0821 UM8-0821_2.DSN

U21H

VSS[0] AB16, VSS[1] AA19, VSS[2] AA20, VSS[3] AA22, VSS[4] AM19, VSS[5] AA24, VSS[6] AA26, VSS[7] AA28, VSS[8] AA30, VSS[9] AA31, VSS[10] AA32, VSS[11] AB11, VSS[12] AB15, VSS[13] AB23, VSS[14] AB30, VSS[15] AB31, VSS[16] AB32, VSS[17] AB39, VSS[18] AB43, VSS[19] AB47, VSS[20] AB5, VSS[21] AB8, VSS[22] AC2, VSS[23] AC52, VSS[24] AD11, VSS[25] AD12, VSS[26] AD16, VSS[27] AD23, VSS[28] AD30, VSS[29] AD31, VSS[30] AD32, VSS[31] AD34, VSS[32] AU22, VSS[33] AD42, VSS[34] AD46, VSS[35] AD49, VSS[36] AD7, VSS[37] AE2, VSS[38] AE4, VSS[39] AF12, VSS[40] Y13, VSS[41] AH49, VSS[42] AU4, VSS[43] AF35, VSS[44] AP13, VSS[45] AN34, VSS[46] AF45, VSS[47] AF46, VSS[48] AF49, VSS[49] AF5, VSS[50] AF8, VSS[51] AG2, VSS[52] AG52, VSS[53] AH11, VSS[54] AH15, VSS[55] AH16, VSS[56] AH24, VSS[57] AH32, VSS[58] AV18, VSS[59] AH43, VSS[60] AH47, VSS[61] AH7, VSS[62] AJ19, VSS[63] AJ2, VSS[64] AJ20, VSS[65] AJ22, VSS[66] AJ23, VSS[67] AJ26, VSS[68] AJ28, VSS[69] AJ32, VSS[70] AJ34, VSS[71] AT5, VSS[72] AJ4, VSS[73] AK12, VSS[74] AM41, VSS[75] AN19, VSS[76] AK26, VSS[77] AK22, VSS[78] AK23, VSS[79] AK28

VSS[80] AK30, VSS[81] AK31, VSS[82] AK32, VSS[83] AK34, VSS[84] AK35, VSS[85] AK38, VSS[86] AK43, VSS[87] AK46, VSS[88] AK49, VSS[89] AK5, VSS[90] AK8, VSS[91] AL2, VSS[92] AL52, VSS[93] AM11, VSS[94] BB44, VSS[95] AD24, VSS[96] AM20, VSS[97] AM22, VSS[98] AM24, VSS[99] AM26, VSS[100] AM28, VSS[101] BA42, VSS[102] AM30, VSS[103] AM31, VSS[104] AM32, VSS[105] AM34, VSS[106] AM35, VSS[107] AM38, VSS[108] AM39, VSS[109] AM42, VSS[110] AU20, VSS[111] AM46, VSS[112] AV22, VSS[113] AM49, VSS[114] AM7, VSS[115] AA50, VSS[116] BB10, VSS[117] AN32, VSS[118] AN50, VSS[119] AN52, VSS[120] AP12, VSS[121] AP42, VSS[122] AP46, VSS[123] AP49, VSS[124] AP5, VSS[125] AP8, VSS[126] AR2, VSS[127] AR52, VSS[128] AT11, VSS[129] BA12, VSS[130] AH48, VSS[131] AT32, VSS[132] AT36, VSS[133] AT41, VSS[134] AT47, VSS[135] AT7, VSS[136] AV12, VSS[137] AV16, VSS[138] AV20, VSS[139] AV24, VSS[140] AV30, VSS[141] AV34, VSS[142] AV38, VSS[143] AV42, VSS[144] AV46, VSS[145] AV49, VSS[146] AV5, VSS[147] AV8, VSS[148] AW14, VSS[149] AW18, VSS[150] AW2, VSS[151] BF9, VSS[152] AW32, VSS[153] AW36, VSS[154] AW40, VSS[155] AW52, VSS[156] AY11, VSS[157] AY43, VSS[158] AY47

IbexPeak-M_Rev1_0

VGA Strap

+3.3V_SUS
Park 1G — R261 *10K/F_4_NC
VGA_TYPE
Park — R267 10K/F_4

R230 10K GPIO35

+3.3V_SUS
TP_PCH_GPIO28 R232 10K
GPIO46 R432 10K
GPIO45 R436 10K
LAN_PHY_PWR_CTRL R259 *10K_NC

+3.3V_RUN
RCIN# R409 10K
GATEA20 R408 10K
BT_RADIO_DIS# R410 10K
SATA2GP R223 10K
SATA3GP R222 10K
SATA4GP R401 10K
PCIE_MCARD1_DET#_R R248 10K
PCIE_MCARD2_DET# R238 10K
SIO_EXT_SMI# R270 10K
SIO_EXT_SCI# R274 10K
SIO_EXT_WAKE# R246 10K
WLAN_RADIO_DIS# R403 10K
CRIT_TEMP_REP# R228 10K
USB_MCARD2_DET# R250 10K

+3.3V_RUN
PCH_GPIO0 R404 10K
WWAN_RADIO_DIS# R220 10K

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

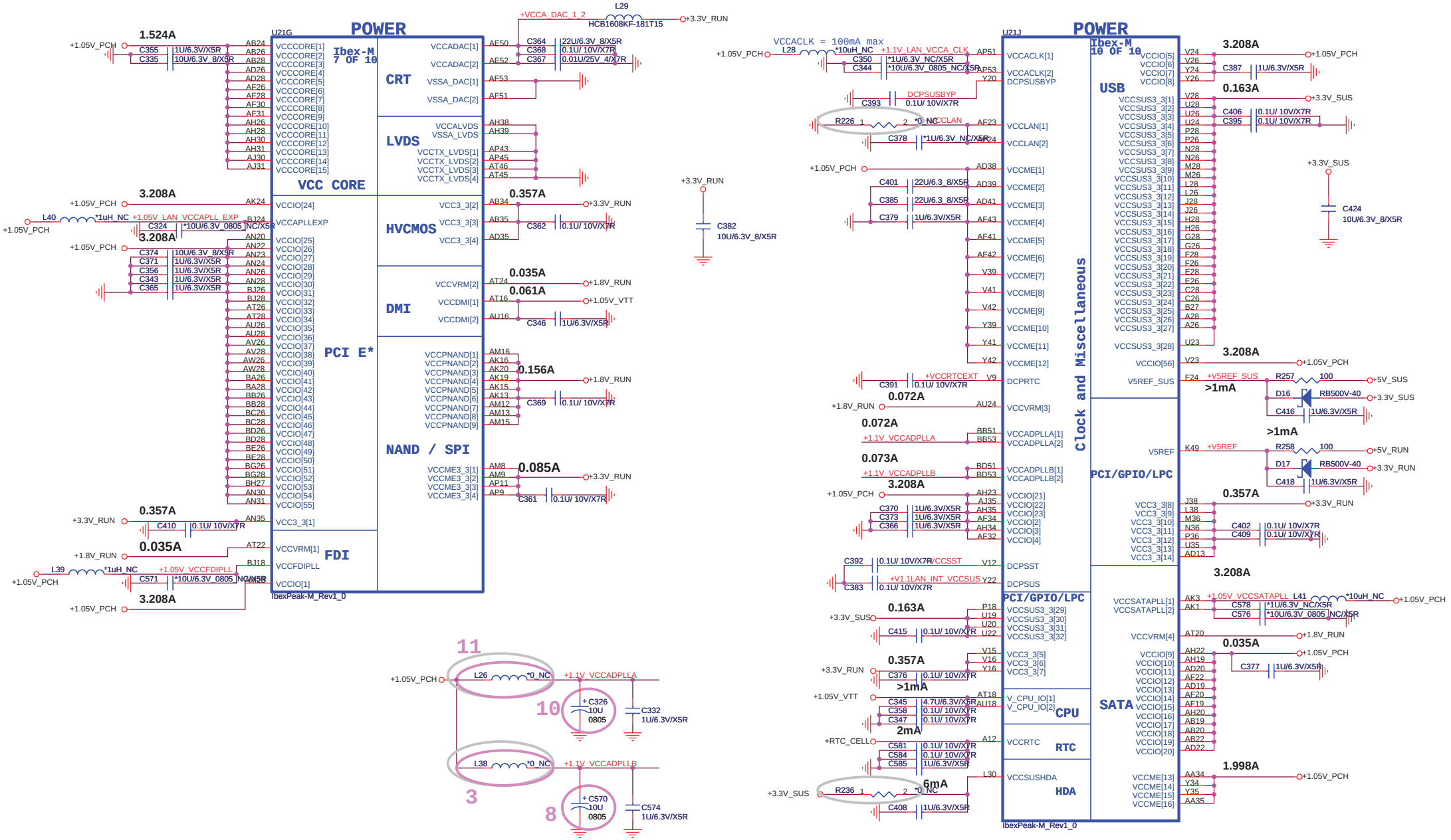
BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

WWAN_RADIO_DIS#	1-X High = Strong (Default)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
Date: Wednesday, February 10, 2010	Sheet 10 of 46	

Cap quantities follow UM3



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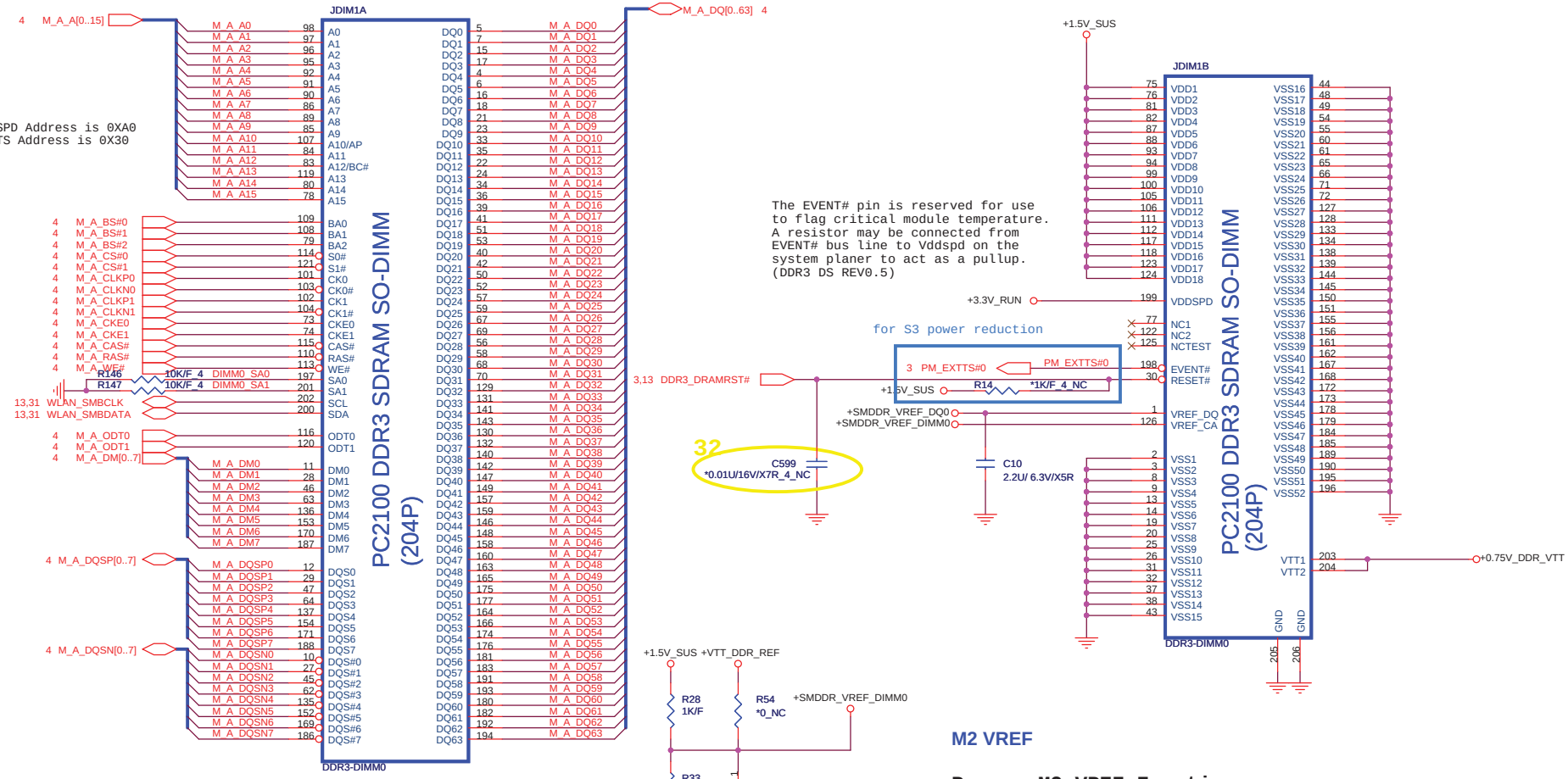
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 5/5 (POWER)	1A
Date: Wednesday, February 10, 2010	Sheet 11 of 46	



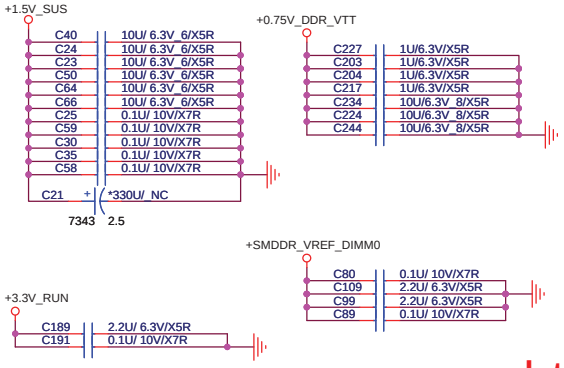
M2 VREF

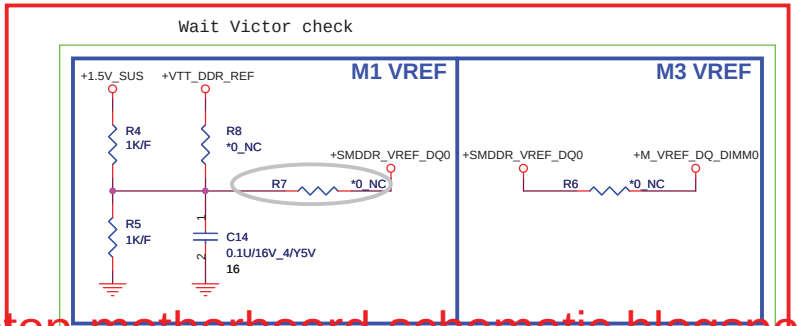
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





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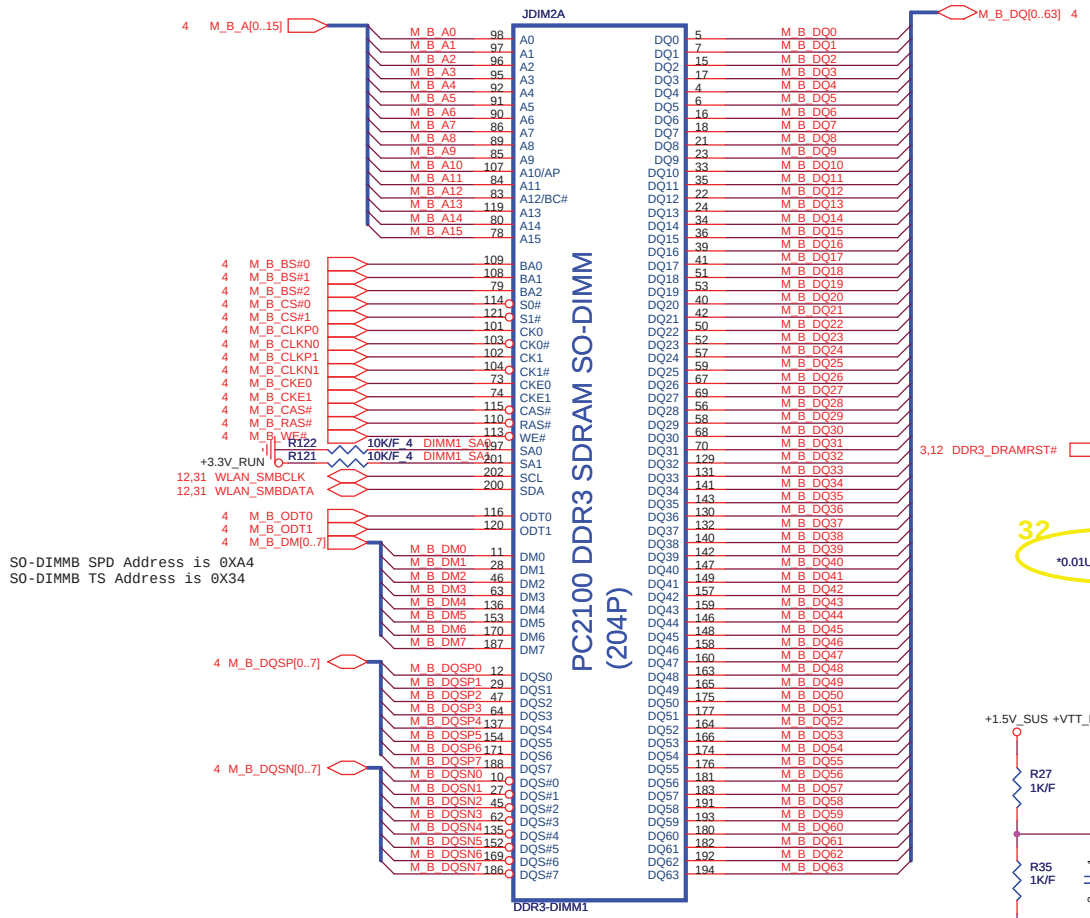
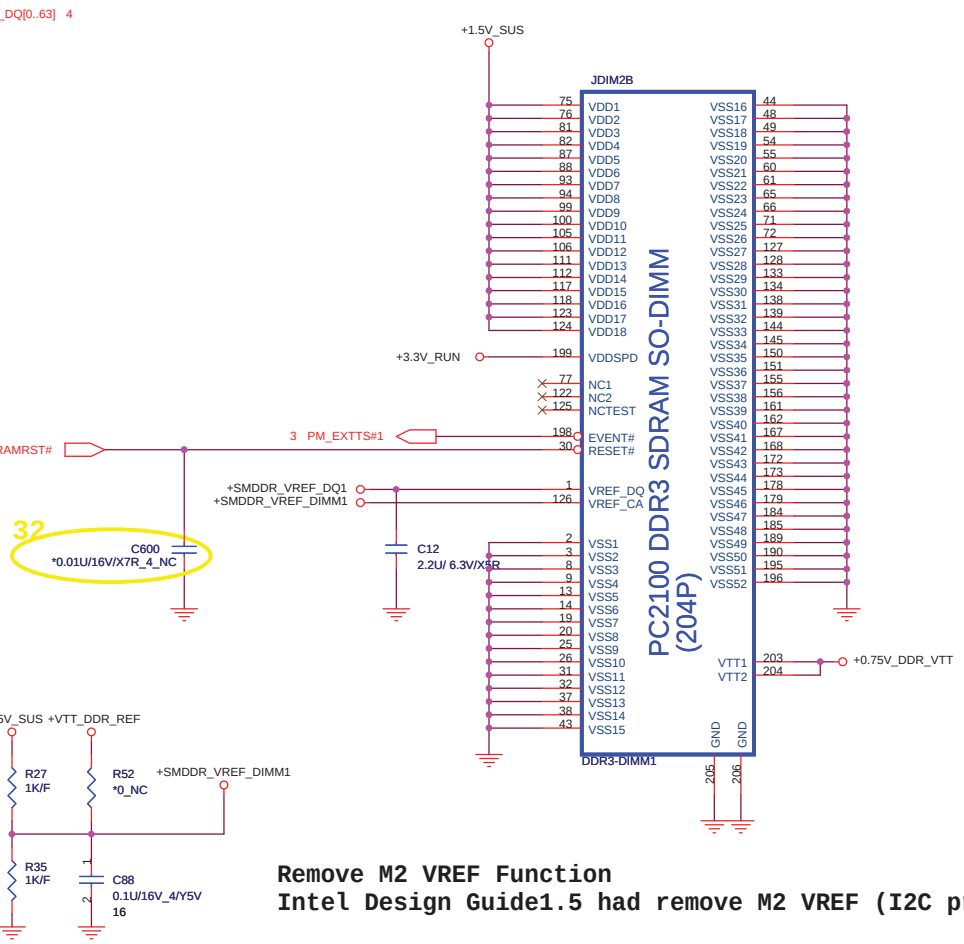
PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-0	1A
Date: Wednesday, February 10, 2010	Sheet 12 of 46	



SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

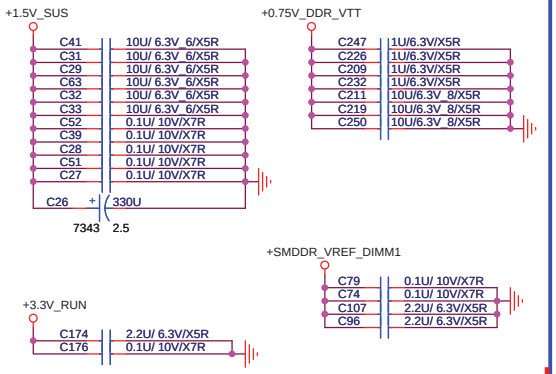


Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

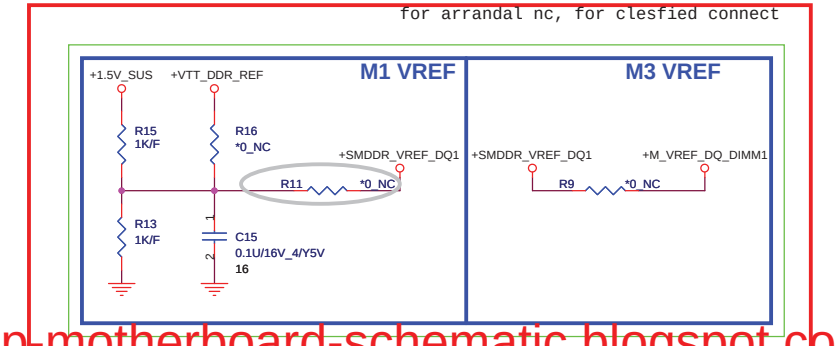
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



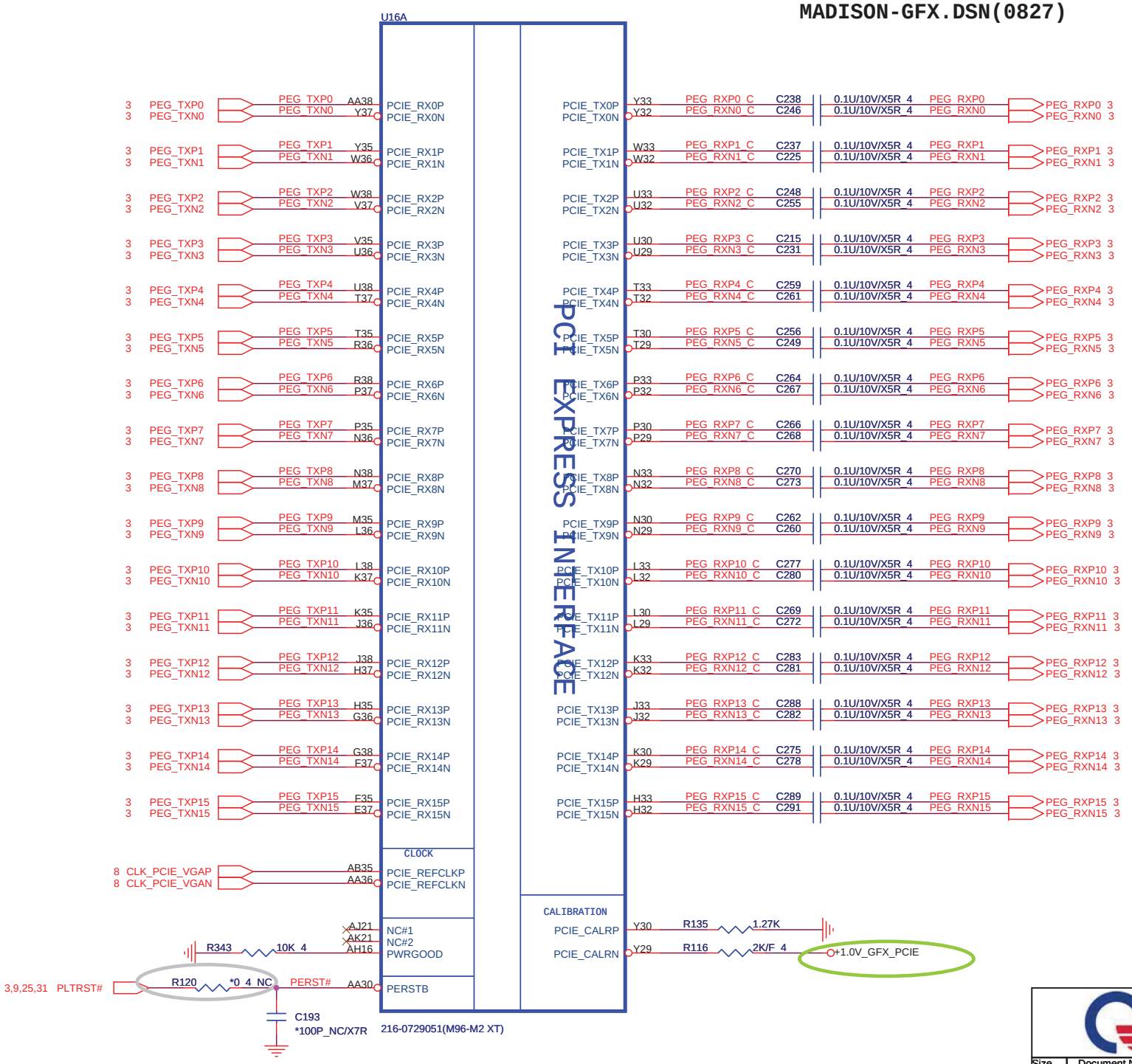
Wait Victor check

for arrandal nc, for clesfied connect



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date: Wednesday, February 10, 2010	Sheet 13 of 46	



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison PCIE I/F	1A

Date: Wednesday, February 10, 2010 Sheet 14 of 46

Memory Straps		R342 RAM_TYPE_CFG3	R340 RAM_TYPE_CFG2	R341 RAM_TYPE_CFG1	R339 RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
800 MHz 1Gb(128M*16) Hynix_Orion die	H5TQ2G63BFR-12C	0	0	1	0
800 MHz 1Gb(128M*16) Samsung_E die	K4W2G1646b-HC12	0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

(GPIO_19_CTF)
Critical temperature fault (active high)
CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power.

!!! NC when PARK-M2

!!! NC when PARK-M2

!!! NC when PARK-M2

Park and Madison

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	VGAVSYNC2	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0
BIOS_ROM_EN (Internal pull down)	GPIO_22_ROMCSB	1 = Enable external BIOS ROM device 0 = Disable external BIOS ROM device	0

GPU Power-on sequence

1 => +3V_D
2 => +1.5V_GPU = +1.5V_RUN
3 => +VGPU_CORE
4 => +VGPU_IO
5 => +1V = +1.0V_GFX_PCIE
6 => +1.8V_GPU = +1.8V_RUN_GFX
7 => dGPU_PWROK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

1.0V @ 150mA DPLL_VDDC

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

Solve Intermittent System Boot-up Hangs

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function

216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM8B DIS
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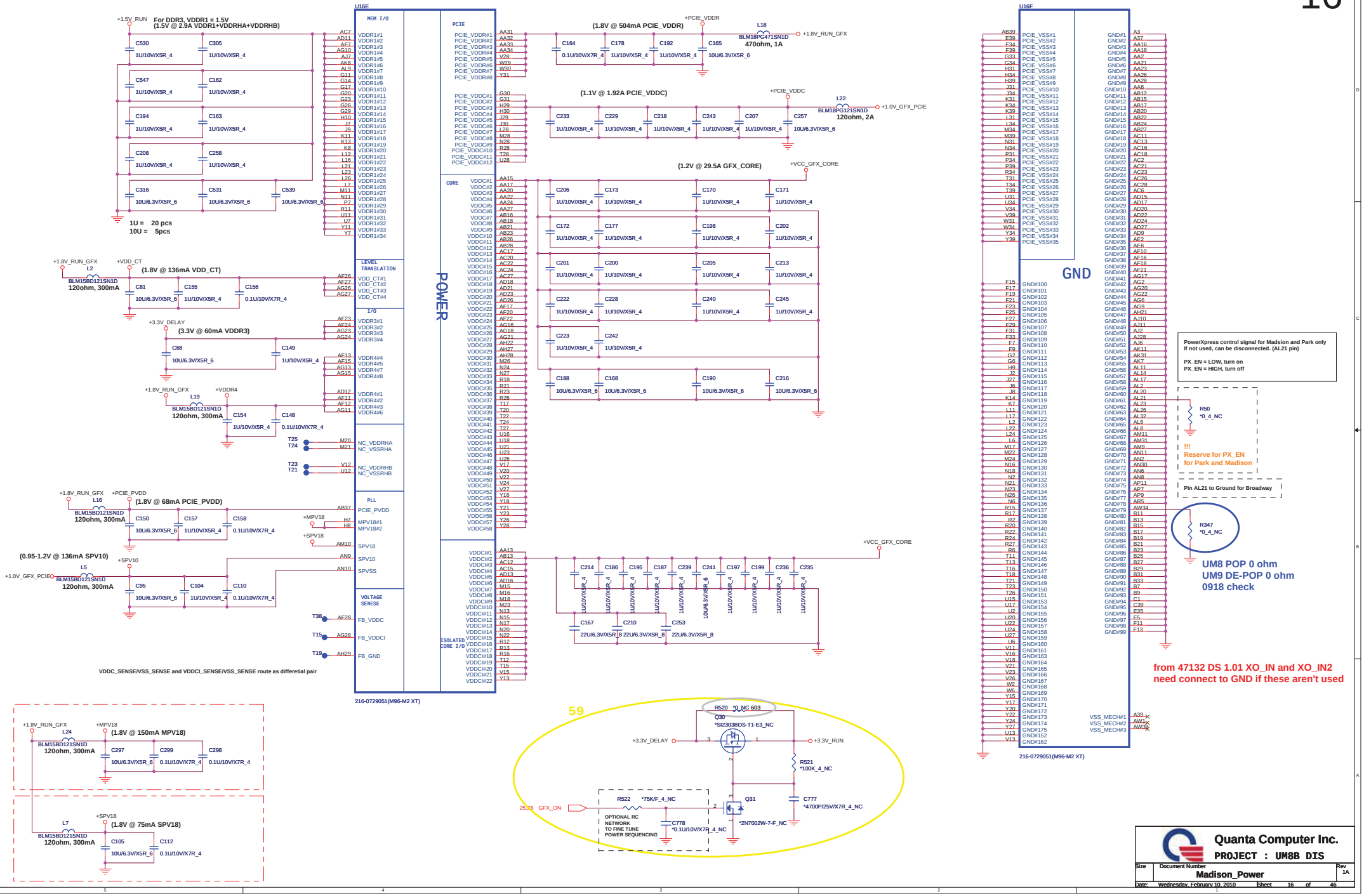

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

DPC & DPD aren't used.

U16H

DP C/D POWER | DP A/B POWER

+1.8V_RUN_GFX
AP20 DPC_VDD18#1
AP21 DPC_VDD18#2
C499 *0.1U/10V/X7R_4_NC
+1.0V_GFX_PCIE
AP13 DPC_VDD10#1
AT13 DPC_VDD10#2
C106 *0.1U/10V/X7R_4_NC
AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5

+1.8V_RUN_GFX
AP22 DPD_VDD18#1
AP23 DPD_VDD18#2
C502 *0.1U/10V/X7R_4_NC
+1.0V_GFX_PCIE
AP14 DPD_VDD10#1
AP15 DPD_VDD10#2
C97 *0.1U/10V/X7R_4_NC
AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5

DPA_VDD18#1 AN24 +DPA_VDD18
DPA_VDD18#2 AP24
DPA_VDD10#1 AP31
DPA_VDD10#2 AP32
+DPA_VDD10 (1V @ 200mA DPA_VDD10)
L3 BLM15BD121SN1D 120ohm, 300mA +1.0V_GFX_PCIE
DPA for HDMI
C101 0.1U/10V/X7R_4
C111 1U/10V/X5R_4
C83 10U/6.3V/X5R_6
DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26

DPB_VDD18#1 AP25 +DPB_VDD18
DPB_VDD18#2 AP26
+1.8V_RUN_GFX
C513 *0.1U/10V/X7R_4_NC
DPB_VDD10#1 AN33
DPB_VDD10#2 AP33
+1.0V_GFX_PCIE
C67 *0.1U/10V/X7R_4_NC
DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32

(1.8V @ 400mA DPE_VDD18; 200mA for DPE/DPF respectively)
+1.8V_RUN_GFX
L10 BLM18PG600SN1D 60ohm, 500mA
+DPE_VDD18
C131 C128 C127
10U/6.3V/X5R_6 1U/10V/X5R_4 0.1U/10V/X7R_4
DPE & DPF for LVDS
150/F_4 R344 AW18 DPCD_CALR
DPAB_CALR AW28 R345 150/F_4

DP E/F POWER | DP PLL POWER

DPE_VDD18#1 AH34
DPE_VDD18#2 AJ34
+DPE_VDD10
DPE_VDD10#1 AL33
DPE_VDD10#2 AM33
DPE_VSSR#1 AN34
DPE_VSSR#2 AP39
DPE_VSSR#3 AR39
DPE_VSSR#4 AU37
DPE_VSSR#5 AW35

UM8 POP 0 ohm
UM9 DE-POP 0 ohm
0918 check
R348 0_4
+DPE_VDD18

(1.1V @ 200mA DPE_VDD10; 100mA for DPE/DPF respectively)
+1.0V_GFX_PCIE
L4 BLM15BD121SN1D 120ohm, 300mA
+DPE_VDD10
C94 C86 C102
10U/6.3V/X5R_6 1U/10V/X5R_4 0.1U/10V/X7R_4
DPF_VDD18#1 AE34
DPF_VDD18#2 AG34
DPF_VDD10#1 AK33
DPF_VDD10#2 AK34
DPF_VSSR#1 AF39
DPF_VSSR#2 AH39
DPF_VSSR#3 AK39
DPF_VSSR#4 AL34
DPF_VSSR#5 AM34
150/F_4 R354 AM39 DPEF_CALR

DPA_PVDD AU28
DPA_PVSS AV27
DPB_PVDD AV29
DPB_PVSS AR28
DPC_PVDD AU18
DPC_PVSS AV17
DPD_PVDD AV19
DPD_PVSS AR18
DPE_PVDD AM37
DPE_PVSS AN38
NC_DPF_PVDD AL38
NC_DPF_PVSS AM35

(1.8V @ 20 mA DPA_PVDD)
+DPA_PVDD
L33 BLM15BD121SN1D 120ohm, 300mA +1.8V_RUN_GFX
C511 C501 C498
0.1U/10V/X7R_4 1U/10V/X5R_4 10U/6.3V/X5R_6
+1.8V_RUN_GFX
C492 *0.1U/10V/X7R_4_NC

DPC & DPD aren't used.
+1.8V_RUN_GFX
C494 *0.1U/10V/X7R_4_NC
C508 *0.1U/10V/X7R_4_NC

(1.8V @ 40mA DPE_PVDD; 20mA for DPE/DPF respectively)
+DPE_PVDD
L35 BLM15BD121SN1D 120ohm, 300mA +1.8V_RUN_GFX
C529 C528 C523
0.1U/10V/X7R_4 1U/10V/X5R_4 10U/6.3V/X5R_6

+DPA_VDD18
(1.8V @ 110mA DPA_VDD18)
L34 BLM15BD121SN1D 120ohm, 300mA +1.8V_RUN_GFX
C87 C512 C500
0.1U/10V/X7R_4 1U/10V/X5R_4 10U/6.3V/X5R_6

216-0729051(M96-M2 XT)

U16G

LVDS CONTROL
VARY_BL AK27
DIGON AJ27
R346 10K_4
R30 10K_4
BIA_PWM 22
ENVDD 22

LVTMDP
TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
TXOUT_U3P AF35 PAD T37
TXOUT_U3N AG36 PAD T20
TXCLK_LP_DPE3P AP34 LCD_ACLK+ LCD_ACLK+ 22
TXCLK_LN_DPE3N AR34 LCD_ACLK- LCD_ACLK- 22
TXOUT_L0P_DPE2P AW37 LCD_A0+ LCD_A0+ 22
TXOUT_L0N_DPE2N AU35 LCD_A0- LCD_A0- 22
TXOUT_L1P_DPE1P AR37 LCD_A1+ LCD_A1+ 22
TXOUT_L1N_DPE1N AU39 LCD_A1- LCD_A1- 22
TXOUT_L2P_DPE0P AP35 LCD_A2+ LCD_A2+ 22
TXOUT_L2N_DPE0N AR35 LCD_A2- LCD_A2- 22
TXOUT_L3P AN36 PAD T36
TXOUT_L3N AP37 PAD T35

216-0729051(M96-M2 XT)

from 47132 DS 1.01 XO_IN and XO_IN2
need connect to GND if these aren't used

Quanta Computer Inc.
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	Madison_DP_POWER	1A
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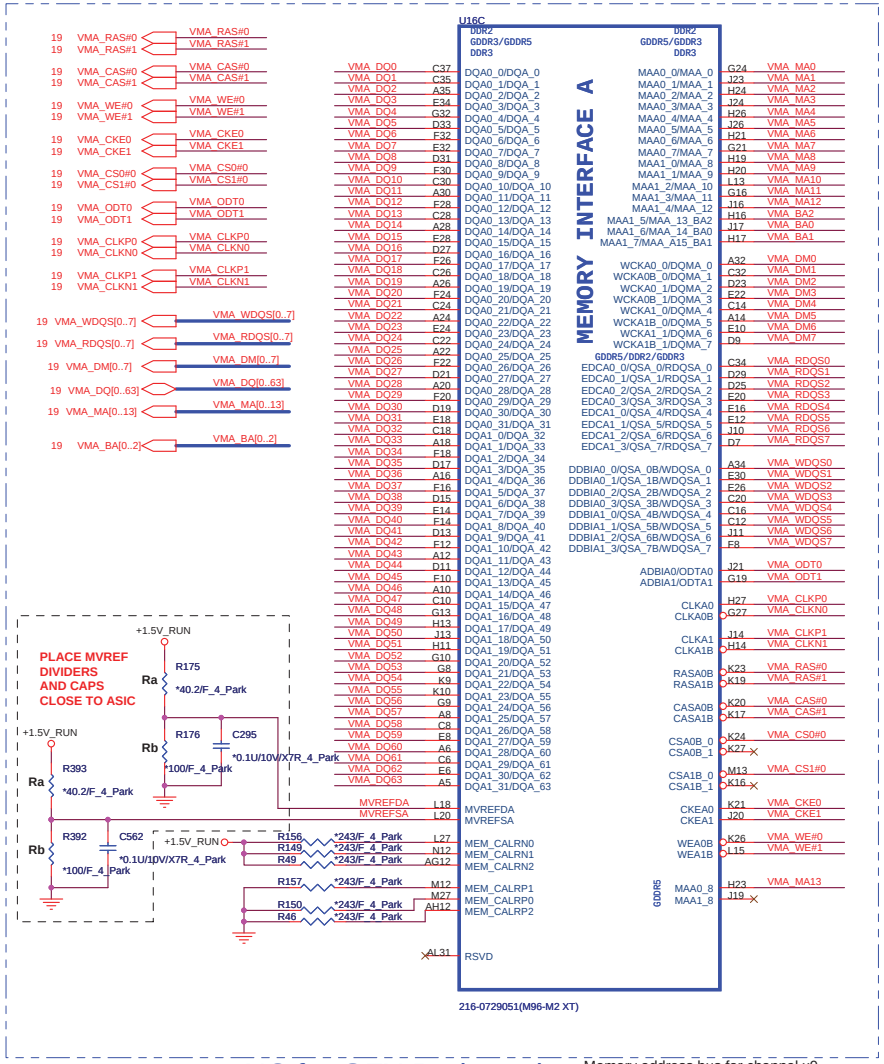
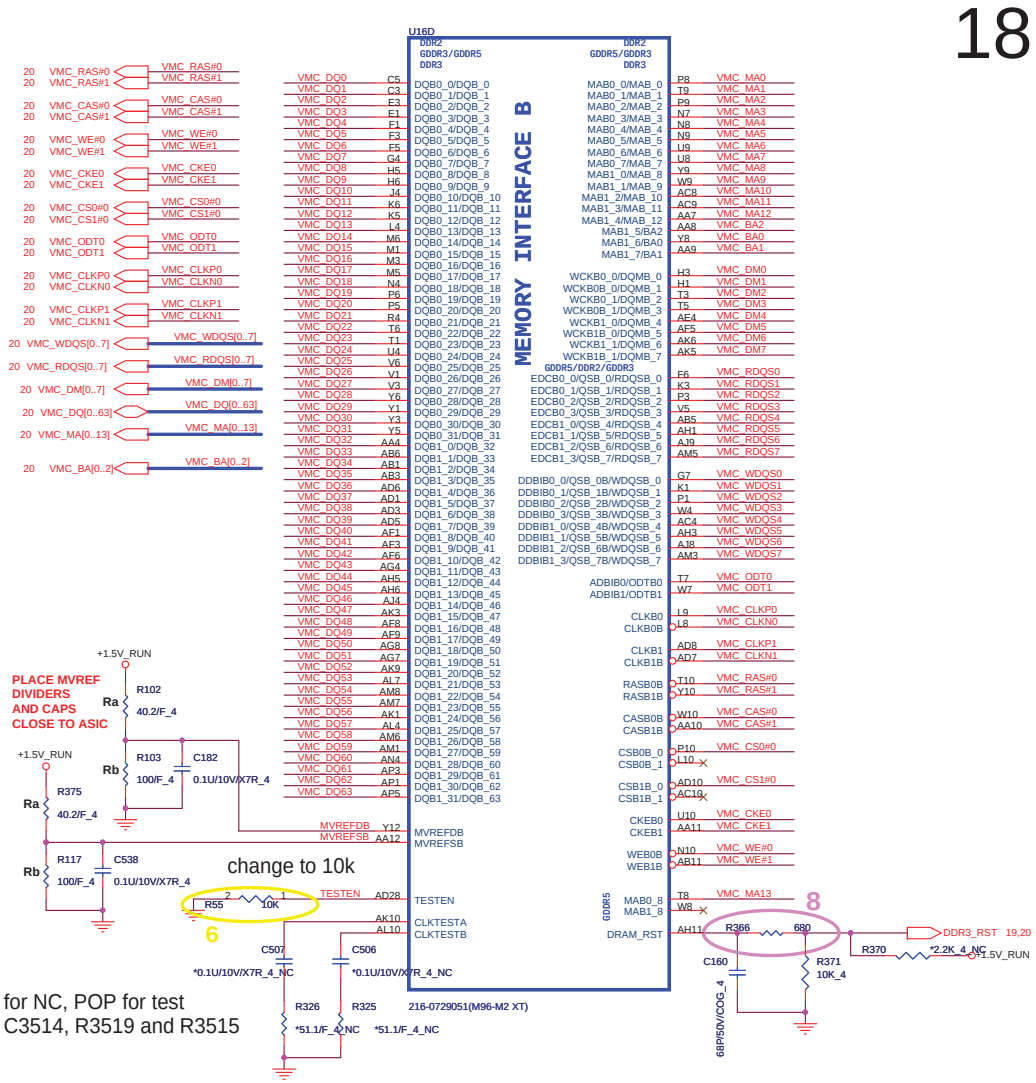




Normal for NC, POP for test
C3513, C3514, R3519 and R3515

NC for GFX Park portion

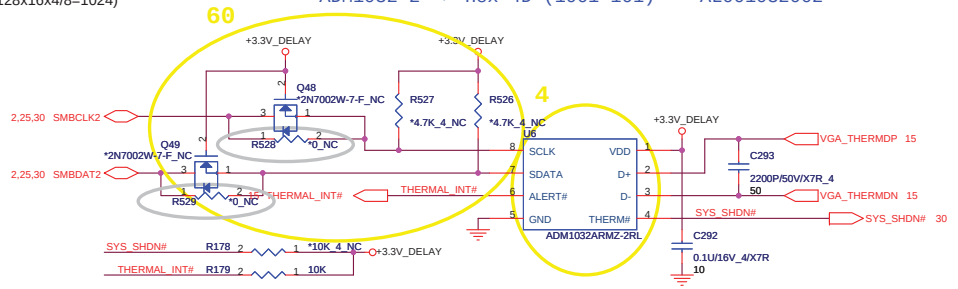
For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

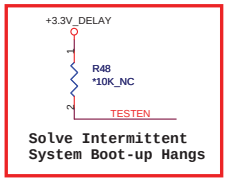
Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

Memory address bus for channel x0. Provides multiplexed row and column addresses. For 128-Mbit x16 DDR3 support, MAx13 is supported on MAx0_8. (128x16x4/8=1024)

ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002



Designator	For M97-M2	For Madison
R272	10K	10K
R271	0R/Short	680R
R273	NC	NC
C408	2.2nF	68pF



DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

Quanta Computer Inc.
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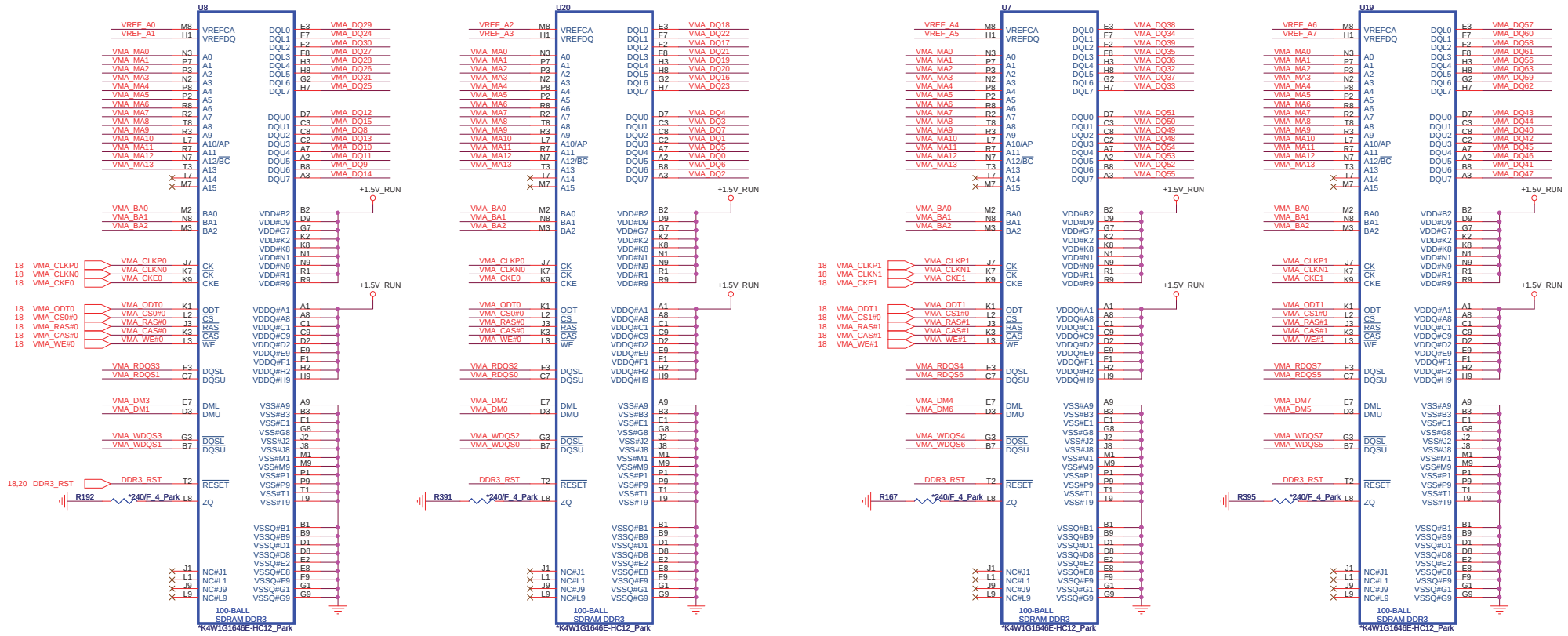
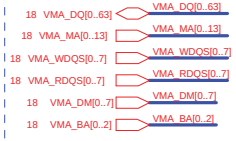
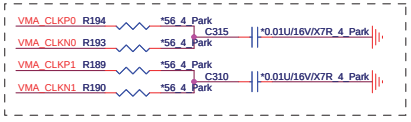
CHECK PN

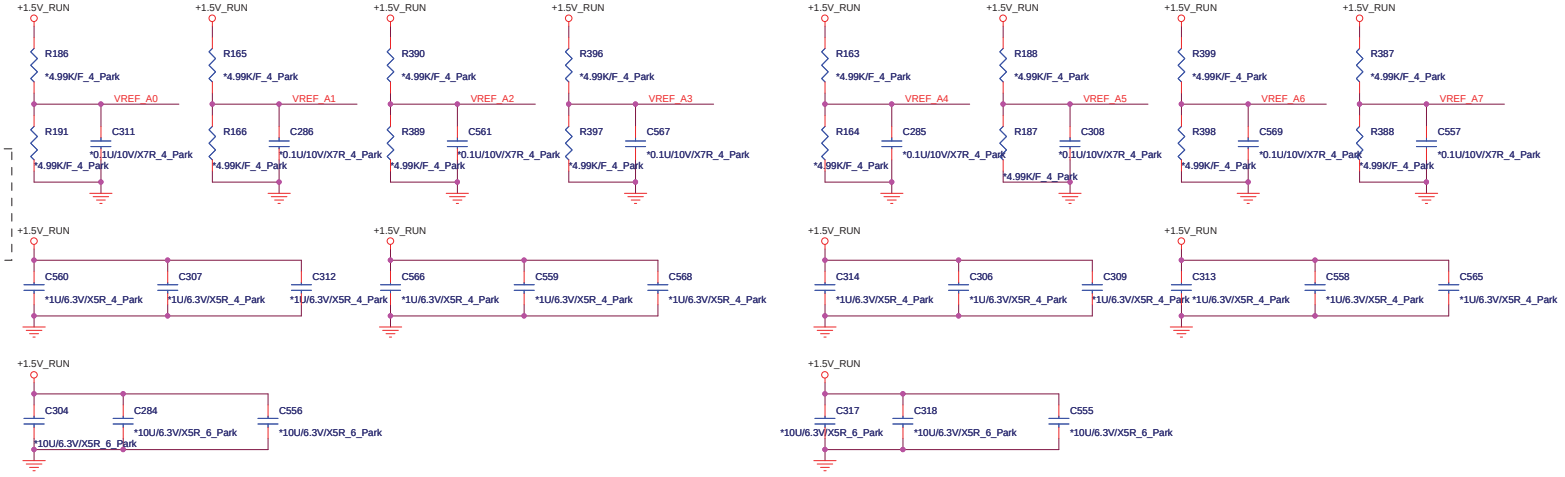
DDR3 64MX16, CH A : 512MB





Placement has to be close to VRAM





NC for GFX Park portion

Samsung: AKD5LGGT505

Hynix: AKD5LZGTW03

Quanta Computer Inc.		
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	Madison_DDR3_A_512M	1A
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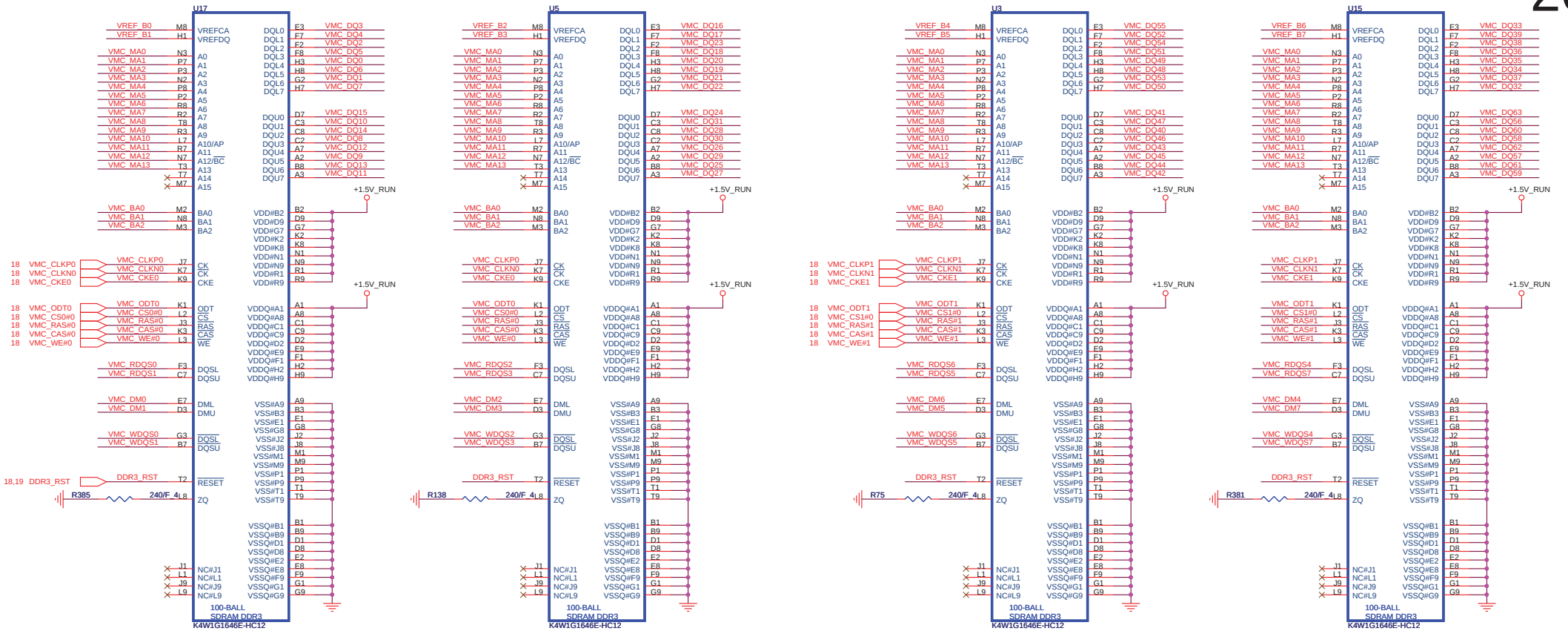
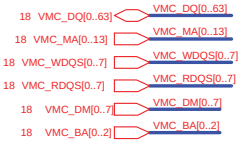
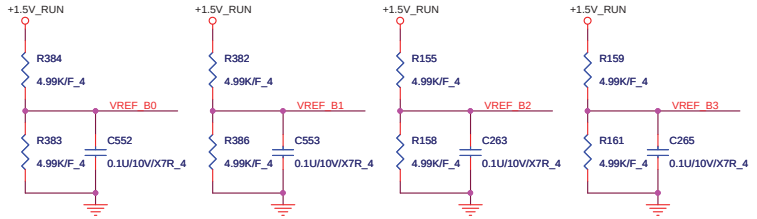
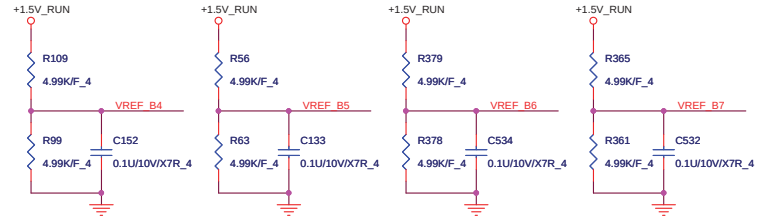
DDR3 64MX16, CH B : 512MB

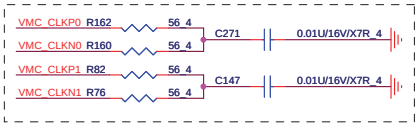


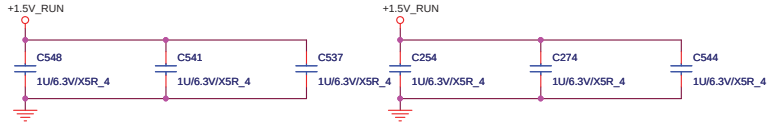


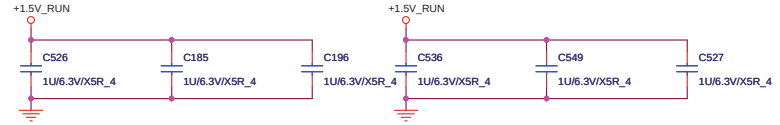


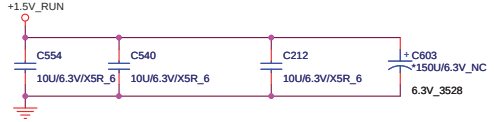


Placement has to be close to VRAM









Quanta Computer Inc.
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	Madison_DDR3_B_512M	1A
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Quanta Computer Inc.

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	Blank	1A
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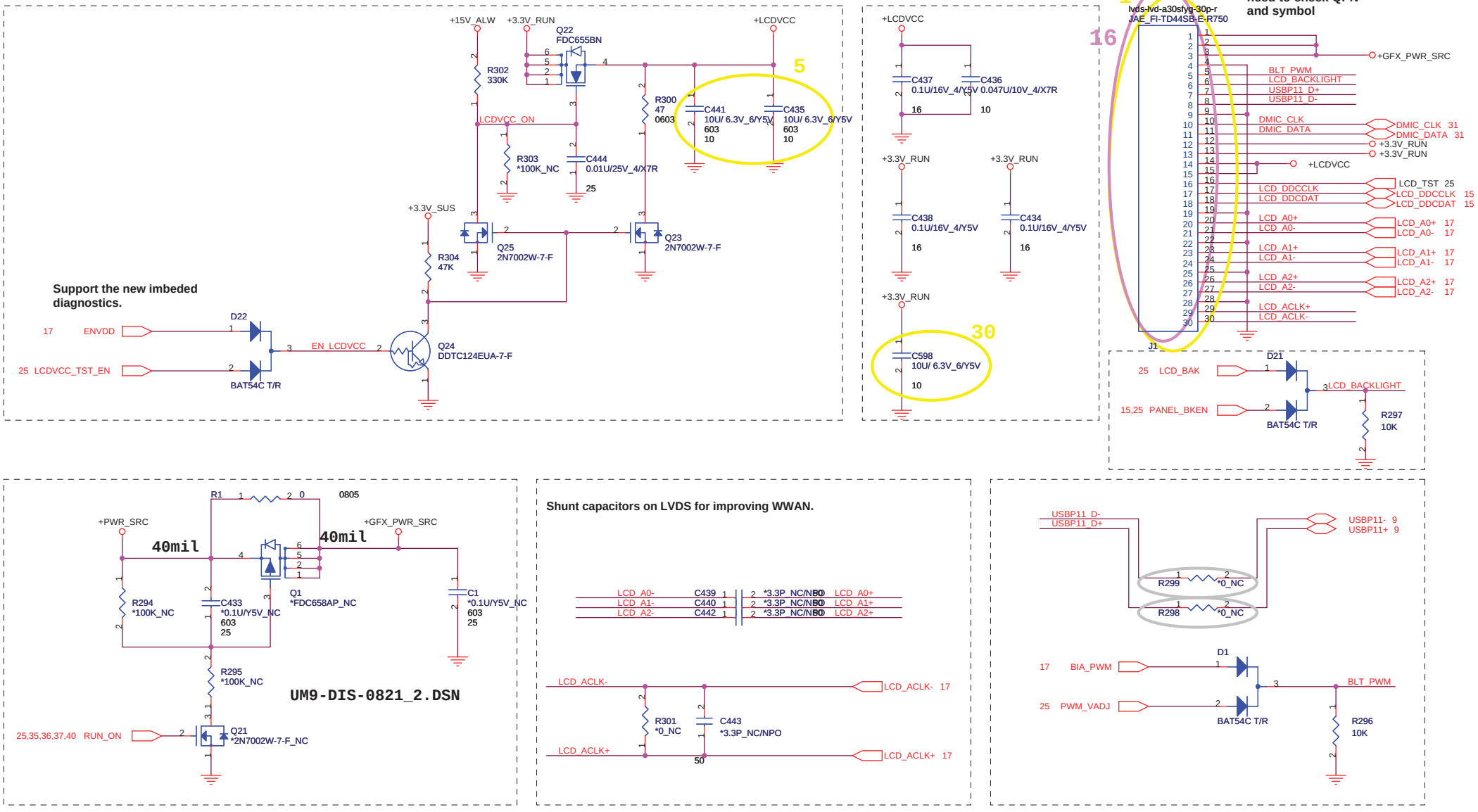

Quanta Computer Inc.		
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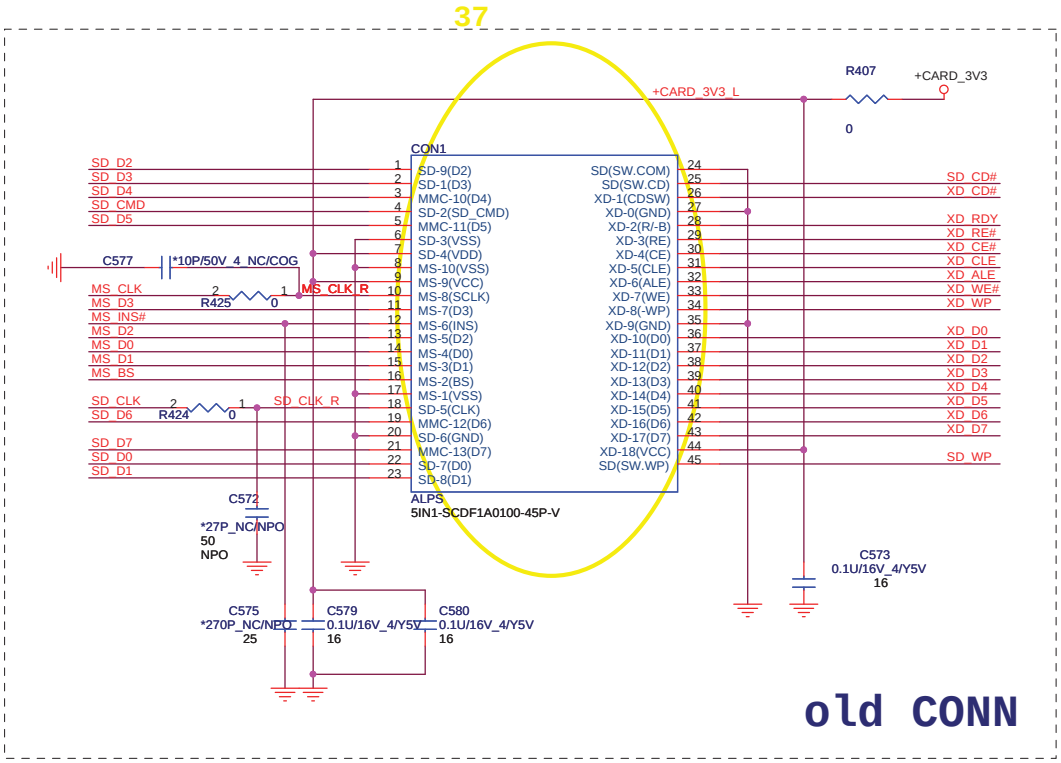

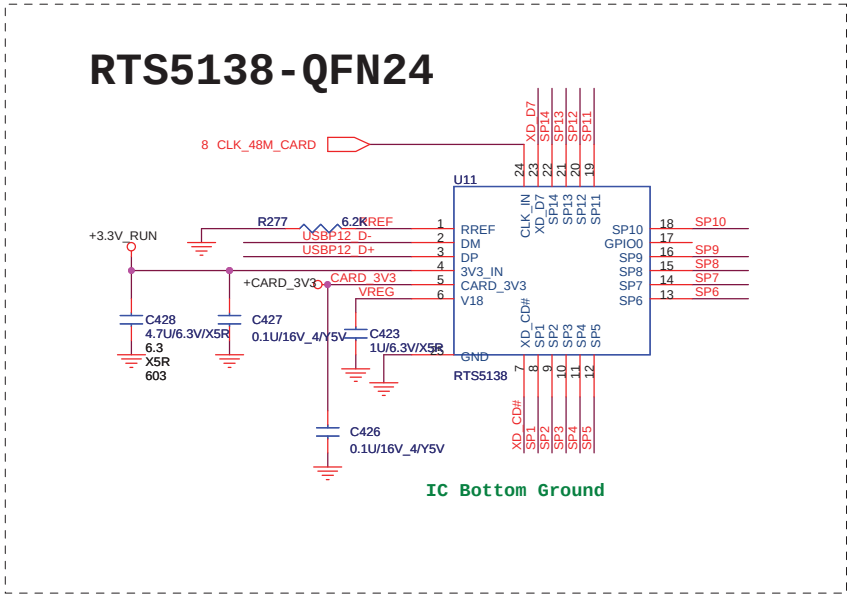

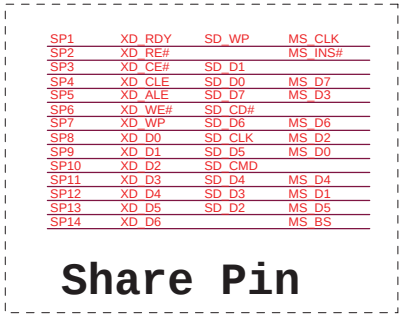

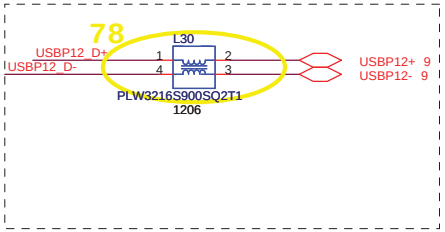

Quanta Computer Inc.

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Size	Document Number	Rev
	Card Reader(RST5138)	1A
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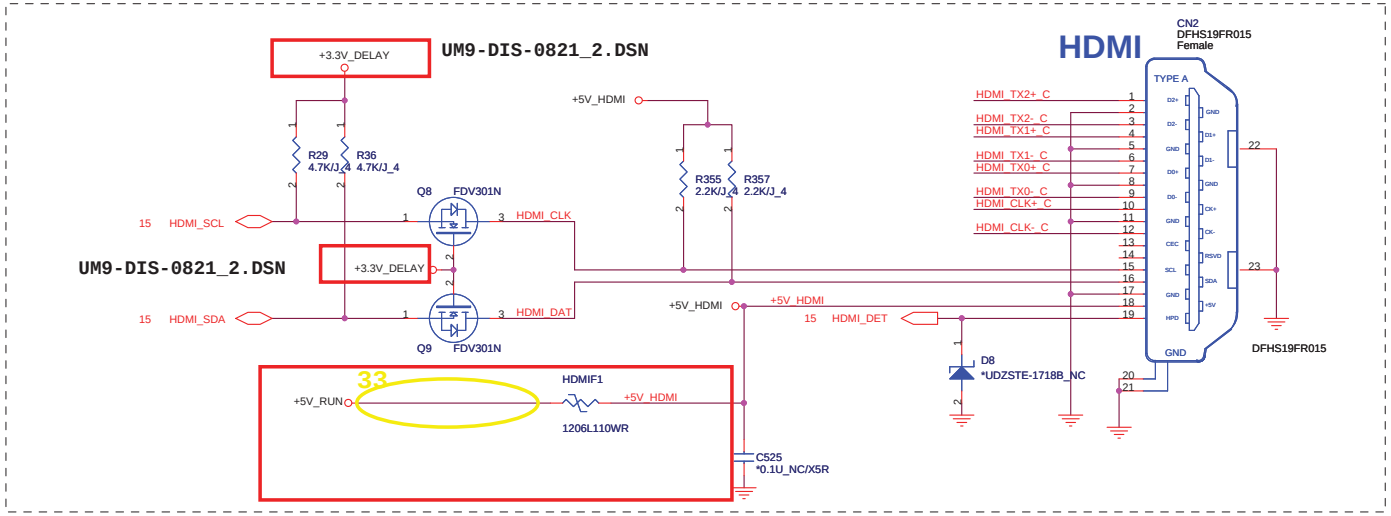

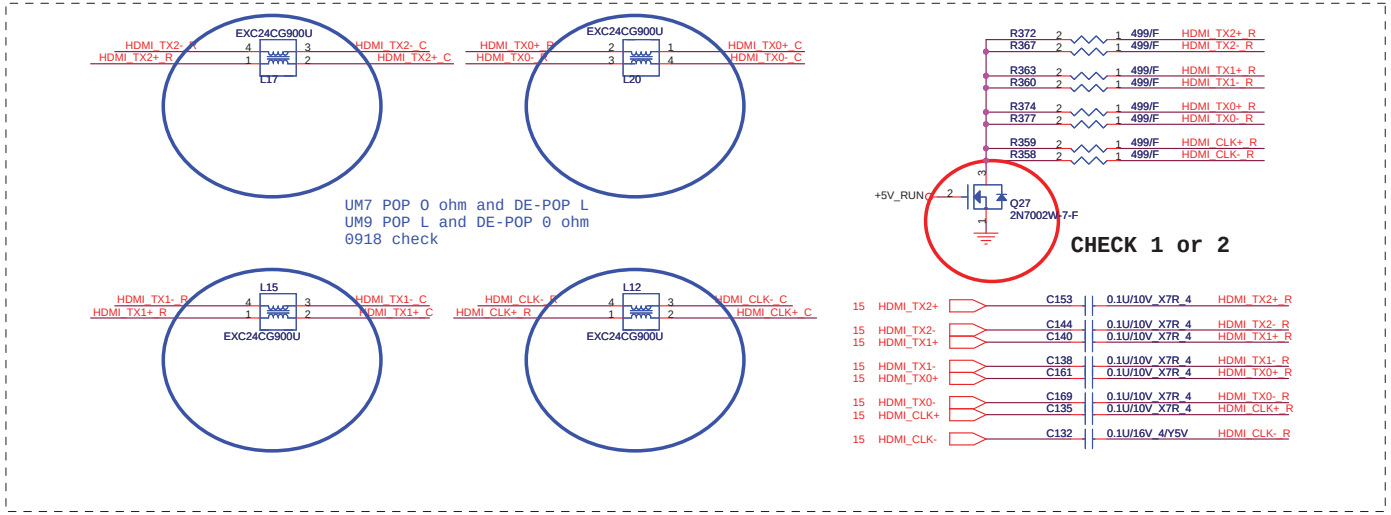

Quanta Computer Inc.

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UM3

U4

ITE8502E
LQFP-128L

KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO

Place these caps close to ITE8502.

Charge and BAT
PCH
LAN, Clock Thermal IC

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Check

UM7 POP 2.2k
UM9 POP 10k
0918 check

UM7 DE-POP
UM9 POP
0918 check

Board ID Straps
Park 1G
Discrete
Park
UMA
VGA_TYPE
VGA_IDENTIFY

BID1	USB_RIGHT_EN#	UM8(UMA)	UM8C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

32KHz Clock.

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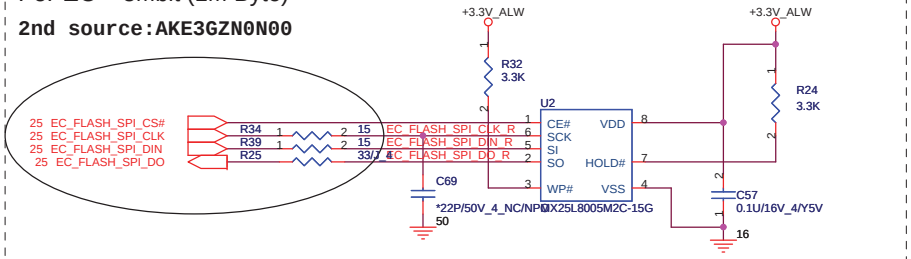
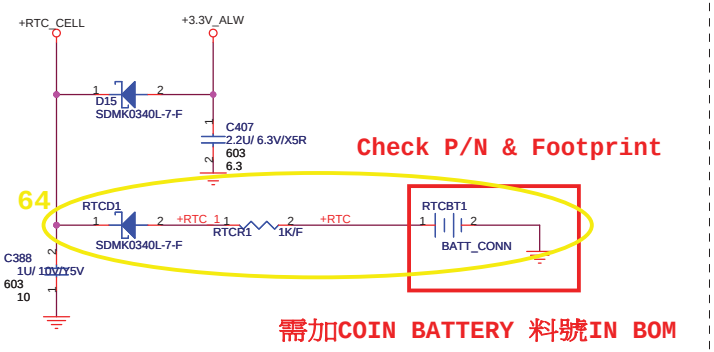
For EC 8Mbit (1M Byte)

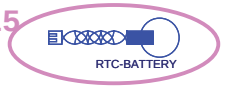
2nd source:AKE3GZN0N00



RTC BATTERY



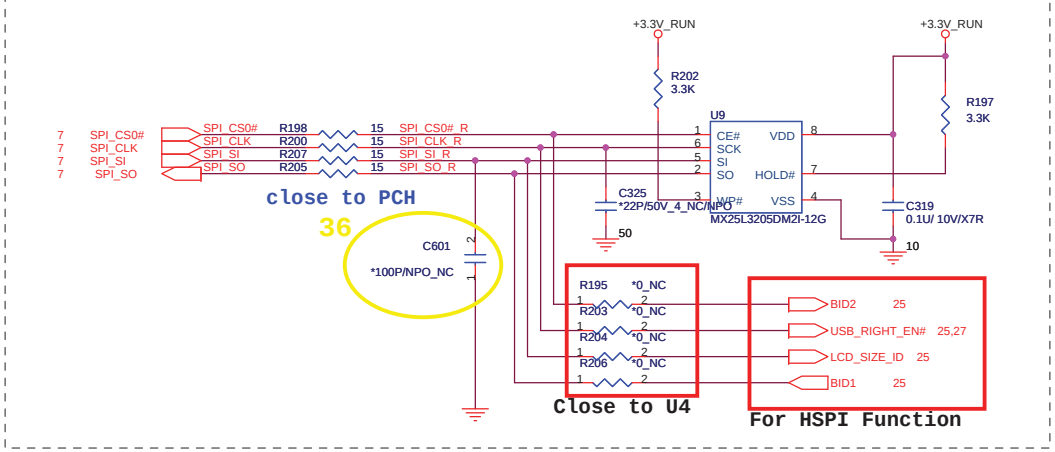
15



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	FLASH/RTC	1A
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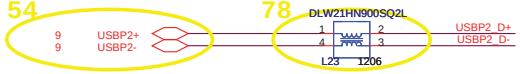
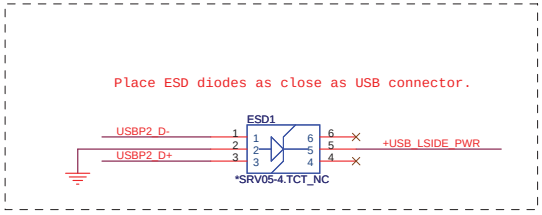
eSATA and USB To DB

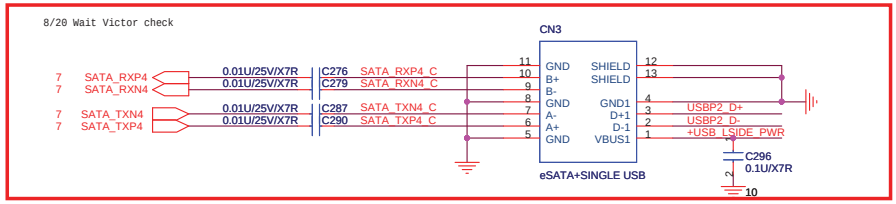
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

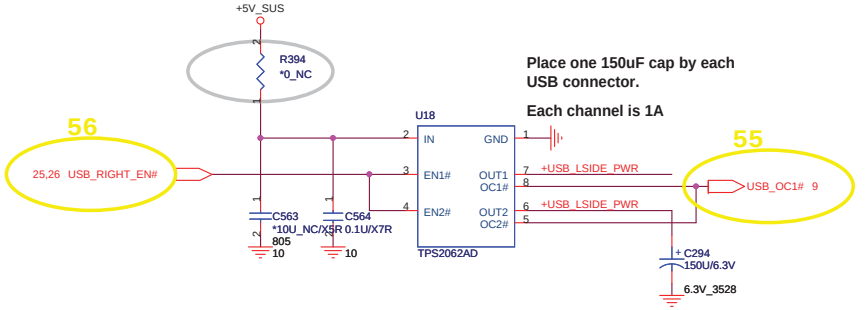


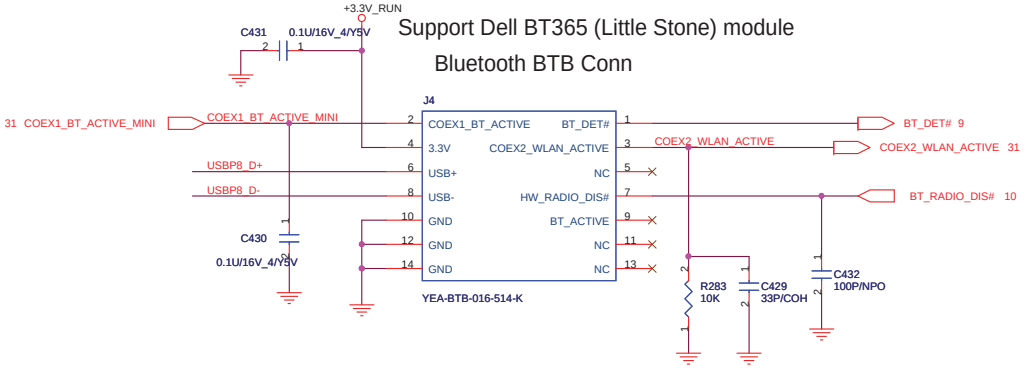
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

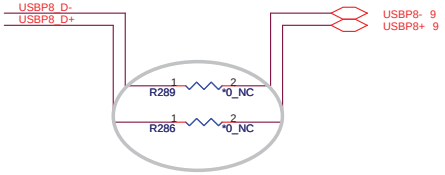


USB and eSATA Conn.









Quanta Computer Inc.
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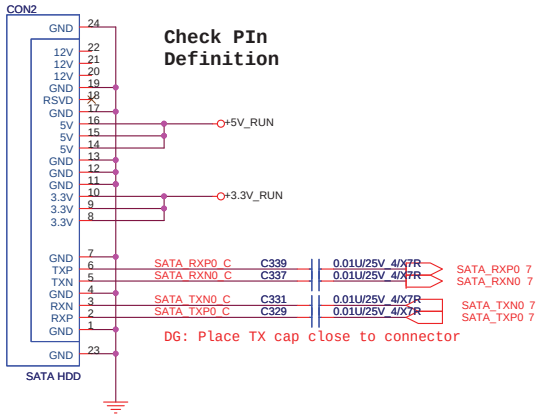
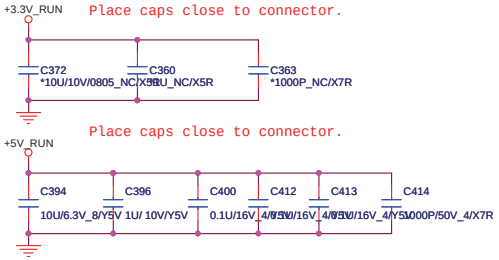
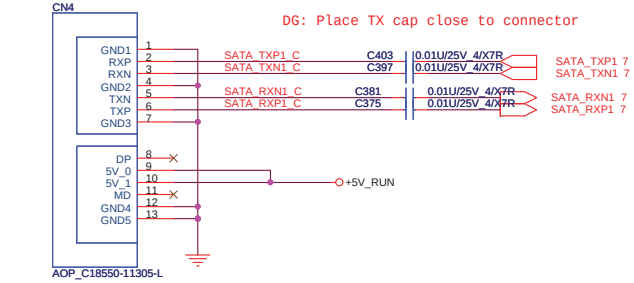
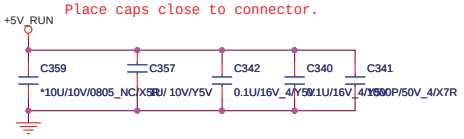
SATA Connector.

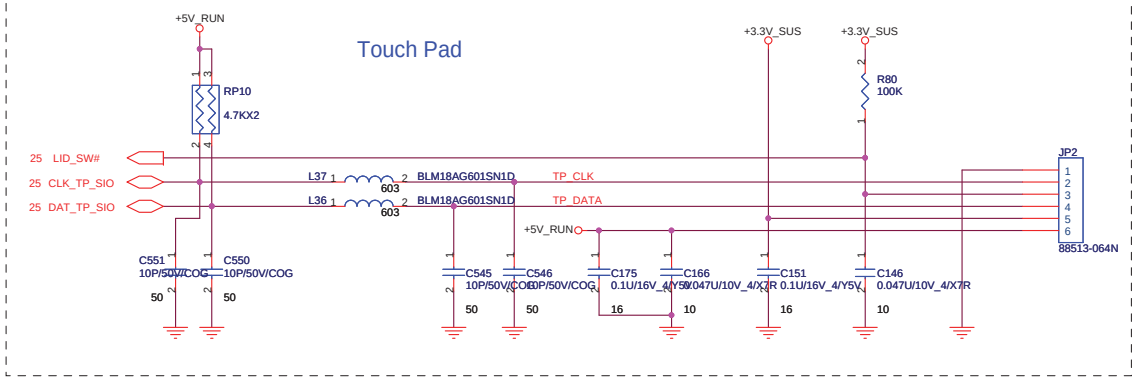




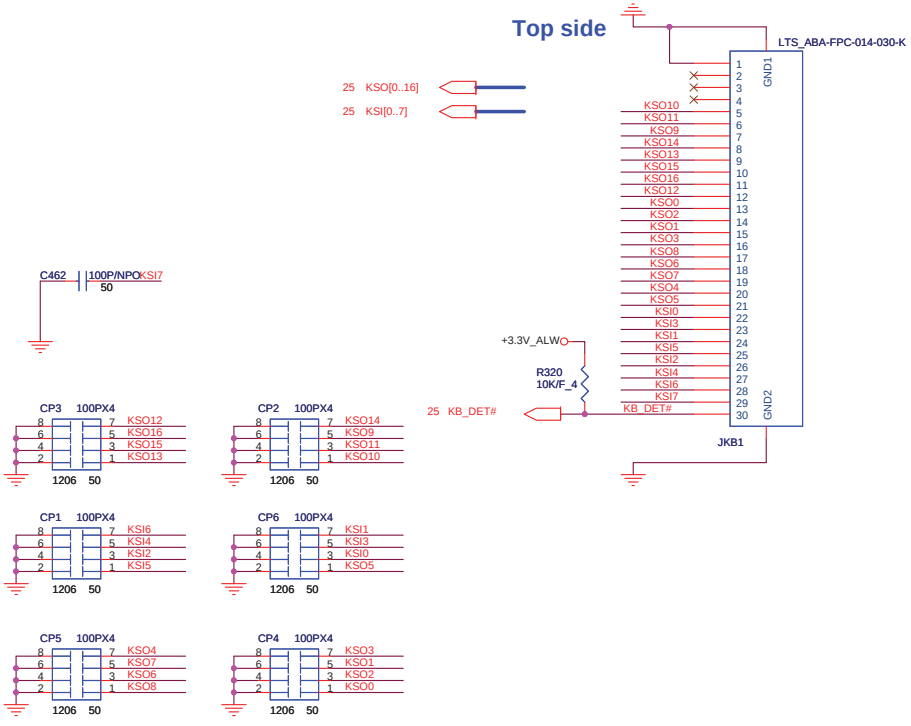
ODD Connector







KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

Quanta Computer Inc.
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	SATA (HDD&ODD) & TP & KB	1A
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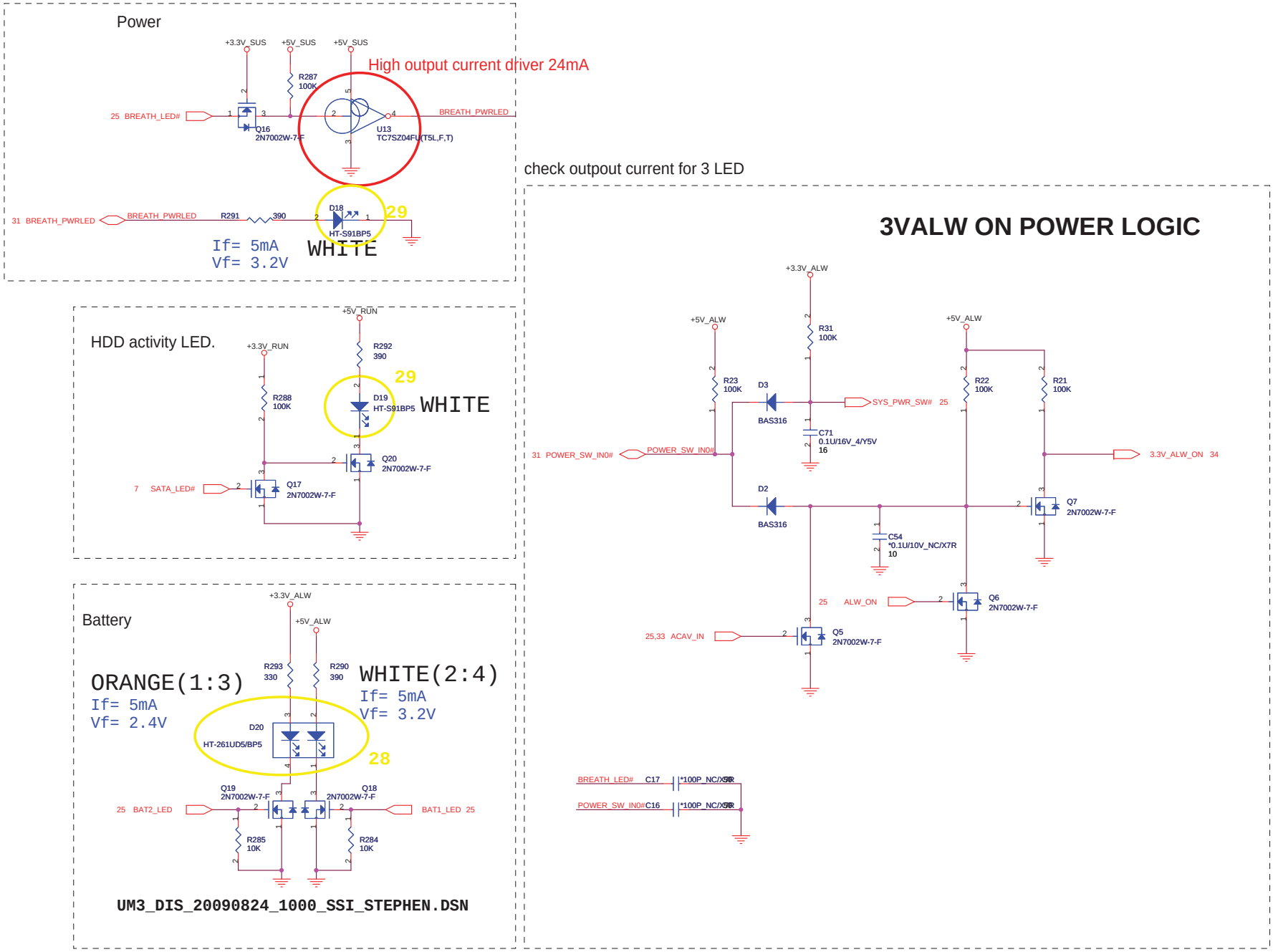

Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number	Rev
	SWITCH, LED	1A
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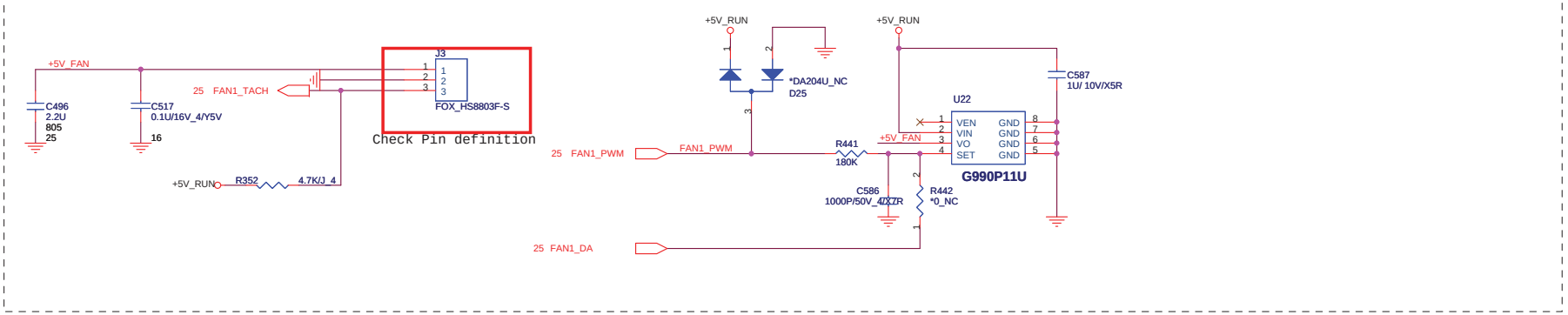
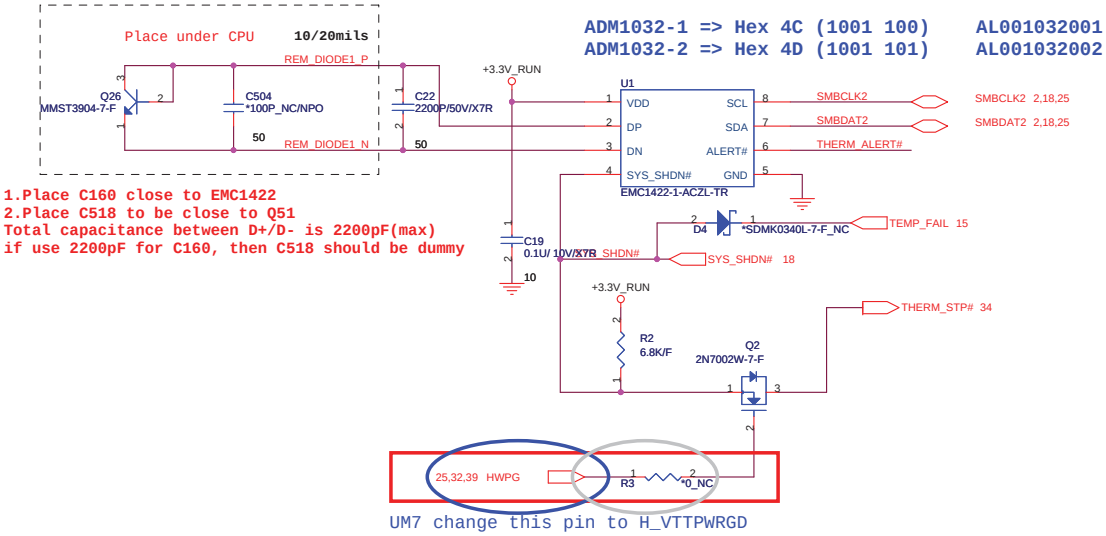
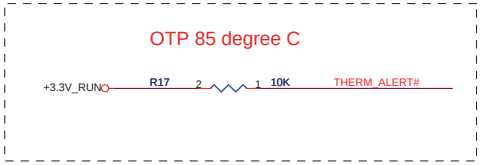
FAN CONTROL







SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

Quanta Computer Inc.
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Size | Document Number: FAN & THERMAL | Rev 1A
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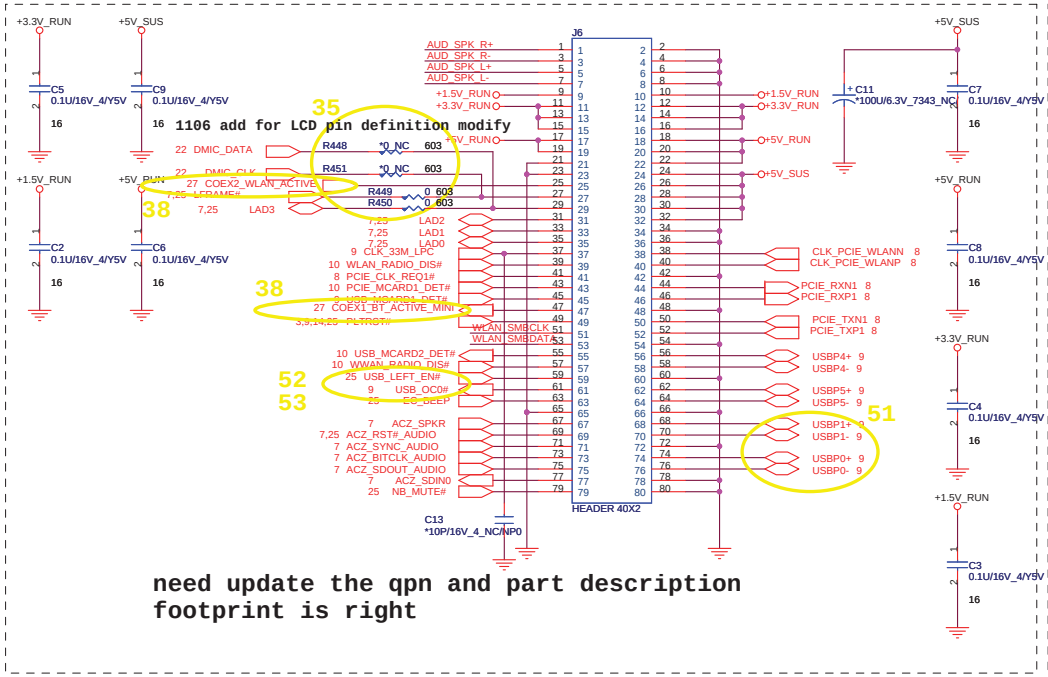

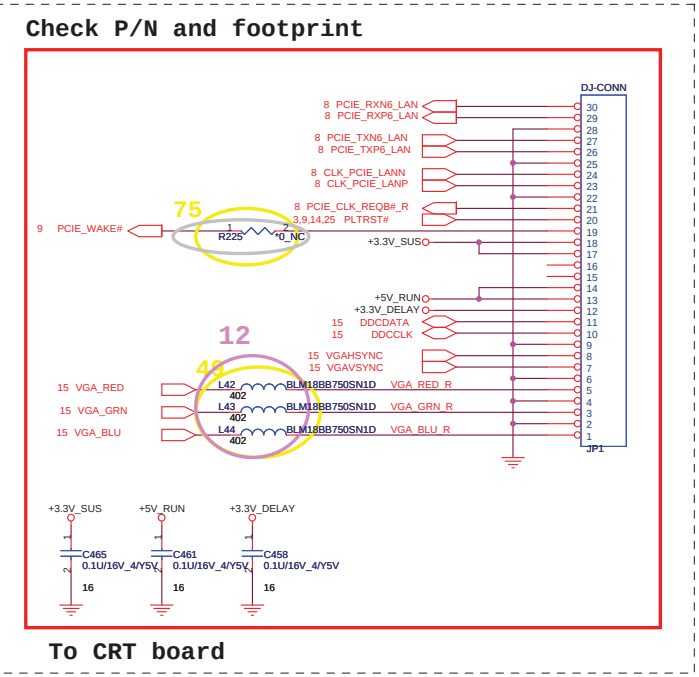

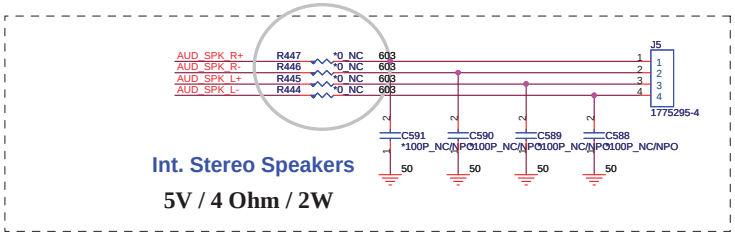

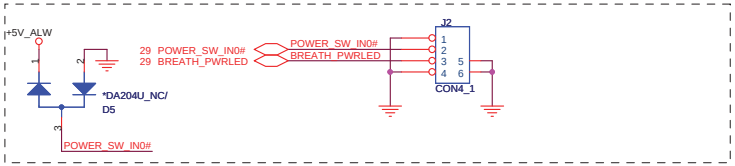

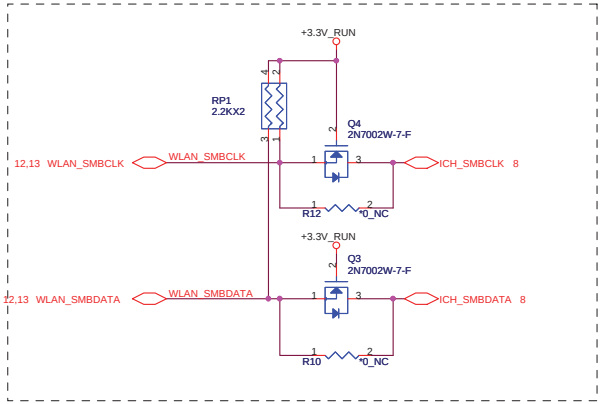

Quanta Computer Inc.
PROJECT : UM8B DIS
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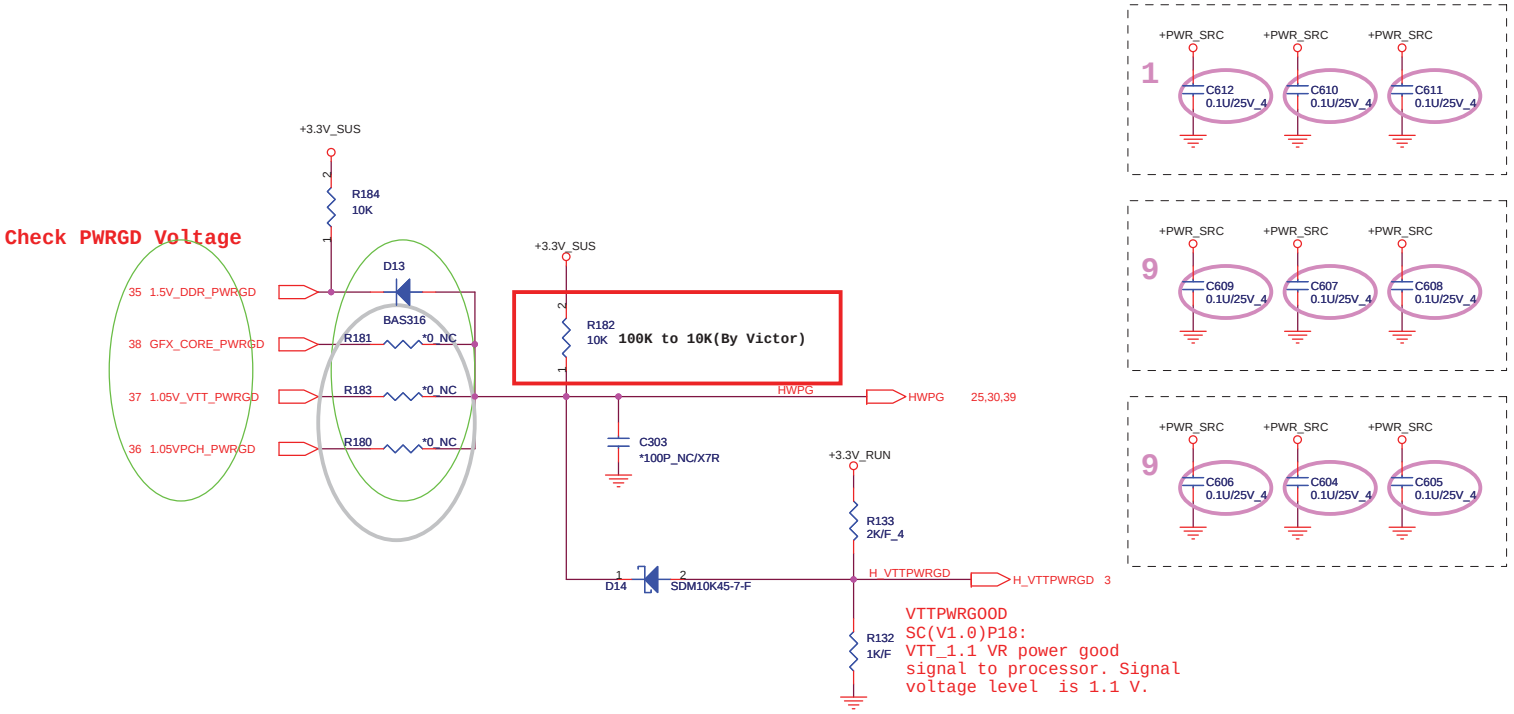

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	System Reset Circuit	1A

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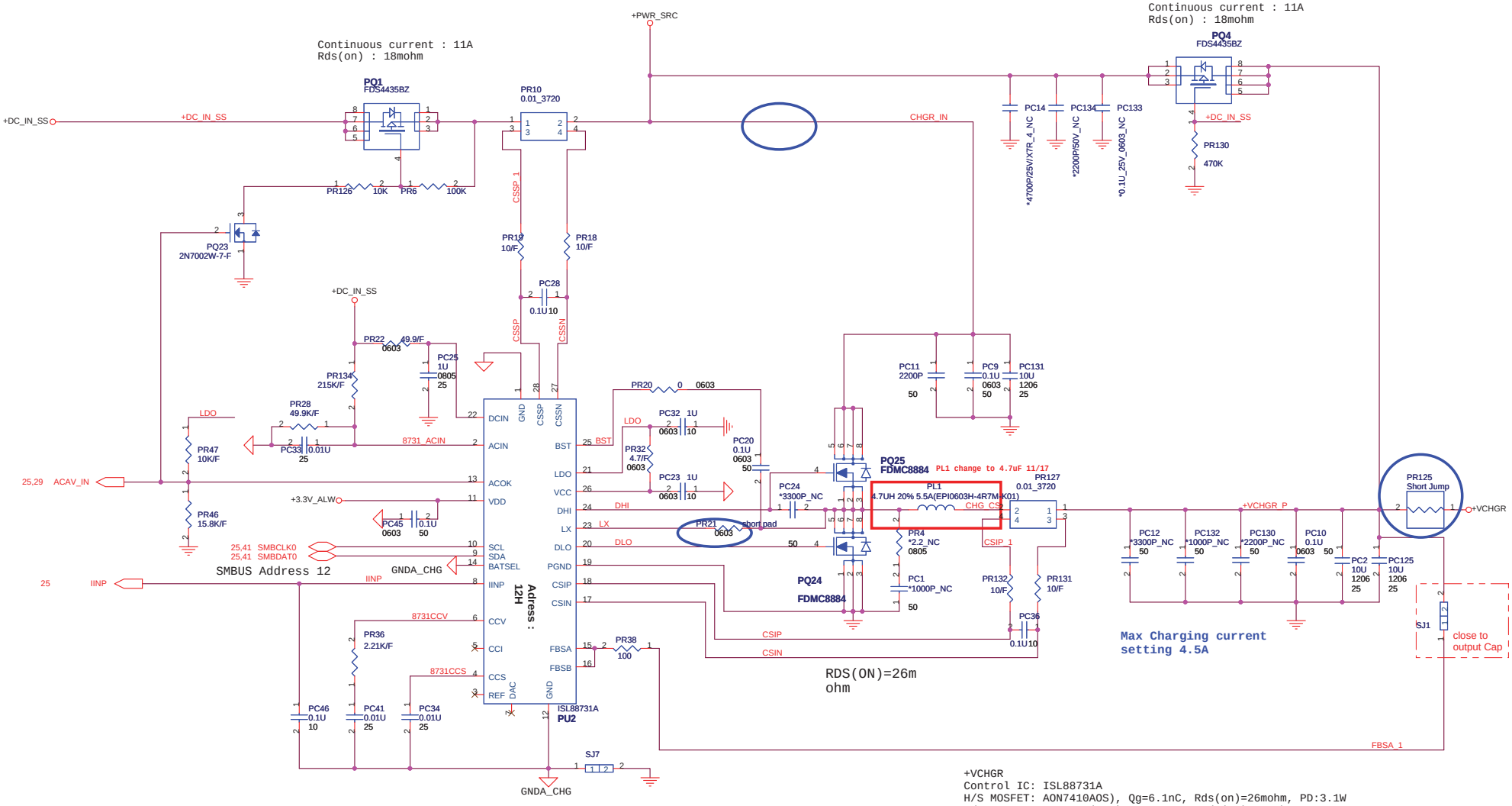

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Charger	1A
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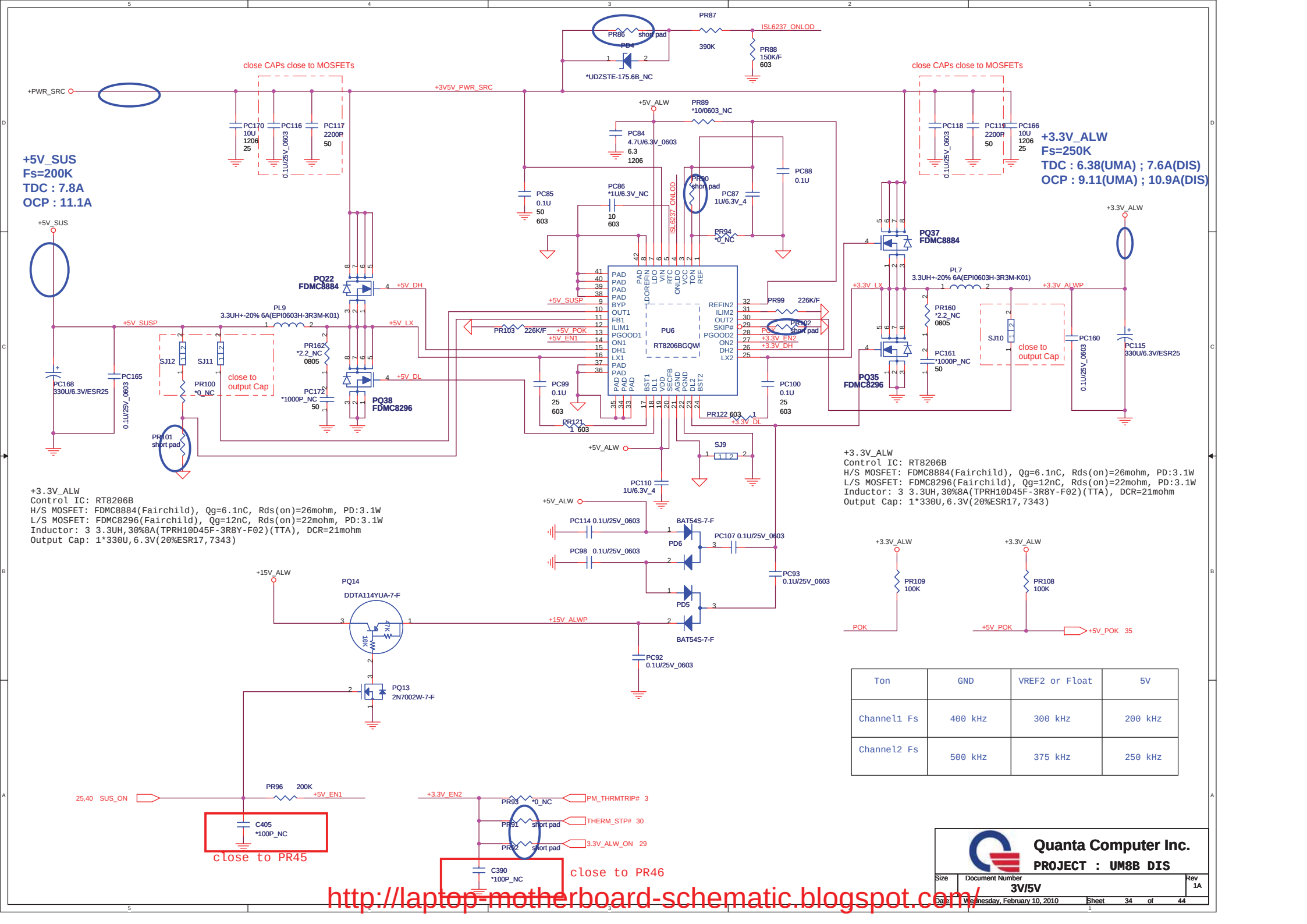

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.
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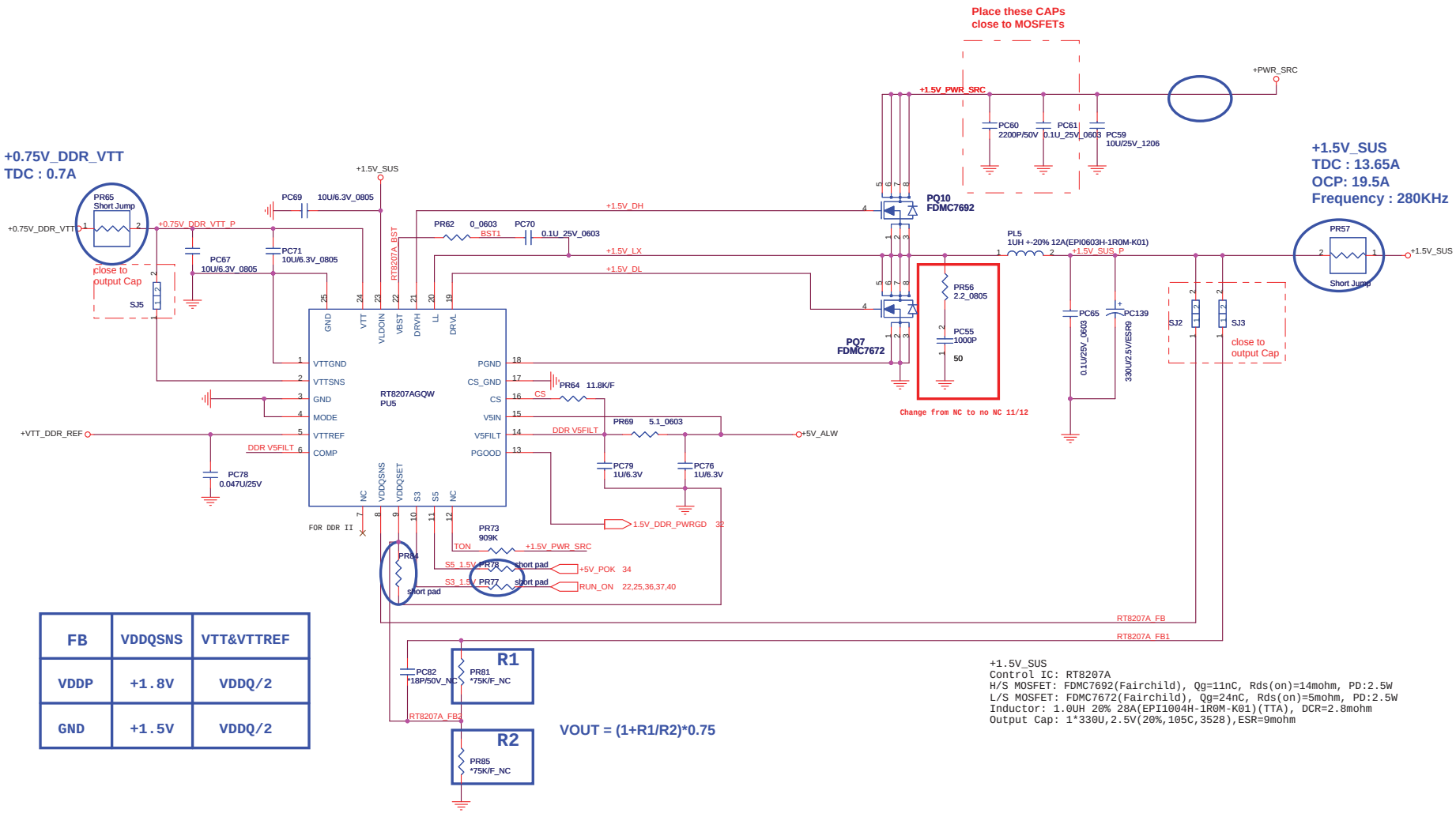
Size	Document Number	Rev
	3V/5V	1A
Date:	Wednesday, February 10, 2010	Sheet 34 of 44



FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

Quanta Computer Inc.
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Size: Document Number: 1.5V_DDR/0.75V Rev 1A
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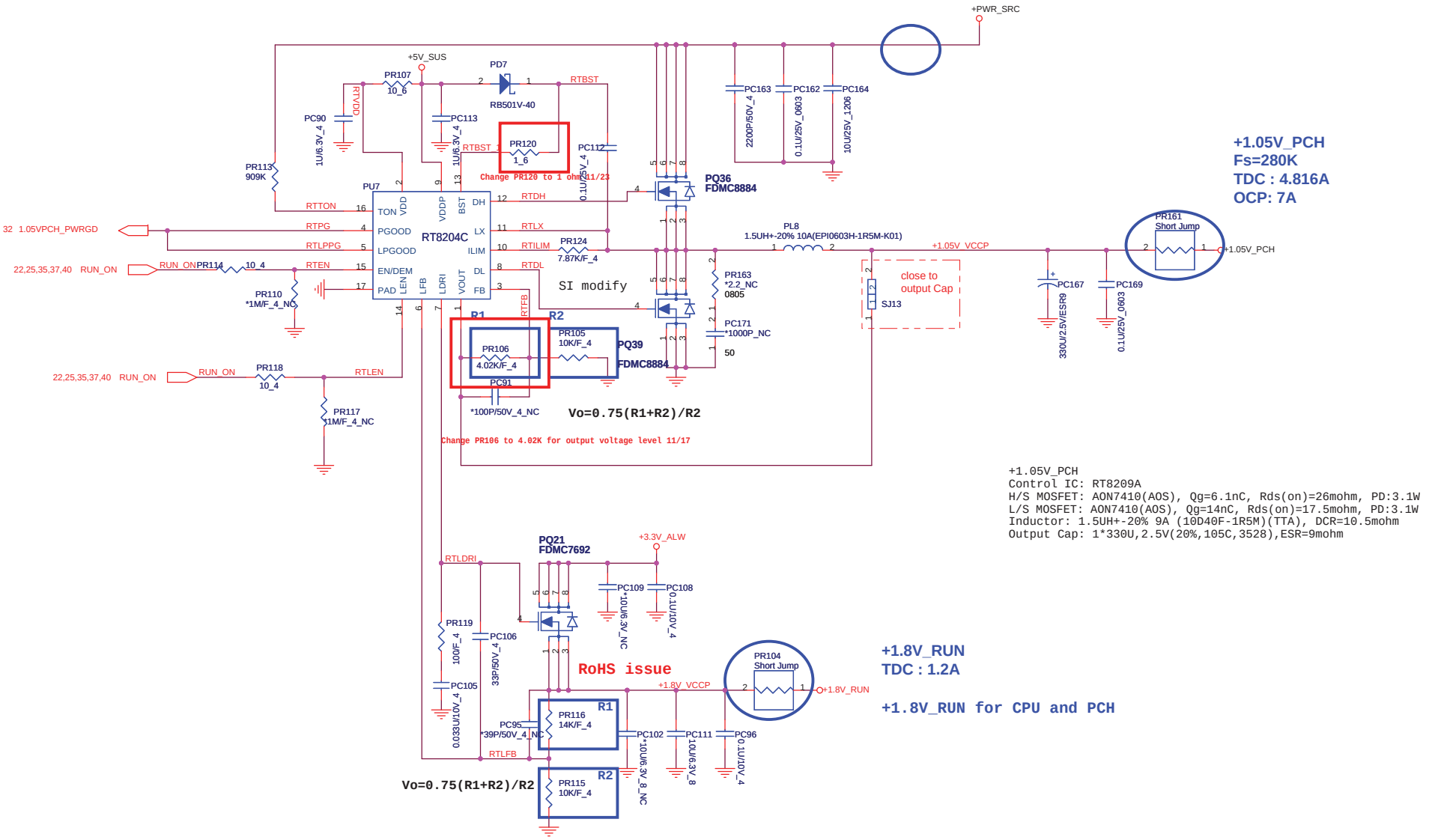
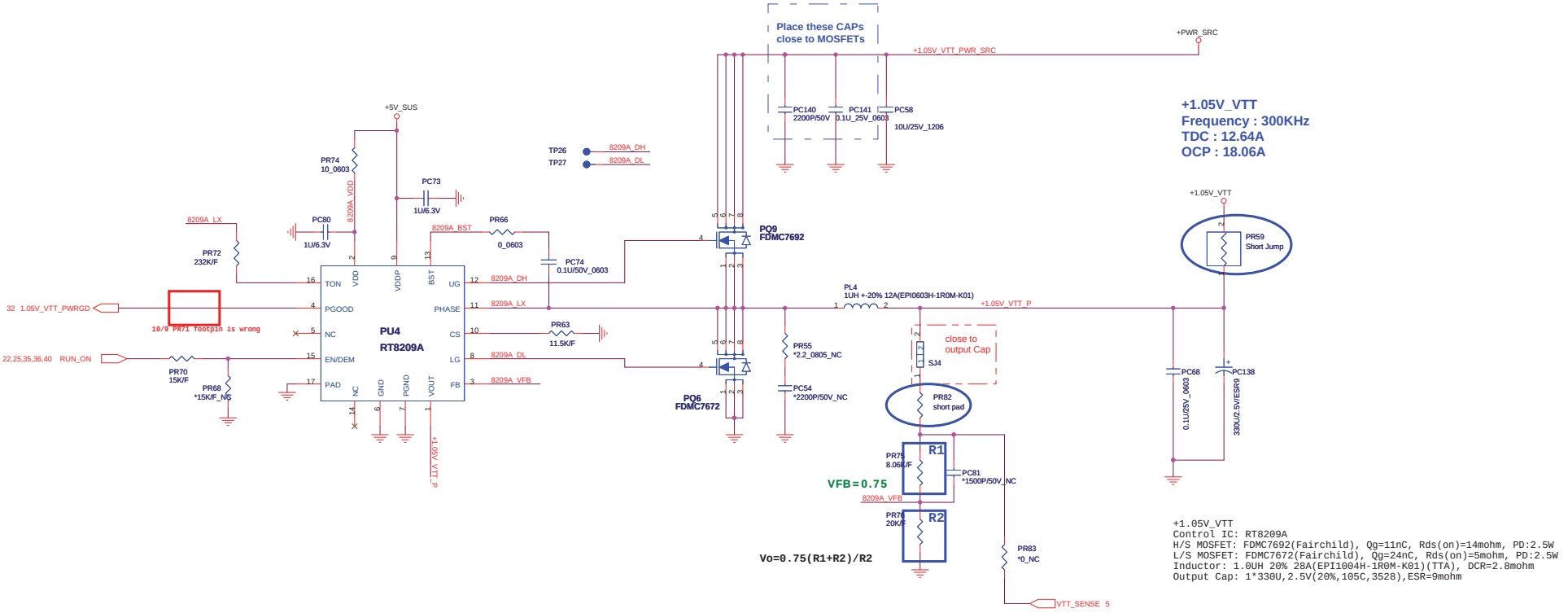


Quanta Computer Inc.

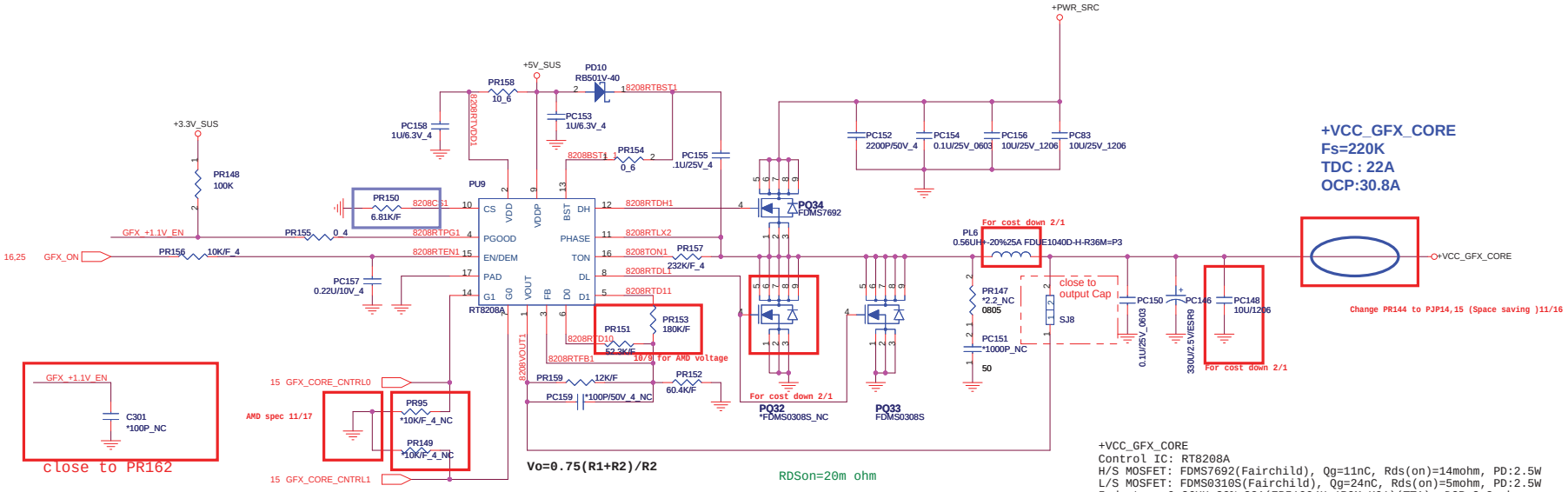
PROJECT : UM8B DIS

Size	Document Number	Rev
	1.05V_PCH	1A
Date:	Wednesday, February 10, 2010	Sheet 36 of 44



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	1.05V_VTT	1A
Date: Wednesday, February 10, 2010	Sheet 37 of 44	



+VCC_GFX_CORE
Fs=220K
TDC : 22A
OCP:30.8A

Vo=0.75(R1+R2)/R2

RDSon=20m ohm

+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U,2.5V(20%,105C,3528),ESR=9mohm

+VCC_GFX_CORE_M92

For M96-LP:

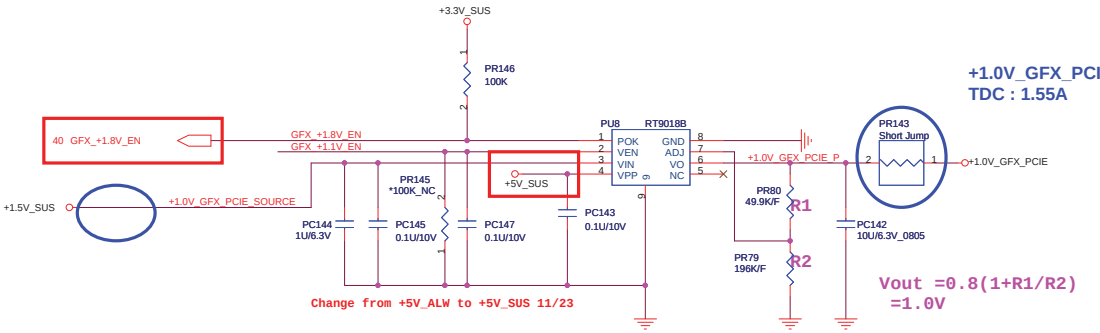
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.0V
HIGH	HIGH	1.05V(N/A)

For Park-XT:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

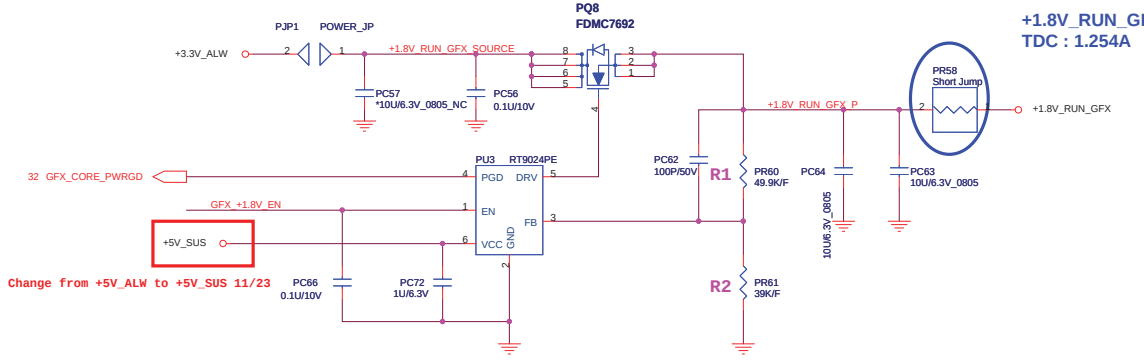
Chagne List:

For Park-XT:	For M96-LP:
PR151:52.3K	PR151:90.9K
PN:CS35232FB10	PN:CS39092FB11
PR79:196K	PR79:133K
PN:CS41962FB01	PN:CS41332FB06



+1.0V_GFX_PCIE
TDC : 1.55A

Vout =0.8(1+R1/R2)
=1.0V



+1.8V_RUN_GFX
TDC : 1.254A

Quanta Computer Inc.
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Size | Document Number: VGA power | Rev 1A
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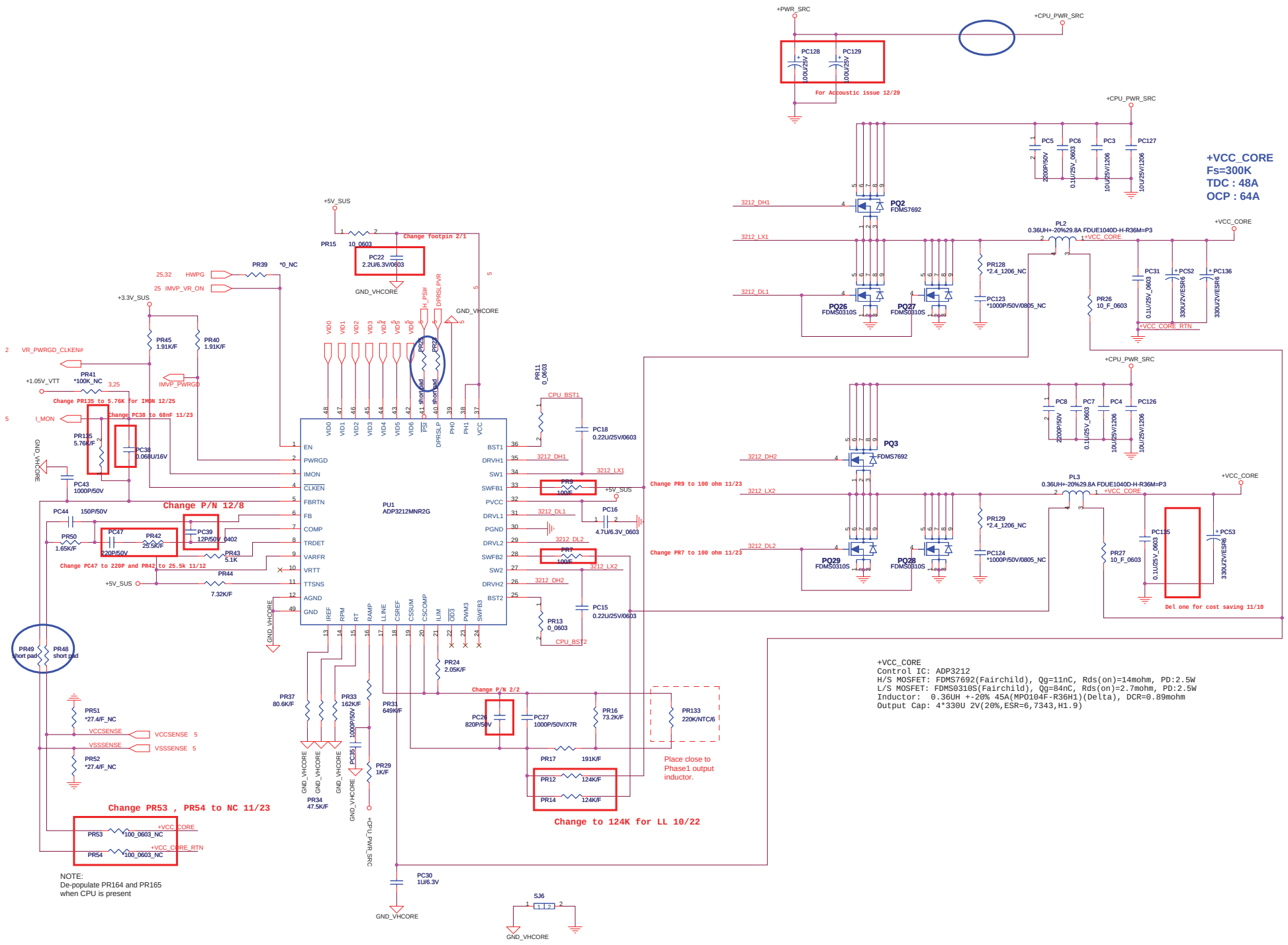

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	CPU_CORE	1A
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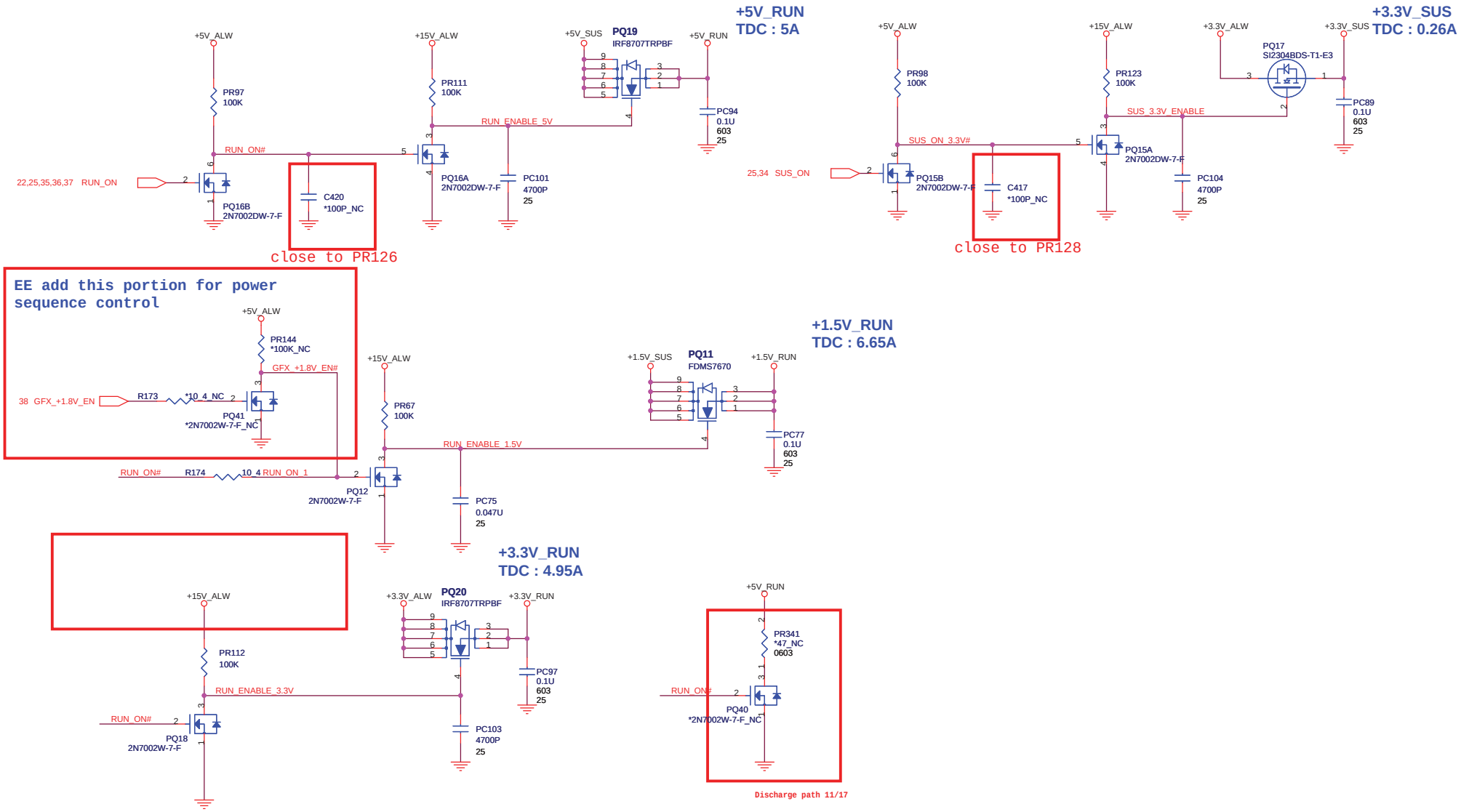

Quanta Computer Inc.		
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Size	Document Number: Run Power Switch	Rev: 1A
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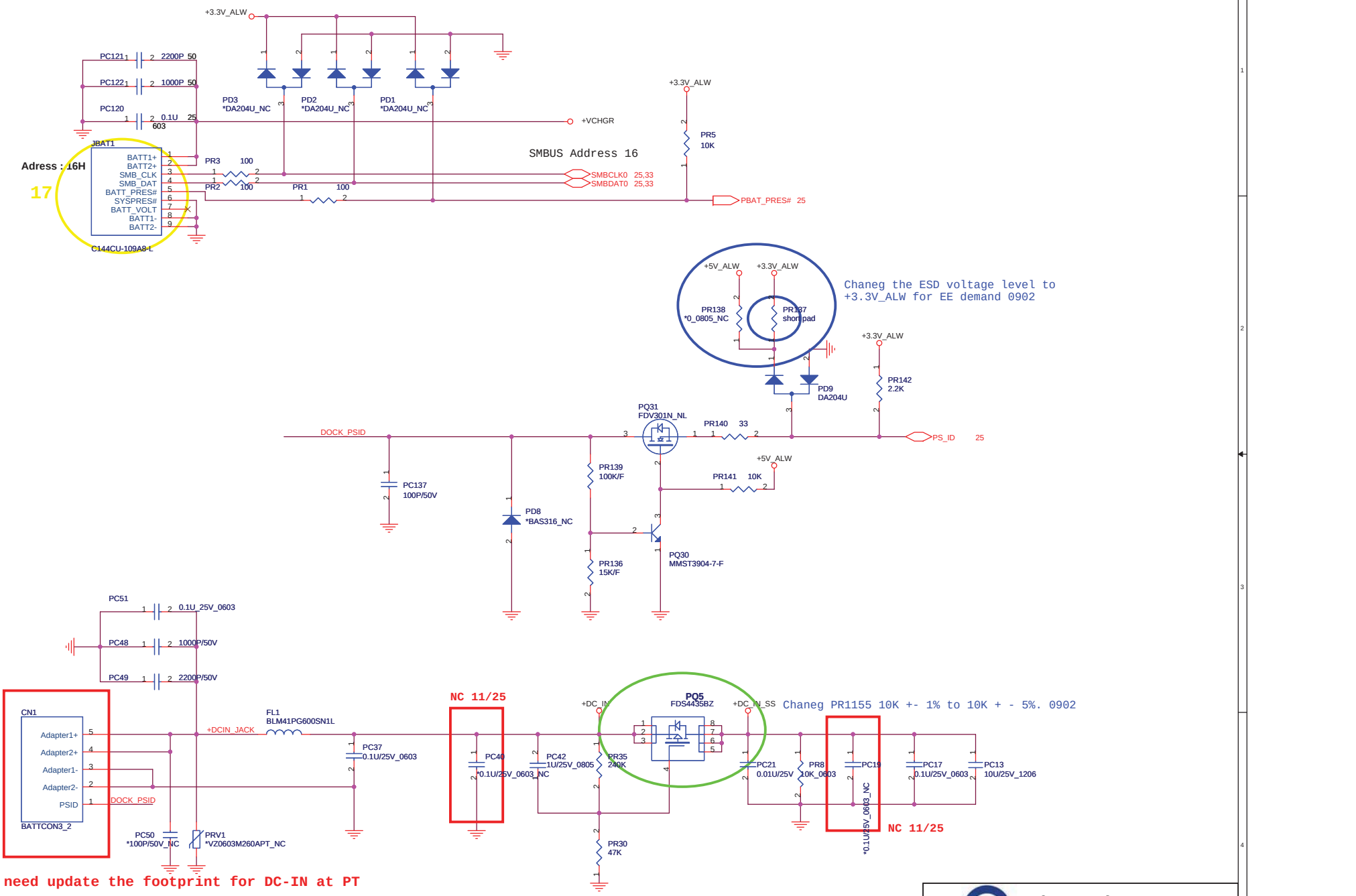

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Batt & DC-IN	1A
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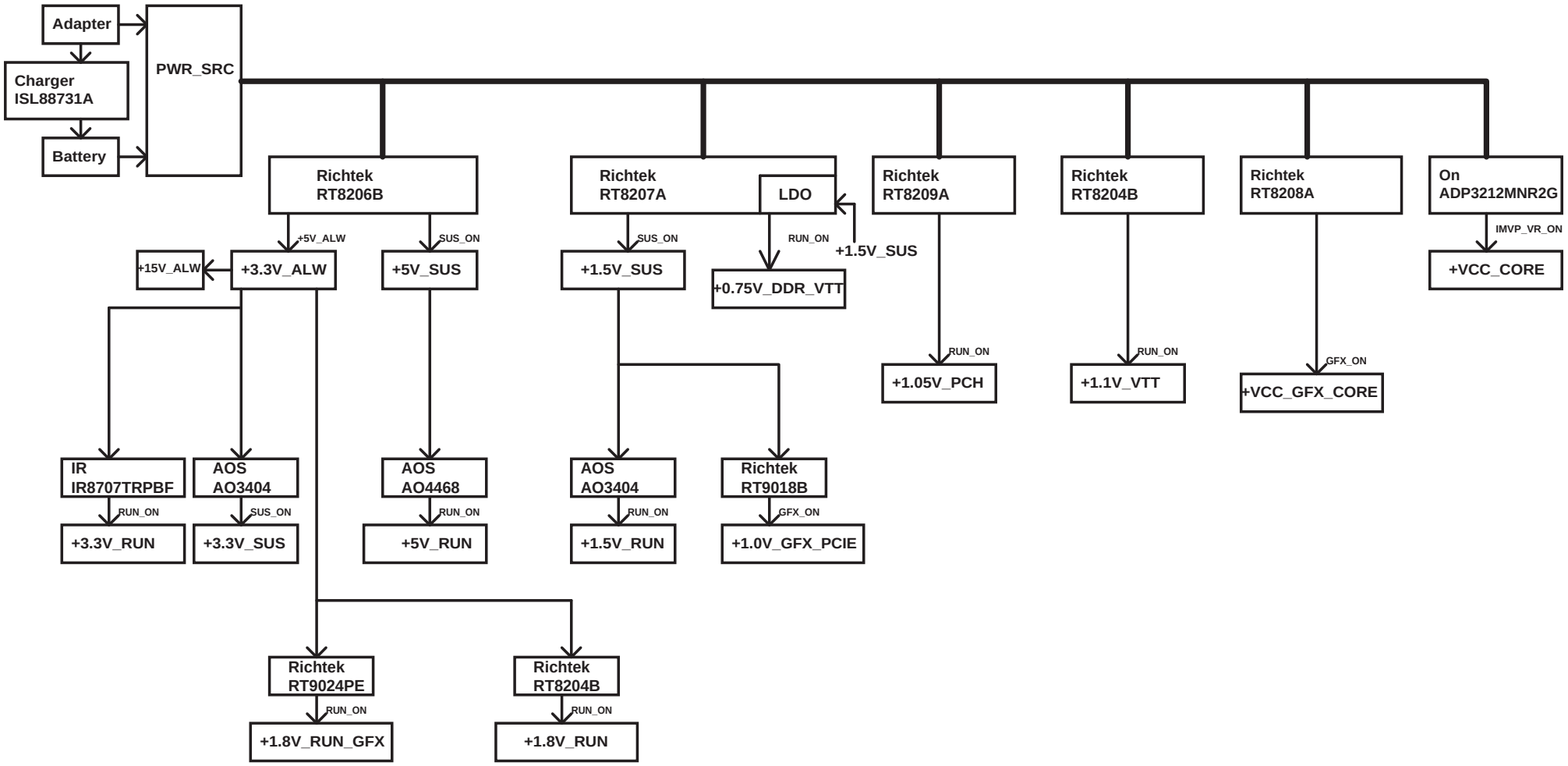
VER : 1A



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Schematic Block Diagram1	1A
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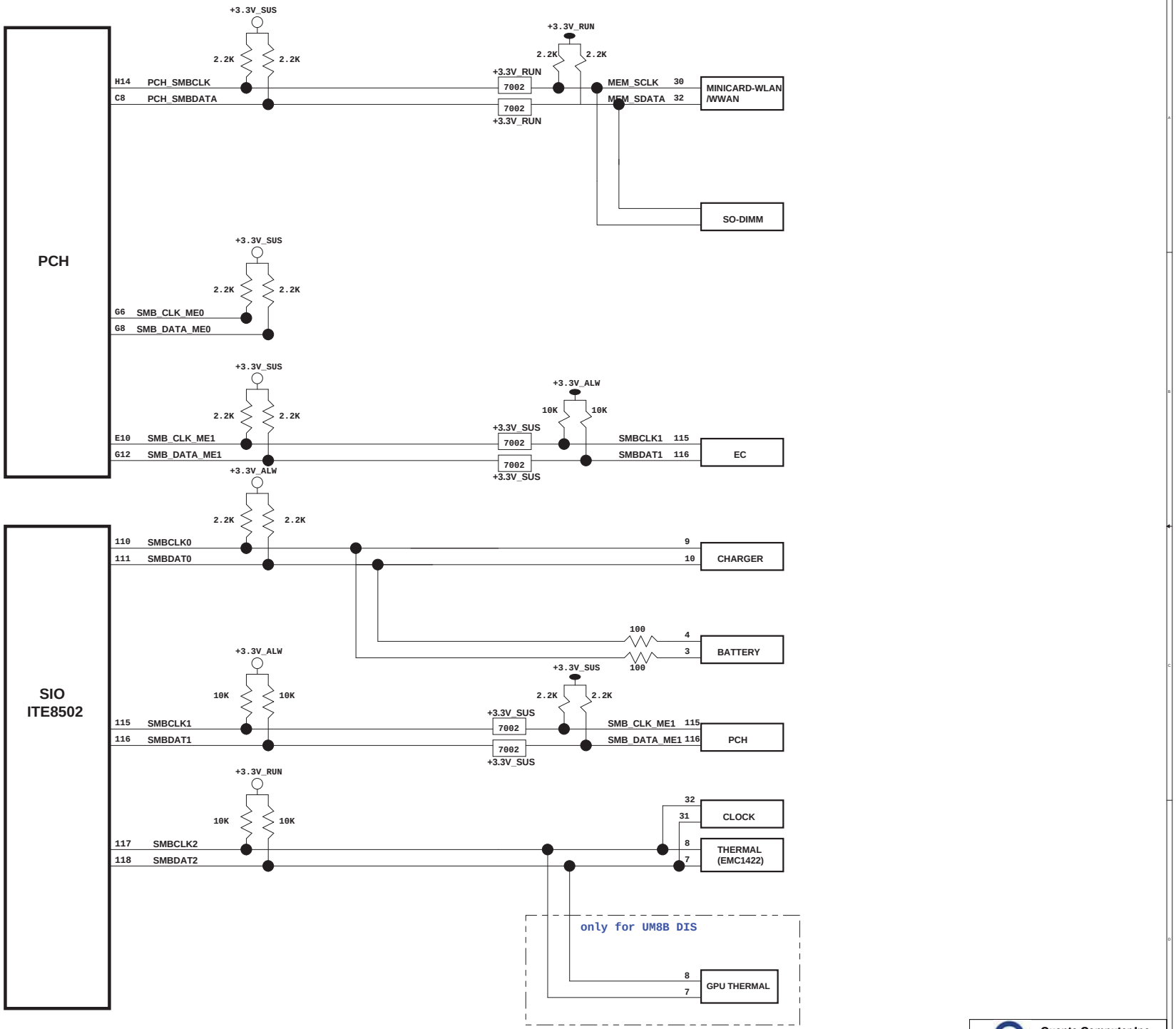

Quanta Computer Inc.
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SMBUS BLOCK
Size | Document Number | Rev 1A
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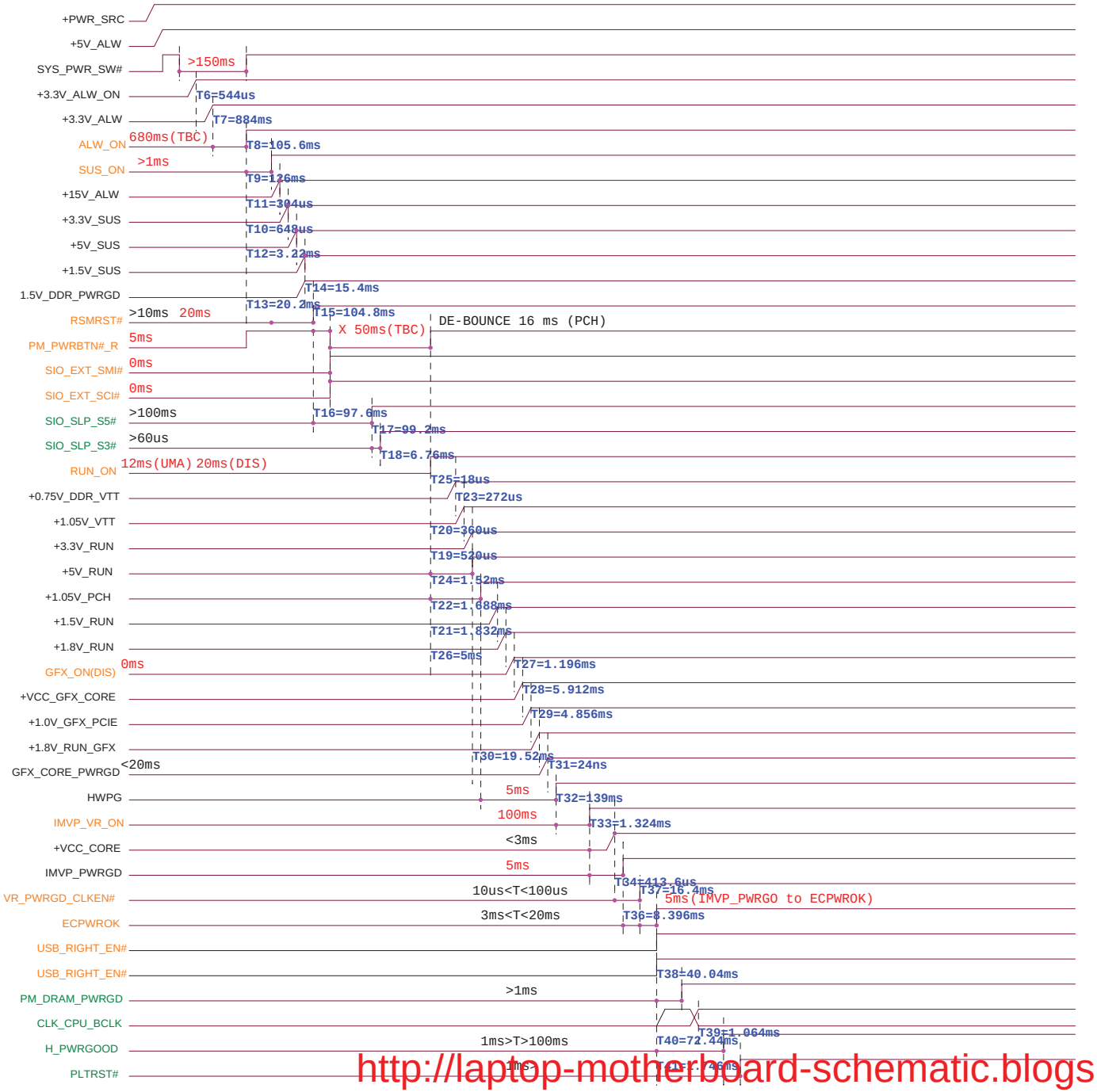
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



Quanta Computer Inc.
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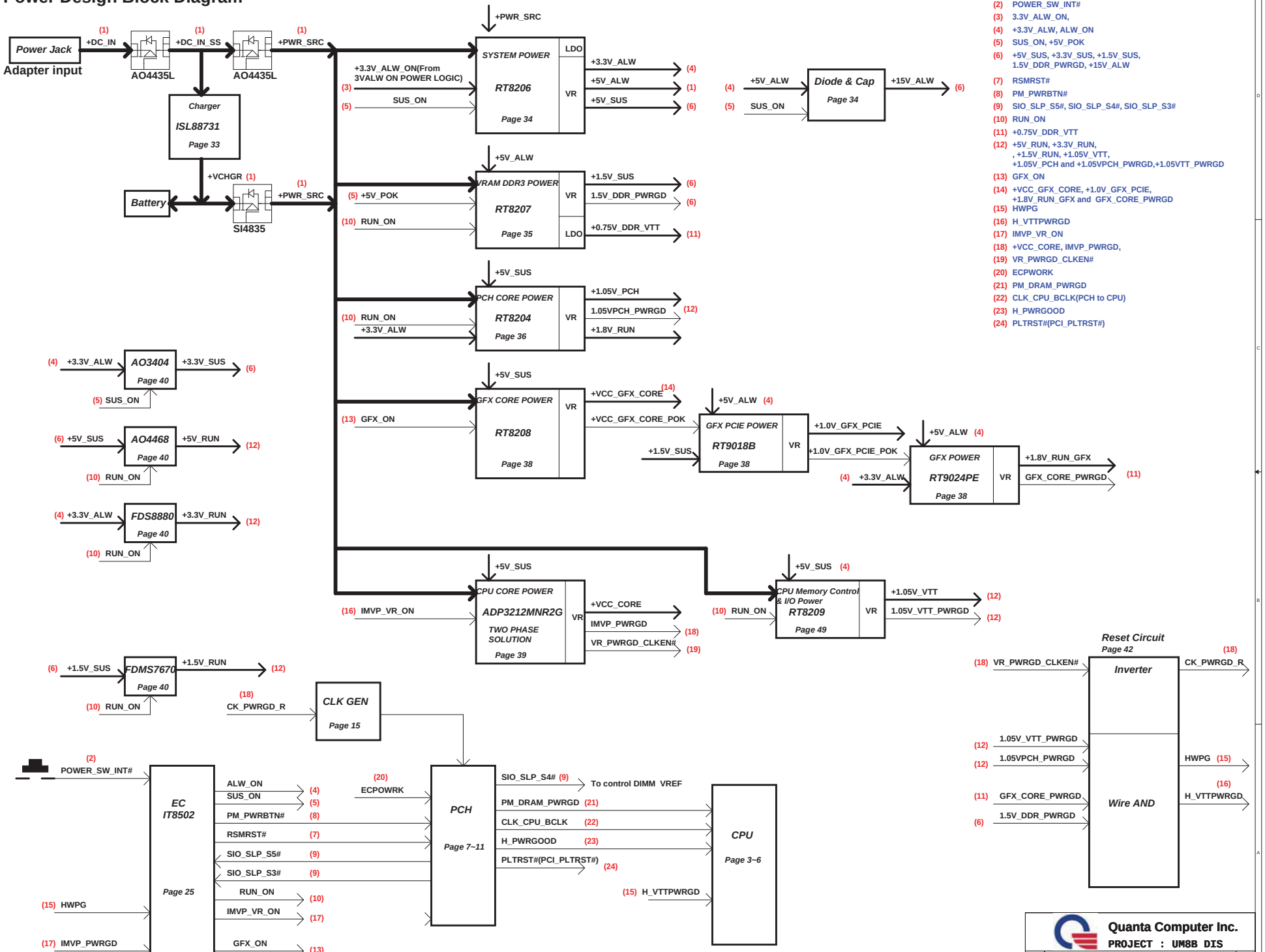
Power Design Block Diagram



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON, +5V_POK
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) RUN_ON
(11) +0.75V_DDR_VTT
(12) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(13) GFX_ON
(14) +VCC_GFX_CORE, +1.0V_GFX_PCIE, +1.8V_RUN_GFX and GFX_CORE_PWRGD
(15) HWPG
(16) H_VTTPWRGD
(17) IMVP_VR_ON
(18) +VCC_CORE, IMVP_PWRGD,
(19) VR_PWRGD_CLKEN#
(20) ECPWORK
(21) PM_DRAM_PWRGD
(22) CLK_CPU_BCLK(PCH to CPU)
(23) H_PWRGOOD
(24) PLTRST#(PCI_PLTRST#)

Quanta Computer Inc.
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Size | Document Number | POWER SEQUENCE BLOCK | Rev 1A
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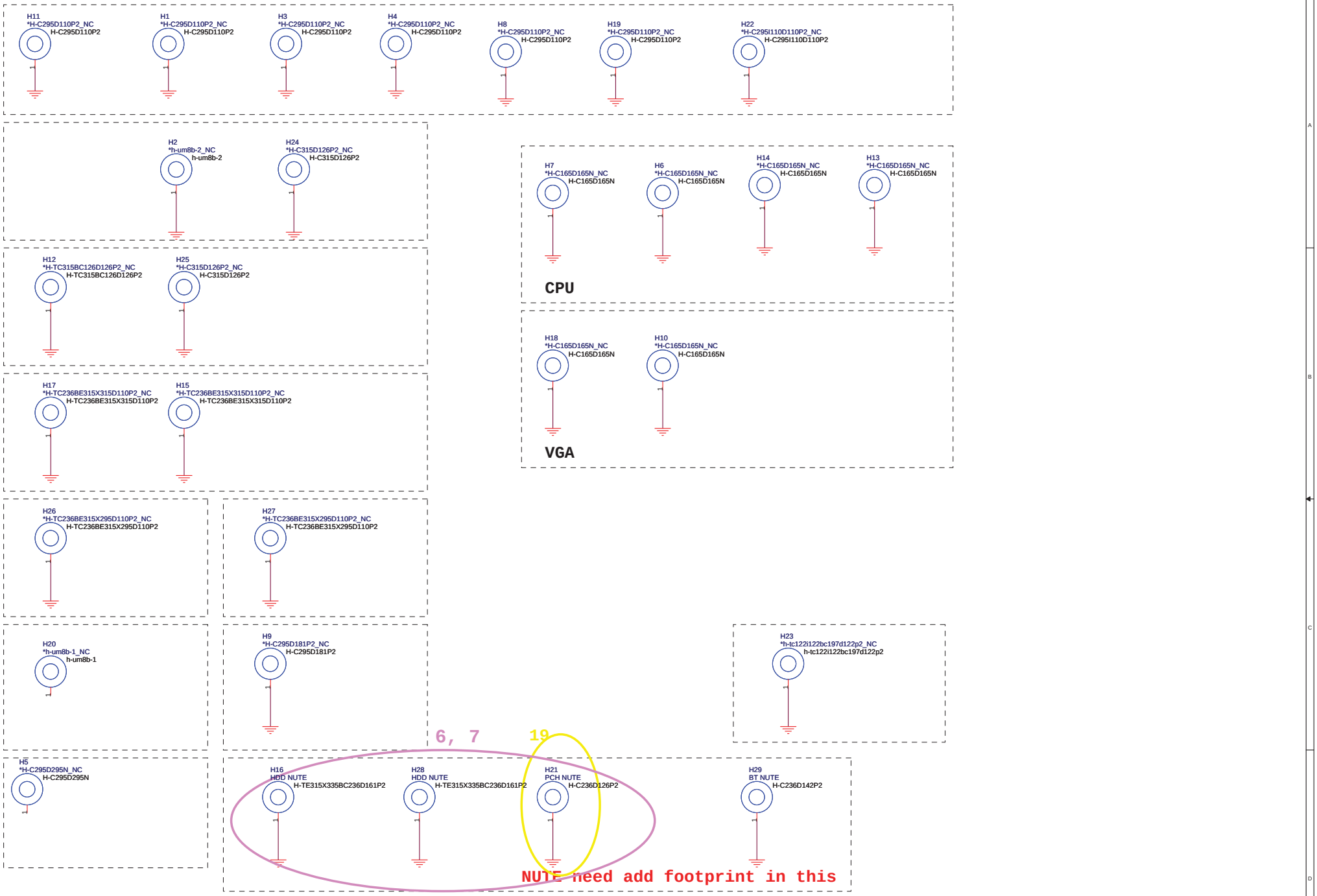

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	PAD&SCREW	1A
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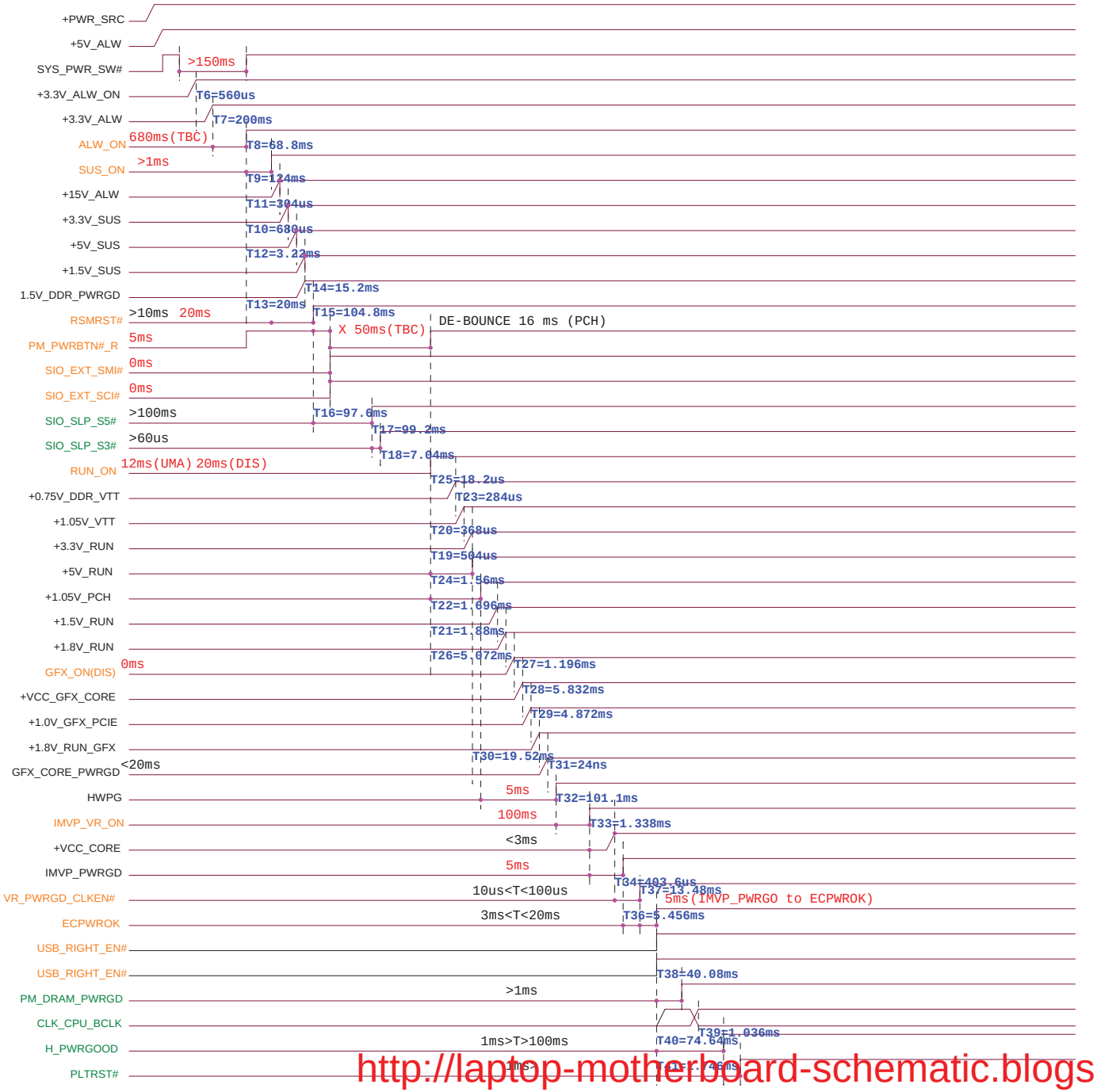
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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