# UM8 UMA SYSTEM DIAGRAM

+3V/+5V PG.34
+1.05V/+1.8V PG.36
CPU Core PG.39
VGA Core/+1.1V PG.38
+1.5V/+0.75V PG.35
+1.05VTT PG.37
UMA VGACORE
Charger PG.33

14.318MHz
CLOCK GEN PG.2

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

FDI
DMI

PI3VDP411LSZDE PG.27 — HDMI — HDMI PG.24
CRT — DB1 — CRT
LVDS — LVDS PG.22

4M ROM PG.26

DB2

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.30

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

LANE0 — WWAN — USB 2.0 PORT5
SATA0 — HDD PG.28
SATA1 — ODD PG.28

PCI-E x 1
LANE6 — LAN Atheros/AR8152 10/100
LANE1 — WLAN — USB 2.0 PORT4

USB2.0 X1 — PORT0,1,7
USB2.0 X1 — PORT0,1,7
Webcam PG.22 — PORT11
USB 2.0
PORT12 — Card Reader RTS5138 PG.23
PORT9 — BT BT365 PG.32

PCI-E x 1
LANE5 — eSATA SN75LVCP412 Combo port PG.27 — USB 2.0 PORT8

LPC

KBC ITE 8502 PG.25
KB PG.28
TP PG.28
1M ROM PG.26

Azalia
AUDIO CODEC
ALC269-GR
Speaker PG.31
HP/MIC
Analog MIC

Stackup
TOP
VCC
IN1
IN2
GND
BOT

Quanta Computer Inc.
PROJECT : UM8 UMA
Size | Document Number: BLOCK DIAGRAM | Rev 1A
Date: Wednesday, February 10, 2010 | Sheet 1 of 46

25mA

+1.05V_PCH — L14 HCB1608KF-181T15_6 — +VDDIO_CLK

C113 0.1U/ 10V/X7R
C109 0.1U/ 10V/X7R
C112 10U/6.3V_8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L13 HCB1608KF-181T15_6 — +VDDSE_CLK

C106 10U/6.3V_8/X5R
C101 0.1U/ 10V/X7R
C110 0.1U/ 10V/X7R
C108 0.1U/ 10V/X7R
C107 0.1U/ 10V/X7R
C111 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

**PDC (Power Cap quantities follow UM3)**

# Check CLK P/N and footprint

U6 — 9LRS3197 — QFN32

| | | | |
|---|---|---|---|
| 5 | VDD_LCD | CPU-0 | 23 |
| 29 | VDD_REF | CPU-0# | 22 |
| 1 | VDD_USB | CPU-1 | 20 |
| 17 | VDD_SRC | CPU-1# | 19 |
| 24 | VDD_CPU | | |
| 18 | VDD_CPU_IO | DOT96T_LPR | 3 |
| 15 | VDD_SRC_IO | DOT96C_LPR | 4 |
| 31 | SDATA | SRC-1 | 13 |
| 32 | SCLK | SRC-1# | 14 |
| 16 | CPU_STOP# | SATA | 10 |
| 30 | REF_0/CPU_SEL | SATA# | 11 |
| 25 | CK_PWRGD/PD#_3.3 | 27MHz_nonSS | 6 |
| | | 27MHz_SS | 7 |
| 27 | XOUT | GND | 33 |
| 28 | XIN | VSS_REF | 26 |
| 9 | VSS_SATA | VSS_CPU | 21 |
| 2 | VSS_USB | VSS_SRC | 12 |
| 8 | VSS_LCD | | |

+VDDSE_CLK

+VDDIO_CLK

25,30 SMBDAT2
25,30 SMBCLK2

+3.3V_RUN — R113 10K — CLK_PCH_14M — R99 33/J_4 — CPU_SEL
8 CLK_PCH_14M — C96 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

CK_PWRGD_R

XTAL_OUT
XTAL_IN

Place within 0.5" of C/G

| | | | | |
|---|---|---|---|---|
| CLK_BUF_BCLKP_R | RP4 | 4 | 3 | 0X2 |
| CLK_BUF_BCLKN_R | | 2 | 1 | |
| CLK_BUF_DREFCLKP_R | RP5 | 2 | 1 | 0X2 |
| CLK_BUF_DREFCLKN_R | | 4 | 3 | |
| CLK_BUF_PCIE_3GPLLP_R | RP6 | 2 | 1 | 0X2 |
| CLK_BUF_PCIE_3GPLLN_R | | 4 | 3 | |
| CLK_BUF_DREFSSCLKP_R | RP7 | 2 | 1 | 0X2 |
| CLK_BUF_DREFSSCLKN_R | | 4 | 3 | |

CLK_BUF_BCLKP 8
CLK_BUF_BCLKN 8
CLK_BUF_DREFCLKP 8
CLK_BUF_DREFCLKN 8
CLK_BUF_PCIE_3GPLLP 8
CLK_BUF_PCIE_3GPLLN 8
CLK_BUF_DREFSSCLKP 8
CLK_BUF_DREFSSCLKN 8

**Discrete only**

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

+3.3V_RUN
R107 *10K_NC
CPU_SEL
R101 10K

| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

**BOM check**

+3.3V_RUN
R106 1K/J_4
CK_PWRGD_R
Q14 FDN357N
39 VR_PWRGD_CLKEN#
R105 *100K/F_4_NC

R8253 => UM7 POP
UM9 DE-POP
0918 check

Y4 14.318MHZ
XTAL_IN — XTAL_OUT
C99 33P/50V_4/NPO
C100 33P/50V_4/NPO

Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Clock Gen(9LRS3197)/HOLES | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 2 of 46 | |

**DPLL_REF_SSCLK/DPLL_REF_SSCLK#:**
**Embedded Display Port PLL Differential Clock in.**

| | DIS | UMA |
|---|---|---|
| DPLL_REF_SSCLK | GND | PCH |
| DPLL_REF_SSCLK# | GND | PCH |

03

U15A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

U15B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

TP48 For ITP Clk

TP49

TP47 TP16

TP14 TP15 TP12 TP13 TP28 TP21 TP20

## CPU THERMTRIP

+3.3V_RUN

R196 *10M_NC

Q12 *2N7002W-7-F_NC

PM_THRMTRIP# 34

H_THERM

*2.2K/J_4_NC R104

C361 *0.1U_NC

Q13 *MMST3904-7-F_NC

+1.5V_SUS

Use a voltage divider with VDDQ (1.5 V) rail (ON in S3) and resistor combination of 1.1K ± (to VDDQ)/3K ± (to GND) to convert to processor VTT level.

R136 1.1K/F

R135 3K/F

C277 *100P_NC

PM_DRAM_PWRGD

## JTAG MAPPING

XDP_TDO_M

R100 0

XDP_TDI_M

XDP_TRST#

R301 51/J_4

Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins. (DS 403777 Page 81)

+1.05V_VTT

H_CATERR# R119 49.9/F_4

H_PROCHOT# R102 49.9/F_4

CPU_PLTRST# R138 *68/J_4_NC

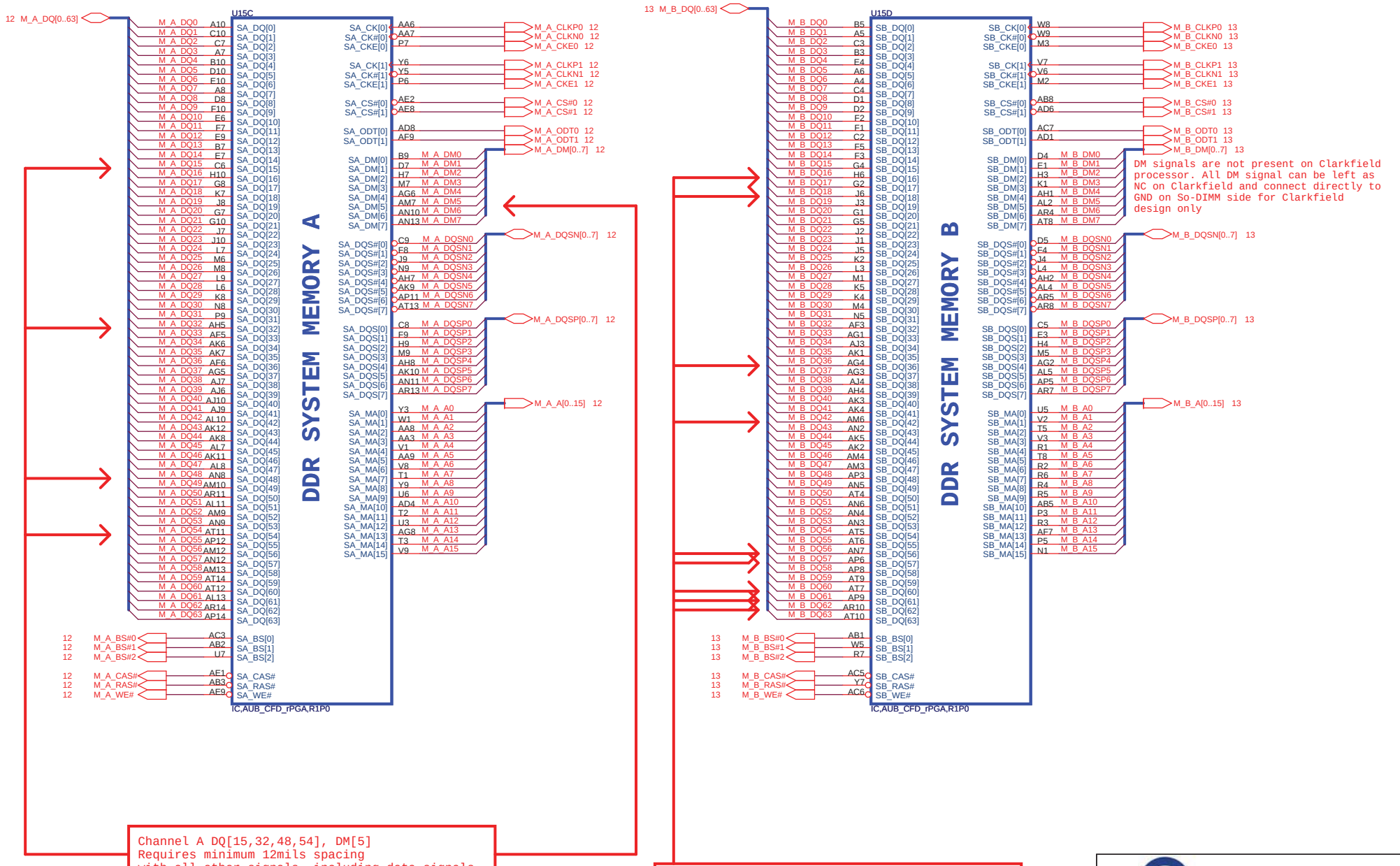
H_CPURST# R304 *68/J_4_NC

C259 *100P_NC

C278 *100P_NC

| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : UM8 UMA | |
| Size | Document Number: PROCESSER 1/4(HOST&PEX) — Rev 1A |
| Date: Wednesday, February 10, 2010 | Sheet 3 of 46 |

# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)






| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : UM8 UMA | | |
| Size | Document Number: PROCESSER 2/4(DDR) | Rev 1A |
| Date: Wednesday, February 10, 2010 | Sheet 4 of 46 | |

Name different with power

+VCC_CORE

U15F

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

18A

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

IC,AUB_CFD_rPGA,R1P0

U15G

GRAPHICS

POWER

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

FDI

PEG & DMI

1.1V

1.8V

2A

IC,AUB_CFD_rPGA,R1P0

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

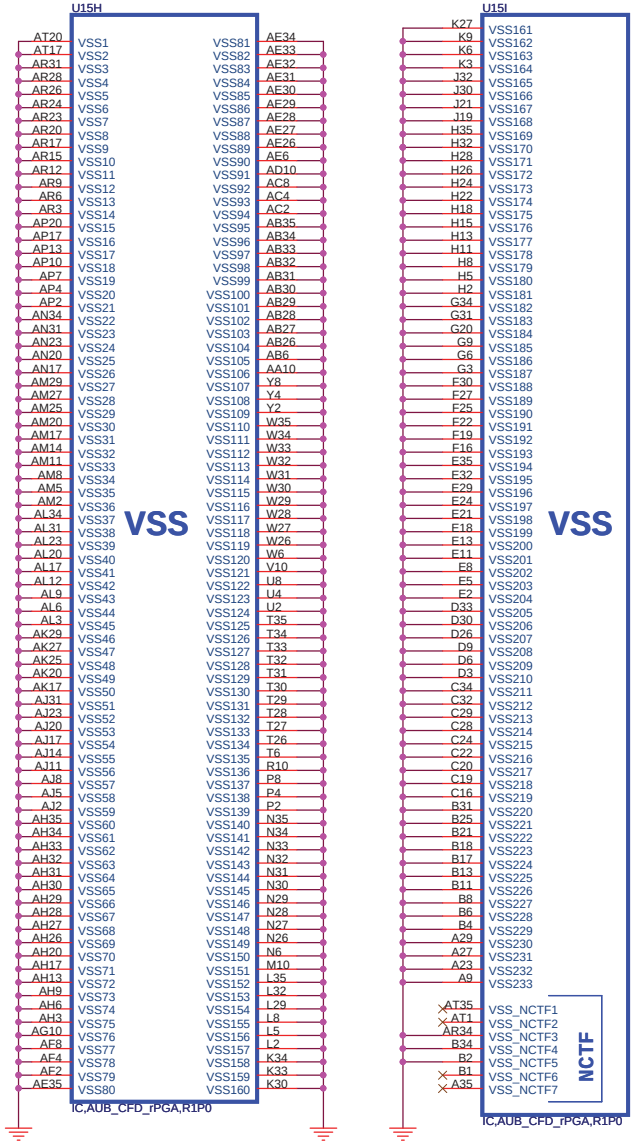
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

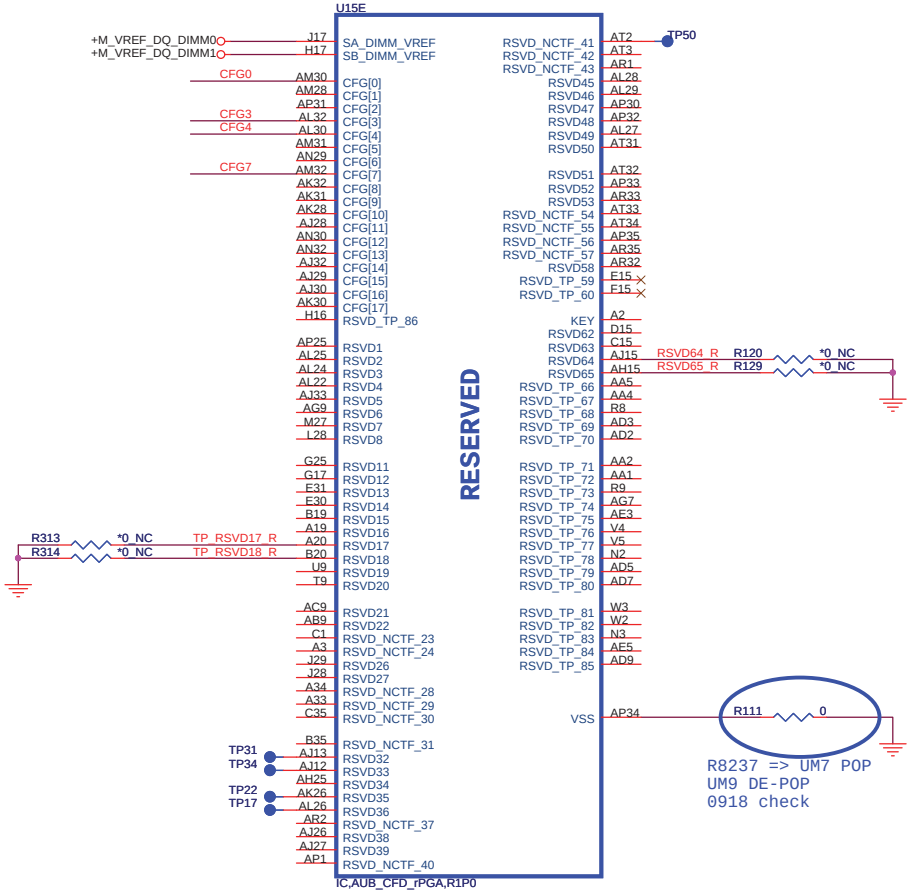
Quanta Computer Inc.
PROJECT : UM8 UMA

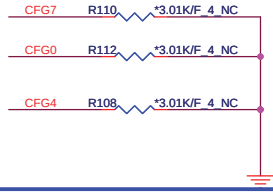
| Size | Document Number | Rev |
|---|---|---|
| | PROCESSER 3/4(POWER) | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 5 of 46 | |

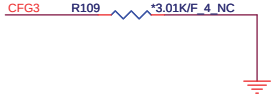
# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)




# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




| | 1 | 0 |
|---|---|---|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed 15 -> 0 , 14 -> 1 |

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PROCESSER 4/4 (GND) | 1A |

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

# IBEX PEAK-M (HDA,JTAG,SATA)

U14A — Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)
SATA: SATA0RXN/RXP, SATA0TXN/TXP, SATA1RXN/RXP, SATA1TXN/TXP, SATA2RXN/RXP, SATA2TXN/TXP, SATA3RXN/RXP, SATA3TXN/TXP, SATA4RXN/RXP, SATA4TXN/TXP, SATA5RXN/RXP, SATA5TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

IbexPeak-M_Rev1_0

C287 18P/50V_4/COG — C288 18P/50V_4/COG — Y5 32.768KHZ — R265 10M/J_4
RTC_X1 B13 — RTC_X2 D13
T25 PAD — RTC_RST# C14
T26 PAD — SRTC_RST# D17
SM_INTRUDER# A16
+RTC_CELL — R266 330K/J_6 — PCH_INVRMEN A14 — T24 PAD
ACZ_BITCLK A30
ACZ_SYNC D29
31 ACZ_SPKR — ACZ_RST# C30
31 ACZ_SDIN0 — G30
F30
E32
F32
B29
ACZ_SDOUT H32
PCH_GPIO33 J30
25 PCH_MELOCK — R339 *0_NC

11

TP37 PCH_JTAG_TCK_BUF M3
TP38 PCH_JTAG_TMS K3
TP39 PCH_JTAG_TDI K1
TP40 PCH_JTAG_TDO J2
TP41 PCH_JTAG_RST# J4
must add test point.

26 SPI_CLK — SPI_CLK BA2
26 SPI_CS0# — SPI_CS0# AV3
TP4
TP43 — SPI_CS1# AY3
26 SPI_SI — SPI_SI AY1
TP6
26 SPI_SO — SPI_SO AV1
TP3
C362 *100P/NPO_NC

20

## Flash Descriptor Security Override

| | |
|---|---|
| GPIO33 | Low = Enabled<br>High = Disabled |

R62 1 — 2 *1K_NC — PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

**Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.**

8

24

ESATA
SATA_RXN4 27
SATA_RXP4 27
SATA_TXN4 27
SATA_TXP4 27

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

SATA_COMP R58 37.4/F_4 — +1.05V_PCH
SATA_LED# — SATA_LED# 29

DG: Place TX cap close to connector
SATA port 2/3 are not support in HM55 . They are only in PM 55

HDD
ODD

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k ) to +V3.3.

R242 10K/J_4 — SATA_LED#

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

+3.3V_RUN — R37 10K/J_4 — SATA_DET0#
R240 10K/J_4 — SATA_DET1#

## iTPM ENABLE/DISABLE

+3.3V_RUN — R263 *1K_NC — SPI_SI

| TPM Function | |
|---|---|
| Enable | Mount |
| Disable | NC (Default) |

## For AUDIO

25,31 ACZ_RST#_AUDIO — R276 33/J_4 — ACZ_RST#
31 ACZ_SDOUT_AUDIO — R273 33/J_4 — ACZ_SDOUT
C292 *10P/50V_4_NC/COG
31 ACZ_SYNC_AUDIO — R274 33/J_4 — ACZ_SYNC
C293 *10P/50V_4_NC/COG
31 ACZ_BITCLK_AUDIO — R275 33/J_4 — ACZ_BITCLK
C294 10P/50V_4/COG

55

+3.3V_RUN — R226 *1K/F_4_NC — ACZ_SPKR

| No Reboot strap. | |
|---|---|
| SPKR | Low = Default.<br>High = No Reboot. |

## RTC

1mA

+RTC_CELL
R267 20K/F_4 — RTC_RST# — C289 1U/6.3V/X5R
R271 20K/F_4 — SRTC_RST# — C291 1U/6.3V/X5R
R268 1M/J_4 — SM_INTRUDER#

# UMA CRT,LVDS&HDMI signals
# IBEX PEAK-M (LVDS,DDI)

U14D — Ibex-M 4 OF 10

LVDS--A: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0..3, LVDSA_DATA0..3
LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0..3, LVDSB_DATA0..3
CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN
SDVO: SDVO_TVCLKINN, SDVO_TVCLKINP, SDVO_STALLN, SDVO_STALLP, SDVO_INTN, SDVO_INTP, SDVO_CTRLCLK, SDVO_CTRLDATA
Digital Display Interface
DISPLAY PORT B: DDPB_AUXN, DDPB_AUXP, DDPB_HPD, DDPB_0N..3N, DDPB_0P..3P
DISPLAY PORT C: DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN, DDPC_AUXP, DDPC_HPD, DDPC_0N..3N, DDPC_0P..3P
DISPLAY PORT D: DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN, DDPD_AUXP, DDPD_HPD, DDPD_0N..3N, DDPD_0P..3P

22,25 PANEL_BKEN — PANEL_BKEN T48
22 ENVDD — ENVDD T47
22 BIA_PWM — Y48
22 LCD_DDCCLK — LCD_DDCCLK AB48
22 LCD_DDCDAT — LCD_DDCDAT Y45
L_CTRL_CLK AB46
L_CTRL_DATA V48
R65 2.37K/F_4 — T4 PAD — LVDS_VBG AP39
T6 PAD — AP41
T3 PAD — AT43
T10 PAD — AT42
22 LCD_ACLK- — AV53
22 LCD_ACLK+ — AV51
22 LCD_A0- — BB47
22 LCD_A1- — BA52
22 LCD_A2- — AY48
T8 PAD — INT_TXLOUTN3 AV47
22 LCD_A0+ — BB48
22 LCD_A1+ — BA50
22 LCD_A2+ — AY49
T9 PAD — INT_TXLOUTP3 AV48
T13 PAD
T12 PAD
31 VGA_BLU — VGA_BLU AA52
31 VGA_GRN — VGA_GRN AB53
31 VGA_RED — VGA_RED AD53
31 DDCCLK — DDCCLK V51
31 DDCDATA — DDCDAT V53
31 VGAHSYNC — R85 33/J_4 — Y53
31 VGAVSYNC — R84 33/J_4 — Y51
R78 1K/D_4 — AD48 AB51

UMA 0.5%
DIS 1%

+3.3V_RUN
R92 2.2K/J_4 — R91 2.2K/J_4
HDMI_SCL T51 — HDMI_SCL 24
HDMI_SDA T53 — HDMI_SDA 24
INT_HDMI_HPD AU38

25

INT_HDMI_TXDN0 BD42 — C76 0.1U/10V_4/X7R — INT_HDMI_TXDN2_C 24
INT_HDMI_TXDP0 BC42 — C74 — INT_HDMI_TXDP2_C 24
INT_HDMI_TXDN1 BJ42 — C73 — INT_HDMI_TXDN1_C 24
INT_HDMI_TXDP1 BG42 — C71 — INT_HDMI_TXDP1_C 24
INT_HDMI_TXDN2 BB40 — C68 — INT_HDMI_TXDN0_C 24
INT_HDMI_TXDP2 BA40 — C66 — INT_HDMI_TXDP0_C 24
INT_HDMI_TXCN AW38 — C62 — INT_HDMI_TXCN_C 24
INT_HDMI_TXCP BA38 — C57 — INT_HDMI_TXCP_C 24

Close to VGA side

35

VGA_BLU — R95 150/F_4 — C592 *22P_NC — 50
VGA_GRN — R83 150/F_4 — C593 *22P_NC — 50
VGA_RED — R94 150/F_4 — C594 *22P_NC — 50

PANEL_BKEN R76 100K/J_4
ENVDD R77 100K/J_4
LCD_DDCDAT R90 2.2K/J_4
LCD_DDCCLK R89 2.2K/J_4
L_CTRL_CLK R86 10K/F_4
L_CTRL_DATA R87 10K/F_4
+3.3V_RUN
+5V_RUN
Q11 2N7002K-T1-E3
INT_HDMI_HPD — R74 100K/J_4 — R96 *0/J_4_NC — HDMI_DET 24

+3.3V_SUS **Res. of TDI near PCH**

R228 *200_NC — R229 *200_NC — R230 *200_NC — R231 20K/F_4_NC
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R245 *100_NC — R246 *100_NC — R247 *100_NC — R248 *10K_NC

**NC all Res. when PCH is production stage.**

**Res. of TDO**
**PCH ES1 stage : NC**
**PCH ES2 stage : pop**

R244 51/J_4 — PCH_JTAG_TCK_BUF

**Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.**

Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PCH 1/5 (SATA,HDA,LPC) | 1A |

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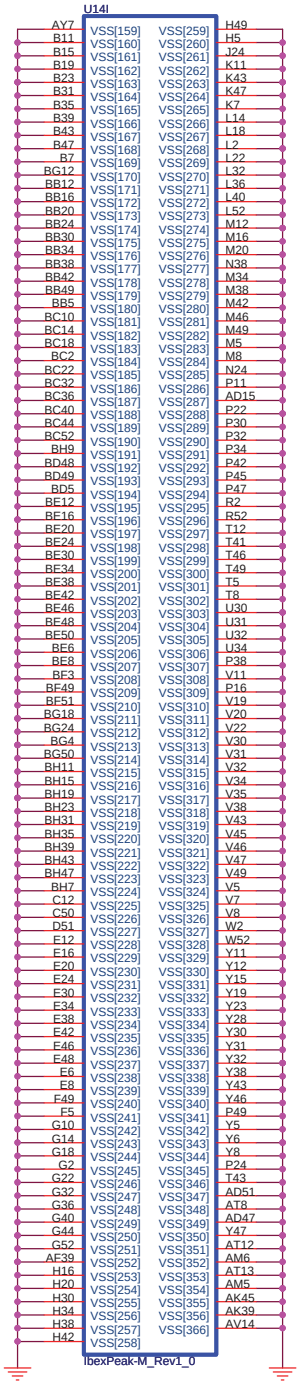
# IBEX PEAK-M (GND)




# IBEX PEAK-M (PCI-E,SMBUS,CLK)

08

U14B

Ibex-M 2 OF 10

PCI-E*

[WLAN] [LAN] MiniWLAN LAN

SMBus (+3V_S5)
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SMB0ALERT# / GPIO60
SMB0CLK
SMB0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75

SMB1 Check R value...
(R8283, R8296)

Controller Link
CL_CLK1
CL_DATA1
CL_RST1#

PEG (+3V_S5)
PEG_A_CLKRQ# / GPIO47

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

Clock Flex (+3V)
CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

Intel recommendation

R8236 => UM7 POP 33ohm
UM9 POP 22ohm
0918 check

55

43

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S (DS 401376 Table2-26)

6

Q8 FDN357N
Q10 FDN357N

| | |
|---|---|
| UMA | POP Y8201, C8411, C8412 and R8401, de-POP R8999 for Internal GFX |
| DIS | de-POP Y8201, C8411, C8412 and R8401, POP R8999 for Internal GFX |

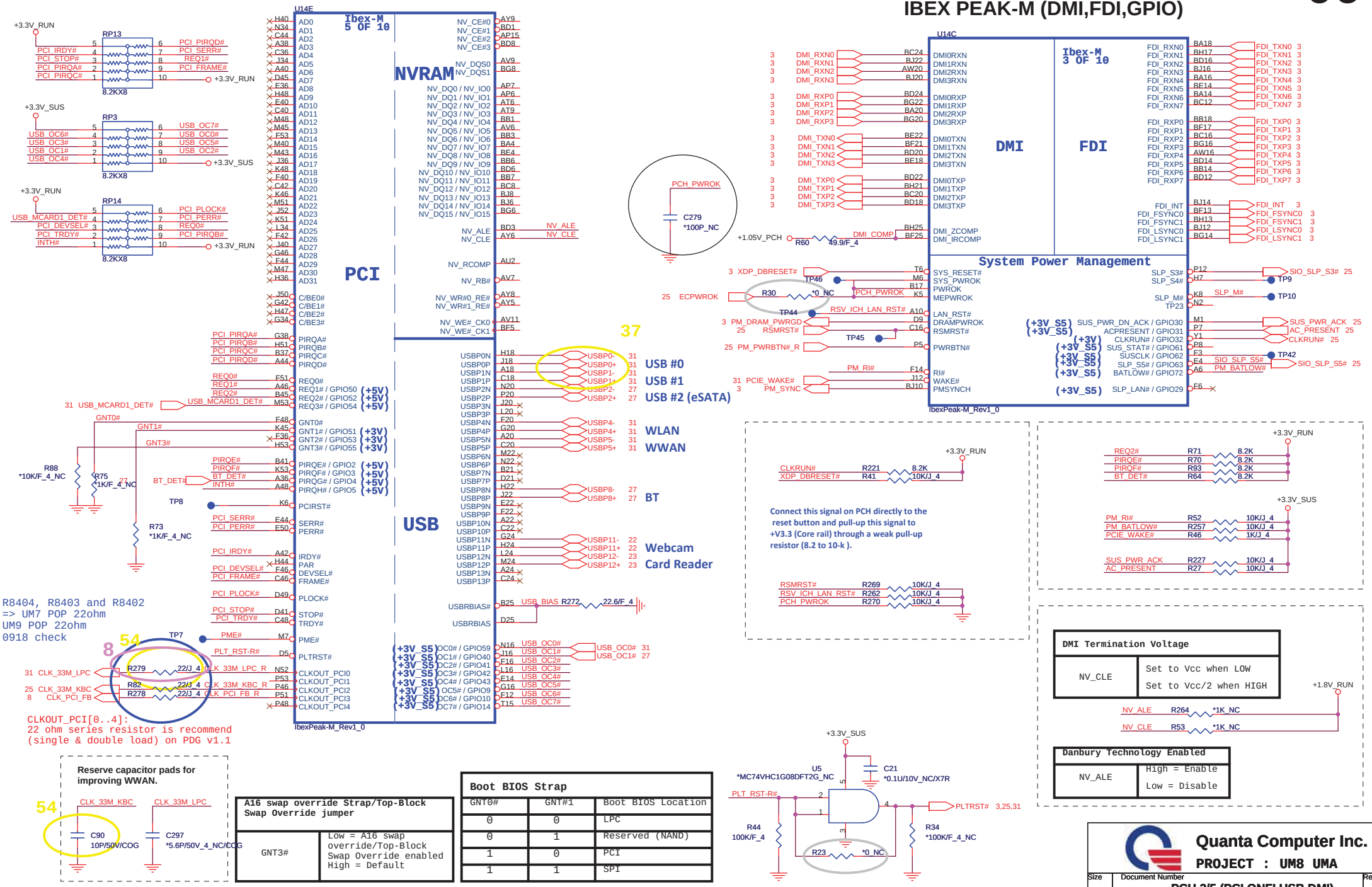
Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PCH 2/5 (PCIE, SMBUS, CK) | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 8 of 46 | |

# IBEX PEAK-M (PCI,USB,NVRAM)

# IBEX PEAK-M (DMI,FDI,GPIO)

09

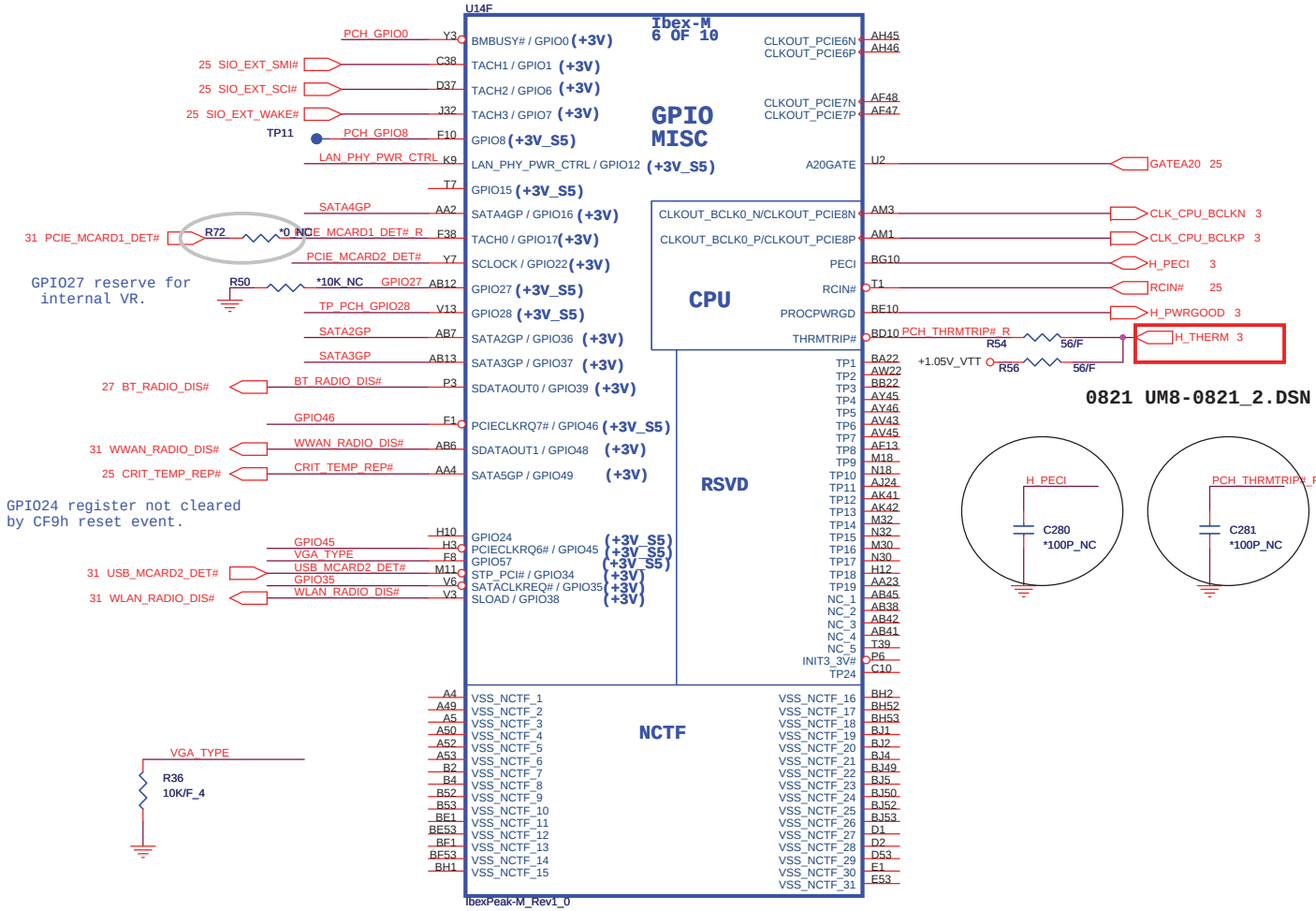





Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PCH 3/5 (PCI,ONFI,USB,DMI) | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 9 of 46 | |

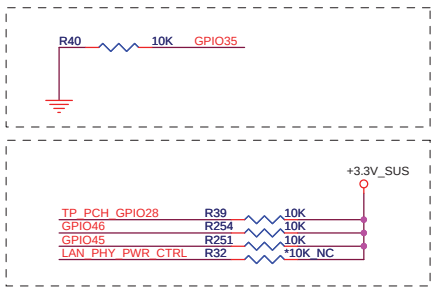
# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

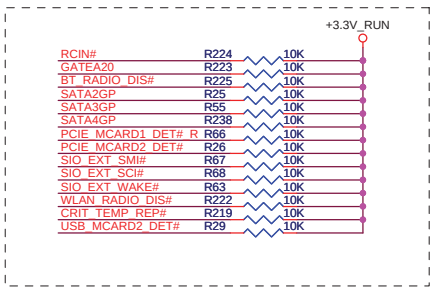


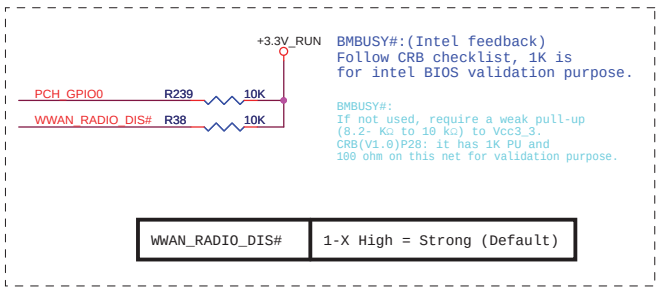

0821 UM8-0821_2.DSN




# IBEX PEAK-M (GND)

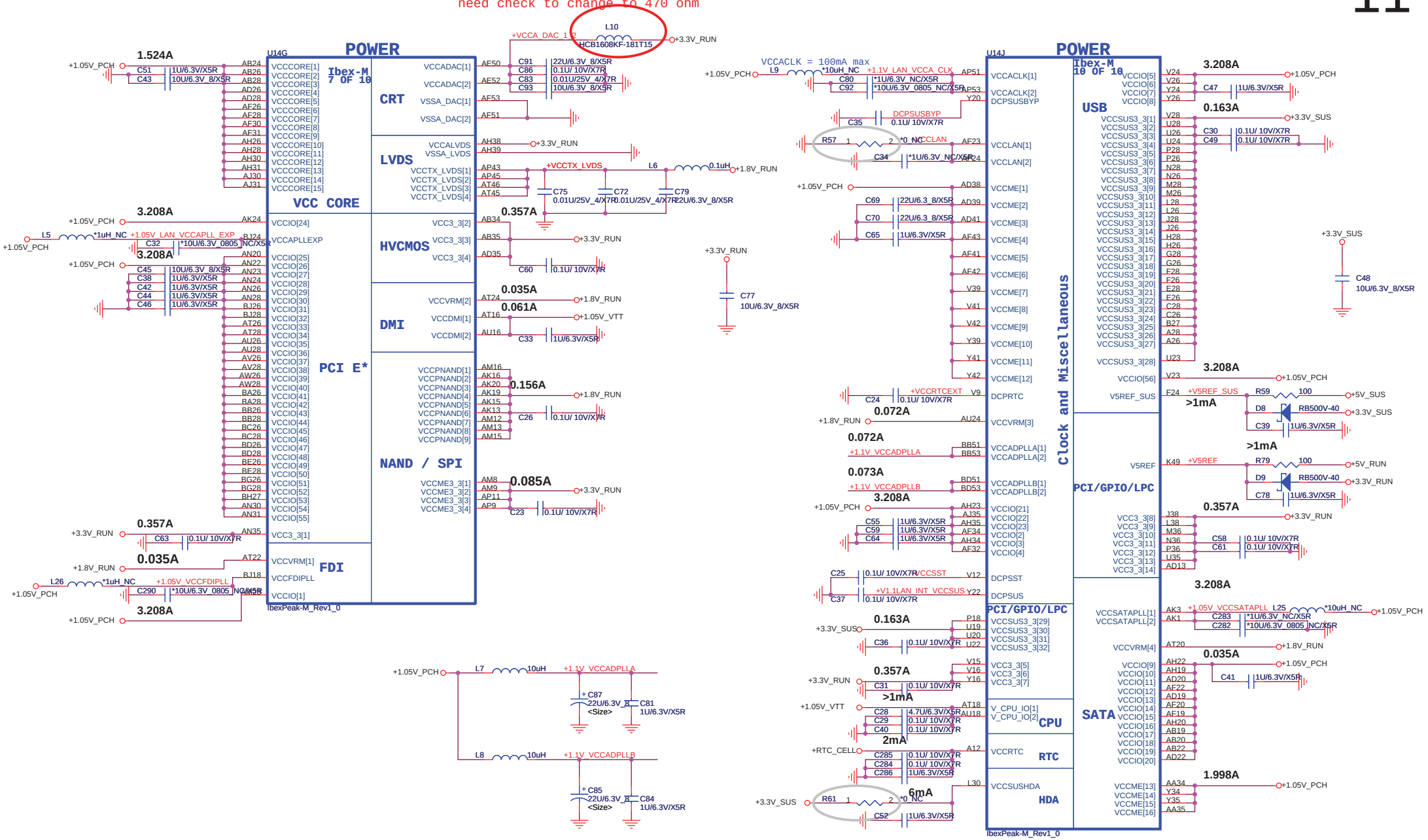



Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PCH 4/5 (GPIO & Strap) | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 10 of 46 | |

# Cap quantities follow UM3

need check to change to 470 ohm



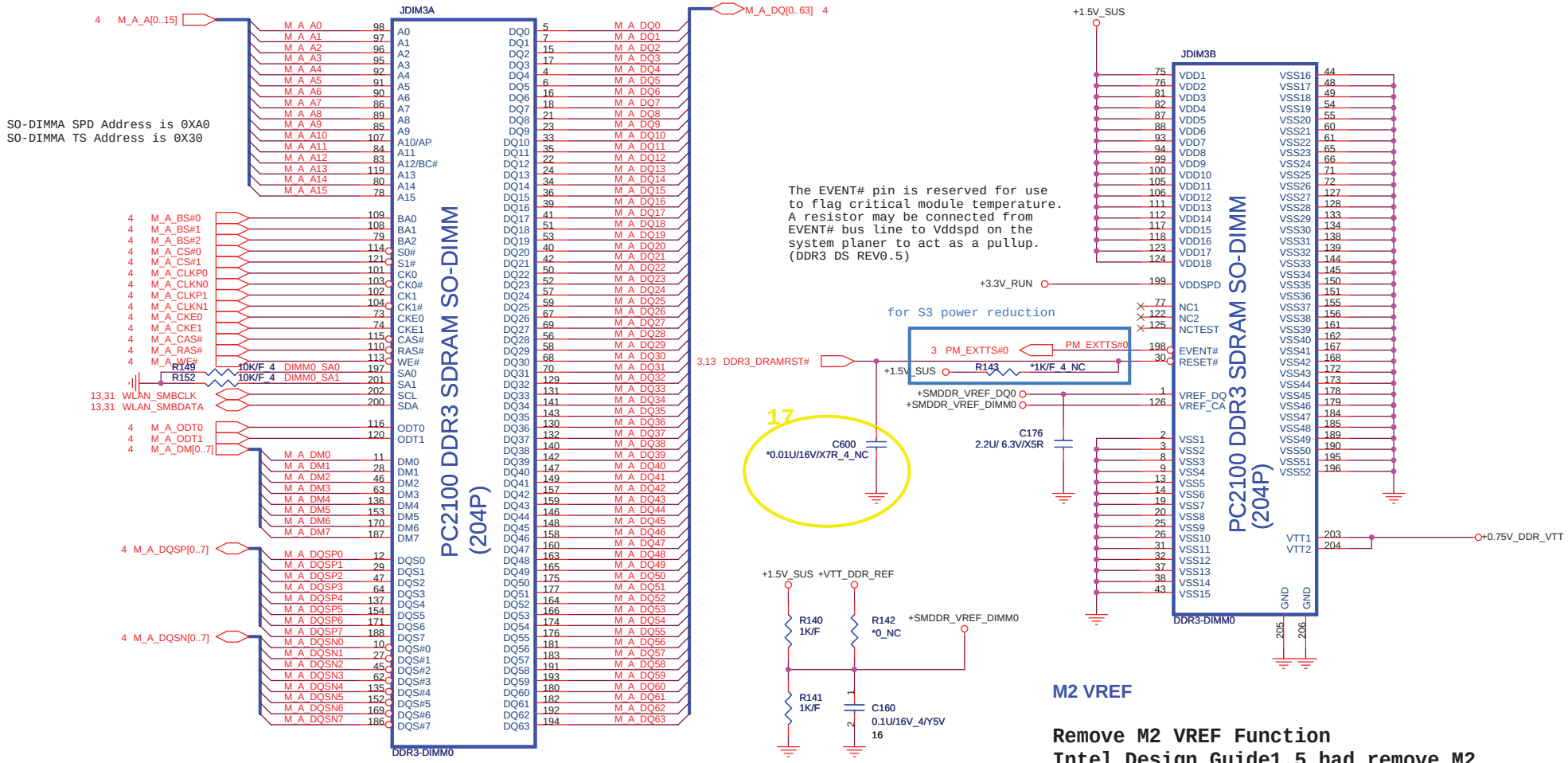



Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | PCH 5/5 (POWER) | 1A |

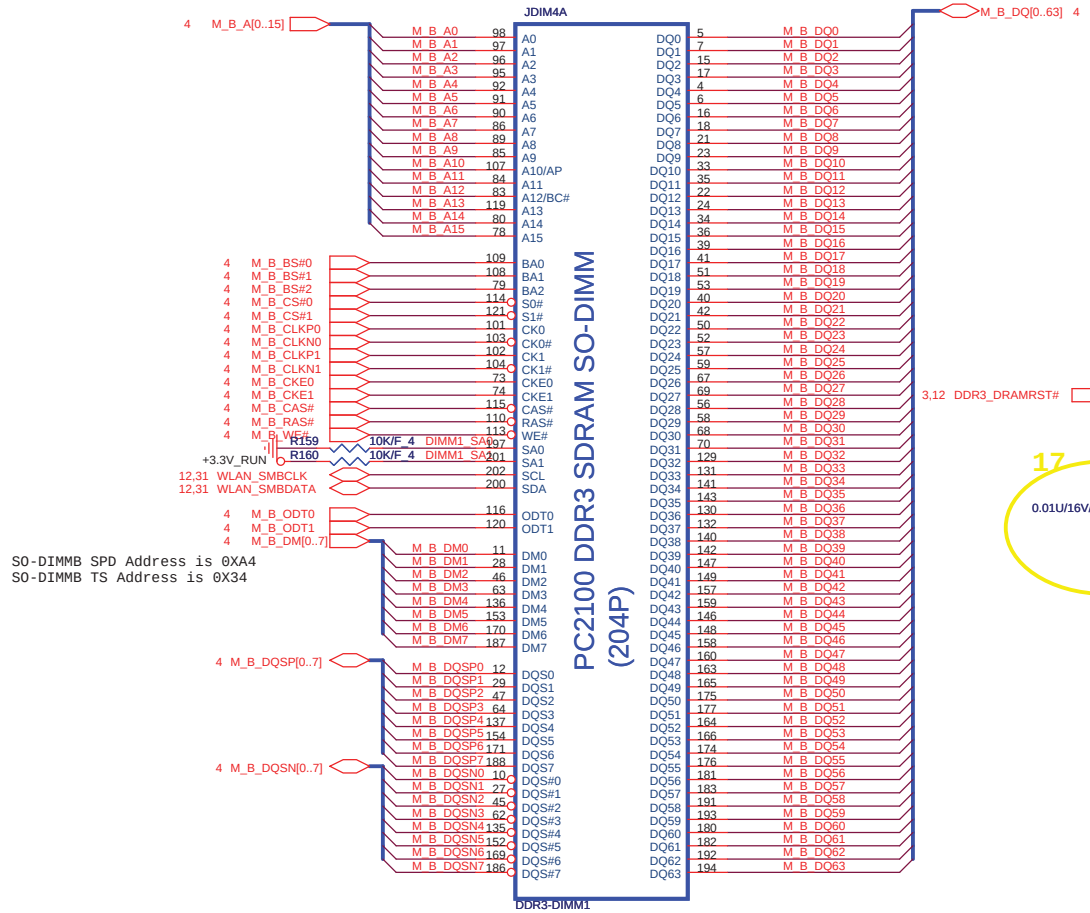
Date: Wednesday, February 10, 2010 Sheet 11 of 46

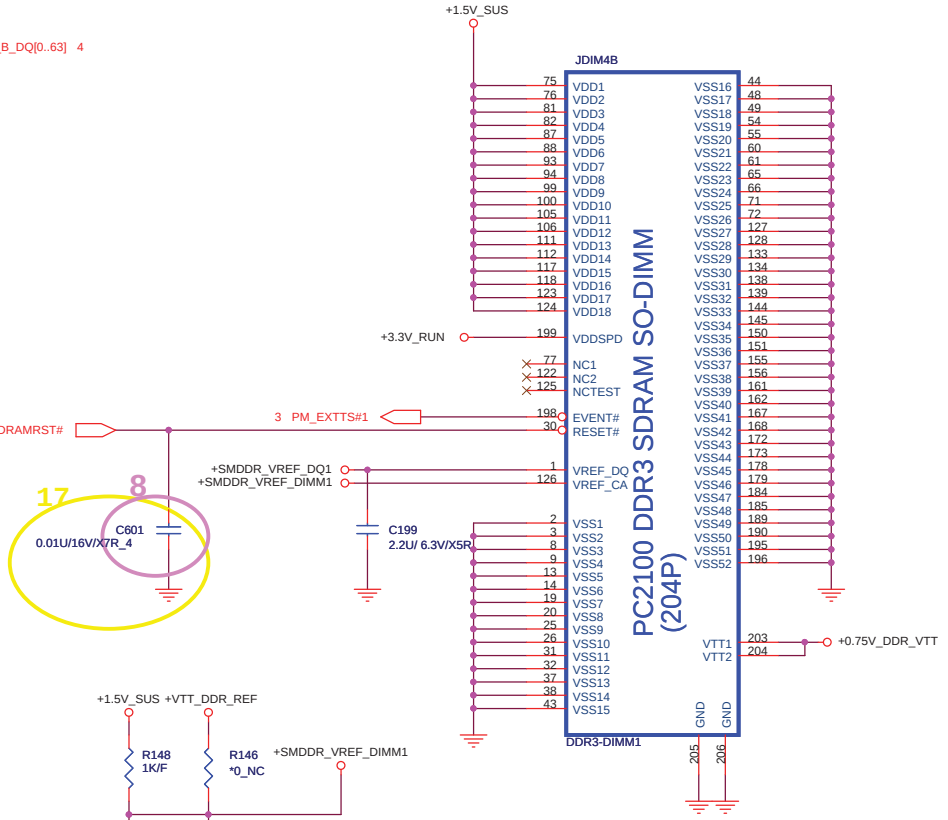



Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 DIMM-0 | 1A |

Date: Wednesday, February 10, 2010 Sheet 12 of 46



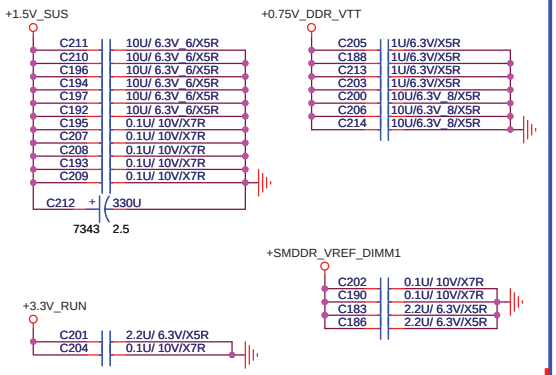




**Remove M2 VREF Function**
**Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)**

**M3 => support for Clarksfield processor**

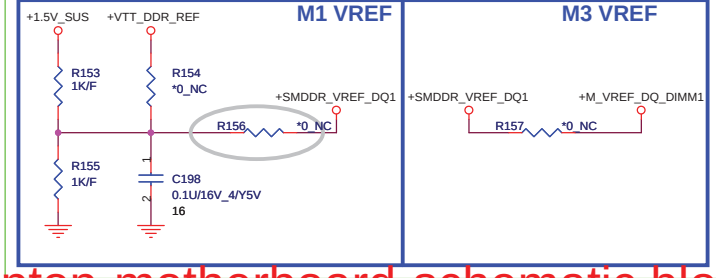
## Place these Caps near So-Dimm1.

**Some Projects replace 10UF 0805 by 4.7UF 0603**
**It can cost down 30%**




Wait Victor check

for arrandal nc, for clesfied connect




Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 DIMM-1 | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 13 of 46 | |

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

Date: Wednesday, February 10, 2010 Sheet 14 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

Date: Wednesday, February 10, 2010 Sheet 15 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 16 of 46 | |

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

Date: Wednesday, February 10, 2010 Sheet 17 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

Date: Wednesday, February 10, 2010 Sheet 18 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 19 of 46 | |

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

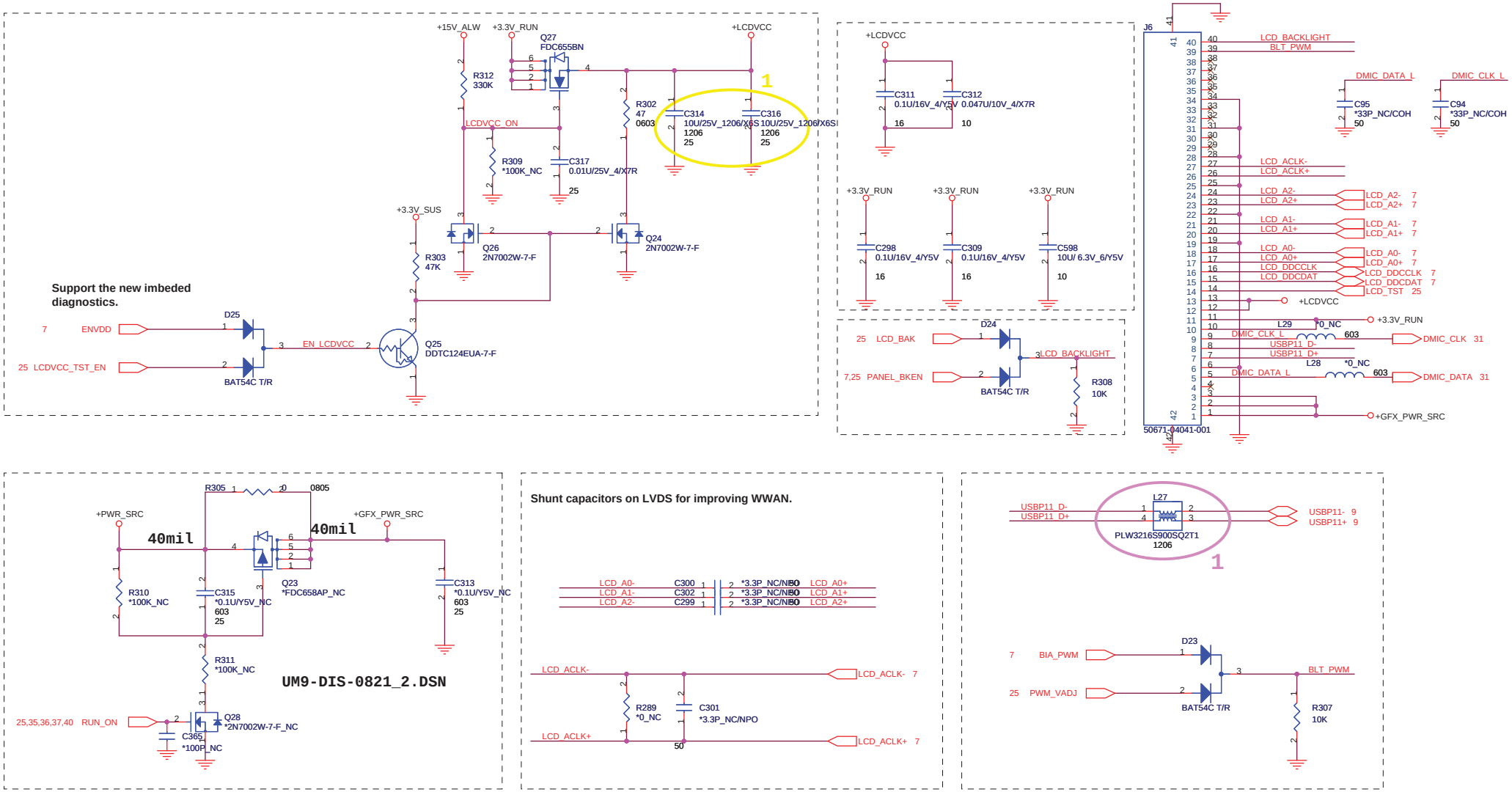
Date: Wednesday, February 10, 2010 Sheet 20 of 46

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

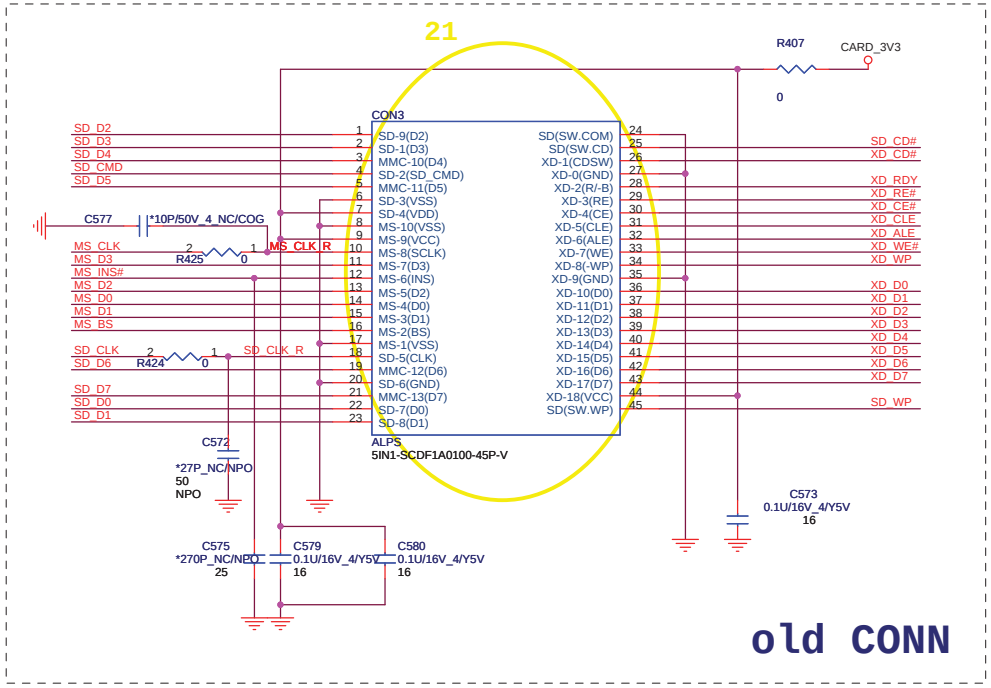
Date: Wednesday, February 10, 2010 Sheet 21 of 46

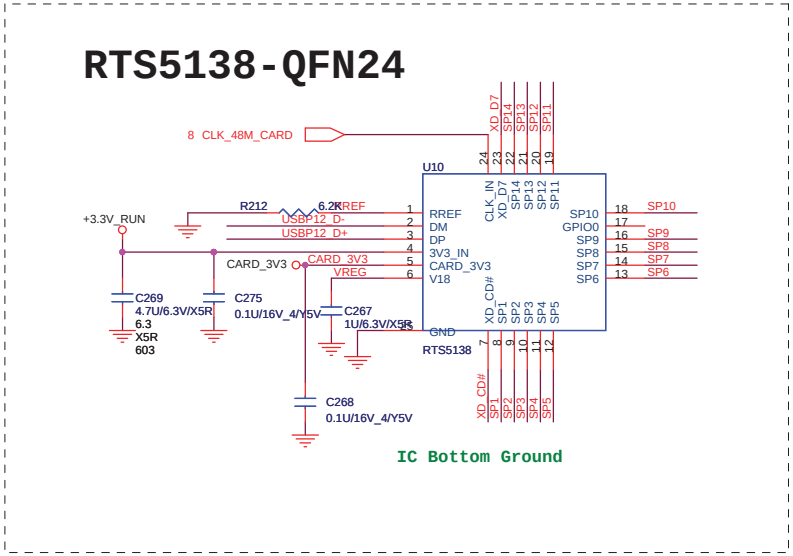


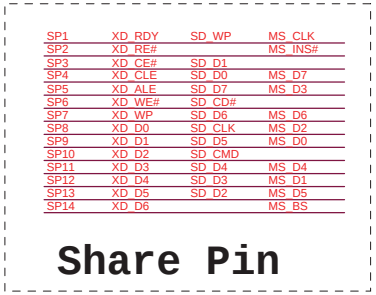

Quanta Computer Inc.

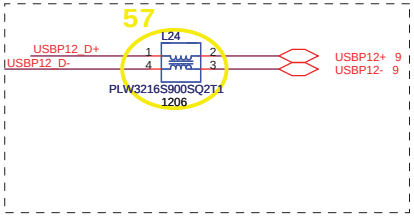
PROJECT : UM8B DIS

| Size | Document Number | Rev |
|---|---|---|
| | LCD CONN | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 22 of 46 | |



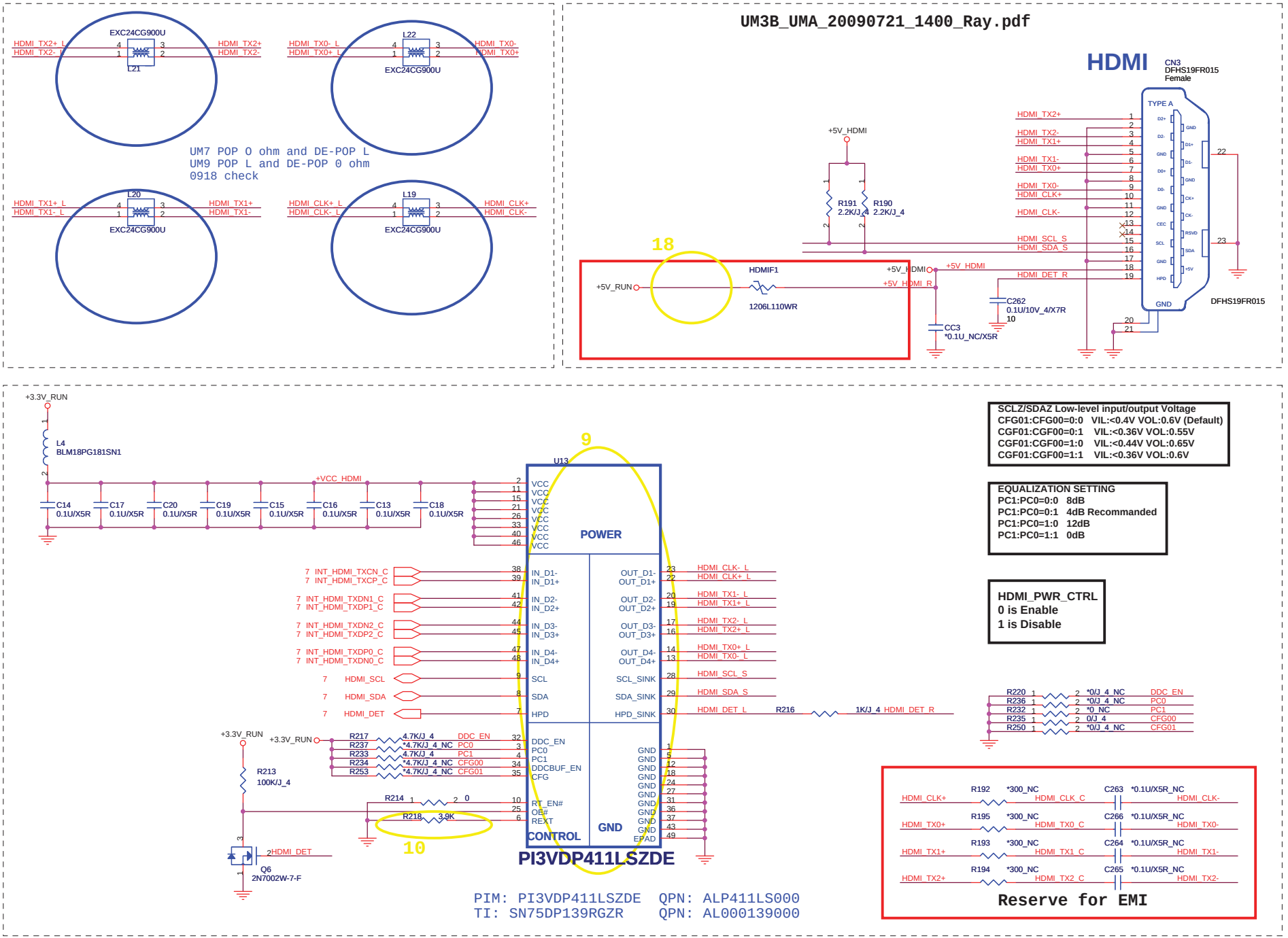




Quanta Computer Inc.
PROJECT : UM8B DIS

| Size | Document Number | Rev |
|---|---|---|
| | Card Reader(RST5138) | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 23 of 46 | |



UM3

U8

ITE8502E
LQFP-128L

KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO

Place these caps close to ITE8502.

Charge and BAT

PCH

LAN, Clock Thermal IC

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

32KHz Clock.

Check

UM7 POP 2.2k
UM9 POP 10k
0918 check

UM7 DE-POP
UM9 POP
0918 check

Madison
Discrete
Park
UMA

VGA_TYPE
VGA_IDENTIFY

| | LCD_SIZE_ID (99) | LCD_SIZE_ID2 (107) |
|---|---|---|
| 13" | 0 | 0 |
| 14" | 1 | 0 |
| 17" | 0 | 1 |

| BID1 | USB_RIGHT_EN# | UM9(UMA) | UM9C (Dis) |
|---|---|---|---|
| 0 | 0 | SSI (X00) | SSI (X00) |
| 0 | 1 | PT (X01) | PT (X01) |
| 1 | 0 | ST (X02) | ST (X02) |
| 1 | 1 | QT (A00) | QT (A00) |
| 0 | 0 | (A01) | (A01) |

Quanta Computer Inc.
PROJECT : UM8 UMA

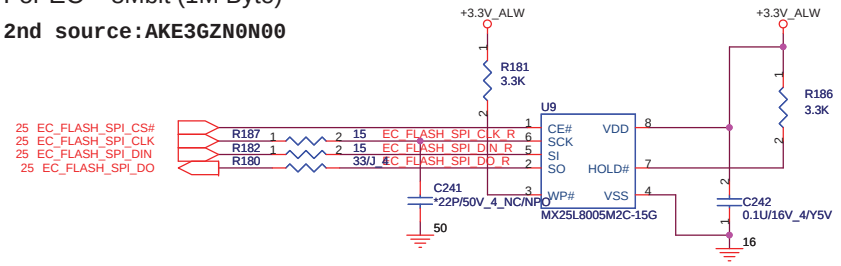
| Size | Document Number | Rev |
|---|---|---|
| | SIO ITE8502 | 1A |

Date: Wednesday, February 10, 2010 Sheet 25 of 46

UM3

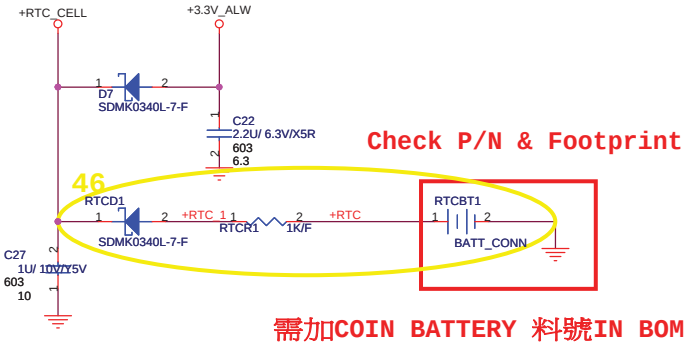
## For EC 8Mbit (1M Byte)

**2nd source:AKE3GZN0N00**




MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

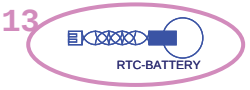
## RTC BATTERY




需加COIN BATTERY 料號IN BOM

need modify the location of this portions

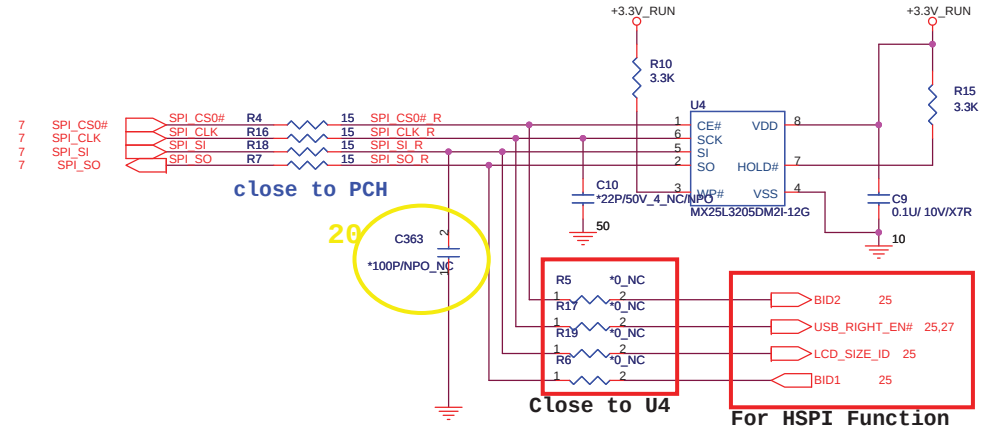
13




## For PCH

32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00



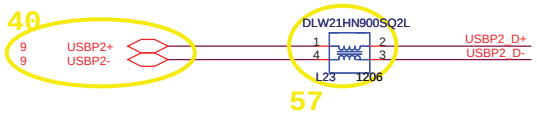

Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | FLASH/RTC | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 26 of 46 | |

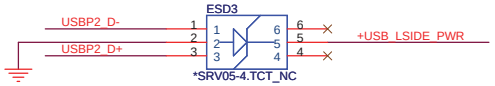
## eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

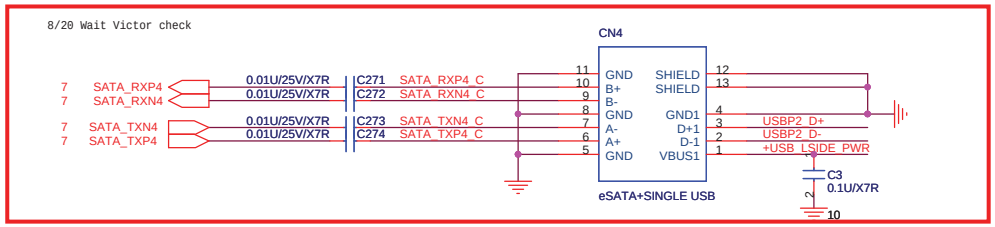


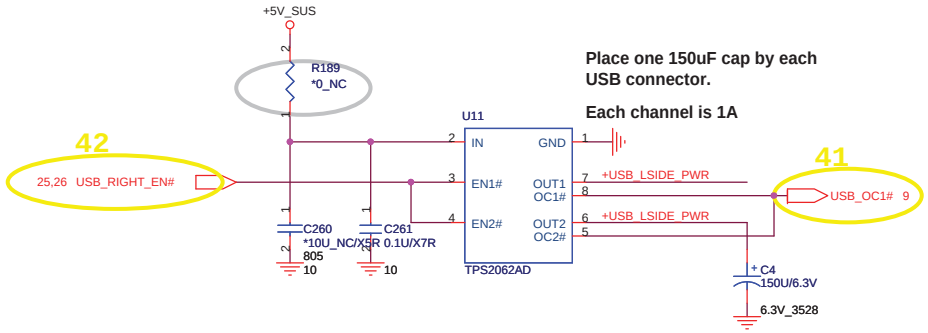

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



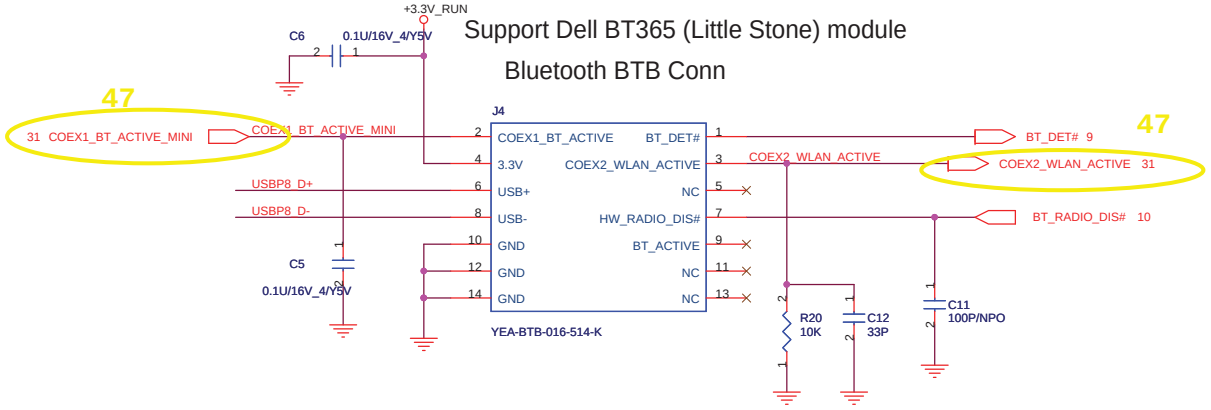

## USB and eSATA Conn.

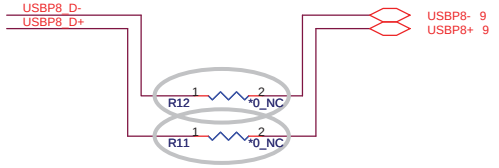



Support Dell BT365 (Little Stone) module

Bluetooth BTB Conn



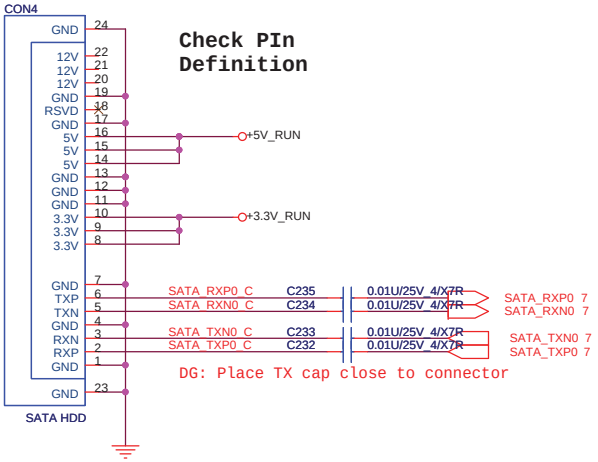



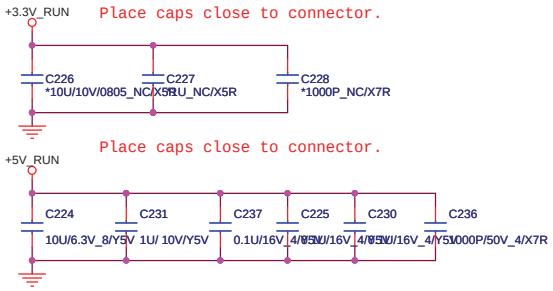

Quanta Computer Inc.

PROJECT : UM8 UMA

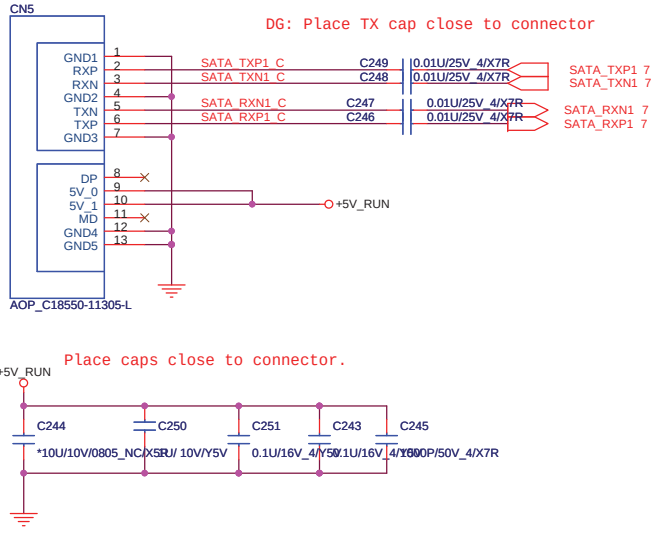
| Size | Document Number | Rev |
|---|---|---|
| | eSATA & Right USB | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 27 of 46 | |

## SATA Connector.



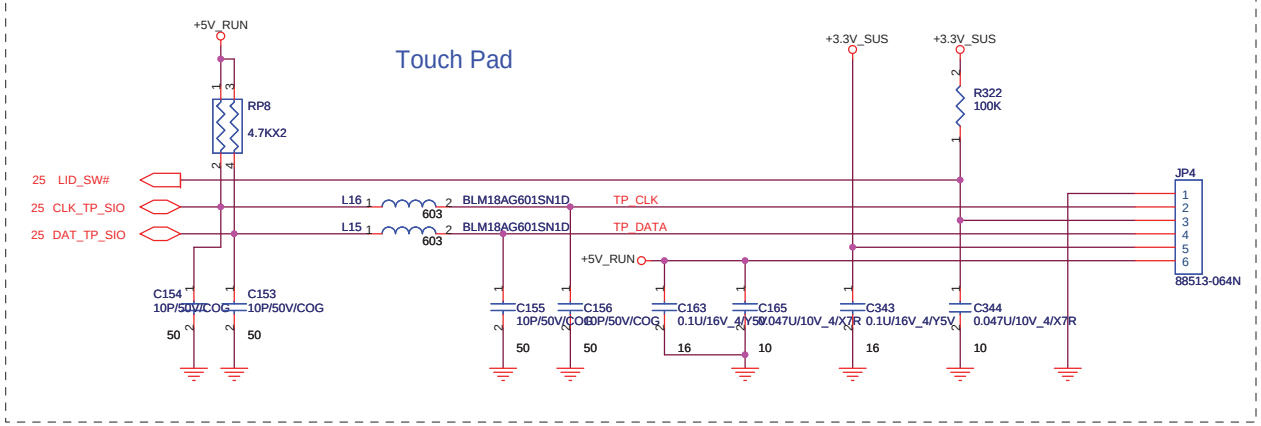




## ODD Connector

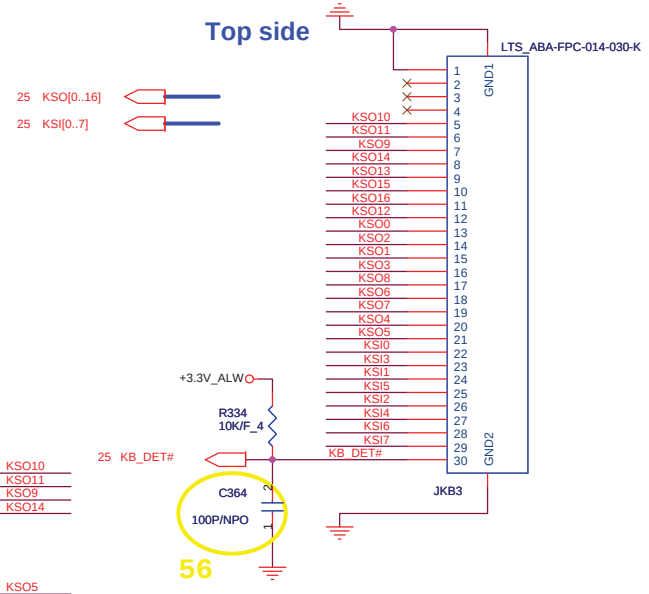


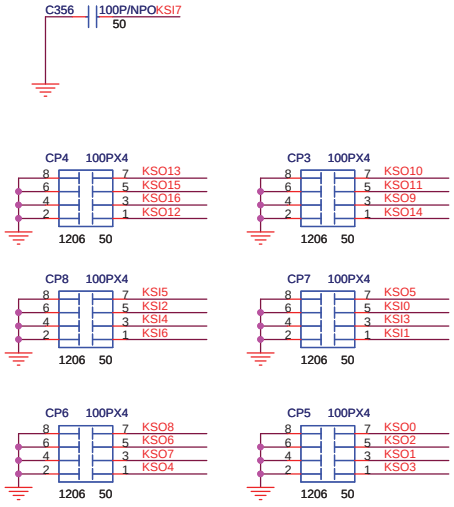







## KEYBOARD CONNECTOR




100P CAPS CLOSE TO JKB1

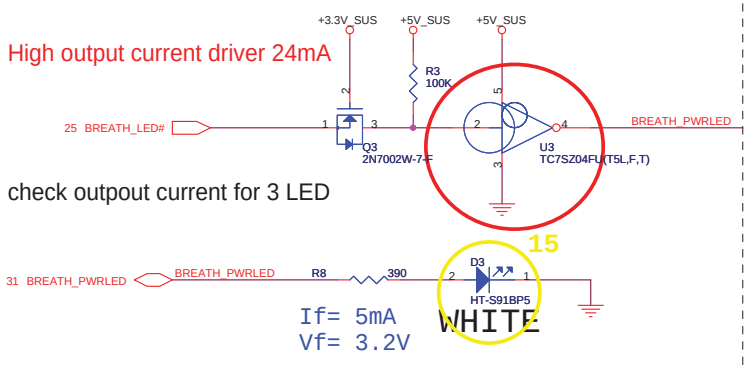
56

Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | SATA (HDD&ODD) & TP & KB | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 28 of 46 | |

## Power

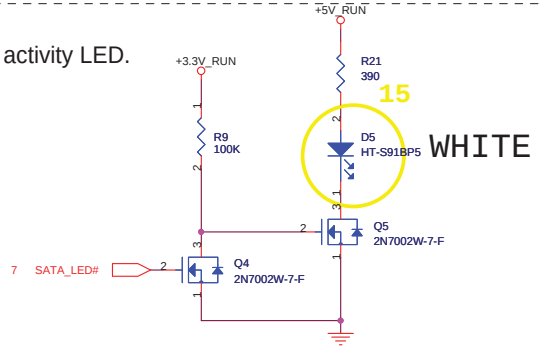
High output current driver 24mA



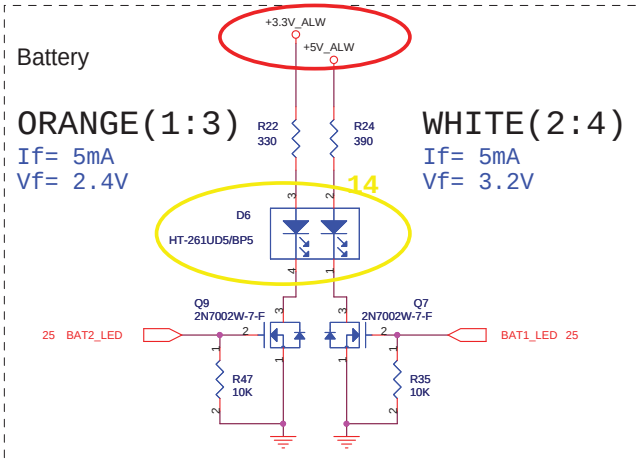

check outpout current for 3 LED




## HDD activity LED.

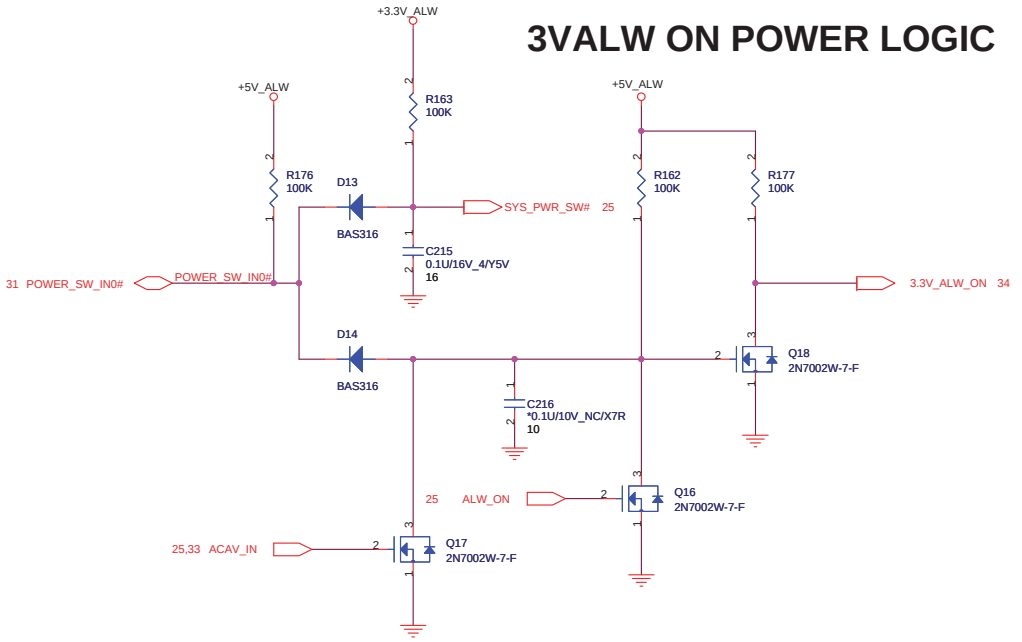


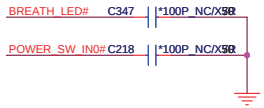

## Battery




UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

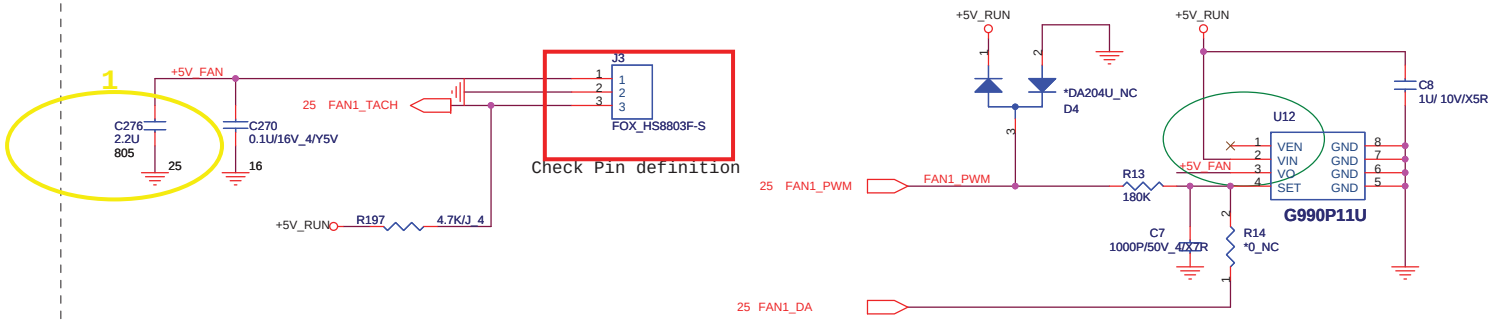
## 3VALW ON POWER LOGIC



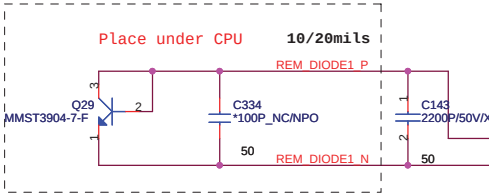




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : UM8B DIS | | |
| Size | Document Number: SWITCH, LED | Rev 1A |
| Date: Wednesday, February 10, 2010 | Sheet 29 of 46 | |

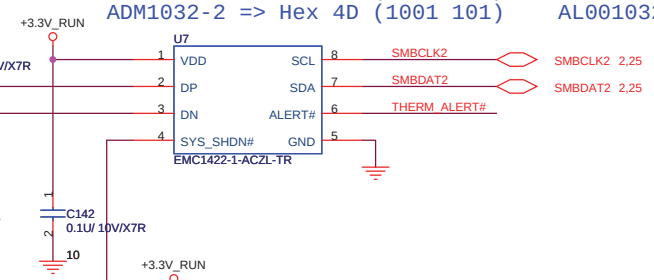
## FAN CONTROL



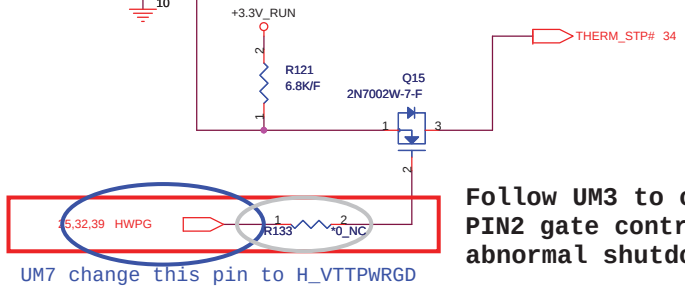

Place under CPU 10/20mils




ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002




1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy




UM7 change this pin to H_VTTPWRGD

Follow UM3 to change Q11 PIN2 gate control to avoid abnormal shutdown?

OTP 85 degree C


| SYS_SHD# / ALERT# | 4.7K | 6.8K | 10K | 15K | 22K | 33K |
|---|---|---|---|---|---|---|
| 4.7K | 77'C | 83'C | 89'C | 95'C | 101'C | 107'C |
| 6.8K | 78'C | 84'C | 90'C | 96'C | 102'C | 108'C |
| 10K | 79'C | 85'C | 91'C | 97'C | 103'C | 109'C |
| 15K | 80'C | 86'C | 92'C | 98'C | 104'C | 110'C |
| 22K | 81'C | 87'C | 93'C | 99'C | 105'C | 111'C |
| 33K | 82'C | 88'C | 94'C | 100'C | 106'C | 112'C |

Quanta Computer Inc.
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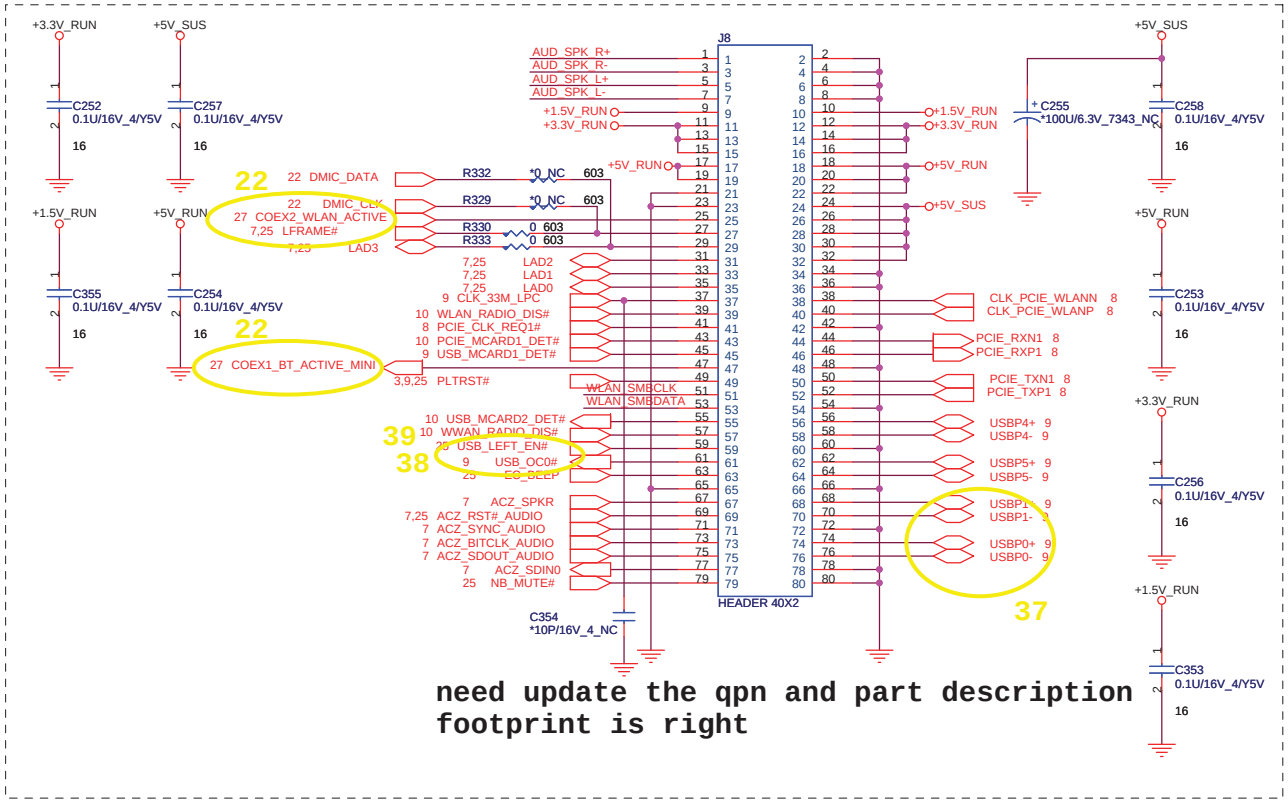
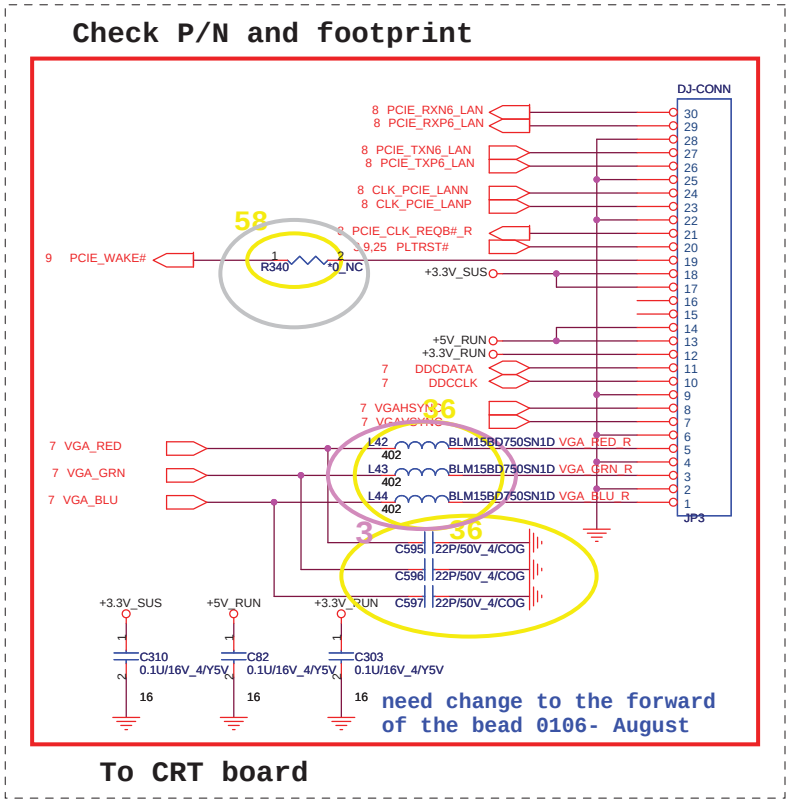
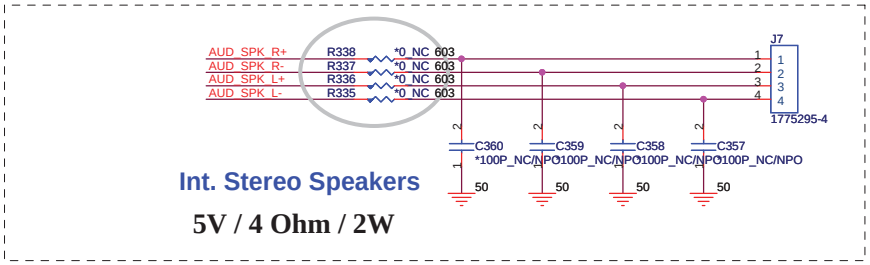
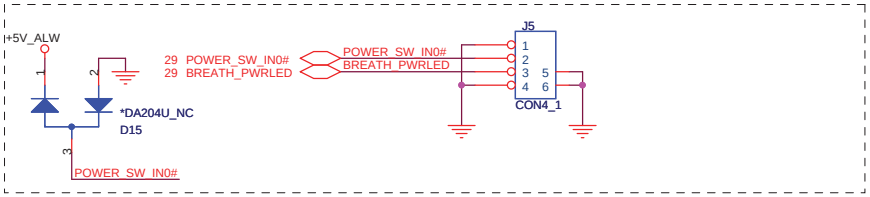
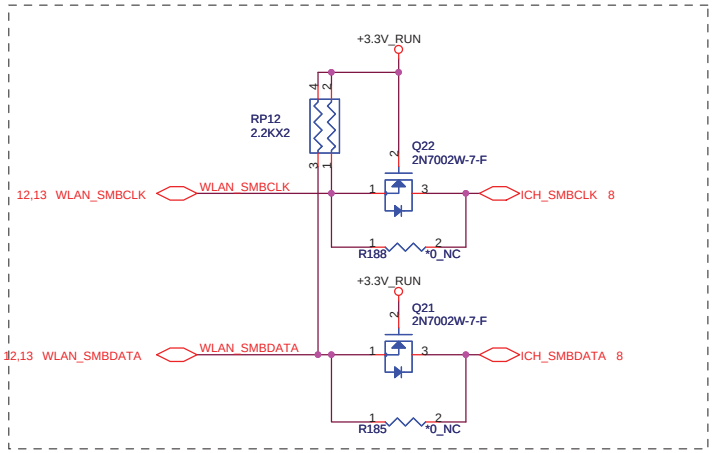


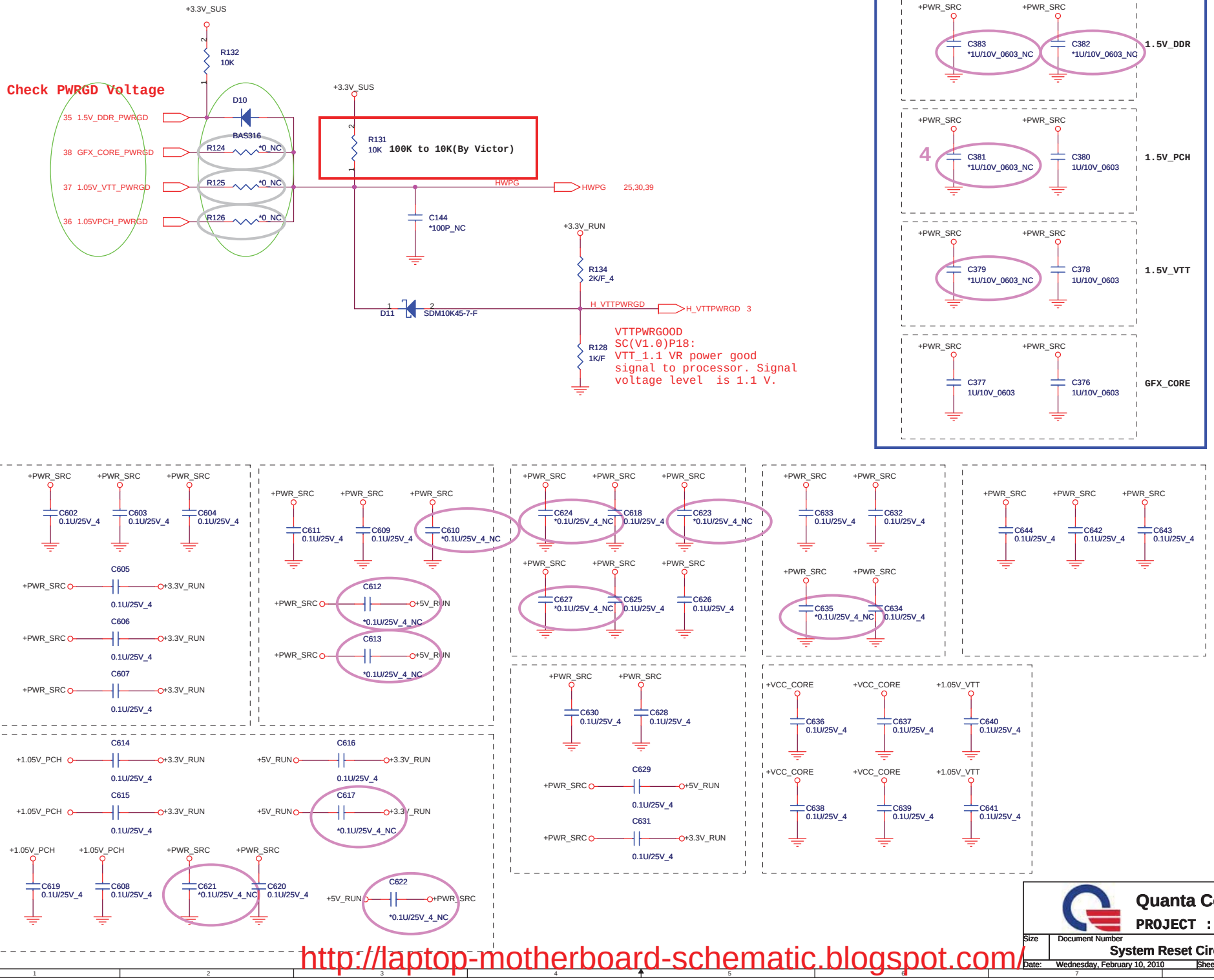




Quanta Computer Inc.

PROJECT : UM8B DIS

| Size | Document Number | Rev |
|---|---|---|
| | BTB CONN & Audio conn | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 31 of 46 | |




Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | System Reset Circuit | 1A |

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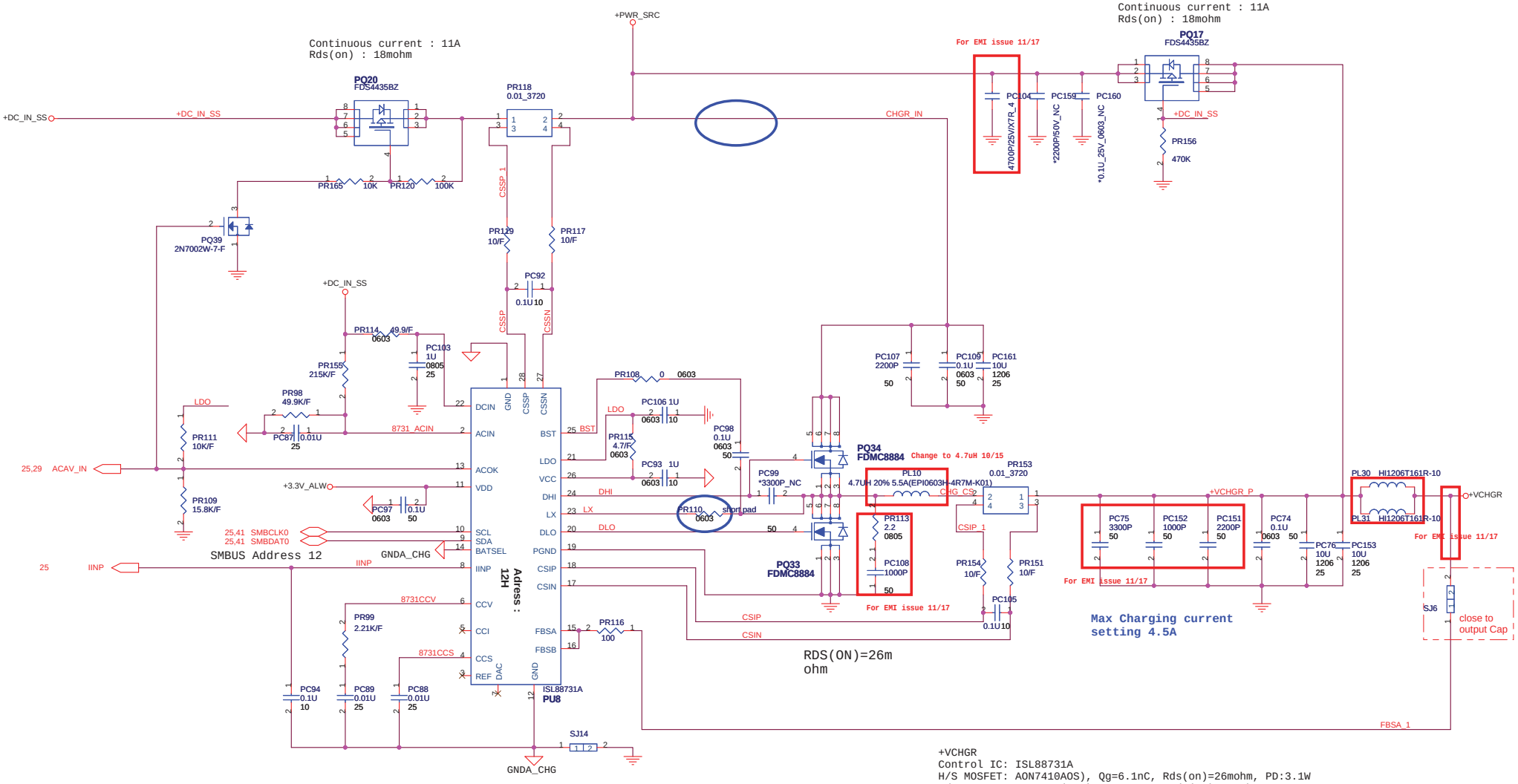
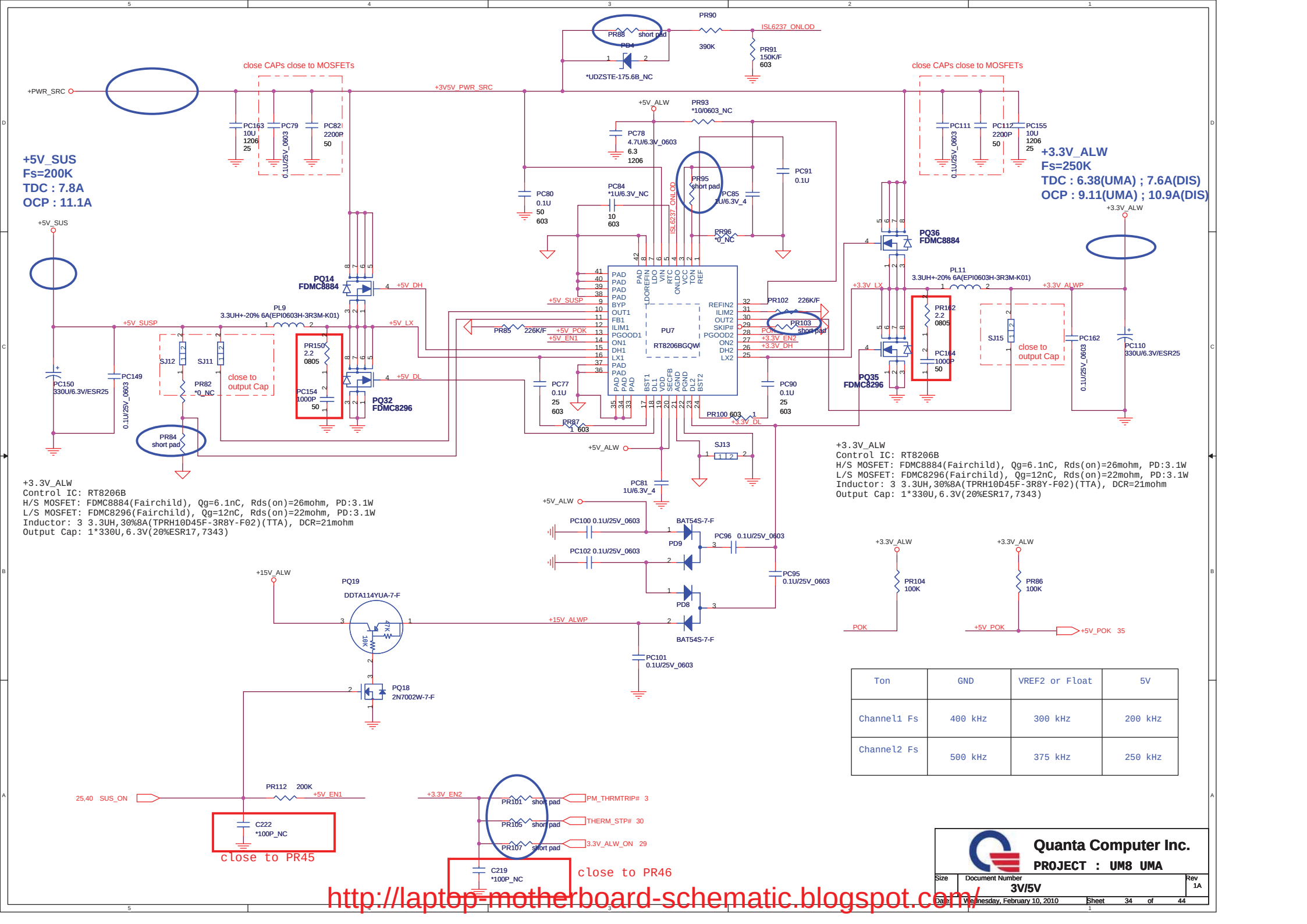
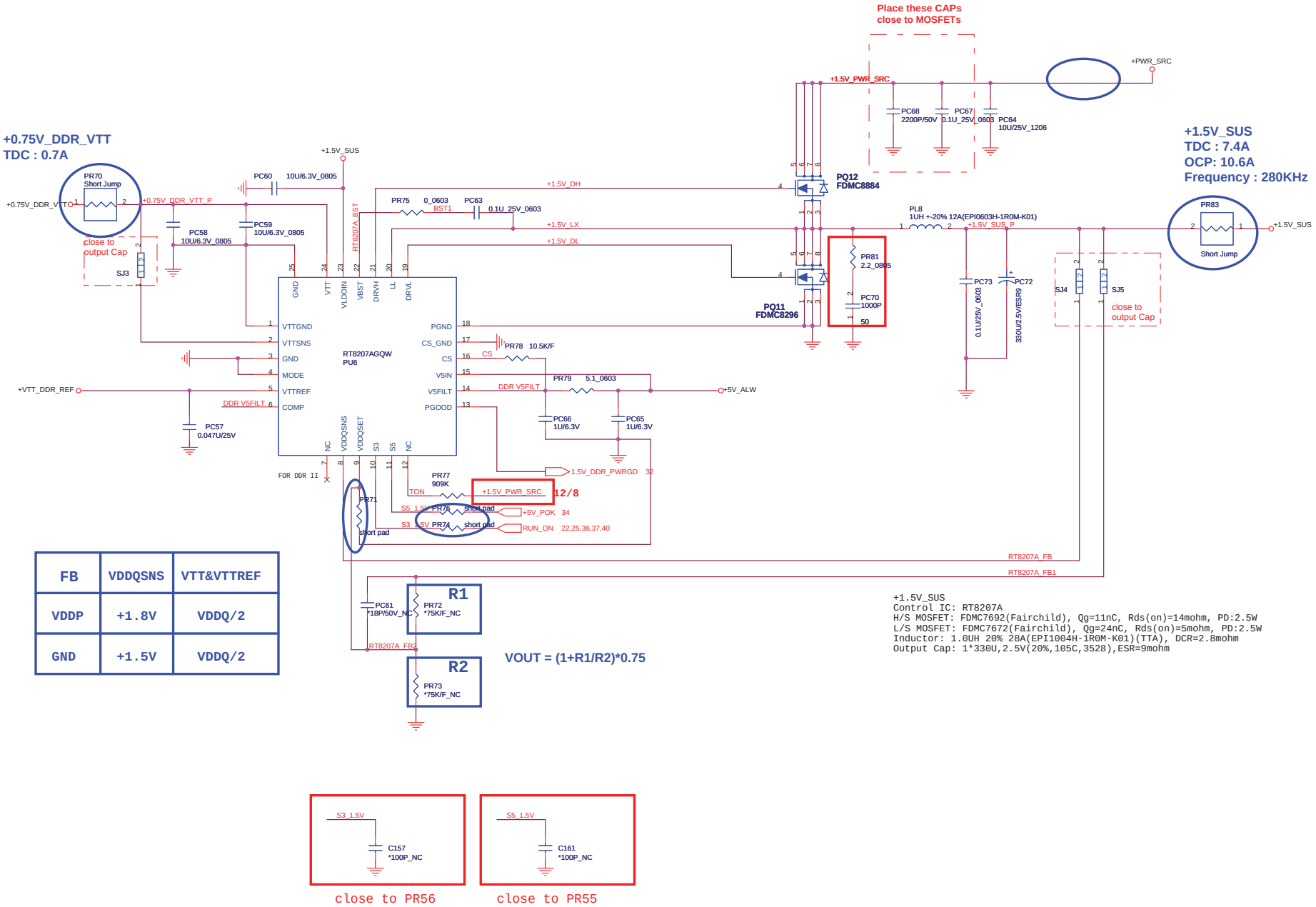





| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : UM8 UMA | | |
| Size | Document Number: Charger | Rev: 1A |
| Date: Wednesday, February 10, 2010 | Sheet 33 of 44 | |






| FB | VDDQSNS | VTT&VTTREF |
|---|---|---|
| VDDP | +1.8V | VDDQ/2 |
| GND | +1.5V | VDDQ/2 |

Quanta Computer Inc.
PROJECT : UM8 UMA
Size: Document Number: 1.5V_DDR Rev 1A
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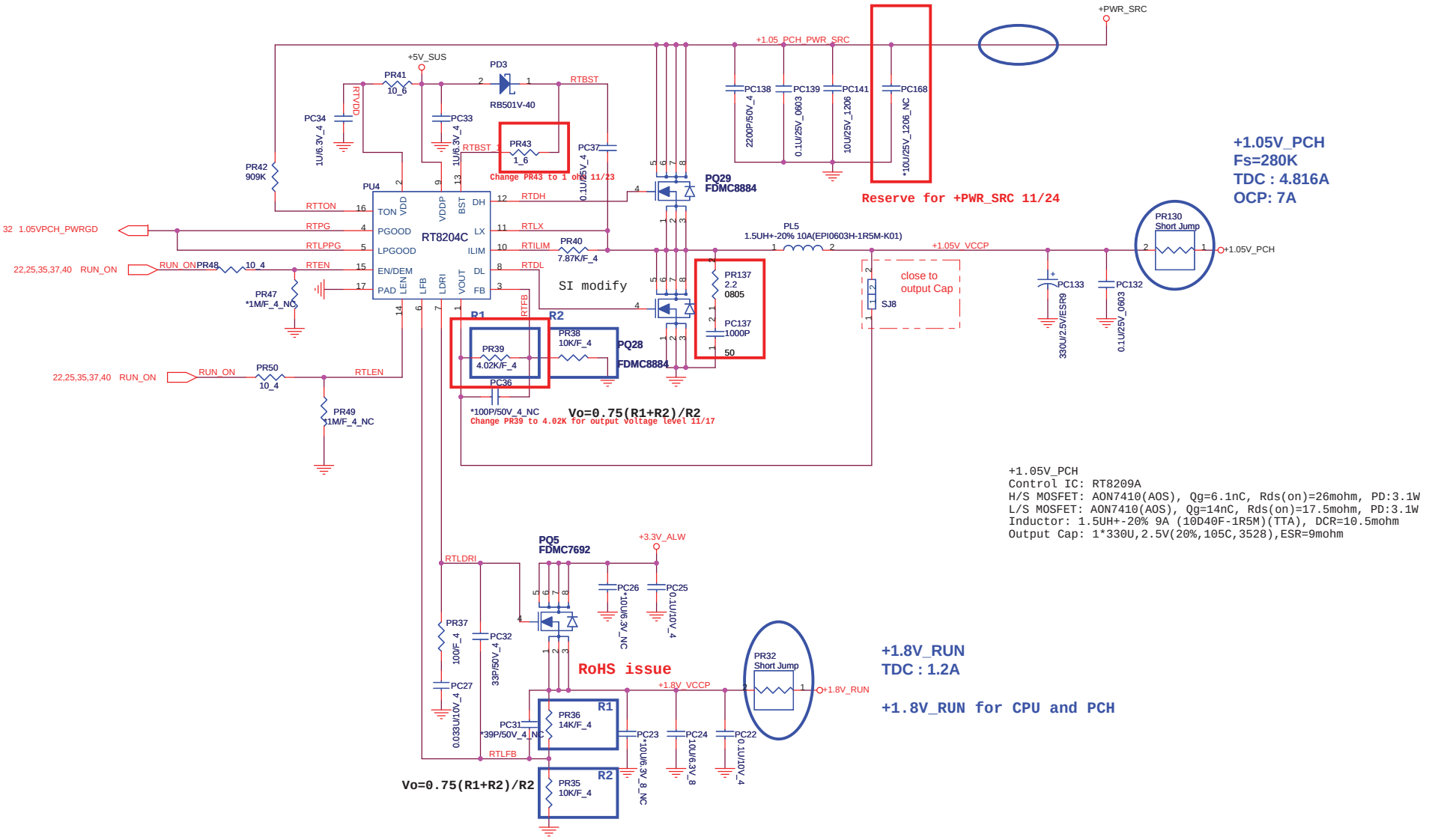
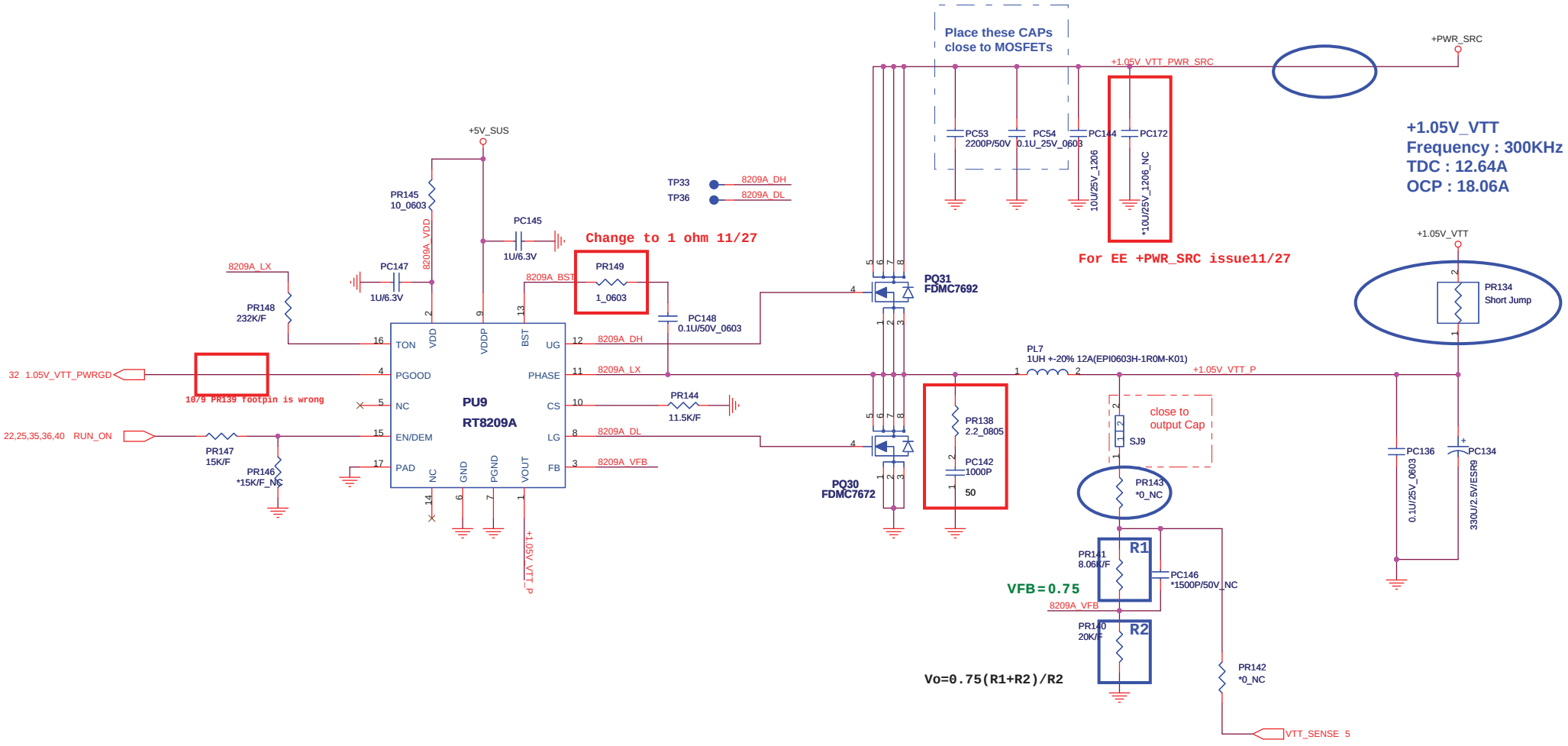



Quanta Computer Inc.

PROJECT : UM8 UMA

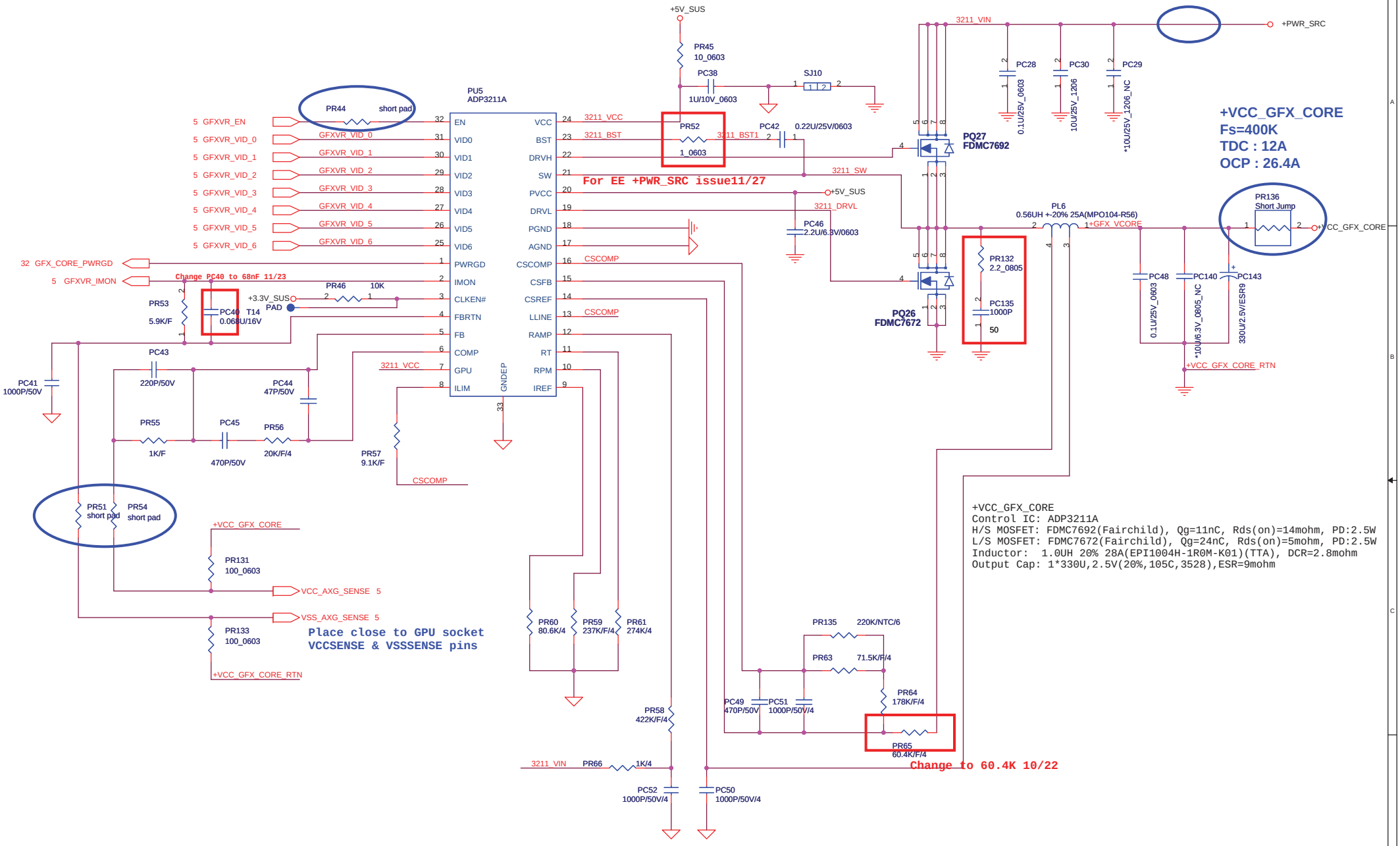
| Size | Document Number | Rev |
|---|---|---|
| | 1.05_PCH | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 36 of 44 | |




+1.05V_VTT
Control IC: RT8209A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

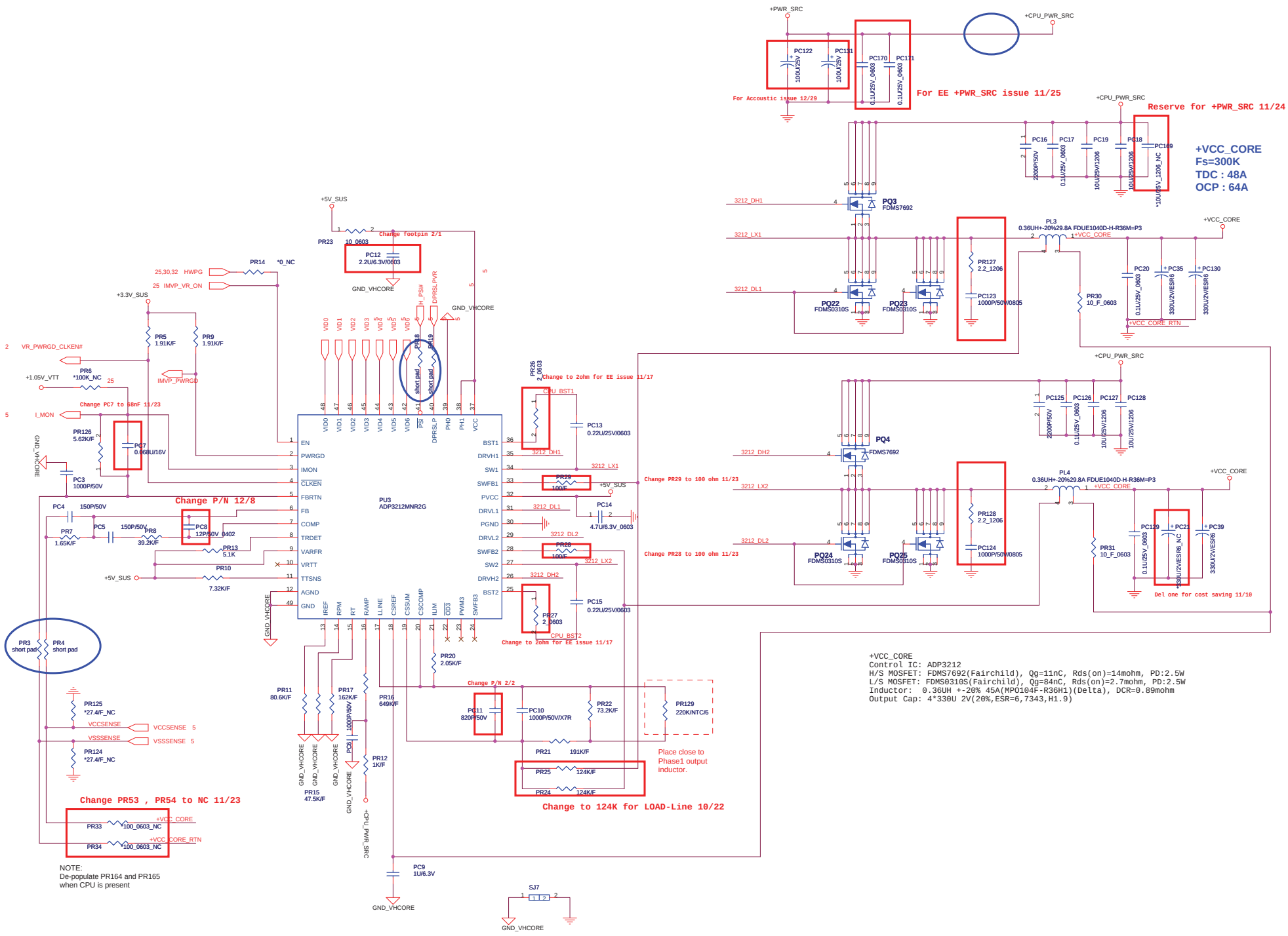
Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | 1.05_VTT | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 37 of 44 | |





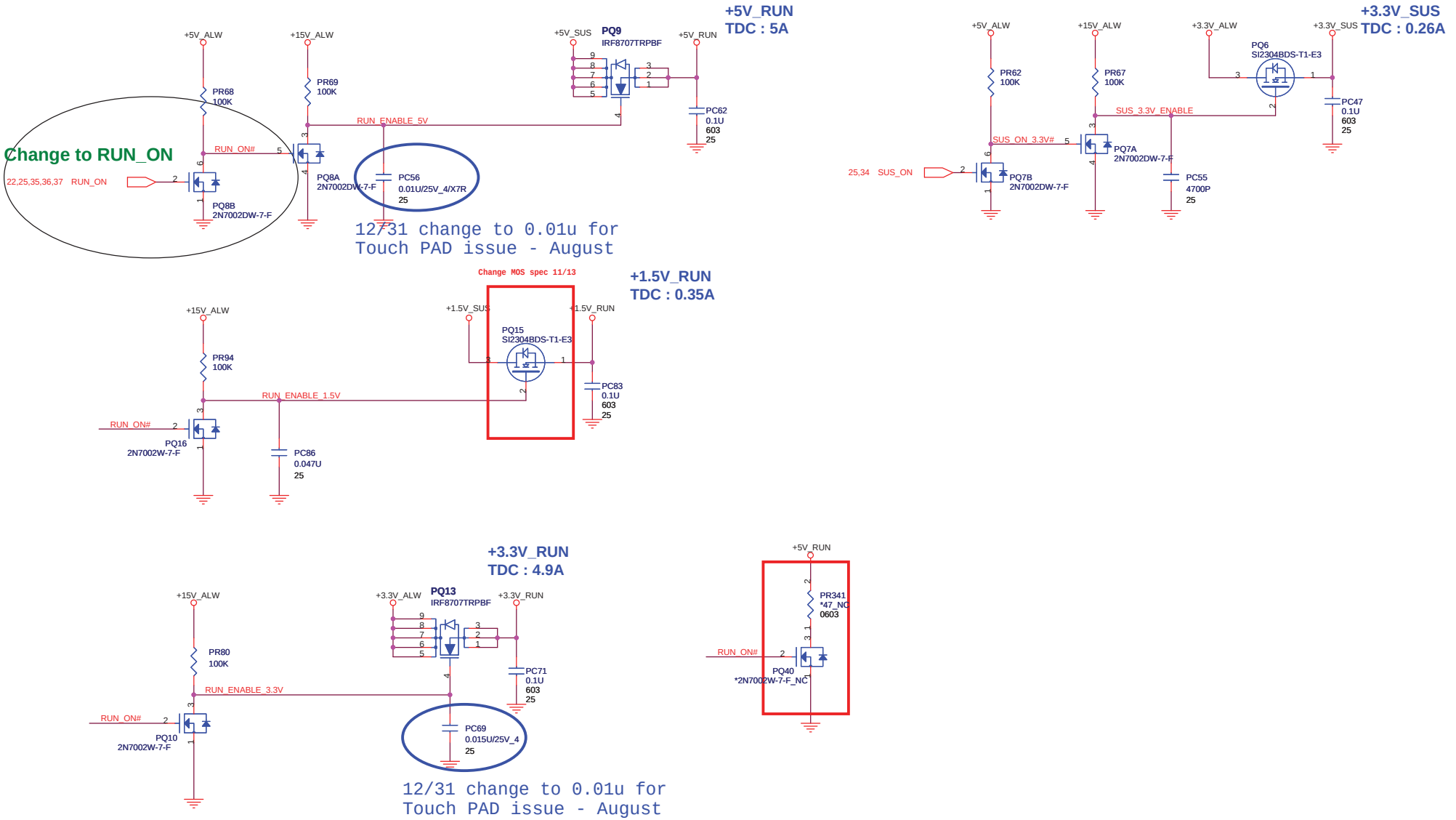

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : UM8 UMA | | |
| Size | Document Number: GFX_CORE | Rev: 1A |
| Date: Wednesday, February 10, 2010 | Sheet 38 of 44 | |






Quanta Computer Inc.
PROJECT : UM8 UMA

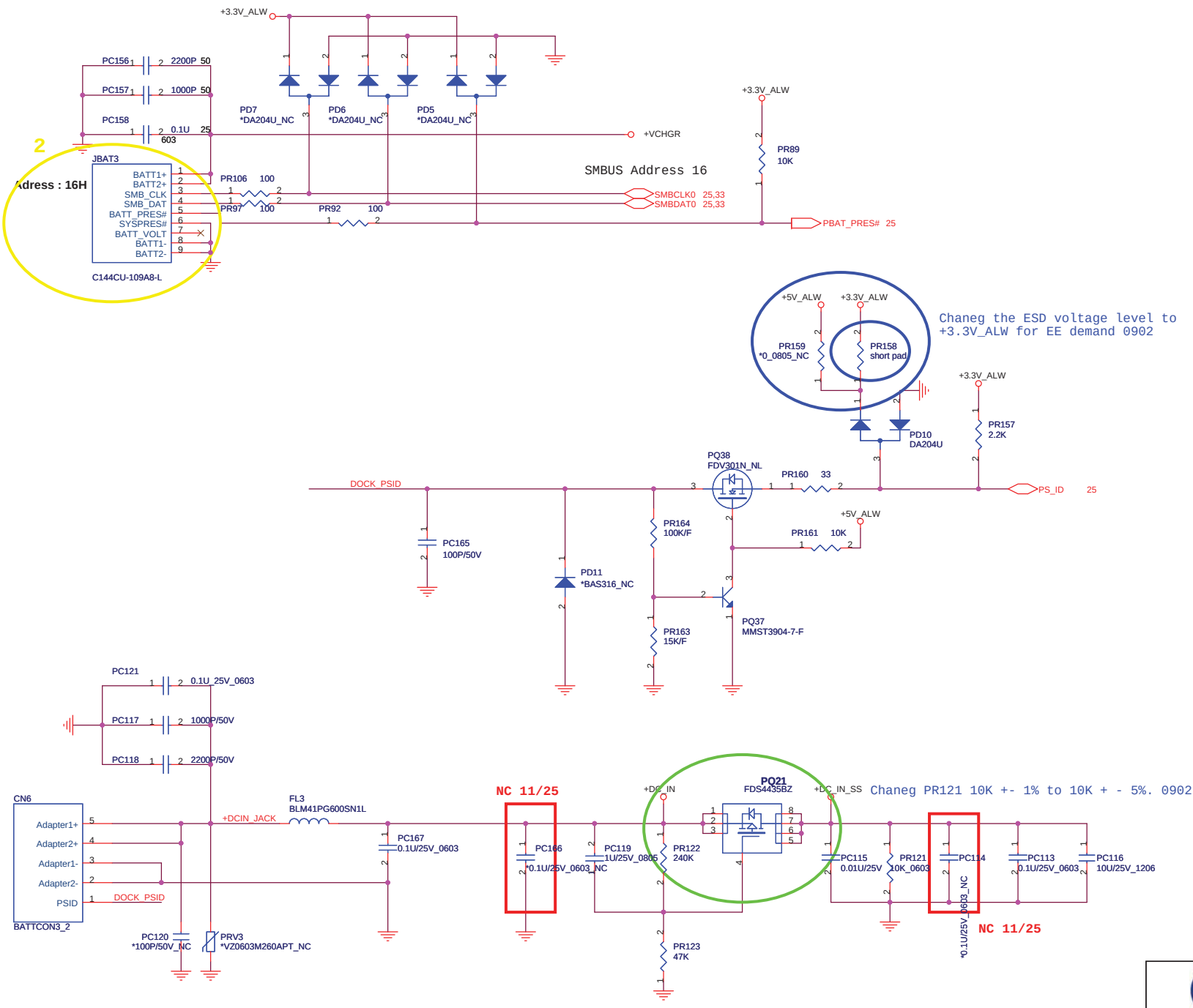
| Size | Document Number | Rev |
|---|---|---|
| | CPU CORE | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 39 of 44 | |




Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Run Power Switch | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 40 of 44 | |






Quanta Computer Inc.
PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Batt & DC-IN | 1A |
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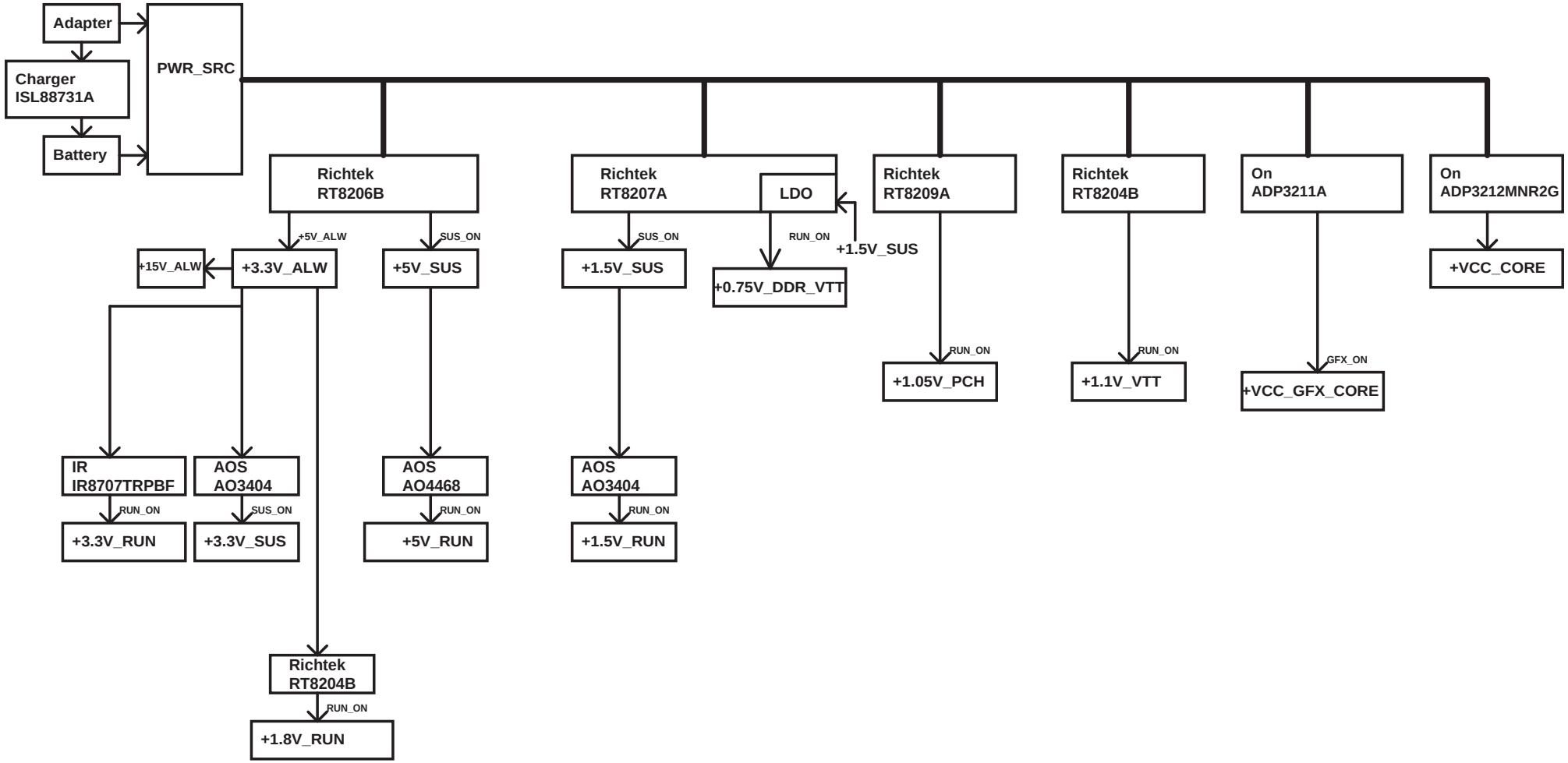
VER : 1A




Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | Schematic Block Diagram1 | 1A |
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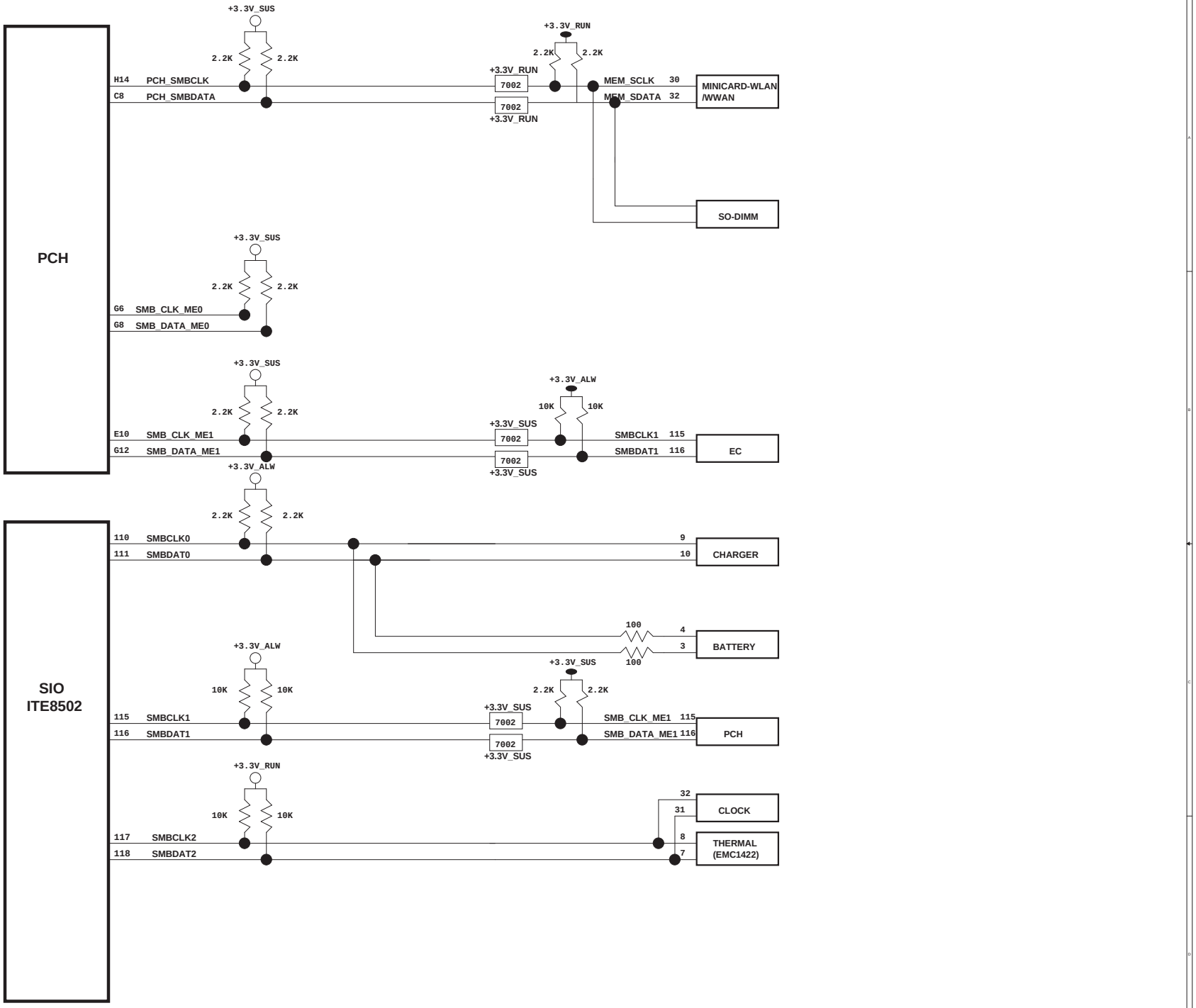
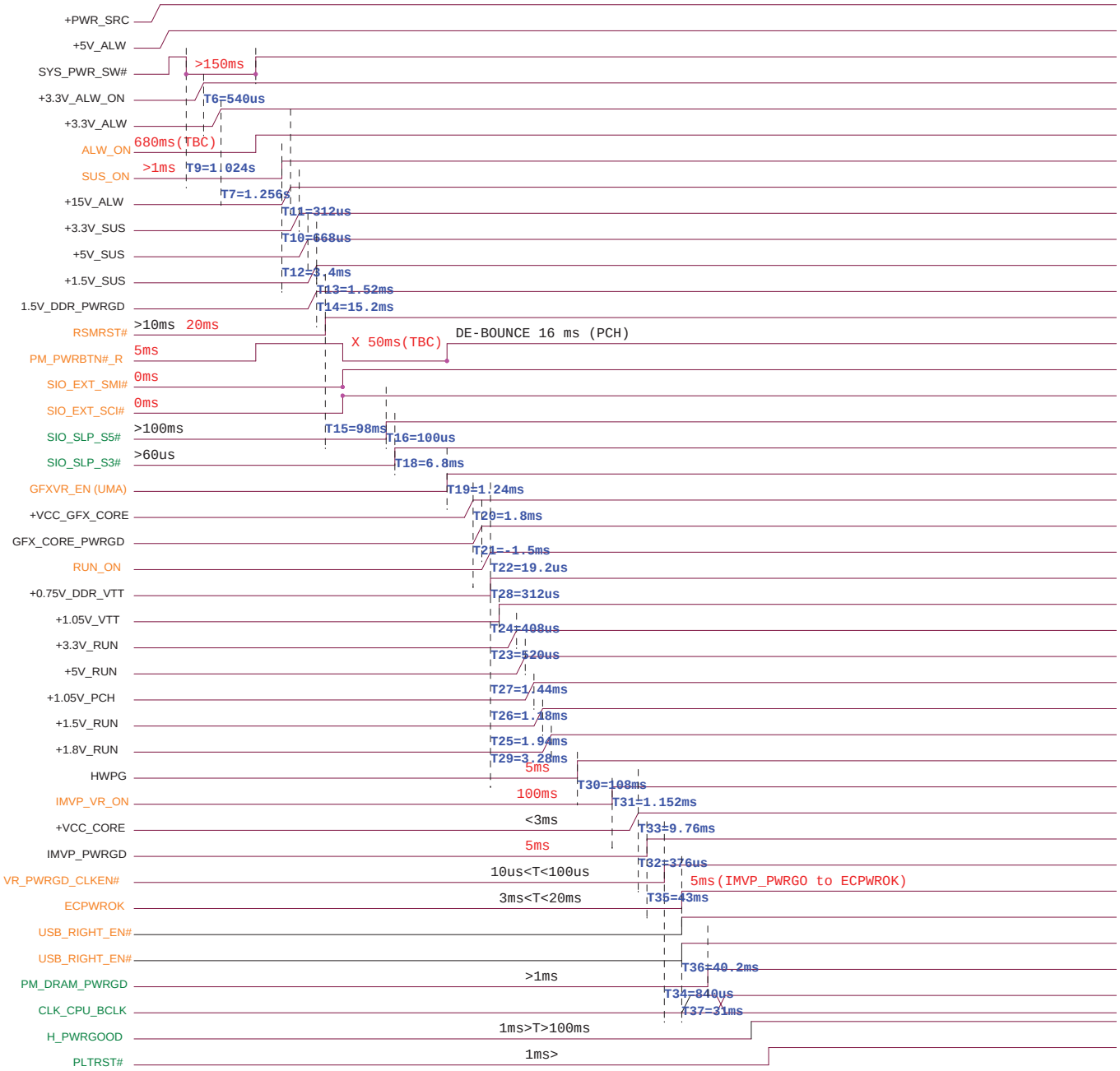



Quanta Computer Inc.
PROJECT : UM8 UMA
SMBUS BLOCK
Size | Document Number | Rev 1A
Date: | Wednesday, February 11, 2009 | Sheet 43 of 45

# UM8_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)






Quanta Computer Inc.

PROJECT : UM8 UMA

| Size | Document Number | Rev |
|---|---|---|
| | POWER SEQUENCE | 1A |

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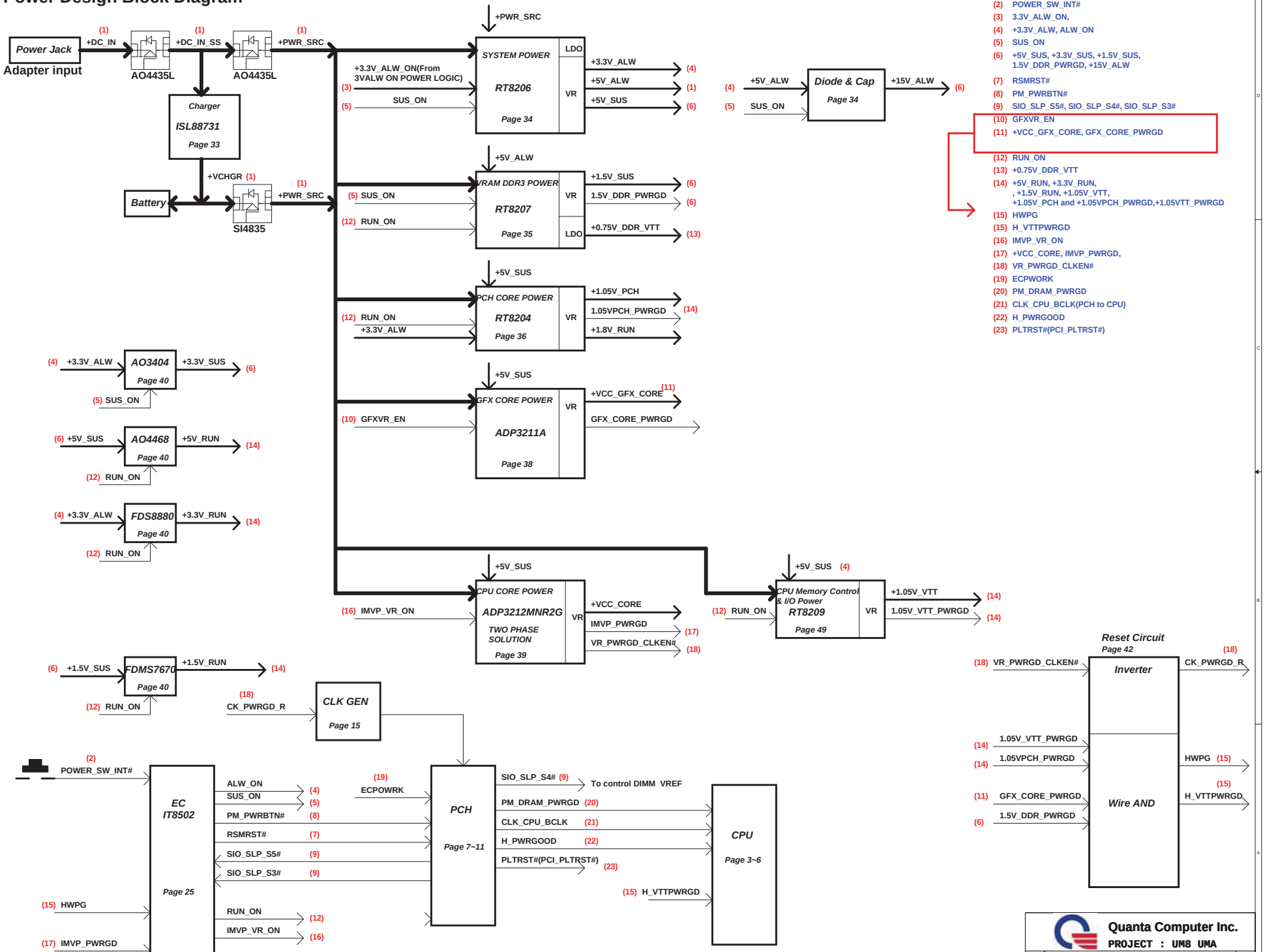
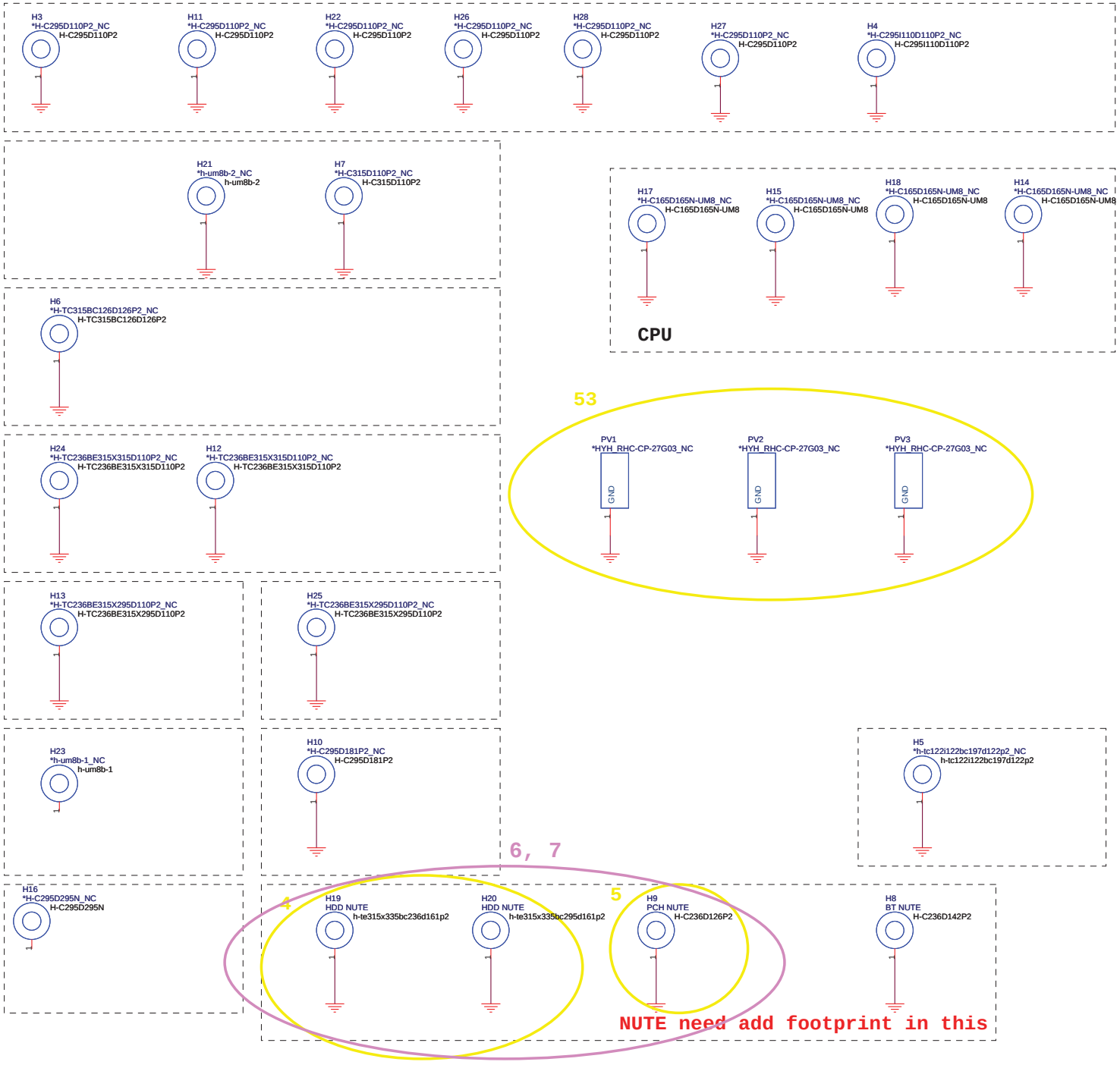
# Power Design Block Diagram




(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFXVR_EN
(11) +VCC_GFX_CORE, GFX_CORE_PWRGD
(12) RUN_ON
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(15) HWPG
(15) H_VTTPWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD,
(18) VR_PWRGD_CLKEN#
(19) ECPWORK
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : UM8 UMA | | | |
| Size | Document Number | | Rev |
| | POWER SEQUENCE BLOCK | | 1A |
| Date: Wednesday, February 10, 2010 | Sheet 45 of 46 | | |




Quanta Computer Inc.

PROJECT : UM8B DIS

| Size | Document Number | Rev |
|---|---|---|
| | PAD&SCREW | 1A |
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