

Compal Confidential

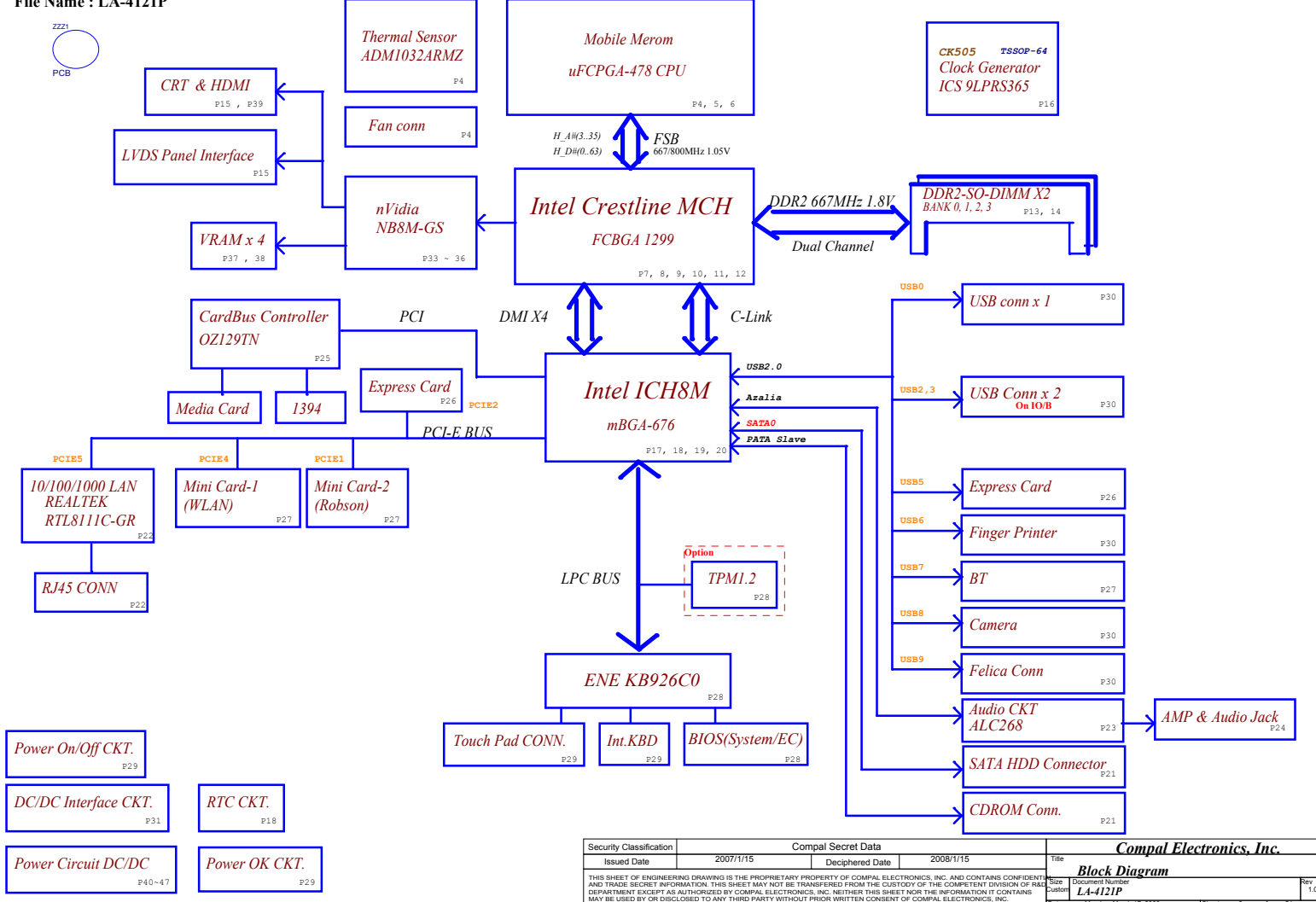
Schematic Document

Crestline_GM/PM+NB8M-GS & ICH8M

2008 / 3 / 17 Rev:1.0

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title
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JAL30 UMA/Discrete



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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Block Diagram		
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Voltage Rails

State \ Power plane	O MEANS ON X MEANS OFF			CLOCK
	+B	+5VALW +3VALW	+1.8V	
s0	O	O	O	O
s3	O	O	X	O
s5 s4/AC	O	O	X	O
s5 s4/ Battery only	O	X	X	X
s5 s4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b7	ADM1032	4D
EEPROM(24C16/02)	1010 000X b7 (24C04)		
	1011 000Xb7		

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb7
DDRII DIMM0	1001 000Xb7
DDRII DIMM2	1001 010Xb7

STATE	SIGNAL				+VALW	+V	+VS	Clock
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#				
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

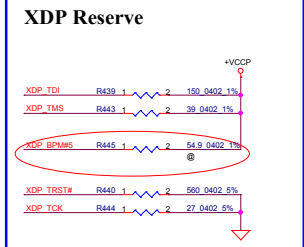
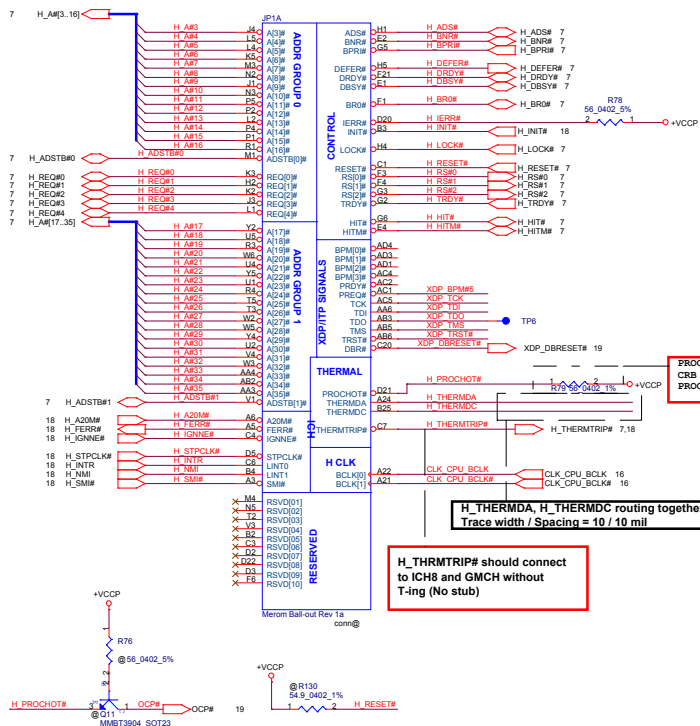
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

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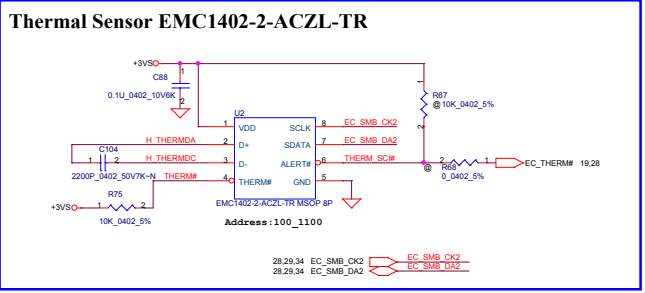
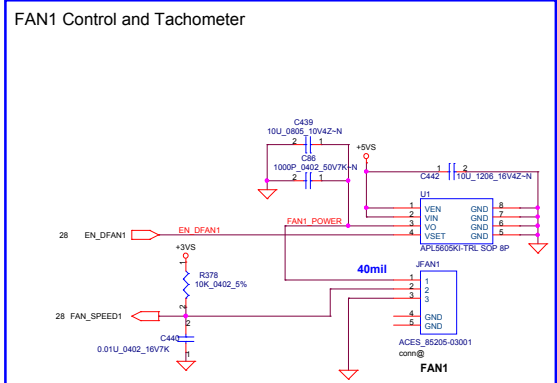
GRATIS - FOR FREE
hexainf@hotmail.com



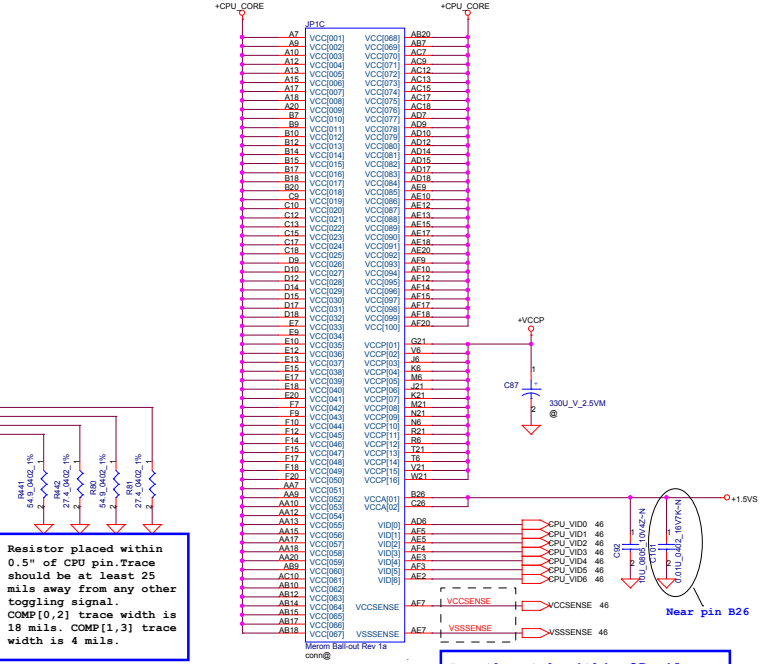
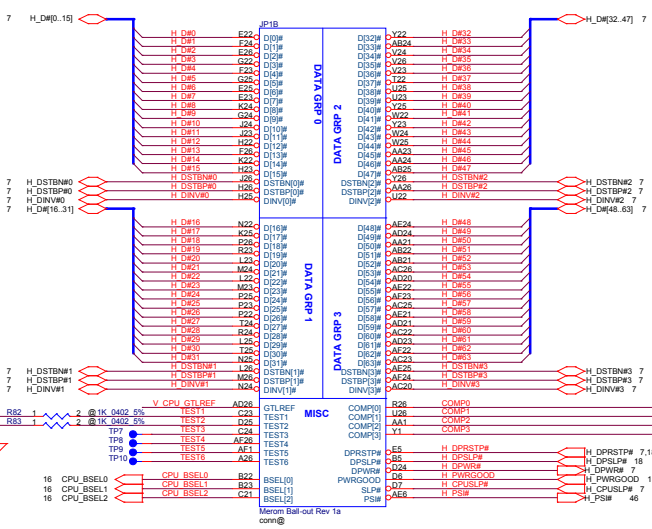
PROCBOT# is not used ----> 56 ohms pull-up
 CRB uses 1K ohms pull-up resistor to fix
 PROCBOT# failure when driven by a thermal sensor.

H_THERMDA, H_THERMDC routing together,
 Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect
 to ICHB and GMCH without
 T-ing (No stub)



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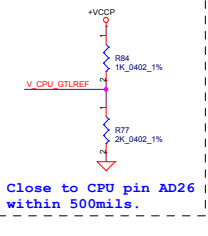


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

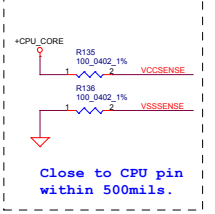
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other coupling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.

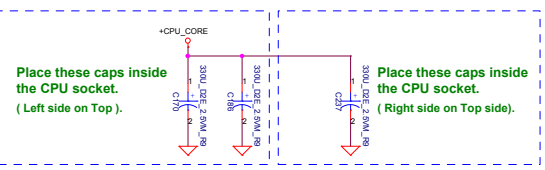
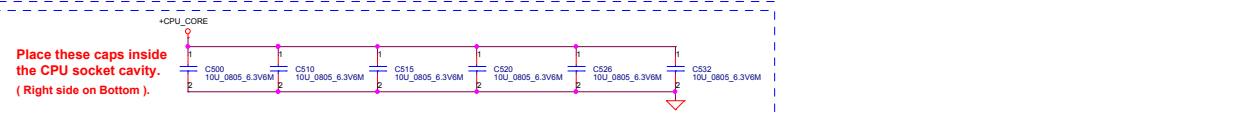
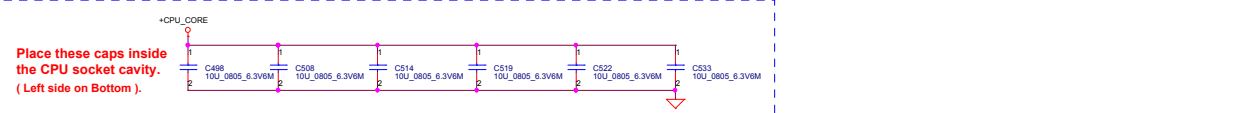
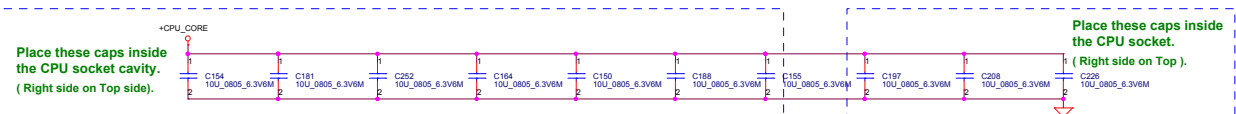
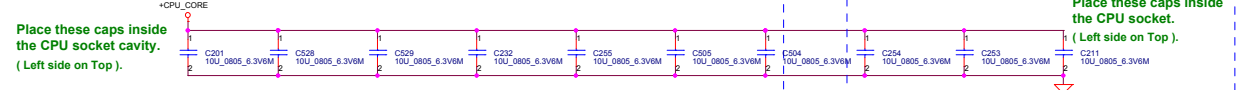


Close to CPU pin within 500mils.

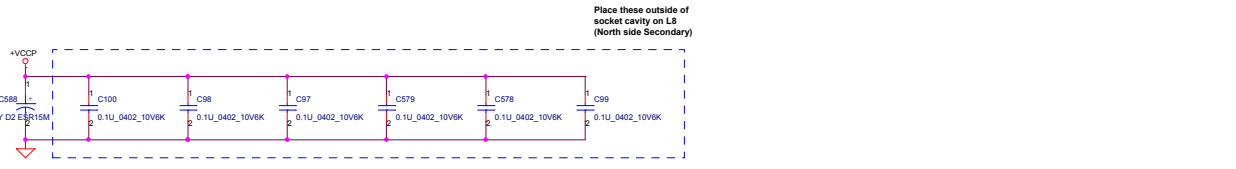
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	File	Merom(2/3)-AGTL+/PWR
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High Frequency Decoupling
10uF 0805 X5R -> 85 degree.

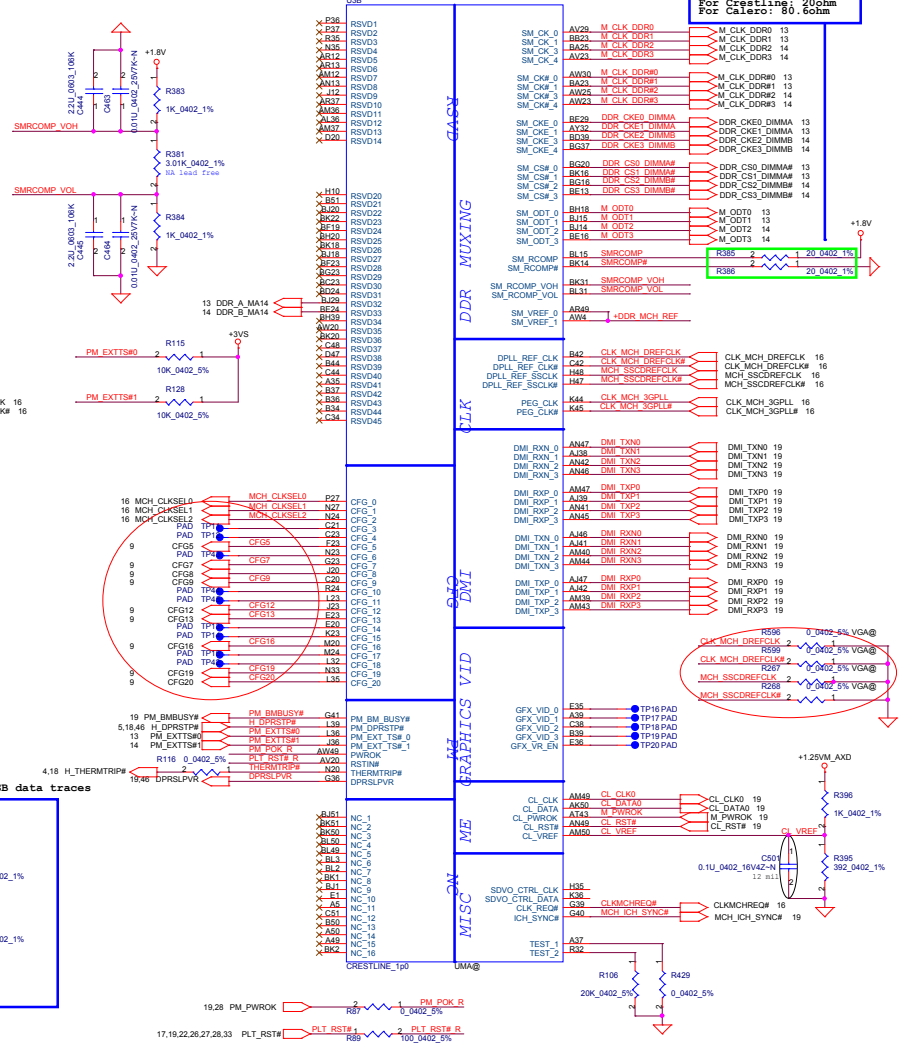
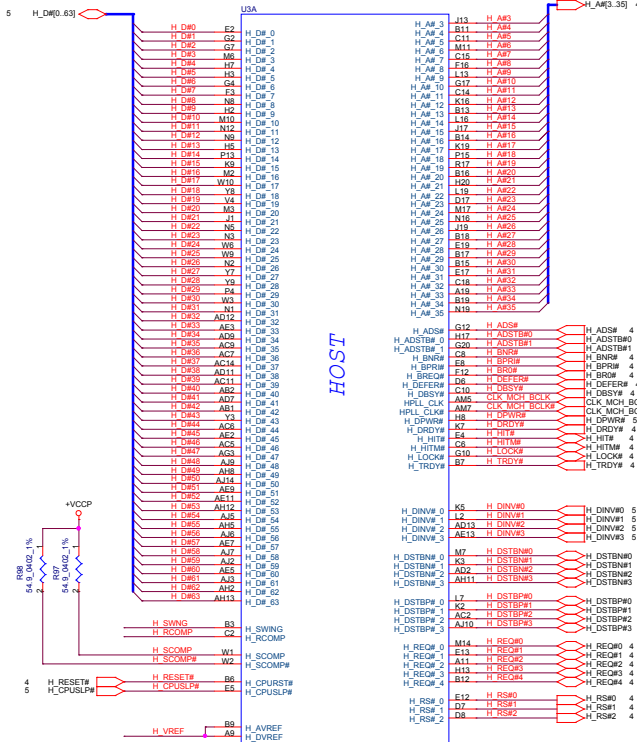
JHD		
A4	VSS001	PS
A8	VSS002	P21
A11	VSS003	P24
A14	VSS004	RS
A16	VSS005	R2
A19	VSS006	R22
A23	VSS007	T1
A27	VSS008	T2
B6	VSS009	T23
B8	VSS010	T24
B11	VSS011	US
B13	VSS012	US
B18	VSS013	US
B24	VSS014	US
B29	VSS015	US
C2	VSS016	V2
C3	VSS017	V2
C4	VSS018	V2
C11	VSS019	W1
C14	VSS020	W1
C16	VSS021	W2
C18	VSS022	W2
C22	VSS023	W3
C25	VSS024	W3
C26	VSS025	W3
D1	VSS026	Y1
D4	VSS027	Y2
D6	VSS028	Y2
D11	VSS029	AA2
D13	VSS030	AA2
D16	VSS031	AA2
D19	VSS032	AA2
D23	VSS033	AA2
D28	VSS034	AA2
E3	VSS035	AA2
E8	VSS036	AA2
E11	VSS037	AB1
E16	VSS038	AB1
E18	VSS039	AB1
E19	VSS040	AB1
E24	VSS041	AB1
E27	VSS042	AB1
F4	VSS043	AB1
F5	VSS044	AB2
F8	VSS045	AB2
F13	VSS046	AC2
F16	VSS047	AC2
F19	VSS048	AC1
F2	VSS049	AC1
F22	VSS050	AC1
F25	VSS051	AC1
G4	VSS052	AC1
G1	VSS053	AC24
G3	VSS054	AC24
G28	VSS055	AD2
H3	VSS056	AD2
H6	VSS057	AD11
H21	VSS058	AD13
H24	VSS059	AD16
J2	VSS060	AD19
J6	VSS061	AD22
J22	VSS062	AD25
K6	VSS063	AE1
K1	VSS064	AE4
K4	VSS065	AE8
K8	VSS066	AE11
K23	VSS067	AE14
K28	VSS068	AE14
L3	VSS069	AE16
L6	VSS070	AE19
L1	VSS071	AE23
L4	VSS072	AE28
M2	VSS073	AF2
M6	VSS074	AF6
M22	VSS075	AF8
M25	VSS076	AF11
N1	VSS077	AF13
N4	VSS078	AF16
N23	VSS079	AF19
N28	VSS080	AF22
P3	VSS081	AF25
P1	VSS082	AF28



ESR <= 1.5m ohm
Capacitor > 880 uF

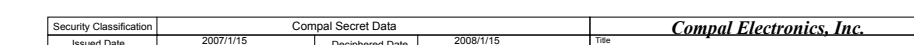
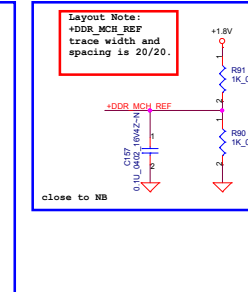
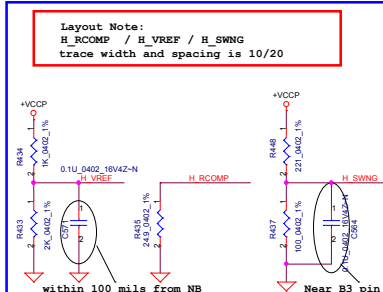


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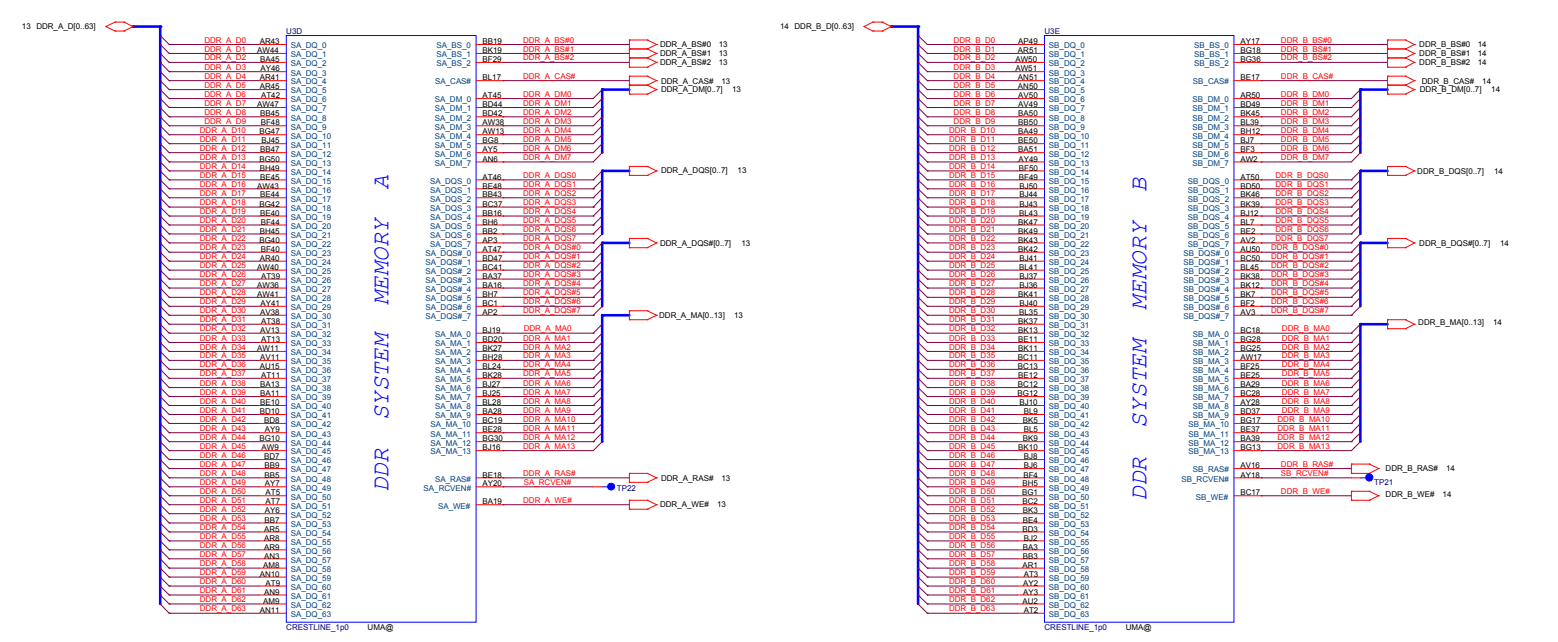


layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as PSB data traces

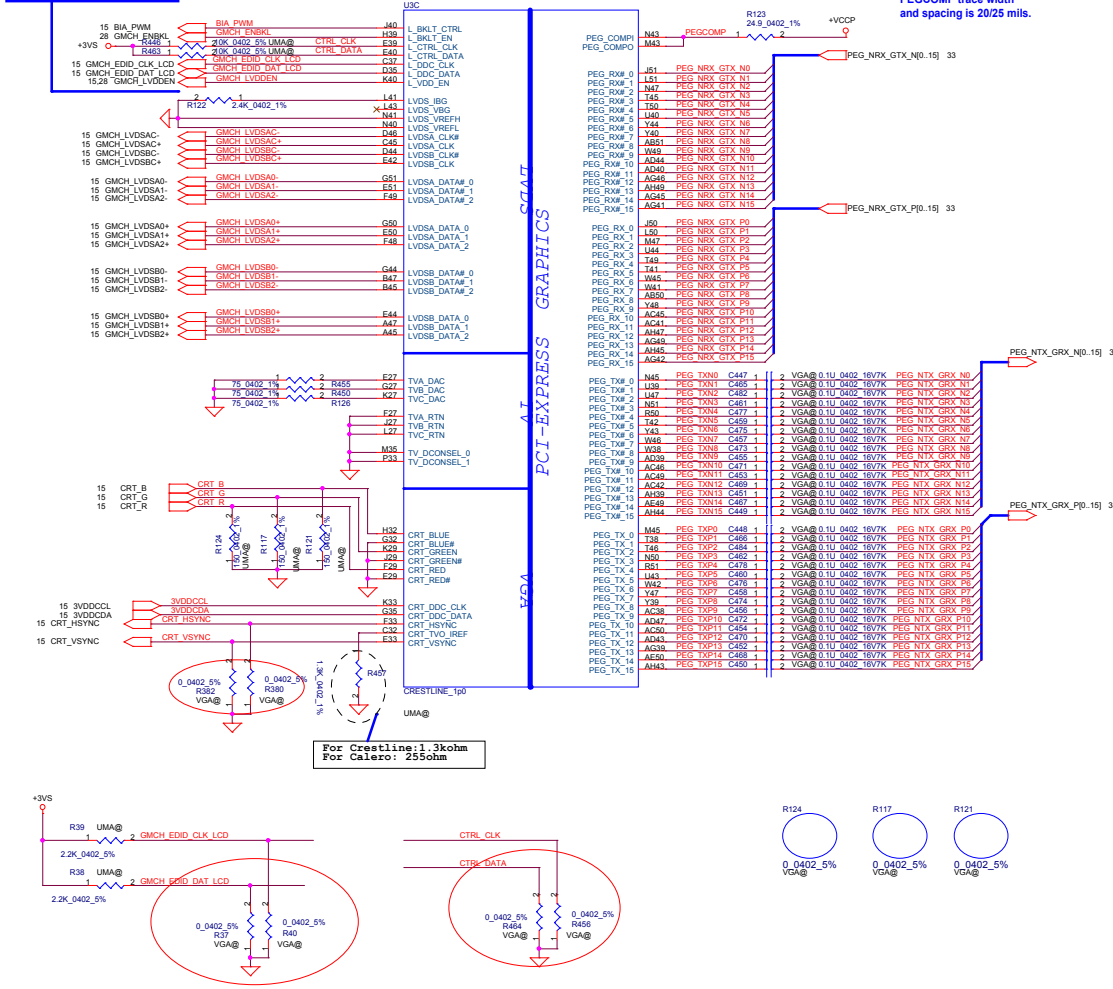


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				CRESTLINE(1/6)-AGTL+DMI/DDR2
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For Crestline: 2.4kohm
For Calero: 1.5kohm



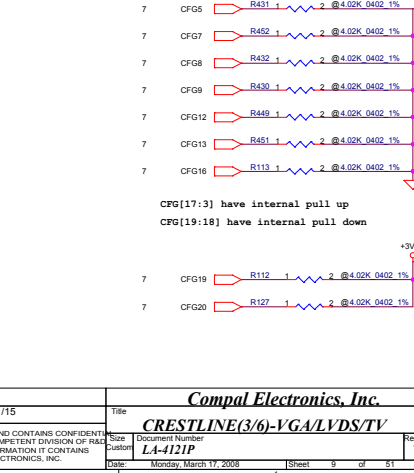
For Crestline: 1.3kohm
For Calero: 255ohm

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

PEGCOMP trace width and spacing is 20/25 mils.

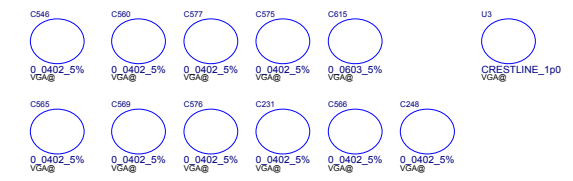
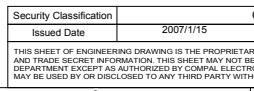
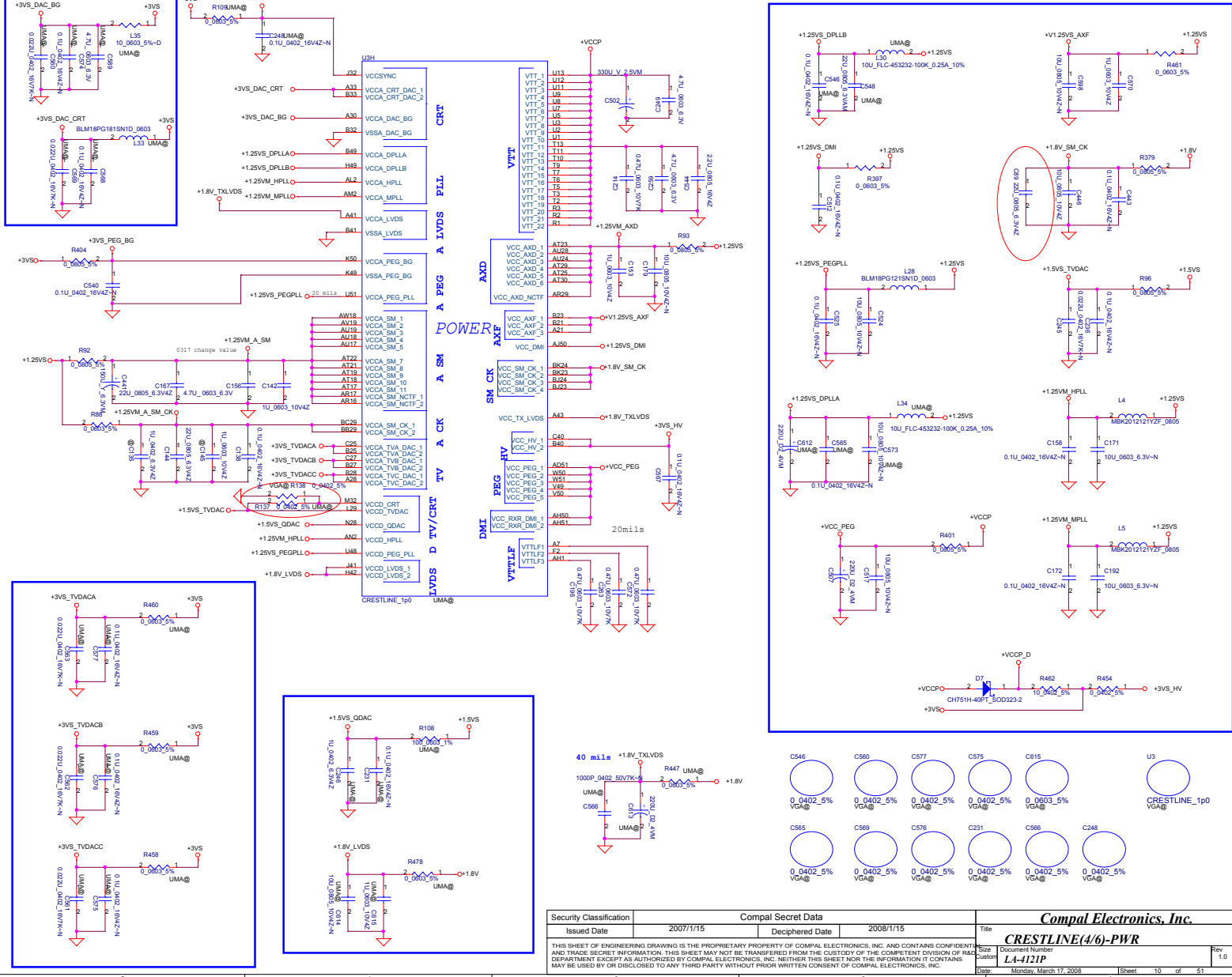
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simul.

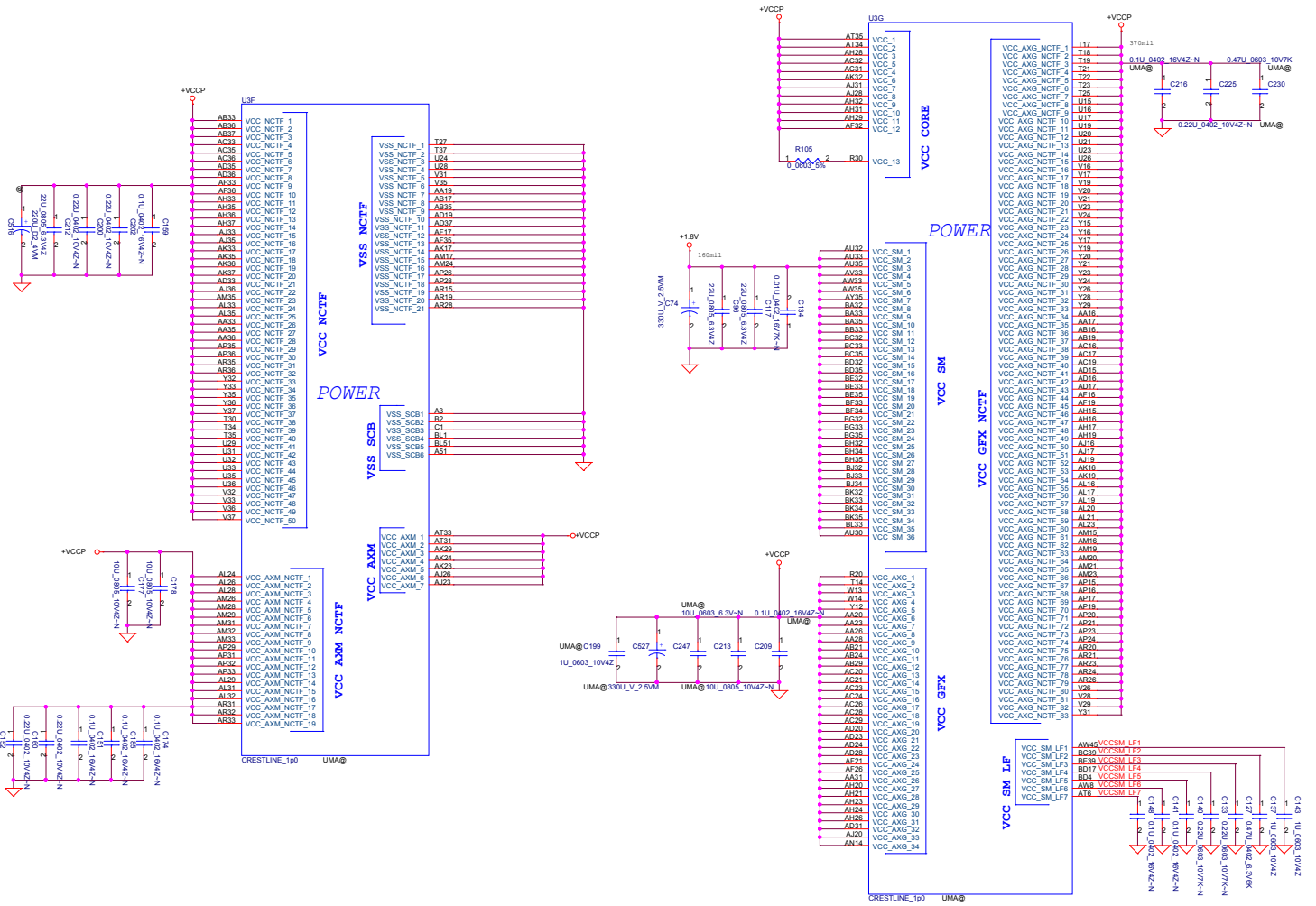


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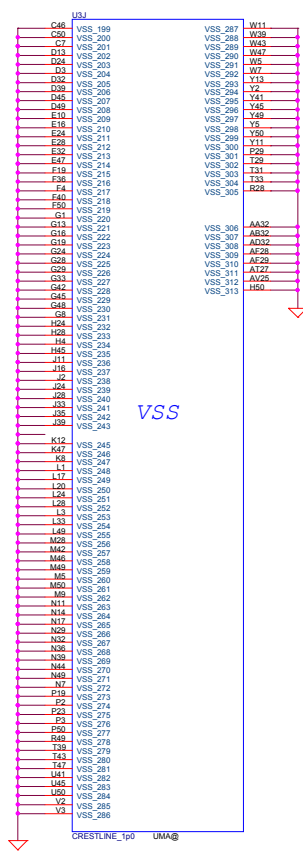
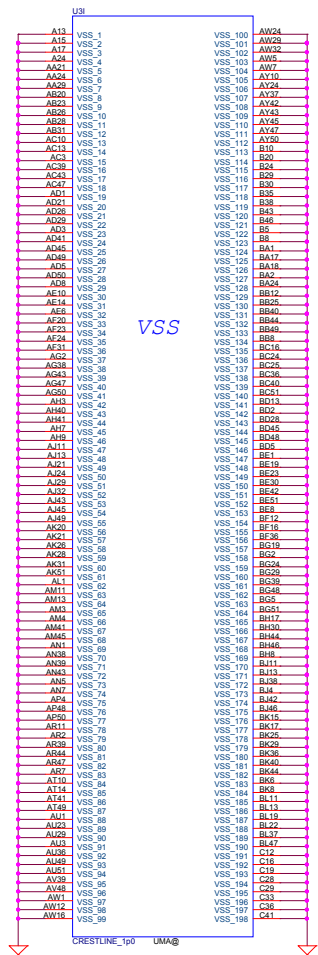
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Title: CRESTLINE(3/6)-VGA/LVDS/TV
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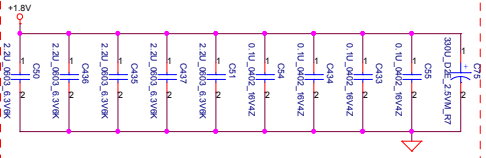
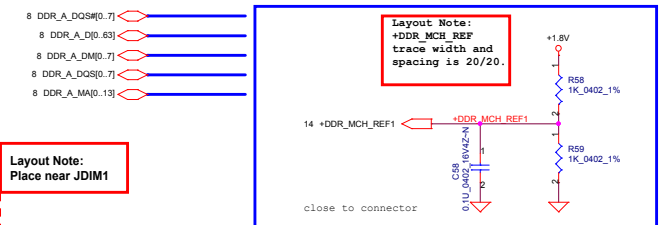
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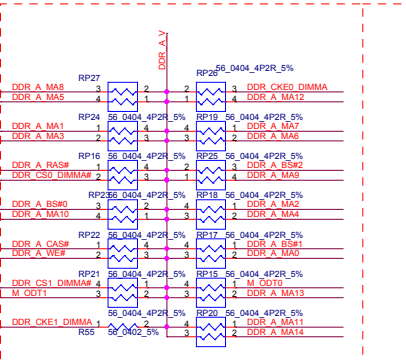
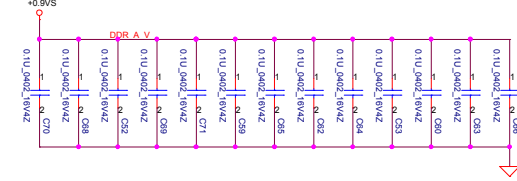
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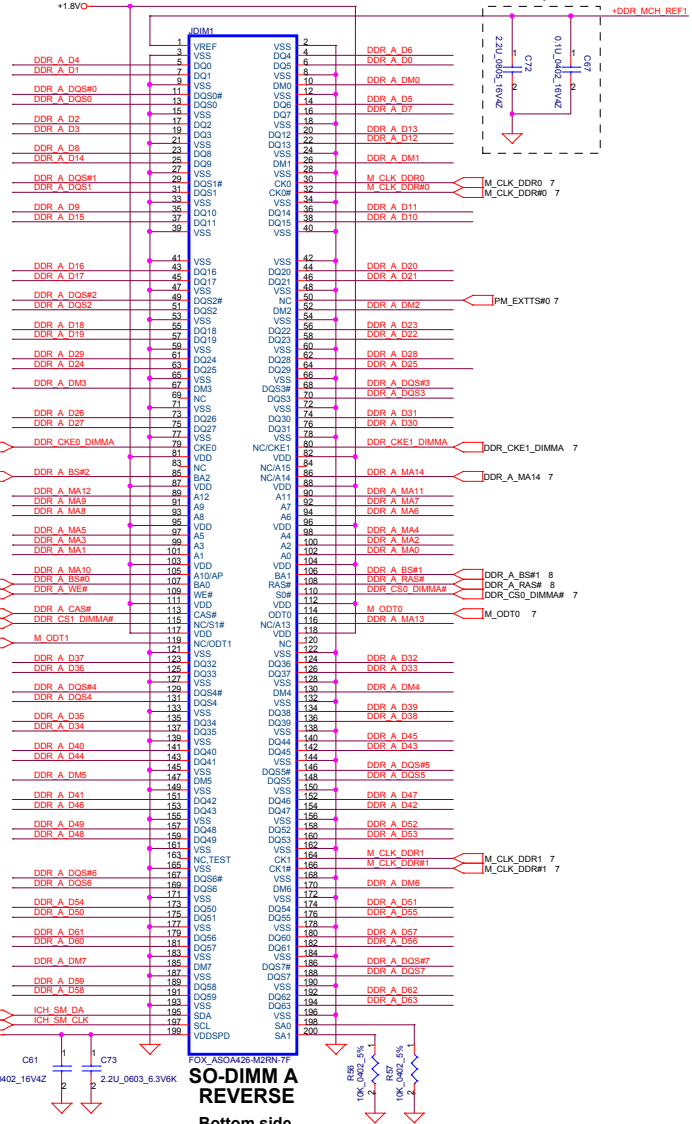
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Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely J41, all trace length Max=1.5"



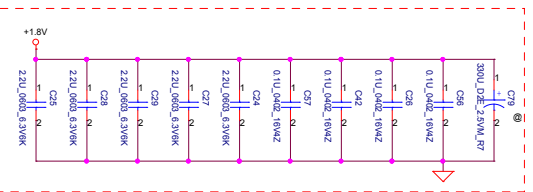
Close to VREF pins of SO-DIMM

SO-DIMM A REVERSE
Bottom side

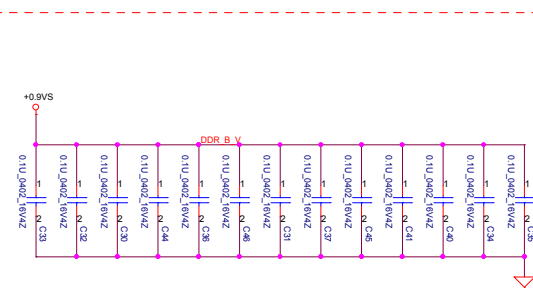
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Document Number
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				13 of 51

- 8 DDR_B_DQS#0[0..7]
- 8 DDR_B_D0[0..63]
- 8 DDR_B_DM[0..7]
- 8 DDR_B_DQS0[0..7]
- 8 DDR_B_MA[0..13]

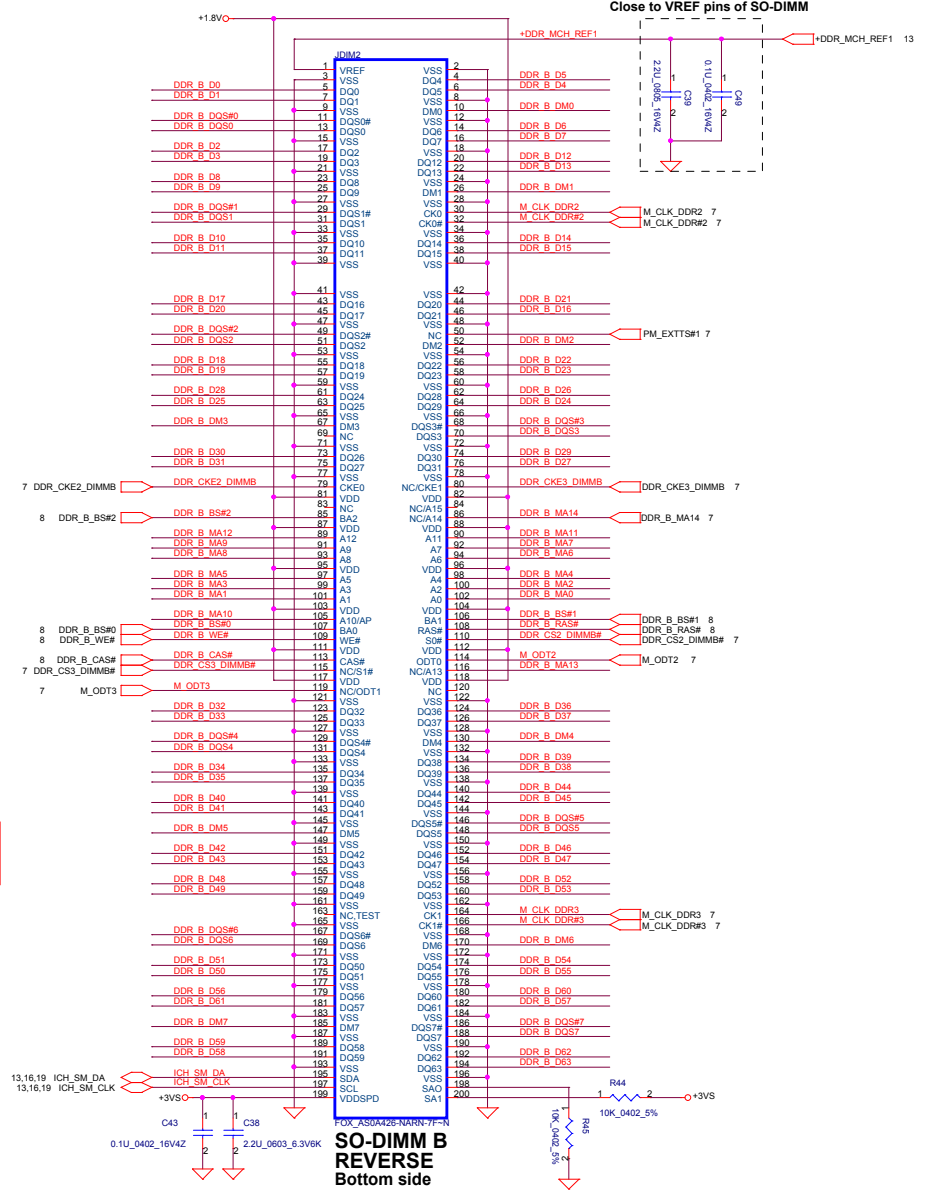
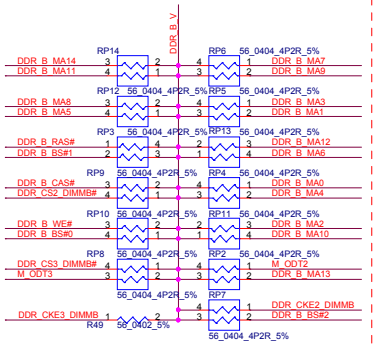
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

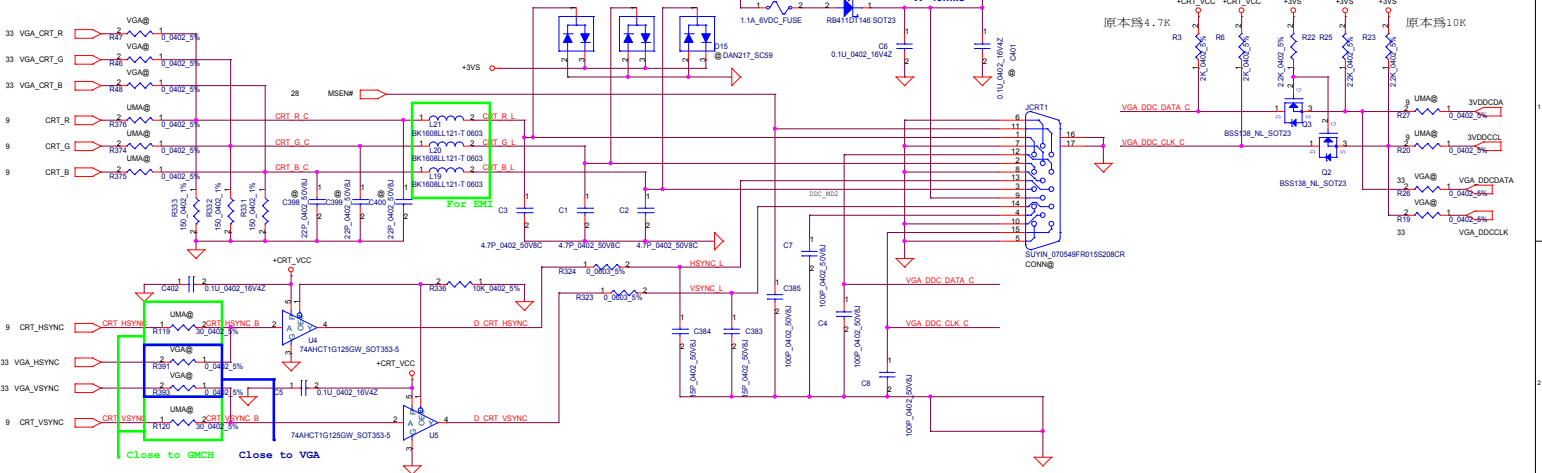


Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"

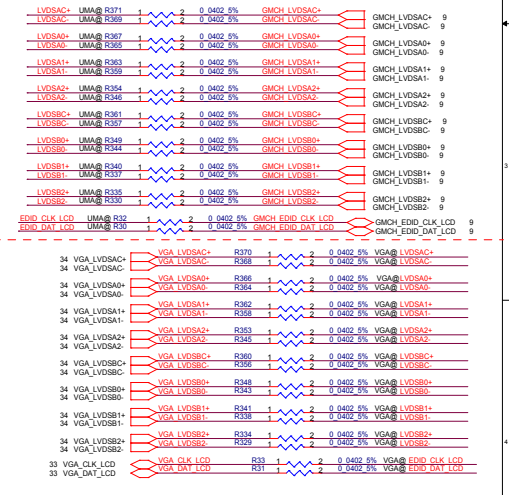
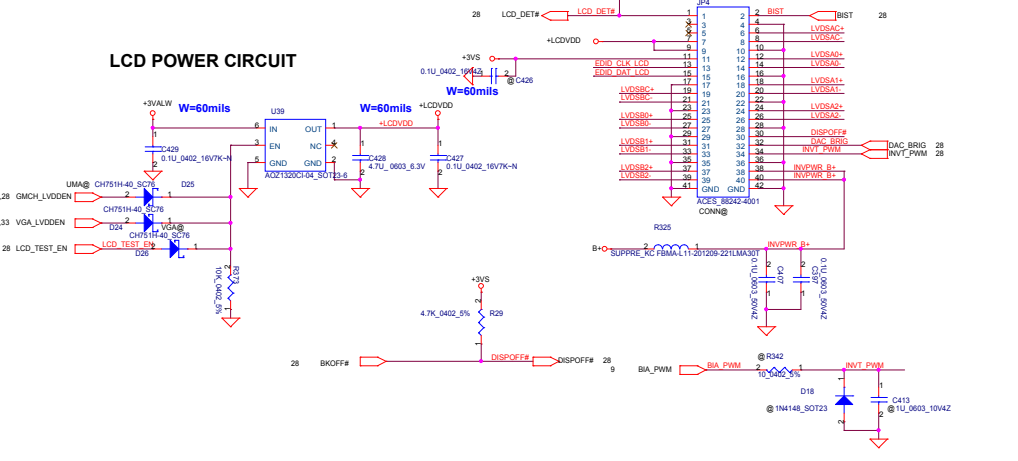


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CRT

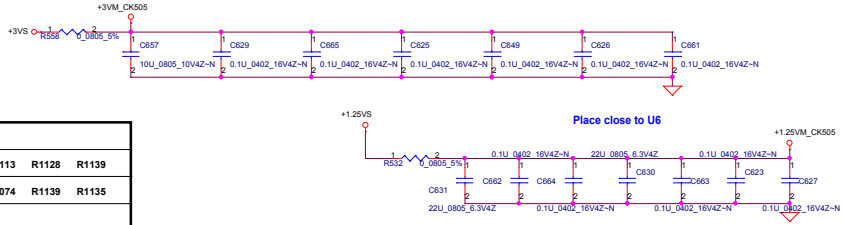


LCD



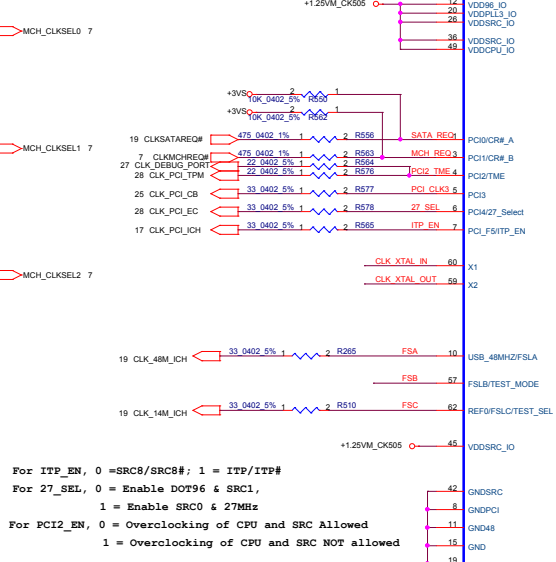
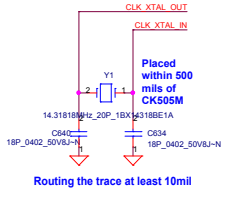
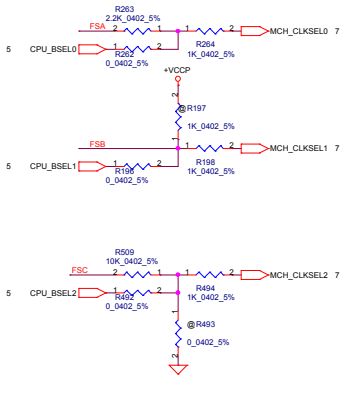
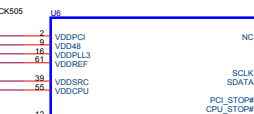
Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Rev
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Compal Electronics, Inc. CRT CONN/LCD CONN				1.0
Document Number	LA-4121P			Rev
Date	Monday, March 17, 2008			Sheet 15 of 51

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	1.66	100	33.3

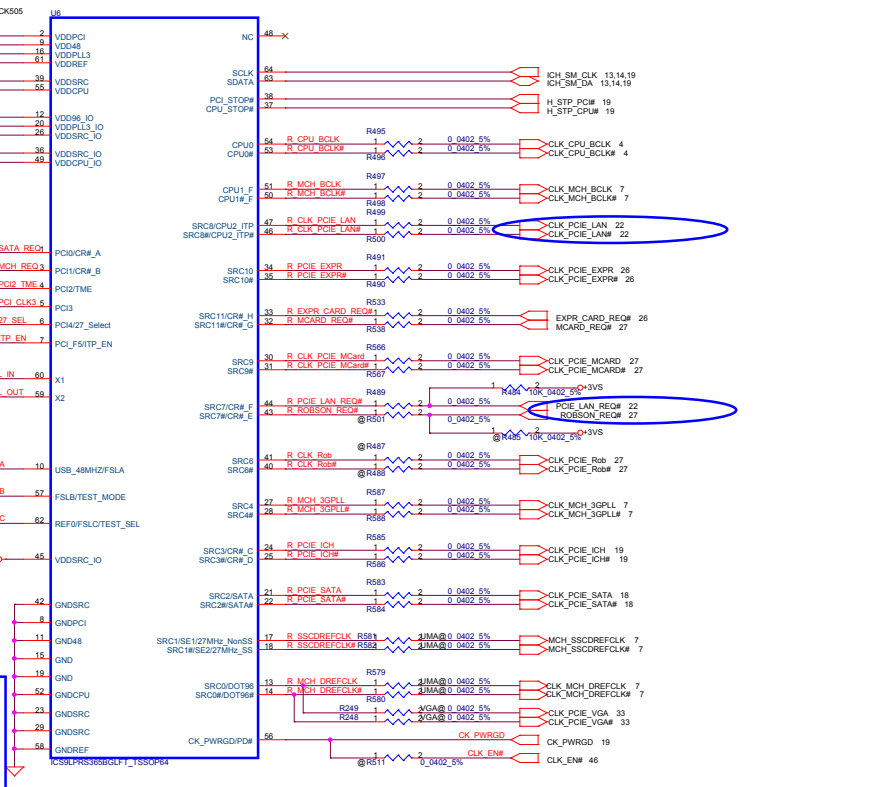


FSB Frequency Select:

CPU Driven	Stuff	R1107	R1135	R1083			
* (Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
667MHz	No Stuff	R1083	R1107	R1128	R1113	R1098	
800MHz	Stuff	R1135	R1139				
800MHz	No Stuff	R1083	R1086	R1098	R1128		

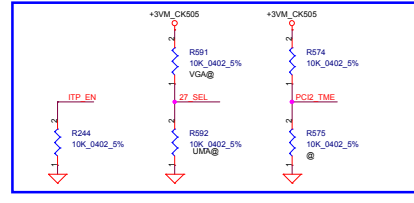


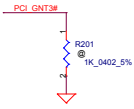
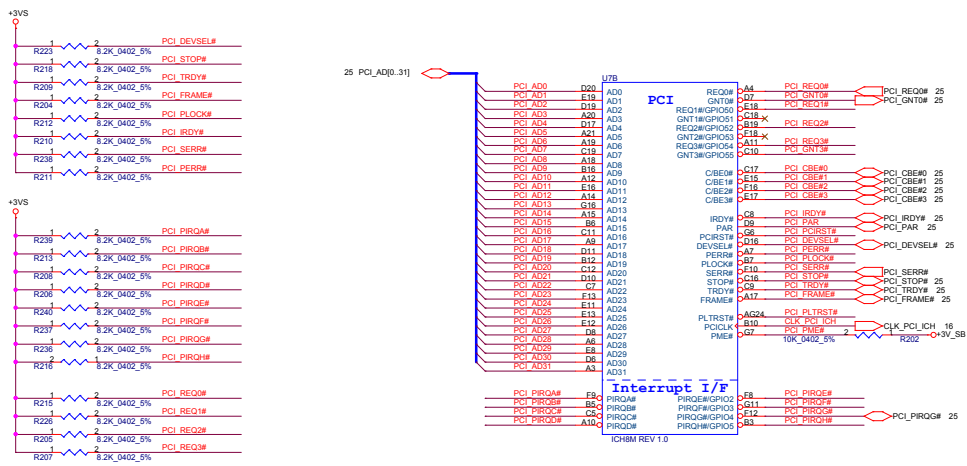
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1, 1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed, 1 = Overclocking of CPU and SRC NOT allowed



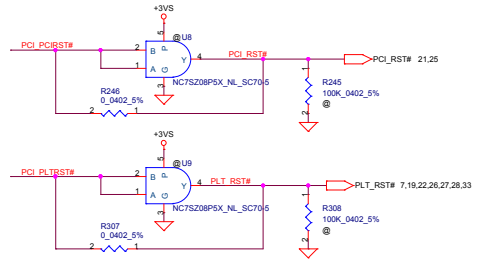
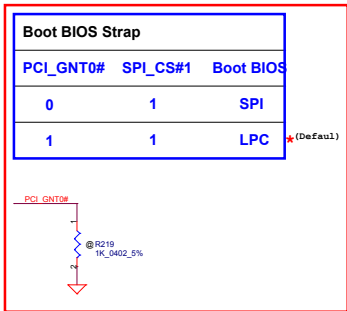
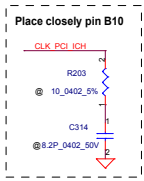
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Issued Date	2007/1/15	Deciphered Date	2008/1/15
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Routing the trace at least 10mil





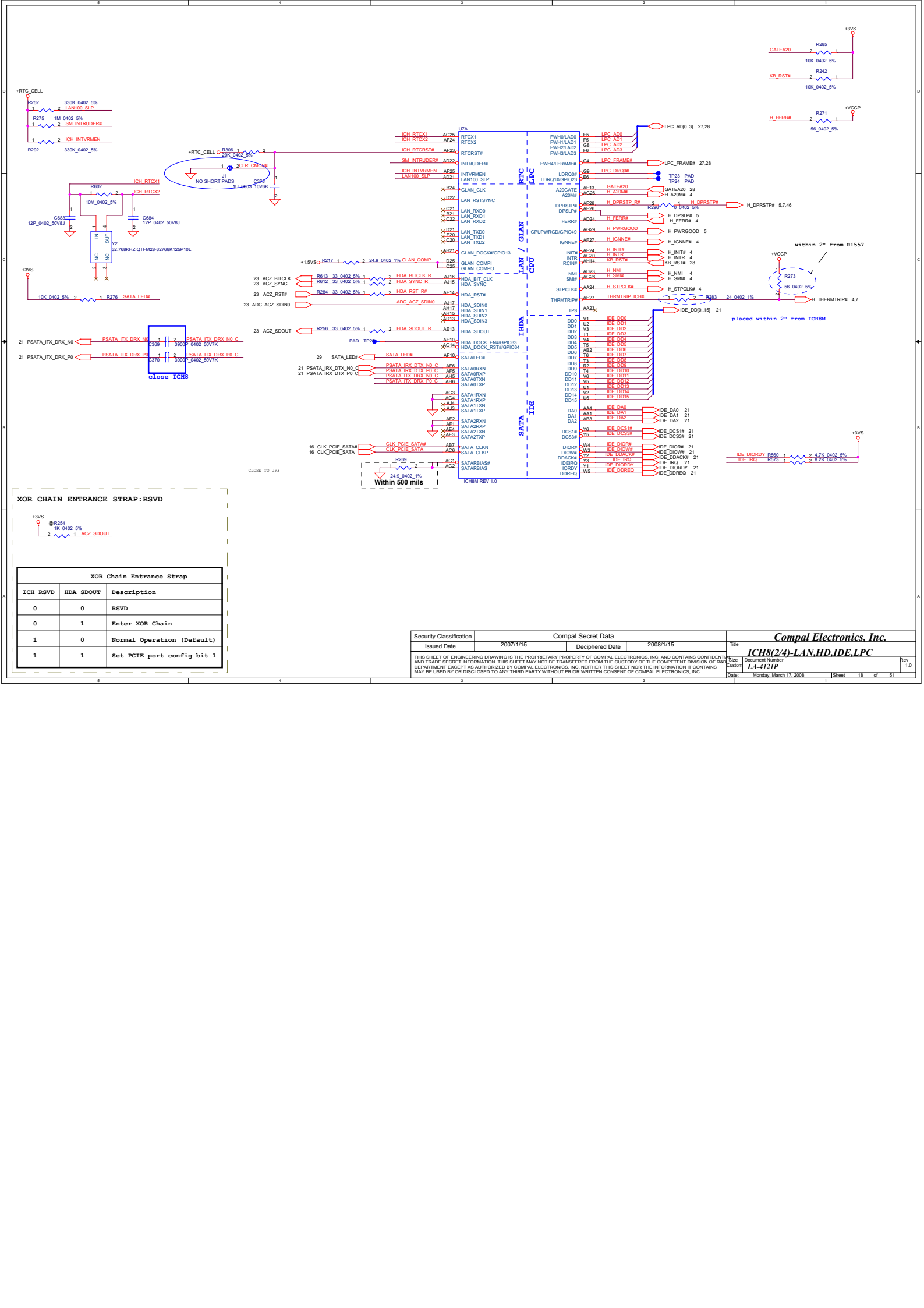
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	ICH8(I/A)-PCI/INT
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Size	Customer	Document Number	Rev	Date	Sheet
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DELL CONFIDENTIAL

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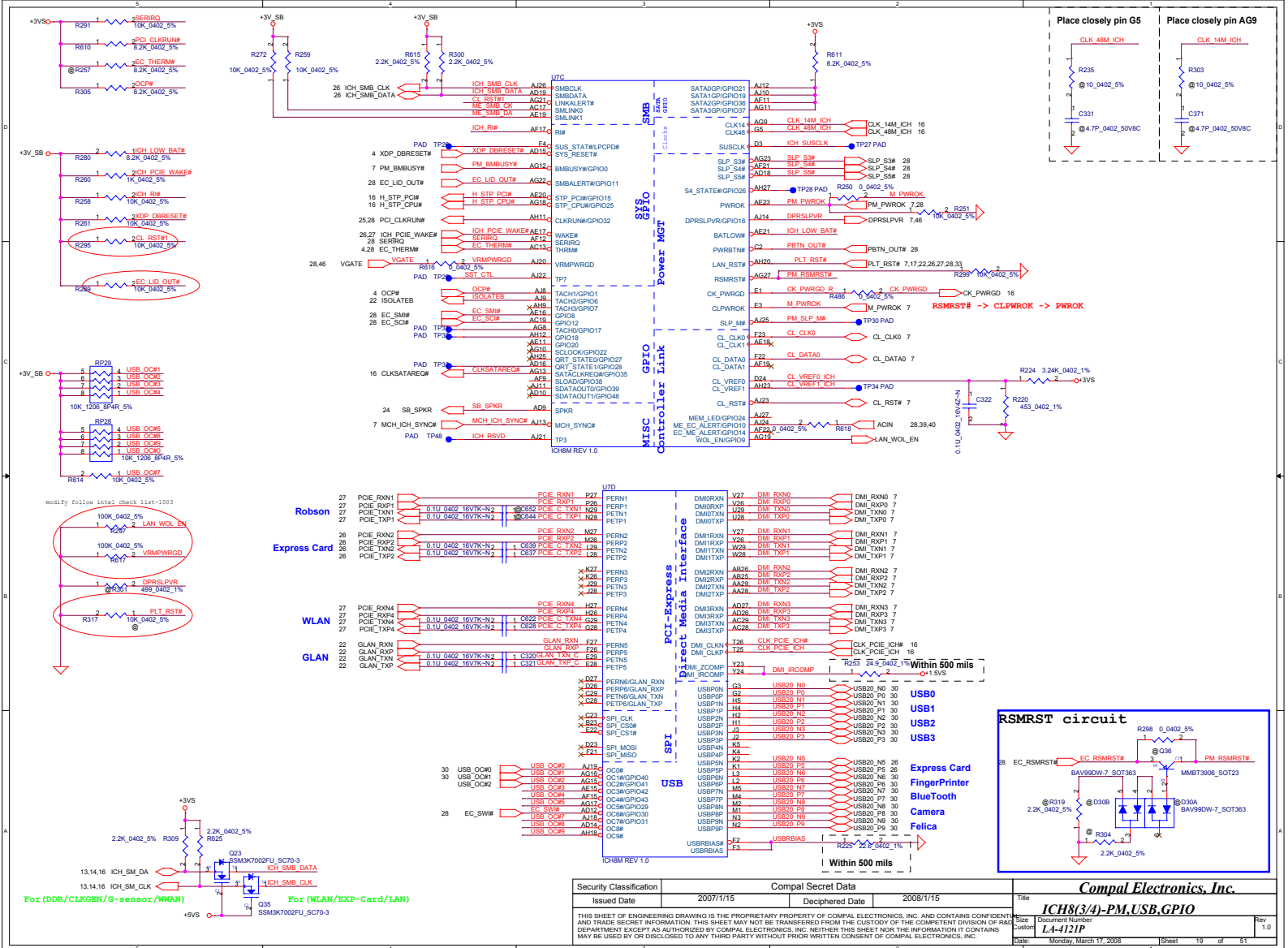


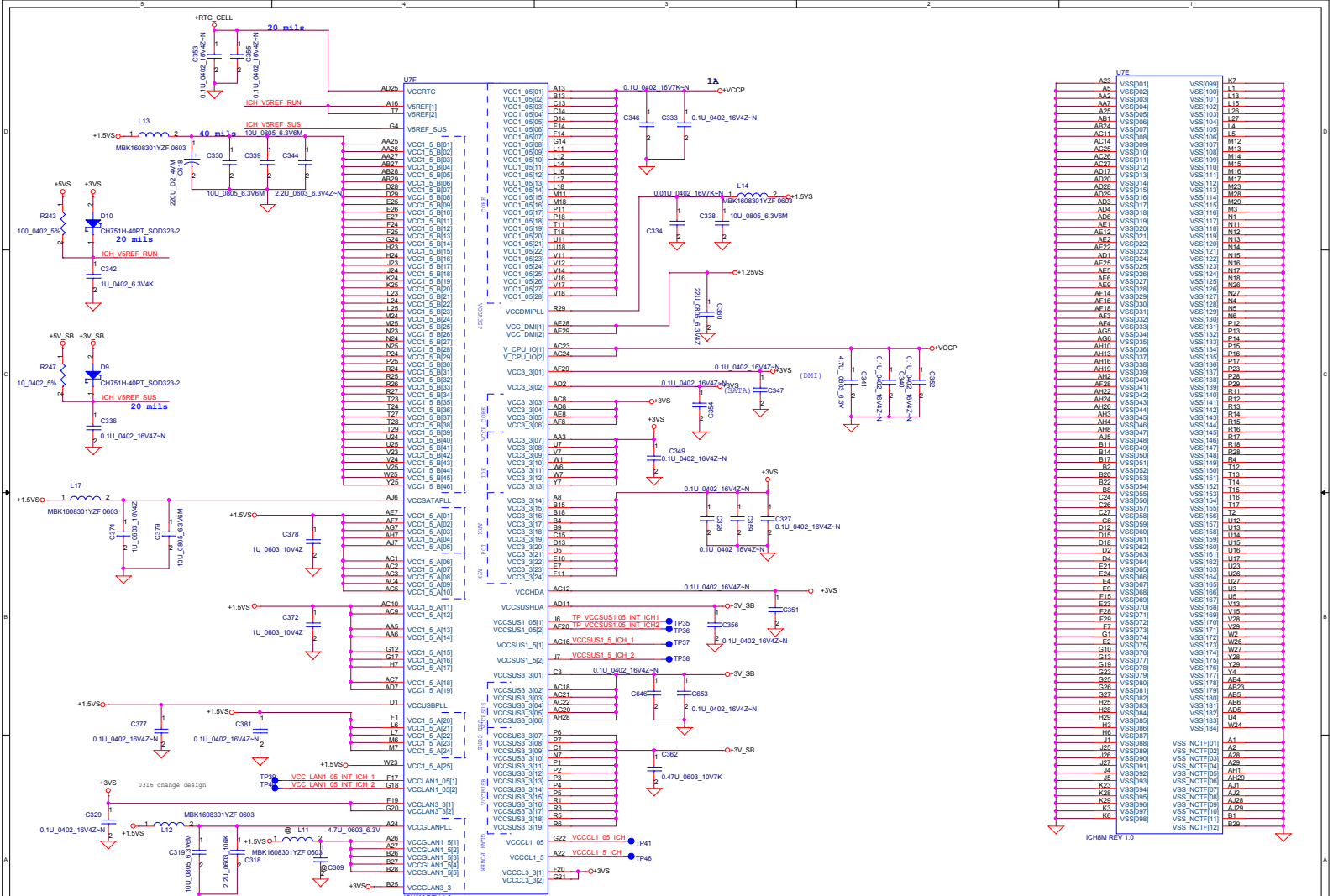
XOR CHAIN ENTRANCE STRAP:RSVD

+3VS @R254
1K_0402_5%
1
2 ACZ_SDOUT

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

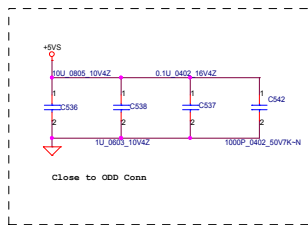
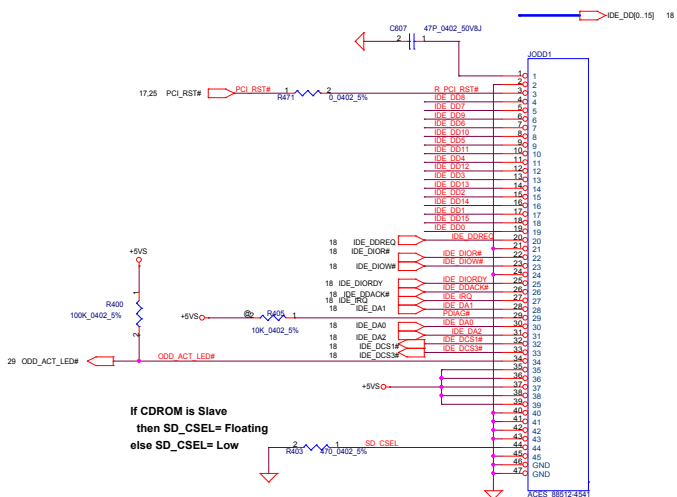
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15
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			Rev 1.0 Sheet 18 of 51





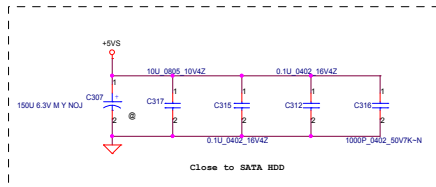
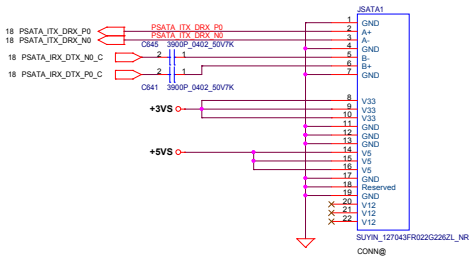
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Issued Date	2007/1/15		Deciphered Date	2008/1/15	
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Title	IC8H(44)-POWER&GND			Rev	1.0
Customer	LA-412P			Date	Monday, March 17, 2008
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CDROM CONN



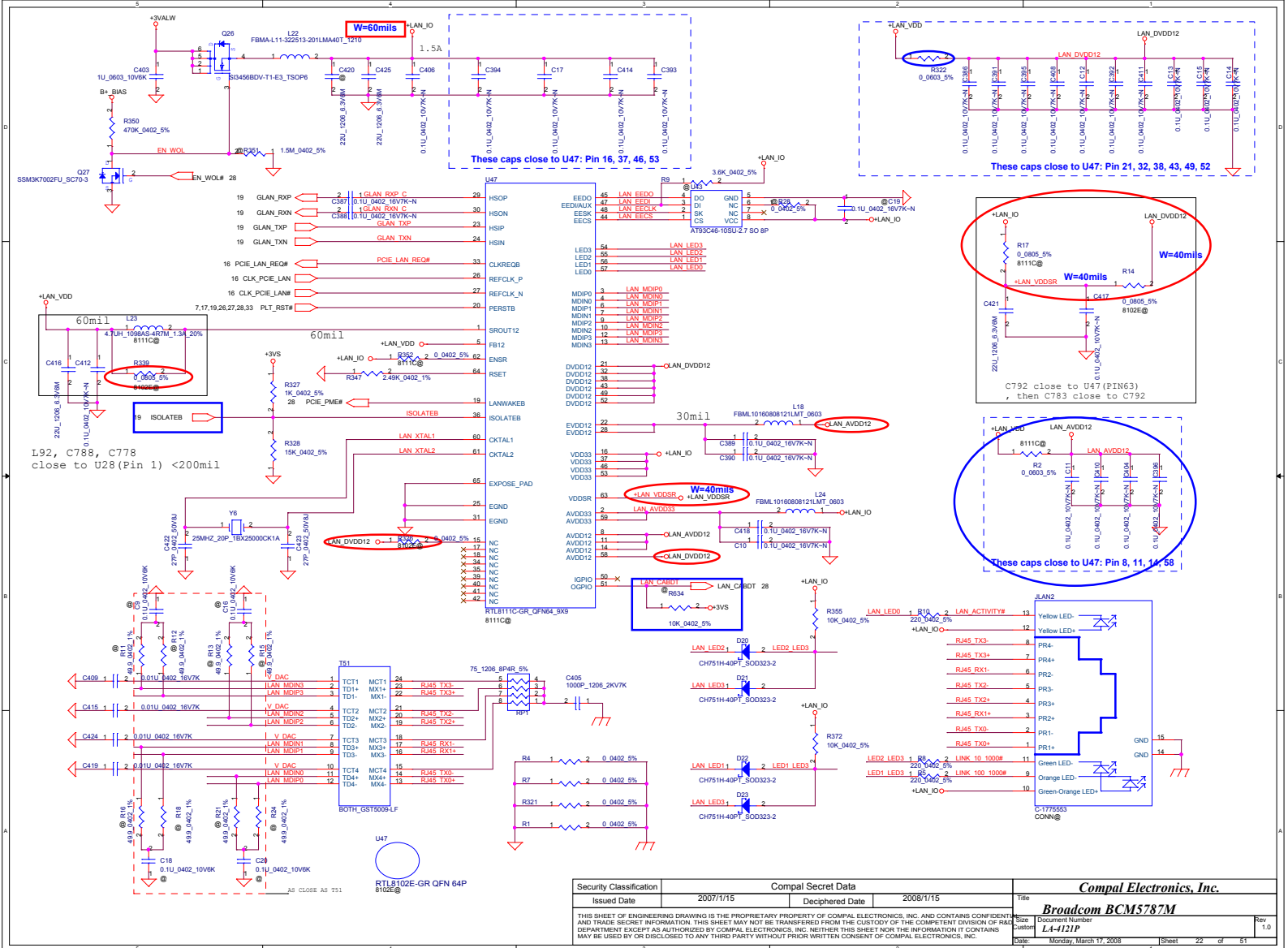
If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low

SATA HDD CONN

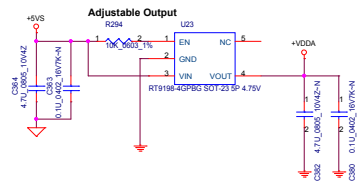


then SD_CSEL= Floating
else SD_CSEL= Low

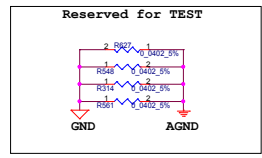
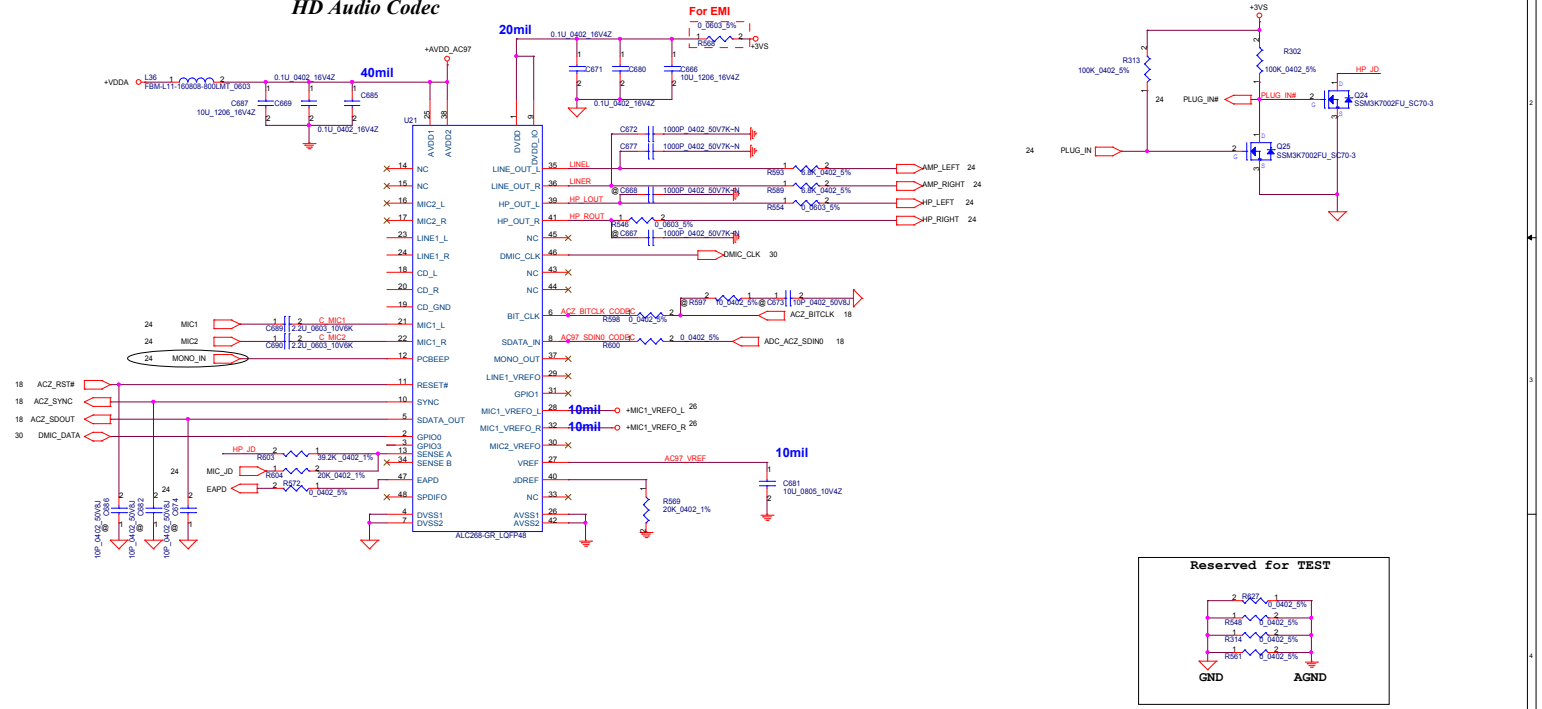
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Issued Date	2007/11/15	Deciphered Date	2008/1/15	21
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Security Classification: Compal Secret Data Issued Date: 2007/11/15 Deciphered Date: 2008/1/15			Title: HDD/CDROM Document Number: LA-4121P Date: Monday, March 17, 2008	
Size: Custom Sheet: 21 of 51			Date: Monday, March 17, 2008	



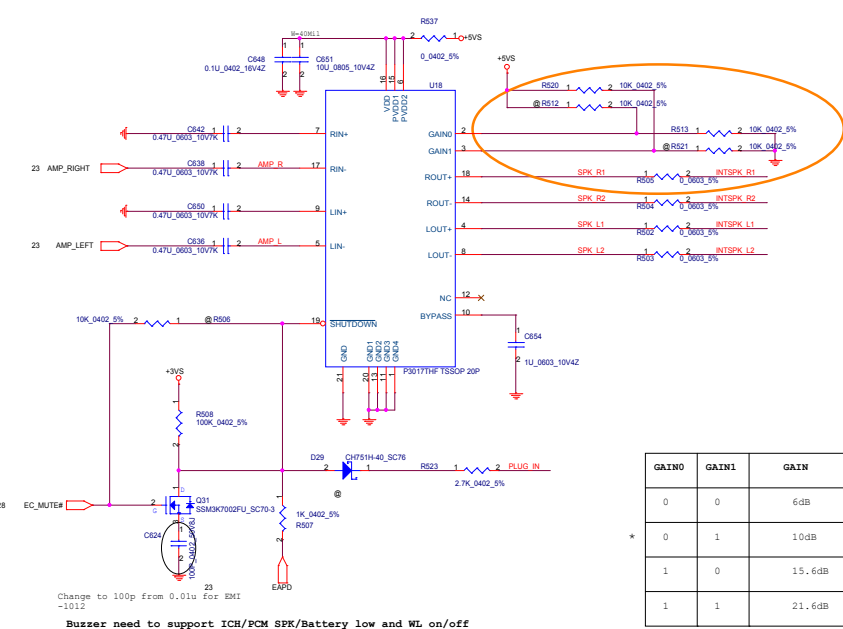
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Broadcom BCM578M
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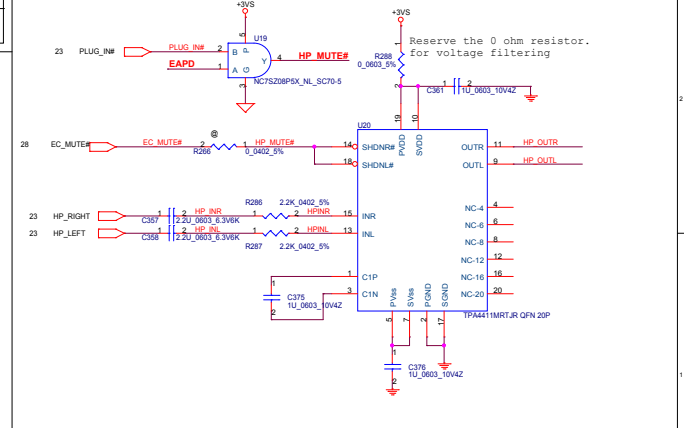
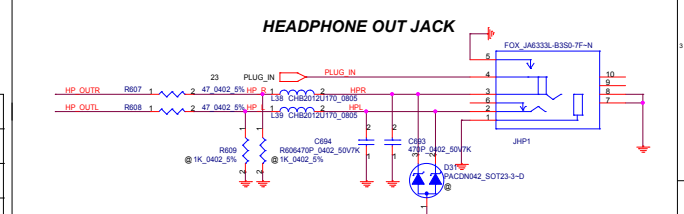
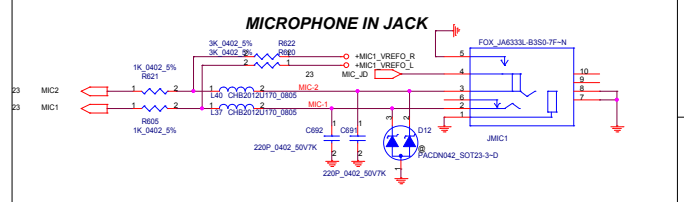
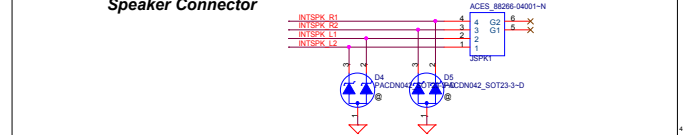
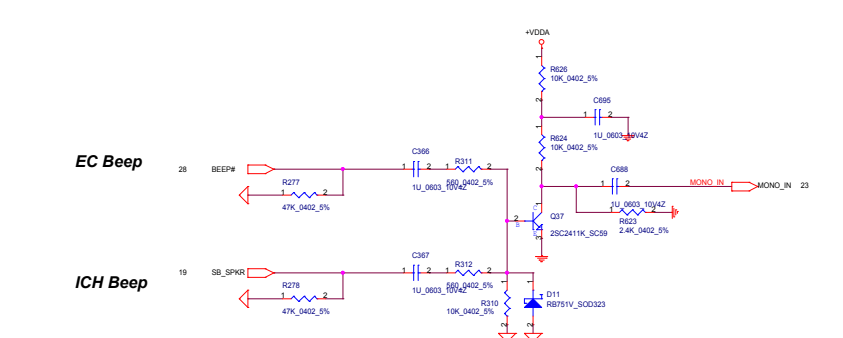
HD Audio Codec



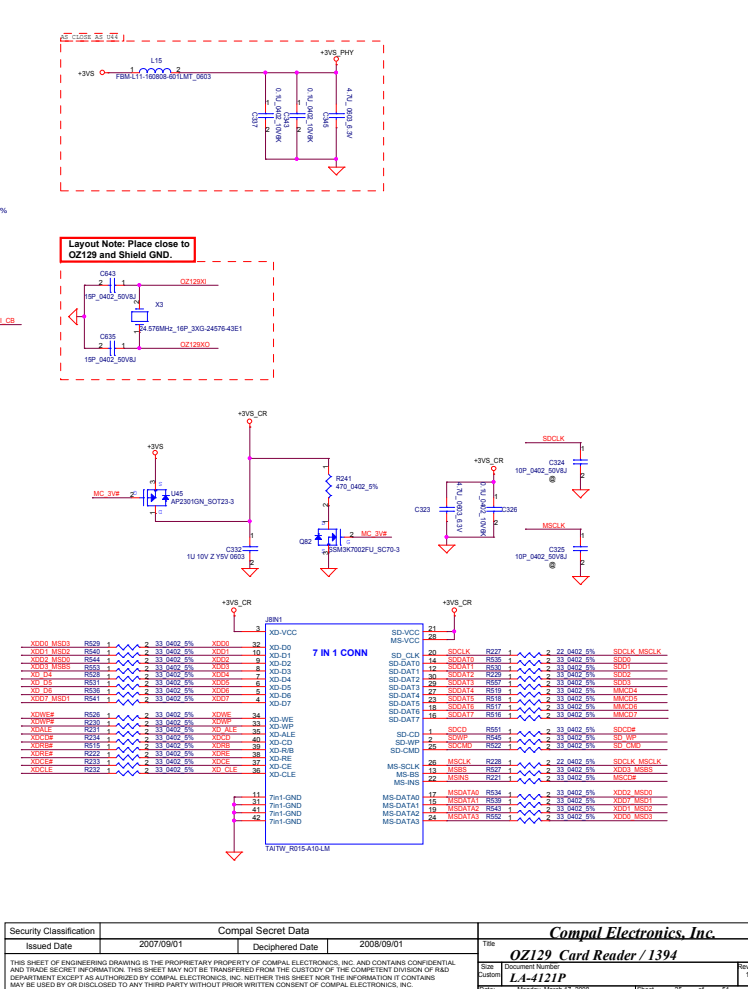
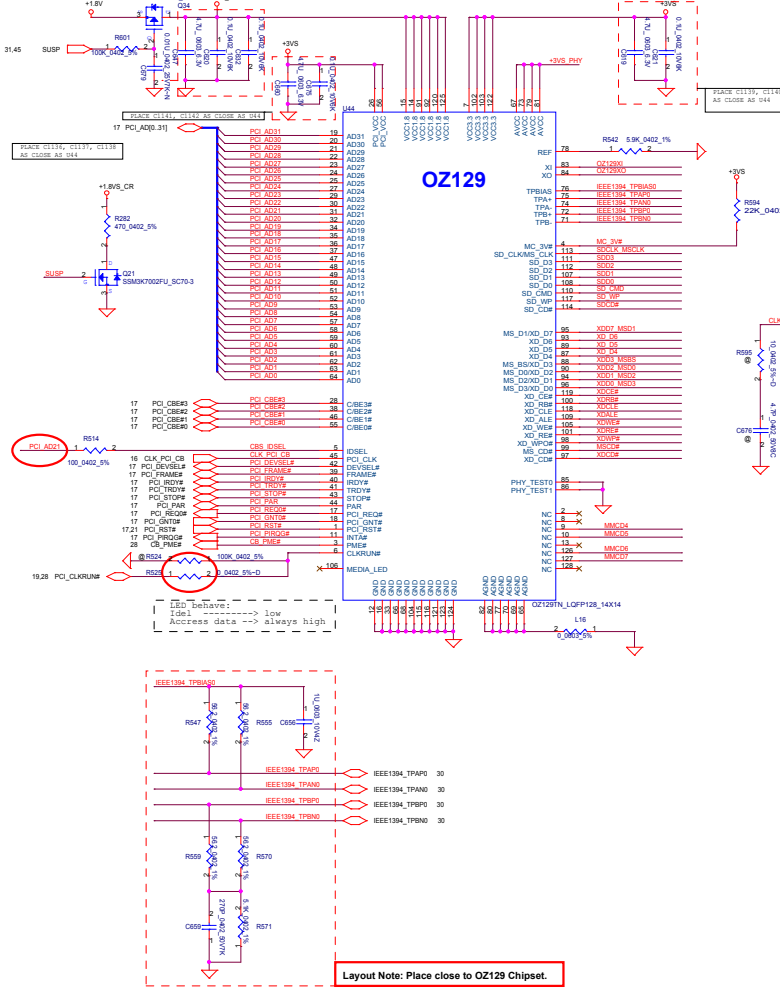
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GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

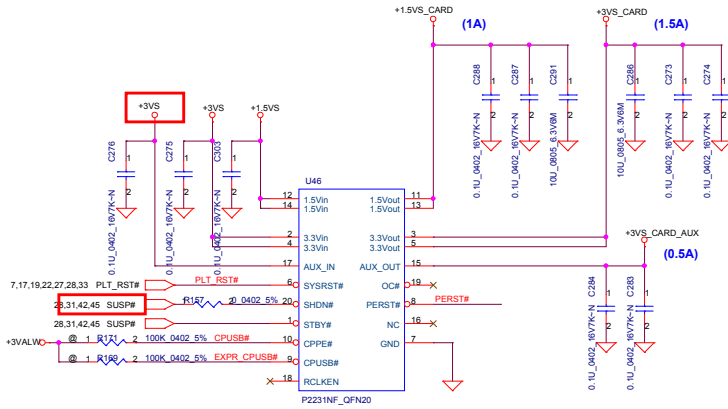


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title		AMP/Audio Jack		
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Size	Document Number	LA-4121P	Rev	1.0				
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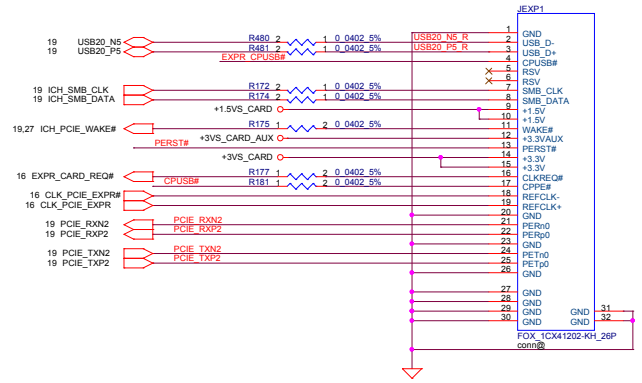


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Issued Date	2007/09/01	Deciphered Date				
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Site Location	Document Number		Title			
	L4-4121P		OZ129 Card Reader / 1394			
Date	Monday, March 11, 2008	Issue	25	of	51	

Express Card Power Switch

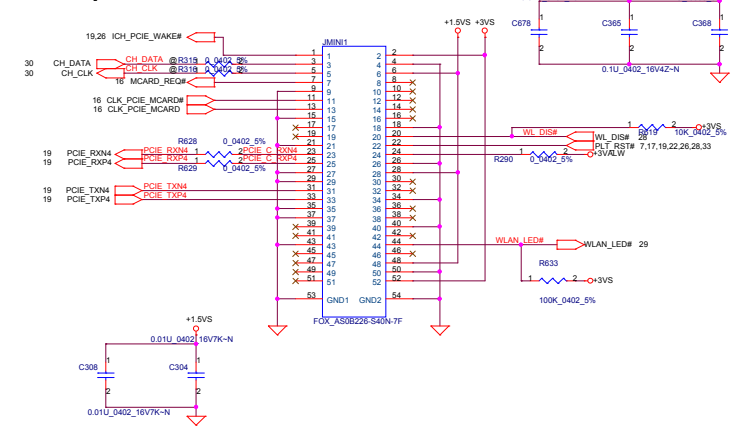


Express Card

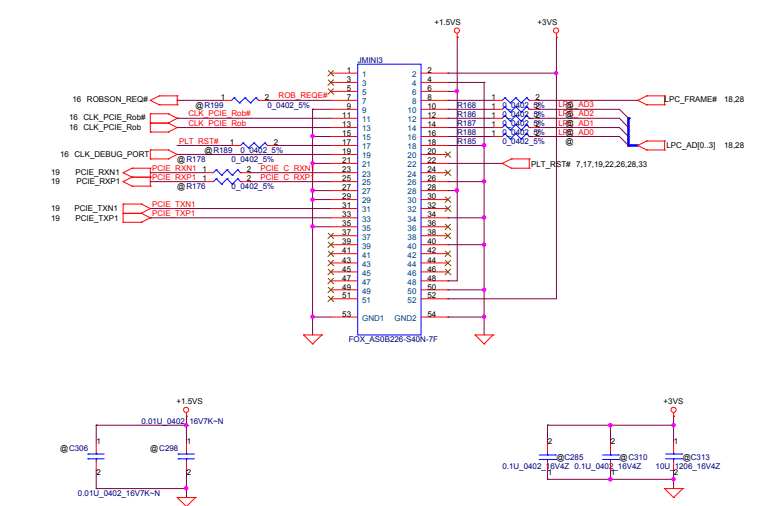


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Mini-Express Card---WLAN



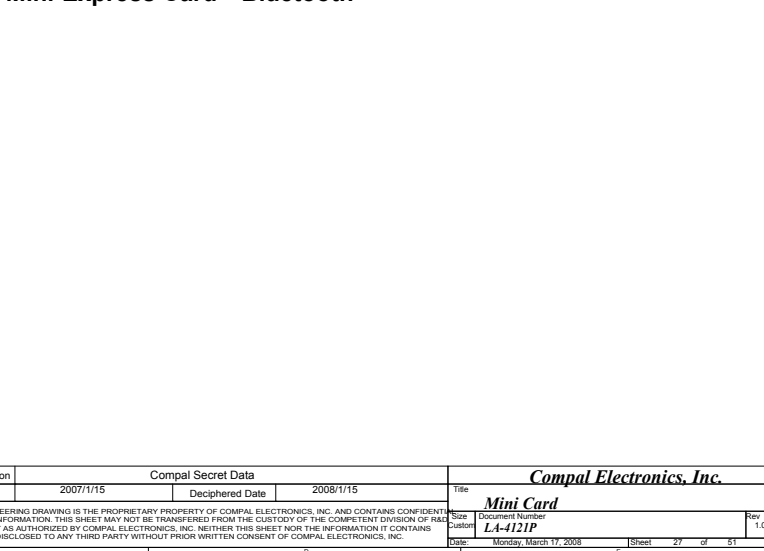
Robson



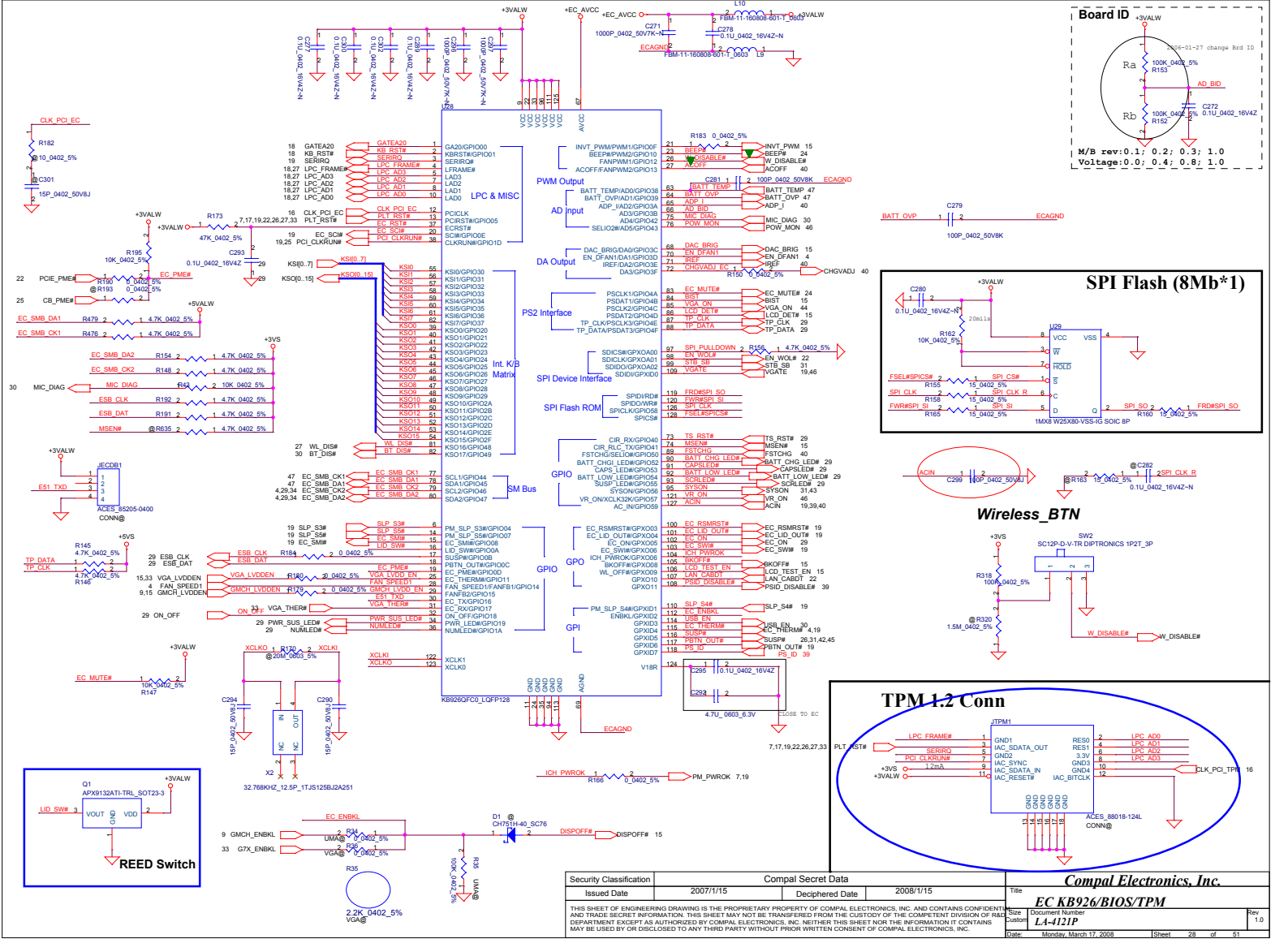
Mini-Express Card---WWAN



Mini-Express Card---Bluetooth

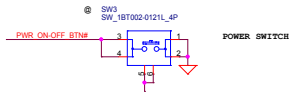
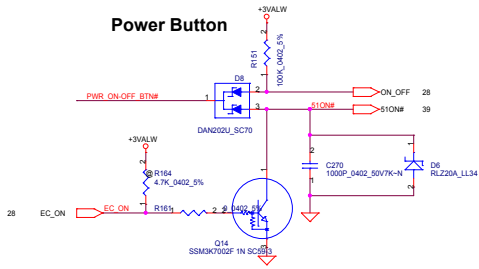


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				LA-4121P	1.0
				Date	Monday, March 17, 2008
				Sheet	27 of 51

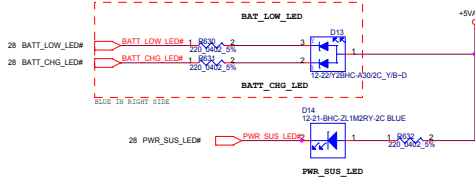
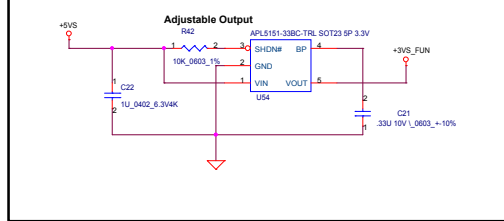


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				L4-121P
				Rev 1.0
				Date: Monday, March 17, 2008
				Sheet 28 of 51

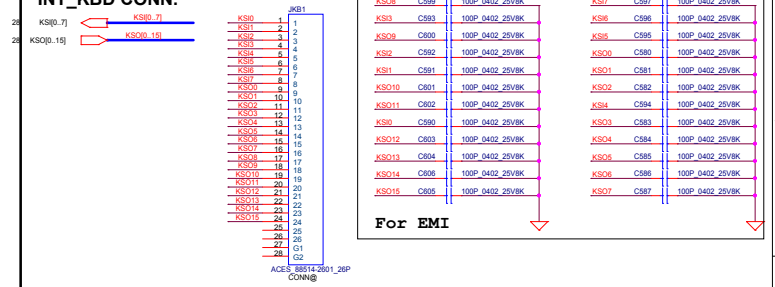
Power Button



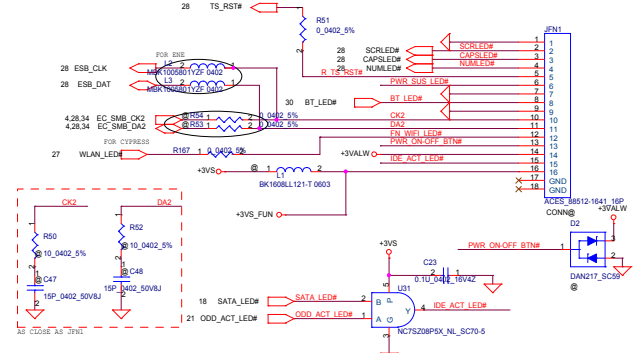
Regulator for ENE sensor



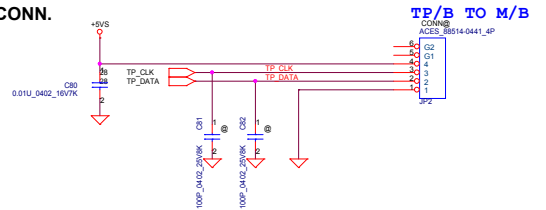
INT_KBD CONN.



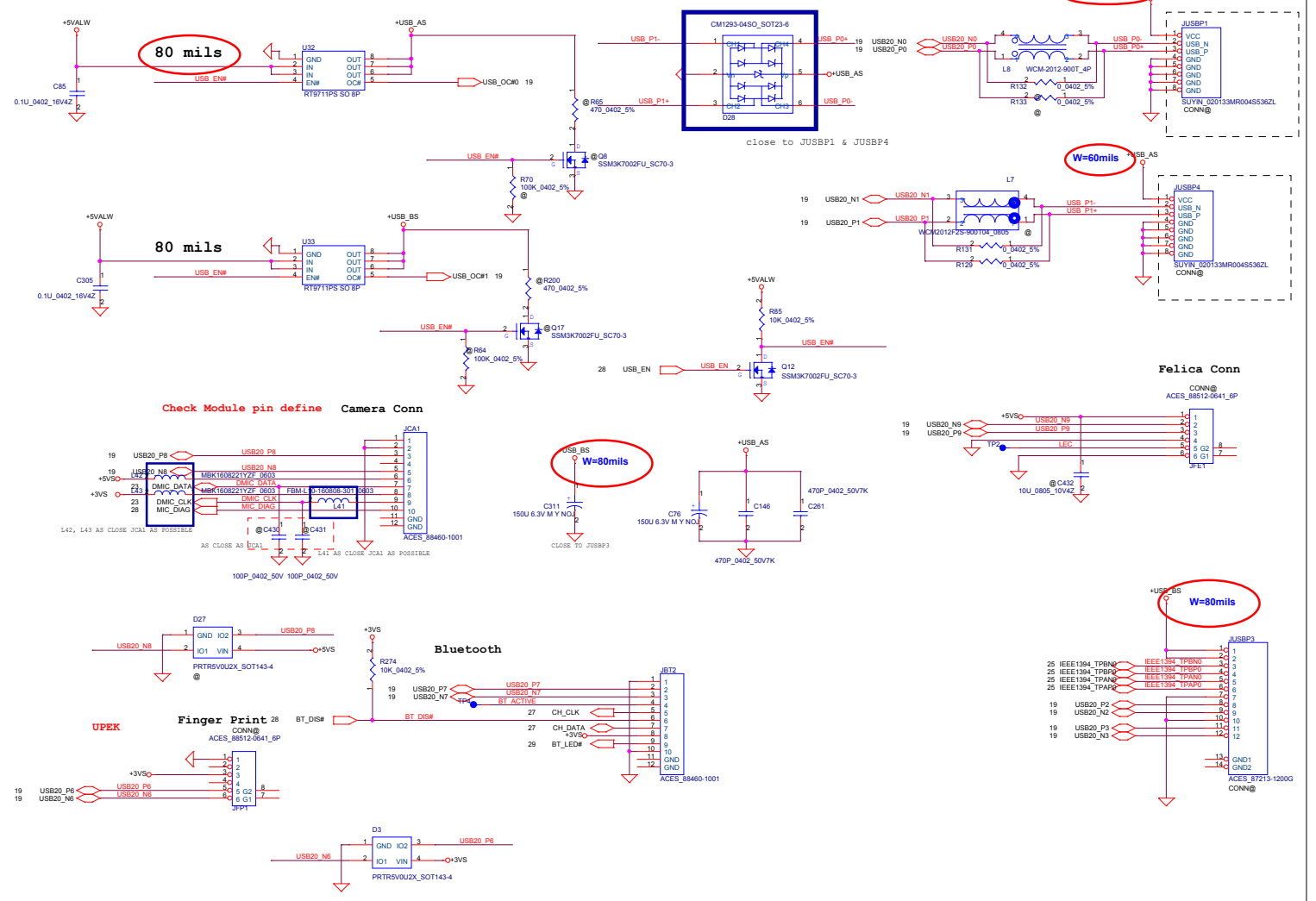
Function/B CONN.



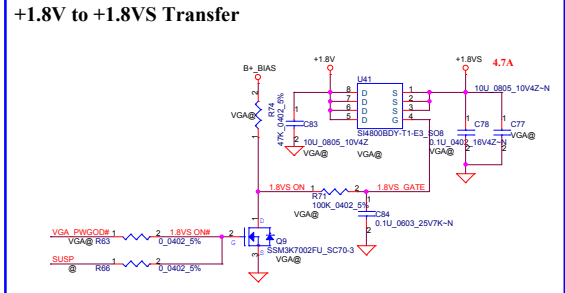
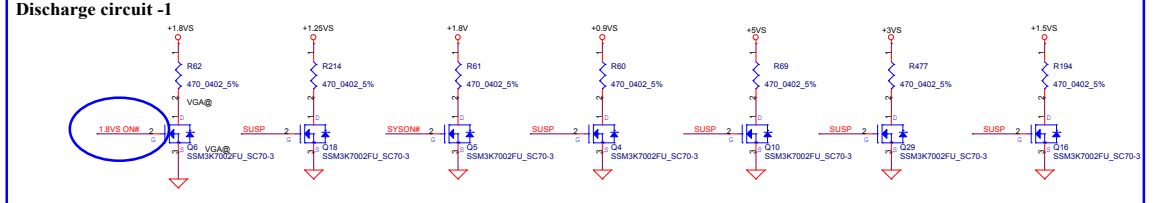
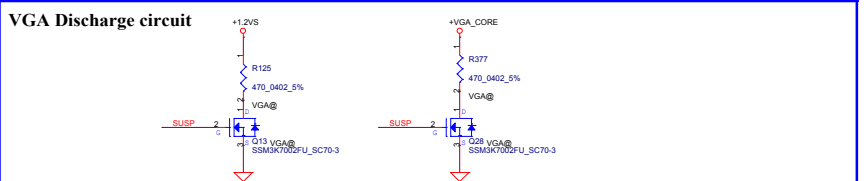
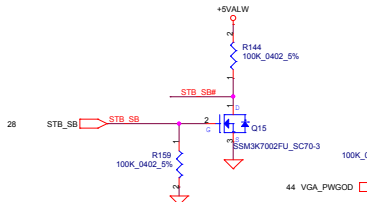
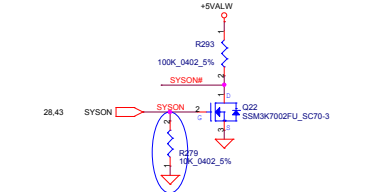
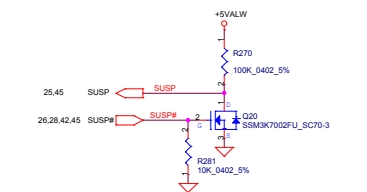
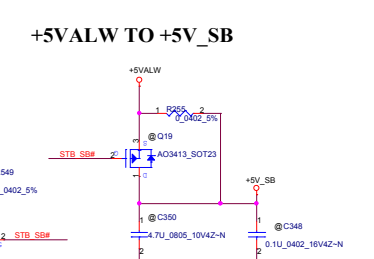
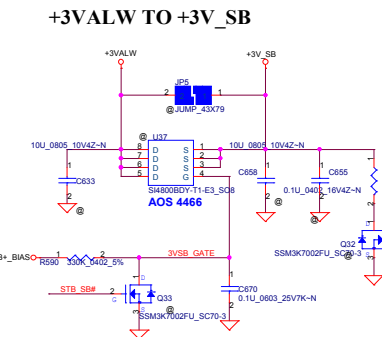
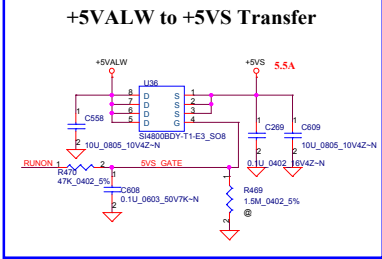
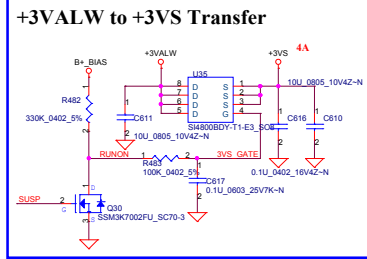
Touch PAD/B CONN.



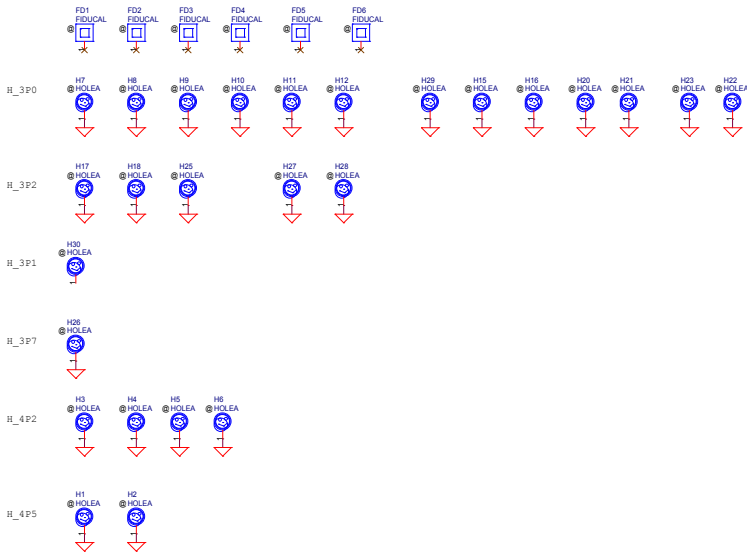
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Sheet	30	of	51	Rev
				1.0

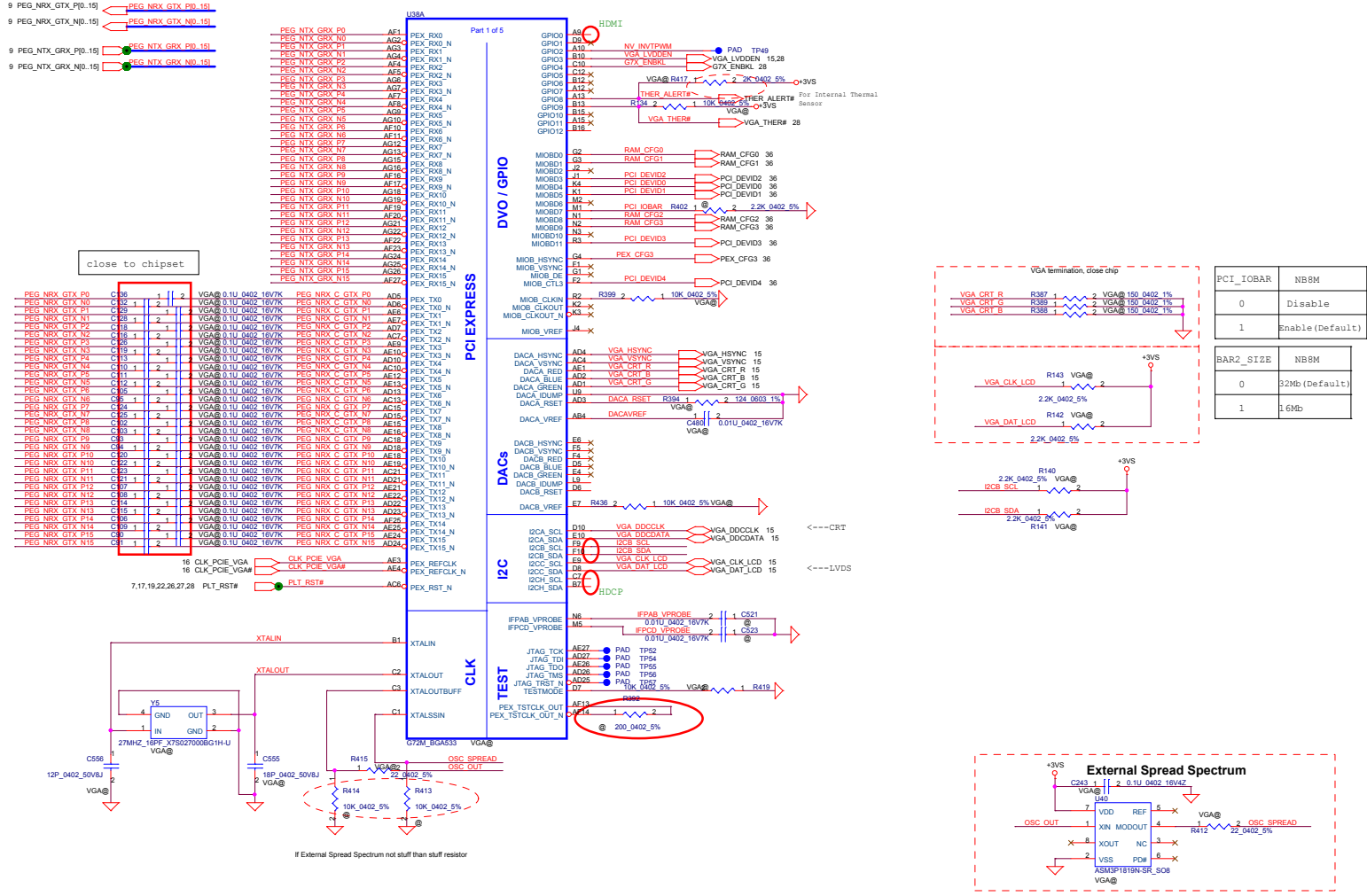


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Size	Document Number	Date	Monday, March 17, 2008	Sheet	31 of 51
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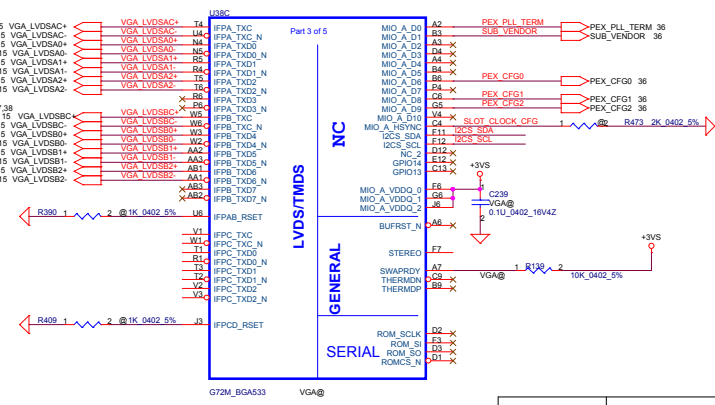
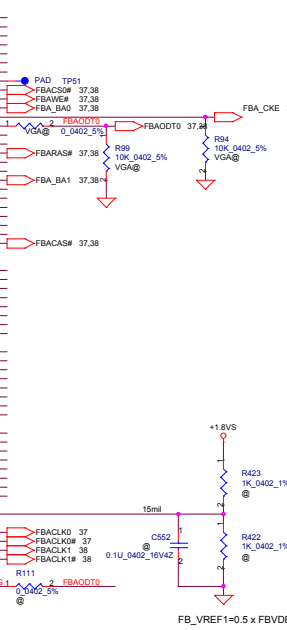
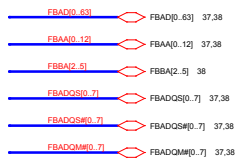


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9 PEG_NRX_GTX_PD[0..15] ← PEG_NRX_GTX_PD[0..15]
 9 PEG_NRX_GTX_ND[0..15] ← PEG_NRX_GTX_ND[0..15]
 9 PEG_NTX_GRX_PD[0..15] ← PEG_NTX_GRX_PD[0..15]
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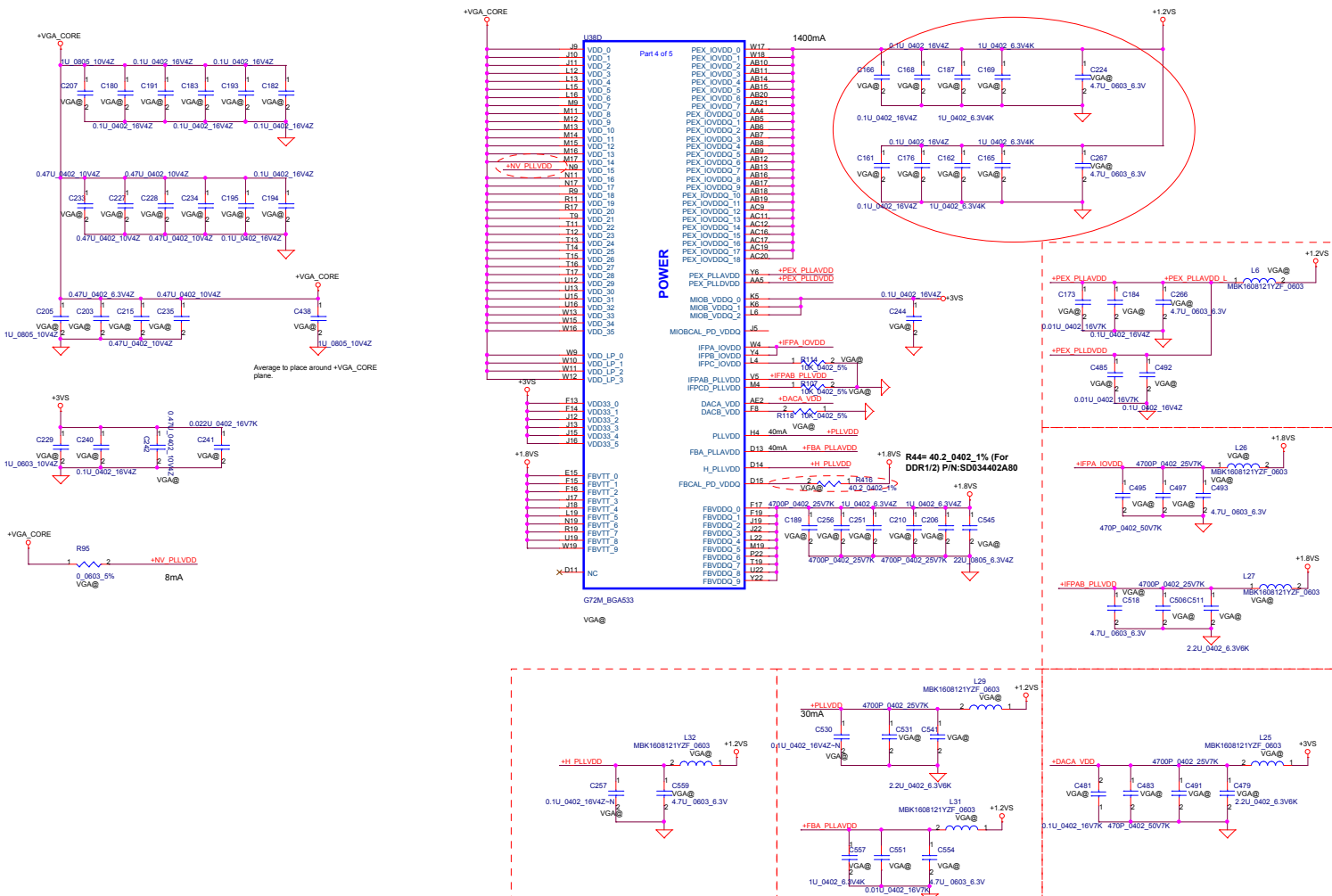


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				NB8M-GS Main
				Size
				Custom
				Date
				Monday, March 17, 2009
				Sheet
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				1.0

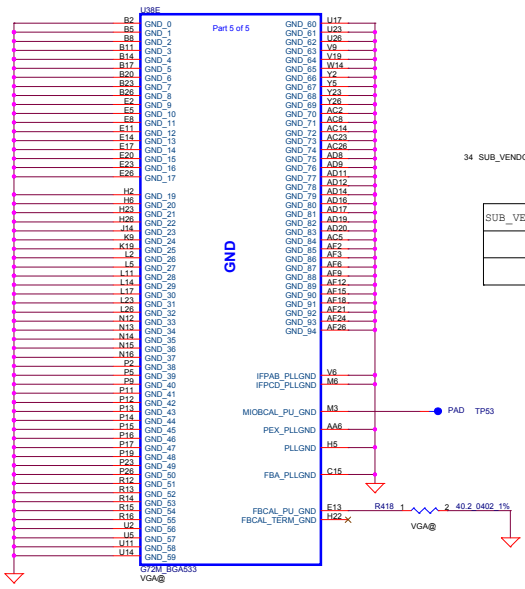


SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable (Default)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/07/10	Deciphered Date	2007/07/10	Title	
				NB8M-GS Memory	
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Size	Document Number	Rev			
Custom		1.0			
Date	Monday, March 17, 2008	Sheet	34	of 51	

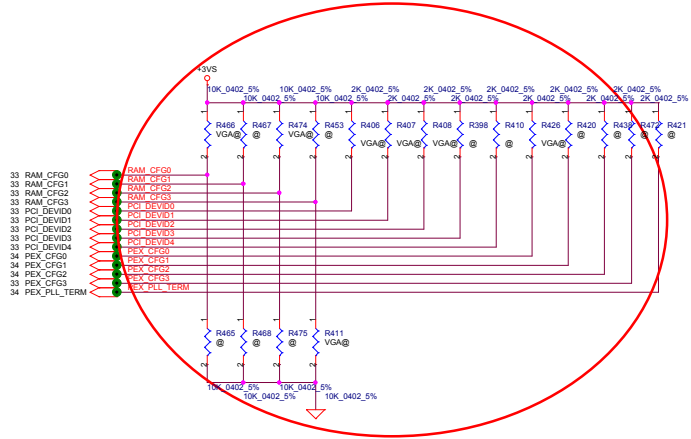


Security Classification			Compal Secret Data		Title	
Issued Date	2006/07/10	Deciphered Date	2007/07/10	NB8M-GS Power		Rev 1.0
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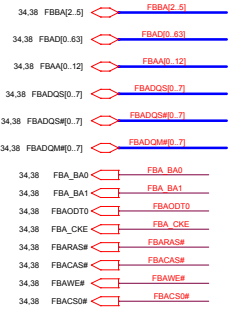
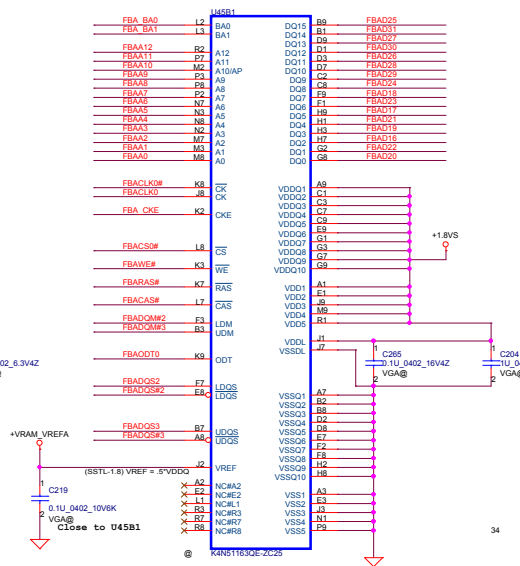
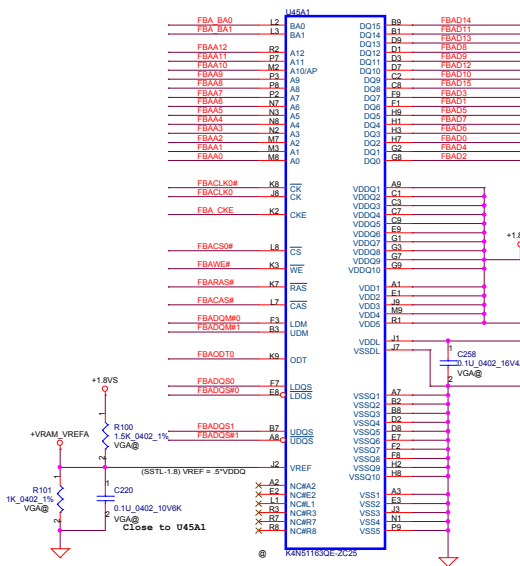
SUB_VENDOR	Description
0	NO VIDEO BIOS ROM
1	BIOS ROM is present (Default)

STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOADD0		0	
PEX_CFG[2:0]	MIOAD[19:8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	RAM_CFG[3] (Bandwidth 0=Full, 1=Half) RAM_CFG[2] (0=16M or 1=32M) RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)		
PCI_DEVID[3:0]	VIPO[5:3] MIOA_HSINC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SB : 0X0428 G72M-0x01D7 TBD/TBD	0111 1000	0111

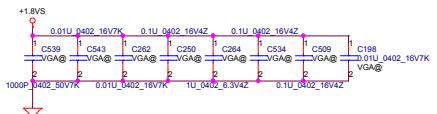


Bandwidth	RAM Type	Vendor	Package	Part Number	Manufacturer
FULL R17	32M R11	Samsung R20, R19	(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
HALF R12	16M R16	Hynix R18, R19	(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
		Infineon R18, R21	(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-Z5)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-Z8)

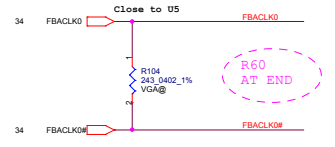
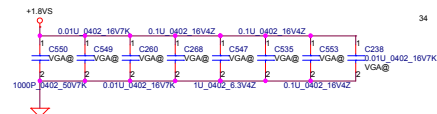
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Size	Custom	Document Number		Rev	1.0
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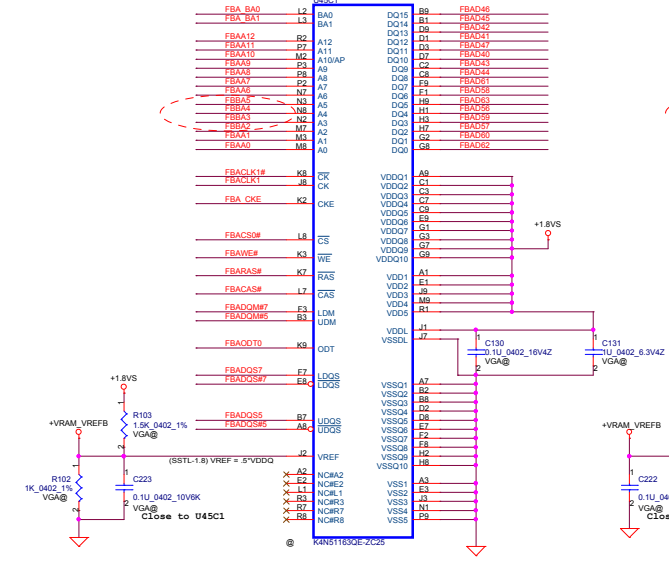
DDR2 BGA MEMORY



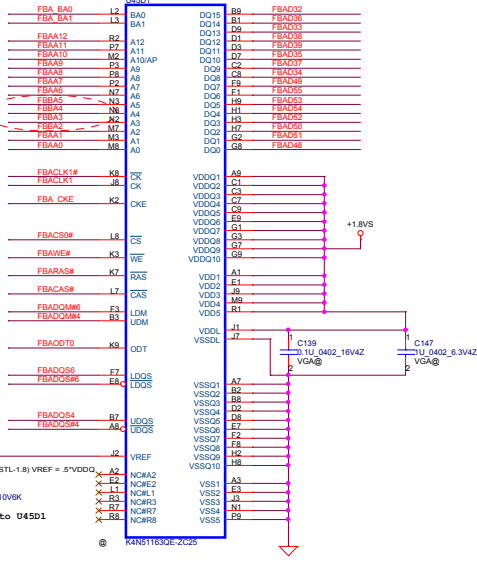
DDR2 BGA MEMORY



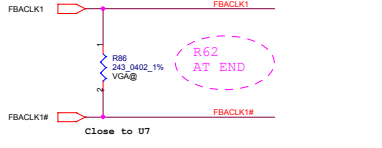
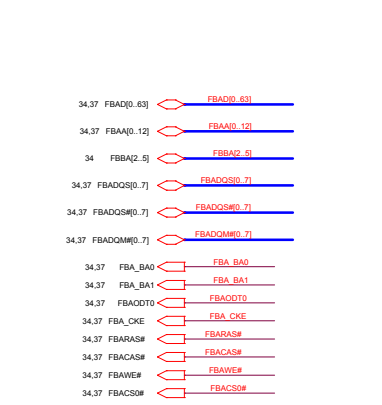
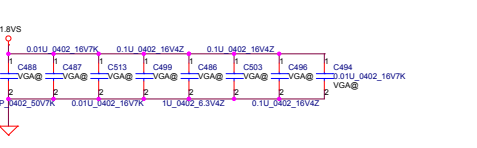
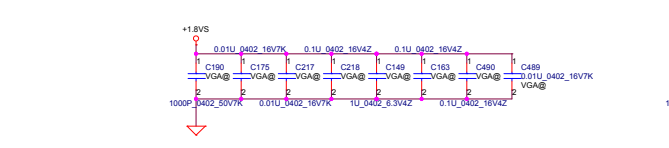
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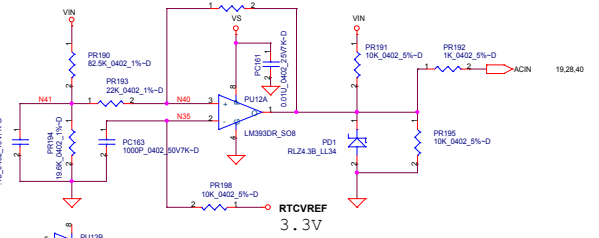
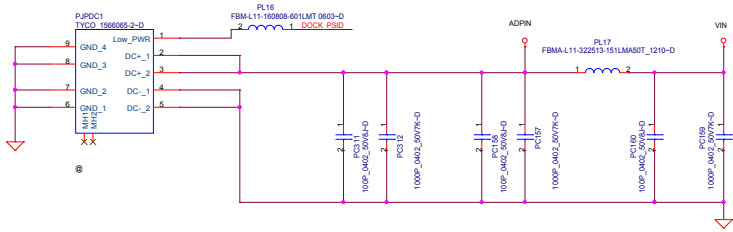
DDR2 BGA MEMORY



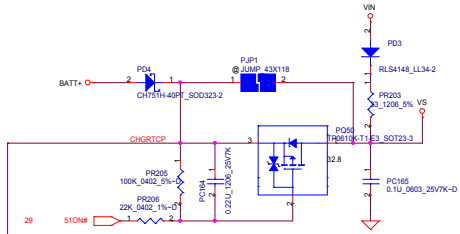
DDR2 BGA MEMORY



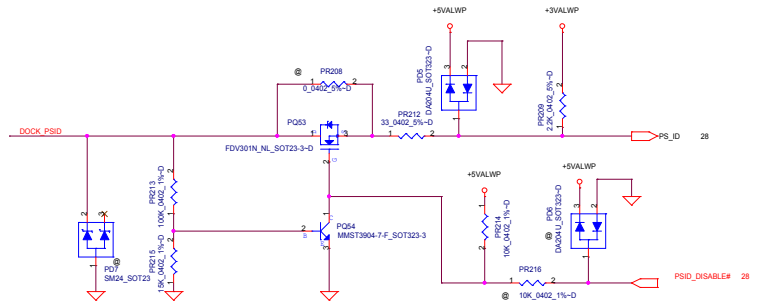
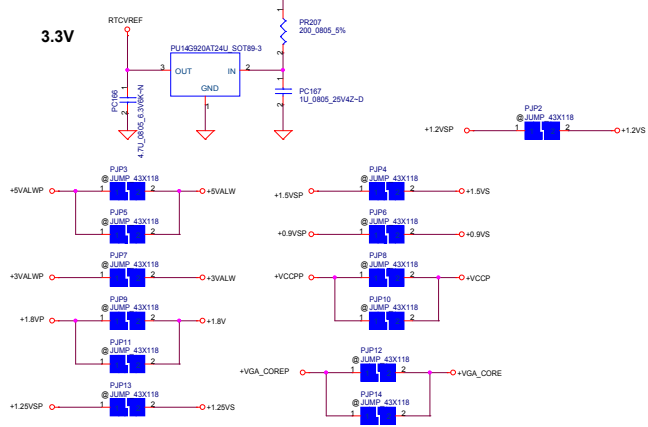
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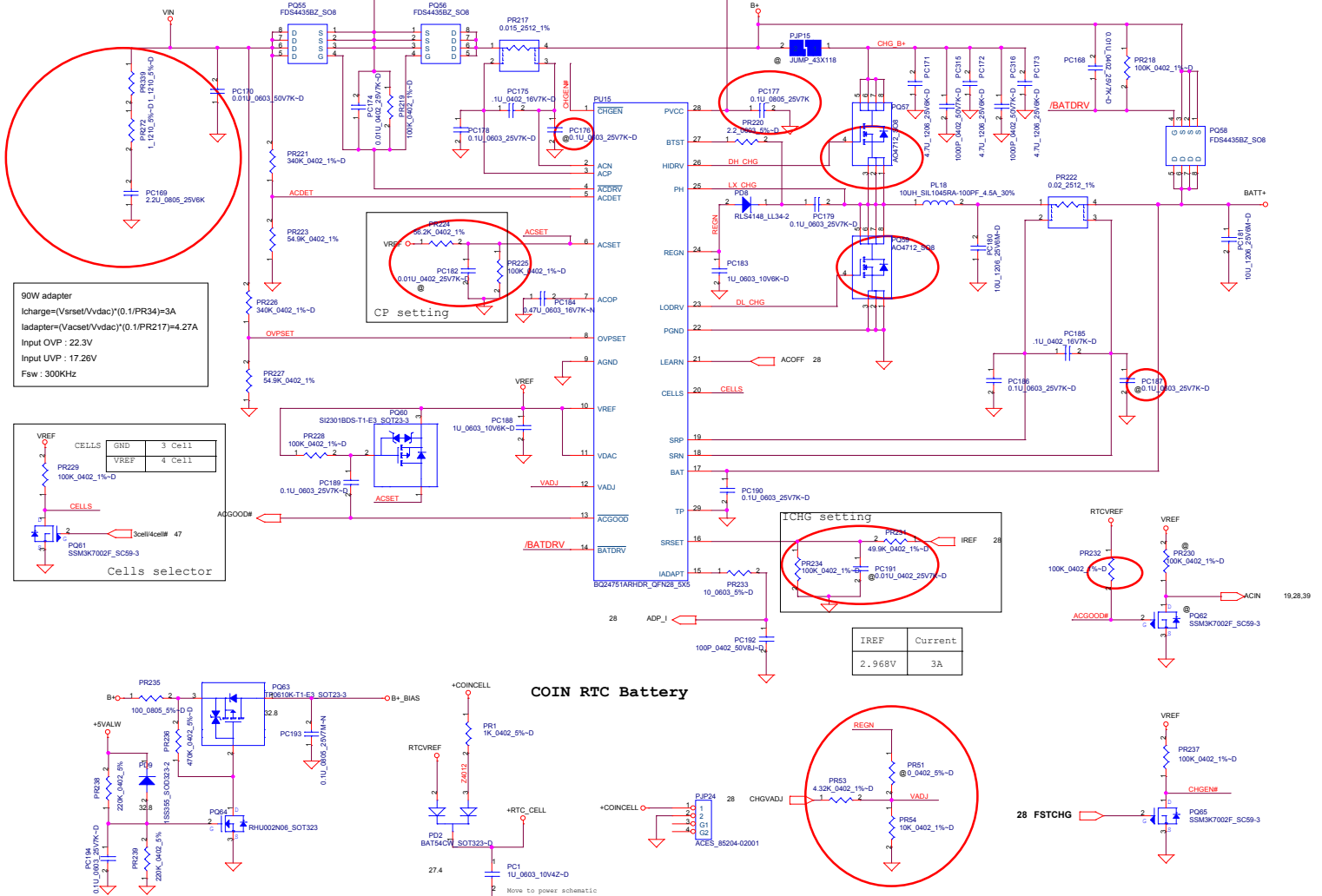
Vin Detector			
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



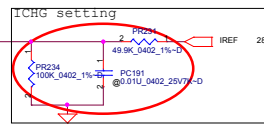
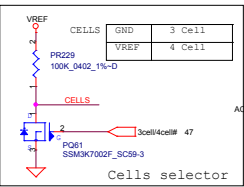
3.3V



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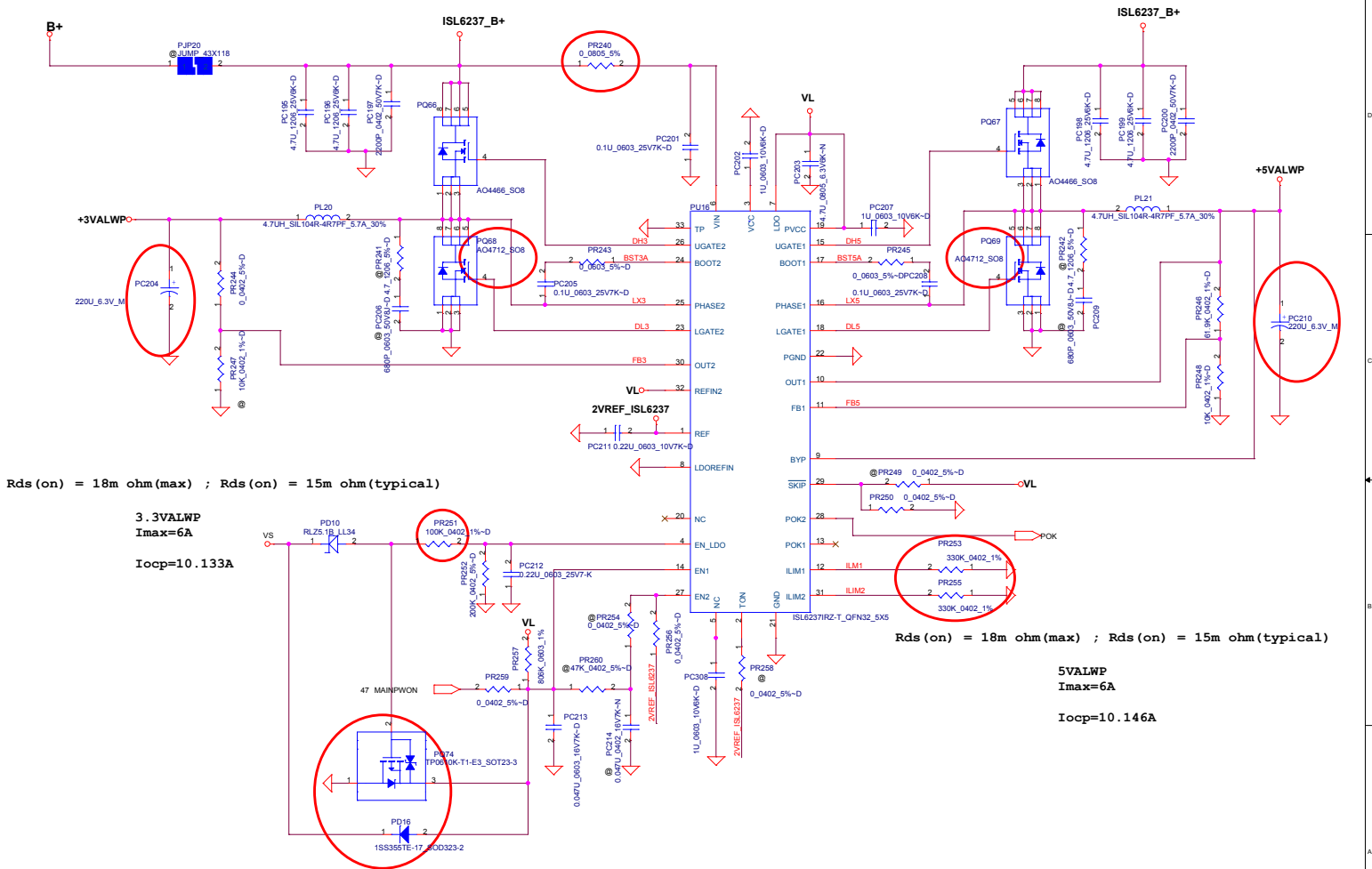
90W adapter
 $I_{charge} = (V_{set}/V_{dac}) \cdot (0.1/PR34) = 3A$
 $I_{adapter} = (V_{acset}/V_{dac}) \cdot (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input LVP : 17.26V
 Fsw : 300KHz



IREF	Current
2.968V	3A

COIN RTC Battery

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				Date: Monday, March 17, 2008
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Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

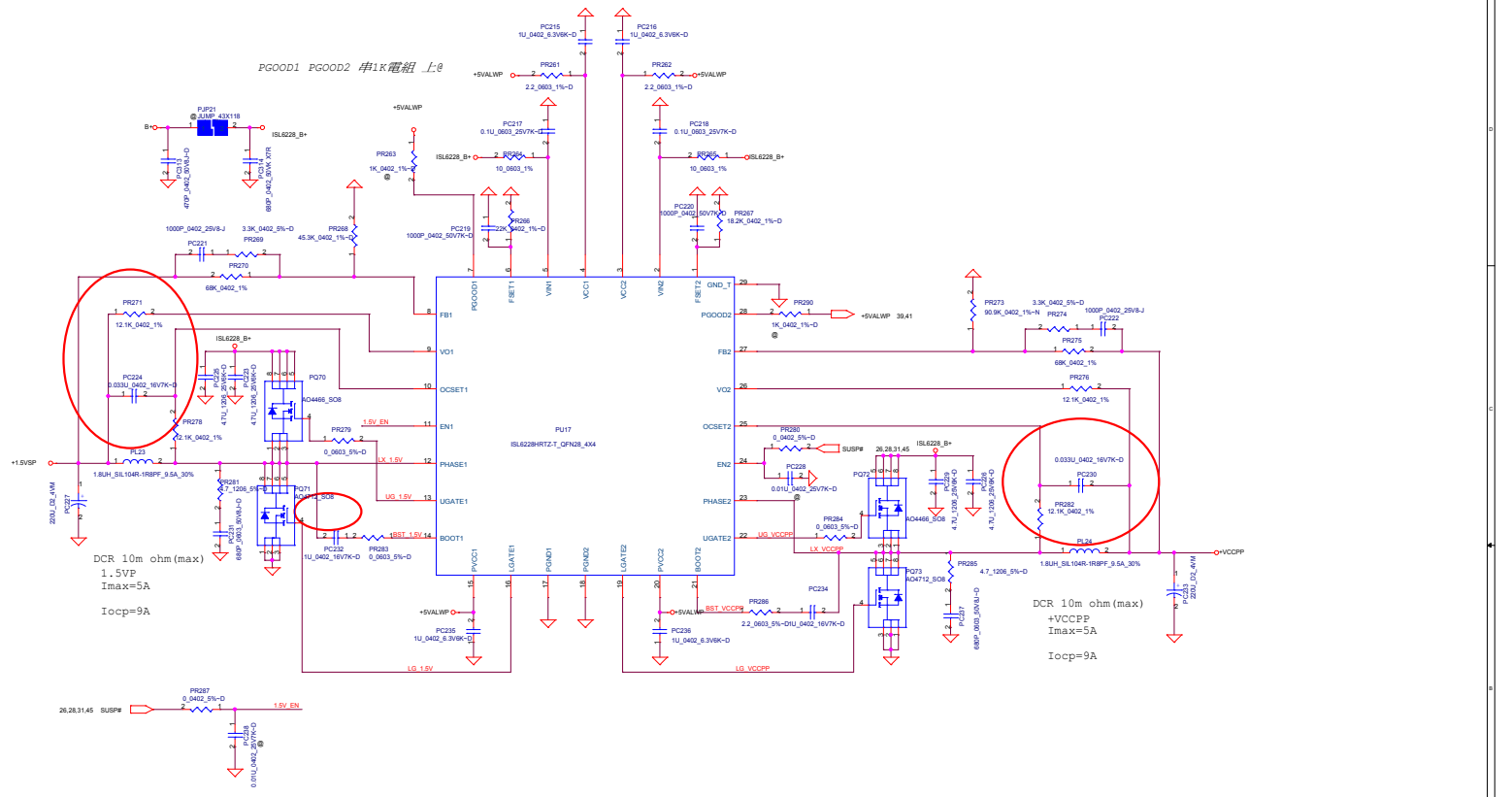
3.3VALWP
Imax=6A
Iocp=10.133A

Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

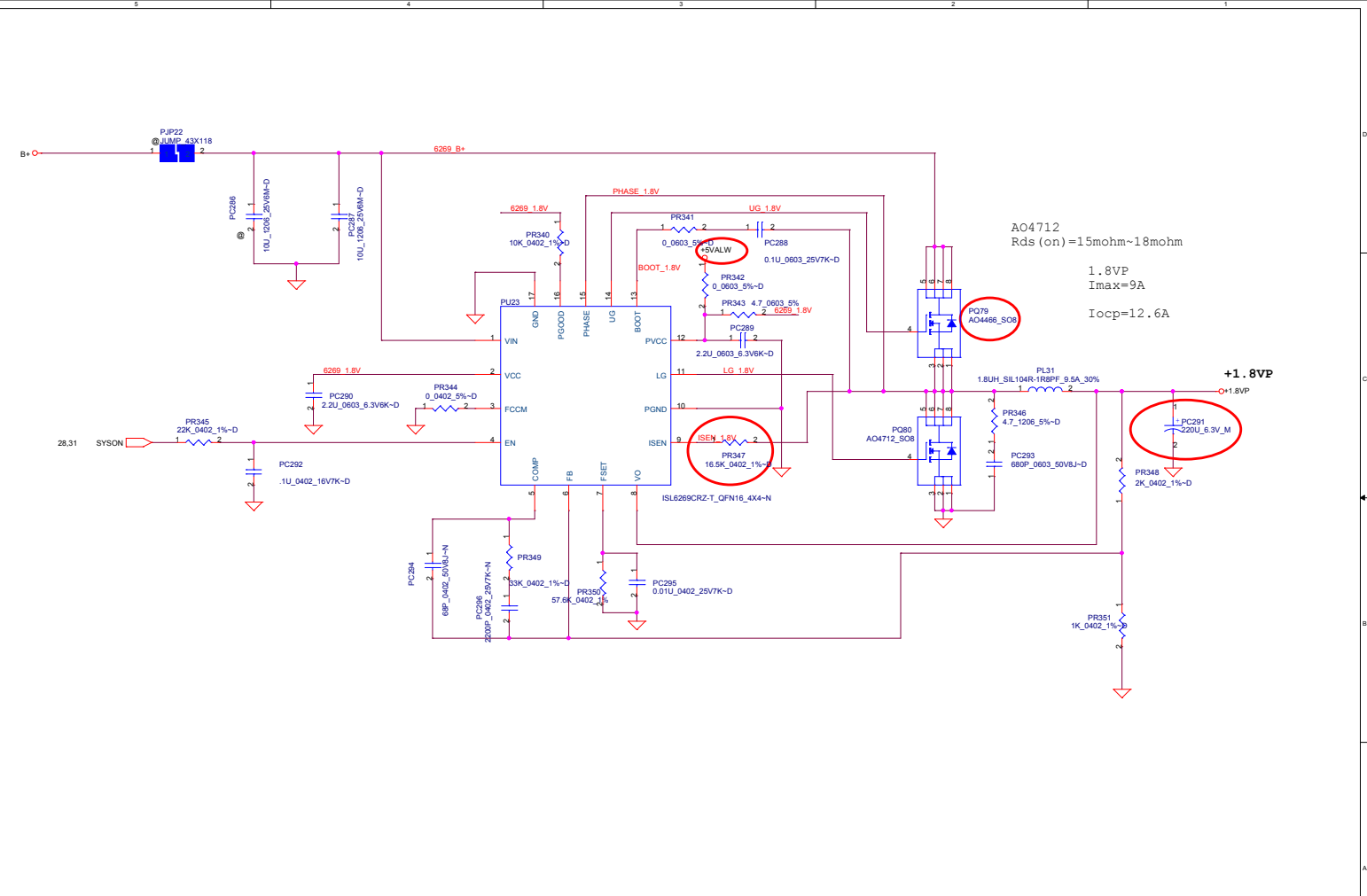
5VALWP
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Iocp=10.146A

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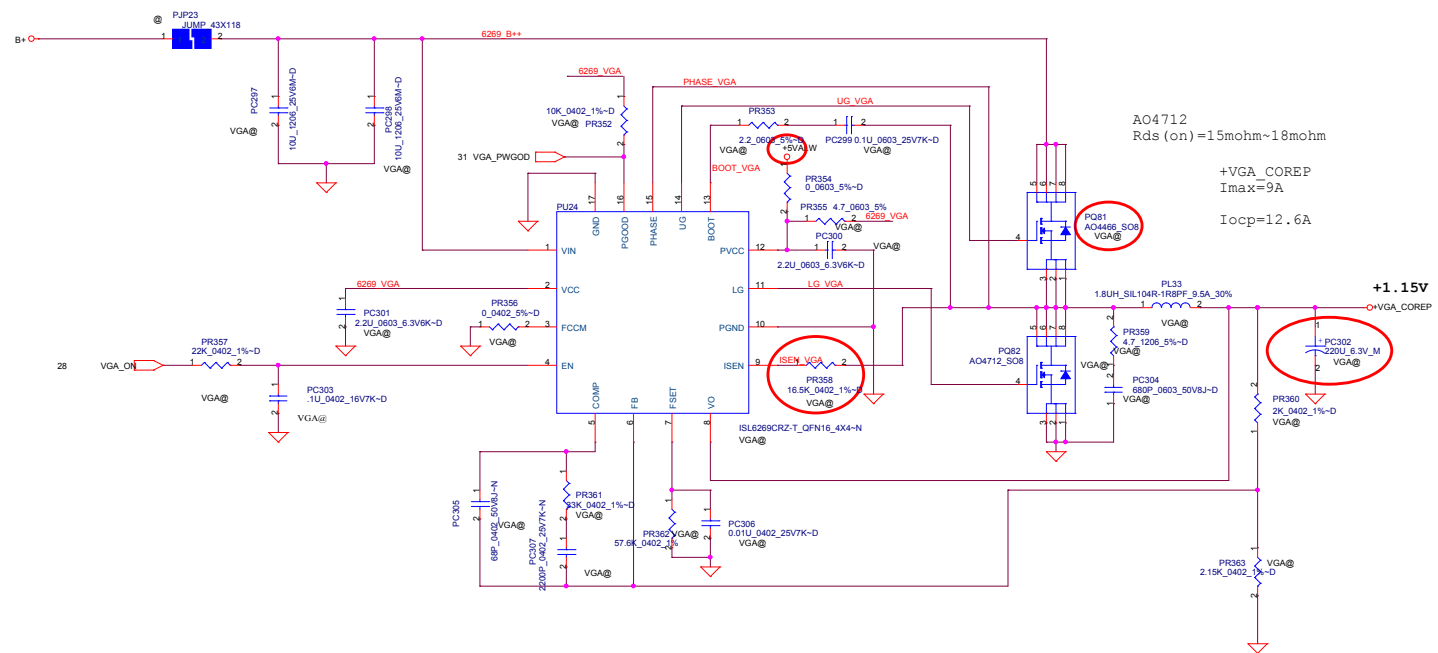
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01
Title			+1.5VP/VCCPP
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Doc. No.	Document Number	Rev.	1.0
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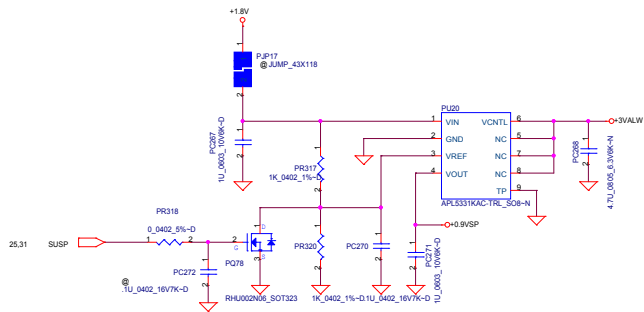
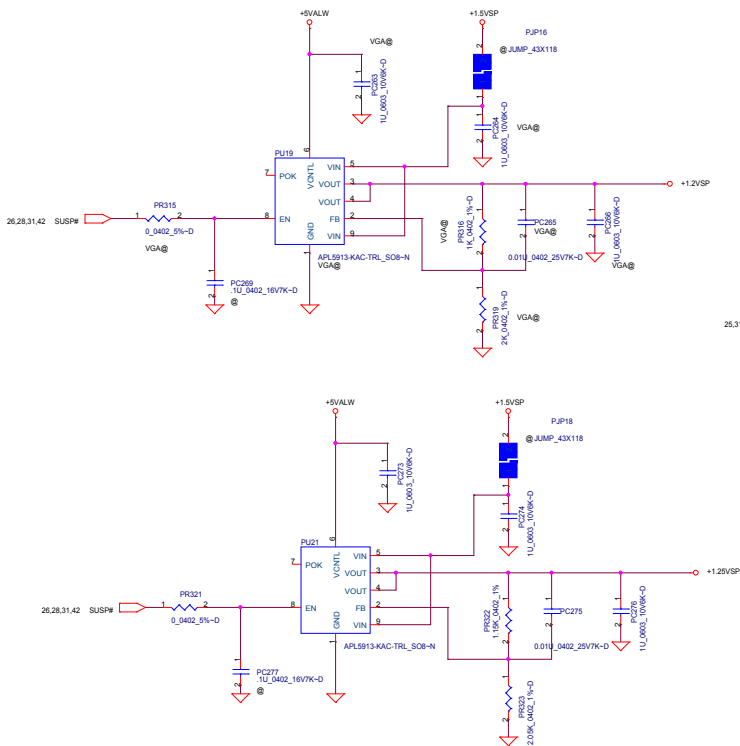
AO4712
 $R_{ds(on)} = 15\text{m}\Omega \sim 18\text{m}\Omega$
 $I_{max} = 9\text{A}$
 $I_{ocp} = 12.6\text{A}$

+1.8VP

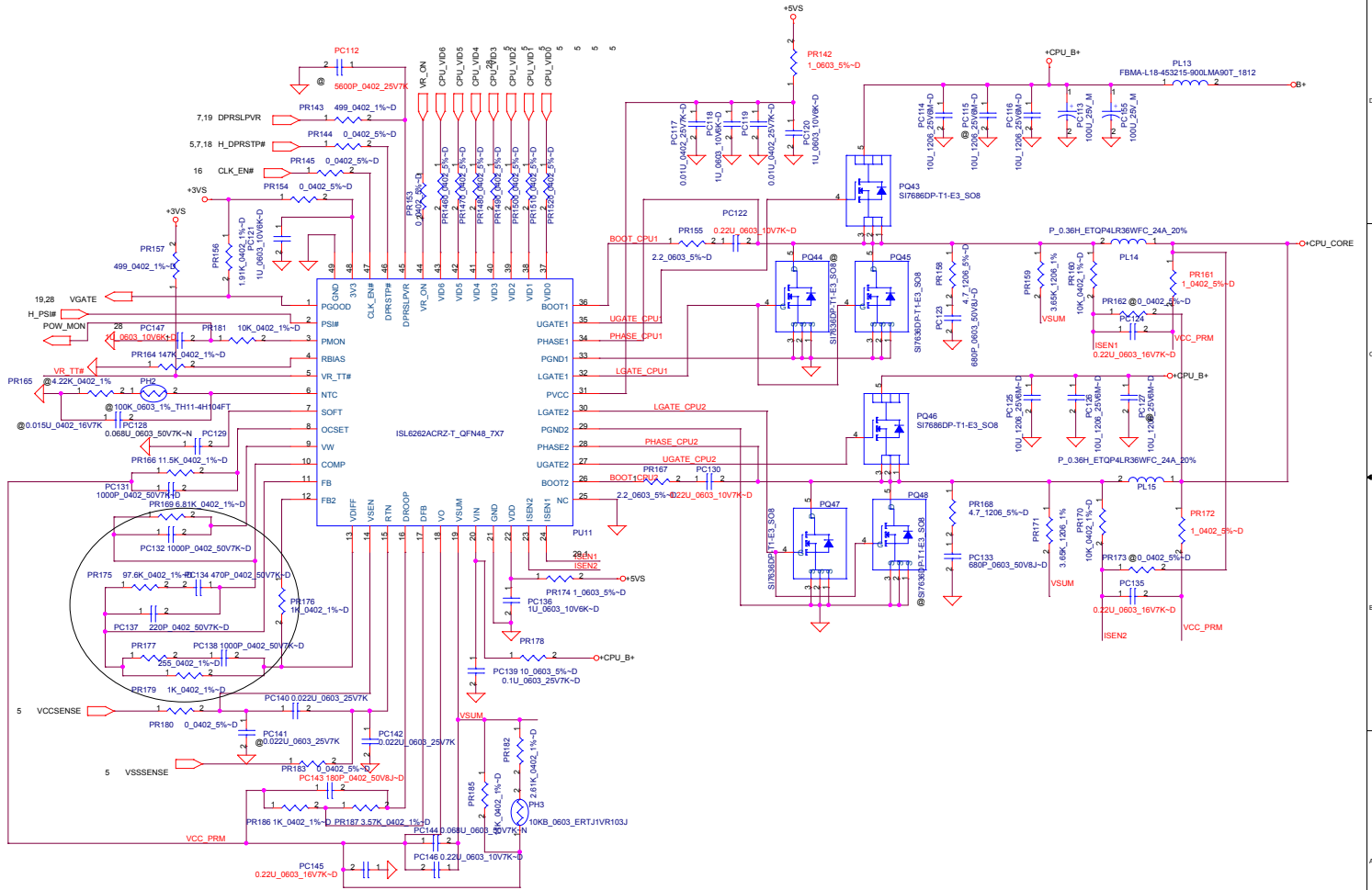
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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				+VGA_COREP
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				JAL60
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				Date: Monday, March 17, 2008
				Sheet 44 of 51

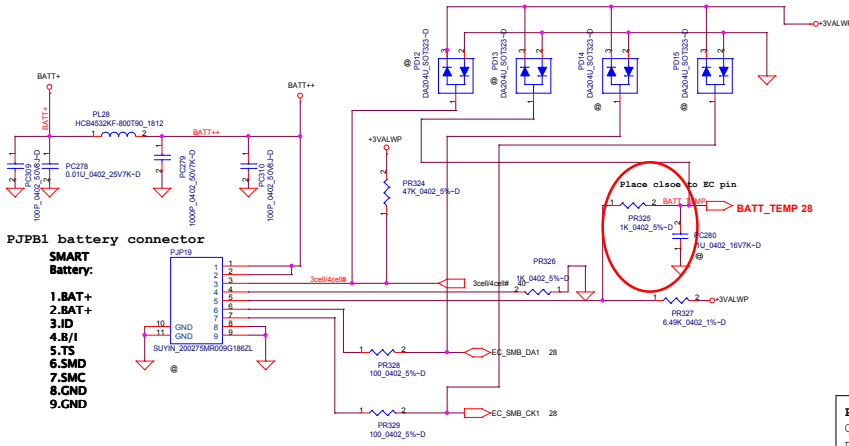


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5	4	3	2	1

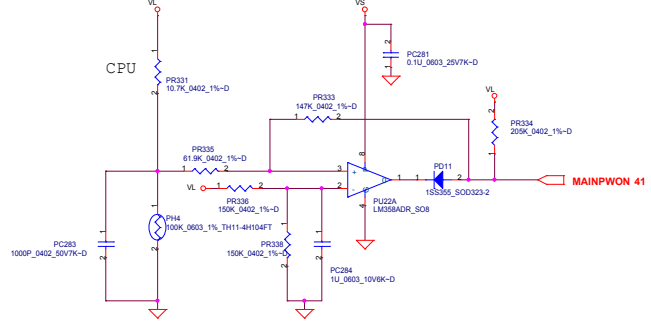
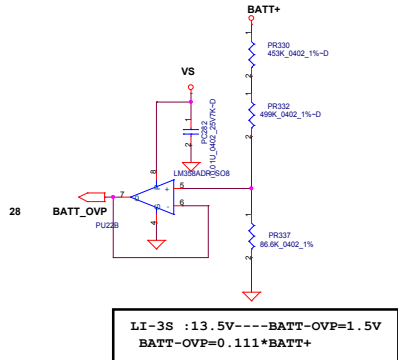


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Battery Connect/OTP



CPU
 PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



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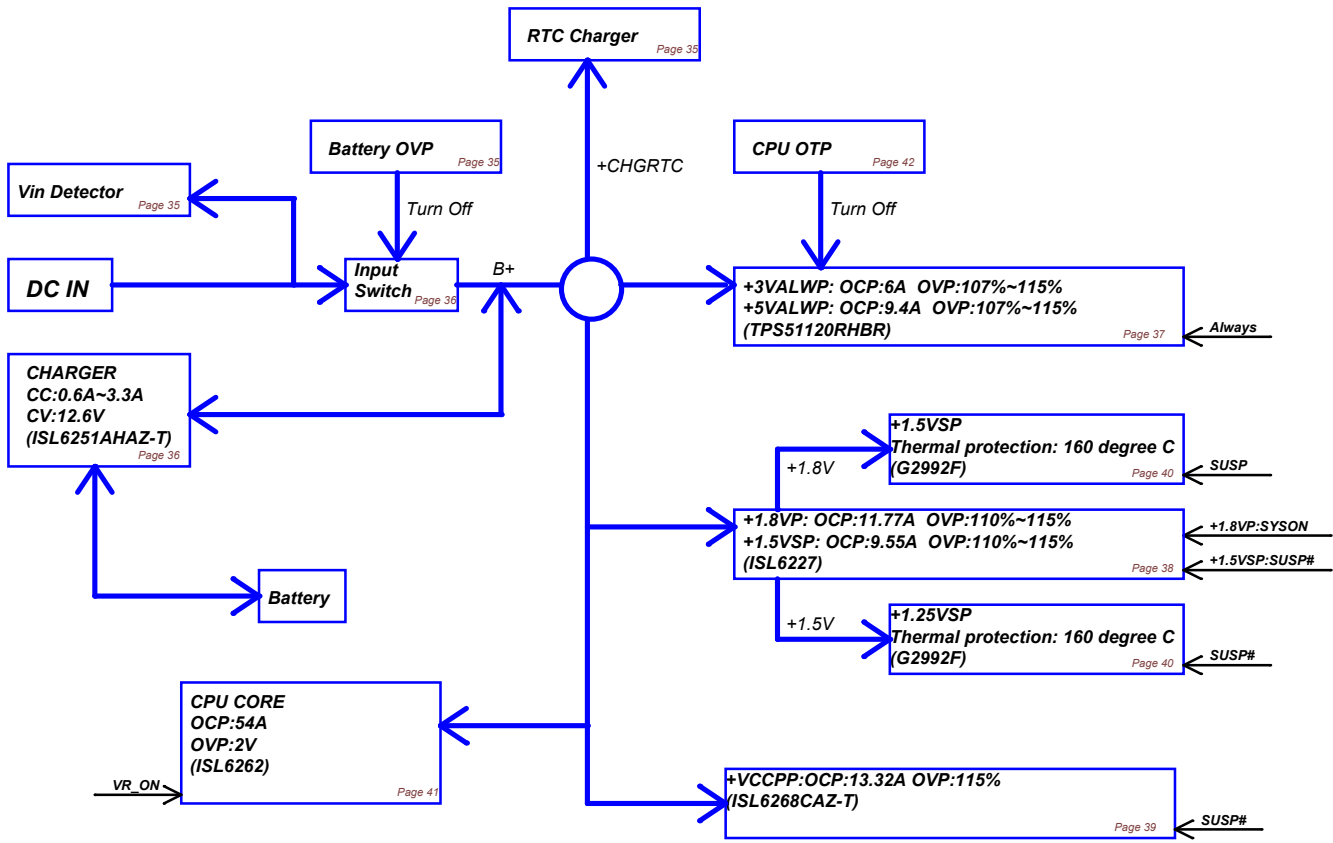
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD FQ76 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	40	Charge	07/11/25	COMPAL	Change RTC circuitry part	del PD16 PC285 PL29 JRTC1	
3	40	Charge	07/11/25	COMPAL	change charge voltage can to adjust	ADD PR53 PR54	
4	40	Charge	07/11/25	COMPAL	increase Coin RTC battery circuitry	ADD PD2 PR1 PC1	
5	40	Charge	07/11/25	COMPAL	increase BQ24751 Vin Detector function	increase PR232	
6	40	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
7	42	1.5VSP/+VCCFP	07/12/26	COMPAL	adjust 1.5VSP/+VCCFP OCP set	Change PR271 PR276 PR278 PR282 from 9.09K to 12.1K	
8	43	1.8VP	07/12/26	COMPAL	adjust 1.8VP OCP set	Change PR347 from 12.1K to 16.5K	
9	44	VGA_CORE	07/12/26	COMPAL	adjust VGA_CORE OCP set	Change PR358 from 12.1K to 16.5K	
10	41	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location doesn't correspond to PCBA	Change location from PQ76 to PQ74	
11	43	1.8VP	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR342	
12	44	VGA_CORE	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR354	
13	46	CPU_CORE	07/12/26	COMPAL	modify MOS type S08 to Power Pack for height limit	DEL PQ44 PQ48	
14	43	1.8VP	08/01/04	COMPAL	In order to replace IC for system request	ADD PU23 PR342	
15	44	VGA_CORE	08/01/04	COMPAL	In order to replace IC for system request	ADD PU24 PR354	
16	41	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD16 to turn off 5VALWP wehn shut down the system in the DC-mode	
17	40	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR53 from 15K to 4.3K	
18	40	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR230 PQ62	
19							
20			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	CHANGE PR220 PR286from 0 to 2.2 ohm	
21			08/01/04	COMPAL	Increase Capacitor on charge boot for EMI request	ADD PC123 PC133 PC231 PC237 PC309 PC310 PC311 PC313 PC312 PC314 PC293	
22			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	ADD PR158 PR168 PR285 PR281 PR346	
23			08/01/04	COMPAL	Increase Bead on charge boot for EMI request	ADD PL17 PL28	
24							
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				Customer	1.0
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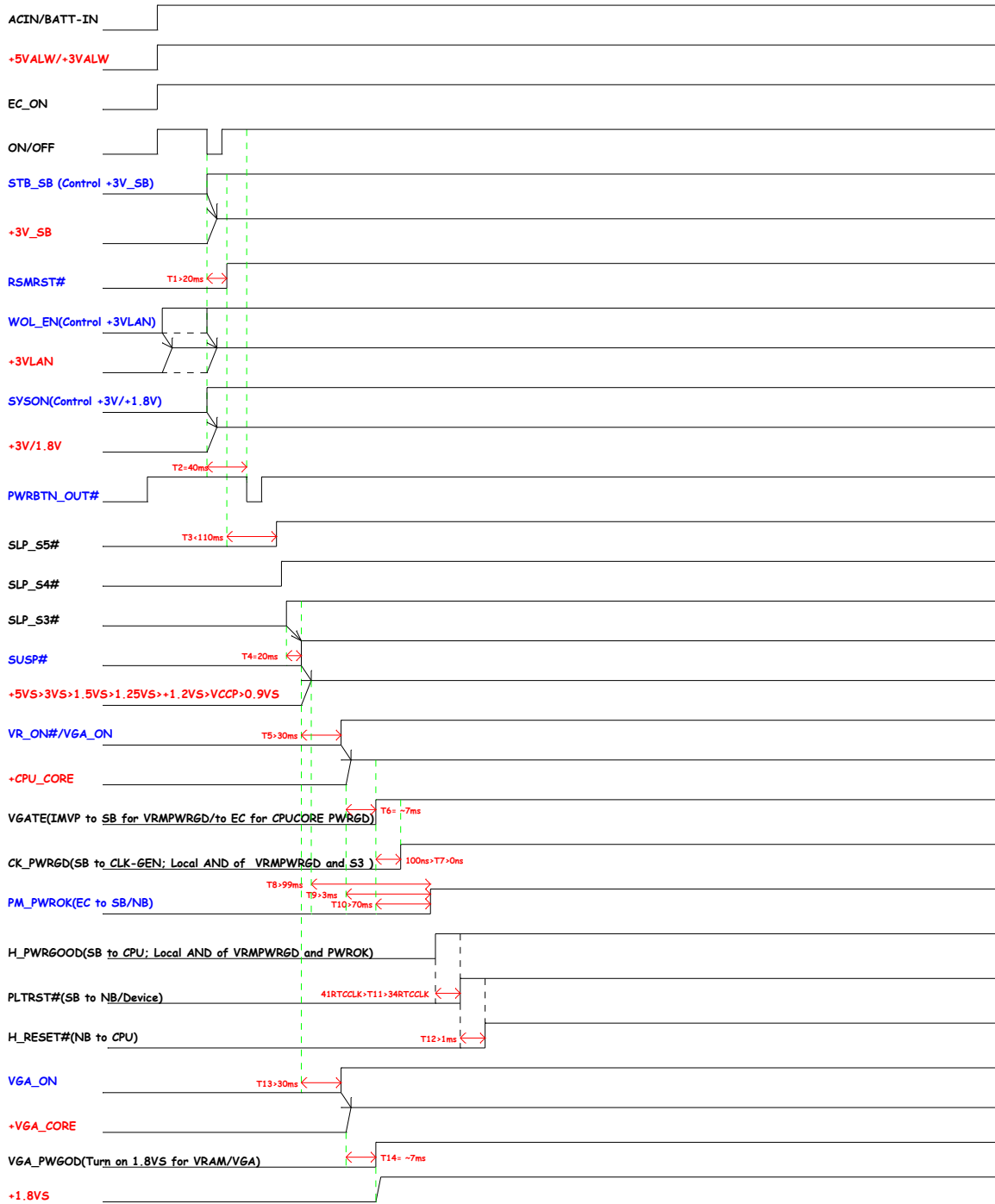
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	O2129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to O2129	0.3
2	28	EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.3
3	28	EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.3
4	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.3
5	28	EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.3
6	31	DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.3
7	31	DC/DC Interface	07/11/12	compal	Delete	Remove SIM card connector	0.3
8	15	CRT Conn. & LCD Conn.	07/11/16	compal	Add LCD control pin	Add LCD control pin LCD_DET# & LCD_TST & LCD_VCC_TEST_EN	0.3
9	30	USB/ BT/ FP/ Felica/Camera	07/11/22	compal	support wake up by USB key	change U32, U33 from 3VS to 3VALW	0.3
10	28	EC KB926/REED SW/TPM1.2	08/01/07	compal	Change for quick-set function	ADD W_DISABLE#, WL_DIS#, BT_DIS#	0.4
11	29	PWR_OK/ BTN/ KB / TouchPad	08/01/08	compal	Add Bead for EMI from function board	ADD L93, L94 FOR ESB_DAT, ESB_CLK	1.0
12	25	O2129_Card Reader/1394	08/02/25	compal	For MS can't access after reboot	ADD Q82, R932, DELETE C335 FOR CARD READER	1.0
13	27	Mini Card/WLAN/WWAN/Robson	08/02/27	customer	remove Robson & felica function	Delete JMINI3 & JFE1	1.0
14							
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JAL30 Power Bock



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				Power On Sequence
				4.4-21P
				1/15