

14" & 15.6" ULV + GS45 Block Diagram

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Rev: X01



POWER	
1.5VSUS & 0.75VTT (RT8207A) PG 32	CHARGER (MAX8731A) PG 29
CPU CORE (ADP3211A) PG 31	1.05_VCCP (OZ8116) PG 30
RUN POWER SW PG 33	Power Button PG 27
AC/BATT CONNECTOR PG 34	

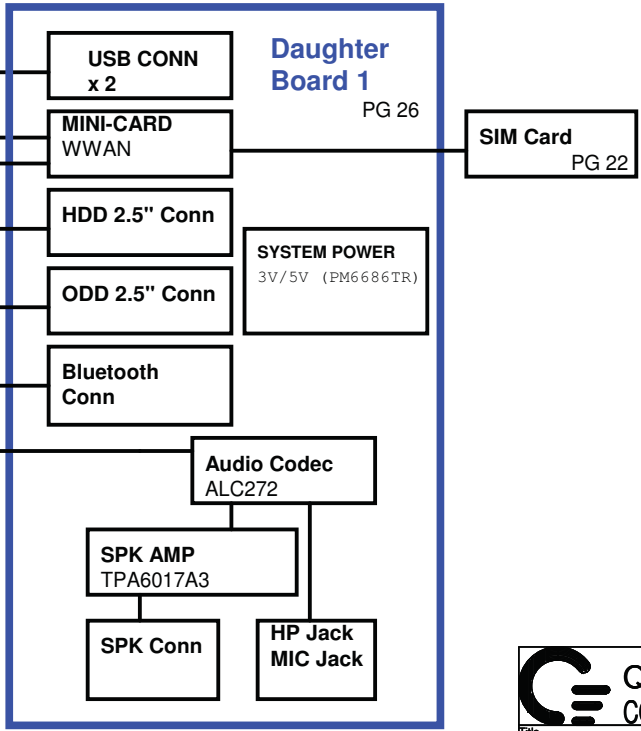
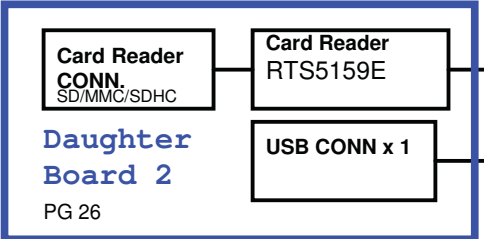
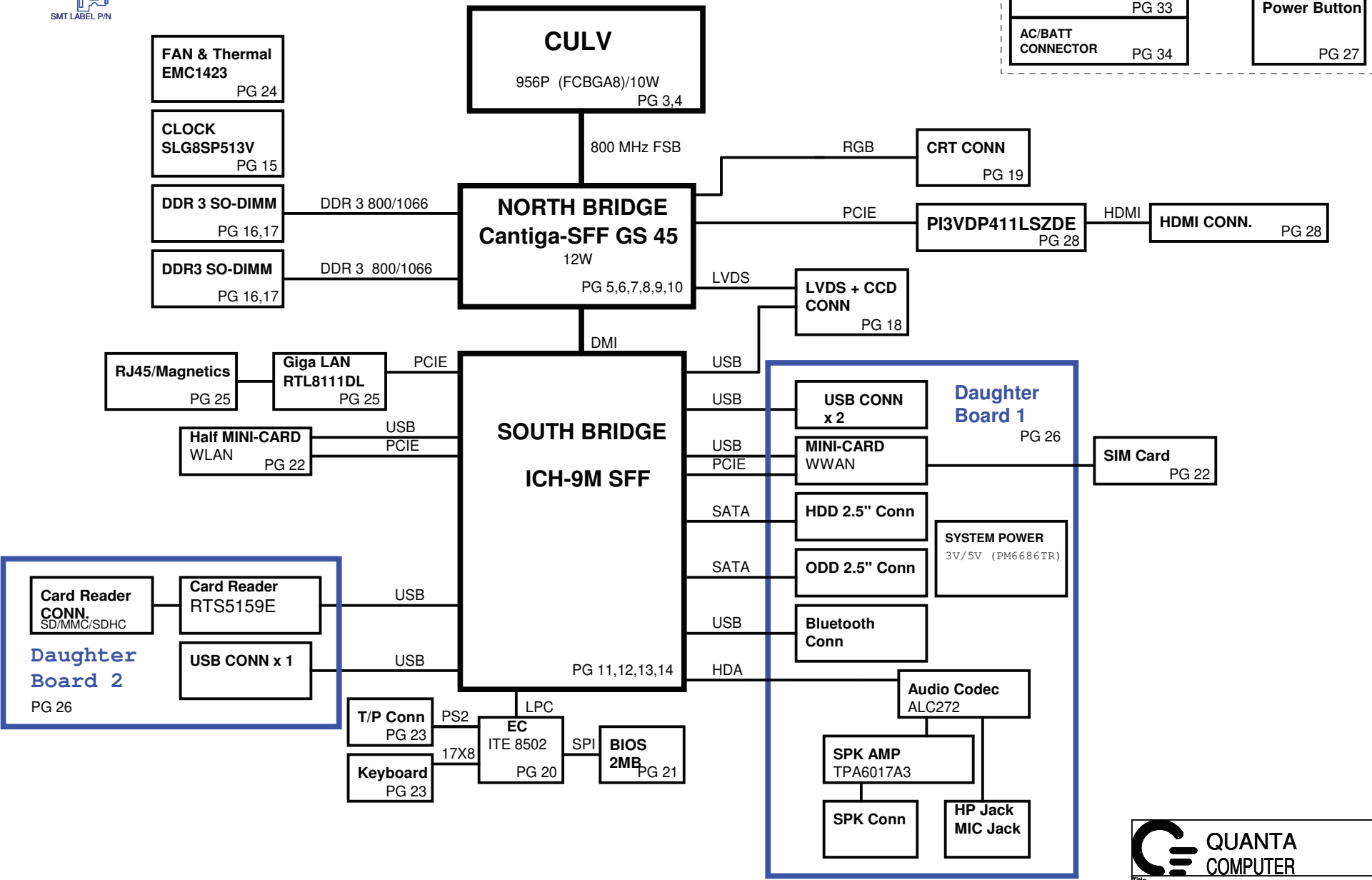







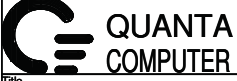


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23	TP/KB
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34	DCin & Batt
35	SMBUS BLOCK
36	PAD&SCREW&SPRING

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
 8731AGND	46	
 AGND_0.9V	49	
 AGND_DC/DC	52	
 AGND_DC2	48	
 AGND_DDR	49	
 AGND_ISL6260	51	
 GND	ALL	

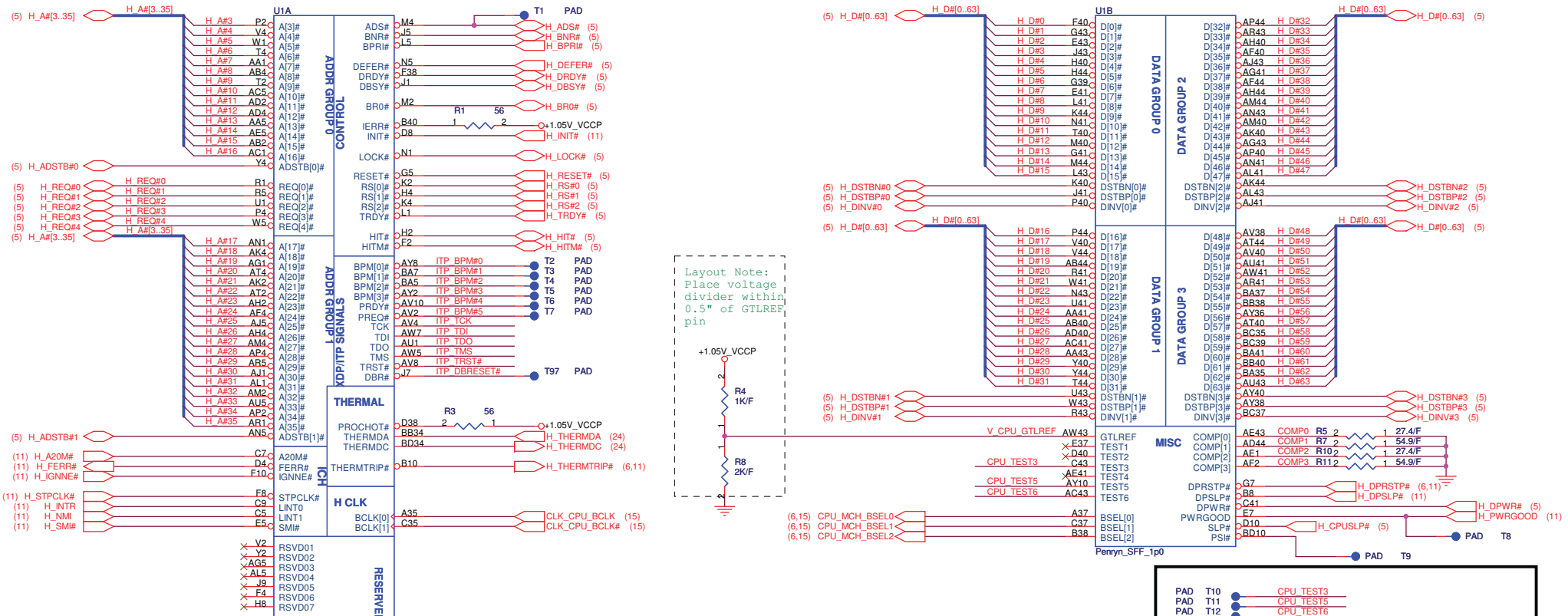


**QUANTA
COMPUTER**

Title: Index & Power Status

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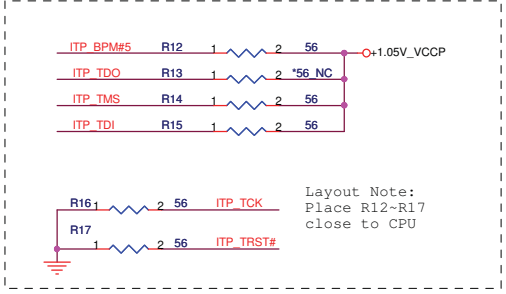


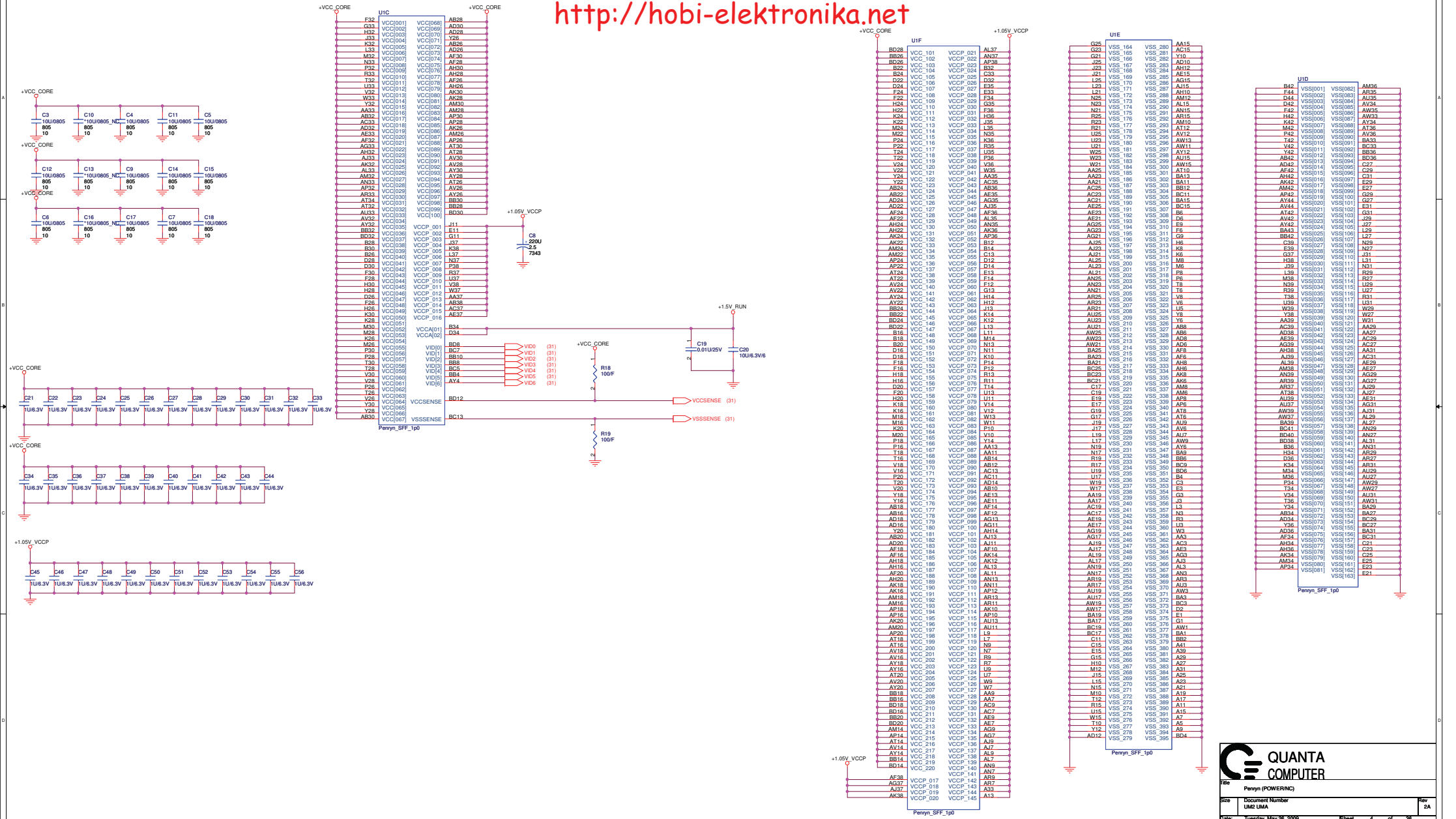
Layout Note:
Place voltage divider within 0.5" of GTLREF pin

PAD T10 CPU TEST3
 PAD T11 CPU TEST5
 PAD T12 CPU TEST6

For the purpose of testability, route these signals through a ground referenced Z0 = 50ohm trace which ends in a via that is near a GND via and is accessible through an oscilloscope connection.

- AJSLB5VVT01
CPU (956P)SU9400 1.4G SLB5V(BGA)WIN B/S
- AJSLGFMTT03
CPU (956P)SU3500 1.4G SLGFM(BGA)WIN BSQ
- AJSLGS8VT03
CPU (956P)SU2700 1.3G SLGS8(BGA)WIN BSQ



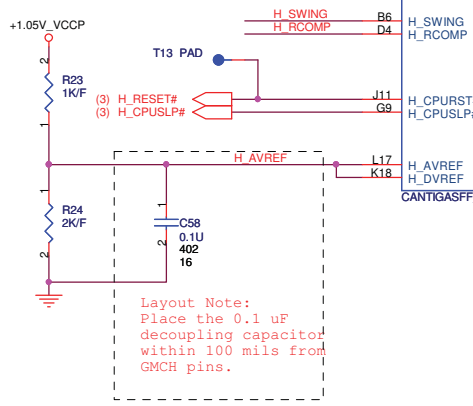
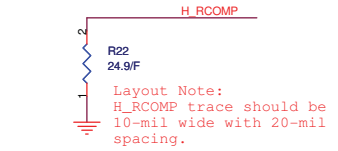
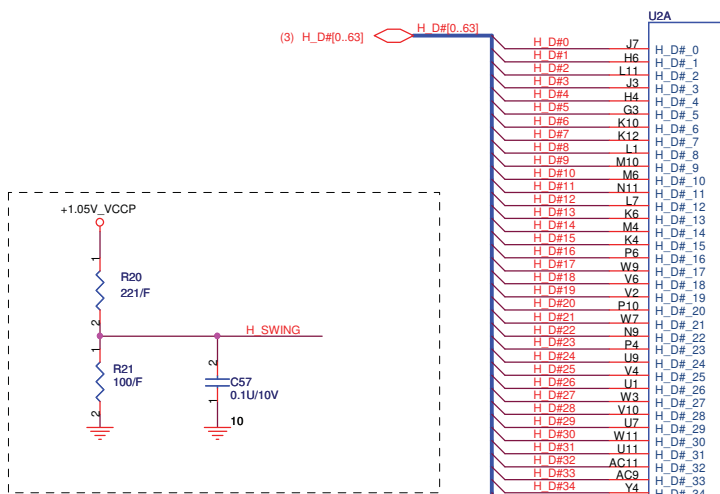


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Pin	Label	Signal
H D#0	J7	H_D#_0
H D#1	H6	H_D#_1
H D#2	L11	H_D#_2
H D#3	J3	H_D#_3
H D#4	H4	H_D#_4
H D#5	G3	H_D#_5
H D#6	K10	H_D#_6
H D#7	K12	H_D#_7
H D#8	L1	H_D#_8
H D#9	M10	H_D#_9
H D#10	M6	H_D#_10
H D#11	N11	H_D#_11
H D#12	L7	H_D#_12
H D#13	K6	H_D#_13
H D#14	M4	H_D#_14
H D#15	K4	H_D#_15
H D#16	P6	H_D#_16
H D#17	W9	H_D#_17
H D#18	V6	H_D#_18
H D#19	V2	H_D#_19
H D#20	P10	H_D#_20
H D#21	W7	H_D#_21
H D#22	N9	H_D#_22
H D#23	P4	H_D#_23
H D#24	U9	H_D#_24
H D#25	V4	H_D#_25
H D#26	U1	H_D#_26
H D#27	W3	H_D#_27
H D#28	V10	H_D#_28
H D#29	U7	H_D#_29
H D#30	W11	H_D#_30
H D#31	U11	H_D#_31
H D#32	AC11	H_D#_32
H D#33	AC9	H_D#_33
H D#34	Y4	H_D#_34
H D#35	Y10	H_D#_35
H D#36	AB6	H_D#_36
H D#37	AA9	H_D#_37
H D#38	AB10	H_D#_38
H D#39	AA1	H_D#_39
H D#40	AC3	H_D#_40
H D#41	AC7	H_D#_41
H D#42	AD12	H_D#_42
H D#43	AB4	H_D#_43
H D#44	Y6	H_D#_44
H D#45	AD10	H_D#_45
H D#46	AA11	H_D#_46
H D#47	AB2	H_D#_47
H D#48	AD4	H_D#_48
H D#49	AE7	H_D#_49
H D#50	AD2	H_D#_50
H D#51	AD6	H_D#_51
H D#52	AE3	H_D#_52
H D#53	AG9	H_D#_53
H D#54	AG7	H_D#_54
H D#55	AE11	H_D#_55
H D#56	AK6	H_D#_56
H D#57	AF6	H_D#_57
H D#58	AJ9	H_D#_58
H D#59	AH6	H_D#_59
H D#60	AF12	H_D#_60
H D#61	AH4	H_D#_61
H D#62	AJ7	H_D#_62
H D#63	AE9	H_D#_63

HOST

Pin	Label	Signal
H_A#_3	L15	H_A#3
H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	F14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	F14	H_A#13
H_A#_14	K16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	B16	H_A#16
H_A#_17	C21	H_A#17
H_A#_18	D18	H_A#18
H_A#_19	J19	H_A#19
H_A#_20	J21	H_A#20
H_A#_21	B18	H_A#21
H_A#_22	D22	H_A#22
H_A#_23	G19	H_A#23
H_A#_24	J17	H_A#24
H_A#_25	L21	H_A#25
H_A#_26	L19	H_A#26
H_A#_27	G21	H_A#27
H_A#_28	D20	H_A#28
H_A#_29	K22	H_A#29
H_A#_30	F18	H_A#30
H_A#_31	K20	H_A#31
H_A#_32	F20	H_A#32
H_A#_33	F22	H_A#33
H_A#_34	B20	H_A#34
H_A#_35	A19	H_A#35

H_ADS#	F10	H_ADS# (3)
H_ADSTB#_0	A15	H_ADSTB#0 (3)
H_ADSTB#_1	C19	H_ADSTB#1 (3)
H_BNR#	C9	H_BNR# (3)
H_BPRI#	B8	H_BPRI# (3)
H_BREQ#	C11	H_BREQ# (3)
H_DEFER#	E5	H_DEFER# (3)
H_DBSY#	D6	H_DBSY# (3)
HPLL_CLK	AH10	CLK_MCH_BCLK (15)
HPLL_CLK#	AJ11	CLK_MCH_BCLK# (15)
H_DPWR#	G11	H_DPWR# (3)
H_DRDY#	H2	H_DRDY# (3)
H_HIT#	C7	H_HIT# (3)
H_HITM#	F8	H_HITM# (3)
H_LOCK#	A11	H_LOCK# (3)
H_TRDY#	D8	H_TRDY# (3)

H_DINV#_0	L9	H_DINV#0 (3)
H_DINV#_1	N7	H_DINV#1 (3)
H_DINV#_2	AA7	H_DINV#2 (3)
H_DINV#_3	AG3	H_DINV#3 (3)

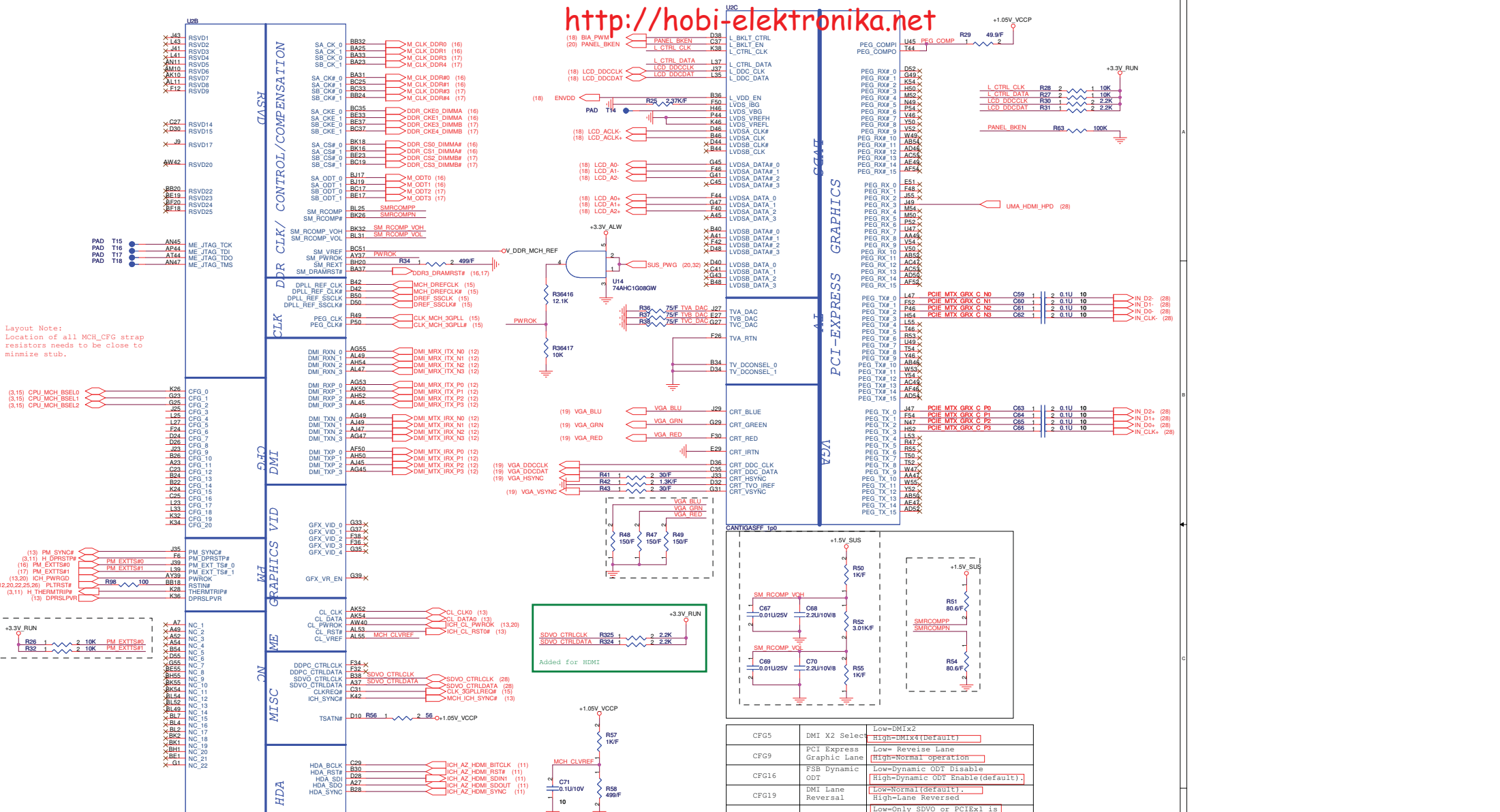
H_DSTBN#_0	K2	H_DSTBN#0 (3)
H_DSTBN#_1	N3	H_DSTBN#1 (3)
H_DSTBN#_2	AA3	H_DSTBN#2 (3)
H_DSTBN#_3	AF4	H_DSTBN#3 (3)

H_DSTBP#_0	L3	H_DSTBP#0 (3)
H_DSTBP#_1	M2	H_DSTBP#1 (3)
H_DSTBP#_2	Y2	H_DSTBP#2 (3)
H_DSTBP#_3	AF2	H_DSTBP#3 (3)

H_REQ#_0	J13	H_REQ#0 (3)
H_REQ#_1	L13	H_REQ#1 (3)
H_REQ#_2	C13	H_REQ#2 (3)
H_REQ#_3	G13	H_REQ#3 (3)
H_REQ#_4	G15	H_REQ#4 (3)

H_RS#_0	F4	H_RS#0 (3)
H_RS#_1	F2	H_RS#1 (3)
H_RS#_2	G7	H_RS#2 (3)





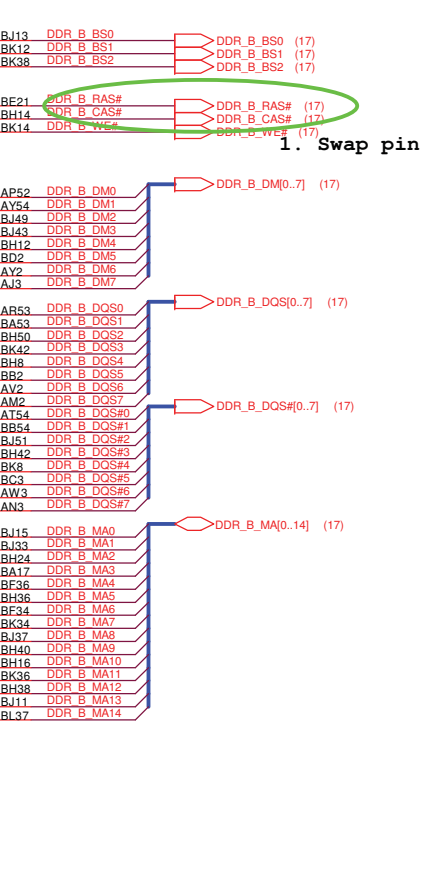
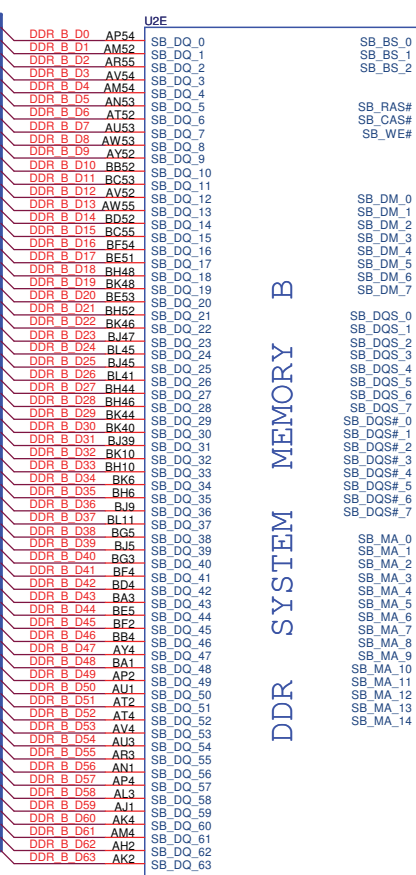
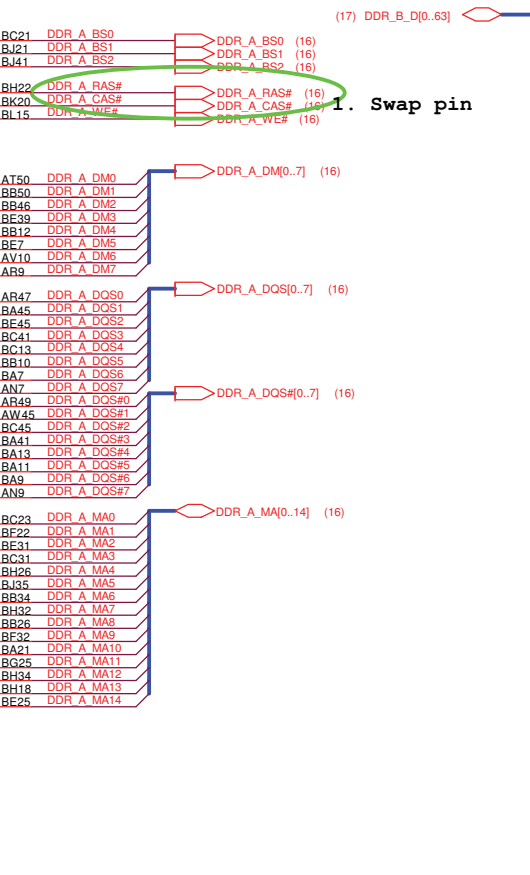
Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal(Default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

SDVO/HDMI/DP Configuration		
	SDVO_CTRLDATA	DDPC_CTRLDATA
PEG	0	0
PEG Enabled	1	1
SDVO/HDMI/DP Enabled	1	1

DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable DisplayPort.

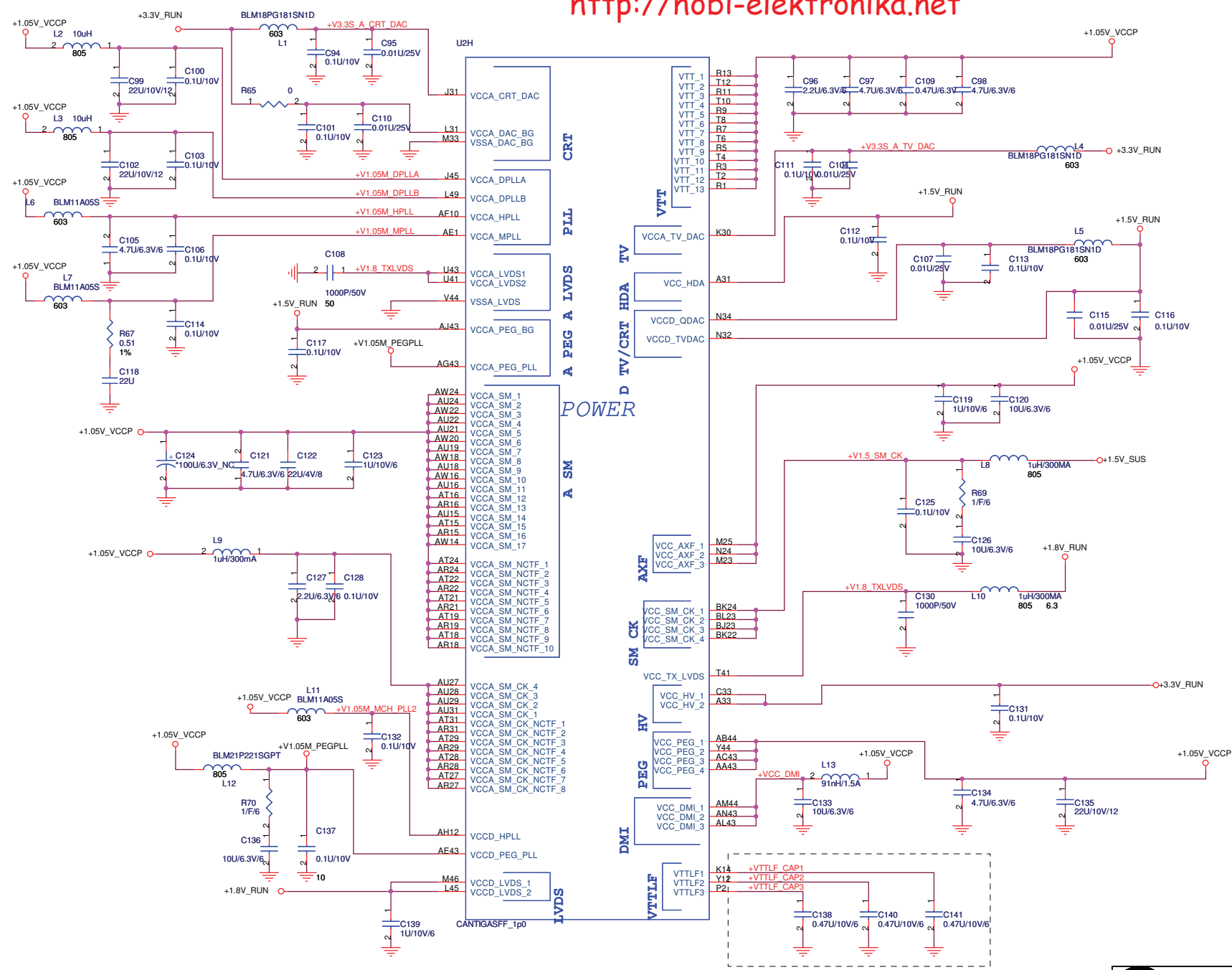


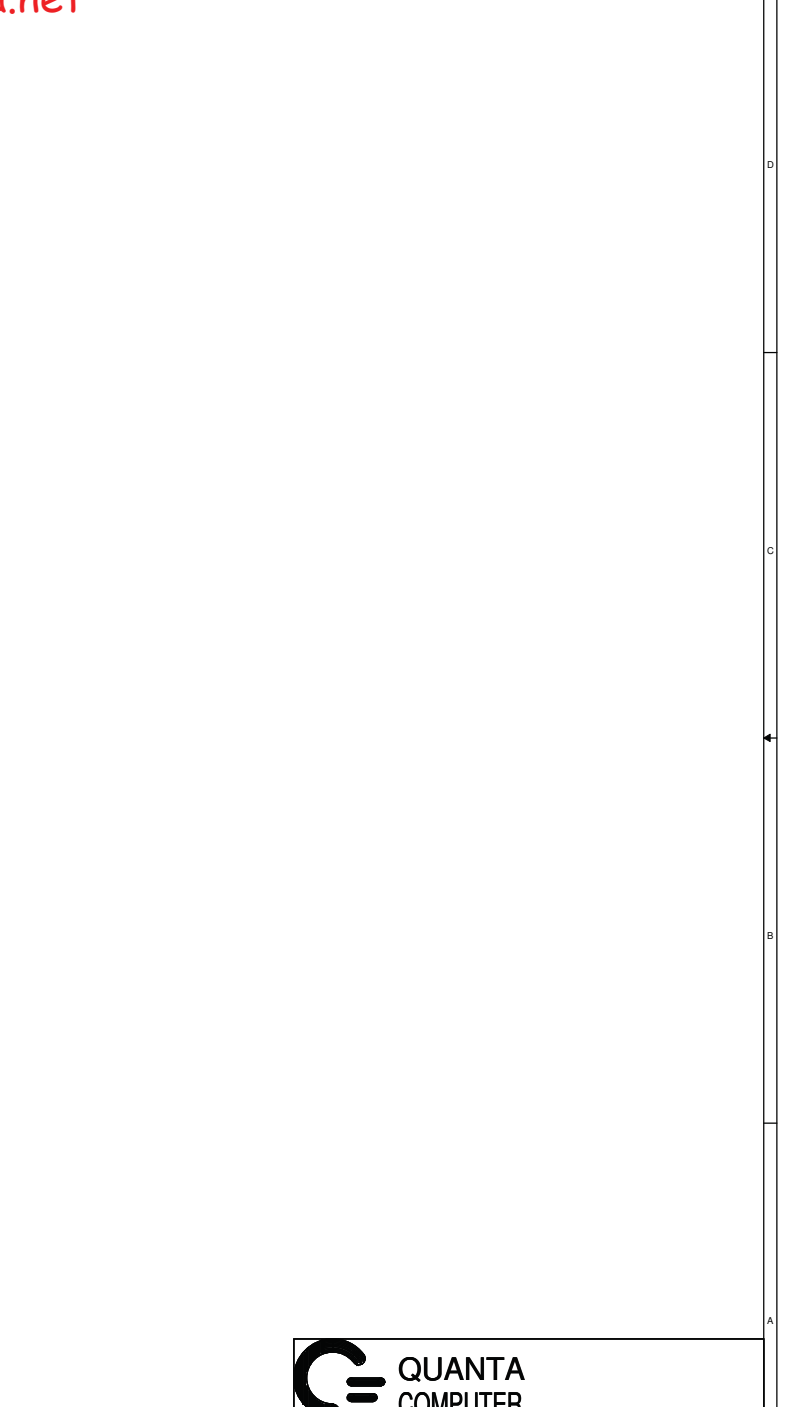
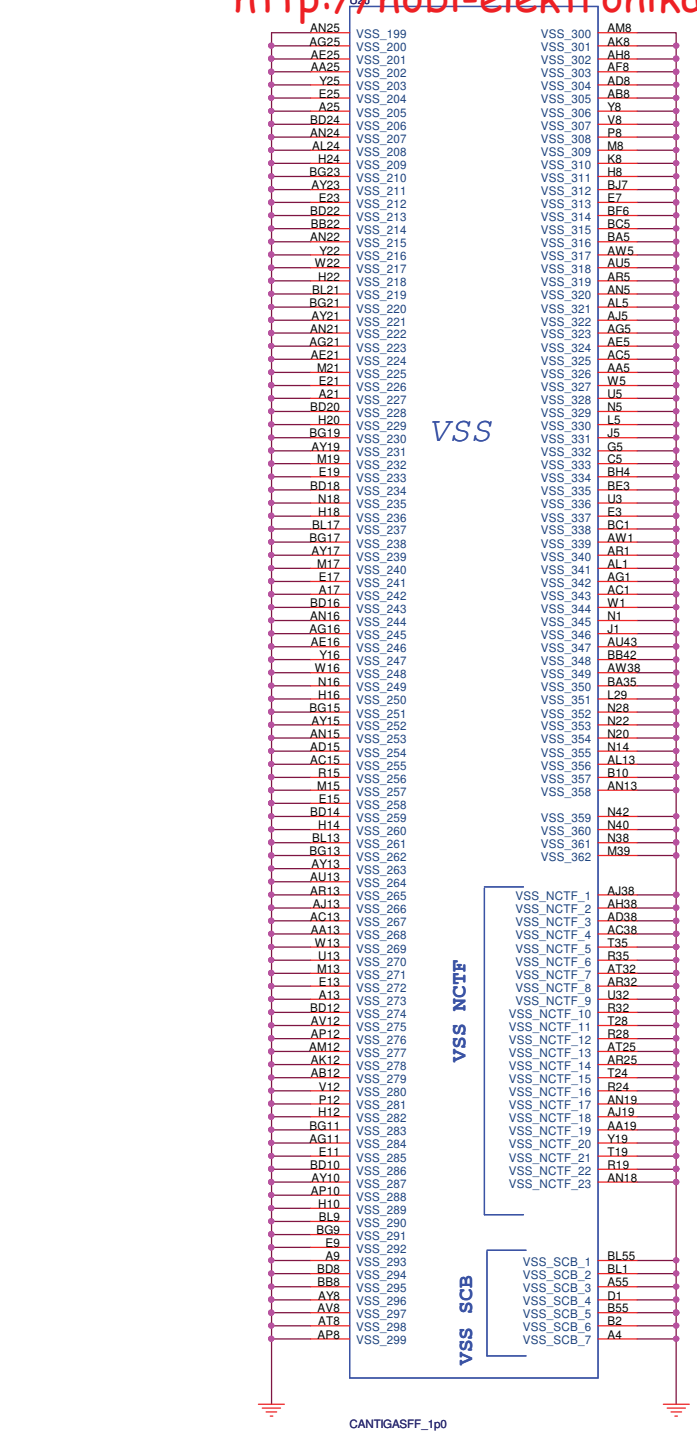
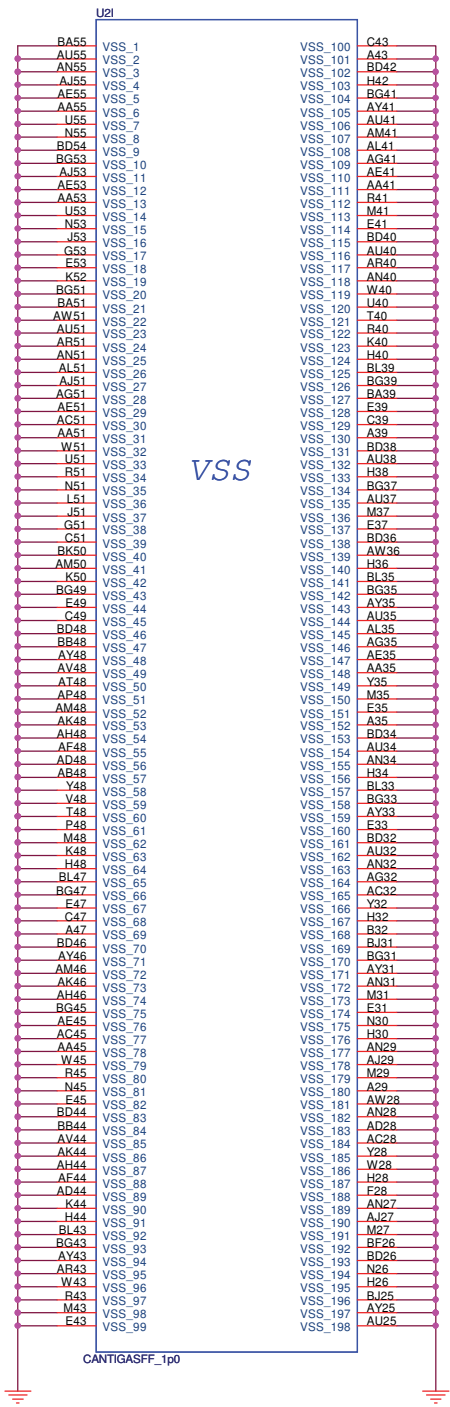


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Title: Cantiga_C (DDR3)

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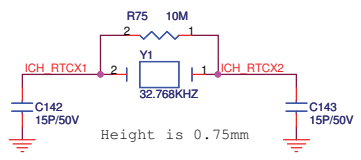
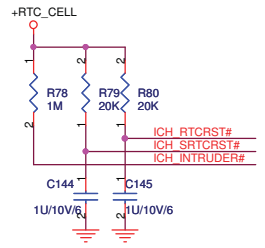


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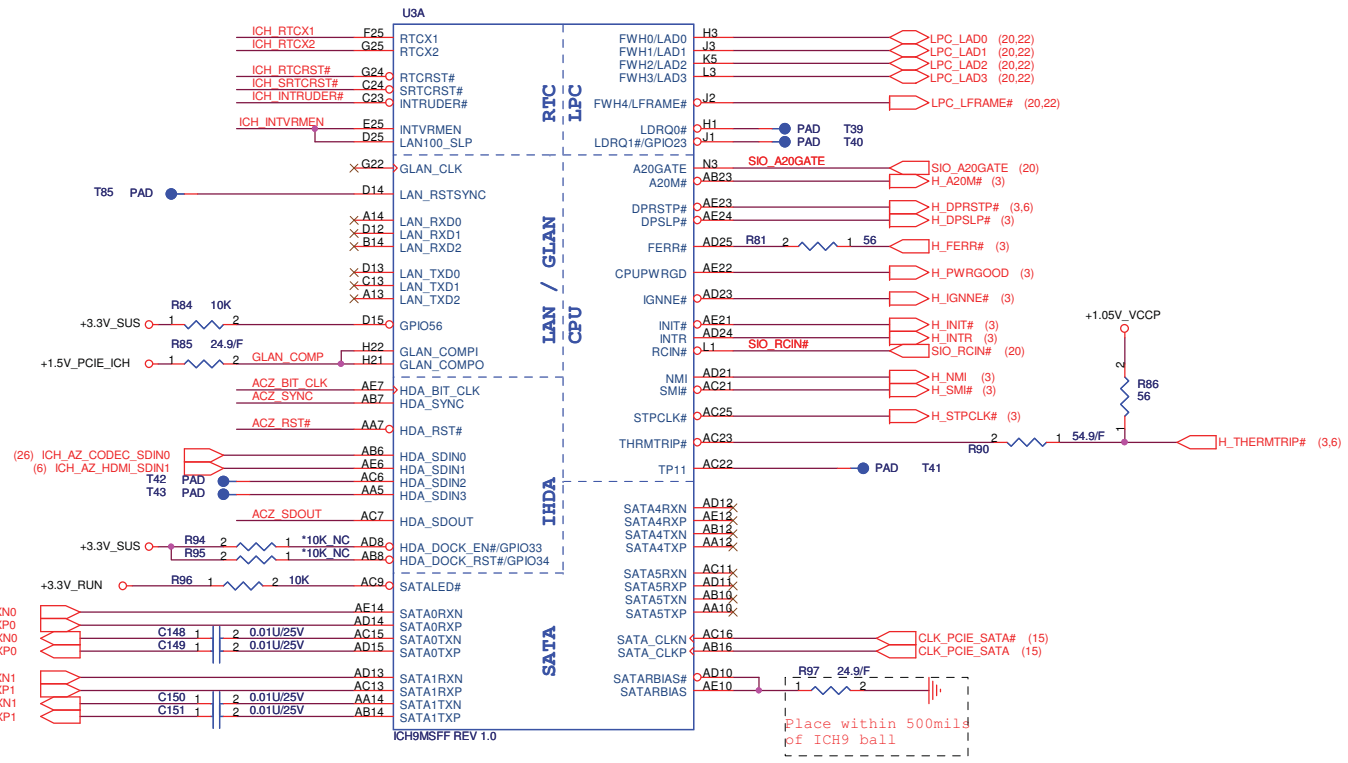
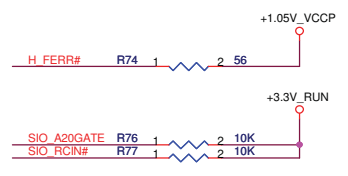
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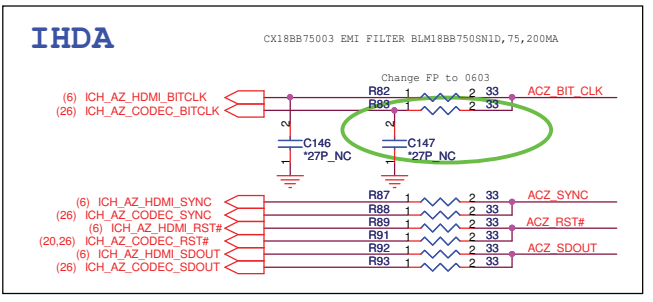


(Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05)

ICH_INTVRMEN	Low = Internal VR Disabled
ICH_INTVRMEN	High = Internal VR Enabled(Default)

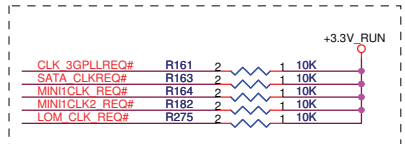
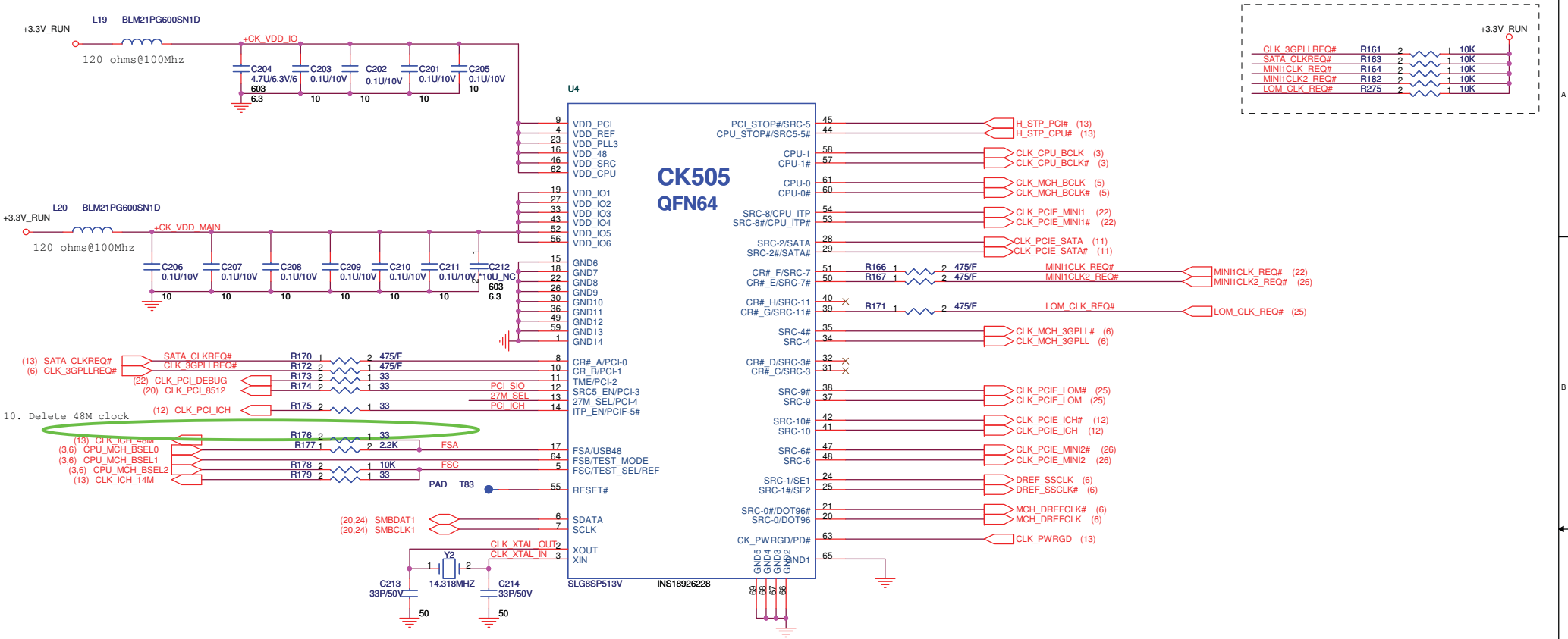


ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

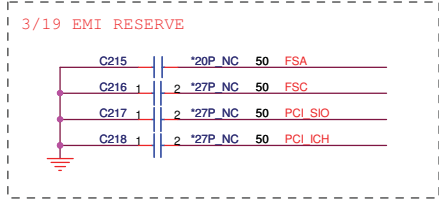


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Title: ICH9-M (CPU,SATA,IDE)		
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10. Delete 48M clock (12) CLK_PCI_ICH

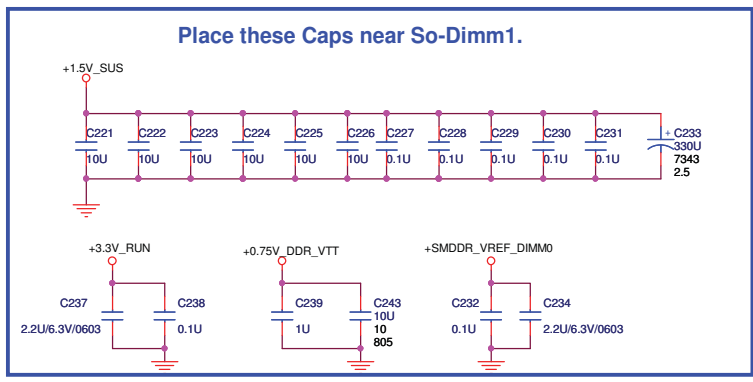
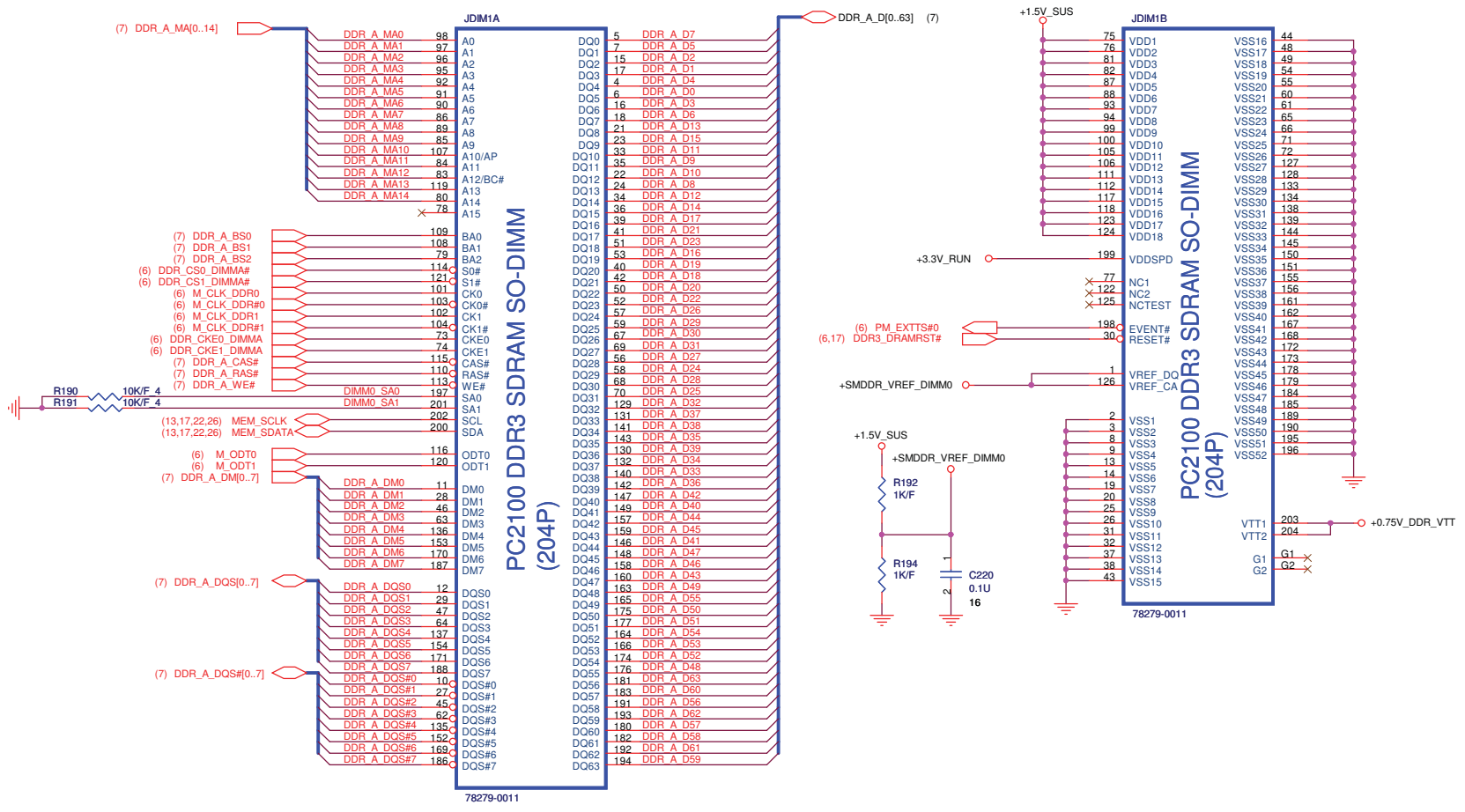


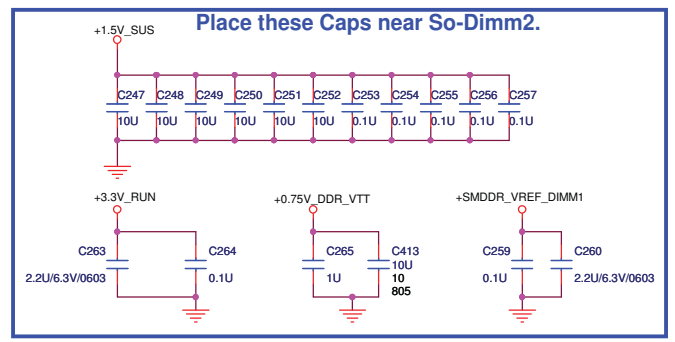
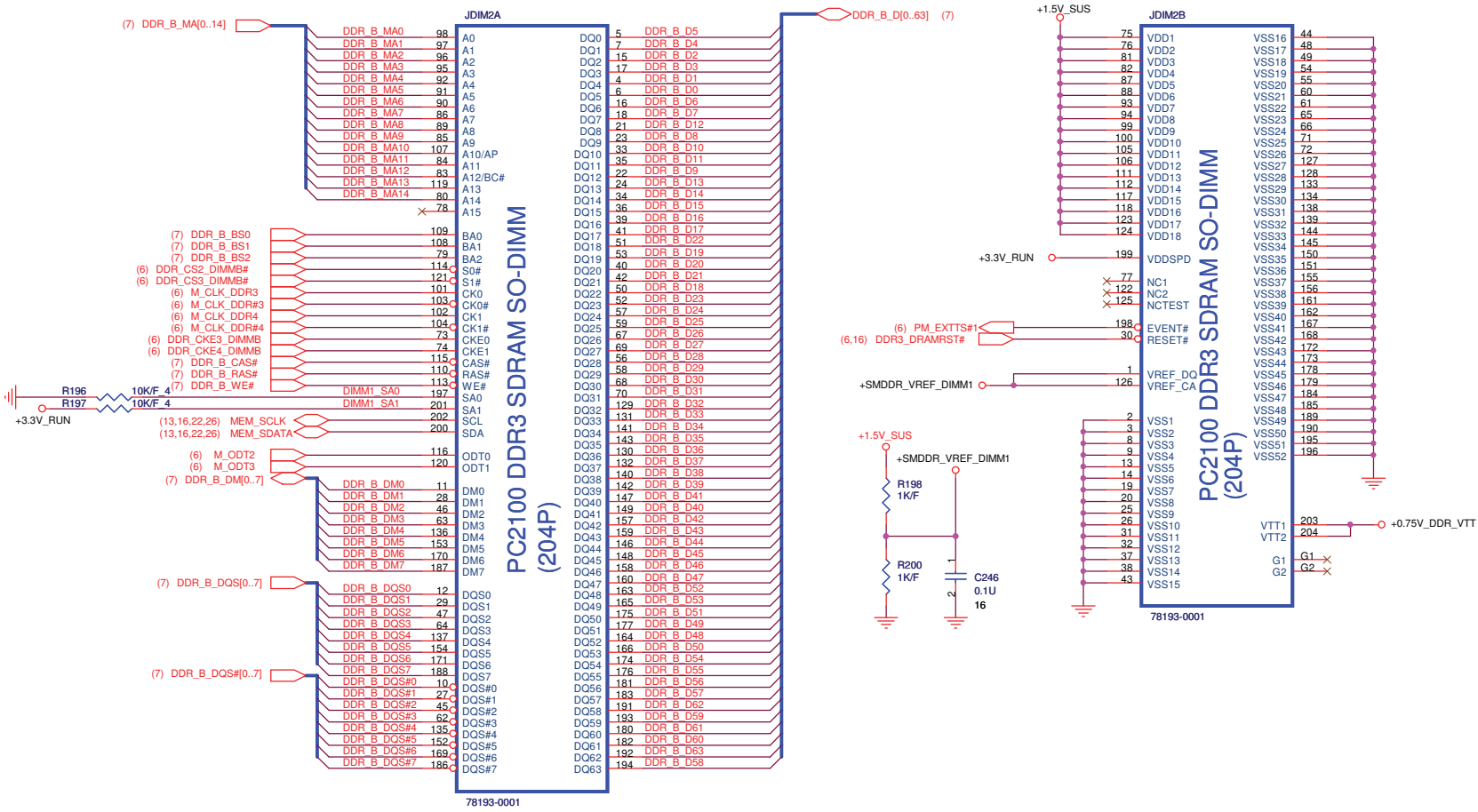
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	FSD	100	33

27M_SEL

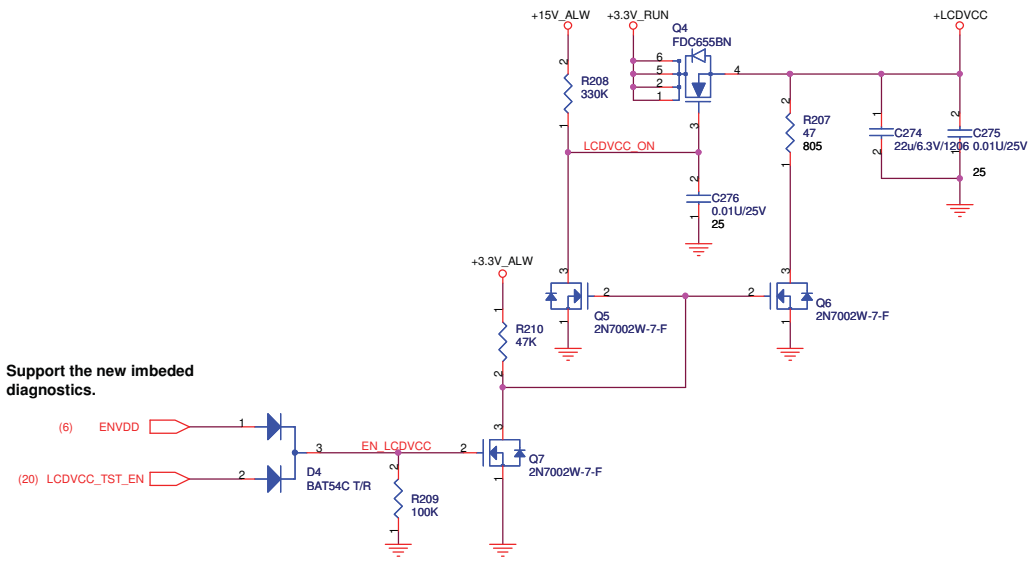
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	100M_T	100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



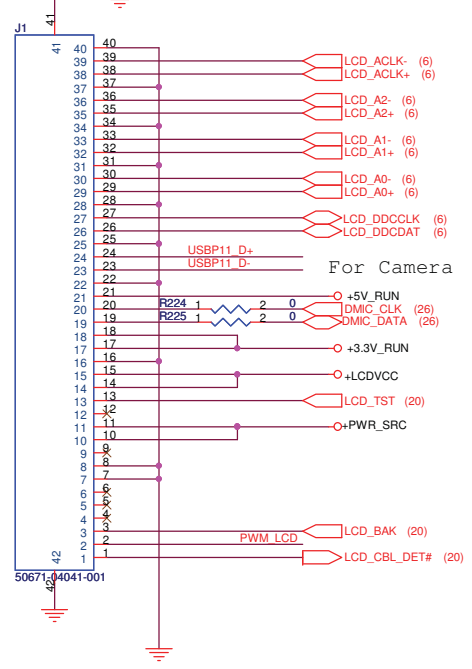




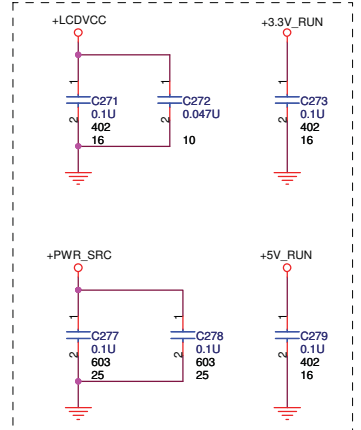
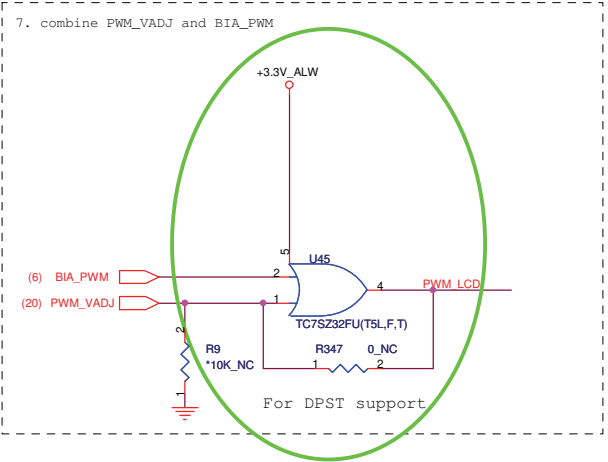
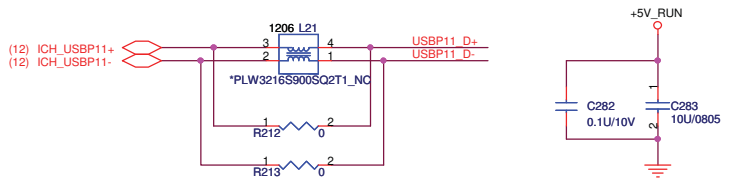
LCD



Support the new imbedded diagnostics.



CCD

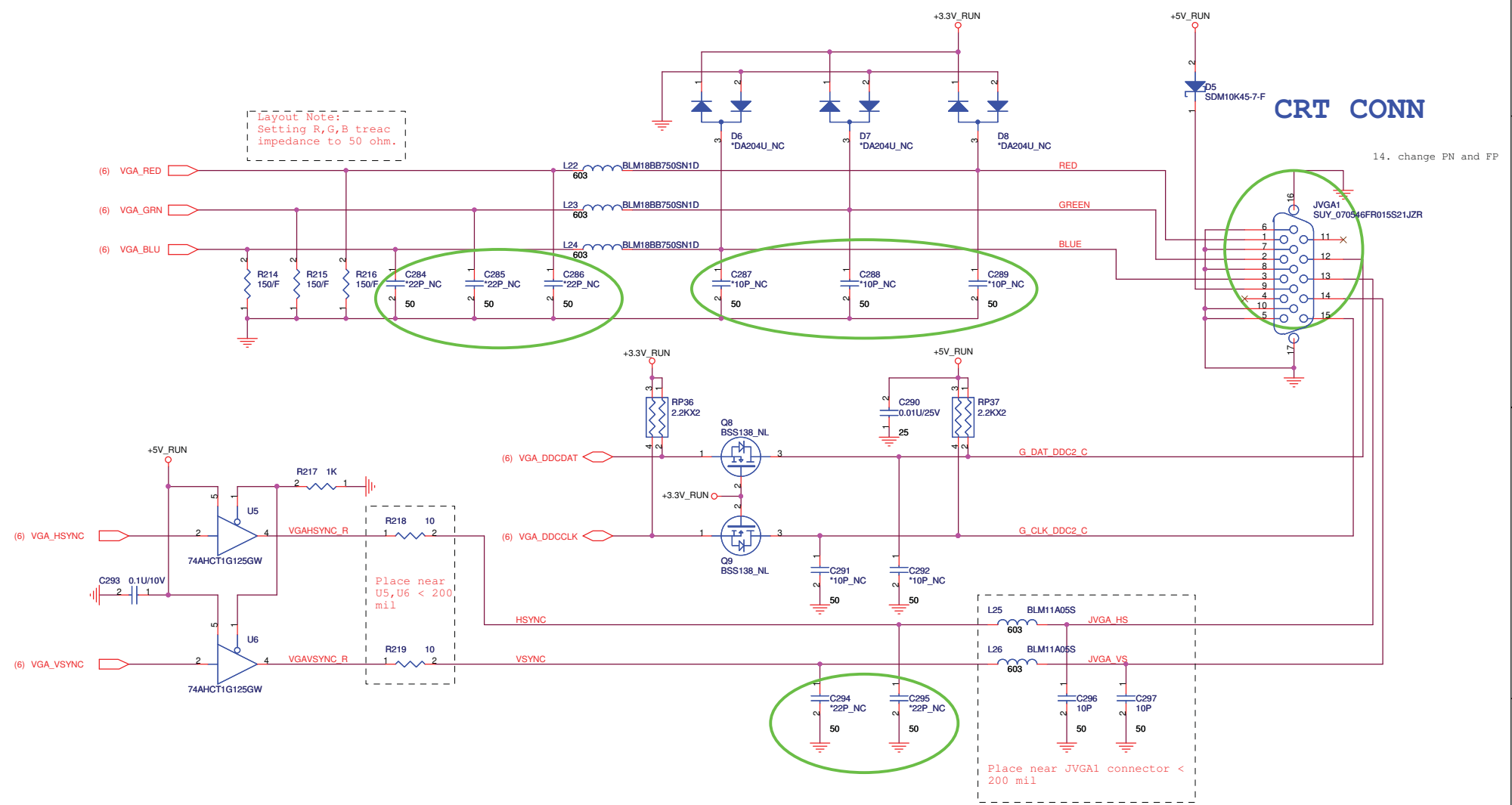


QUANTA COMPUTER

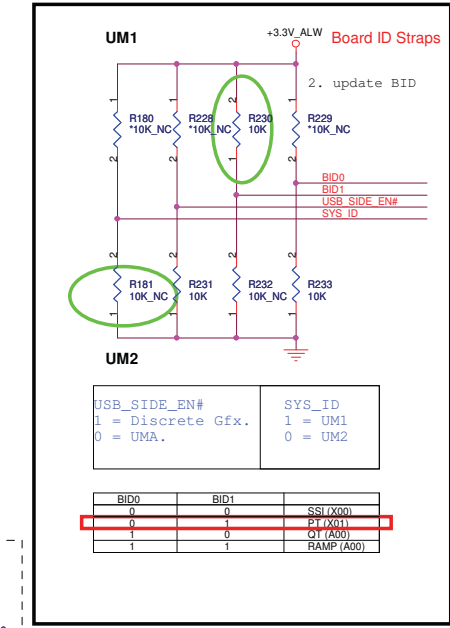
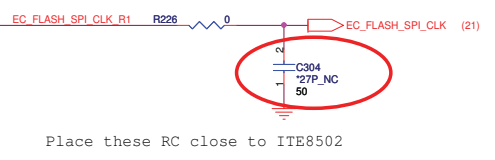
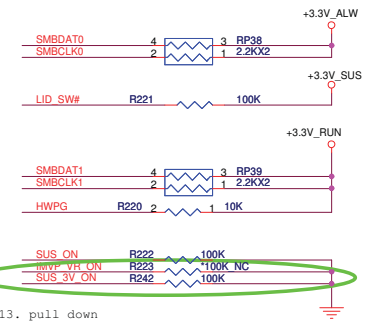
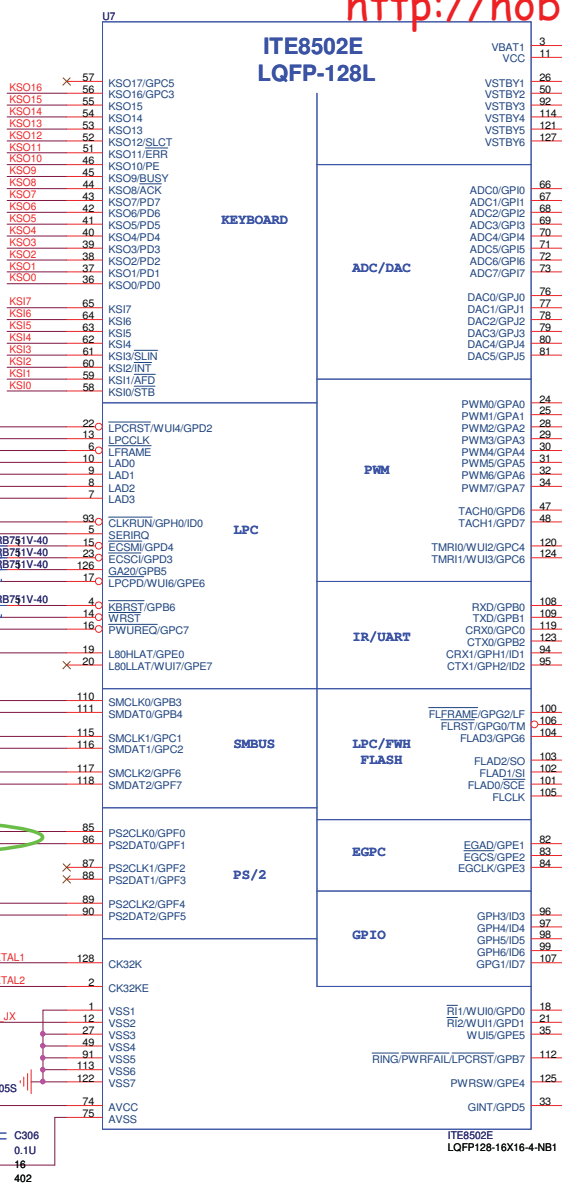
Title: LCD CONN & CCD

Size: Document Number UM2 UMA Rev 2A

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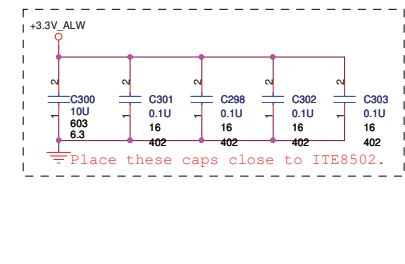
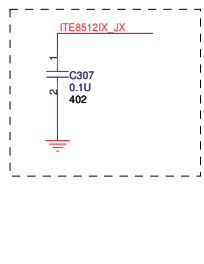
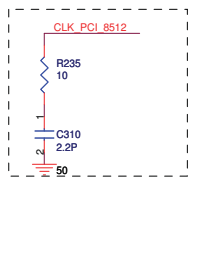
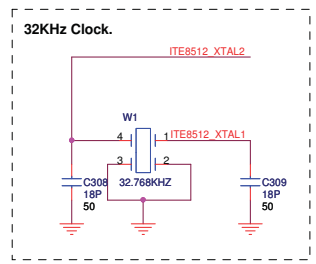
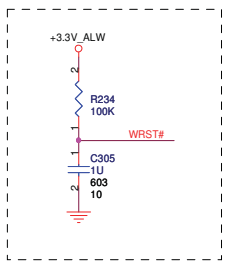
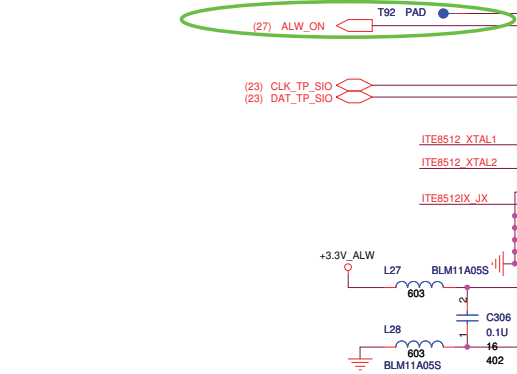


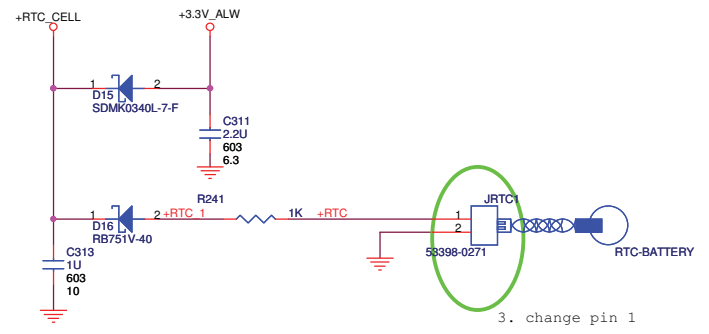
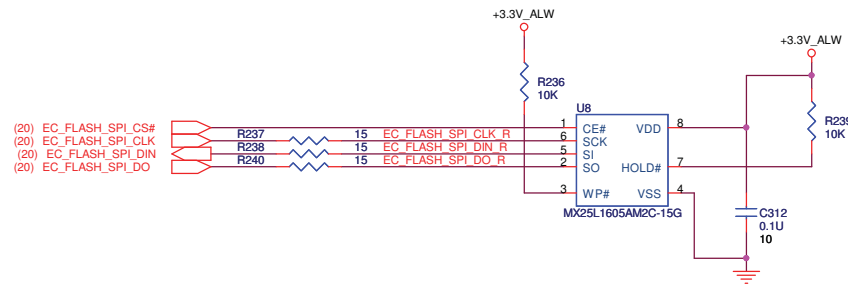
(23) KSO[0..16]
(23) KSJ[0..7]



Charge and BAT

11. add ALW_ON for 3.3V_ALW_ON





QUANTA COMPUTER

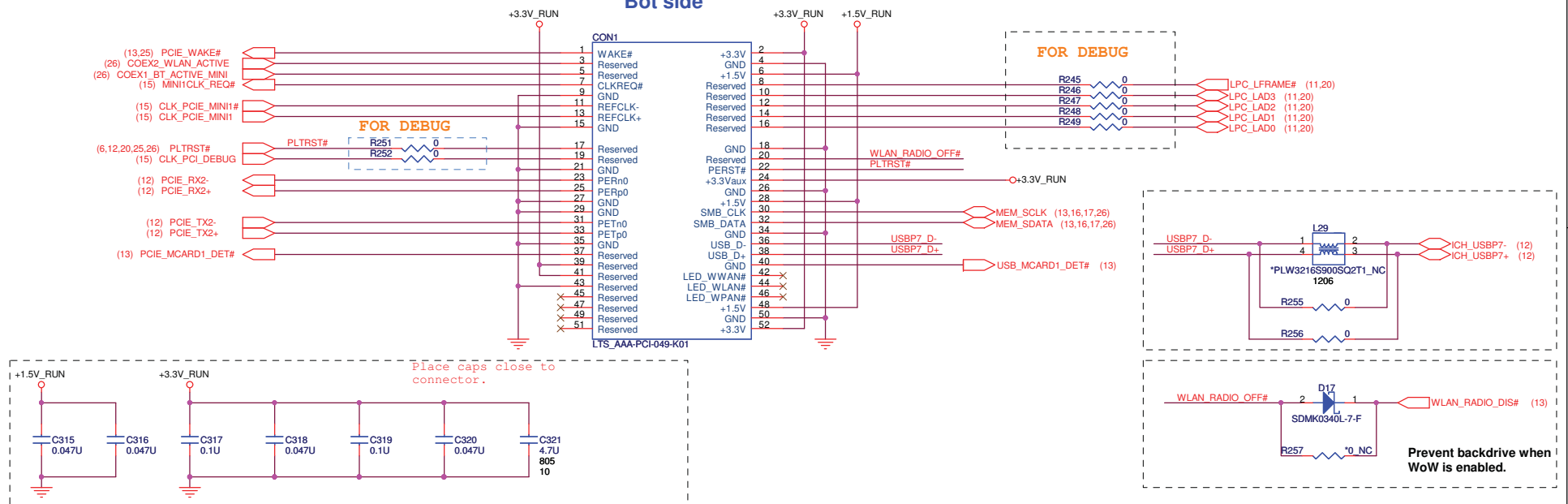
Title: Flash / RTC

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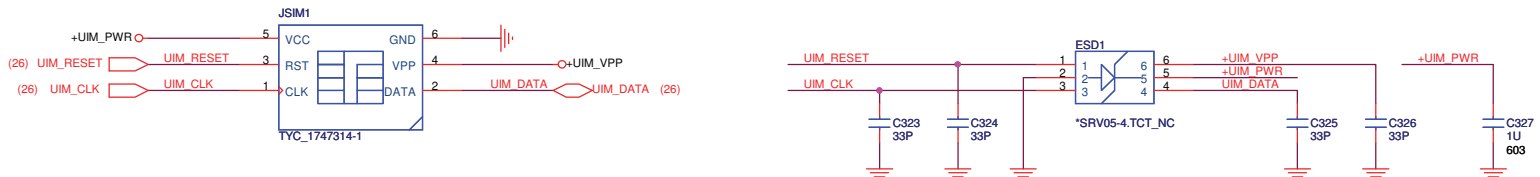
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MiniCard WLAN connector (Half) <http://hobi-elektronika.net>

Bot side



SIM CONN

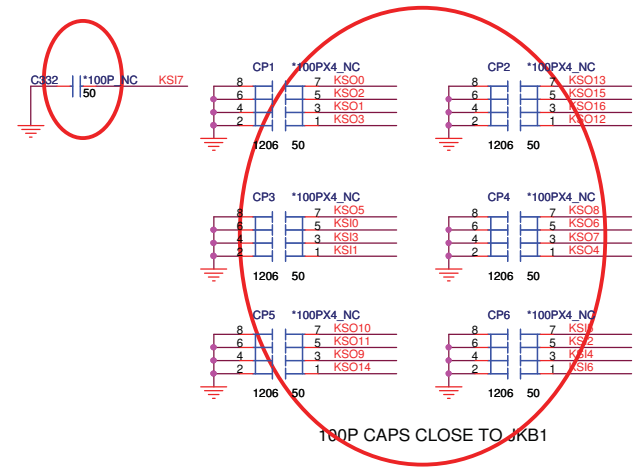
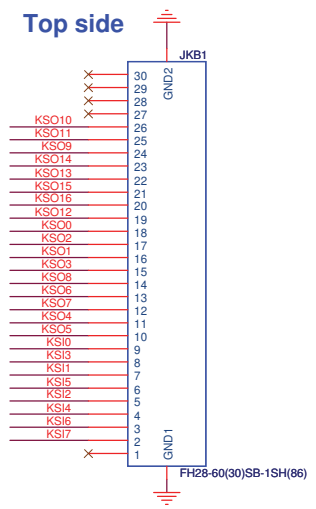


layout note: 10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil
Place as close as possible to WWAN connector

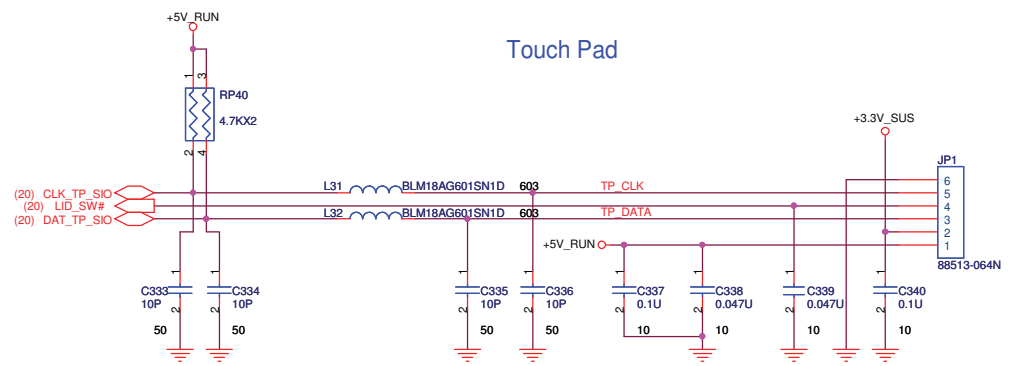


KEYBOARD CONN

(20) KSO[0..16]
(20) KSI[0..7]



Touch Pad CONN

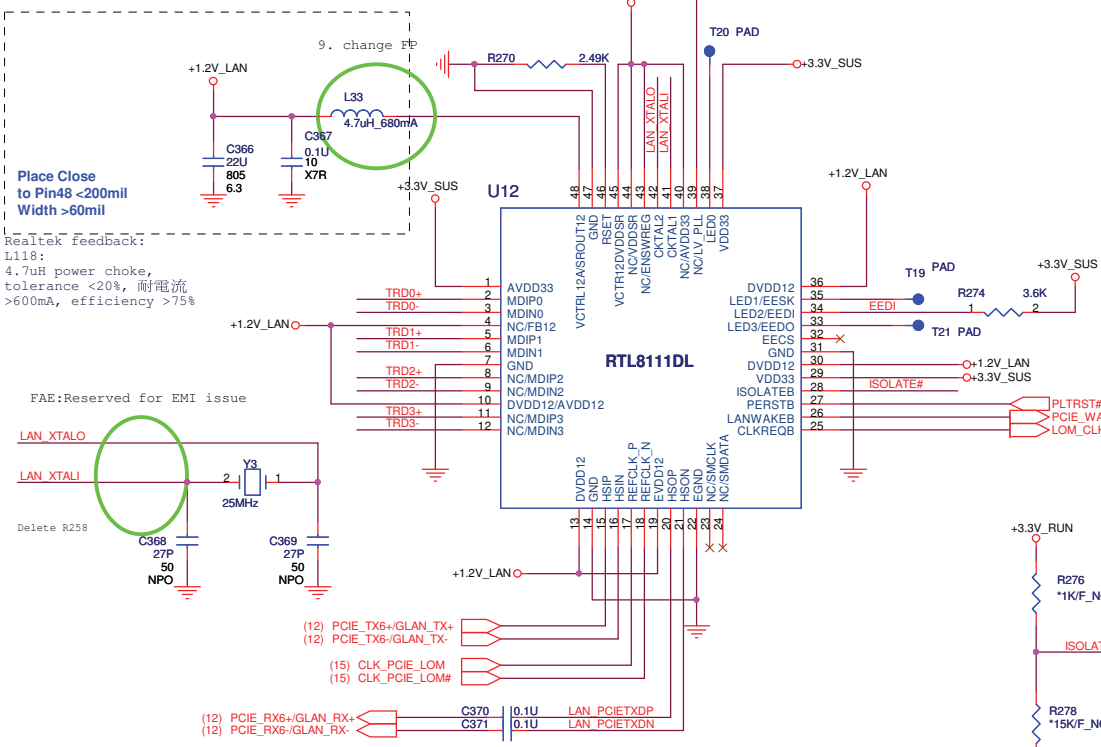
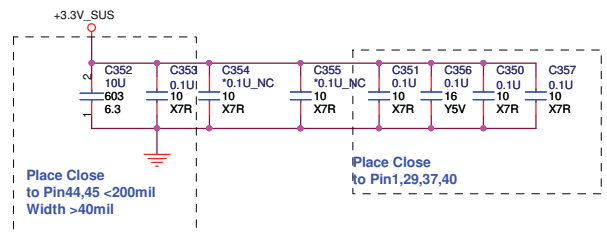
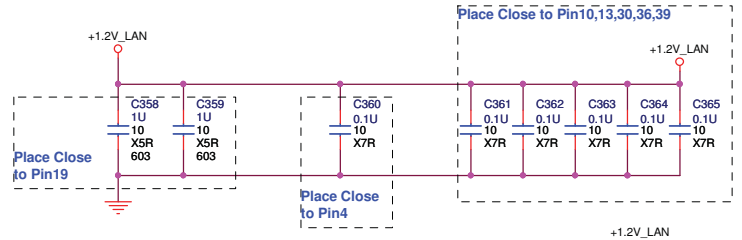


QUANTA COMPUTER

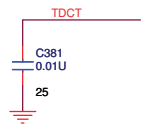
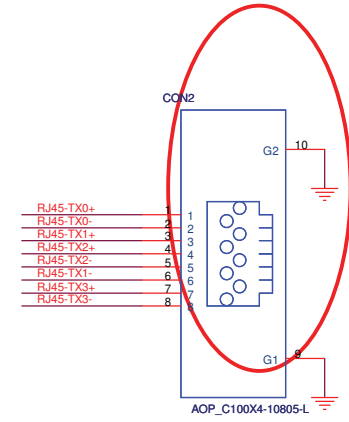
Title: TOUCH PAD, KEYBOARD

Size: Document Number UM2 UMA Rev 2A

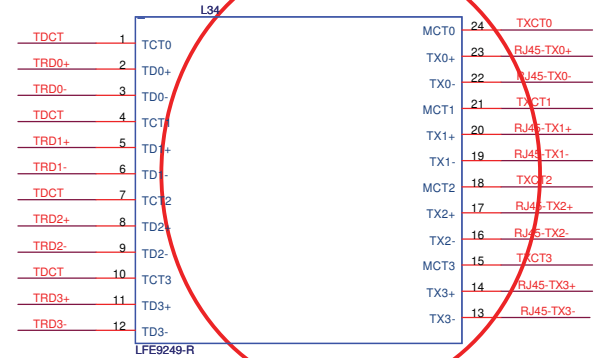
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ISOLATEB
 Datasheet(V1.4)P5:
 Used to isolate the RTL8111DL from the PCI-E bus. RTL8111DL will not drive its PCI-E outputs(excluding LANWAKEB) and will not sample its PCI-E input as long as the isolate pin is asserted.
 Realtek feed back:
 進入S3,S4,S5要
 拉low 離開S3,S4,S5要拉high for WOL support



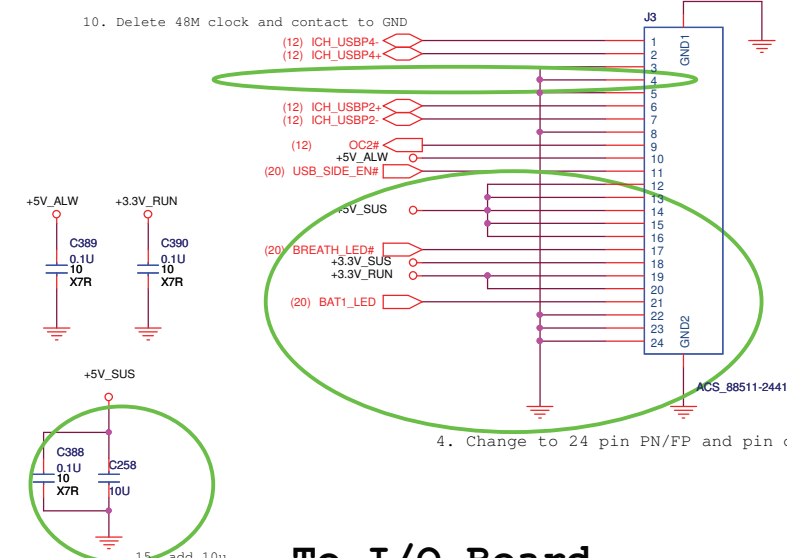
LAYOUT NOTE:
 CAP CLOSE TO TRANSFORMER
 one cap for each pin
 Reserved for EMI.



Title LAN/RJ45		
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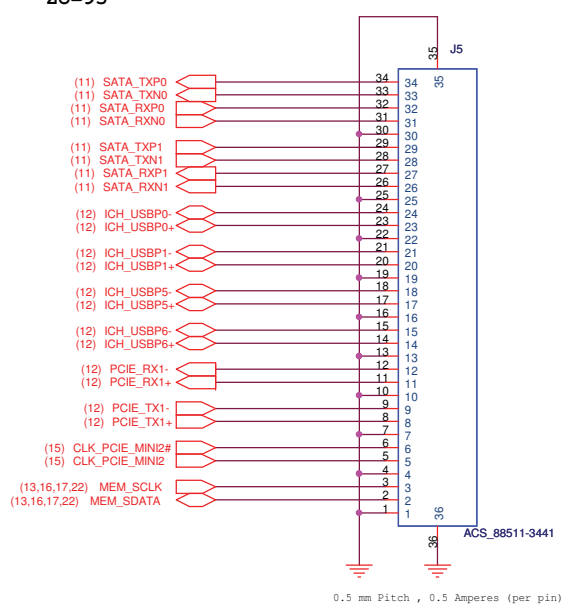
To CardReader Board

Cable connect to DB directly
DB need to reverse pin definition with MB



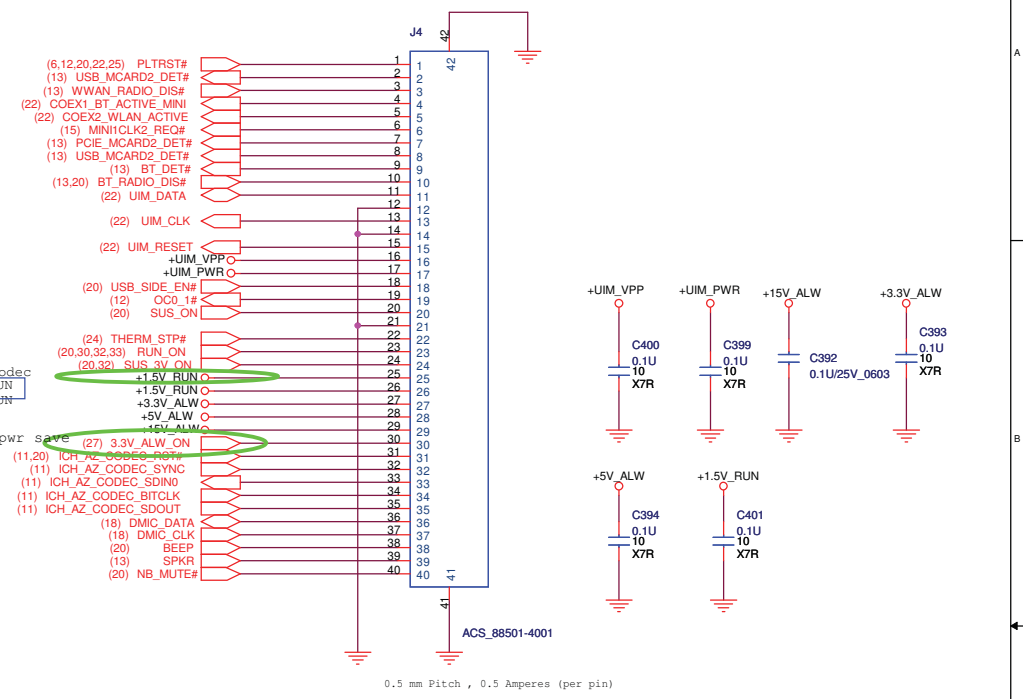
To I/O Board

Cable connect to DB directly
DB need to reverse pin definition with MB
Zo=95

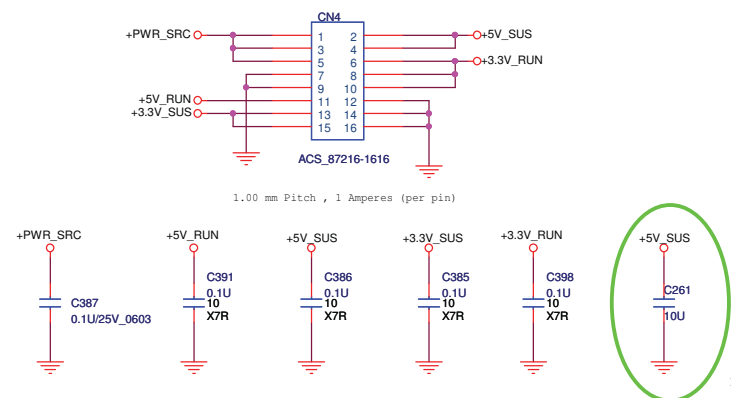


To I/O Board

FFC connect to DB with one turn
DB need to follow pin definition with MB



To I/O Board

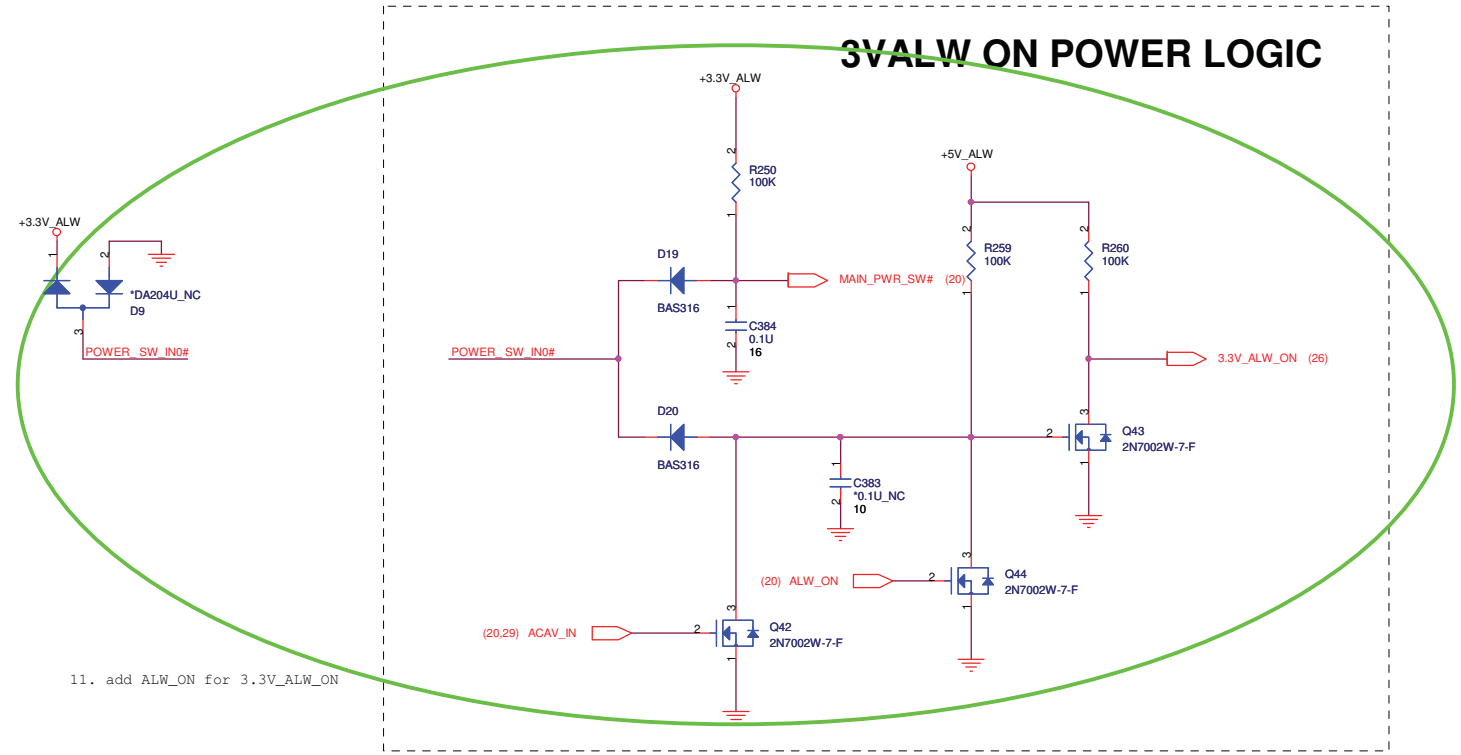
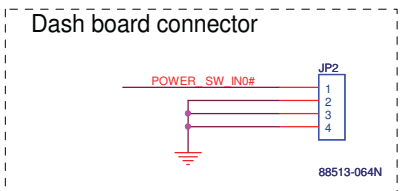


QUANTA COMPUTER


Title: IO BOARD

Size	Document Number UM2 UMA	Rev 2A
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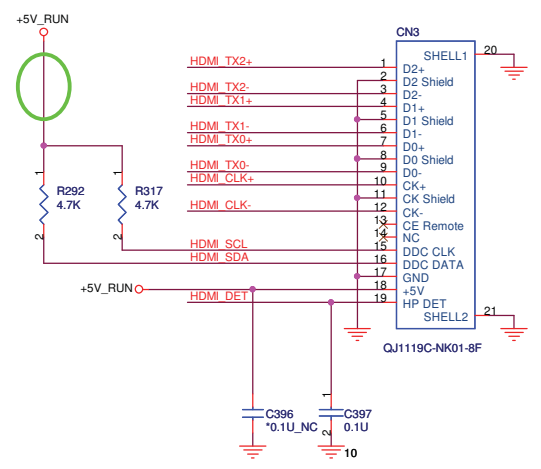
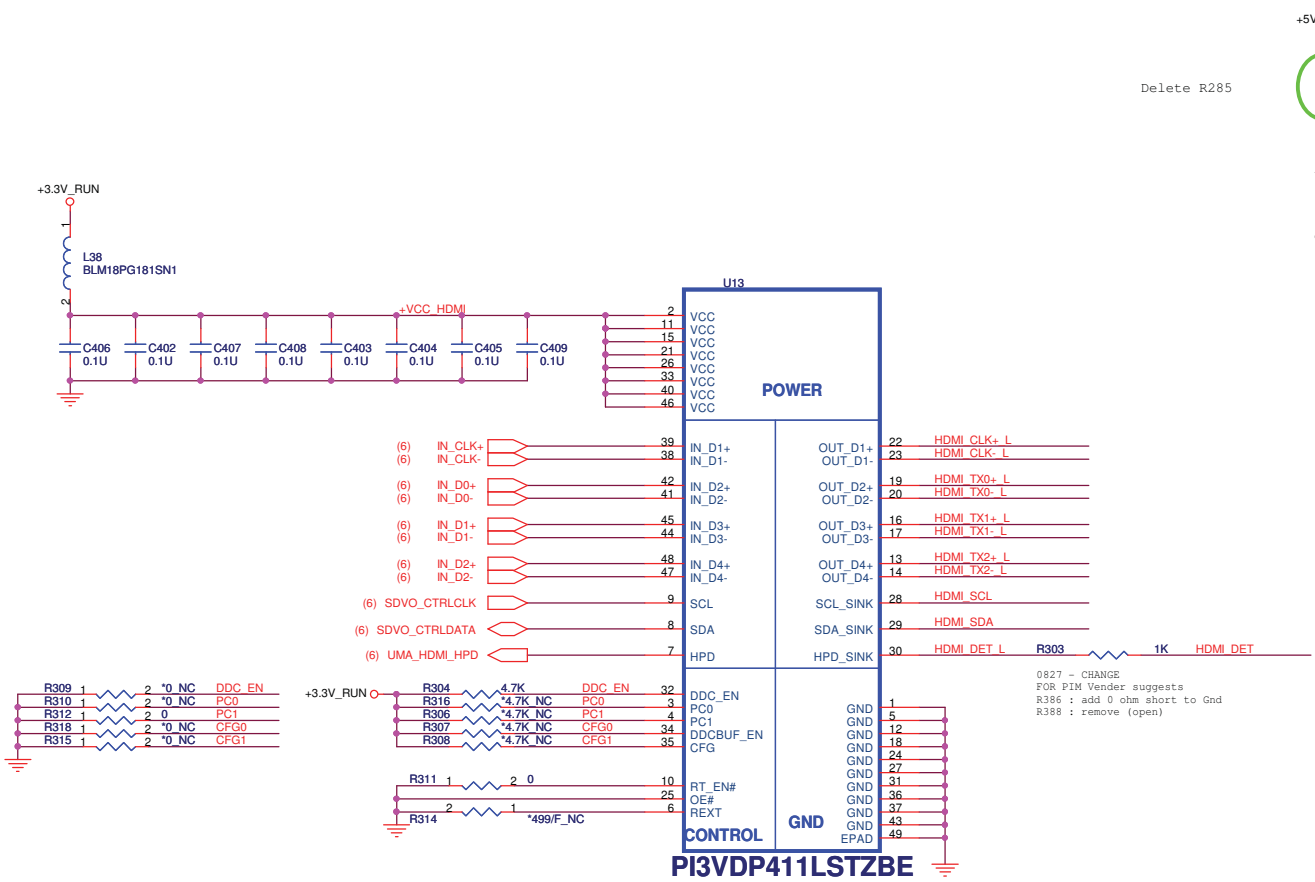
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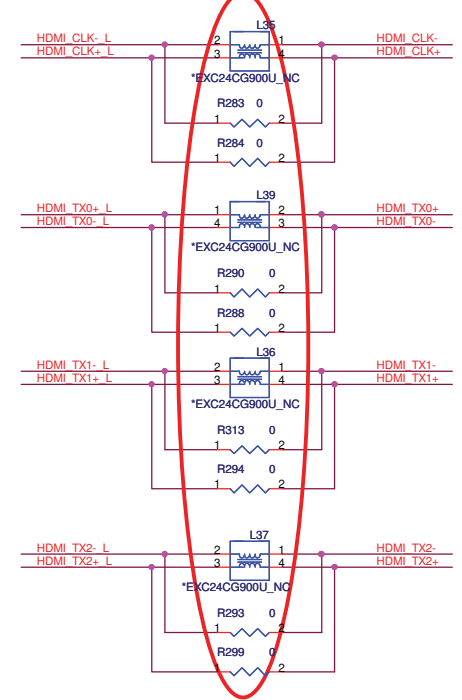
11. add ALW_ON for 3.3V_ALW_ON

 QUANTA COMPUTER		
Title POWER SWITCH		
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HDMI Connector



Reserve for EMI and close to HDMI CONN

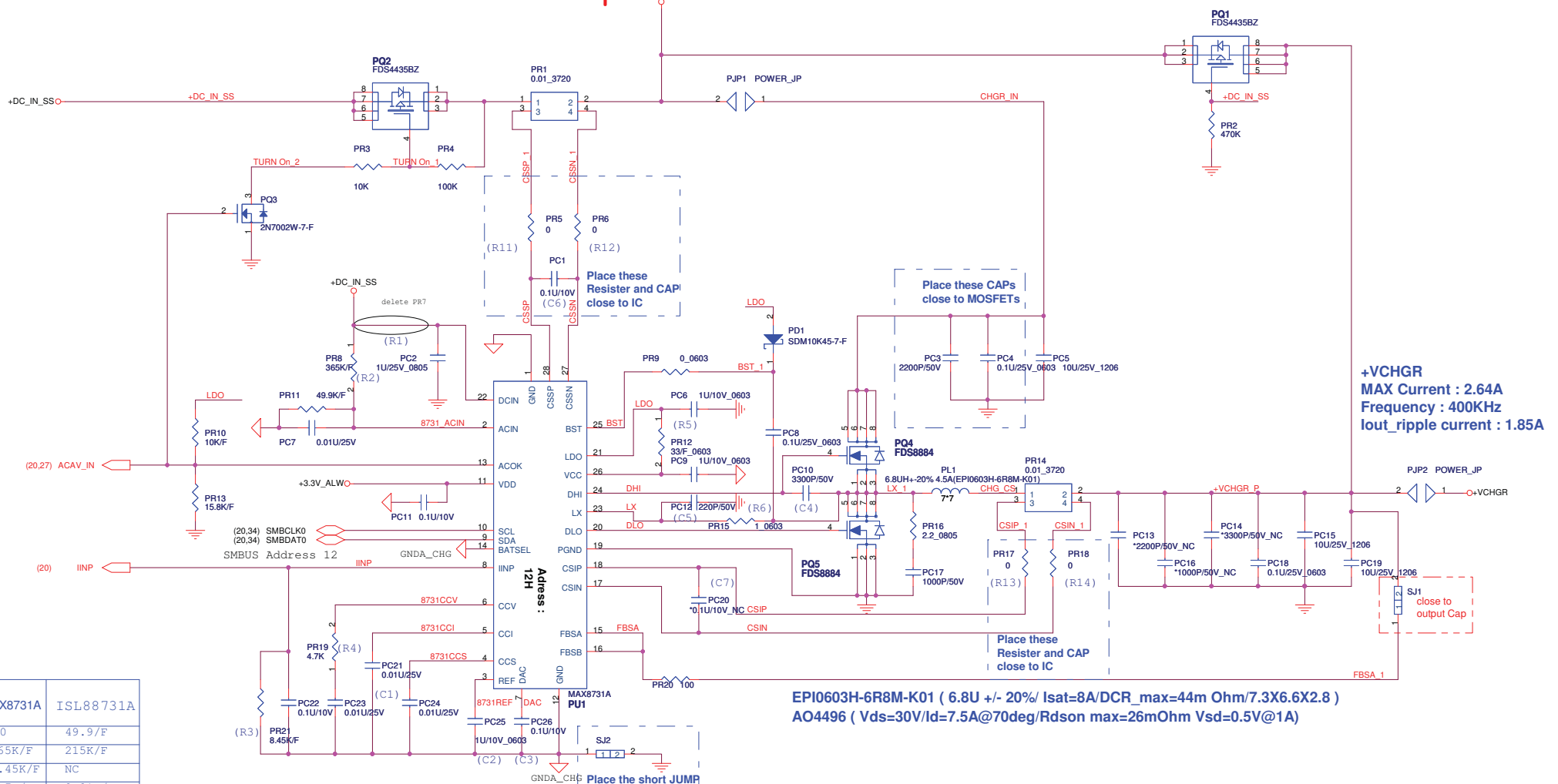


EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
 CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
 CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V



Title HDMI		
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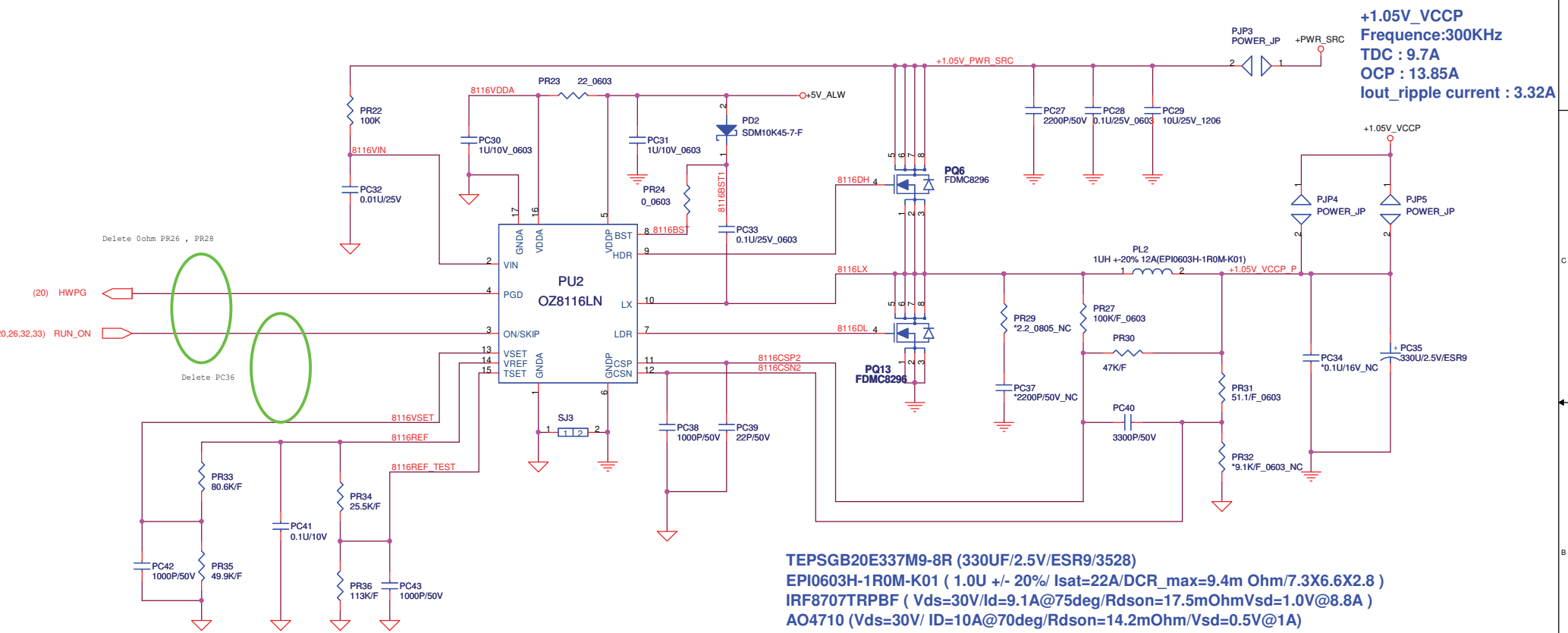
+VCHGR
 MAX Current : 2.64A
 Frequency : 400KHz
 lout_ripple current : 1.85A

EPI0603H-6R8M-K01 (6.8U +/- 20%/ Isat=8A/DCR_max=44m Ohm/7.3X6.6X2.8)
AO4496 (Vds=30V/Id=7.5A@70deg/Rdson max=26mOhm Vsd=0.5V@1A)

	MAX8731A	ISL88731A
R1	0	49.9/F
R2	365K/F	215K/F
R3	8.45K/F	NC
R4	4.7K/F	2.21K/F
R5	33/F	4.7/F
R6	1	0
R7	NC	NC
R8	0	0
R9	NC	NC
R10	0	0
R11	0	10/F
R12	0	10/F
R13	0	10/F
R14	0	10/F
C1	0.01uF	NC
C2	1uF	NC
C3	0.1uF	NC
C4	3300PF	NC
C5	220PF	NC
C6	NC	0.1uF
C7	NC	0.1uF

TABLE 1

ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

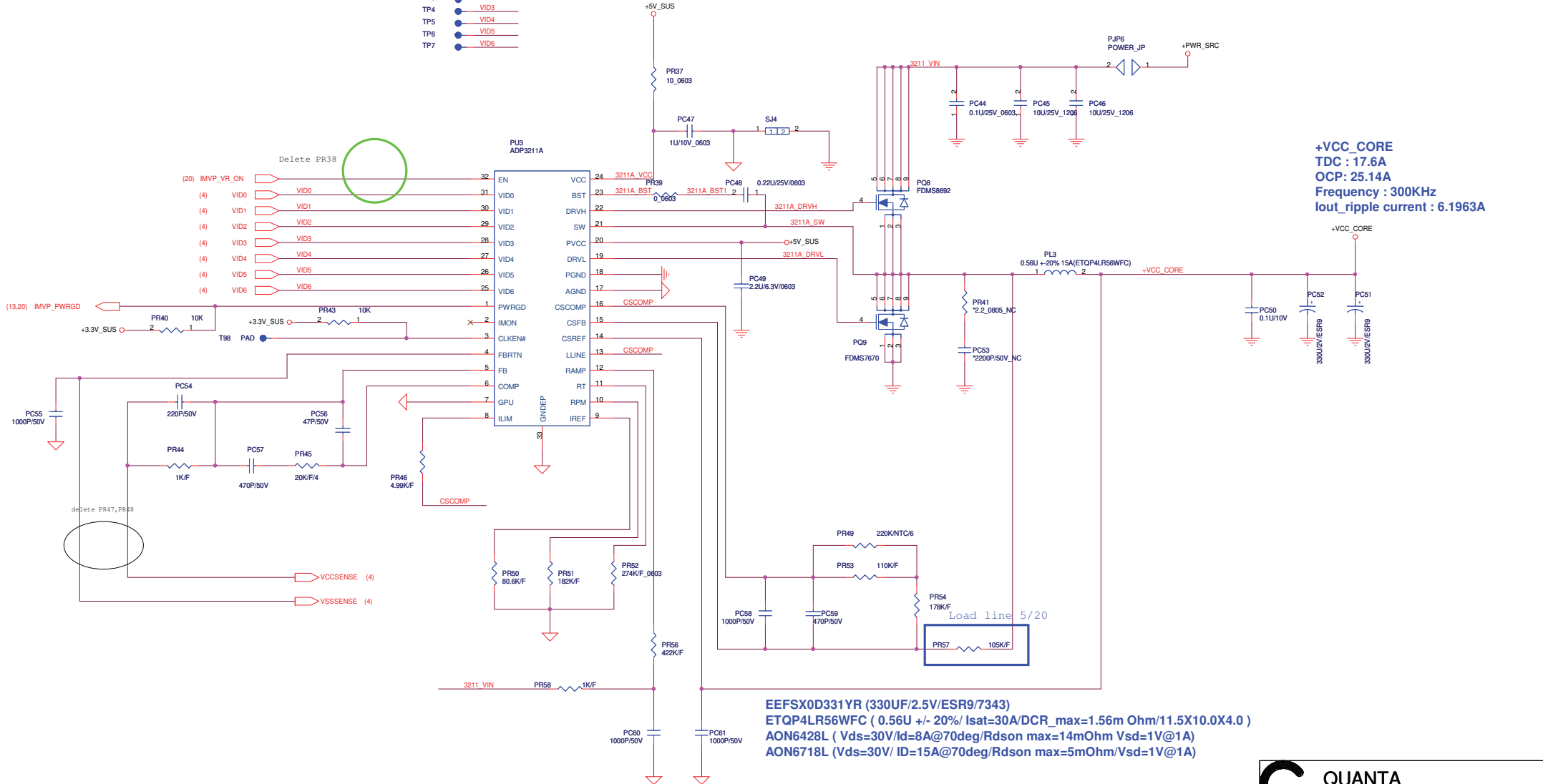


+1.05V_VCCP
 Frequency:300KHz
 TDC : 9.7A
 OCP : 13.85A
 Iout_ripple current : 3.32A

TEPSGB20E337M9-8R (330UF/2.5V/ESR9/3528)
 EPI0603H-1R0M-K01 (1.0U +/- 20%/ Isat=22A/DCR_max=9.4m Ohm/7.3X6.6X2.8)
 IRF8707TRPBF (Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhmVsd=1.0V@8.8A)
 AO4710 (Vds=30V/ ID=10A@70deg/Rdson=14.2mOhm/Vsd=0.5V@1A)

CPU CORE

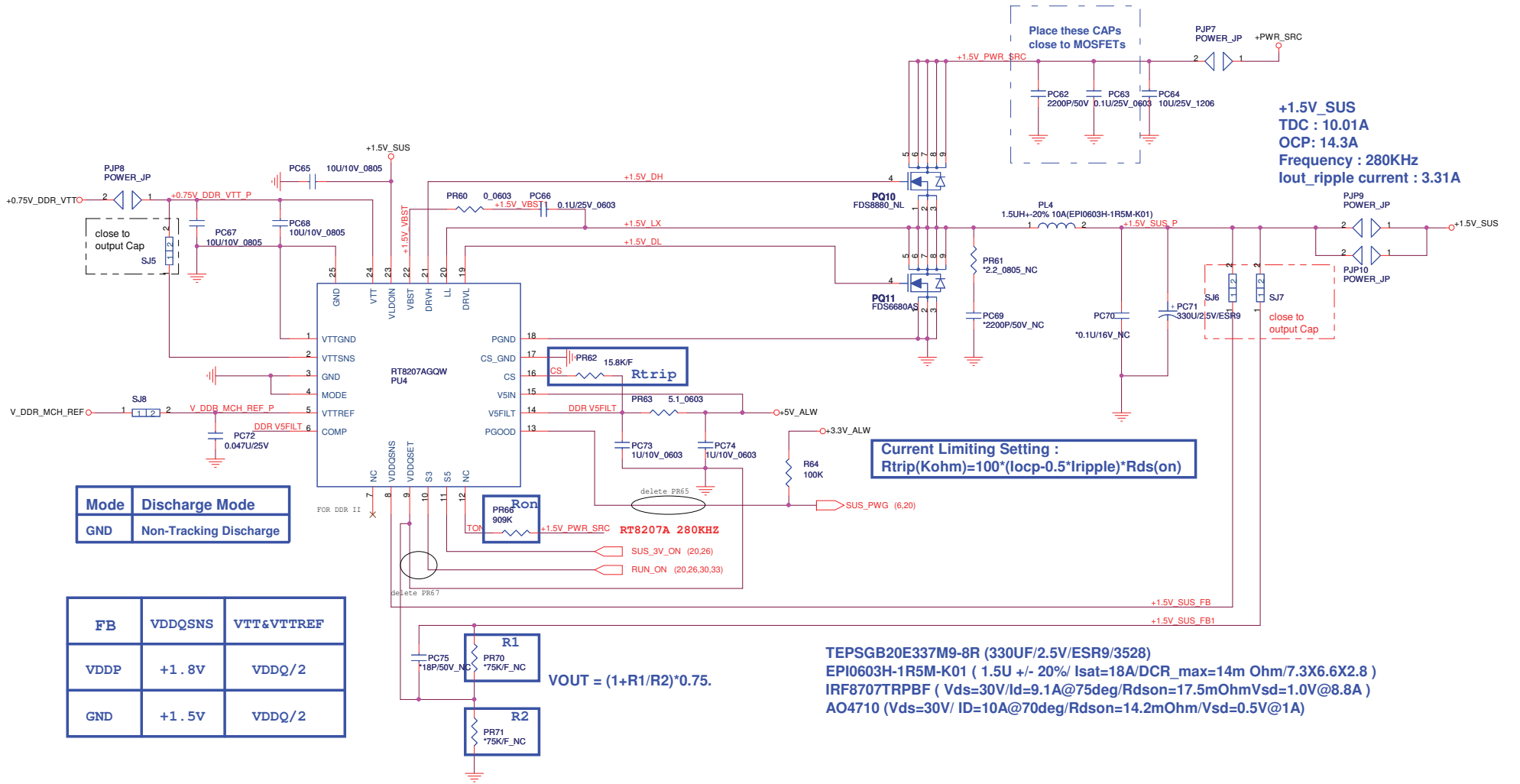
- TP1 ● VID0
- TP2 ● VID1
- TP3 ● VID2
- TP4 ● VID3
- TP5 ● VID4
- TP6 ● VID5
- TP7 ● VID6



+VCC_CORE
 TDC : 17.6A
 OCP: 25.14A
 Frequency : 300KHz
 Iout_ripple current : 6.1963A

EEFSX0D331YR (330UF/2.5V/ESR9/7343)
 ETQP4LR56WFC (0.56U +/- 20%/ Isat=30A/DCR_max=1.56m Ohm/11.5X10.0X4.0)
 AON6428L (Vds=30V/Id=8A@70deg/Rdson max=14mOhm Vsd=1V@1A)
 AON6718L (Vds=30V/ ID=15A@70deg/Rdson max=5mOhm/Vsd=1V@1A)

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+1.5V_SUS
 TDC : 10.01A
 OCP: 14.3A
 Frequency : 280KHz
 Iout_ripple current : 3.31A

Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

Mode	Discharge Mode
GND	Non-Tracking Discharge

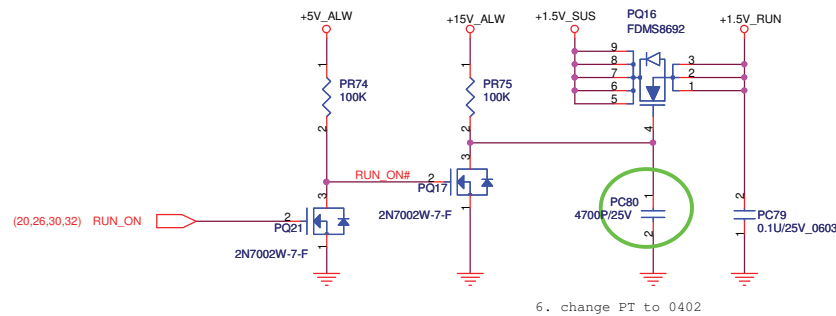
FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

$V_{OUT} = (1 + R1/R2) * 0.75.$

TEPSGB20E337M9-8R (330UF/2.5V/ESR9/3528)
 EPI0603H-1R5M-K01 (1.5U +/- 20% / Isat=18A/DCR_max=14m Ohm/7.3X6.6X2.8)
 IRF8707TRPBF (Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhm/Vsd=1.0V@8.8A)
 AO4710 (Vds=30V/ ID=10A@70deg/Rdson=14.2mOhm/Vsd=0.5V@1A)

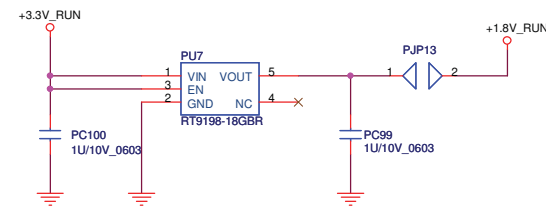
+1.5V_RUN

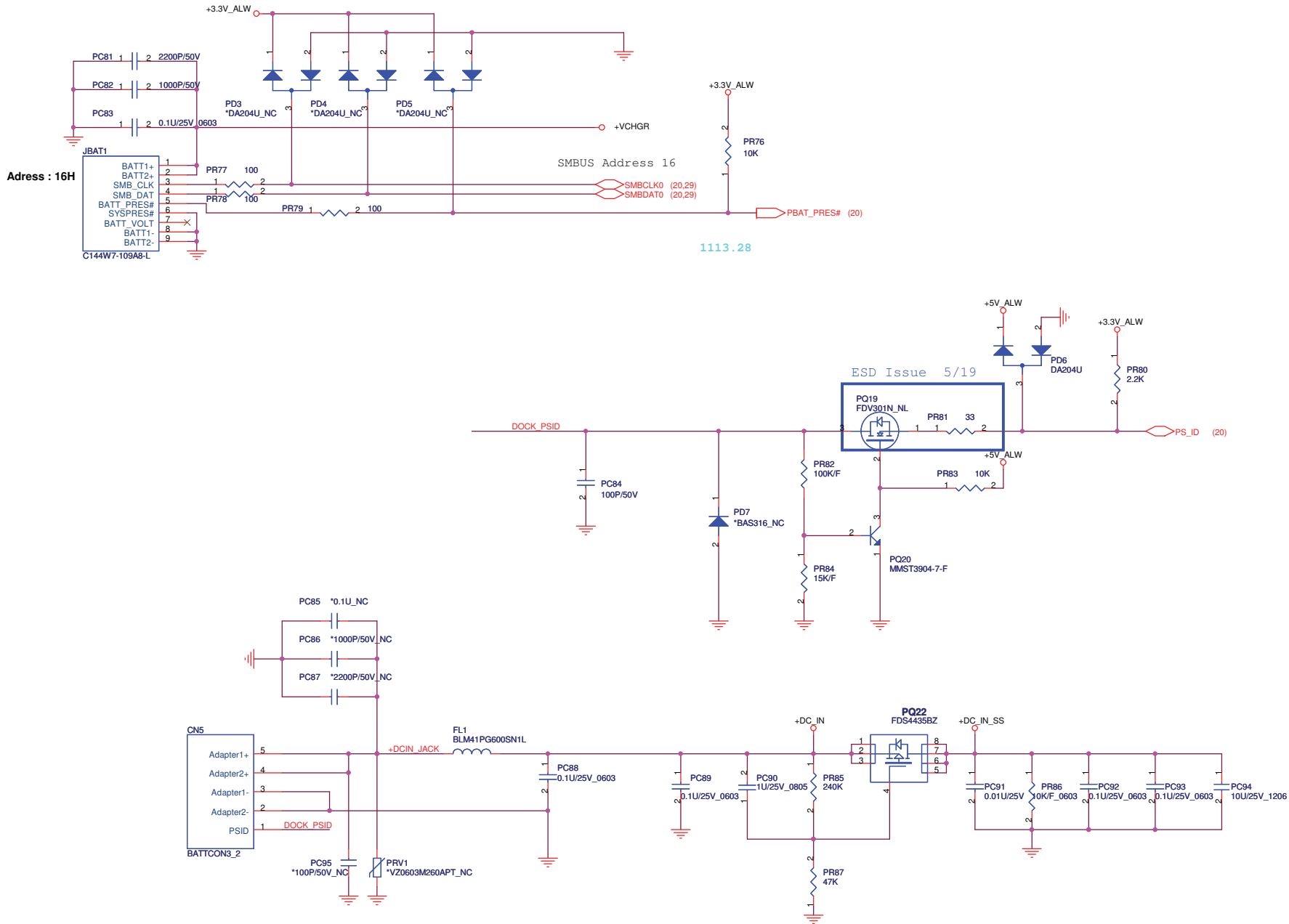
Max current(TDC) : 1.6A

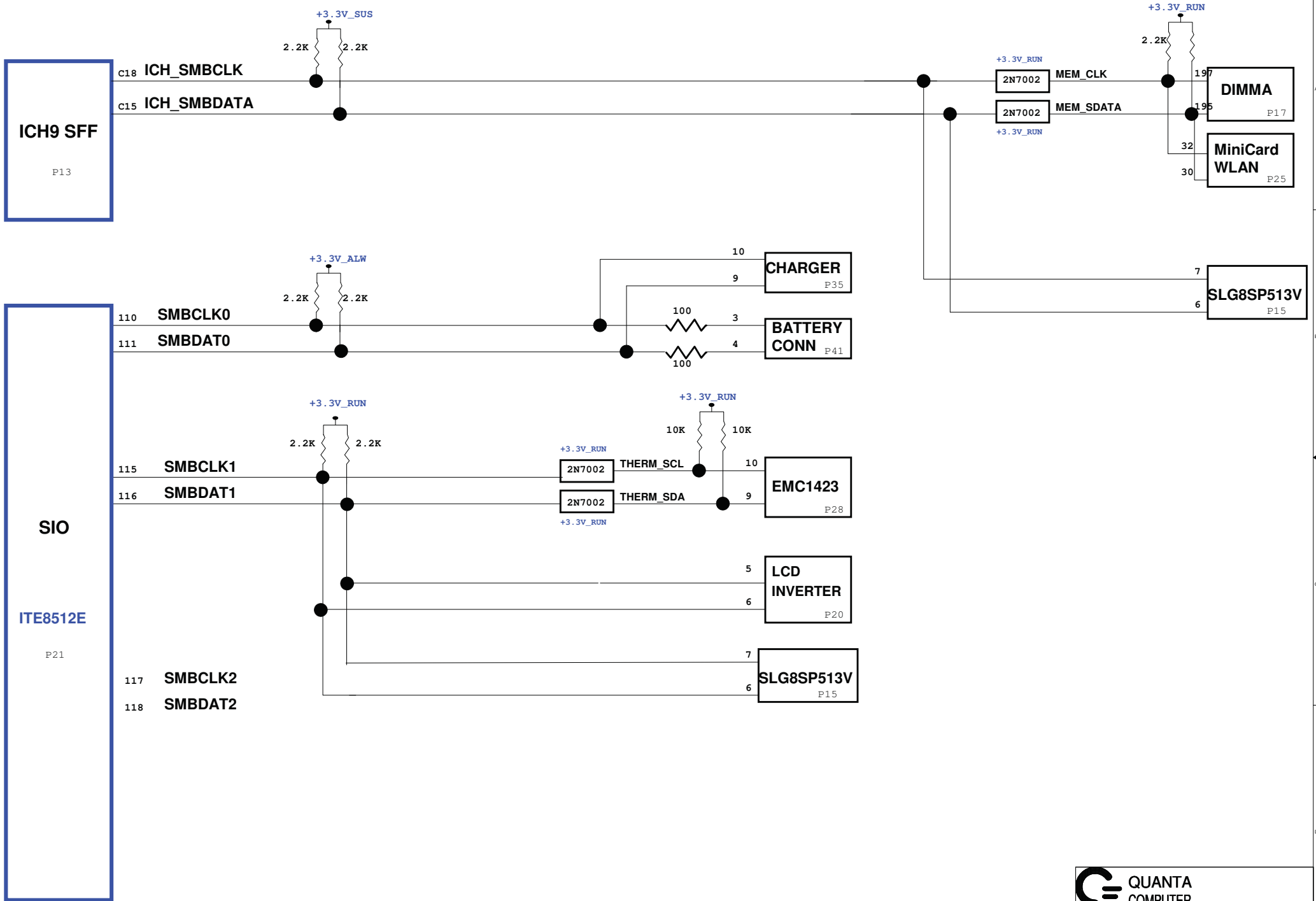


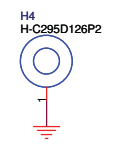
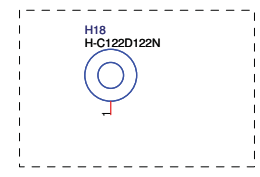
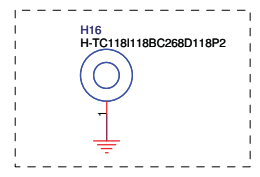
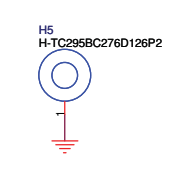
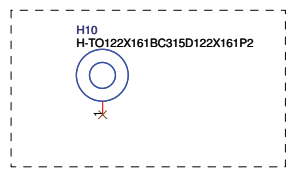
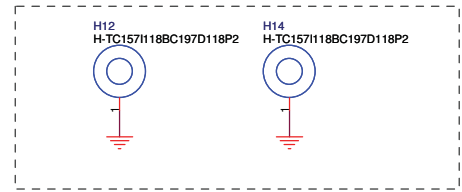
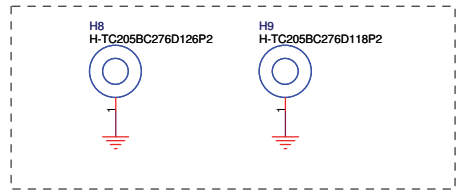
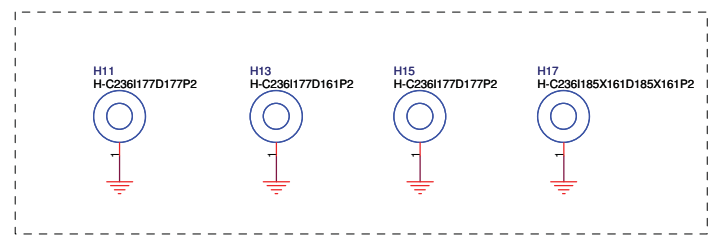
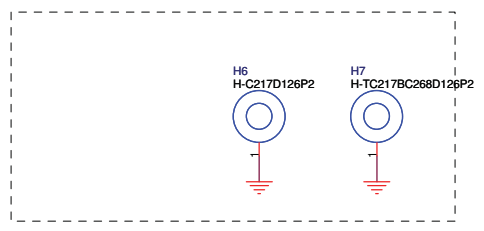
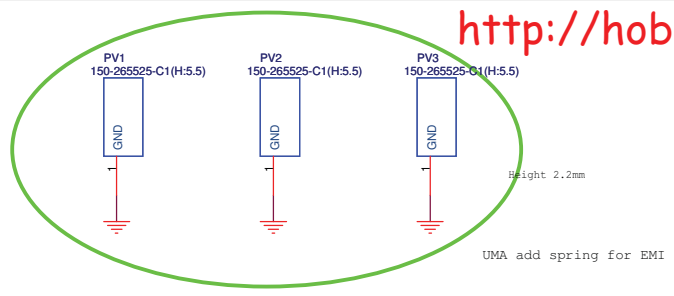
+1.8V_RUN


Max current (TDC) ->105mA
For UMA









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Title: PAD & SCREW & SPRING		
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