

Mosaic Schematics Document
uFCBGA/uFCPGA Northwood

2001-09-19

REV: 0.1

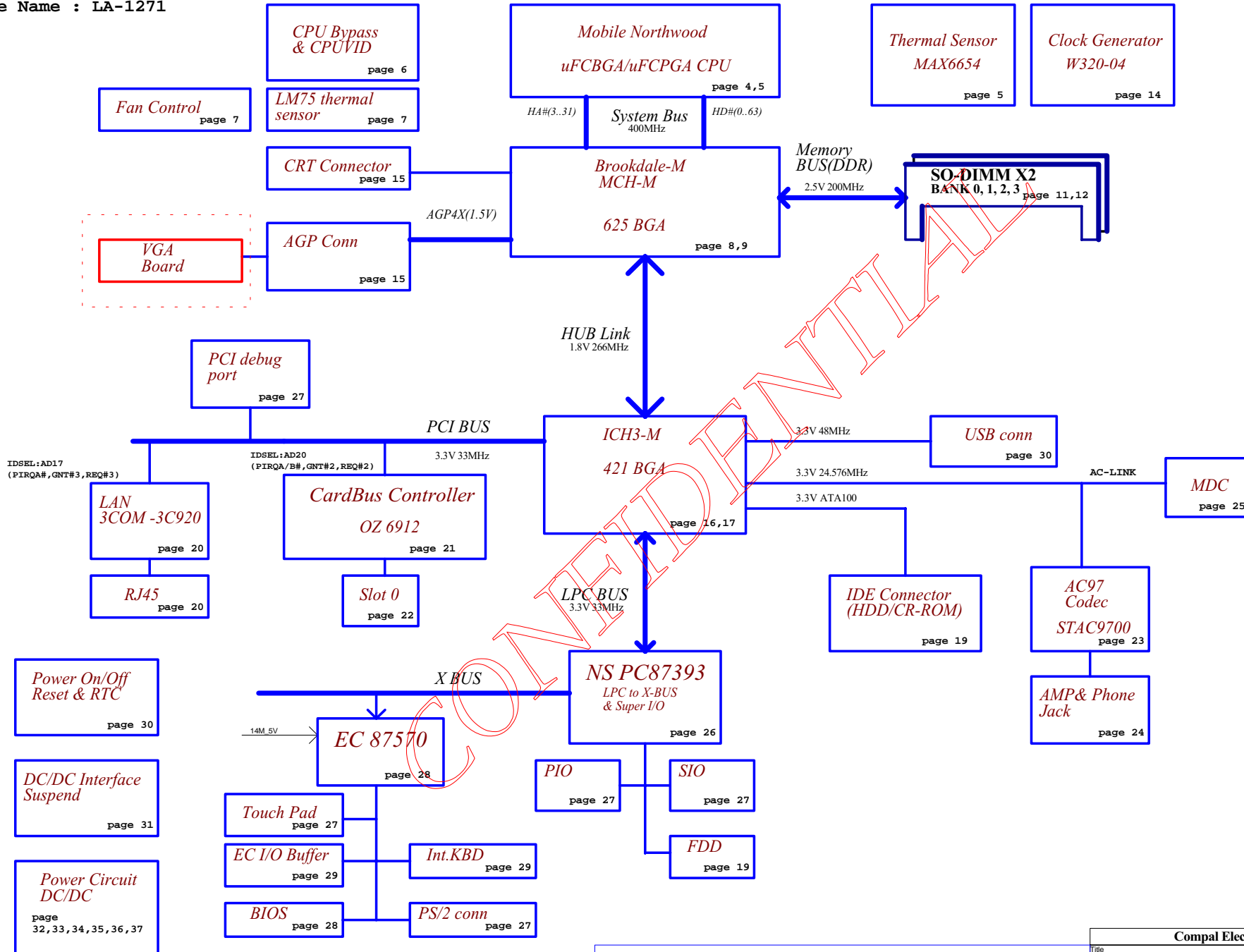
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Compal Electronics, Inc.		
Title		
Cover Sheet		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date:	Wednesday, September 19, 2001 Sheet 1 of 37	

Model Name :ADY13(Mosaic)

File Name : LA-1271



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Title Block Diagram		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Wednesday, September 19, 2001	Sheet 2 of 37

Function	Mosaic	Midas
FDD	YES	YES
PS/2	YES	YES
Serial port	NO	NO
Parallel port	YES	YES
RJ45	YES	YES
OZ6912/TPS2211	YES	YES
3Com Lan chipset(3C920)	YES S/W disable	YES

Power Managment table

Signal	+3VALW	+3V	+3VS
	+5VALW	+5V	+5VS
State	+1.8VALW	+2.5V	+1.8VS
	+12VALW		+1.5VS
			+1.2VP
			+CPU_CORE
			+1.25V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

SST-Build	CHIPS Rev	CHIPS Rev
	RG82845	FW82801CAM
	A3(QC45)	B1(QC42)

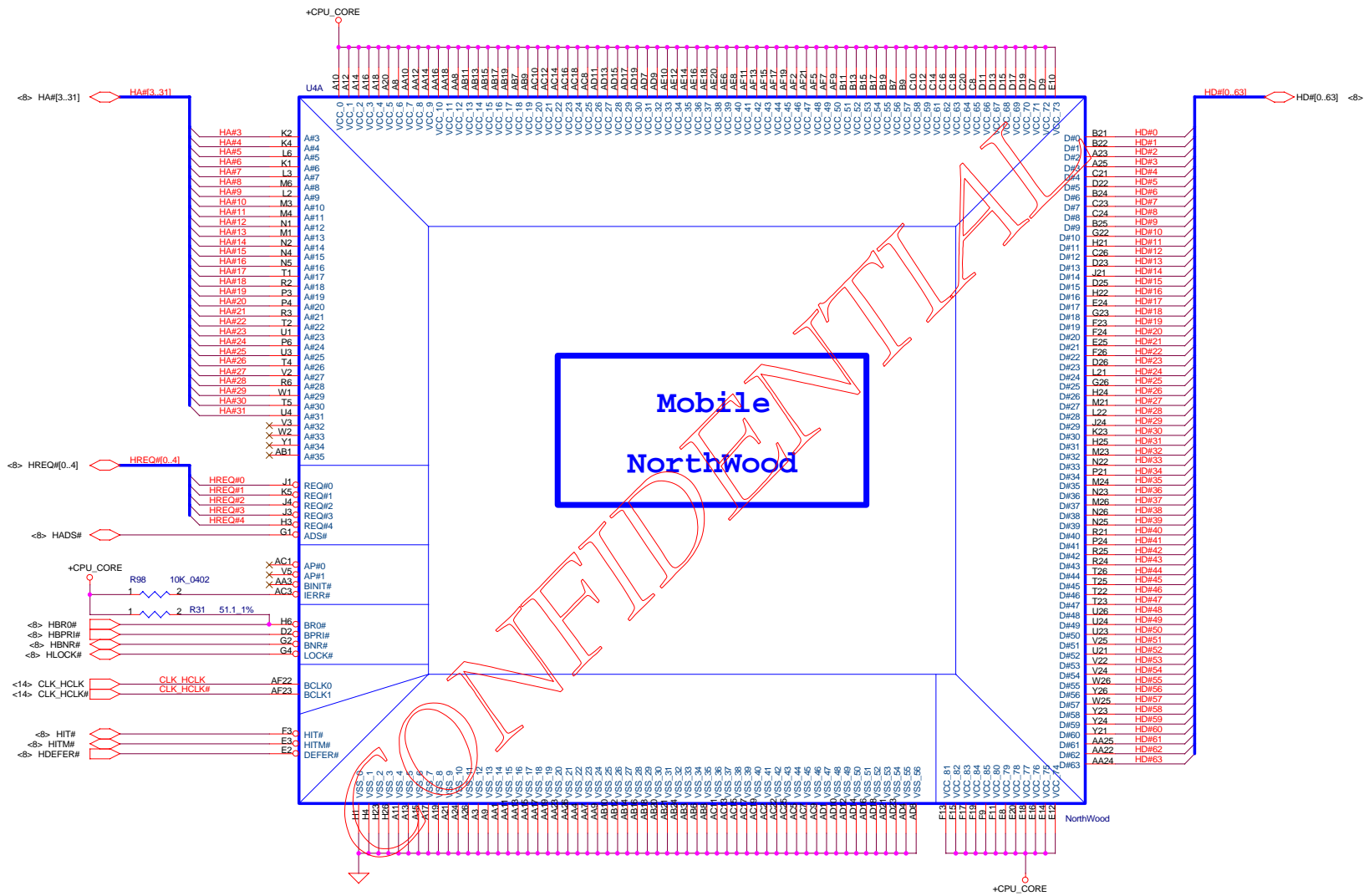
Note1: "@" means all model depop

Note2: Removed serial port,because add 2nd Fan

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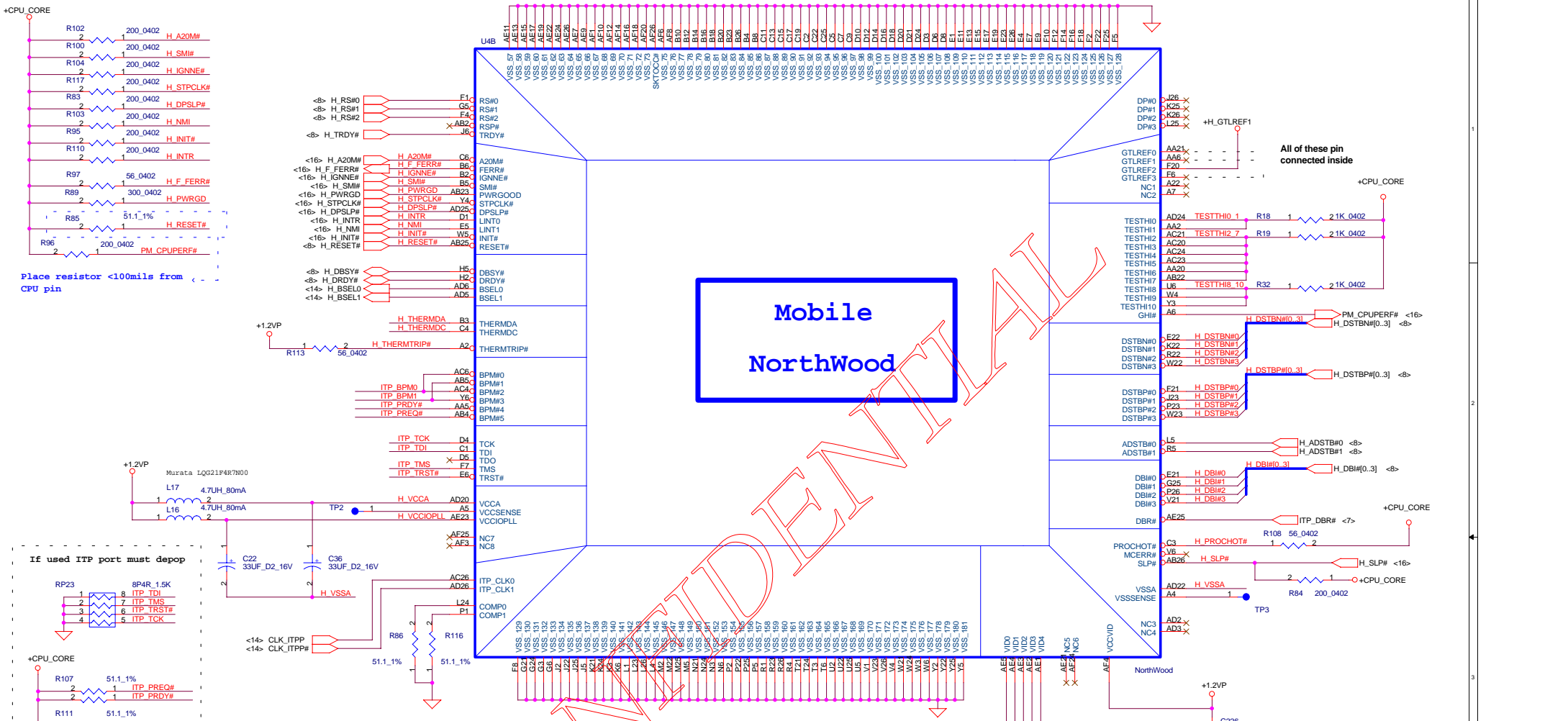
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Title Note & Revision		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date:	Wednesday, September 19, 2001 Sheet 3 of 37	



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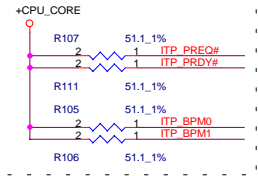
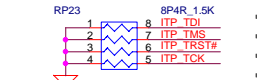
Compal Electronics, Inc.		
Mobile Northwood uFCPGA		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 4 of 37



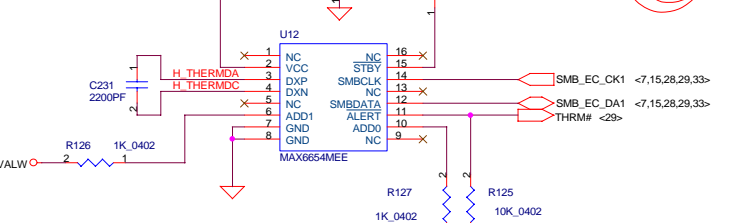
Mobile NorthWood

Place resistor <100mils from CPU pin

If used ITP port must depop



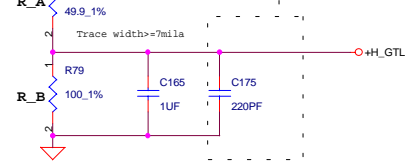
Thermal Sensor MAX6654MEE



Address:1001_110X

GTL Reference Voltage

- Layout note:
1. Place R_A and R_B near CPU.
 2. Place decoupling cap 220PF near CPU.(Within 500mils)



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All of these pin connected inside

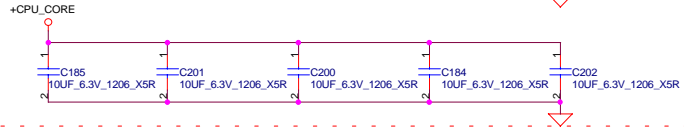
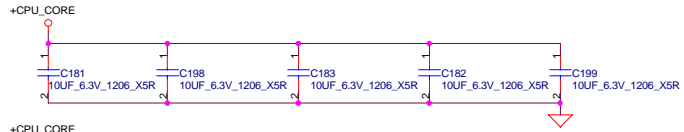
Compal Electronics, Inc.

Mobile NorthWood uFCPGA & Thermal sensor		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 5 of 37

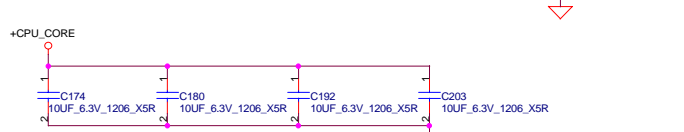
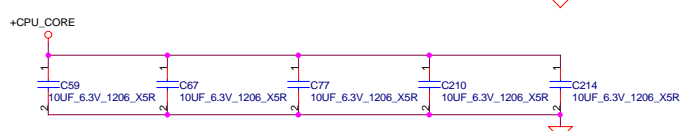
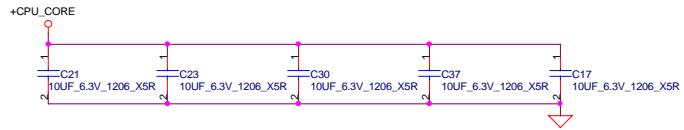
Layout note :

Place close to CPU. Use 2-3 vias per PAD.
 Place .22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

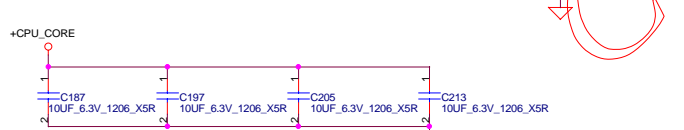
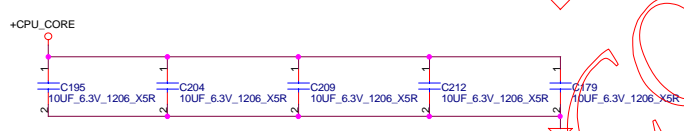
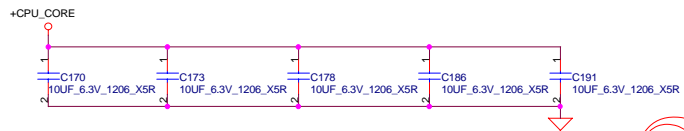
Please place these cap in the socket cavity area



Please place these cap on the socket north side



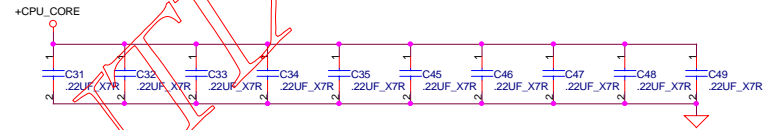
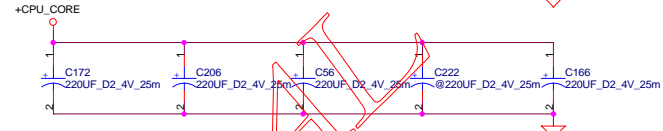
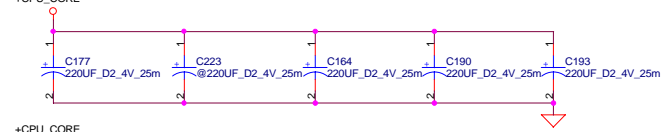
Please place these cap on the socket south side



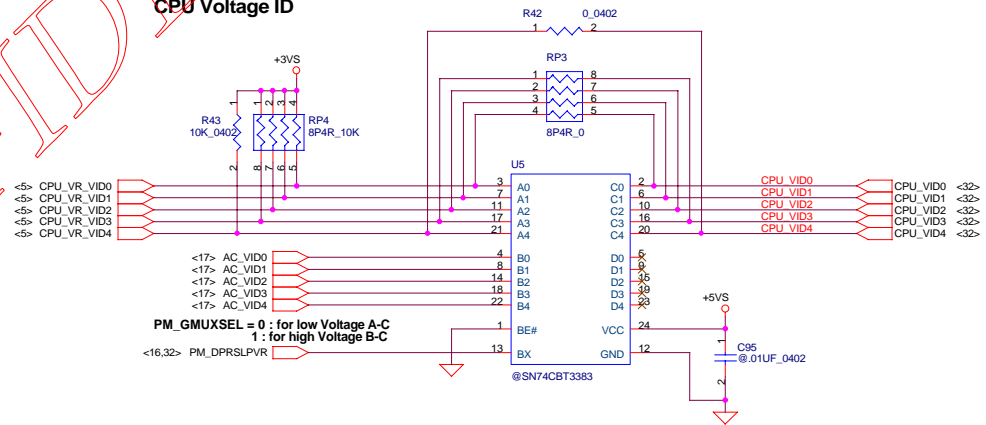
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

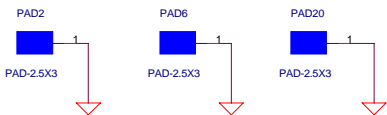
Used ESR 25m ohm cap total ESR=2.5m ohm



CPU Voltage ID

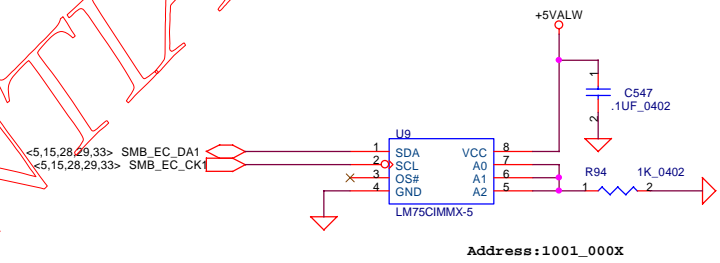
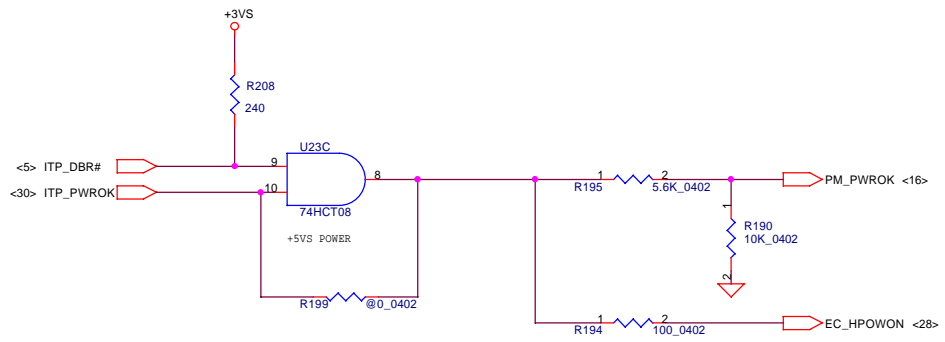


EMI Clip PAD for CPU



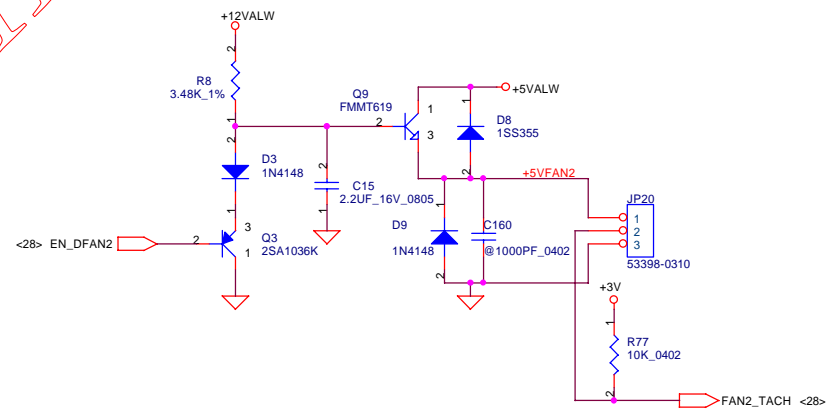
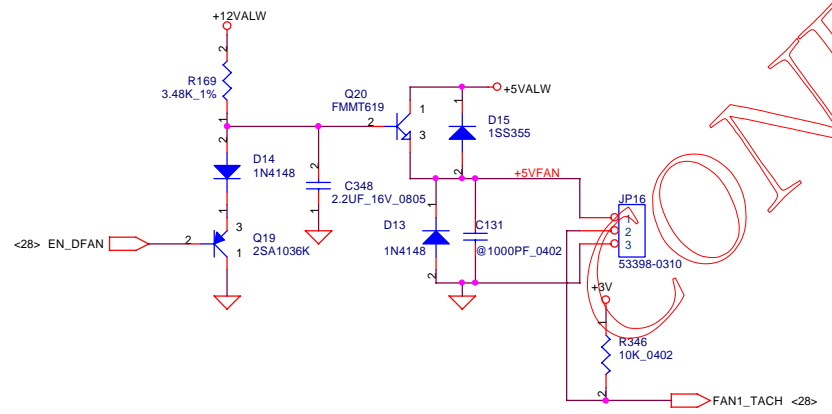
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Compal Electronics, Inc.		
CPU Bypass & CPU VID		
Title	Document Number	
Size	ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 6 of 37



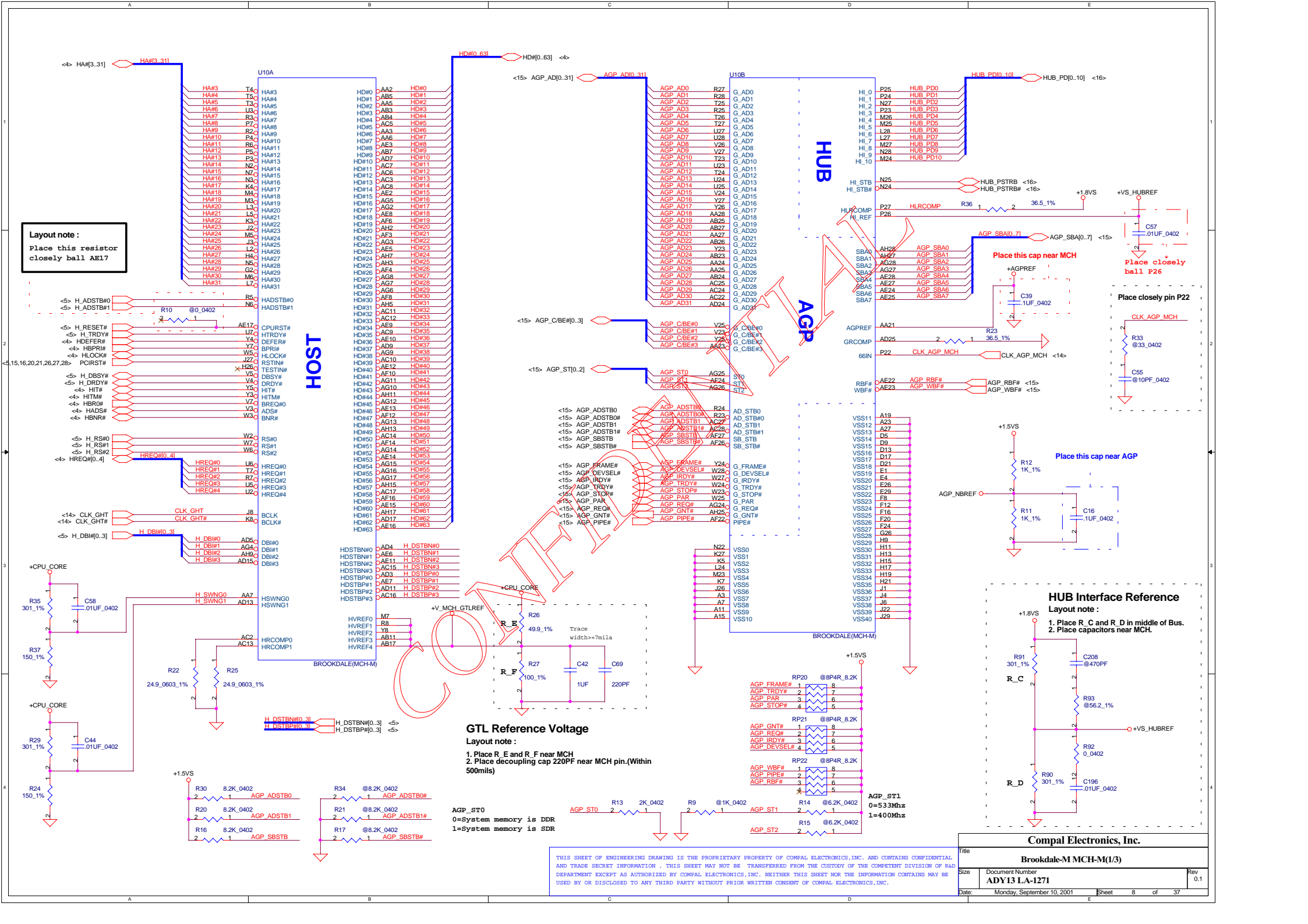
Fan1 Control circuit

Fan2 Control circuit



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COMPAL Electronics, Inc		
Title	LM75 Thermal sensor & Fan control	
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date:	Monday, September 10, 2001	Sheet 7 of 37



Layout note :
Place this resistor closely ball AE17

Place this cap near MCH

Place closely pin P22

Place this cap near AGP

HUB Interface Reference
Layout note :
1. Place R_C and R_D in middle of Bus.
2. Place capacitors near MCH.

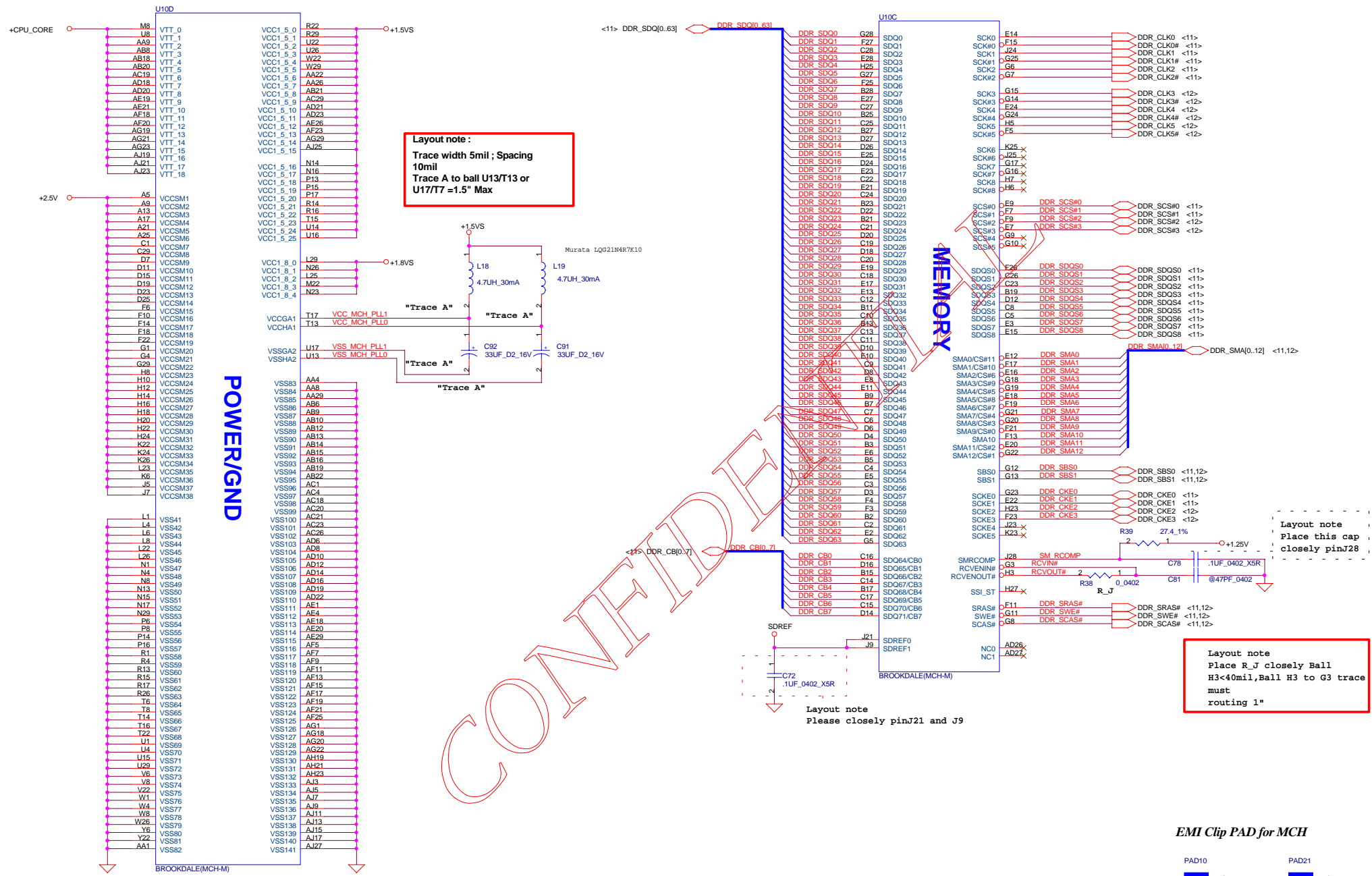
GTL Reference Voltage
Layout note :
1. Place R_E and R_F near MCH
2. Place decoupling cap 220PF near MCH pin.(Within 500mils)

AGP_ST0
0=System memory is DDR
1=System memory is SDR

AGP_ST1
0=533Mhz
1=400Mhz

Compal Electronics, Inc.		
Brookdale-M MCH-M(U3)		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 8 of 37

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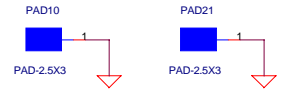
Layout note :
 Trace width 5mil ; Spacing 10mil
 Trace A to ball U13/T13 or U17/T7 =1.5" Max

Layout note
 Place this cap closely pinJ28

Layout note
 Place R_J closely Ball H3<40mil,Ball H3 to G3 trace must routing 1"

Layout note
 Please closely pinJ21 and J9

EMI Clip PAD for MCH

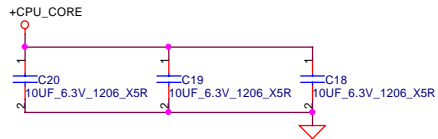
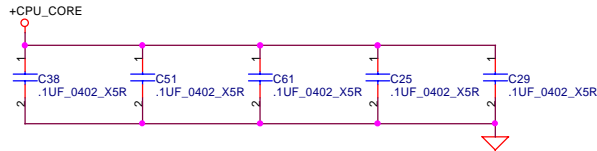
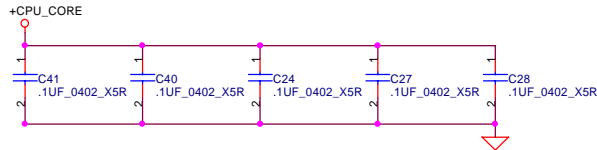


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Compal Electronics, Inc.		
Title Brookdale-M MCH-M(2/3)		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 9 of 37

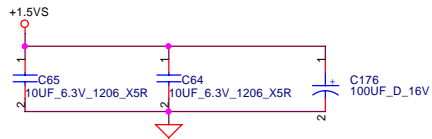
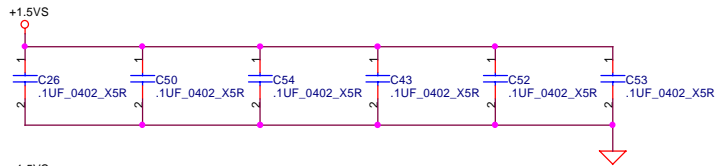
Layout note : Processor system bus

Distribute as close as possible to MCH Processor Quadrant.(between VTTFSB and VSS pin)



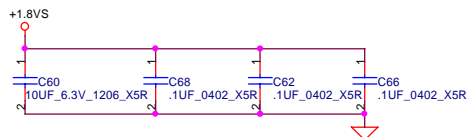
Layout note : AGP / CORE

Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)



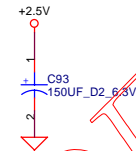
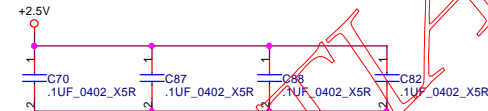
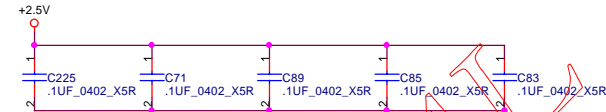
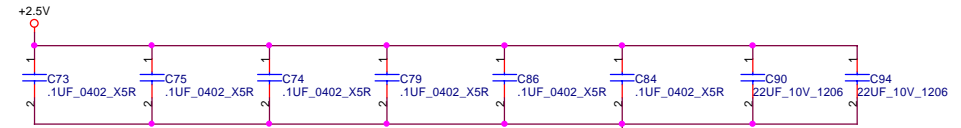
Layout note : Hub-Link

Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)



Layout note : DDR Memory interface

Distribute as close as possible to MCH Processor Quadrant.(between VCCSM and VSS pin)



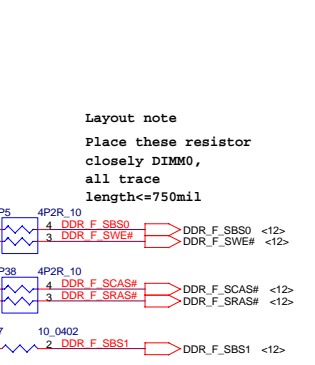
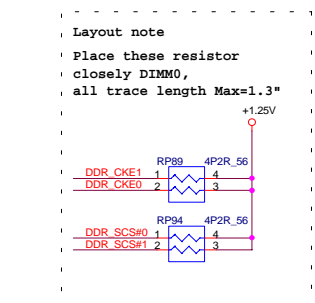
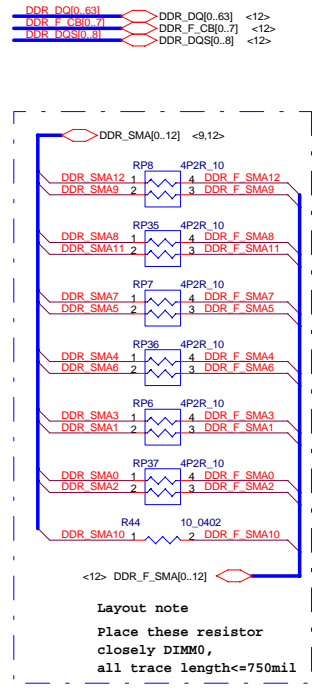
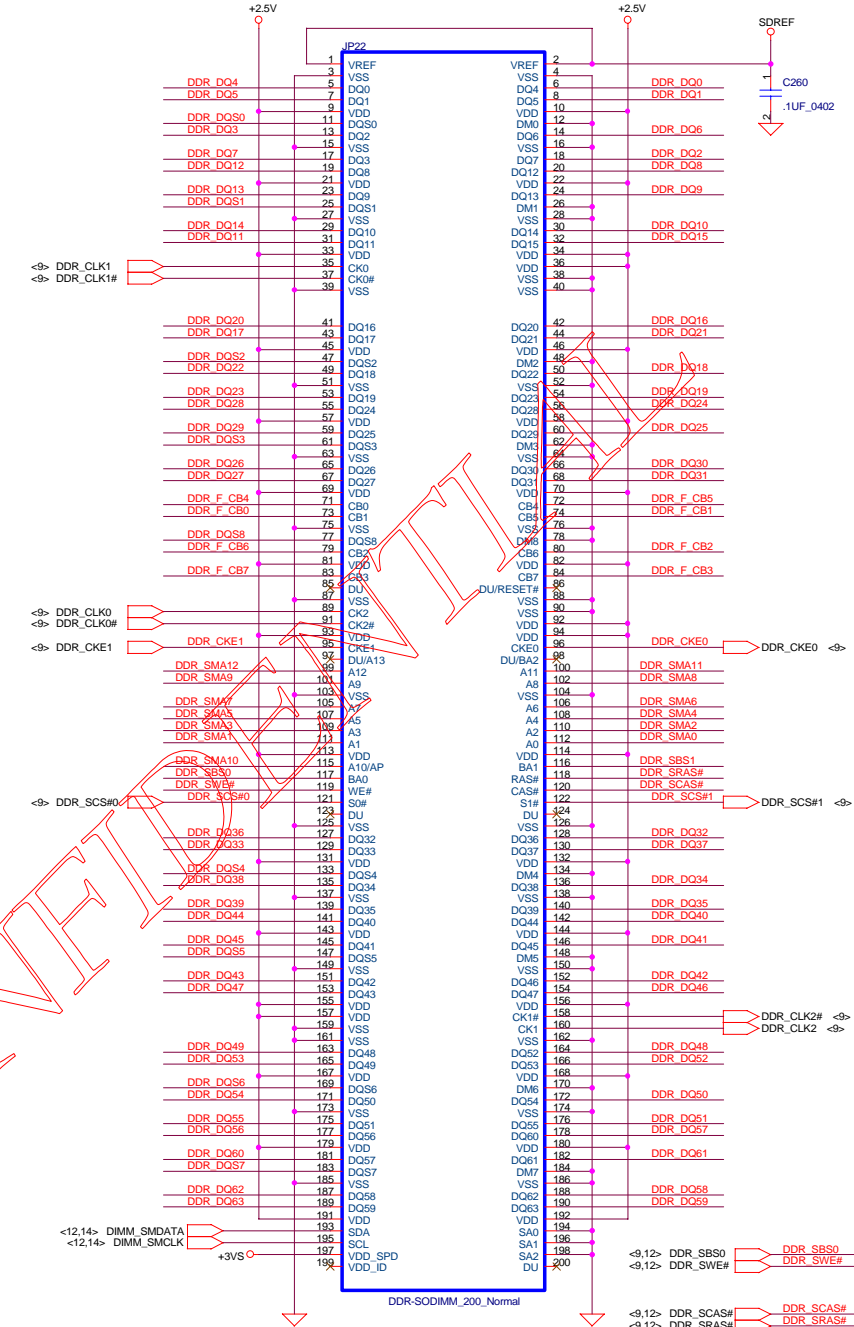
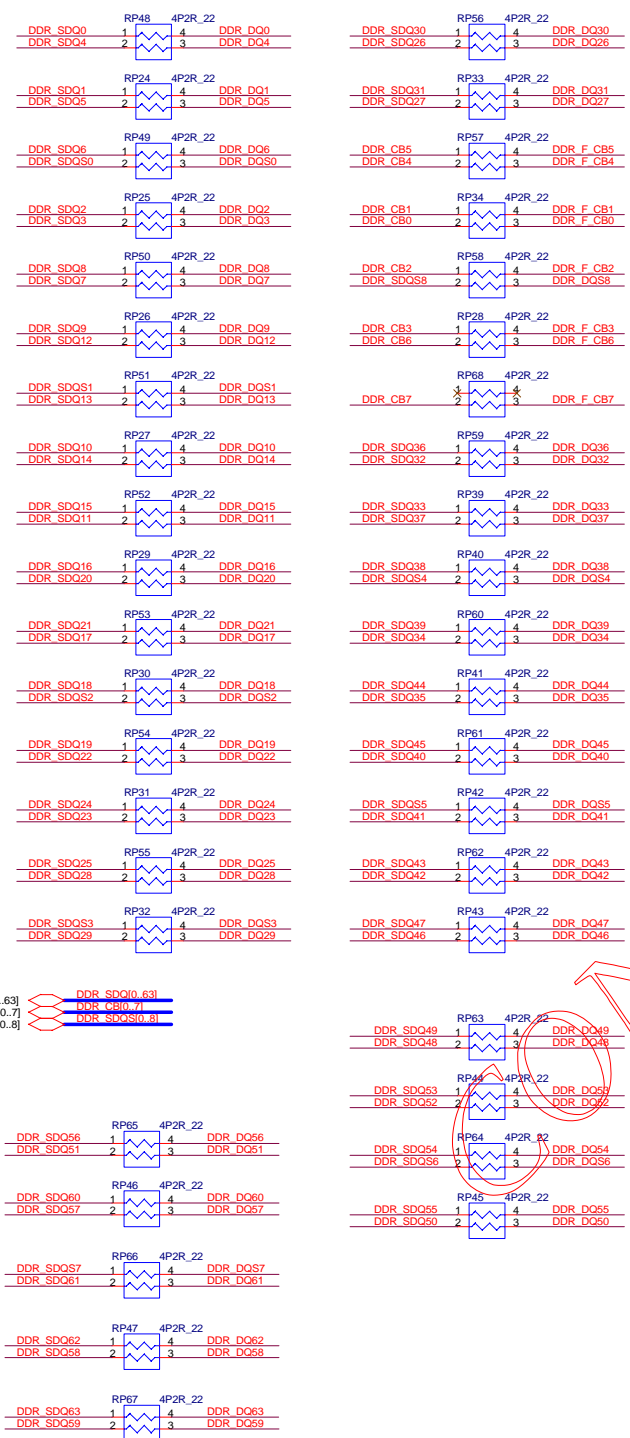
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Title		MCH-M Decoupling	
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
Date:	Wednesday, September 19, 2001	Sheet	10 of 37

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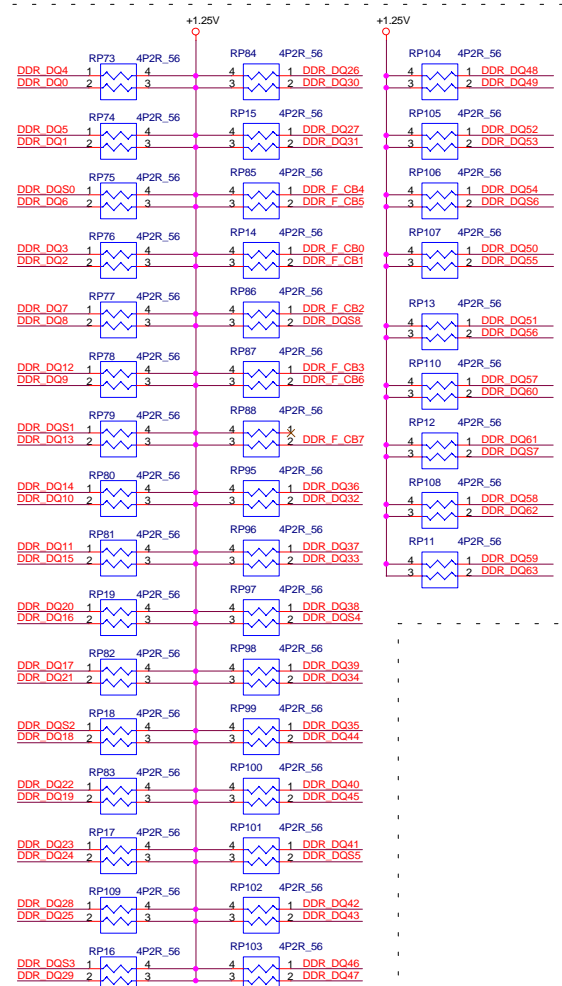
Layout note
Place these resistor closely DIMMO, all trace length<750mil



DIMMO
Bottom side

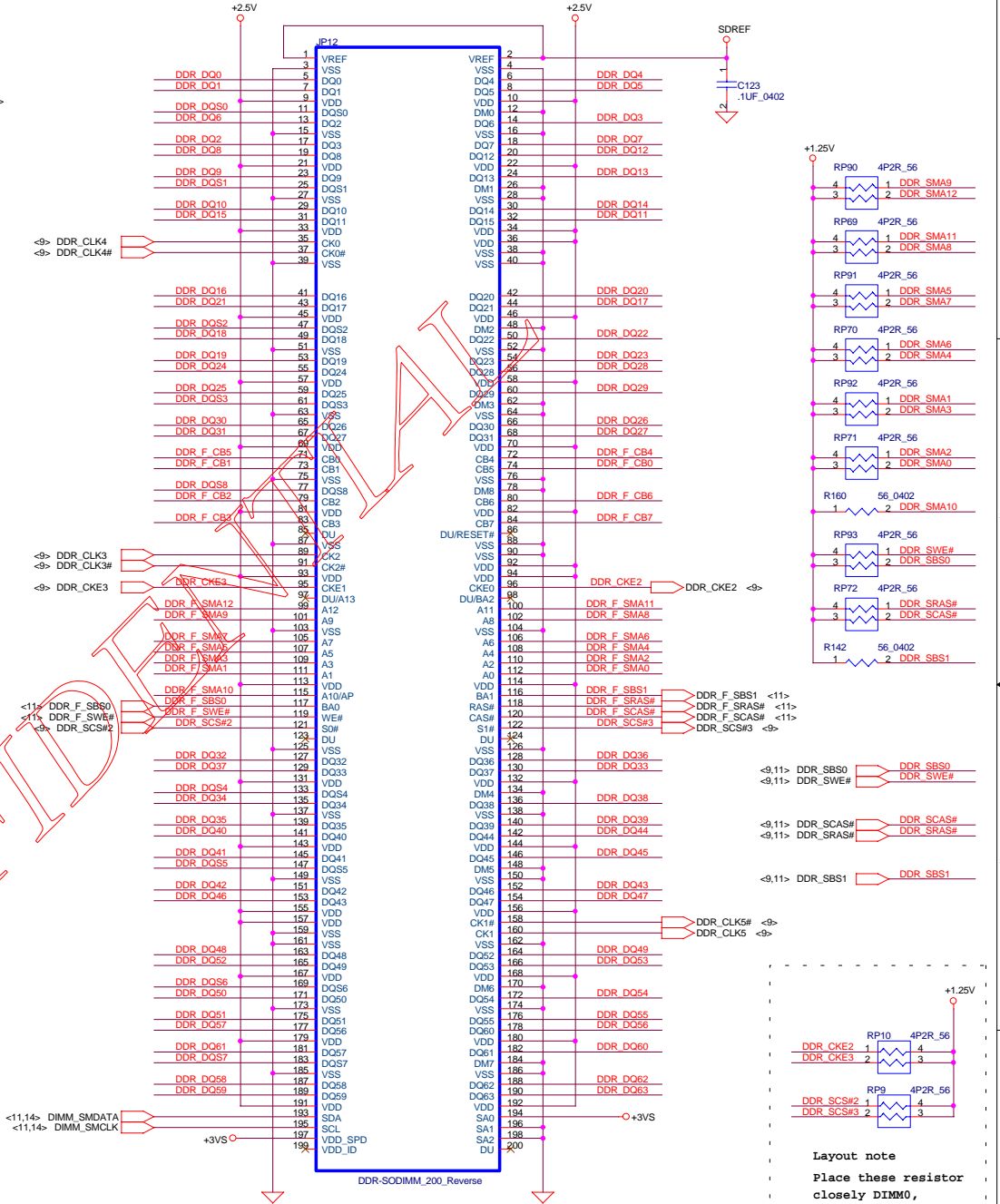
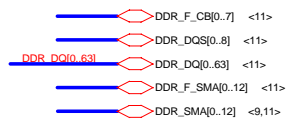
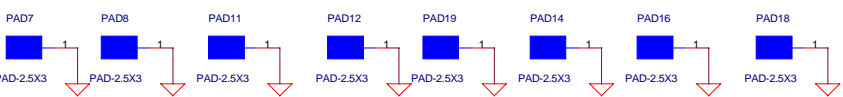
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Compal Electronics, Inc.		
DDR-SODIMMSLOT1		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 11 of 37



Layout note
Place these resistor closely DIMM1, all trace length<=800mil

EMI Clip PAD for Memory Door



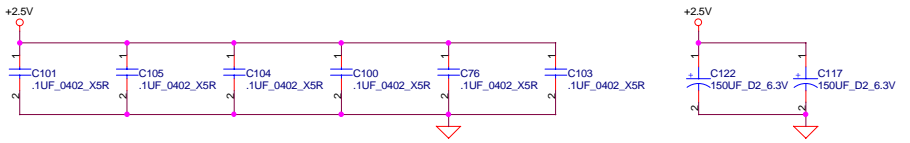
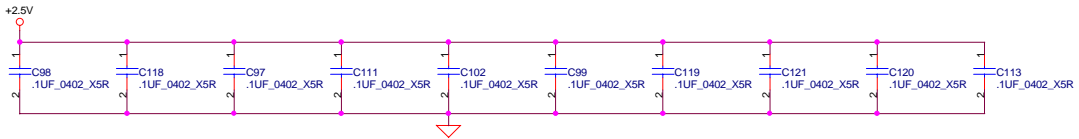
DIMM1
Top side

Layout note
Place these resistor closely DIMM0, all trace length Max=1.3"

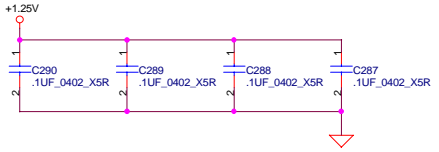
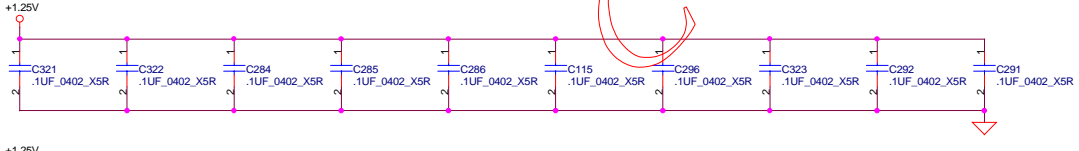
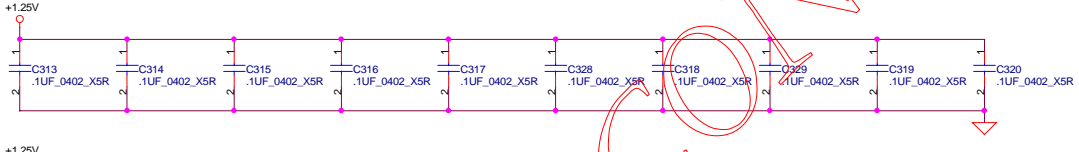
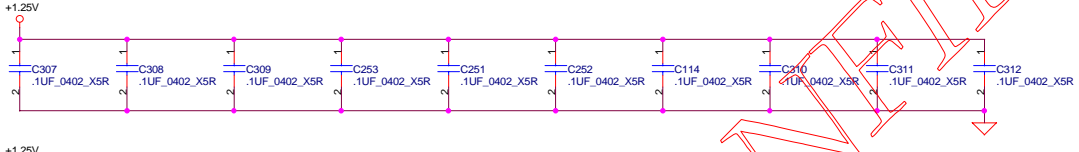
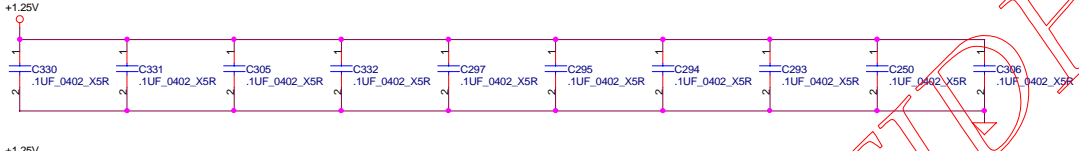
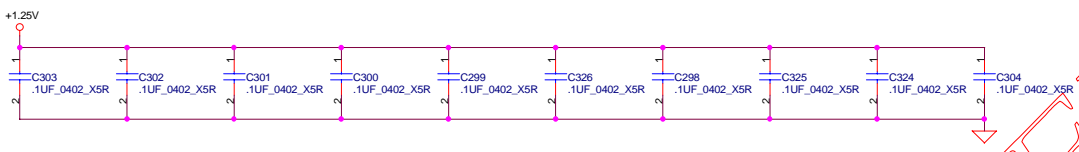
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Compal Electronics, Inc.		
DDR-SODIMM SLOT1		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 12 of 37

Layout note :
Distribute as close as possible to DDR-SODIMM.



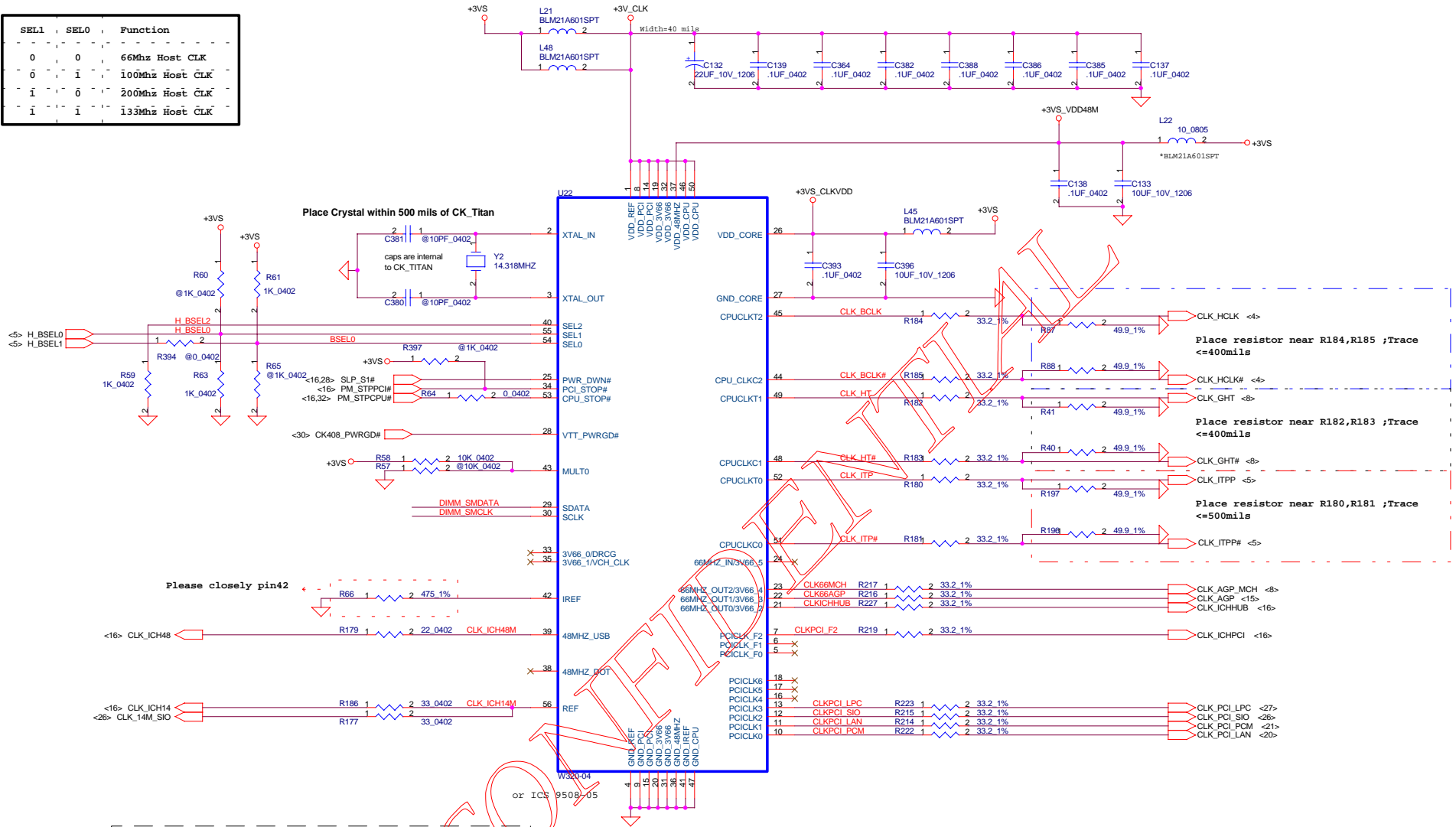
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



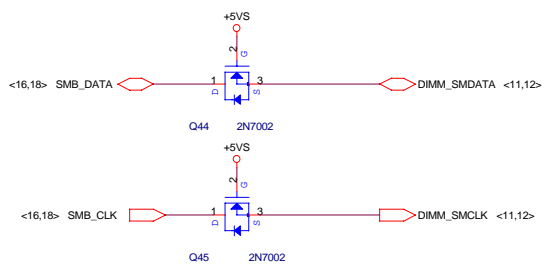
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Compal Electronics, Inc.		
DDR SODIMM Decoupling		
Title	Document Number ADY13 LA-1271	
Size	Rev 0.1	
Date:	Wednesday, September 19, 2001	Sheet 13 of 37

SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



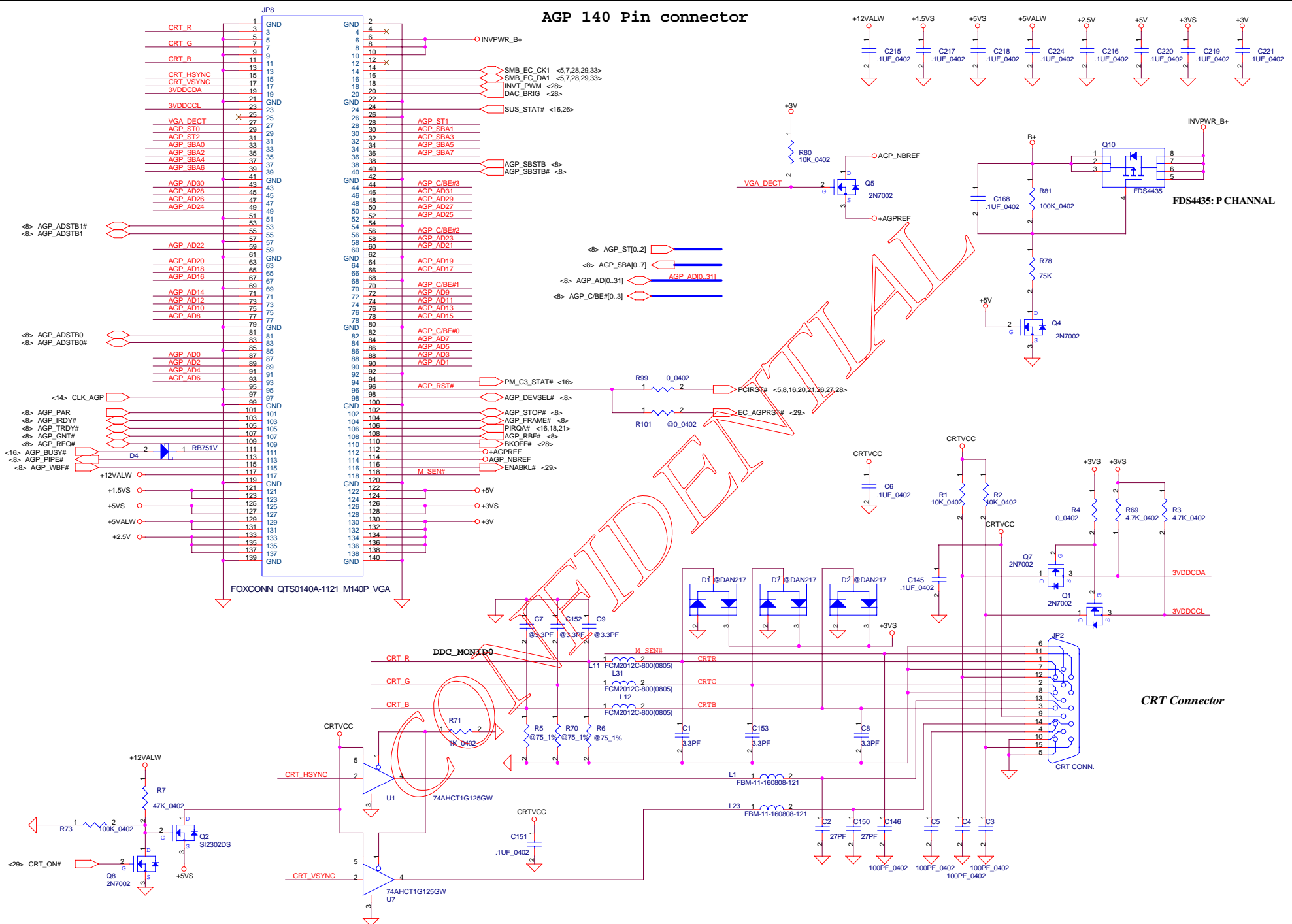
Note:
CPU_CLK[2:0] needs to be running in C3, C4.



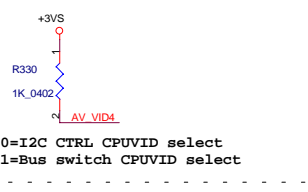
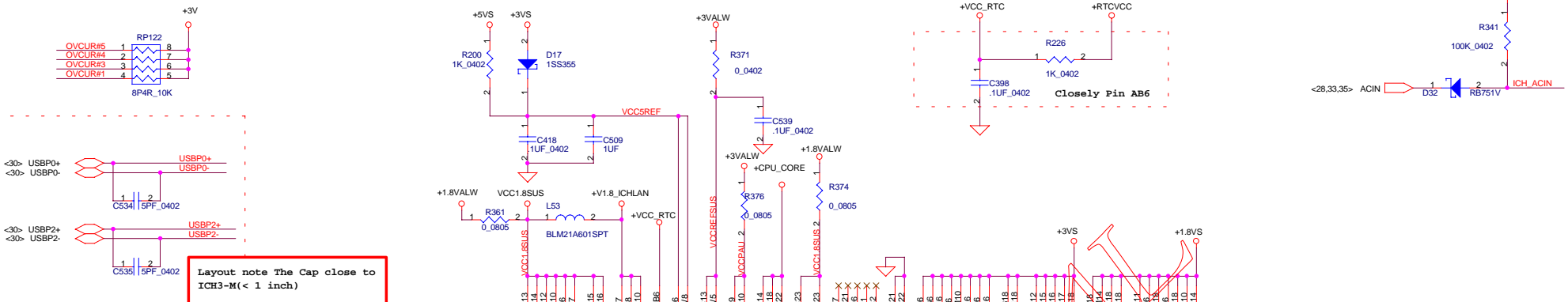
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Compal Electronics, Inc.		
Clock Generator		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date:	Monday, September 10, 2001	Sheet 14 of 37

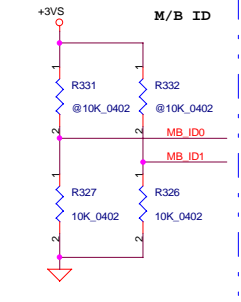
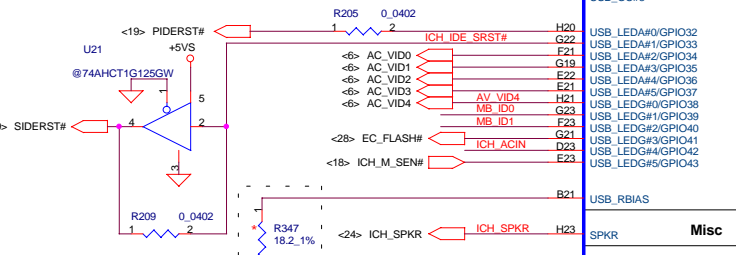
AGP 140 Pin connector



Compal Electronics, Inc.

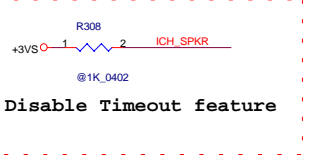


0=I2C CTRL CPUVID select
1=Bus switch CPUVID select

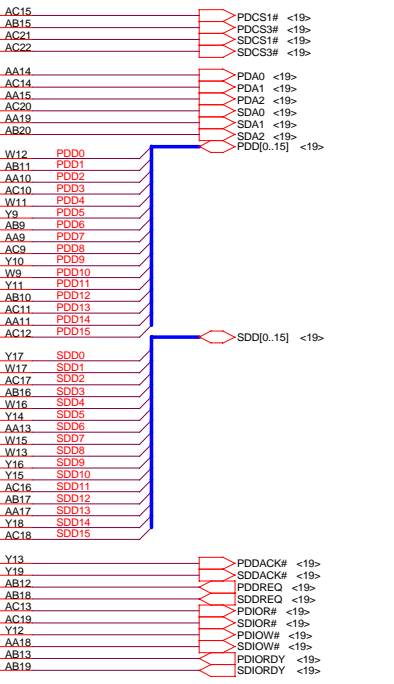
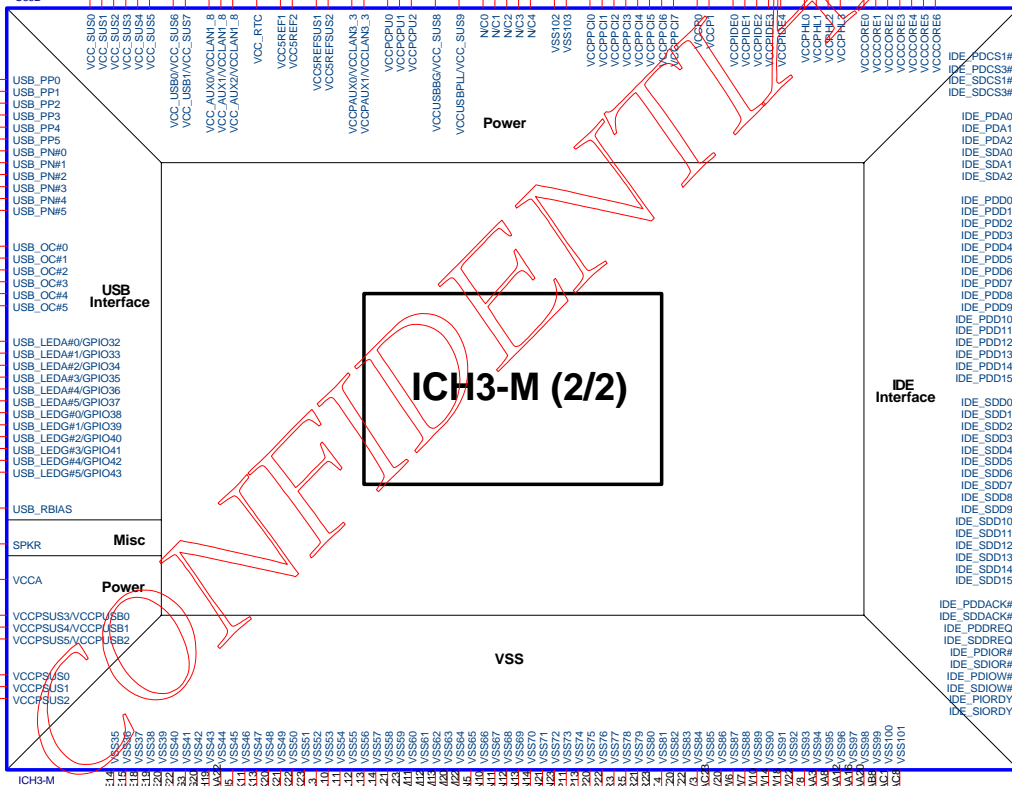


MB_ID0	MB_ID1
SST	0
PT	0
ST	0
QT	1

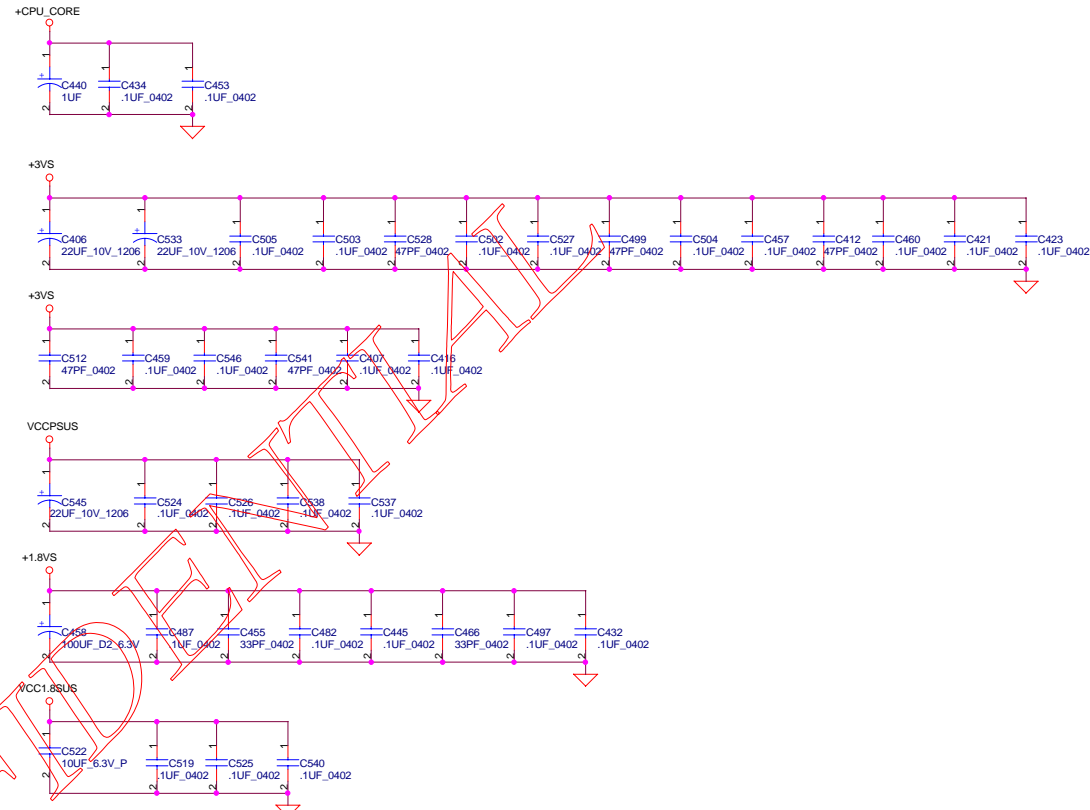
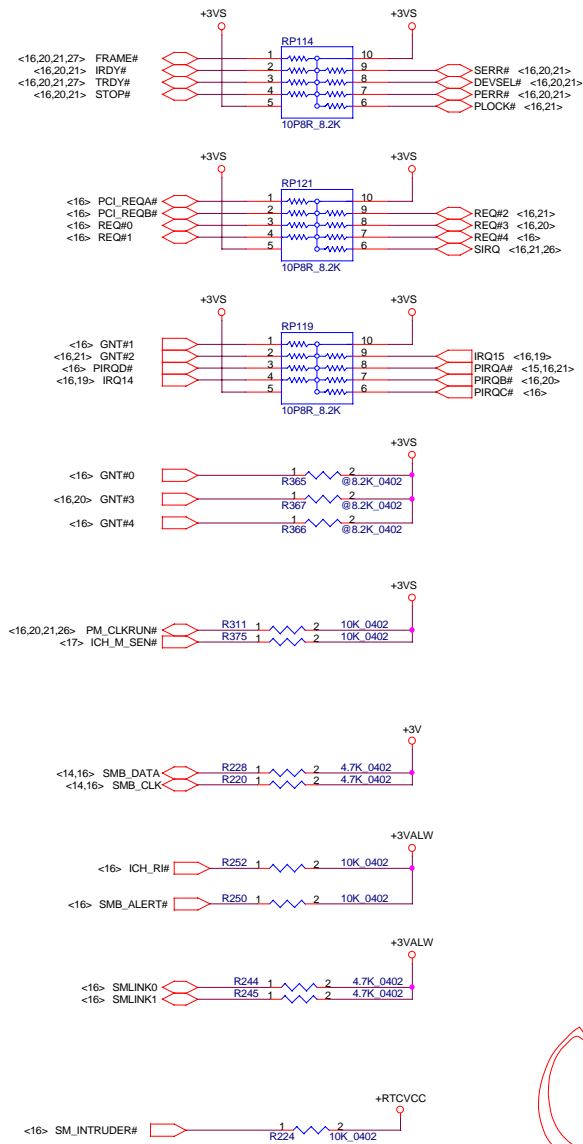
Note:
R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LP part)



Disable Timeout feature



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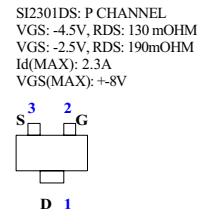
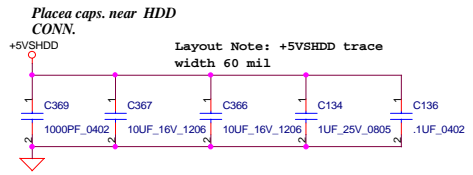
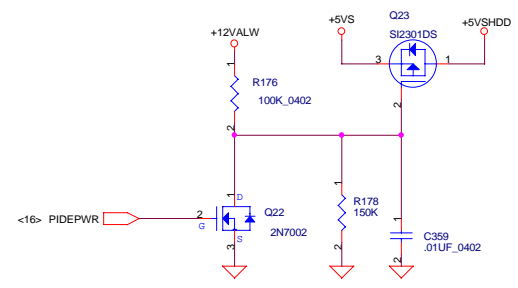
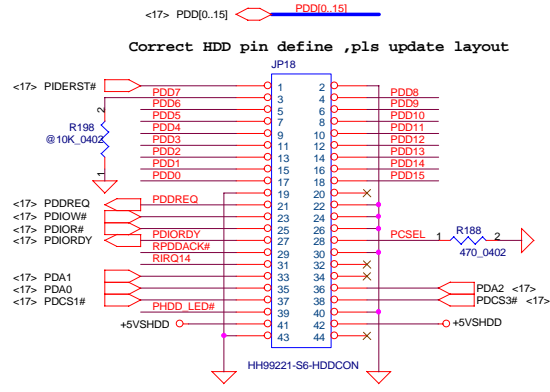


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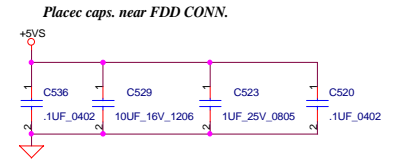
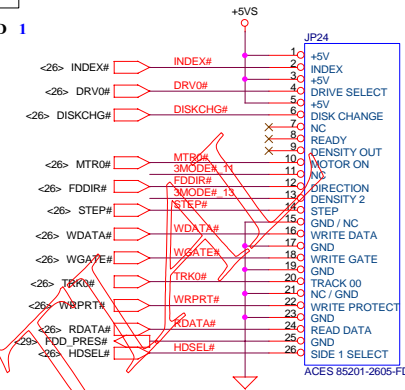
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Compal Electronics, Inc.		
ICH3-M Decoupling & Pull-Up		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 18 of 37

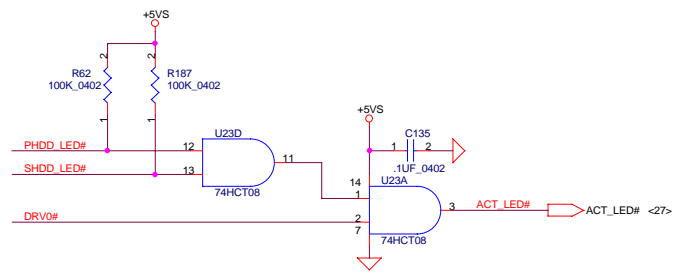
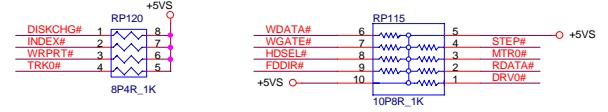
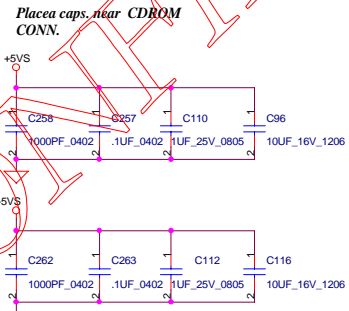
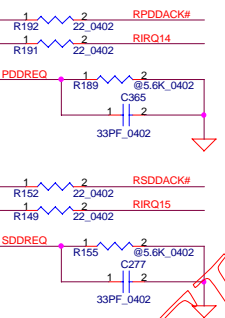
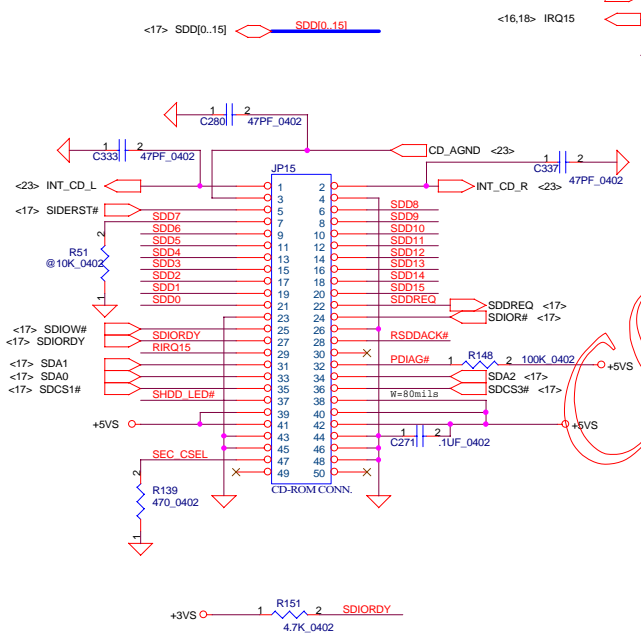
HDD Connector



FDD Connector

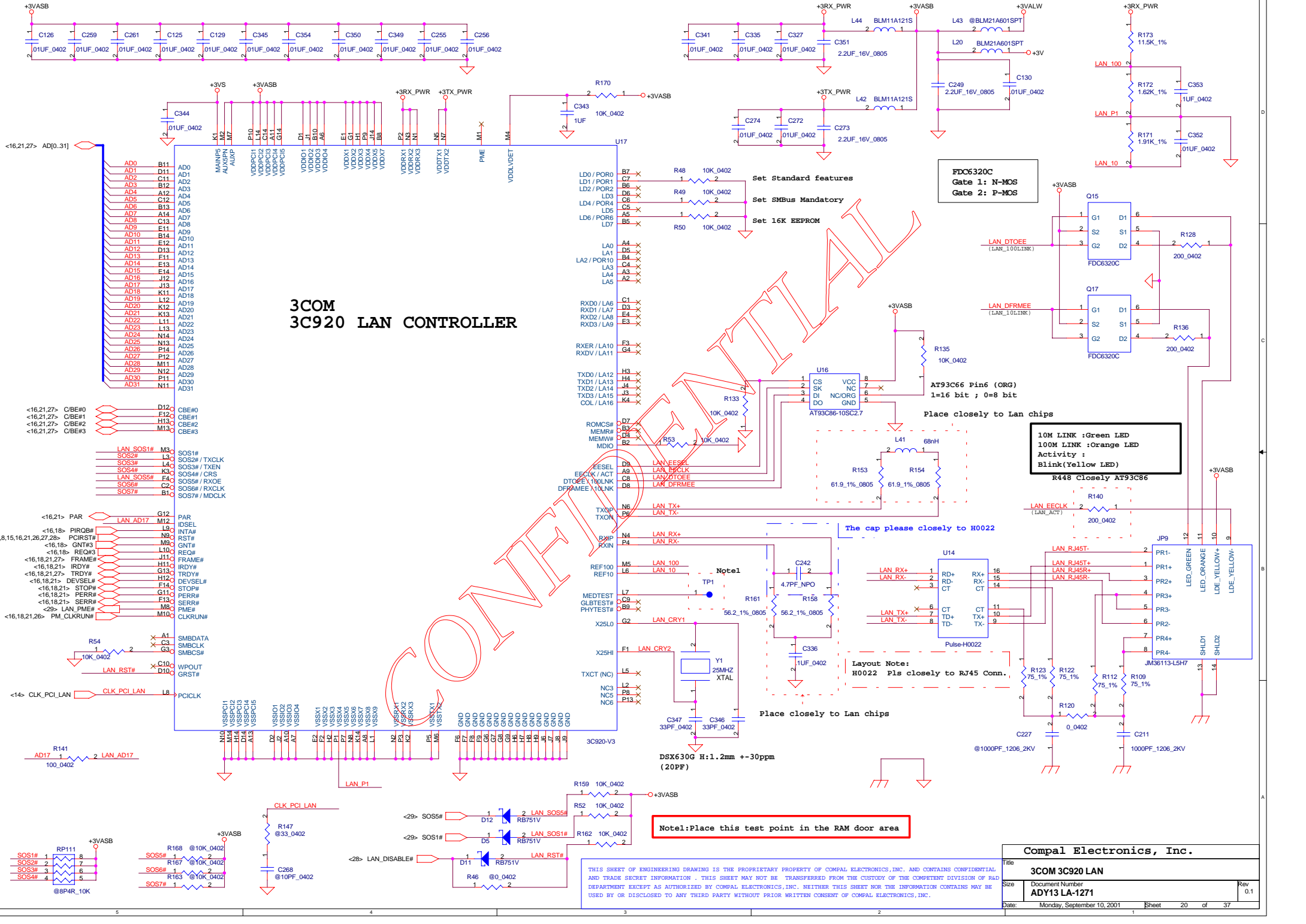


CD-ROM Connector



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Compal Electronics, Inc.		
IDE/FDD/CD-ROM Module		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 19 of 37



**3COM
3C920 LAN CONTROLLER**

FDC6320C
Gate 1: N-MOS
Gate 2: P-MOS

Set Standard features

Set SMBus Mandatory

Set 16K EEPROM

AT93C66 Pin6 (ORG)
1=16 bit ; 0=8 bit

Place closely to Lan chips

10M LINK :Green LED
100M LINK :Orange LED
Blink (Yellow LED)
R448 Closely AT93C86

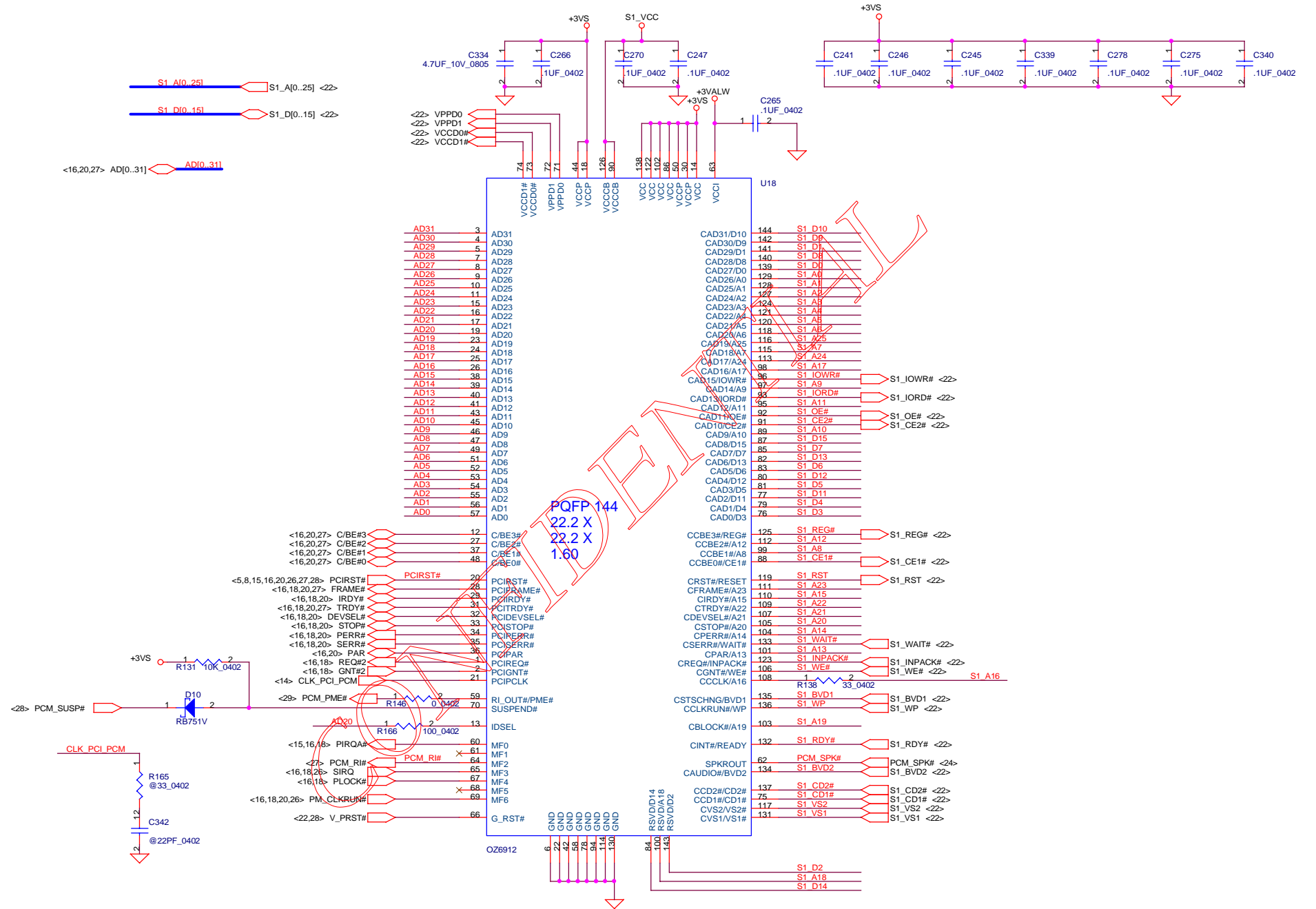
The cap please closely to H0022

Layout Note:
H0022 Pls closely to RJ45 Conn.

Place closely to Lan chips

Notel: Place this test point in the RAM door area

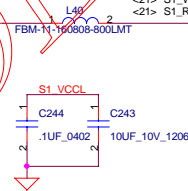
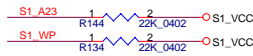
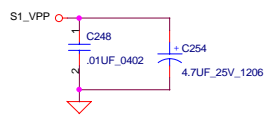
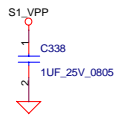
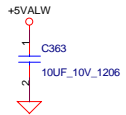
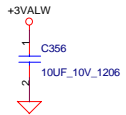
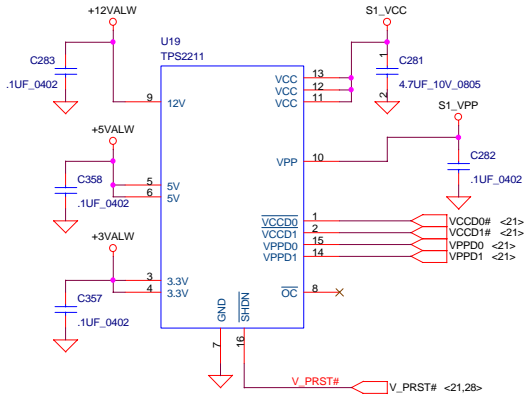
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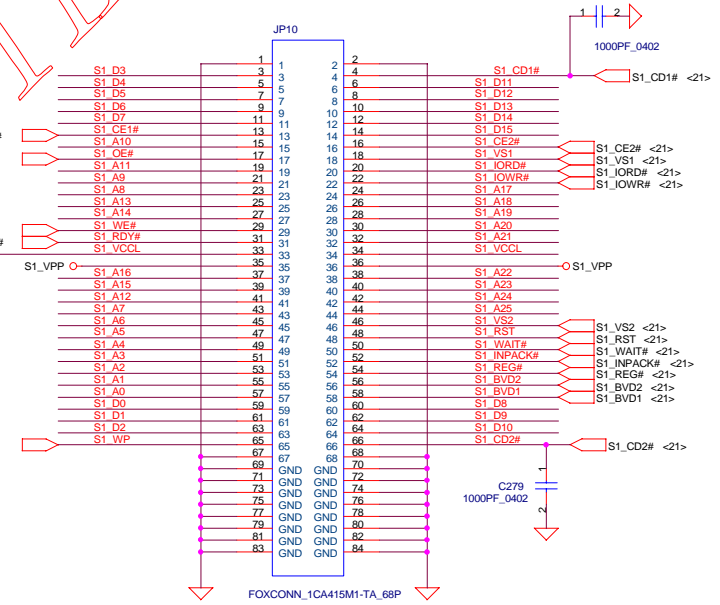
Compal Electronics, Ltd.		
Title PCMCIA controller OZ6912		
Size: Document Number ADY13 LA-1271	Rev 0.1	
Date: Monday, September 10, 2001	Sheet 21	of 37

PCMCIA Power Controller



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CardBus Socket

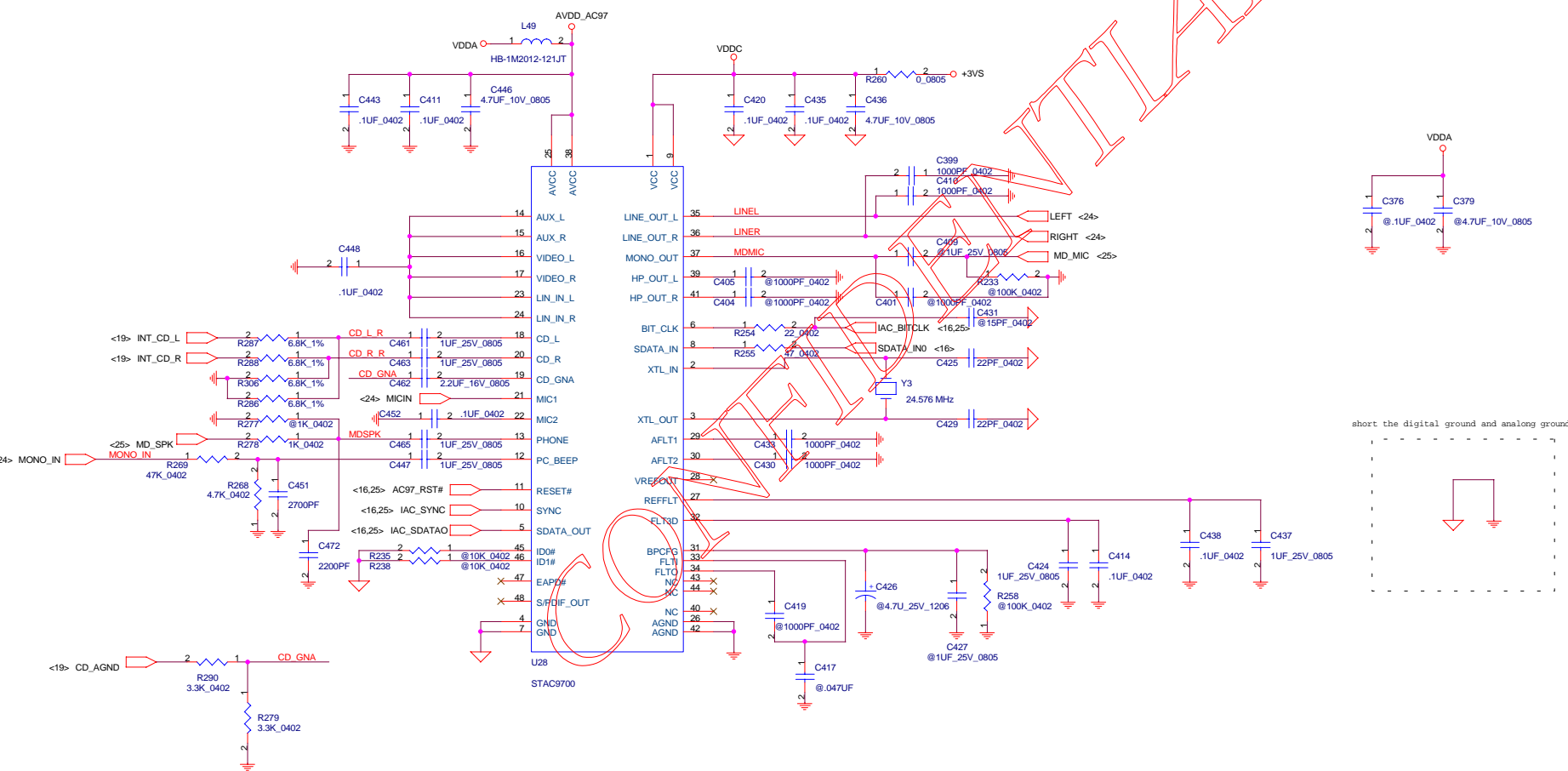
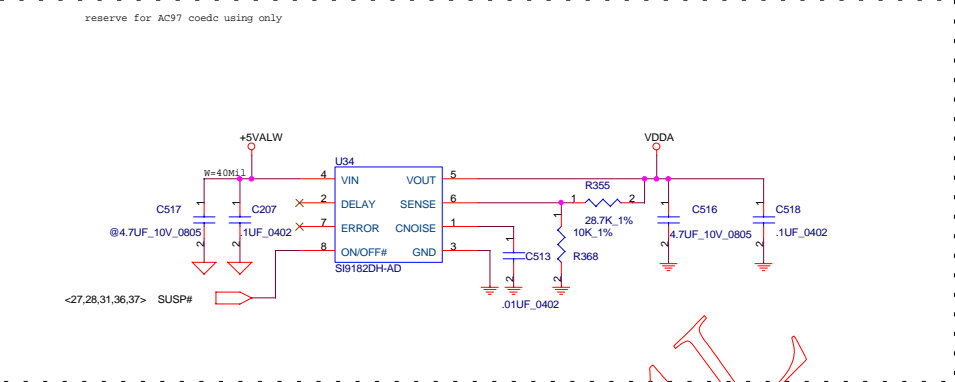
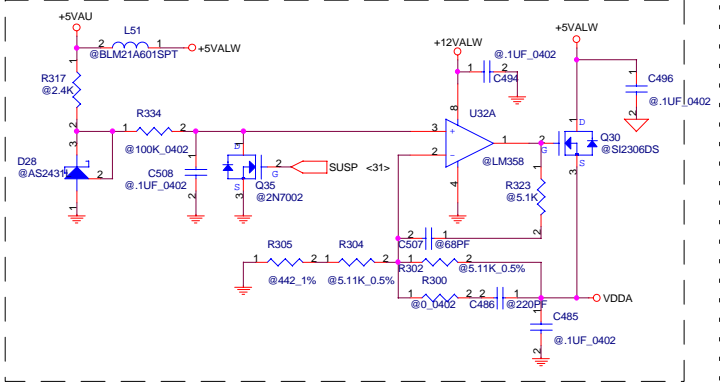


Compal Electronics, Inc.

CardBus Socket

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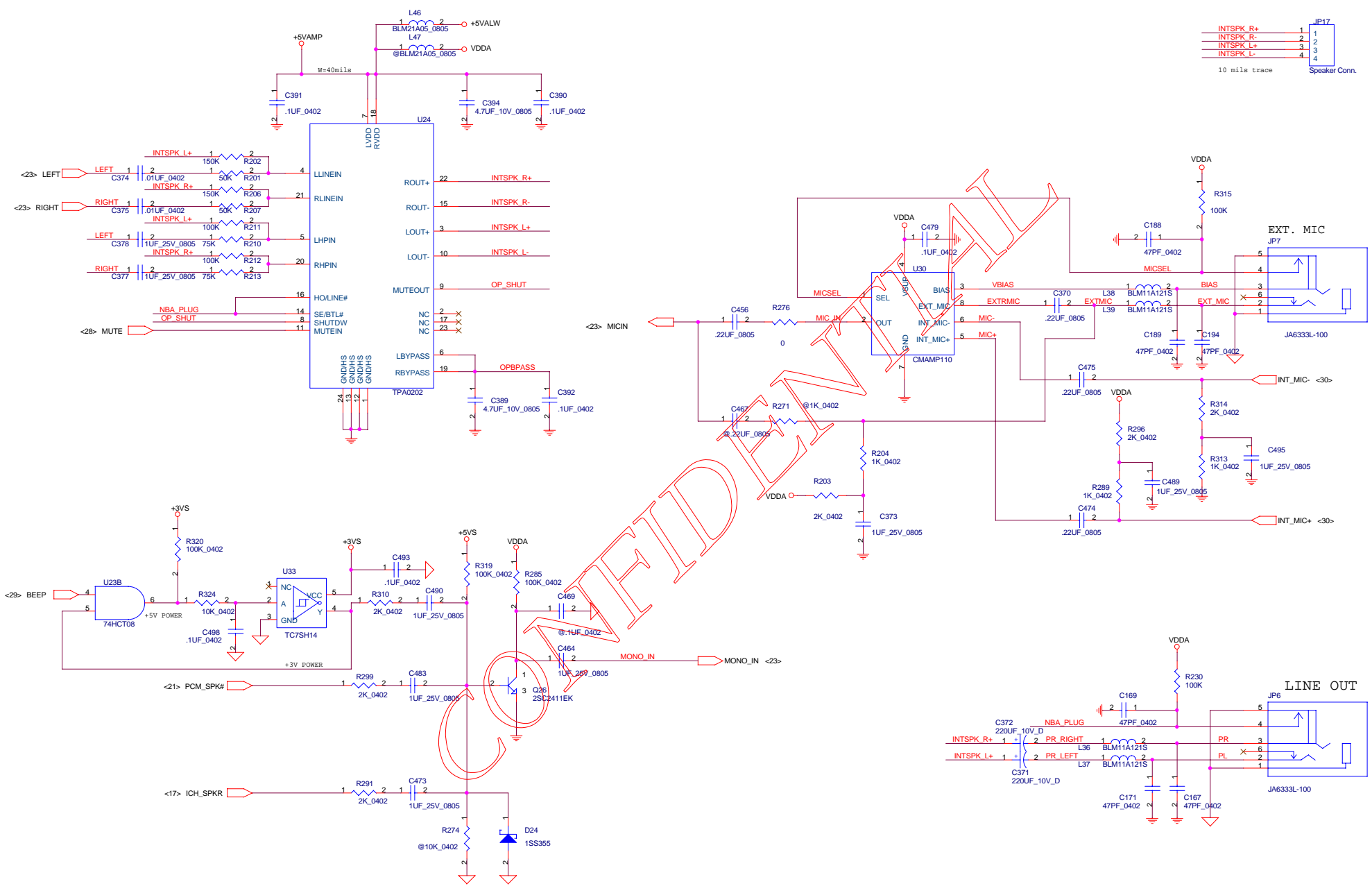
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 22 of 37



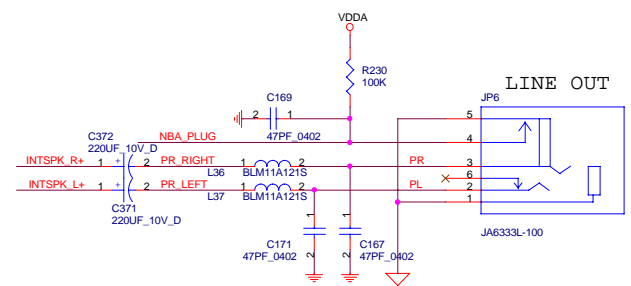
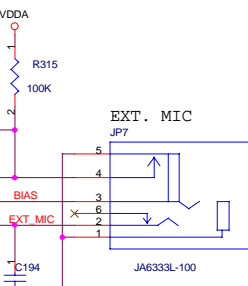
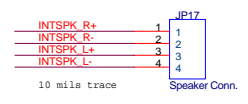
DRAFT

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Compal Electronics, Inc.			
Title		AC97 CODEC	
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
Date:	Monday, September 10, 2001	Sheet	23 of 37

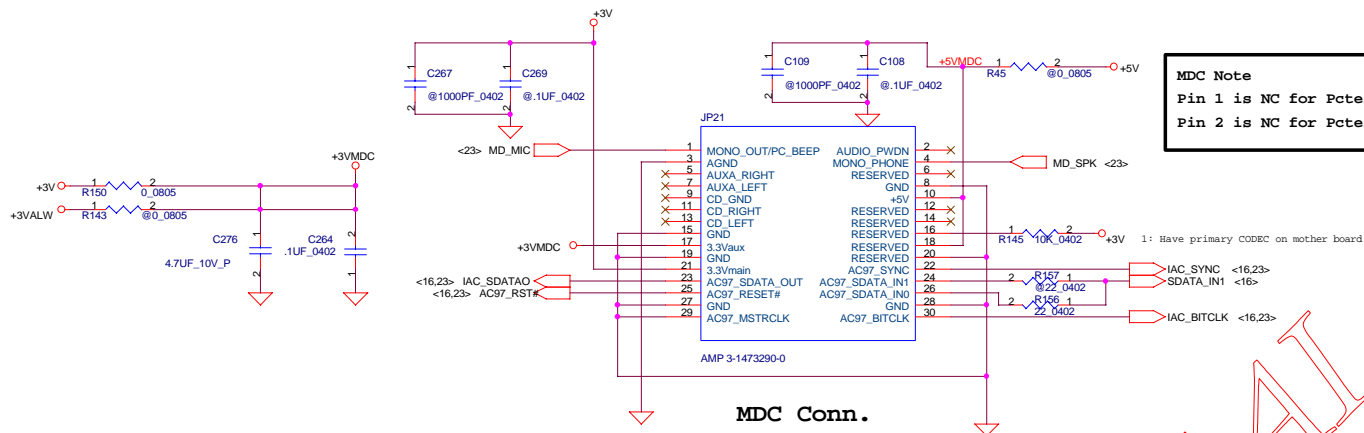


Speaker Connector



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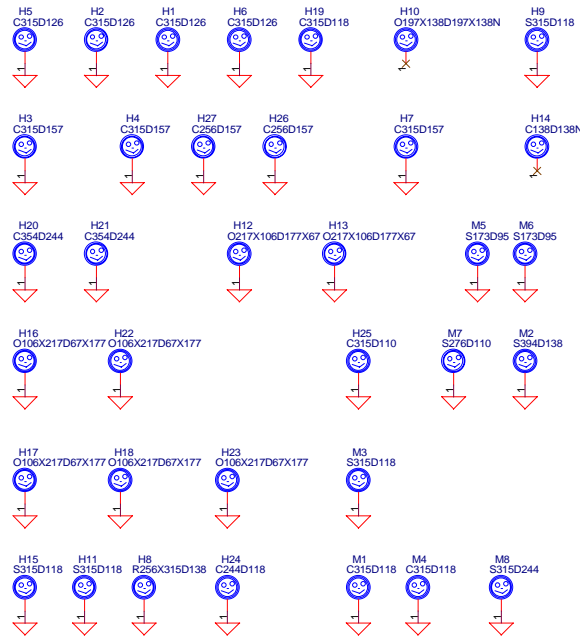
Compal Electronics, Inc.			
AMP & Audio Jack			
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
Date	Monday, September 10, 2001	Sheet	24 of 37



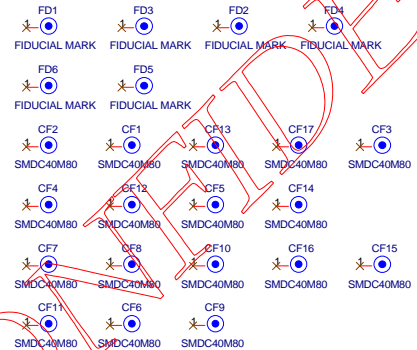
MDC Note
 Pin 1 is NC for Pctel and connexant MDC modem
 Pin 2 is NC for Pctel and connexant MDC modem

MDC Conn.

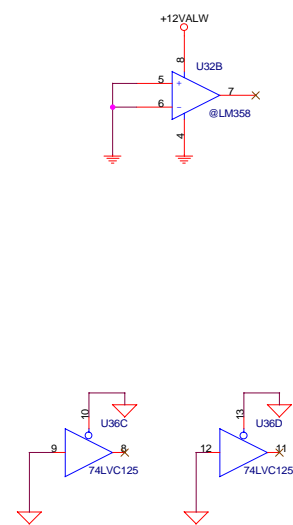
Screw Hole



Fiducial Mark

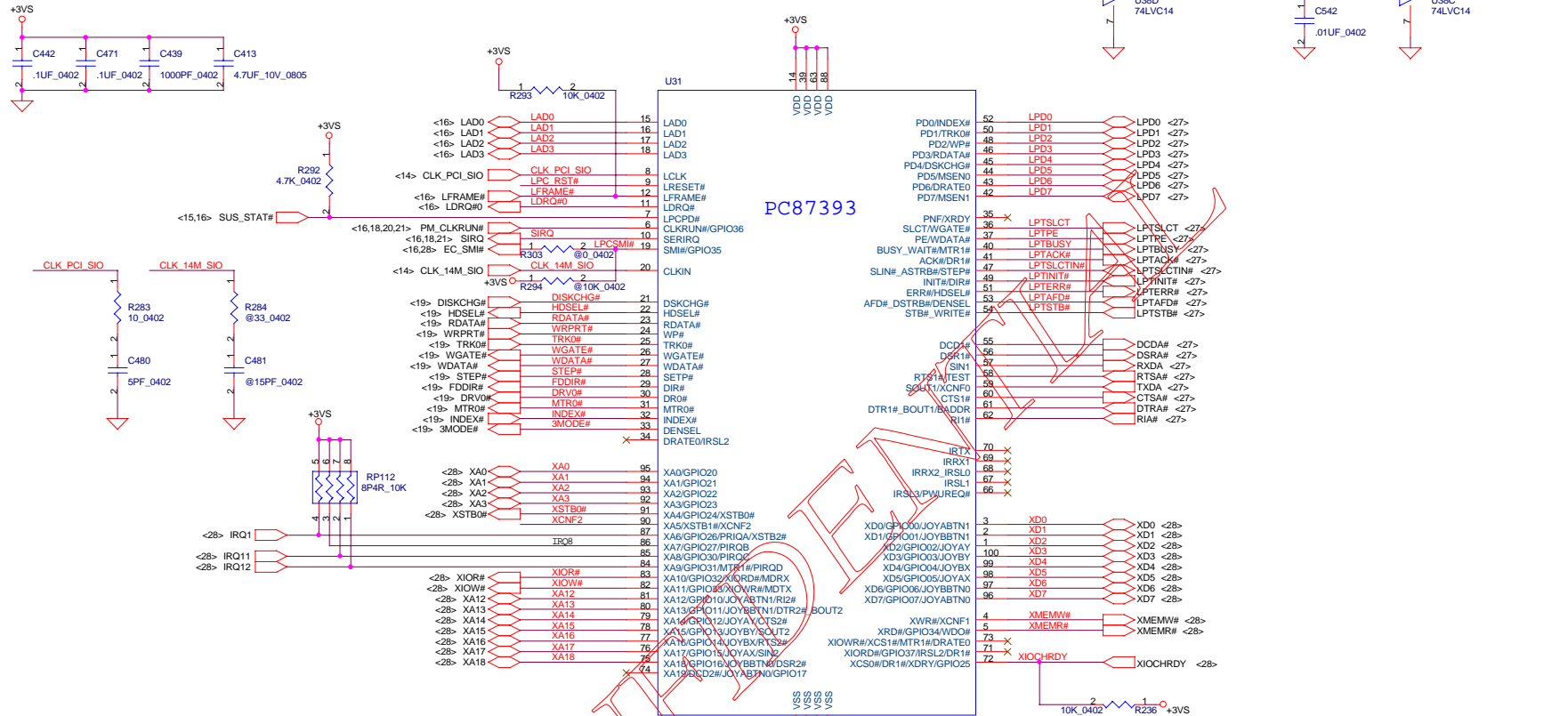


Spare Logic Gate



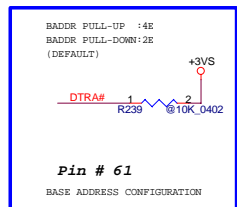
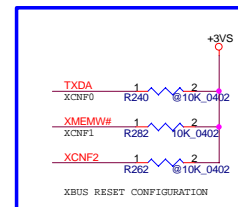
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Compal Electronics, Inc.		
Title		
MDC connector / Skew Hole		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date:	Monday, September 10, 2001	Sheet 25 of 37



Signal	Pin #	Description
BADDR	61	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F
TEST	58	"0": Normal (Default) "1": Test Mode
XCNF[2:0]	90, 4, 59	2 1 0 Function
		x 0 0 No BIOS
		x 0 1 Normal Mode. XRDY disabled
		(default) 0 1 0 Latch Mode. XA12-19, XRDY enabled
		1 1 0 Latch Mode. GPIO10-17, XRDY enabled
		0 1 1 Latch Mode. XA12-19, XRDY disabled
		1 1 1 Latch Mode. GPIO10-17, XRDY disabled

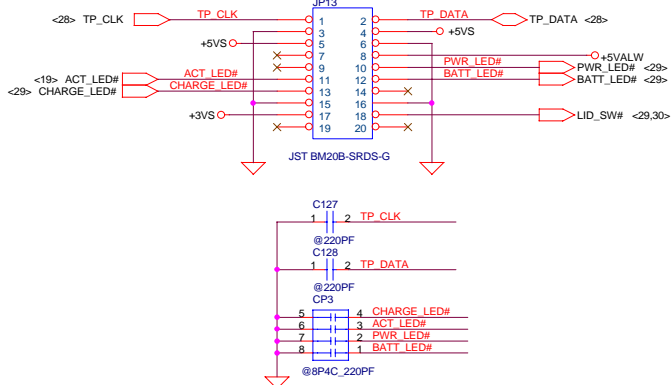
* 1 ROM SOLUTION



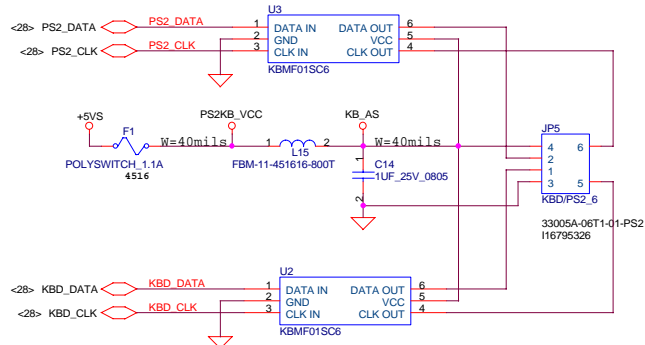
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Compal Electronics, Inc.		
LPC Super I/O NS PC87393		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 26 of 37

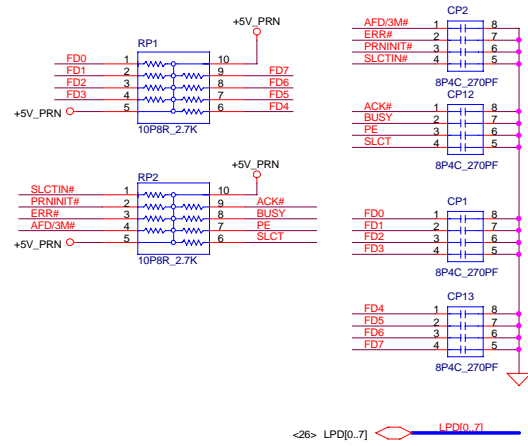
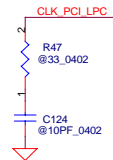
Touch Pad & Status LED Conn.



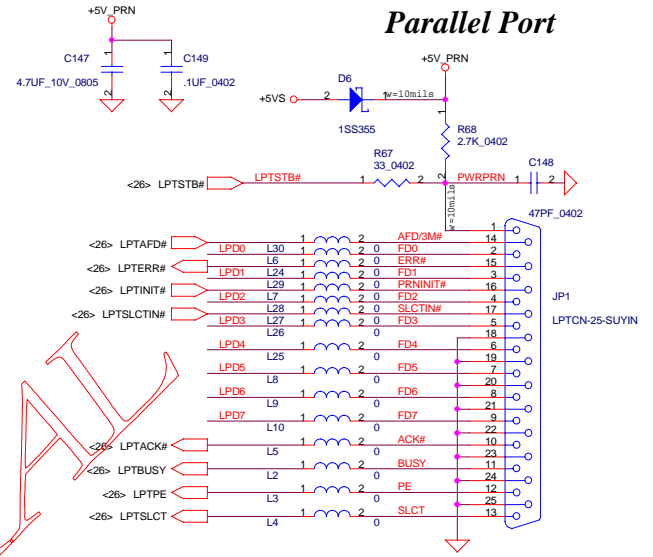
PS2 CONN.



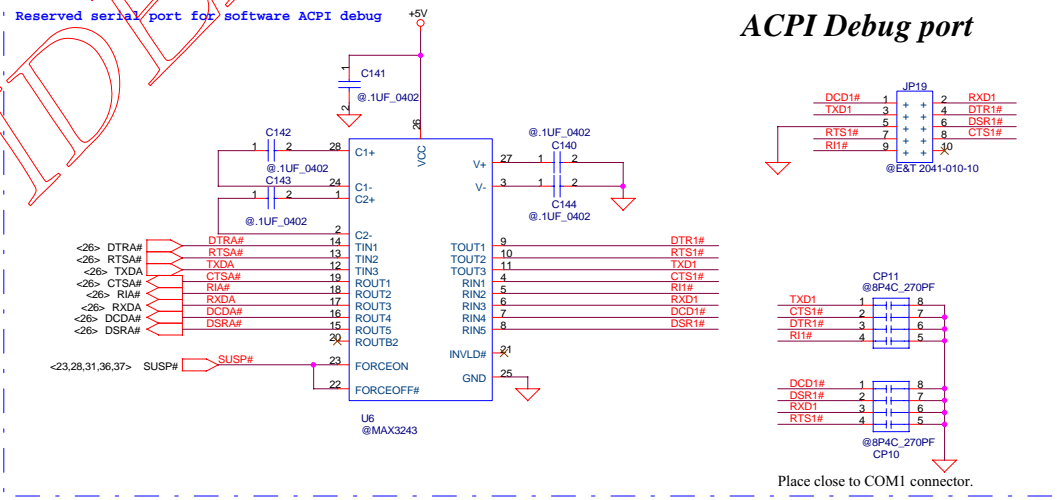
Debug PORT



Parallel Port

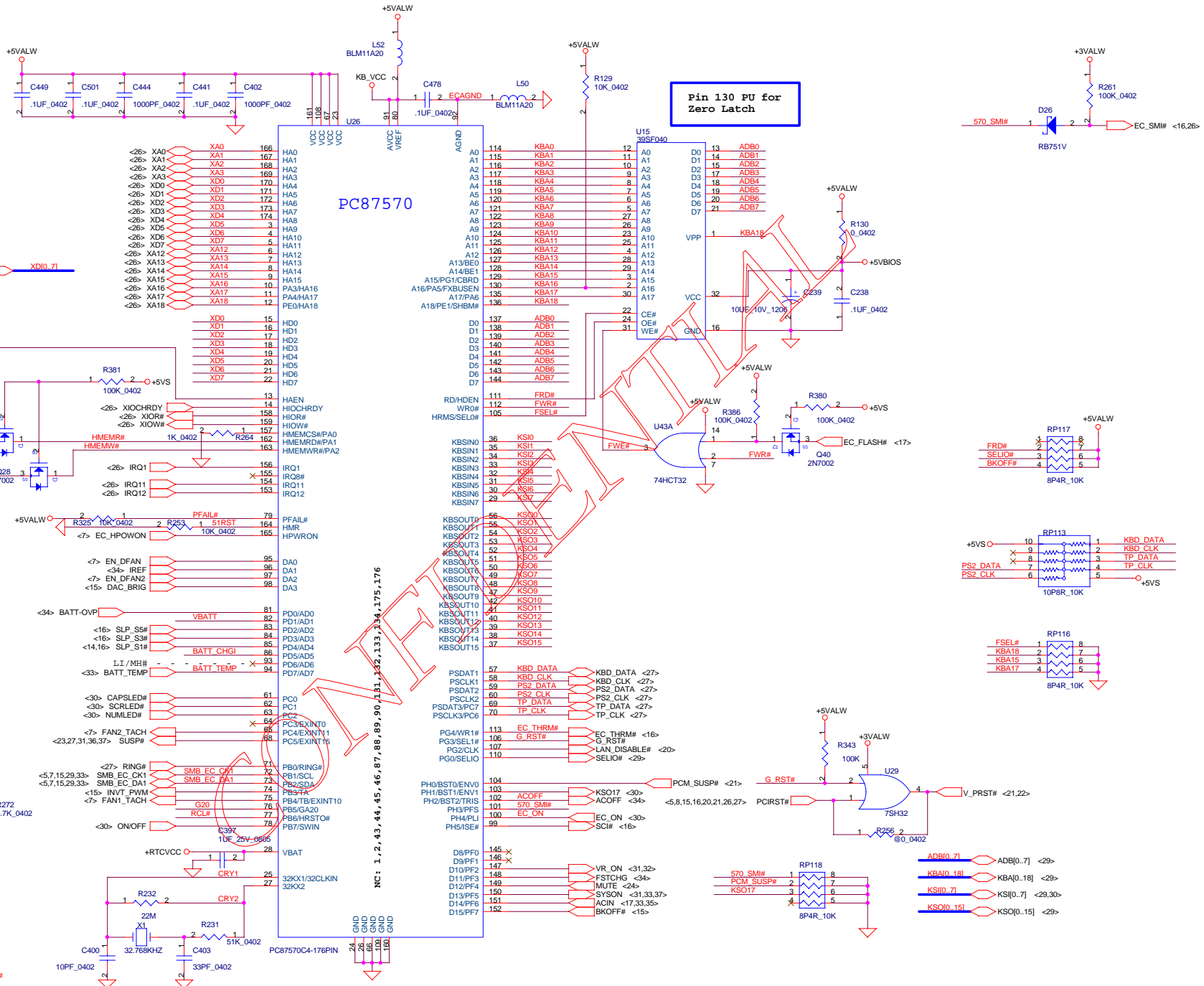


Reserved serial port for software ACPI debug




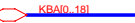
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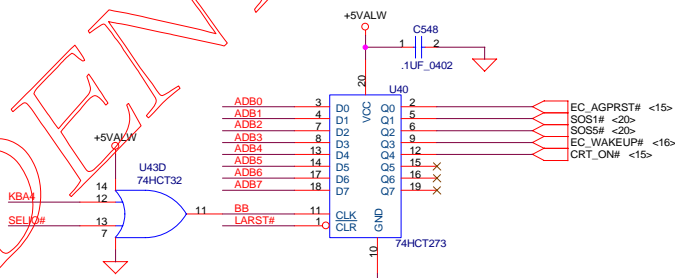
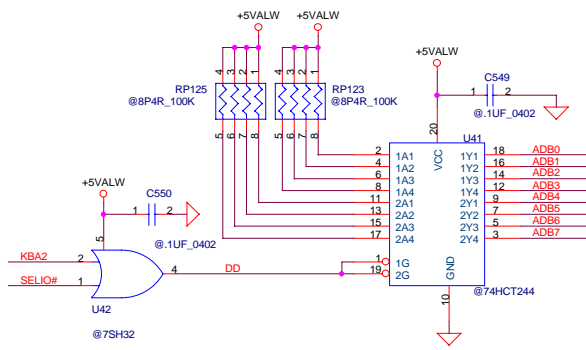
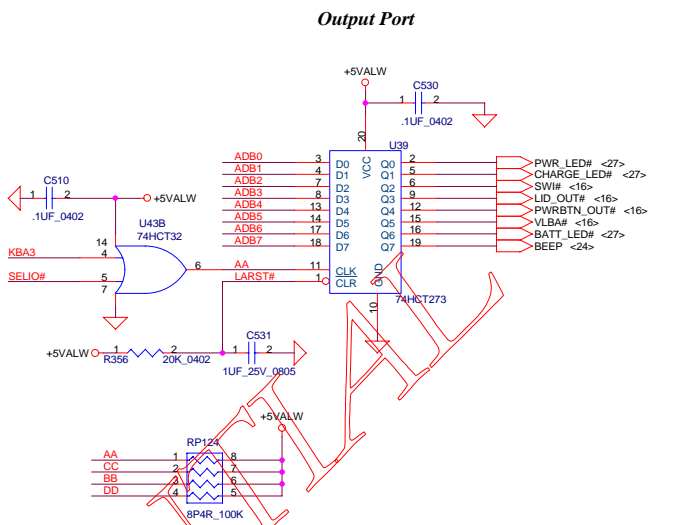
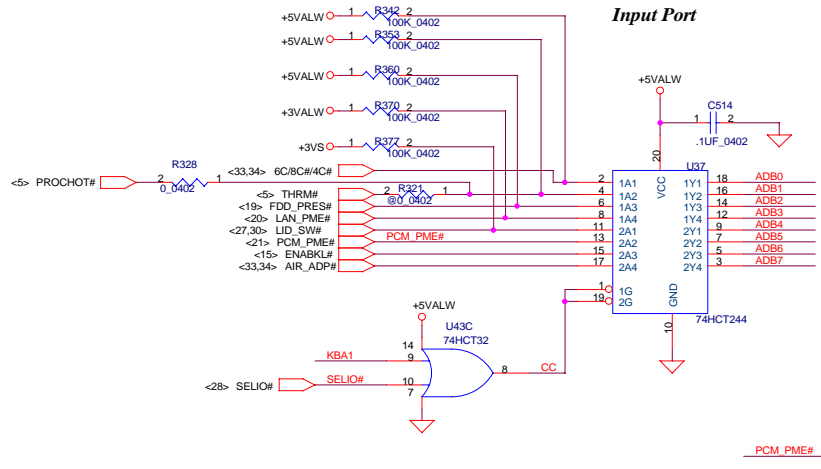
Compal Electronics, Inc.			
Title	PIO/PS2 Port/T_P Conn. & PCI Debug Conn.		
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
Date	Monday, September 10, 2001	Sheet	27 of 37

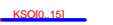



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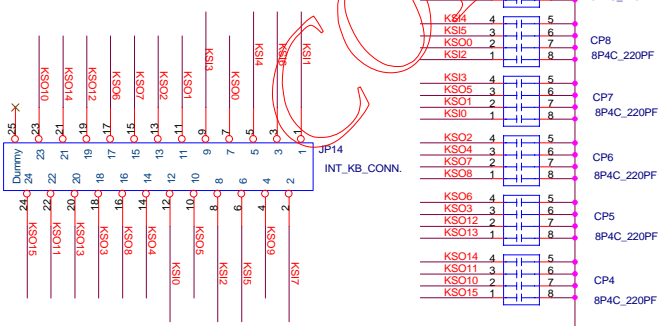
Compal Electronics, Inc.			
File	PC8750		
Size	Document Number	Rev	
	ADY13 LA-1271	0.1	
Date	Monday, September 10, 2001	Sheet	28 of 37

<28> ADB[0..7]  ADB[0..7]
 <28> KBA[0..18]  KBA[0..18]

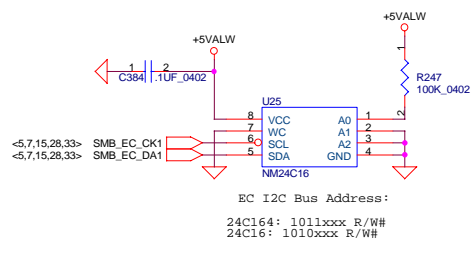


<28> KSO[0..15]  KSO[0..15]
 <28,30> KSI[0..7]  KSI[0..7]

INT_KBD CONN.



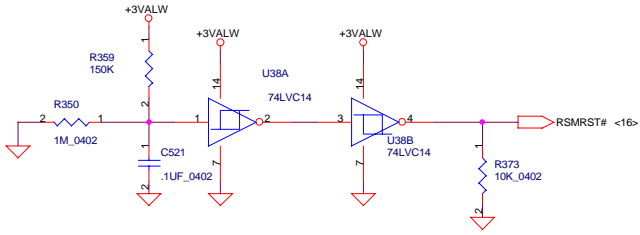
NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



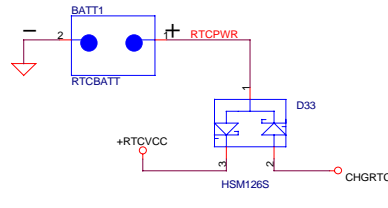
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Compal Electronics, Inc.		
EC Extend I/O KB Conn. & BIOS		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 29 of 37

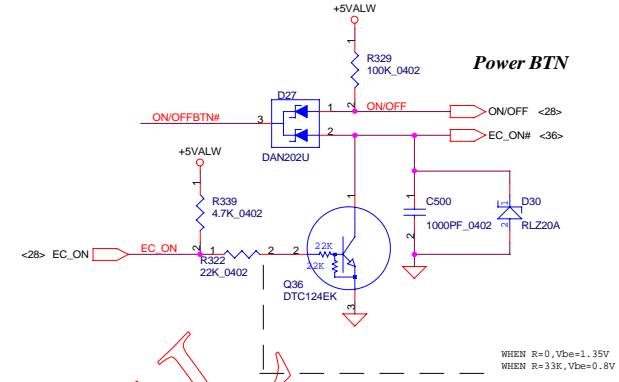
Power ON Circuit



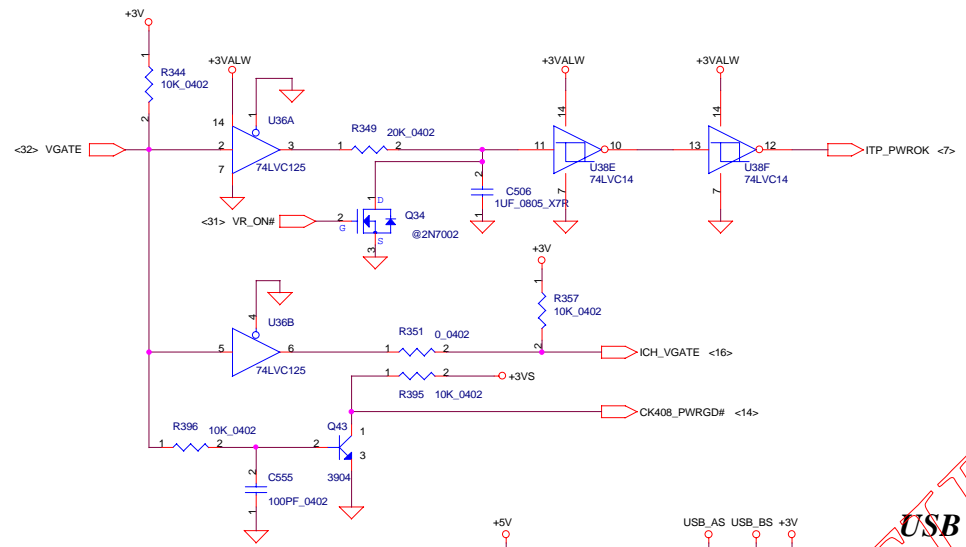
RTC Battery



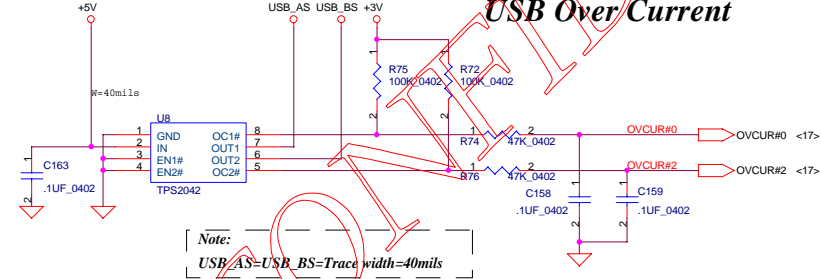
Power BTN



WHEN R=0, Vbe=1.35V
WHEN R=33K, Vbe=0.8V

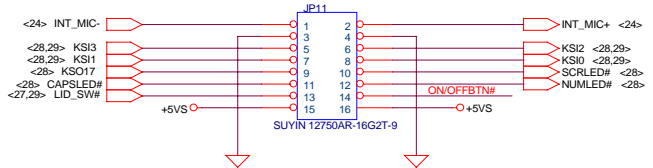


USB Over Current

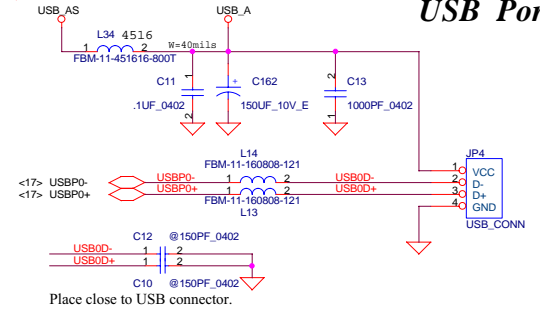


Note:
USB_AS=USB_BS=Trace width=40mils

LID Switch & Function Button

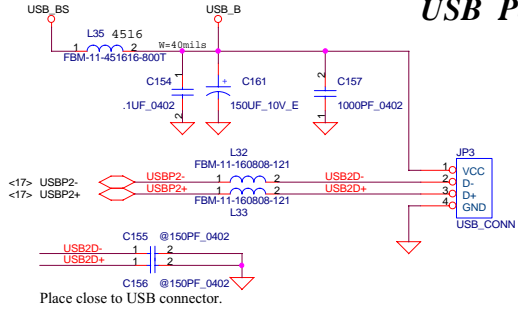


USB Port 0



Place close to USB connector.

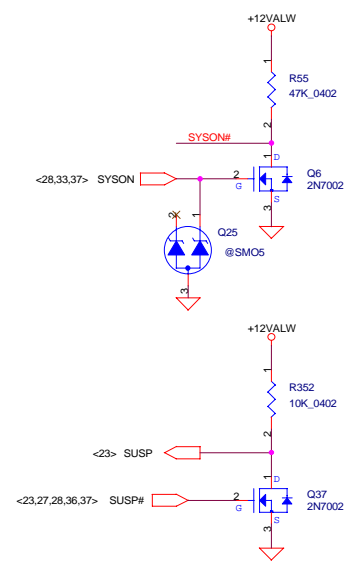
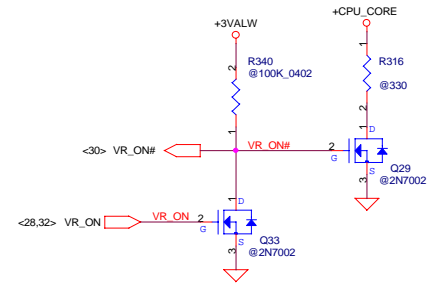
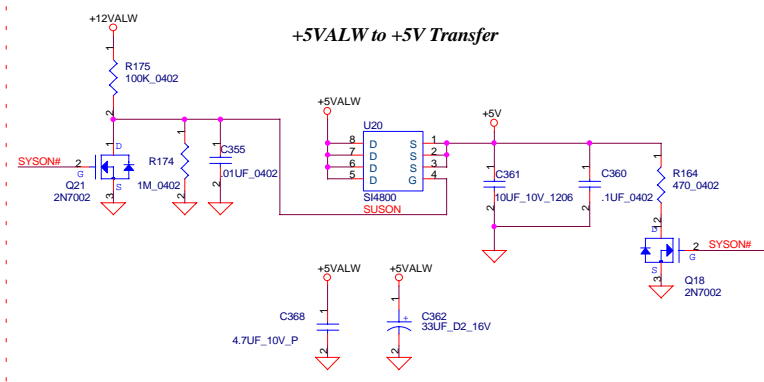
USB Port 1



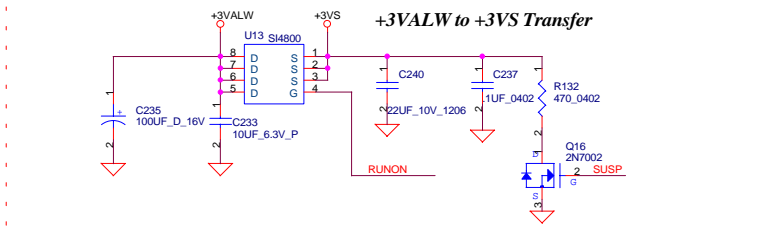
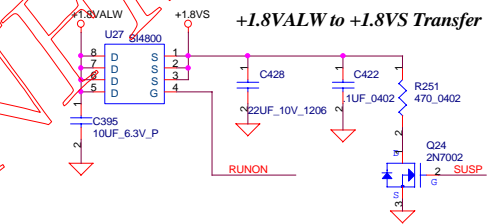
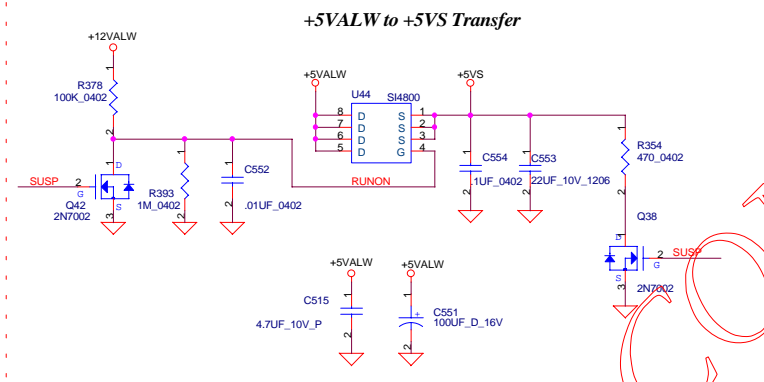
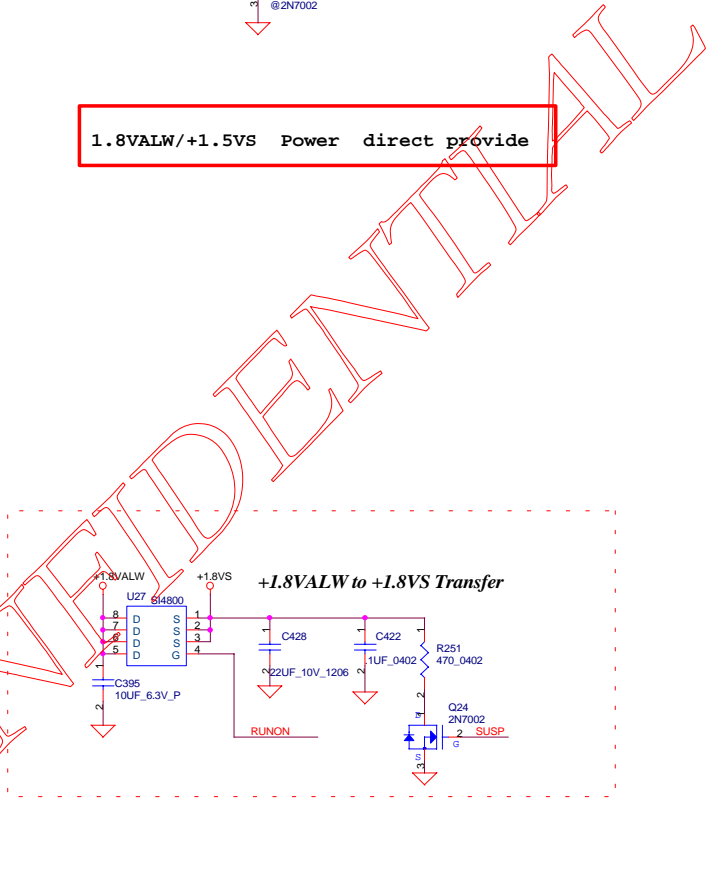
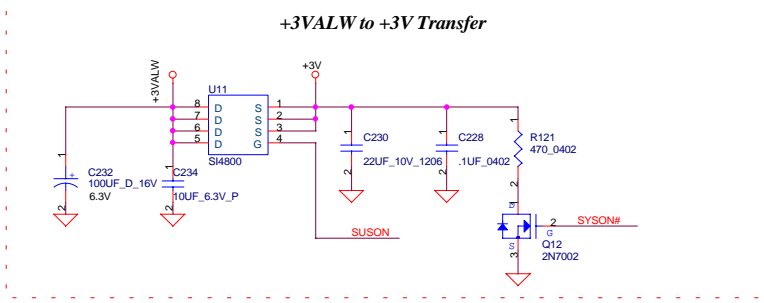
Place close to USB connector.

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Compal Electronics, Inc.			
Title	Power OK/Reset/RTC battery/USB Conn.& Lid Switch		
Size	Document Number	Rev	0.1
	ADY13 LA-1271		
Date	Monday, September 10, 2001	Sheet	30 of 37



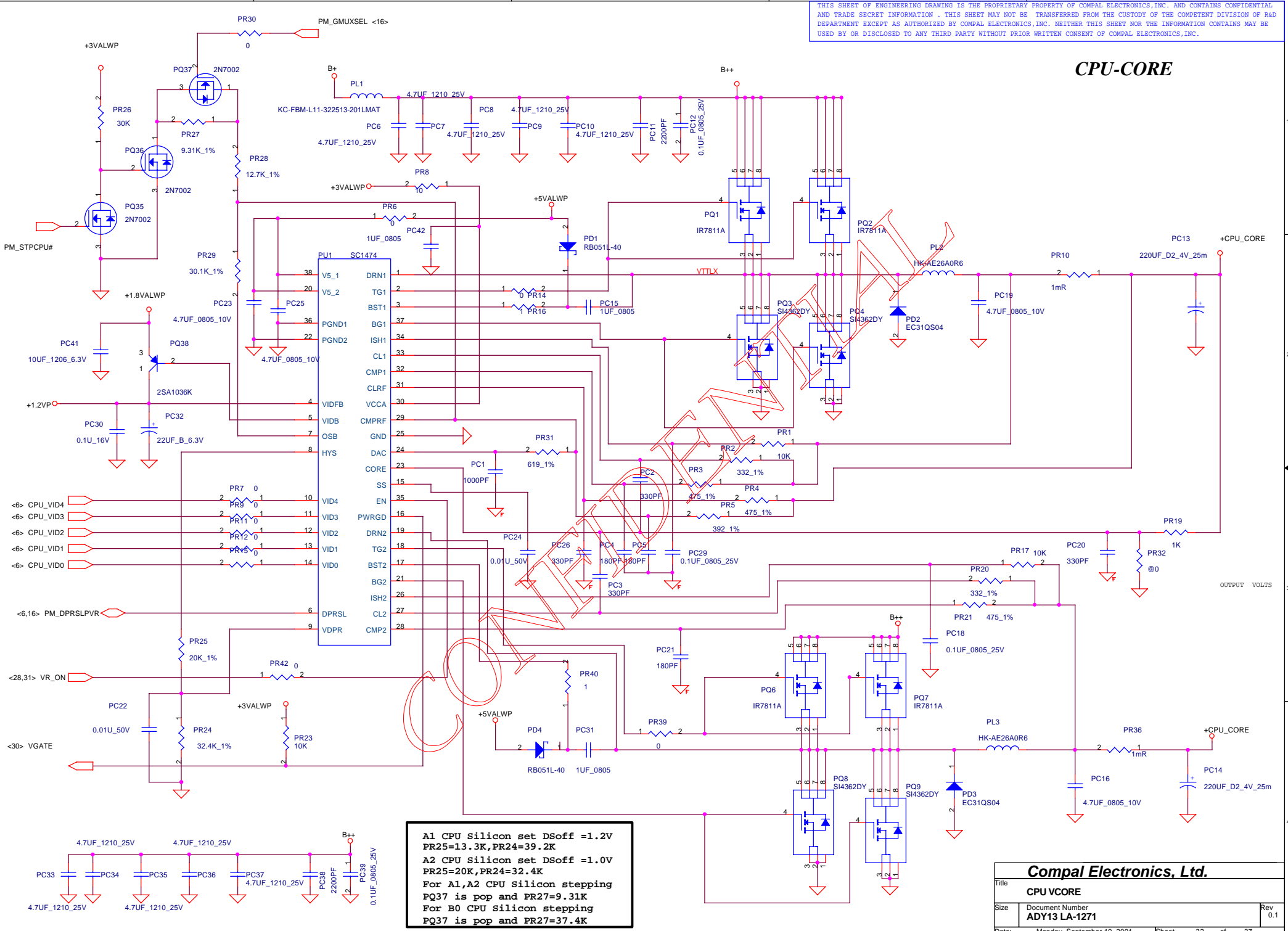
1.8VALW/+1.5VS Power direct provide



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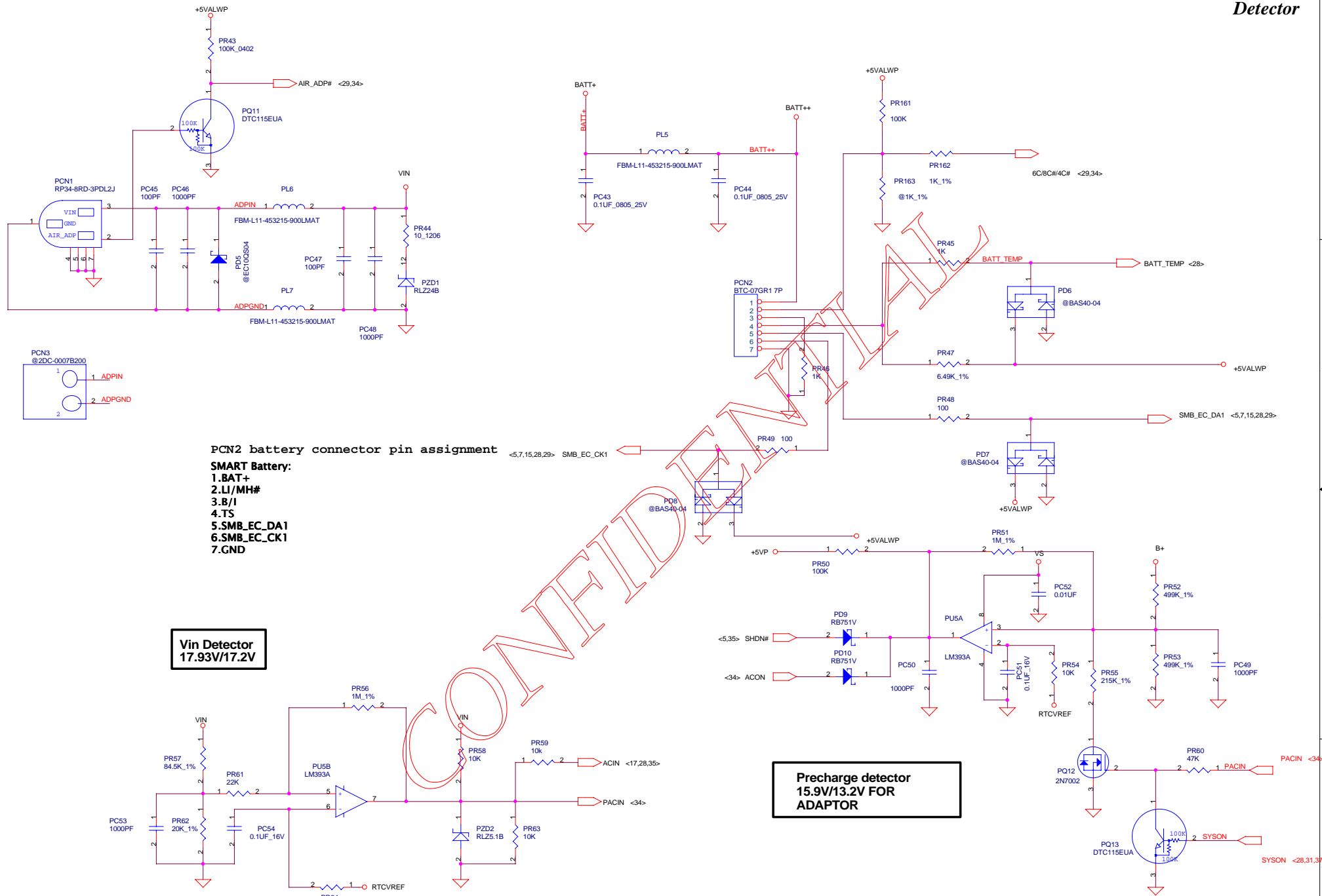
Compal Electronics, Inc.		
DC/DC Circuit		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 31 of 37

CPU-CORE



**A1 CPU Silicon set Dsoff =1.2V
 PR25=13.3K, PR24=39.2K
 A2 CPU Silicon set Dsoff =1.0V
 PR25=20K, PR24=32.4K
 For A1,A2 CPU Silicon stepping
 PQ37 is pop and PR27=9.31K
 For B0 CPU Silicon stepping
 PQ37 is pop and PR27=37.4K**

Compal Electronics, Ltd.		
Title	CPU VCORE	
Size	Document Number	Rev
	ADY13 LA-1271	0.1
Date:	Monday, September 10, 2001	Sheet 32 of 37



PCN2 battery connector pin assignment

- SMART Battery:**
 1. BATT+
 2. LI/MH#
 3. B/I
 4. TS
 5. SMB_EC_DA1
 6. SMB_EC_CK1
 7. GND

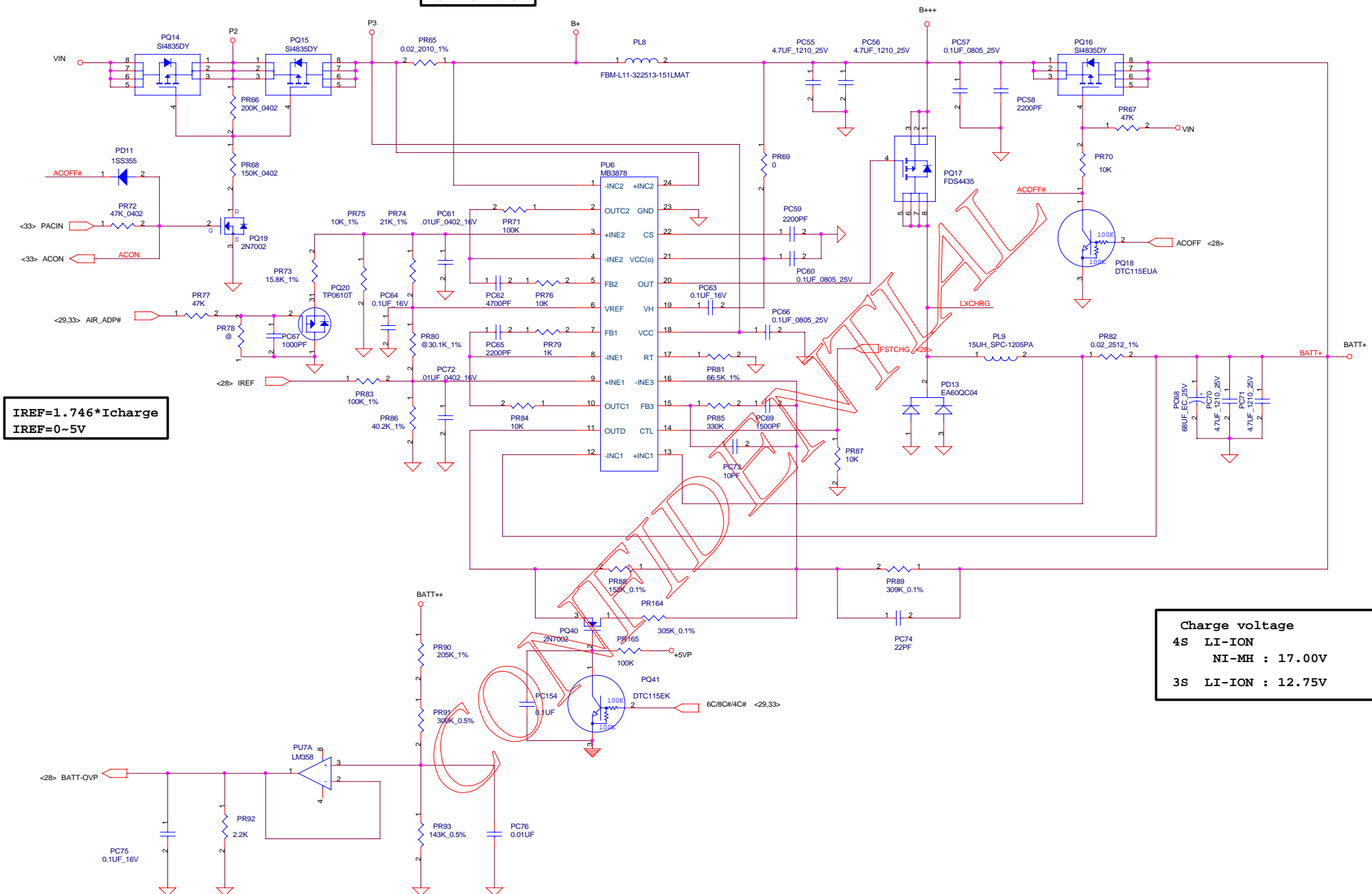
Vin Detector
 17.93V/17.2V

Precharge detector
 15.9V/13.2V FOR
 ADAPTOR

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Compal Electronics, Inc.		
Title Detector		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 33 of 37

$I_{adp}=0\sim 3.22A$ <-----Actually about 3A
 $I_{air}=0\sim 2.26A$



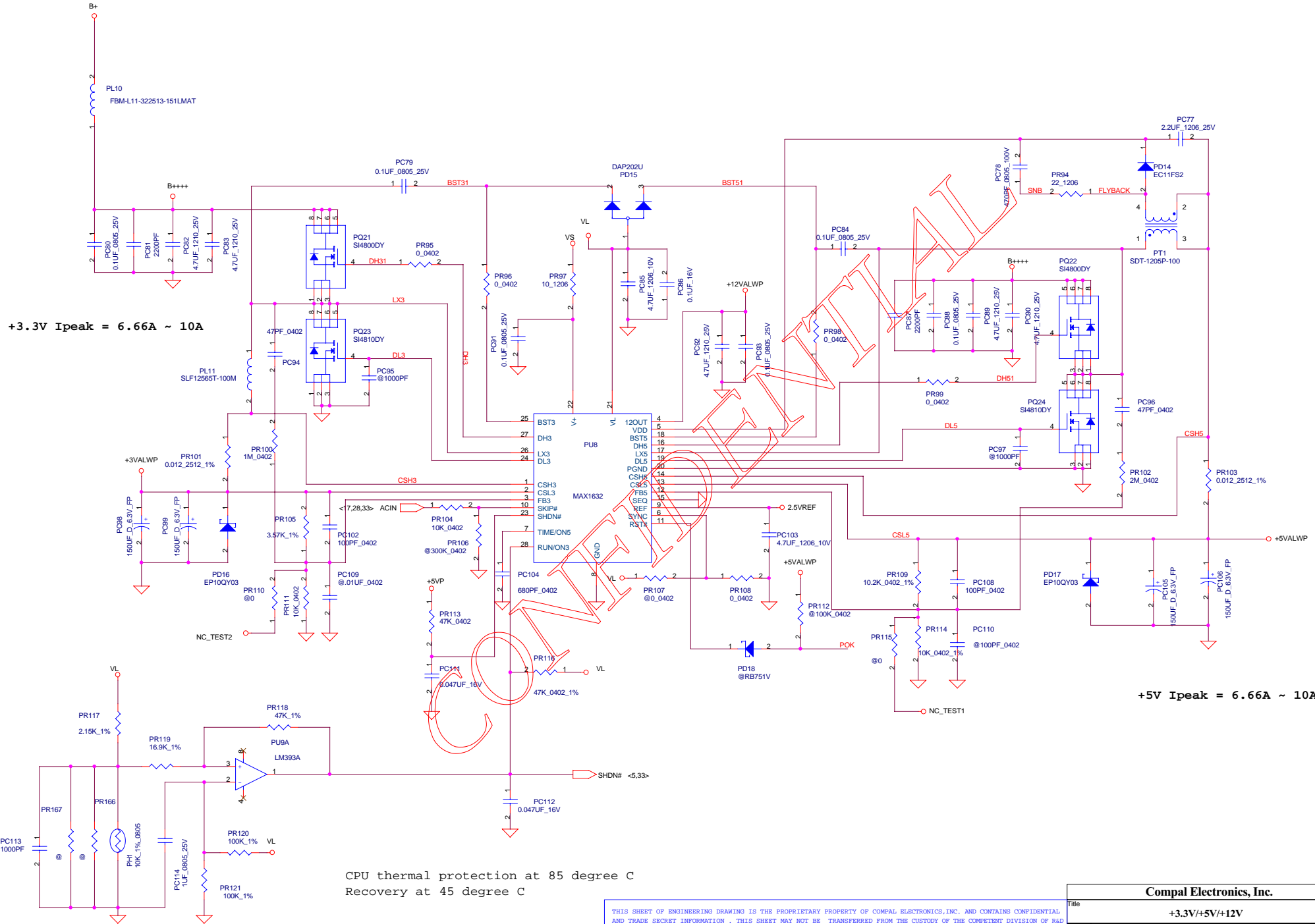
$I_{REF}=1.746 \cdot I_{charge}$
 $I_{REF}=0\sim 5V$

Charge voltage
 4S LI-ION
 NI-MH : 17.00V
 3S LI-ION : 12.75V

OVP voltage :
 LI-4S : 18.3V----BATT-OVP=4.04V
 LI-3S : 13.5V----BATT-OVP=3.82V
 BATT-OVP=0.2206*BATT++

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Compal Electronics, Inc.		
Charger		
Title	Document Number	Rev
	ADY13 LA-1271	0.1
Date	Monday, September 10, 2001	Sheet 34 of 37

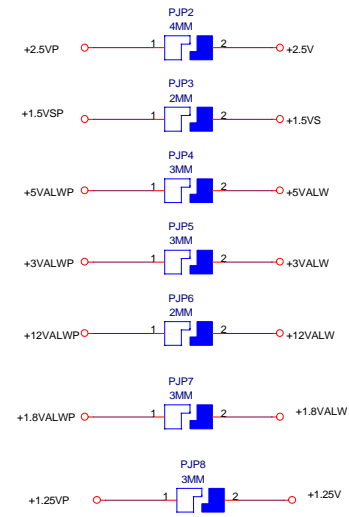
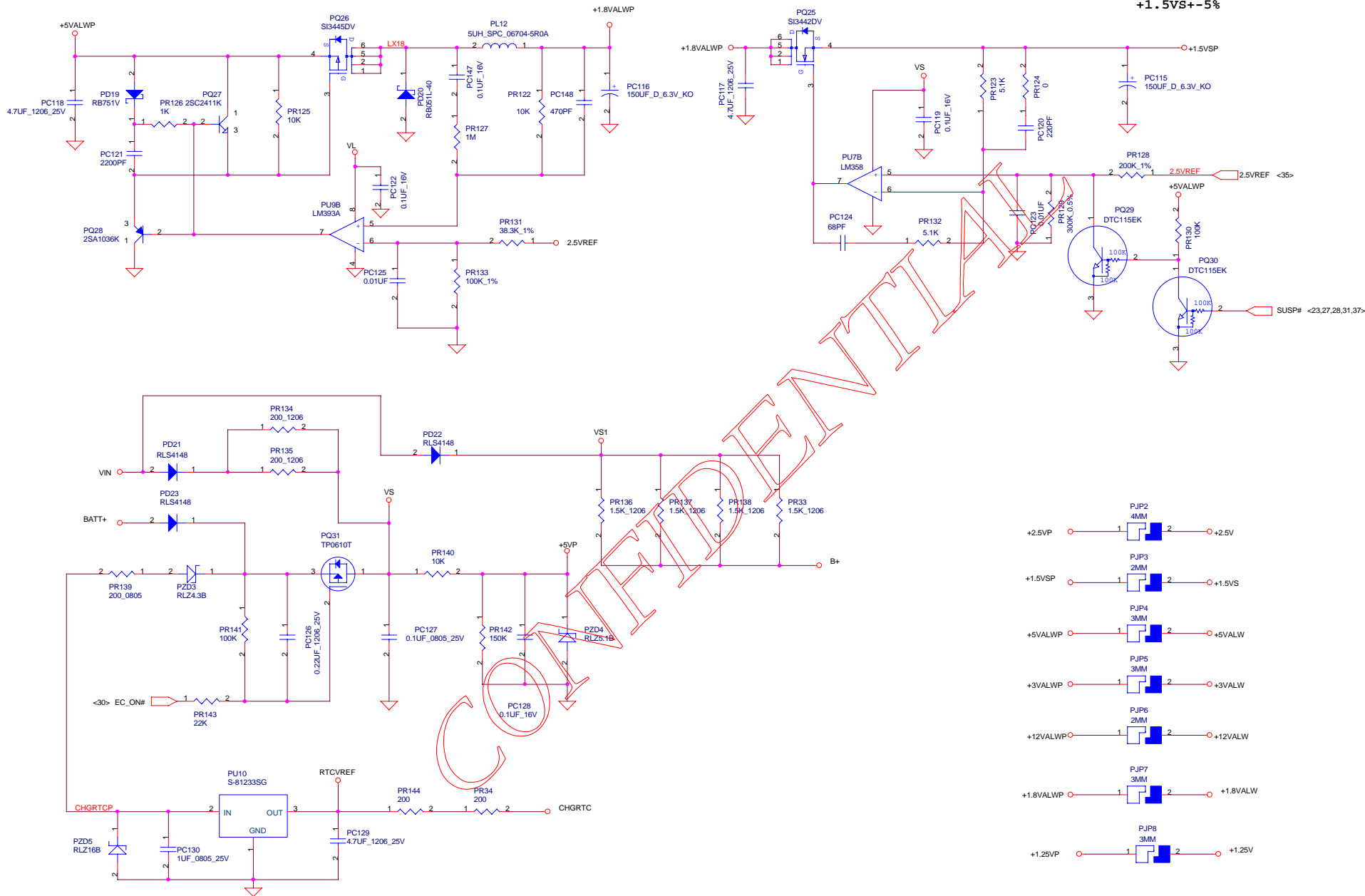


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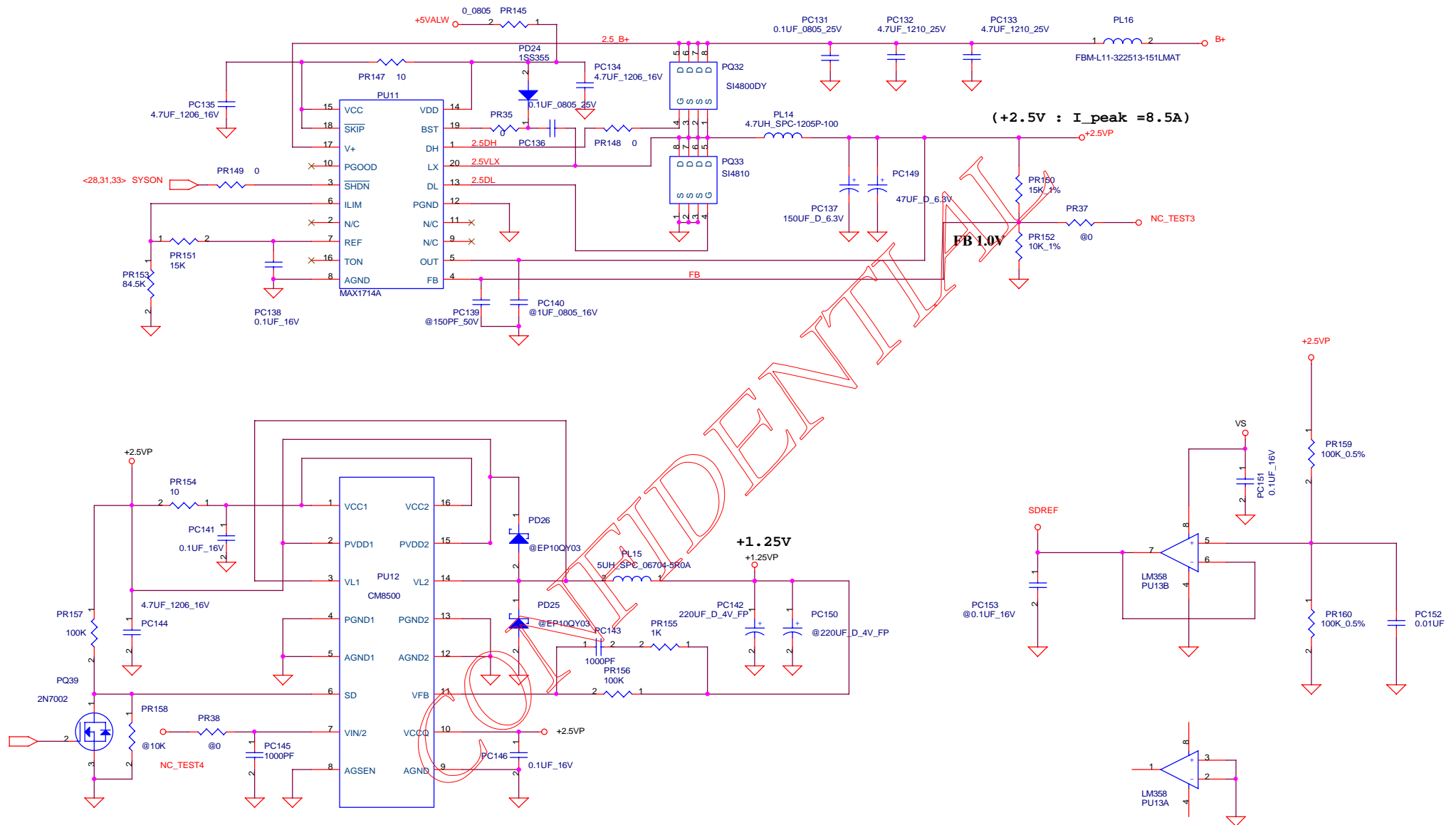
Compal Electronics, Inc.		
Title +3.3V/+5V/+12V		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 35 of 37

+1.8V+-5%

+1.5VS+-5%



Compal Electronics, Inc.		
Title +1.8VALW		
Size	Document Number ADY13 LA-1271	Rev 0.1
Date	Monday, September 10, 2001	Sheet 36 of 37



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COMPAL ELECTRONICS, INC			
Title DDR POWER 2.5V & 1.25V			
Size B	Document Number ADY13 LA-1271	Rev 0.1	
Date: Monday, September 10, 2001	Sheet	37	of 37