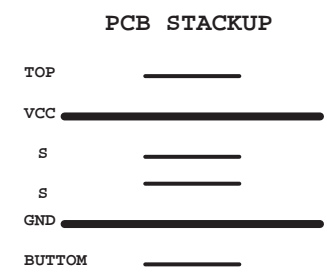
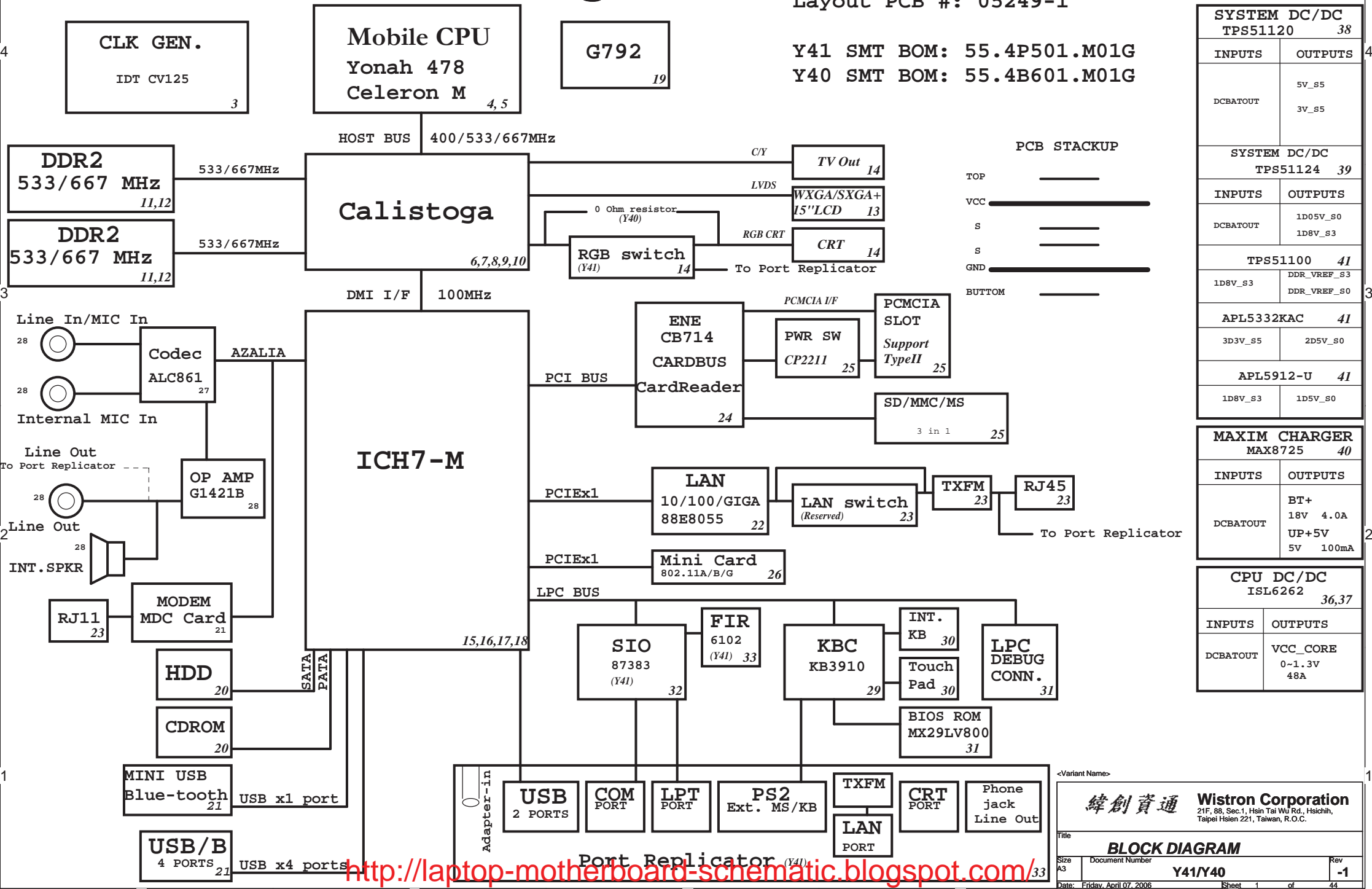


# Y41/Y40 Block Diagram

Project code: 91.4P501.001  
 PCB P/N : 48.4P501.011  
 Layout PCB #: 05249-1

Y41 SMT BOM: 55.4P501.M01G  
 Y40 SMT BOM: 55.4B601.M01G



<b>SYSTEM DC/DC</b>		<b>TPS51120</b>	<b>38</b>
INPUTS	OUTPUTS		
DCBATOUT	5V_S5	3V_S5	
<b>SYSTEM DC/DC</b>		<b>TPS51124</b>	<b>39</b>
INPUTS	OUTPUTS		
DCBATOUT	1D05V_S0	1D8V_S3	
<b>TPS51100</b>		<b>41</b>	
1D8V_S3	DDR_VREF_S3	DDR_VREF_S0	
<b>APL5332KAC</b>		<b>41</b>	
3D3V_S5	2D5V_S0		
<b>APL5912-U</b>		<b>41</b>	
1D8V_S3	1D5V_S0		
<b>MAXIM CHARGER</b>		<b>MAX8725</b>	<b>40</b>
INPUTS	OUTPUTS		
DCBATOUT	BT+	18V 4.0A	
	UP+5V	5V 100mA	
<b>CPU DC/DC</b>		<b>ISL6262</b>	<b>36,37</b>
INPUTS	OUTPUTS		
DCBATOUT	VCC_CORE	0~1.3V	
		48A	

<Variant Name>

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Title: **BLOCK DIAGRAM**

Size A3 Document Number: **Y41/Y40** Rev: **-1**

Date: Friday, April 07, 2006 Sheet 1 of 44

# ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

# ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

# ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

# 954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

# PCI Routing

page 24

IDSEL	INT ->	PIRQ	REQ/GNT
CB714	22	A->G, B->E,	0

# Calistoga Strapping Signals and Configuration

EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

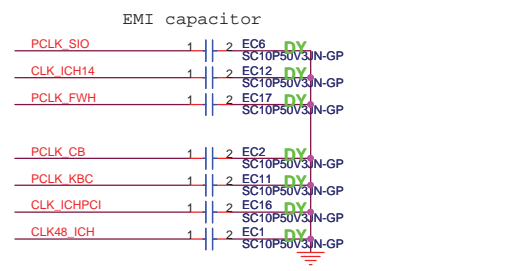
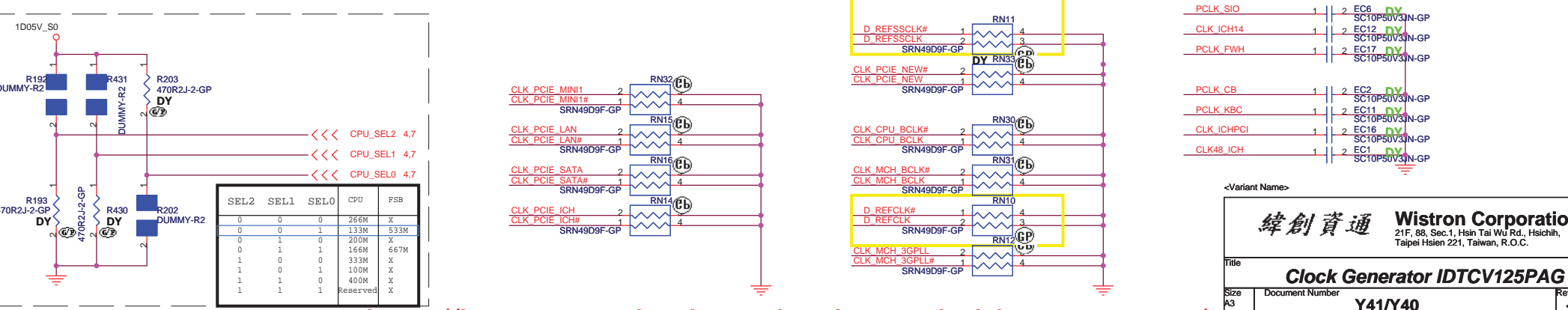
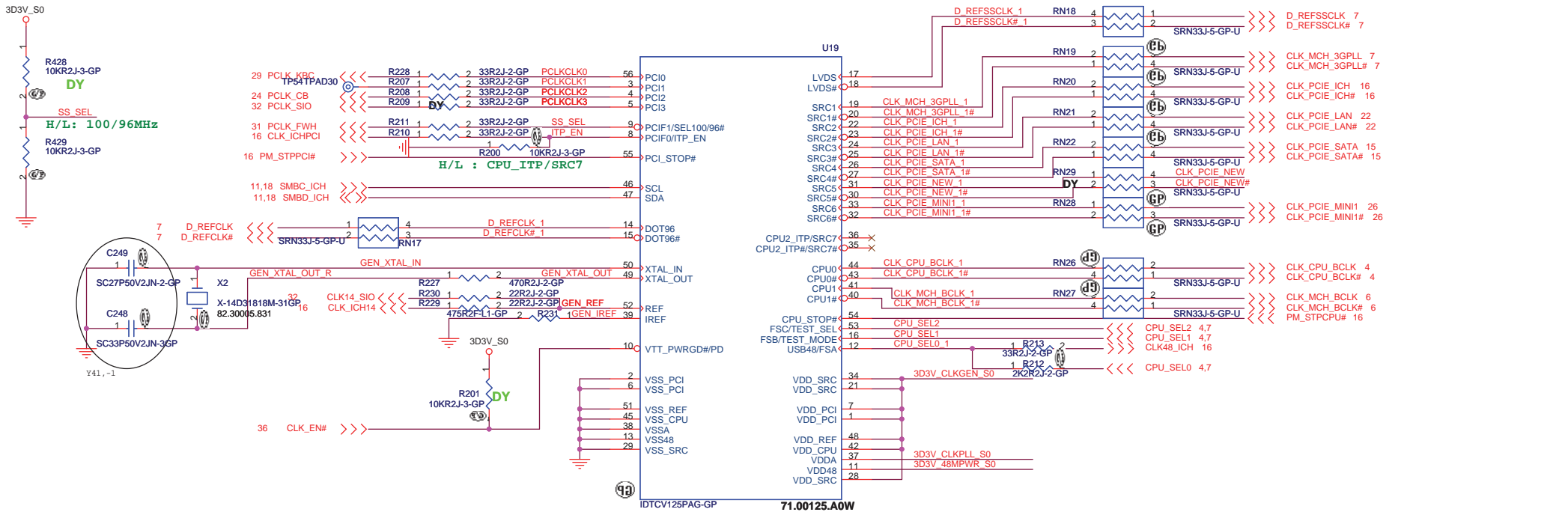
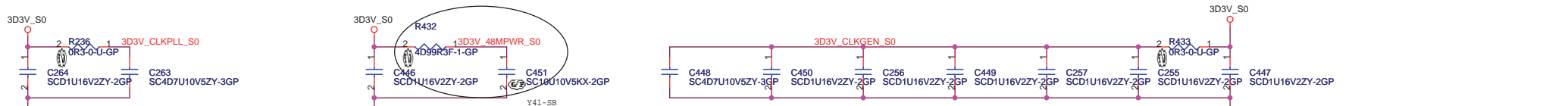
NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

# Device SSID/SVID

Device	SSID	SVID
LAN 88E8055	10C1	1734
Codec ALC861	10C1	1734


<Variant Name>

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<b>Reference</b>			
Size A3	Document Number	Rev	
	<b>Y41/Y40</b>	<b>-1</b>	
Date: Friday, April 07, 2006	Sheet 2	of	44



EMI capacitor

<Variant Name>



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Clock Generator IDTCV125PAG

Title

Size A3

Date: Wednesday, April 12, 2006

Document Number

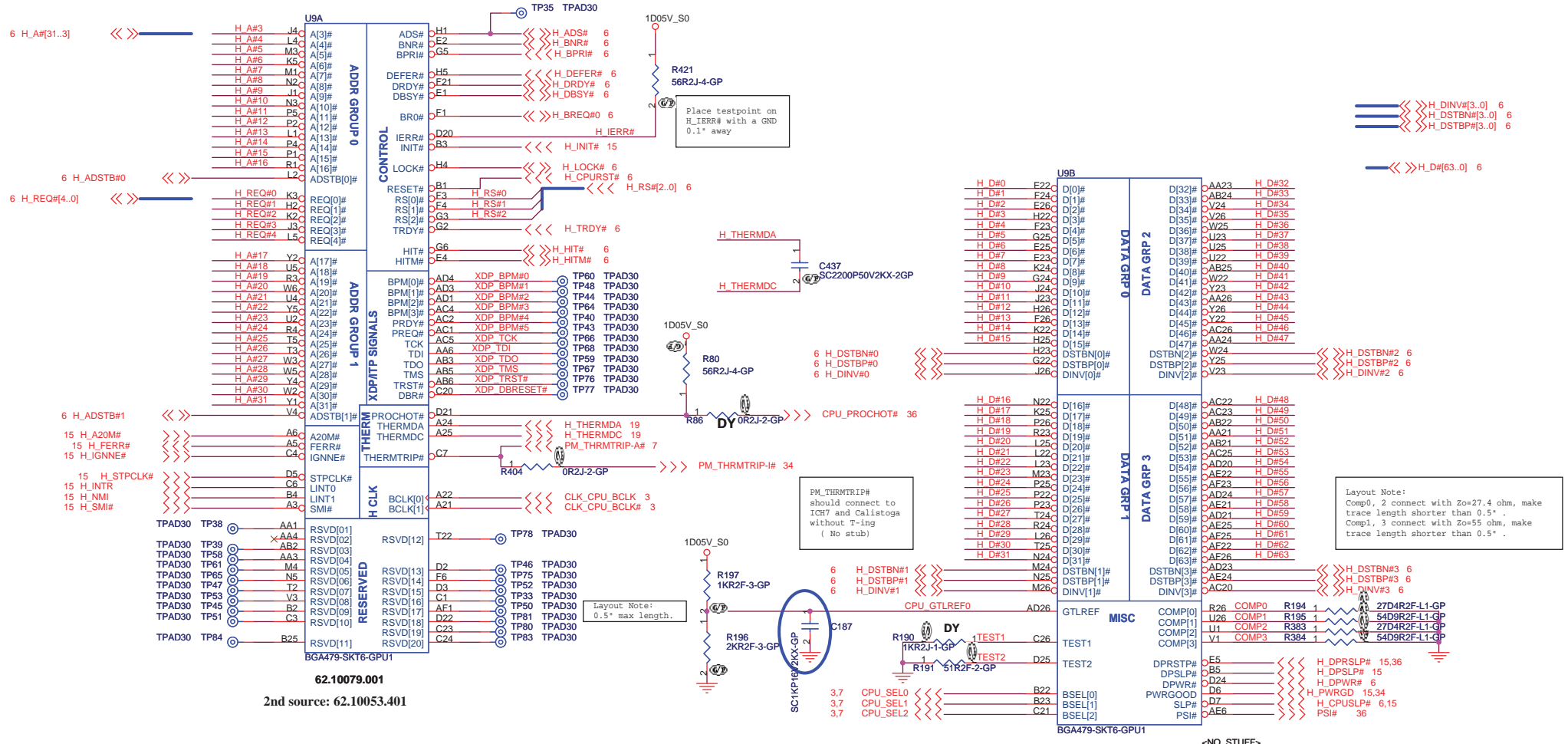
Y41/Y40

Sheet 3 of 44

Rev

-1

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H\_DINV# [3.0] 6  
H\_DSTBN# [3.0] 6  
H\_DSTBP# [3.0] 6

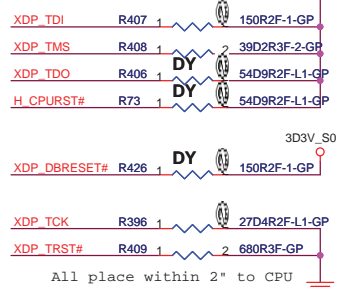
H\_D# [63.0] 6

Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

PM\_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)

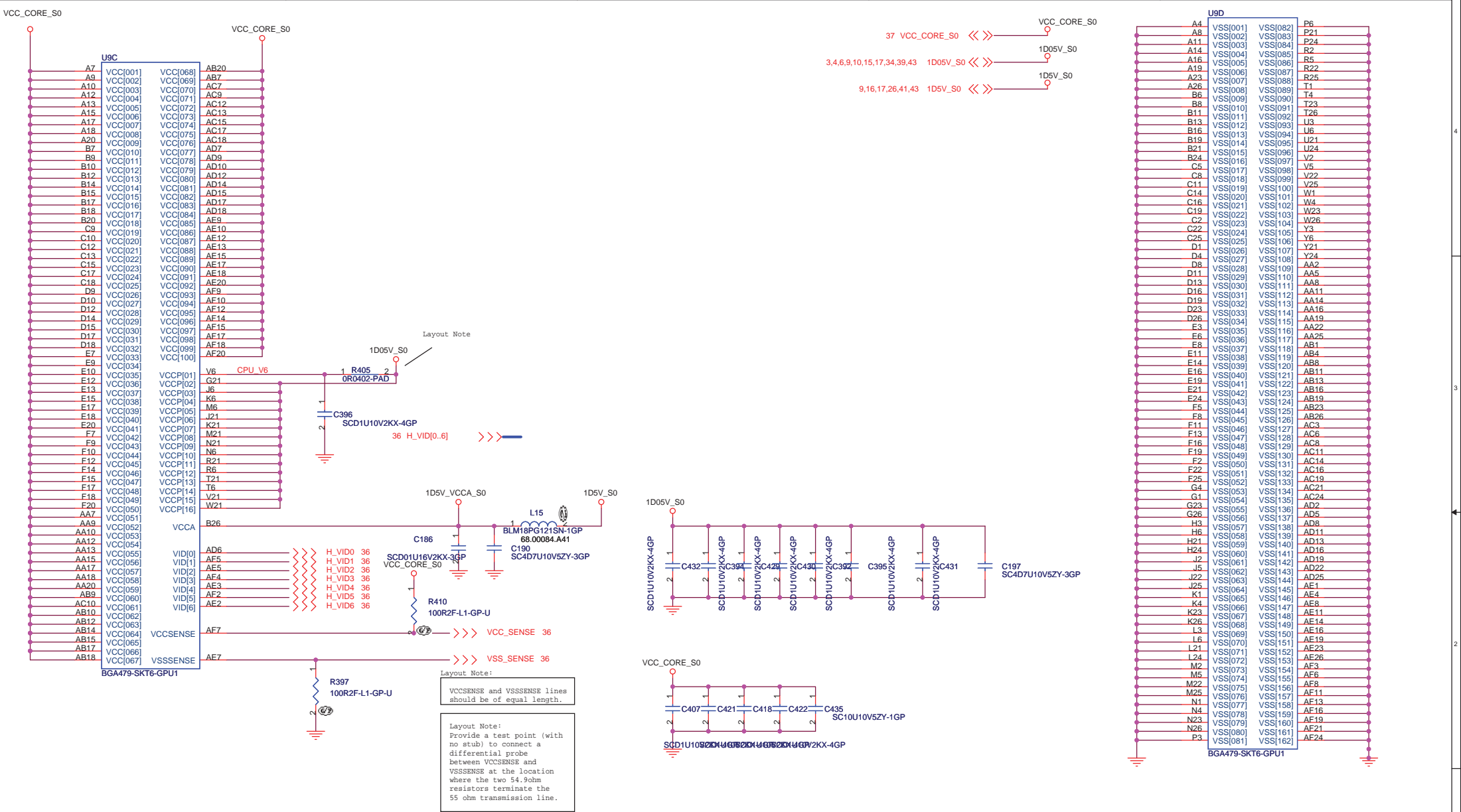
Layout Note: 0.5" max length.

<-NO\_STUFF->



All place within 2" to CPU

Wistron Corporation logo and title block containing document number, date, and sheet information.

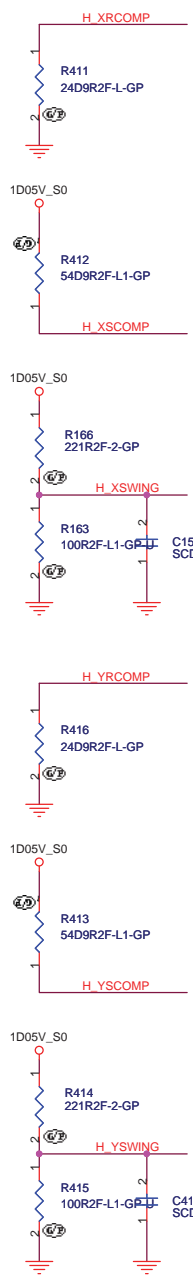


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Title: **CPU (2 of 2)**

Size A3 Document Number: **Y41/Y40** Rev: **-1**

Date: Wednesday, April 12, 2006 Sheet 5 of 44



4 H\_D# [63..0] <<>>

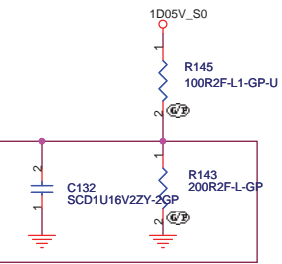
3 CLK\_MCH\_BCLK  
3 CLK\_MCH\_BCLK# <<>>

**U50A**

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J8	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63
H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSWING	U1	H_YSWING
H_YSCOMP	U11	H_YSCOMP
H_YSWING	W1	H_YSWING
H_CLKIN	AG2	H_CLKIN
H_CLKIN#	AG1	H_CLKIN#

**HOST**

H_A#_3	H9	H_A#3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	E9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	J14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	J15	H_A#16
H_A#_17	F14	H_A#17
H_A#_18	D12	H_A#18
H_A#_19	A11	H_A#19
H_A#_20	C11	H_A#20
H_A#_21	A12	H_A#21
H_A#_22	A13	H_A#22
H_A#_23	E13	H_A#23
H_A#_24	G13	H_A#24
H_A#_25	F12	H_A#25
H_A#_26	B12	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31	D14	H_A#31
H_ADS#	E8	H_ADS# 4
H_ADSTB#_0	B9	H_ADSTB#0 4
H_ADSTB#_1	C13	H_ADSTB#1 4
H_VREF	J13	H_VREF
H_BNR#	C6	H_BNR# 4
H_BPR#	F6	H_BPR# 4
H_BREQ#0	C7	H_BREQ#0 4
H_CPURST#	A7	H_CPURST# 4
H_DBSY#	B7	H_DBSY# 4
H_DEFER#	C3	H_DEFER# 4
H_DPWR#	J9	H_DPWR# 4
H_DRDY#	H8	H_DRDY# 4
H_VREF_1	K13	H_VREF_1
H_DINV#_0	J7	H_DINV#0
H_DINV#_1	W8	H_DINV#1
H_DINV#_2	U3	H_DINV#2
H_DINV#_3	AB10	H_DINV#3
H_DSTBN#_0	K4	H_DSTBN#0
H_DSTBN#_1	T7	H_DSTBN#1
H_DSTBN#_2	Y5	H_DSTBN#2
H_DSTBN#_3	AC4	H_DSTBN#3
H_DSTBP#_0	K3	H_DSTBP#0
H_DSTBP#_1	T6	H_DSTBP#1
H_DSTBP#_2	AA5	H_DSTBP#2
H_DSTBP#_3	AC5	H_DSTBP#3
H_HIT#	D3	H_HIT# 4
H_HITM#	D4	H_HITM# 4
H_LOCK#	B3	H_LOCK# 4
H_REQ#_0	D8	H_REQ#0
H_REQ#_1	G8	H_REQ#1
H_REQ#_2	B8	H_REQ#2
H_REQ#_3	F8	H_REQ#3
H_REQ#_4	A8	H_REQ#4
H_RS#_0	B4	H_RS#0
H_RS#_1	E6	H_RS#1
H_RS#_2	D6	H_RS#2
H_SLPCPU#	E3	H_SLPCPU# 4,15
H_TRDY#	E7	H_TRDY# 4



Place them near to the chip (< 0.5")

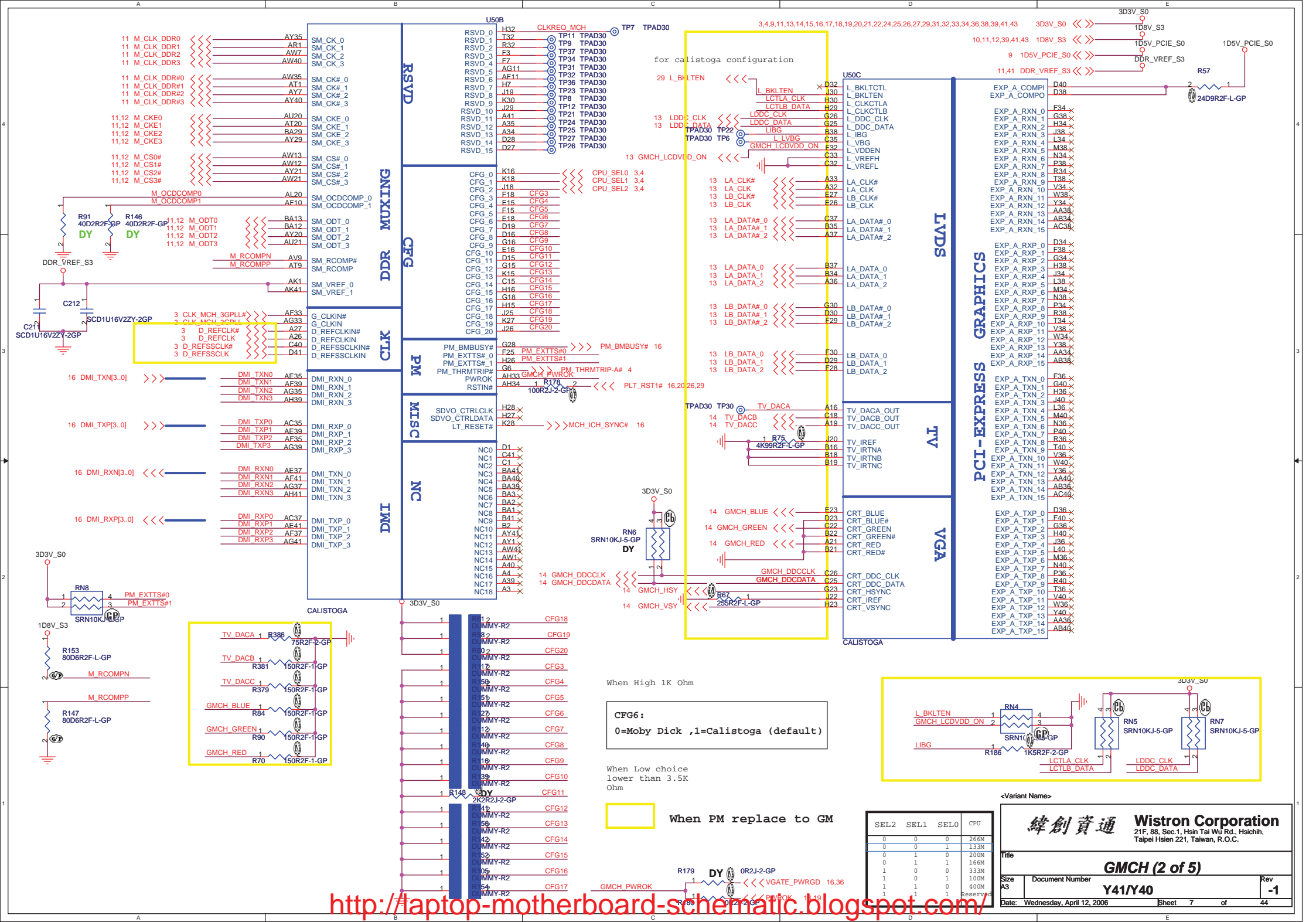
<Variant Name>

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Title: **GMCH (1 of 5)**

Size A3 Document Number **Y41/Y40** Rev **-1**

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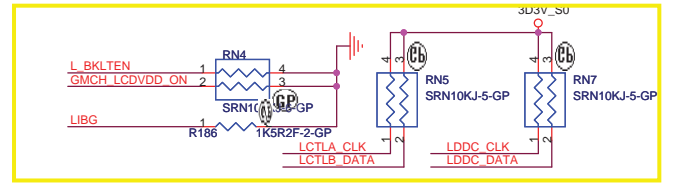
<http://laptop-motherboard-schematic.blogspot.com/>

When High 1K Ohm

CFG6:  
0=Moby Dick ,1=Calistoga (default)

When Low choice lower than 3.5K Ohm

When PM replace to GM



SEL2	SEL1	SEL0	CPU
0	0	0	266M
0	0	1	333M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reset

<Variant Name>

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**GMCH (2 of 5)**

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11 M\_A\_DQ[63..0] <<>>

U50D		
M_A_DQ0	AJ35	SA_DQ0
M_A_DQ1	AJ34	SA_DQ1
M_A_DQ2	AM31	SA_DQ2
M_A_DQ3	AM33	SA_DQ3
M_A_DQ4	AJ36	SA_DQ4
M_A_DQ5	AK35	SA_DQ5
M_A_DQ6	AJ32	SA_DQ6
M_A_DQ7	AH31	SA_DQ7
M_A_DQ8	AN35	SA_DQ8
M_A_DQ9	AP33	SA_DQ9
M_A_DQ10	AR31	SA_DQ10
M_A_DQ11	AP31	SA_DQ11
M_A_DQ12	AN38	SA_DQ12
M_A_DQ13	AM36	SA_DQ13
M_A_DQ14	AM34	SA_DQ14
M_A_DQ15	AN33	SA_DQ15
M_A_DQ16	AK26	SA_DQ16
M_A_DQ17	AL27	SA_DQ17
M_A_DQ18	AM26	SA_DQ18
M_A_DQ19	AN24	SA_DQ19
M_A_DQ20	AK28	SA_DQ20
M_A_DQ21	AL28	SA_DQ21
M_A_DQ22	AM24	SA_DQ22
M_A_DQ23	AP26	SA_DQ23
M_A_DQ24	AP23	SA_DQ24
M_A_DQ25	AL22	SA_DQ25
M_A_DQ26	AP21	SA_DQ26
M_A_DQ27	AN20	SA_DQ27
M_A_DQ28	AL23	SA_DQ28
M_A_DQ29	AP24	SA_DQ29
M_A_DQ30	AP20	SA_DQ30
M_A_DQ31	AT21	SA_DQ31
M_A_DQ32	AR12	SA_DQ32
M_A_DQ33	AR14	SA_DQ33
M_A_DQ34	AP13	SA_DQ34
M_A_DQ35	AP12	SA_DQ35
M_A_DQ36	AT13	SA_DQ36
M_A_DQ37	AT12	SA_DQ37
M_A_DQ38	AL14	SA_DQ38
M_A_DQ39	AL12	SA_DQ39
M_A_DQ40	AK9	SA_DQ40
M_A_DQ41	AN7	SA_DQ41
M_A_DQ42	AK8	SA_DQ42
M_A_DQ43	AK7	SA_DQ43
M_A_DQ44	AP9	SA_DQ44
M_A_DQ45	AN9	SA_DQ45
M_A_DQ46	AT5	SA_DQ46
M_A_DQ47	AL5	SA_DQ47
M_A_DQ48	AY2	SA_DQ48
M_A_DQ49	AW2	SA_DQ49
M_A_DQ50	AP1	SA_DQ50
M_A_DQ51	AN2	SA_DQ51
M_A_DQ52	AV2	SA_DQ52
M_A_DQ53	AT3	SA_DQ53
M_A_DQ54	AN1	SA_DQ54
M_A_DQ55	AL2	SA_DQ55
M_A_DQ56	AG7	SA_DQ56
M_A_DQ57	AF9	SA_DQ57
M_A_DQ58	AG4	SA_DQ58
M_A_DQ59	AF6	SA_DQ59
M_A_DQ60	AG9	SA_DQ60
M_A_DQ61	AH6	SA_DQ61
M_A_DQ62	AF4	SA_DQ62
M_A_DQ63	AF8	SA_DQ63

CALISTOGA

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M_A_BS# 11,12
SA_BS_1	AV14	M_A_BS#1 11,12
SA_BS_2	BA20	M_A_BS#2 11,12
SA_CAS#	AY13	M_A_CAS# 11,12
SA_DM_0	AJ33	M_A_DM0
SA_DM_1	AM35	M_A_DM1
SA_DM_2	AL26	M_A_DM2
SA_DM_3	AN22	M_A_DM3
SA_DM_4	AM14	M_A_DM4
SA_DM_5	AL9	M_A_DM5
SA_DM_6	AR3	M_A_DM6
SA_DM_7	AH4	M_A_DM7
SA_DQS_0	AK33	M_A_DQS0
SA_DQS_1	AT33	M_A_DQS1
SA_DQS_2	AN28	M_A_DQS2
SA_DQS_3	AM22	M_A_DQS3
SA_DQS_4	AN12	M_A_DQS4
SA_DQS_5	AN8	M_A_DQS5
SA_DQS_6	AP3	M_A_DQS6
SA_DQS_7	AG5	M_A_DQS7
SA_DQS#_0	AK32	M_A_DQS#0
SA_DQS#_1	AJ33	M_A_DQS#1
SA_DQS#_2	AN27	M_A_DQS#2
SA_DQS#_3	AM21	M_A_DQS#3
SA_DQS#_4	AM12	M_A_DQS#4
SA_DQS#_5	AL8	M_A_DQS#5
SA_DQS#_6	AN3	M_A_DQS#6
SA_DQS#_7	AH5	M_A_DQS#7
SA_MA_0	AY16	M_A_A0
SA_MA_1	AU14	M_A_A1
SA_MA_2	AW16	M_A_A2
SA_MA_3	BA16	M_A_A3
SA_MA_4	BA17	M_A_A4
SA_MA_5	AU16	M_A_A5
SA_MA_6	AV17	M_A_A6
SA_MA_7	AU17	M_A_A7
SA_MA_8	AW17	M_A_A8
SA_MA_9	AT16	M_A_A9
SA_MA_10	AU13	M_A_A10
SA_MA_11	AT17	M_A_A11
SA_MA_12	AV20	M_A_A12
SA_MA_13	AV12	M_A_A13
SA_RAS#	AW14	M_A_RAS# 11,12
SA_RCVENIN#	AK23	SA_RCVENIN#
SA_RCVENOUT#	AK24	SA_RCVENOUT#
SA_WE#	AY14	M_A_WE# 11,12

Place Test PAD Near to Chip as could as possible

11 M\_B\_DQ[63..0] <<>>

U50E		
M_B_DQ0	AK39	SB_DQ0
M_B_DQ1	AJ37	SB_DQ1
M_B_DQ2	AP39	SB_DQ2
M_B_DQ3	AR41	SB_DQ3
M_B_DQ4	AJ38	SB_DQ4
M_B_DQ5	AK38	SB_DQ5
M_B_DQ6	AN41	SB_DQ6
M_B_DQ7	AP41	SB_DQ7
M_B_DQ8	AT40	SB_DQ8
M_B_DQ9	AV41	SB_DQ9
M_B_DQ10	AU38	SB_DQ10
M_B_DQ11	AV38	SB_DQ11
M_B_DQ12	AP38	SB_DQ12
M_B_DQ13	AR40	SB_DQ13
M_B_DQ14	AW38	SB_DQ14
M_B_DQ15	AV38	SB_DQ15
M_B_DQ16	BA38	SB_DQ16
M_B_DQ17	AV36	SB_DQ17
M_B_DQ18	AR36	SB_DQ18
M_B_DQ19	AP36	SB_DQ19
M_B_DQ20	BA36	SB_DQ20
M_B_DQ21	AP35	SB_DQ21
M_B_DQ22	AP35	SB_DQ22
M_B_DQ23	AP34	SB_DQ23
M_B_DQ24	AY33	SB_DQ24
M_B_DQ25	BA33	SB_DQ25
M_B_DQ26	AT31	SB_DQ26
M_B_DQ27	AU29	SB_DQ27
M_B_DQ28	AU31	SB_DQ28
M_B_DQ29	AW31	SB_DQ29
M_B_DQ30	AV29	SB_DQ30
M_B_DQ31	AW29	SB_DQ31
M_B_DQ32	AM19	SB_DQ32
M_B_DQ33	AL19	SB_DQ33
M_B_DQ34	AP14	SB_DQ34
M_B_DQ35	AN14	SB_DQ35
M_B_DQ36	AN17	SB_DQ36
M_B_DQ37	AM16	SB_DQ37
M_B_DQ38	AP15	SB_DQ38
M_B_DQ39	AL15	SB_DQ39
M_B_DQ40	AH11	SB_DQ40
M_B_DQ41	AH10	SB_DQ41
M_B_DQ42	AJ9	SB_DQ42
M_B_DQ43	AH10	SB_DQ43
M_B_DQ44	AK13	SB_DQ44
M_B_DQ45	AH11	SB_DQ45
M_B_DQ46	AK10	SB_DQ46
M_B_DQ47	AJ8	SB_DQ47
M_B_DQ48	BA10	SB_DQ48
M_B_DQ49	AW10	SB_DQ49
M_B_DQ50	BA4	SB_DQ50
M_B_DQ51	AW4	SB_DQ51
M_B_DQ52	AY10	SB_DQ52
M_B_DQ53	AY9	SB_DQ53
M_B_DQ54	AW5	SB_DQ54
M_B_DQ55	AY5	SB_DQ55
M_B_DQ56	AV4	SB_DQ56
M_B_DQ57	AR5	SB_DQ57
M_B_DQ58	AK4	SB_DQ58
M_B_DQ59	AK3	SB_DQ59
M_B_DQ60	AT4	SB_DQ60
M_B_DQ61	AK5	SB_DQ61
M_B_DQ62	AJ5	SB_DQ62
M_B_DQ63	AJ3	SB_DQ63

CALISTOGA

DDR SYSTEM MEMORY B

SB_BS_0	AT24	M_B_BS#0 11,12
SB_BS_1	AV23	M_B_BS#1 11,12
SB_BS_2	AY28	M_B_BS#2 11,12
SB_CAS#	AR24	M_B_CAS# 11,12
SB_DM_0	AK36	M_B_DM0
SB_DM_1	AR33	M_B_DM1
SB_DM_2	AT36	M_B_DM2
SB_DM_3	BA31	M_B_DM3
SB_DM_4	AL17	M_B_DM4
SB_DM_5	AH8	M_B_DM5
SB_DM_6	BA5	M_B_DM6
SB_DM_7	AN4	M_B_DM7
SB_DQS_0	AM39	M_B_DQS0
SB_DQS_1	AT39	M_B_DQS1
SB_DQS_2	AU35	M_B_DQS2
SB_DQS_3	AR29	M_B_DQS3
SB_DQS_4	AR16	M_B_DQS4
SB_DQS_5	AR10	M_B_DQS5
SB_DQS_6	AR7	M_B_DQS6
SB_DQS_7	AN5	M_B_DQS7
SB_DQS#_0	AM40	M_B_DQS#0
SB_DQS#_1	AU39	M_B_DQS#1
SB_DQS#_2	AT35	M_B_DQS#2
SB_DQS#_3	AP29	M_B_DQS#3
SB_DQS#_4	AP16	M_B_DQS#4
SB_DQS#_5	AT10	M_B_DQS#5
SB_DQS#_6	AT7	M_B_DQS#6
SB_DQS#_7	AP5	M_B_DQS#7
SB_MA_0	AV23	M_B_A0
SB_MA_1	AW24	M_B_A1
SB_MA_2	AY24	M_B_A2
SB_MA_3	AR28	M_B_A3
SB_MA_4	AT27	M_B_A4
SB_MA_5	AT28	M_B_A5
SB_MA_6	AU27	M_B_A6
SB_MA_7	AV28	M_B_A7
SB_MA_8	AV27	M_B_A8
SB_MA_9	AW27	M_B_A9
SB_MA_10	AV24	M_B_A10
SB_MA_11	BA27	M_B_A11
SB_MA_12	AY27	M_B_A12
SB_MA_13	AR23	M_B_A13
SB_RAS#	AU23	M_B_RAS# 11,12
SB_RCVENIN#	AK16	SB_RCVENIN#
SB_RCVENOUT#	AK18	SB_RCVENOUT#
SB_WE#	AR27	M_B_WE# 11,12

Place Test PAD Near to Chip as could as possible

<Variant Name>

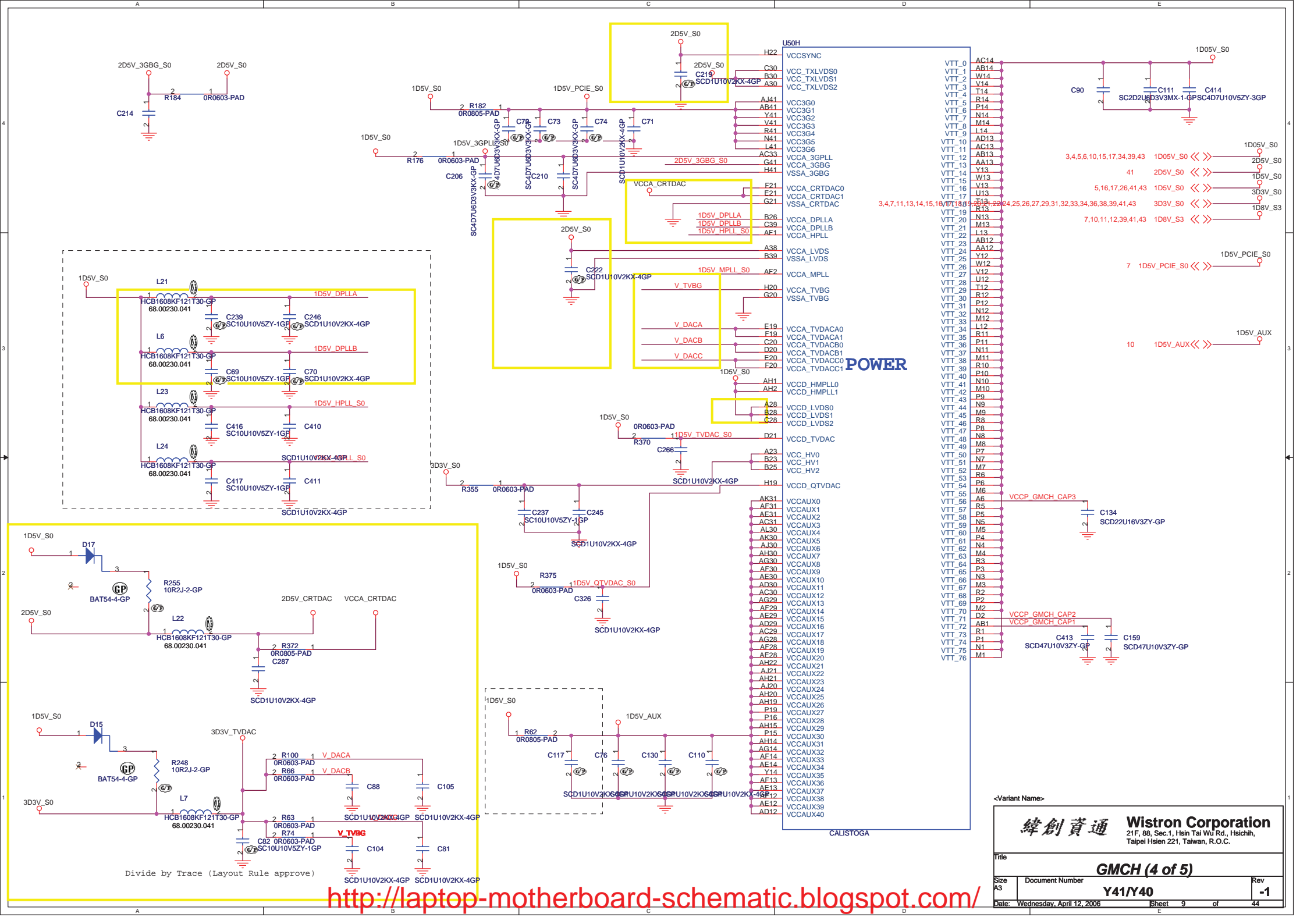
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (3 of 5)**

Size A3 Document Number **Y41/Y40** Rev **-1**

Date: Wednesday, April 12, 2006 Sheet 8 of 44





**POWER**

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 Taipei Hsien 221, Taiwan, R.O.C.

**GMCH (4 of 5)**

Size A3 Document Number **Y41/Y40** Rev **-1**

Date: Wednesday, April 12, 2006 Sheet 9 of 44

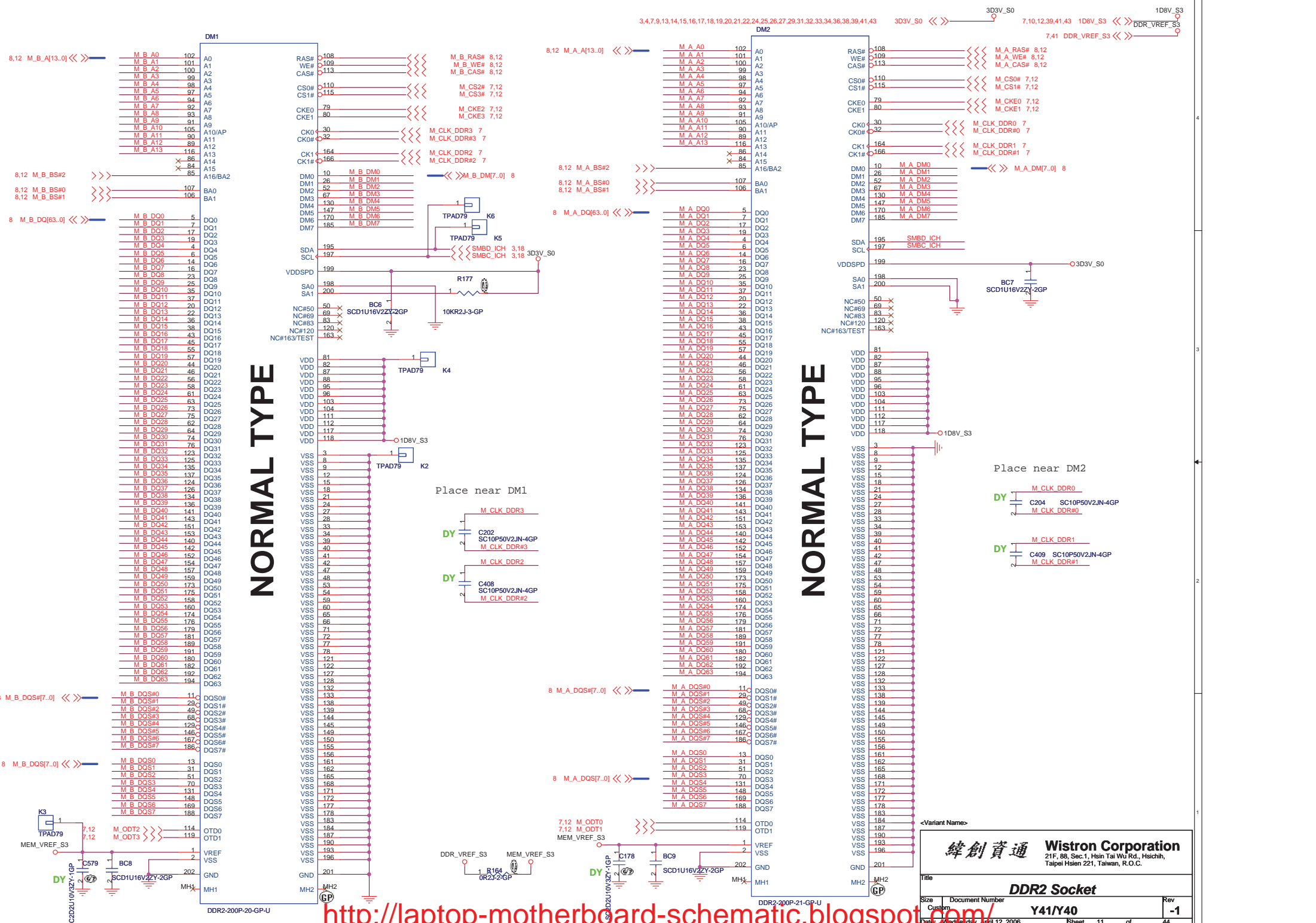
<http://laptop-motherboard-schematic.blogspot.com/>

Divide by Trace (Layout Rule approve)

<Variant Name>

CALISTOGA





**NORMAL TYPE**

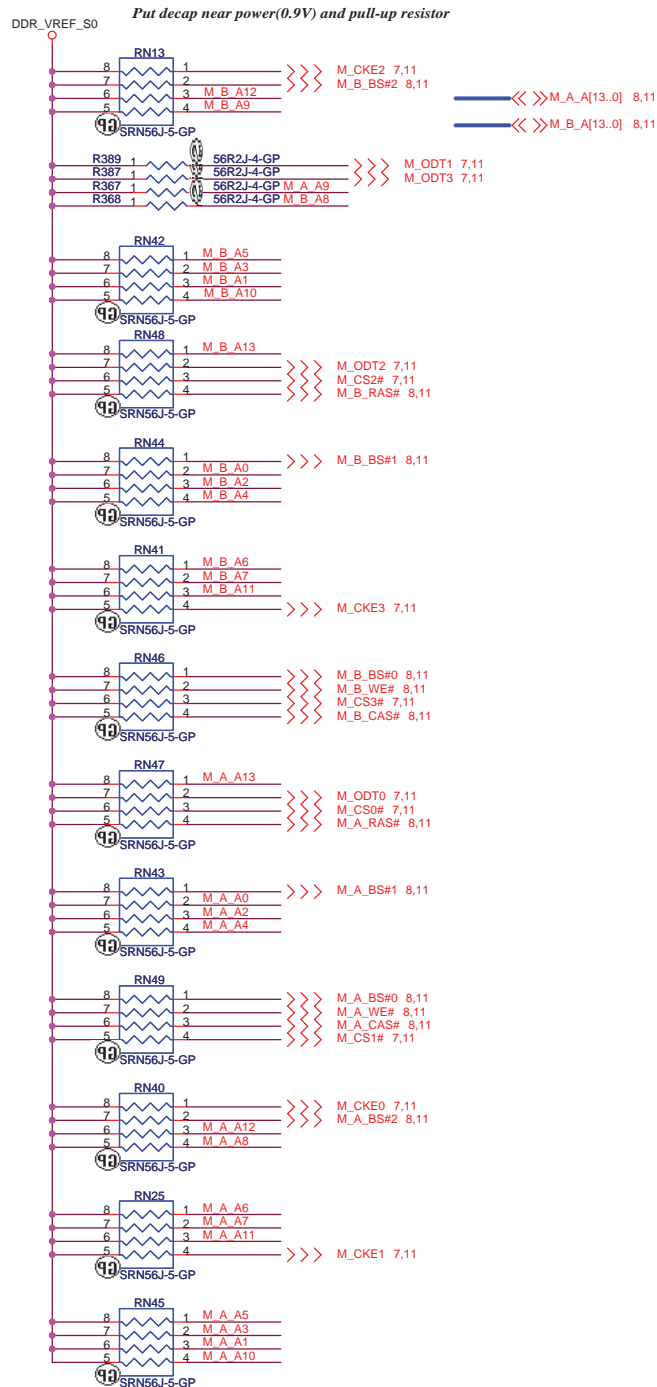
**NORMAL TYPE**

<http://laptop-motherboard-schematic.blogspot.com/>

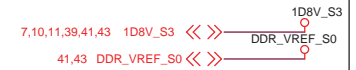
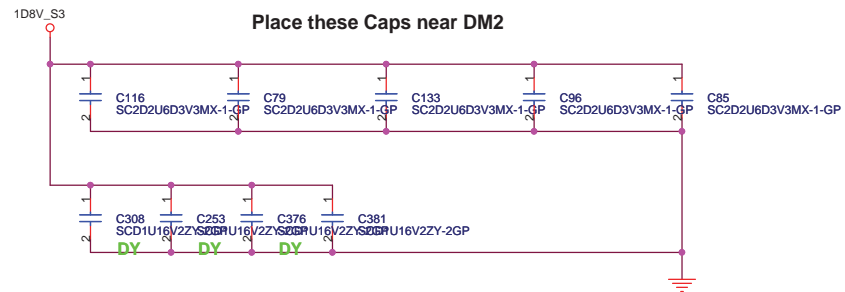
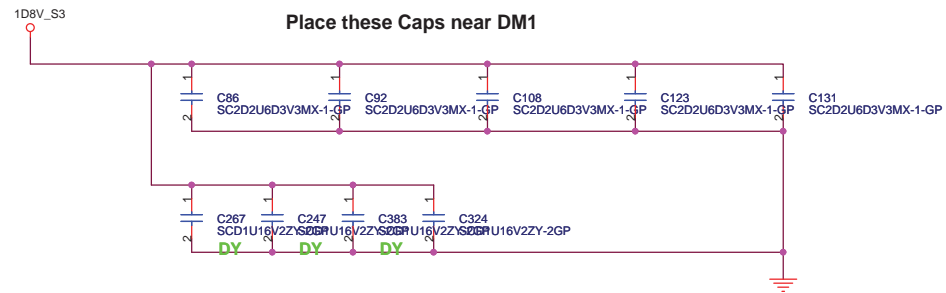
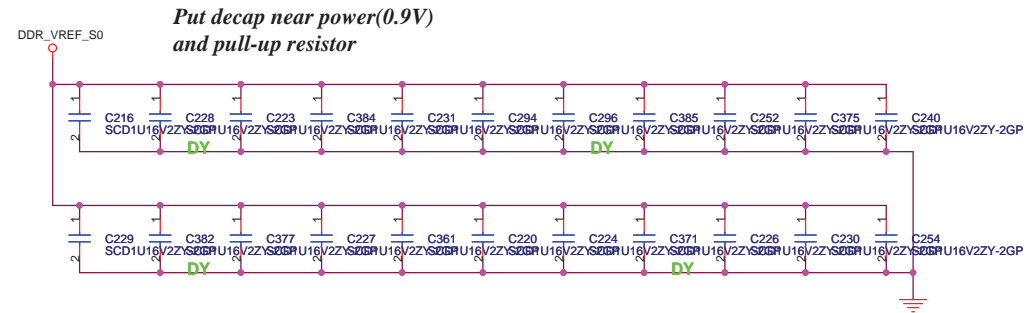
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Socket**  
 Size: Custom Document Number: Y41/Y40 Rev: -1  
 Date: 2006.06.07, 11:12:06 Sheet: 11 of 44

# PARALLEL TERMINATION

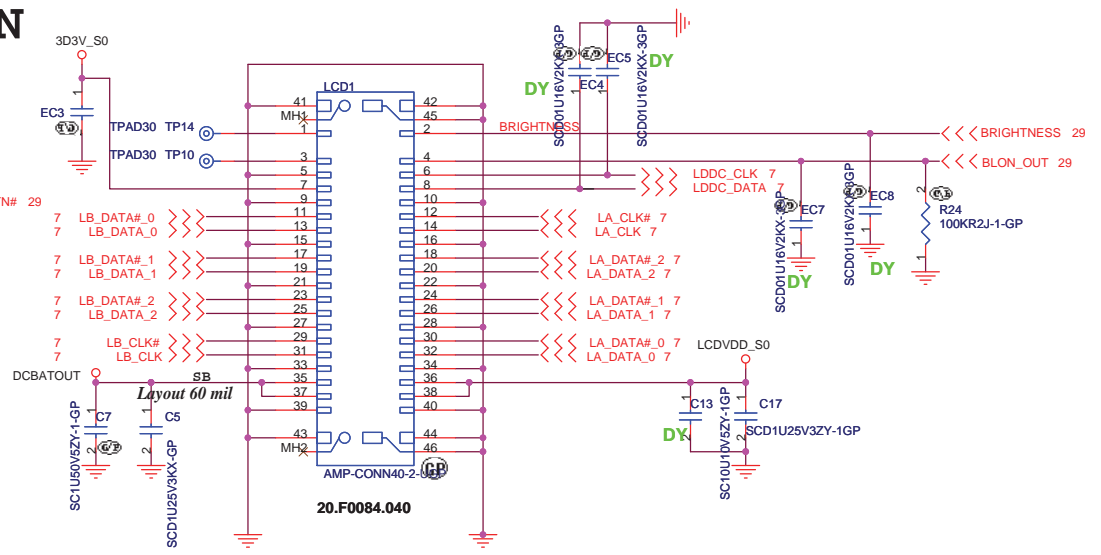
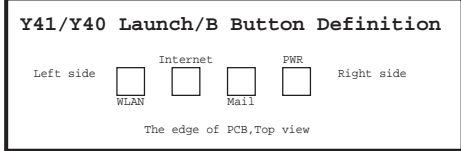
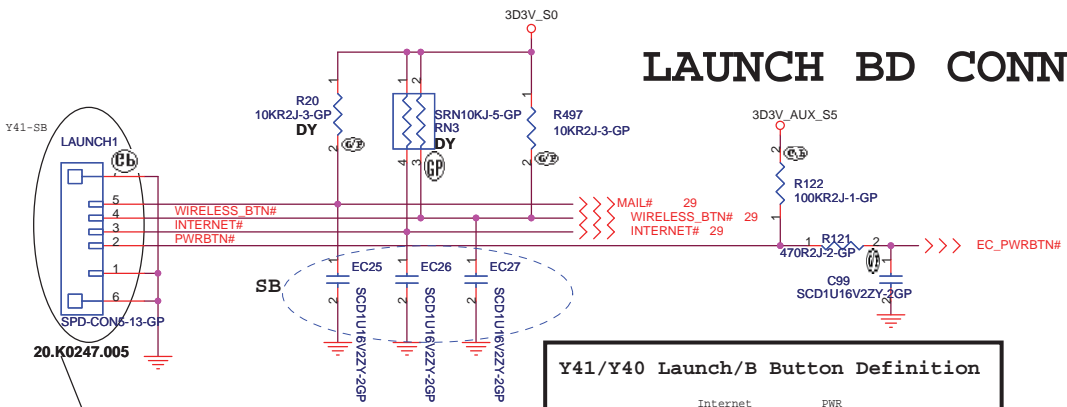


# Decoupling Capacitor

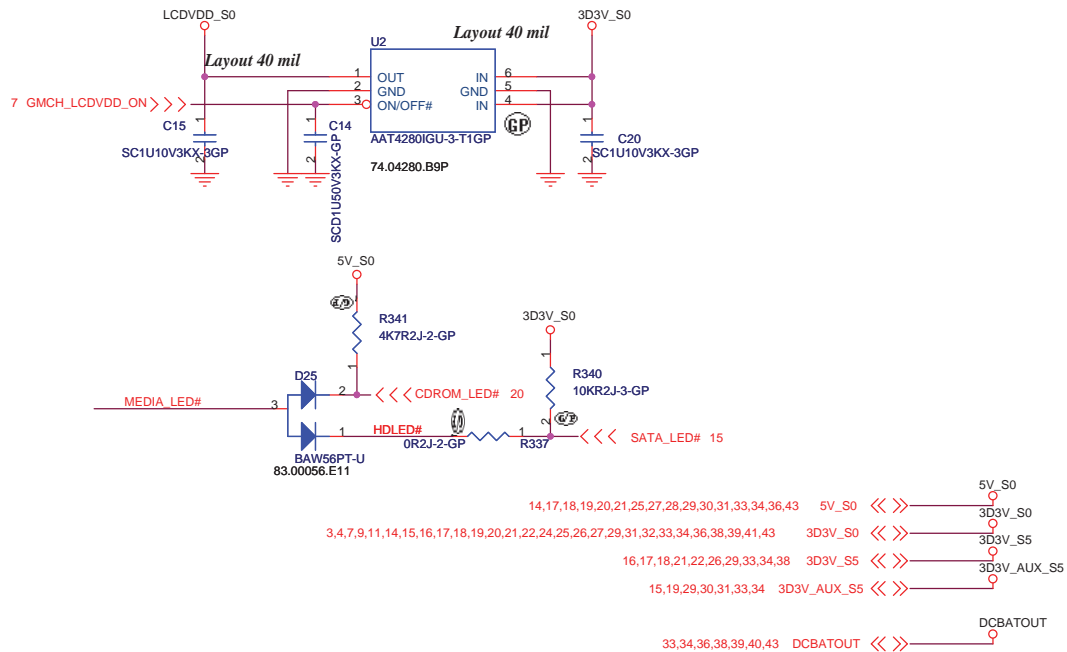
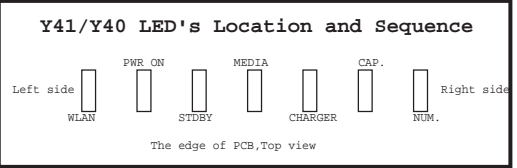
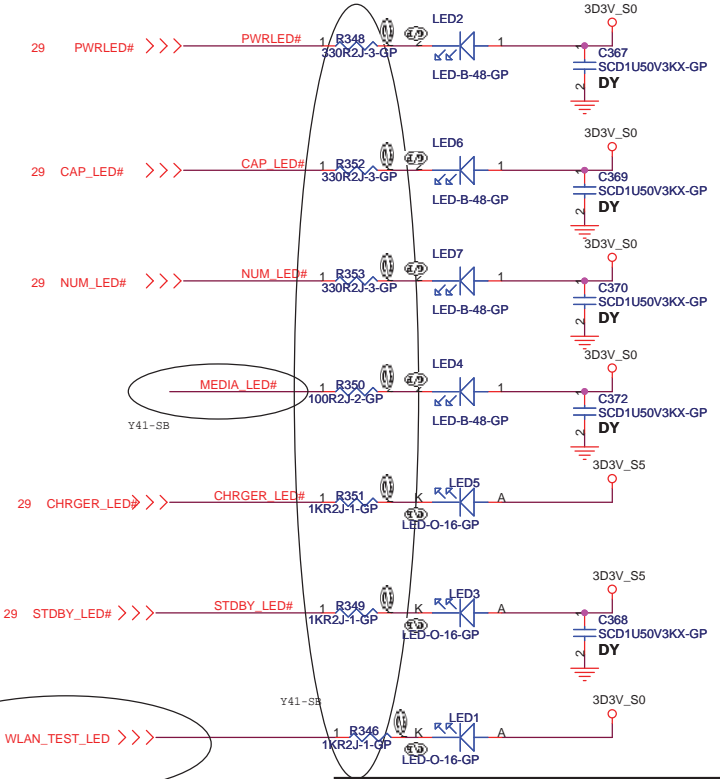


# LCD / INVERTER

## LAUNCH BD CONN



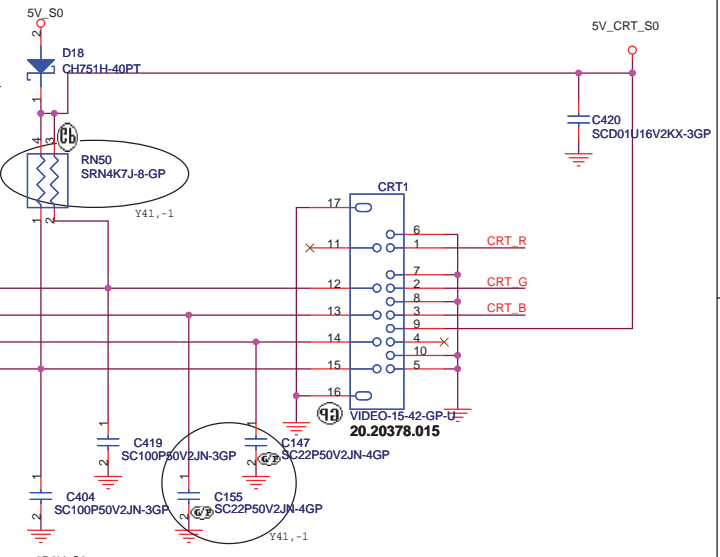
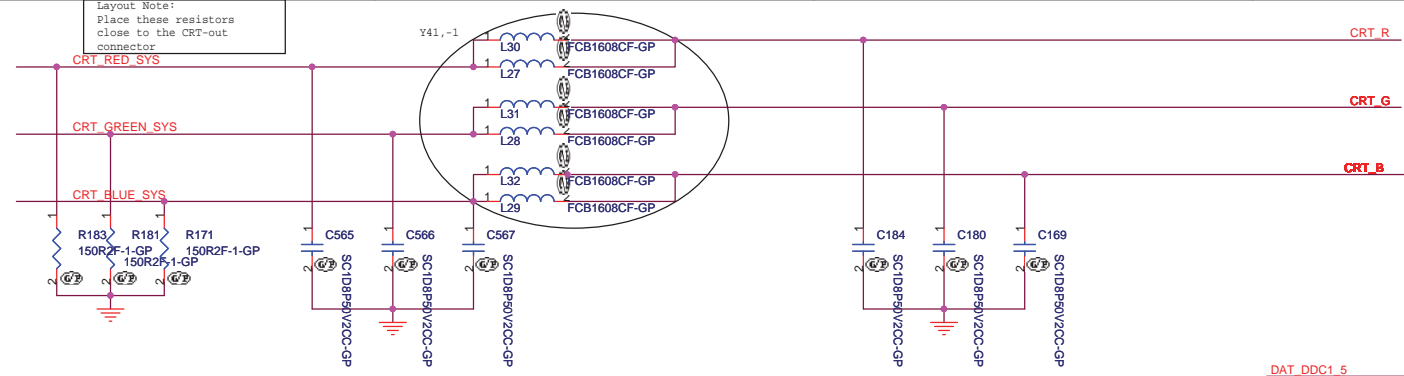
The pin1 of M/B side connects the pin5 of Launch/B side.



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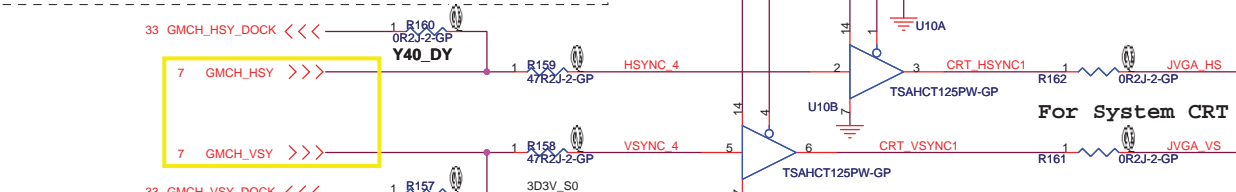
Title		LCD / LAUNCH / LEDs	
Size	Document Number	Y41/Y40	
Custom		Rev	-1
Date:	Wednesday, April 12, 2006	Sheet	13 of 44

# CRT I/F & CONNECTOR



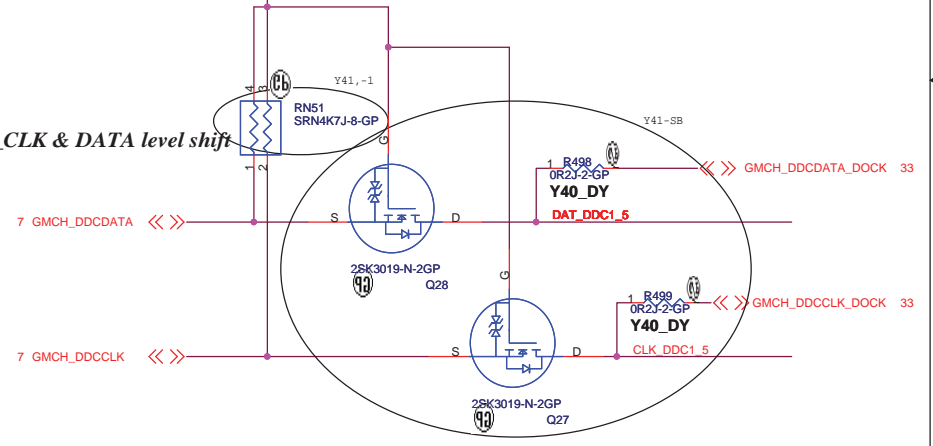
**Layout Note:**  
 Place these resistors close to the CRT-out connector  
 \* Must be a ground return path between this ground and the ground on the VGA connector.  
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## Hsync & Vsync level shift

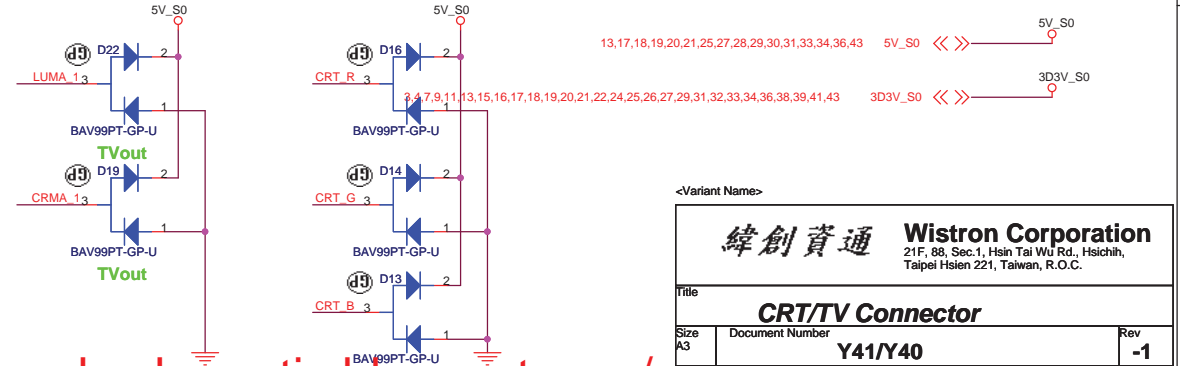
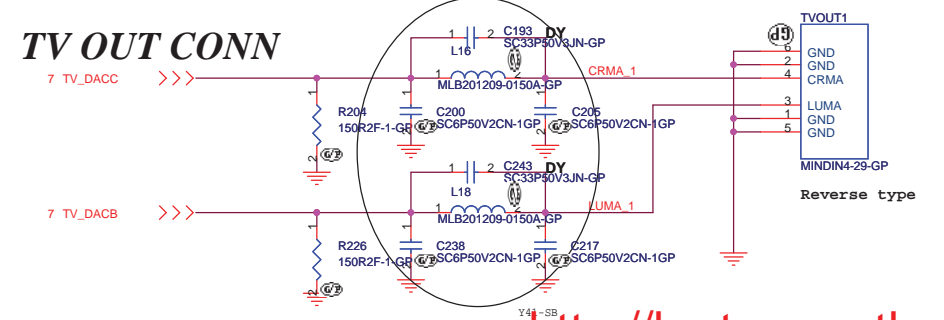


## For System CRT

## DDC\_CLK & DATA level shift



## TV OUT CONN



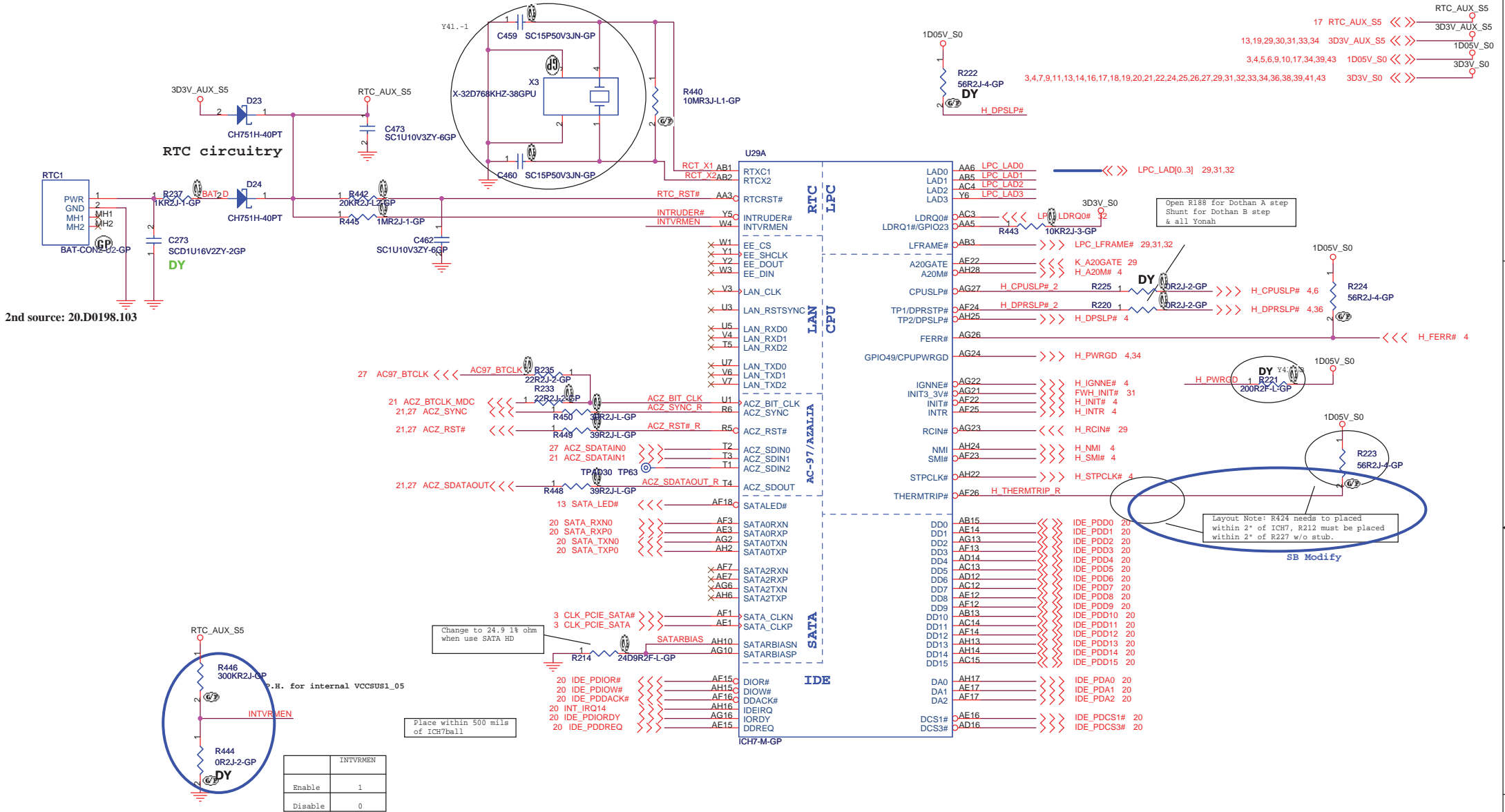
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**

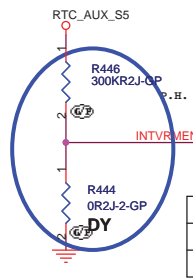
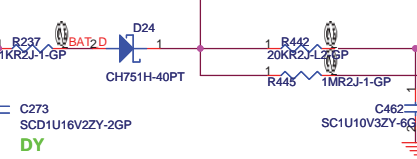
Size A3 Document Number **Y41/Y40** Rev **-1**

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2nd source: 20.D0198.103

**RTC circuitry**



	INTVREN
Enable	1
Disable	0

Placement Note:  
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

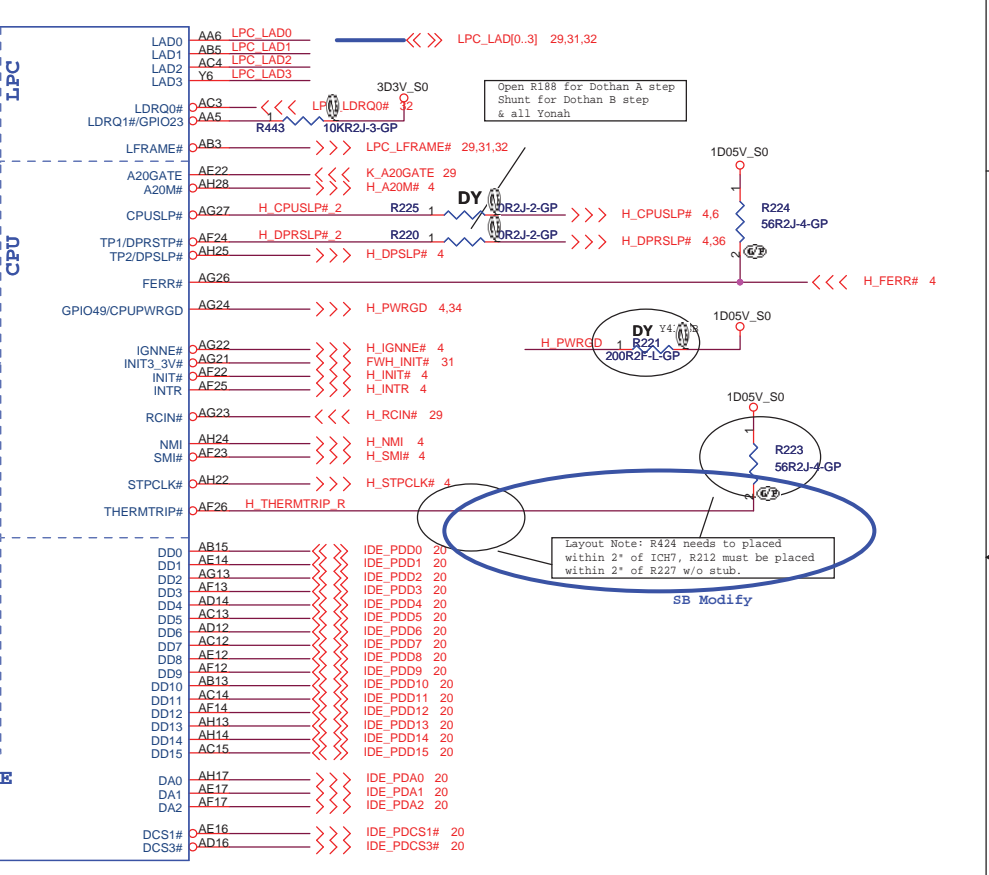
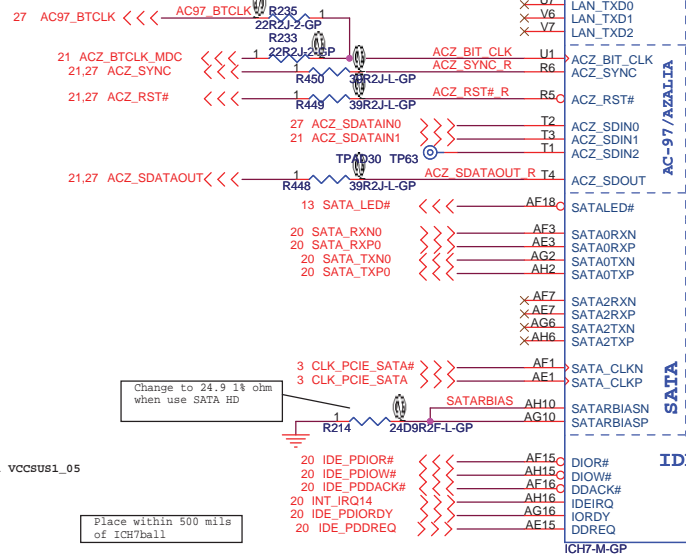
Change to 24.9 1% ohm when use SATA HD

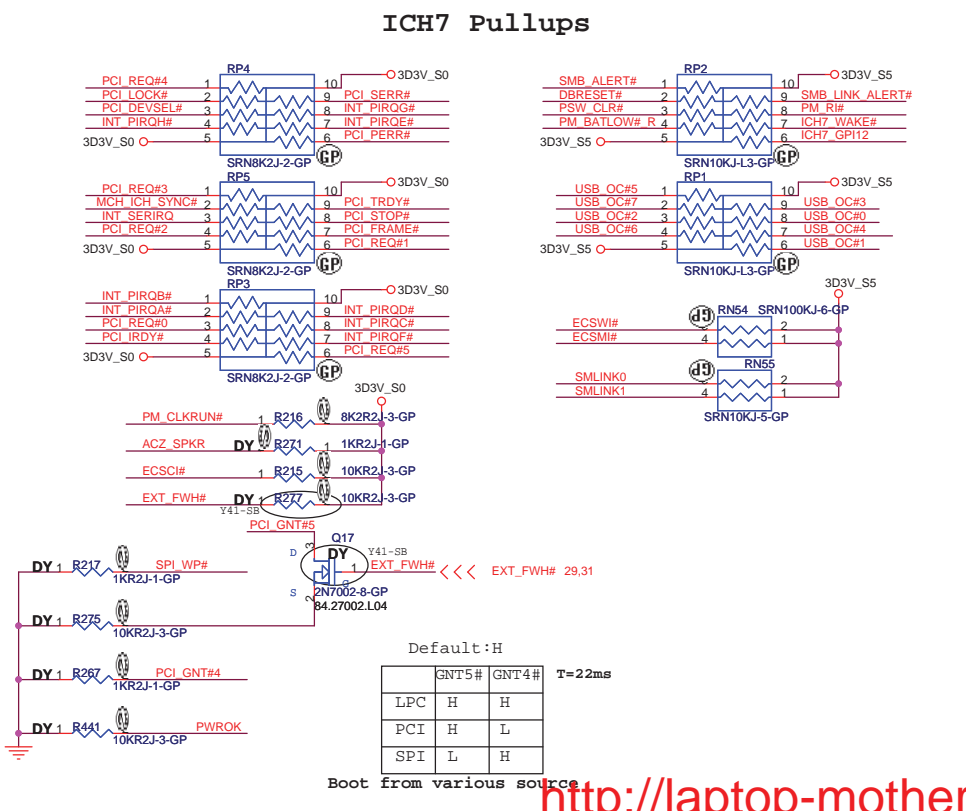
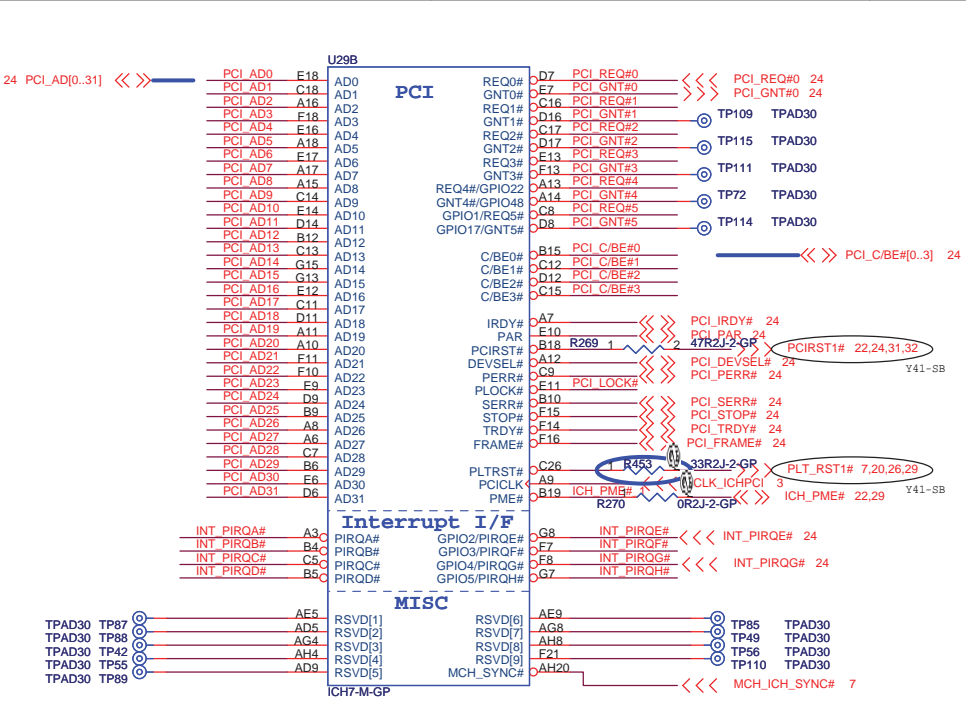
Place within 500 mils of ICH7ball

Open R188 for Dothan A step  
Shunt for Dothan B step & all Yonah

Layout Note: R424 needs to be placed within 2" of ICH7, R212 must be placed within 2" of R227 w/o stub.

SB Modify



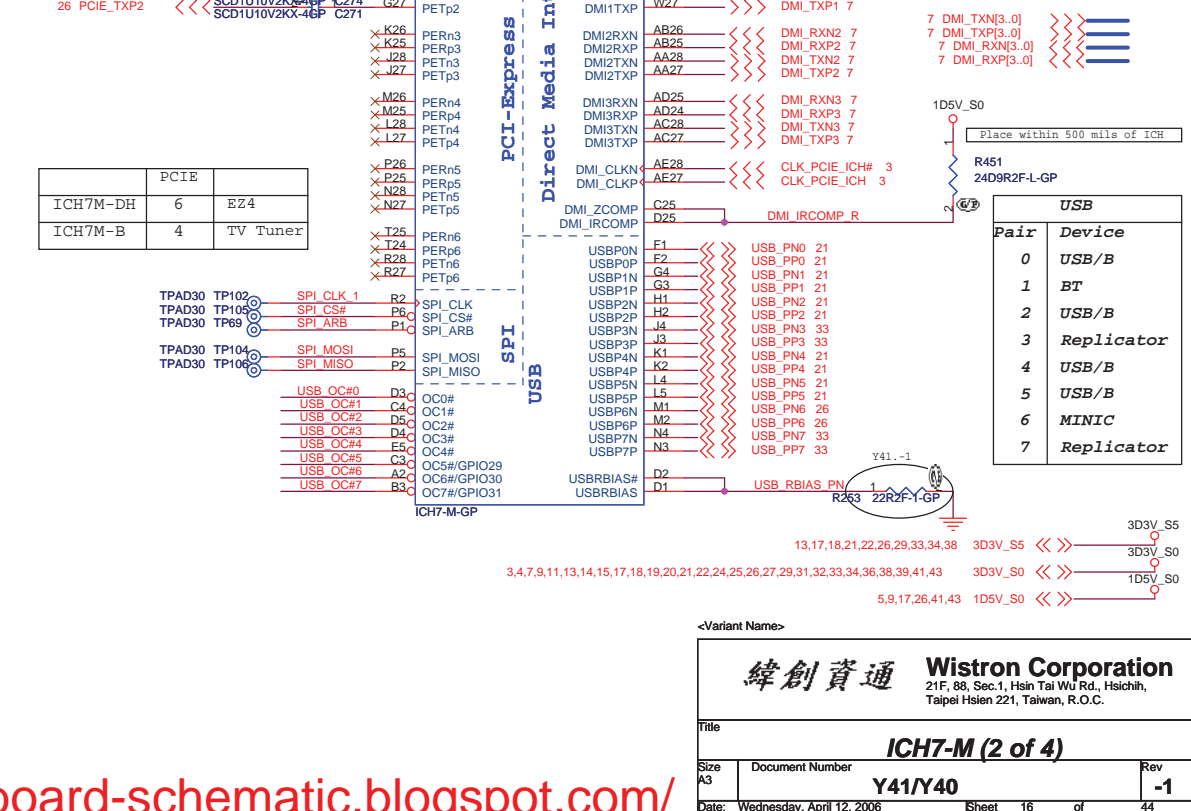
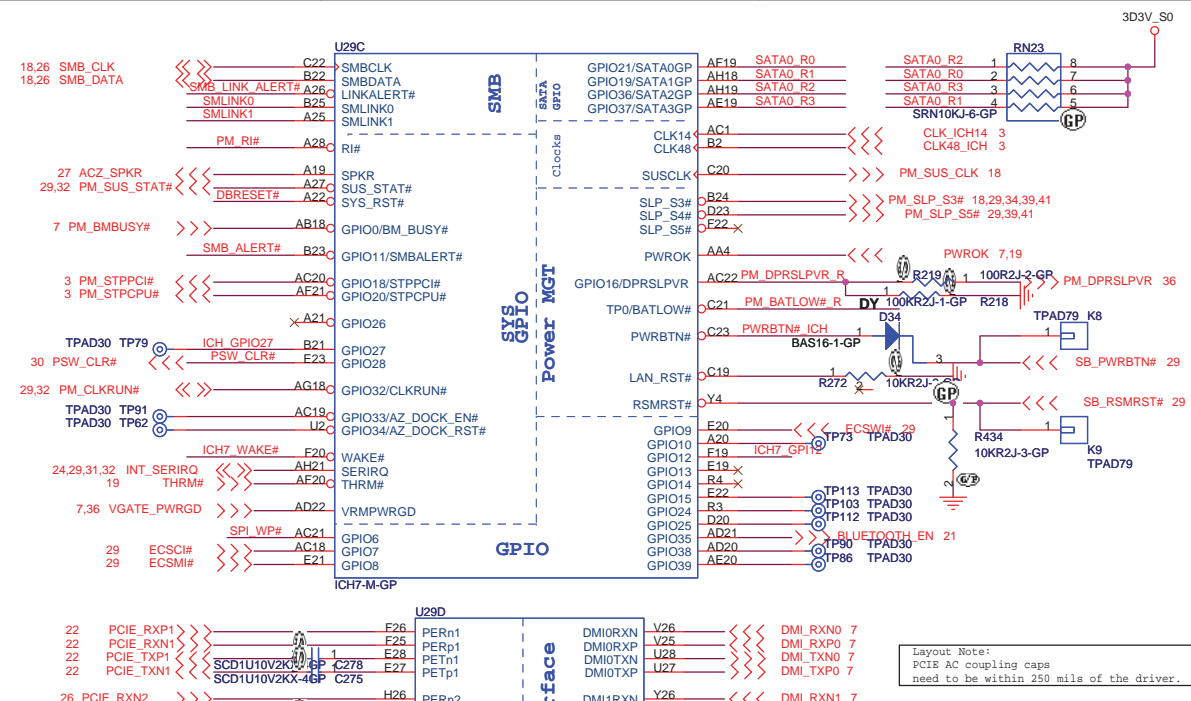


Default: H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

T=22ms

Boot from various sources



	PCIE	
ICH7M-DH	6	E24
ICH7M-B	4	TV Tuner

Layout Note:  
PCIE AC coupling caps  
need to be within 250 mils of the driver.

Pair	Device
0	USB/B
1	BT
2	USB/B
3	Replicator
4	USB/B
5	USB/B
6	MINIC
7	Replicator

<Variant Name>

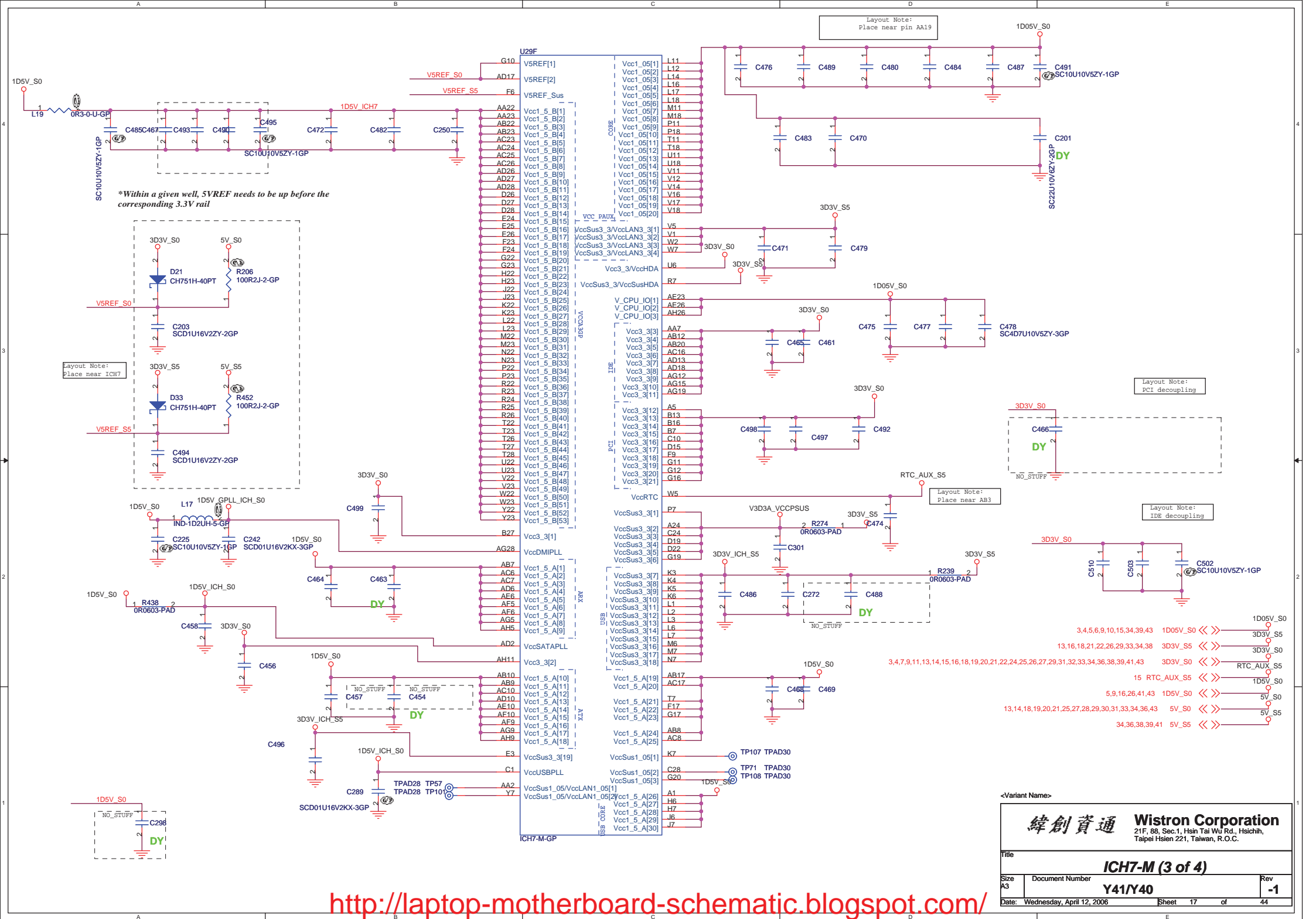
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (2 of 4)**

Size A3 Document Number **Y41/Y40** Rev **-1**

Date: Wednesday, April 12, 2006 Sheet 16 of 44





\*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note:  
Place near ICH7

Layout Note:  
PCI decoupling

Layout Note:  
Place near AB3

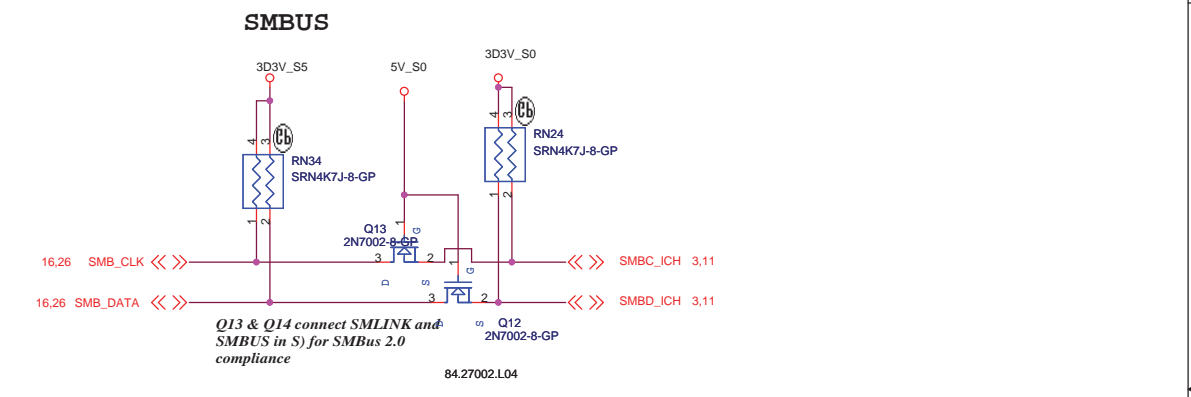
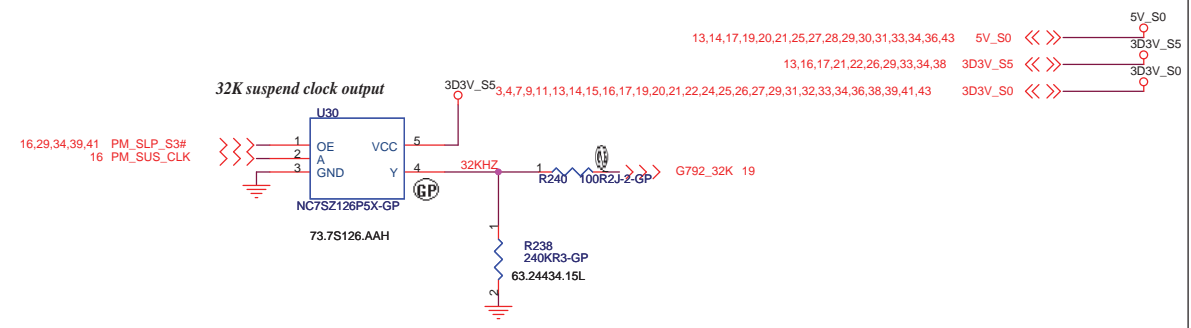
Layout Note:  
IDE decoupling

<Variant Name>  
**緯創資通** **Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>ICH7-M (3 of 4)</b>		
Size	Document Number	Rev
A3	<b>Y41/Y40</b>	<b>-1</b>
Date:	Wednesday, April 12, 2006	Sheet 17 of 44

U29E		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B26	VSS[9]	VSS[106]
B28	VSS[10]	VSS[107]
C2	VSS[11]	VSS[108]
C6	VSS[12]	VSS[109]
C27	VSS[13]	VSS[110]
D10	VSS[14]	VSS[111]
D13	VSS[15]	VSS[112]
D18	VSS[16]	VSS[113]
D21	VSS[17]	VSS[114]
D24	VSS[18]	VSS[115]
E1	VSS[19]	VSS[116]
E2	VSS[20]	VSS[117]
E4	VSS[21]	VSS[118]
E8	VSS[22]	VSS[119]
E15	VSS[23]	VSS[120]
F3	VSS[24]	VSS[121]
F4	VSS[25]	VSS[122]
F5	VSS[26]	VSS[123]
F12	VSS[27]	VSS[124]
F27	VSS[28]	VSS[125]
F28	VSS[29]	VSS[126]
G1	VSS[30]	VSS[127]
G2	VSS[31]	VSS[128]
G5	VSS[32]	VSS[129]
G6	VSS[33]	VSS[130]
G9	VSS[34]	VSS[131]
G14	VSS[35]	VSS[132]
G18	VSS[36]	VSS[133]
G21	VSS[37]	VSS[134]
G24	VSS[38]	VSS[135]
G25	VSS[39]	VSS[136]
G26	VSS[40]	VSS[137]
H3	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J2	VSS[48]	VSS[145]
J5	VSS[49]	VSS[146]
J24	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
J26	VSS[52]	VSS[149]
K24	VSS[53]	VSS[150]
K27	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
N26	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P17	VSS[95]	VSS[192]
P24	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]

ICH7-M-GP



<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

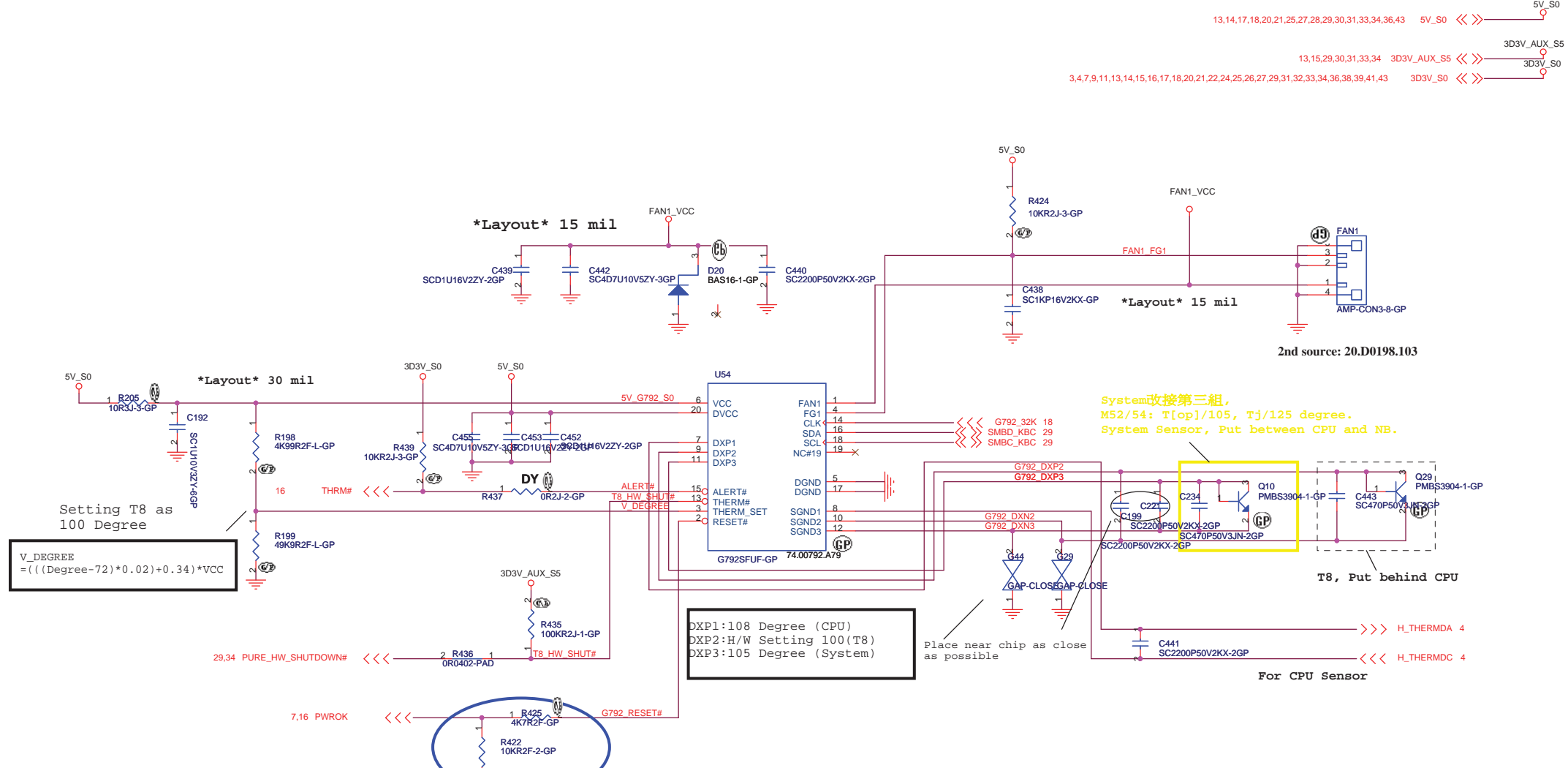
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)/ODD**

Size A3	Document Number <b>Y41/Y40</b>	Rev <b>-1</b>
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Date: Wednesday, April 12, 2006 Sheet 18 of 44

13,14,17,18,20,21,25,27,28,29,30,31,33,34,36,43 5V\_S0 <<<  
 3D3V\_AUX\_S5 <<<  
 3D3V\_S0 <<<  
 3,4,7,9,11,13,14,15,16,17,18,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V\_S0 <<<



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

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<Variant Name>

**緯創資通 Wistron Corporation**  
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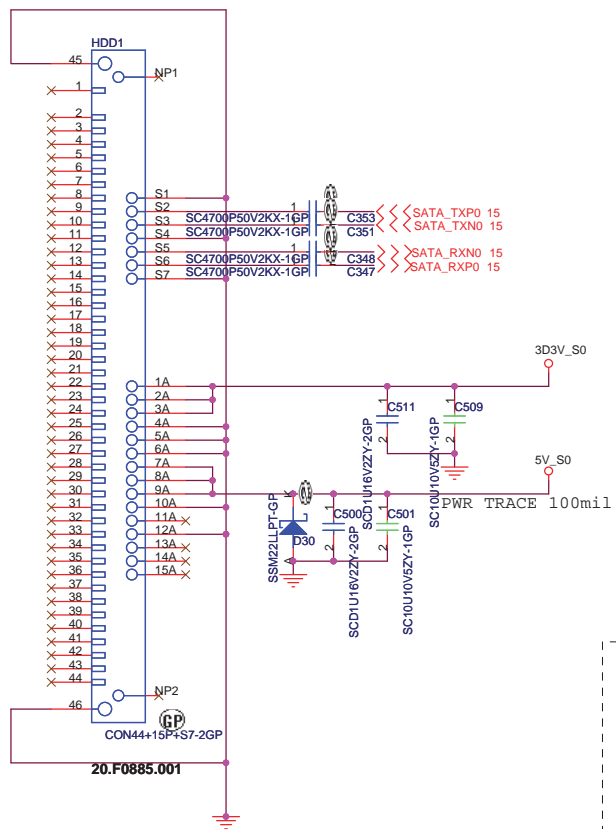
Title  
**Thermal/Fan Controller G792**

Size Custom Document Number  
**Y41/Y40**

Date: Wednesday, April 12, 2006 Sheet 19 of 44

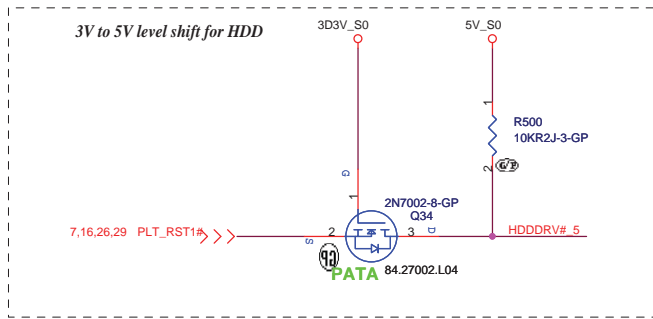
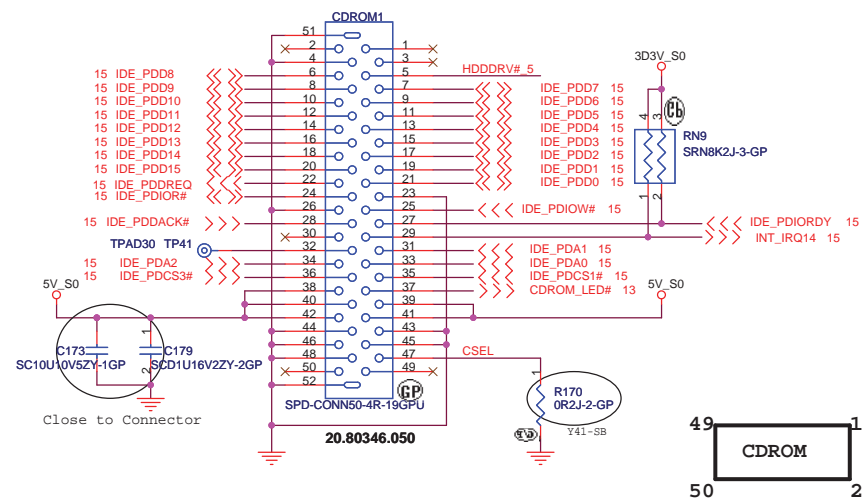
Rev **-1**

# SATA Connector



<http://laptop-motherboard-schematic.blogspot.com/>

# CDROM Connector



<Variant Name>

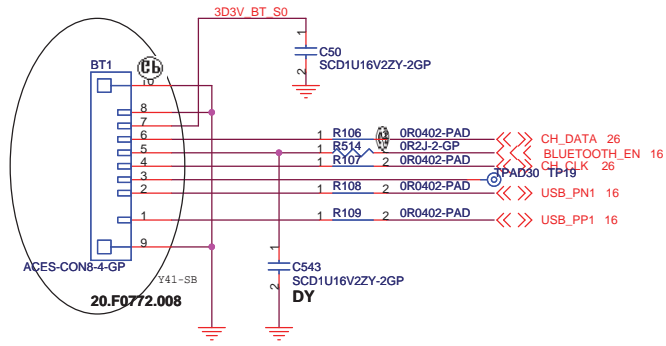
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SATA/PATA HDD ULi-M5285**

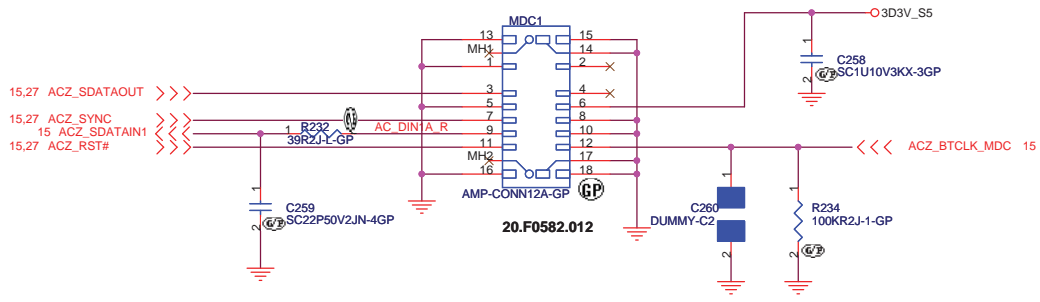
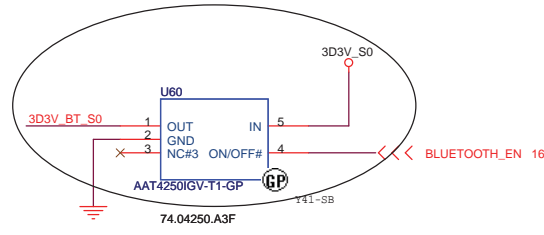
Size A3 Document Number **Y41/Y40** Rev **-1**

Date: Wednesday, April 12, 2006 Sheet 20 of 44

13,16,17,18,22,26,29,33,34,38 3D3V\_S5 <<>>  
 3,4,7,9,11,13,14,15,16,17,18,19,20,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V\_S0 <<>>  
 13,14,17,18,19,20,25,27,28,29,30,31,33,34,36,43 5V\_S0 <<>>

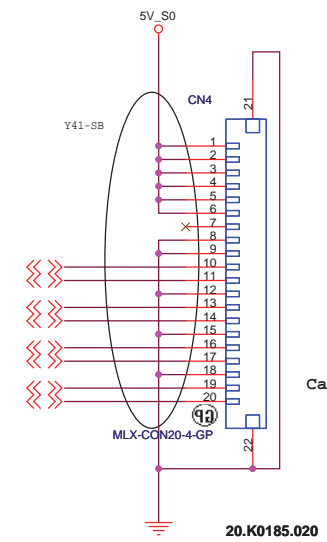


**MDC 1.5 CONN**



**USB PORT**

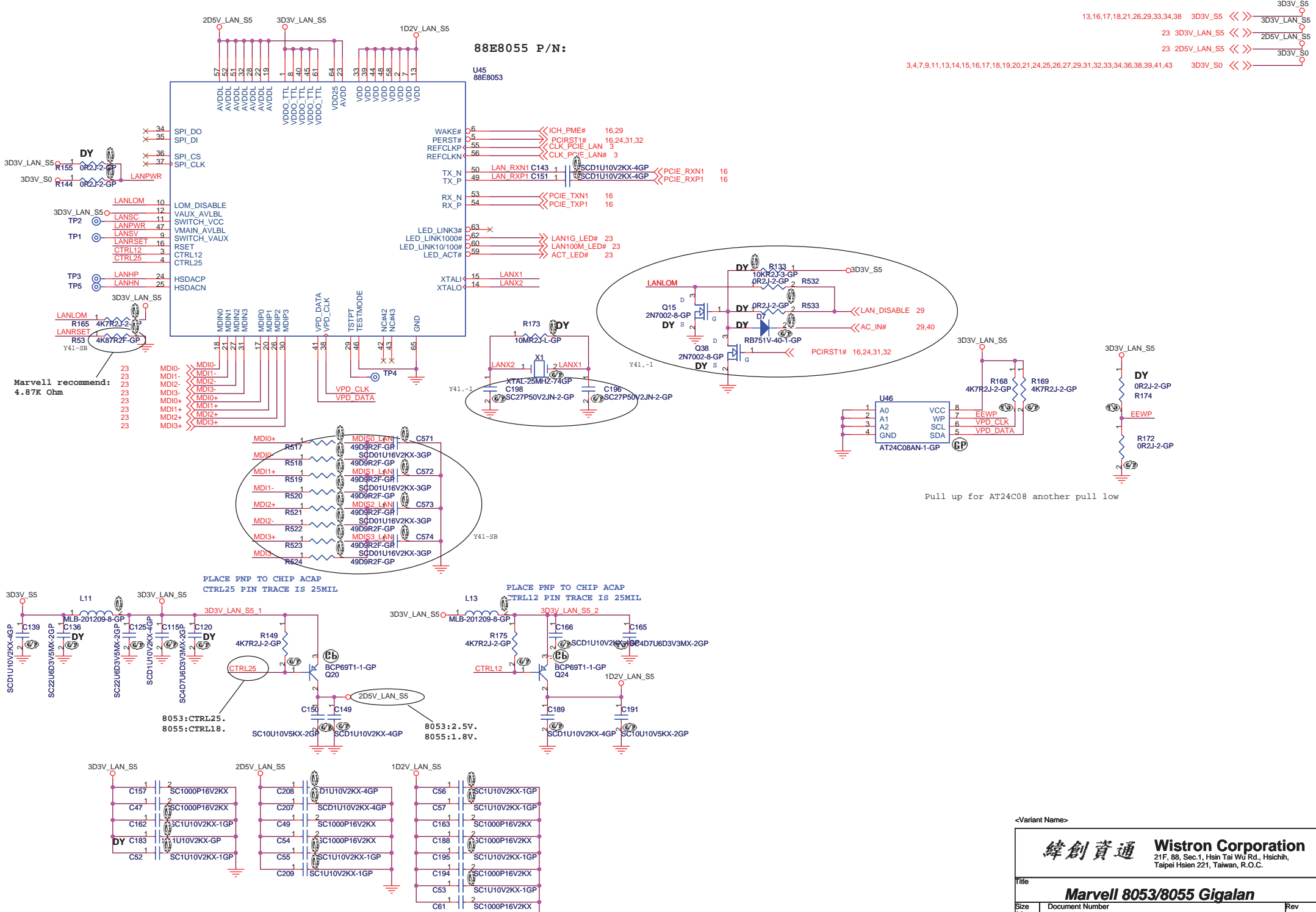
- 16 USB\_PN0
- 16 USB\_PP0
- 16 USB\_PN2
- 16 USB\_PP2
- 16 USB\_PN4
- 16 USB\_PP4
- 16 USB\_PN5
- 16 USB\_PP5



Cable length = 120mm.

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB and MDC I/F</b>			
Size A3	Document Number <b>Y41/Y40</b>	Rev <b>-1</b>	
Date: Wednesday, April 12, 2006	Sheet 21	of	44



88E8055 P/N:

U45  
88E8053

3D3V\_S5 <<>> 3D3V\_LAN\_S5  
 23 3D3V\_LAN\_S5 <<>> 2D5V\_LAN\_S5  
 23 2D5V\_LAN\_S5 <<>> 3D3V\_S0  
 3.4,7,9,11,13,14,15,16,17,18,19,20,21,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V\_S0 <<>>

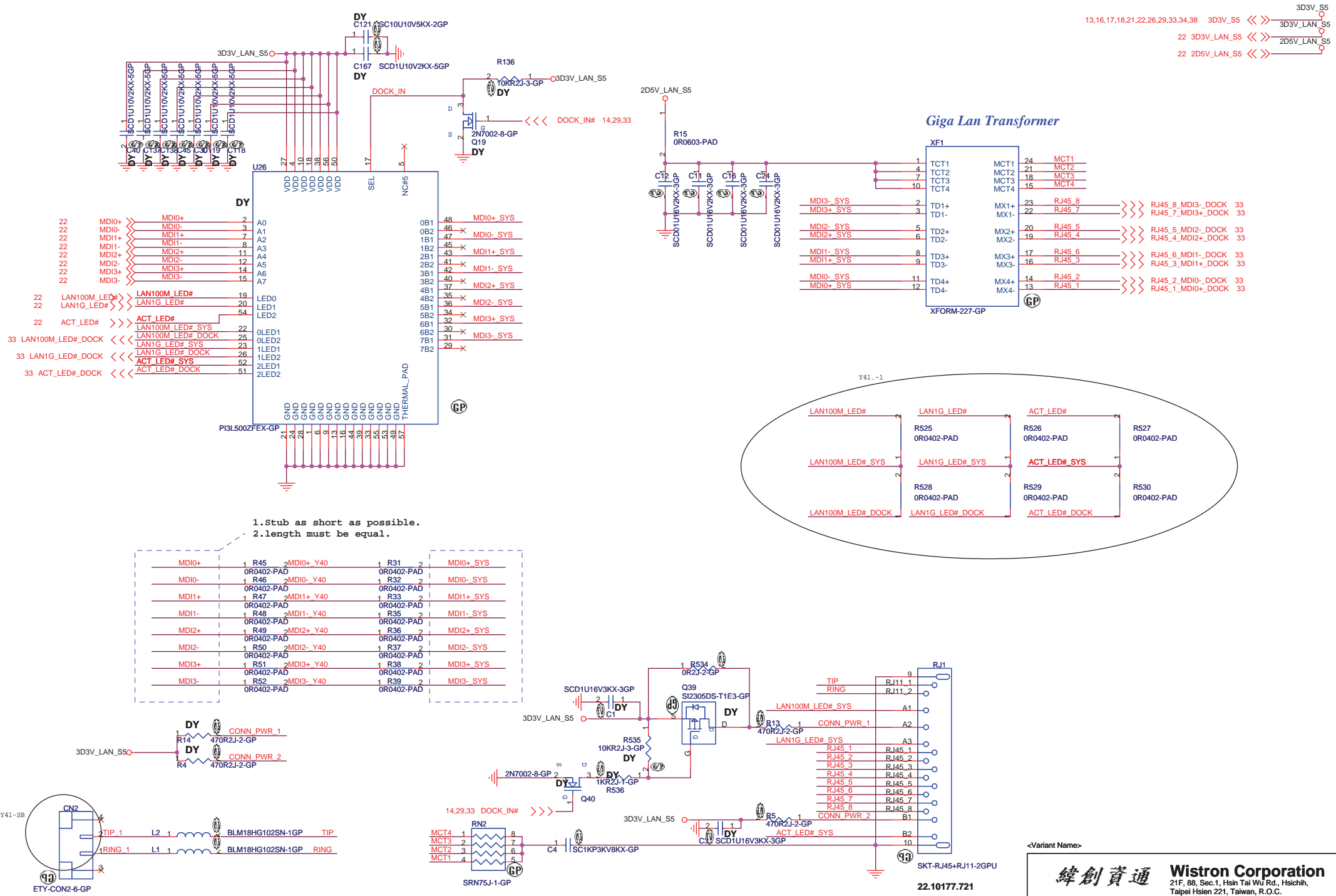
Marvell recommend:  
4.87K Ohm

Pull up for AT24C08 another pull low

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Marvell 8053/8055 Gigalan</b>			
Title			
Size A3	Document Number	Y41/Y40	
Date: Friday, May 26, 2006	Sheet 22	of	44

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1. Stub as short as possible.  
2. length must be equal.

MDIO+	1 R45	2 MDIO+ Y40	1 R31	2 MDIO+ SYS
MDIO-	1 R46	2 MDIO- Y40	1 R32	2 MDIO- SYS
MDI1+	1 R47	2 MDI1+ Y40	1 R33	2 MDI1+ SYS
MDI1-	1 R48	2 MDI1- Y40	1 R35	2 MDI1- SYS
MDI2+	1 R49	2 MDI2+ Y40	1 R36	2 MDI2+ SYS
MDI2-	1 R50	2 MDI2- Y40	1 R37	2 MDI2- SYS
MDI3+	1 R51	2 MDI3+ Y40	1 R38	2 MDI3+ SYS
MDI3-	1 R52	2 MDI3- Y40	1 R39	2 MDI3- SYS

3D3V\_S5 <<< 3D3V\_LAN\_S5  
22 3D3V\_LAN\_S5 <<< 2D5V\_LAN\_S5  
22 2D5V\_LAN\_S5 <<<

### Giga Lan Transformer

TCT1	MCT1	24	MCT1
TCT2	MCT2	21	MCT2
TCT3	MCT3	18	MCT3
TCT4	MCT4	15	MCT4

23	RJ45_8	8	RJ45_8 MDI3- DOCK	33
22	RJ45_7	7	RJ45_7 MDI3+ DOCK	33
20	RJ45_5	5	RJ45_5 MDI2- DOCK	33
19	RJ45_4	4	RJ45_4 MDI2+ DOCK	33
17	RJ45_6	6	RJ45_6 MDI1- DOCK	33
16	RJ45_3	3	RJ45_3 MDI1+ DOCK	33
14	RJ45_2	2	RJ45_2 MDI0- DOCK	33
13	RJ45_1	1	RJ45_1 MDI0+ DOCK	33

LAN100M_LED#	LAN1G_LED#	ACT_LED#
R525	R526	R527
OR0402-PAD	OR0402-PAD	OR0402-PAD
LAN100M_LED#_SYS	LAN1G_LED#_SYS	ACT_LED#_SYS
R528	R529	R530
OR0402-PAD	OR0402-PAD	OR0402-PAD
LAN100M_LED#_DOCK	LAN1G_LED#_DOCK	ACT_LED#_DOCK

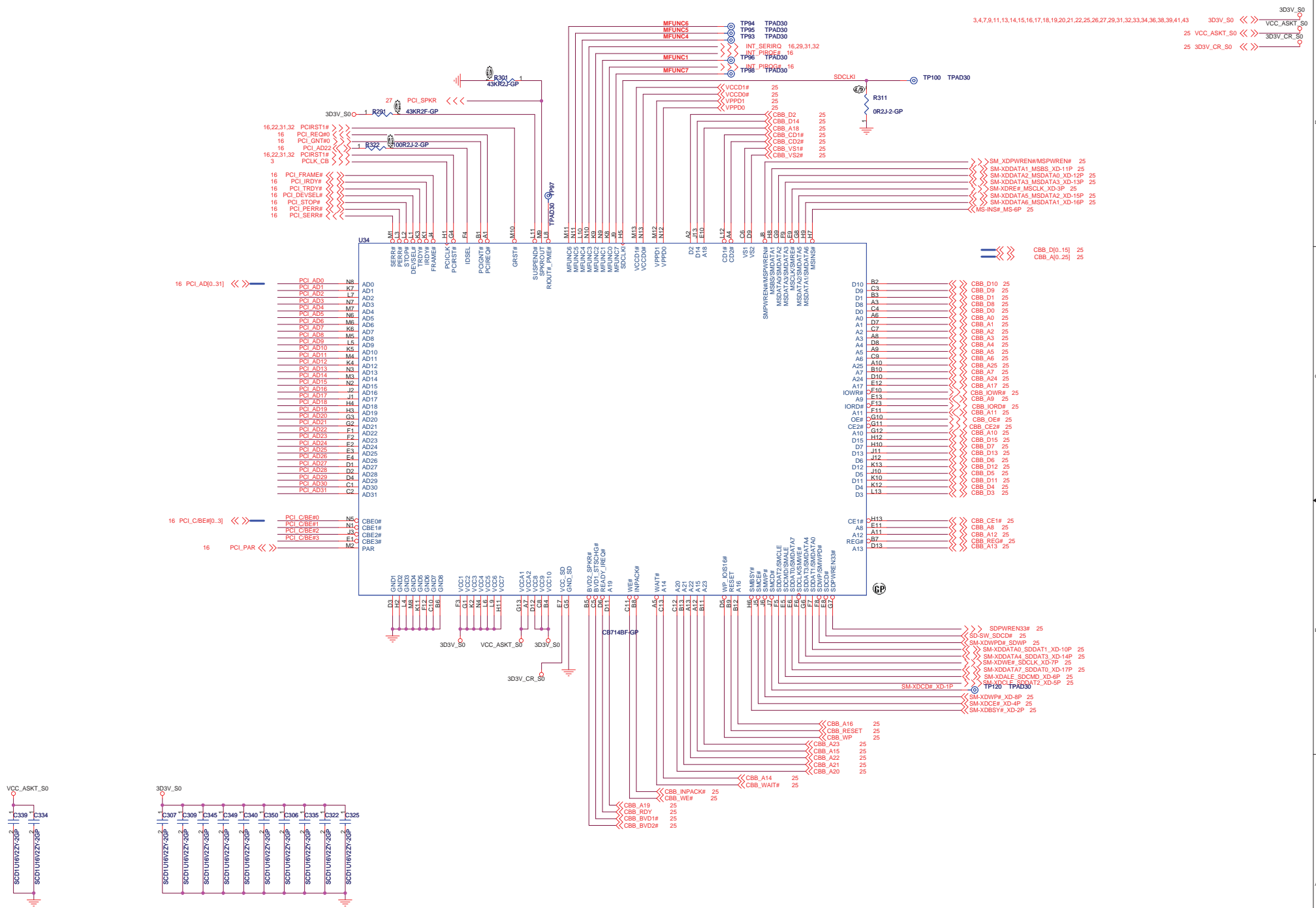
MDIO+	1 R45	2 MDIO+ Y40	1 R31	2 MDIO+ SYS
MDIO-	1 R46	2 MDIO- Y40	1 R32	2 MDIO- SYS
MDI1+	1 R47	2 MDI1+ Y40	1 R33	2 MDI1+ SYS
MDI1-	1 R48	2 MDI1- Y40	1 R35	2 MDI1- SYS
MDI2+	1 R49	2 MDI2+ Y40	1 R36	2 MDI2+ SYS
MDI2-	1 R50	2 MDI2- Y40	1 R37	2 MDI2- SYS
MDI3+	1 R51	2 MDI3+ Y40	1 R38	2 MDI3+ SYS
MDI3-	1 R52	2 MDI3- Y40	1 R39	2 MDI3- SYS

20.F0736.002

22.10177.721

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Taipei Hsien 221, Taiwan, R.O.C.

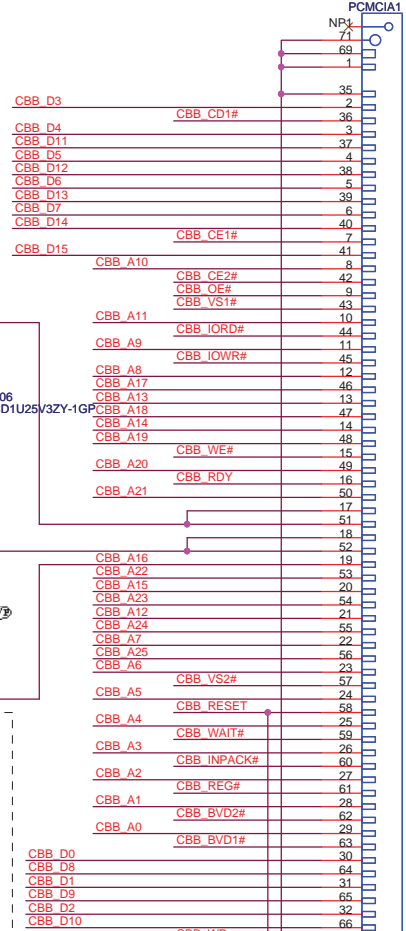
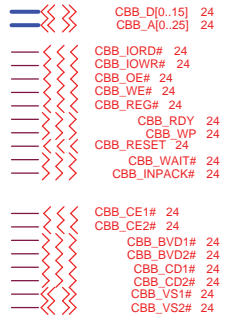
Title: **LAN Connector**  
Size A3 Document Number: **Y41/Y40** Rev: **-1**  
Date: Wednesday, April 12, 2006 Sheet 23 of 44



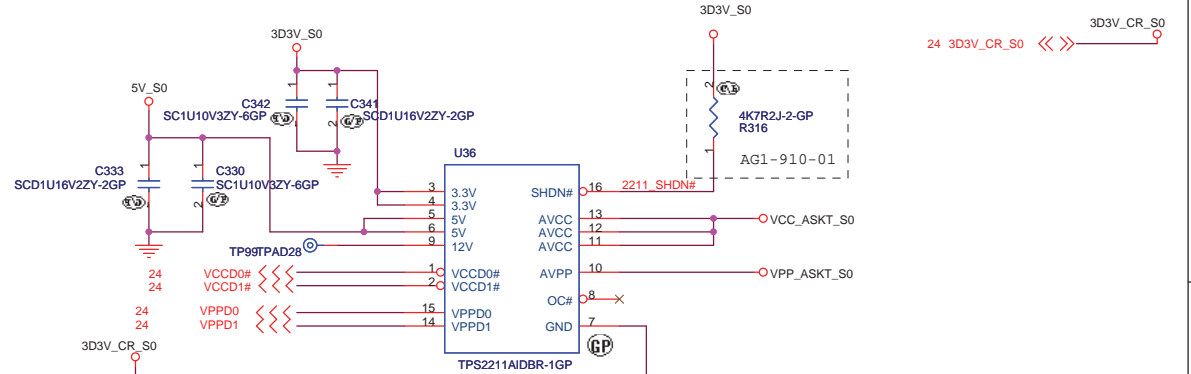


Cardbus I/F

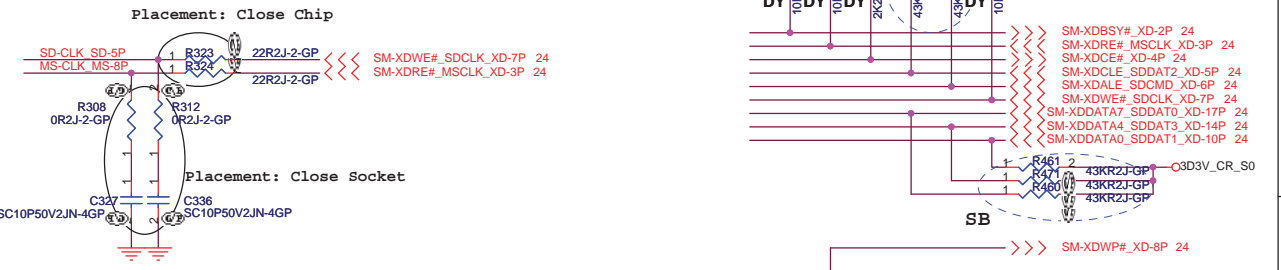
PCMCIA Socket



ENE Power switch

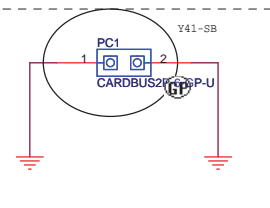


Cardreader P/N: 20.I0033.011



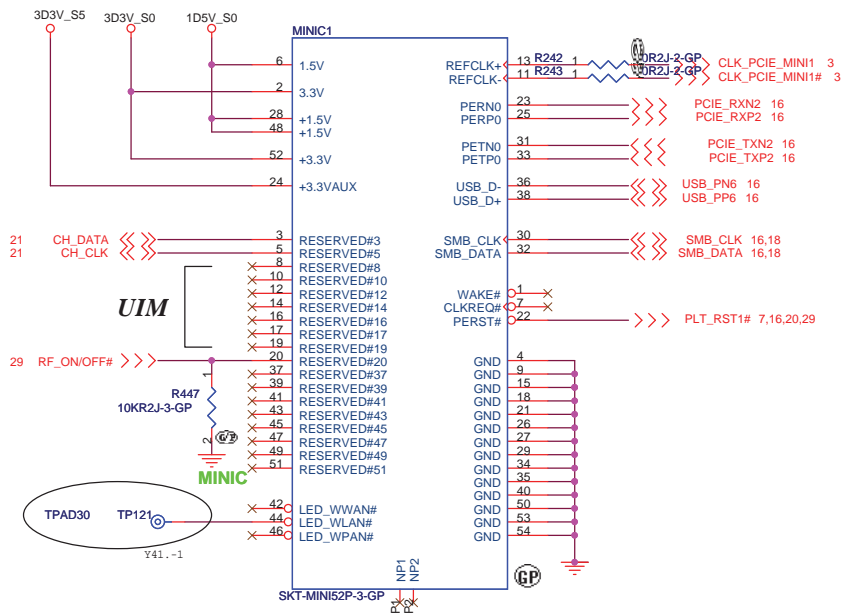
Place close to pin 19.  
C320 DUMMY-C2

Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F

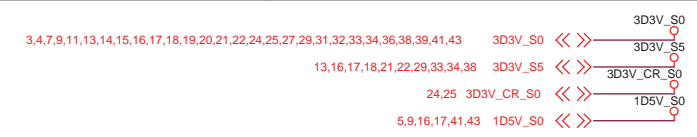
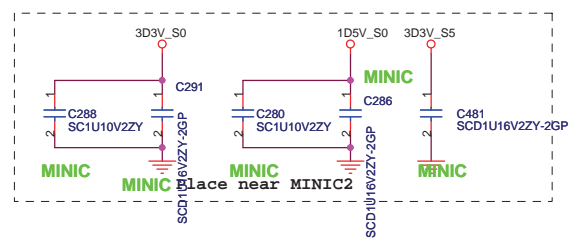


Wistron Corporation logo and contact information. Includes title 'PCMCIA/CardReader', document number 'Y41/Y40', date 'Wednesday, April 12, 2006', and sheet information '25 of 44'.

# Mini Card Connector

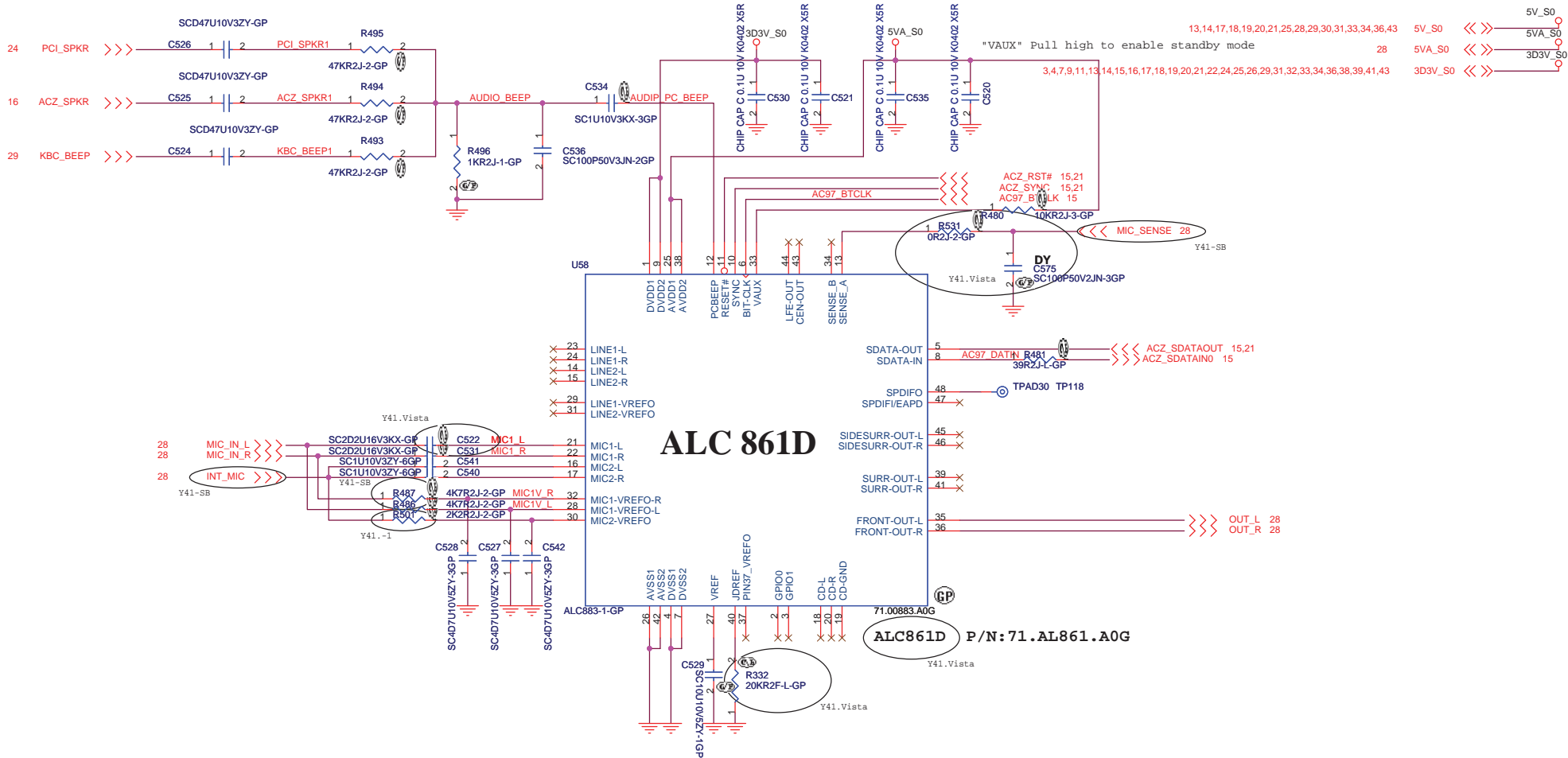


MINIC  
Change part to P/N:62.10043.241



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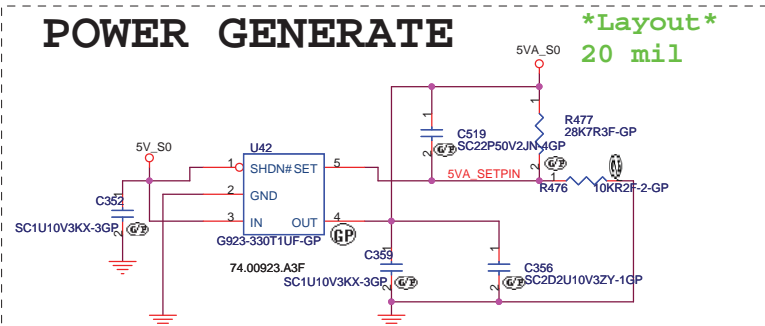
<Variant Name>		
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>MINI CARD</b>		
Title	Document Number	Rev
Size A3	<b>Y41/Y40</b>	<b>-1</b>
Date: Wednesday, April 12, 2006	Sheet 26 of 44	



- 1) When GPIO0 is asserted, AMP should be muted.
- 2) SPDIFO should be turned off when not used.

**Configuration:**  
 (3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.)

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

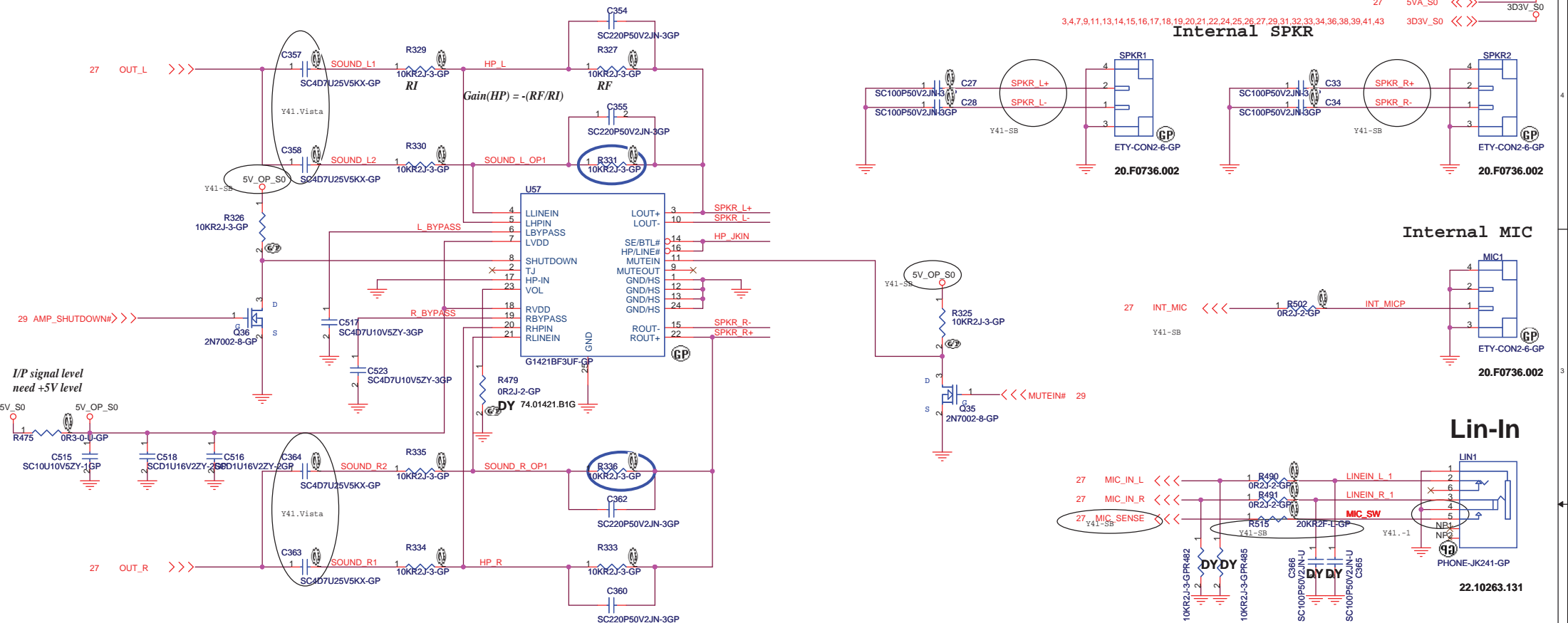
Title: **Azalia codec ALC861**

Size A3	Document Number	Rev
	<b>Y41/Y40</b>	<b>-1</b>

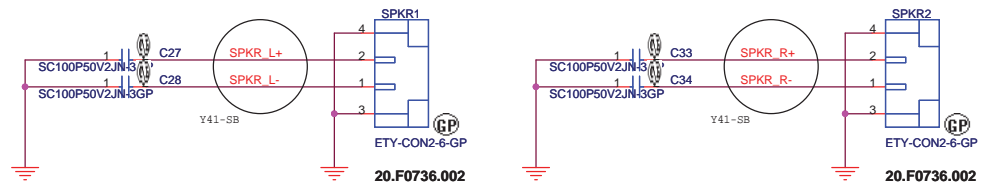
Date: Thursday, November 02, 2006 Sheet 27 of 44

# AUDIO OP AMPLIFIER

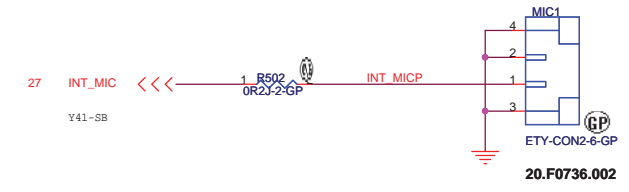
13,14,17,18,19,20,21,25,27,29,30,31,33,34,36,43 5V\_S0 <<>>  
 27 5VA\_S0 <<>>  
 3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V\_S0 <<>>



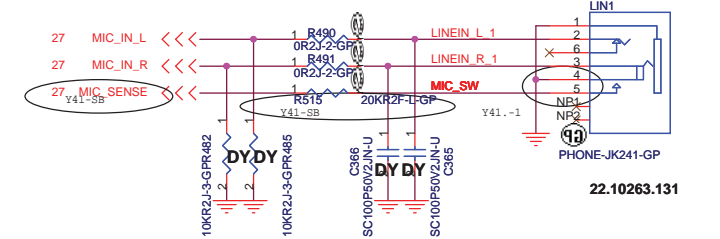
## Internal SPKR



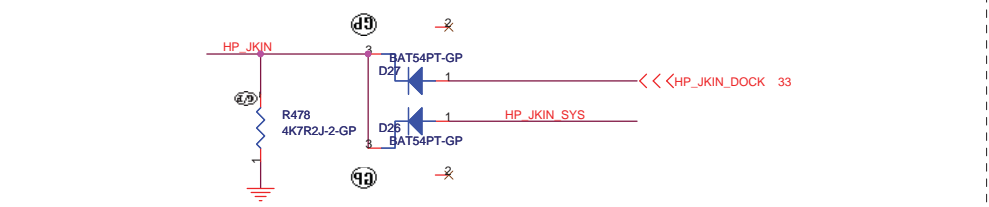
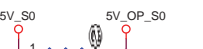
## Internal MIC



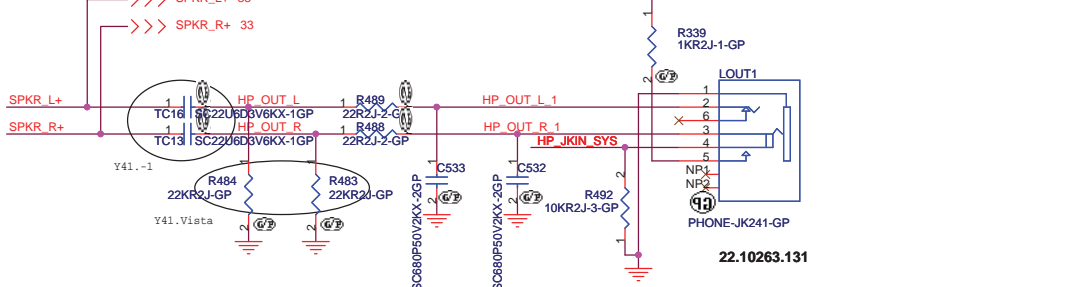
## Lin-In



I/P signal level need +5V level



## Line-Out

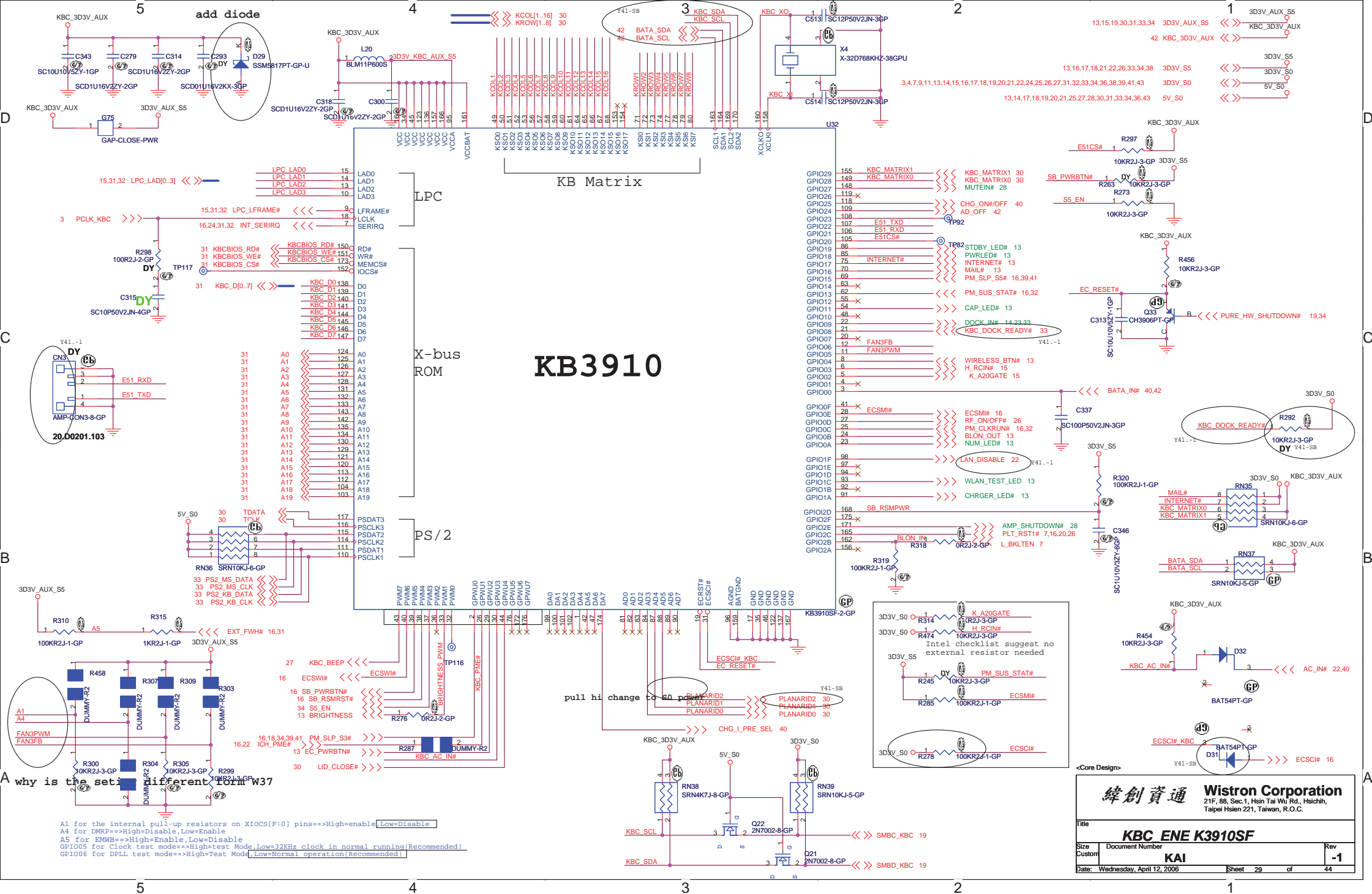


<Variant Name>

**緯創資通 Wistron Corporation**  
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Title **Audio AMP G1421B / Jack**

Size A3	Document Number <b>Y41/Y40</b>	Rev <b>-1</b>
Date: Thursday, November 02, 2006	Sheet 28	of 44



**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiachih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC ENE K3910SF**

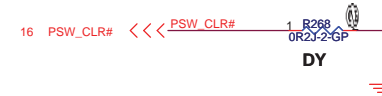
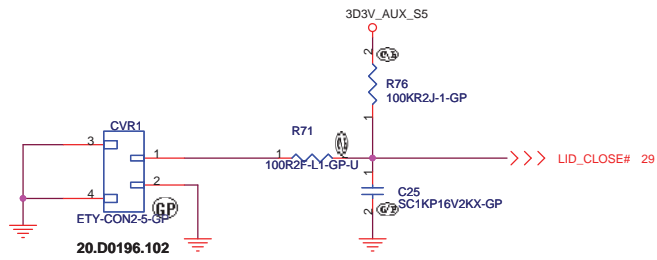
Size: Document Number  
Custom: **KAI** Rev: **-1**

Date: Wednesday, April 12, 2006 Sheet 29 of 44

13,15,19,29,31,33,34 3D3V\_AUX\_S5 <<< 5V\_S0 <<<  
 13,14,17,18,19,20,21,25,27,28,29,31,33,34,36,43 5V\_S0 <<<

# Internal KeyBoard Connector

## COVER SWITCH

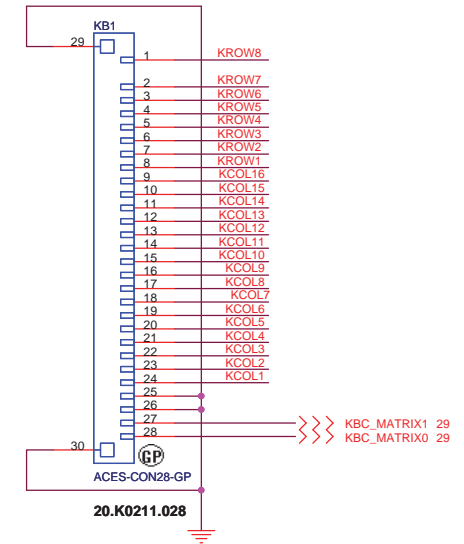


Keyboard matrix ( from vendor )

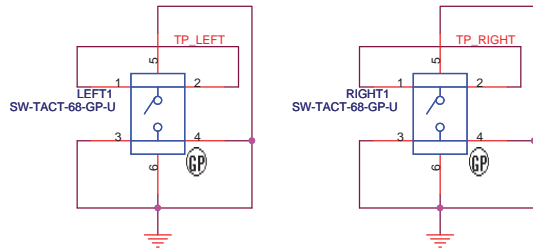
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

PSW_CLR#	Low Active
	1 - 5 ON

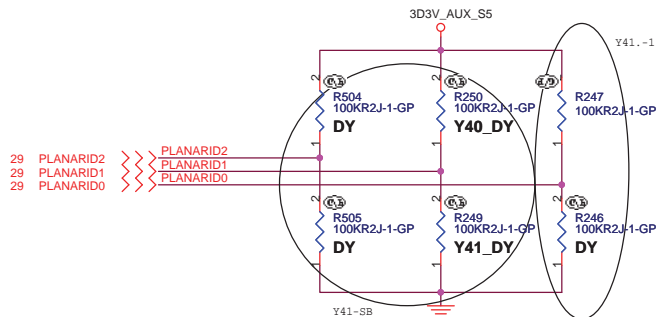
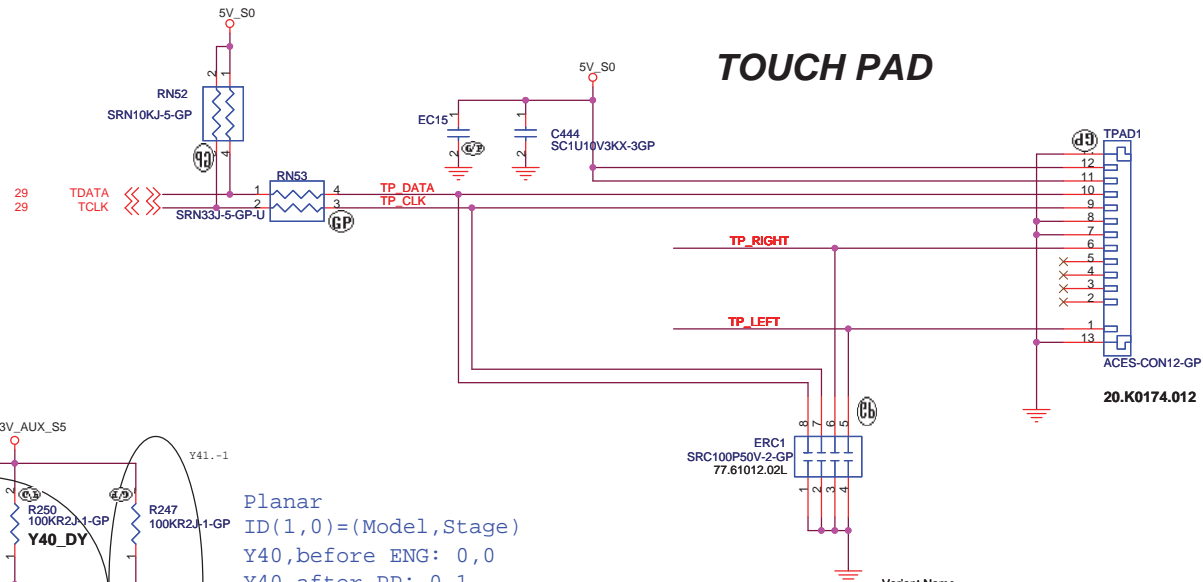
29 KROW[1..8] <<<  
 29 KCOL[1..16] <<<



## SCROLL KEY



## TOUCH PAD



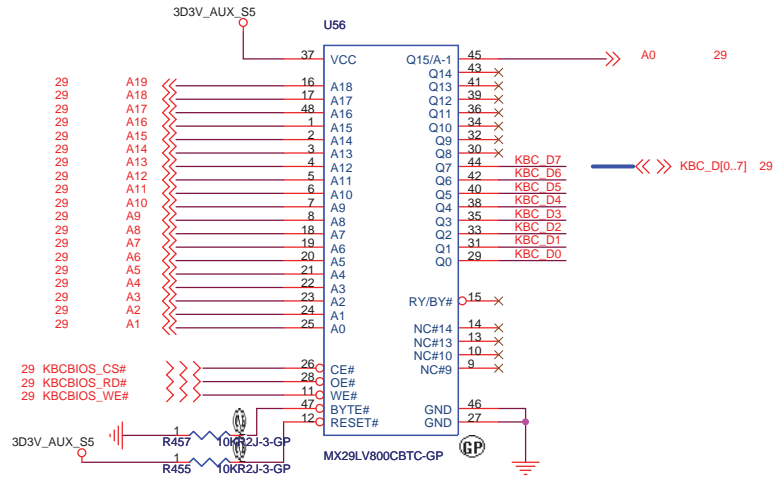
Planar  
 ID(1,0)=(Model,Stage)  
 Y40,before ENG: 0,0  
 Y40,after PP: 0,1  
 Y41,before ENG: 1,0  
 Y41,after PP: 1,1

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 Taipei Hsien 221, Taiwan, R.O.C.

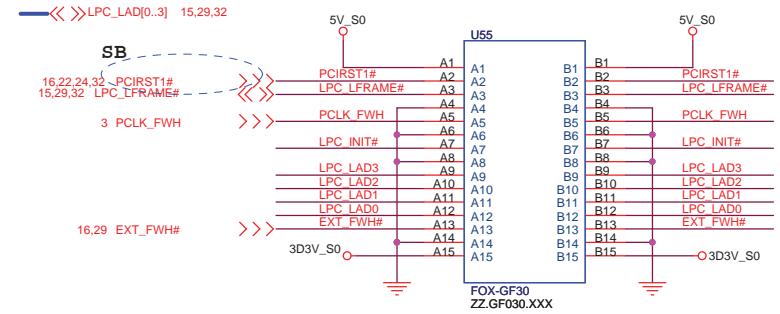
Title: **KEYBOARD/TOUCHPAD**

Size A3 Document Number **Y41/Y40** Rev **-1**

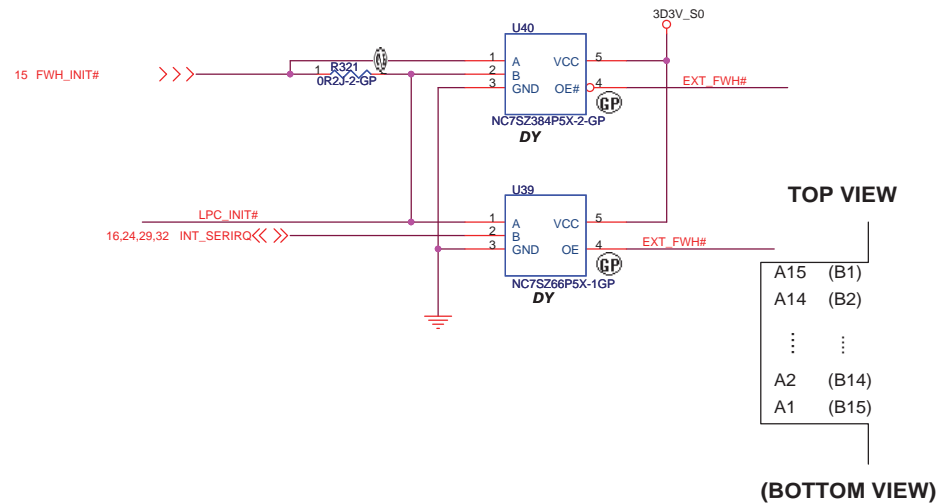
Date: Wednesday, April 12, 2006 Sheet 30 of 44

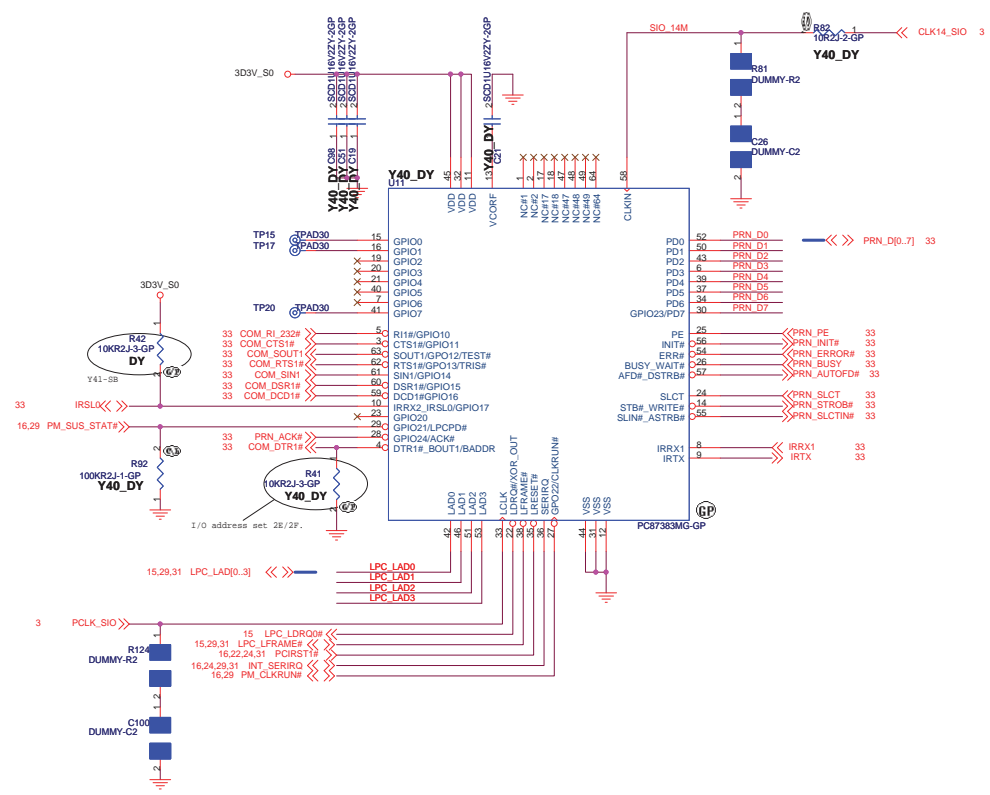


### GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000  
 Has internal pull-down resistors  
 All may be left floated  
 FPET7 Elec. P3-46



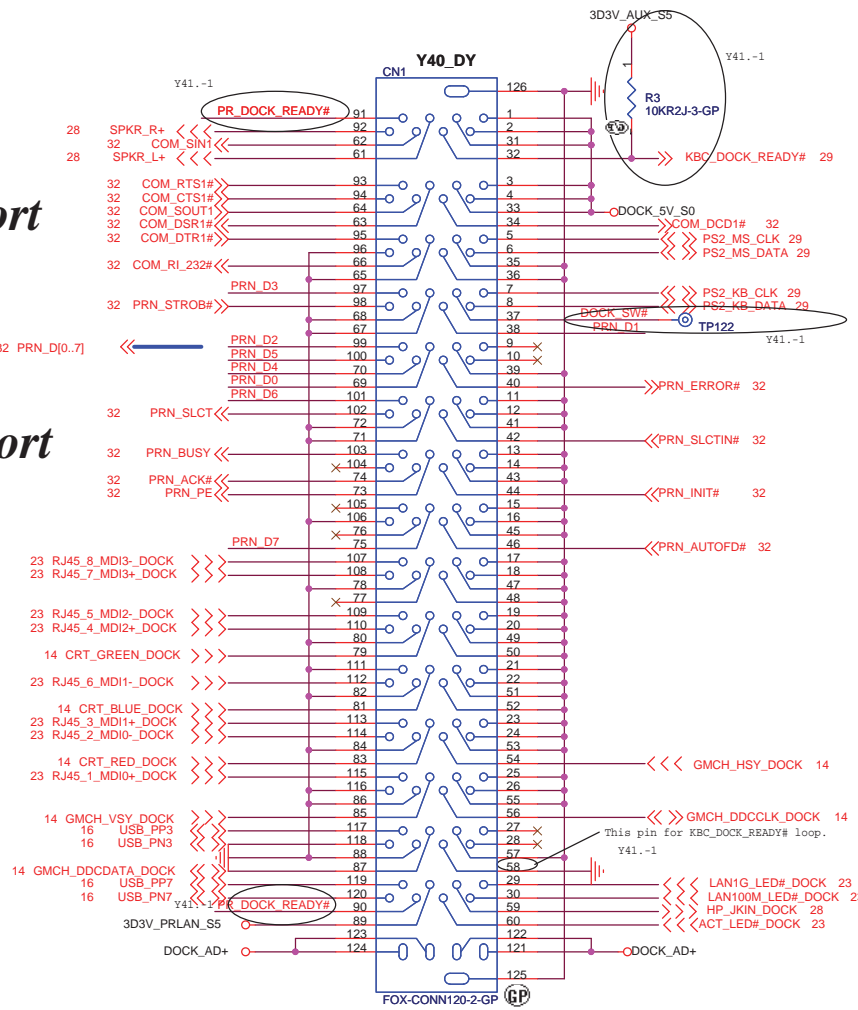


緯創資通 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>SIO PC87383-VS</b>		
Size	Document Number	Rev
C	<b>Y41/Y40</b>	<b>-1</b>
Date:	Wednesday, April 12, 2006	Sheet 32 of 44

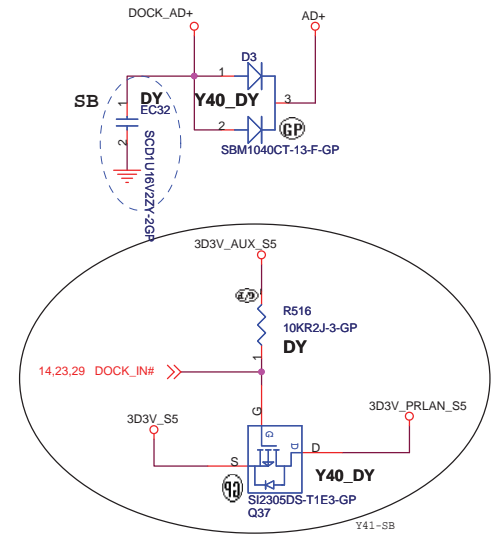
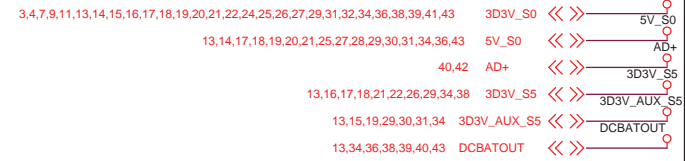


## Serial Port

## Printer Port

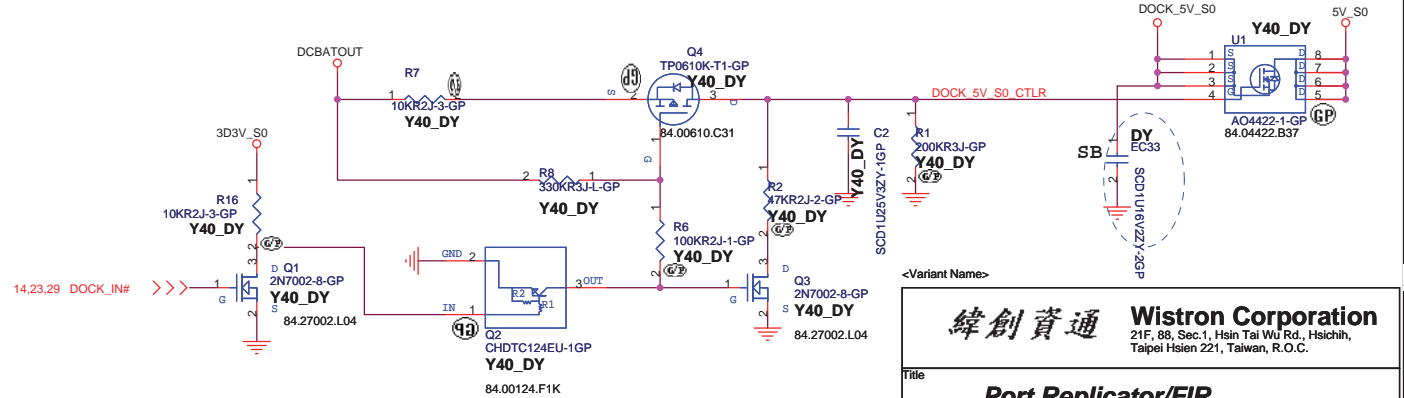
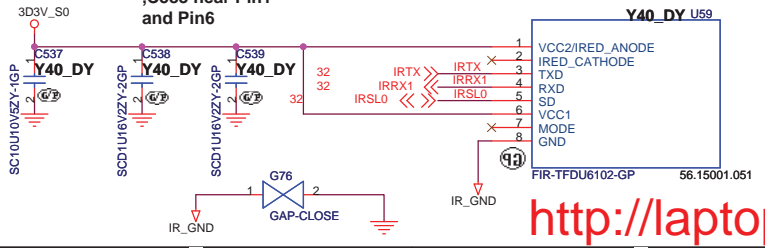


20.80591.120



## VISHAY FIR/CIR Module

Layout Guide:  
 (1) FIR\_3D3V : 30 mils,  
 (2) C583, C581 close  
 to U32

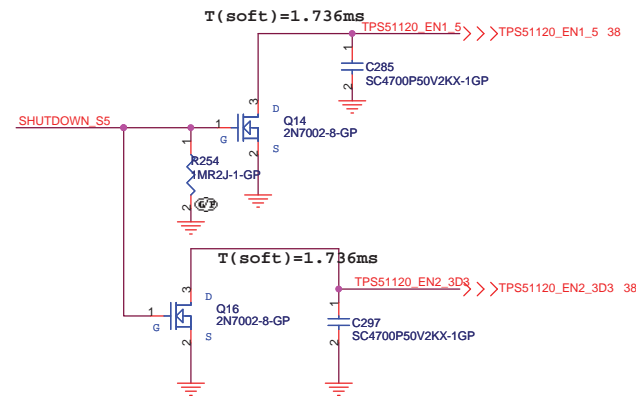
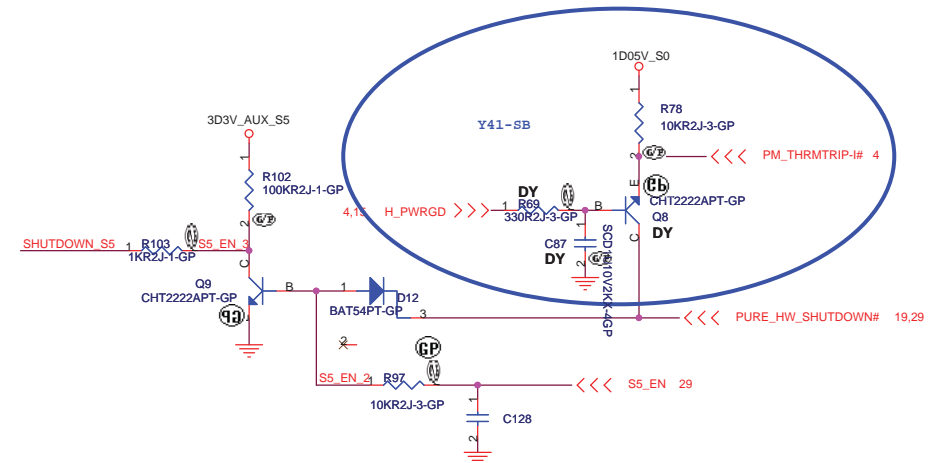
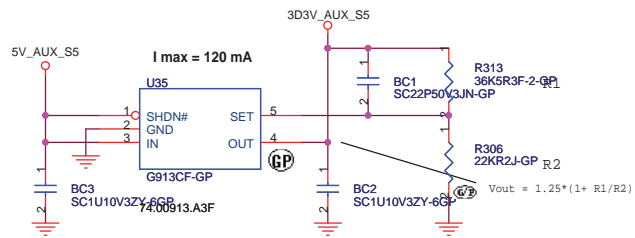
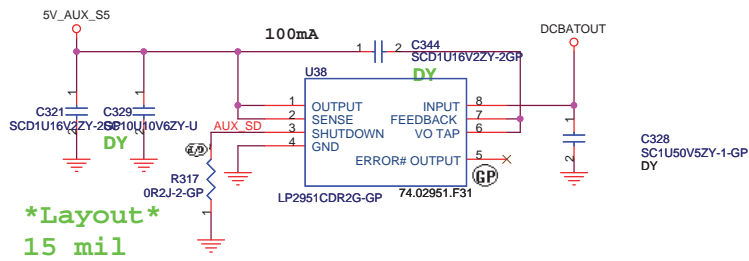


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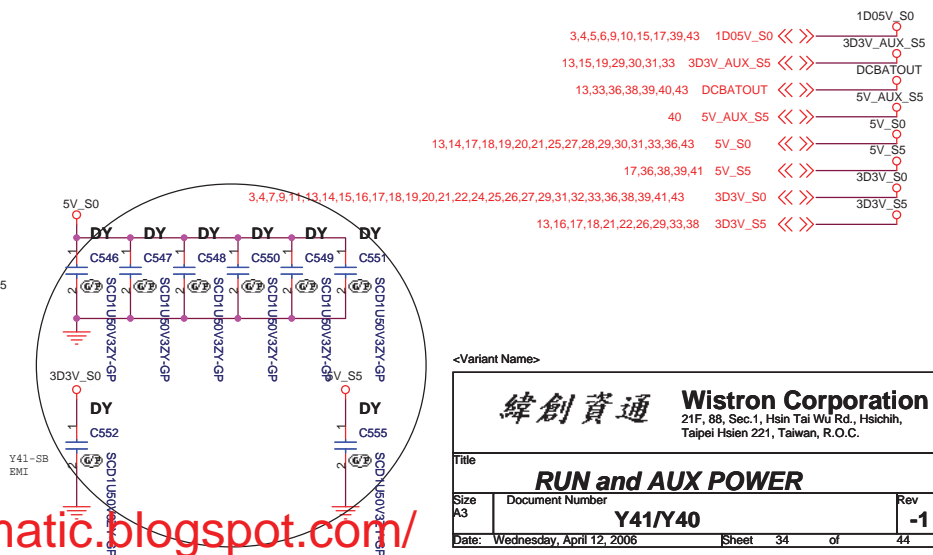
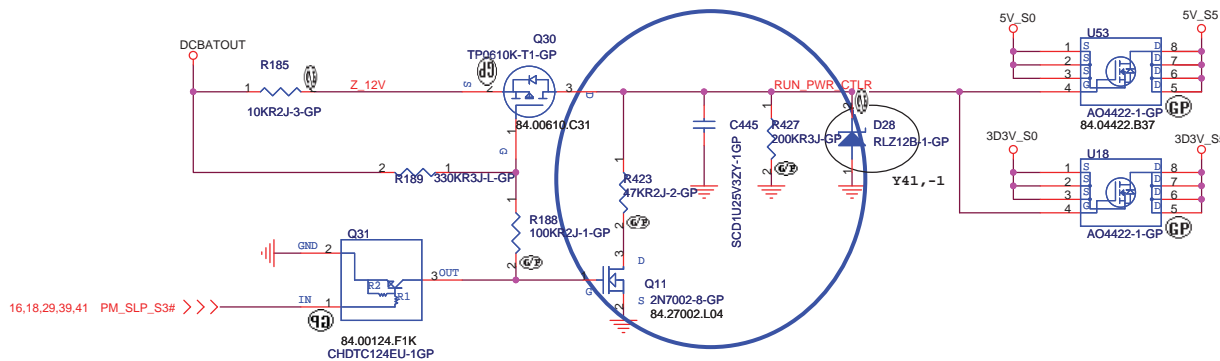
Title: Port Replicator/FIR  
 Size A3 Document Number Y41/Y40 Rev -1  
 Date: Friday, May 26, 2006 Sheet 33 of 44

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# Aux Power



# Run Power



- 3,4,5,6,9,10,15,17,39,43 1D05V\_S0 <<<
- 13,15,19,29,30,31,33 3D3V\_AUX\_S5 <<<
- 13,33,36,38,39,40,43 DCBATOUT <<<
- 40 5V\_AUX\_S5 <<<
- 13,14,17,18,19,20,21,25,27,28,29,30,31,33,36,43 5V\_S0 <<<
- 17,36,38,39,41 5V\_S5 <<<
- 3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,36,38,39,41,43 3D3V\_S0 <<<
- 13,16,17,18,21,22,26,29,33,38 3D3V\_S5 <<<

<Variant Name>

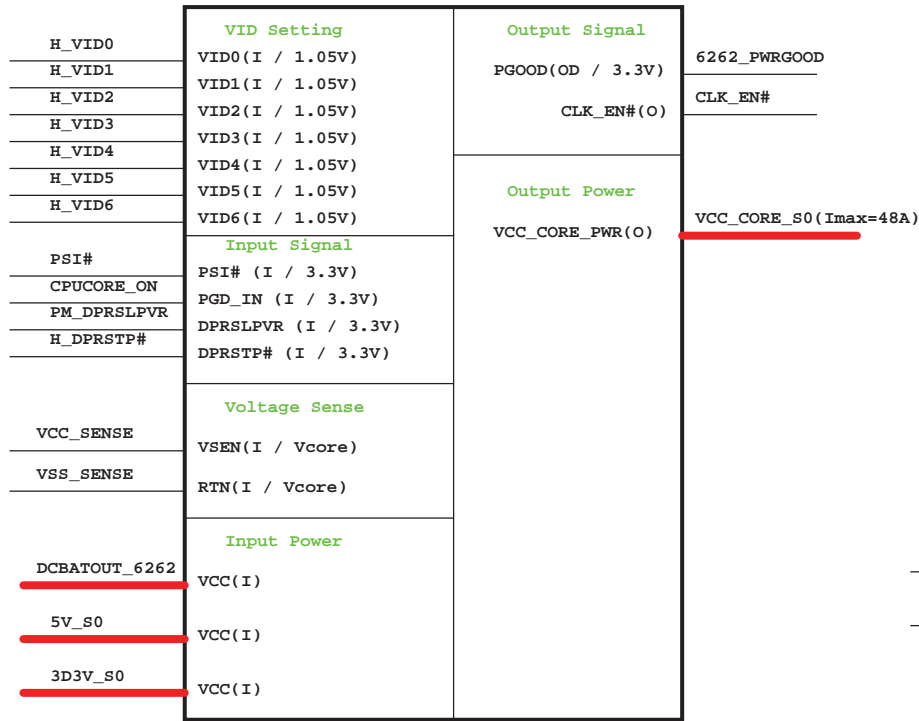
**緯創資通 Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

**RUN and AUX POWER**

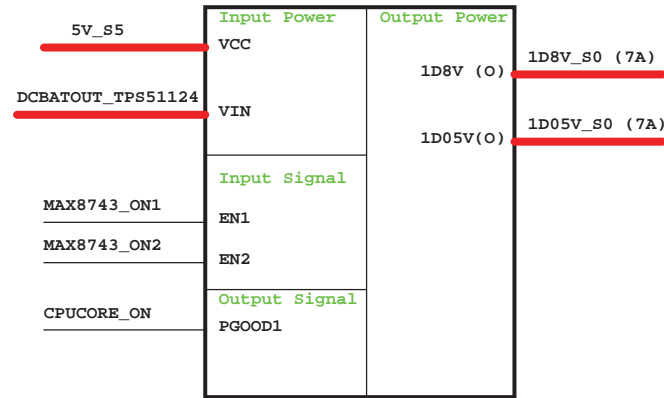
Size A3 Document Number **Y41/Y40** Rev **-1**

Date: Wednesday, April 12, 2006 Sheet 34 of 44

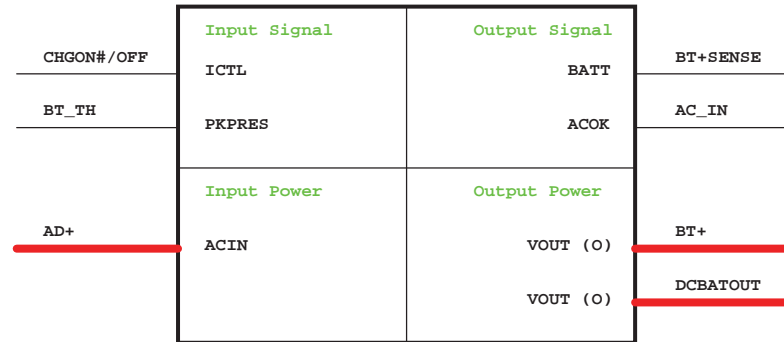
**CPU\_CORE**  
Intersil ISL6262



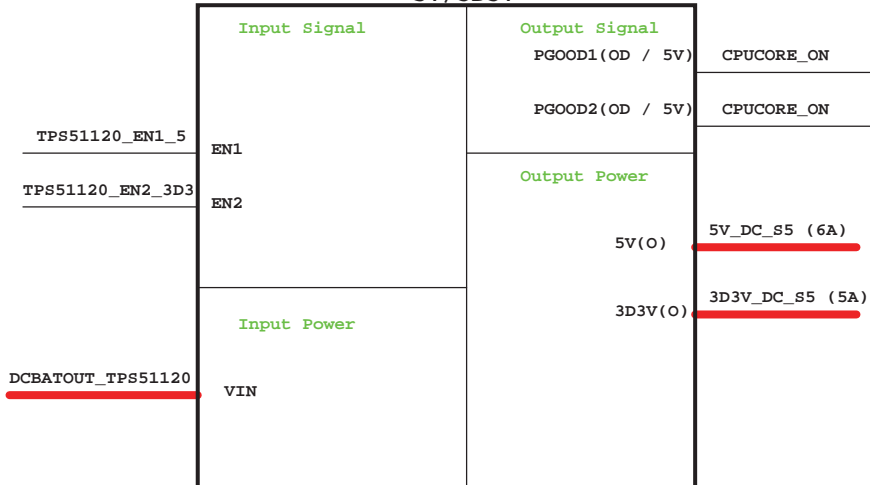
**MAX8743**  
1D8V/1D05V



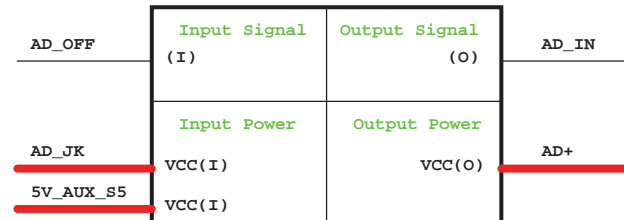
**Charger Max8725**



**TPS51120**  
5V/3D3V



**Adapter**

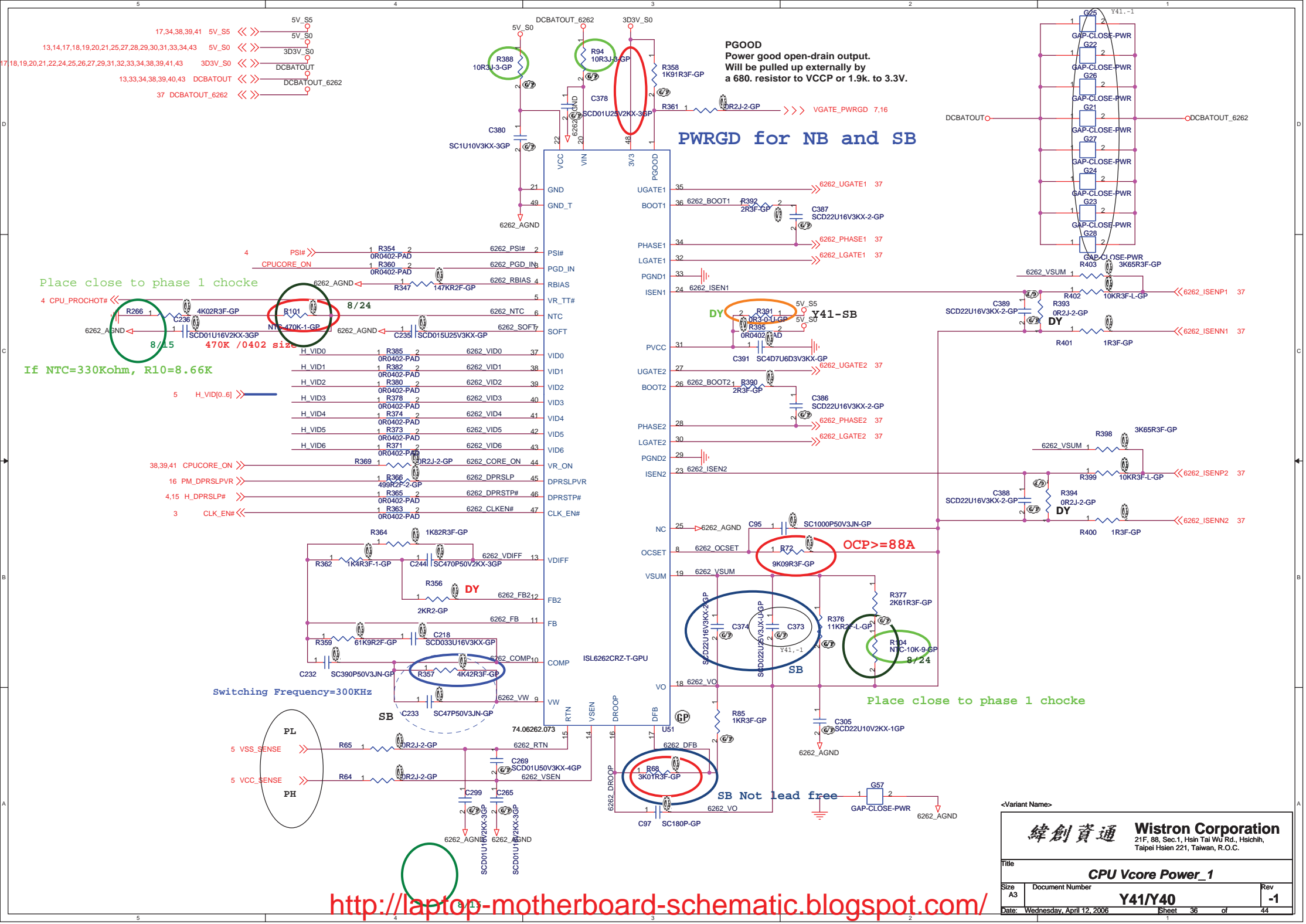


<Variant Name>

**緯創資通 Wistron Corporation**  
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Title: **Power Block Diagram**

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Date: Friday, April 07, 2006	Sheet 35 of 44	



**PGOOD**  
Power good open-drain output.  
Will be pulled up externally by  
a 680. resistor to VCCP or 1.9k. to 3.3V.

**PWRGD for NB and SB**

Place close to phase 1 choke

If NTC=330kOhm, R10=8.66K

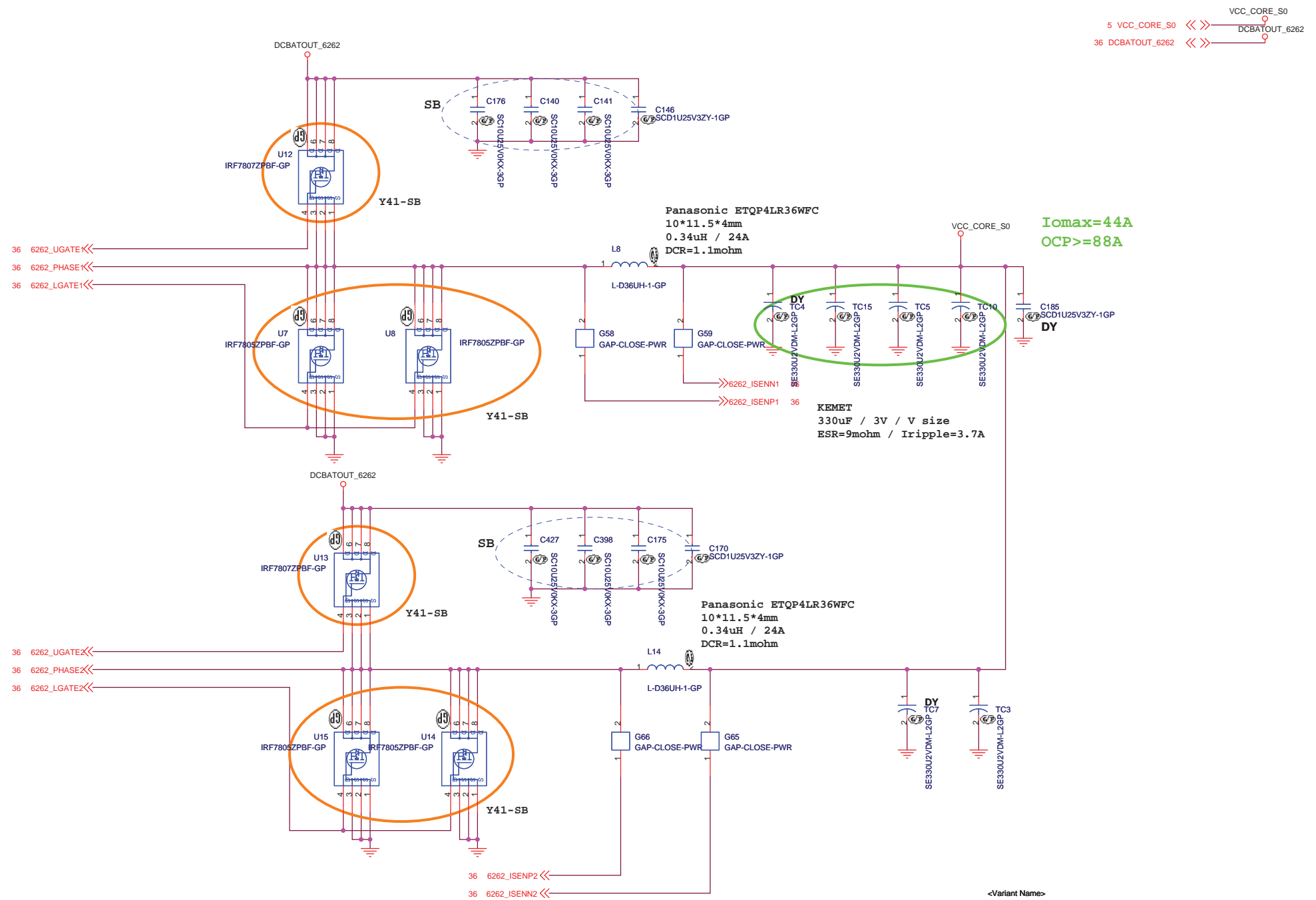
Place close to phase 1 choke

- 38,39,41 CPUCORE\_ON >>>
- 16 PM DPRSLPVR >>>
- 4,15 H DPRSLP# >>>
- 3 CLK\_EN# >>>

Switching Frequency=300KHz

OCP >= 88A

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Title <b>CPU Vcore Power_1</b>	
Size A3	Document Number <b>Y41/Y40</b>
Date: Wednesday, April 12, 2006	Sheet 36 of 44



VCC\_CORE\_S0  
 5 VCC\_CORE\_S0 <<>> DCBATOUT\_6262  
 36 DCBATOUT\_6262 <<>>

**Iomax=44A**  
**OCP>=88A**

**KEMET**  
 330uF / 3V / V size  
 ESR=9mohm / Iripple=3.7A

**Panasonic ETQP4LR36WFC**  
 10\*11.5\*4mm  
 0.34uH / 24A  
 DCR=1.1mohm

**Panasonic ETQP4LR36WFC**  
 10\*11.5\*4mm  
 0.34uH / 24A  
 DCR=1.1mohm

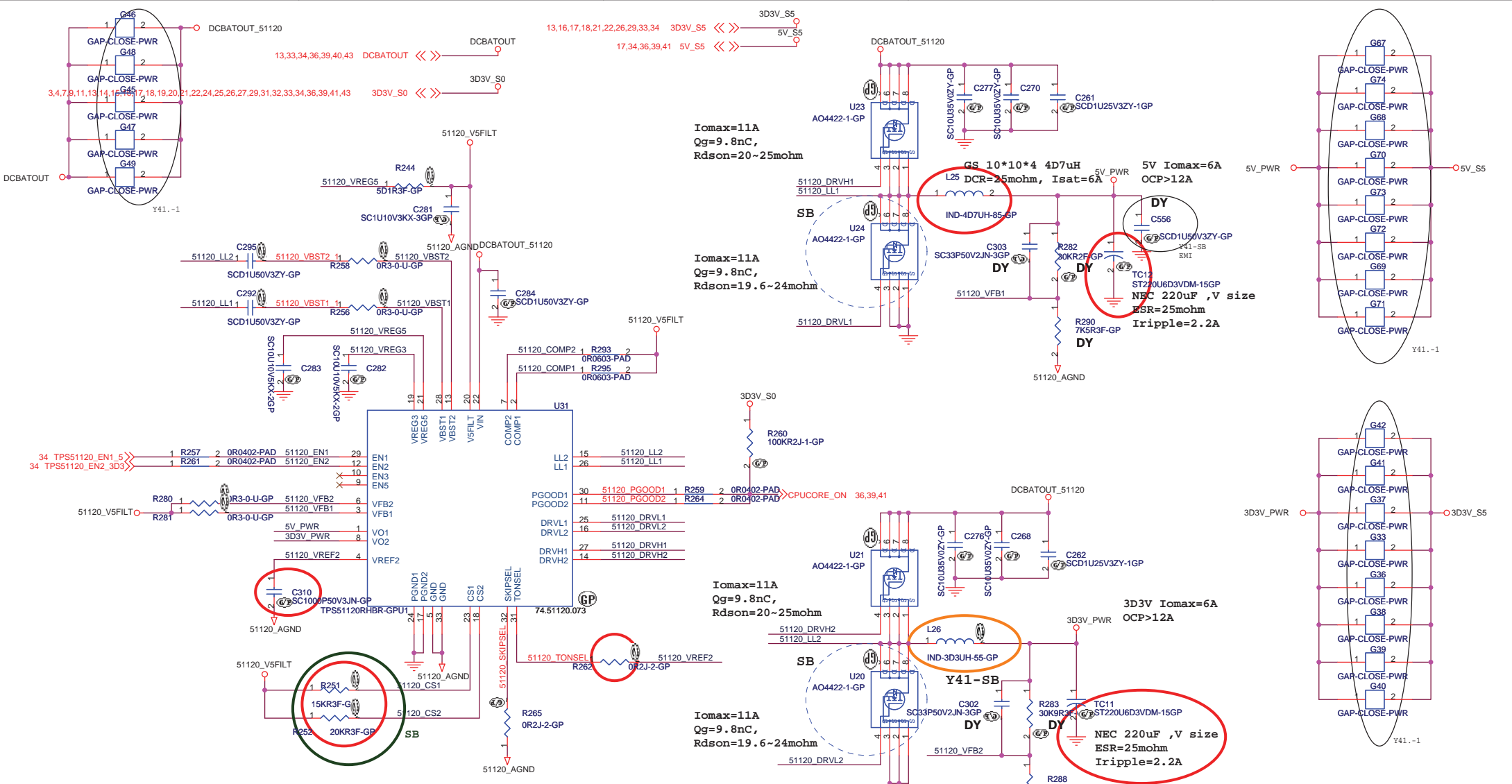
<Variant Name>

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Title  
**CPU Vcore Power\_2**

Size A3	Document Number <b>Y41/Y40</b>	Rev <b>-1</b>
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$I_{omax}=11A$   
 $Q_g=9.8nC$ ,  
 $R_{dson}=20\sim 25m\Omega$

$I_{omax}=11A$   
 $Q_g=9.8nC$ ,  
 $R_{dson}=19.6\sim 24m\Omega$

$I_{omax}=11A$   
 $Q_g=9.8nC$ ,  
 $R_{dson}=20\sim 25m\Omega$

$I_{omax}=11A$   
 $Q_g=9.8nC$ ,  
 $R_{dson}=19.6\sim 24m\Omega$

$$V_{out}=1V \cdot (R1+R2) / R2$$

For TPS51120,  
 $V_{out}=5V$

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

$V_{out}=3.3V$

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

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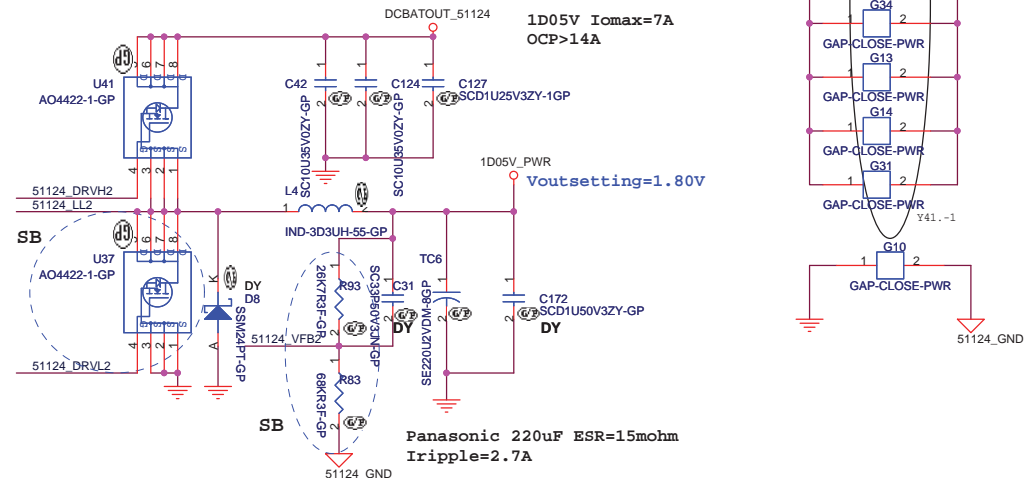
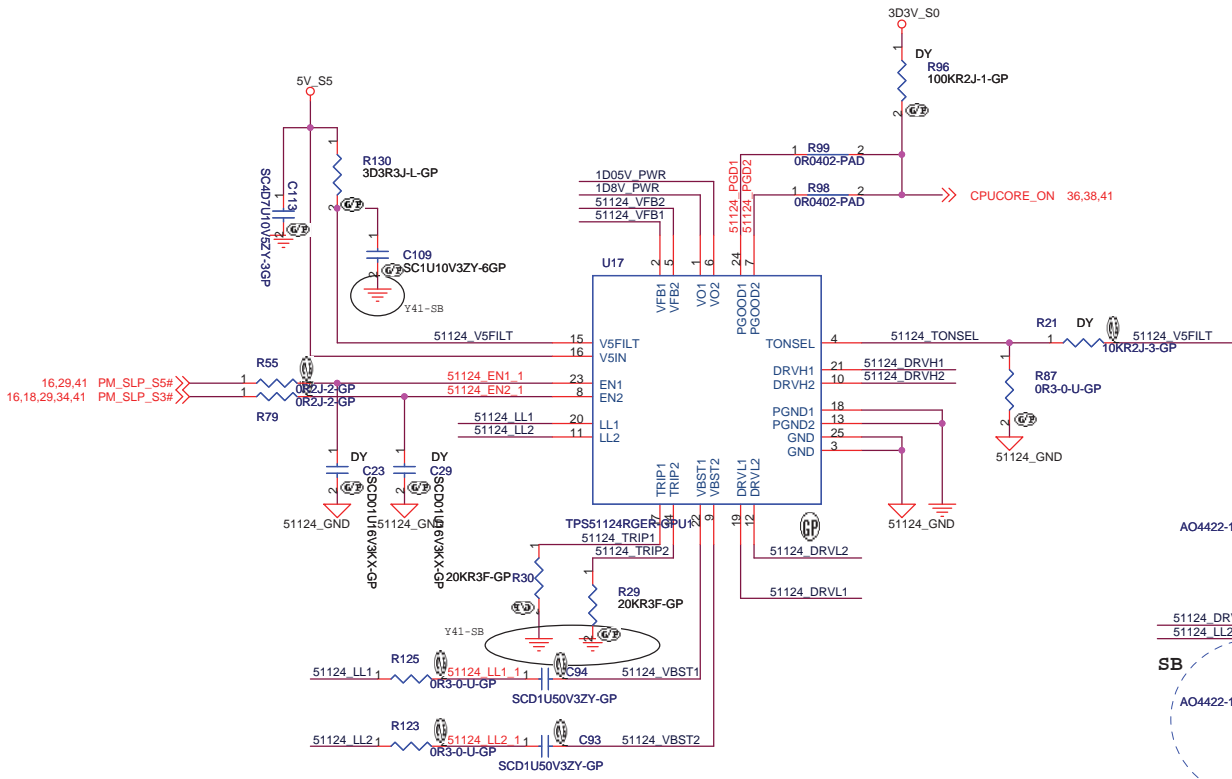
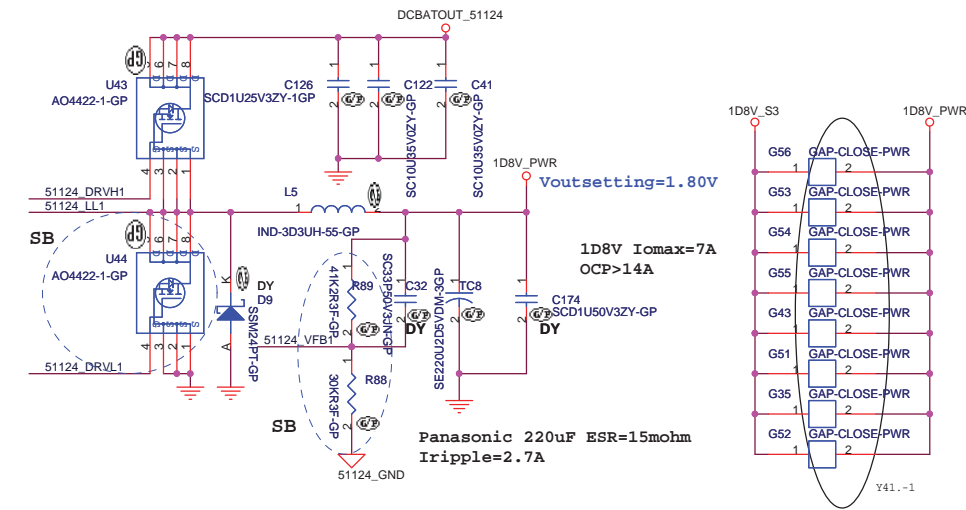
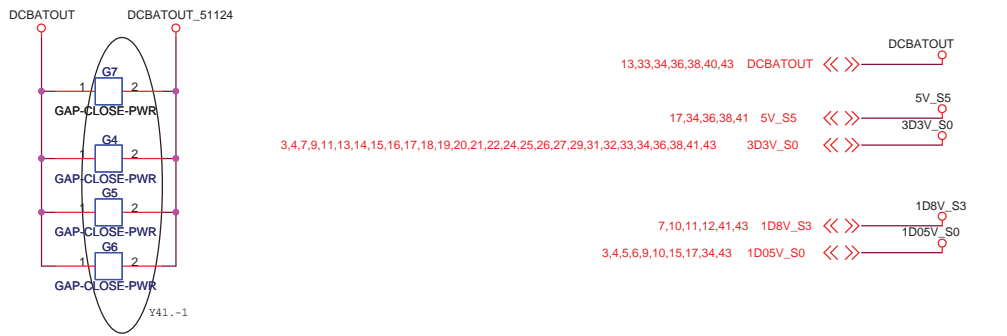
<Variant Name>

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Title: **5V\_UP\_S5/3D3V\_S5/5V\_S5**

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$$V_{out} = 0.75V * (R1 + R2) / R2$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	243k/CH1 346k/CH2	346k/CH1 423k/CH2

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

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<Variant Name>

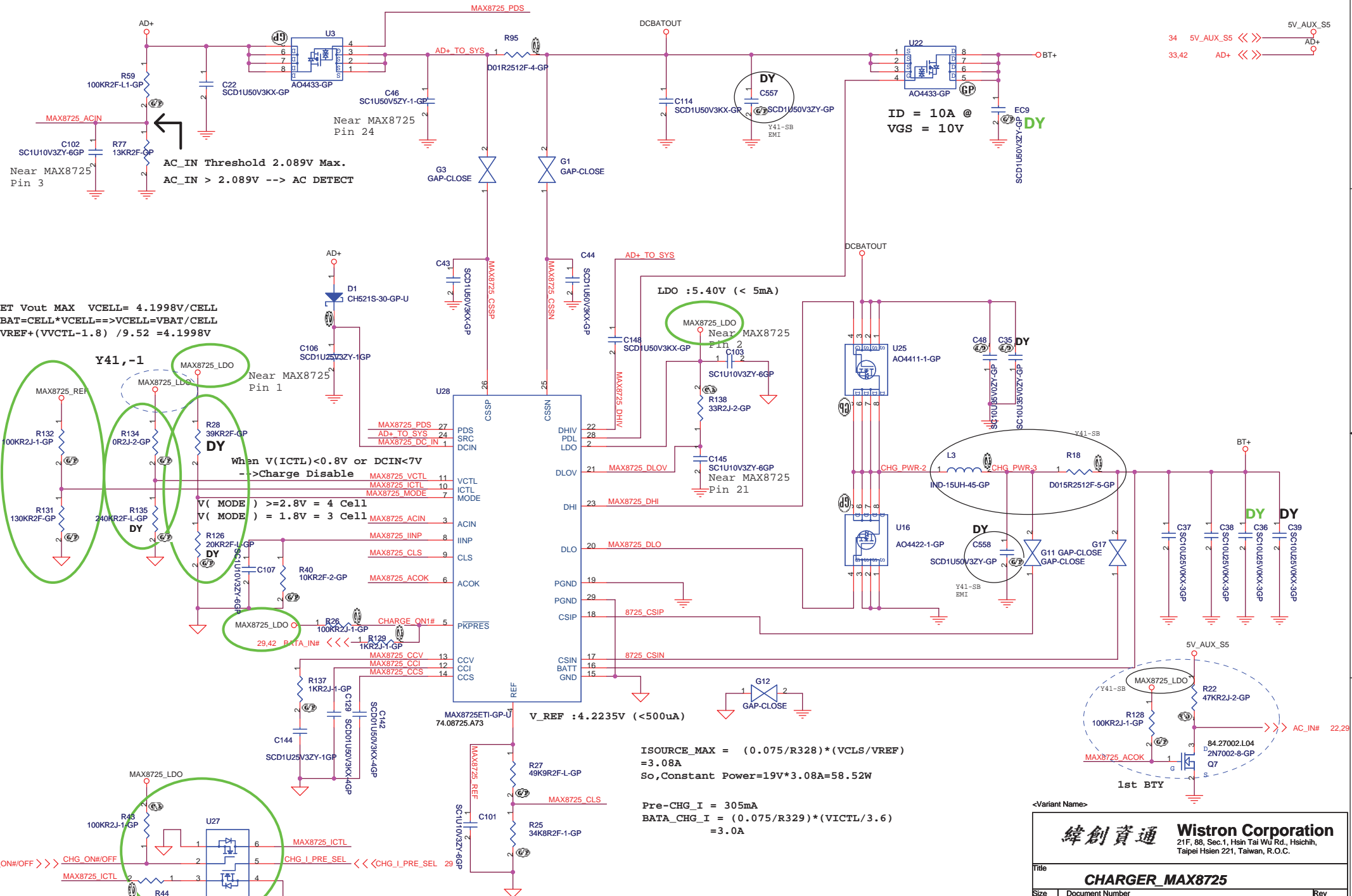
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124\_1D8V\_1D05V**

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13,33,34,36,38,39,43 DCBATOUT <<>>  
 42 BT+ <<>>  
 5V\_AUX\_S5 <<>>  
 34 5V\_AUX\_S5 <<>>  
 33,42 AD+ <<>>



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<Variant Name>

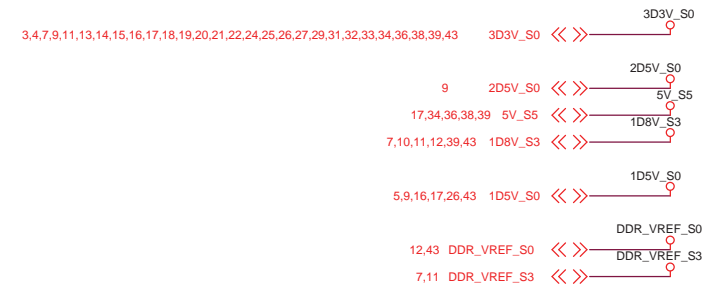
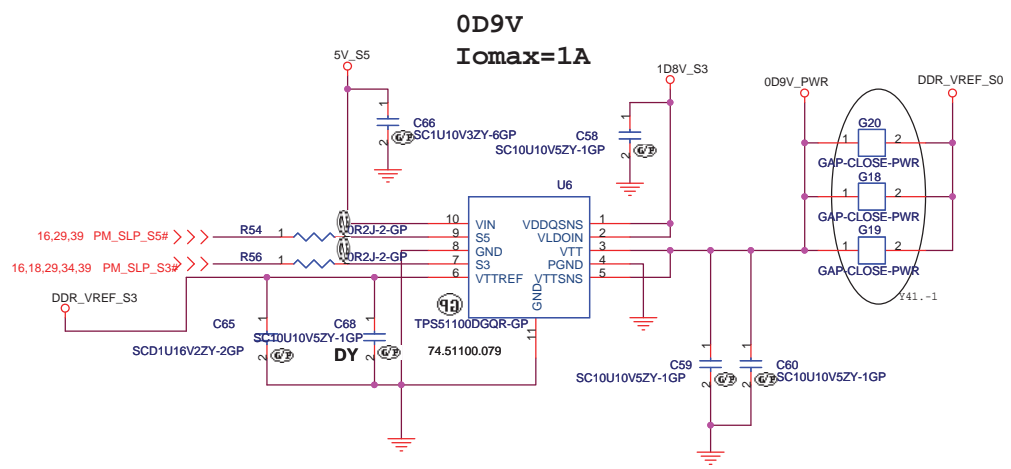
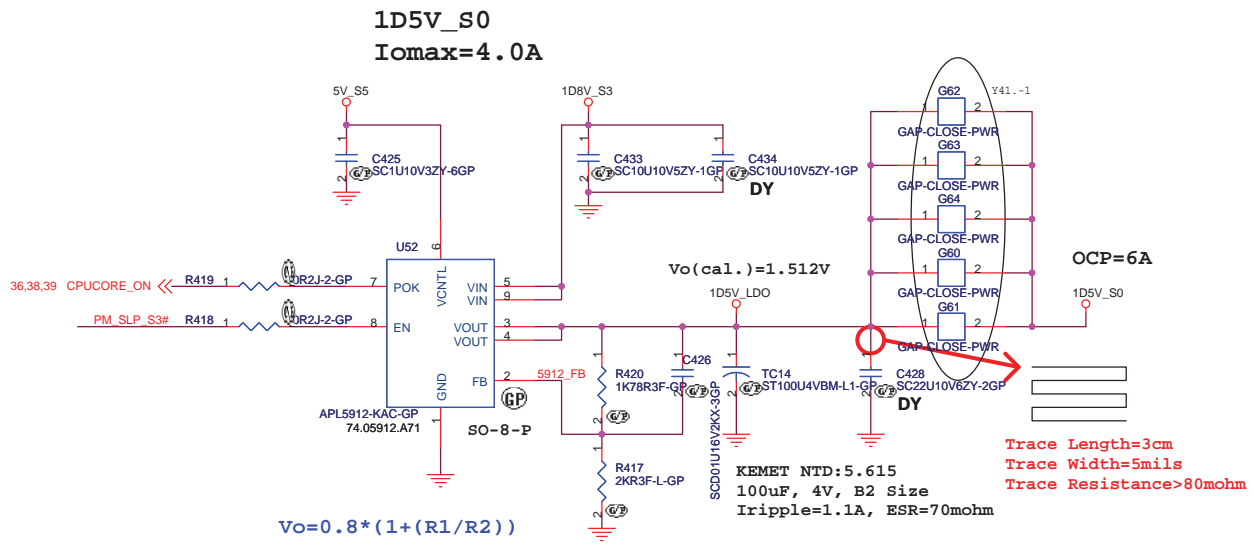
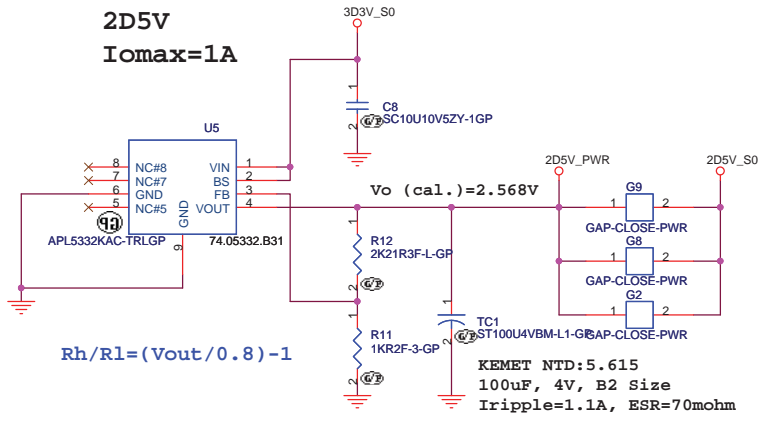
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8725**

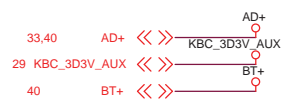
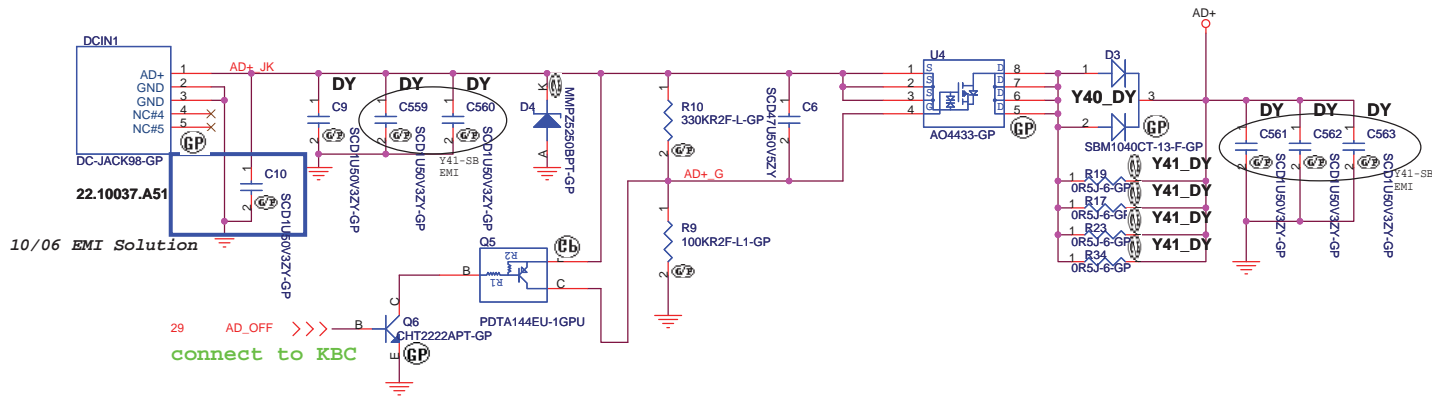
Size A3	Document Number Y41/Y40	Rev -1
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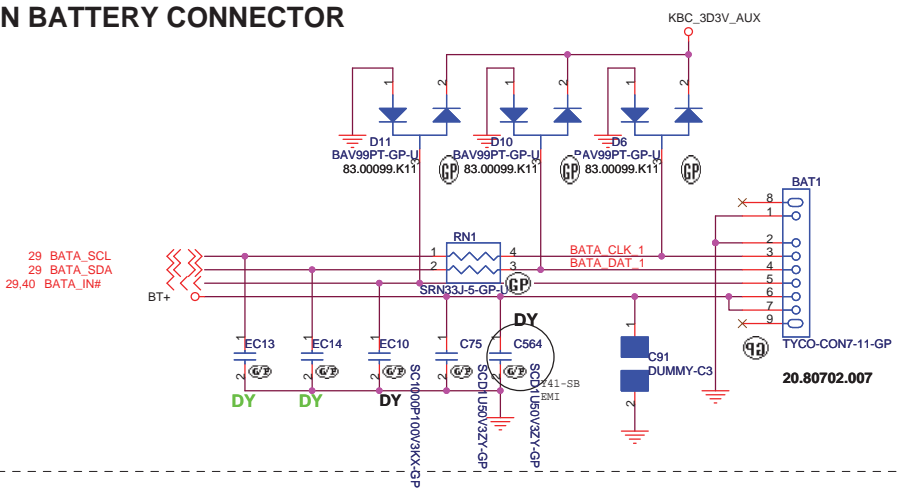




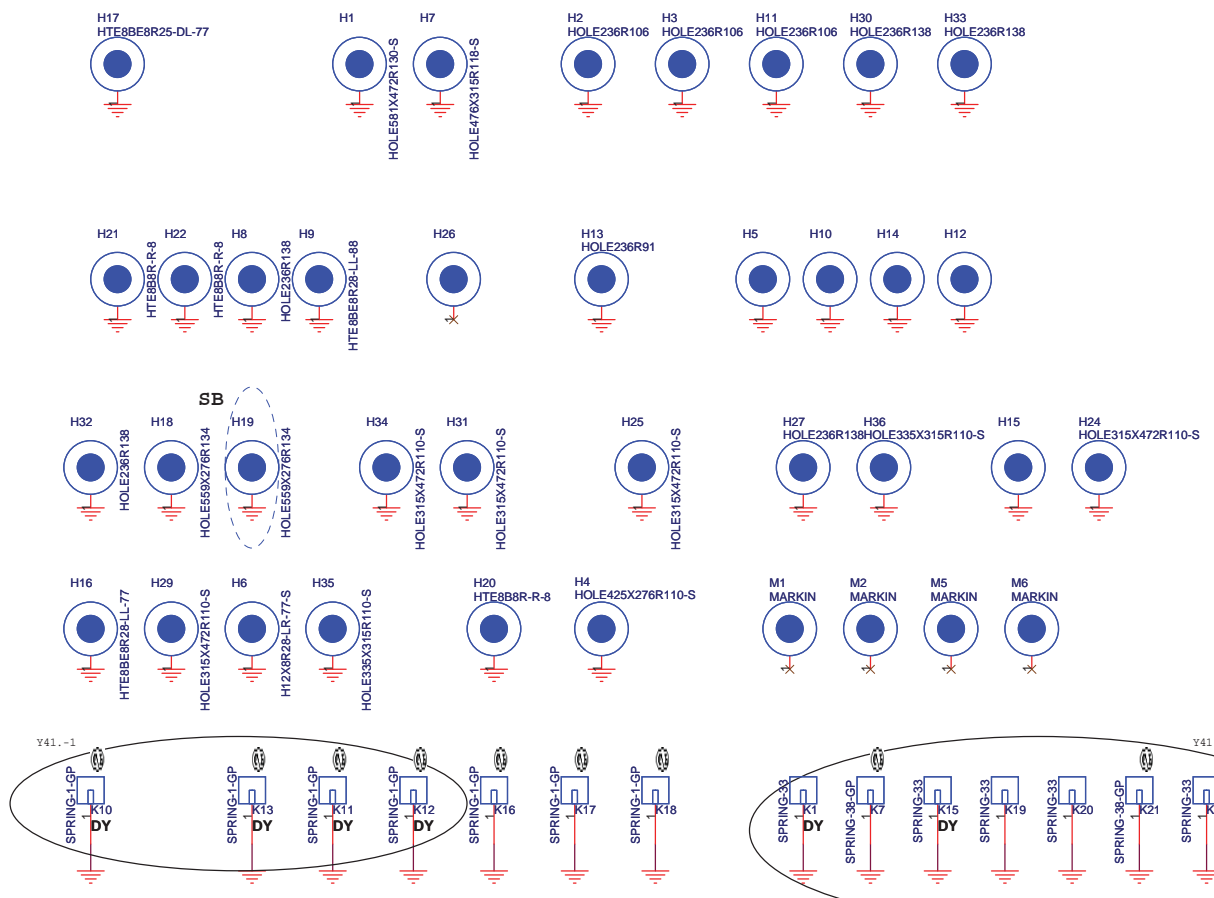
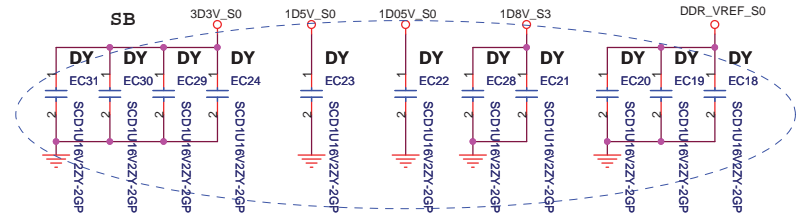
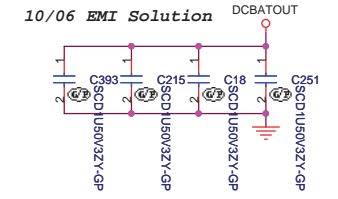
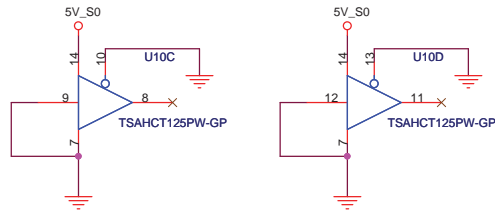
## ADAPTER IN CIRCUIT



## MAIN BATTERY CONNECTOR



<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>AD/BATT CONN</b>		
Size A3	Document Number Y41/Y40	Rev -1
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<Variant Name>

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Title: **SPRING & BOSS & EMI**

Size A3 Document Number **Y41/Y40** Rev **-1**

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**PRT modification list for Layout:**

MINIC1, 62.10043.241  
CDROM1, 20.80338.050  
CN1, 20.80591.120  
U9, 62.10079.001  
U45, 71.88055.A03  
U58, 71.AL861.00G

**PRT modification list for Y41/Y41 BOM:**

FAN1, 20.F0714.003 H32, 34.46114.001  
MINIC1, 62.10043.241 H27, 34.46114.001  
LAUNCH1, 20.K0196.005 H18, 34.46114.001  
U36, 74.02211.B39 H14, 34.4B604.001  
U45, 71.88055.A03 H10, 34.4B604.001  
U58, 71.AL861.00G H30, 34.4B601.001  
XF1, 68.2410S.30B H33, 34.4B601.001  
D2,D3 83.10R04.E87(Y41) H5, 34.4B602.001  
U50, 71.945GM.B0U H8, 34.4B603.001  
U29, 71.ICHPM.C0U  
LCD1, 20.F0853.040 Del K2-K6,K8,K9  
C6, 78.47494.41L  
C280,C288, 78.10593.4FL  
78.10221.2F1 <-> 78.10221.2FL

**Modification list:**

Change parts to meet vista as below:

78.22521.5BL: 2.2uF 16V 0603 XSR; CS22,CS31.(Original:78.10593.4BL,1uF)  
78.47521.51L(SCH)78.47522.51L); 4.7uF 16V 0805 XSR; C363,C364,C357,C358.(Original:78.22591.41L,2.2uF)  
63.22334.1DL: 22K Ohm F 0402; R483,R484.(Original:63.10234.1DL,1K Ohm)  
C575 Dummy.(Original:78.10134.1FL,100pF)  
64.20025.6DL: 20K Ohm F 0402; R332.(Original:64.51015.6DL,5.1K Ohm)  
63.R0034.1DL: 0 Ohm J 0402; R531.(Original:63.47034.1DL,47 Ohm)  
71.AL861.A0G; ALC861-VD; U58.(Original:71.AL861.00G,ALC861)

**Daughter Board information:**

LAUNCH/B Layout Revision: 05572-1.  
LAUNCH/B PCB P/N: 48.4P502.011

USB/B Layout Revision: 05573-1.  
USB/B PCB P/N: 48.4P503.011

Port Replicator/B Layout Revision: 05579-1.  
Port replicator/B PCB P/N: 48.4P504.011

**Key part list:**

<Variant Name>			
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>Remark</b>			
Title	Document Number		Rev
Size A3	<b>Y41/Y40</b>		<b>-1</b>
Date: Wednesday, December 06, 2006	Sheet 44	of	44