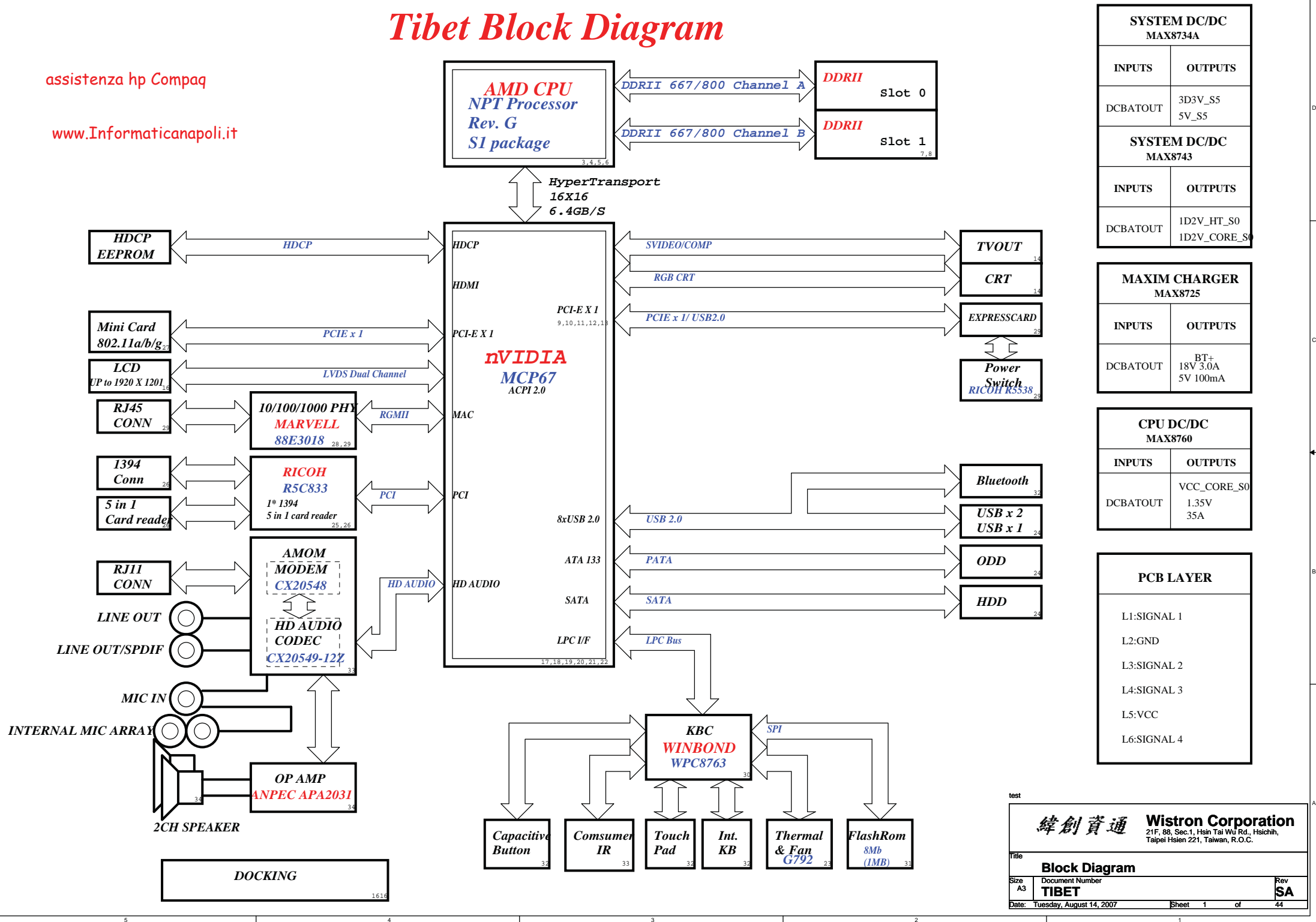


Tibet Block Diagram

assistenza hp Compaq

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SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

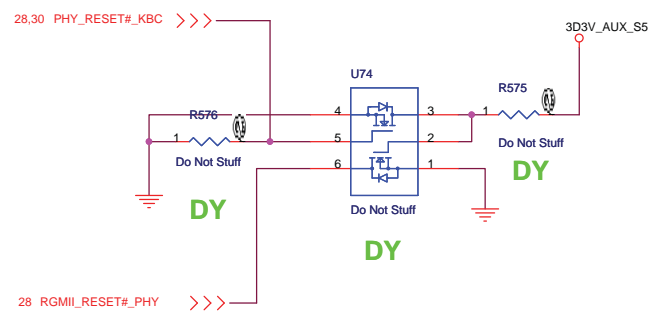
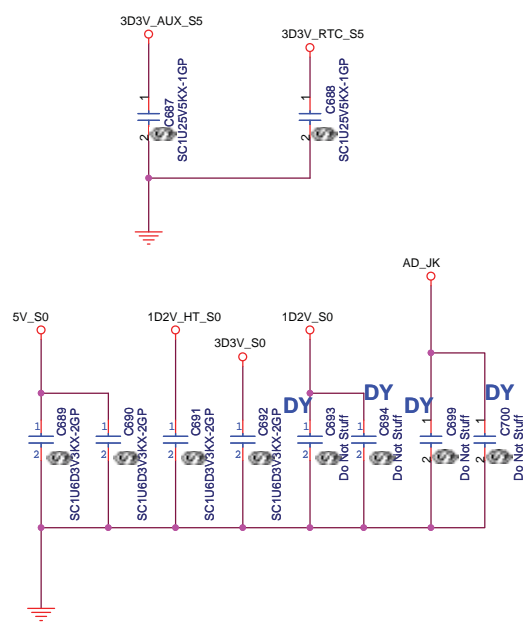
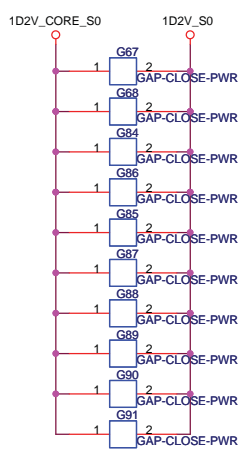
PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	

test

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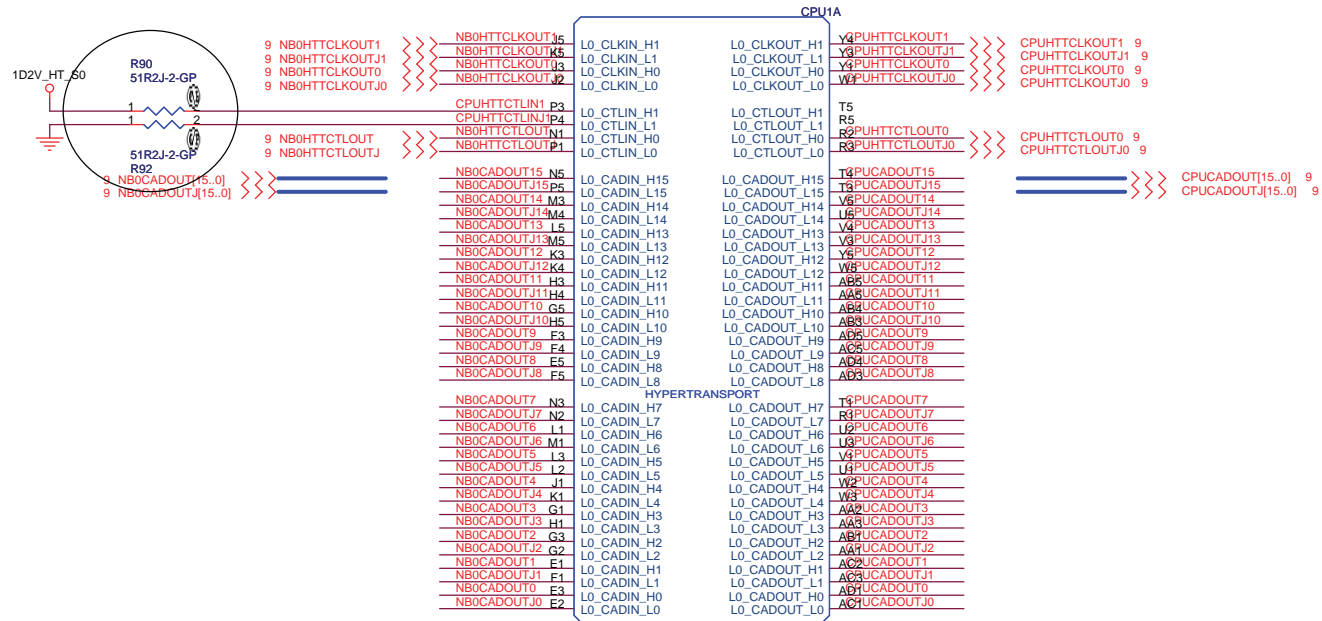
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Size: A3	Document Number: TIBET	Rev: SA
Date: Tuesday, August 14, 2007	Sheet: 1	of: 44

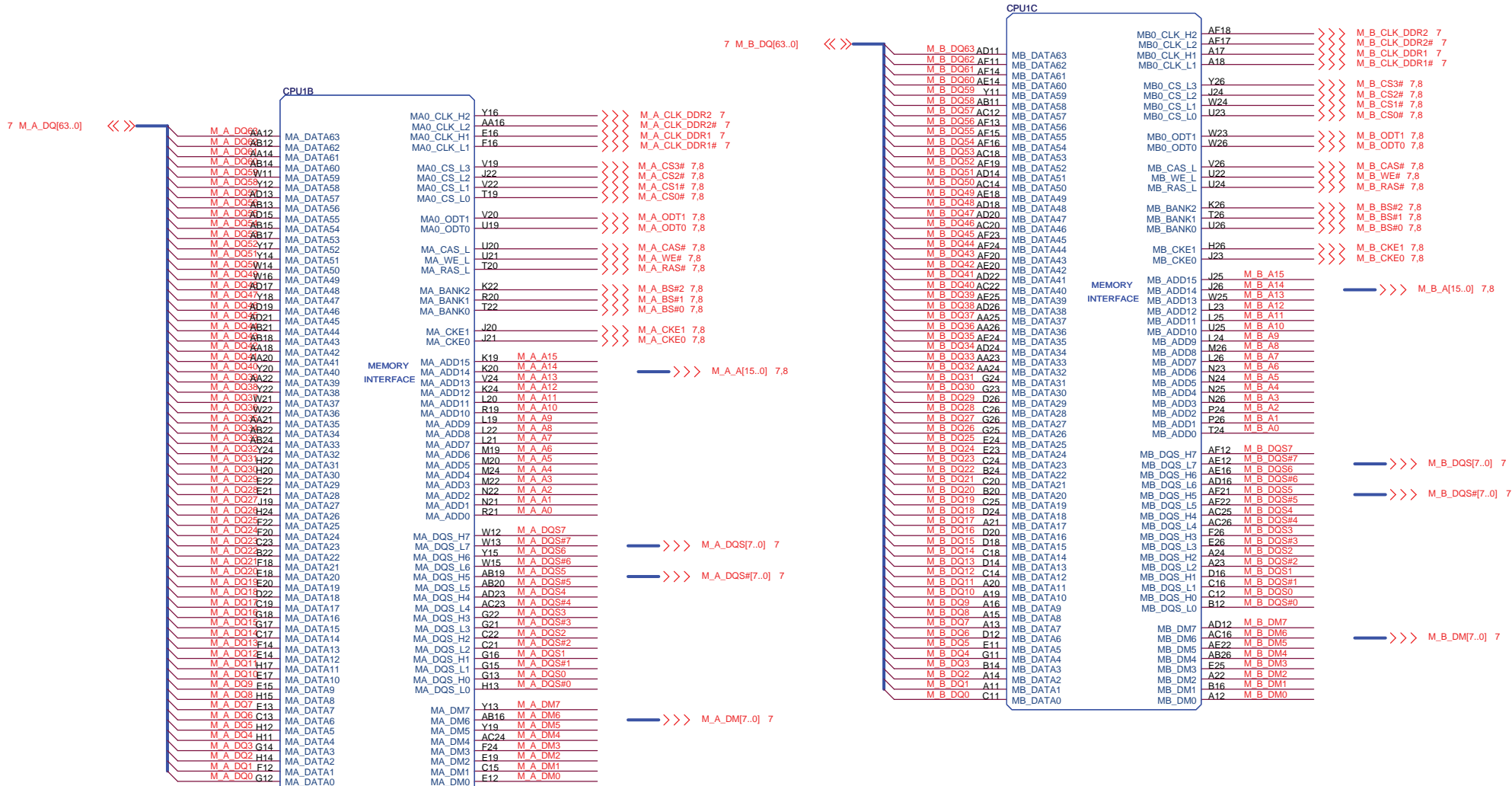


test

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Size A3	Document Number TIBET	Rev SA	
Date: Tuesday, August 14, 2007		Sheet 2	of 44



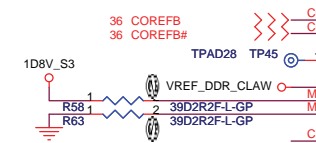
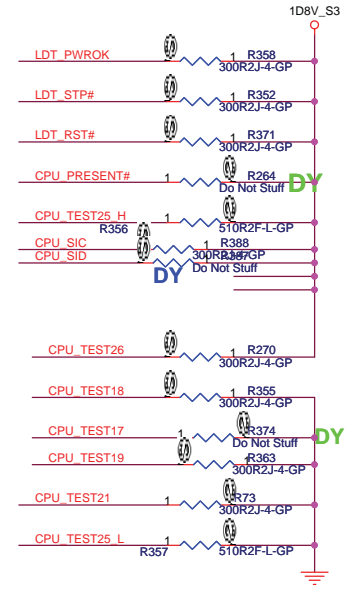
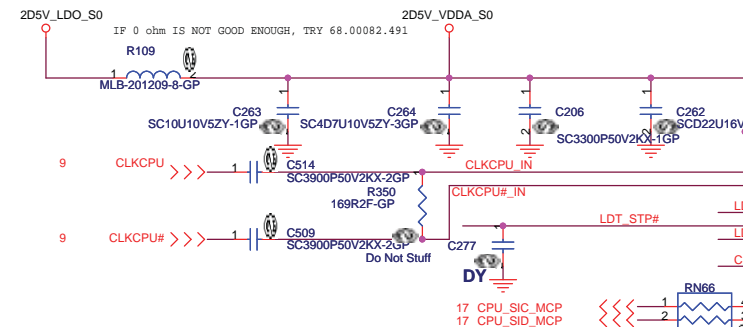
test



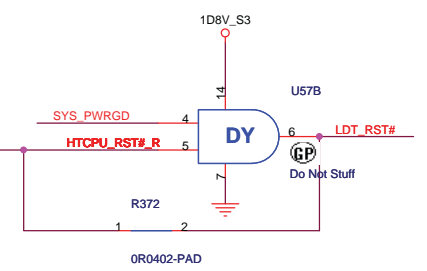
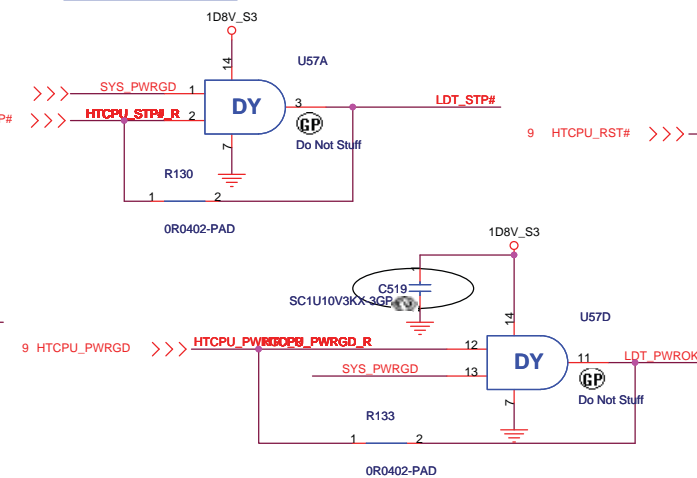
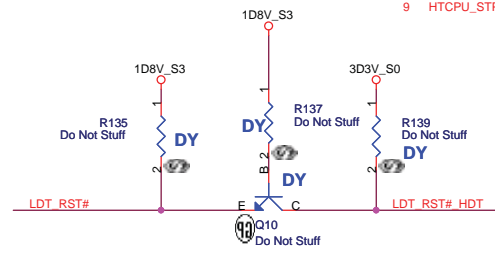
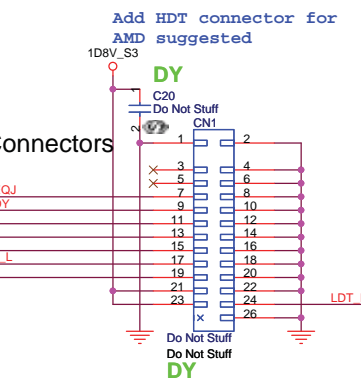
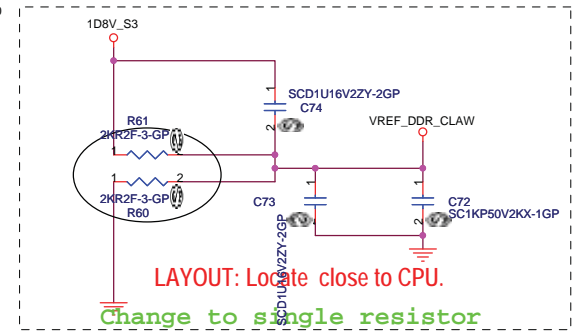


C36 near CLKCPU via

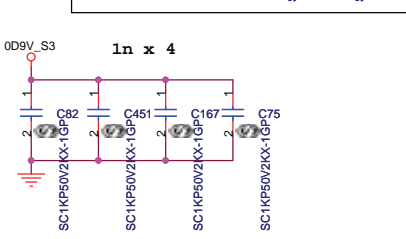
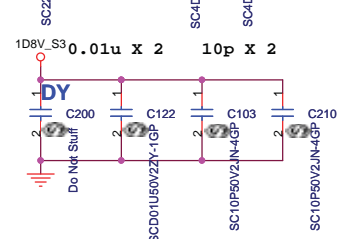
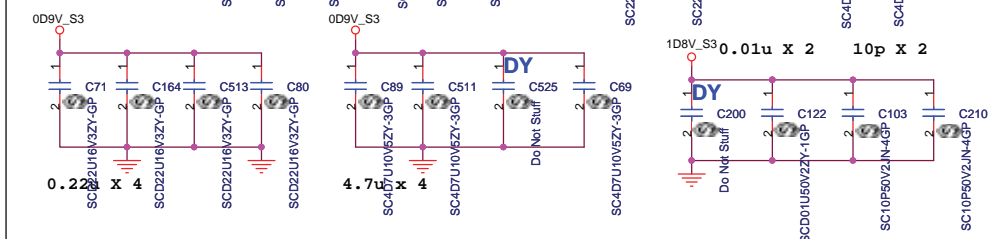
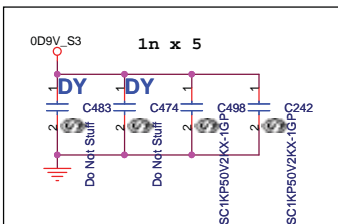
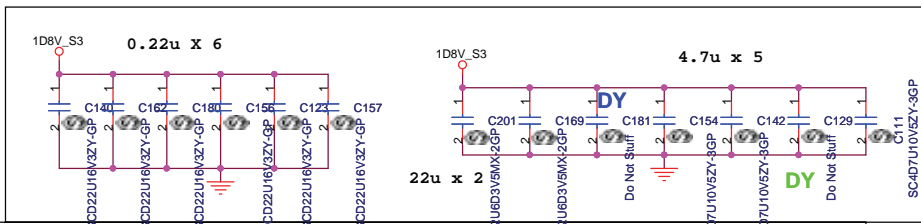
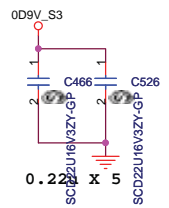
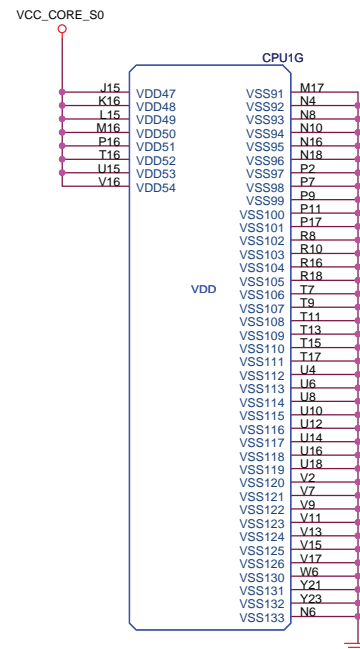
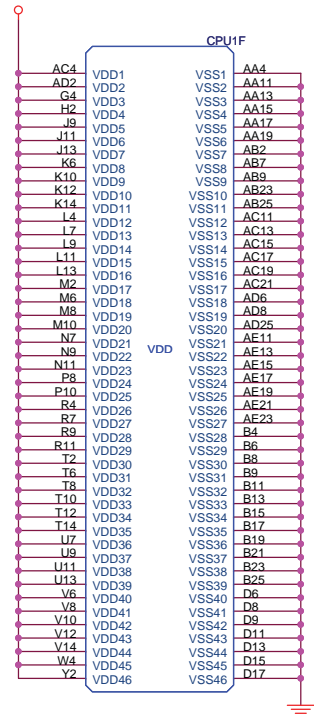
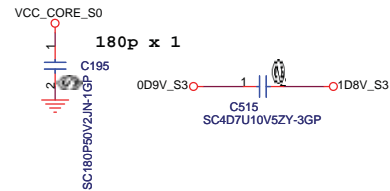
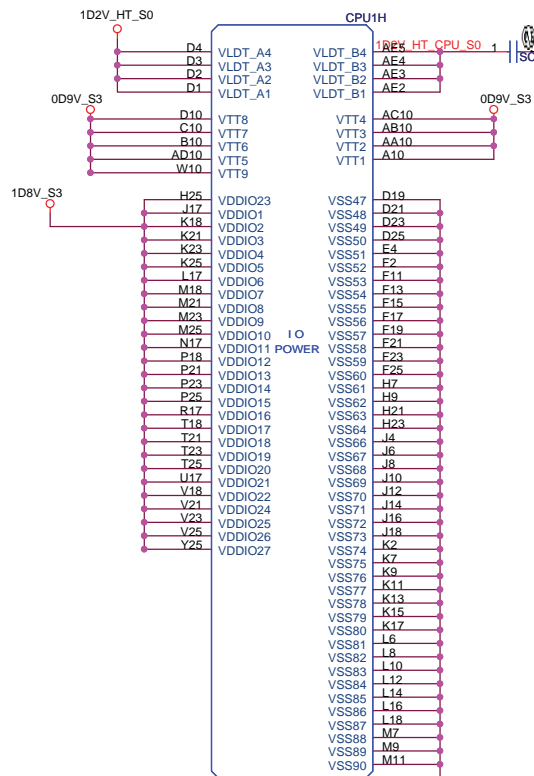
Pinout table for CPU1D showing signals like RSVD_MBO_CLK_H0, RSVD_MBO_CLK_L0, and CPU_PRESENT#.



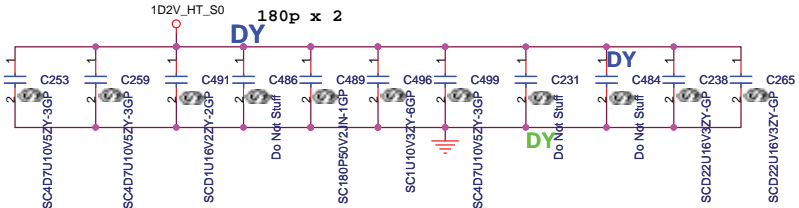
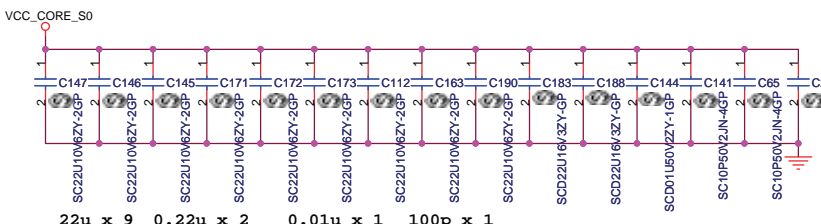
VREF_DDR_CLAW



Wistron Corporation logo and title block information: CPU(3/4) CONTROL, Tibet, Date: Tuesday, August 14, 2007, Sheet 5 of 44.



LAYOUT: Place on backside of processor.



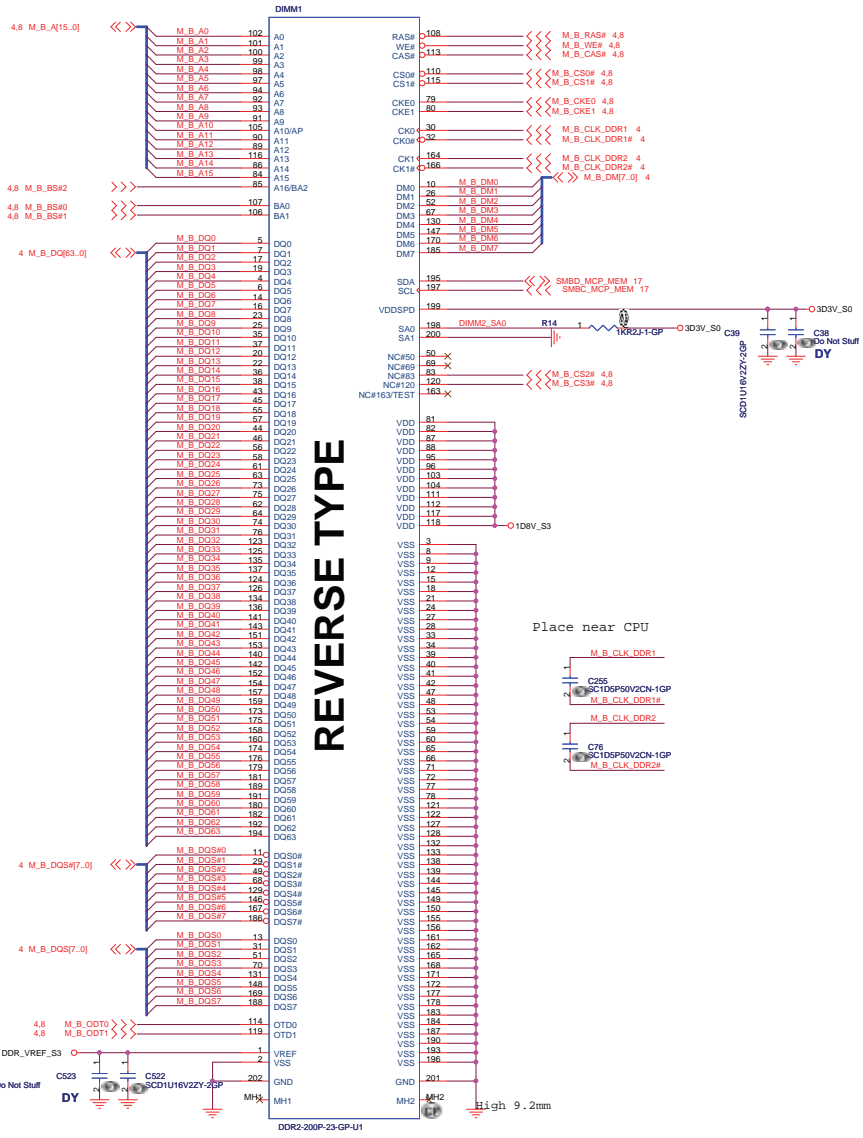
test

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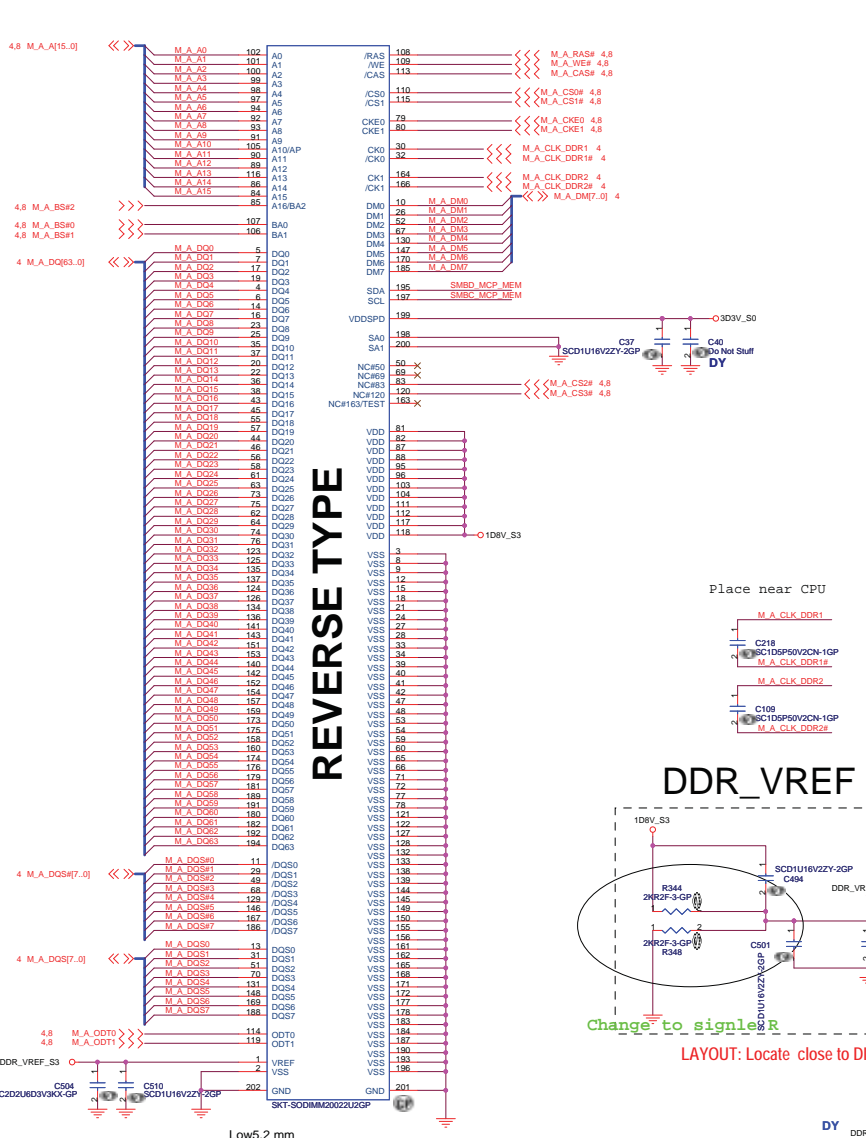
Title: **CPU(4/4) POWER**

Size: A3 Document Number: **TIBET** Rev: **SA**

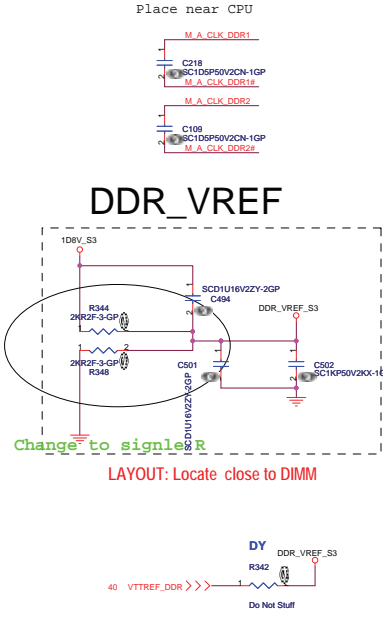
Date: Tuesday, August 14, 2007 Sheet 6 of 44



REVERSE TYPE

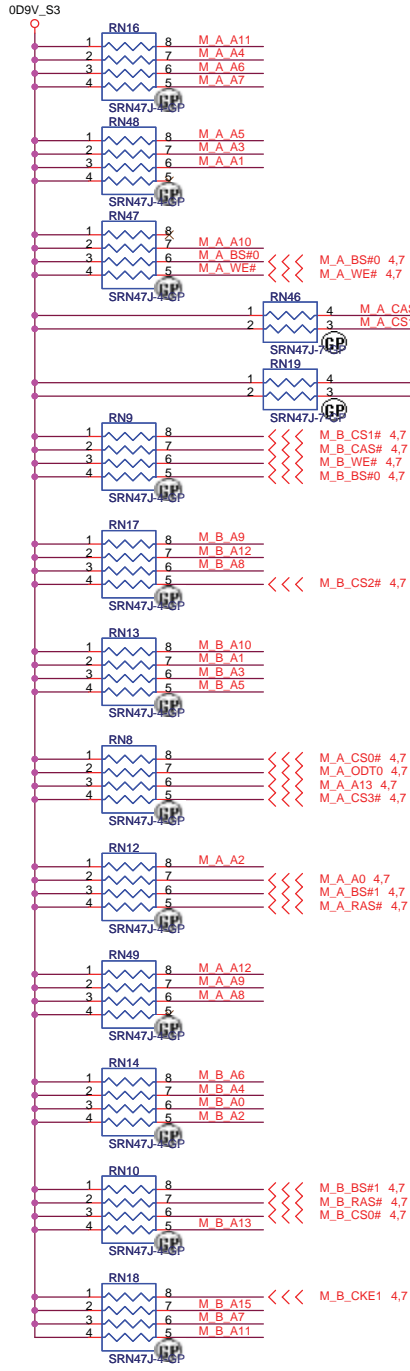


REVERSE TYPE



PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



M_A_[15..0] 4,7
M_B_[15..0] 4,7

M_A_CS2# 4,7
M_A_BS#2 4,7

M_A_CKE0 4,7

M_A_CKE1 4,7

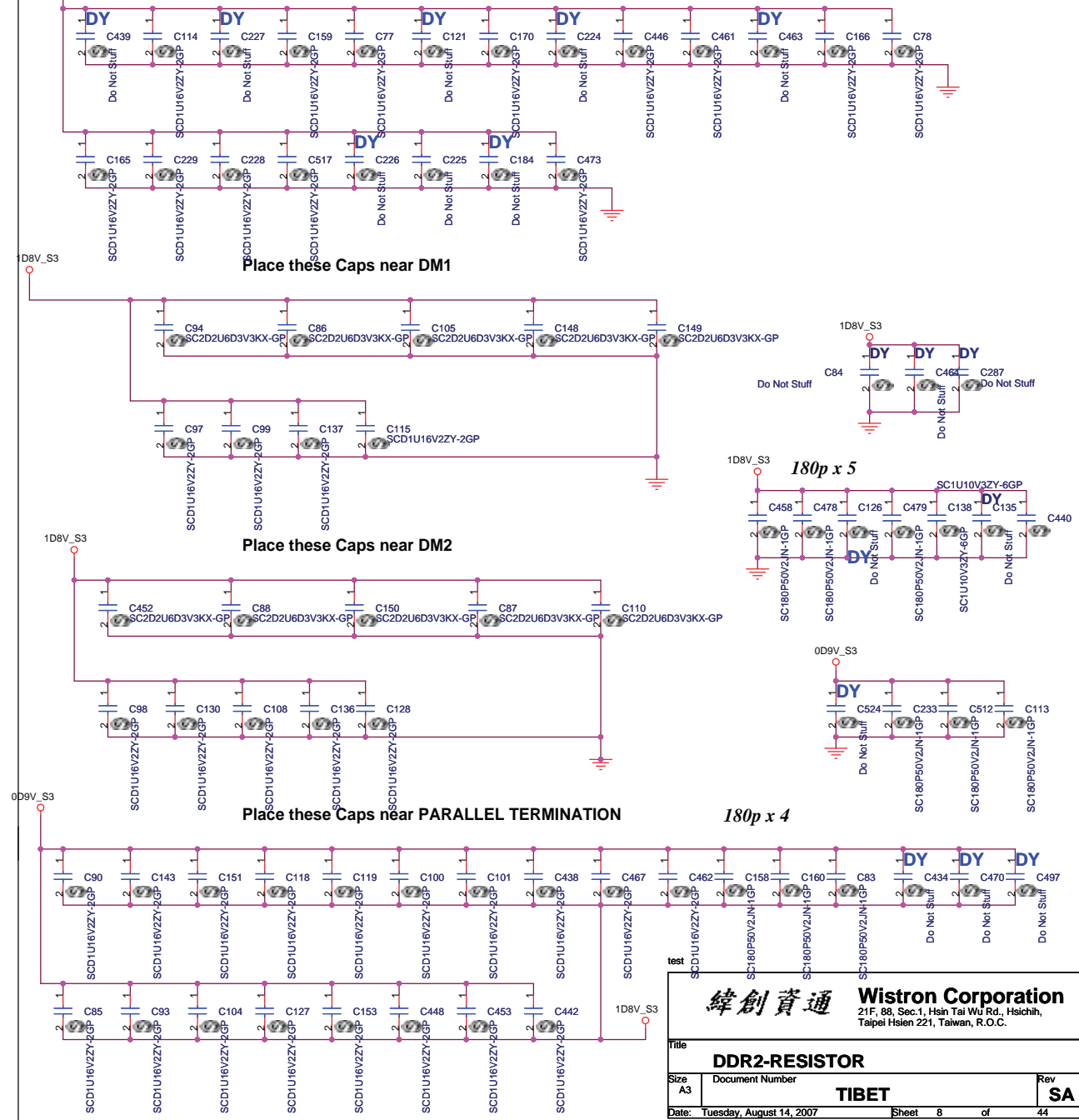
M_B_BS#1 4,7
M_B_RAS# 4,7
M_B_CS0# 4,7

M_B_CKE1 4,7

M_A_ODT1 4,7

Decoupling Capacitor

Put decap near power(0.9V)
and pull-up resistor



0.1u x 15

Place these Caps near DM1

Place these Caps near DM2

Place these Caps near PARALLEL TERMINATION



180p x 5

180p x 4

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR2-RESISTOR	
Size	Document Number	Rev
A3	TIBET	SA
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 CPUCADOUT[15..0] 3
 CPUCADOUTJ[15..0] 3

3 NB0CADOUT[15..0] 
 3 NB0CADOUTJ[15..0] 

U55A 1 OF 8

HT

CPUCADOUT0	AF16	HT_MCP_RXD0_P
CPUCADOUTJ0	AG16	HT_MCP_RXD0_N
CPUCADOUT1	AH16	HT_MCP_RXD1_P
CPUCADOUTJ1	AJ16	HT_MCP_RXD1_N
CPUCADOUT2	AJ15	HT_MCP_RXD2_P
CPUCADOUTJ2	AK15	HT_MCP_RXD2_N
CPUCADOUT3	AK16	HT_MCP_RXD3_P
CPUCADOUTJ3	AL16	HT_MCP_RXD3_N
CPUCADOUT4	AG17	HT_MCP_RXD4_P
CPUCADOUTJ4	AF17	HT_MCP_RXD4_N
CPUCADOUT5	AL17	HT_MCP_RXD5_P
CPUCADOUTJ5	AK17	HT_MCP_RXD5_N
CPUCADOUT6	AL18	HT_MCP_RXD6_P
CPUCADOUTJ6	AK18	HT_MCP_RXD6_N
CPUCADOUT7	AJ19	HT_MCP_RXD7_P
CPUCADOUTJ7	AK19	HT_MCP_RXD7_N
CPUCADOUT8	AD14	HT_MCP_RXD8_P
CPUCADOUTJ8	AE14	HT_MCP_RXD8_N
CPUCADOUT9	AF14	HT_MCP_RXD9_P
CPUCADOUTJ9	AG14	HT_MCP_RXD9_N
CPUCADOUT10	AH14	HT_MCP_RXD10_P
CPUCADOUTJ10	AJ14	HT_MCP_RXD10_N
CPUCADOUT11	AL13	HT_MCP_RXD11_P
CPUCADOUTJ11	AK13	HT_MCP_RXD11_N
CPUCADOUT12	AC15	HT_MCP_RXD12_P
CPUCADOUTJ12	AD15	HT_MCP_RXD12_N
CPUCADOUT13	AD16	HT_MCP_RXD13_P
CPUCADOUTJ13	AE16	HT_MCP_RXD13_N
CPUCADOUT14	AE17	HT_MCP_RXD14_P
CPUCADOUTJ14	AD17	HT_MCP_RXD14_N
CPUCADOUT15	AB17	HT_MCP_RXD15_P
CPUCADOUTJ15	AC17	HT_MCP_RXD15_N

HT_MCP_TXD0_P	AK27	NB0CADOUT0
HT_MCP_TXD0_N	AJ27	NB0CADOUTJ0
HT_MCP_TXD1_P	AK26	NB0CADOUT1
HT_MCP_TXD1_N	AL26	NB0CADOUTJ1
HT_MCP_TXD2_P	AK25	NB0CADOUT2
HT_MCP_TXD2_N	AL25	NB0CADOUTJ2
HT_MCP_TXD3_P	AK24	NB0CADOUT3
HT_MCP_TXD3_N	AK22	NB0CADOUT4
HT_MCP_TXD4_P	AL22	NB0CADOUTJ4
HT_MCP_TXD5_P	AK21	NB0CADOUT5
HT_MCP_TXD5_N	AL21	NB0CADOUTJ5
HT_MCP_TXD6_P	AJ21	NB0CADOUT6
HT_MCP_TXD6_N	AL20	NB0CADOUTJ6
HT_MCP_TXD7_P	AM20	NB0CADOUT7
HT_MCP_TXD7_N	AG27	NB0CADOUT8
HT_MCP_TXD8_P	AH27	NB0CADOUTJ8
HT_MCP_TXD8_N	AE25	NB0CADOUT9
HT_MCP_TXD9_P	AG25	NB0CADOUTJ9
HT_MCP_TXD9_N	AH25	NB0CADOUT10
HT_MCP_TXD10_P	AJ25	NB0CADOUT11
HT_MCP_TXD10_N	AE23	NB0CADOUTJ11
HT_MCP_TXD11_P	AE23	NB0CADOUT12
HT_MCP_TXD11_N	AD21	NB0CADOUTJ12
HT_MCP_TXD12_P	AE21	NB0CADOUT13
HT_MCP_TXD12_N	AG21	NB0CADOUTJ13
HT_MCP_TXD13_P	AC20	NB0CADOUT14
HT_MCP_TXD13_N	AD20	NB0CADOUTJ14
HT_MCP_TXD14_P	AE19	NB0CADOUT15
HT_MCP_TXD14_N	AE19	NB0CADOUTJ15

3 CPUHTCLKOUT0 >>> CPUHTCLKOUT0 AJ17 HT_MCP_RX_CLK0_P
 3 CPUHTCLKOUTJ0 >>> CPUHTCLKOUTJ0 AH17 HT_MCP_RX_CLK0_N
 3 CPUHTCLKOUT1 >>> CPUHTCLKOUT1 AL14 HT_MCP_RX_CLK1_P
 3 CPUHTCLKOUTJ1 >>> CPUHTCLKOUTJ1 AK14 HT_MCP_RX_CLK1_N

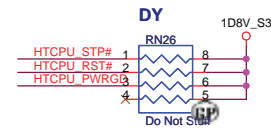
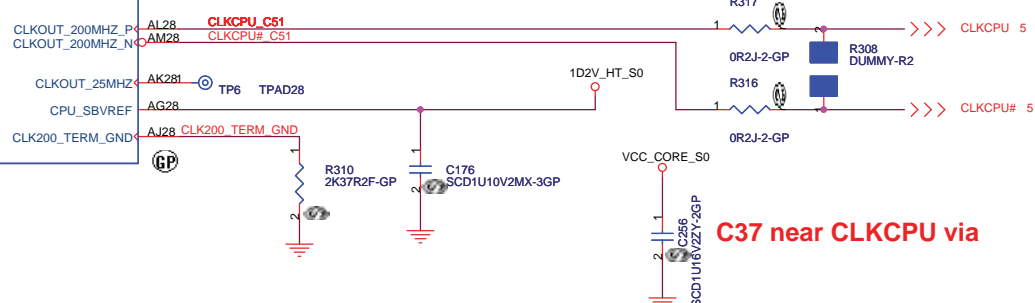
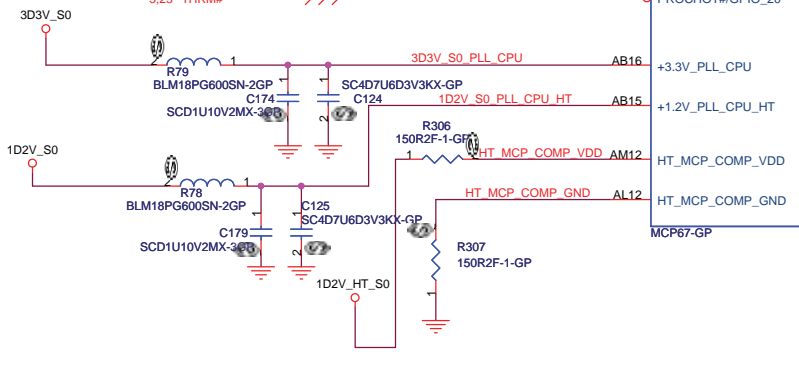
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 NB0HTTCLKOUTJ0 3 >>> NB0HTTCLKOUTJ0 3 AJ23 NB0HTTCLKOUTJ0
 NB0HTTCLKOUT1 3 >>> NB0HTTCLKOUT1 3 AG23 NB0HTTCLKOUT1
 NB0HTTCLKOUTJ1 3 >>> NB0HTTCLKOUTJ1 3 AH23 NB0HTTCLKOUTJ1

3 CPUHTTCTLOUT0 >>> CPUHTTCTLOUT0 AH19 HT_MCP_RXCTL0_P
 3 CPUHTTCTLOUTJ0 >>> CPUHTTCTLOUTJ0 AG19 HT_MCP_RXCTL0_N
 RESERVED#AC18
 RESERVED#AD18

NB0HTTCTLOUT 3 >>> NB0HTTCTLOUT 3 AK20 HT_MCP_TXCTL0_P
 NB0HTTCTLOUTJ 3 >>> NB0HTTCTLOUTJ 3 AJ20 HT_MCP_TXCTL0_N
 RESERVED#AD19
 RESERVED#AC19

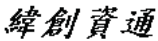
5 CPU_THERMTRIP# >>> THERMTRIP#/GPIO_58 AC13
 5.23 THRM# >>> PROCHOT#/GPIO_20 AB13

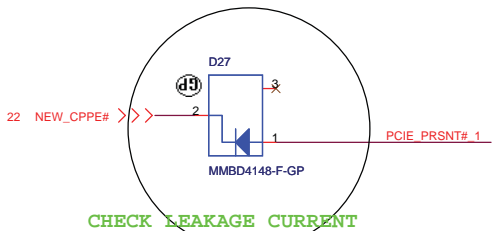
HT_CPU_REQ# >>> HT_CPU_REQ# AD23
 HT_MCP_STOP# >>> HT_MCP_STOP# AB20
 HT_MCP_RST# >>> HT_MCP_RST# AC21
 HT_MCP_PWRGD >>> HT_MCP_PWRGD AD22



C37 near CLKCPU via

test

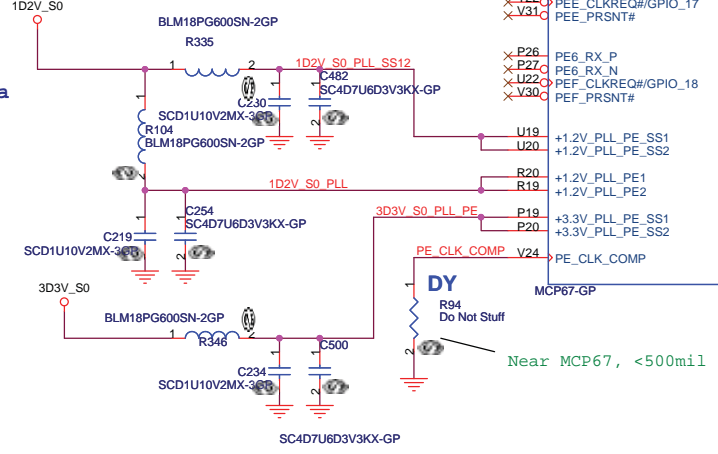
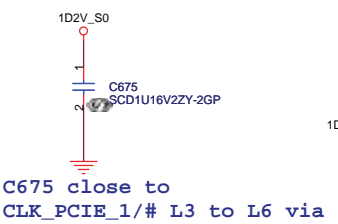
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MCP67(1/8) HT CPU	
Size A3	Document Number TIBET
Date: Tuesday, August 14, 2007	Sheet 9 of 44
Rev SA	



NEW CARD

MINI CARD1

MINI CARD2



U55B 2 OF 8

PCIE

F23	PE0_RX0_P	D24	PE0_TX0_P
G23C	PE0_RX0_N	C24	PE0_TX0_N
F24	PE0_RX1_P	A24	PE0_TX1_P
F25C	PE0_RX1_N	B24	PE0_TX1_N
D25	PE0_RX2_P	B25	PE0_TX2_P
D26C	PE0_RX2_N	C25	PE0_TX2_N
C28	PE0_RX3_P	B26	PE0_TX3_P
D28C	PE0_RX3_N	C26	PE0_TX3_N
C29	PE0_RX4_P	C27	PE0_TX4_P
C30	PE0_RX4_N	D27	PE0_TX4_N
D29	PE0_RX5_P	A28	PE0_TX5_P
D30C	PE0_RX5_N	B28	PE0_TX5_N
F28	PE0_RX6_P	A29	PE0_TX6_P
F27C	PE0_RX6_N	B29	PE0_TX6_N
F29	PE0_RX7_P	A30	PE0_TX7_P
H23	PE0_RX8_P	B30	PE0_TX7_N
H24C	PE0_RX8_N	B31	PE0_TX8_P
H25	PE0_RX9_P	B32	PE0_TX8_N
H26C	PE0_RX9_N	C31	PE0_TX9_P
H27	PE0_RX10_P	C32	PE0_TX9_N
H28C	PE0_RX10_N	D31	PE0_TX10_P
K24	PE0_RX11_P	D32	PE0_TX10_N
K25C	PE0_RX11_N	E31	PE0_TX11_P
K27	PE0_RX12_P	E30	PE0_TX11_N
K28C	PE0_RX12_N	F31	PE0_TX12_P
K29	PE0_RX13_P	F30	PE0_TX12_N
J31	PE0_RX13_N	G29	PE0_TX13_P
J30C	PE0_RX14_P	G30	PE0_TX13_N
K31	PE0_RX14_N	H29	PE0_TX14_P
K30C	PE0_RX15_P	H30	PE0_TX14_N
	PE0_RX15_N	H32	PE0_TX15_P
		H31	PE0_TX15_N
		R29	PE0_REFCLK_P
		R30	PE0_REFCLK_N
H17C	PE_WAKE#/GPIO_21		
U31	PE0_PRSNTX1#/DDC_CLK1		
U30C	PE0_PRSNTX4#/DDC_DATA1		
U29	PE0_PRSNTX8#/EXP_EN		
U28C	PE0_PRSNTX16#		
L29	PE1_RX_P	M28	PCIE_TXP1 MCP67 1
L30C	PE1_RX_N	M29	PCIE_TXN1 MCP67 1
W27	PEA_CLKREQ#	T32	PCIE_TXN1 MCP67 1
W28C	PEA_PRSNT#	T31	PCIE_TXN1 MCP67 1
M26	PE2_RX_P		
M27C	PE2_RX_N		
U26	PEB_CLKREQ#		
U27C	PEB_PRSNT#		
N23	PE3_RX_P		
N22C	PE3_RX_N		
U25	PEC_CLKREQ#		
U24C	PEC_PRSNT#		
N30	PE4_RX_P		
N31C	PE4_RX_N		
R22	PE4_CLKREQ#/GPIO_16		
U23C	PE4_PRSNT#		
P31	PE5_RX_P		
P30C	PE5_RX_N		
J22	PEE_CLKREQ#/GPIO_17		
V31C	PEE_PRSNT#		
P26	PE6_RX_P		
P27C	PE6_RX_N		
U22	PEF_CLKREQ#/GPIO_18		
V30C	PEF_PRSNT#		
U19	+1.2V_PLL_PE_SS1		
U20C	+1.2V_PLL_PE_SS2		
R20	+1.2V_PLL_PE1		
R19C	+1.2V_PLL_PE2		
P19	+3.3V_PLL_PE_SS1		
P20C	+3.3V_PLL_PE_SS2		
V24	PE_CLK_COMP		
	MCP67-GP		
		M30	PE4_TX_P
		M31	PE4_TX_N
		T25	PE4_REFCLK_P
		T26	PE4_REFCLK_N
		P29	PE5_TX_P
		P28	PE5_TX_N
		T23	PE5_REFCLK_P
		T24	PE5_REFCLK_N
		P24	PE6_TX_P
		P25	PE6_TX_N
		P23	PE6_REFCLK_P
		R23	PE6_REFCLK_N
		W30	PCIE_RST#_NEW 22
		R144	PCIE_RST#_1 27
		W29	PCIE_RST#_2 27
		R143	PCIE_RST#_2 27

Near Connector, <500mil

For New_Card

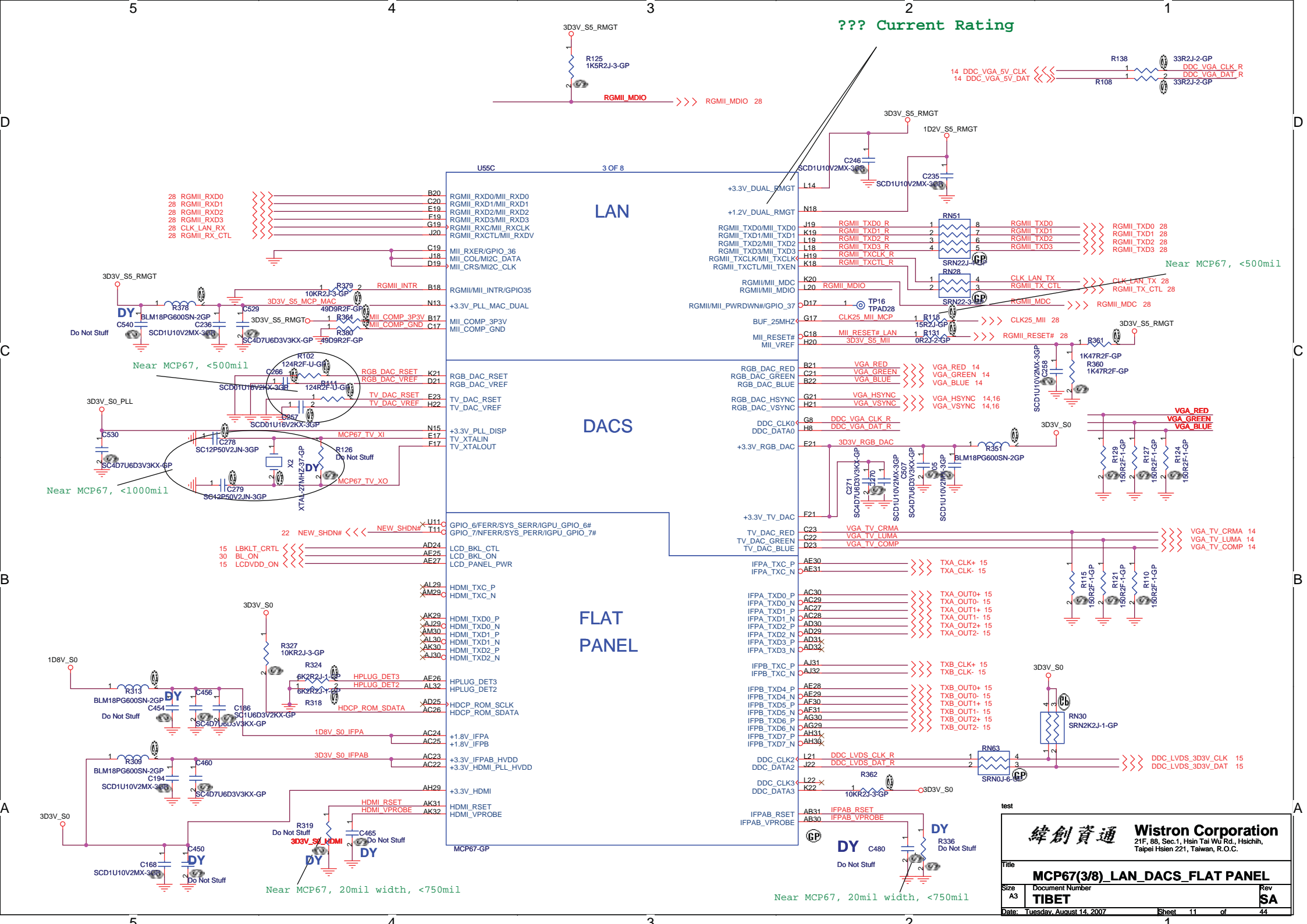
test

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(2/8)_PCIE**

Size: A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 10 of 44



?? Current Rating

LAN

DACS

FLAT PANEL

Near MCP67, <500mil

Near MCP67, <500mil

Near MCP67, <1000mil

Near MCP67, 20mil width, <750mil

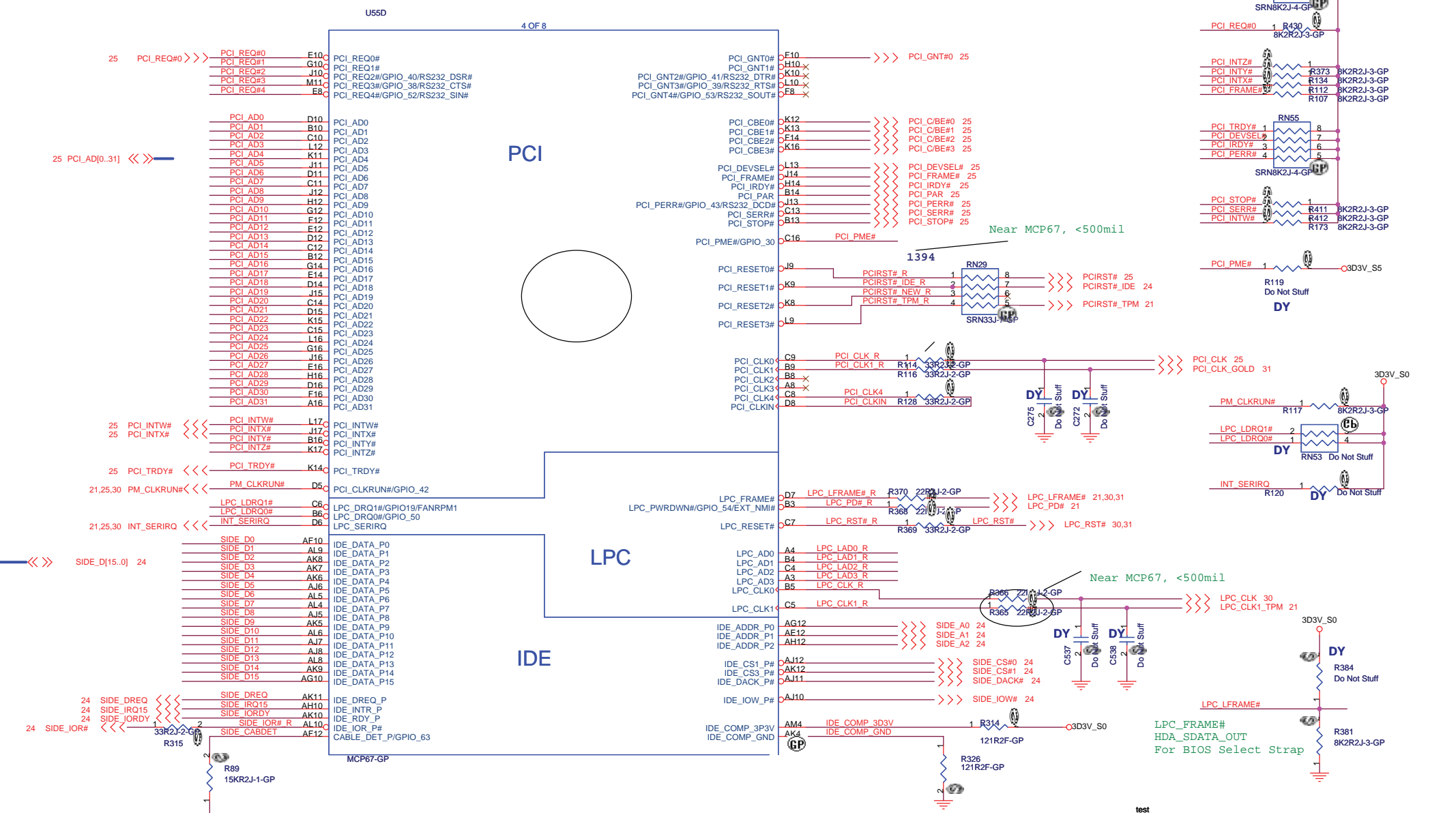
Near MCP67, 20mil width, <750mil

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP67(3/8) LAN DACS FLAT PANEL

Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet: 11 of 44



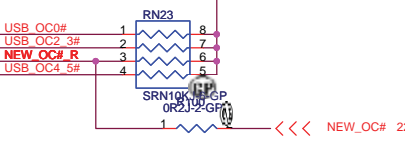
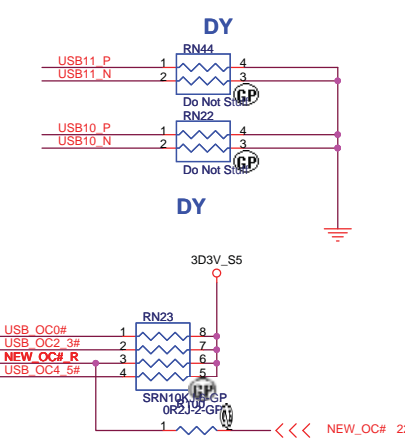
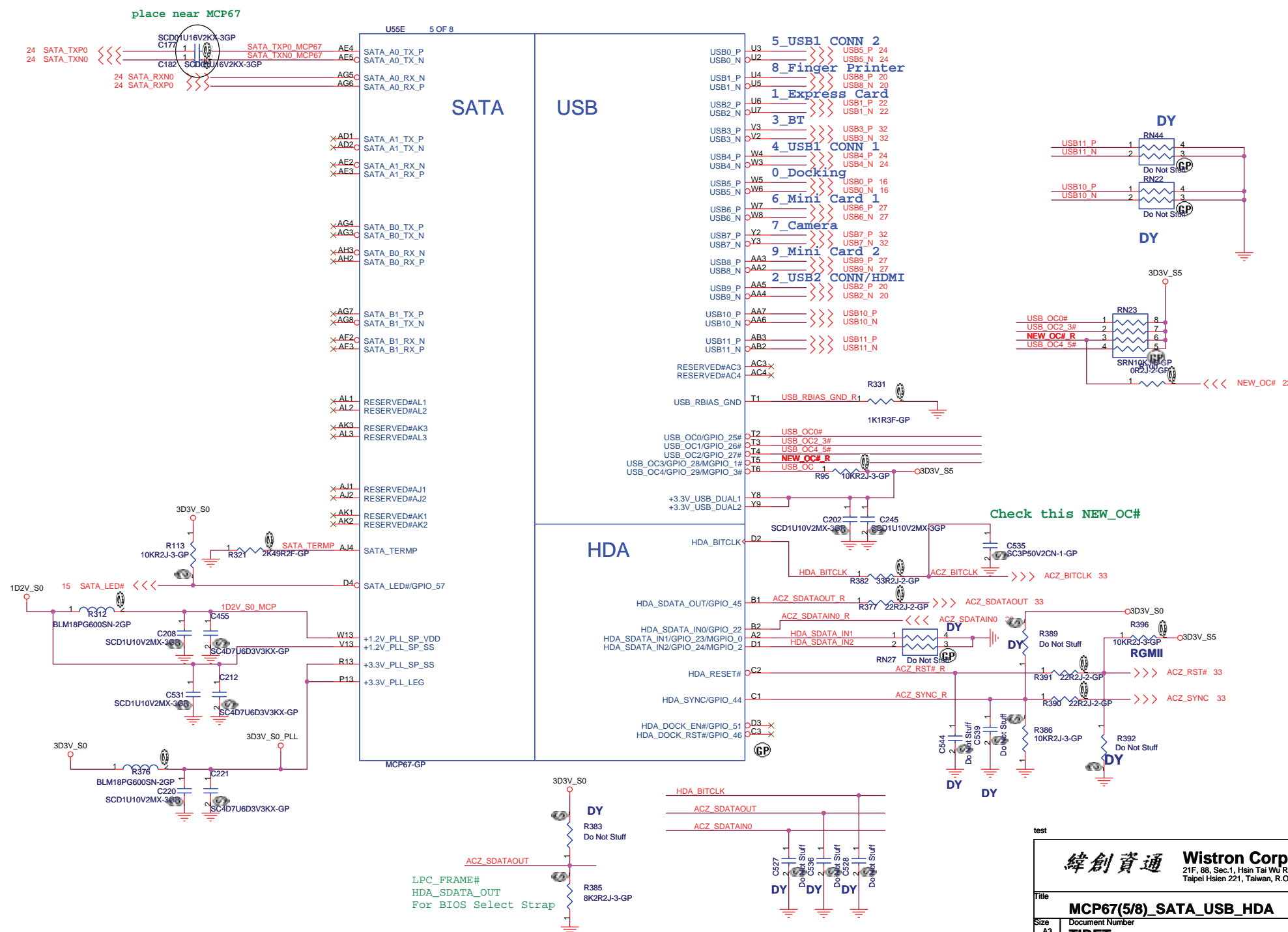
test

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(4/8)_PCI_LPC_IDE**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 12 of 44



Check this NEW_OC#

test

緯創資通 Wistron Corporation
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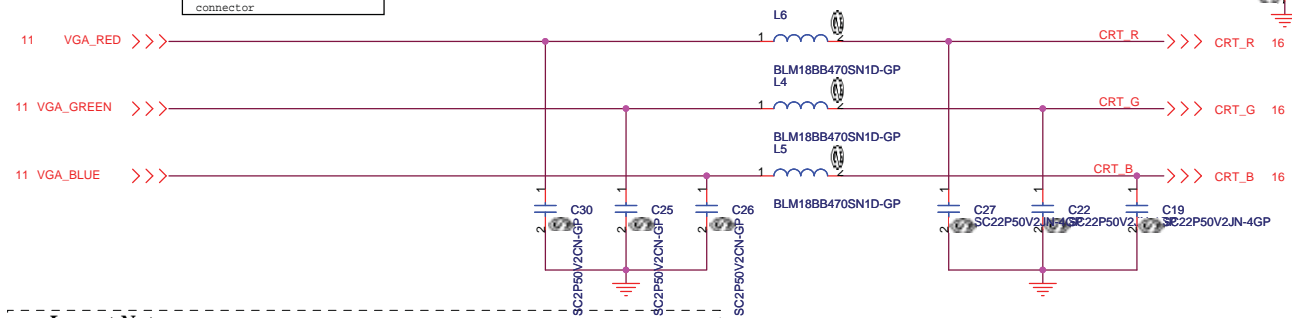
Title: **MCP67(5/8)_SATA_USB_HDA**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 13 of 44

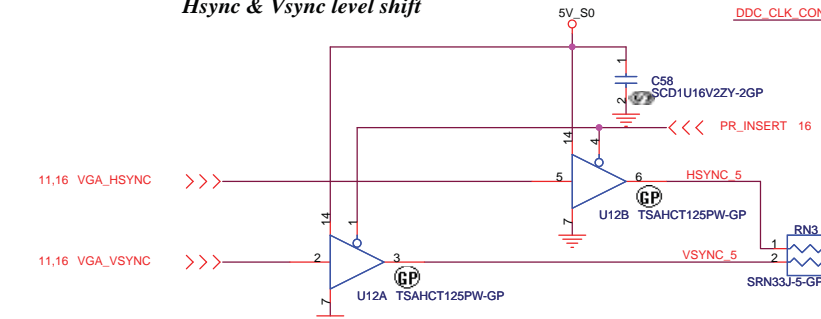
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



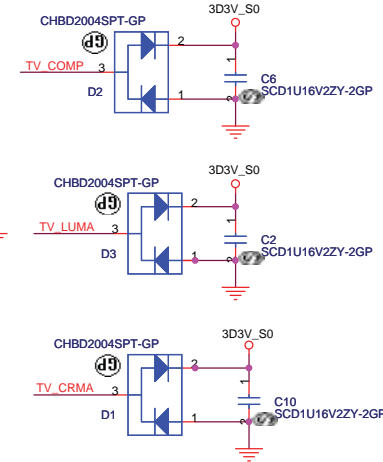
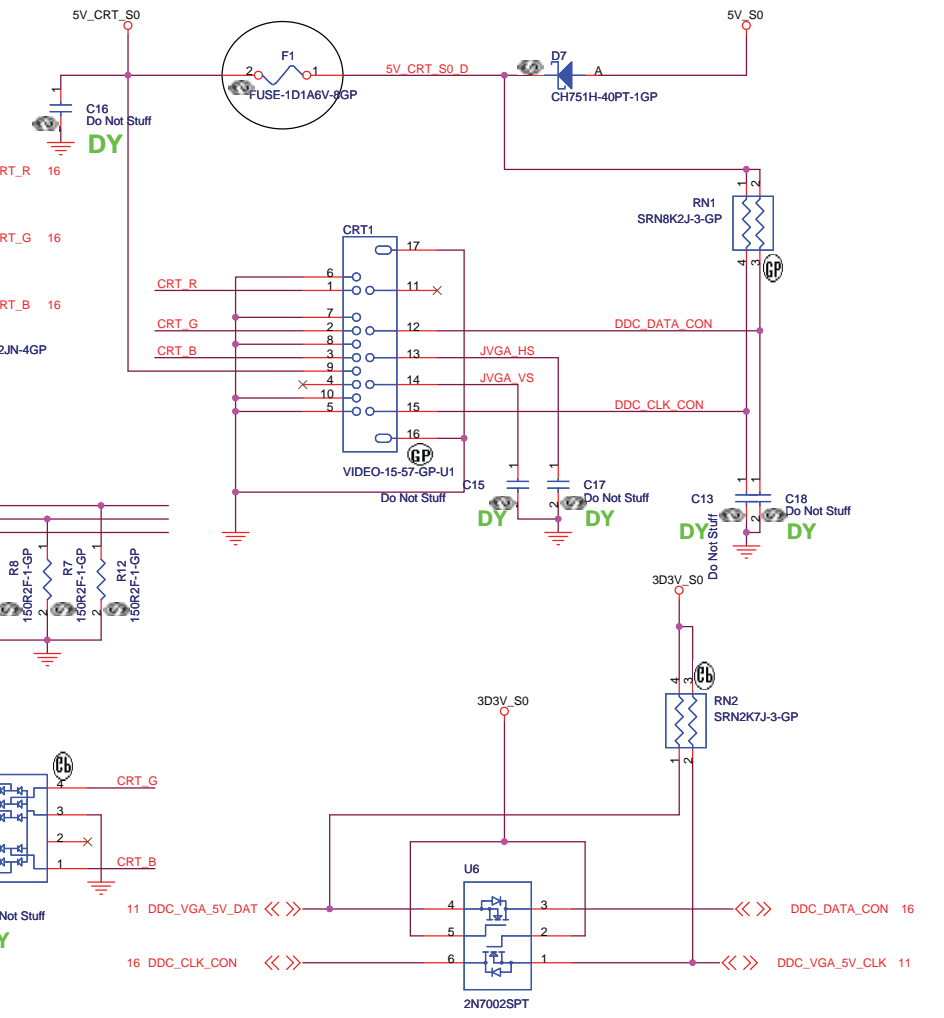
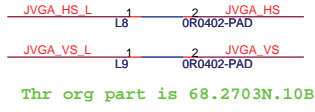
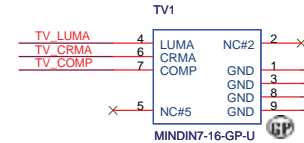
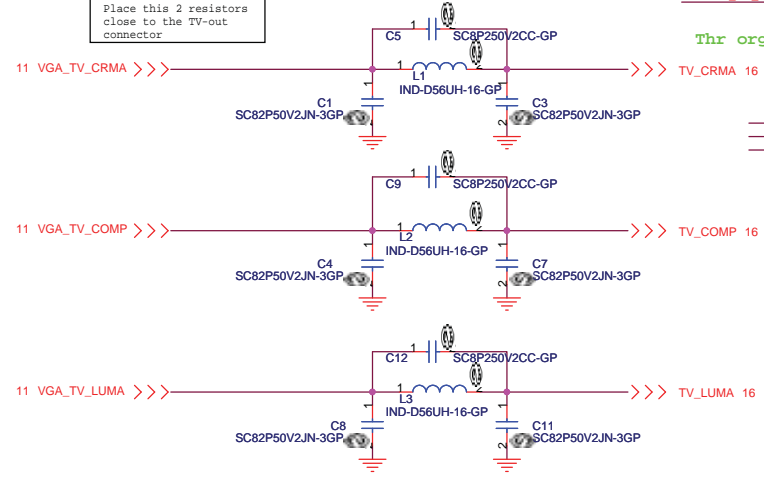
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



5V @ ext. CRT side

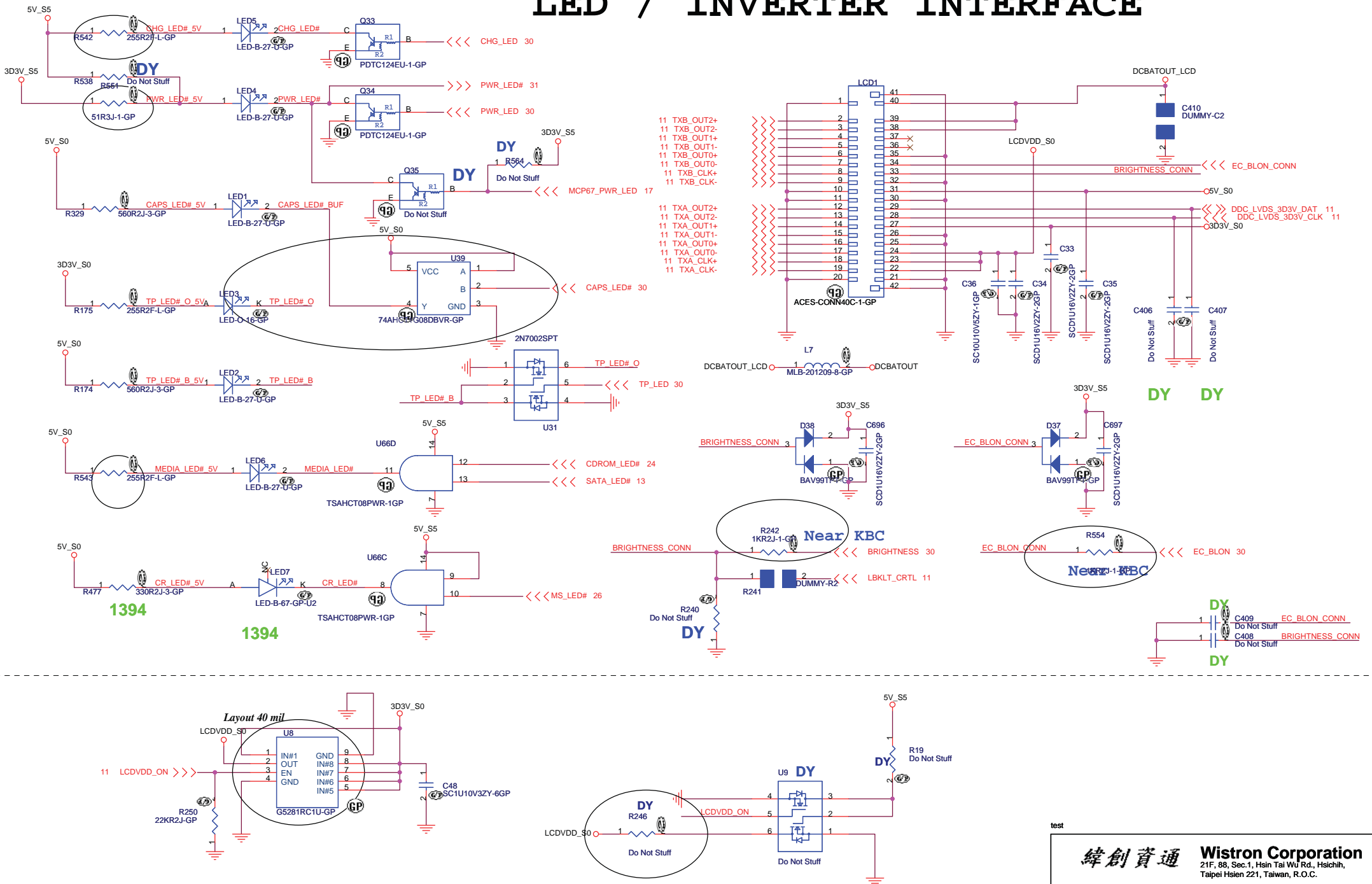
test

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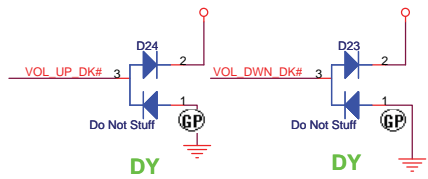
Title: **CRT/TV CONNECTOR**

Size A3	Document Number	Rev SA
TIBET		
Date: Tuesday, August 14, 2007	Sheet 14	of 44

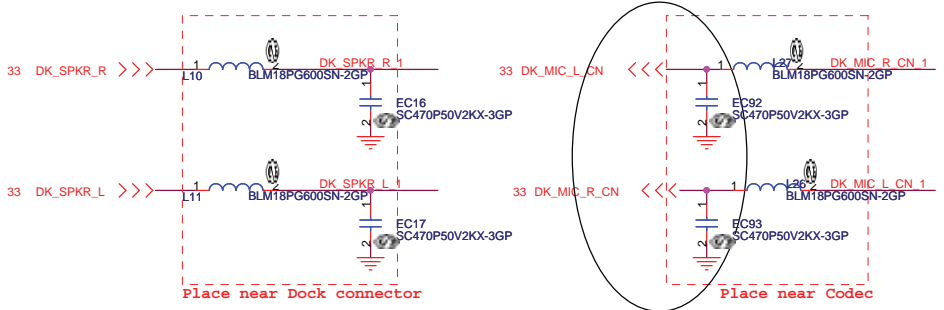
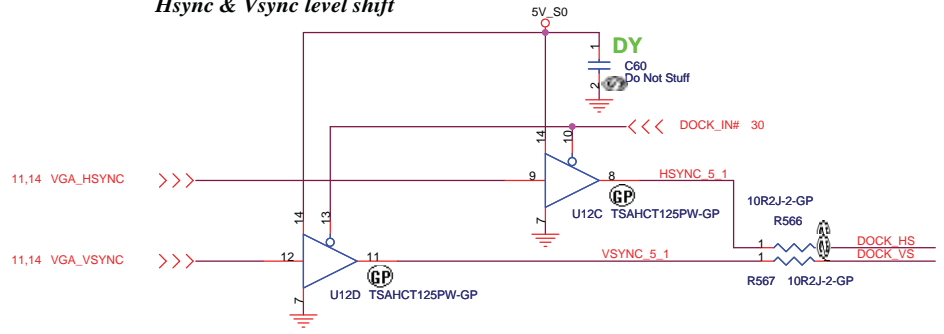
LED / INVERTER INTERFACE



Docking Connector

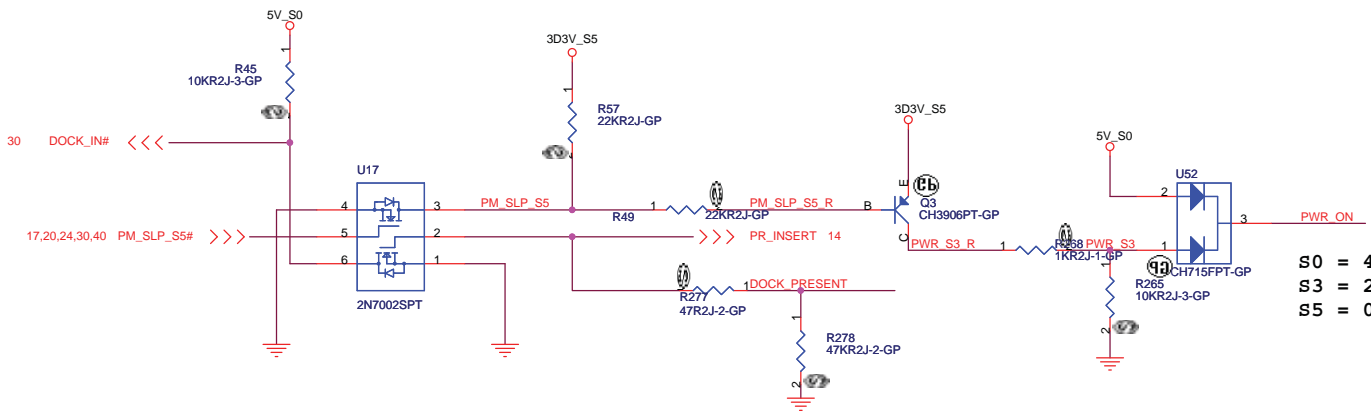
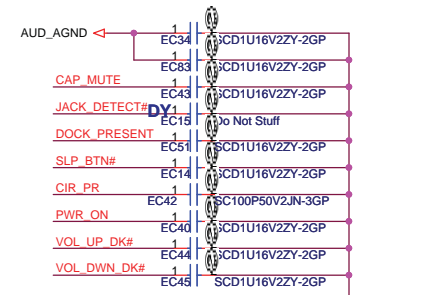
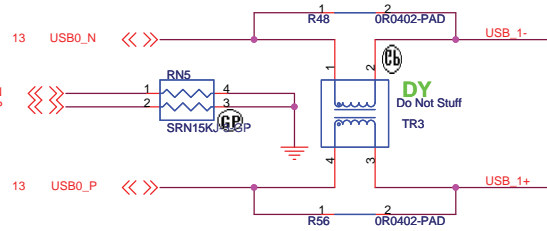
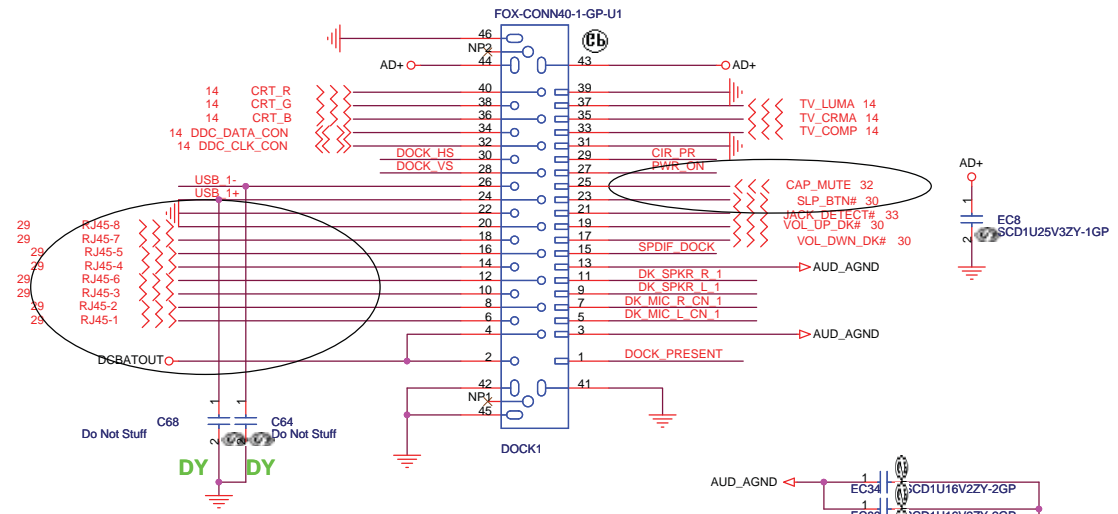


Hsync & Vsync level shift

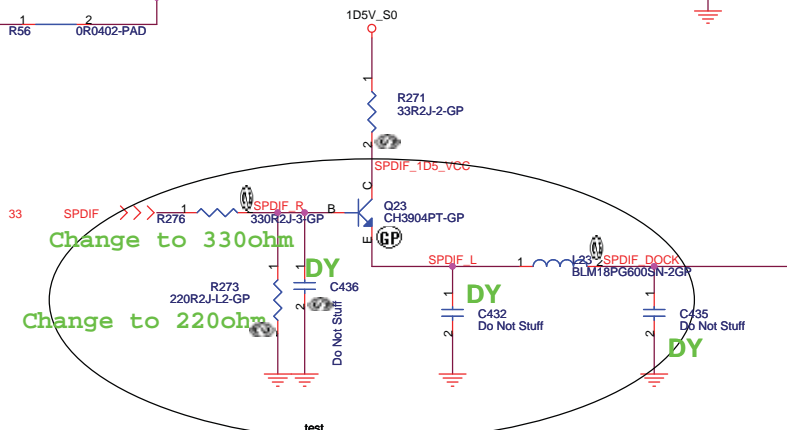


Place near Dock connector

Place near Codec



S0 = 4V
S3 = 2.5V
S5 = 0V



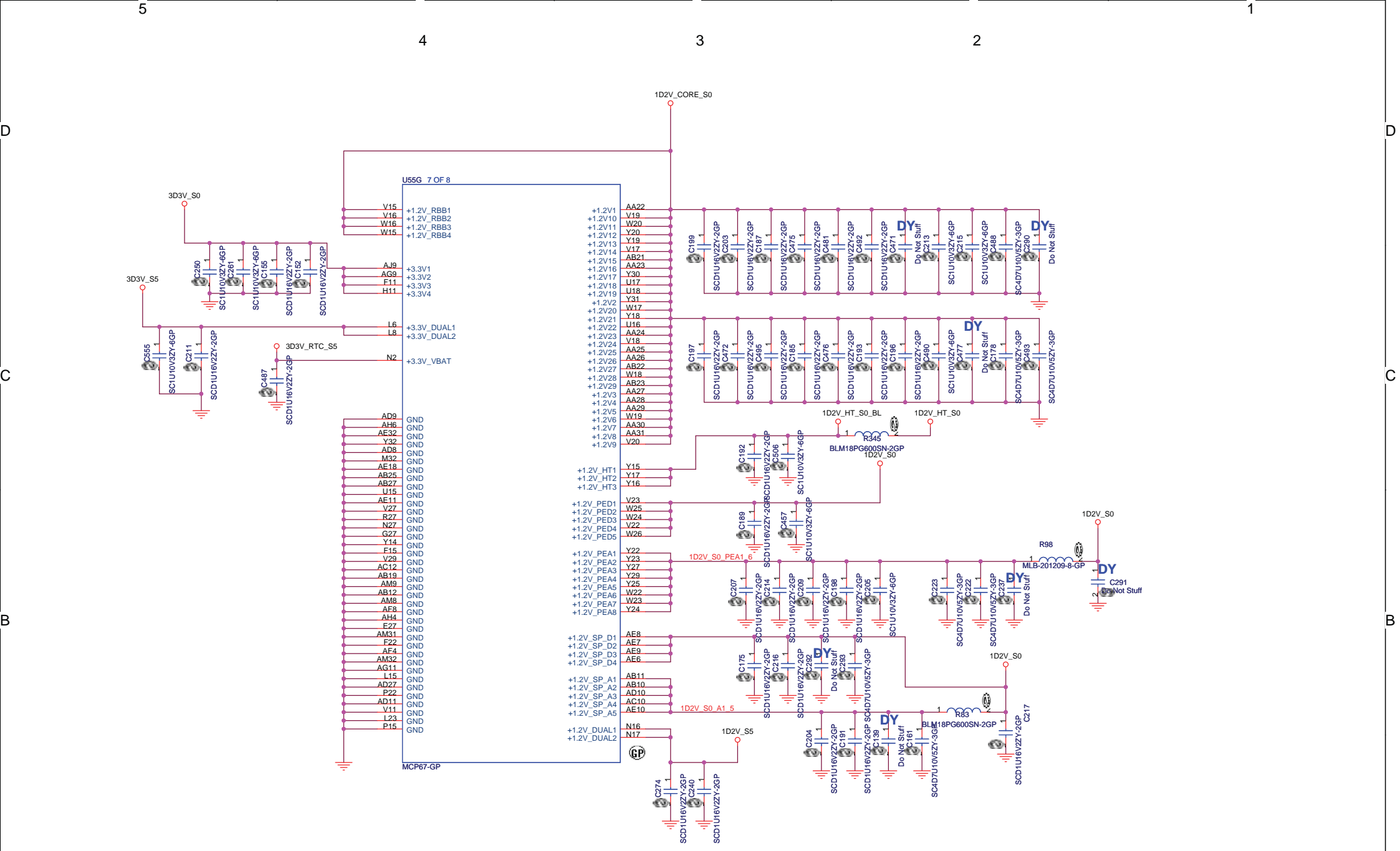
Change to 330ohm
Change to 220ohm

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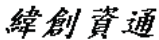
Title: **Board to board conn/ Docking**

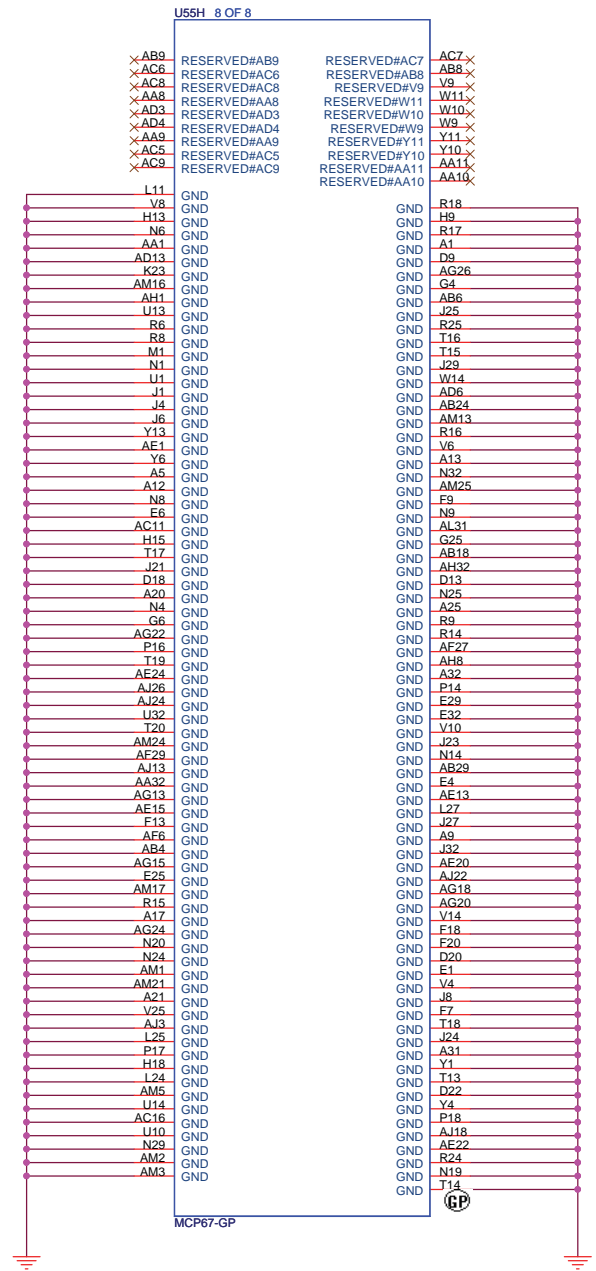
Size: A3 Document Number: **TIBET** Rev: SA

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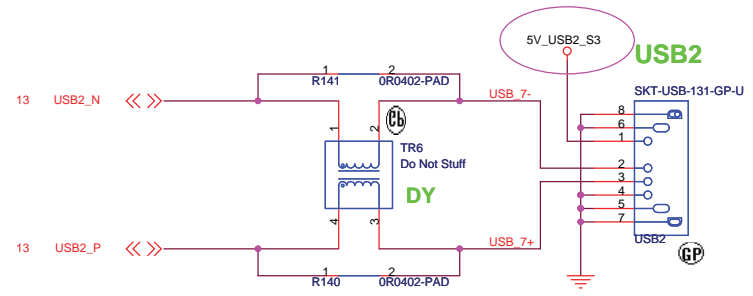
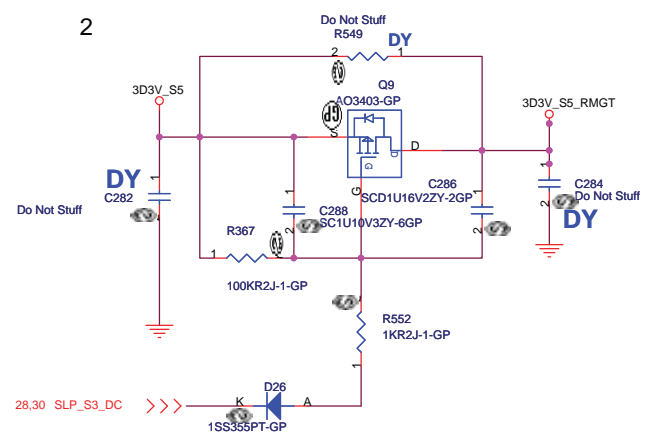
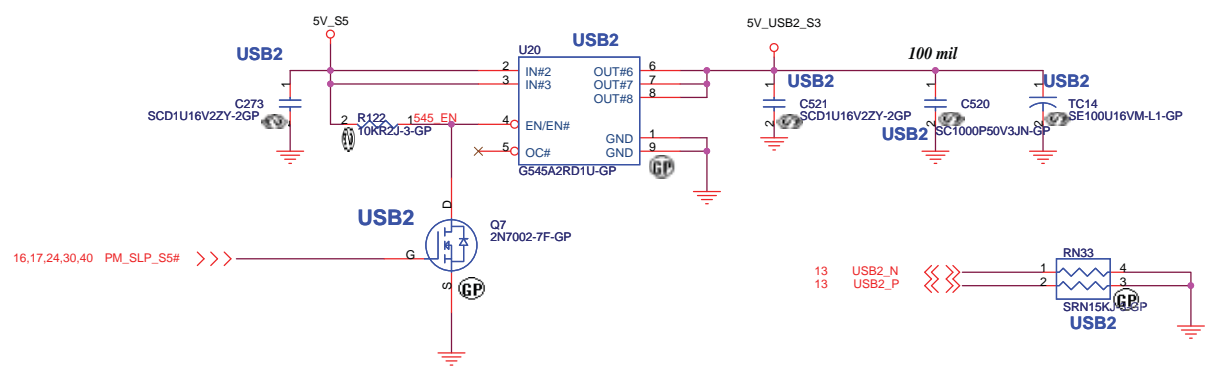
test

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MCP67(7/8)_POWER	
Size	Document Number
A3	TIBET
Date: Tuesday, August 14, 2007	Sheet 18 of 44
Rev	SA

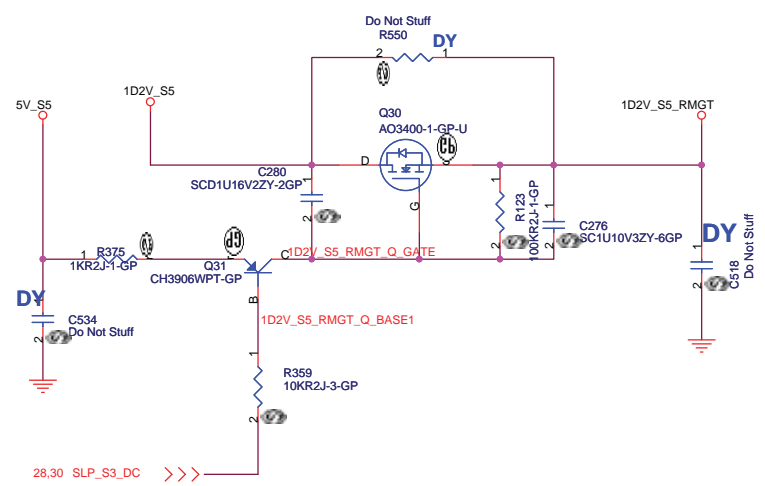


test

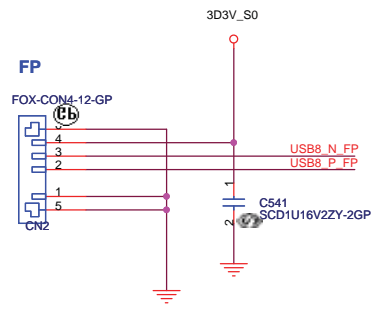
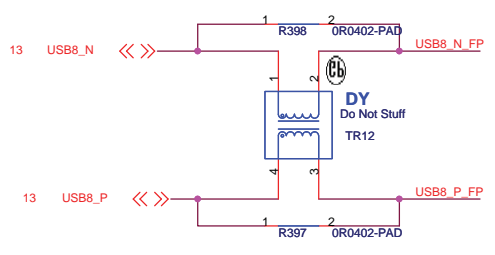
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP67(8/8)_GND			
Size	Document Number		Rev
A3	TIBET		SA
Date: Tuesday, August 14, 2007		Sheet 19 of	44



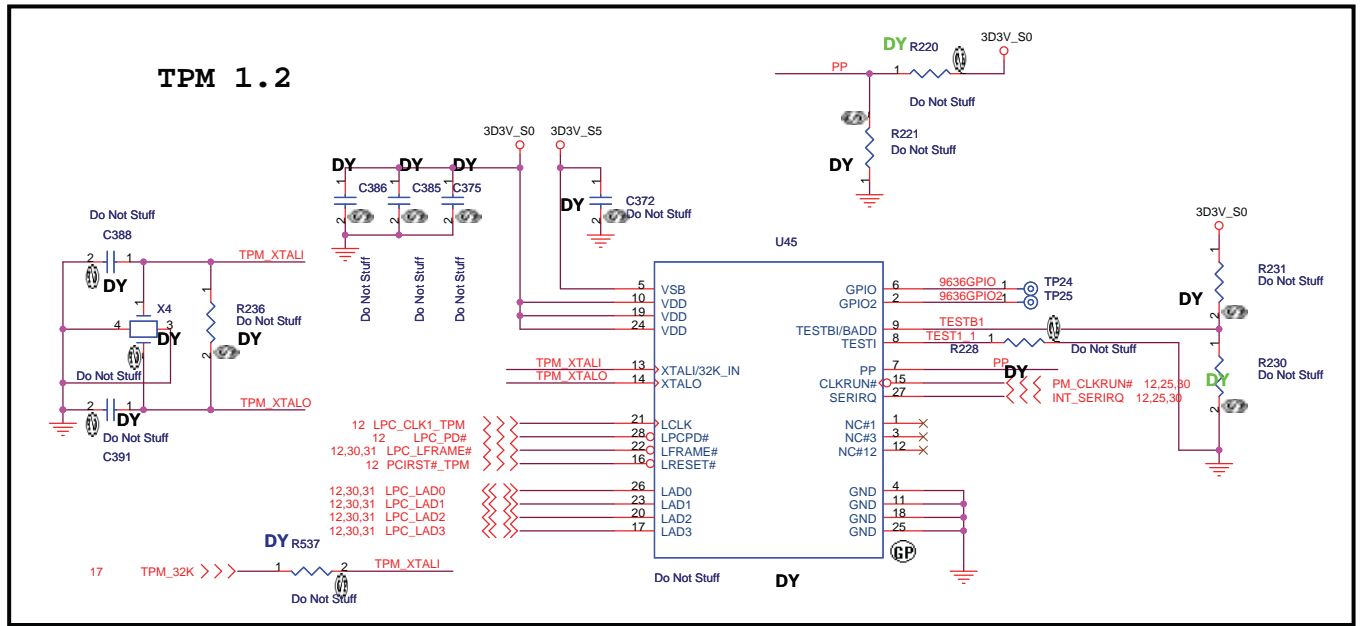
??? Current Rating



Finger Printer



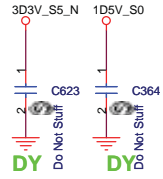
Title		test	
Size		A3	
Document Number		TIBET	
Date		Tuesday, August 14, 2007	
Sheet		20 of 44	
Title		HDMI/FINGER PRINTER	
Rev		SA	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			



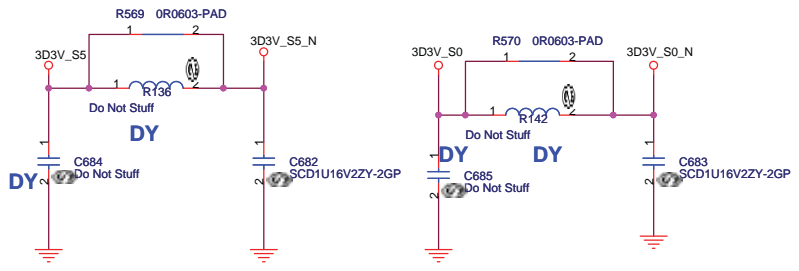
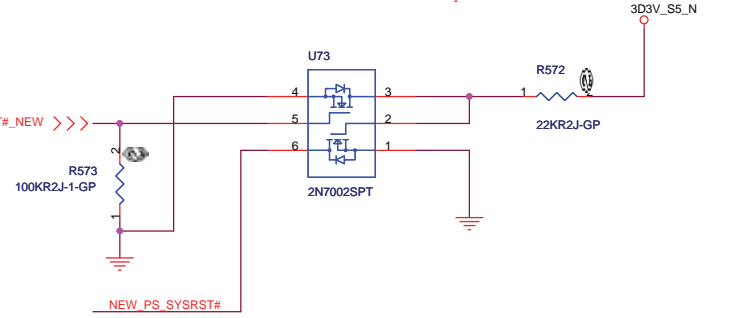
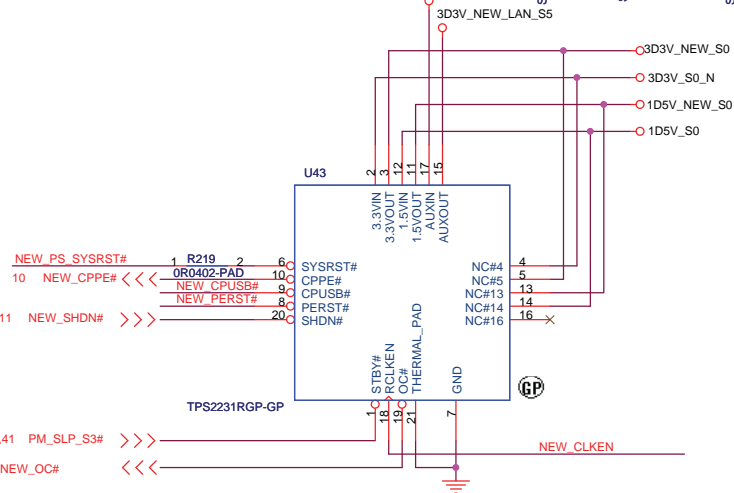
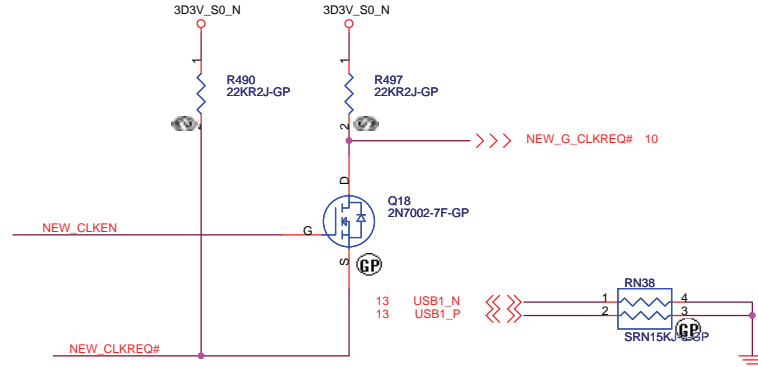
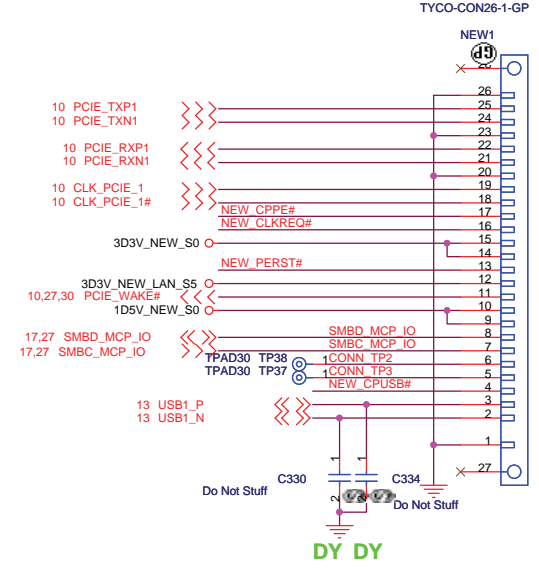
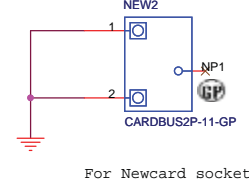
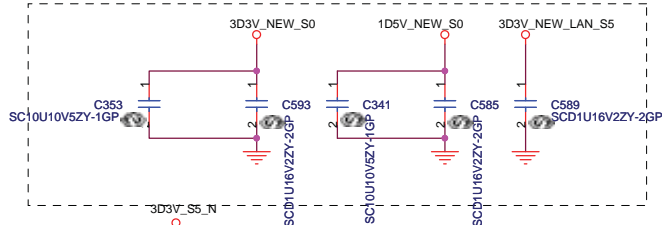
test

NEWCARD Connector

Place them Near to Chip



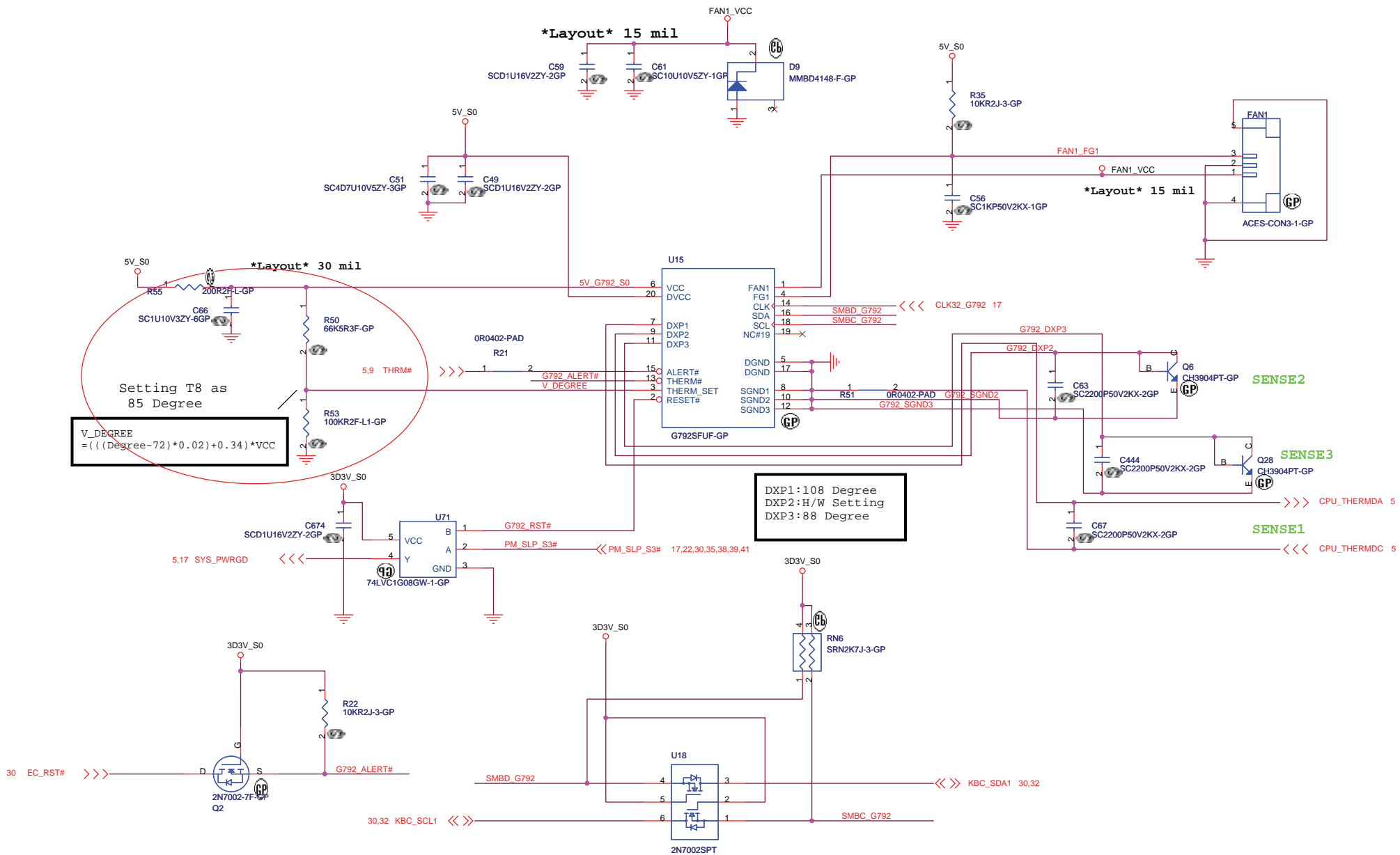
Place them Near to Connector



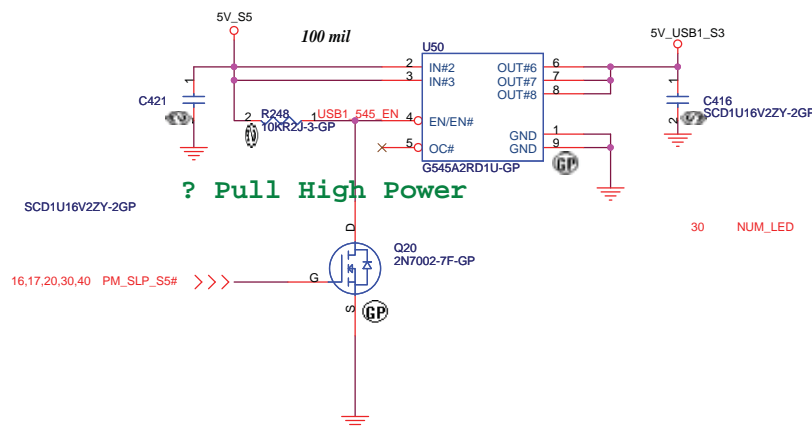
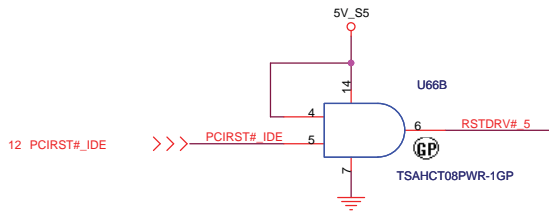
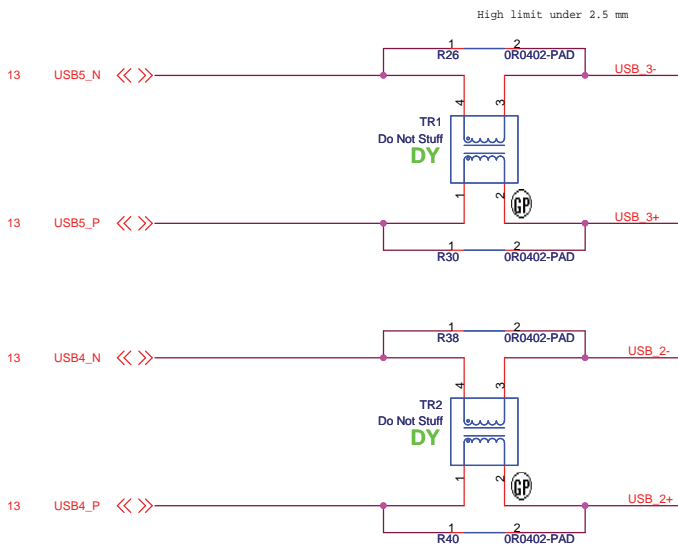
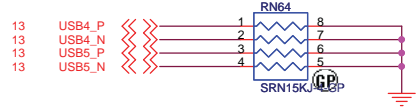
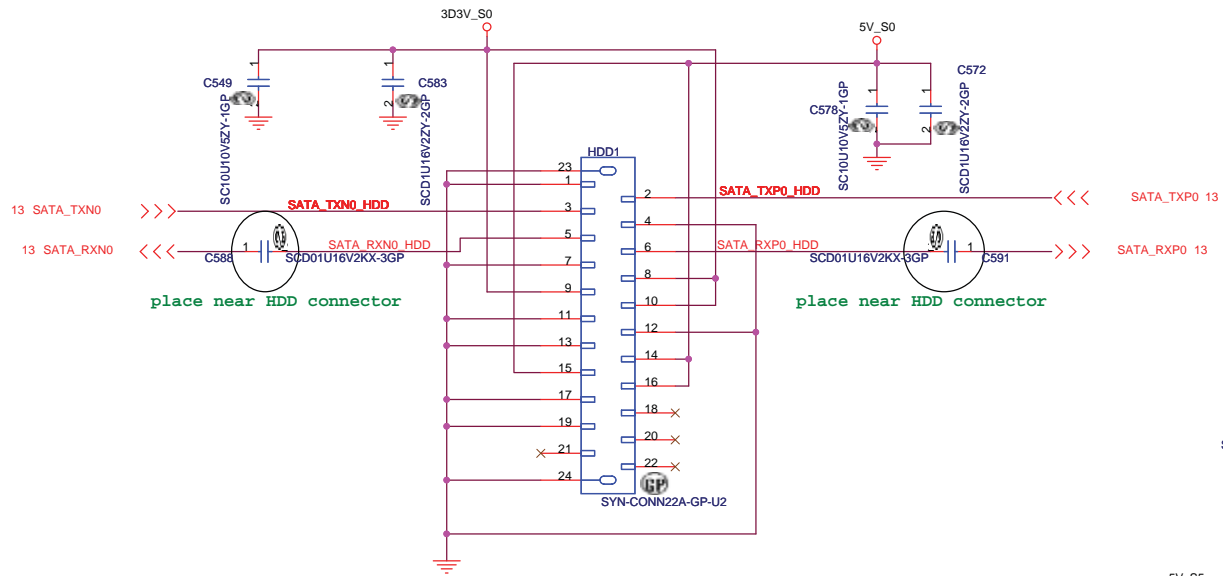
test

緯創資通 Wistron Corporation
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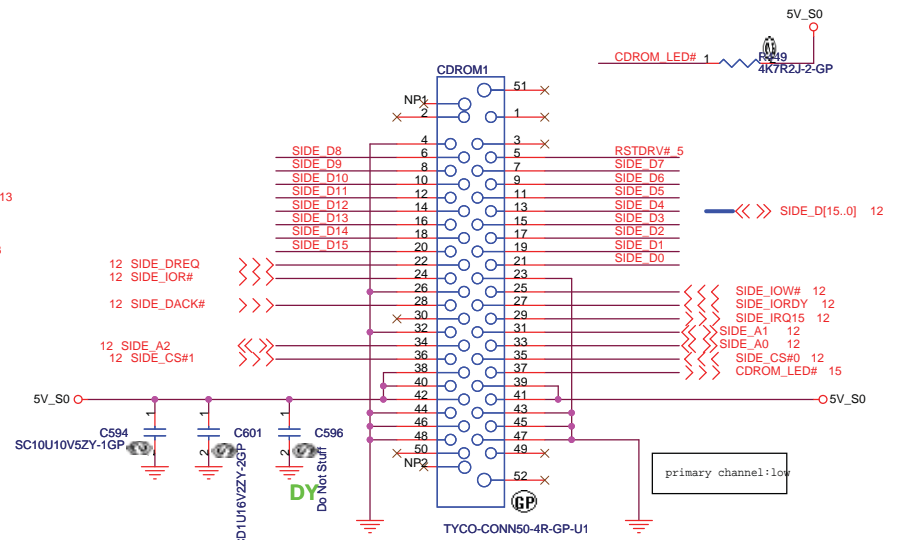
Title NEW CARD		
Size A3	Document Number TIBET	Rev SA
Date: Tuesday, August 14, 2007	Sheet 22	of 44



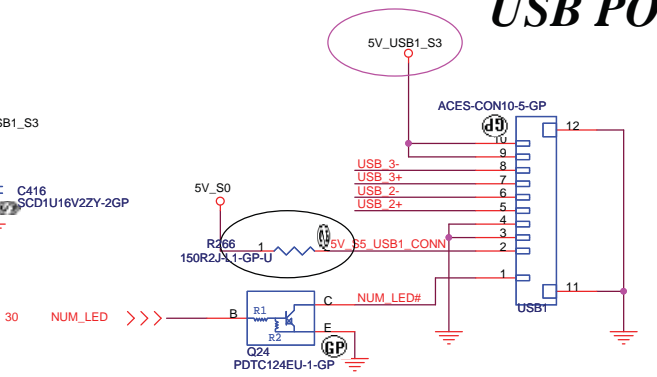
SATA HD Connector

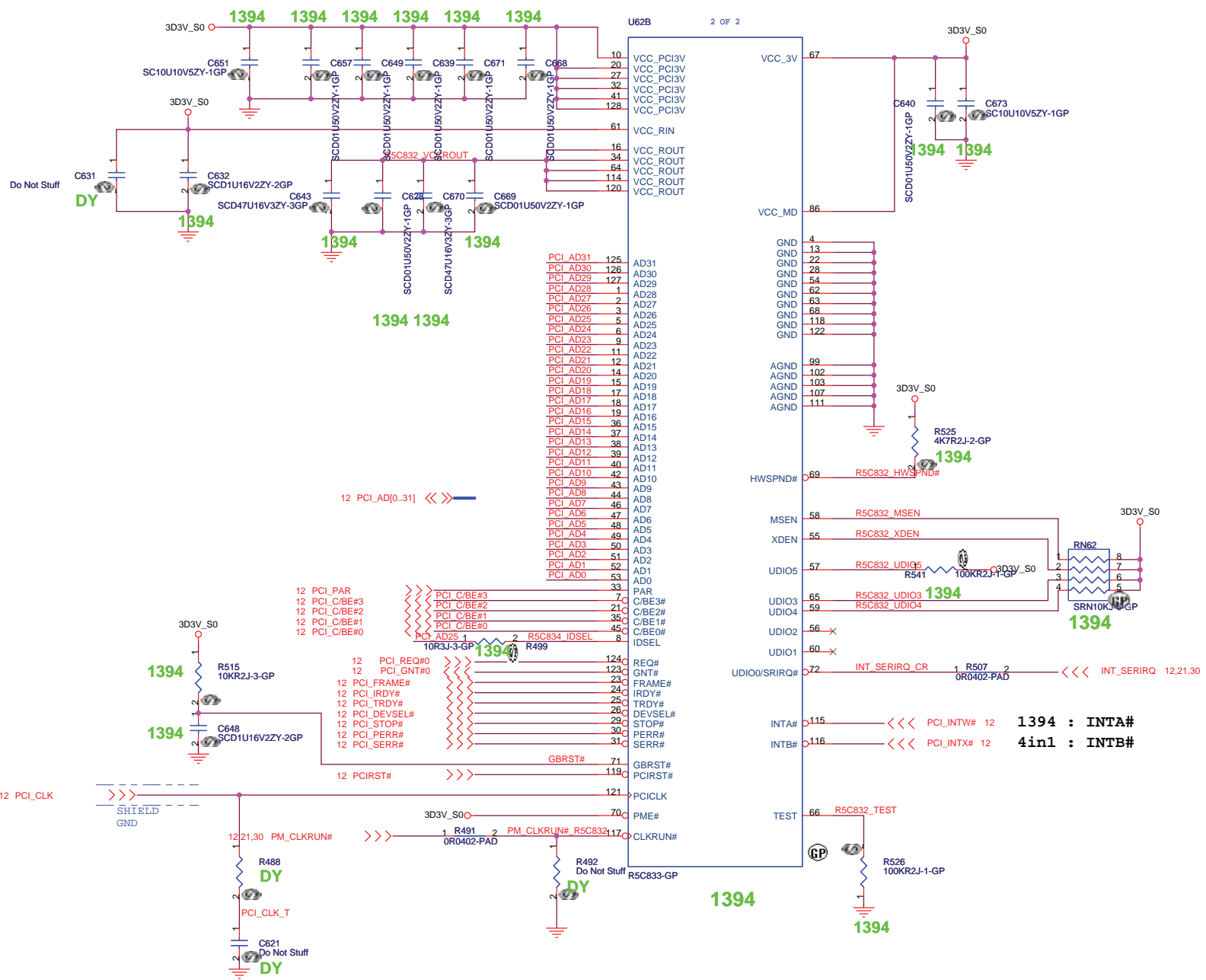


CD-ROM CONNECTOR



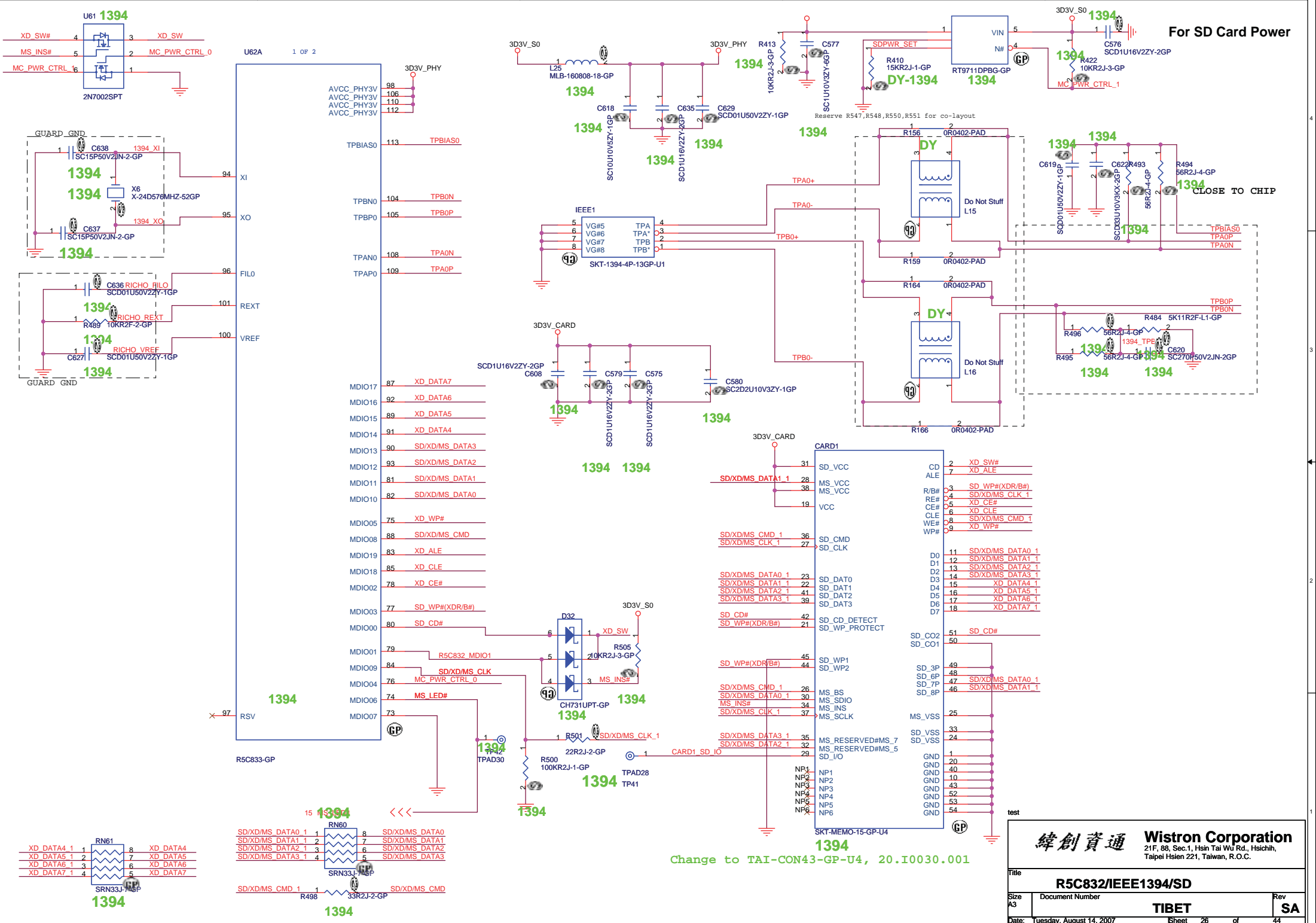
USB PORT





test

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
R5C832/PCI			
Size	Document Number	Rev	
A3	TIBET	SA	
Date: Tuesday, August 14, 2007	Sheet 25	of 44	



For SD Card Power

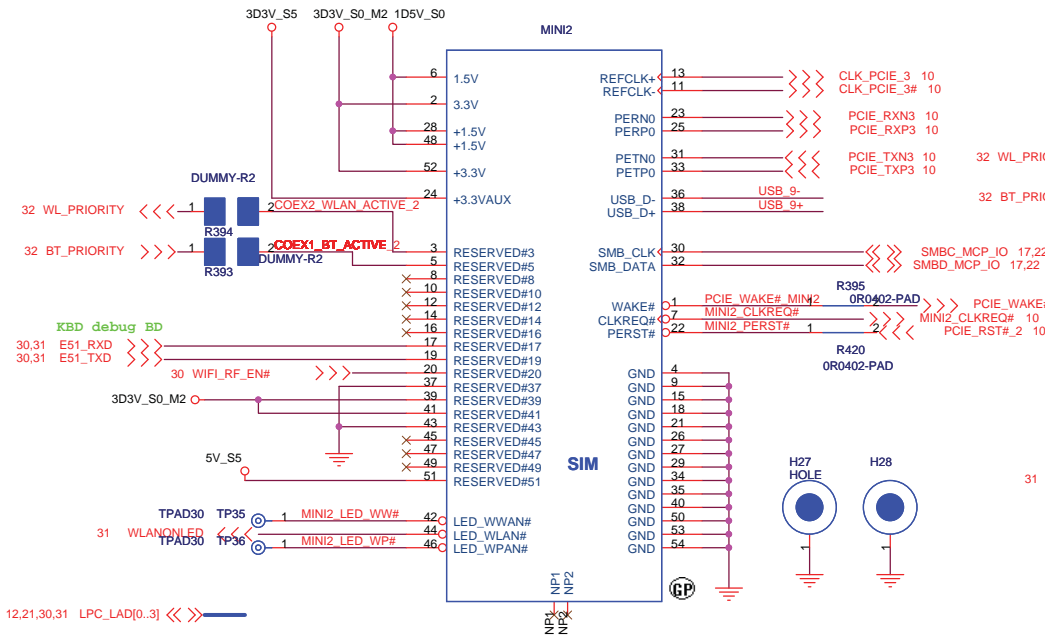
CLOSE TO CHIP

Change to TAI-CON43-GP-U4, 20.I0030.001

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title R5C832/IEEE1394/SD	
Size A3	Document Number TIBET
Date: Tuesday, August 14, 2007	Sheet 26 of 44
Rev SA	

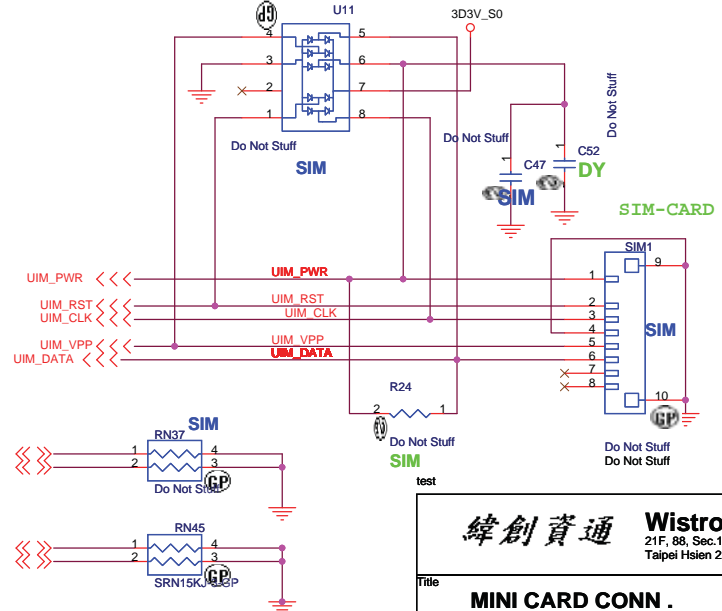
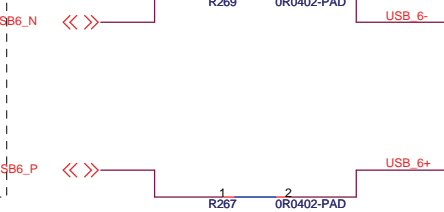
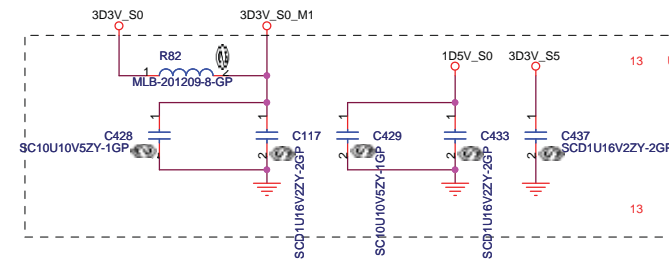
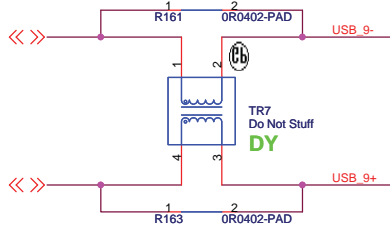
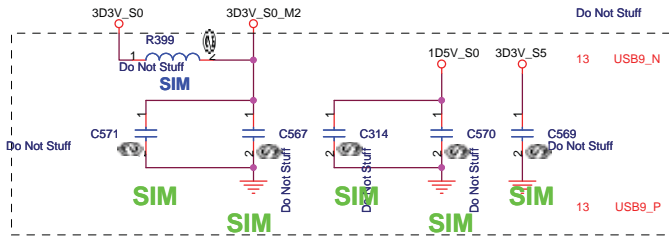
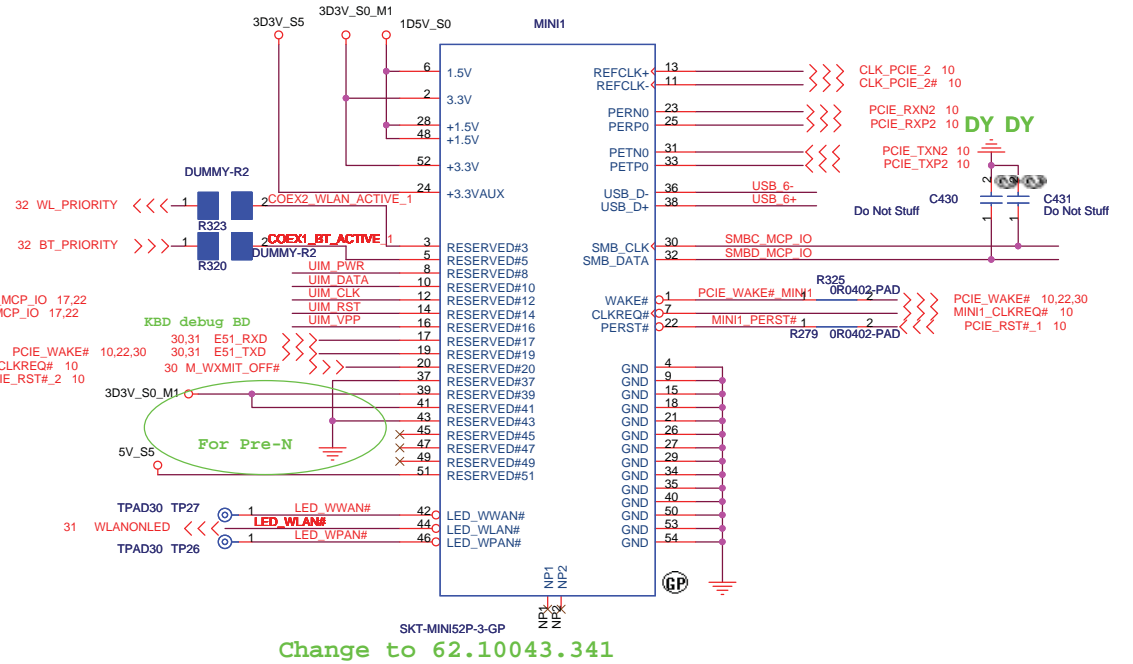
Mini Card Connector 2[®]

Wireless Card



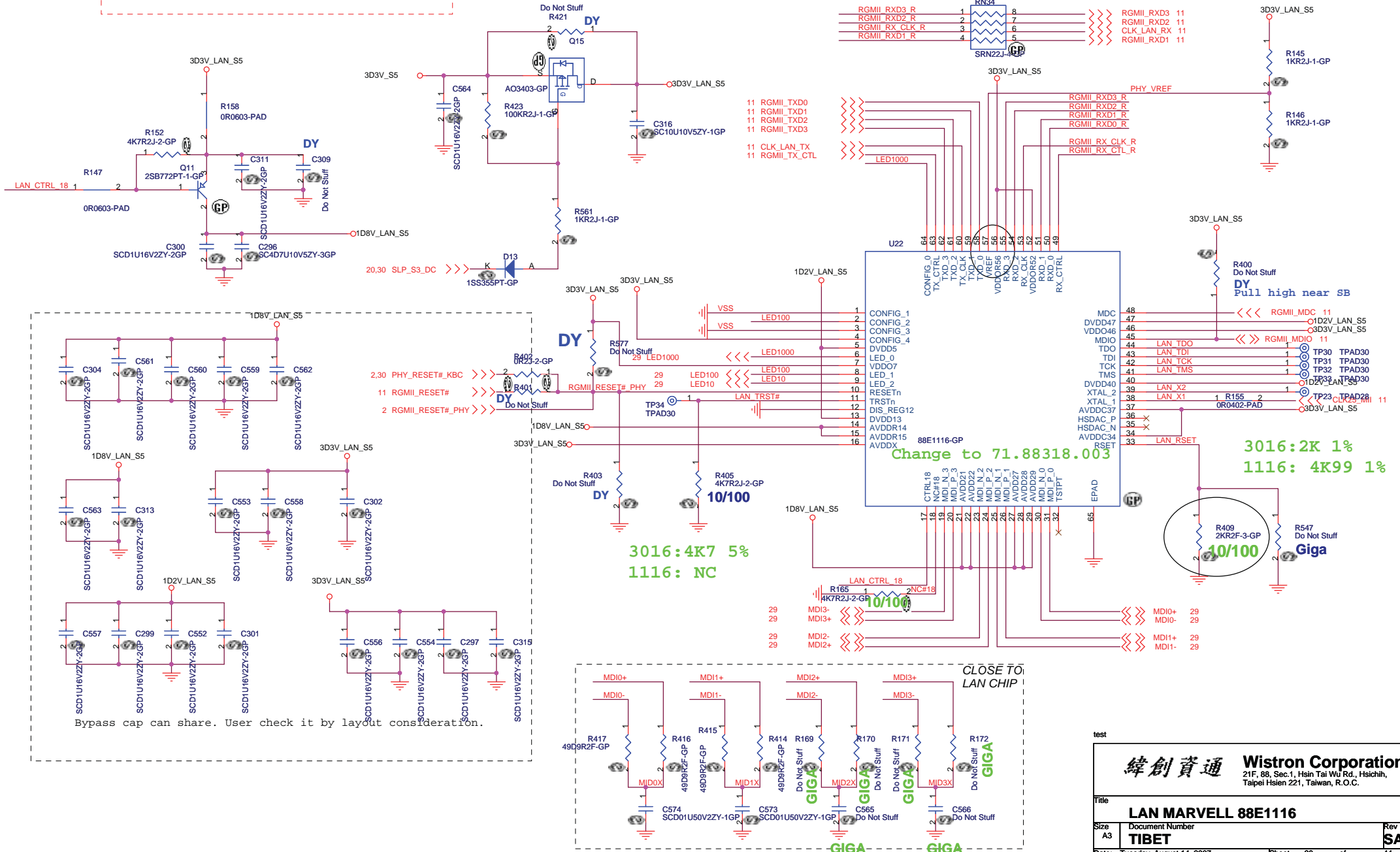
Mini Card Connector 1

WWAN



1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.



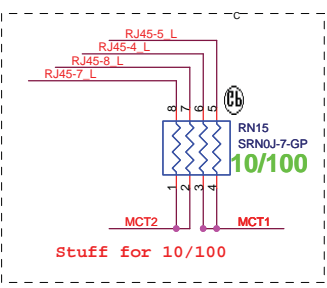
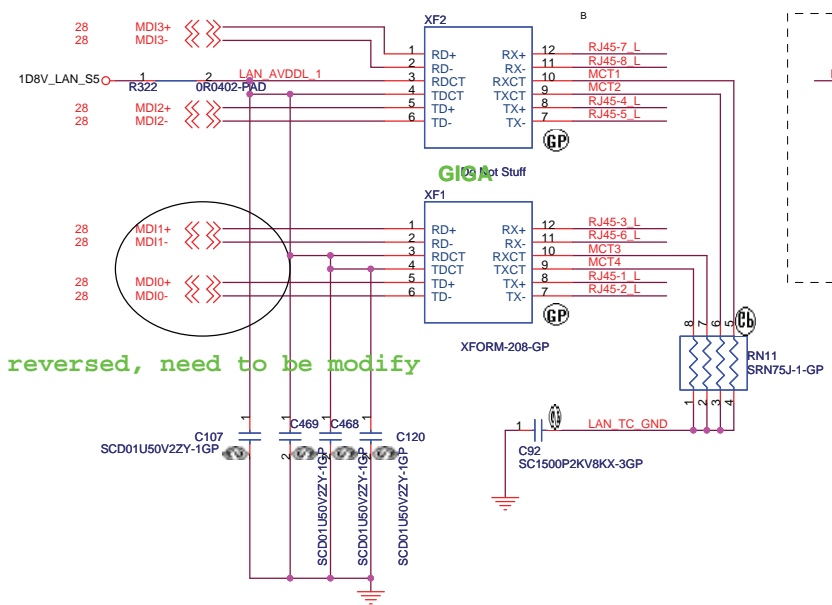
test

緯創資通 Wistron Corporation
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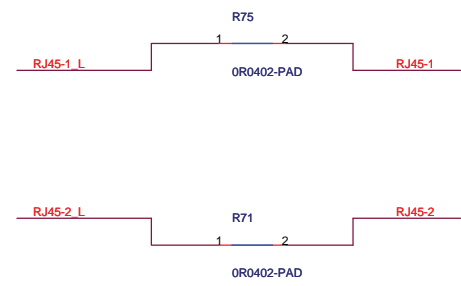
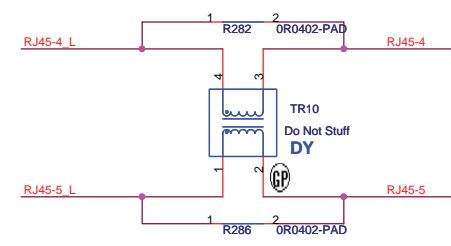
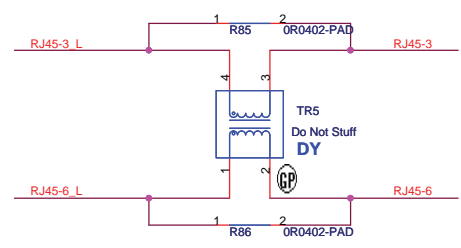
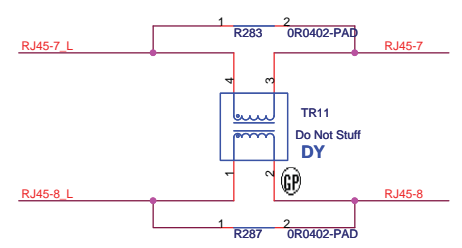
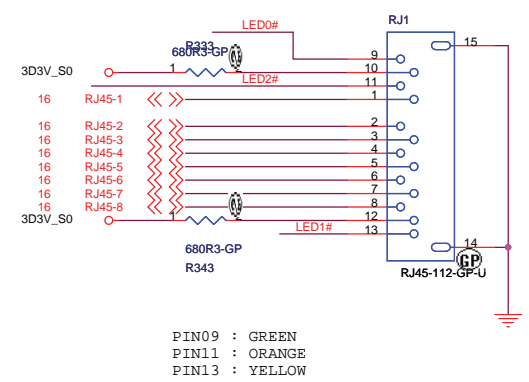
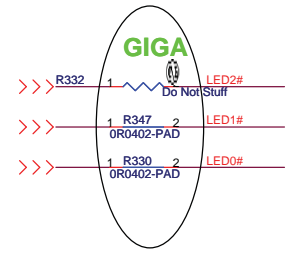
Title: **LAN MARVELL 88E1116**

Size: A3 Document Number: **TIBET** Rev: **SA**

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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



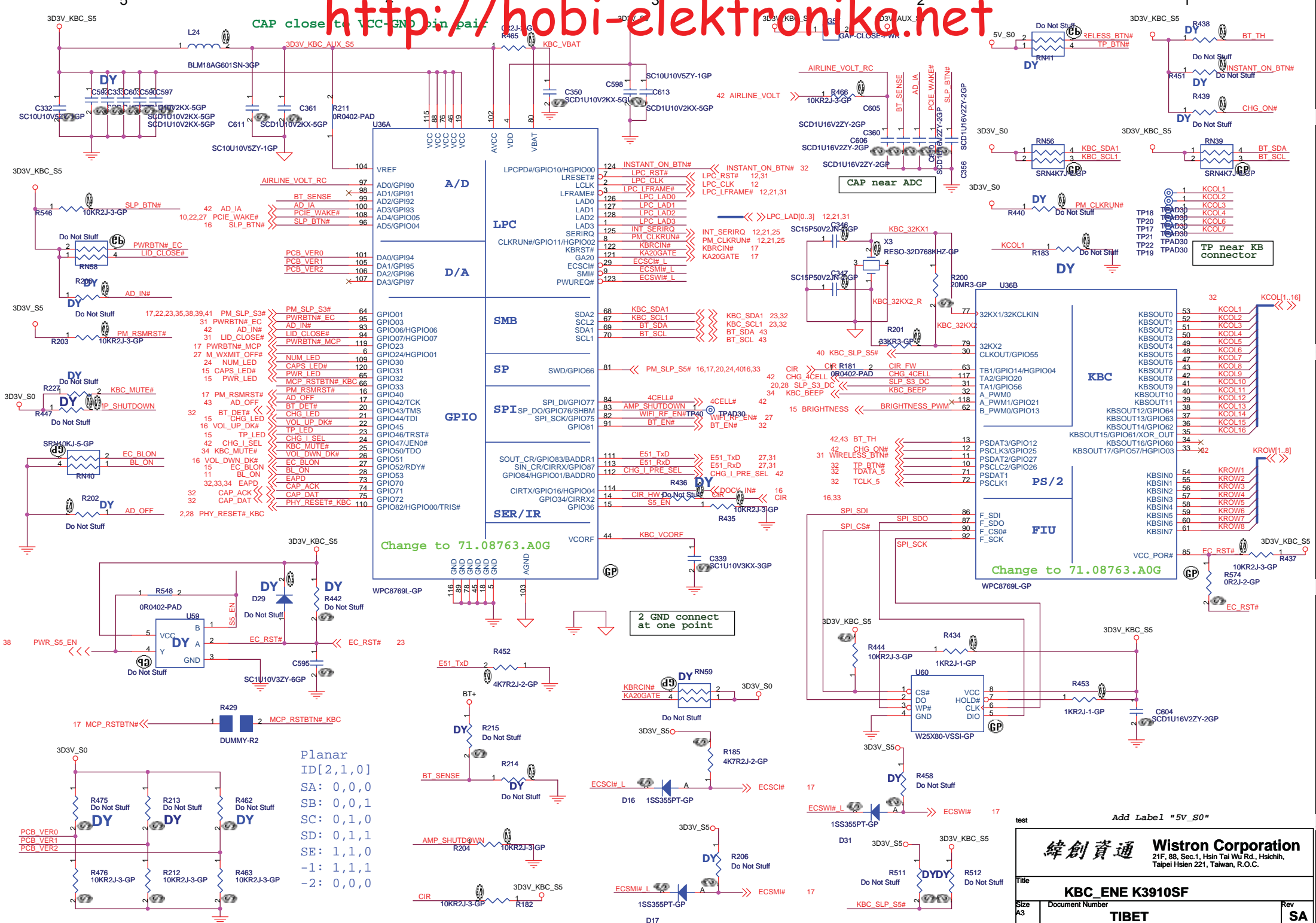
test

緯創資通 Wistron Corporation
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Title: **LAN CONN**

Size A3 Document Number **TIBET** Rev SA

Date: Tuesday, August 14, 2007 Sheet 29 of 44



Change to 71.08763.A0G

Change to 71.08763.A0G

2 GND connect at one point

Planar
ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,1,0
-1: 1,1,1
-2: 0,0,0

test Add Label "5V_S0"

緯創資通 Wistron Corporation
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Title: **KBC_ENE K3910SF**

Size A3 Document Number **TIBET** Rev **SA**

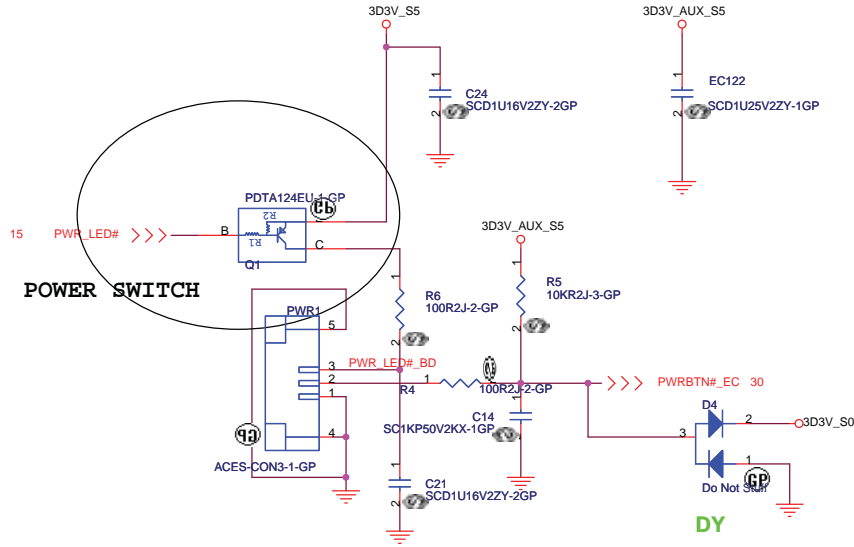
Date: Tuesday, August 14, 2007 Sheet 30 of 44

GOLDEN FINGER FOR DEBUG BOARD

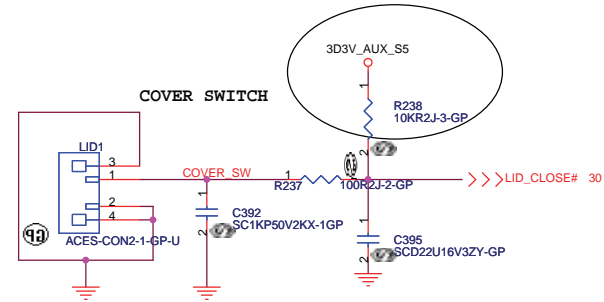
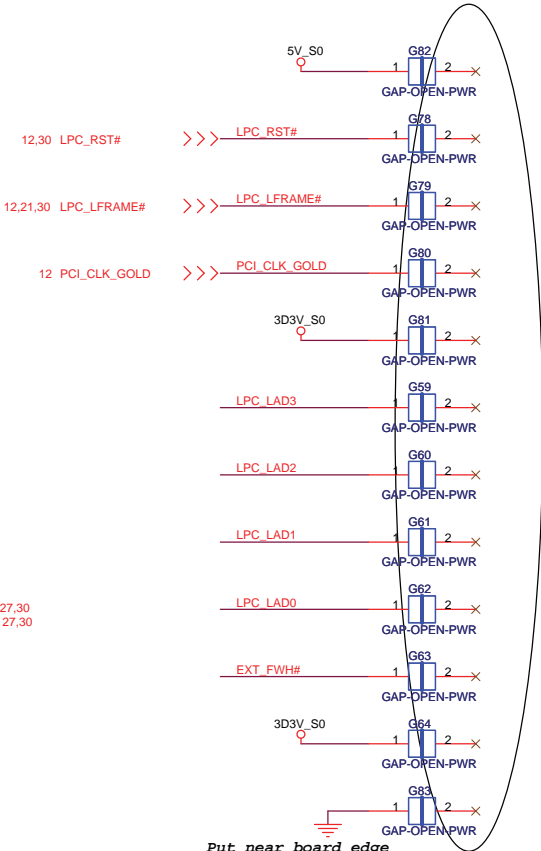
TOP VIEW

A15 (B1)
A14 (B2)
⋮
A2 (B14)
A1 (B15)

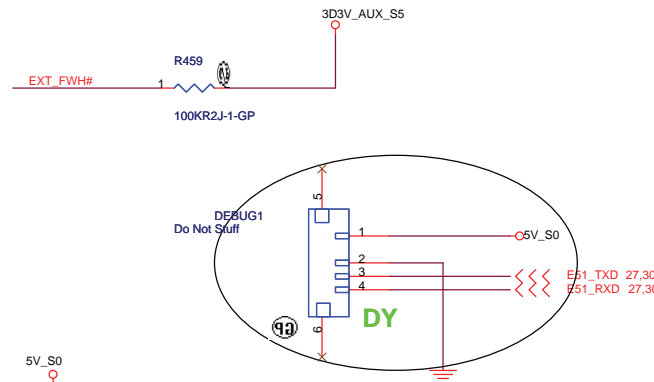
(BOTTOM VIEW)



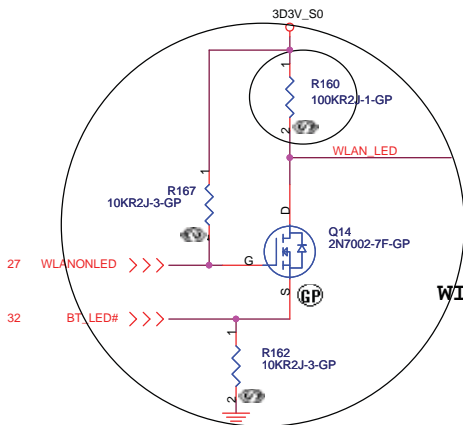
DY



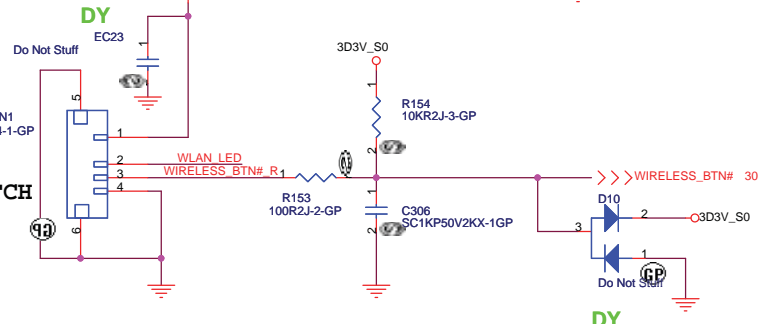
COVER SWITCH



DY



WIRELESS SWITCH



DY

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Title: **FLASH and Debug**

Size: A3 Document Number: **TIBET** Rev: SA

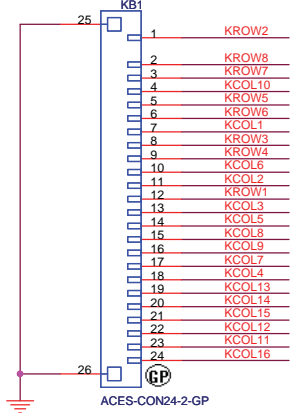
Date: Tuesday, August 14, 2007 Sheet 31 of 44

Internal Keyboard Connector

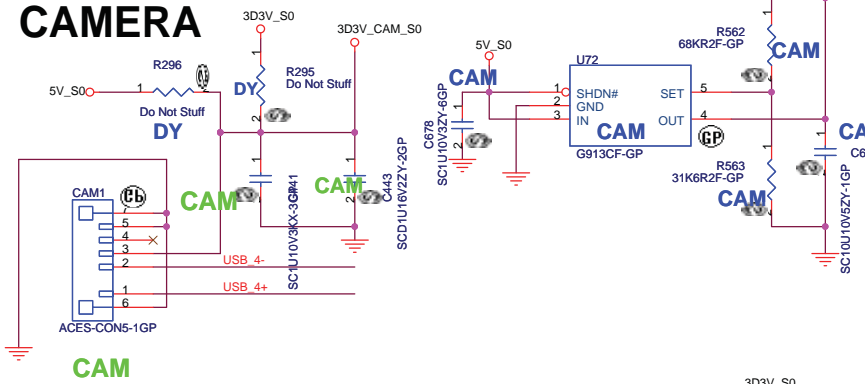
30 KROW[1..8] <<<< 
 30 KCOL[1..16] <<<< 

Keyboard matrix (from vendor)

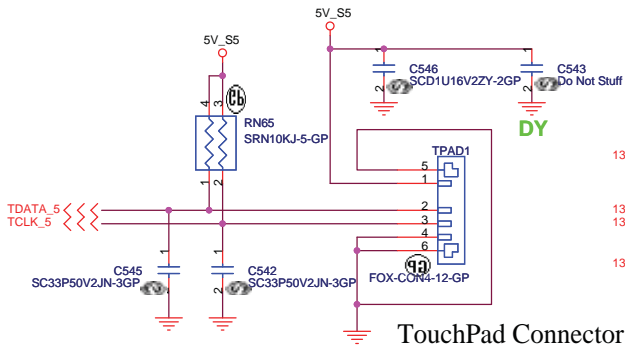
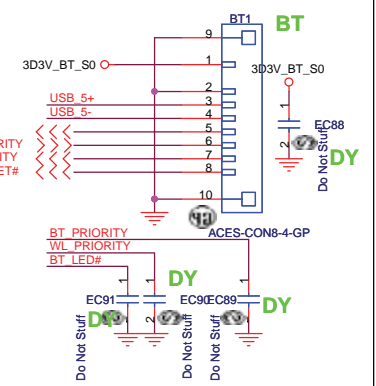
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



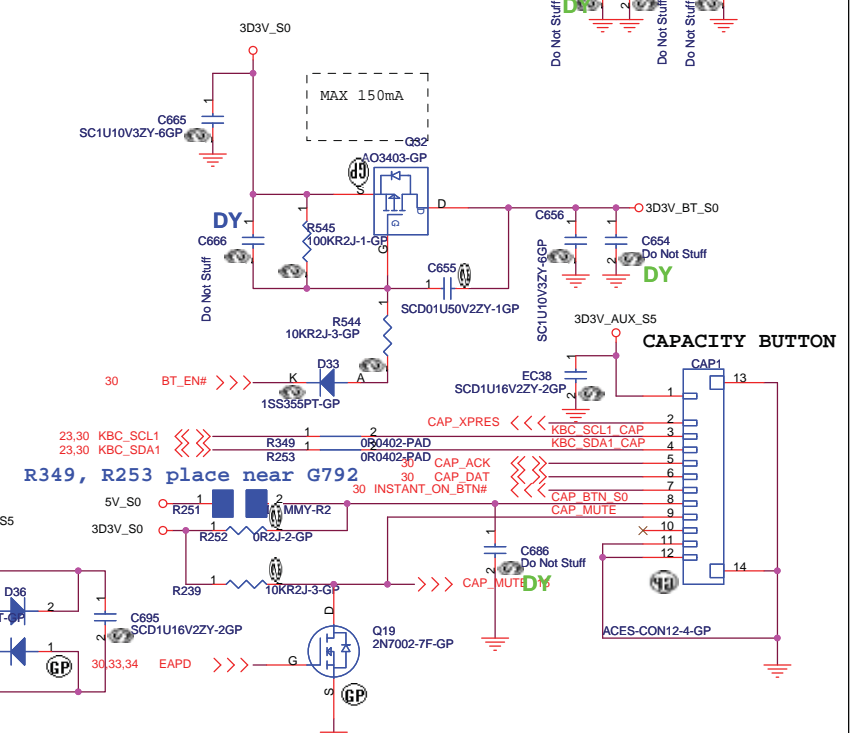
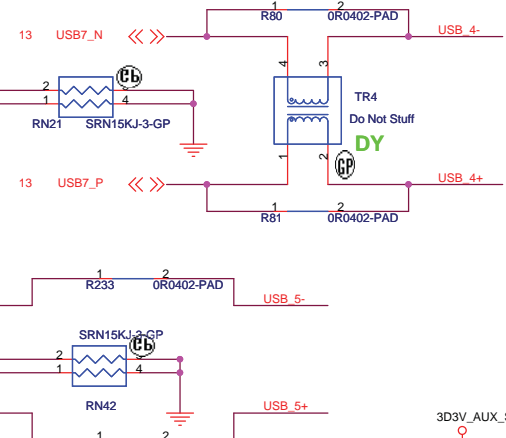
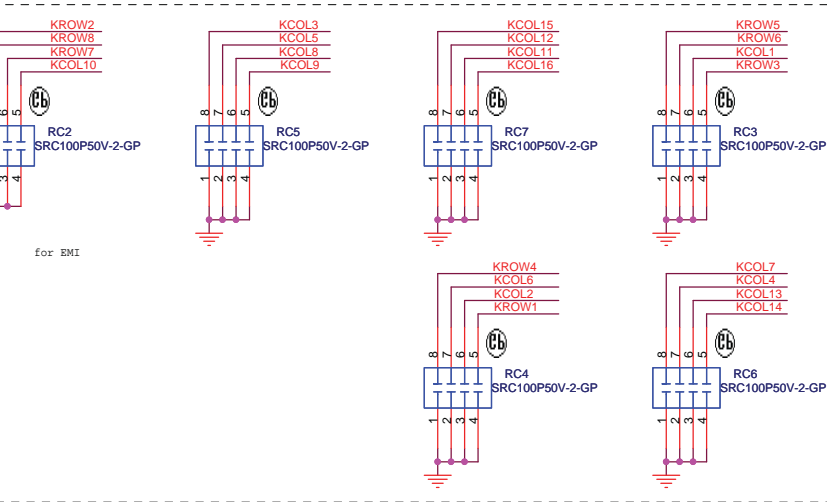
CAMERA



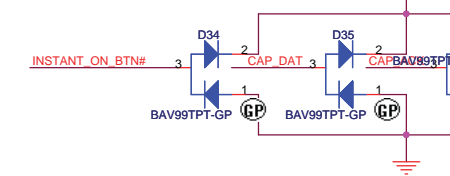
BT



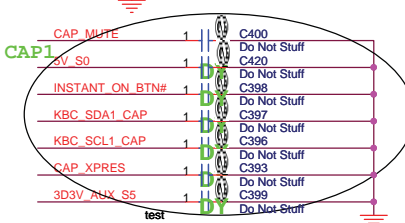
TouchPad Connector



CAPACITY BUTTON



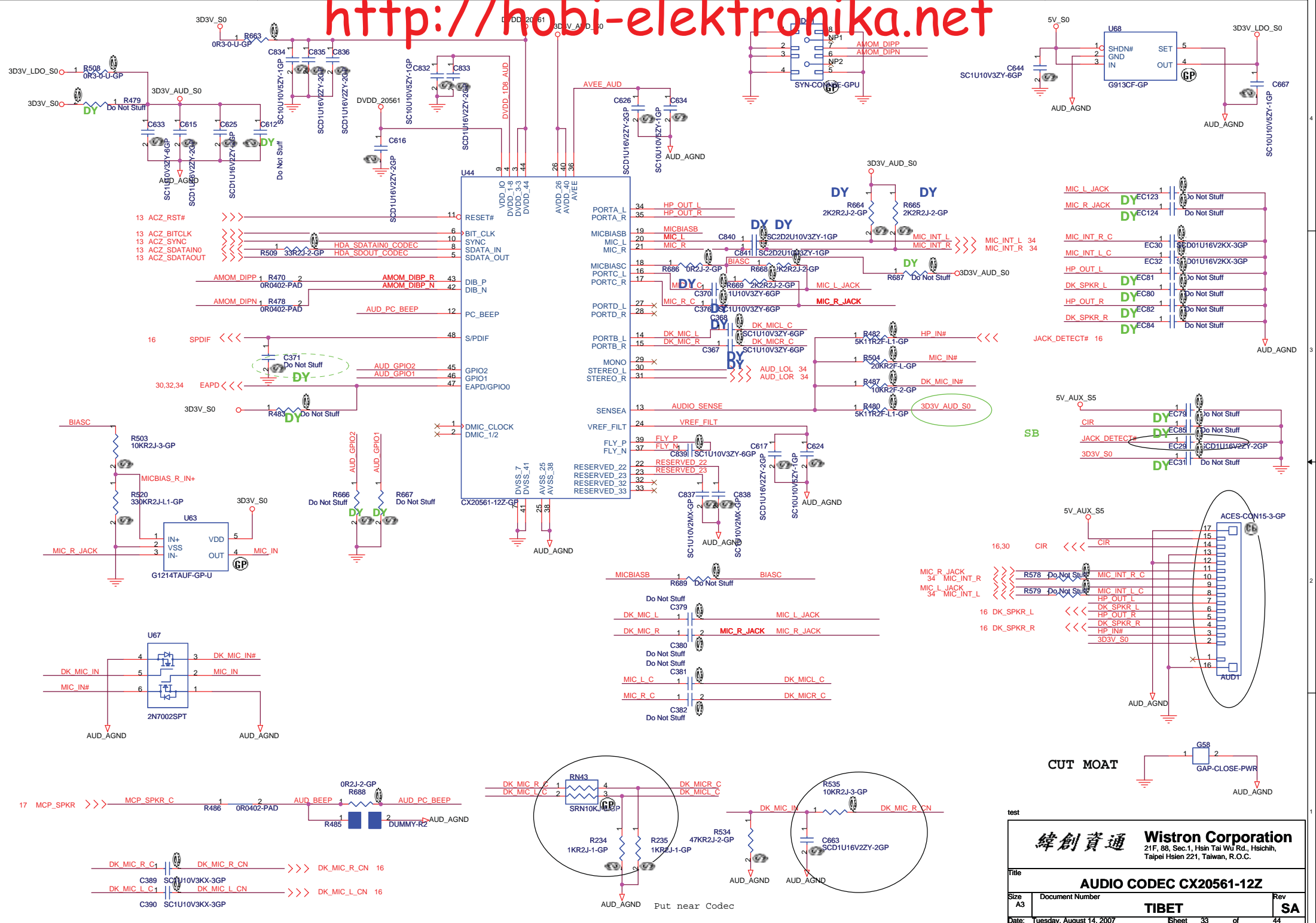
TOUCH-PAD SWITCH



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KeyBoard-CONN

Title	KeyBoard-CONN	Rev	SA
Size	Document Number	TIBET	
A3			
Date:	Tuesday, August 14, 2007	Sheet	32 of 44



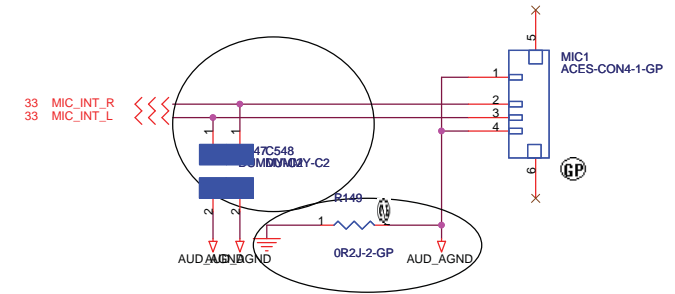
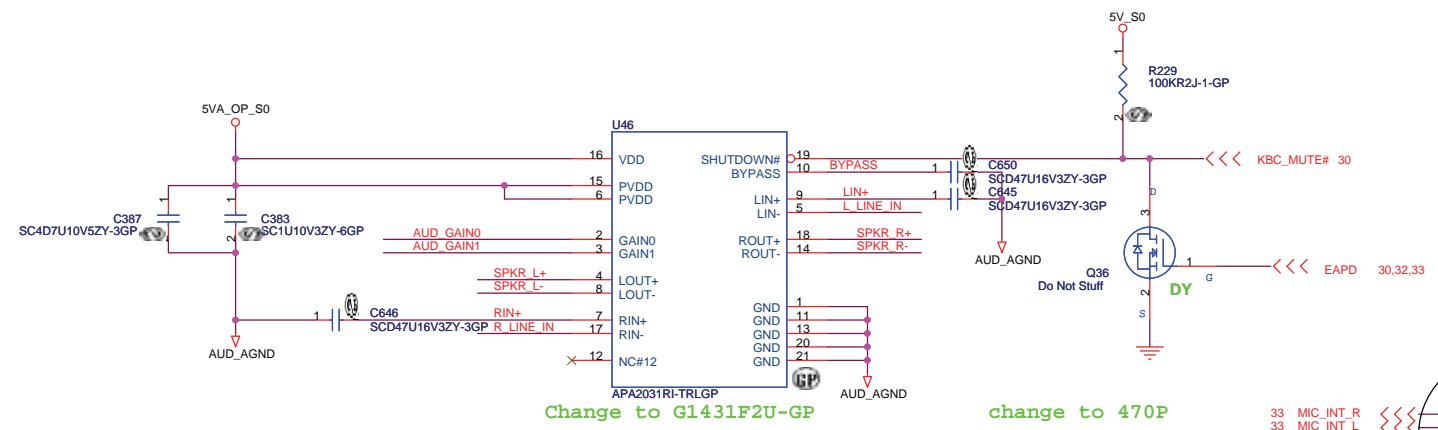
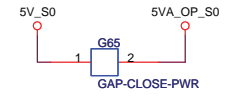
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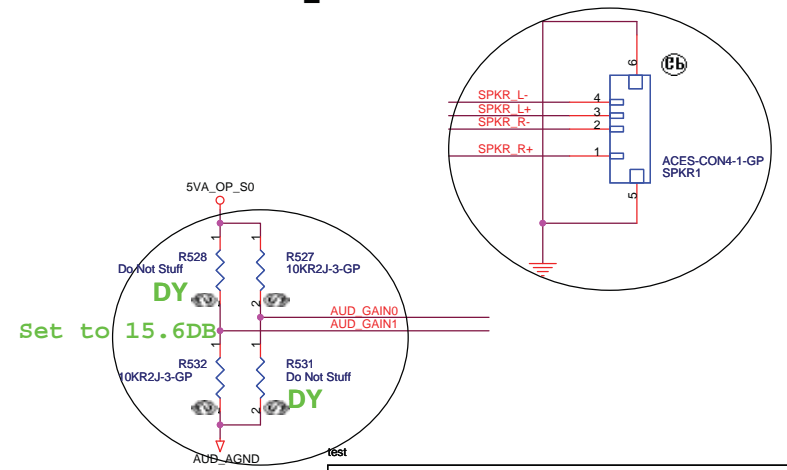
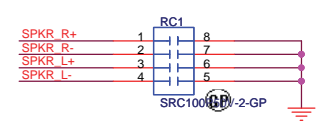
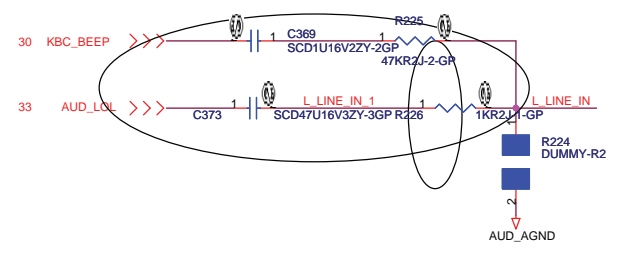
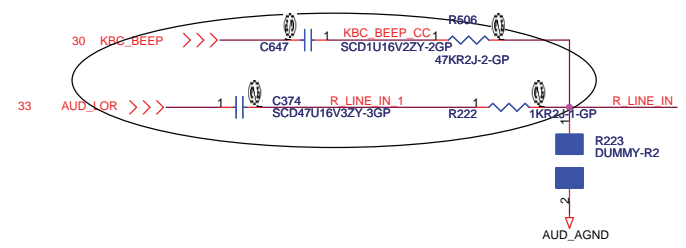
Title: **AUDIO CODEC CX20561-12Z**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 33 of 44



Speaker



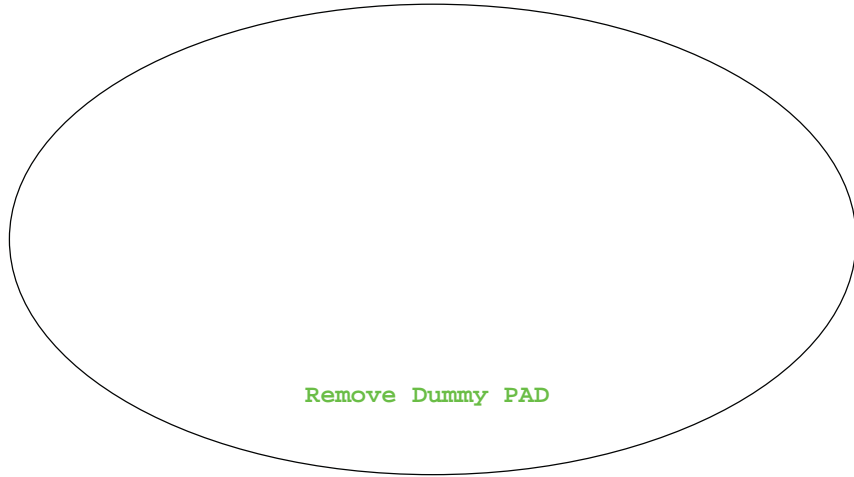
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP APA3031**

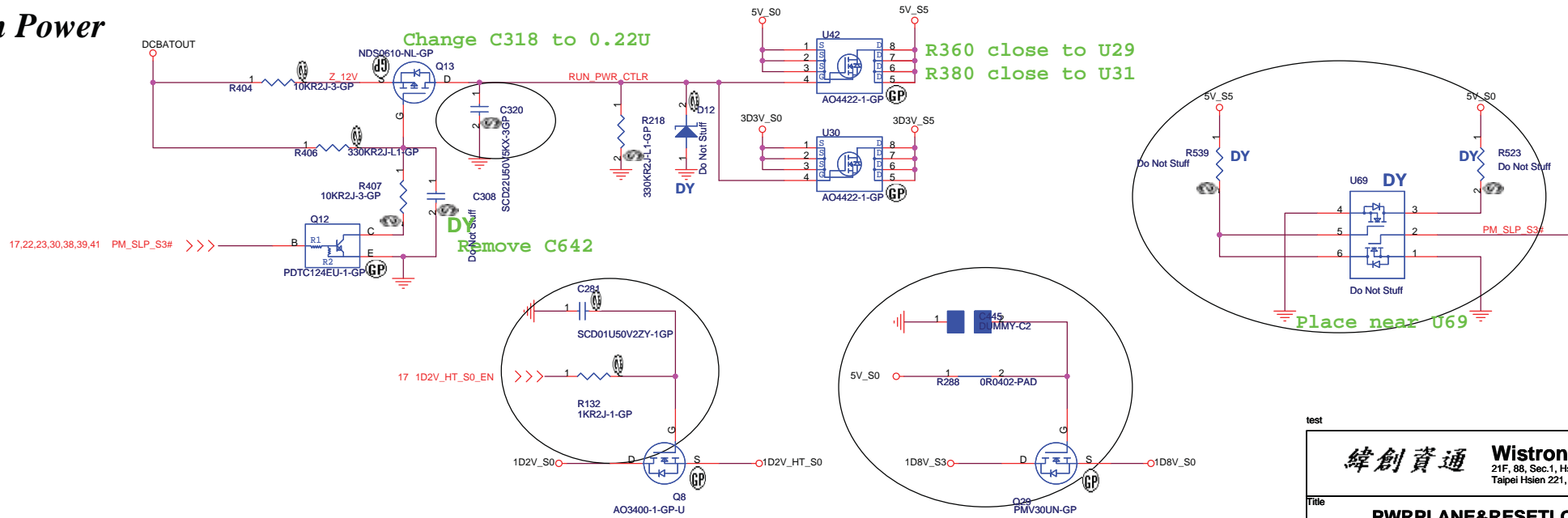
Size: A3 Document Number: **TIBET** Rev: **SA**

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Suspend Power



Run Power

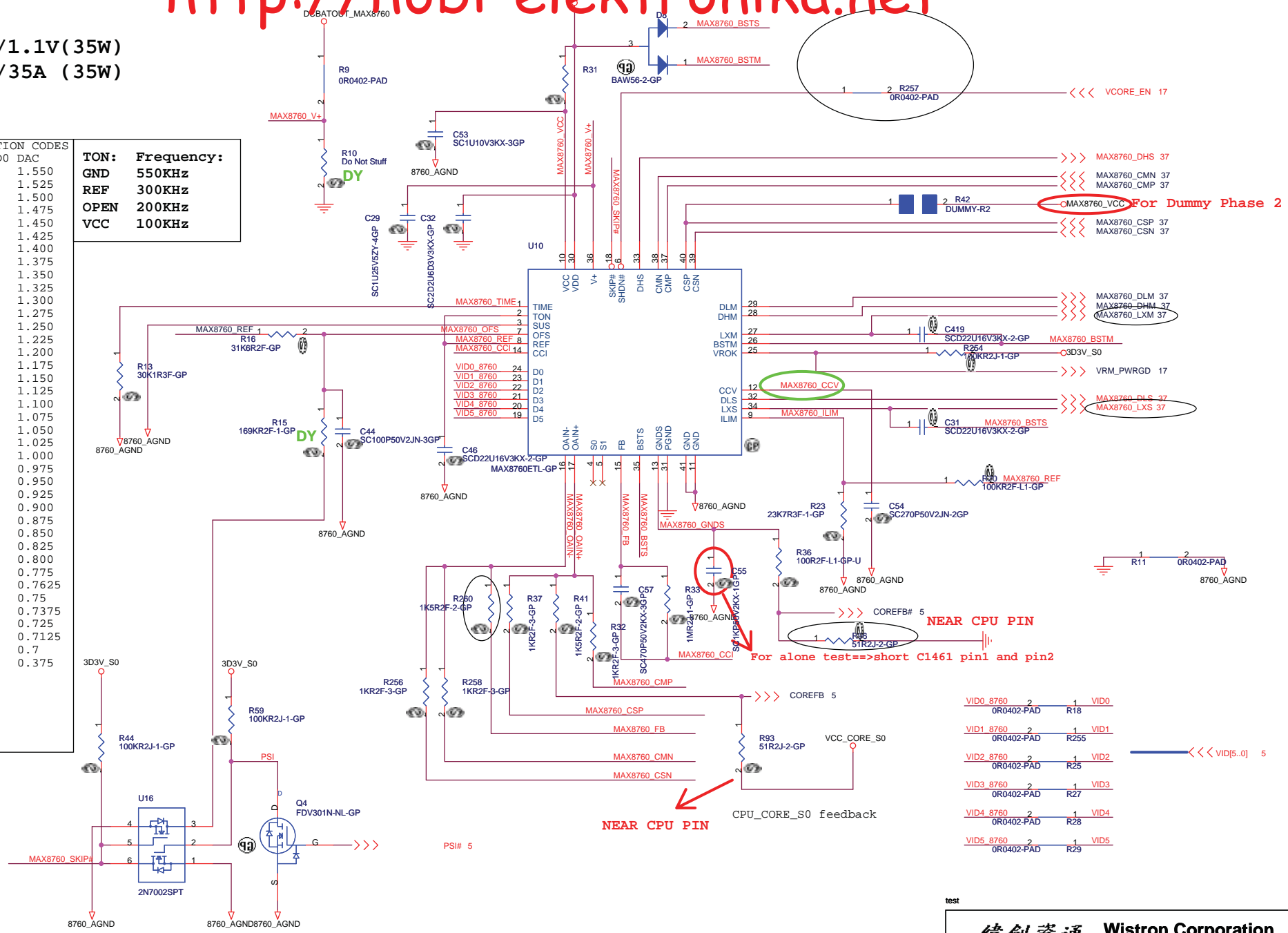


CPU_VCORE
VID=1.15V(25W)/1.1V(35W)
I_{omax}=25A(25W)/35A(35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz



VID0 8760	2	1	VID0
OR0402-PAD		1	R18
VID1 8760	2	1	VID1
OR0402-PAD		1	R255
VID2 8760	2	1	VID2
OR0402-PAD		1	R25
VID3 8760	2	1	VID3
OR0402-PAD		1	R27
VID4 8760	2	1	VID4
OR0402-PAD		1	R28
VID5 8760	2	1	VID5
OR0402-PAD		1	R29

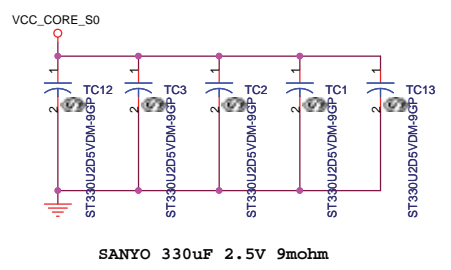
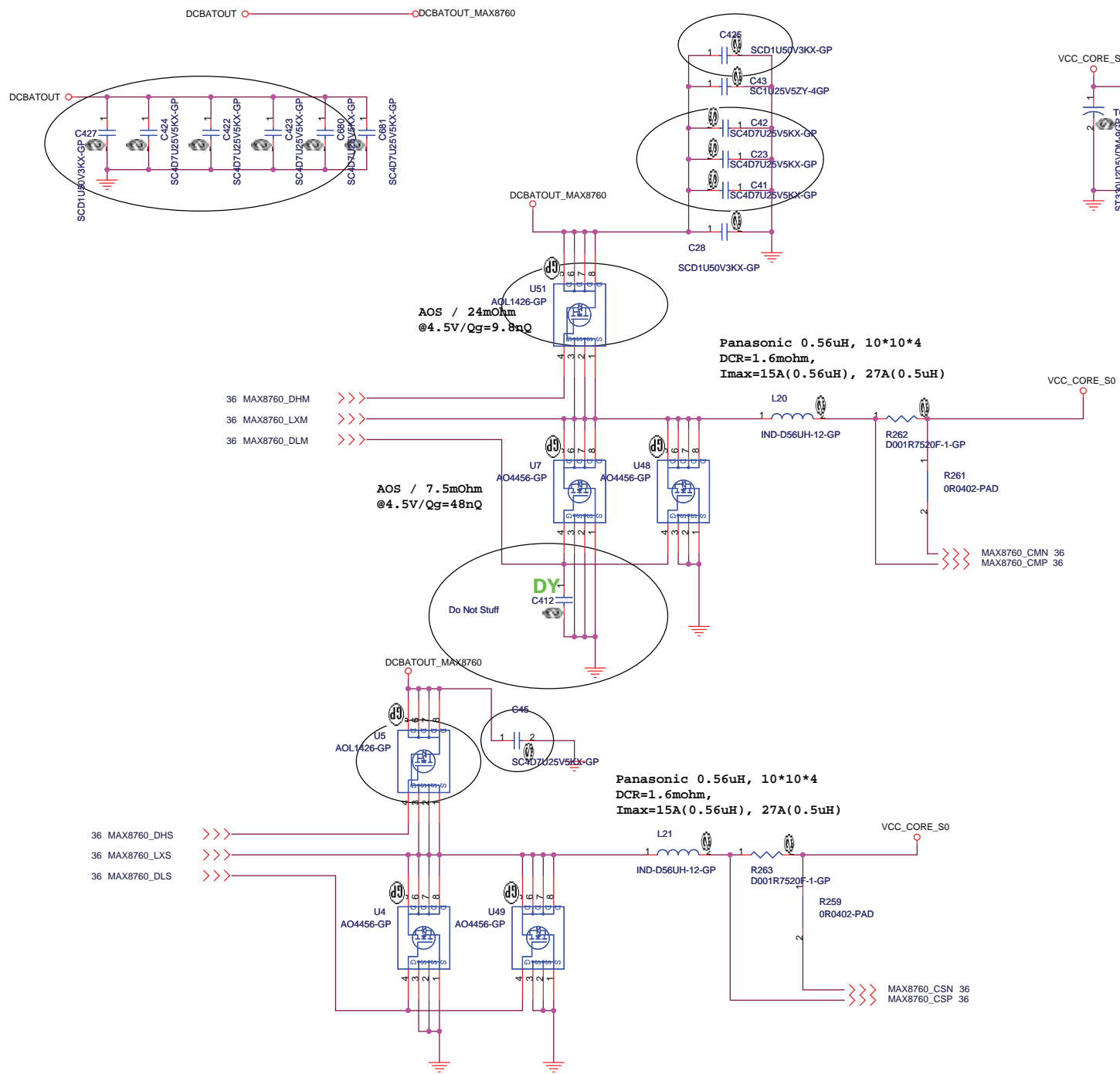
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Title: **CPU CORE MAX8760(1/2)**

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36 MAX8760_DHM
 36 MAX8760_LXM
 36 MAX8760_DLM

AOS / 7.5mOhm
 @4.5V/Qg=48nQ

Panasonic 0.56uH, 10*10*4
 DCR=1.6mohm,
 Imax=15A(0.56uH), 27A(0.5uH)

DY
 Do Not Stuff
 C412

Panasonic 0.56uH, 10*10*4
 DCR=1.6mohm,
 Imax=15A(0.56uH), 27A(0.5uH)

36 MAX8760_DHS
 36 MAX8760_LXS
 36 MAX8760_DLS

MAX8760_CSN 36
 MAX8760_CSP 36

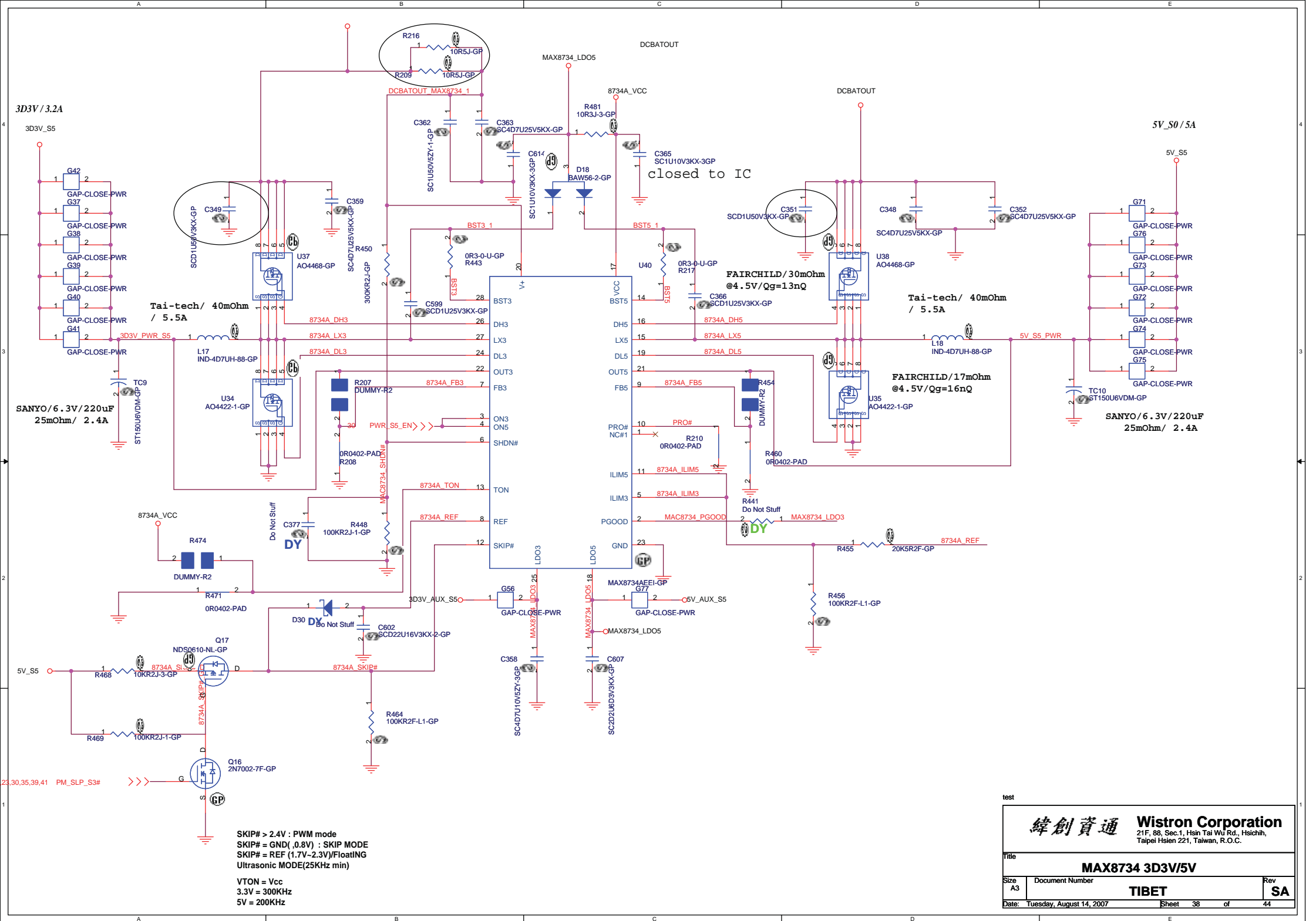
(Power Team)

test

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU CORE MAX8760(2/2)**

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closed to IC

3D3V / 3.2A

5V_S0 / 5A

SANYO / 6.3V / 220uF
25mOhm / 2.4A

SANYO / 6.3V / 220uF
25mOhm / 2.4A

SKIP# > 2.4V : PWM mode
 SKIP# = GND(,0.8V) : SKIP MODE
 SKIP# = REF (1.7V-2.3V)/FloatNG
 Ultrasonic MODE(25KHz min)

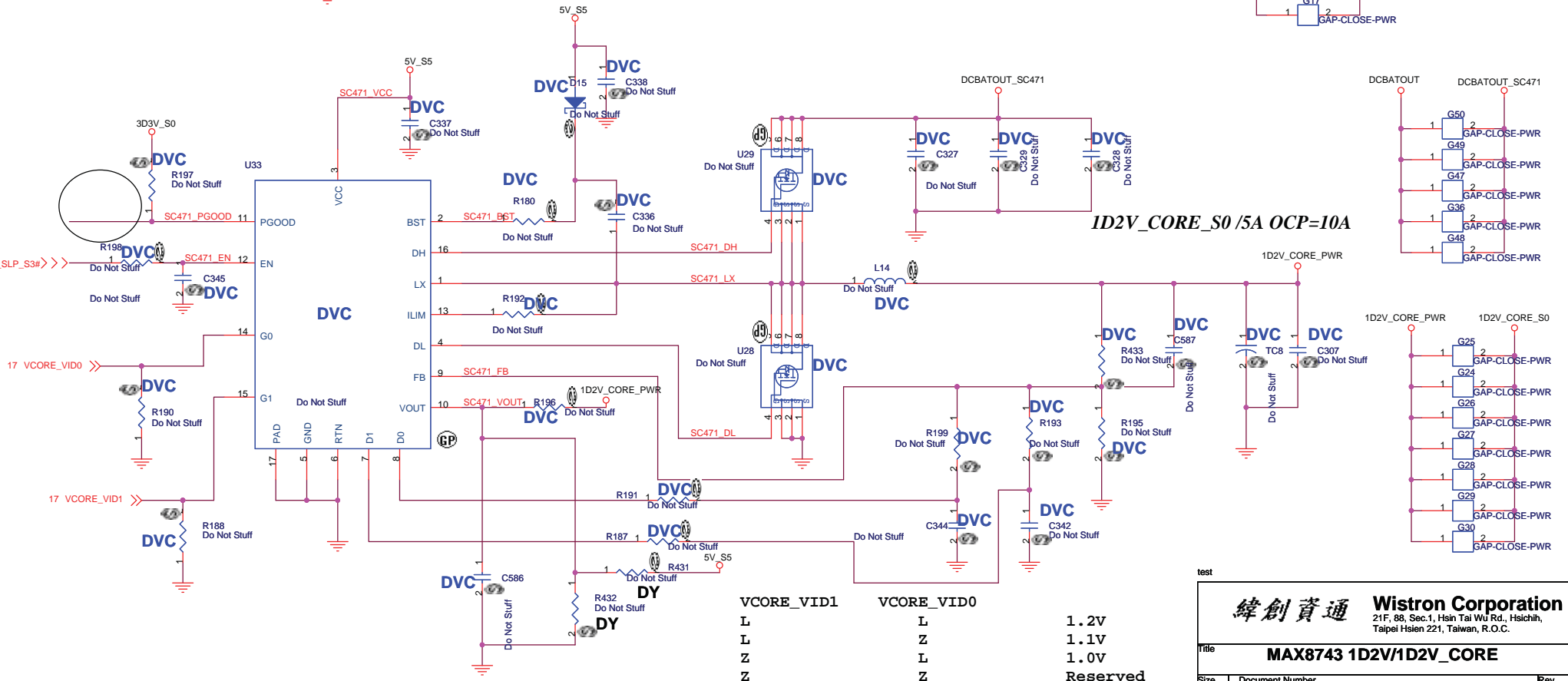
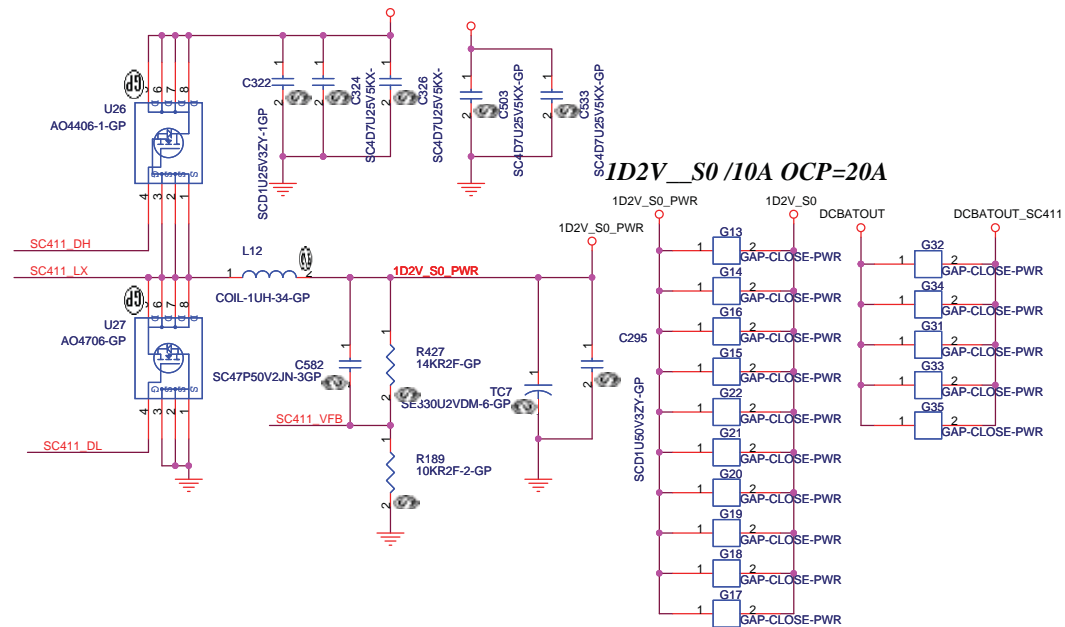
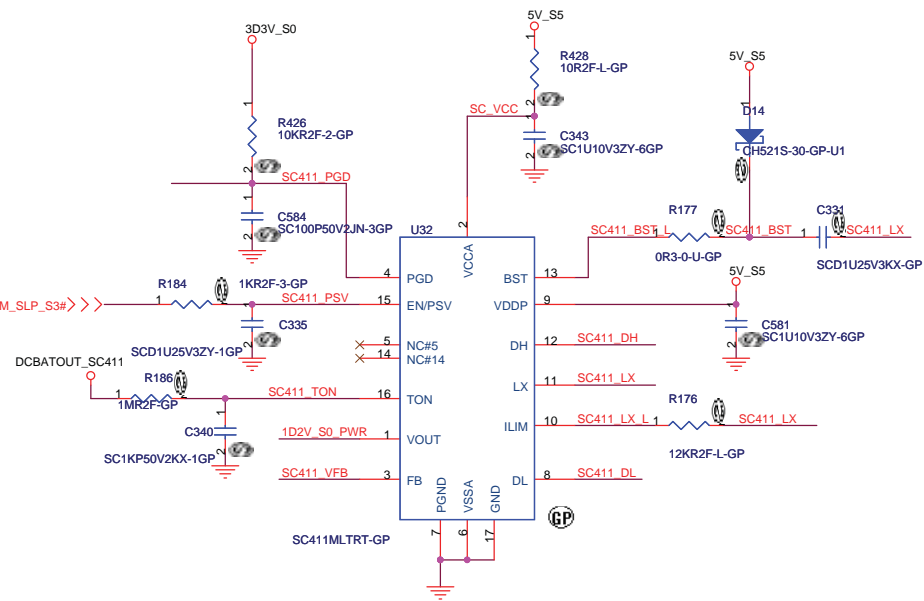
VTON = Vcc
 3.3V = 300KHz
 5V = 200KHz

test

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Title: **MAX8734 3D3V/5V**

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VCORE_VID1	VCORE_VID0	1.2V
L	L	1.1V
Z	Z	1.0V
Z	Z	Reserved

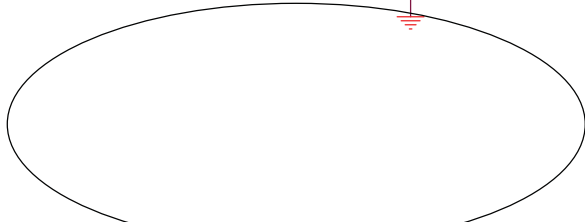
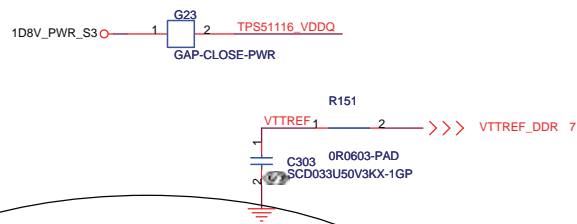
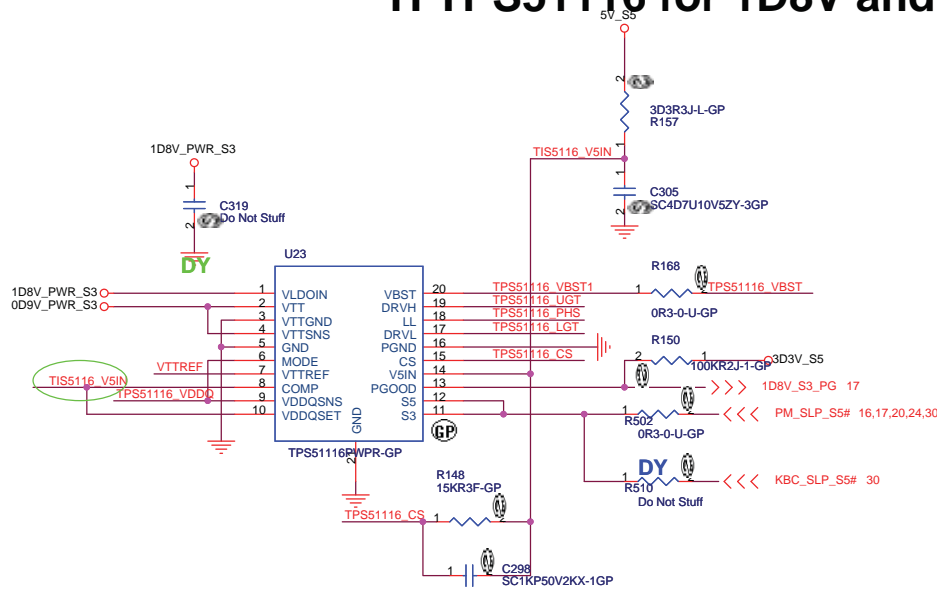
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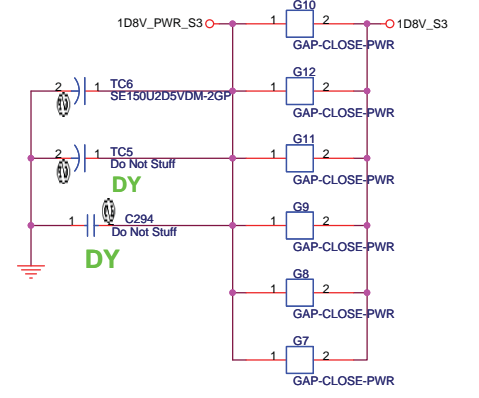
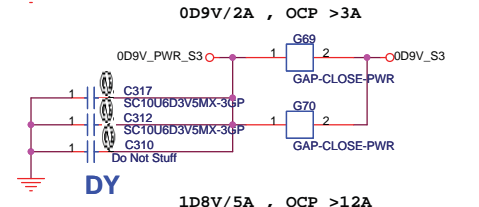
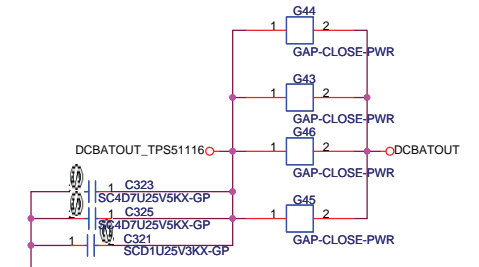
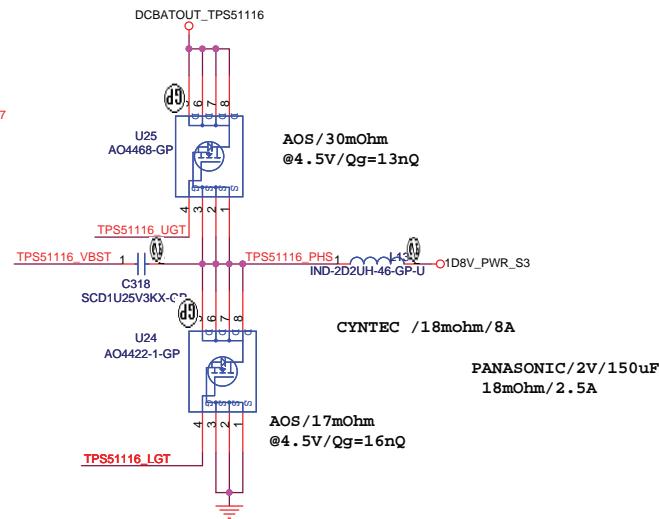
Title: **MAX8743 1D2V/1D2V_CORE**

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TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

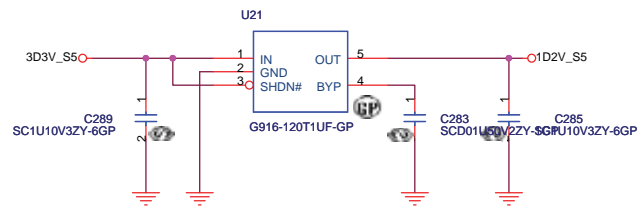
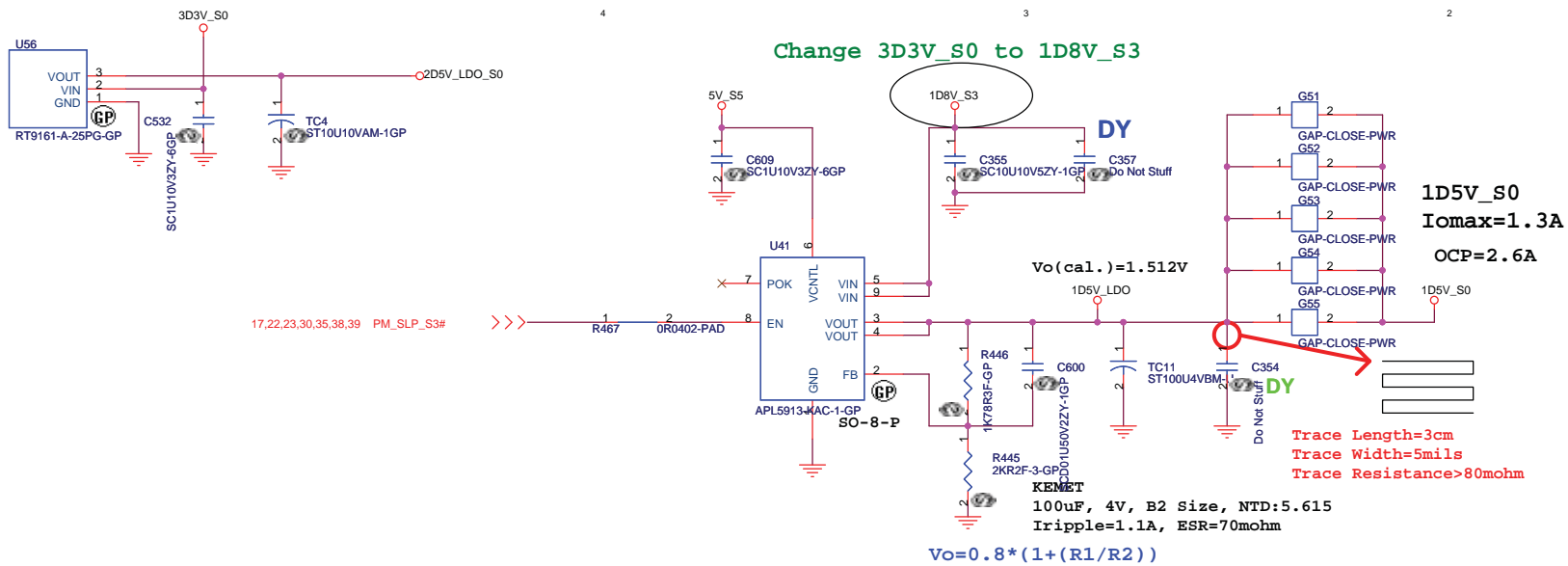


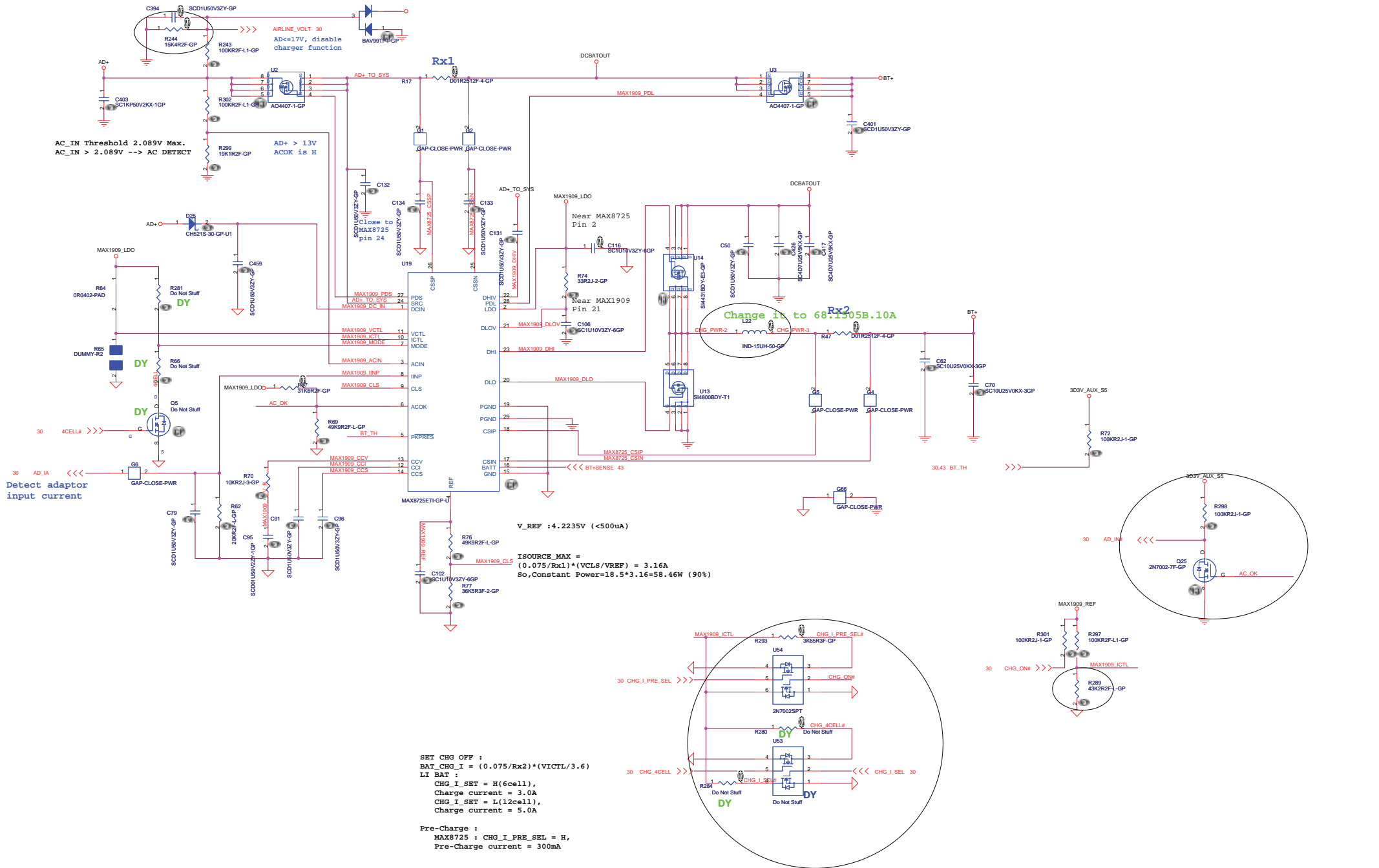
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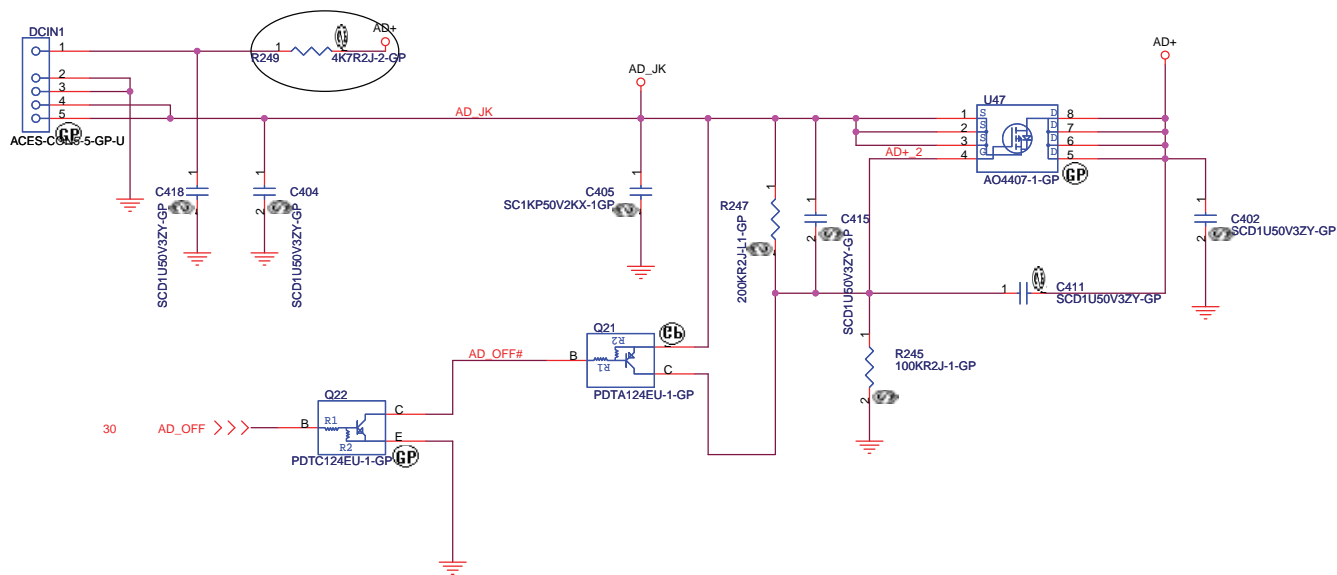
Title: **TPS51116 1D8V/0D9V**

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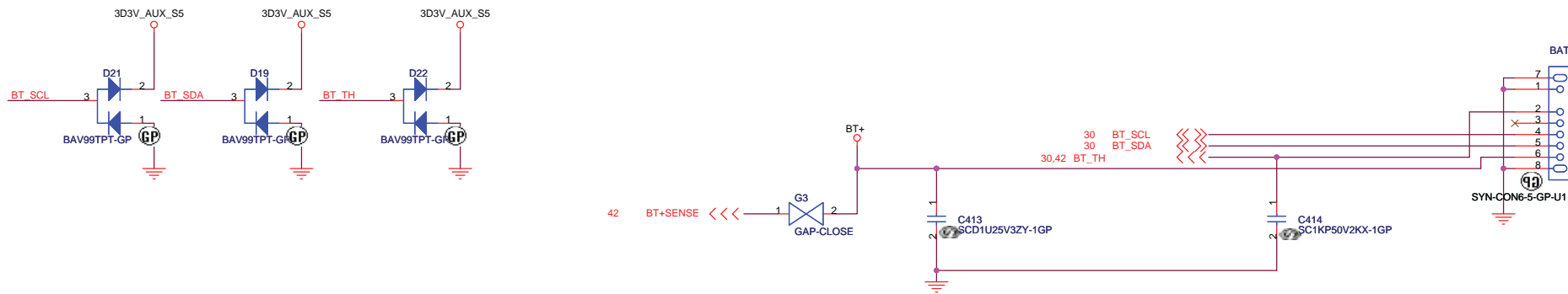




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

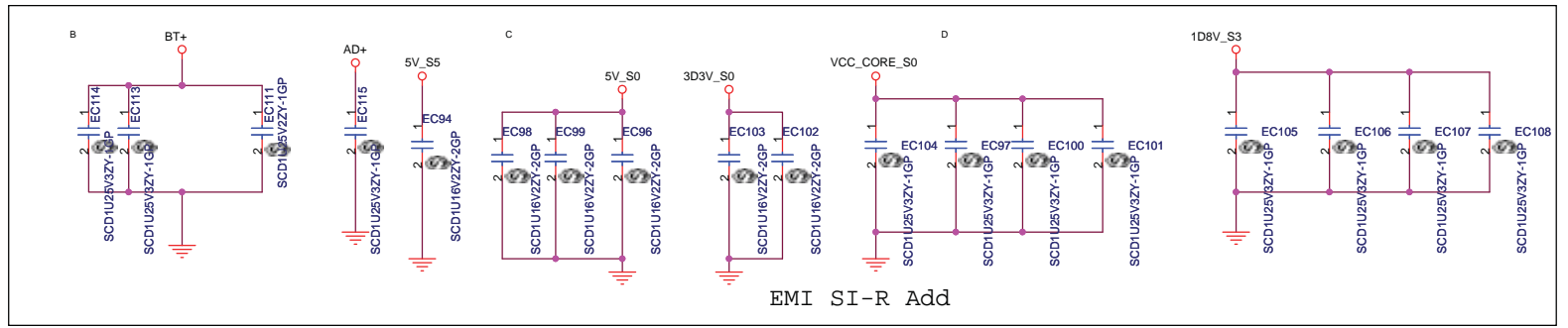
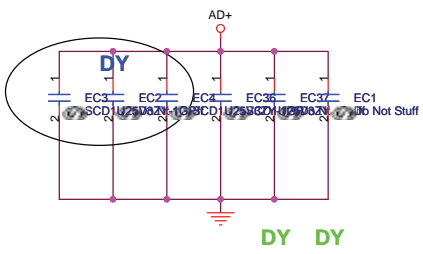


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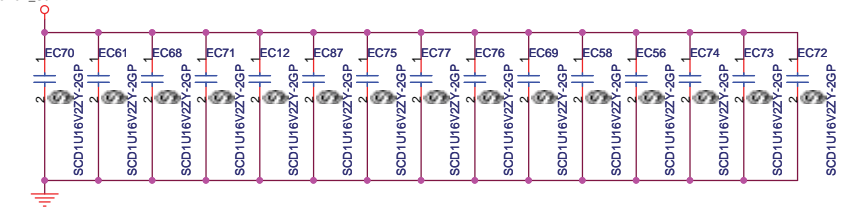
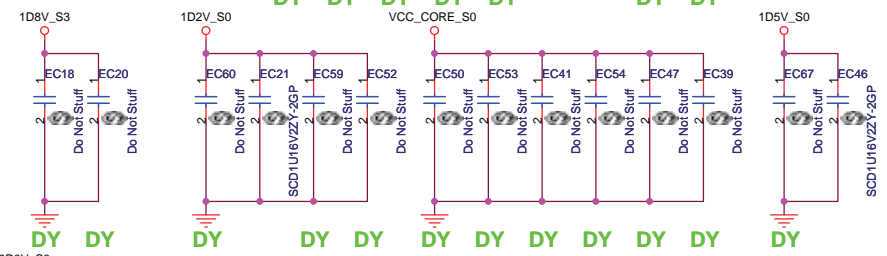
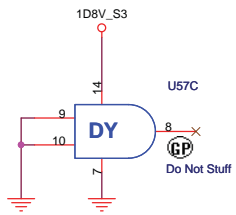
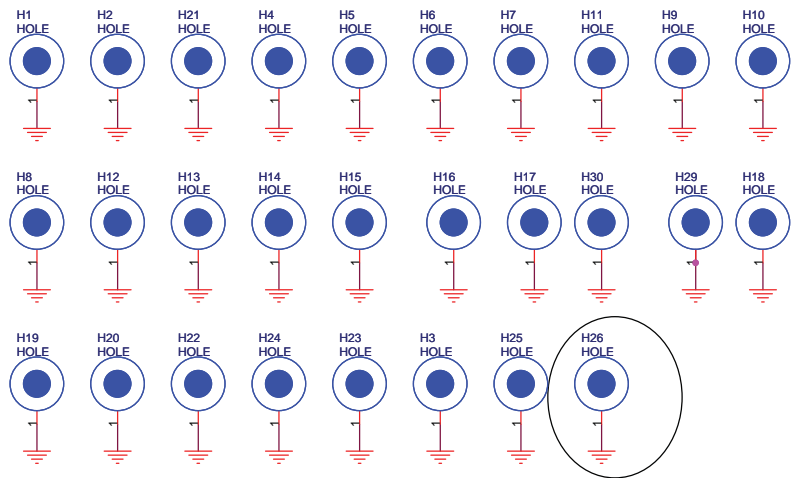
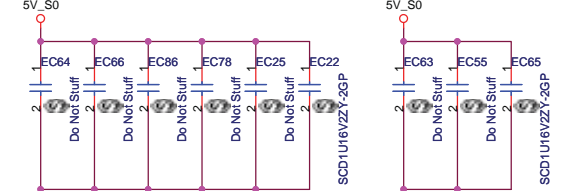
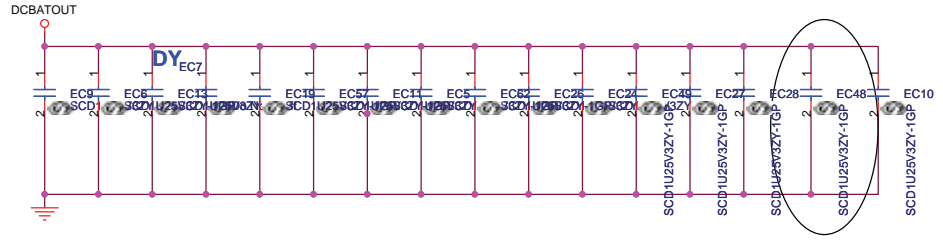
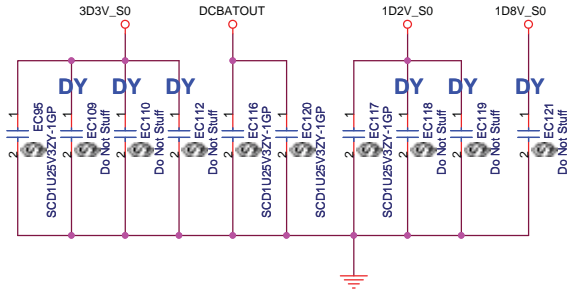
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

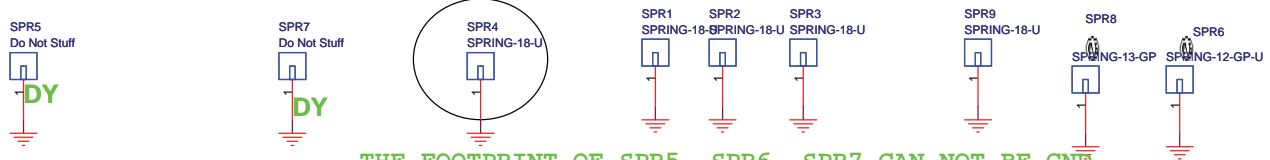
Size: A3	Document Number: TIBET	Rev: SA
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	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



Modify SPR7 P/N manually



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND

test

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size A3 Document Number: **TIBET** Rev SA

Date: Wednesday, August 15, 2007 Sheet 44 of 44