

SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1:	SIGNAL 1
L2:	GND
L3:	SIGNAL 2
L4:	SIGNAL 3
L5:	VCC
L6:	SIGNAL 4

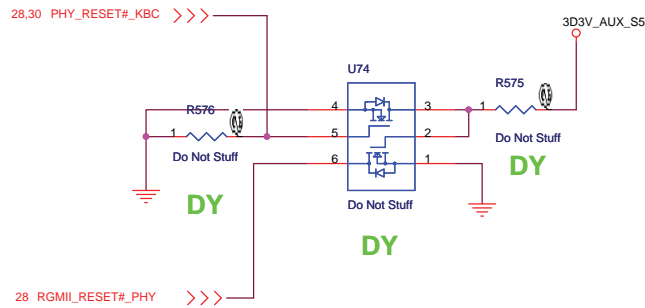
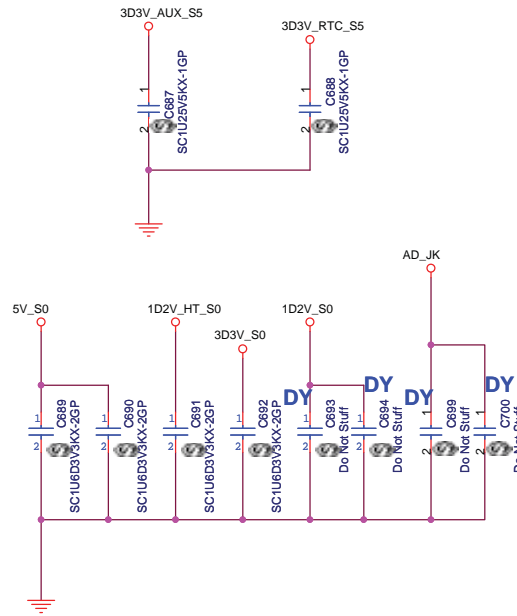
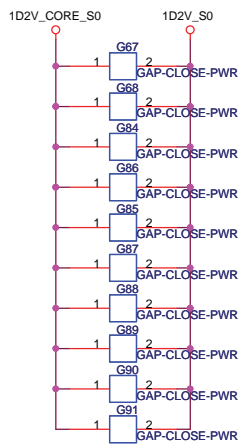
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **TIBET** Rev: SA

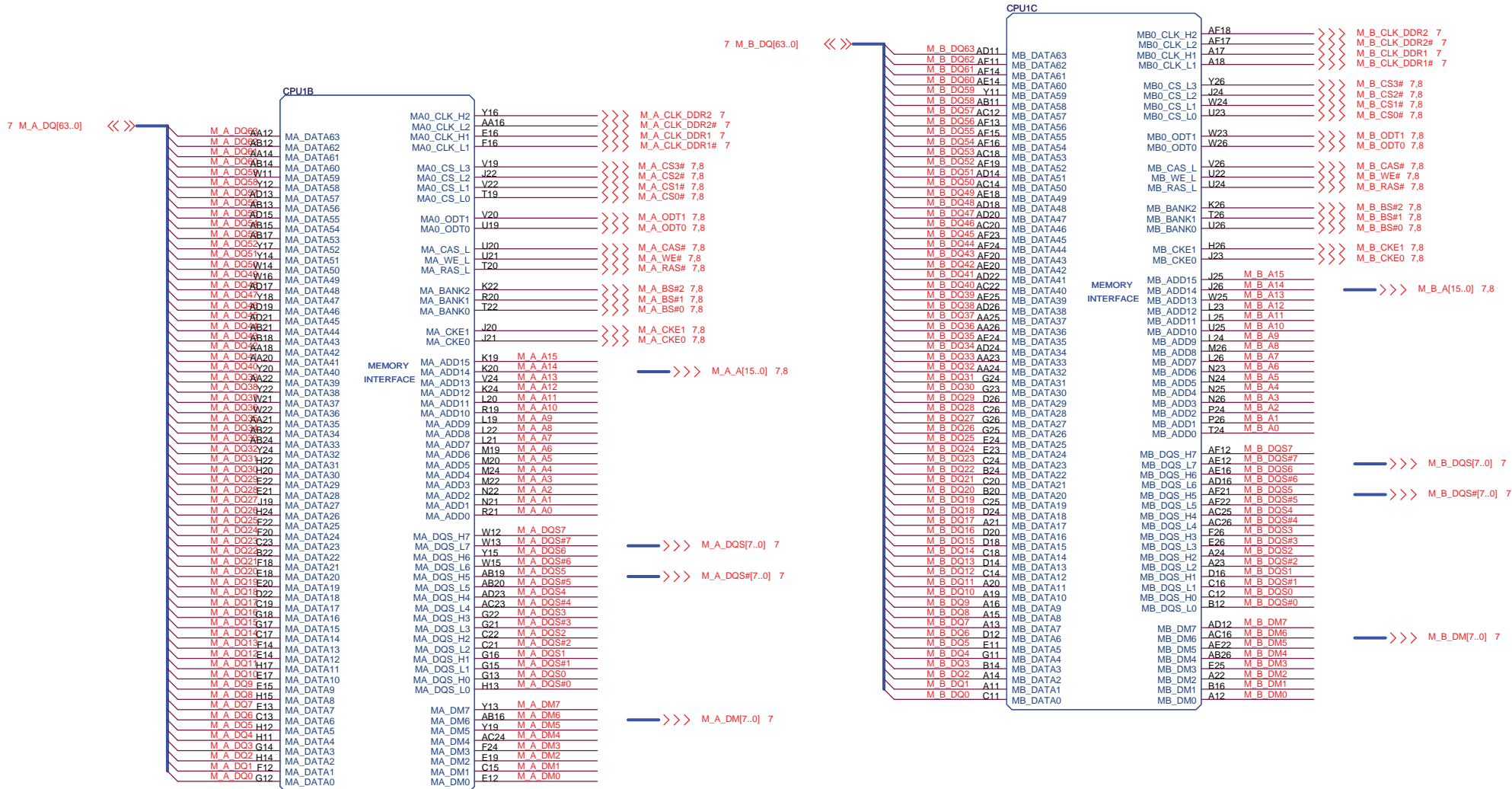
Date: Tuesday, August 14, 2007 Sheet 1 of 44



test

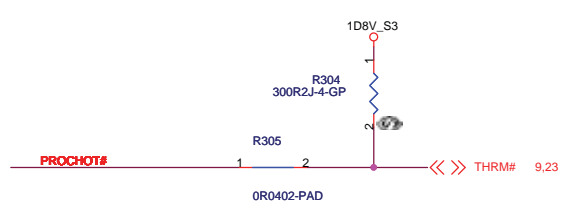
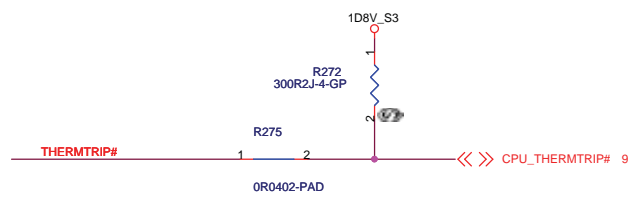
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
Size	Document Number	Rev	
A3	TIBET	SA	
Date: Tuesday, August 14, 2007		Sheet 2	of 44



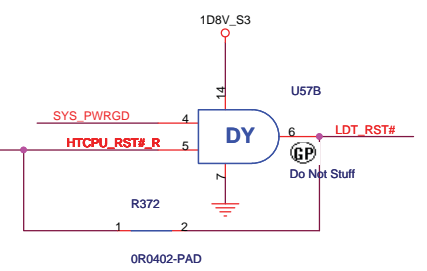
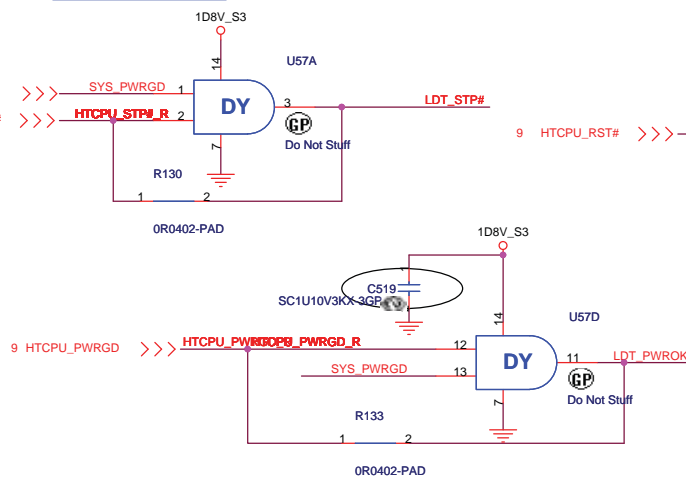
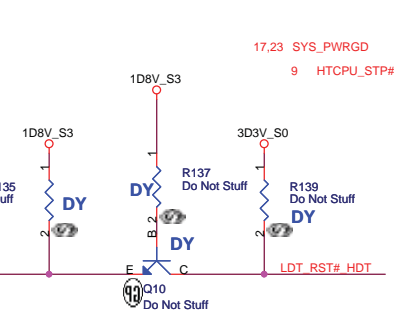
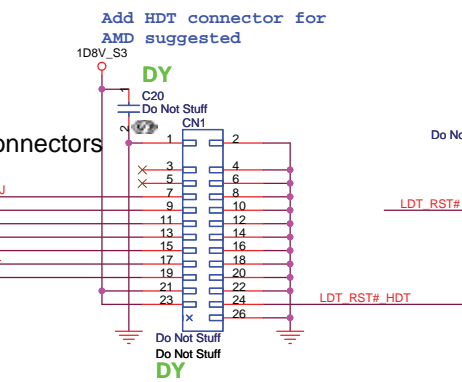
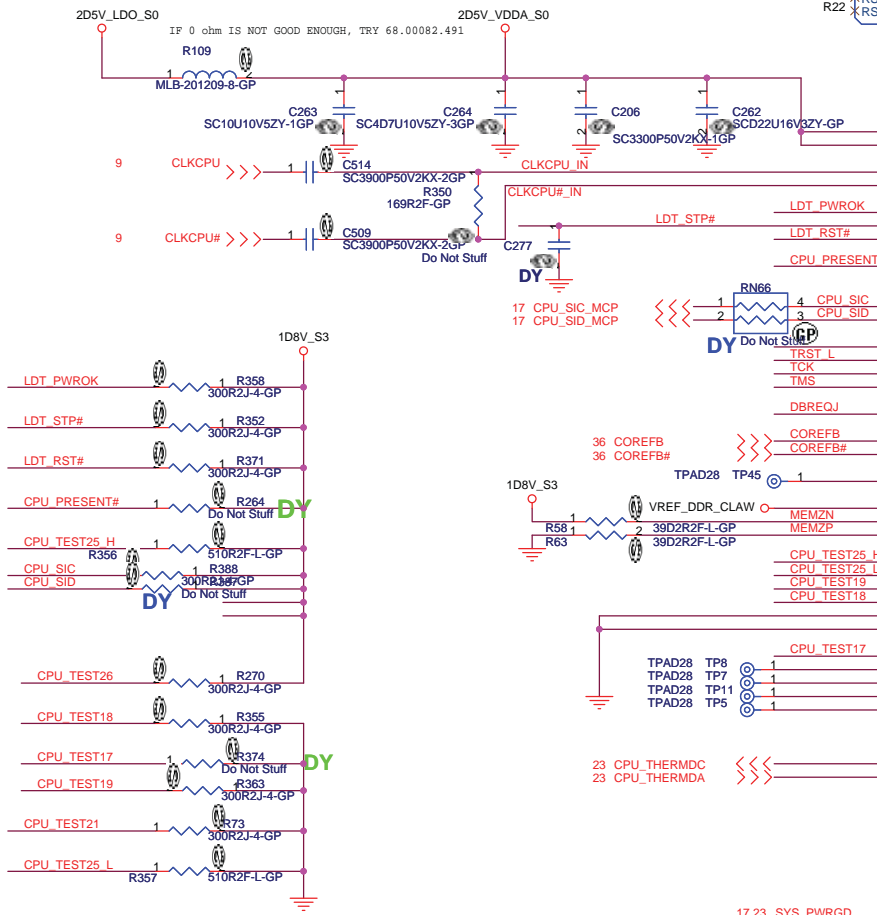
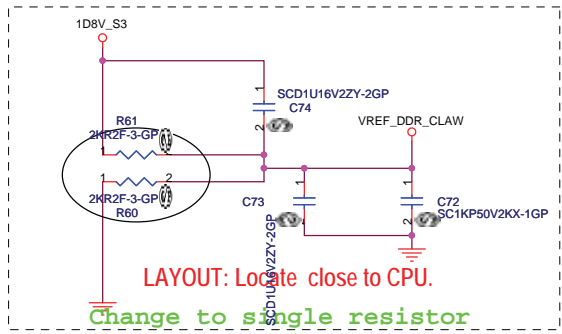


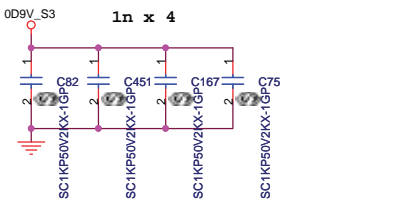
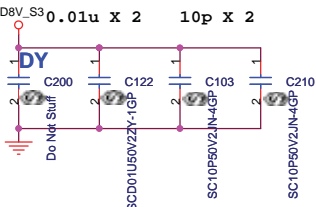
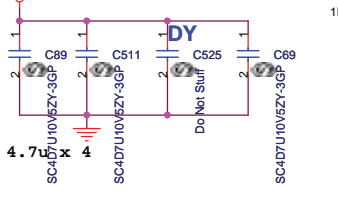
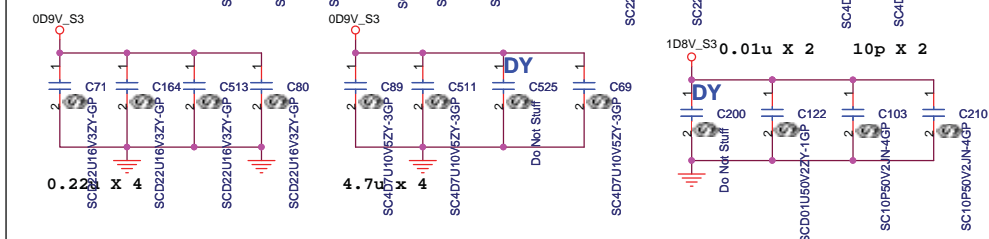
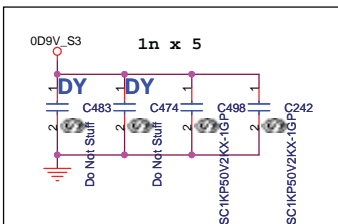
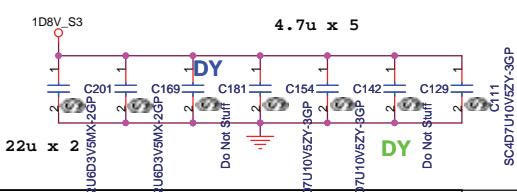
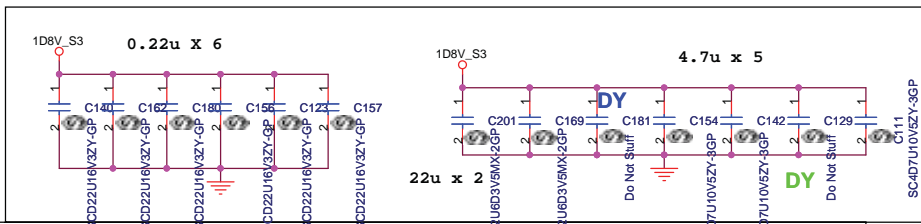
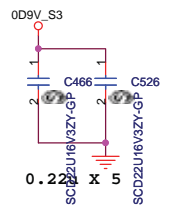
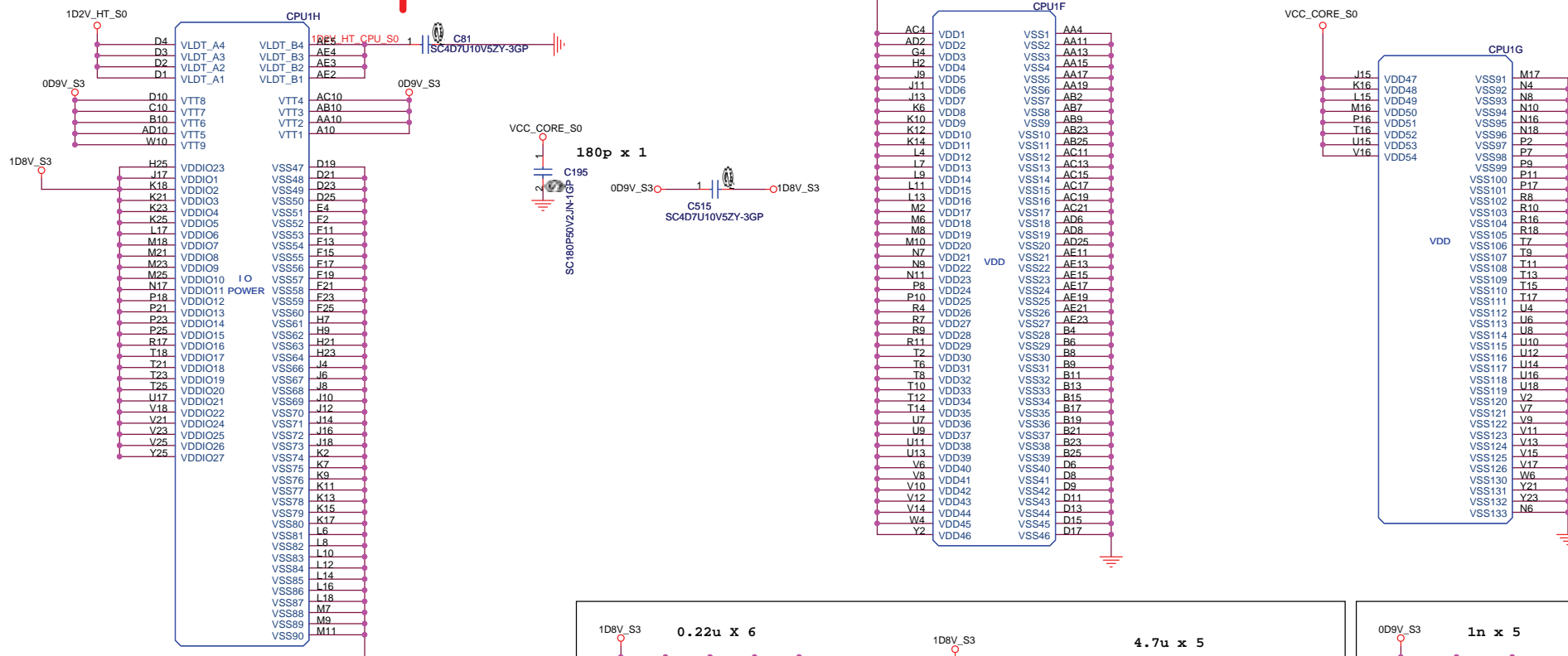


P20	RSVD_MBO_CLK_H0	RESSET_L	B18
P21	RSVD_MBO_CLK_H1	RESSET_L	B19
N20	RSVD_MBO_CLK_H0	RESSET_L	B3
N19	RSVD_MBO_CLK_H1	RESSET_L	C1
	RSVD_VIDSTRB0		
	RSVD_VDDNB_FB_H	H6	
	RSVD_VDDNB_FB_L	G6	
	RSVD_CORE_TYPE	D5	
	MISC		
	INTERNAL		
R26	RSVD_MBO_CLK_H3	FREE5	R24
R25	RSVD_MBO_CLK_L3	FREE6	W18
P22	RSVD_MBO_CLK_H0	FREE4	R23
R22	RSVD_MBO_CLK_H0	FREE1	AA8
	RSVD_MBO_CLK_L0	FREE2	H18
	RSVD_MBO_CLK_L0	FREE3	H19

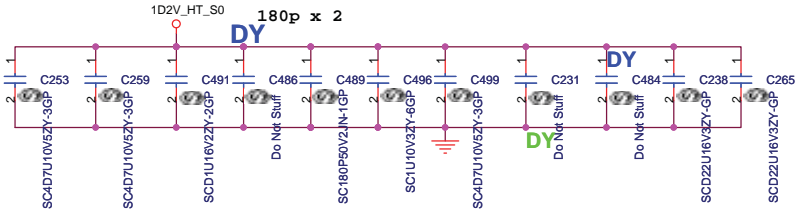
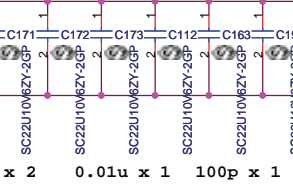
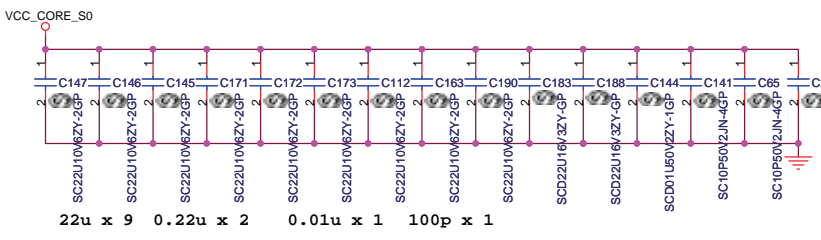


VREF_DDR_CLAW





LAYOUT: Place on backside of processor.



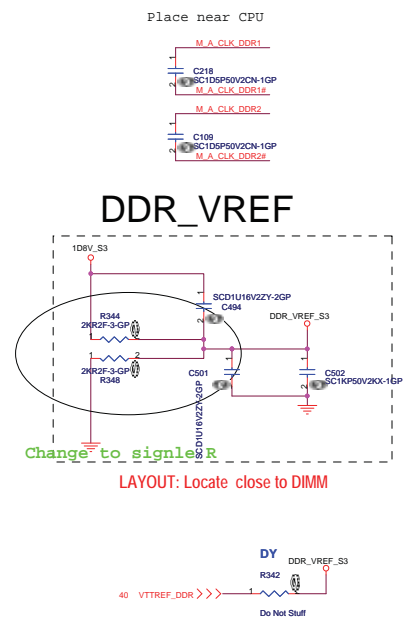
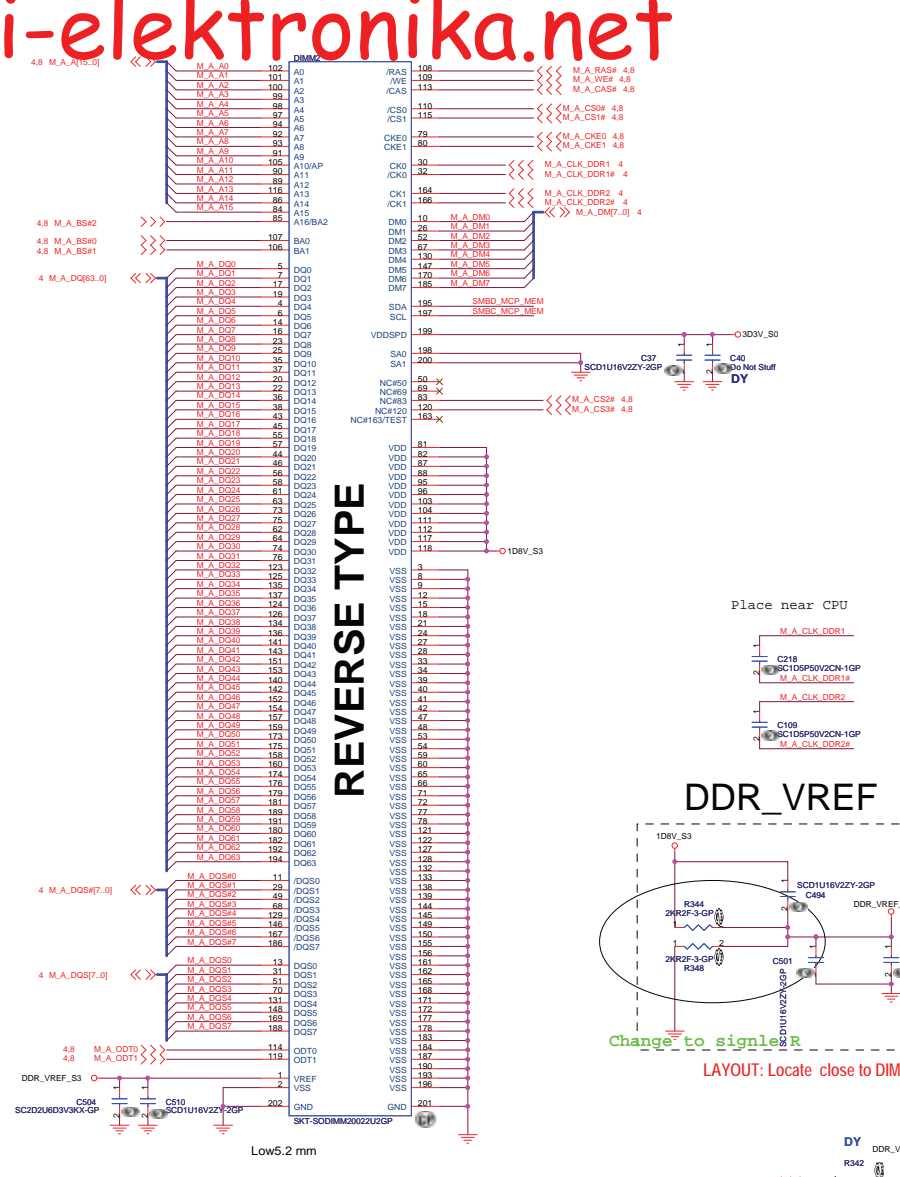
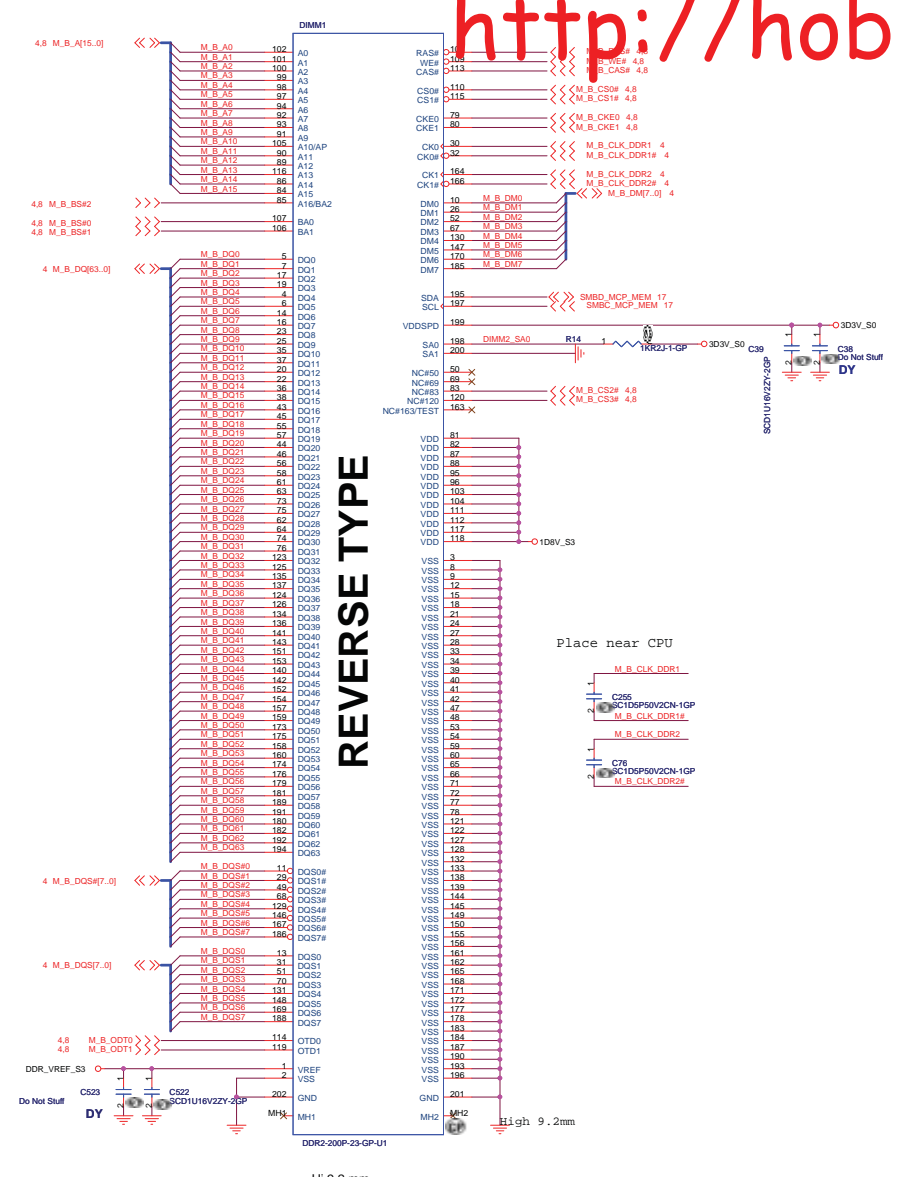
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4) POWER**

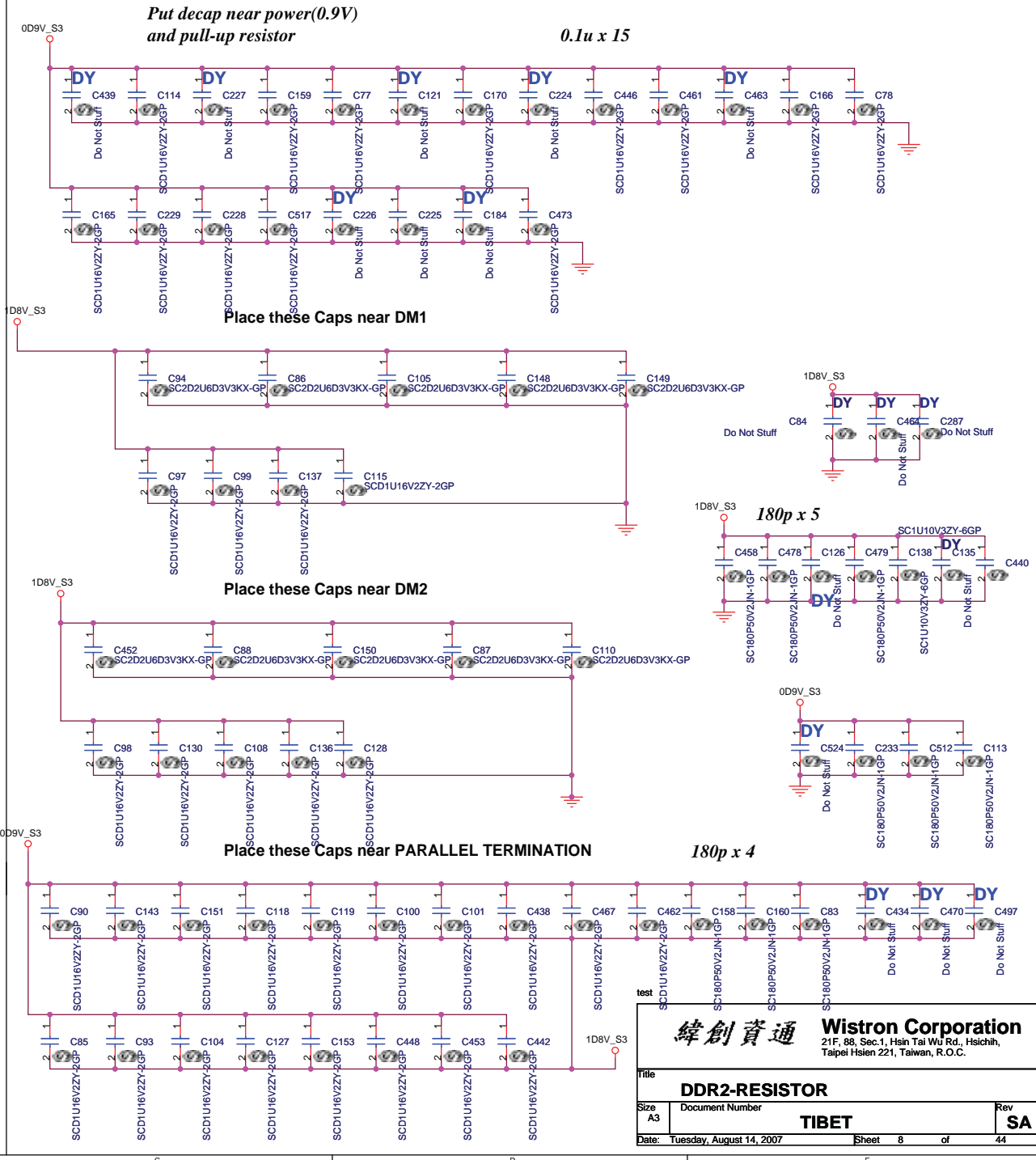
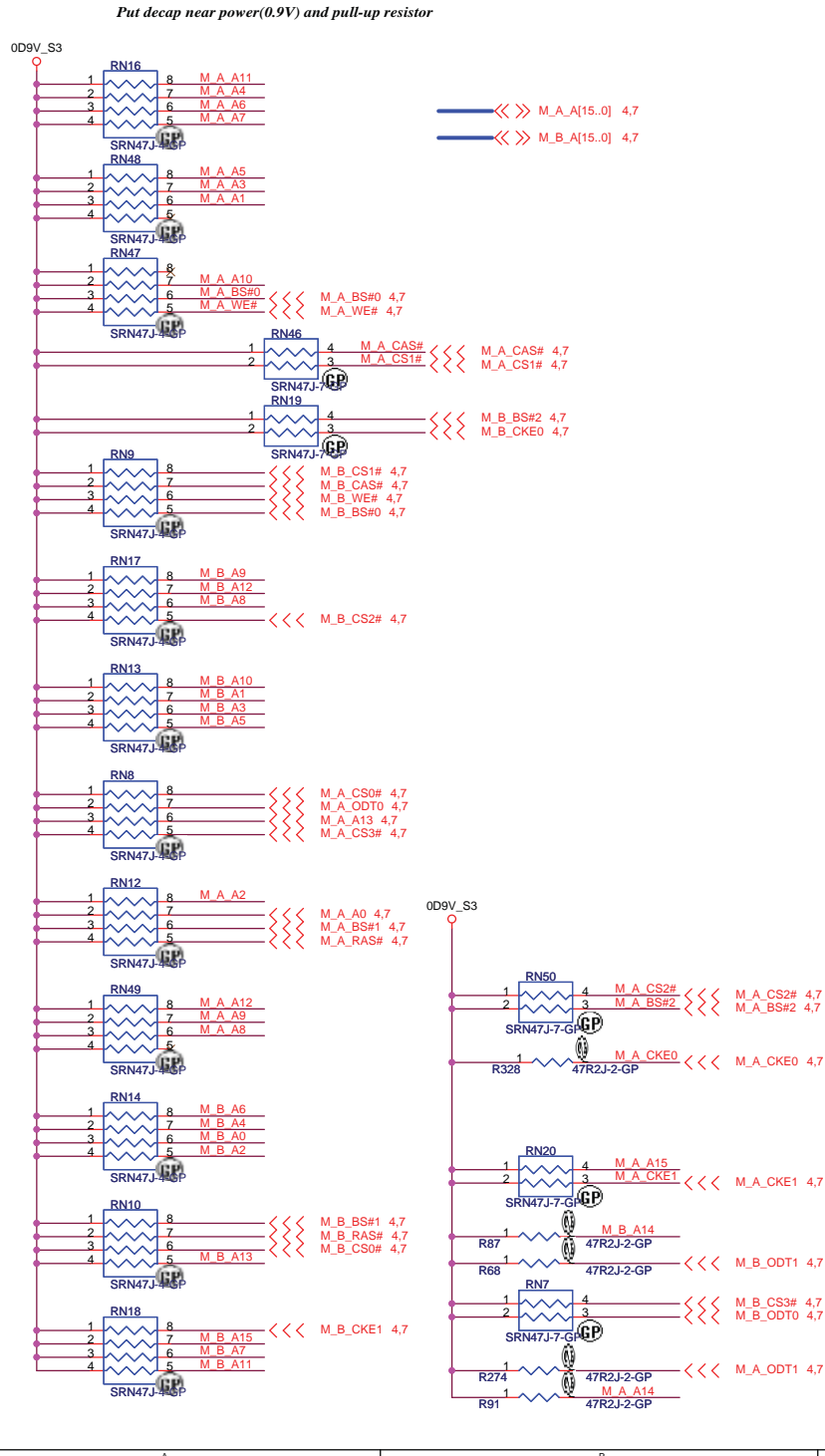
Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet 6 of 44



PARALLEL TERMINATION

<http://hobi-elektronika.decoupling-capacitor>



test

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Title	DDR2-RESISTOR		Rev
Size	Document Number	TIBET	SA
Date:	Tuesday, August 14, 2007	Sheet 8 of 44	

3 CPUCADOUT[15..0] <<<<
3 CPUCADOUTJ[15..0] <<<<

3 NB0CADOUT[15..0] <<<<
3 NB0CADOUTJ[15..0] <<<<

U55A 1 OF 8



3 CPUHTTCLKOUT0 >>>> CPUHTTCLKOUT0 AJ17 HT_MCP_RX_CLK0_P
3 CPUHTTCLKOUTJ0 >>>> CPUHTTCLKOUTJ0 AH17 HT_MCP_RX_CLK0_N
3 CPUHTTCLKOUT1 >>>> CPUHTTCLKOUT1 AL14 HT_MCP_RX_CLK1_P
3 CPUHTTCLKOUTJ1 >>>> CPUHTTCLKOUTJ1 AK14 HT_MCP_RX_CLK1_N

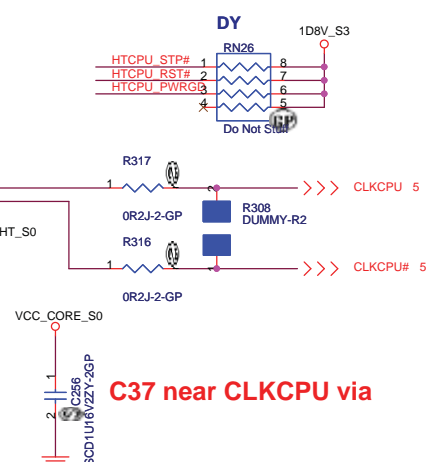
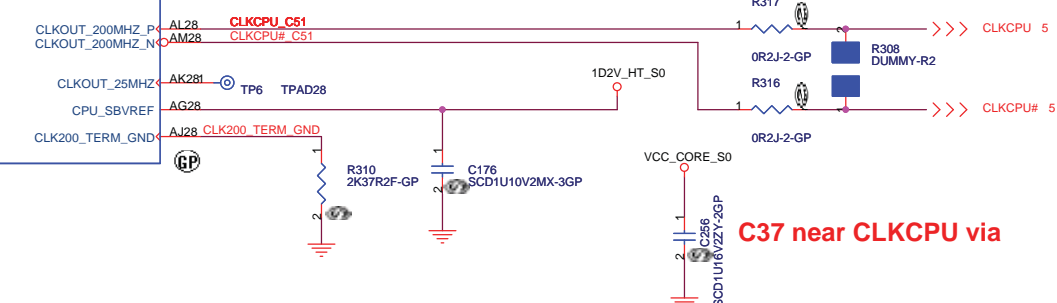
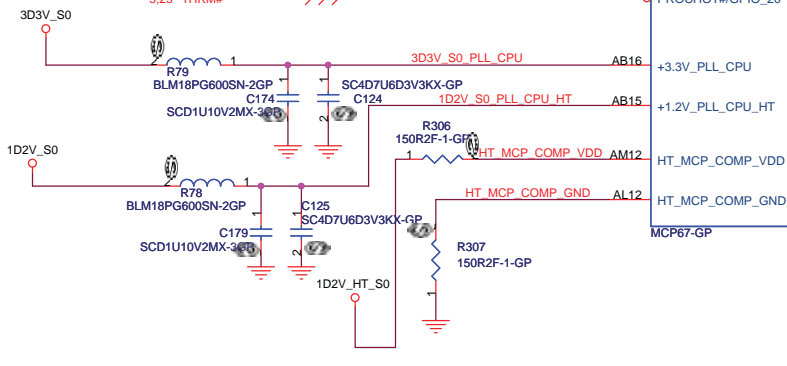
3 NB0HTTCLKOUT0 >>>> NB0HTTCLKOUT0 3 AK23 NB0HTTCLKOUT0
3 NB0HTTCLKOUTJ0 >>>> NB0HTTCLKOUTJ0 3 AJ23 NB0HTTCLKOUTJ0
3 NB0HTTCLKOUT1 >>>> NB0HTTCLKOUT1 3 AG23 NB0HTTCLKOUT1
3 NB0HTTCLKOUTJ1 >>>> NB0HTTCLKOUTJ1 3 AH23 NB0HTTCLKOUTJ1

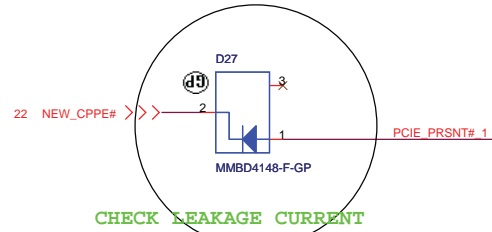
3 CPUHTTCTLOUT0 >>>> CPUHTTCTLOUT0 AH19 HT_MCP_RXCTL0_P
3 CPUHTTCTLOUTJ0 >>>> CPUHTTCTLOUTJ0 AG19 HT_MCP_RXCTL0_N
RESERVED#AC18
RESERVED#AD18

3 NB0HTTCTLOUT 3 AK20 NB0HTTCTLOUT 3
3 NB0HTTCTLOUTJ 3 AJ20 NB0HTTCTLOUTJ 3
RESERVED#AD19
RESERVED#AC19

5 CPU_THERMTRIP# >>>> AC13 THERMTRIP#/GPIO_58
5.23 THRM# >>>> AB13 PROCHOT#/GPIO_20

HT_CPU_REQ# AD23 HT_CPU_REQ# 1
HT_CPU_STOP# AB20 HT_CPU_STOP# 5
HT_CPU_RST# AC21 HT_CPU_RST# 5
HT_CPU_PWRGD AD22 HT_CPU_PWRGD 5



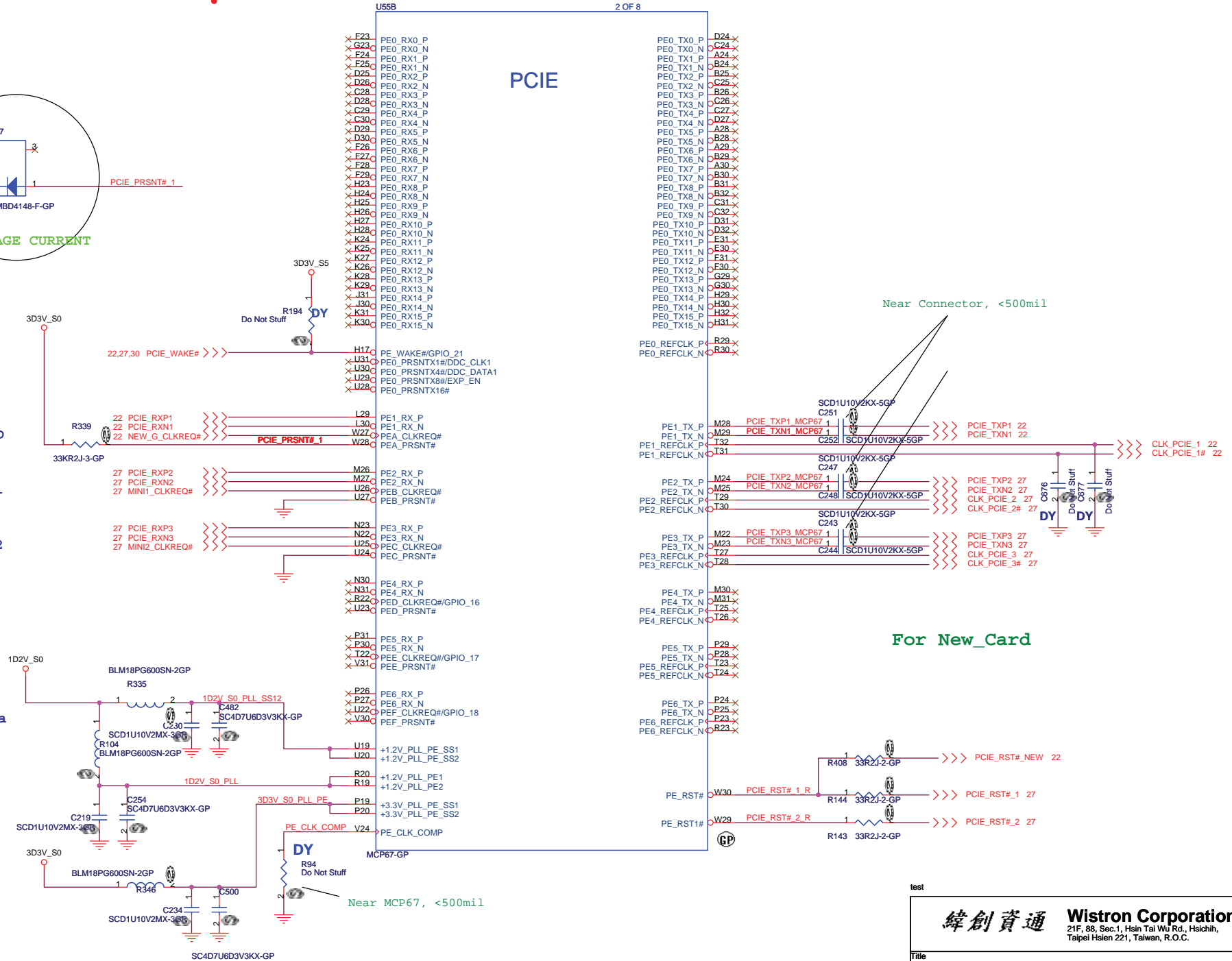


NEW CARD

MINI CARD1

MINI CARD2

C675 close to CLK_PCIE_1/# L3 to L6 via

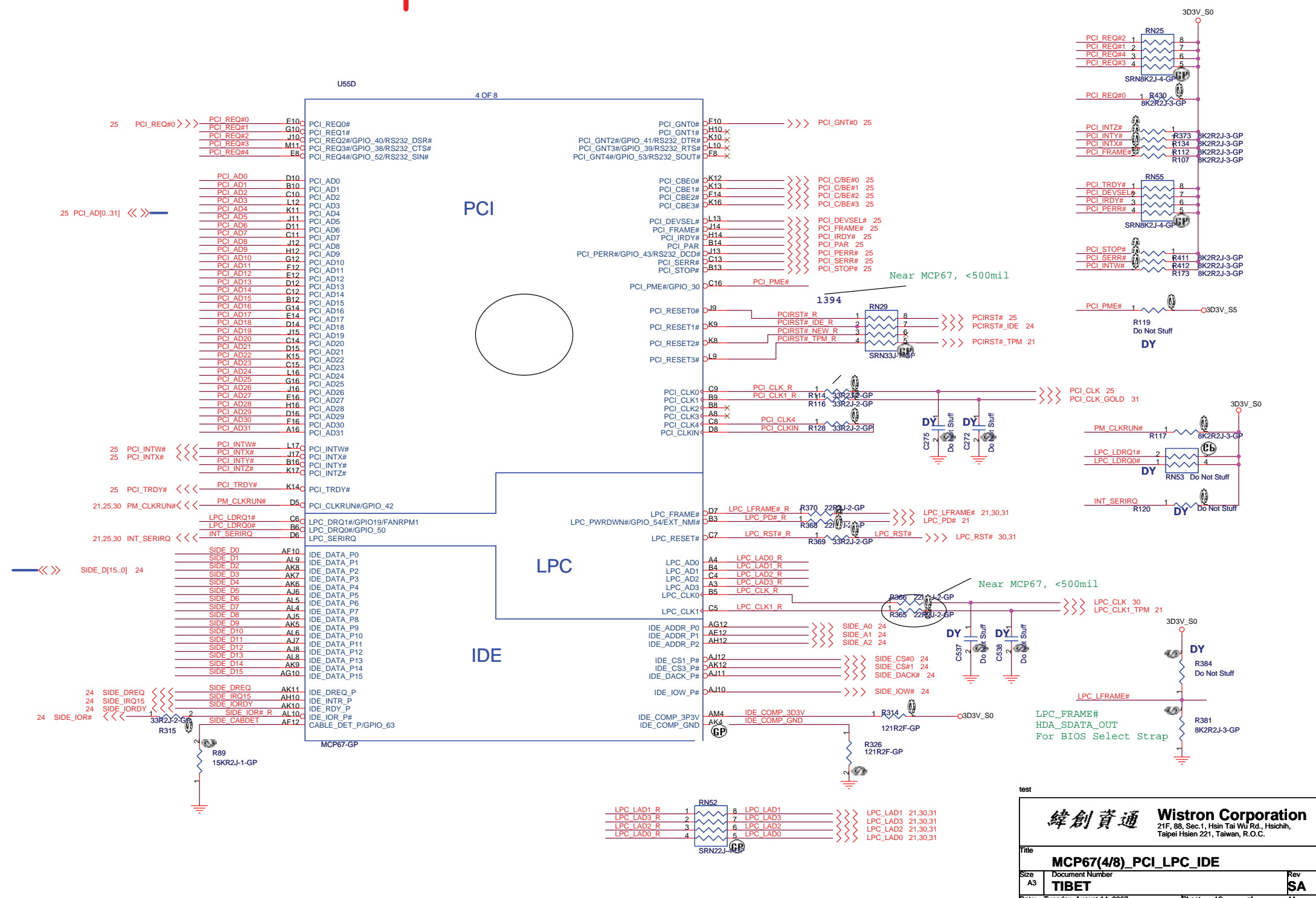


Near Connector, <500mil

For New_Card

test

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title MCP67(2/8)_PCIE	
Size A3	Document Number TIBET
Date: Tuesday, August 14, 2007	Rev SA
Sheet 10 of 44	



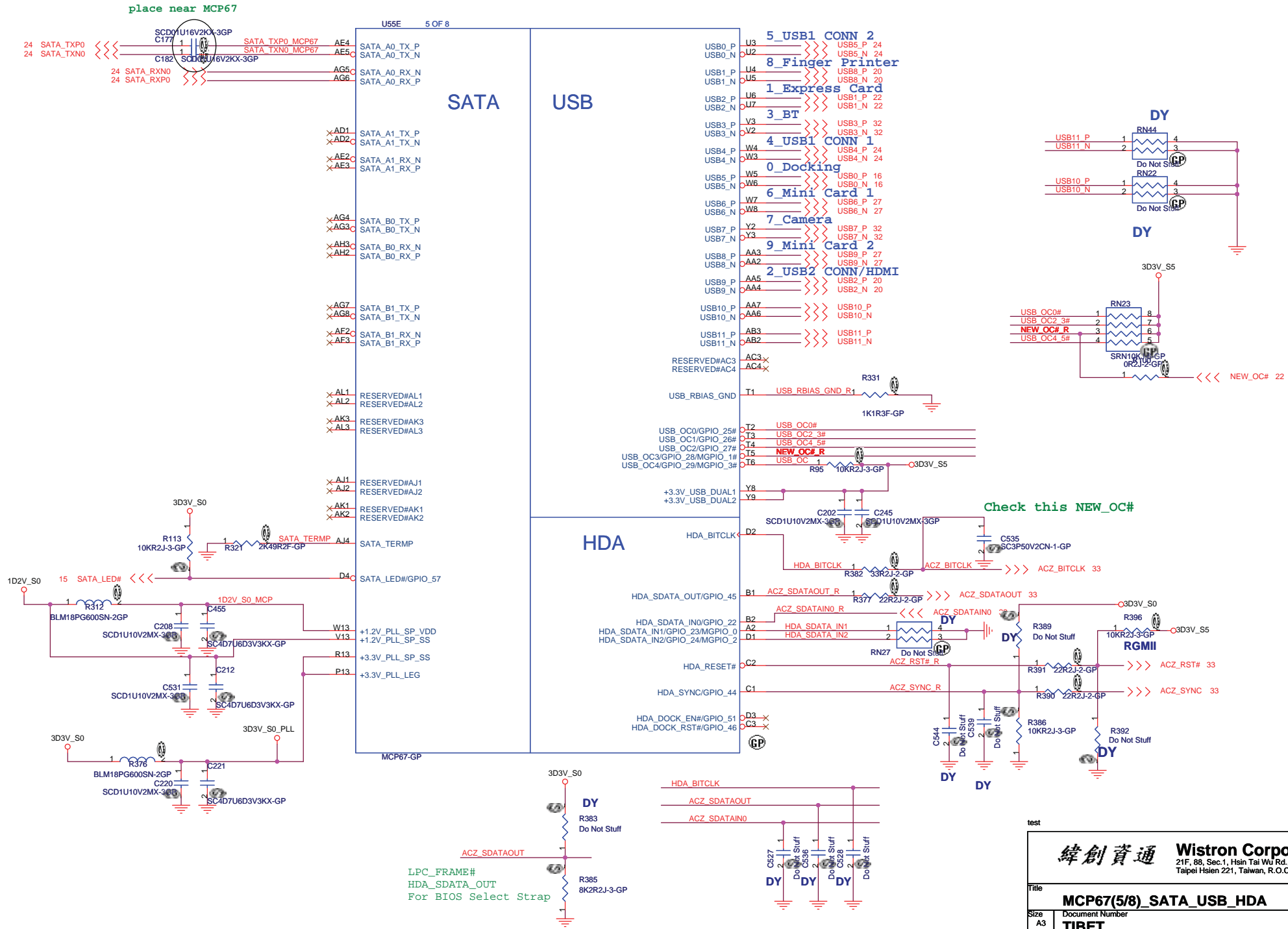
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP67(4/8)_PCI_LPC_IDE

Size: A3 Document Number: TIBET Rev: SA

Date: Tuesday, August 14, 2007 Sheet 12 of 44



test

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

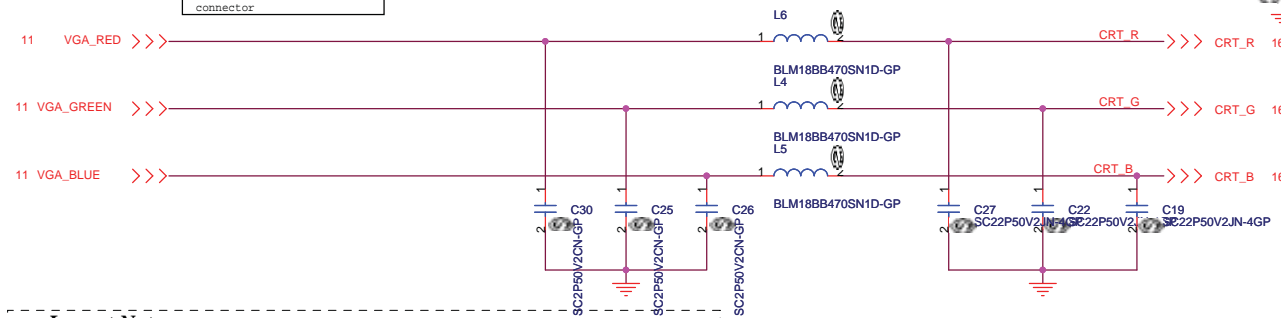
Title: **MCP67(5/8)_SATA_USB_HDA**

Size: A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 13 of 44

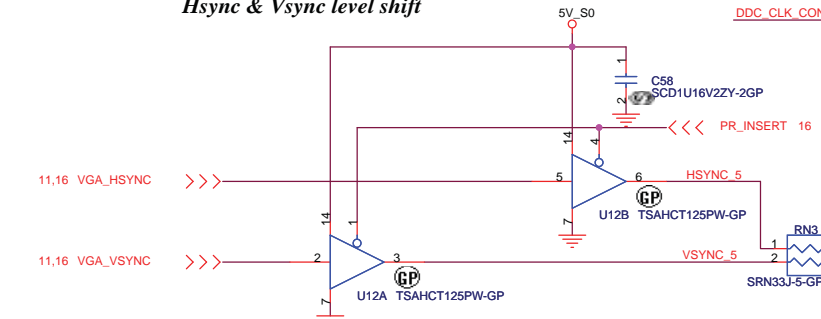
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector



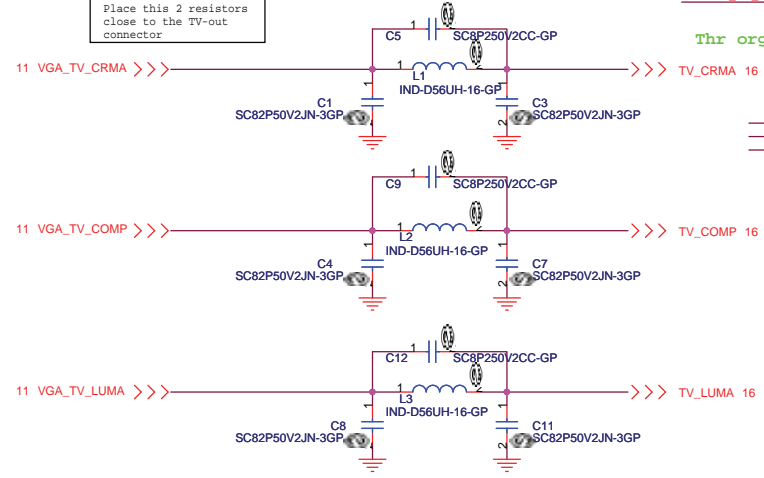
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

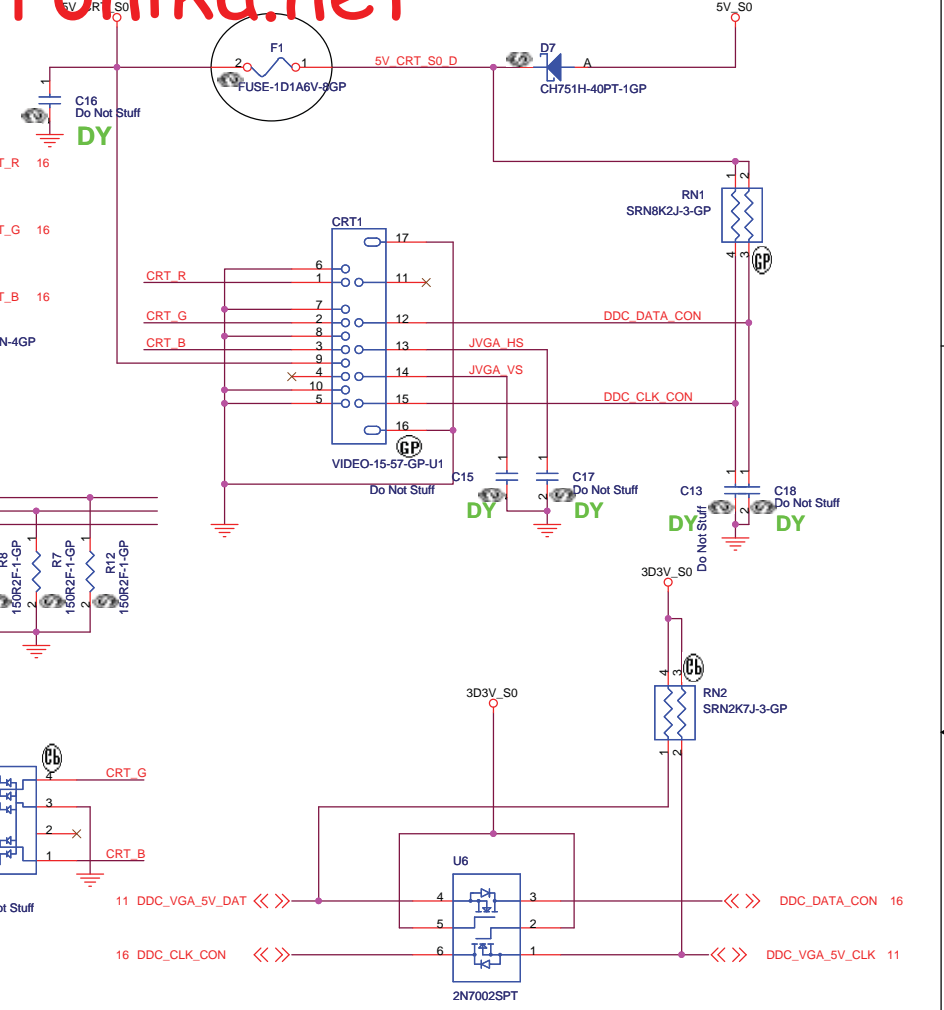
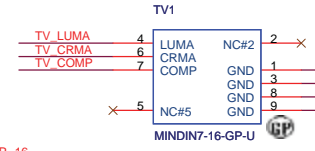


TV OUT CONN

Layout Note:
Place this 2 resistors close to the TV-out connector



Thr org part is 68.2703N.10B



5V @ ext. CRT side

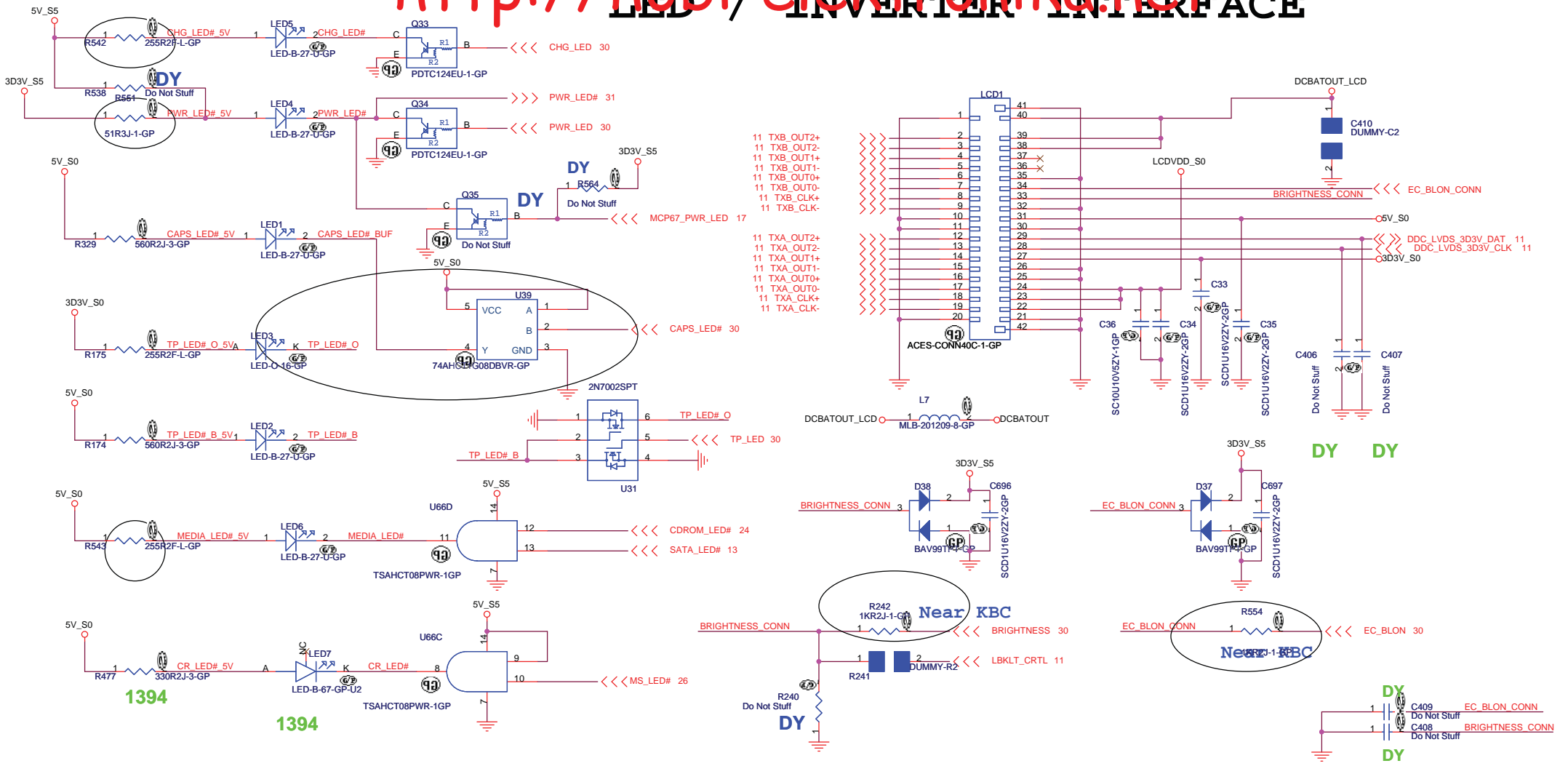
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

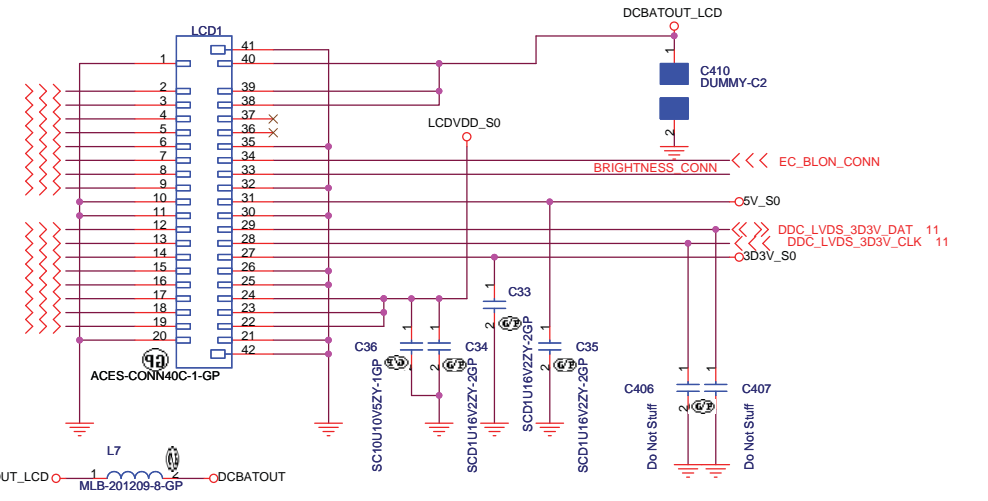
Title: **CRT/TV CONNECTOR**

Size A3	Document Number	Rev SA
TIBET		
Date: Tuesday, August 14, 2007	Sheet 14	of 44

LED / INVERTER INTERFACE



- 11 TXB_OUT2+
- 11 TXB_OUT2-
- 11 TXB_OUT1+
- 11 TXB_OUT1-
- 11 TXB_OUT0+
- 11 TXB_OUT0-
- 11 TXB_CLK+
- 11 TXB_CLK-
- 11 TXA_OUT2+
- 11 TXA_OUT2-
- 11 TXA_OUT1+
- 11 TXA_OUT1-
- 11 TXA_OUT0+
- 11 TXA_OUT0-
- 11 TXA_CLK+
- 11 TXA_CLK-



1394

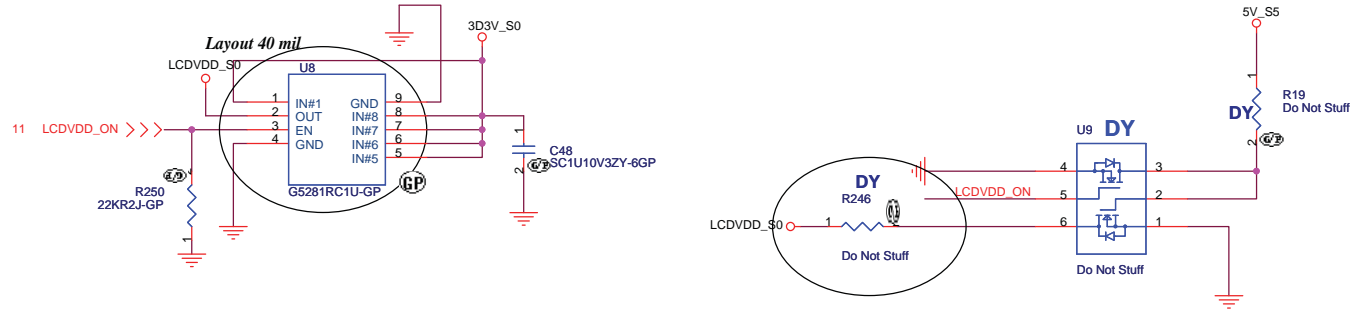
1394

Near KBC

Near KBC

DY

DY



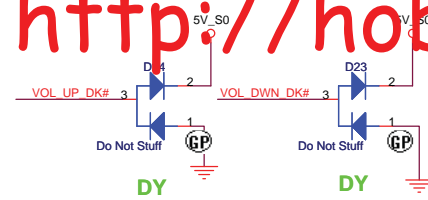
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

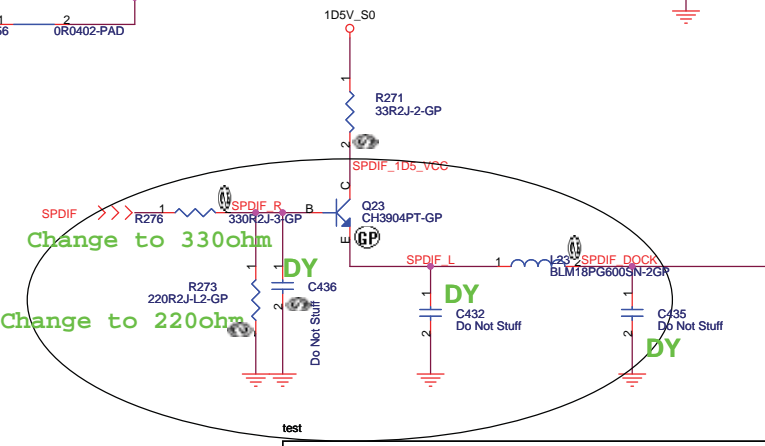
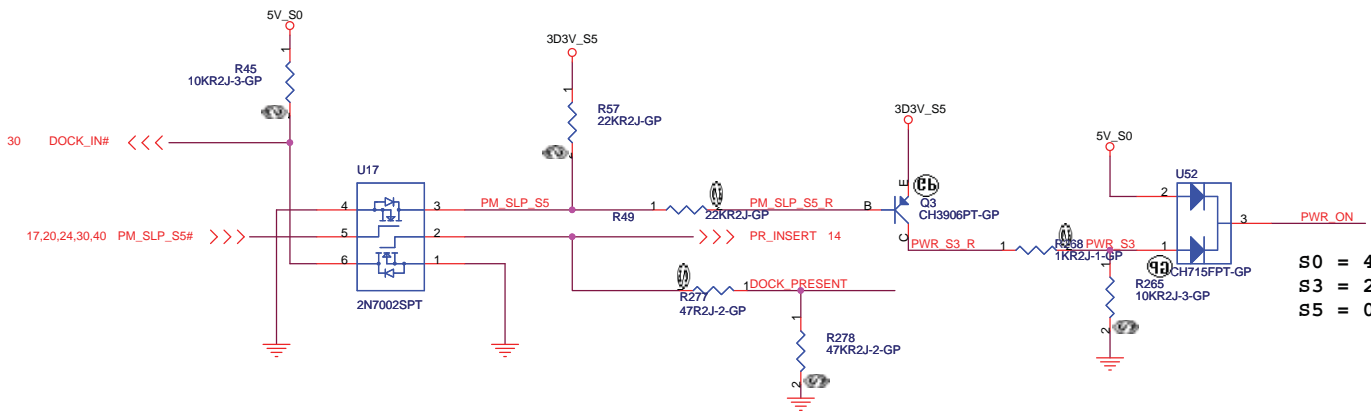
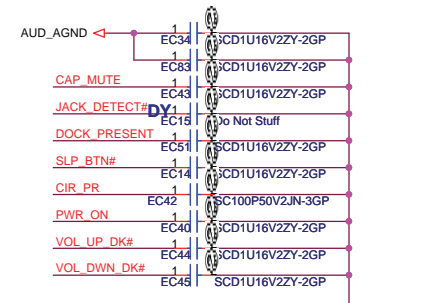
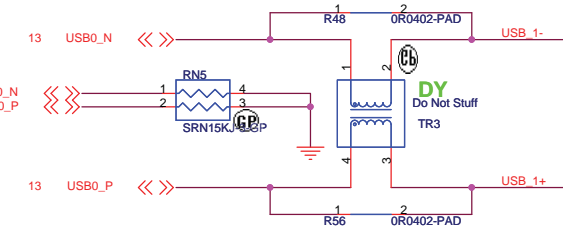
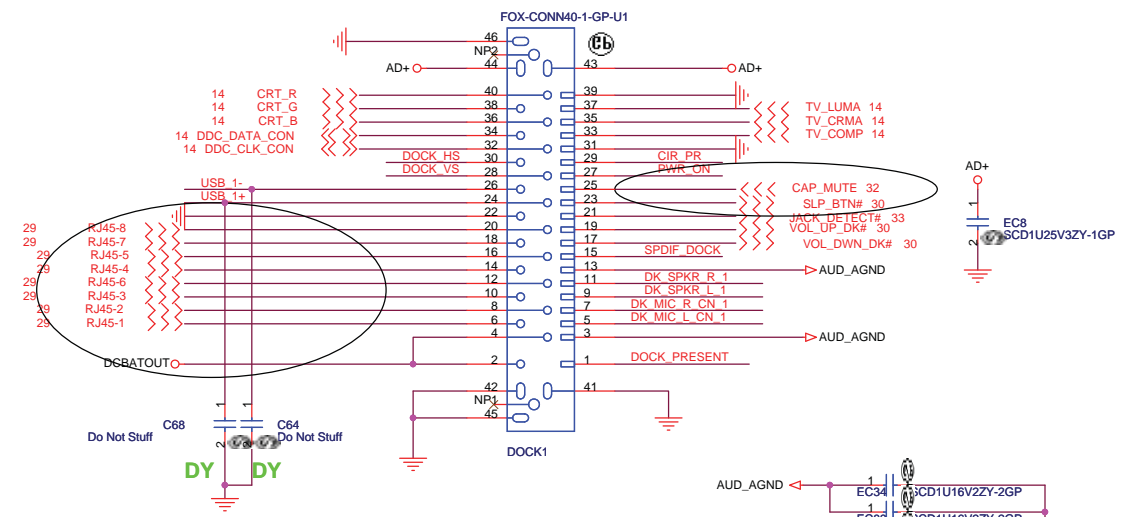
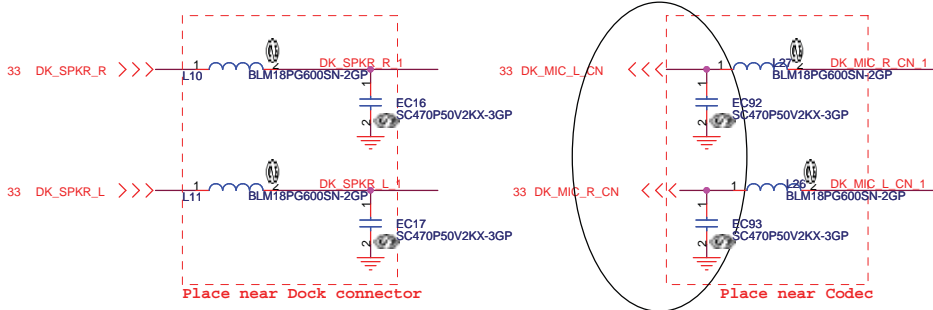
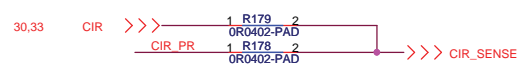
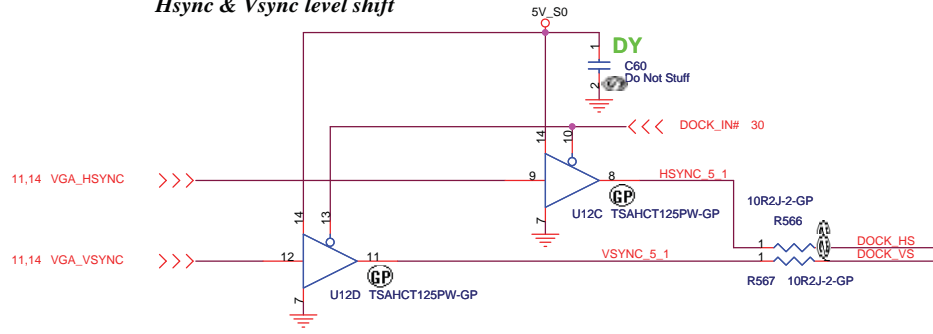
Title: **LCD/Inverter Connector**

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	TIBET	SA

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Hsync & Vsync level shift



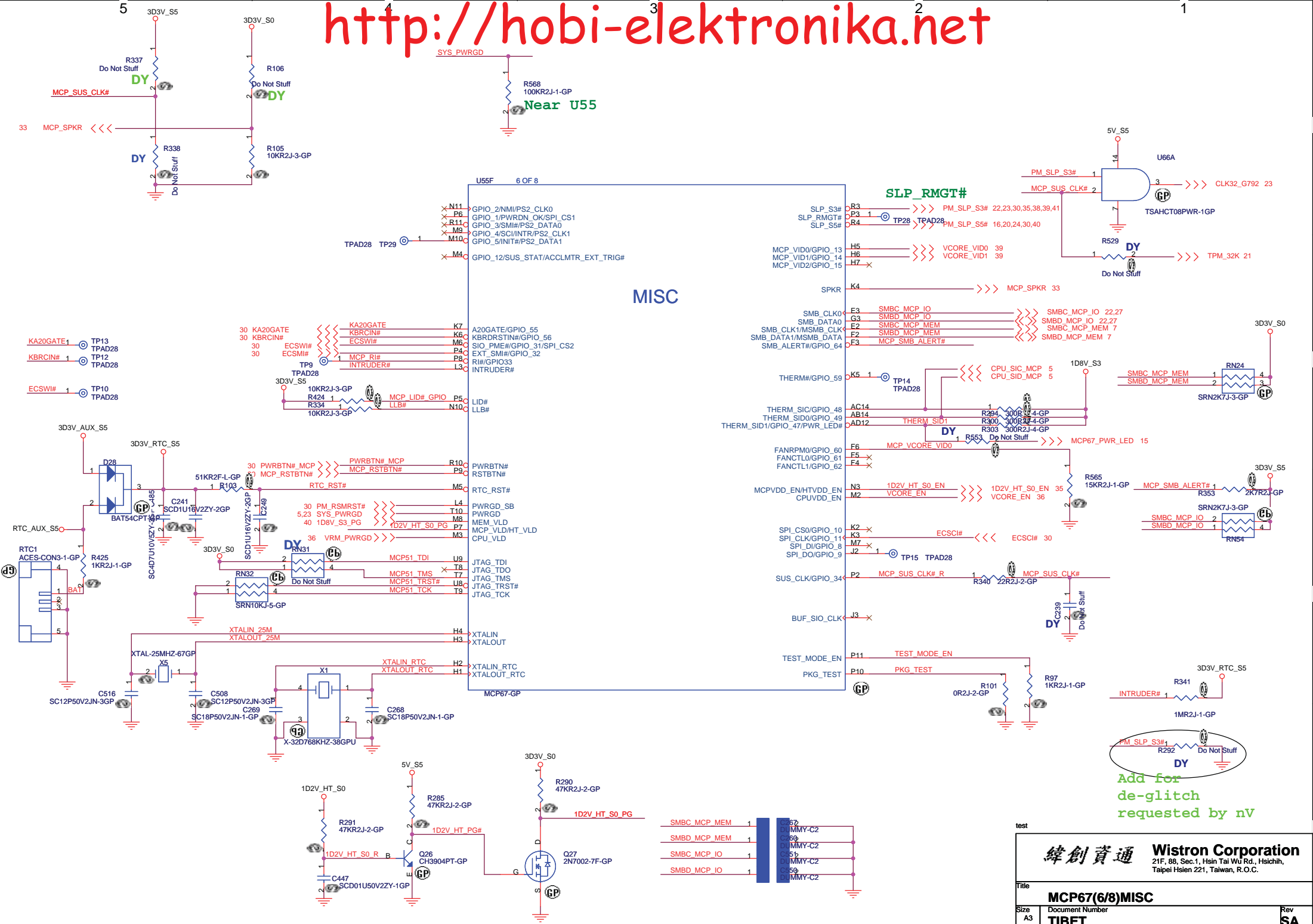
S0 = 4V
S3 = 2.5V
S5 = 0V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

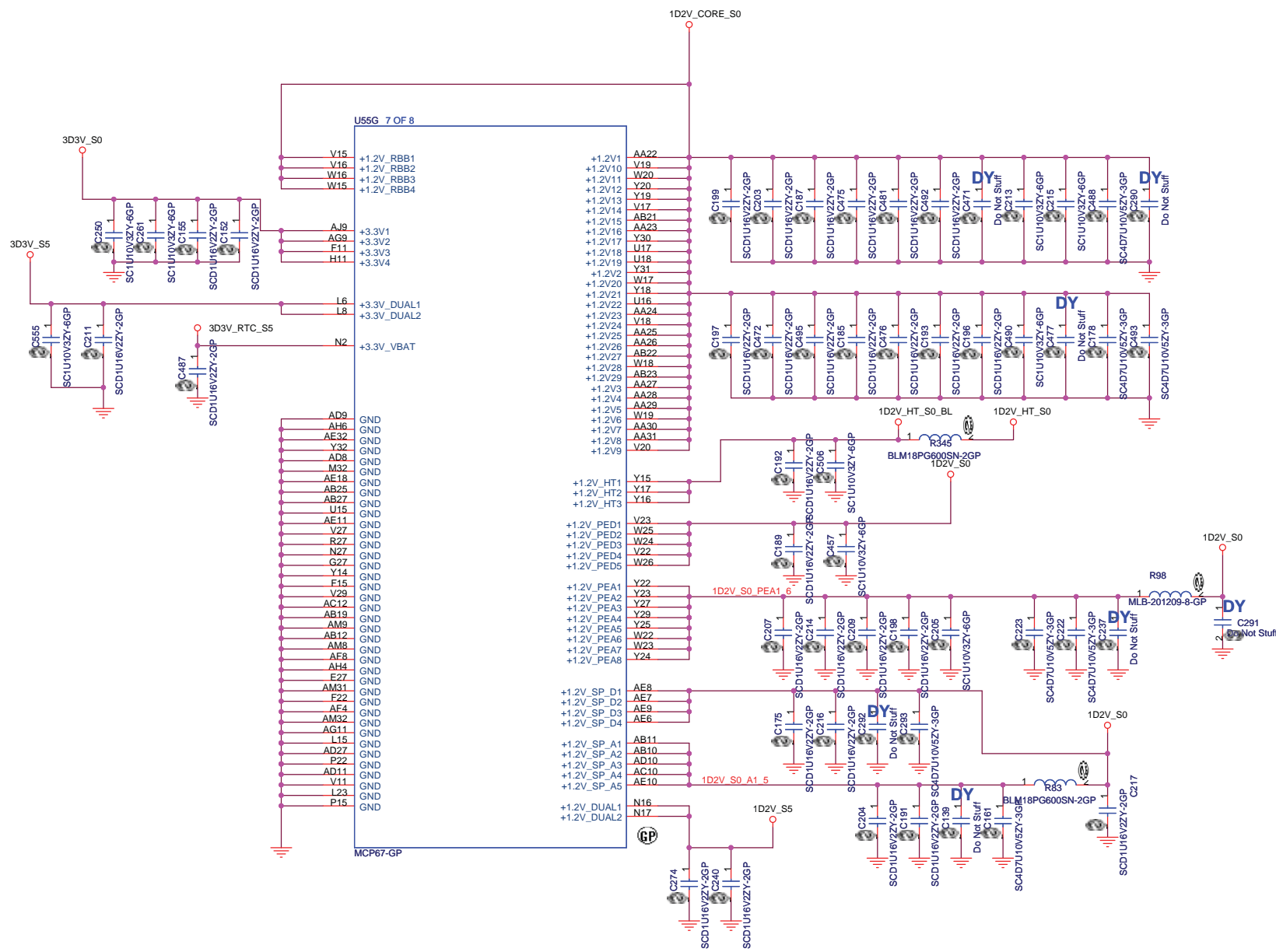
Size: A3 Document Number: **TIBET** Rev: **SA**

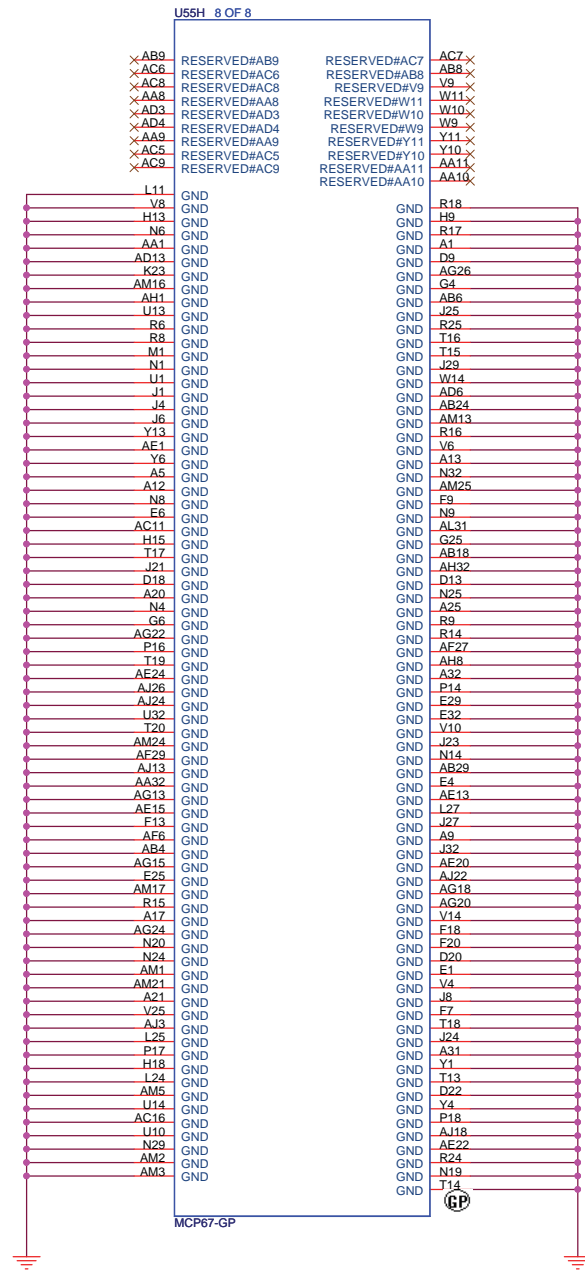
Date: Tuesday, August 14, 2007 Sheet: 16 of 44

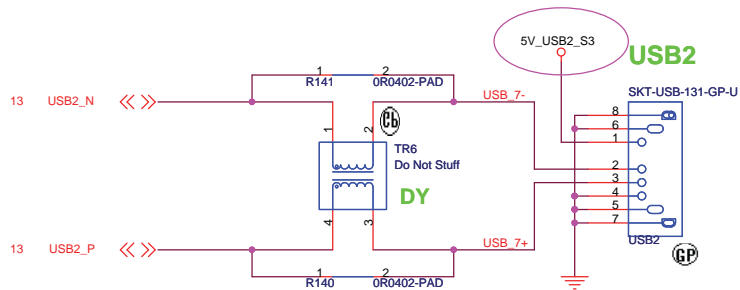
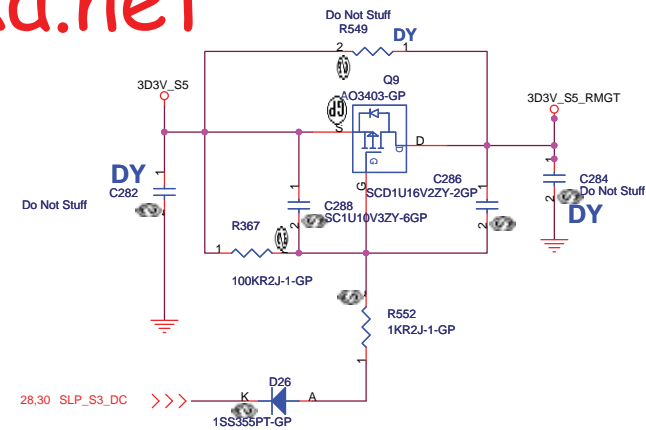
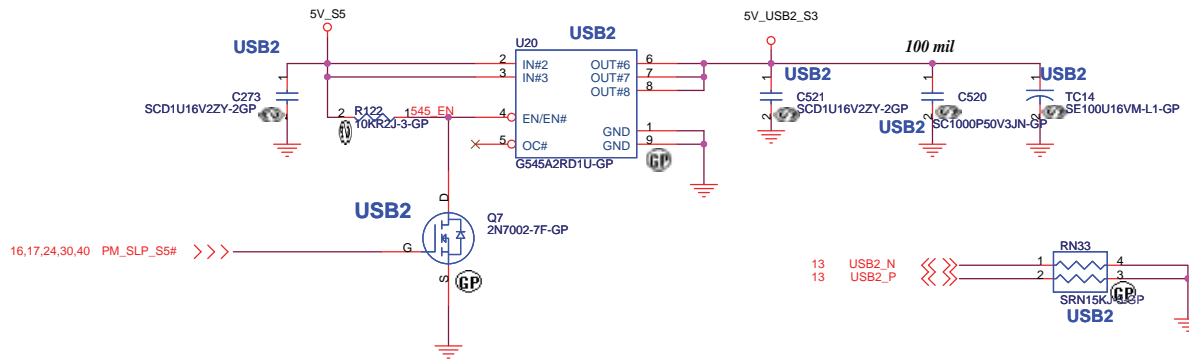


Add for de-glitch requested by nV

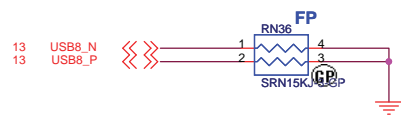
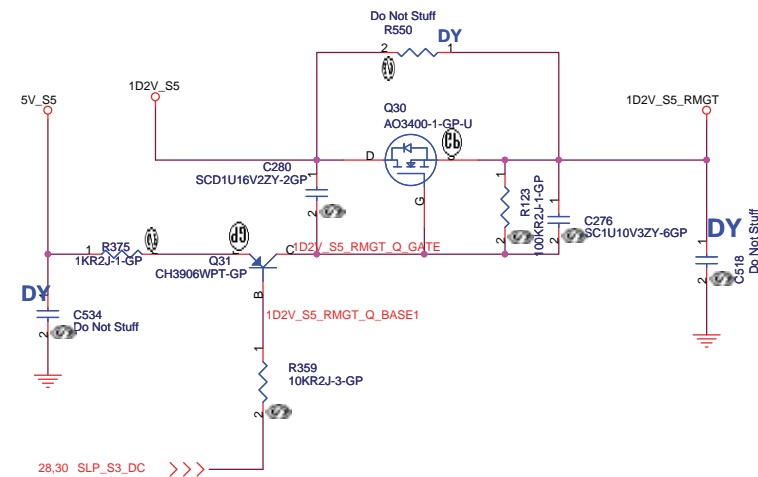
Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MCP67(6/8)MISC	
Title:	Document Number:
Size: A3	TIBET
Date: Tuesday, August 14, 2007	Sheet 17 of 44
Rev: SA	



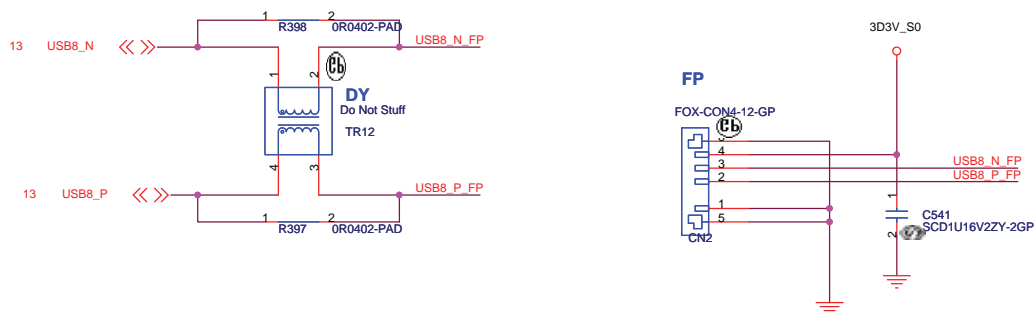




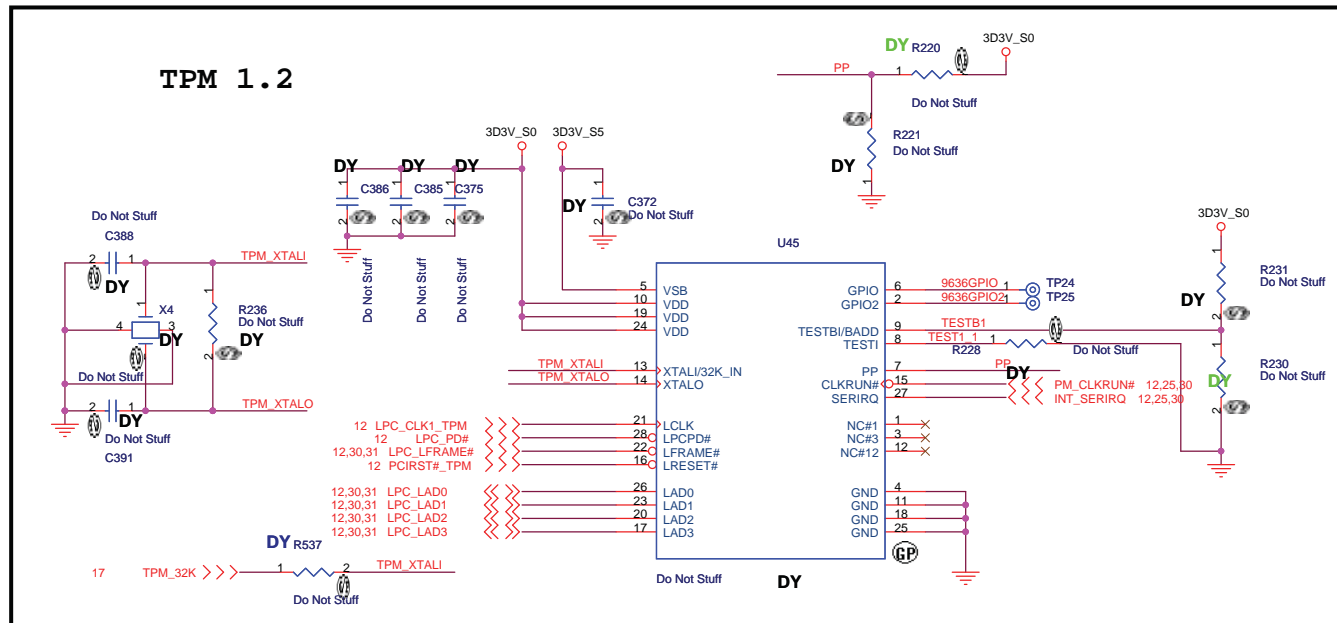
??? Current Rating



Finger Printer



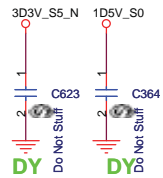
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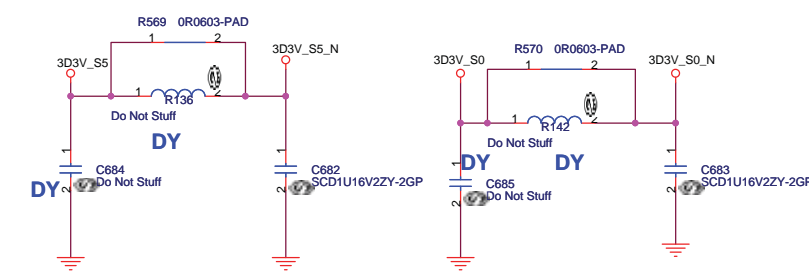
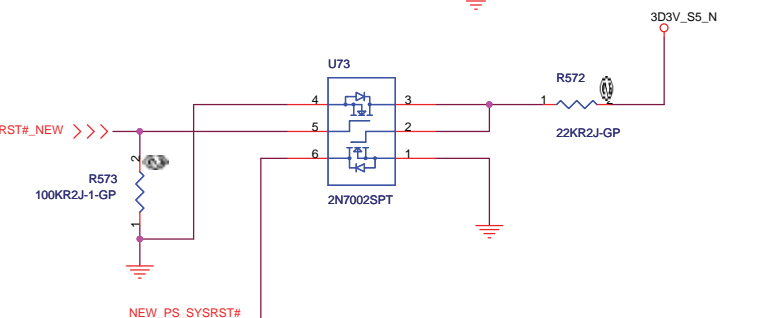
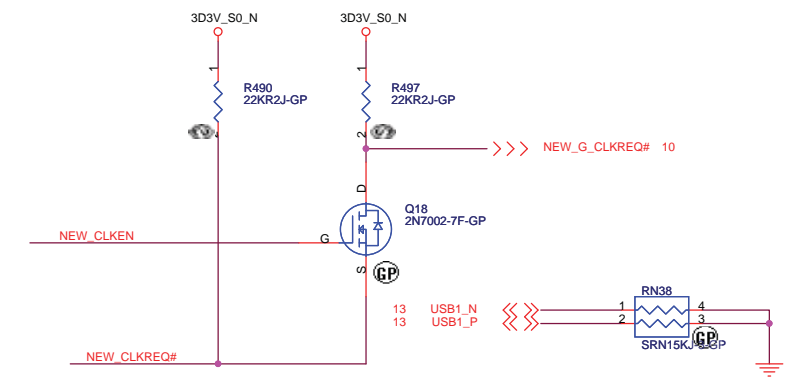
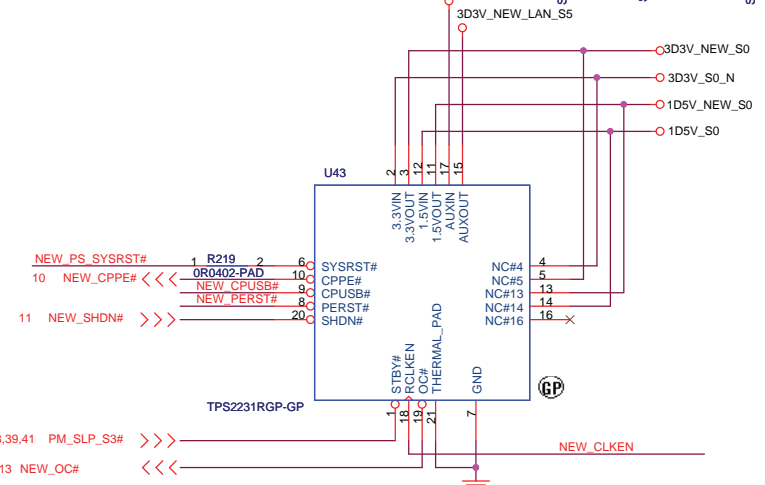
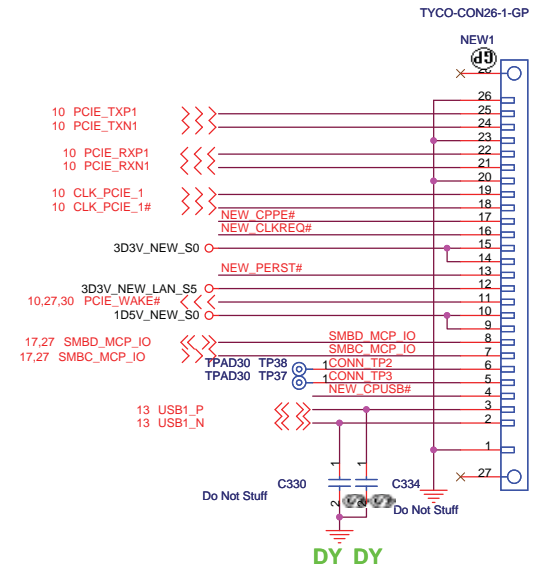
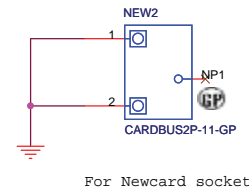
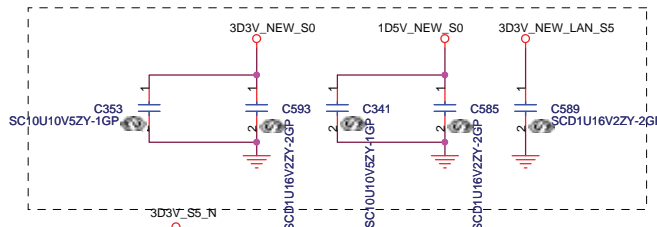
test

NEWCARD Connector

Place them Near to Chip



Place them Near to Connector

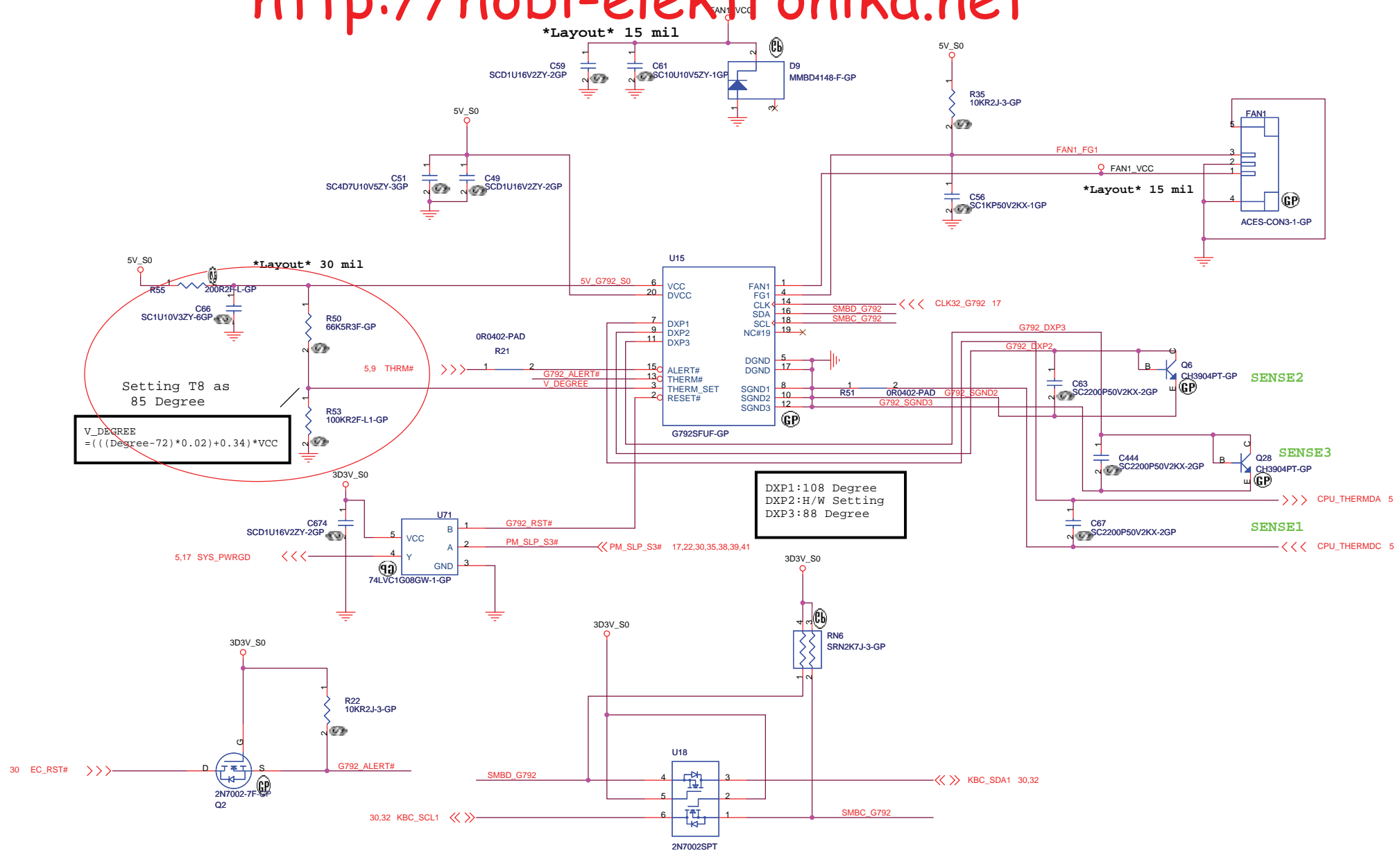


test

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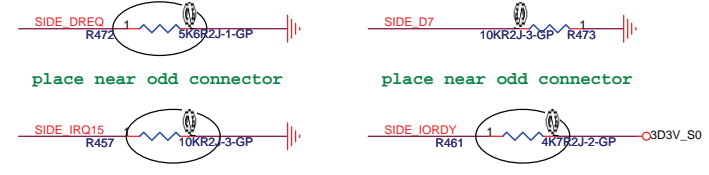
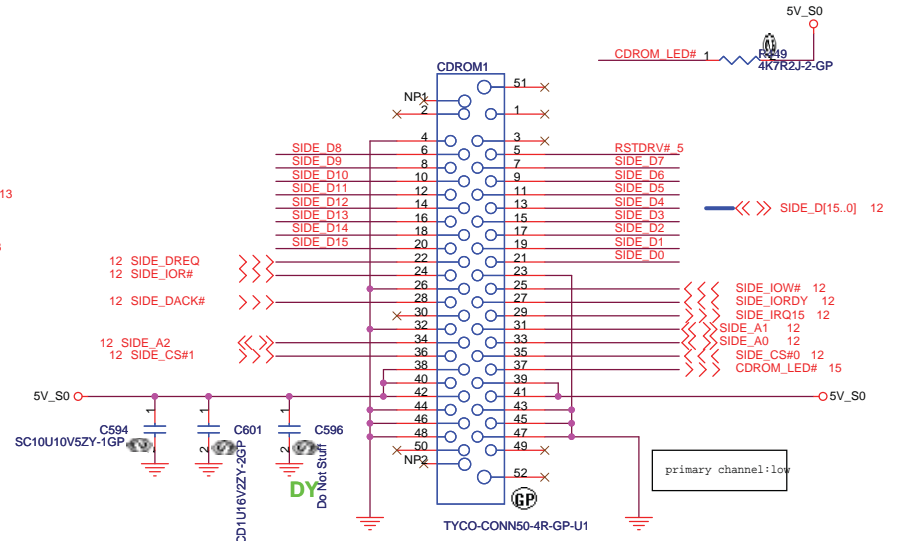
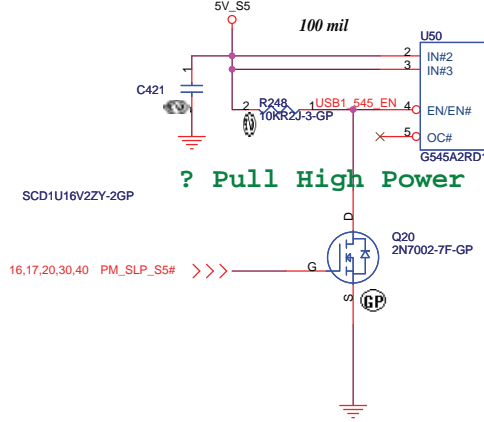
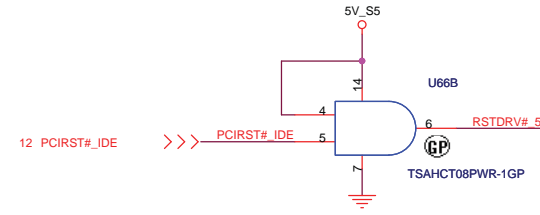
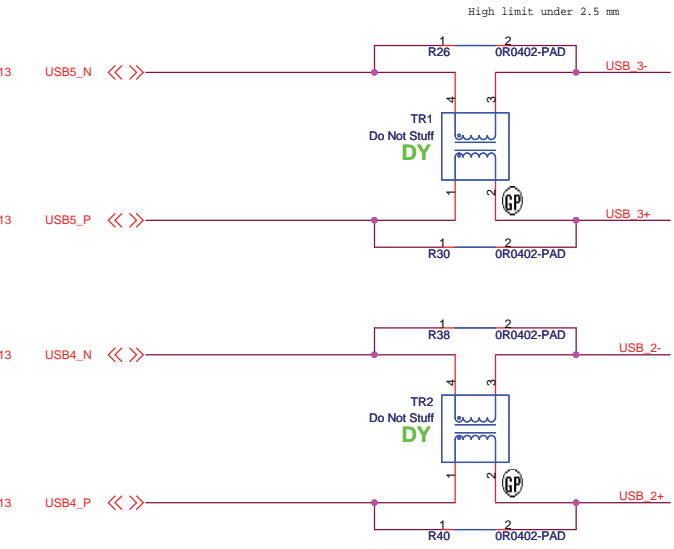
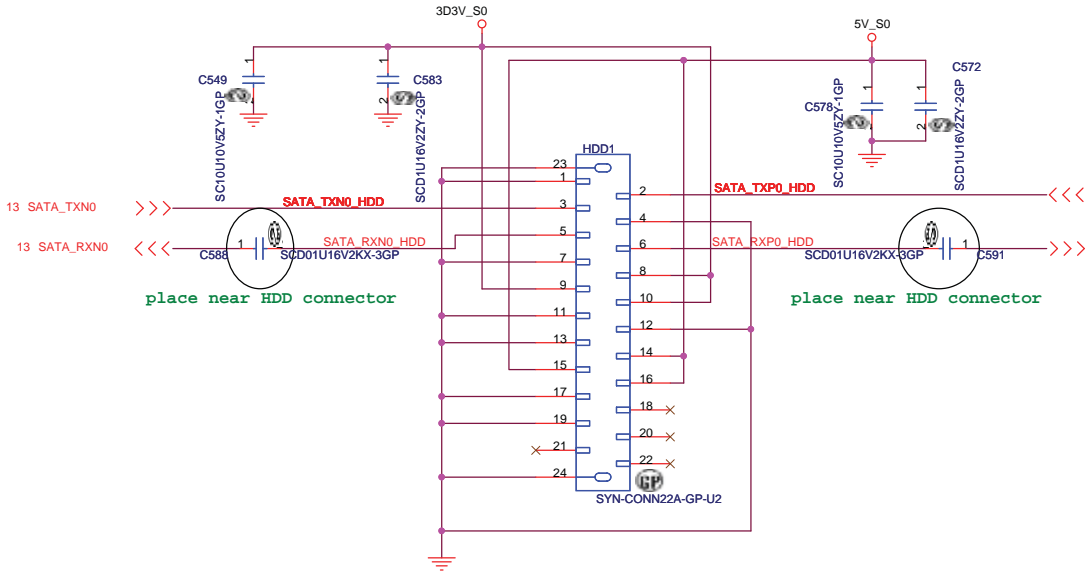
Title: **NEW CARD**

Size A3	Document Number	Rev SA
Date: Tuesday, August 14, 2007		Sheet 22 of 44

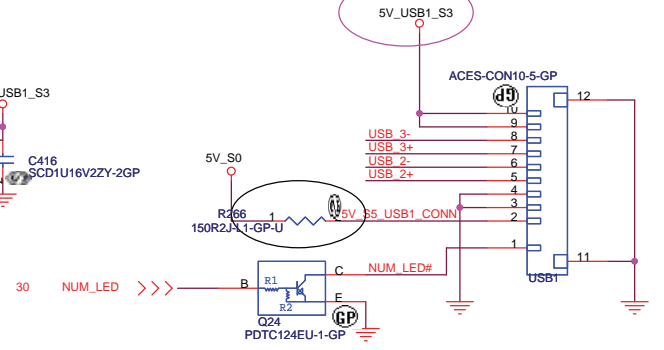


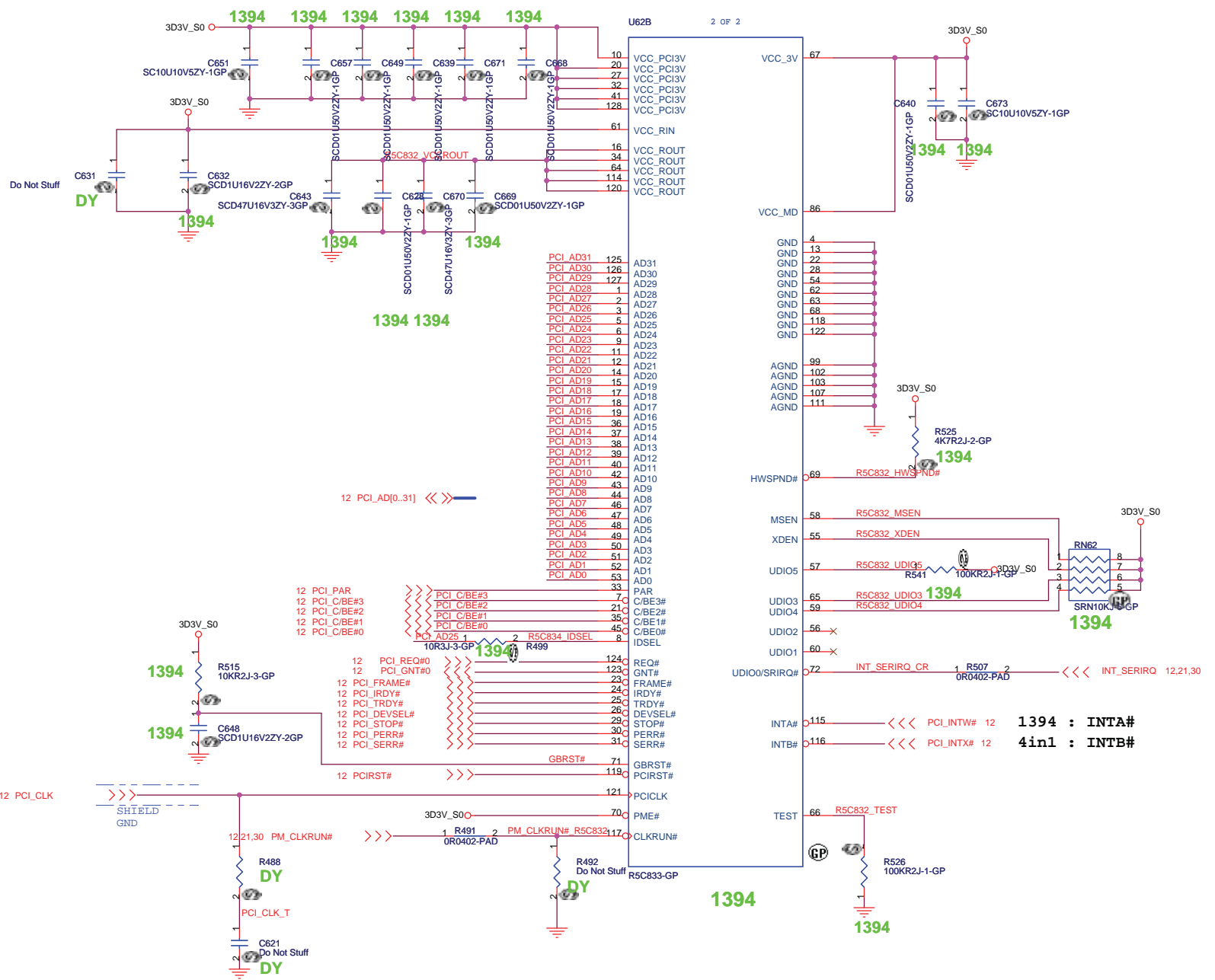
SATA HD Connector

CD-ROM CONNECTOR



USB PORT



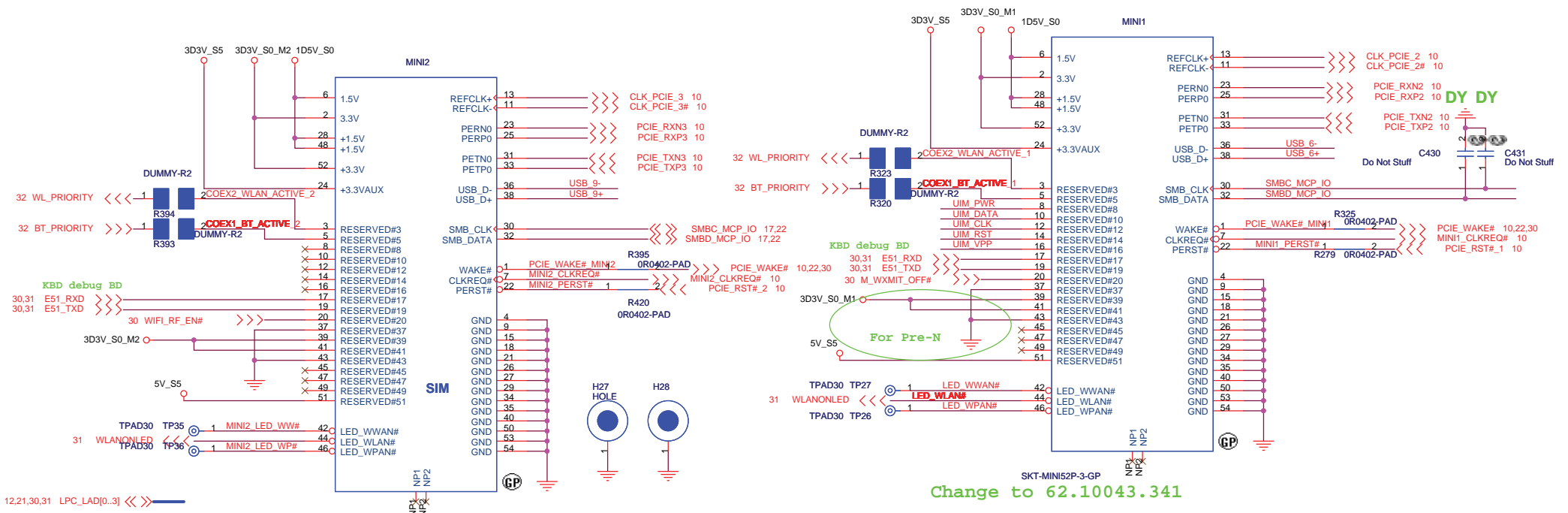


Mini Card Connector 2

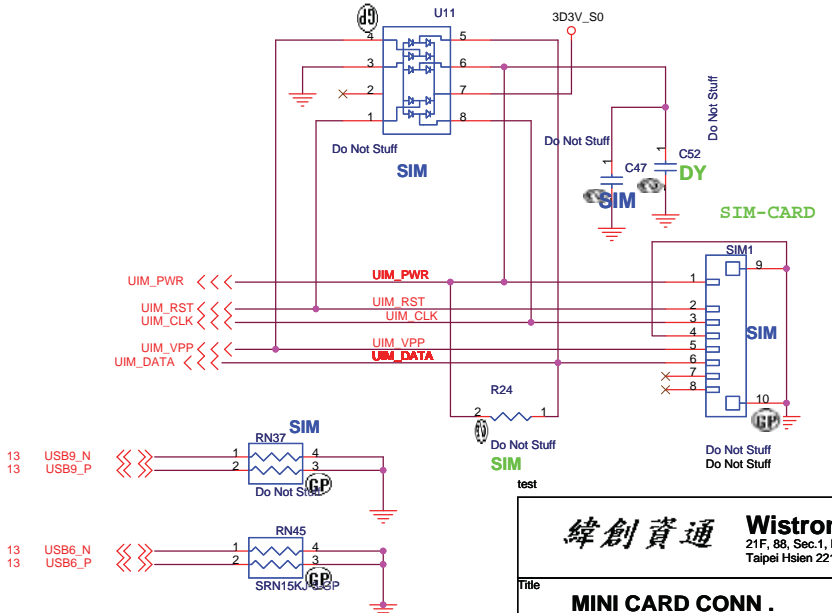
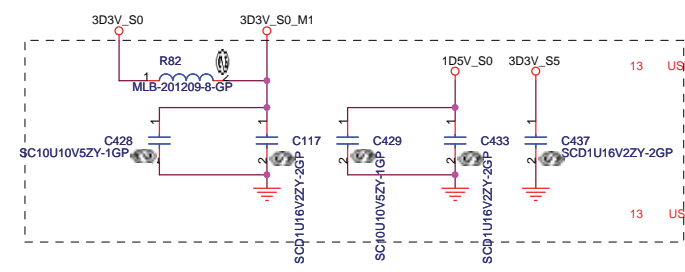
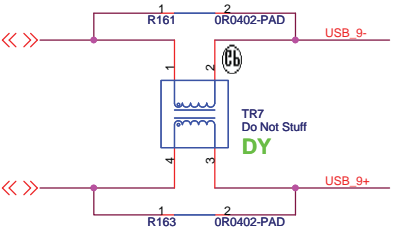
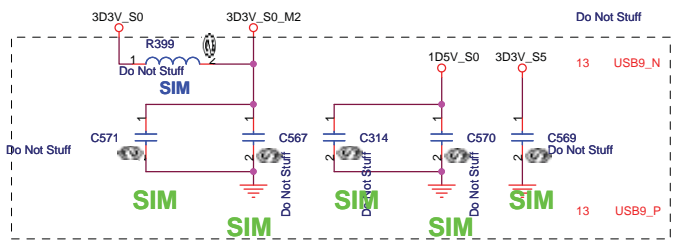
Wireless Card

Mini Card Connector 1

WWAN



Change to 62.10043.341



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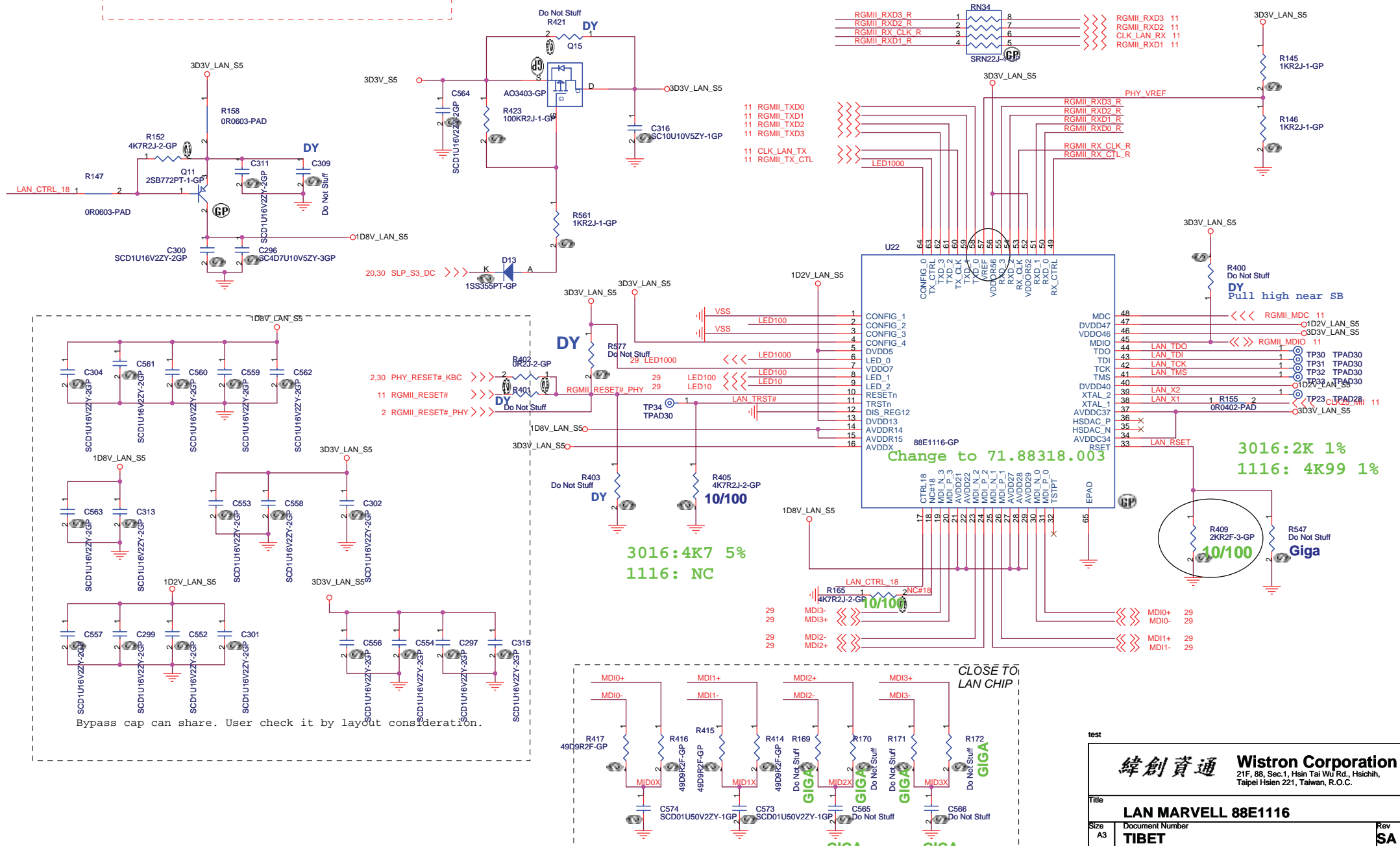
Title: **MINI CARD CONN.**

Size A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 27 of 44

- Hardware Configuration: See Config 0
1. PHY address:00001
 2. ENA_XC:Enable Auto-Crossover
 3. RGMII_TX:Transmit clock not internally delayed
 4. RGMII_RX:Receive clock transition when data transitions
 5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.



Change to 71.88318.003

3016:4K7 5%
1116: NC

3016:2K 1%
1116: 4K99 1%

Bypass cap can share. User check it by layout consideration.

CLOSE TO LAN CHIP

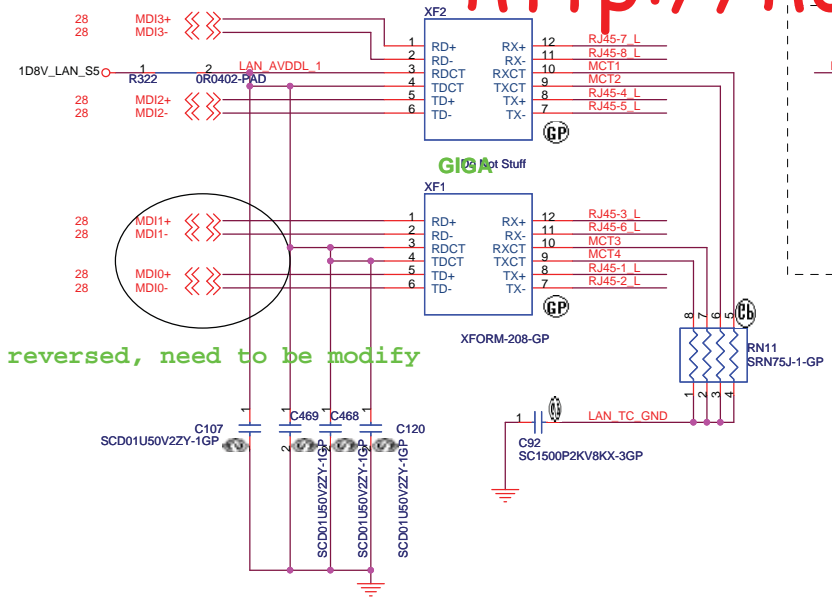
test

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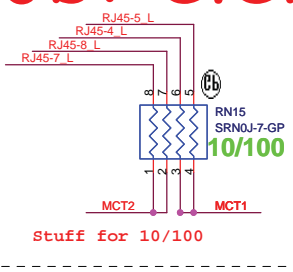
Title: **LAN MARVELL 88E1116**

Size: A3 Document Number: **TIBET** Rev: **SA**

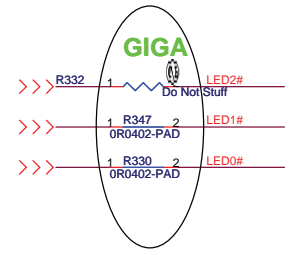
Date: Tuesday, August 14, 2007 Sheet 28 of 44



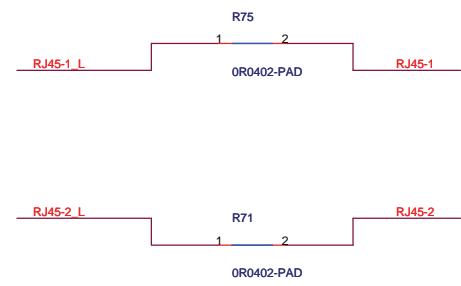
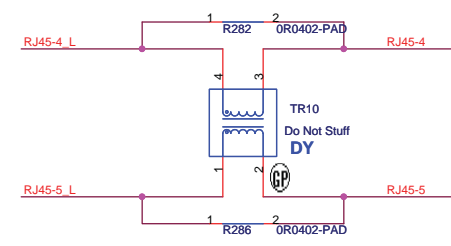
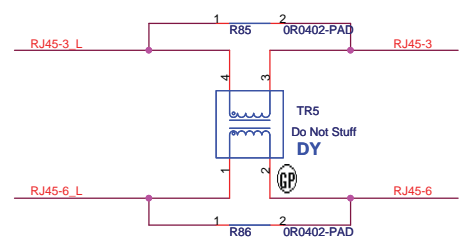
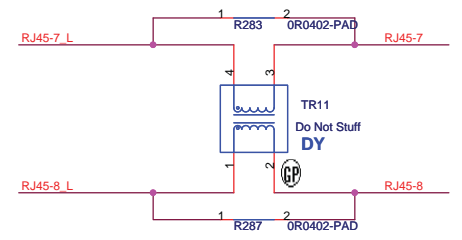
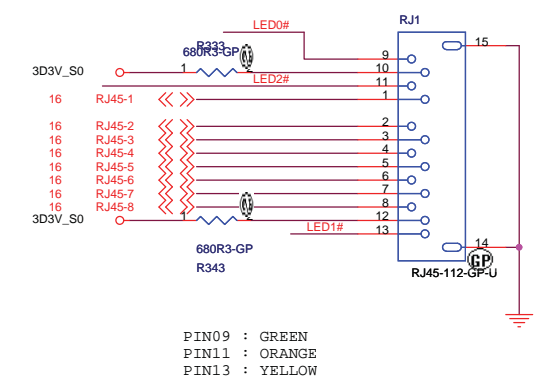
reversed, need to be modify



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



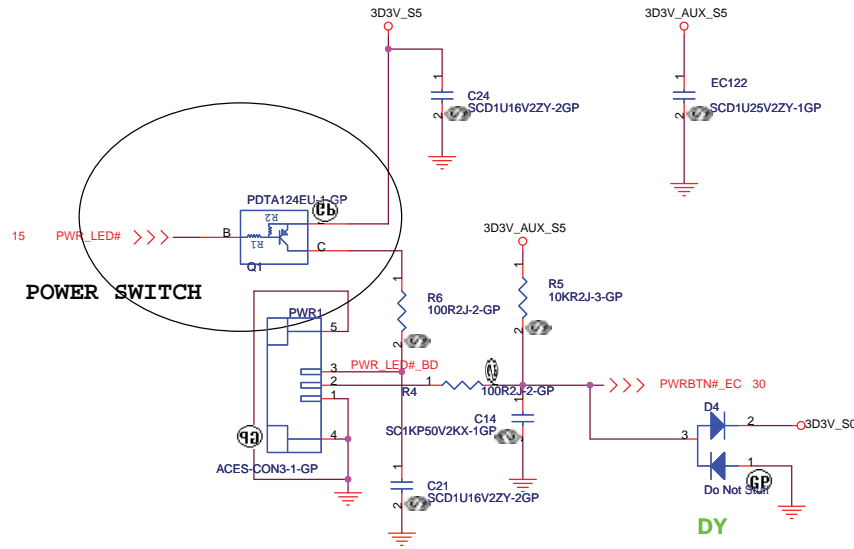
GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps



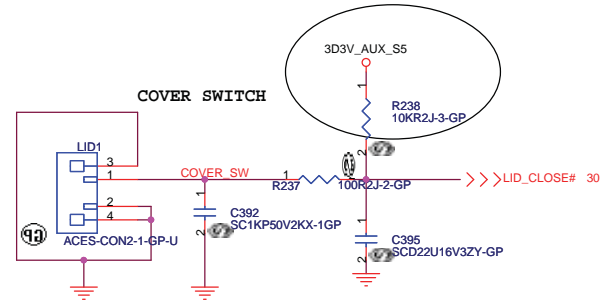
TOP VIEW

A15 (B1)
A14 (B2)
⋮
A2 (B14)
A1 (B15)

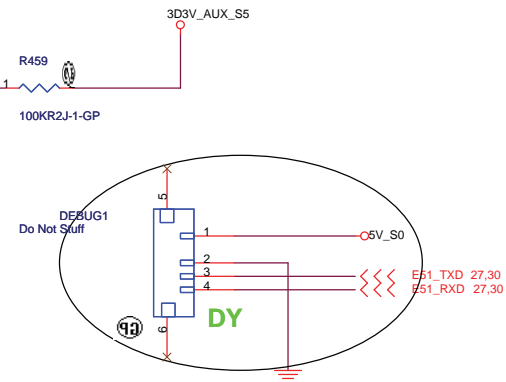
(BOTTOM VIEW)



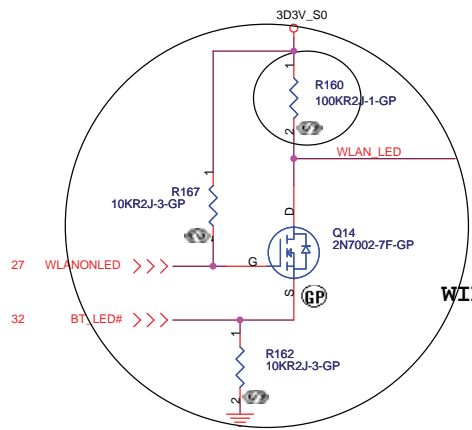
DY



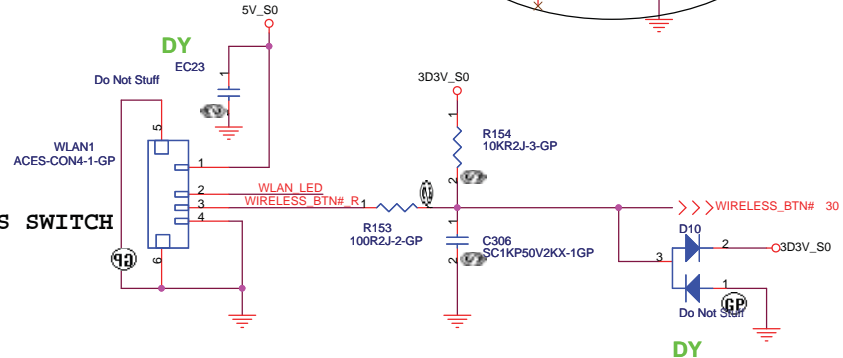
<<< LPC_LAD[0..3] 12,21,30



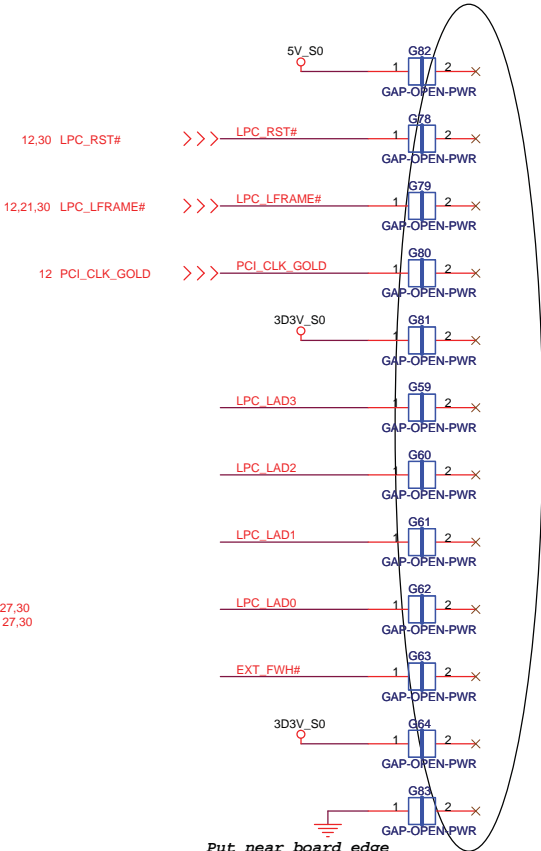
DY



DY

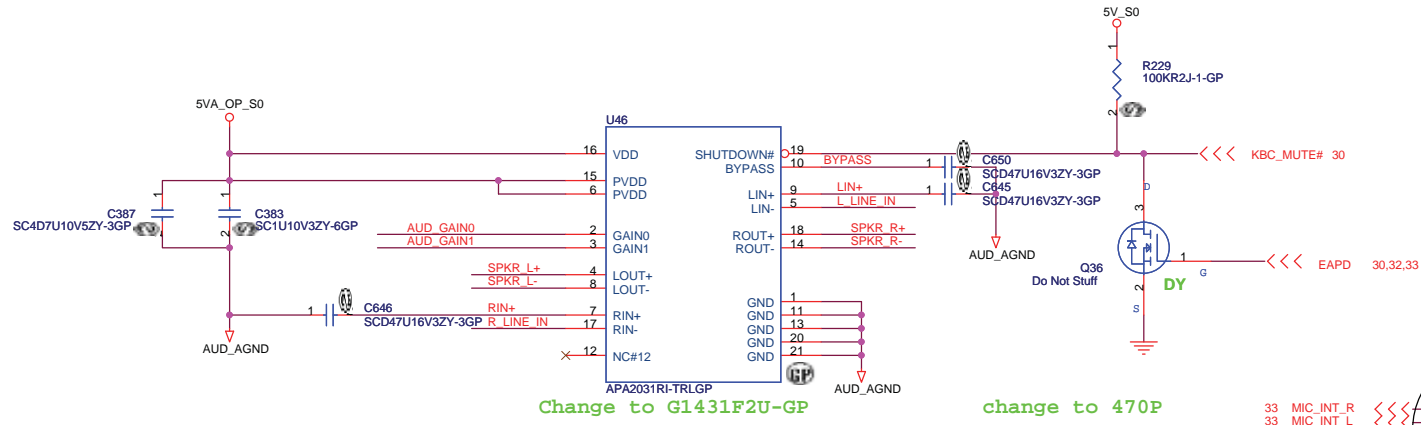
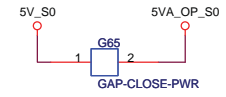


DY



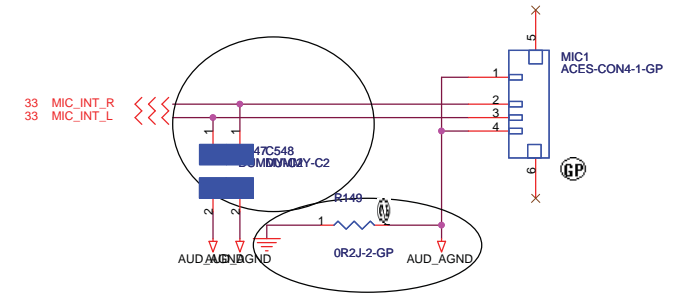
Put near board edge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
FLASH and Debug			
Size	Document Number		Rev
A3			SA
Date:	Tuesday, August 14, 2007	Sheet 31 of 44	

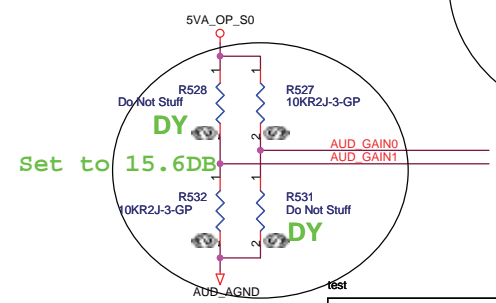
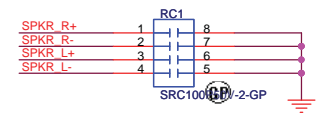
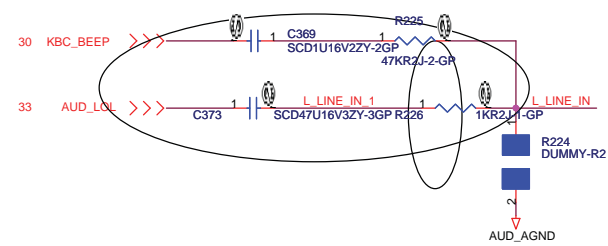
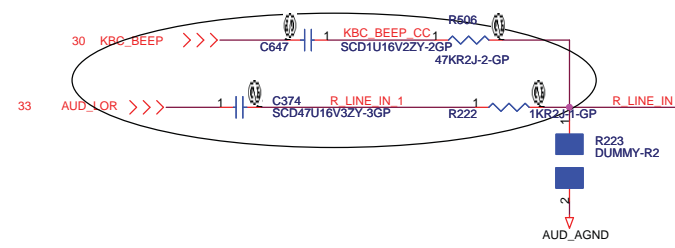


Change to G1431F2U-GP

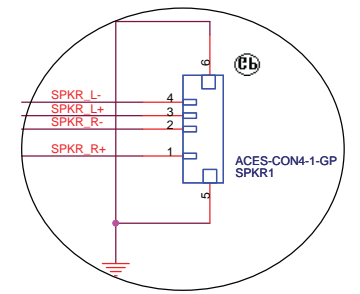
change to 470P

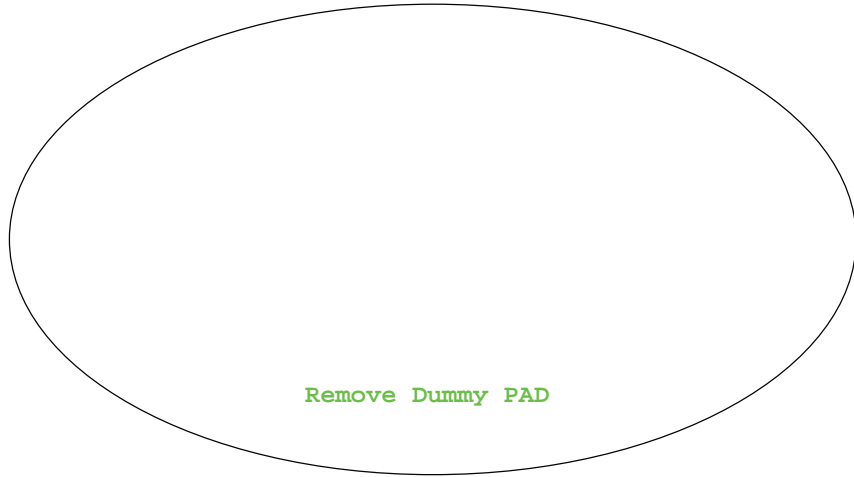


Speaker

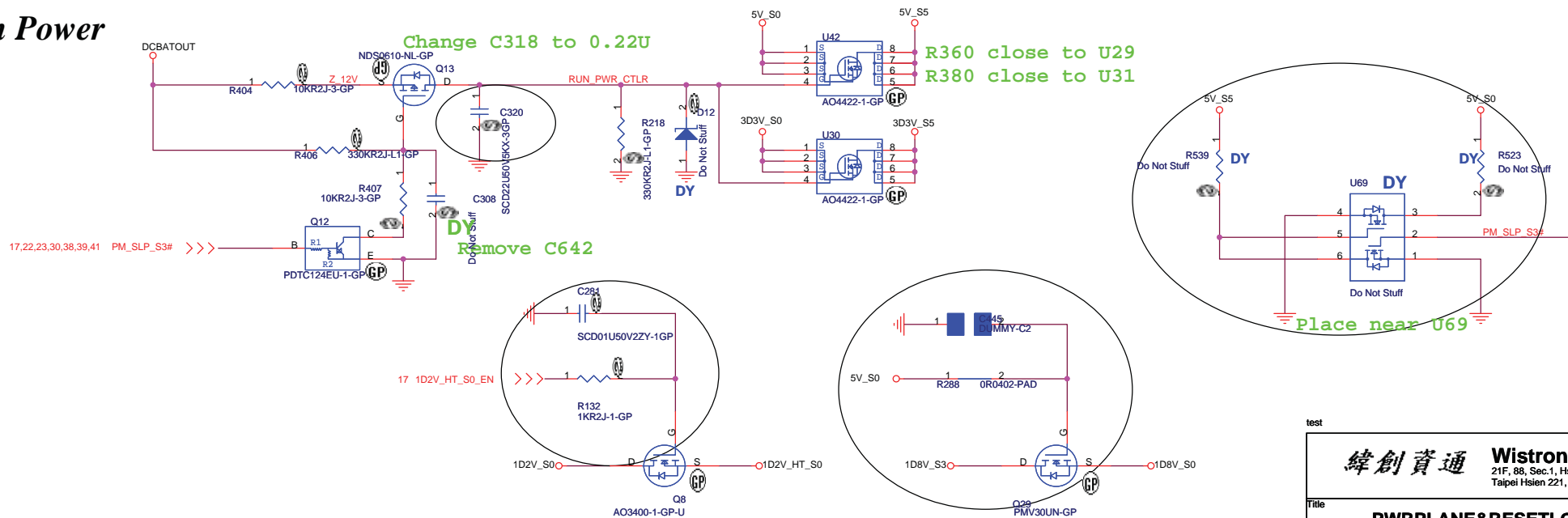


Set to 15.6DB





Run Power

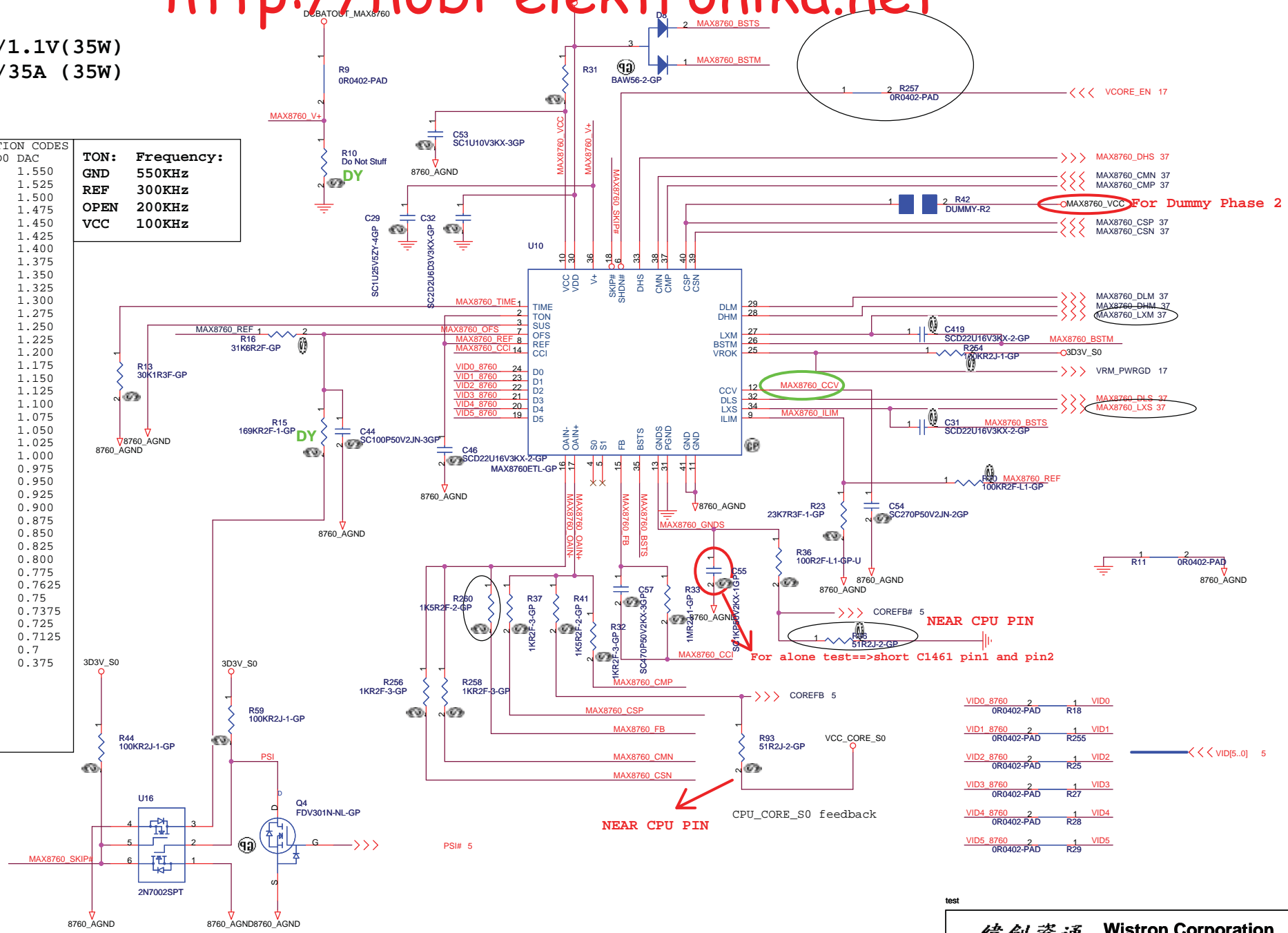


CPU_VCORE
VID=1.15V(25W)/1.1V(35W)
Iomax=25A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz



VID0 8760	2	1	VID0
OR0402-PAD		1	R18
VID1 8760	2	1	VID1
OR0402-PAD		1	R255
VID2 8760	2	1	VID2
OR0402-PAD		1	R25
VID3 8760	2	1	VID3
OR0402-PAD		1	R27
VID4 8760	2	1	VID4
OR0402-PAD		1	R28
VID5 8760	2	1	VID5
OR0402-PAD		1	R29

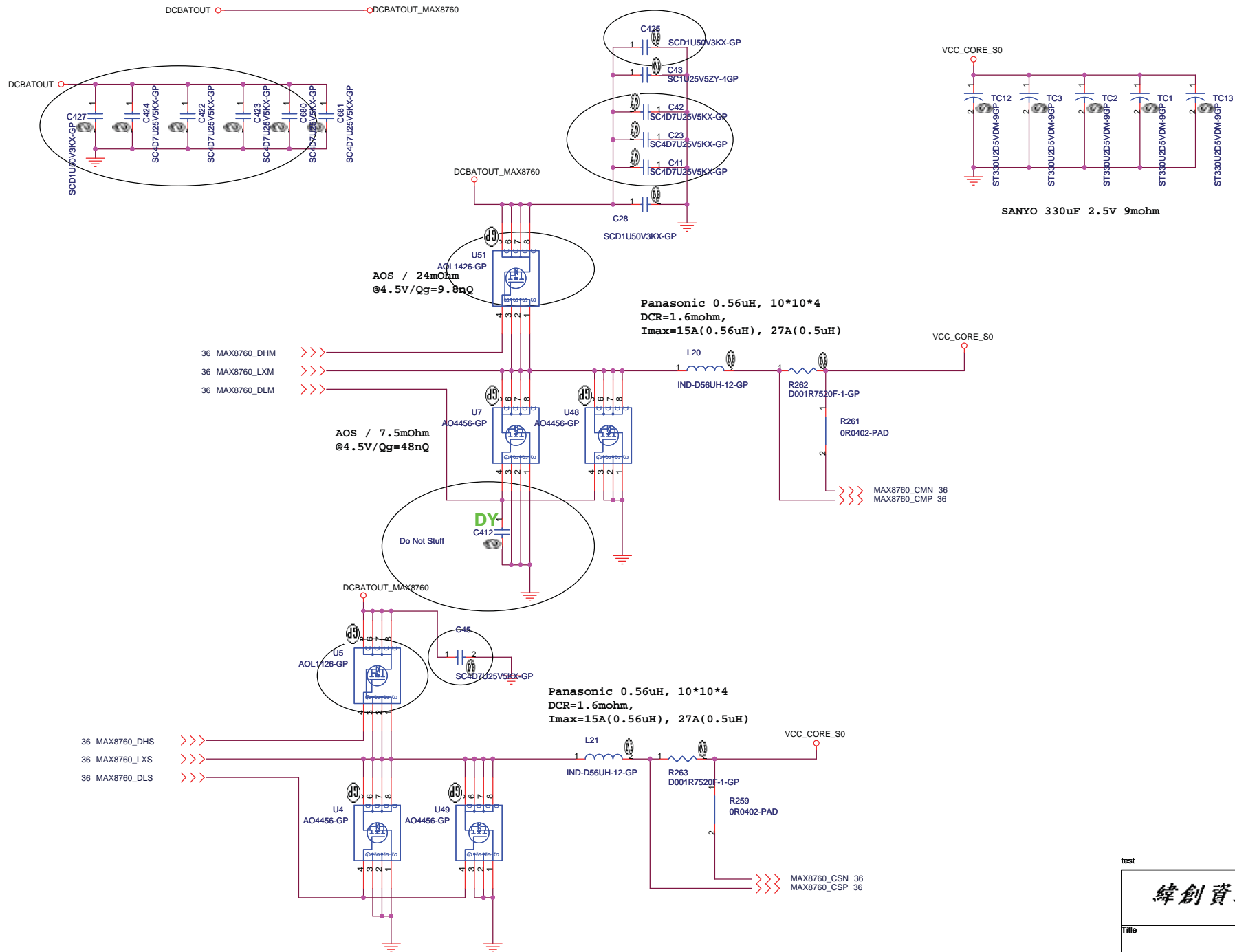
test

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Title: **CPU CORE MAX8760(1/2)**

Size A3	Document Number	Rev
	TIBET	SA

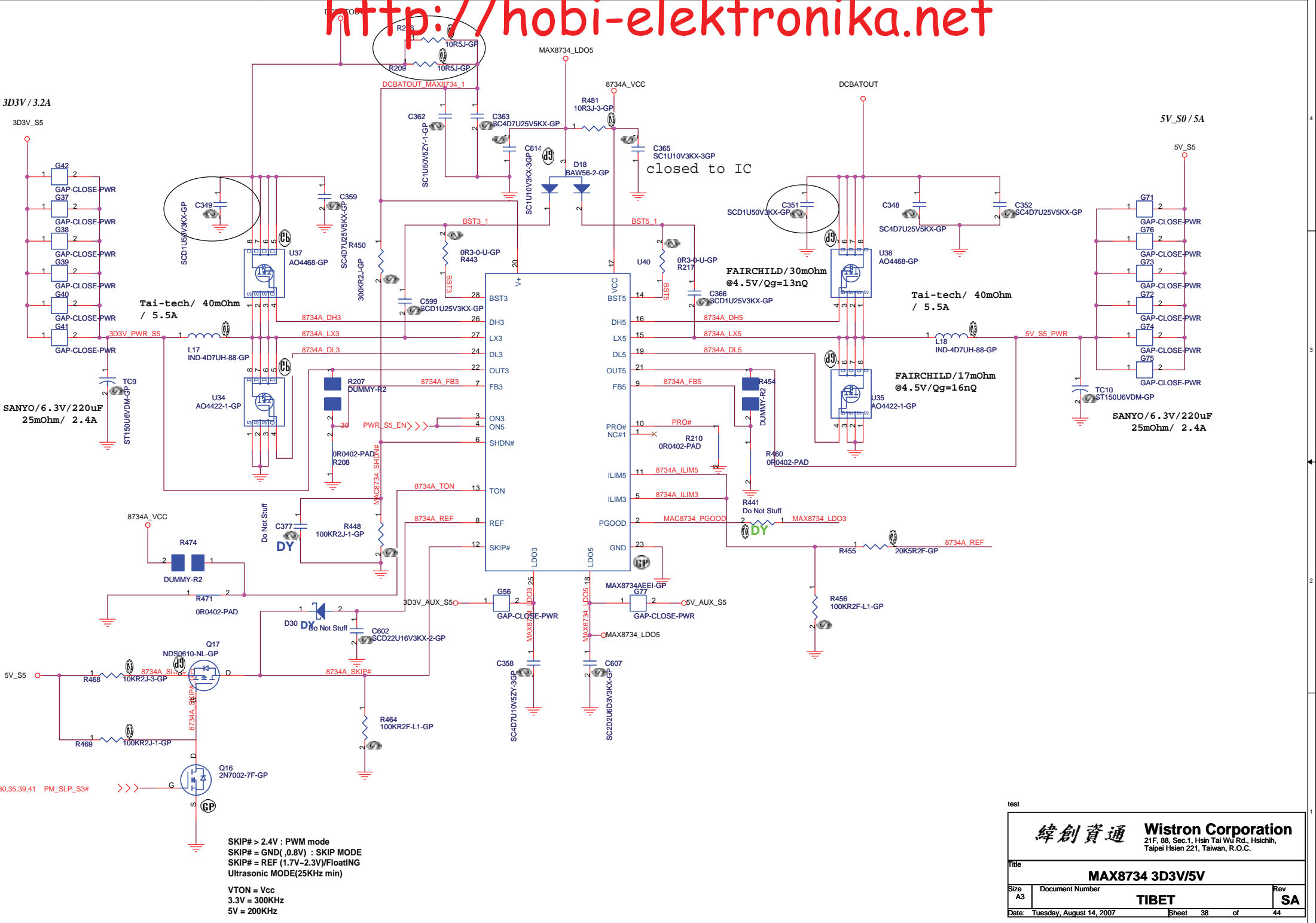
Date: Tuesday, August 14, 2007 Sheet 36 of 44



(Power Team)

test

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Title		
CPU CORE MAX8760(2/2)		
Size A3	Document Number	Rev SA
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3D3V/3.2A

5V_S0/5A

SANYO/6.3V/220uF
25mOhm/ 2.4A

SANYO/6.3V/220uF
25mOhm/ 2.4A

23,30,35,39,41 PM_SLP_S3#

SKIP# > 2.4V : PWM mode
 SKIP# = GND(,0.8V) : SKIP MODE
 SKIP# = REF (1.7V~2.3V)/FloatNG
 Ultrasonic MODE(25KHz min)
 VTON = Vcc
 3.3V = 300KHz
 5V = 200KHz

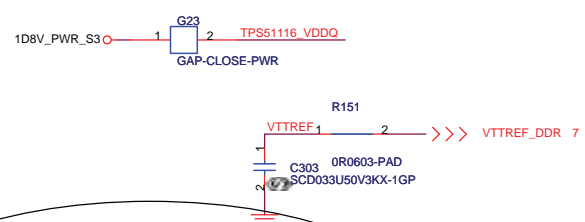
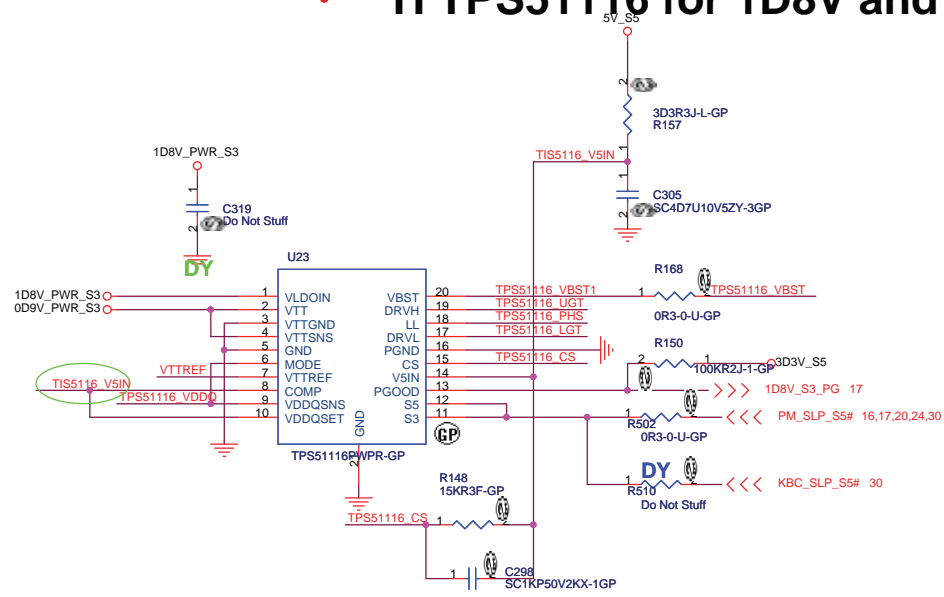
closed to IC

test

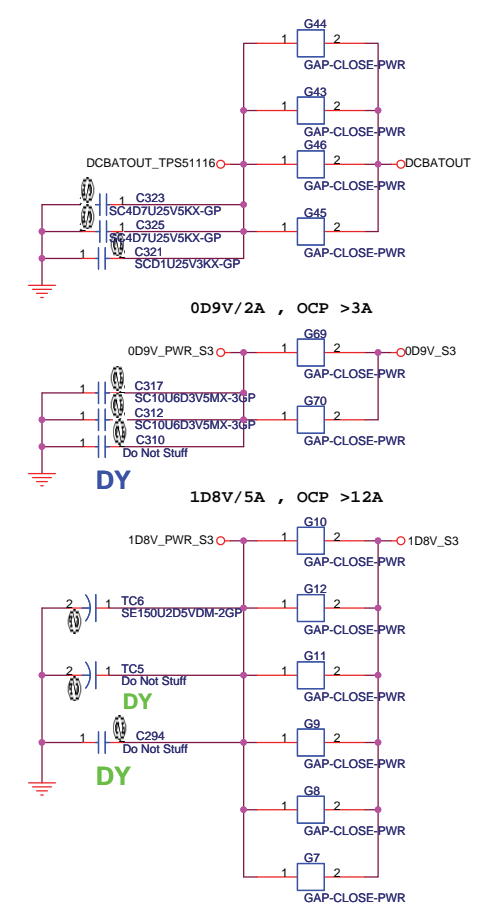
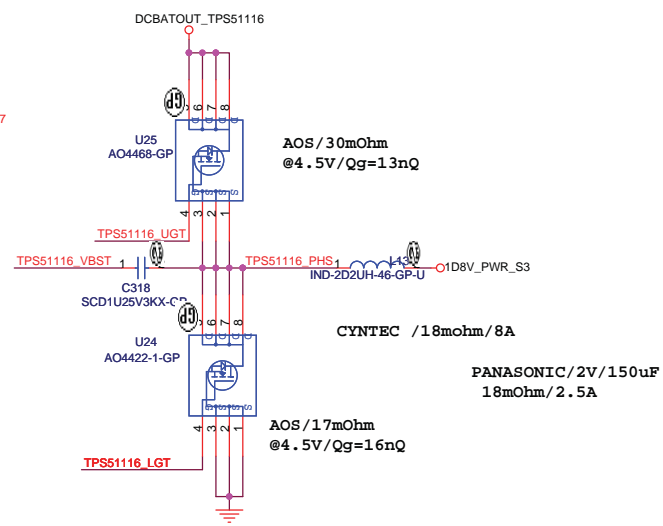
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8734 3D3V/5V**

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State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

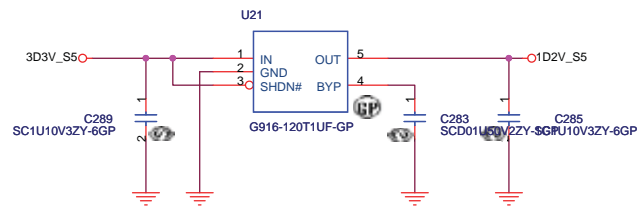
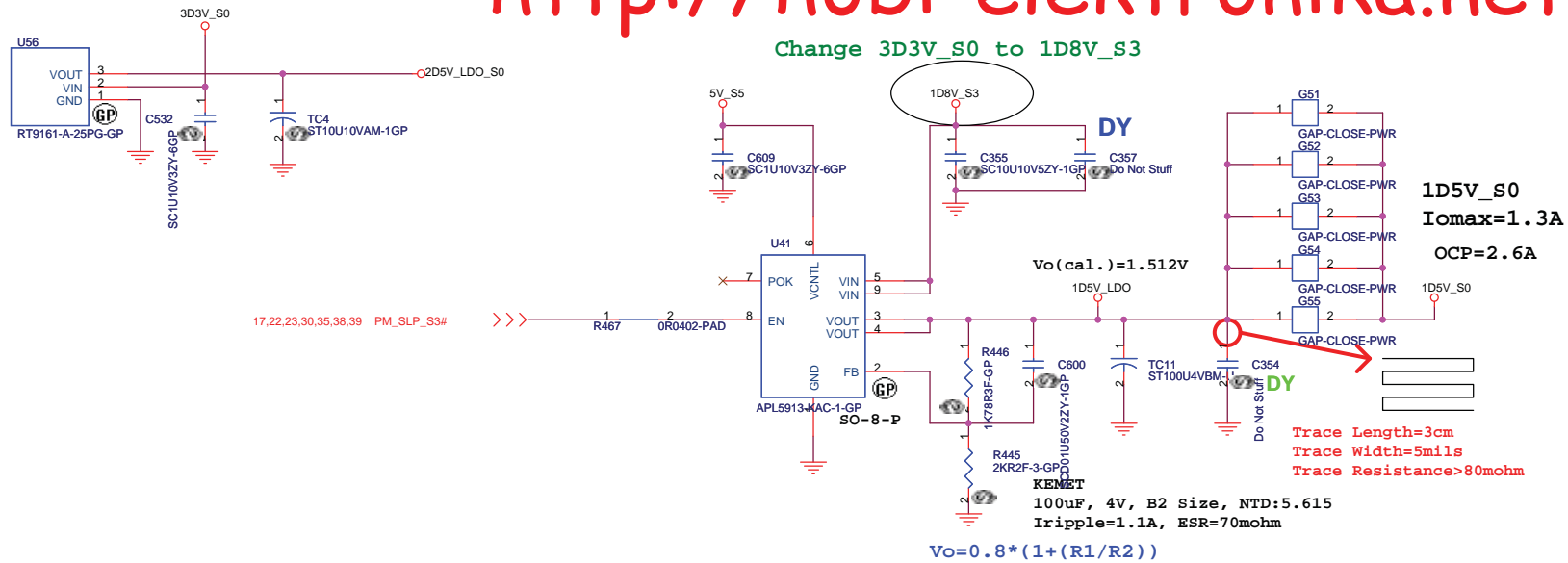


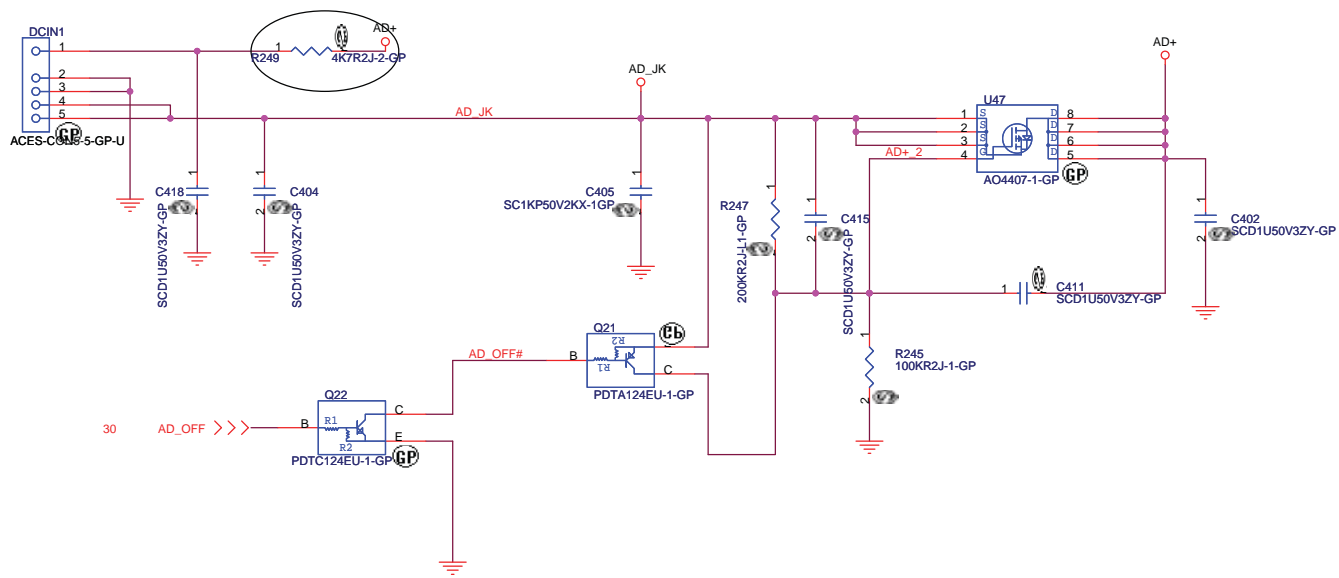
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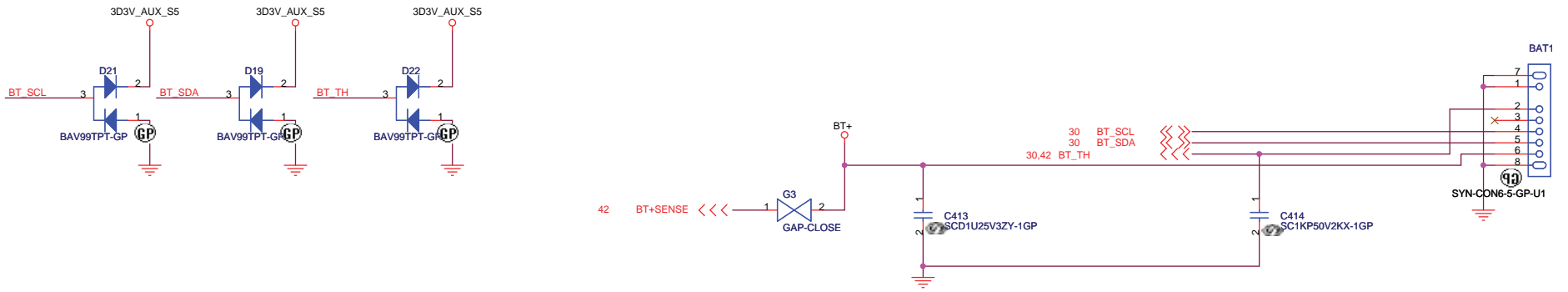
Title: **TPS51116 1D8V/0D9V**

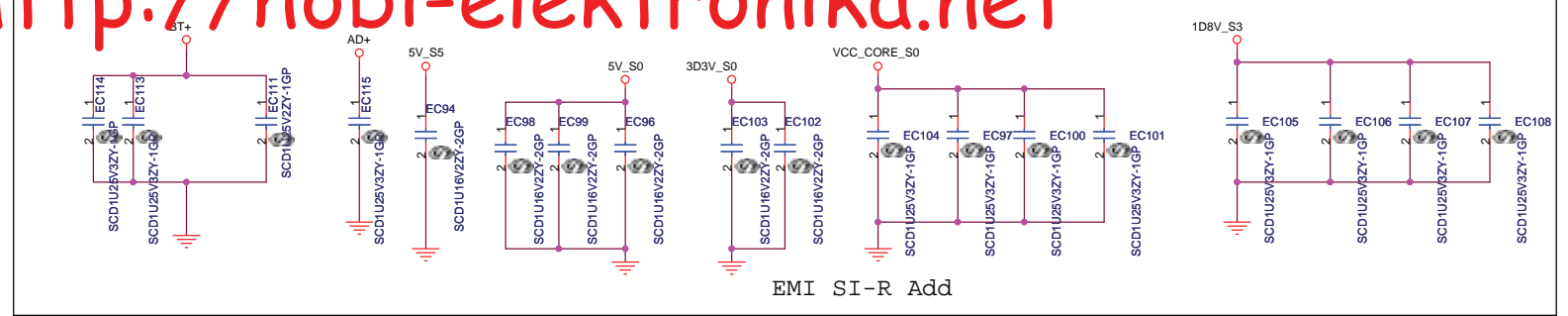
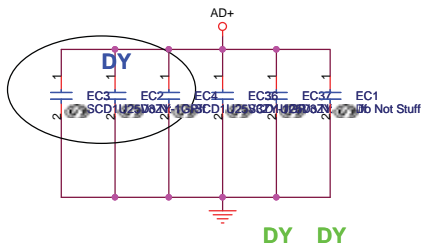
Size A3	Document Number	Rev SA
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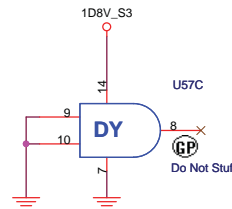
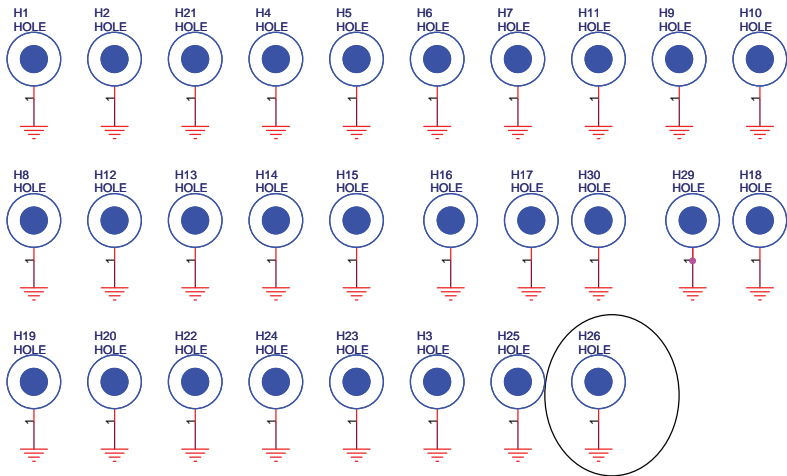
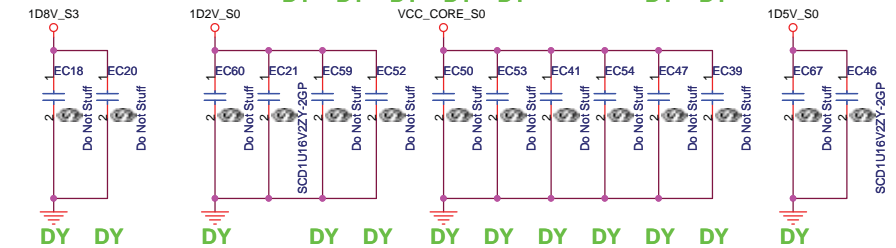
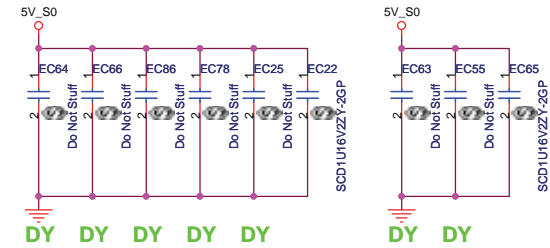
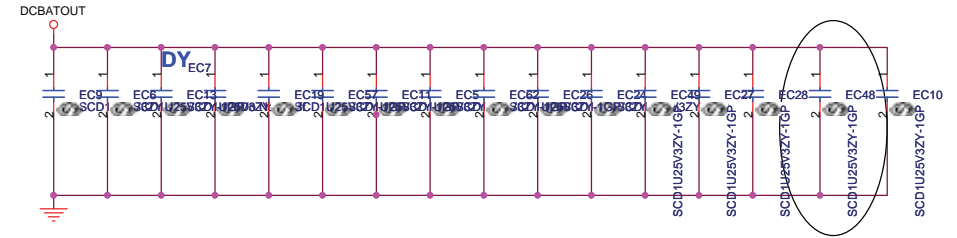
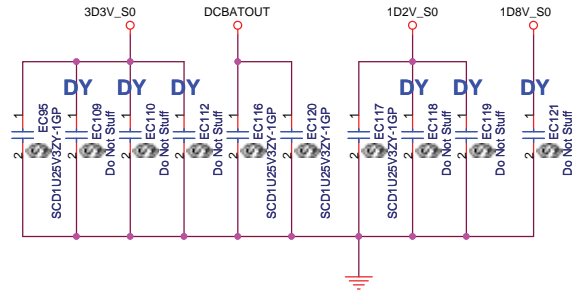


BATTERY CONNECTOR

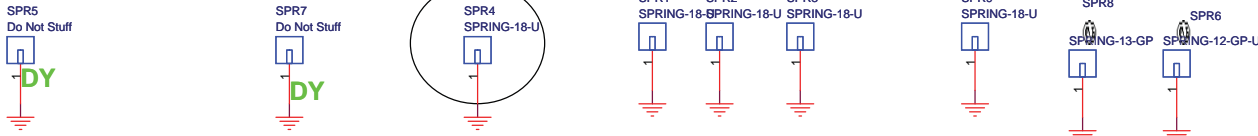




	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



Modify SPR7 P/N manually



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND

test

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size A3 Document Number: **TIBET** Rev SA

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