

# Compal confidential

## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-08-02

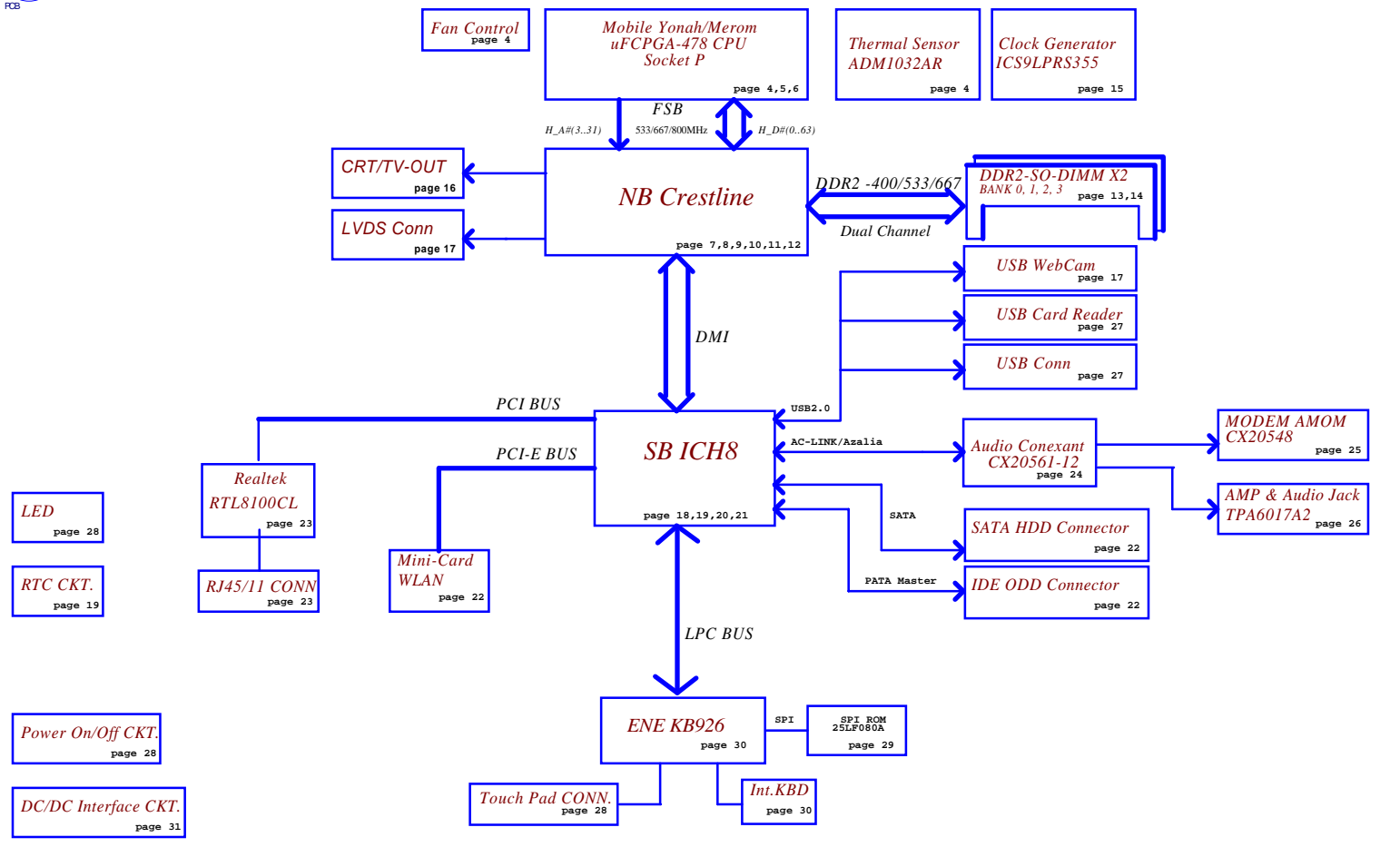
REV: 0.2

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# LEON 1.0 (Merom +Crestline+ICH8)



PCB



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## Block Diagram

### Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

### External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

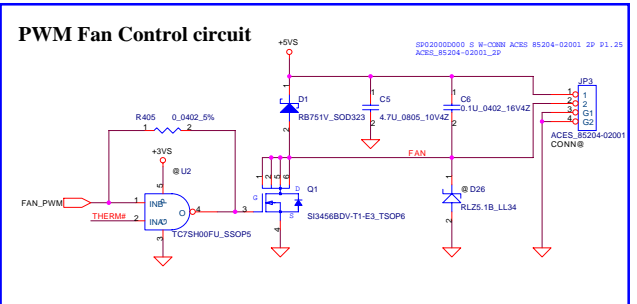
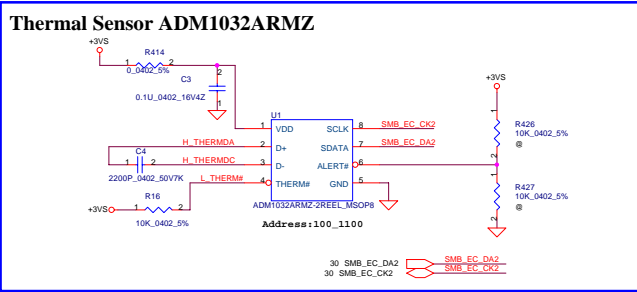
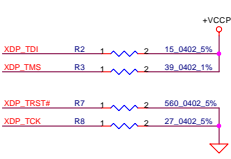
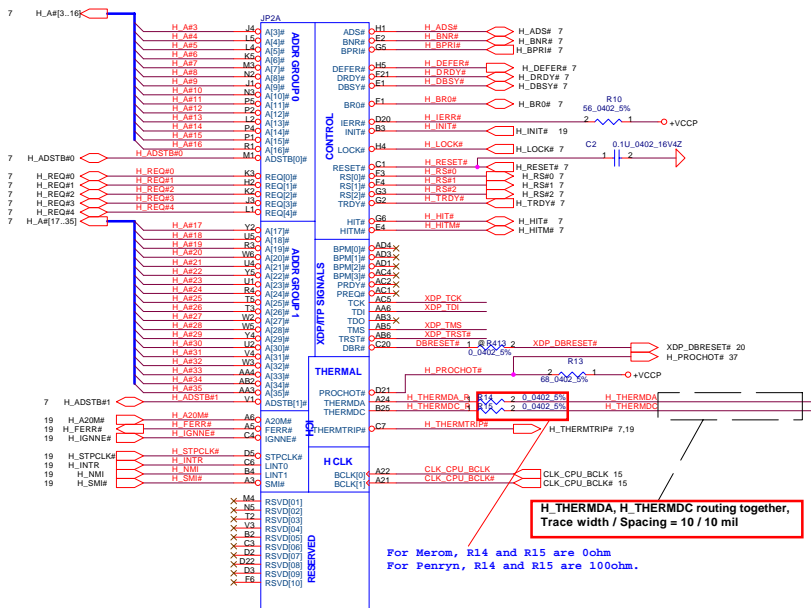
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43151732L01(965GM) & 443151732L02(960GML) with card reader

BOM: 43151732L03(965GM) & 43151732L04(960GML) without card reader

Jump-Short: PJP?

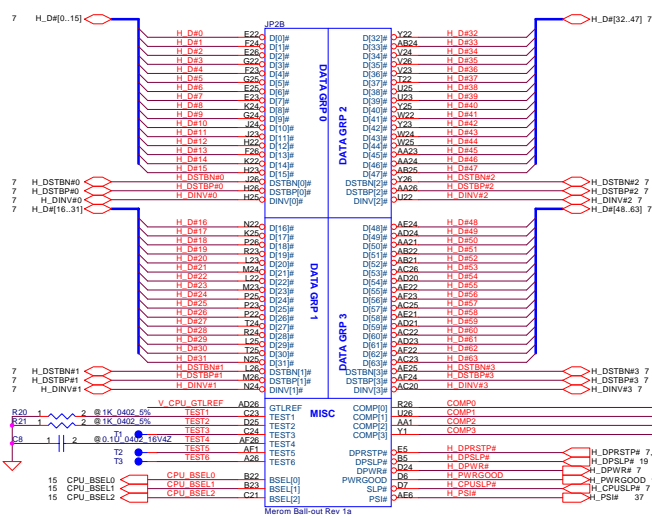
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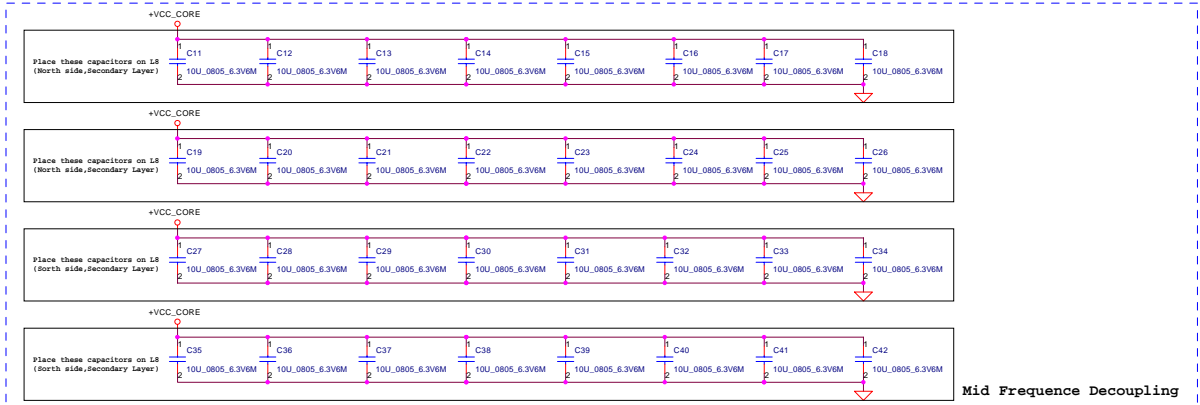
**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm  
 For Penryn, R14 and R15 are 100ohm.

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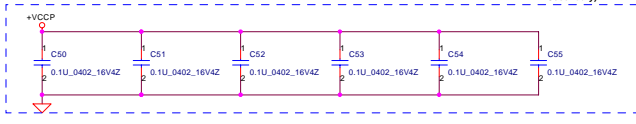
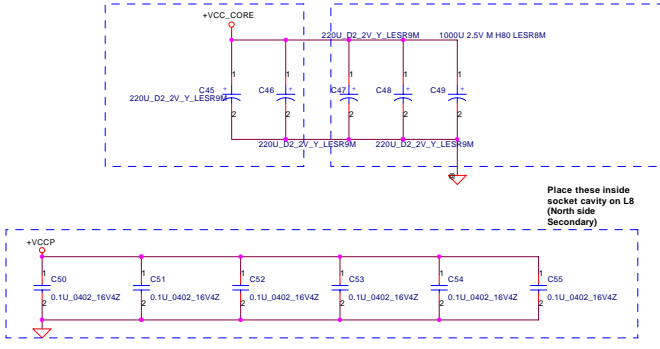


JP2D			
A4	VSS1001	VSS1080	P8
A5	VSS1002	VSS1081	P21
A11	VSS1003	VSS1082	P22
A14	VSS1004	VSS1083	R2
A16	VSS1005	VSS1084	R22
A19	VSS1006	VSS1085	R22
A22	VSS1007	VSS1086	T1
AF2	VSS1008	VSS1087	T1
B6	VSS1009	VSS1088	T4
B8	VSS1010	VSS1089	T7
B11	VSS1011	VSS1090	T26
B13	VSS1012	VSS1091	T27
B16	VSS1013	VSS1092	U6
B19	VSS1014	VSS1093	U6
B21	VSS1015	VSS1094	U24
C2	VSS1016	VSS1095	U5
C4	VSS1017	VSS1096	U2
C8	VSS1018	VSS1097	U22
C9	VSS1019	VSS1098	U25
C14	VSS1020	VSS1099	W1
C16	VSS1021	VSS1100	W4
C19	VSS1022	VSS1101	W22
C2	VSS1023	VSS1102	W22
C22	VSS1024	VSS1103	X3
C25	VSS1025	VSS1104	X6
D1	VSS1026	VSS1105	X2
D4	VSS1027	VSS1106	X24
D8	VSS1028	VSS1107	X24
D11	VSS1029	VSS1108	Y2
D13	VSS1030	VSS1109	Y2
D16	VSS1031	VSS1110	AA8
D18	VSS1032	VSS1111	AA11
D19	VSS1033	VSS1112	AA14
D23	VSS1034	VSS1113	AA16
D28	VSS1035	VSS1114	AA19
E3	VSS1036	VSS1115	AA22
E6	VSS1037	VSS1116	AA25
E8	VSS1038	VSS1117	AB1
E9	VSS1039	VSS1118	AB4
E11	VSS1040	VSS1119	AB6
E16	VSS1041	VSS1120	AB11
E19	VSS1042	VSS1121	AB13
E21	VSS1043	VSS1122	AB16
E24	VSS1044	VSS1123	AB19
F4	VSS1045	VSS1124	AB26
F8	VSS1046	VSS1125	AB26
F11	VSS1047	VSS1126	AC2
F16	VSS1048	VSS1127	AC6
F19	VSS1049	VSS1128	AC11
F22	VSS1050	VSS1129	AC14
F24	VSS1051	VSS1130	AC16
F25	VSS1052	VSS1131	AC19
G4	VSS1053	VSS1132	AC21
G1	VSS1054	VSS1133	AC24
G3	VSS1055	VSS1134	AD2
G8	VSS1056	VSS1135	AD5
H4	VSS1057	VSS1136	AD8
H6	VSS1058	VSS1137	AD11
H21	VSS1059	VSS1138	AD13
H24	VSS1060	VSS1139	AD16
J2	VSS1061	VSS1140	AD19
J6	VSS1062	VSS1141	AD22
J22	VSS1063	VSS1142	AD25
K5	VSS1064	VSS1143	AE1
K1	VSS1065	VSS1144	AE4
K4	VSS1066	VSS1145	AE8
K23	VSS1067	VSS1146	AE11
K28	VSS1068	VSS1147	AE14
L3	VSS1069	VSS1148	AE16
L6	VSS1070	VSS1149	AE19
L21	VSS1071	VSS1150	AE23
L24	VSS1072	VSS1151	AE26
M2	VSS1073	VSS1152	AF
M5	VSS1074	VSS1153	AF
M22	VSS1075	VSS1154	AF8
M28	VSS1076	VSS1155	AF11
N1	VSS1077	VSS1156	AF13
N4	VSS1078	VSS1157	AF16
N23	VSS1079	VSS1158	AF19
N28	VSS1080	VSS1159	AF21
P1	VSS1081	VSS1160	AZ2
			AZ5
			AZ25

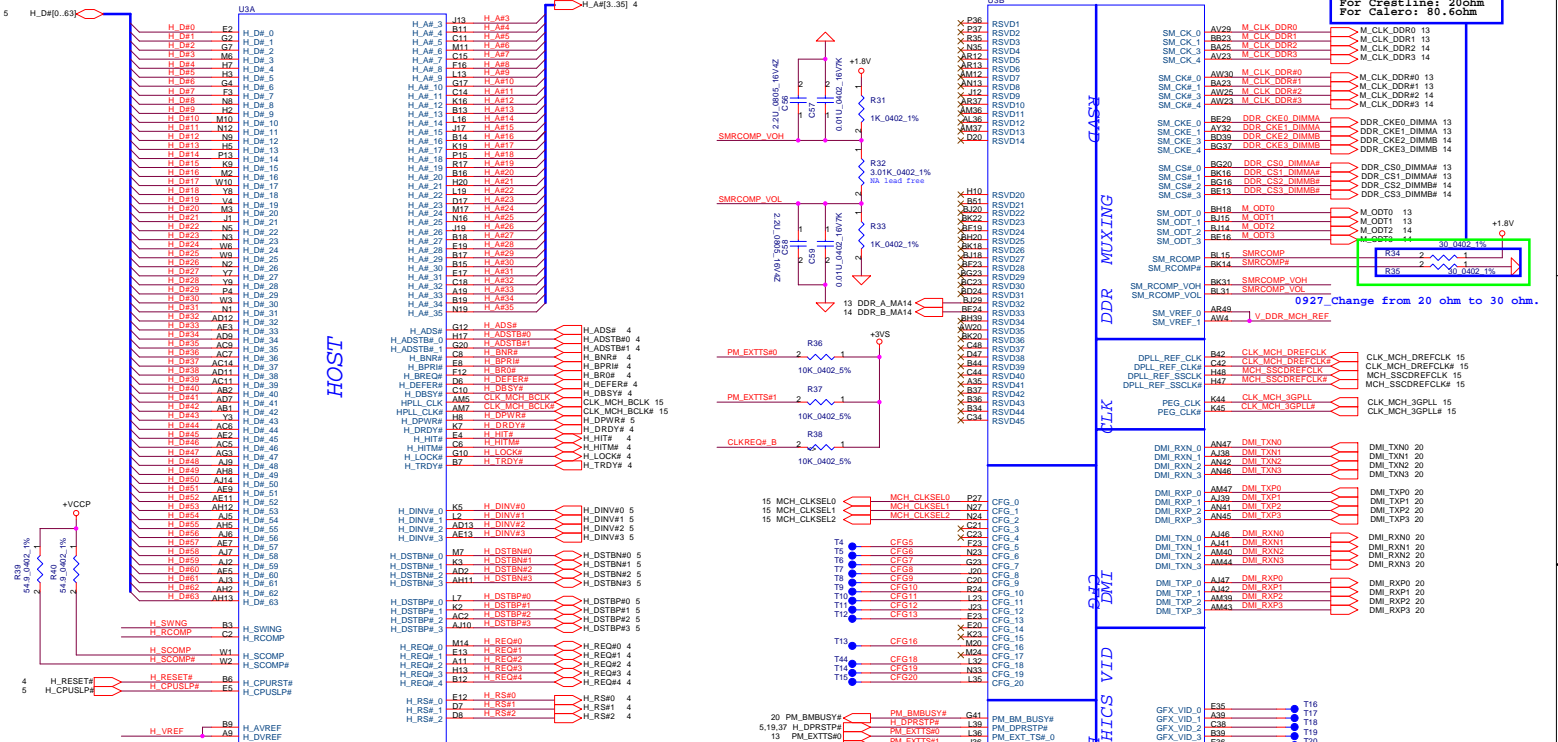


Mid Frequency Decoupling

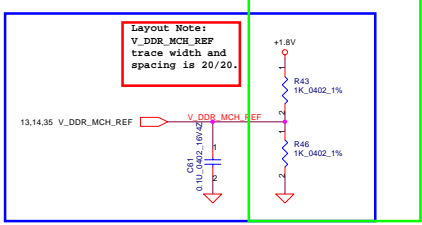
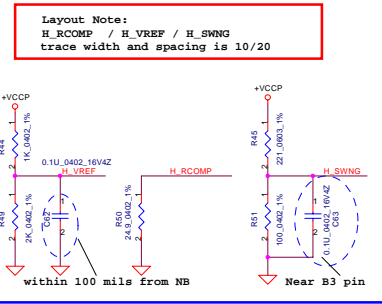
Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



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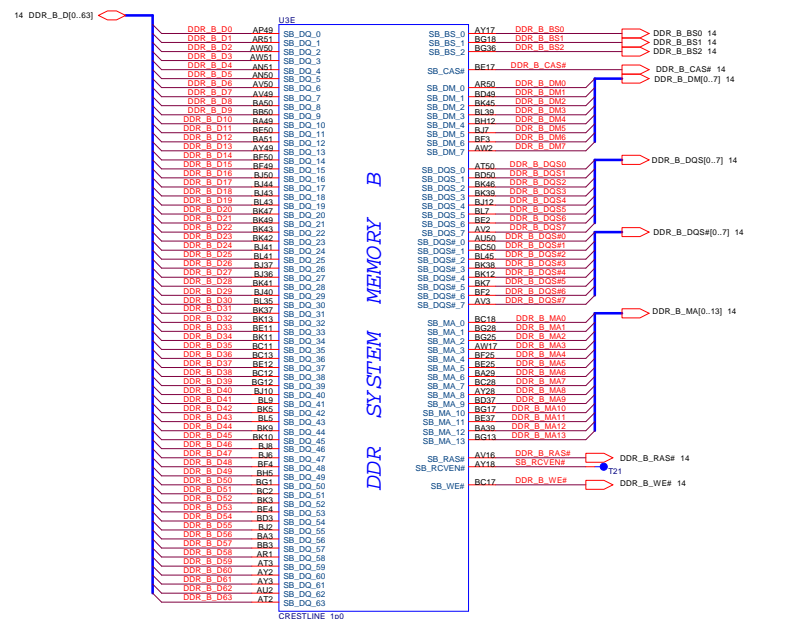
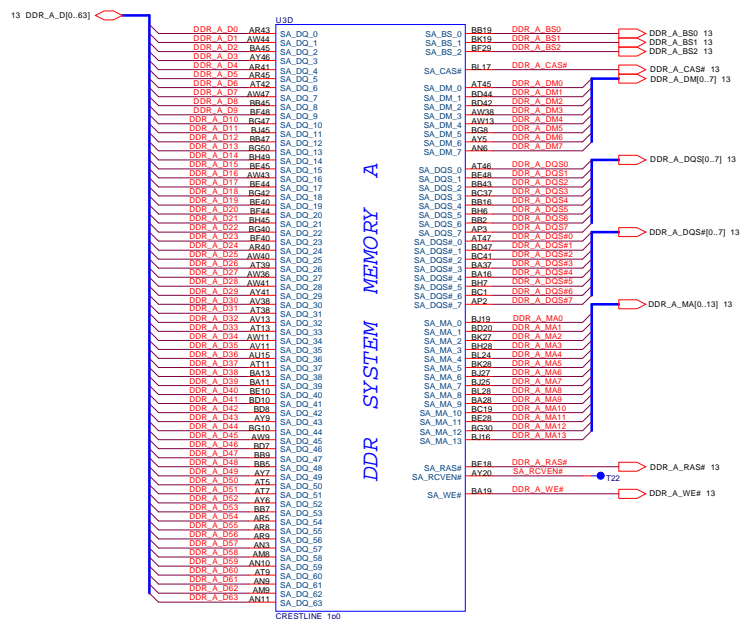
**layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as #8 data traces



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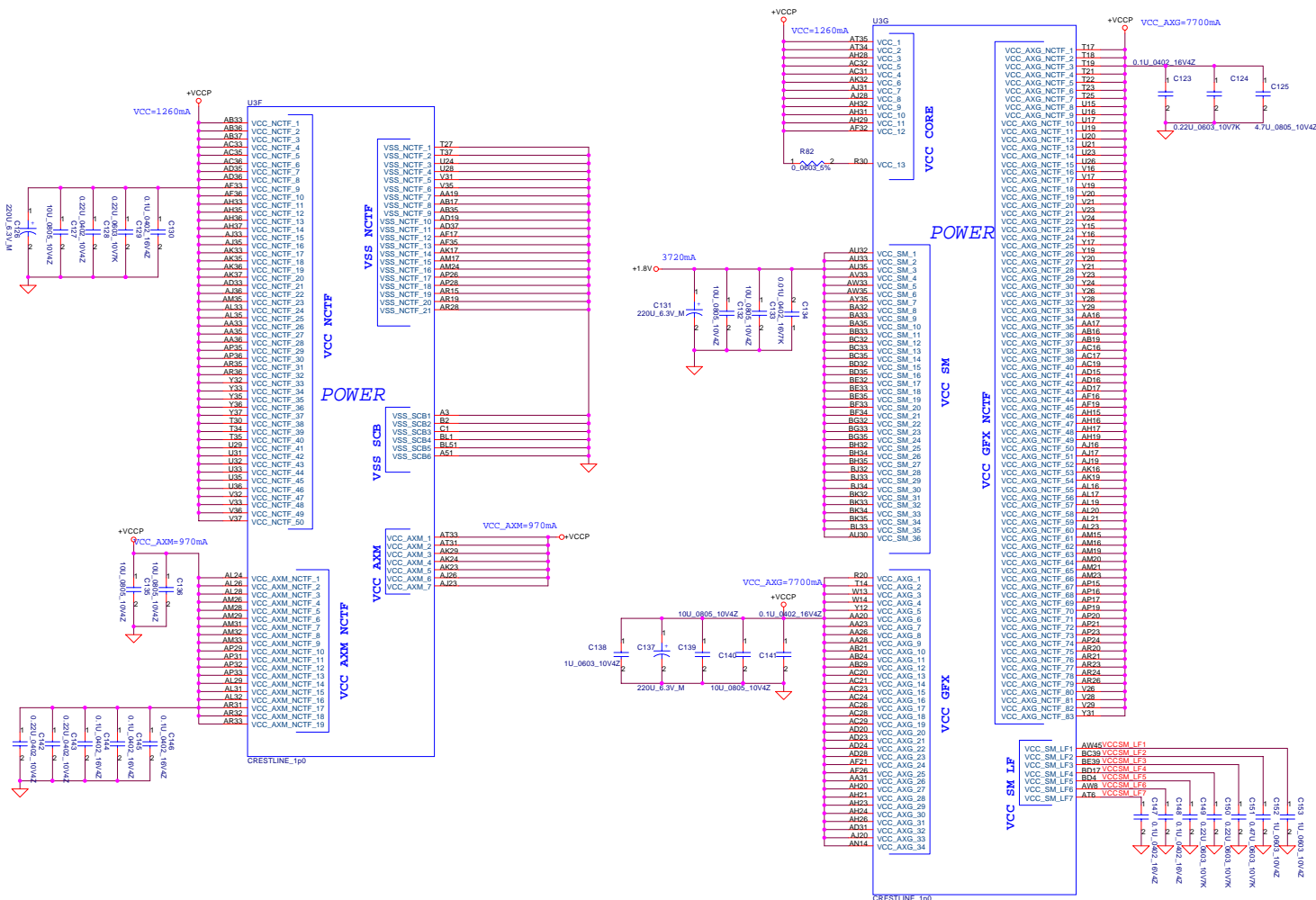
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U31

A13	VSS_1	AW24
A15	VSS_2	AW23
A17	VSS_3	AW22
A2	VSS_4	AW21
AA21	VSS_5	AW20
AA24	VSS_6	AW19
AA25	VSS_7	AW18
AB20	VSS_8	AW17
AB23	VSS_9	AW16
AB26	VSS_10	AW15
AB28	VSS_11	AW14
AB31	VSS_12	AW13
AC10	VSS_13	AW12
AC13	VSS_14	AW11
AC1	VSS_15	AW10
AC2	VSS_16	AW9
AC43	VSS_17	AW8
AD1	VSS_18	AW7
AD11	VSS_19	AW6
AD26	VSS_20	AW5
AD29	VSS_21	AW4
AD3	VSS_22	AW3
AD41	VSS_23	AW2
AD49	VSS_24	AW1
AD5	VSS_25	
AD5	VSS_26	
AD50	VSS_27	
AE10	VSS_28	
AE14	VSS_29	
AE1	VSS_30	
AE1	VSS_31	
AE1	VSS_32	
AF23	VSS_33	
AF24	VSS_34	
AF24	VSS_35	
AF31	VSS_36	
AG2	VSS_37	
AG38	VSS_38	
AG43	VSS_39	
AG47	VSS_40	
AH3	VSS_41	
AH9	VSS_42	
AH41	VSS_43	
AH7	VSS_44	
AI9	VSS_45	
AI11	VSS_46	
AI13	VSS_47	
AI21	VSS_48	
AI24	VSS_49	
AJ23	VSS_50	
AJ32	VSS_51	
AJ32	VSS_52	
AJ45	VSS_53	
AJ45	VSS_54	
AJ45	VSS_55	
AK20	VSS_56	
AK21	VSS_57	
AK28	VSS_58	
AK28	VSS_59	
AK31	VSS_60	
AK51	VSS_61	
AL1	VSS_62	
AM11	VSS_63	
AM13	VSS_64	
AM3	VSS_65	
AM4	VSS_66	
AM41	VSS_67	
AN1	VSS_68	
AN38	VSS_69	
AN38	VSS_70	
AN38	VSS_71	
AN43	VSS_72	
AN7	VSS_73	
AN7	VSS_74	
AP48	VSS_75	
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AP50	VSS_77	
AR1	VSS_78	
AR2	VSS_79	
AR2	VSS_80	
AR44	VSS_81	
AR7	VSS_82	
AR7	VSS_83	
AT10	VSS_84	
AT14	VSS_85	
AT41	VSS_86	
AT66	VSS_87	
AU1	VSS_88	
AU23	VSS_89	
AU23	VSS_90	
AU36	VSS_91	
AU36	VSS_92	
AU49	VSS_93	
AU51	VSS_94	
AV38	VSS_95	
AV48	VSS_96	
AW1	VSS_97	
AW12	VSS_98	
AW16	VSS_99	

VSS

CRESTLINE\_1p0

J31

C46	VSS_199	W11
C50	VSS_200	W39
C7	VSS_201	W43
D13	VSS_202	W47
D24	VSS_203	W5
D3	VSS_204	W7
D32	VSS_205	W13
D39	VSS_206	W2
D45	VSS_207	W41
E10	VSS_208	W46
E10	VSS_209	W49
E14	VSS_210	W5
E24	VSS_211	W50
E28	VSS_212	W51
E47	VSS_213	W52
F19	VSS_214	W53
F36	VSS_215	W54
F4	VSS_216	W55
F40	VSS_217	W56
F50	VSS_218	W57
G1	VSS_219	W58
G13	VSS_220	W59
G16	VSS_221	W60
G19	VSS_222	W61
G24	VSS_223	W62
G28	VSS_224	W63
G30	VSS_225	W64
G42	VSS_226	W65
G46	VSS_227	W66
G48	VSS_228	W67
G8	VSS_229	W68
G8	VSS_230	W69
H24	VSS_231	W70
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H4	VSS_234	W73
H45	VSS_235	W74
J11	VSS_236	W75
J16	VSS_237	W76
J2	VSS_238	W77
J24	VSS_239	W78
J33	VSS_240	W79
J36	VSS_241	W80
J39	VSS_242	W81
J43	VSS_243	W82
K12	VSS_245	W83
K47	VSS_246	W84
L1	VSS_247	W85
L17	VSS_248	W86
L20	VSS_249	W87
L24	VSS_250	W88
L28	VSS_251	W89
L3	VSS_252	W90
L33	VSS_253	W91
L48	VSS_254	W92
M08	VSS_255	W93
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M5	VSS_260	W98
M50	VSS_261	W99
M9	VSS_262	W100
N14	VSS_263	W101
N17	VSS_264	W102
N26	VSS_265	W103
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N44	VSS_269	W107
N49	VSS_270	W108
N7	VSS_271	W109
P13	VSS_272	W110
P2	VSS_273	W111
P23	VSS_274	W112
P3	VSS_275	W113
P30	VSS_276	W114
P49	VSS_277	W115
P59	VSS_278	W116
P79	VSS_279	W117
P87	VSS_280	W118
P87	VSS_281	W119
P92	VSS_282	W120
P95	VSS_283	W121
P95	VSS_284	W122
V2	VSS_285	W123
V3	VSS_286	W124

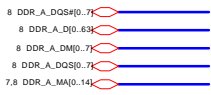
VSS

CRESTLINE\_1p0

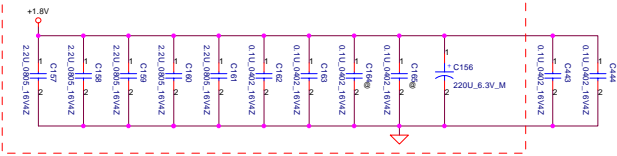
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**CRESTLINE((6/6)-PWR/GND**

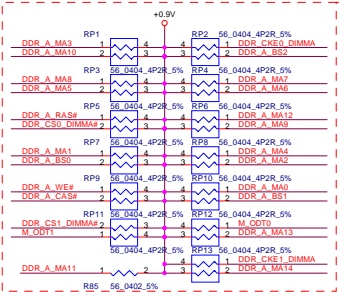
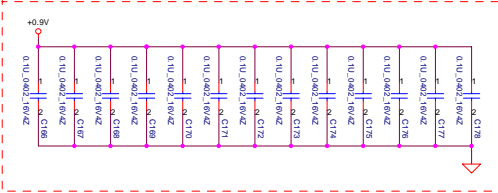
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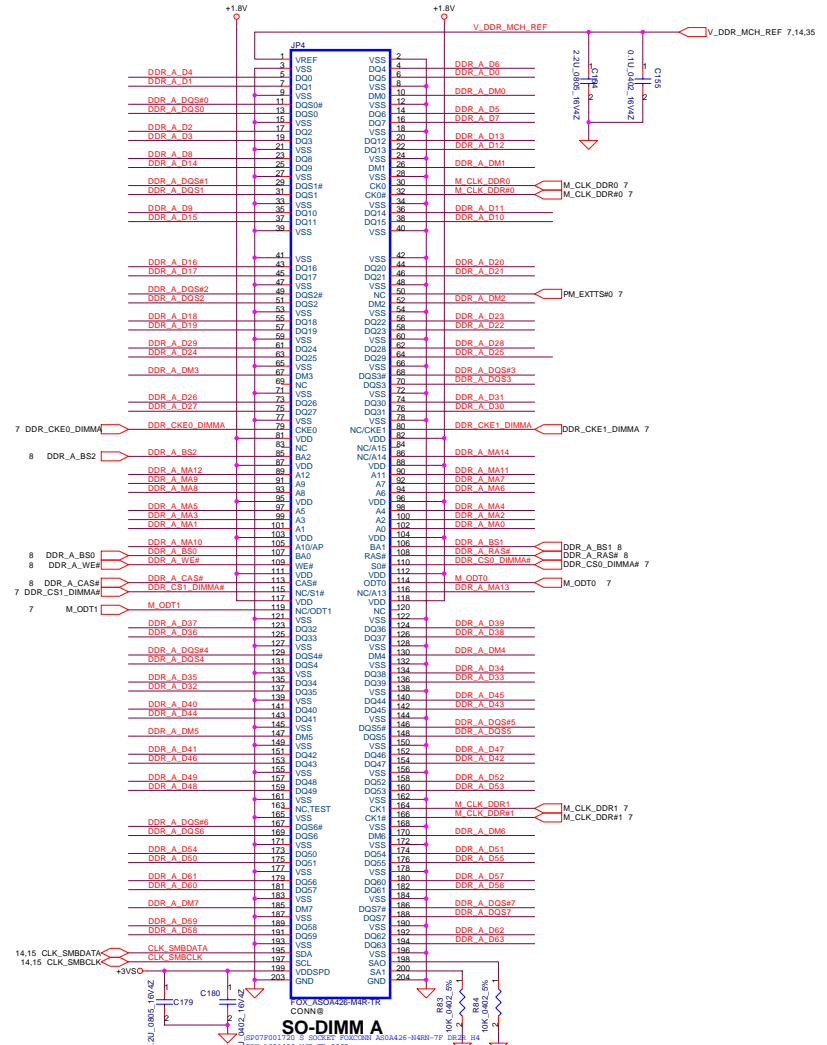
Layout Note:  
Place near JP34



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

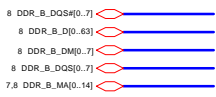


Layout Note:  
Place these resistor closely JP34, all trace length Max=1.5"

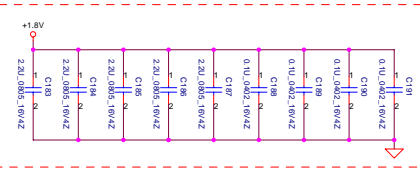


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Customer	LA-3901P	Size	Document Number
Date	Monday, October 22, 2007	Sheet	13 of 42

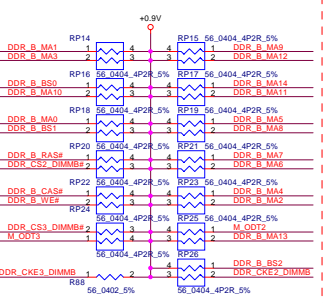
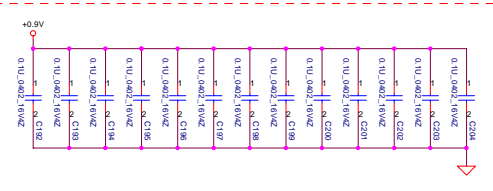
Compal Electronics, Inc.  
DDRII-SODIMM SLOT1



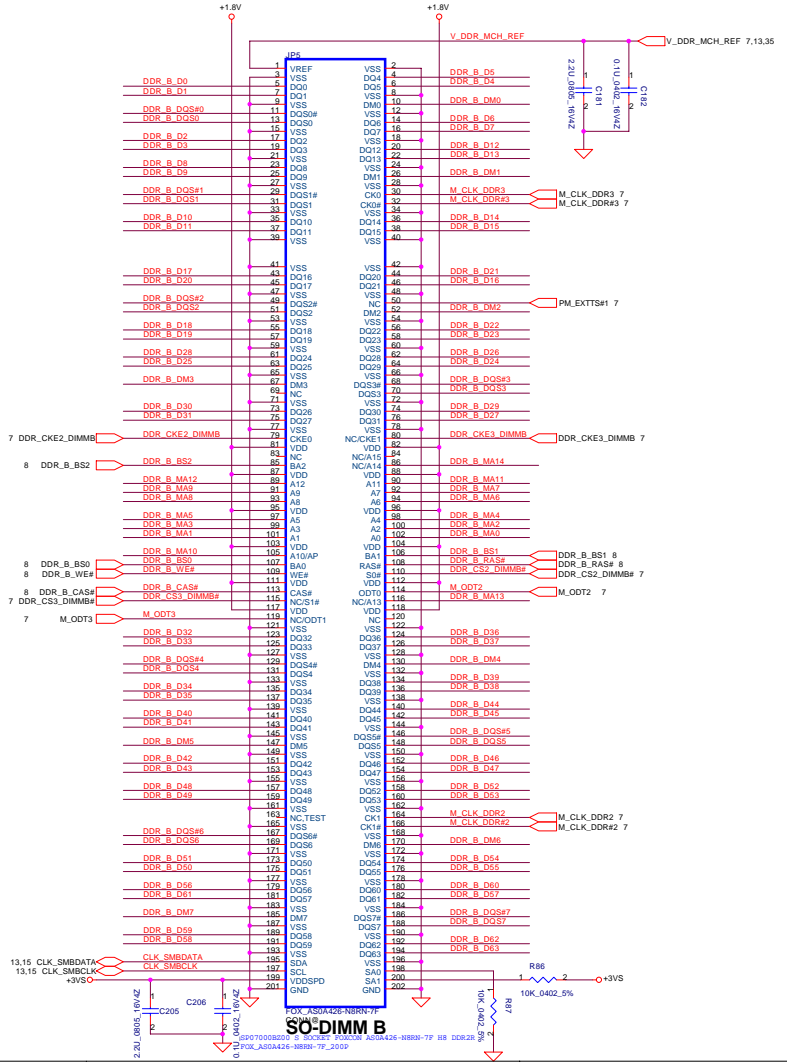
Layout Note:  
Place near JP10



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:  
Place these resistor closely JP10, all trace length Max=1.5"



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Size	Document Number	Rev	0.3
Date	Monday, October 22, 2007	Sheet	14 of 42

Compal Electronics, Inc.  
DDR1-SODIMM SLOT2

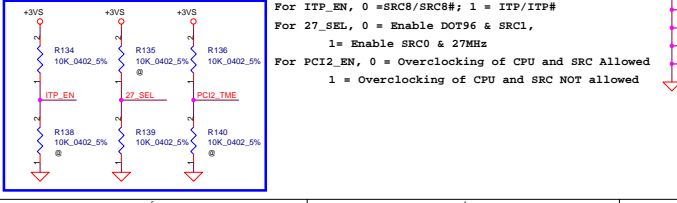
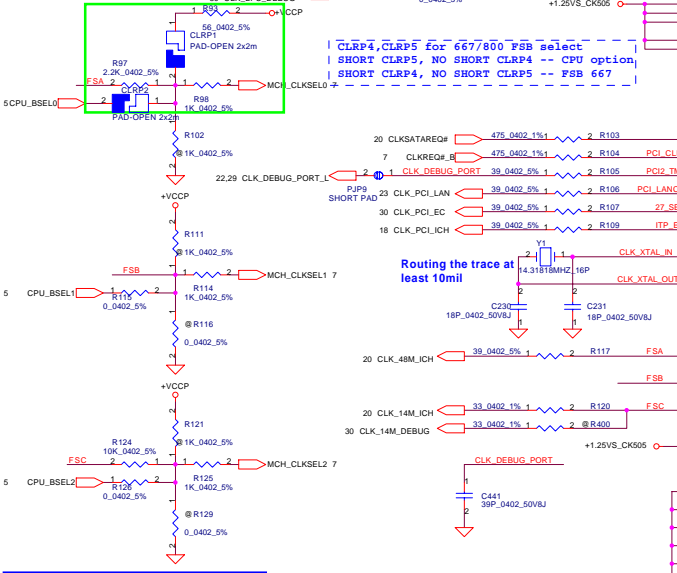
LA-3981P

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

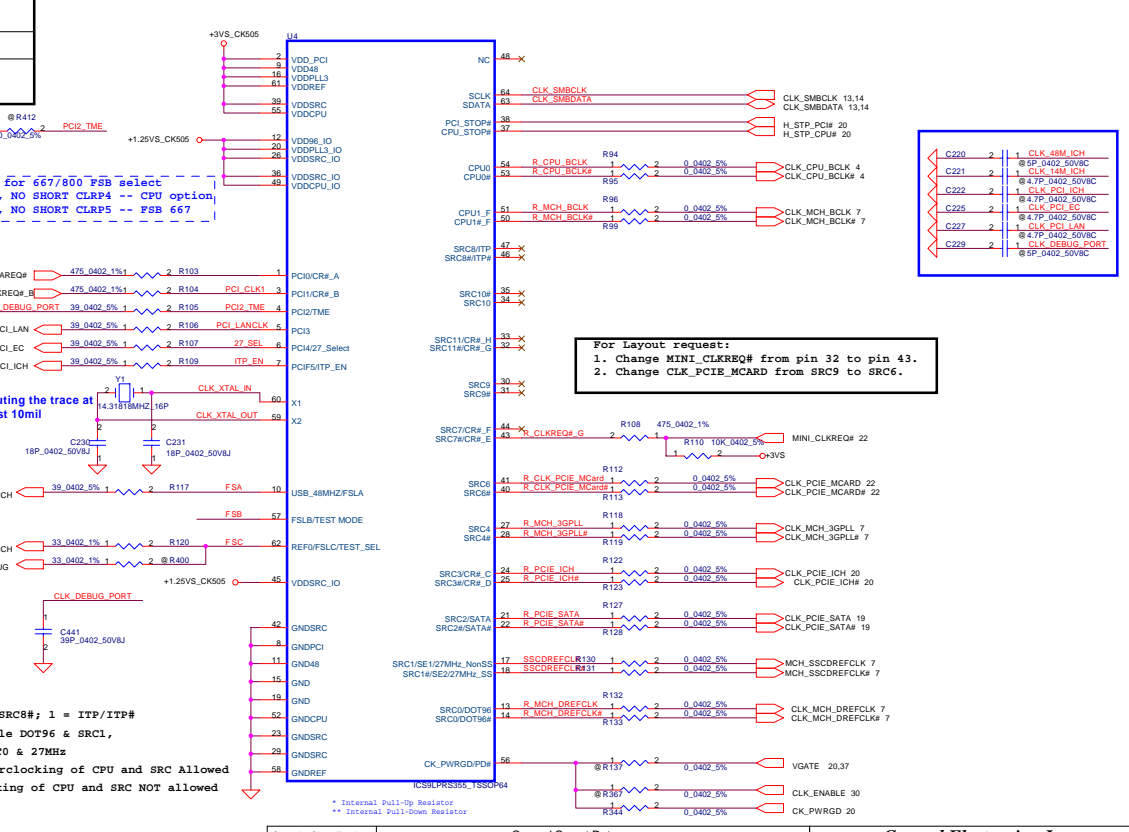
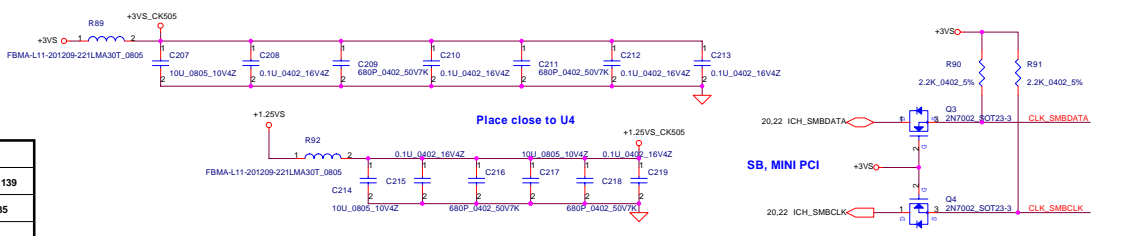
**FSB Frequency Set:**

CPU Driven	Stuff	R107	R113	R1083
*(Default)	No Stuff	R1074	R1086	R1098 R1113 R1128 R1139
	Stuff	R1086	R1139	R1135 R1074 R1139 R1135
667MHz	No Stuff	R1083	R1107	R1128 R1113 R1098
	Stuff	R1135	R1139	
800MHz	No Stuff	R1083	R1086	R1098 R1128 R1074 R1107 R1113

1019\_Change CLR1 and CLR2 type like the same as PJP4.



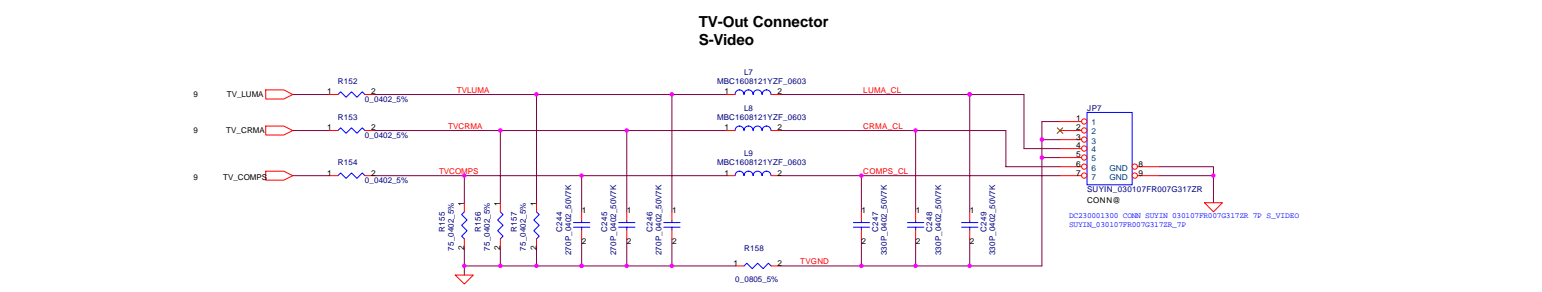
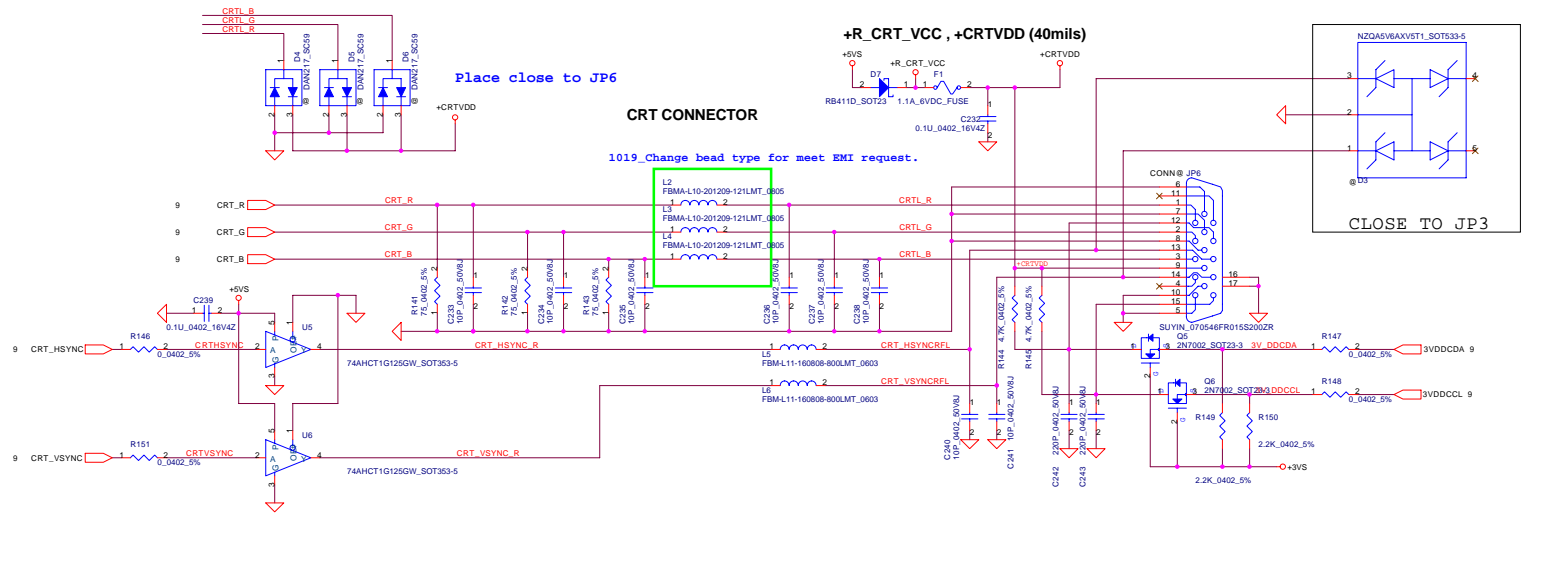
For ITP\_EN, 0 = SRC8/SRC#; 1 = ITP/ITP#  
 For 27\_SEL, 0 = Enable DOT96 & SRC1, 1 = Enable SRC0 & 27MHz  
 For PCI2\_EN, 0 = Overclocking of CPU and SRC Allowed, 1 = Overclocking of CPU and SRC NOT allowed



**For Layout request:**  
 1. Change MINI\_CLKREQ# from pin 32 to pin 43.  
 2. Change CLK\_PCIE\_MCARD from SRC9 to SRC6.

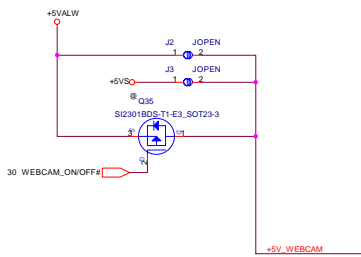
C220	2	1	CLK_48M_I
C221	2	1	SP_0402_50VBC
C222	2	1	CLK_14M_I
C223	2	1	4.7P_0402_50VBC
C224	2	1	CLK_PCI_I
C225	2	1	4.7P_0402_50VBC
C226	2	1	4.7P_0402_50VBC
C227	2	1	CLK_PCI_LAN
C228	2	1	4.7P_0402_50VBC
C229	2	1	CLK_DEBUG_PORT
			SP_0402_50VBC

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Size	Document Number	LA-3981P	Rev	0.3	
Date	Monday, October 22, 2007	Sheet	16	of	42

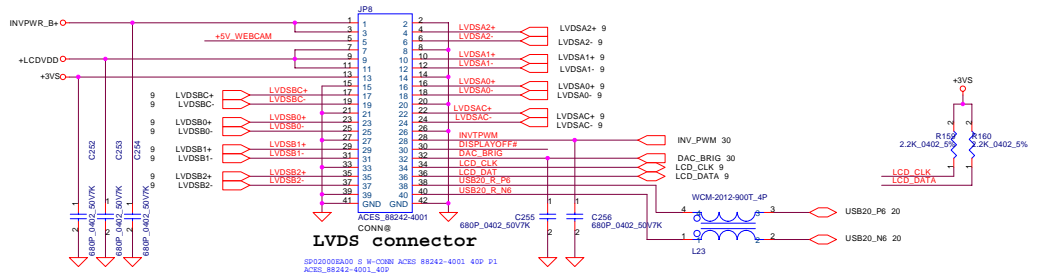
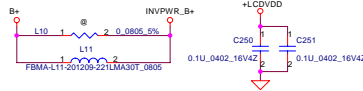


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<b>Compal Electronics, Inc.</b> <b>CRT &amp; TVout Connector</b>			Title <b>CRT &amp; TVout Connector</b>
Size Document Number <b>LA-3981P</b>			Rev <b>0.3</b>
Date: Monday, October 22, 2007			Sheet 16 of 42

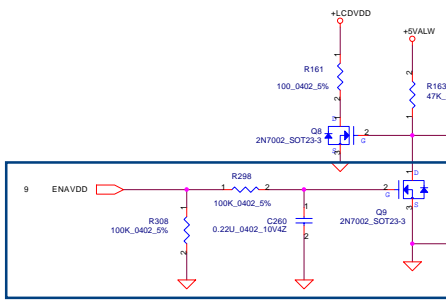




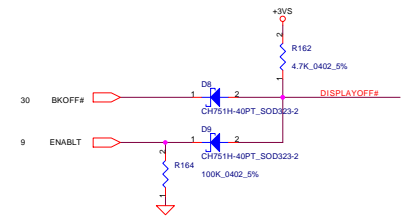
**LVDS CONN**



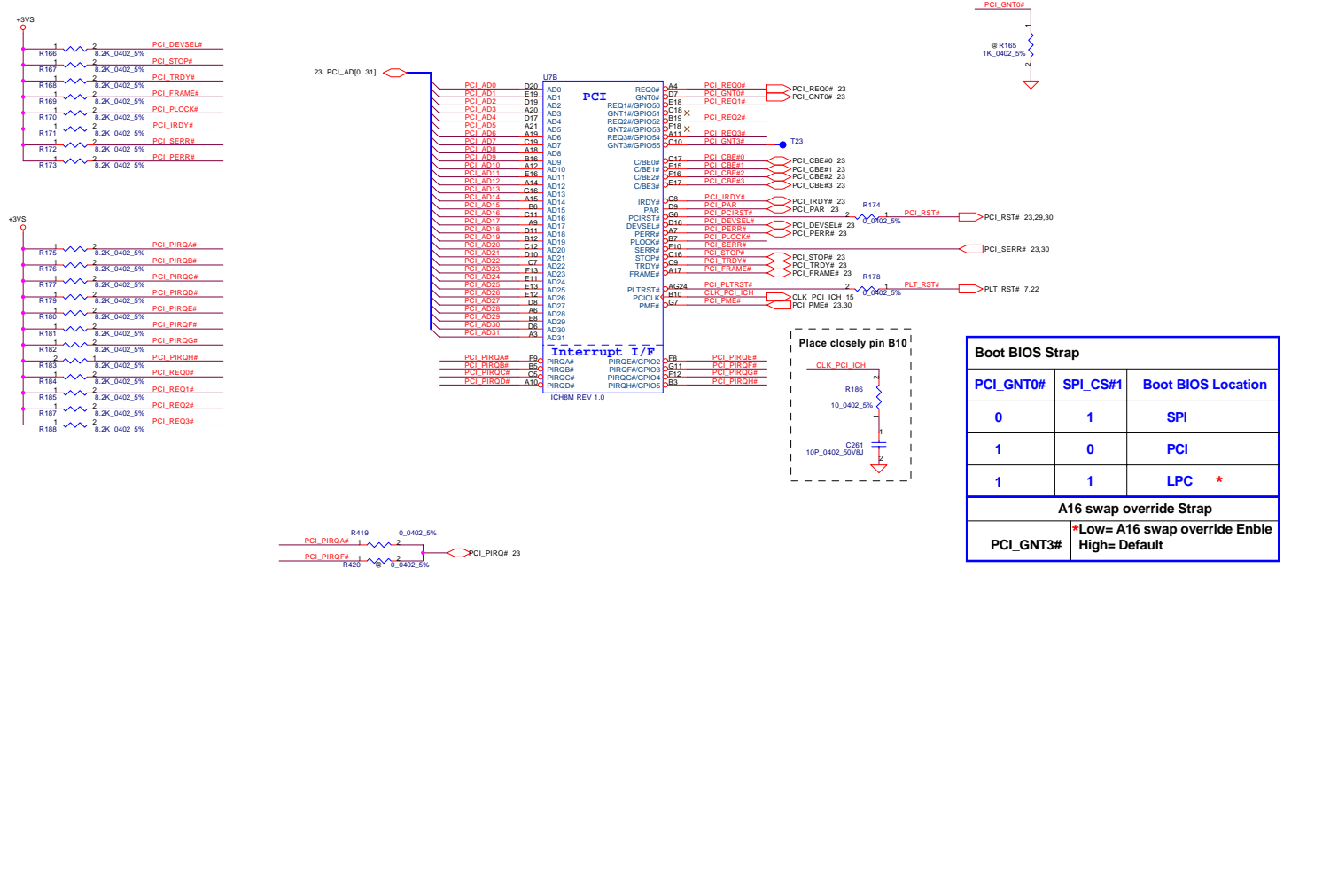
**LVDS connector**  
 ACES\_86242-4001  
 CONNR  
 680P\_0402\_50V7K  
 C256 680P\_0402\_50V7K  
 WCM-2012-900T\_4P  
 L23  
 USB20\_P6 20  
 USB20\_N6 20  
 ACES\_86242-4001\_40P P1  
 ACES\_86242-4001\_40P



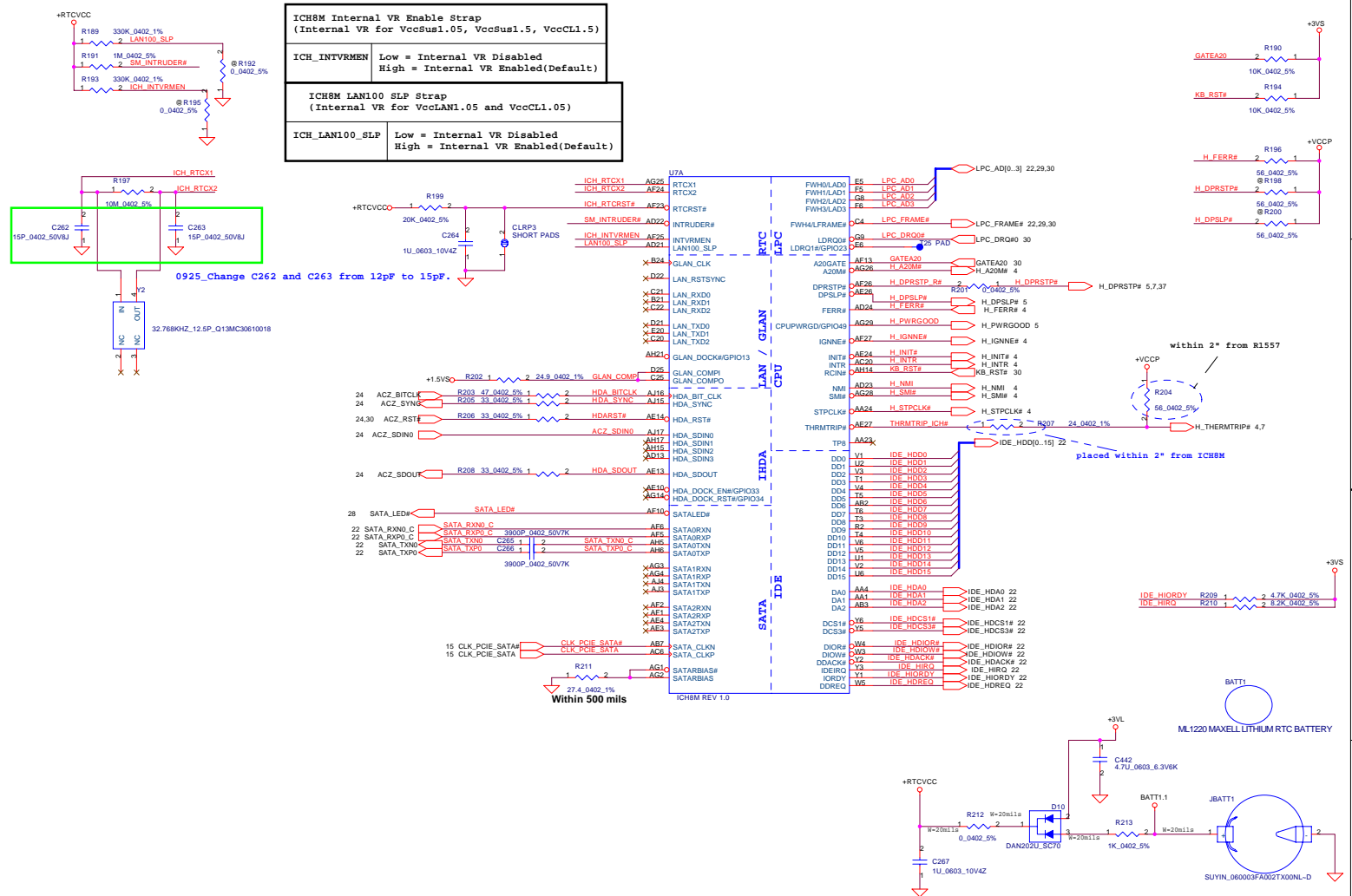
Avoid Panel display garbage after power on.



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Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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Size	Document Number	Rev		Date	
	LA-398IP	0.3		Monday, October 22, 2007	
			Sheet	17	of 42



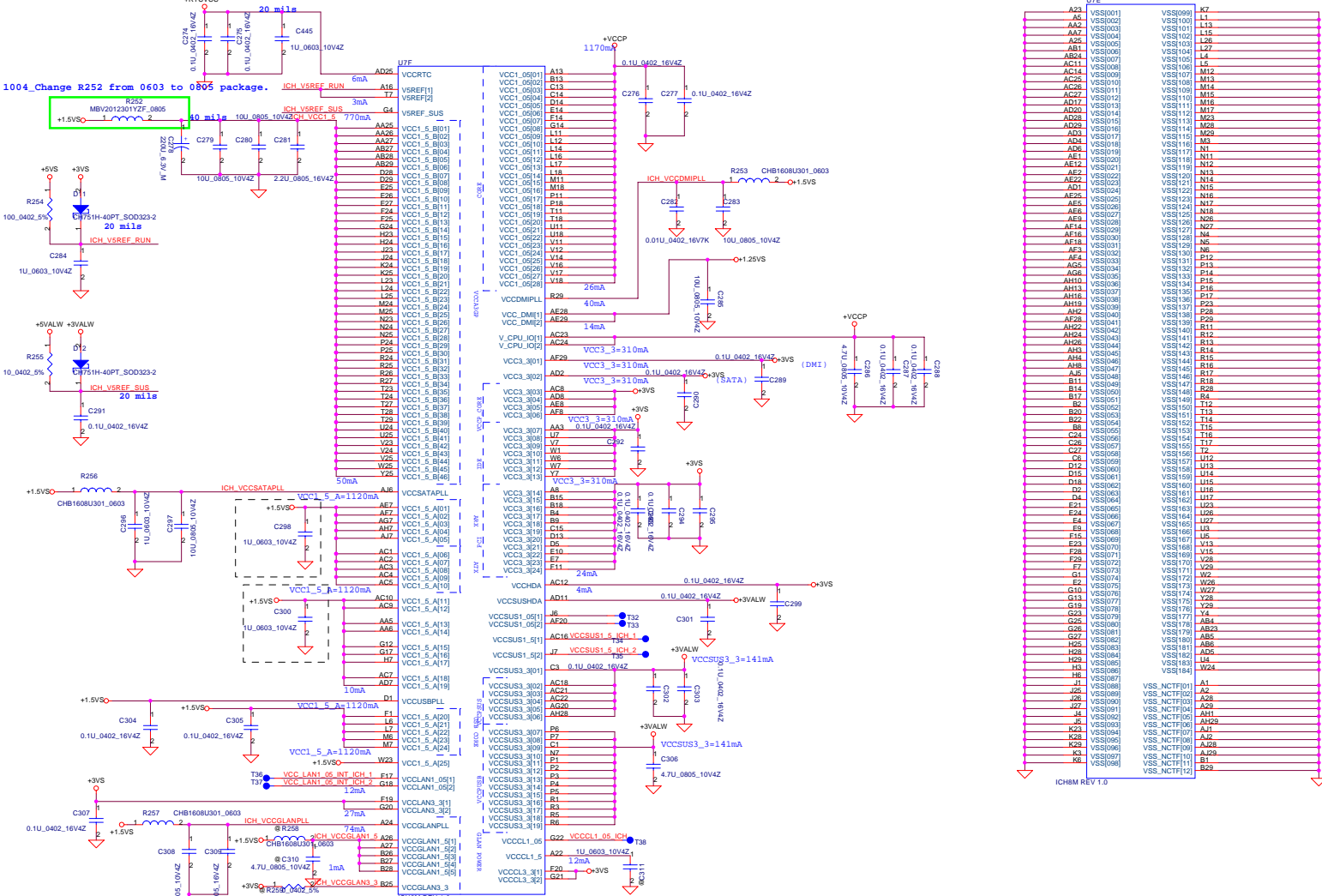
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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<b>ICH8M Internal VR Enable Strap</b> (Internal VR for VccSus1.05, VccCLL1.5)	
<b>ICH_INTVRMEN</b>	Low = Internal VR Disabled High = Internal VR Enabled(Default)
<b>ICH8M LAN100 SLP Strap</b> (Internal VR for VccLAN1.05 and VccCLL1.05)	
<b>ICH_LAN100_SLP</b>	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	ICH8(2/4) LAN,HD,IDE,LPC
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Date	Monday, October 22, 2007	Sheet	18	of 42

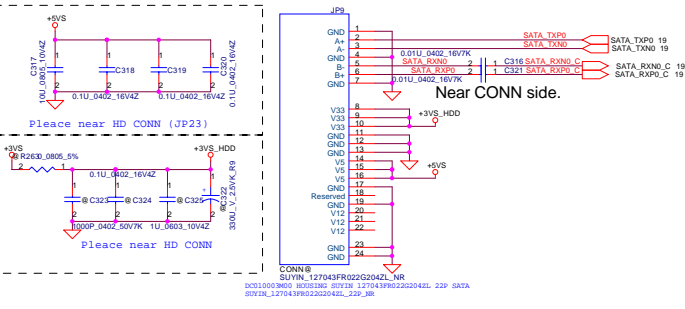




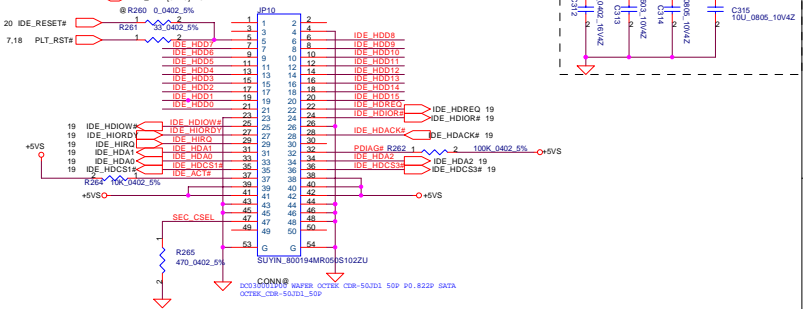
U7E	K7
AC	VSS000
AA2	VSS001
AA7	VSS002
AA5	VSS003
AB1	VSS004
AB2	VSS005
AB4	VSS006
AB1	VSS007
AC14	VSS008
AC2	VSS009
AC5	VSS010
AC6	VSS011
AC7	VSS012
AD17	VSS013
AD10	VSS014
AD3	VSS015
AD4	VSS016
AD5	VSS017
AD6	VSS018
AE1	VSS019
AE2	VSS020
AE3	VSS021
AE4	VSS022
AE5	VSS023
AE6	VSS024
AE7	VSS025
AE8	VSS026
AE9	VSS027
AF4	VSS028
AF6	VSS029
AF3	VSS030
AF4	VSS031
AG5	VSS032
AG6	VSS033
AH10	VSS034
AH13	VSS035
AH8	VSS036
AH9	VSS037
AH10	VSS038
AH11	VSS039
AH12	VSS040
AH13	VSS041
AH14	VSS042
AH15	VSS043
AH16	VSS044
AH17	VSS045
AH18	VSS046
AH19	VSS047
AH20	VSS048
AH21	VSS049
AH22	VSS050
AH23	VSS051
AH24	VSS052
AH25	VSS053
AH26	VSS054
AH27	VSS055
AH28	VSS056
AH29	VSS057
AH30	VSS058
AH31	VSS059
AH32	VSS060
AH33	VSS061
AH34	VSS062
AH35	VSS063
AH36	VSS064
AH37	VSS065
AH38	VSS066
AH39	VSS067
AH40	VSS068
AH41	VSS069
AH42	VSS070
AH43	VSS071
AH44	VSS072
AH45	VSS073
AH46	VSS074
AH47	VSS075
AH48	VSS076
AH49	VSS077
AH50	VSS078
AH51	VSS079
AH52	VSS080
AH53	VSS081
AH54	VSS082
AH55	VSS083
AH56	VSS084
AH57	VSS085
AH58	VSS086
AH59	VSS087
AH60	VSS088
AH61	VSS089
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AH71	VSS099
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AH167	VSS195
AH168	VSS196
AH169	VSS197
AH170	VSS198
AH171	VSS199
AH172	VSS200

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<b>Compal Electronics, Inc.</b> <b>IC8M(4) POWER&amp;GND</b>		Title Customer: <b>LA-390IP</b>	
Size: Document Number Date: Monday, October 22, 2007		Rev: 0.3 Sheet: 21 of 42	

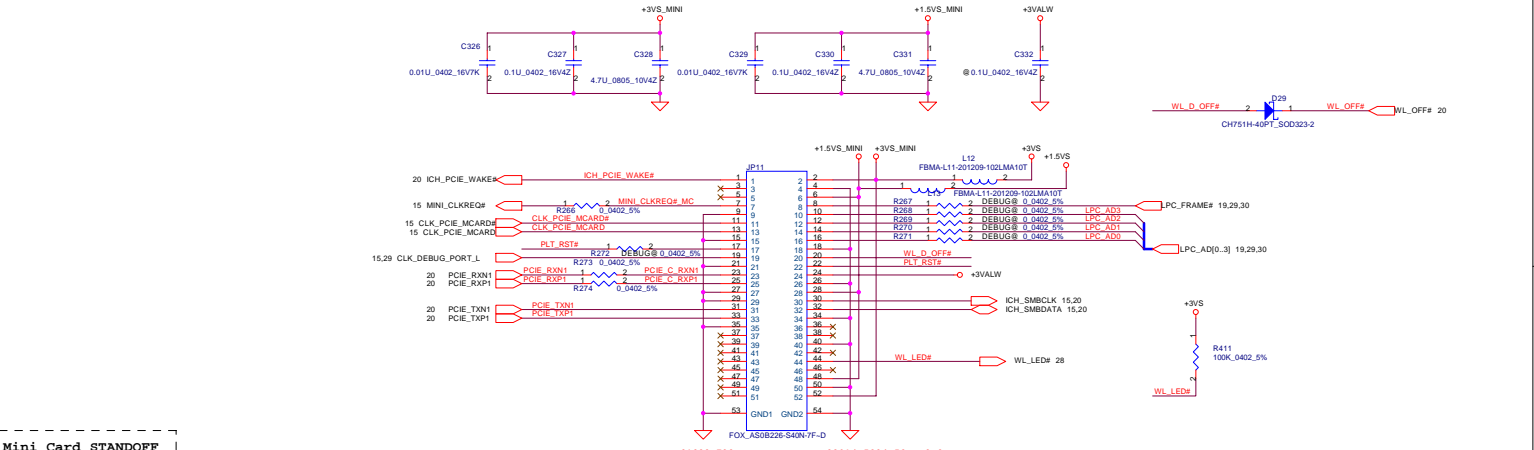
### HDD Connector



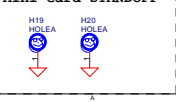
### CD-ROM Connector



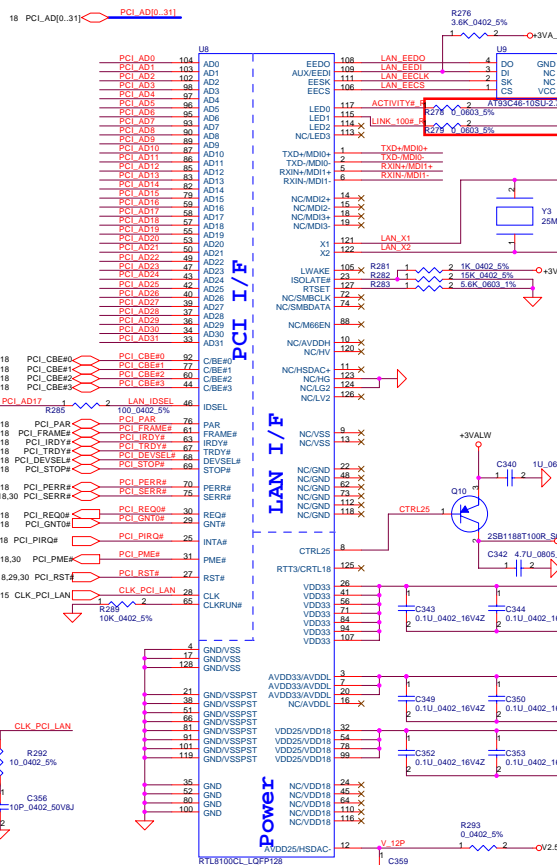
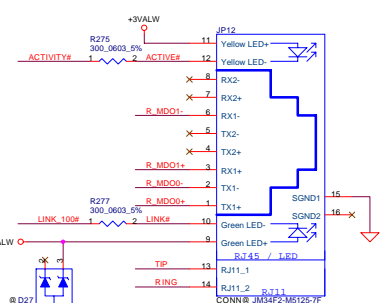
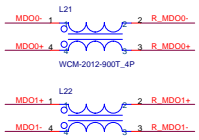
### Mini-Express Card---WLAN



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Issued Date		Deciphered Date		HDD/ODD/Mini Card CONN.	
2007/03/26		2007/08/29		LA-3981P	
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				Monday, October 22, 2007	Sheet 22 of 42



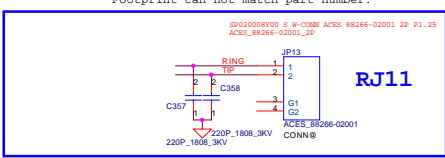
Close to JP12.



For RMI, locate close to LAN chip

close to chip

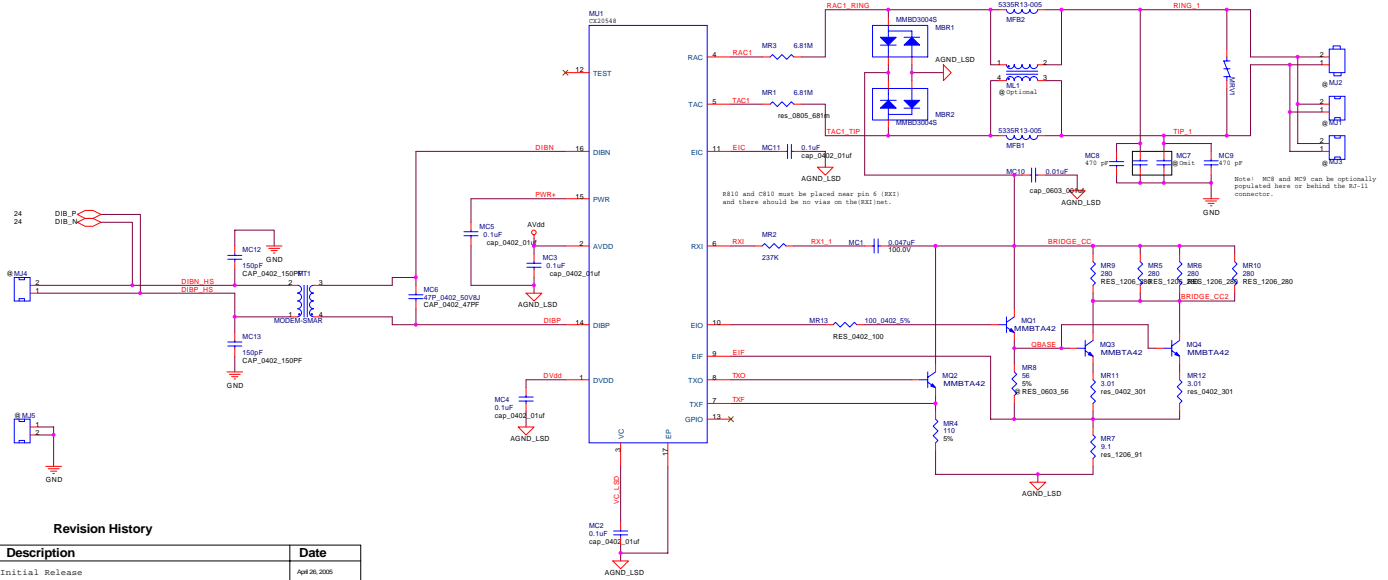
close to magnetic



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Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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				LA-3981P	Rev 0.3
				Date	Monday, October 22, 2007
				Sheet	23 of 42







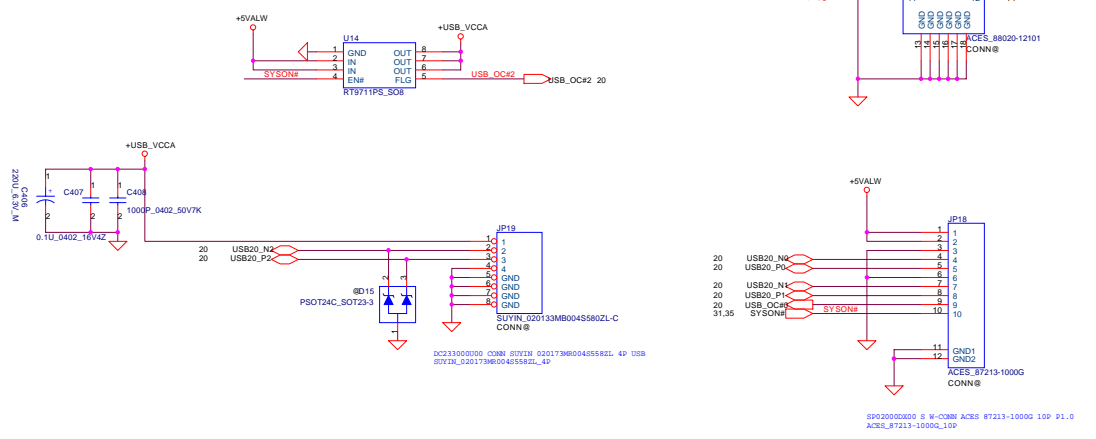
**Revision History**

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 15, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

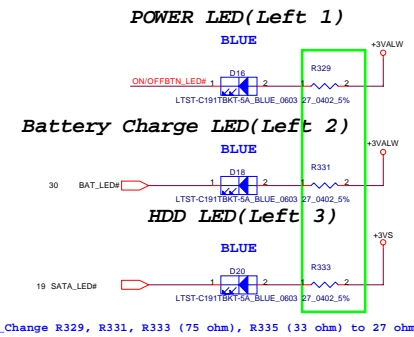
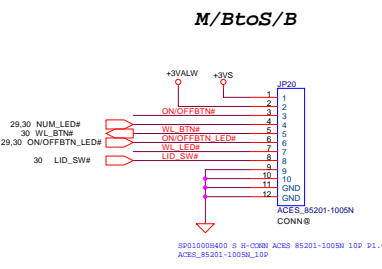
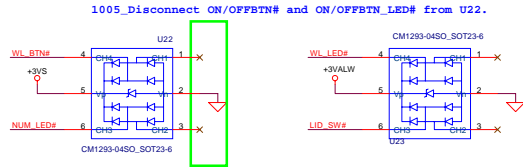
Security Classification	Compal Secret Data	Deciphered Date	File
	2007/03/26	2007/07/26	AMOM-CX20548
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### USB Port

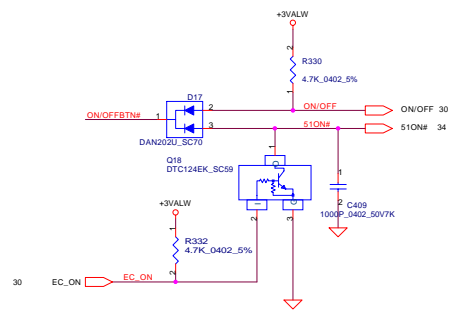


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Issued Date	2007/03/26	Deciphered Date	2006/07/26	<b>USB CONN.</b>	
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Size	Document Number	Rev	Date: Monday, October 22, 2007 Sheet 27 of 42		
	<b>LA-398IP</b>	0.3			

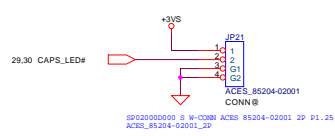


0927\_Change R329, R331, R333 (75 ohm), R335 (33 ohm) to 27 ohm.

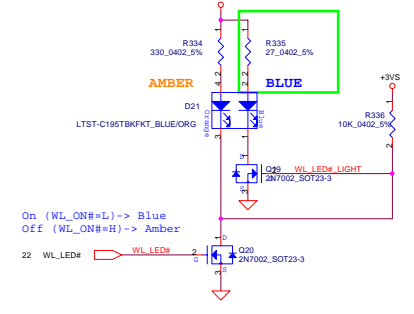
Power ON/OFF



M/B to SB(Caps Lock LED)

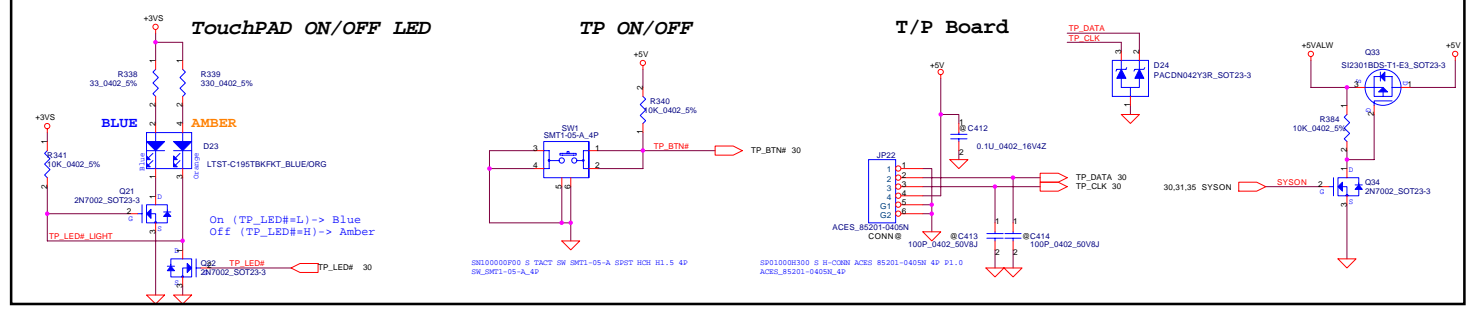


Wireless ON/OFF LED(Left 4)

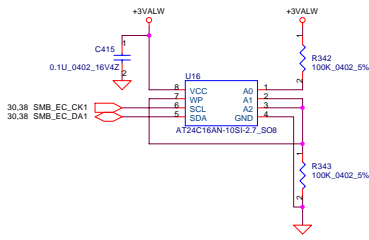


On (WL\_ON#=L) -> Blue  
Off (WL\_ON#=H) -> Amber

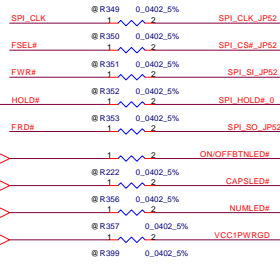
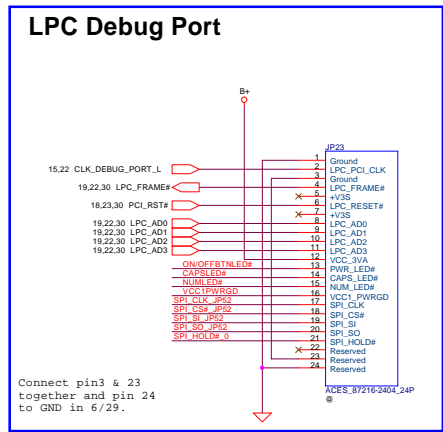
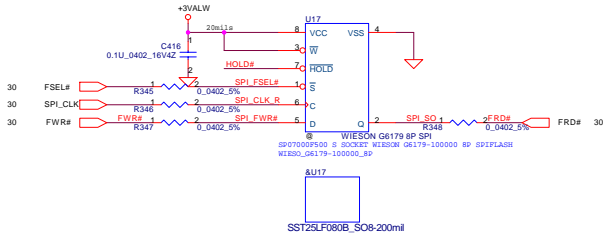
D21, D25, D23 Footprint can not match part number.



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				Rev: 0.3

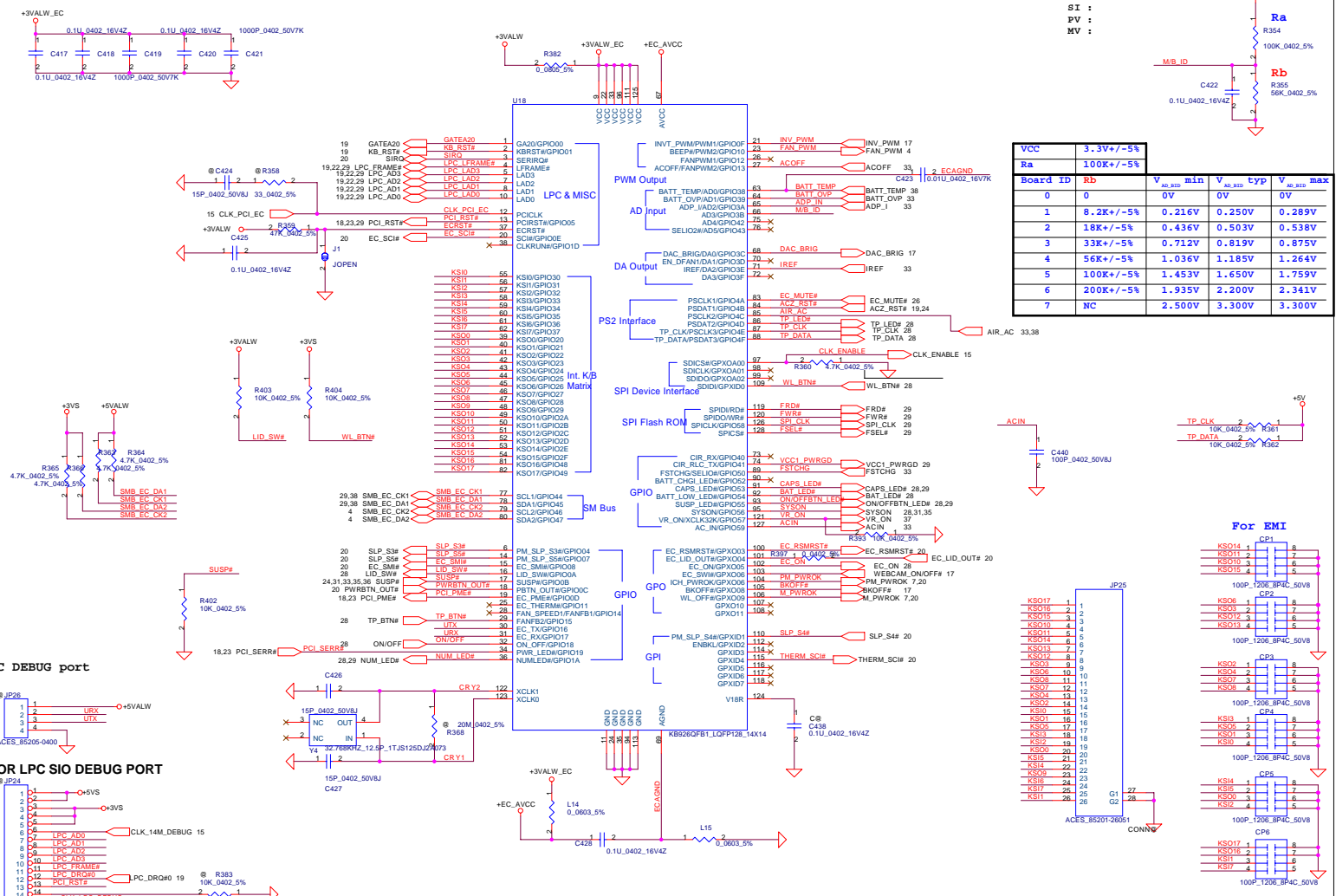


**SPI ROM**



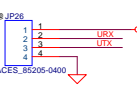
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Date	Monday, October 22, 2007	Sheet	29	of 42

Board ID : DB : 4  
 SI :  
 PV :  
 MV :  
 +3VALW\_EC  
 Ra  
 R354  
 100K\_0402\_5%

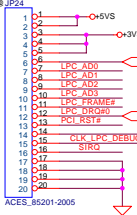


Board ID	Rb	V <sub>min</sub>	V <sub>AD_BSD</sub>	typ	V <sub>max</sub>
0	0	0V	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V	
2	1.8K+/-5%	0.436V	0.503V	0.538V	
3	33K+/-5%	0.712V	0.819V	0.875V	
4	56K+/-5%	1.036V	1.185V	1.264V	
5	100K+/-5%	1.453V	1.650V	1.759V	
6	200K+/-5%	1.935V	2.200V	2.341V	
7	NC	2.500V	3.300V	3.300V	

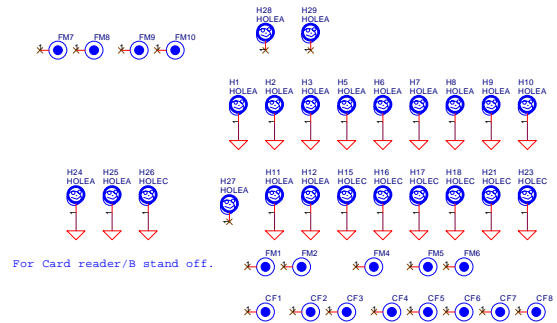
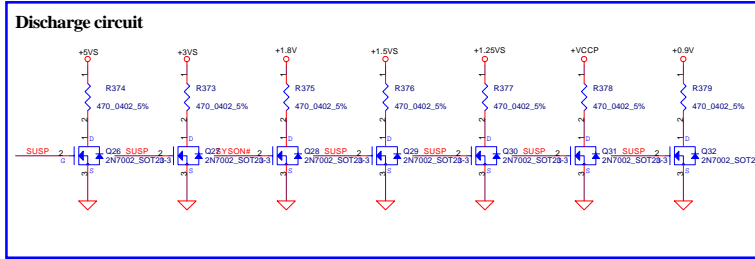
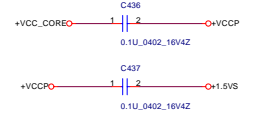
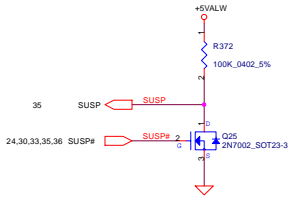
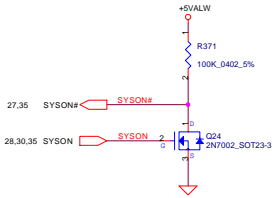
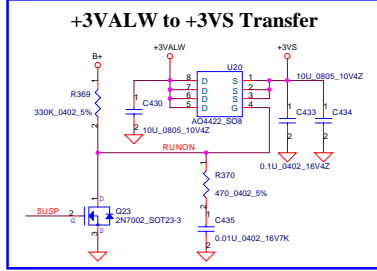
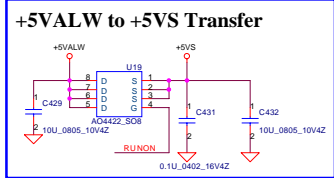
**EC DEBUG port**



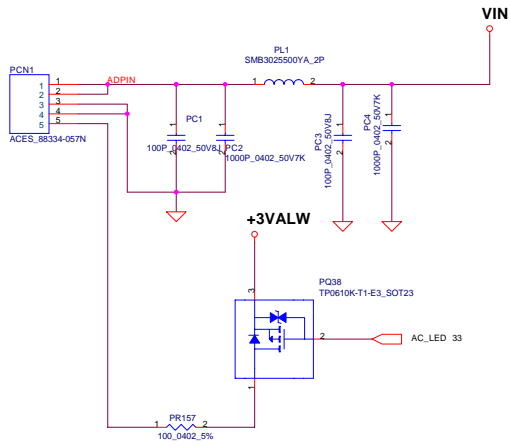
**FOR LPC SIO DEBUG PORT**



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Size	Document Number	Sheet	30	of 42
Date	Monday, October 22, 2007	Rev	0.3	

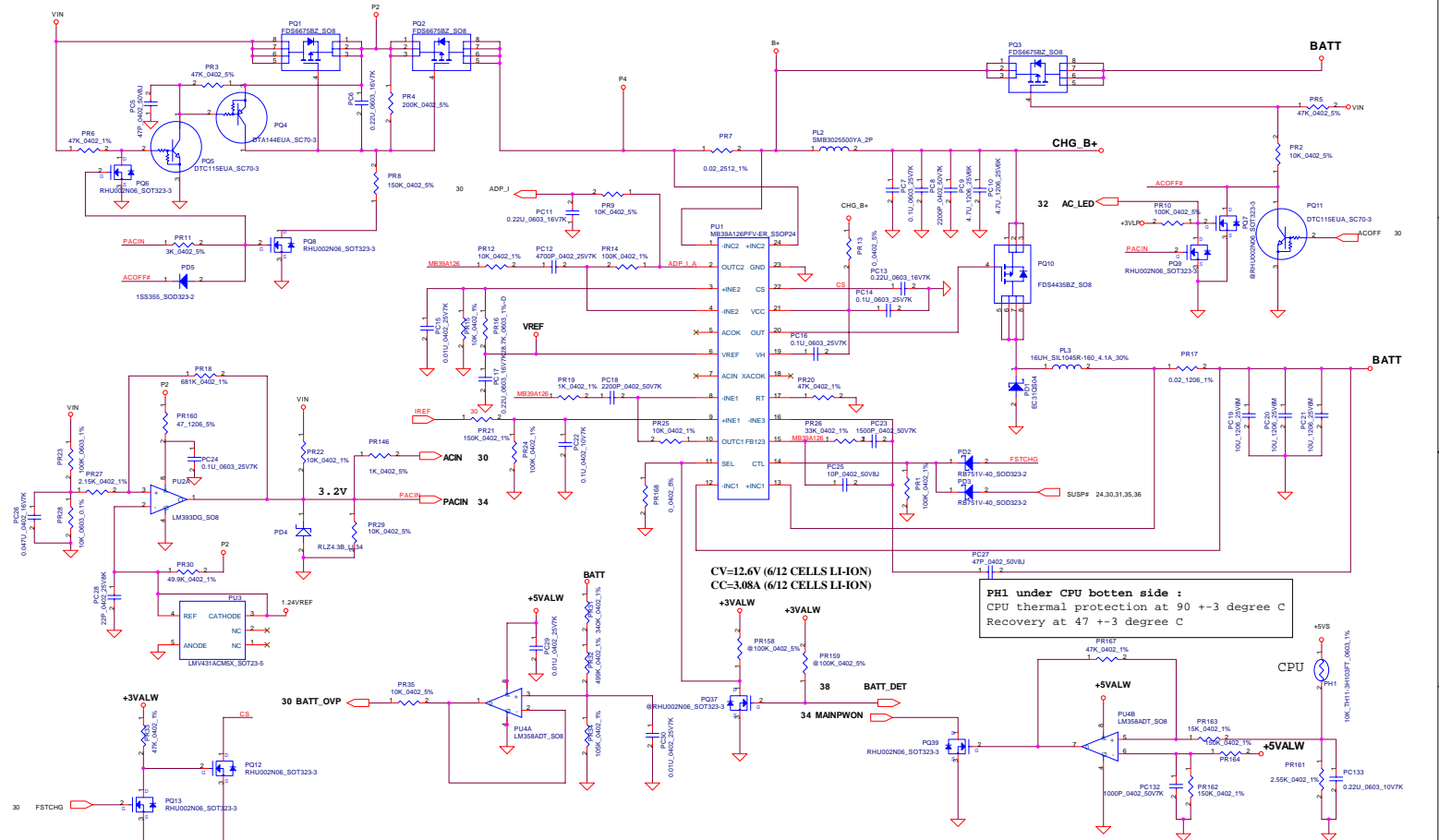


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Date	Monday, October 22, 2007	Sheet	32 of 42	Rev

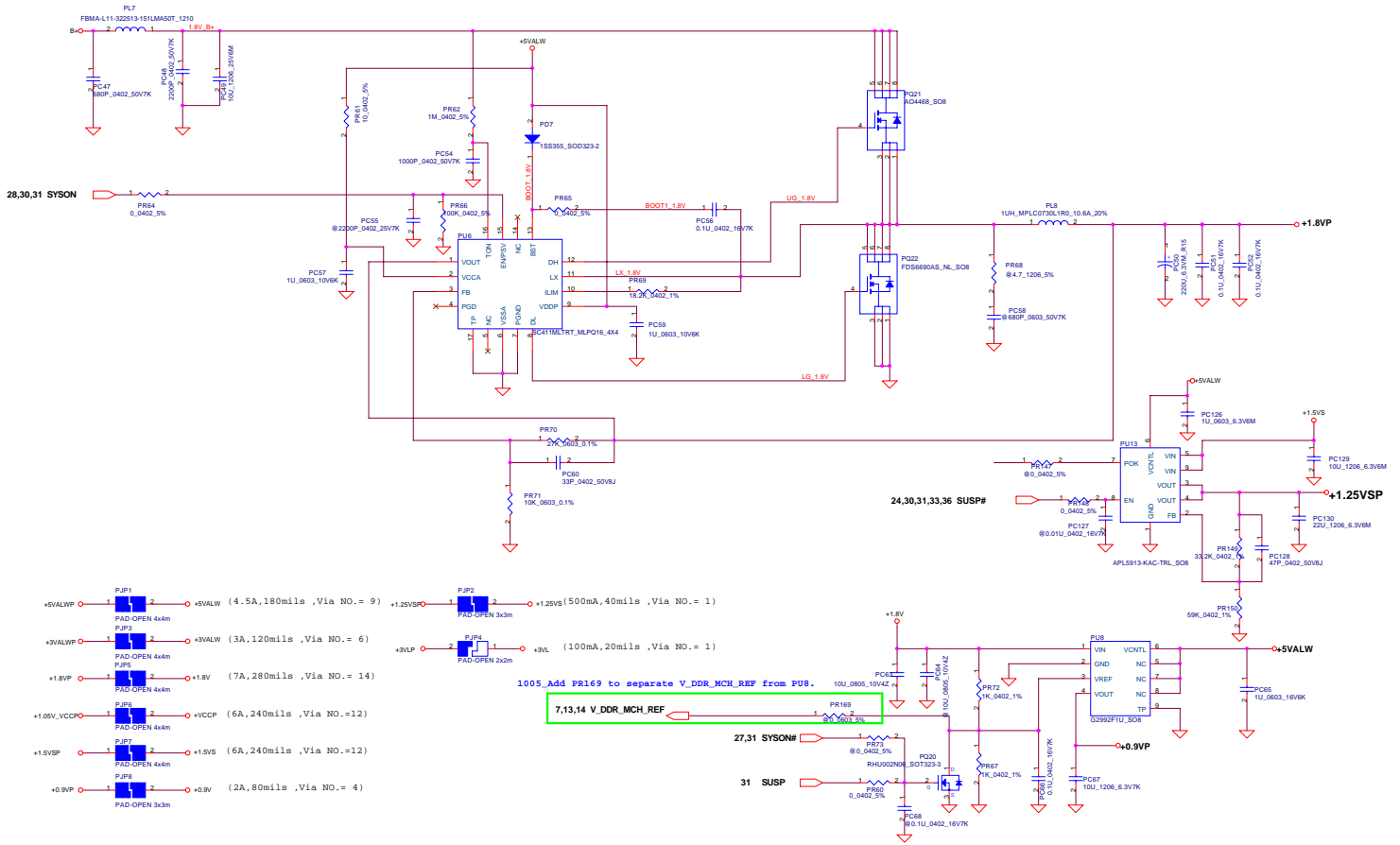




PH1 under CPU bottom side :  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 47 +/-3 degree C

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28,30,31 SYSON

24,30,31,33,36 SUSP#

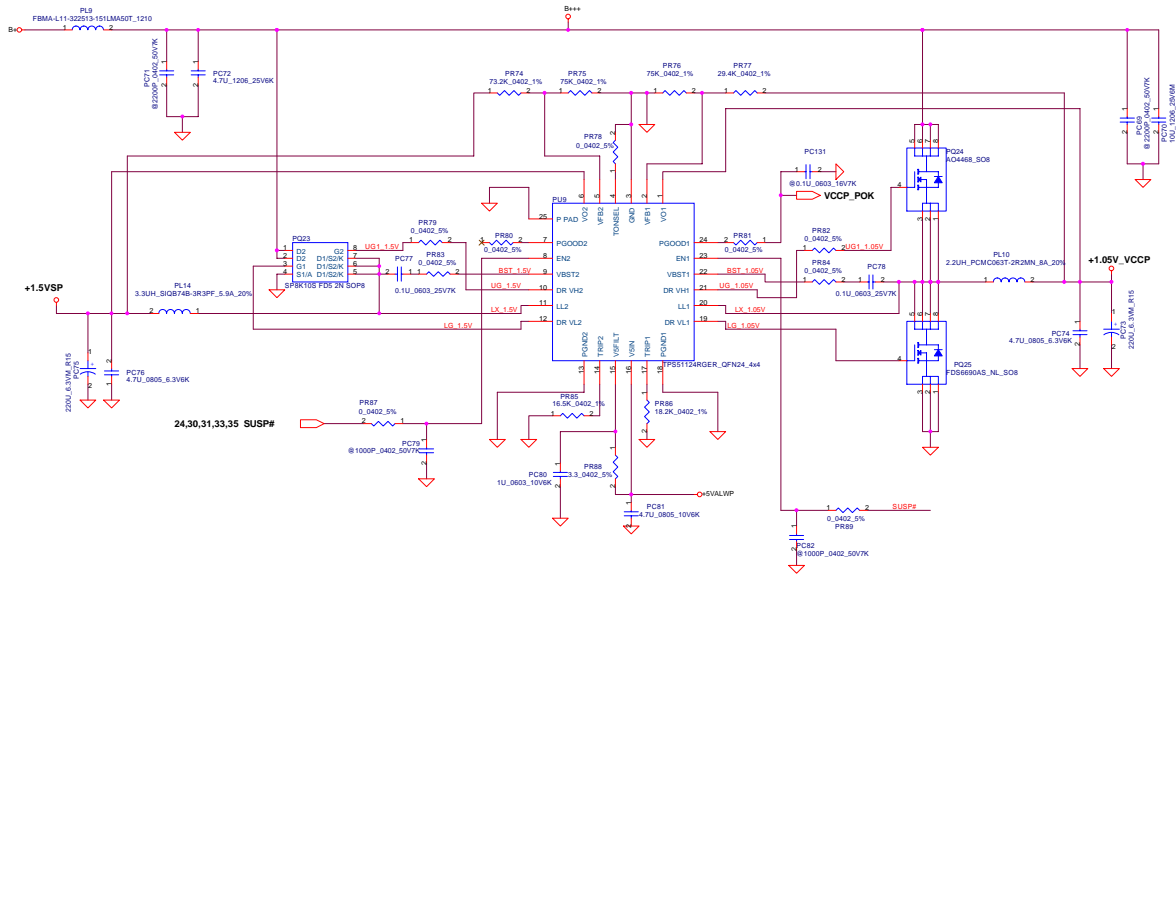
27,31 SYSON#

31 SUSP

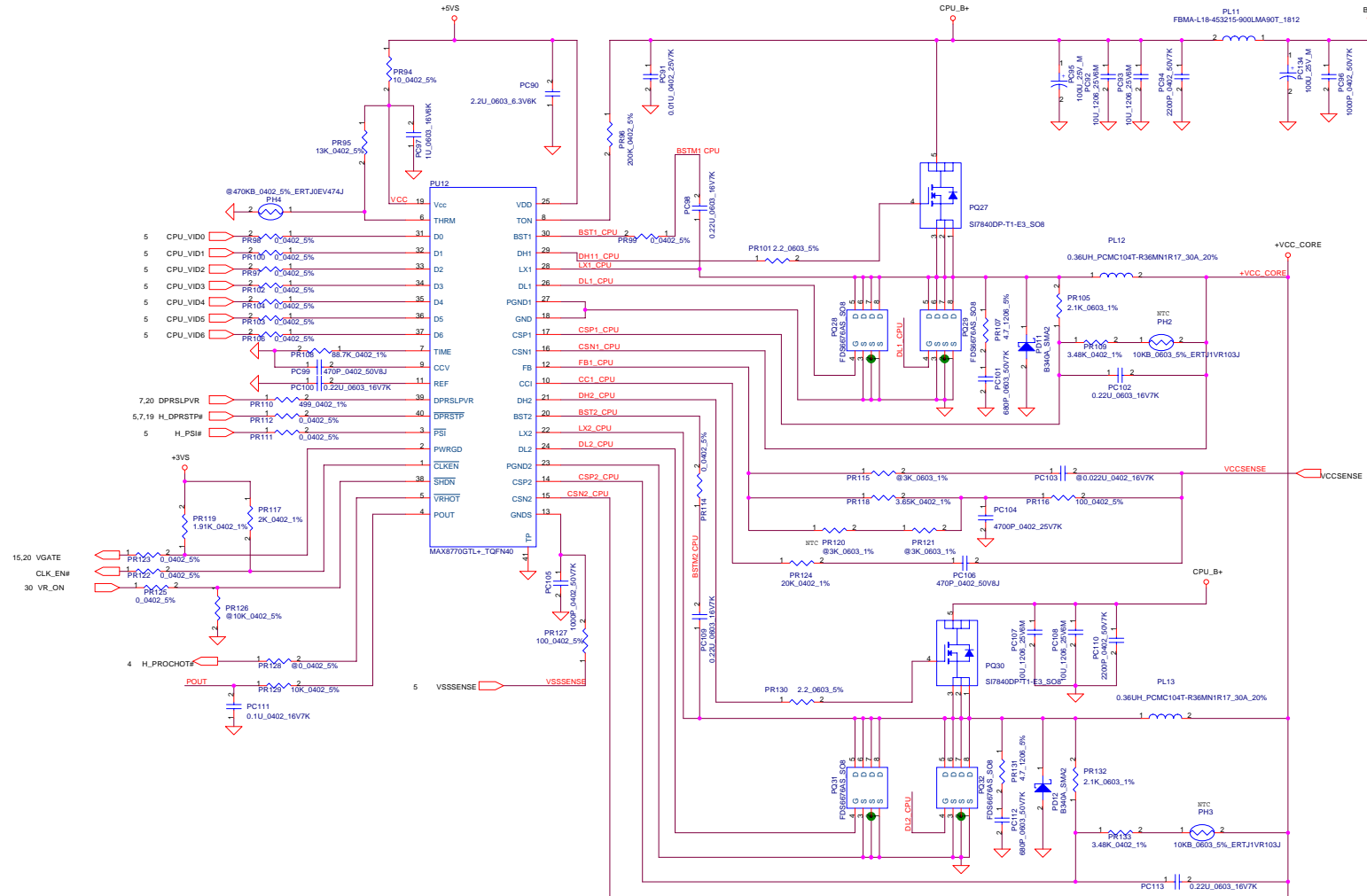
1005\_Add FR169 to separate V\_DDR\_MCH\_REF from PUS.  
7,13,14 V\_DDR\_MCH\_REF

- +SVALWP PJP1 2 +SVALW (4.5A,180mils ,Via NO.= 9)
- +SVALWP PJP2 2 +SVALW (3A,120mils ,Via NO.= 6)
- +1.8VP PJP3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V\_VCCP PJP6 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PJP7 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PJP8 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PJP2 2 +1.25VS (500mA,40mils ,Via NO.= 1)
- +9VP PJP1 1 +9V (100mA,20mils ,Via NO.= 1)

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Size	Document Number	Rev	03		
8.5x	LA-3981P	01	03		
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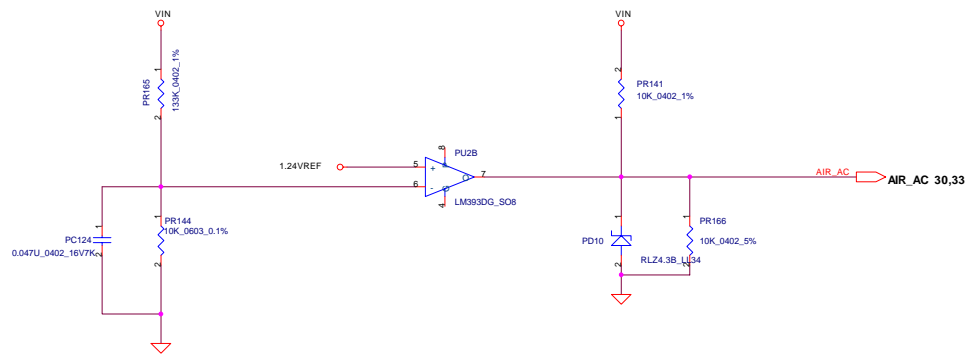
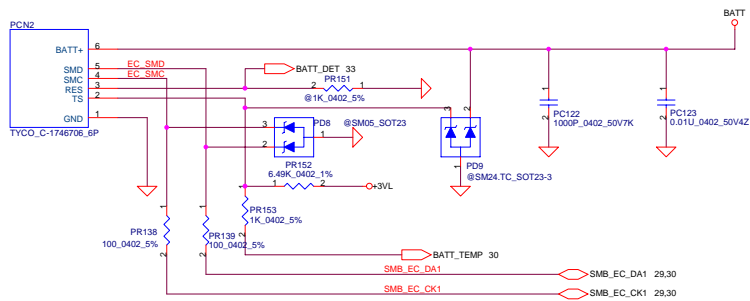


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<b>Compal Electronics, Inc.</b>		
File	<b>+CPU CORE</b>	
Site	Document Number	Rev
Cust		0.9
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				Date: Monday, October 22, 2007

Item	Reason for change	PG#	Modify List	Date	Phase
1			1009_FL8 change to 1uH.		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Security Classification	Compal Secret Data		Title	
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Version Change List ( P. I. R. List ) for HW Circuit

Item	Change Item	Page	Date	Phase
1	Change C262 and C263 from 15pF to 12pF	19	7/16	DB --> SI
2	Reserved R245 and Add R422	20	7/16	DB --> SI
3	Add D29 prevent leakage issue	22	7/16	DB --> SI
4	Reserved diode D30 D31 for ESD	26	7/16	DB --> SI
5	Reserved R423 for coat down plan	24	7/24	DB --> SI
6	Remove Q12-Q17, R323 R324 R327 R328 R417 R418	26	7/30	DB --> SI
7	Change EXT MIC port B to port C	24	7/31	DB --> SI
8				DB --> SI
9				DB --> SI
10				DB --> SI
11				DB --> SI
12				DB --> SI
13				DB --> SI
14				DB --> SI
15				DB --> SI
16				DB --> SI
17				DB --> SI
18				DB --> SI
19				DB --> SI
20				DB --> SI
21				DB --> SI
22				DB --> SI
23				DB --> SI
24				DB --> SI
25				DB --> SI
26				DB --> SI
27				DB --> SI
28				DB --> SI
29				DB --> SI

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3

2

1

Rev

0.3



Version Change List ( P. I. R. List ) for HW Circuit

Item	Change Item	Page	Date	Phase	
1	Change R296 R337 R value	24	Follow conexant new design rule	8/6	SI --> FV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI --> FV
3	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI --> FV
4	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI --> FV
5	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI --> FV
6	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI --> FV
7	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI --> FV
8	For EMI request.	26	Add L24-L27	9/5	SI --> FV
9	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF	9/7	SI --> FV
10	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI --> FV
11	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI --> FV
12					SI --> FV
13					SI --> FV
14					SI --> FV
15					SI --> FV
16					SI --> FV
17					SI --> FV
18					SI --> FV
19					SI --> FV
20					SI --> FV
21					SI --> FV
22					SI --> FV
23					SI --> FV
24					SI --> FV
25					SI --> FV
26					SI --> FV
27					SI --> FV
28					SI --> FV
29					SI --> FV
30					SI --> FV
31					SI --> FV
32					SI --> FV
33					SI --> FV
34					SI --> FV
35					SI --> FV
36					SI --> FV
37					SI --> FV
38					SI --> FV

Security Classification	Compal Secret Data		Title	
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Version Change List ( P. I. R. List ) for HW Circuit

Item	Change item	Page		Date	Phase
1	Solve Vref miss when entry S3 mode.	7	Stuff R43 and R46.	9/25	PV --> MV
2	Solve wave ripple on CRT and TV.	10	Change C439 from 0.47uF to 4.7uF.	9/25	PV --> MV
3	Solve RTC timing too exceed.	18	Change C262 and C263 from 12pF to 15pF.	9/25	PV --> MV
4	Reduce INT.MIC noise.	24	Add LFP (R429 and C452).	9/25	PV --> MV
5	Solve S3 resume fail when use Micron DDR module.	35	Add PR169 to separate V_DDR_MCH_REF from PUS.	10/05	PV --> MV
6	Solve pop noise when entry or resume from S3.	24	Modify FC Beep (C373, R302, R306) circuit.	9/27	PV --> MV
7	Solve EMI fail for Memory module.	7	Change R34/R35 from 20 ohm to 30 ohm.	9/27	PV --> MV
8	Fine-tune LED brightness.	28	Change R329, R331, R333, R335 from 33 ohm to 27 ohm.	9/27	PV --> MV
9	ICH 1.5V power rail 700mA current requirement.	21	Change R252 package from 0603 to 0805.	10/04	PV --> MV
10	Solve can not power on when stuff U22.	28	Disconnect ON/OFFBTN# and ON/OFFBTN_LED# from U22.	10/05	PV --> MV
11	For EMI request.	16	Change L2, L3, L4 to FBMA-L10-201209-121LMT_0805.	10/19	PV --> MV
12	To avoid too easy to open solder for CLR2.	15	Change CLR2P1 and CLR2P2 type like the same as PJP4.	10/19	PV --> MV
13	Solve acoustic noise issue.	10	Change R64, R79, R81 from 0 ohm to 1uH/400mA inductor.	10/22	PV --> MV

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				LA-3981P
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