

Compal confidential

Schematics Document

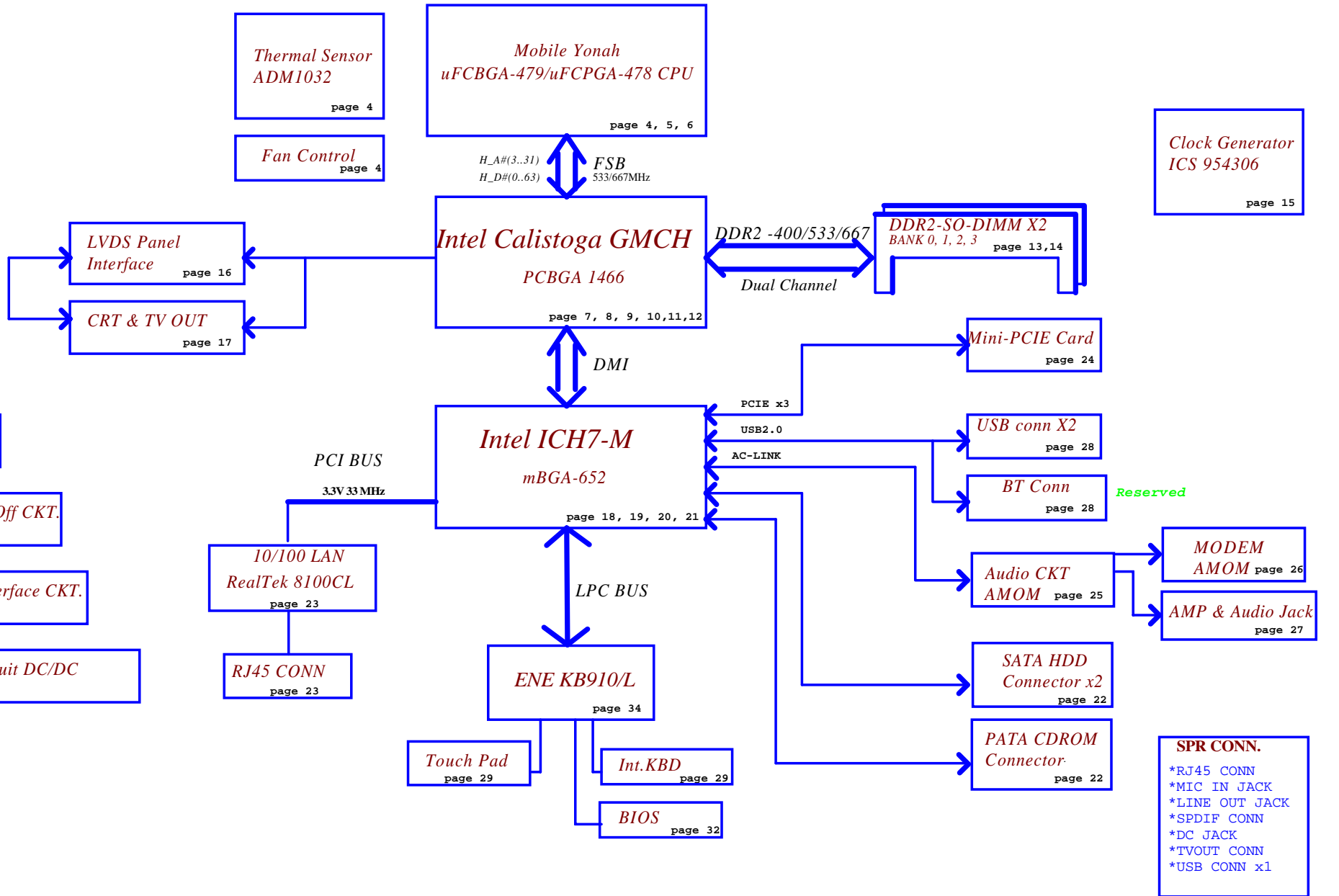
Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-07-24

REV:1.0



Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Cover Sheet		
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Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
s0	○	○	○	○
s1	○	○	○	○
s3	○	○	○	✗
s5 s4/AC	○	○	✗	✗
s5 s4/ Battery only	○	✗	✗	✗
s5 s4/AC & Battery don't exist	✗	✗	✗	✗

○ MEANS ON
✗ MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTek 8100CL	AD24	1	A

Load BOM check item

MV step from PIRQE change to PIRQA for LAN poor performance.

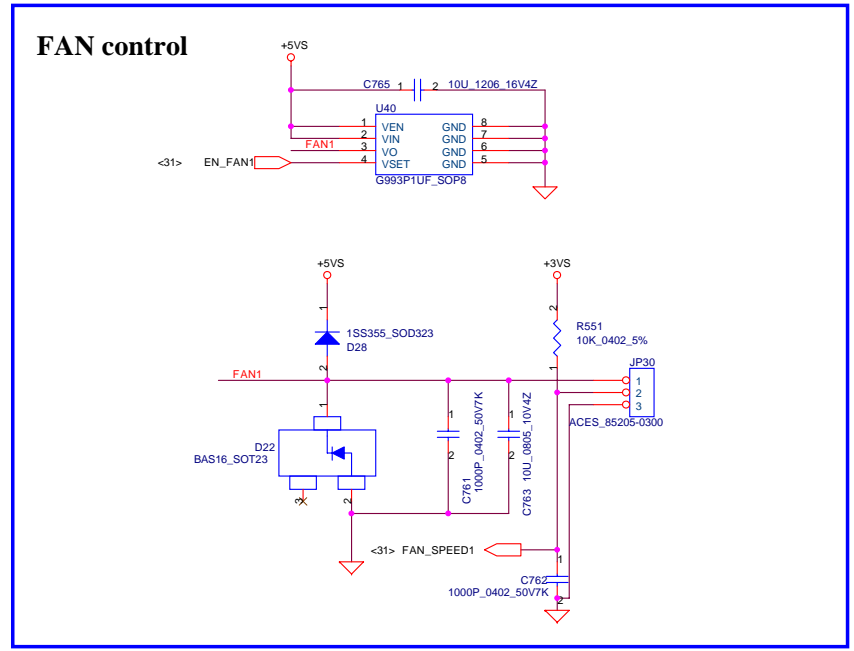
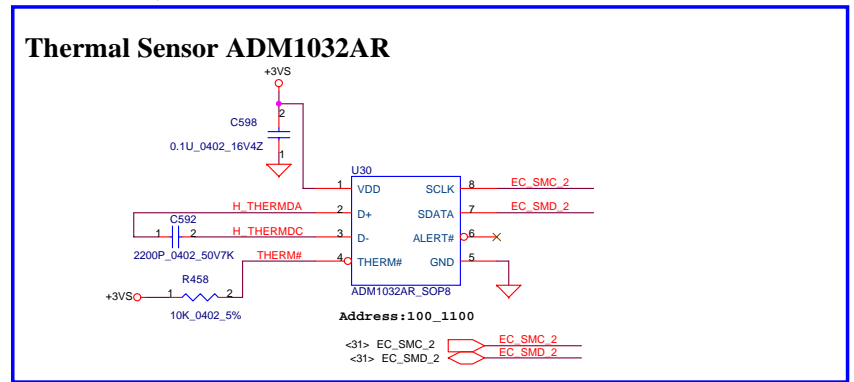
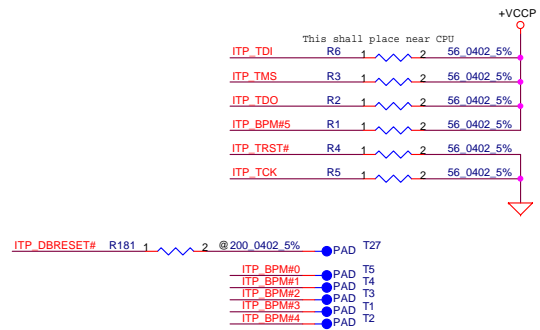
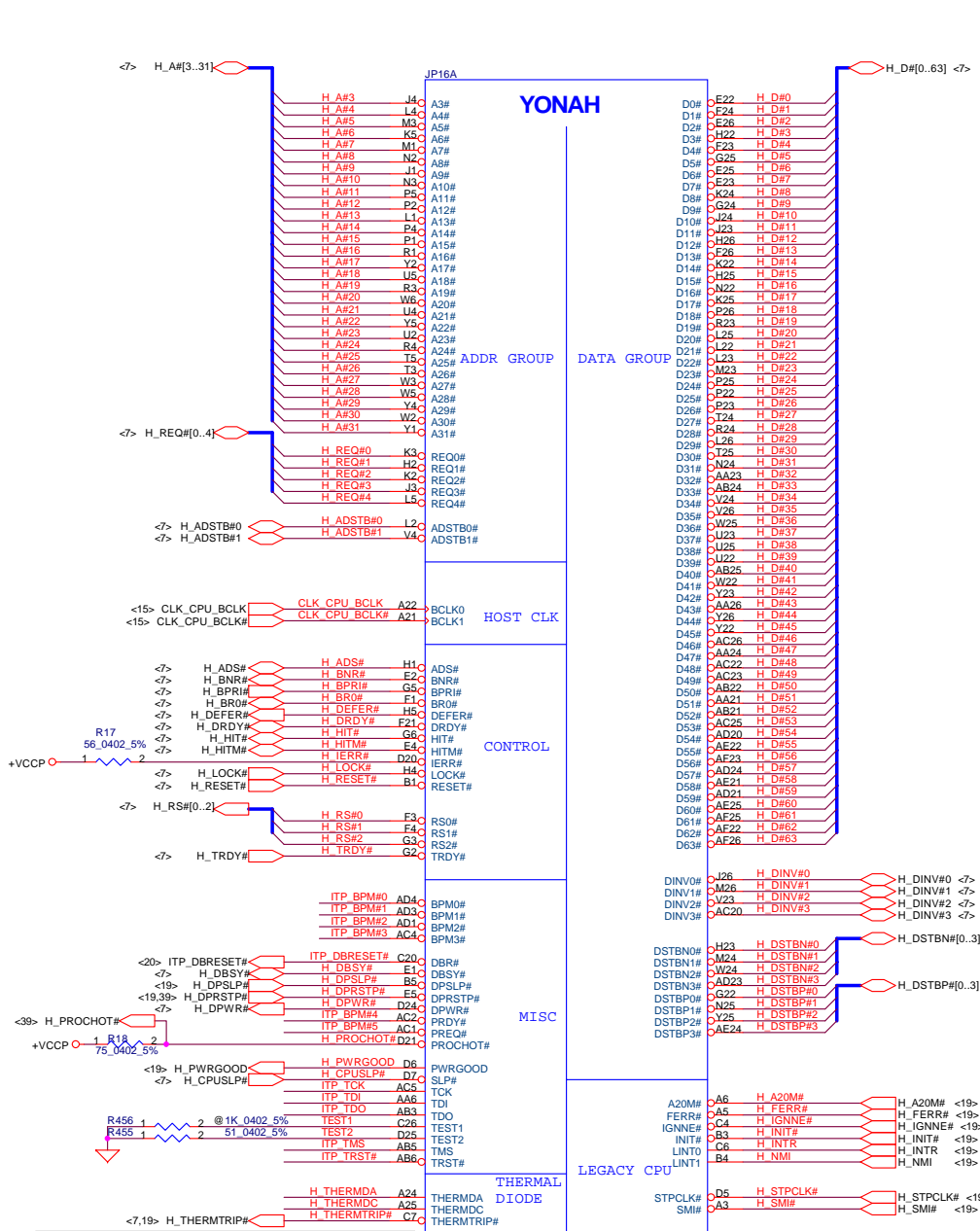
- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

BOM: 43144132L01 (GM)
43144132L02 (GML)

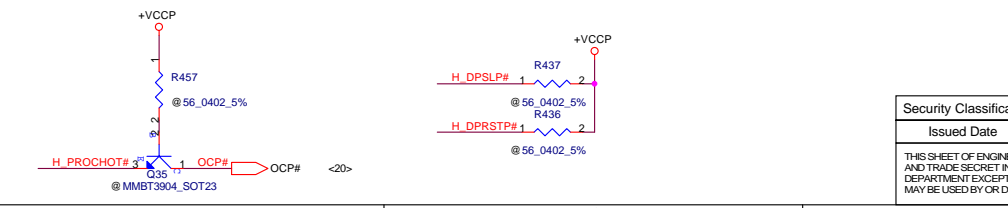
Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25

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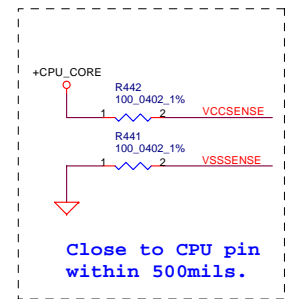
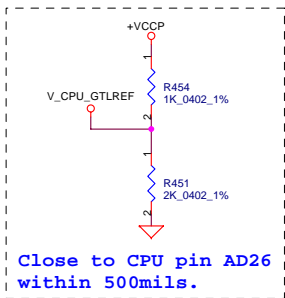
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



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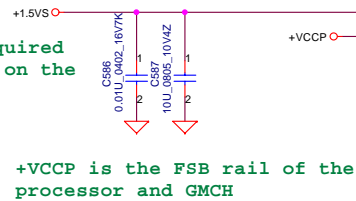
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Compal Electronics, Inc.			
Title Yonah CPU in mFCPGA479			
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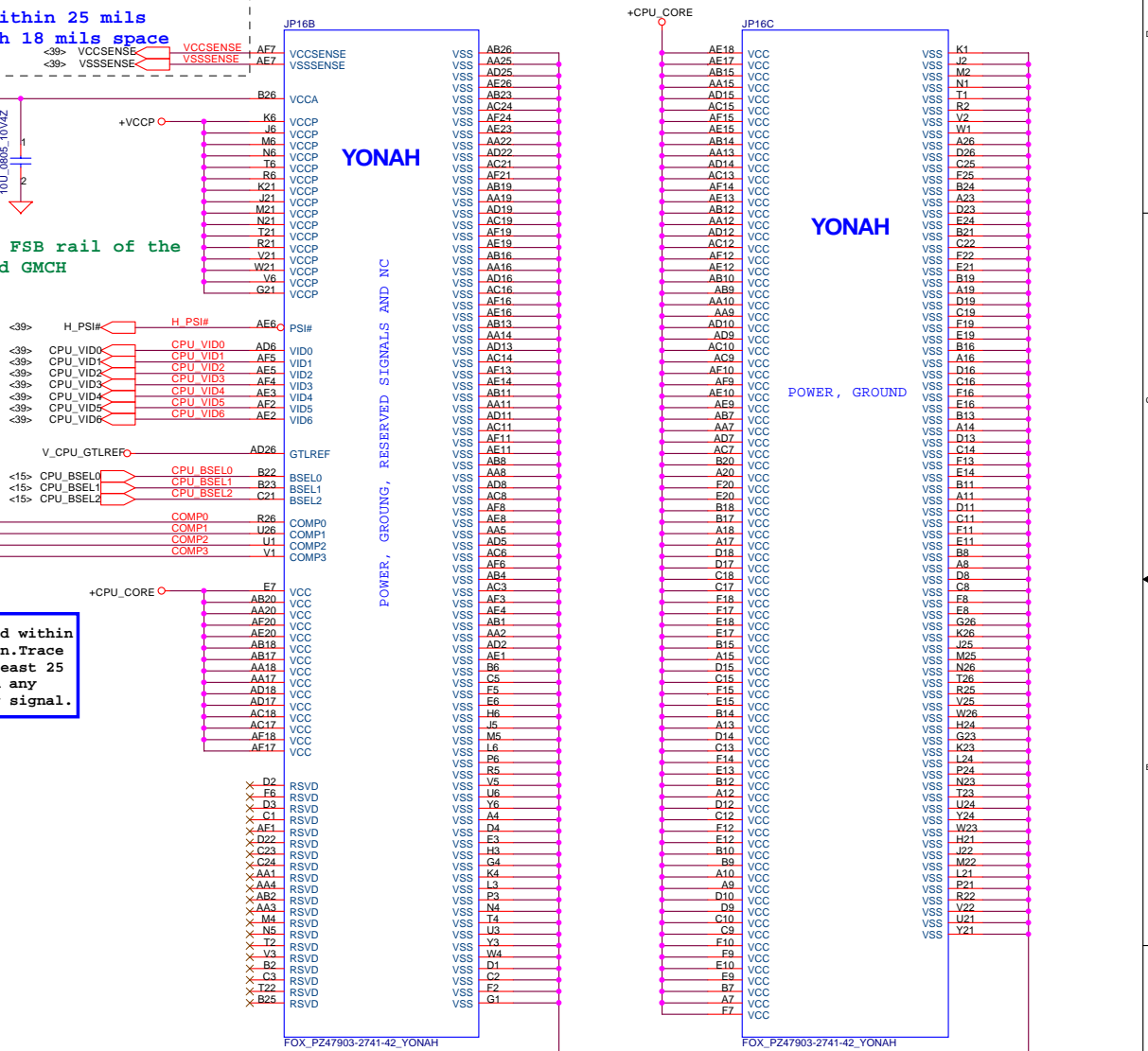
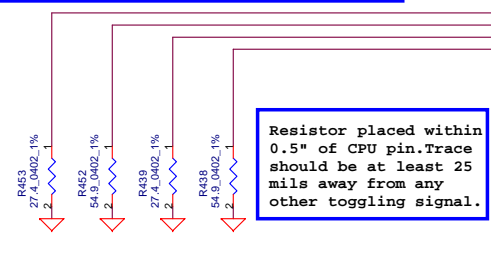


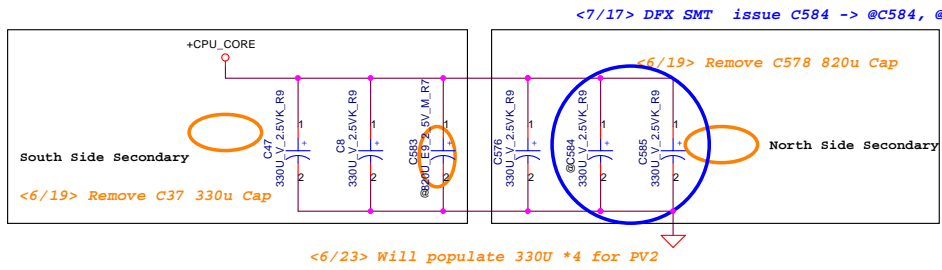
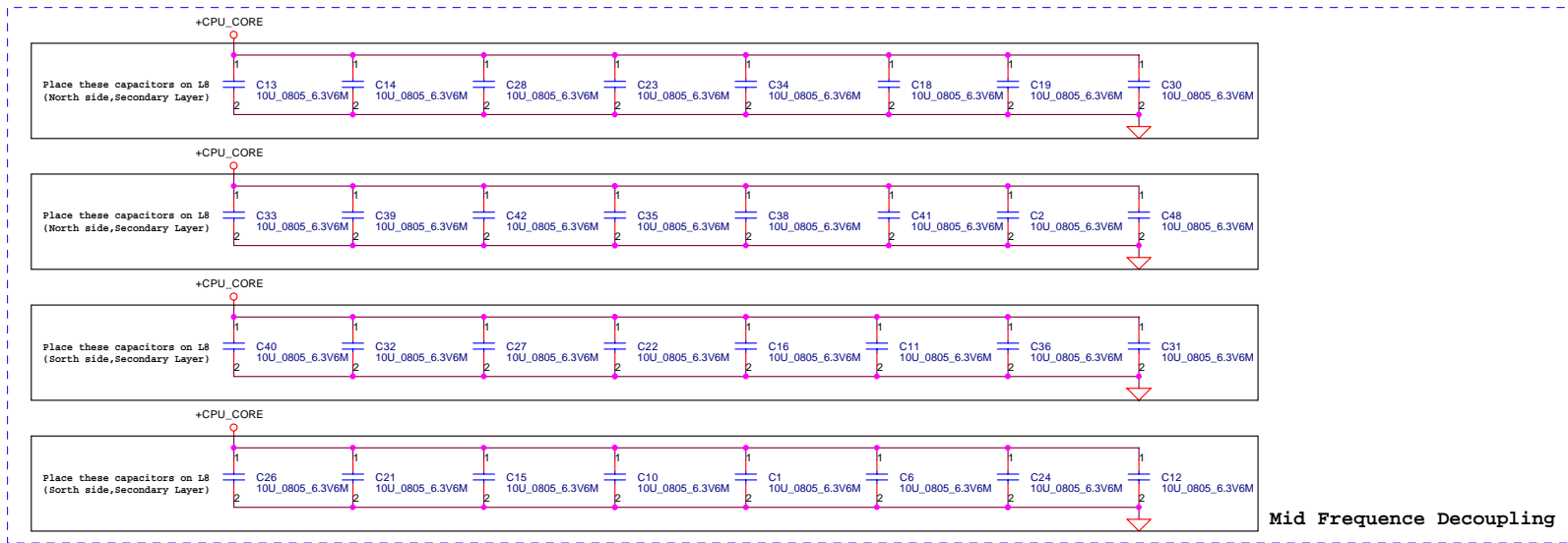
+1.5vs is a power source required by the PL clock generator on the processorsilicon

**Length match within 25 mils
The trace width 18 mils space
7 mils**

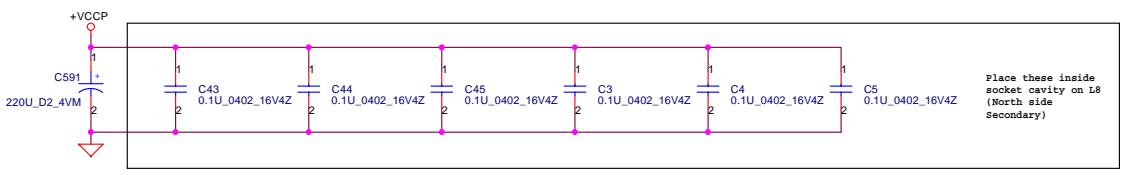


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

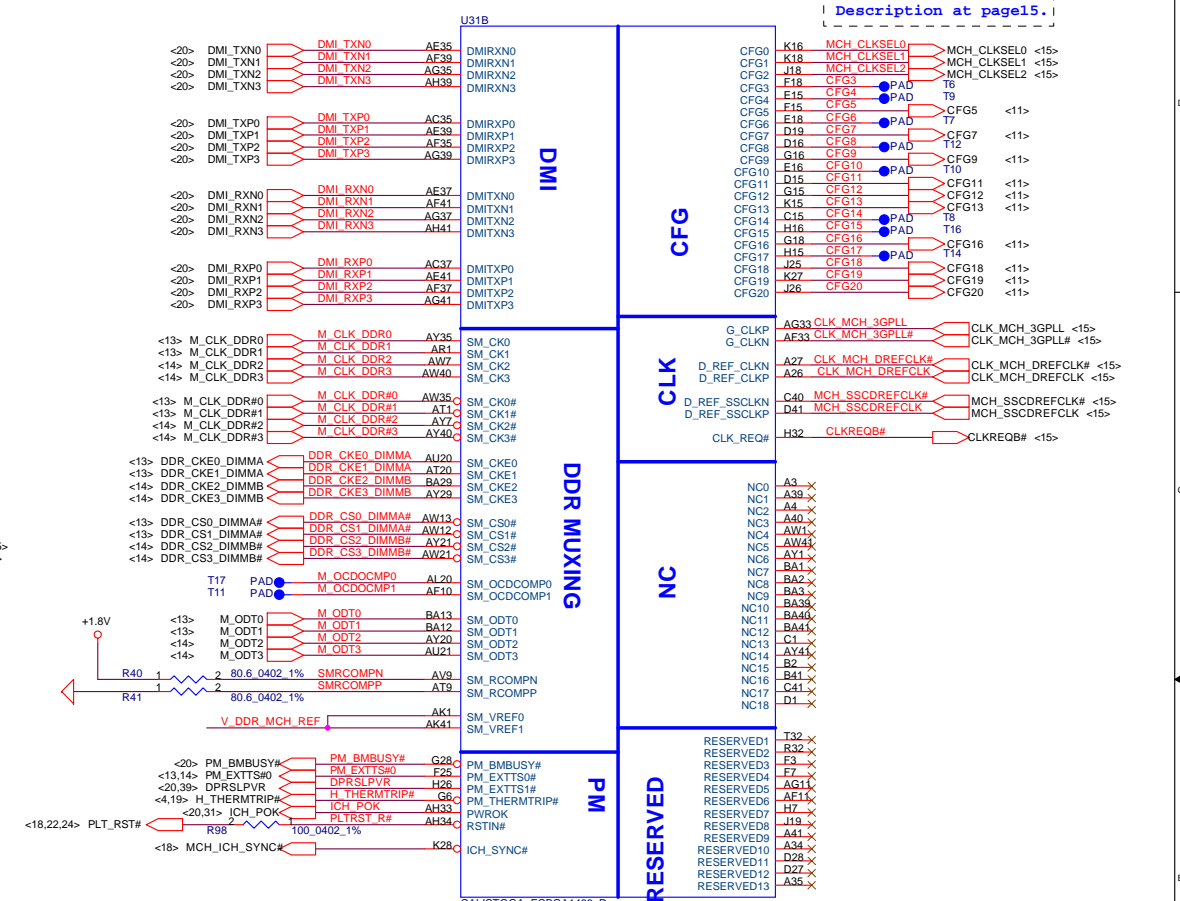
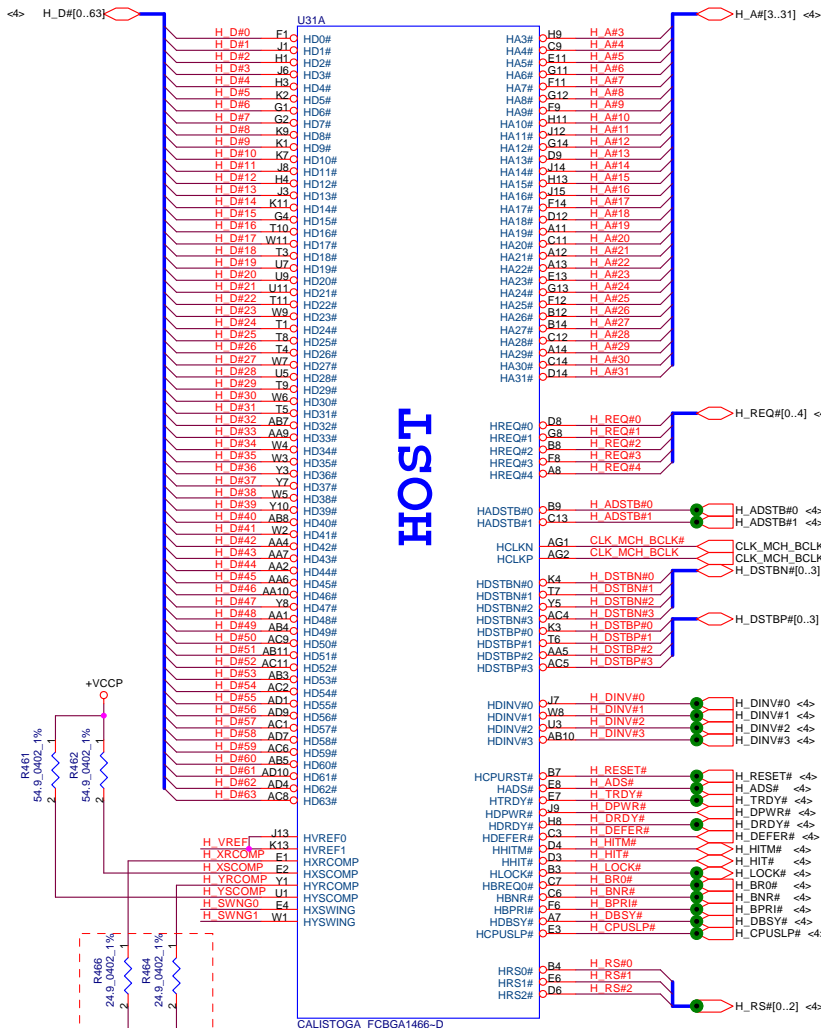




**ESR <= 1.5m ohm
Capacitor > 1980uF**



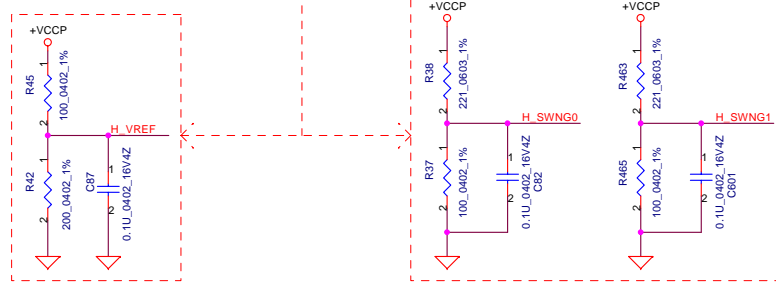
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc. CPU Bypass capacitors	
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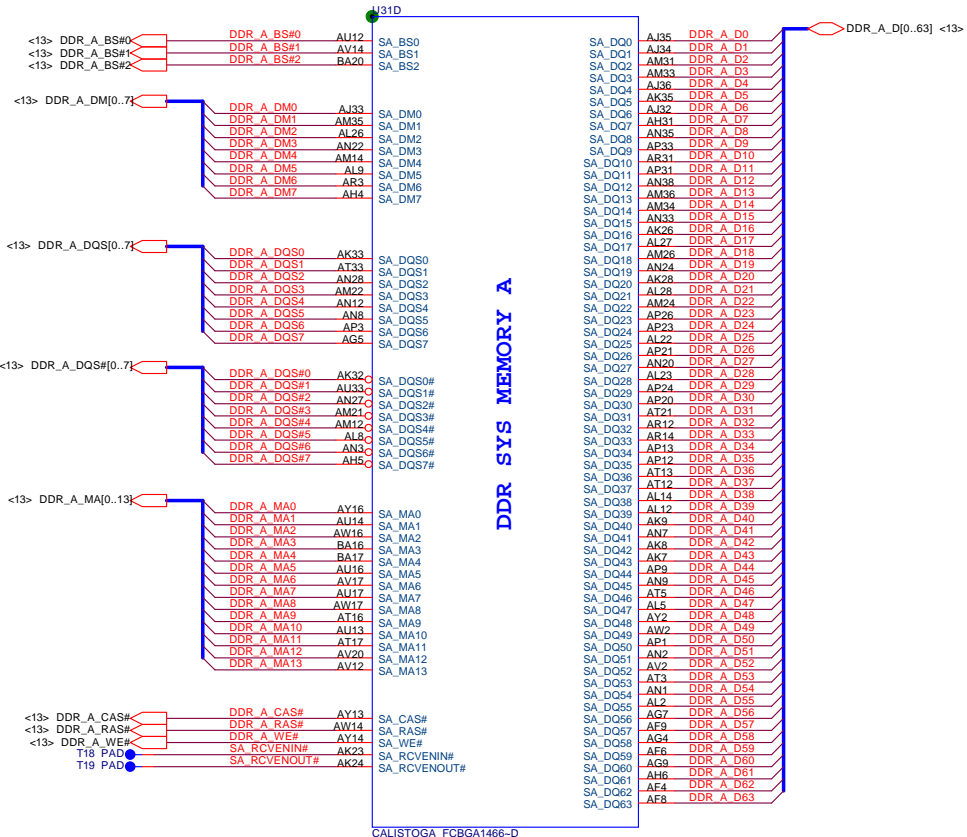
Description at page 15.

Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

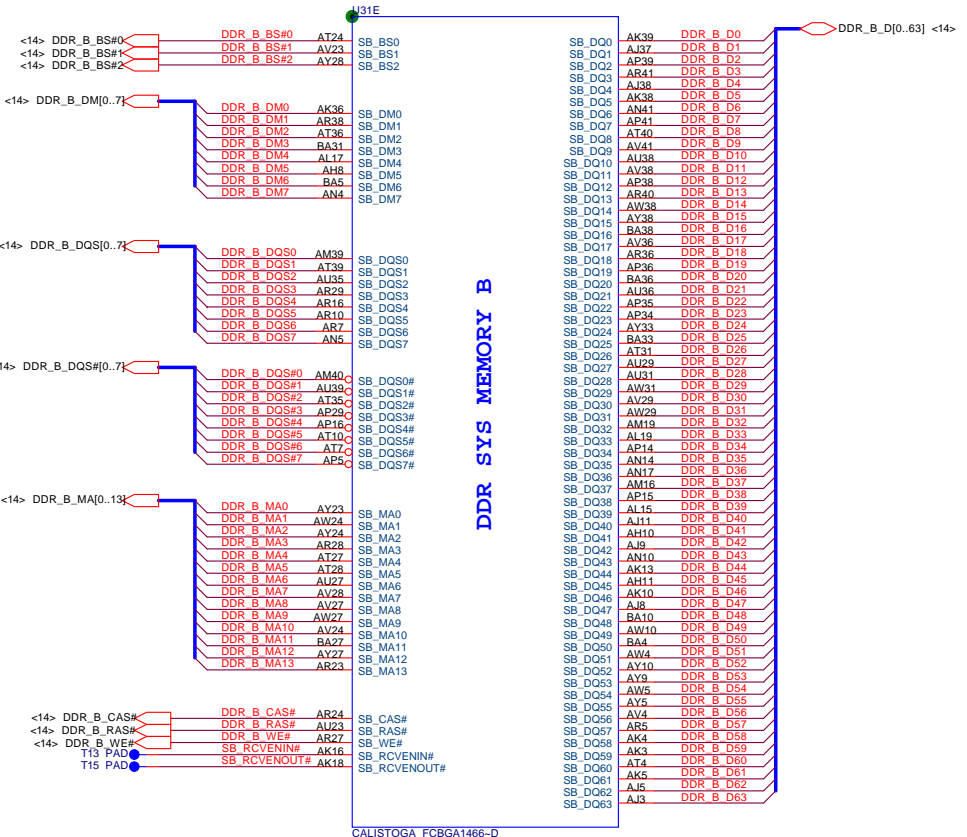
Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.



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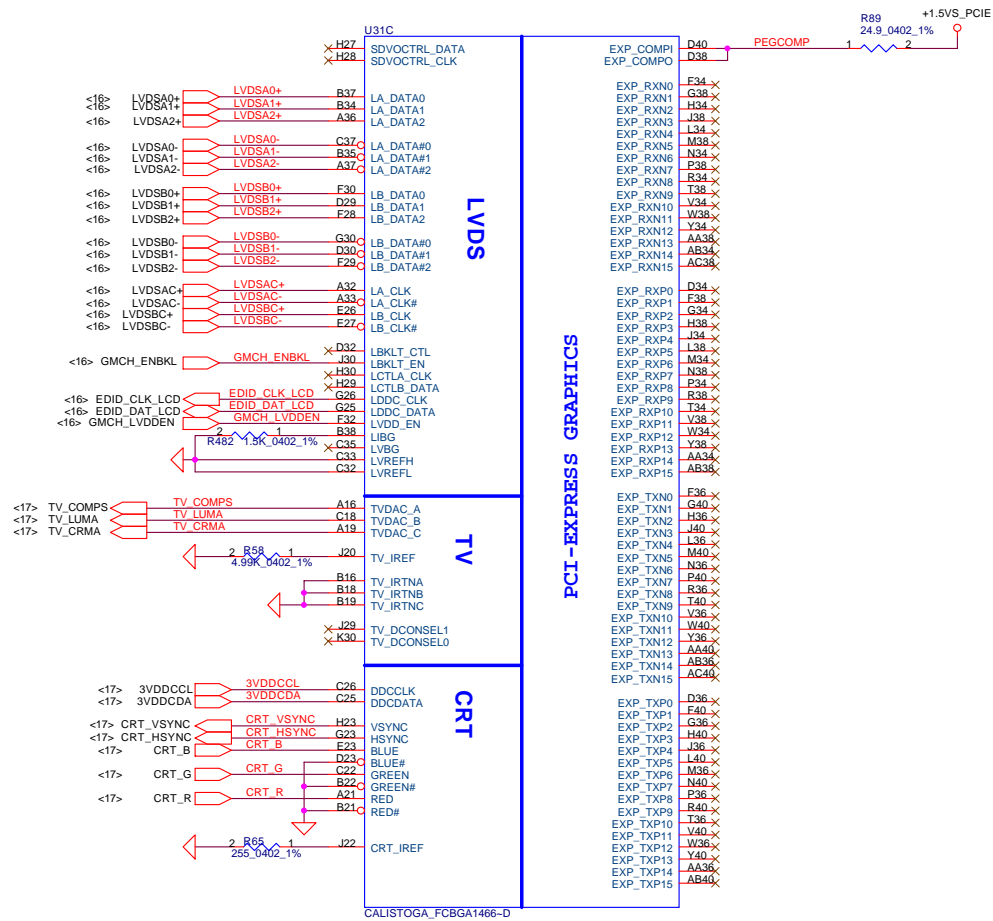


CALISTOGA_FCBGA1466-D



CALISTOGA_FCBGA1466-D

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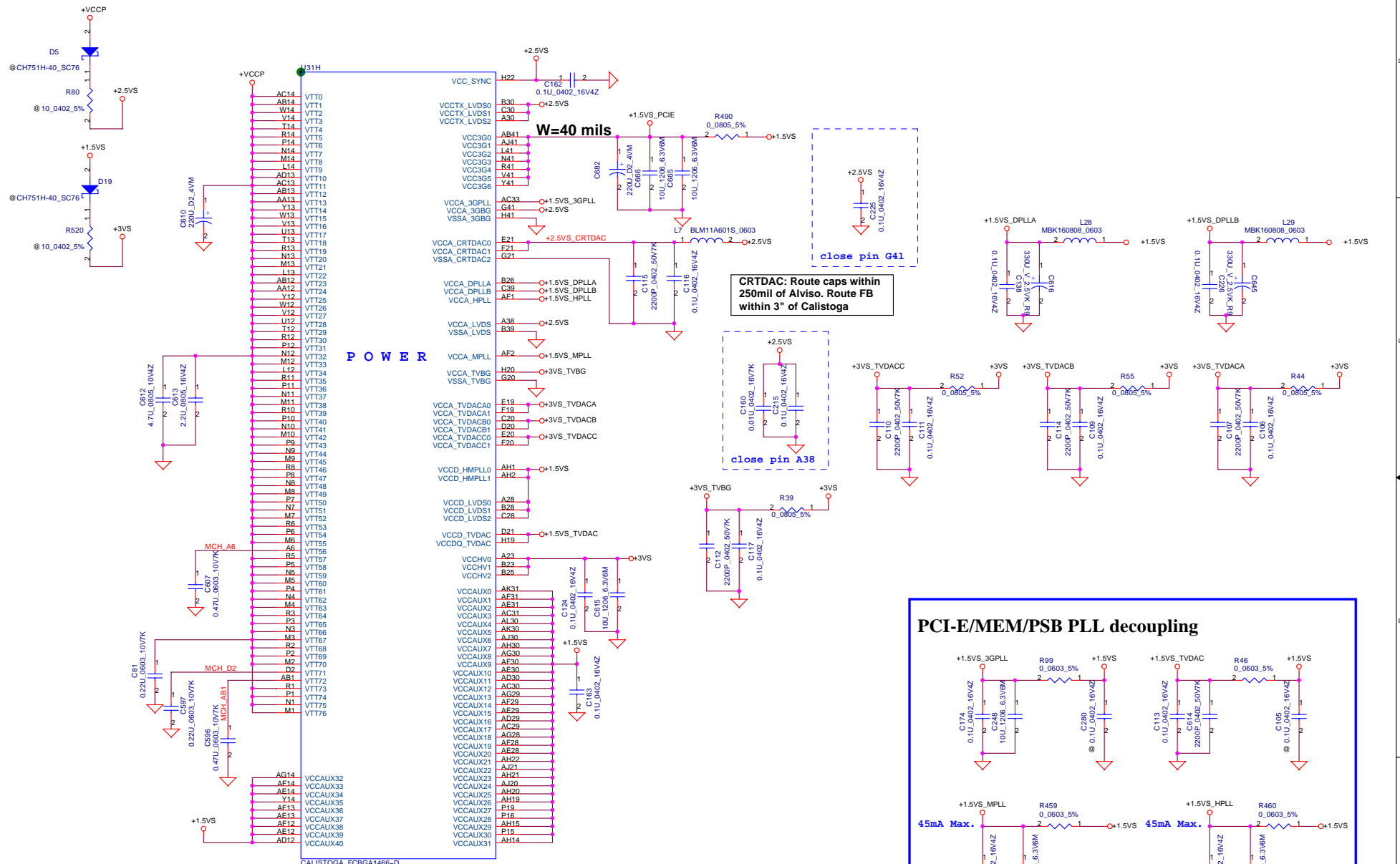


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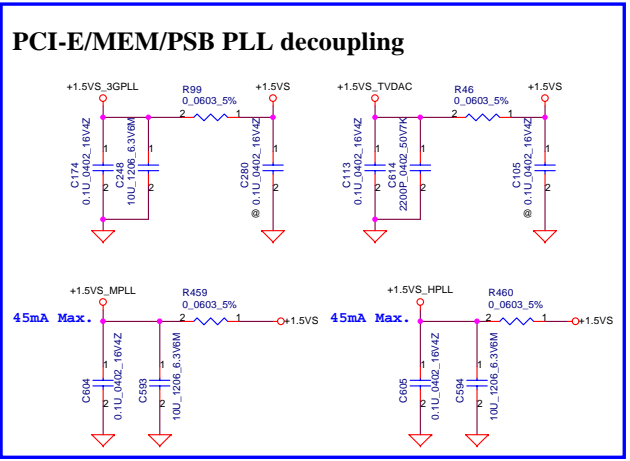
POWER

W=40 mils

CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga

close pin A38

close pin G41

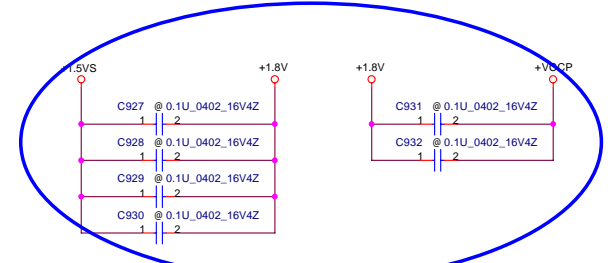
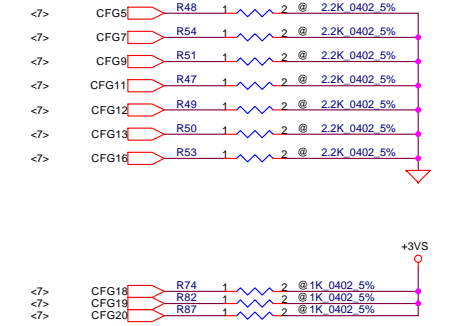
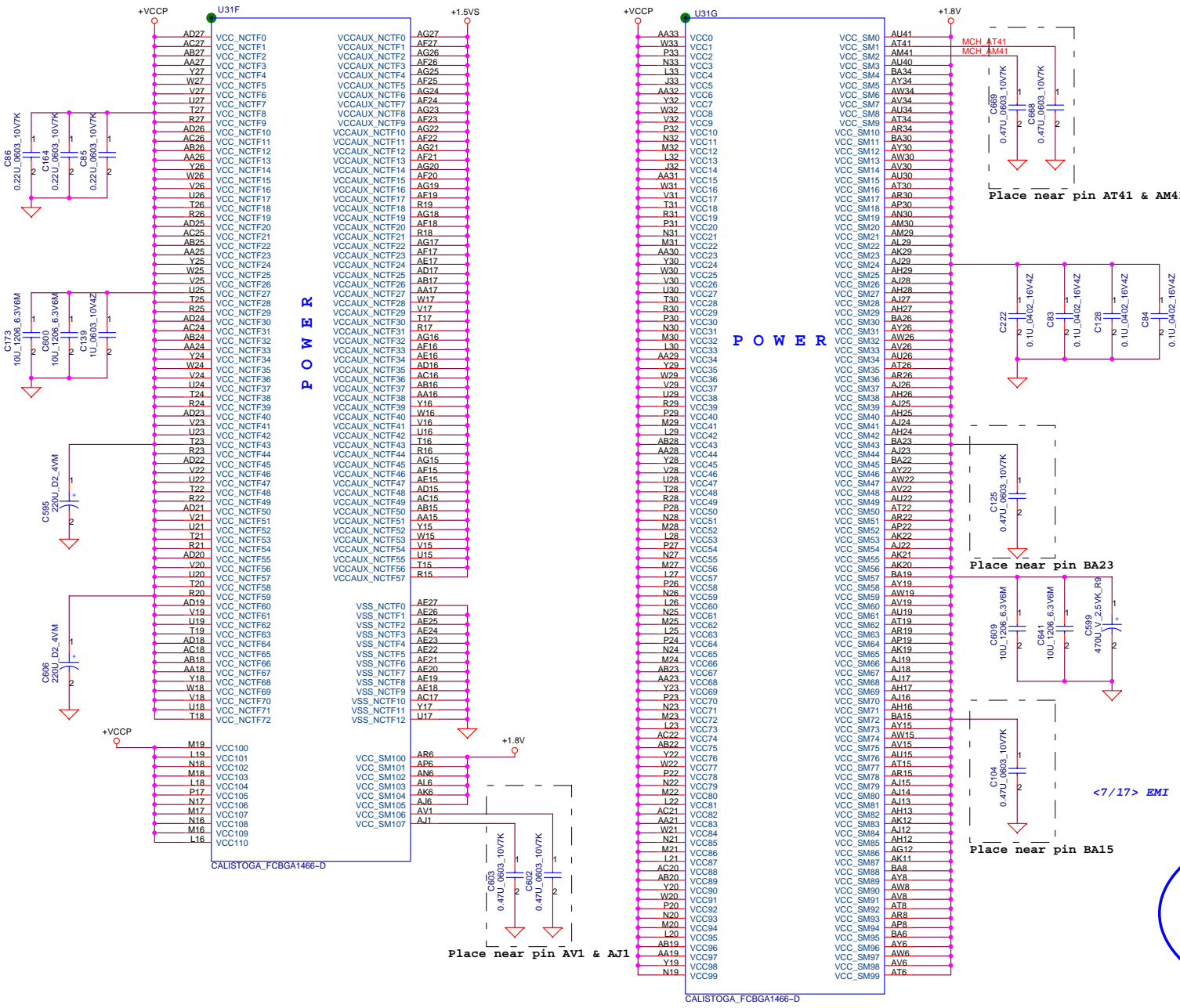


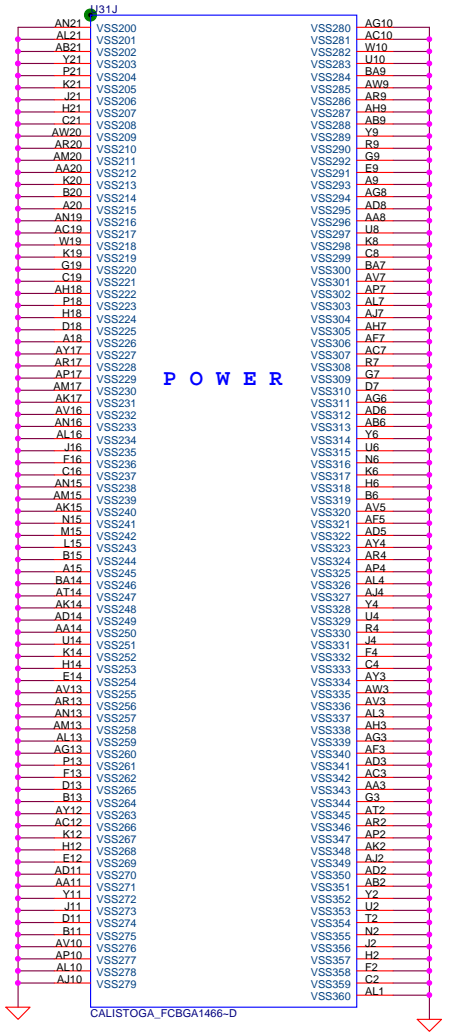
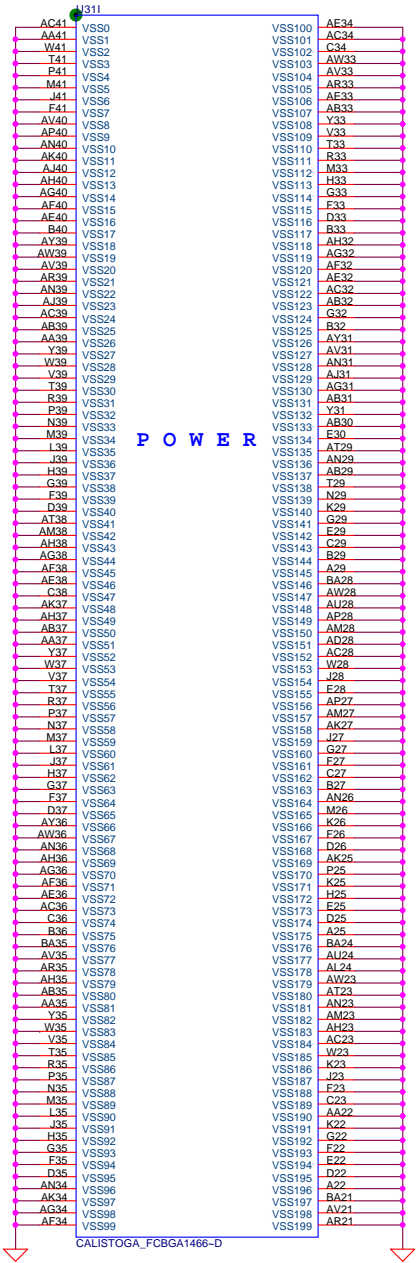
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Strap Pin Table

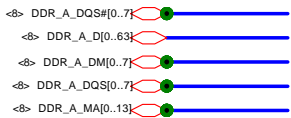
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.

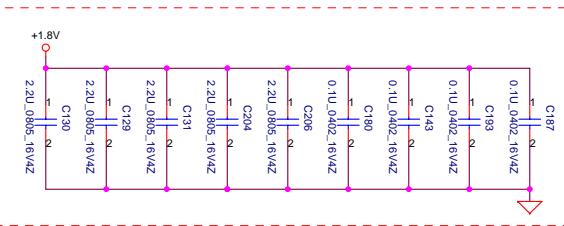




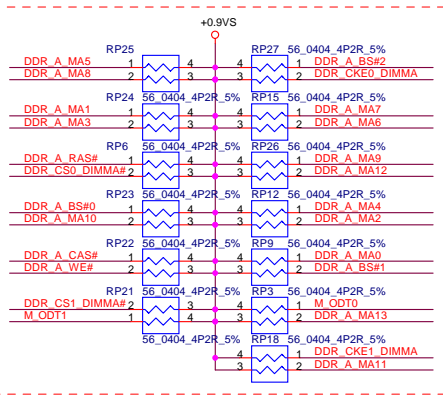
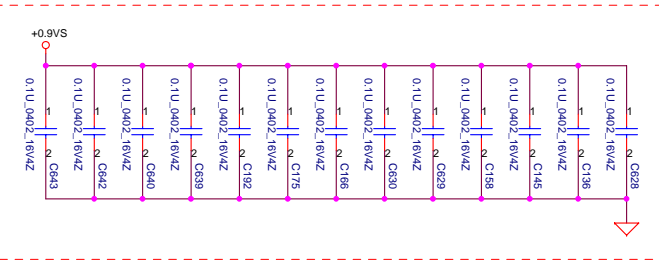
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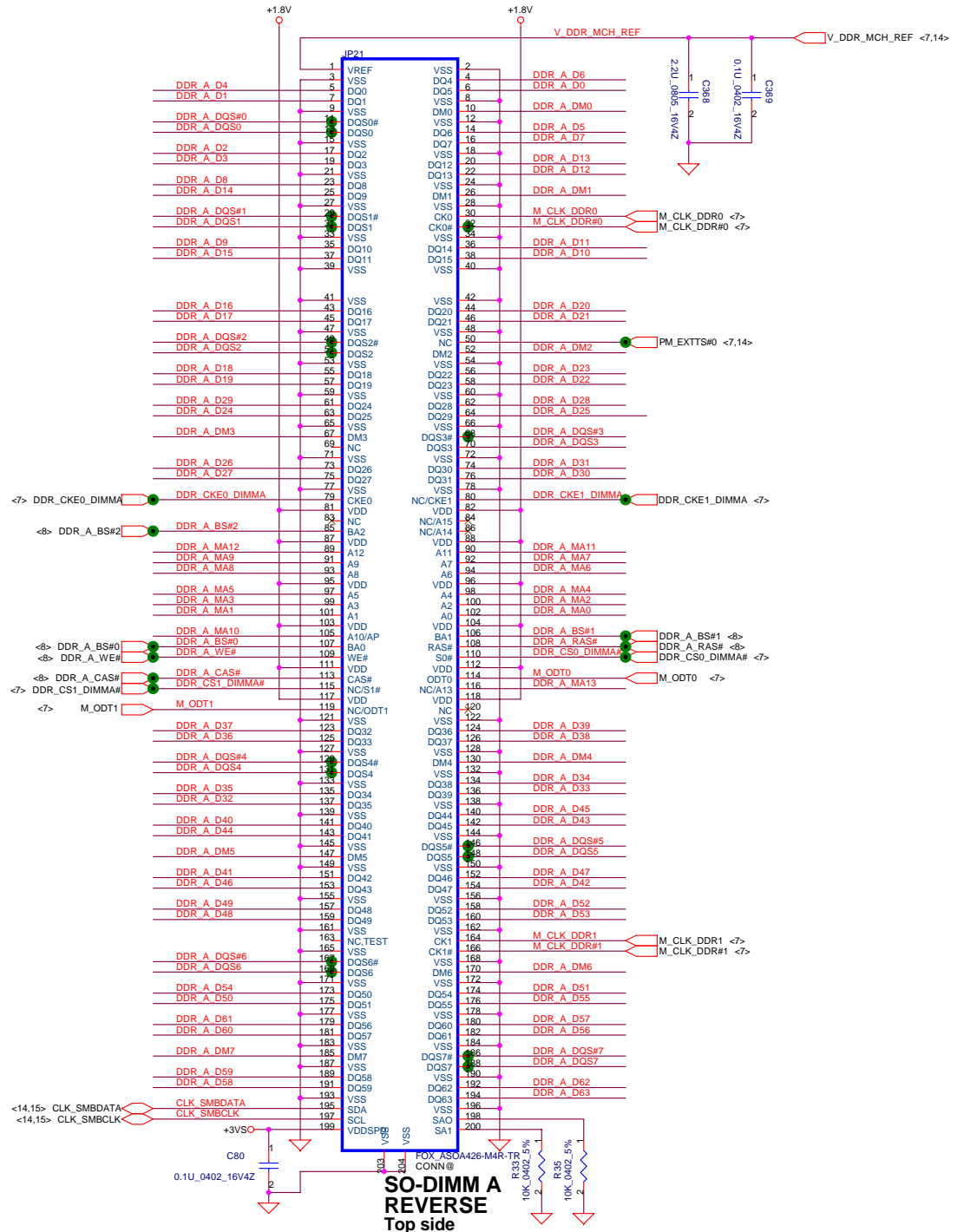
Layout Note:
Place near JP41



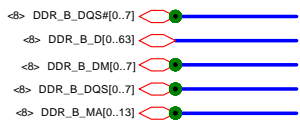
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



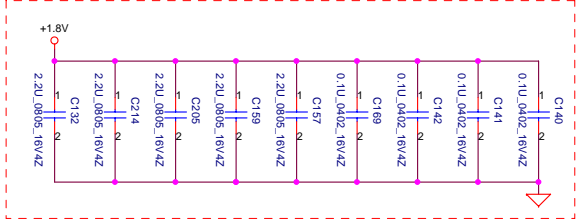
Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



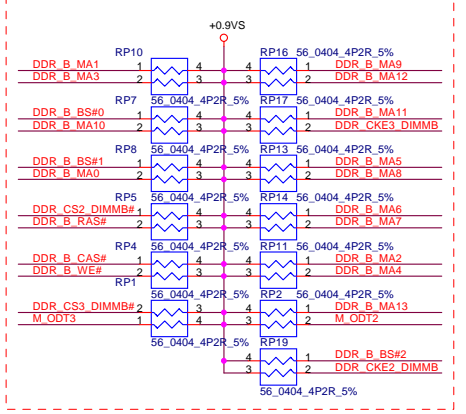
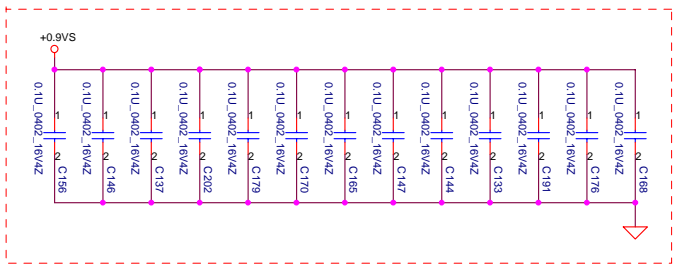
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Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



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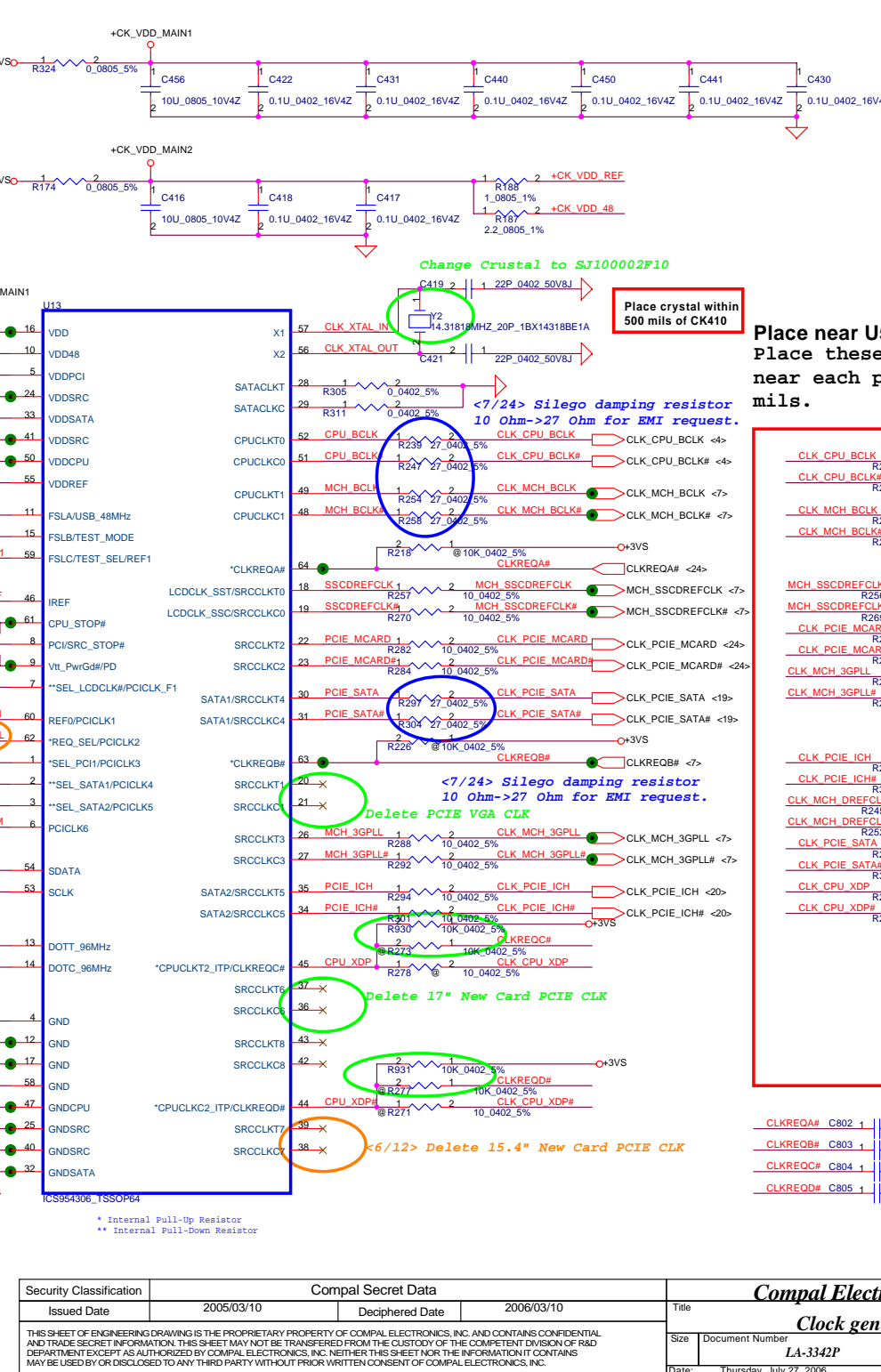
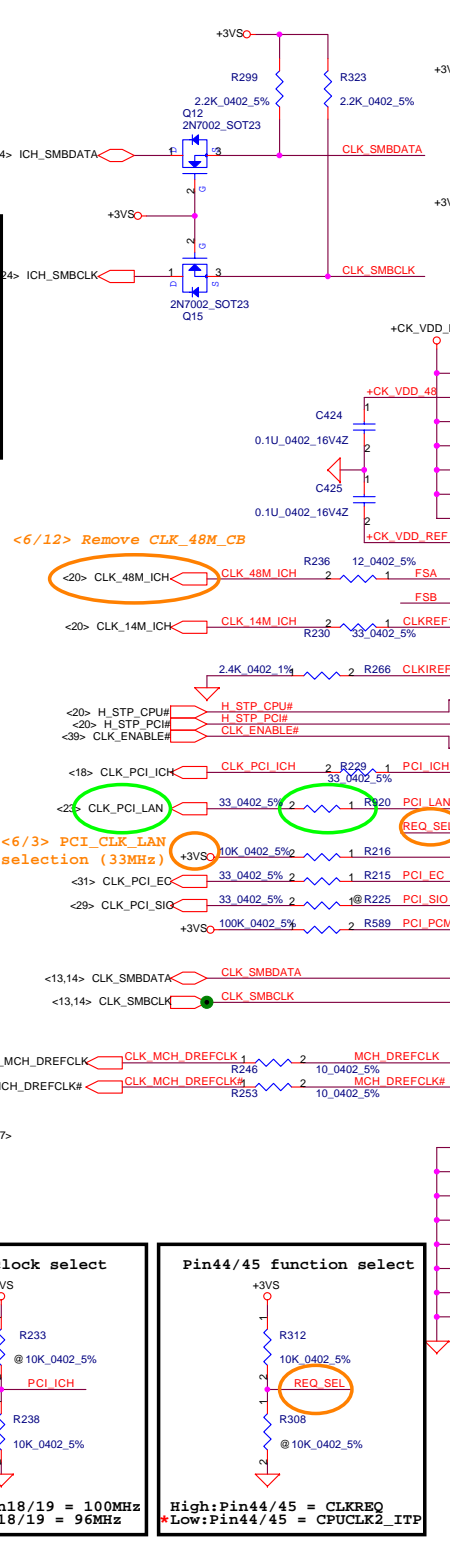
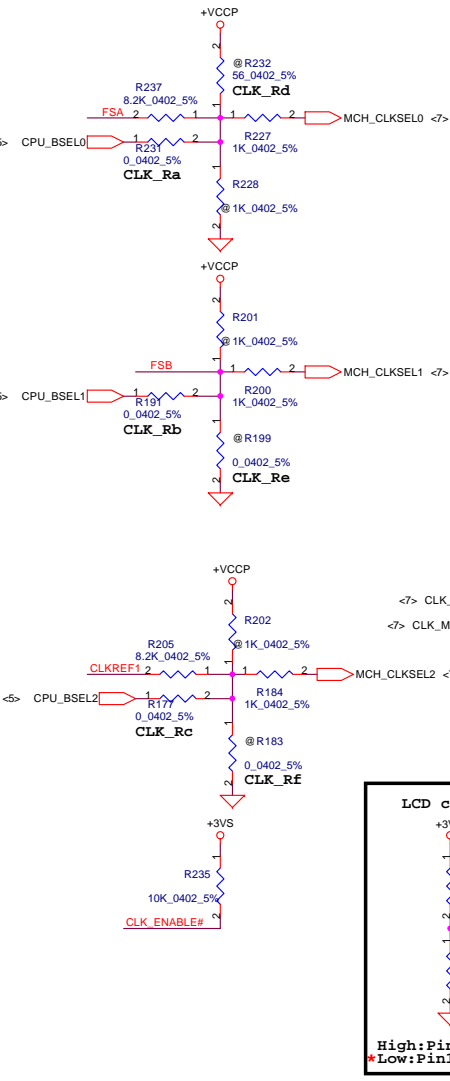
Title			
Compal Electronics, Inc.			
DDRII-SODIMM SLOT2			
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

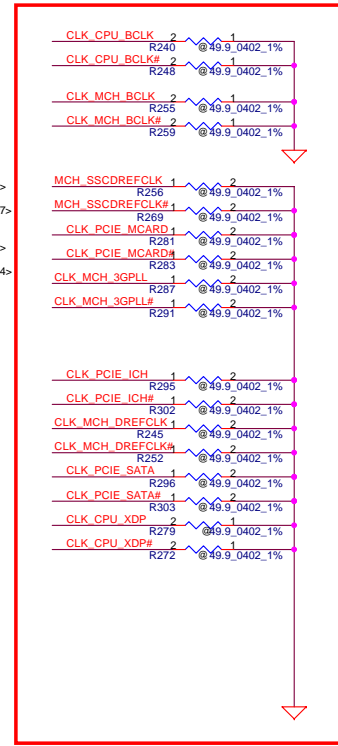
Table : ICS954306

FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



Place near U54
Place these components
near each pin within 40
mils.

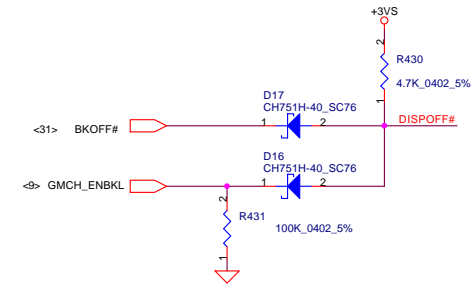
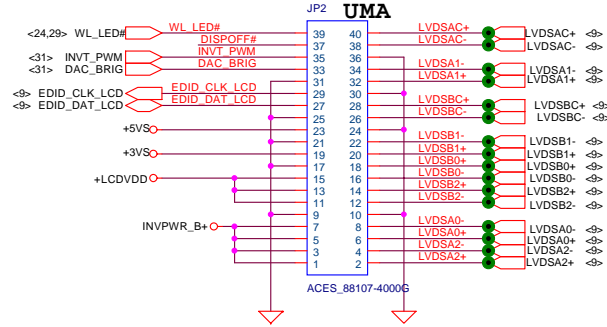
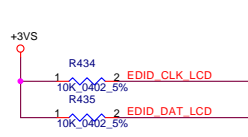


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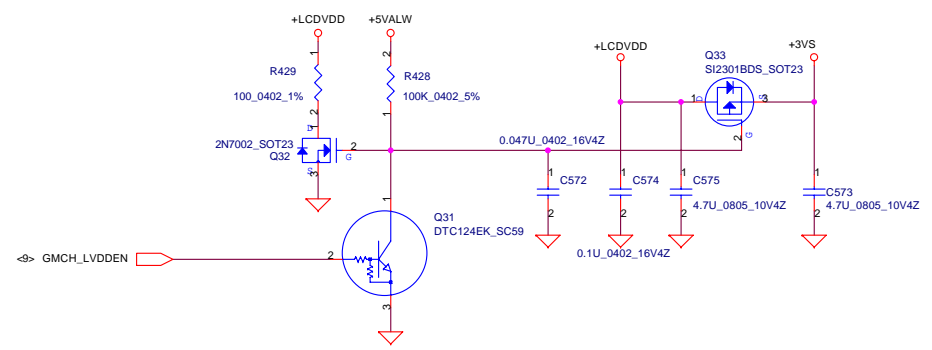
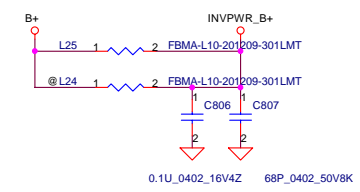
Compal Electronics, Inc.			
Clock generator			
Title	Size	Document Number	Rev
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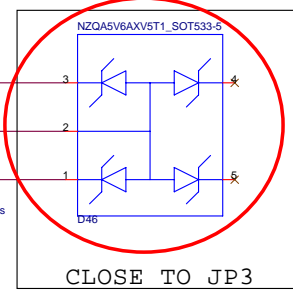
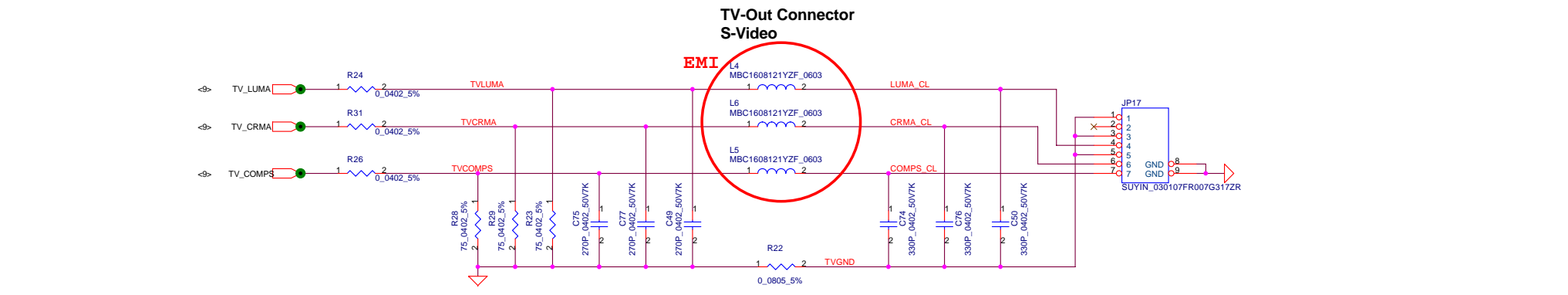
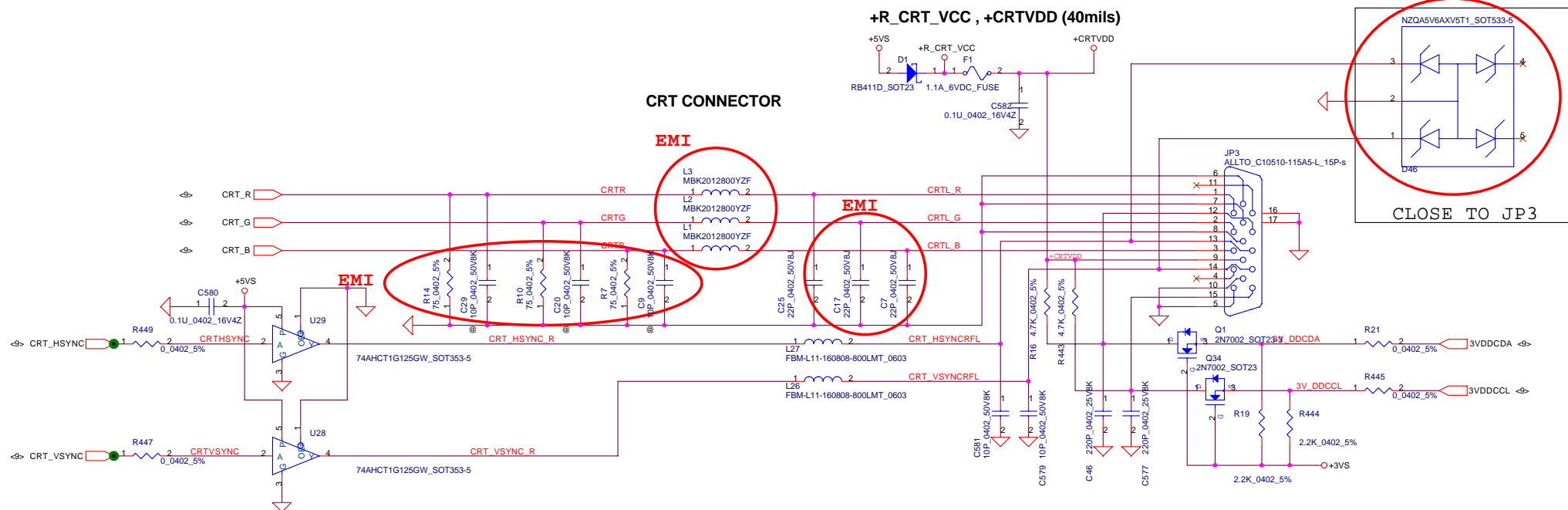
LCD Panel & inverter Connector



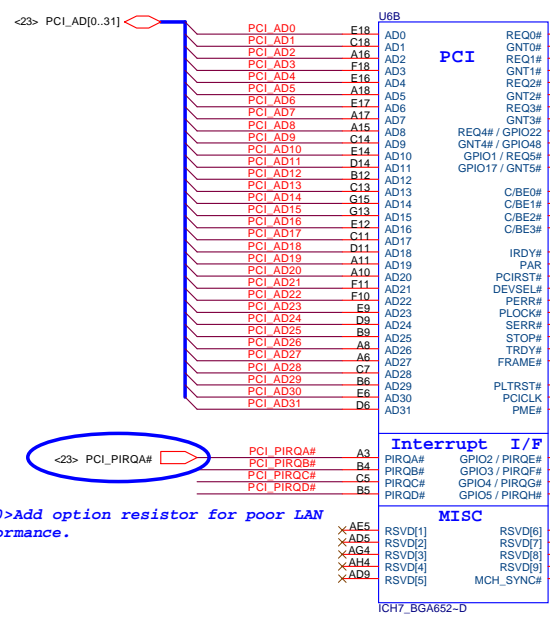
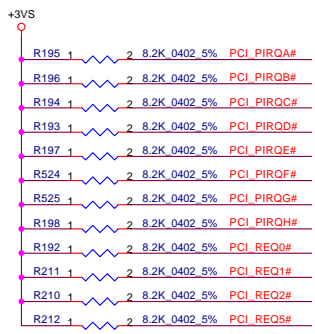
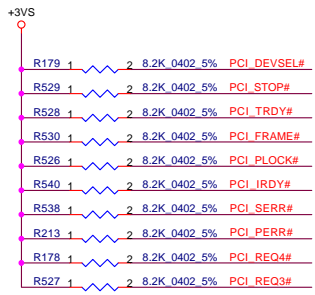
Delete 17" LVDS Conn JP1



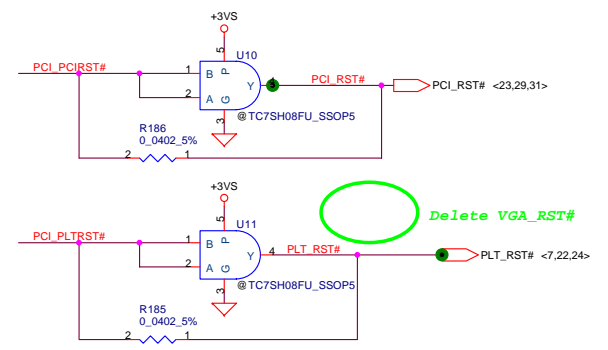
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				LA-3342P	
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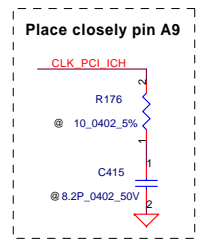
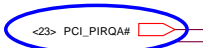


<7/20>Add option resistor for poor LAN performance.

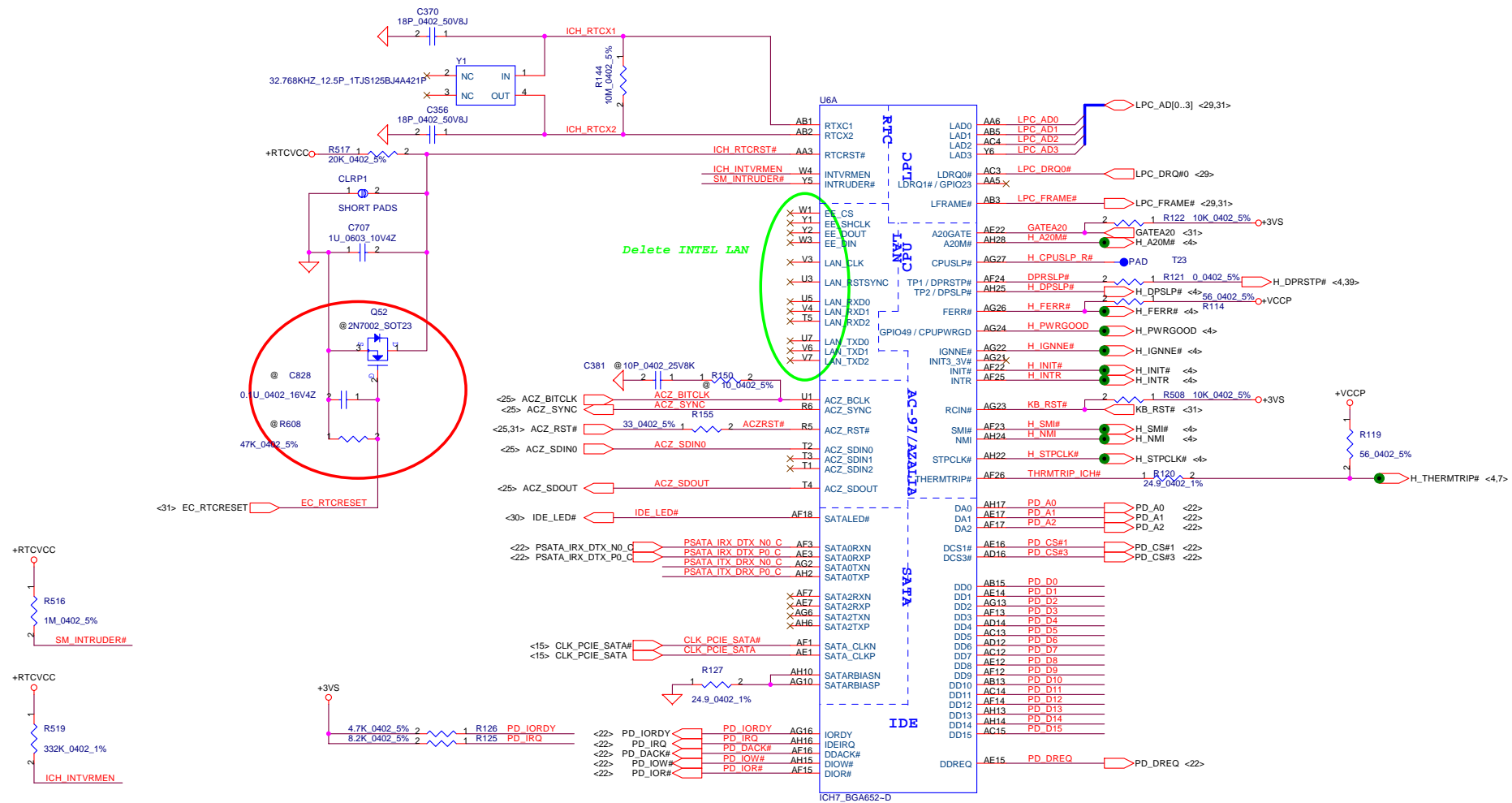


Delete VGA_RST#

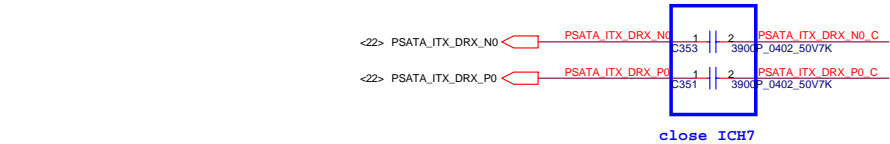
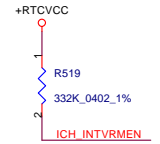
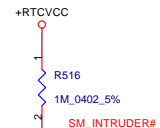
<7/20>Add option resistor for poor LAN performance.



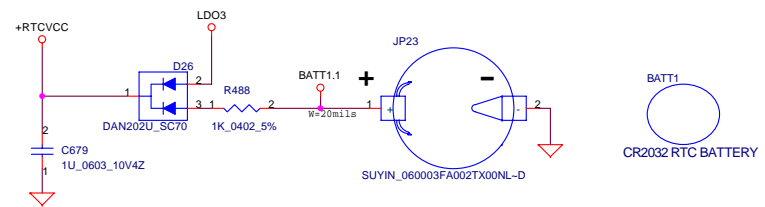
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Delete INTEL LAN

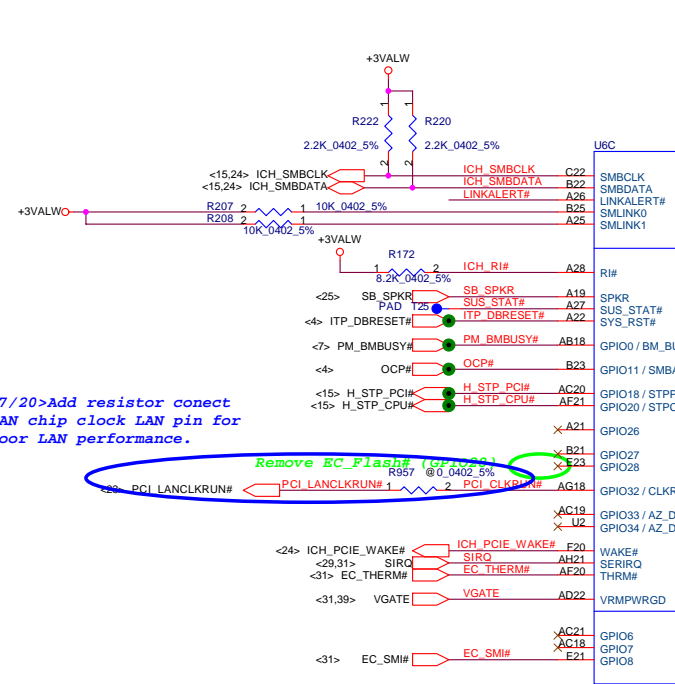
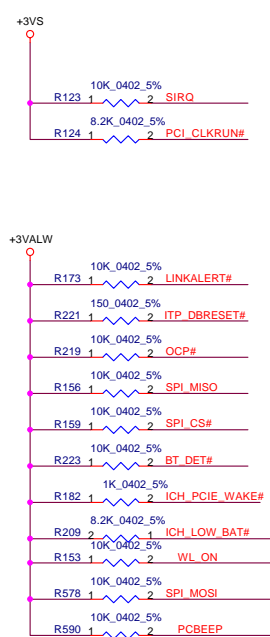


close ICH7



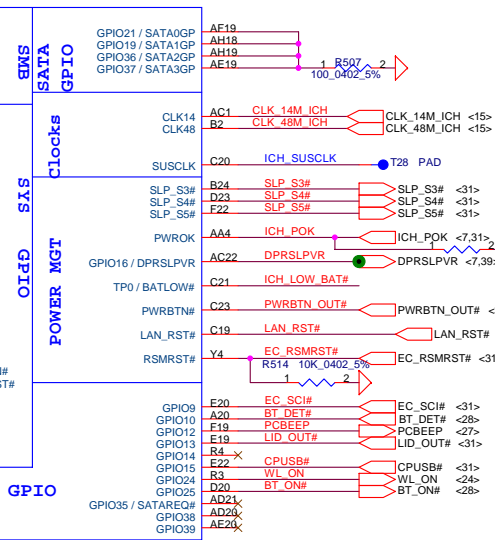
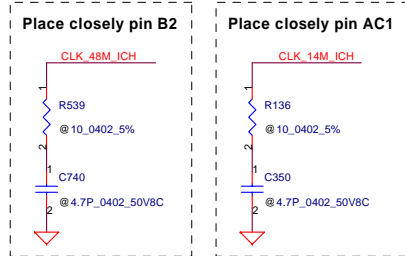
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Issued Date	2005/03/10	Deciphered Date
		2006/03/10
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ICH7-M(2/4)	
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<7/20> Add resistor connect LAN chip clock LAN pin for poor LAN performance.

Remove EC Flash# (C31220) @ 0.0402 5%
 PCI LANCLKRUN# 1 2 PCI CLKRUN#

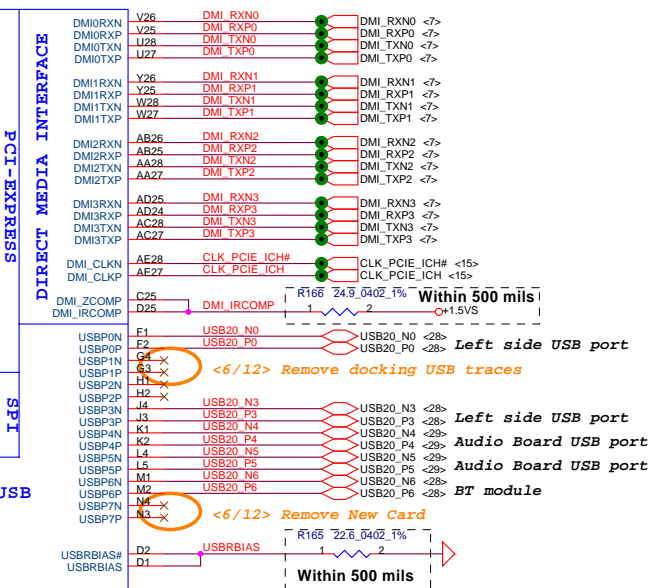
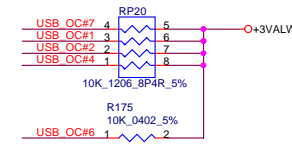
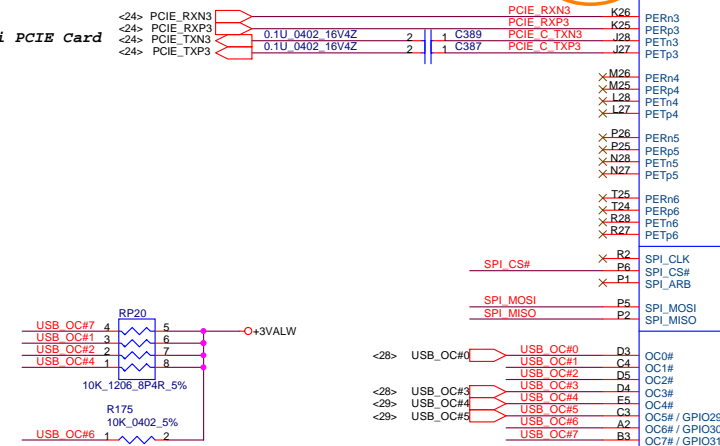


Need update symbol

Delete 17" New Card PCIE traces

<6/20> Remove New Card trace

To mini PCIE Card



Within 500 mils

<6/12> Remove docking USB traces

Left side USB port

Left side USB port

Audio Board USB port

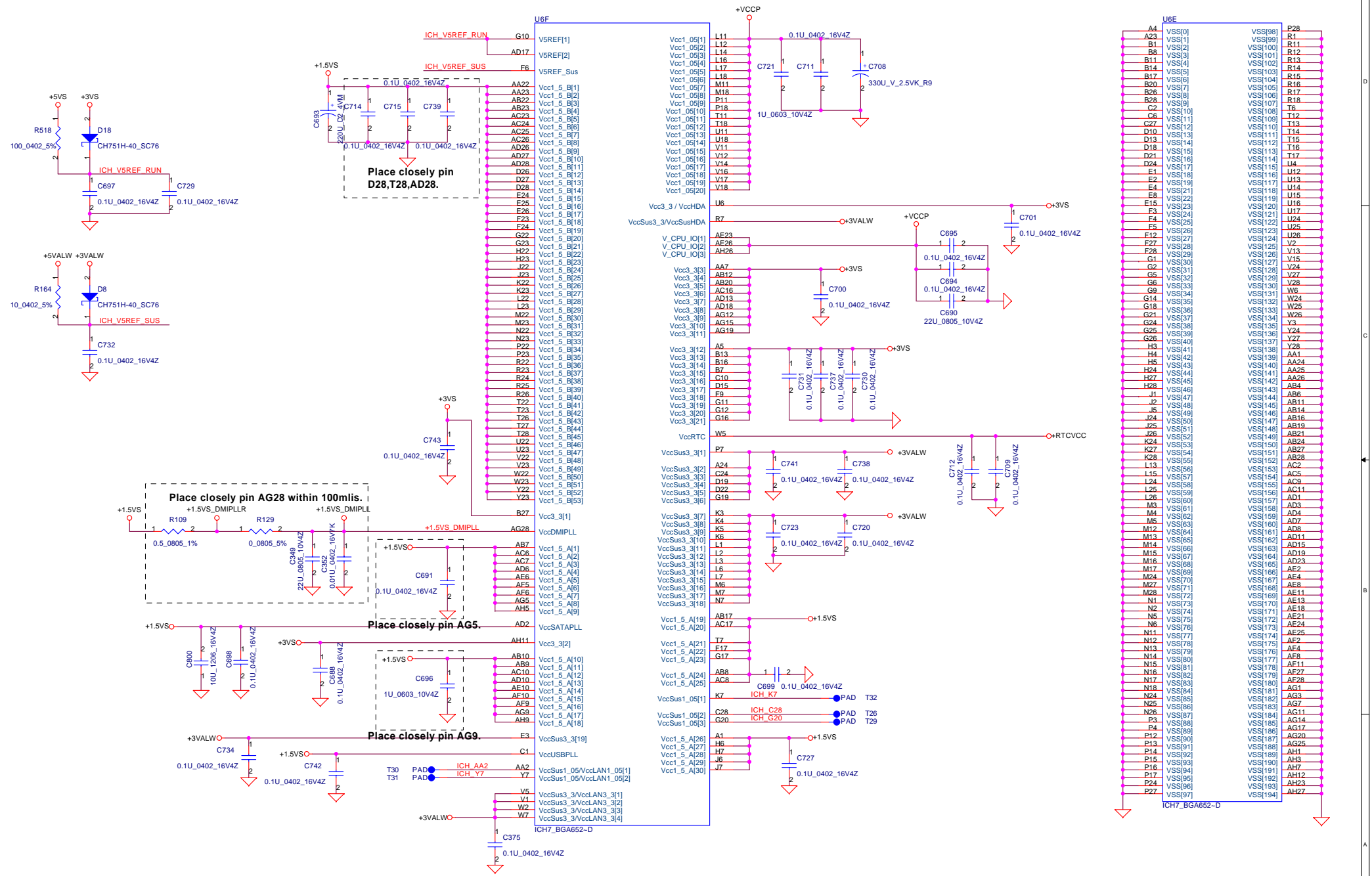
Audio Board USB port

BT module

<6/12> Remove New Card

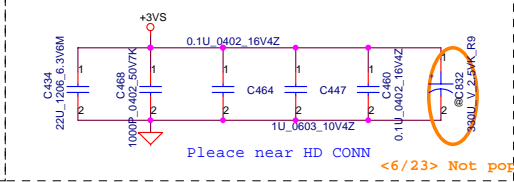
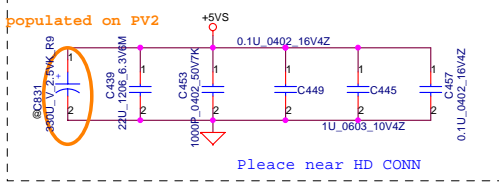
Within 500 mils

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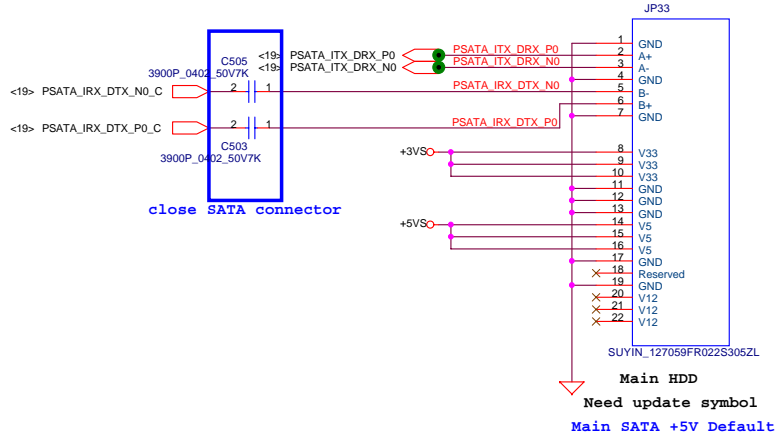


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<6/23> Not populated on PV2

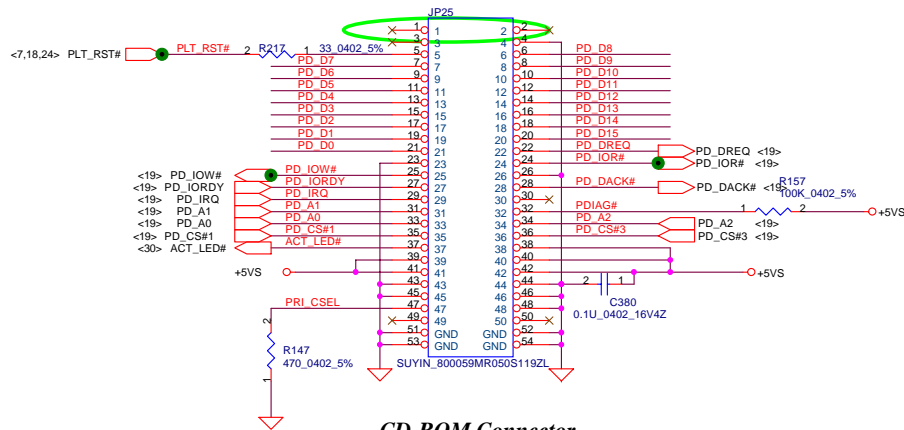


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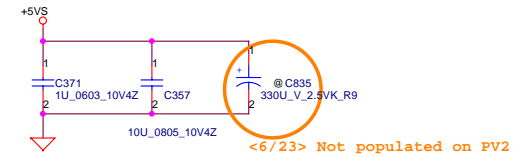


PD_D[0..15] PD_D[0..15] <19>

Delete CD traces (JP25 pin1,2 and3)



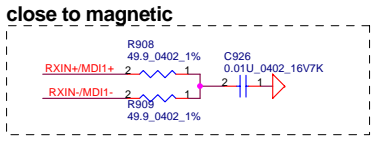
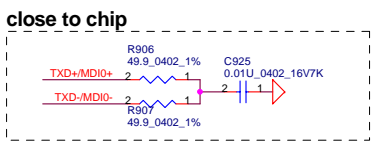
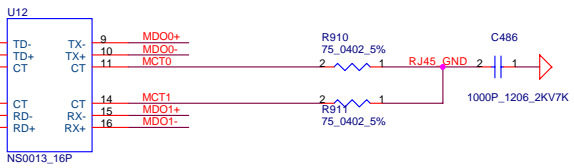
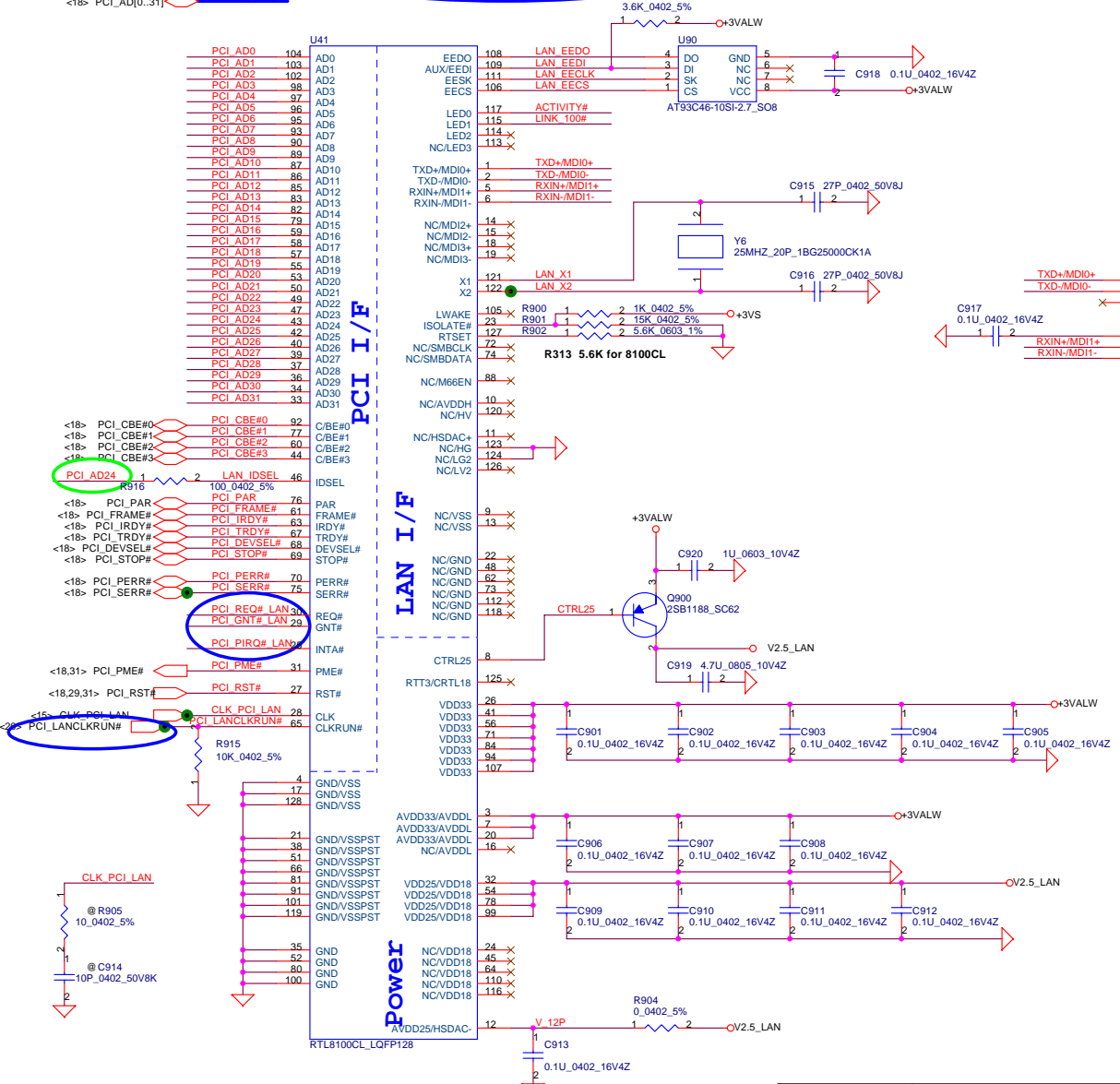
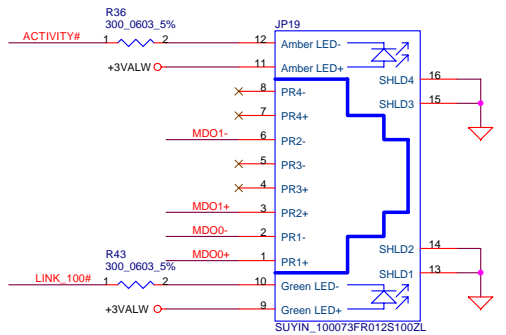
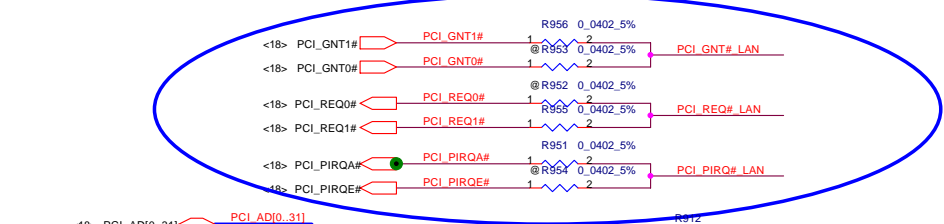
CD-ROM Connector



<6/23> Not populated on PV2

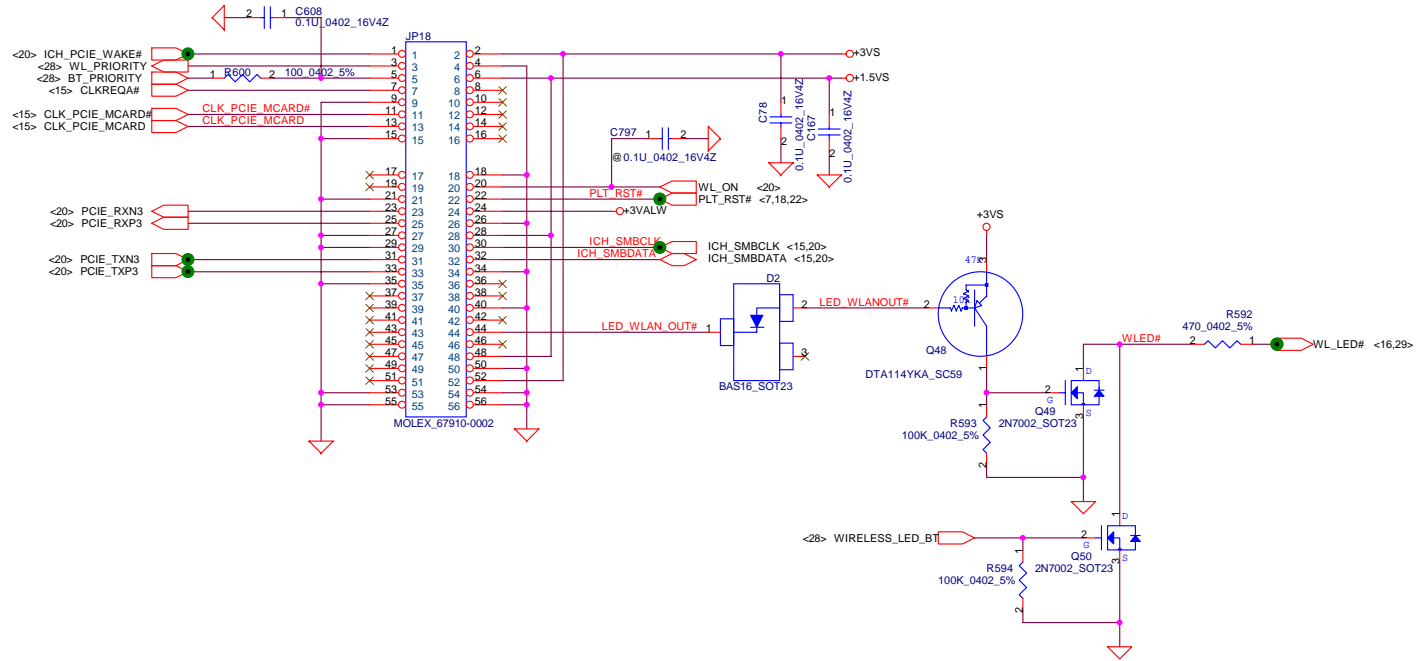
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HDD & CDROM		
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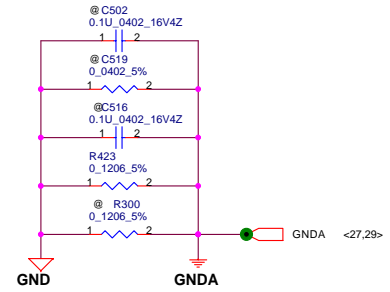
Mini-Express Card(Slot 1-WLAN)



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<6/12> Remove PCM_SPK

For Layout:
Place decoupling caps near the power pins of SmartAMC device.



Delete CD traces

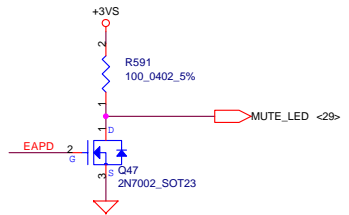
<6/12> Remove Docking line out

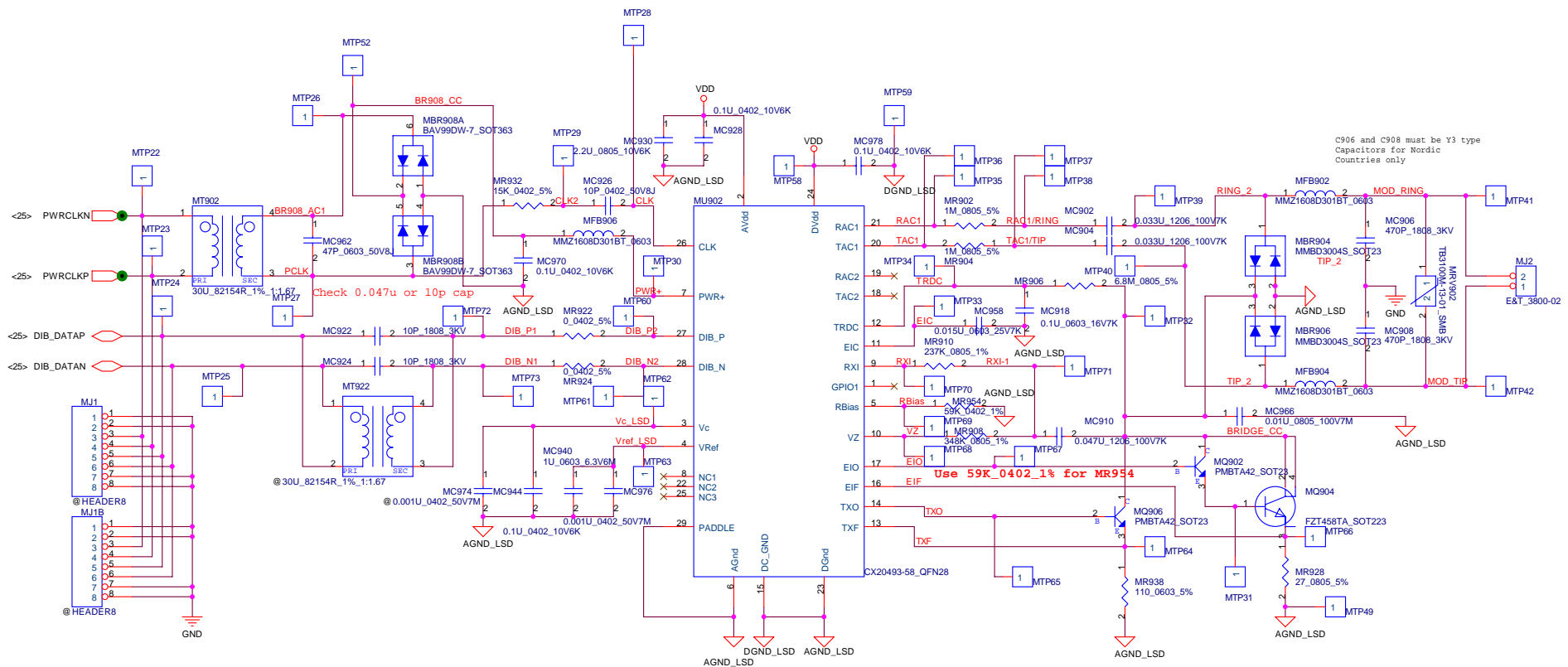
<6/12> Remove Docking MIC

<6/12> Remove JACK_DET from Docking

HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

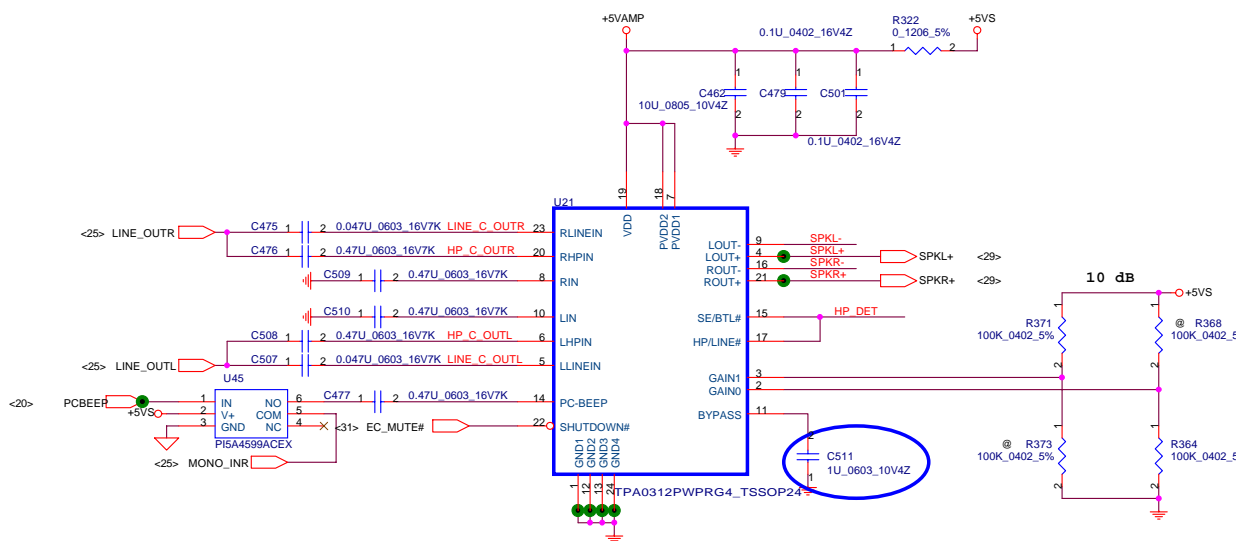
MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON





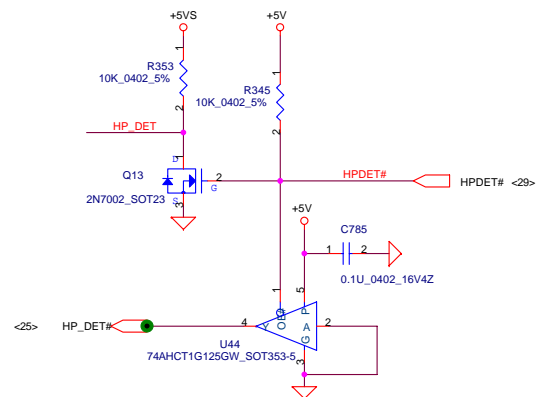
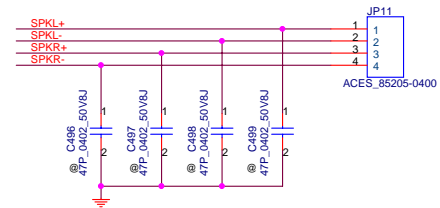
C906 and C908 must be Y3 type Capacitors for Nordic Countries only

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				AMOM modem		
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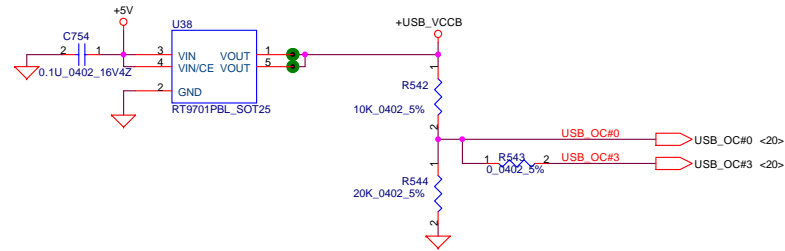


HEADPHONE OUT/LINE OUT

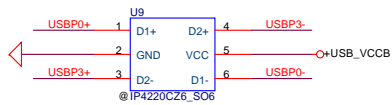
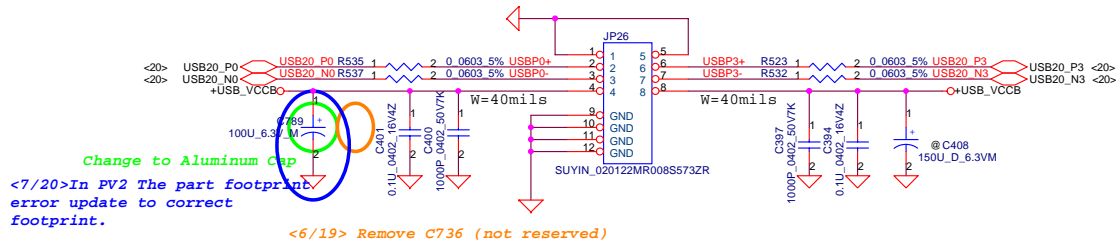
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av (inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



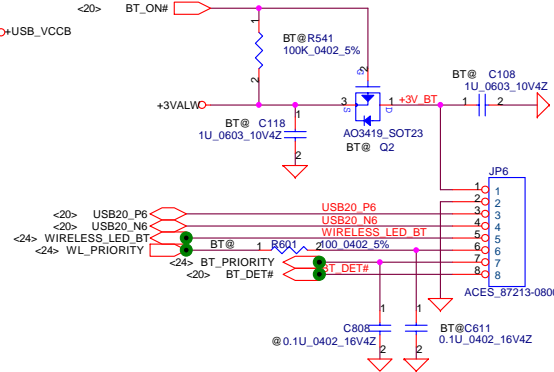
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title AMP & Audio Jack
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USB CONNECTOR (Left side)

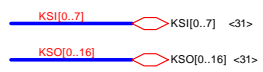


BT CONNECTOR

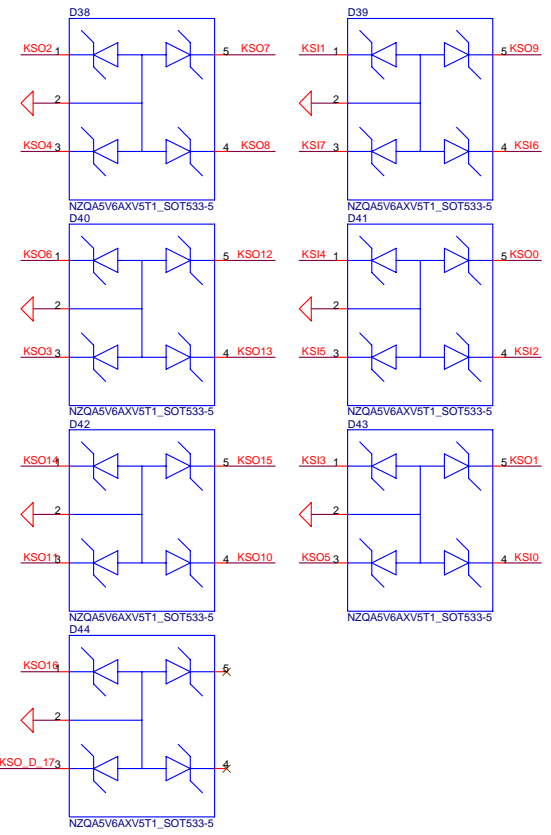


Reserve Bluetooth

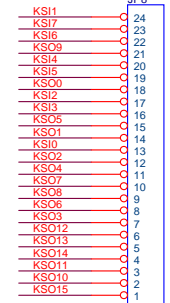
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				Size	Document Number
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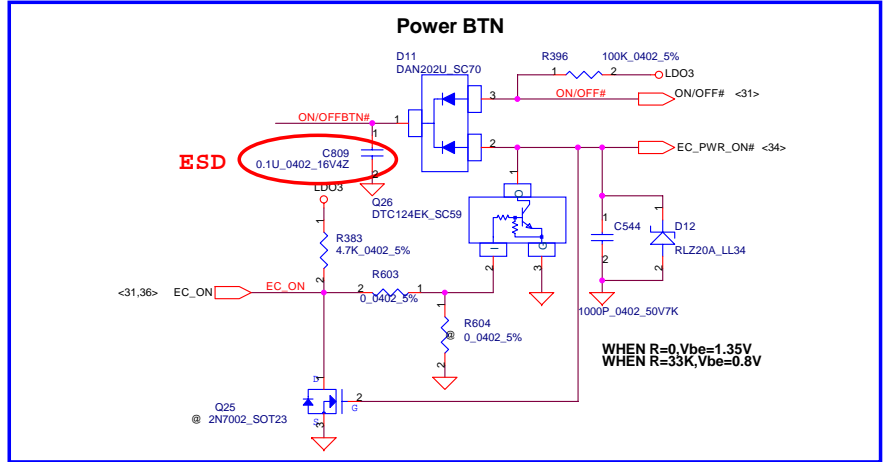
<31> KSO_D_17 ← KSO_D_17<3>



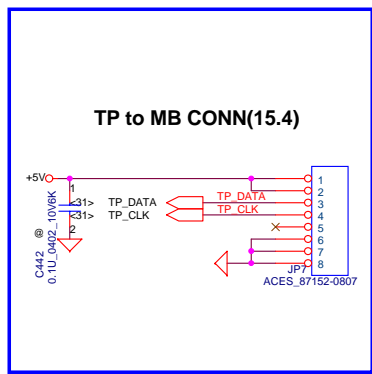
15.4 (TYPE "C" KB)



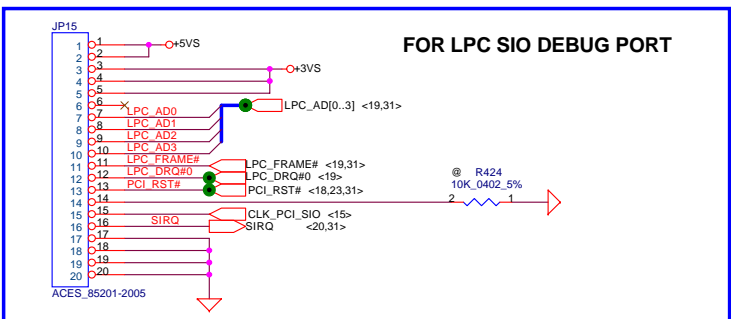
ACES_85201-2405



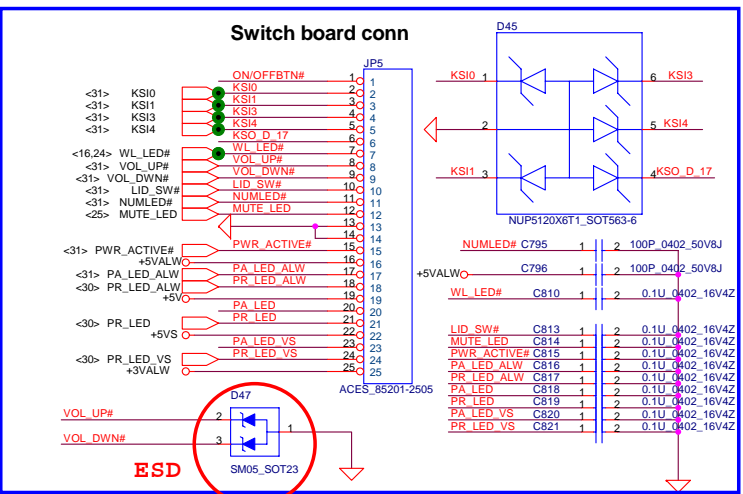
WHEN R=0, Vbe=1.35V
WHEN R=33K, Vbe=0.8V



<6/21> Remove CIR

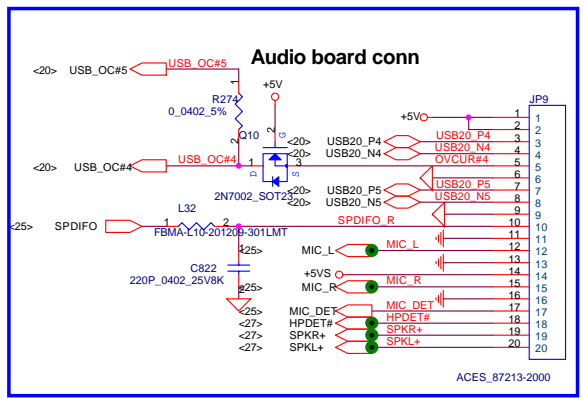


FOR LPC SIO DEBUG PORT



Switch board conn

ESD



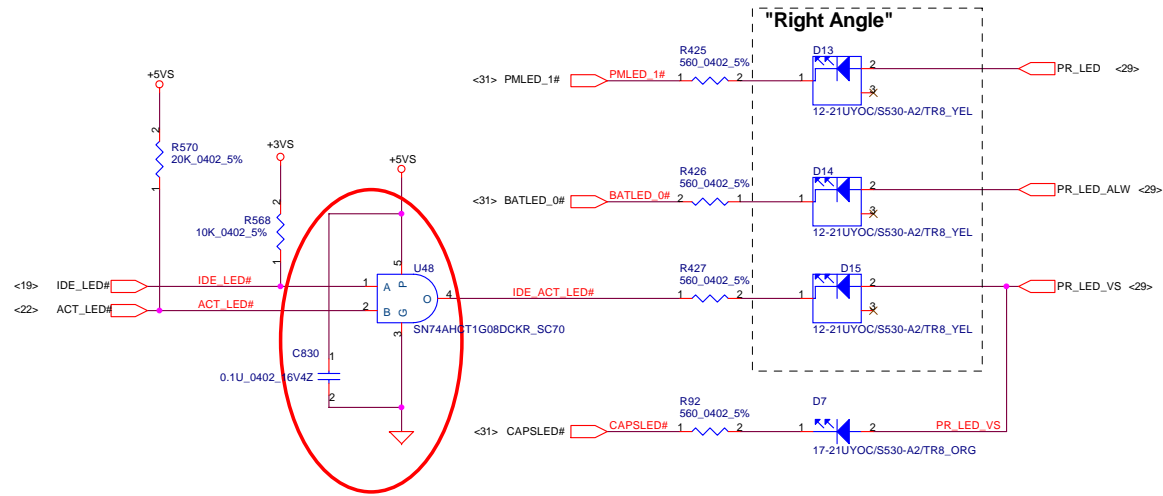
Audio board conn

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		2006/03/10
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Title		Compal Electronics, Inc.	
		KBD,ON/OFF,TP,LED/B,DEBUG	
Size	Document Number		Rev
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For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	INDICATE LED	
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Compal Electronics, Inc.

INDICATE LED

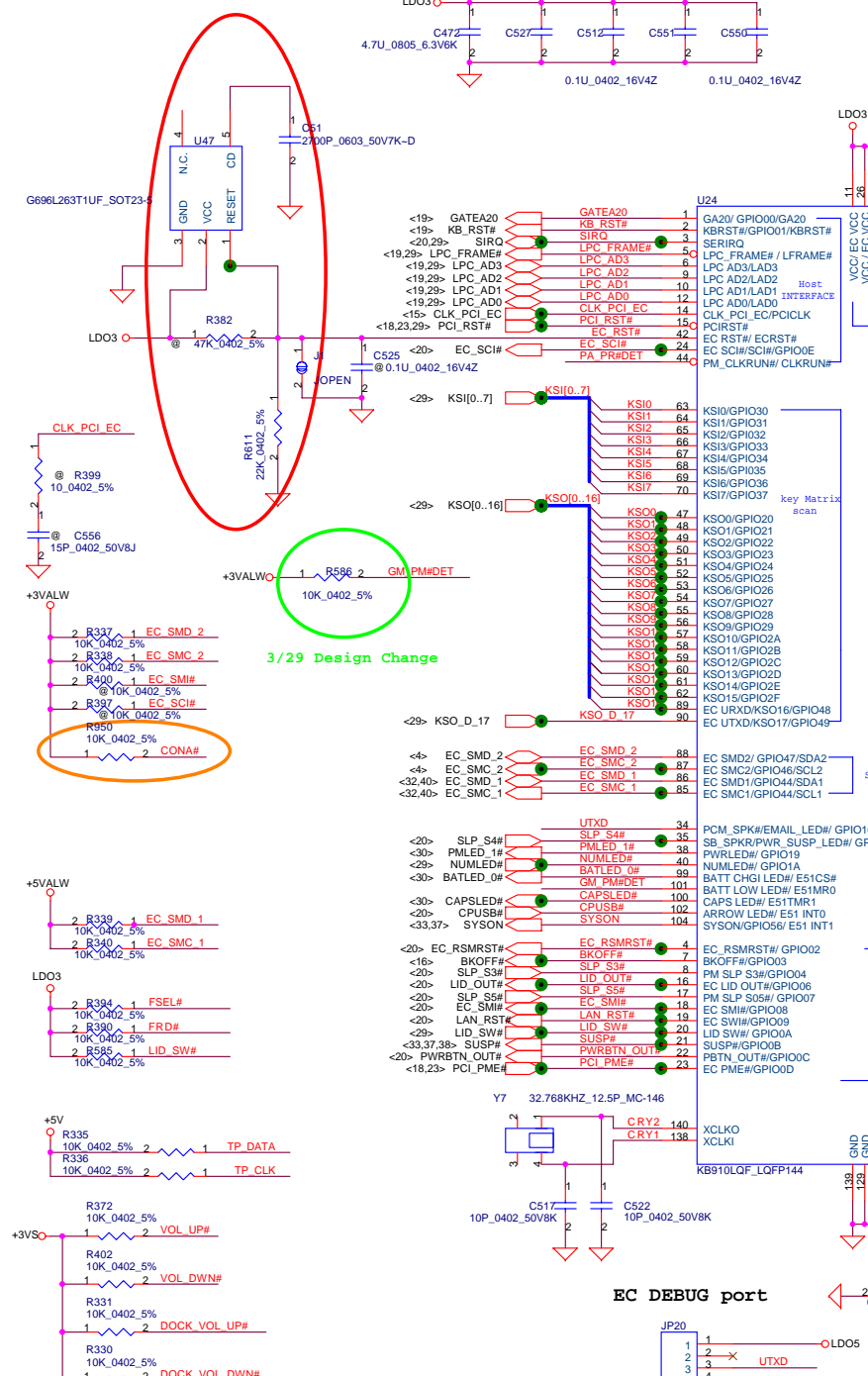
Document Number
LA-3342P

Rev
0.1

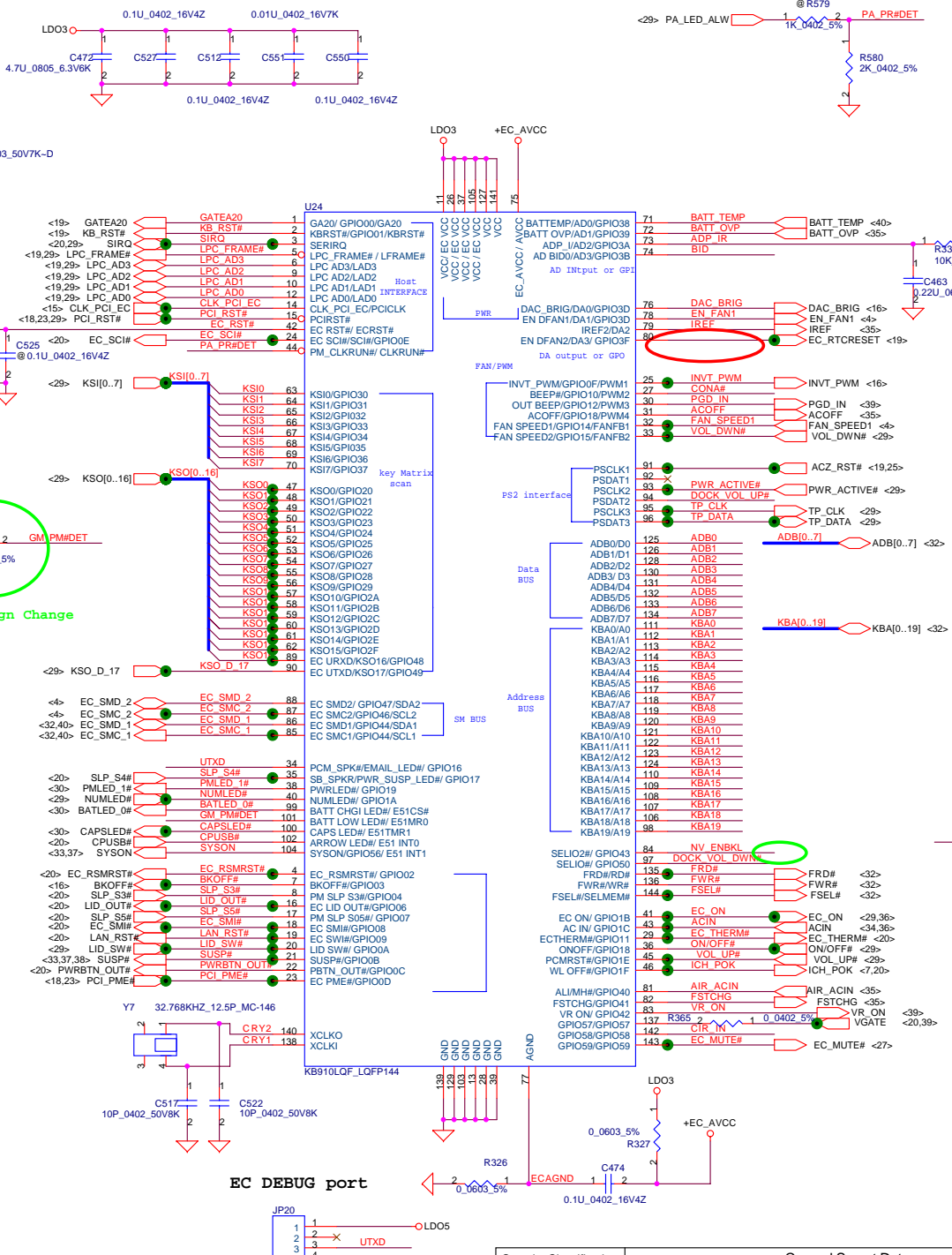
Date: Thursday, July 27, 2006

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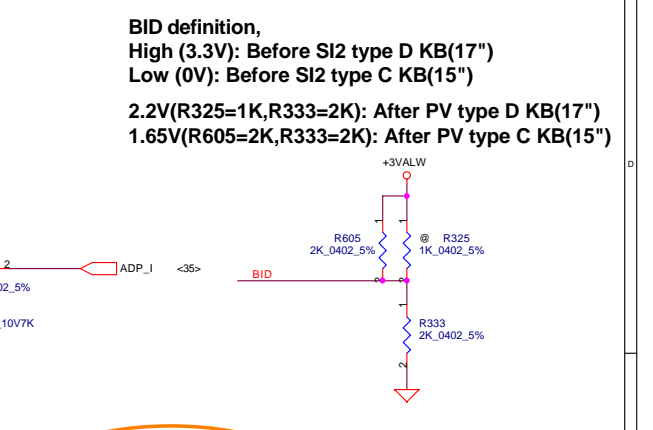
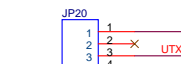
$Cd(uF)=T(ms) / 1685$
 $Cd=2700PF \rightarrow T=3.6ms$



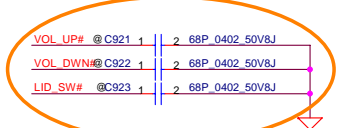
3/29 Design Change



EC DEBUG port

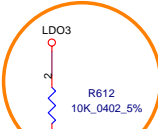


BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")
2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")



<6/3> To eliminate coupling noise

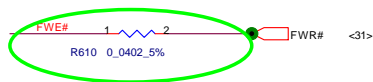
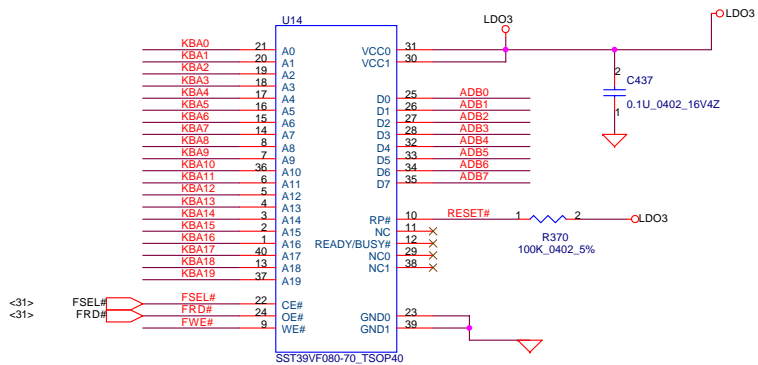
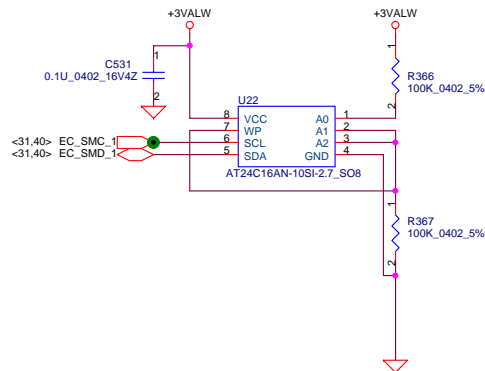
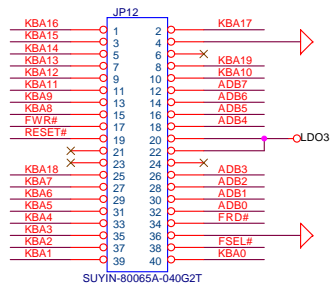
NV ENBKL



<6/21> Remove CIR, but keep CIR_IN pull-high

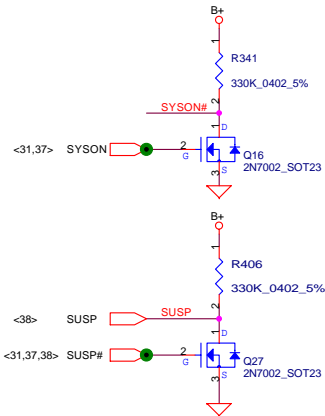
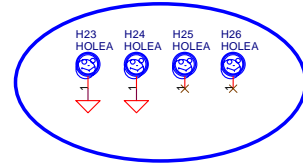
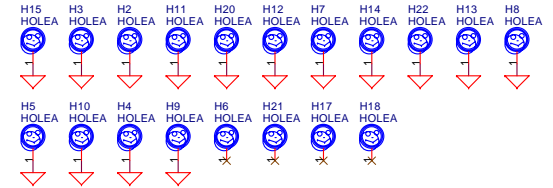
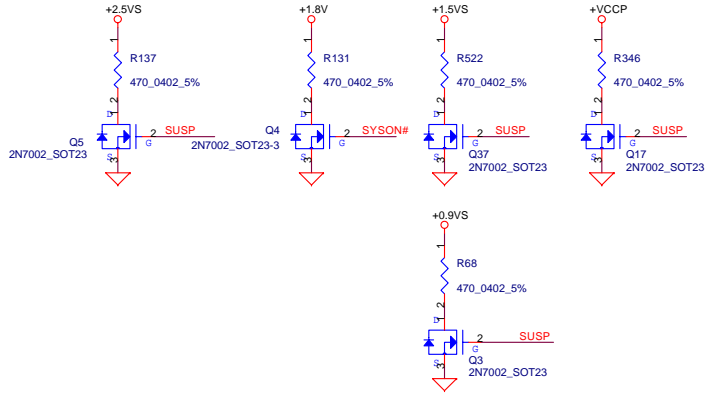
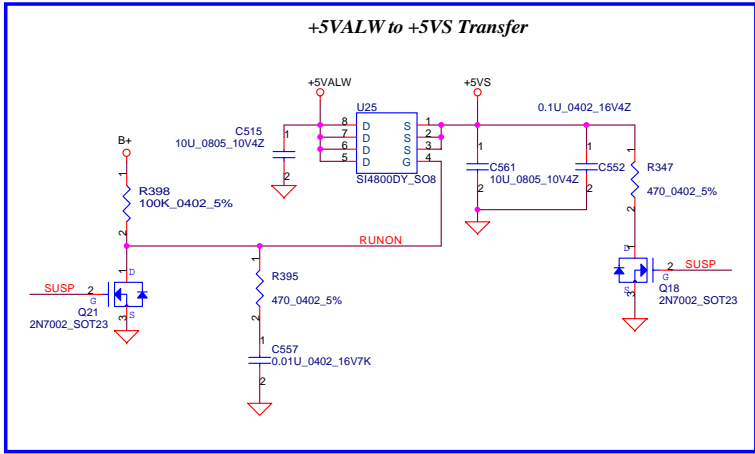
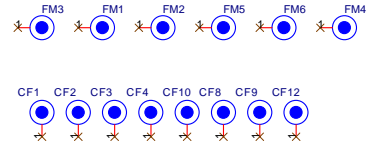
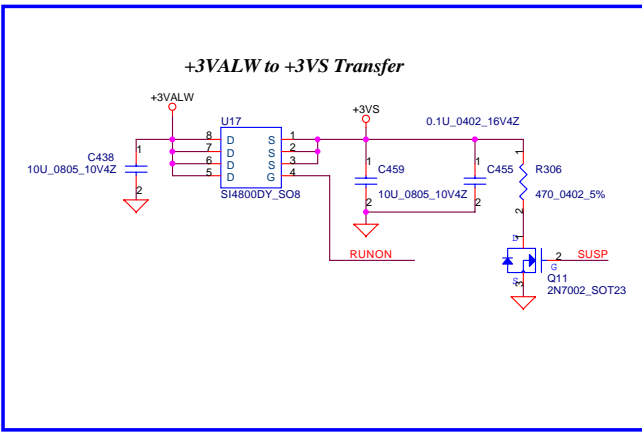
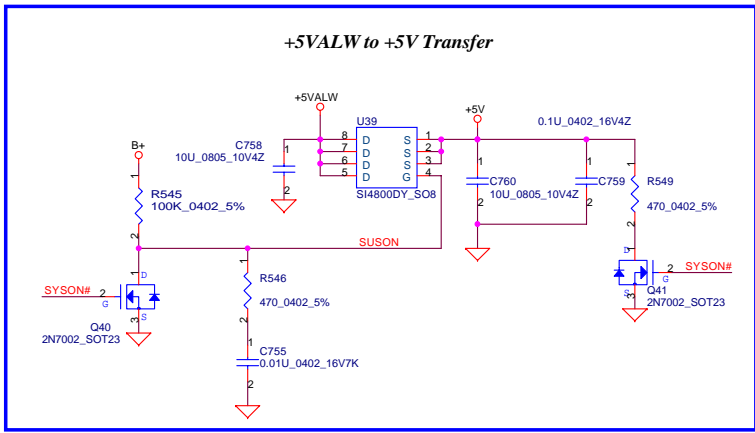
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<31> ADB[0..7] \leftrightarrow ADB[0..7]
 <31> KBA[0..19] \leftrightarrow KBA[0..19]

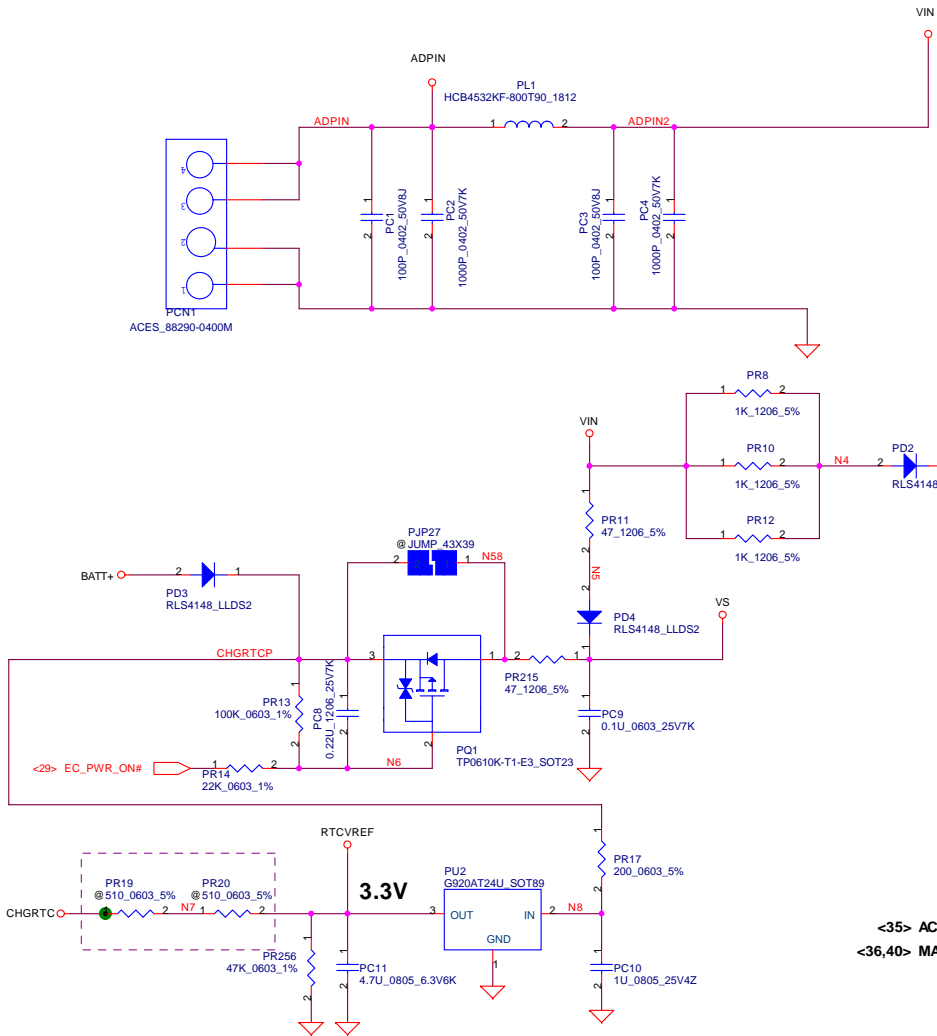


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Compal Electronics, Inc.		
Title BIOS & EC I/O Port		
Size Custom	Document Number LA-3342P	Rev 0.1
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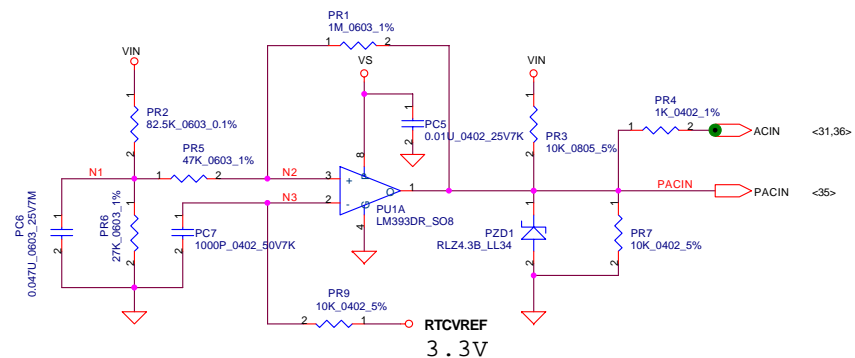


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Vin Detector :

14.698	14.285	13.879
13.818	13.411	13.000



ACIN:

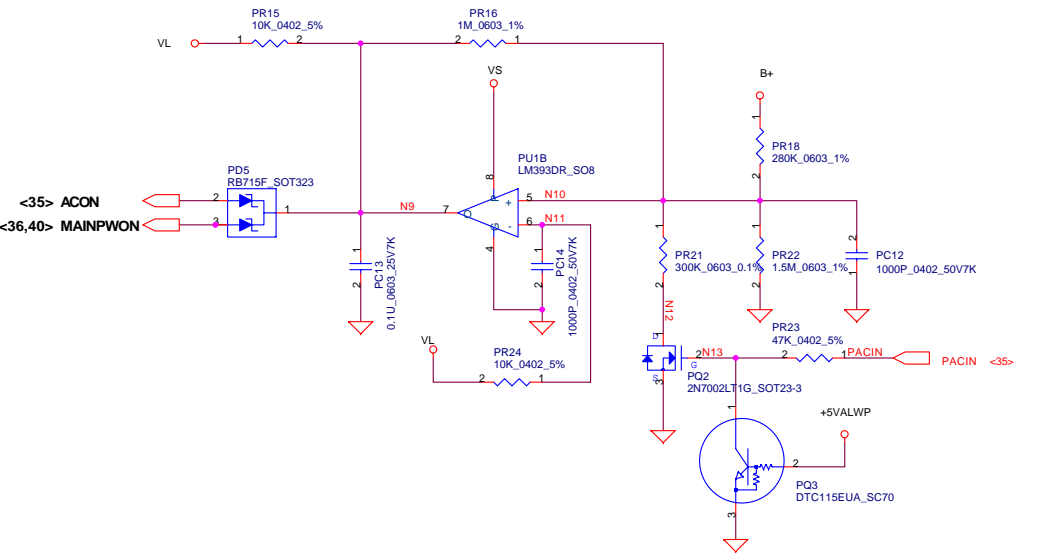
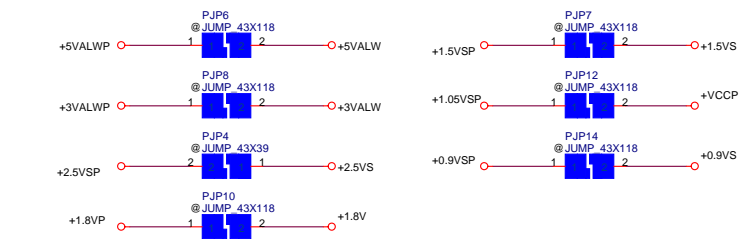
Precharge detector

12.384	12.000	11.624
10.927	10.600	10.223

BATT

Precharge detector

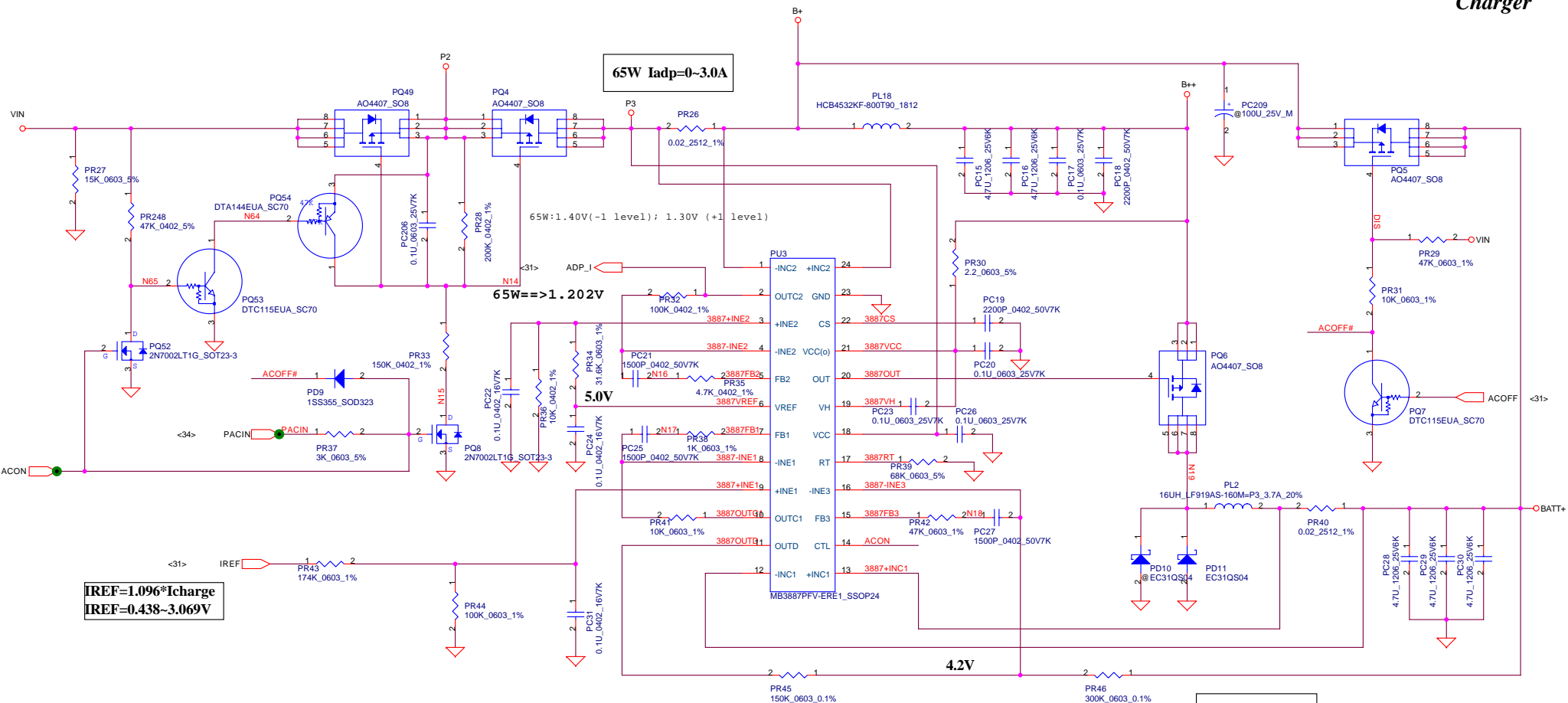
7.558	7.333	7.112
6.108	5.933	5.704



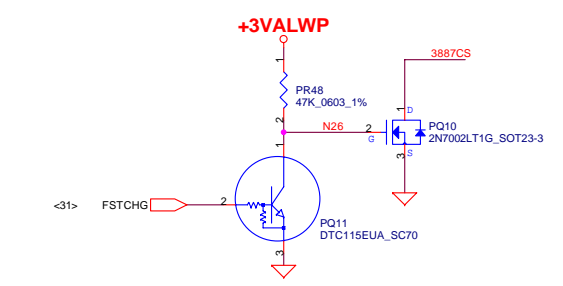
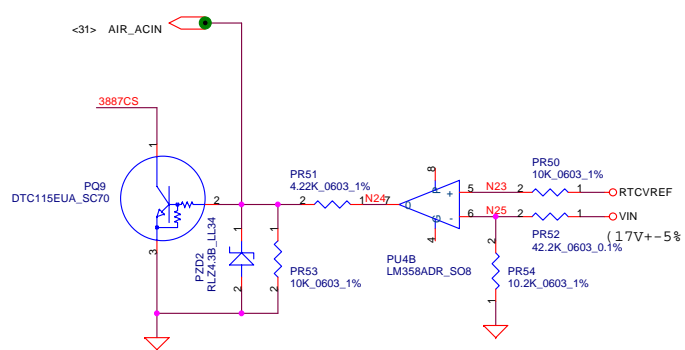
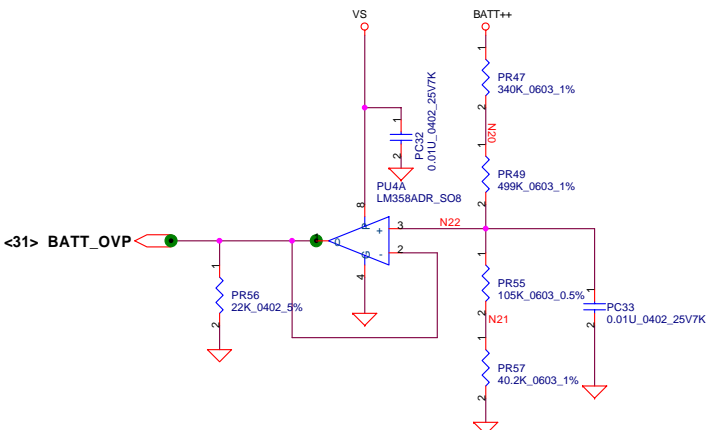
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Charger

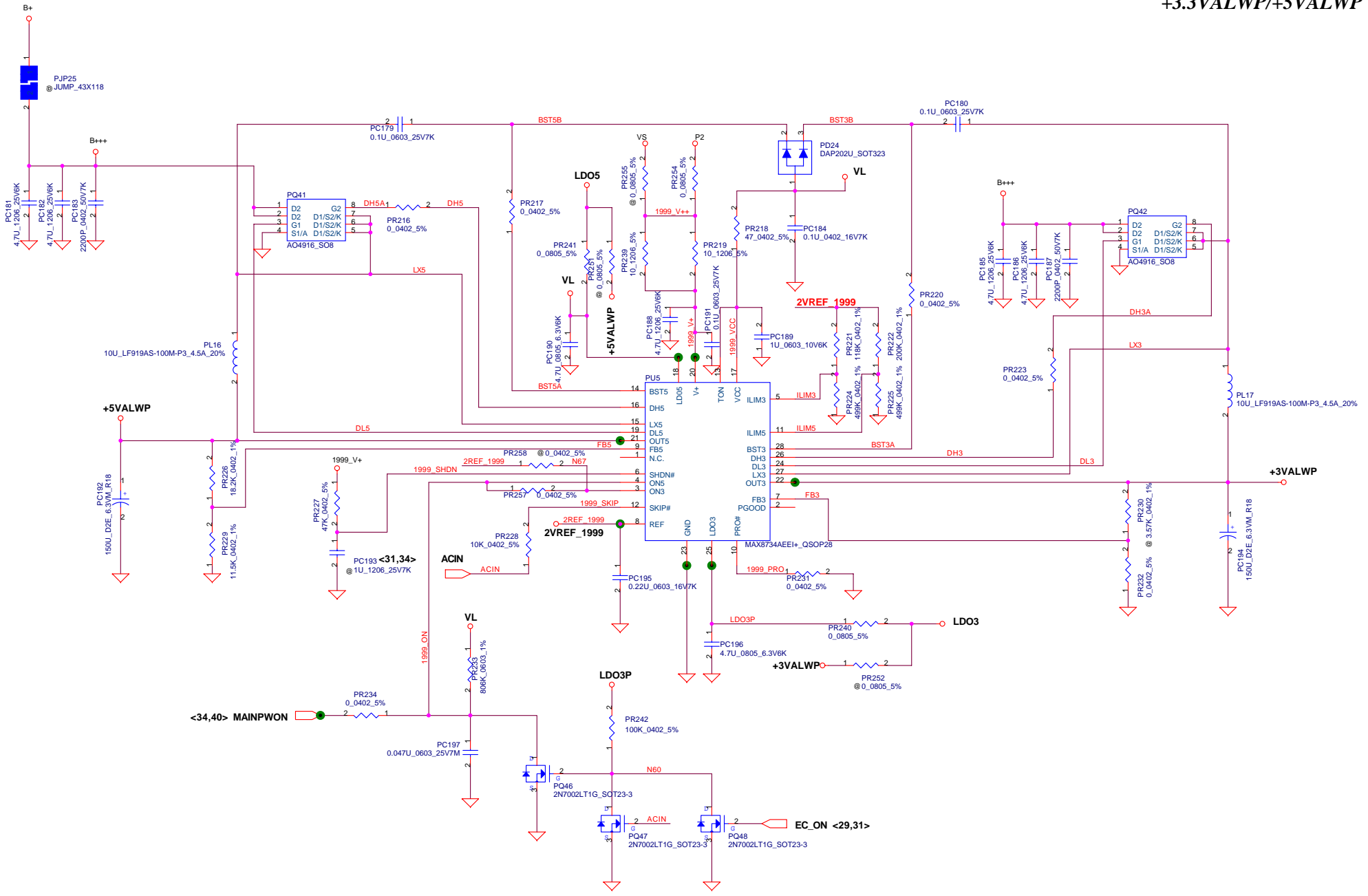


3S2P/3S4P : 13.5V--> BATT_OVP = 2.0V
(BAT_OVP=0.14753 *BATT+)



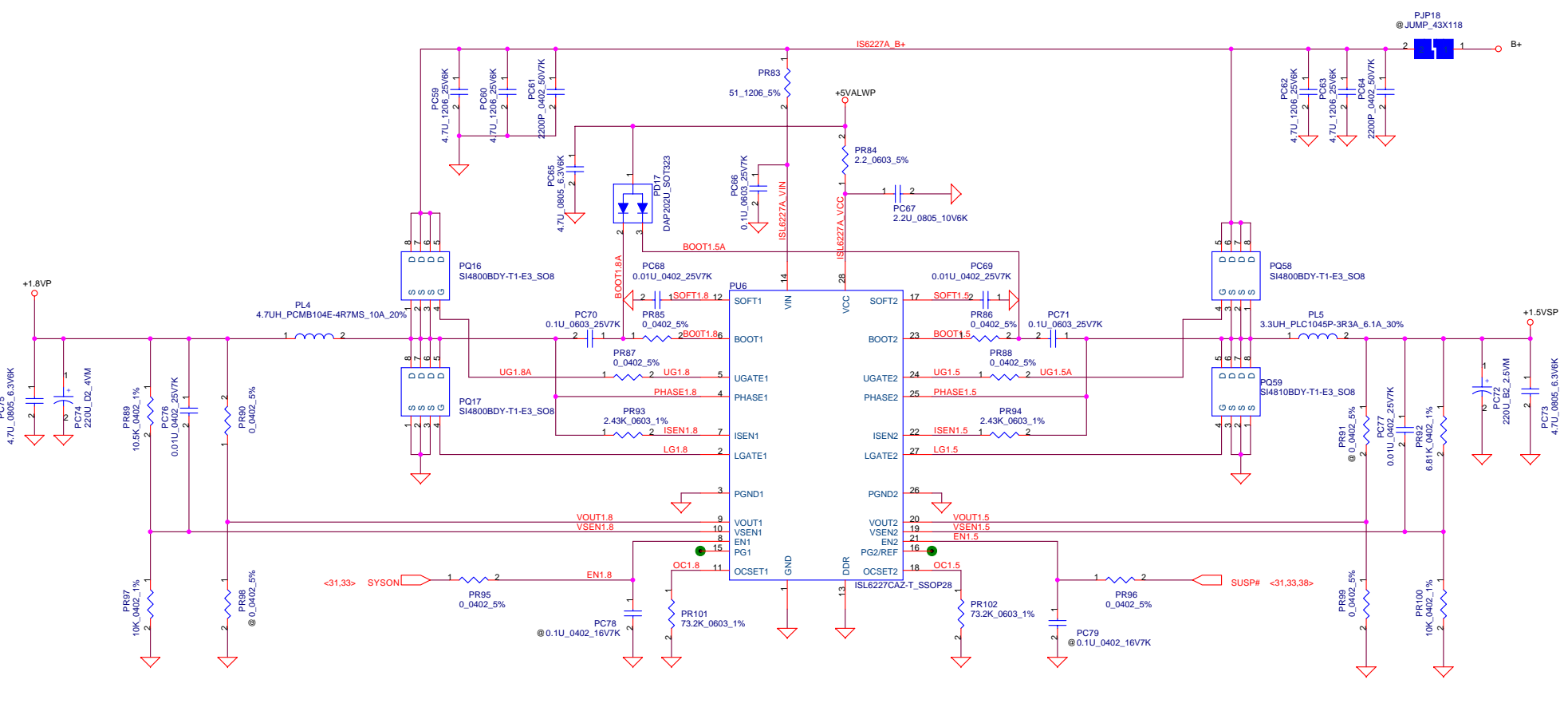
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Issued Date	2006/04/03	Deciphered Date	2007/04/03	Charger	
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+3.3VALWP/+5VALWP

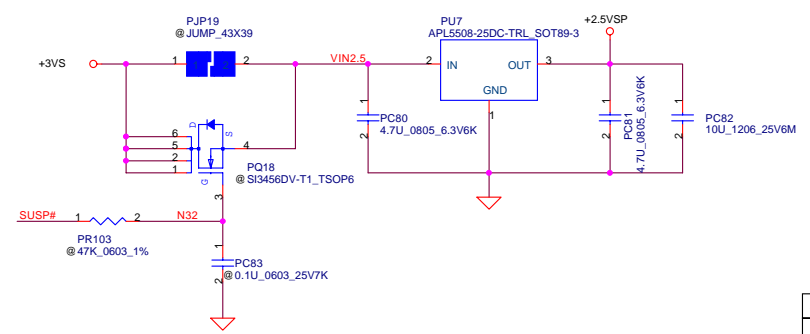


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+2.5VSP/+1.8VP/+1.5VSP

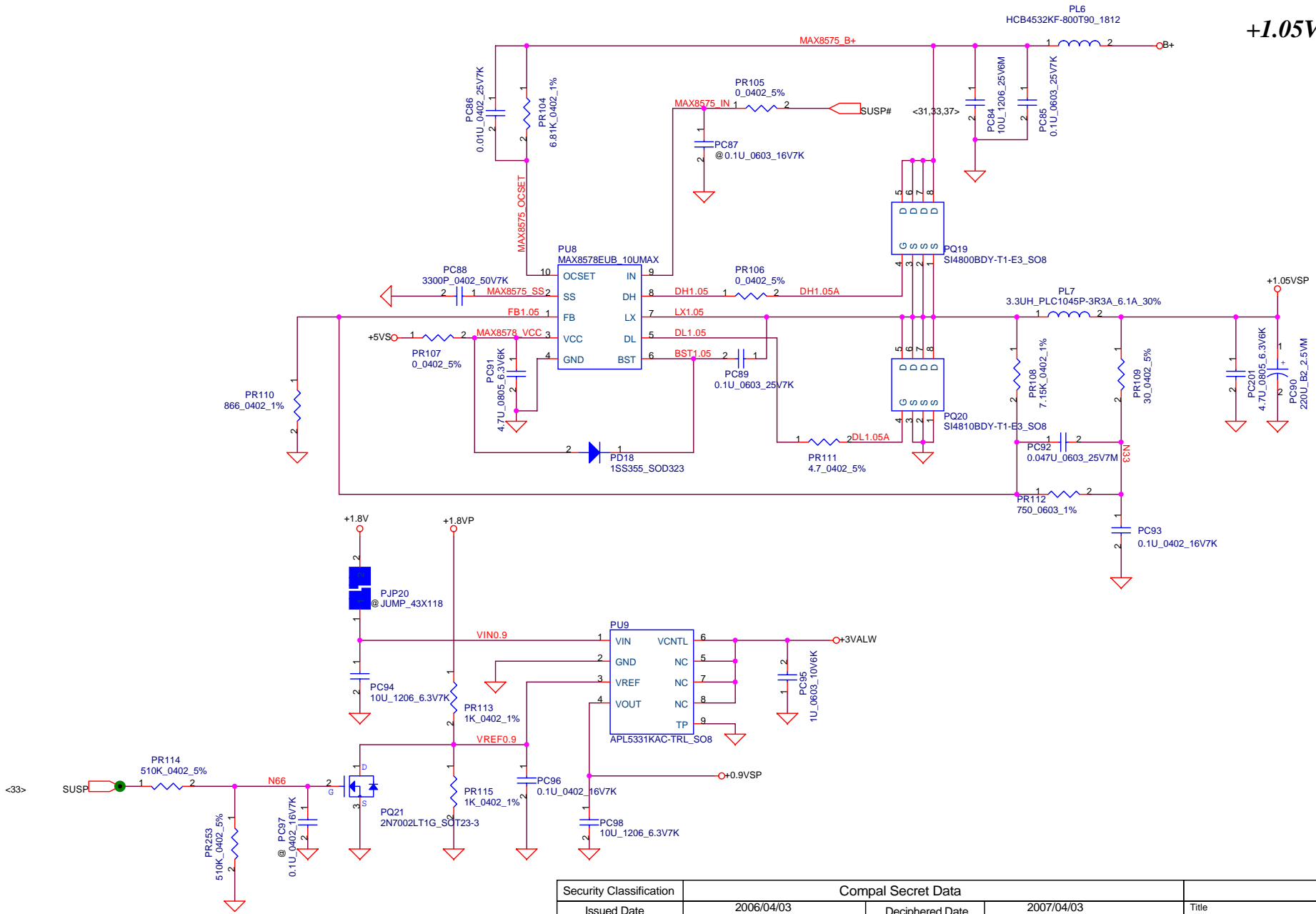


(400mA, 40mils, Via NO. = 1)



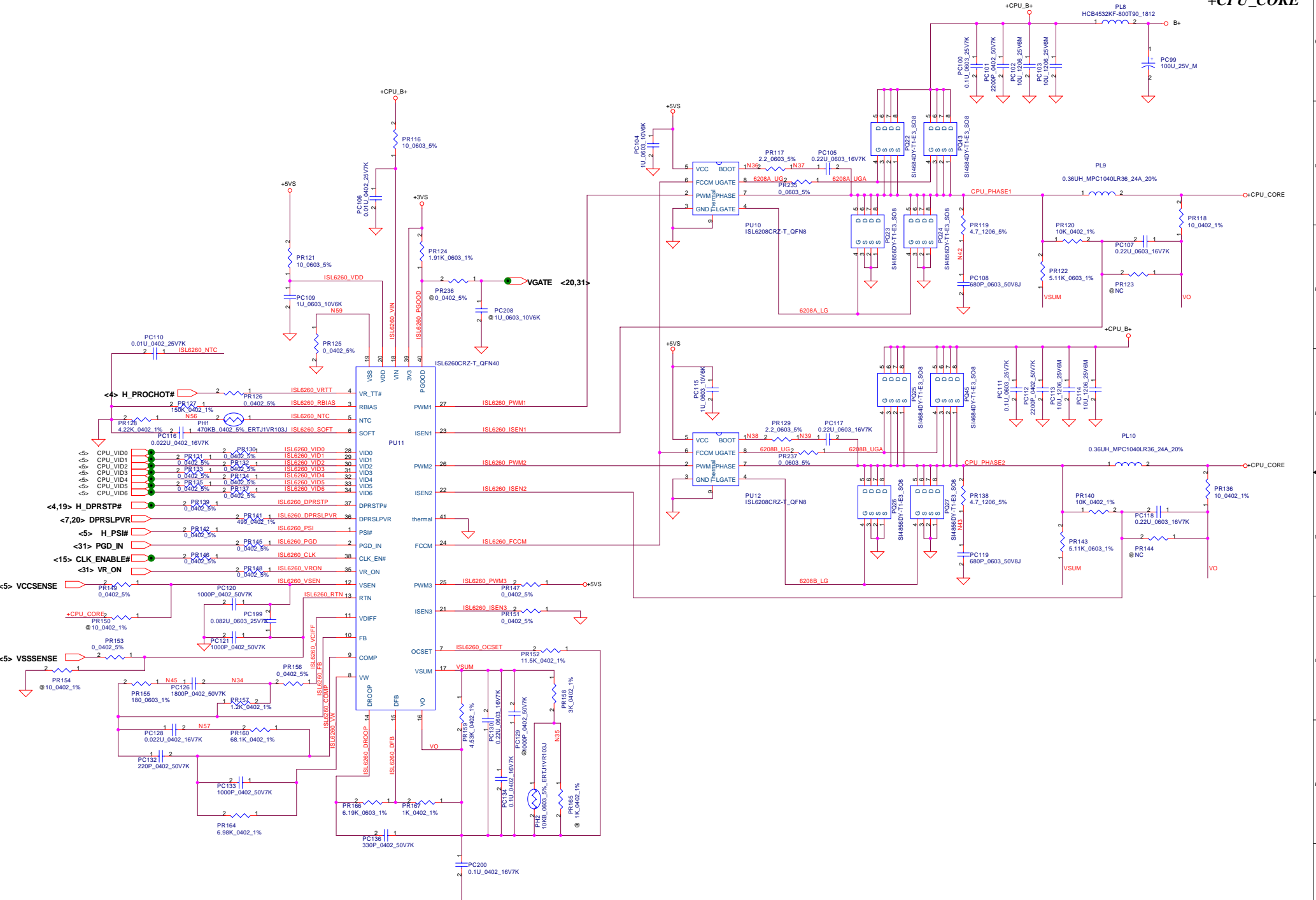
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+1.05V_VCCPP/+0.9VSP



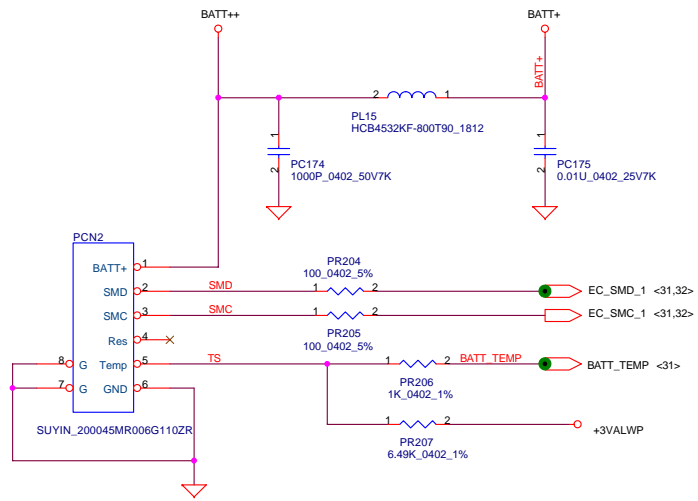
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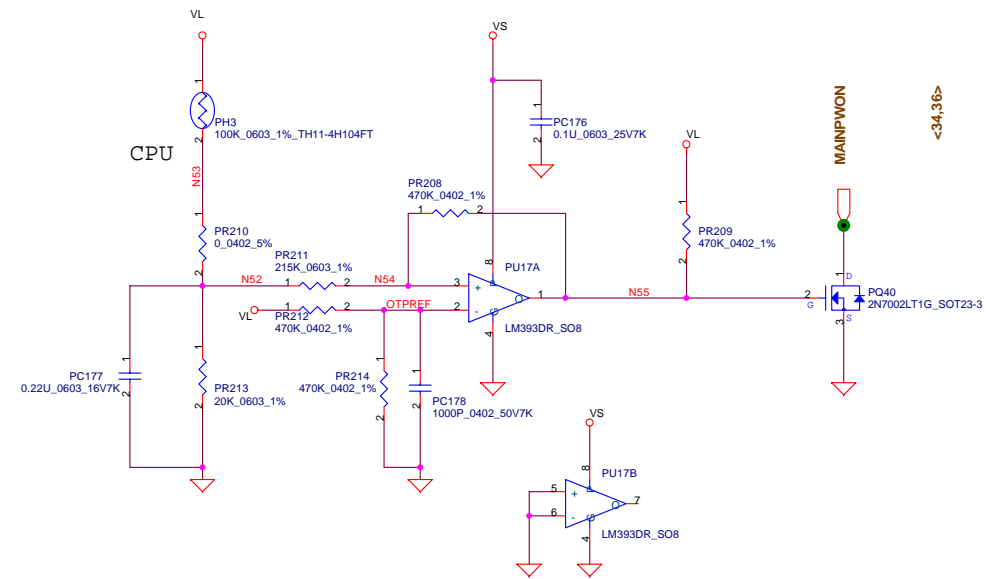
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Battery Connect/OTP



PJPB1 battery connector
SMART
Battery:
1. BATT+
2. SMD
3. SMC
4. Res
5. Temp
6. GND

PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



Security Classification	Compal Secret Data		Title	Battery Connect/OTP	
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