

Compal Confidential

Schematics Document

INTEL AUBURNDALE with IBEX core logic

Cartier UMA

LA-4902P

2009-12-07

REV: 1.0

機 密	等級	硬體二部
	產出人員	
	產出日期	
	解密日期	

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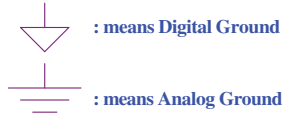
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Compal Electronics, Inc.		
Block Diagram		
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+3VM +1.05VM	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

N10M@ : Install for N10M Graphic controller

1098@ : Install for 1098 KBC controller

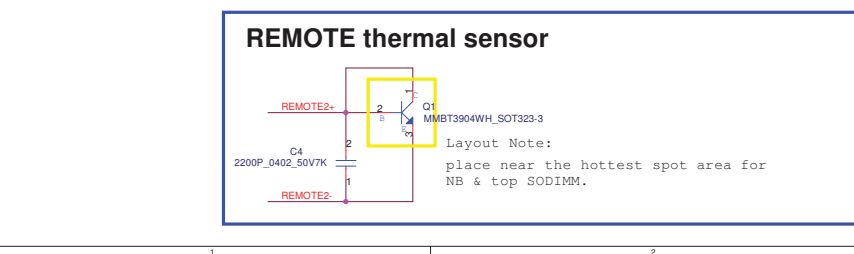
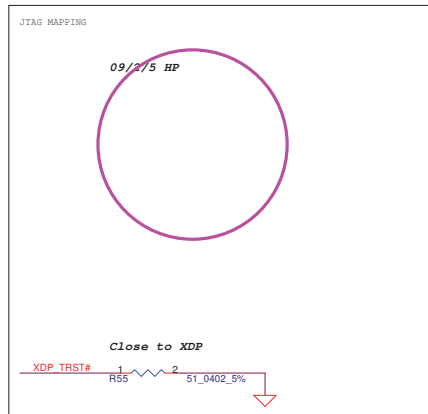
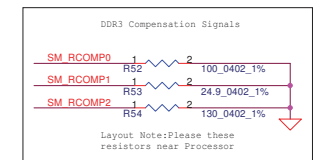
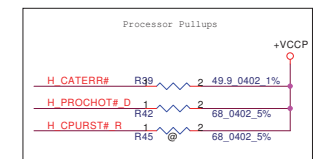
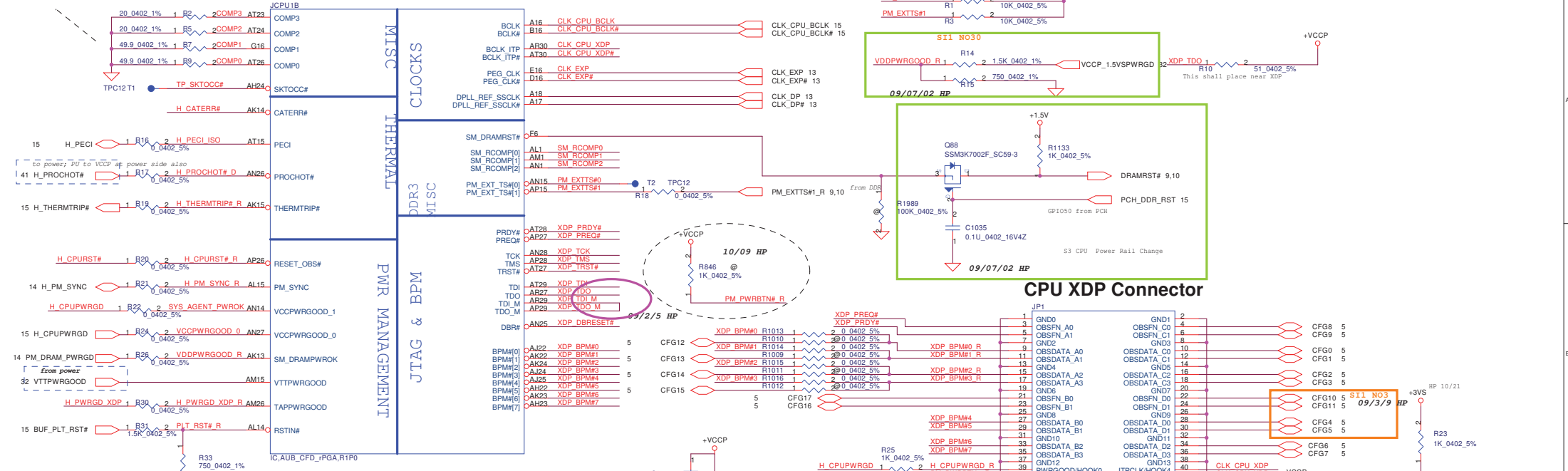
Reserve below BOM structure for ver. 0.1

1091@ : Install for 1091 KBC controller

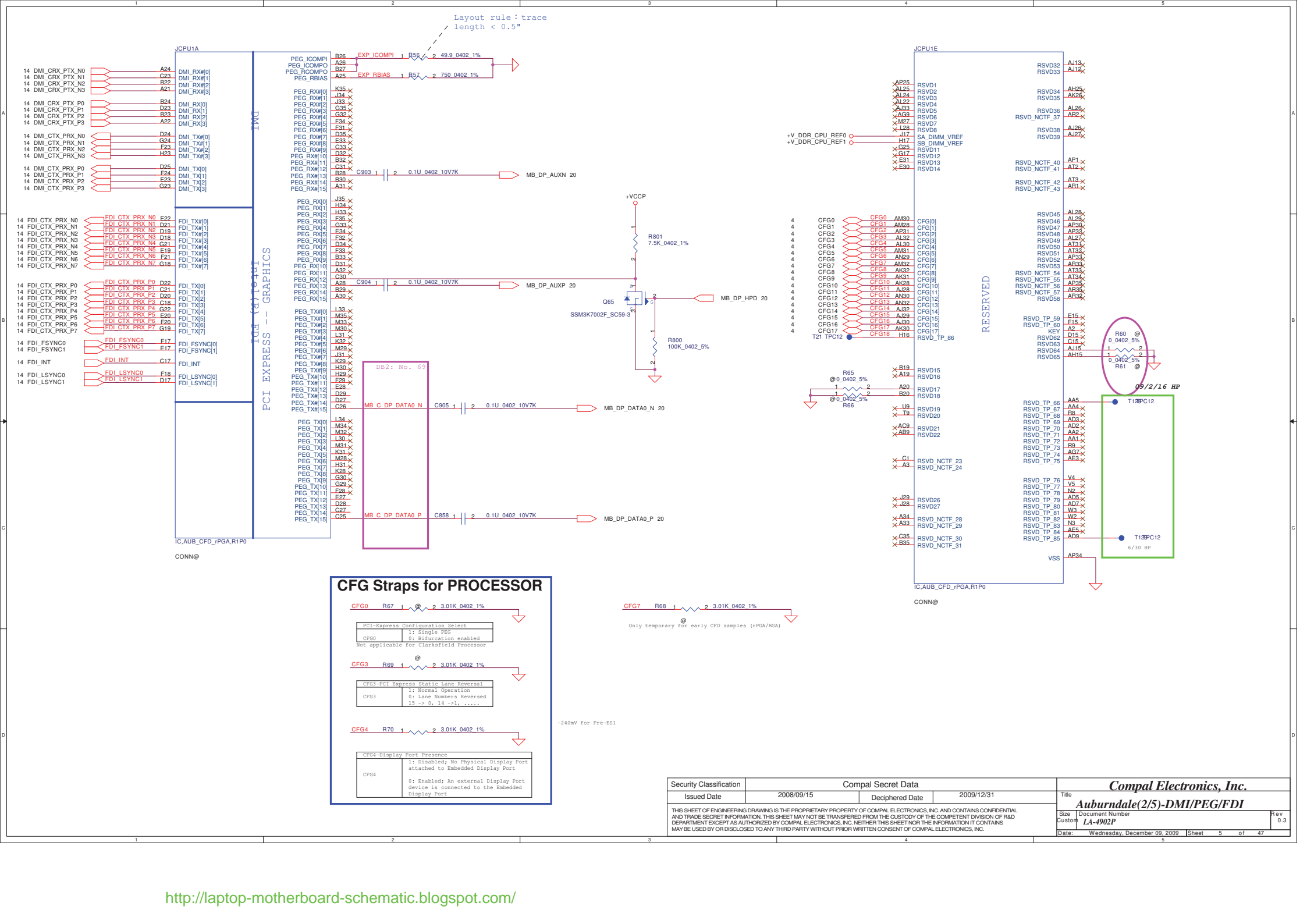
SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

Layout rule: 10mil width trace
length < 0.5", spacing 20mil



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Layout rule: trace length < 0.5"

CFG Straps for PROCESSOR

CFG0 R67 1 @ 2 3.01K 0402 1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled Not applicable for classfield Processor

CFG3 R69 1 @ 2 3.01K 0402 1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1,

CFG4 R70 1 @ 2 3.01K 0402 1%

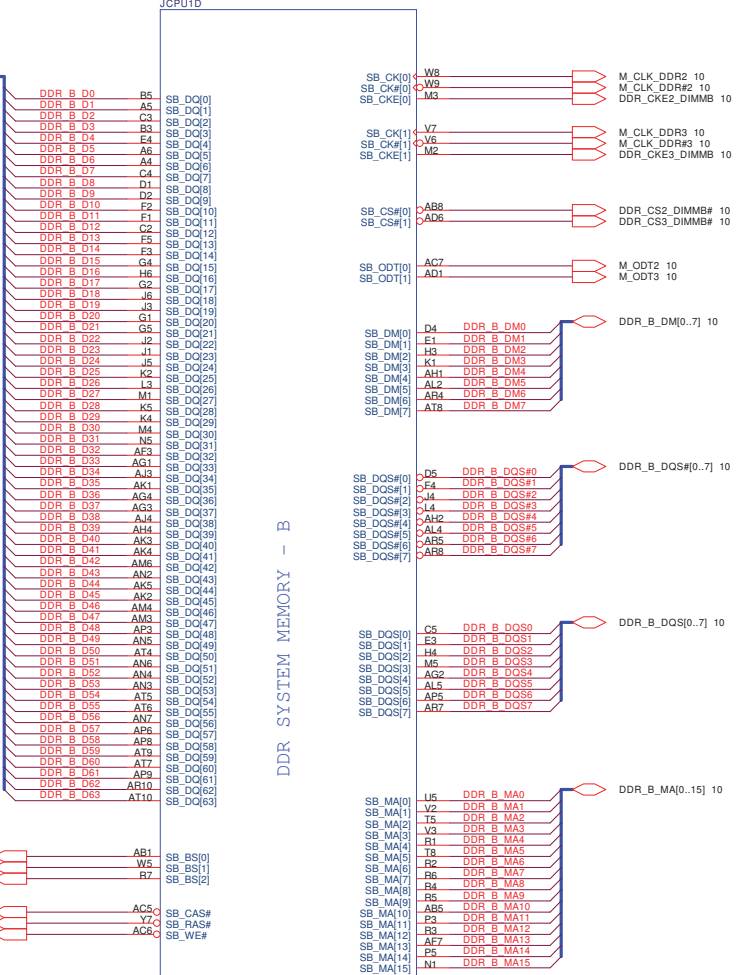
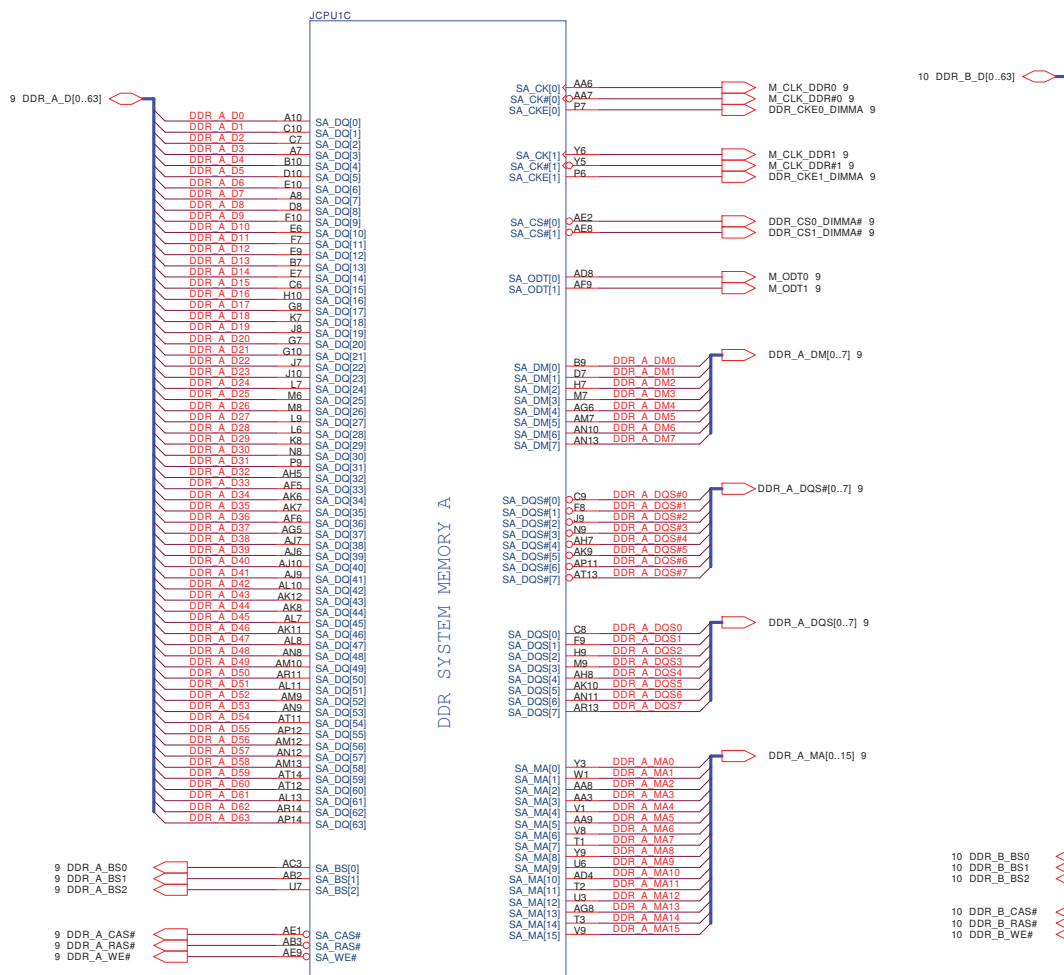
CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port.

CFG7 R68 1 @ 2 3.01K 0402 1%

Only temporary for early CFD samples (PGA/BGA)

-240mV for Pre-E81

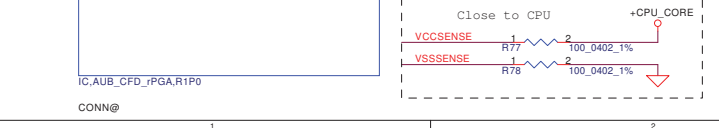
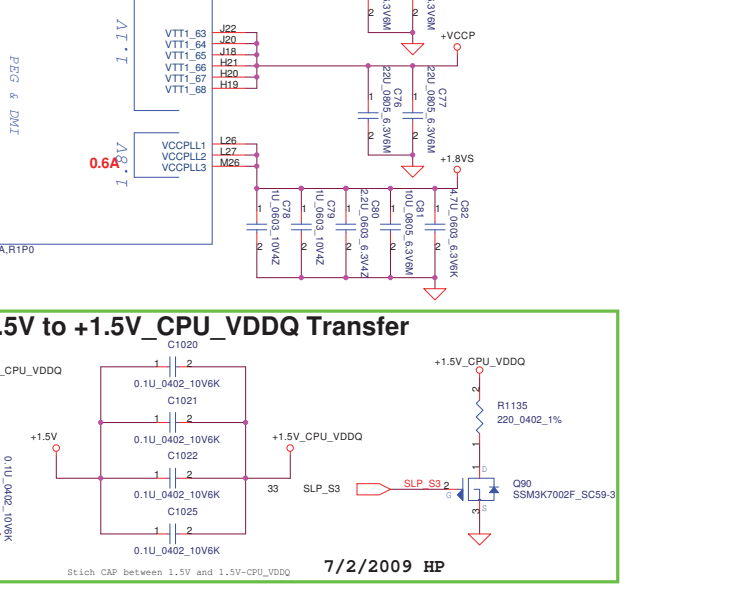
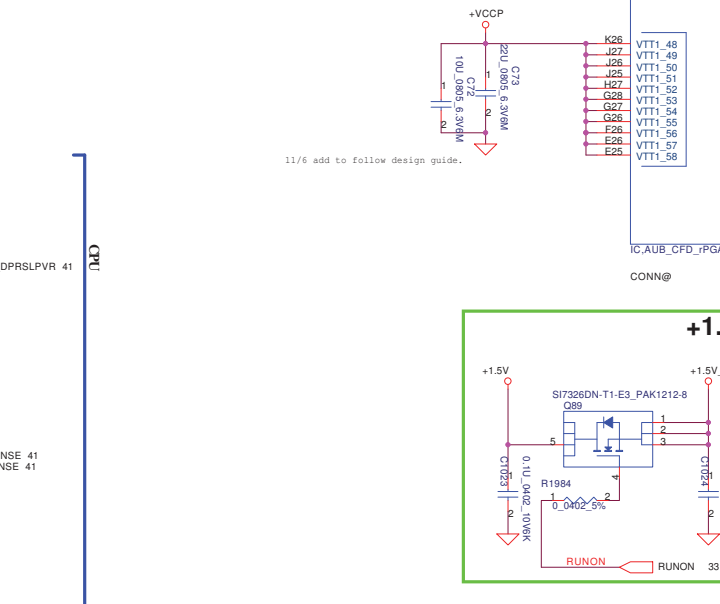
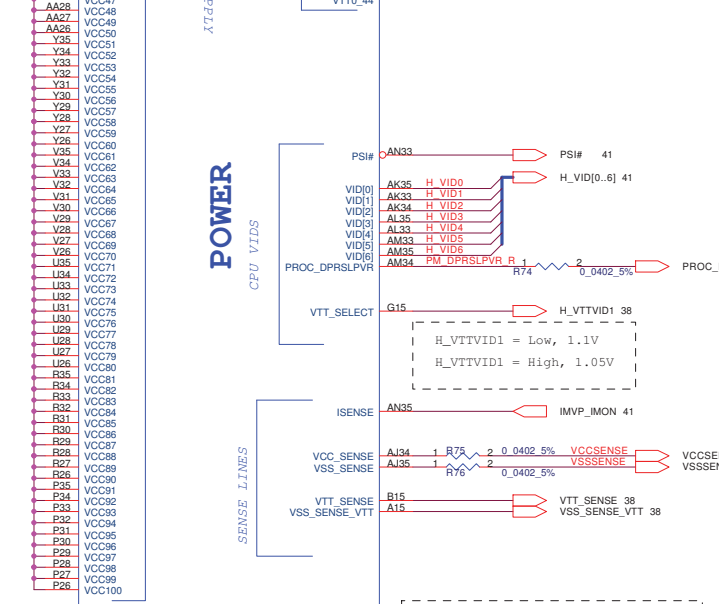
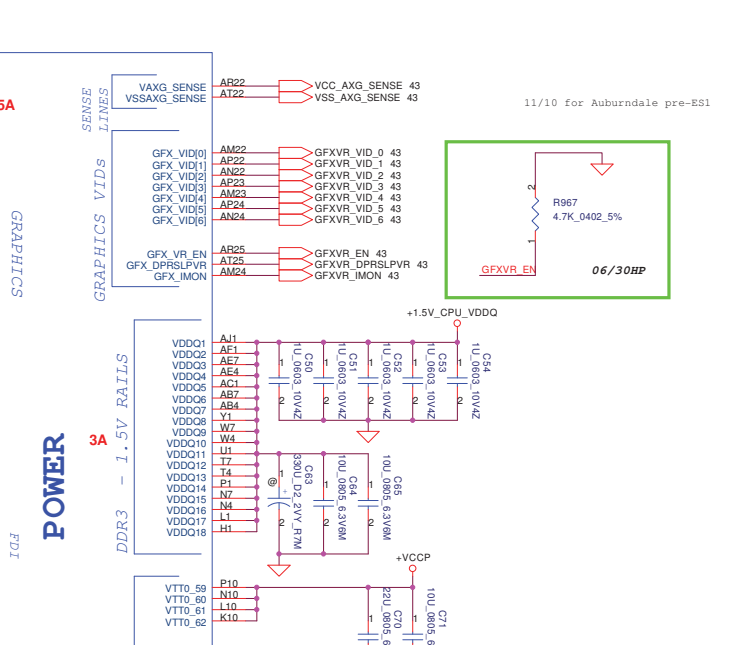
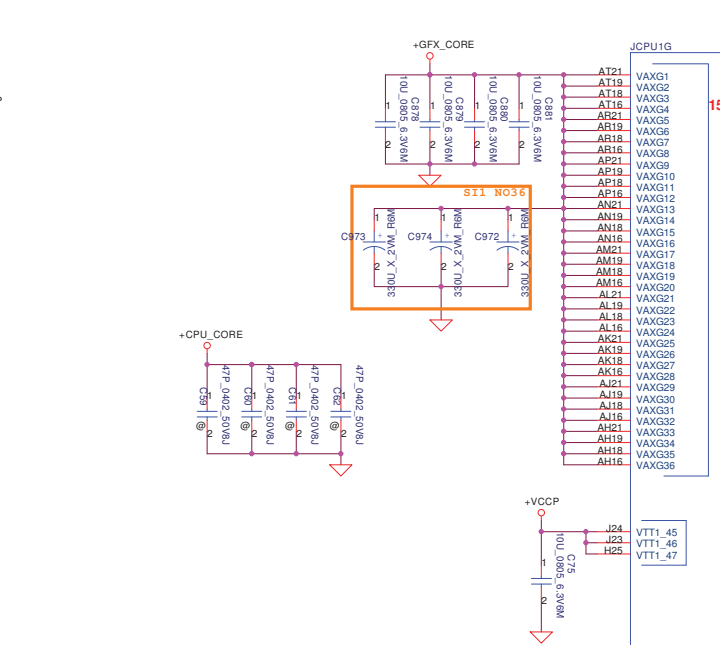
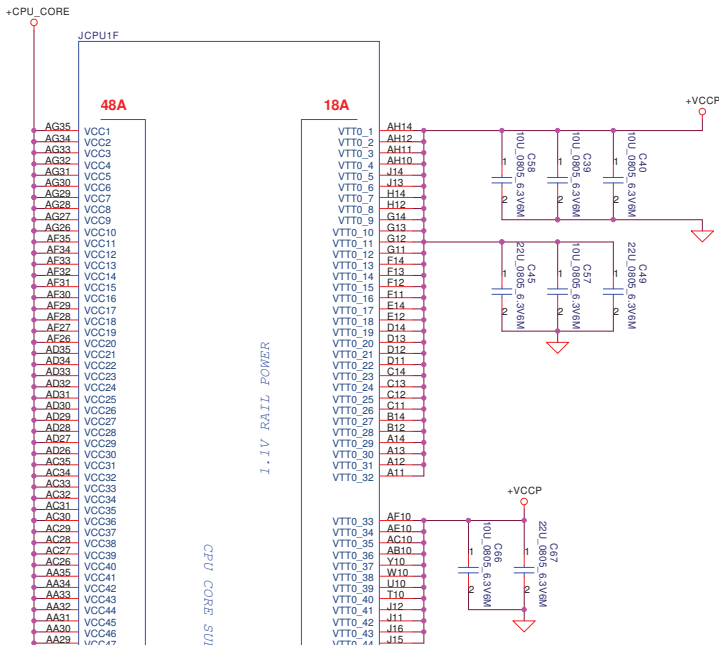
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Title Auburndale(2/5)-DMI/PEG/FDI			Rev 0.3
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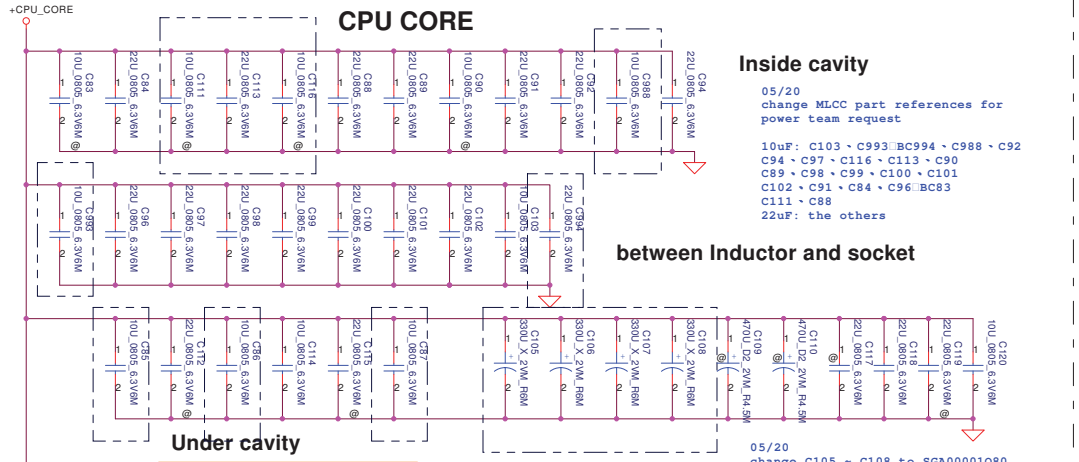
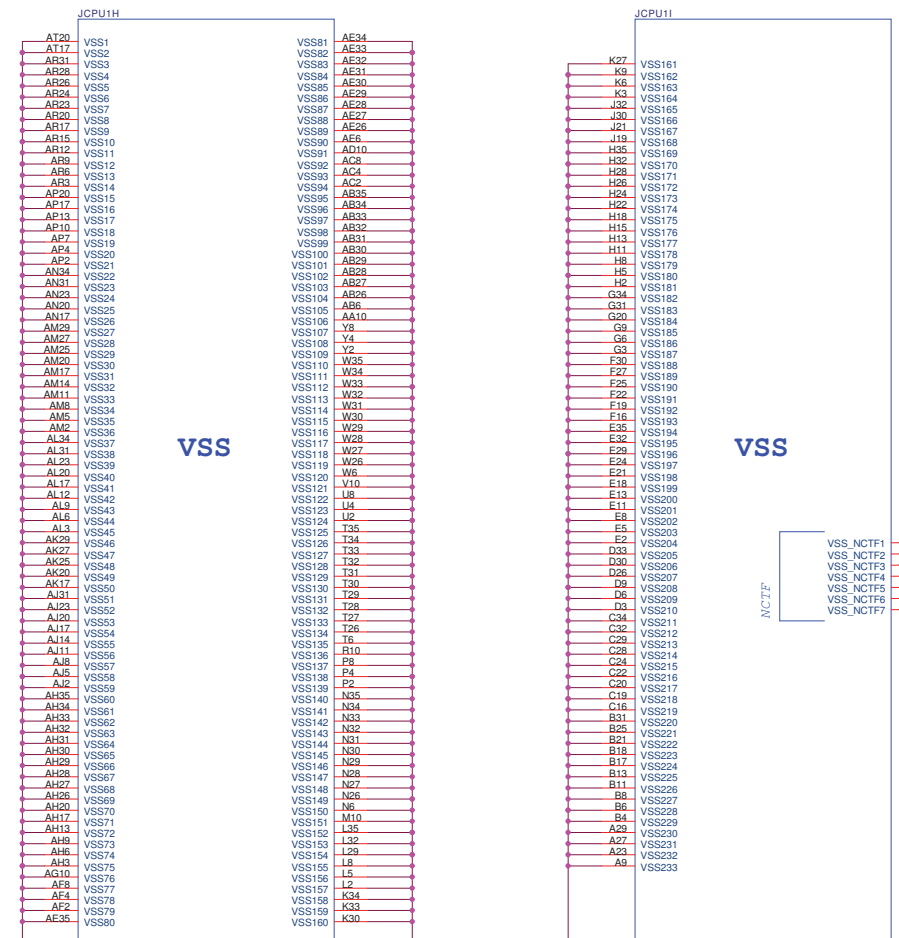
IC:AUB_CFD_PGA,R1P0
CONN@

IC:AUB_CFD_PGA,R1P0
CONN@

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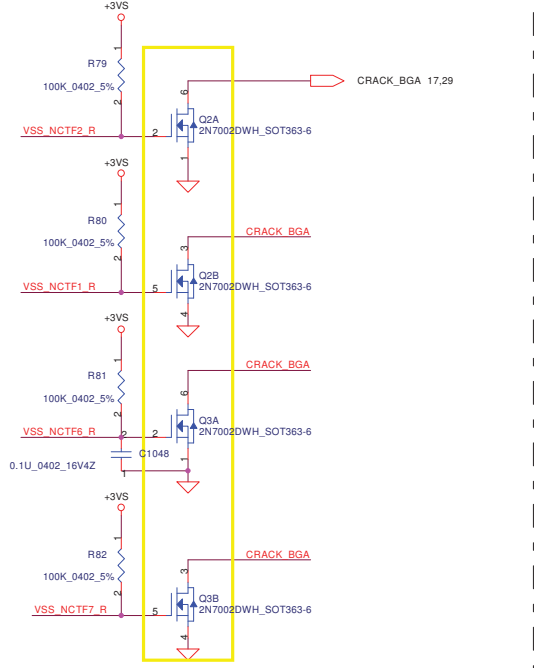
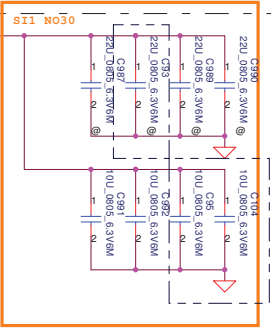
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05/20
change MLCC part references for
power team request

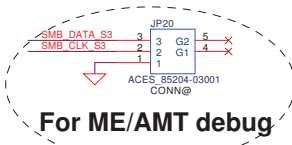
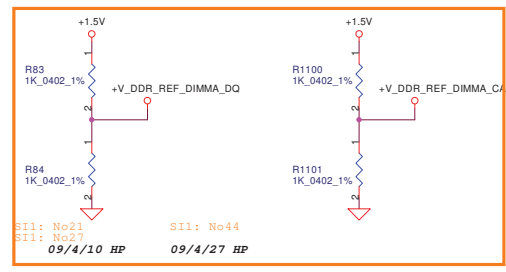
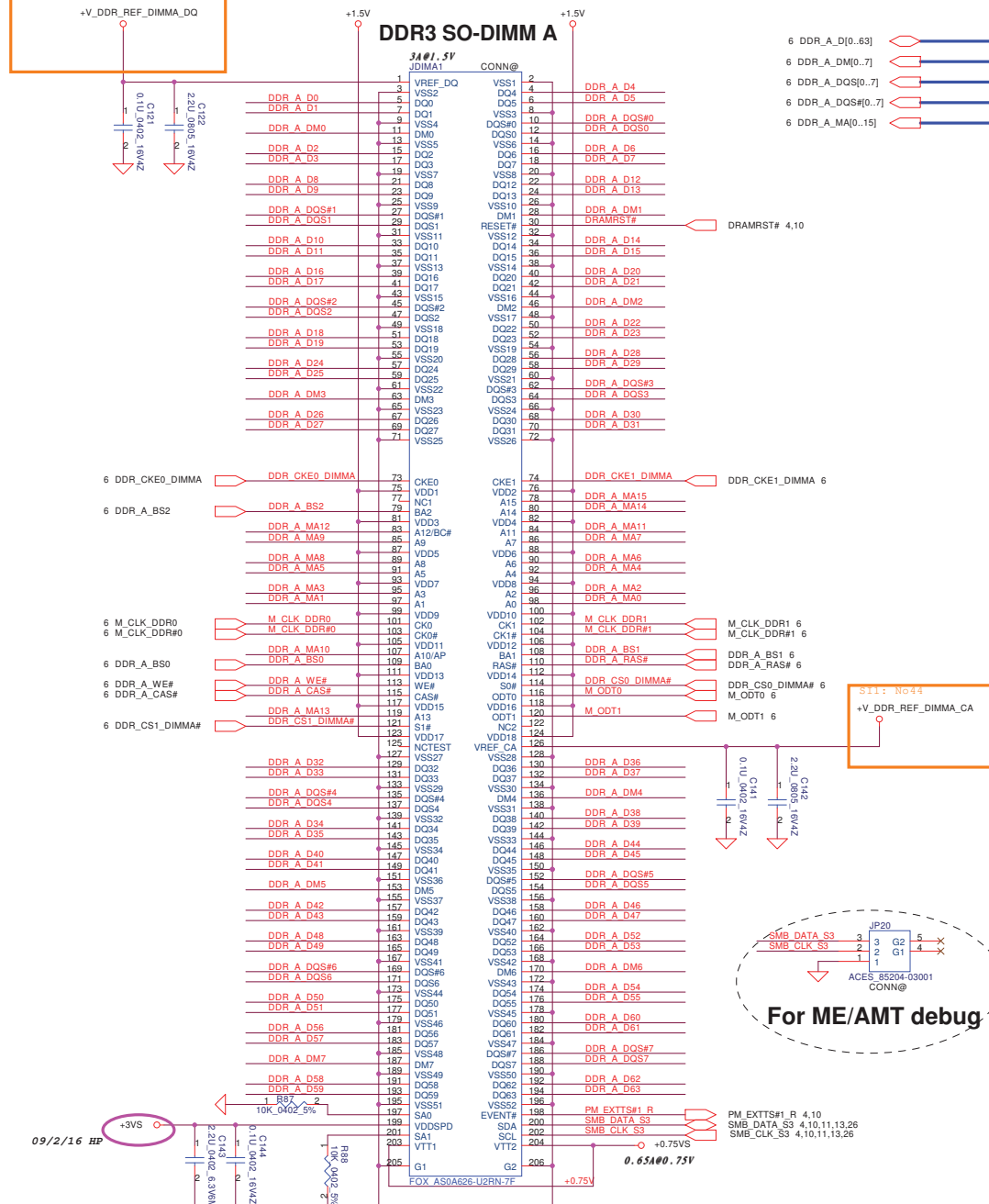
100µF: C103 - C993 BC994 - C988 - C92
C94 - C97 - C116 - C113 - C90
C89 - C98 - C99 - C100 - C101
C102 - C91 - C84 - C96 BC83
C111 - C98
220µF: the others

05/20
change C105 ~ C108 to SGA00001Q80



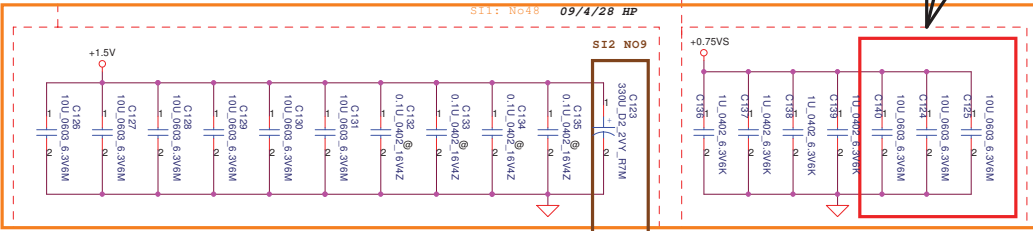
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S11: No44



Layout Note: Place near DIMMA

Layout Note: Place near DIMMA



Layout Note: Shared between the two SO-DIMMs. Place two capacitors close to the VR and one between the two SODIMMs

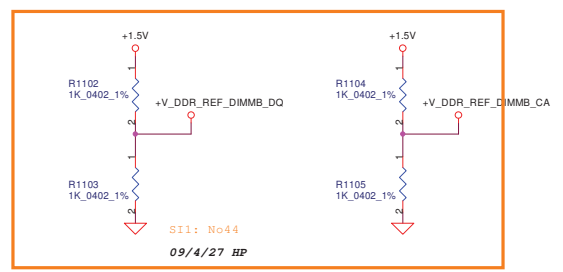
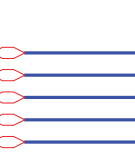
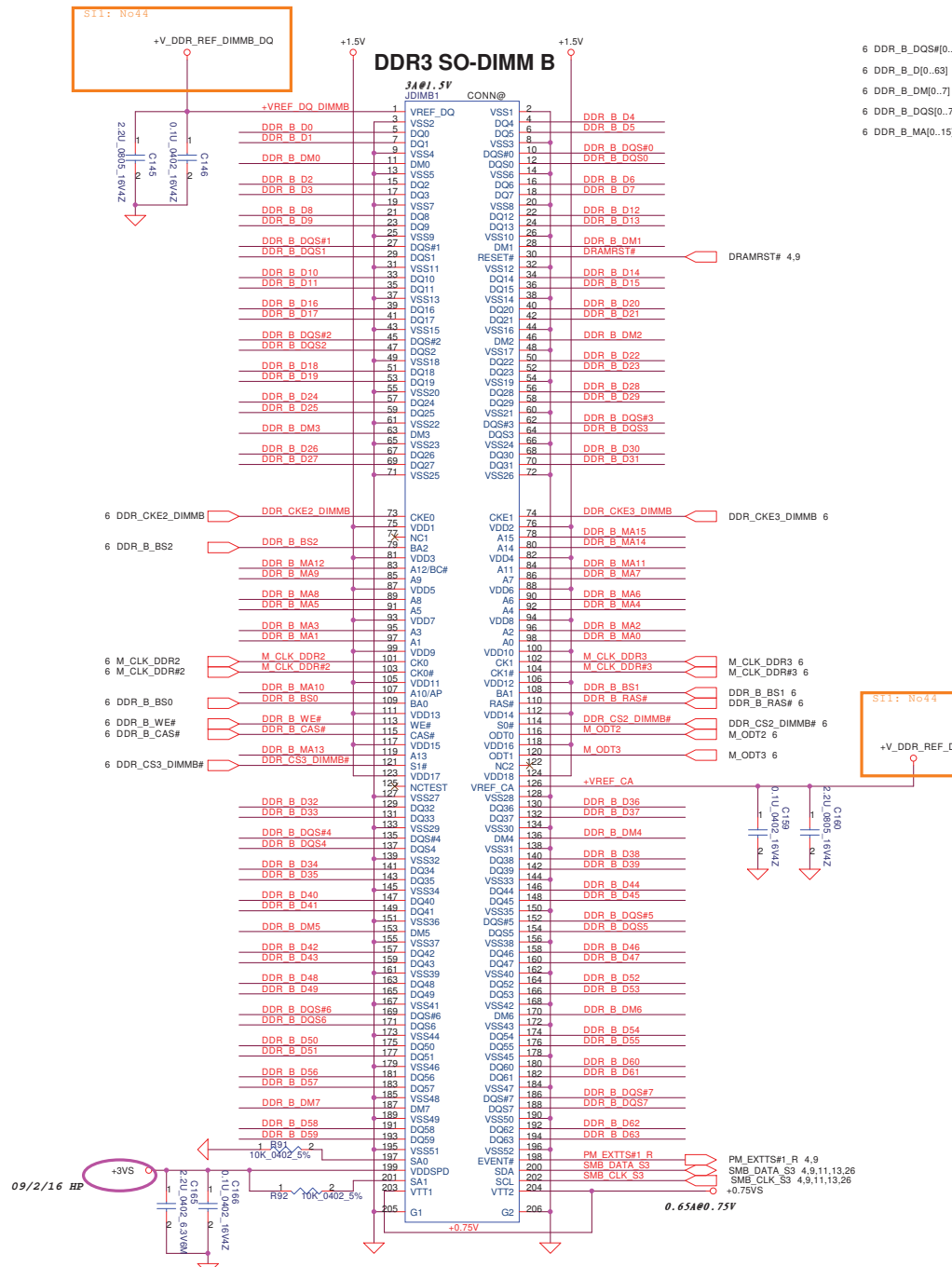
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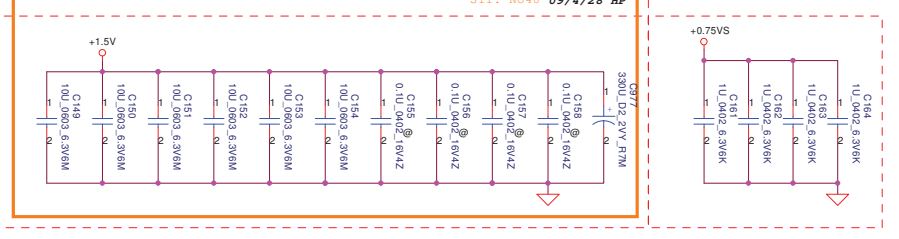
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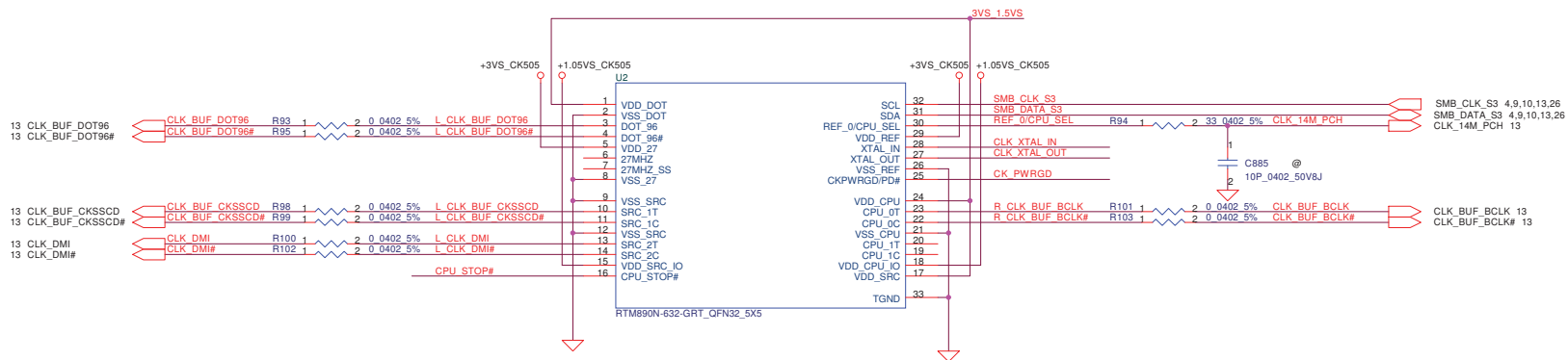
Layout Note:
Place near DIMMB

Layout Note:
Place near DIMM

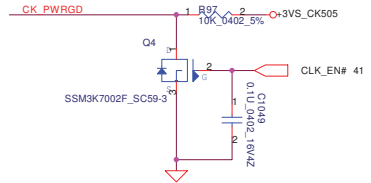
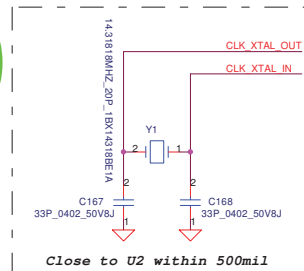
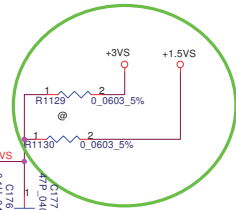
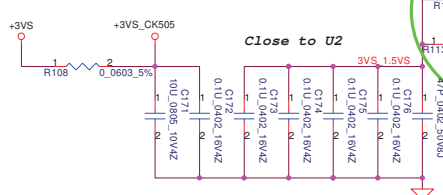
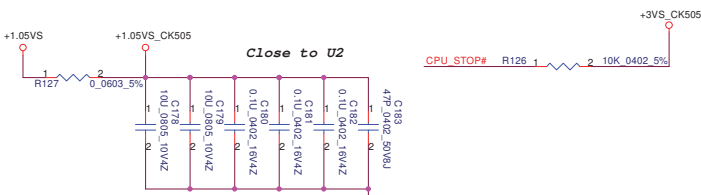


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DDRIII-SODIMM SLOT2		
Title		
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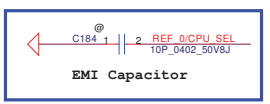


CLK Gen feature 1.5V support 6/29

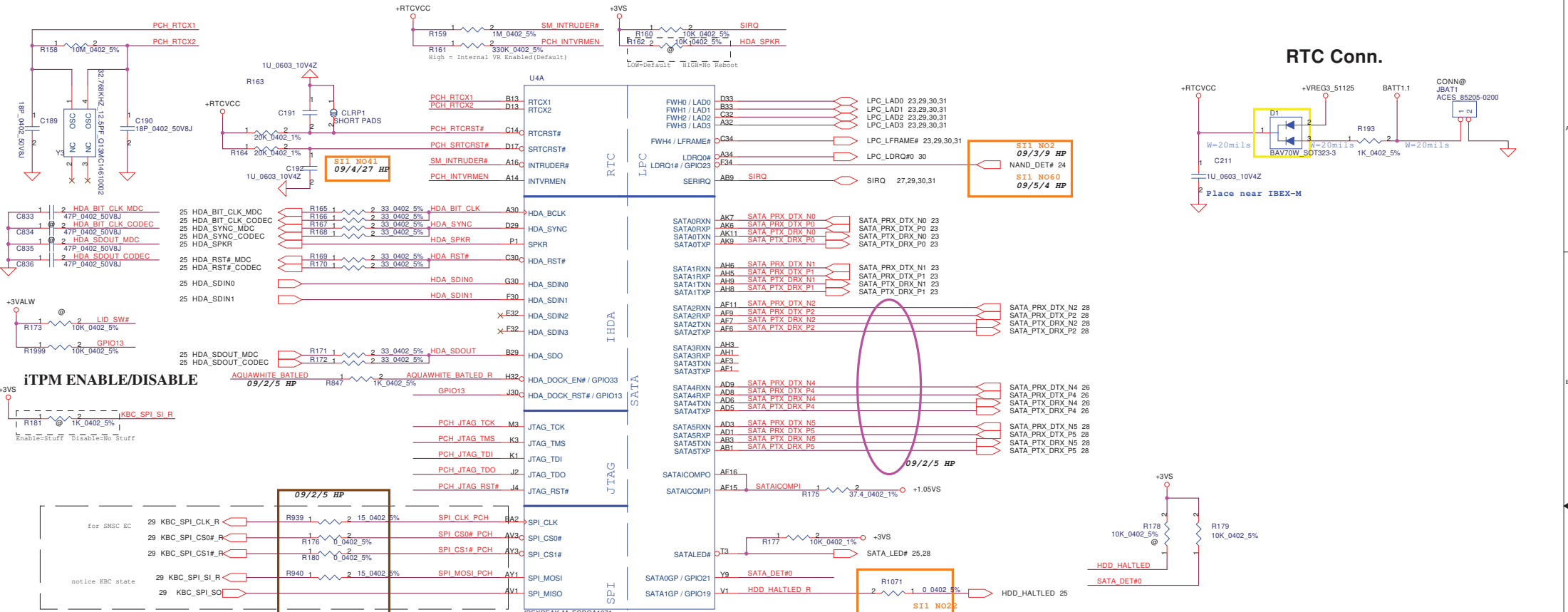


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

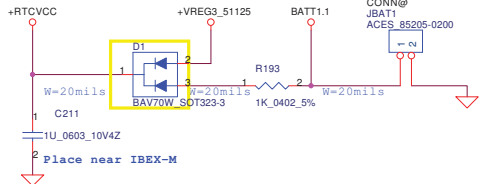
09/2/5 HP



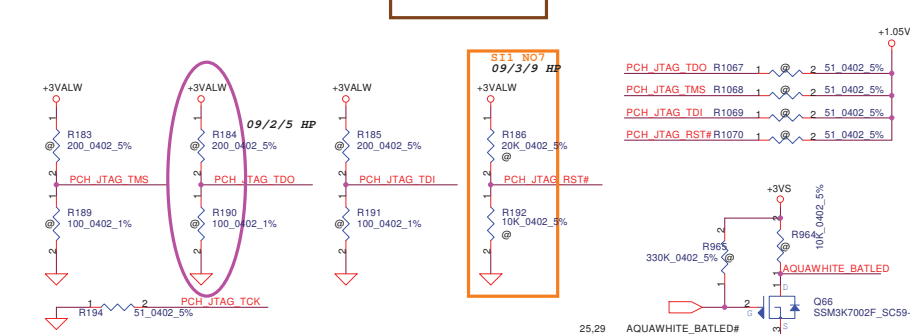
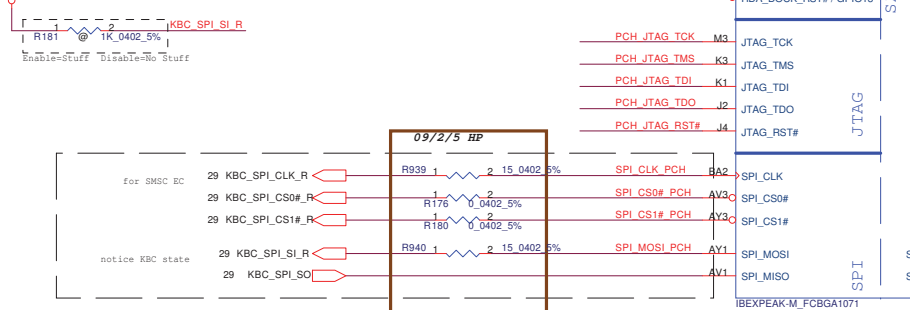
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc. CLOCK GENERATOR	
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RTC Conn.



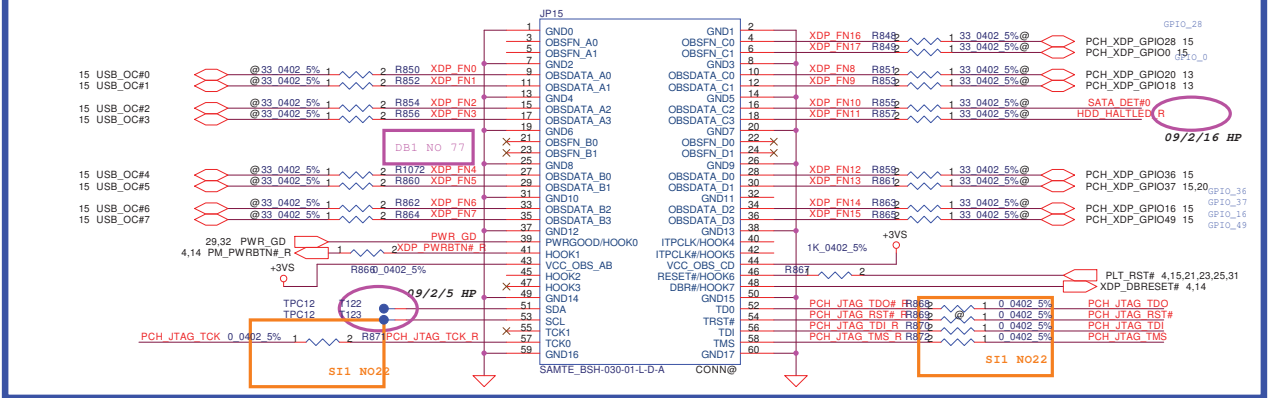
ITPM ENABLE/DISABLE



PCH Pin	Refdes	PCH JTAG Pre-Production	PCH JTAG Production
PCH_JTAG_TDO	R184	No Install	200ohm
PCH_JTAG_TDO	R190	No Install	100ohm
PCH_JTAG_TMS	R1067	No Install	No Install
PCH_JTAG_TMS	R183	200ohm	200ohm
PCH_JTAG_TMS	R189	100ohm	100ohm
PCH_JTAG_TDI	R1068	No Install	No Install
PCH_JTAG_TDI	R185	200ohm	200ohm
PCH_JTAG_TDI	R191	100ohm	100ohm
PCH_JTAG_TDI	R1069	No Install	No Install
PCH_JTAG_TDI	R194	51ohm	51ohm
PCH_JTAG_TCK	R186	20Kohm	20Kohm
PCH_JTAG_TCK	R192	20Kohm	20Kohm
PCH_JTAG_RST#	R192	10Kohm	10Kohm
PCH_JTAG_RST#	R1070	No Install	No Install
PCH_JTAG_RST#	R194	51ohm	51ohm

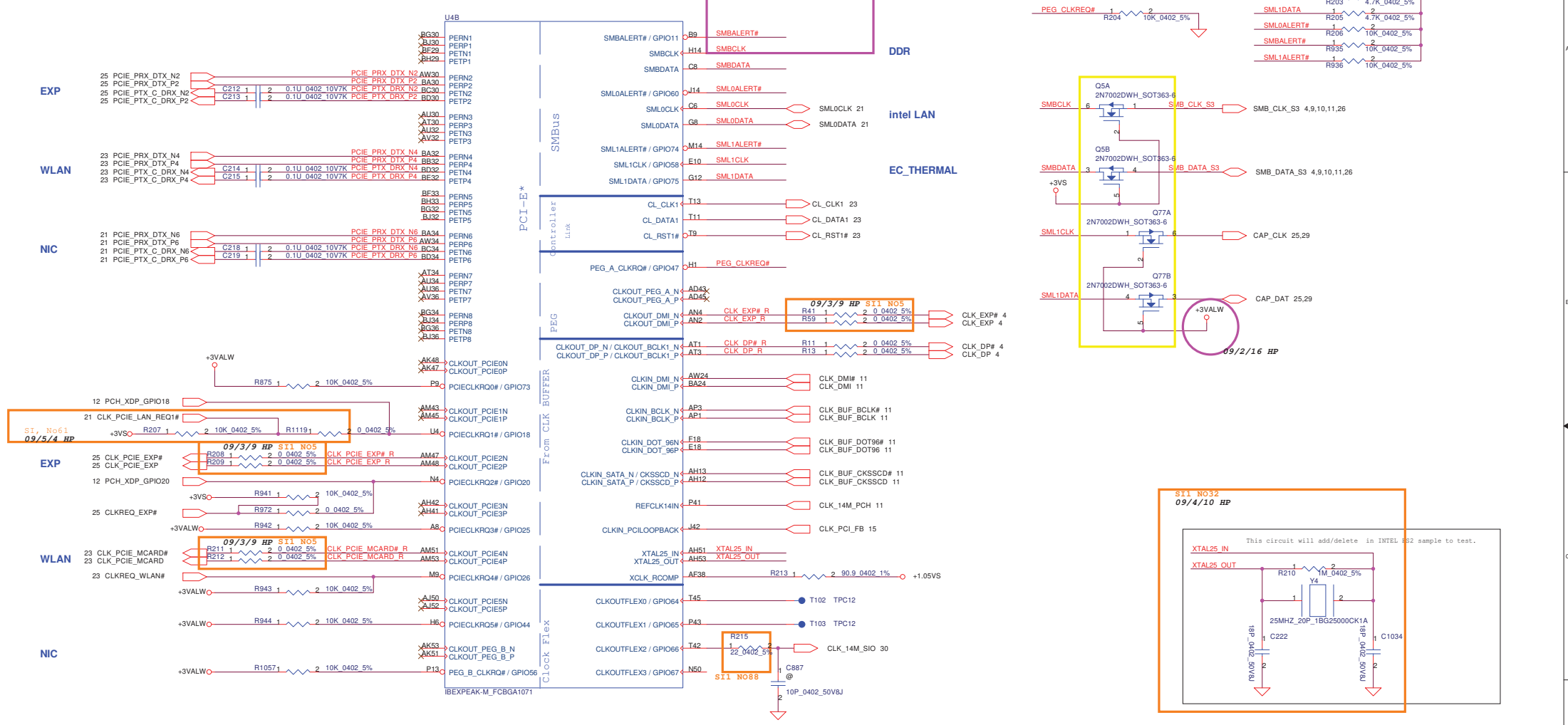
GPIO33	iAMT Enable /Disable
Hi	Disable
Lo	Enable Default

PCH XDP Conn.

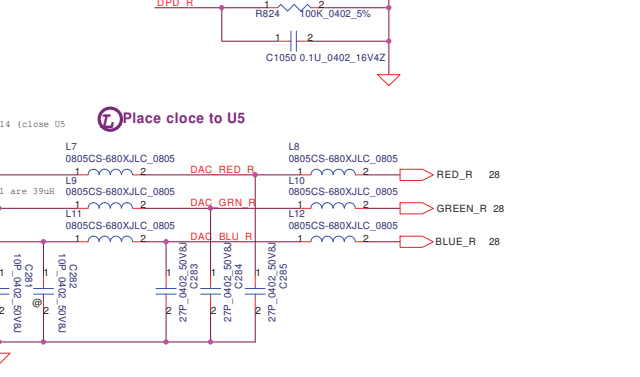
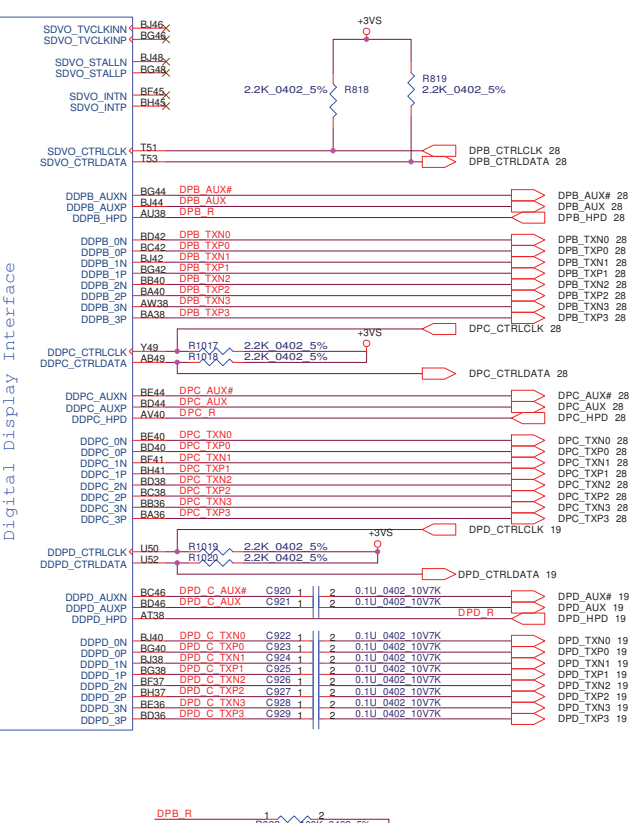
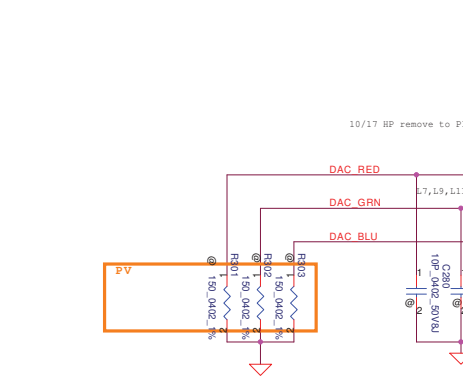
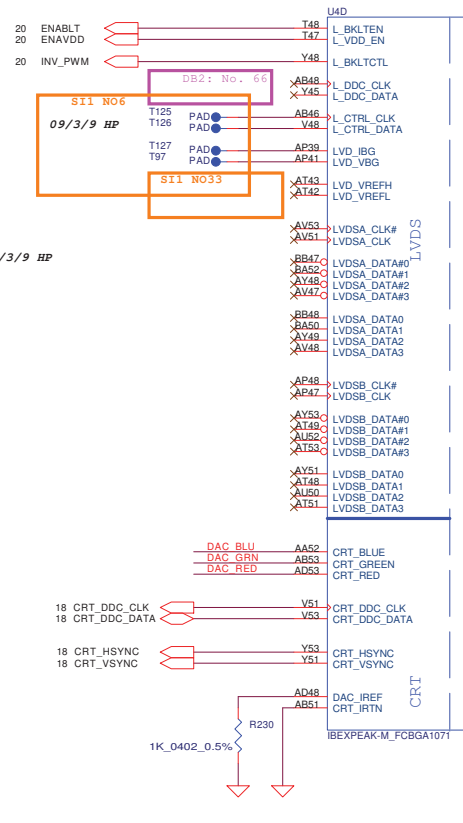
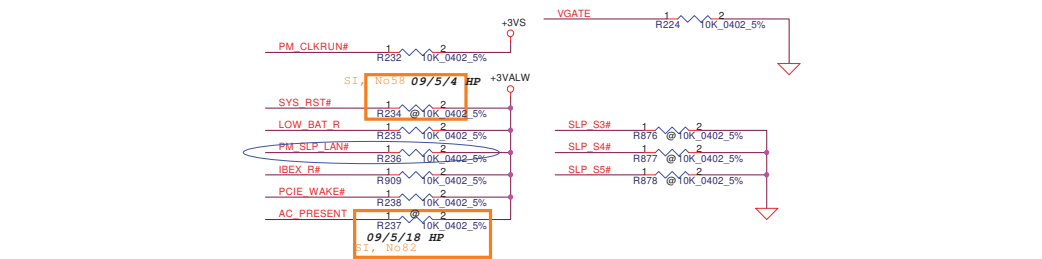
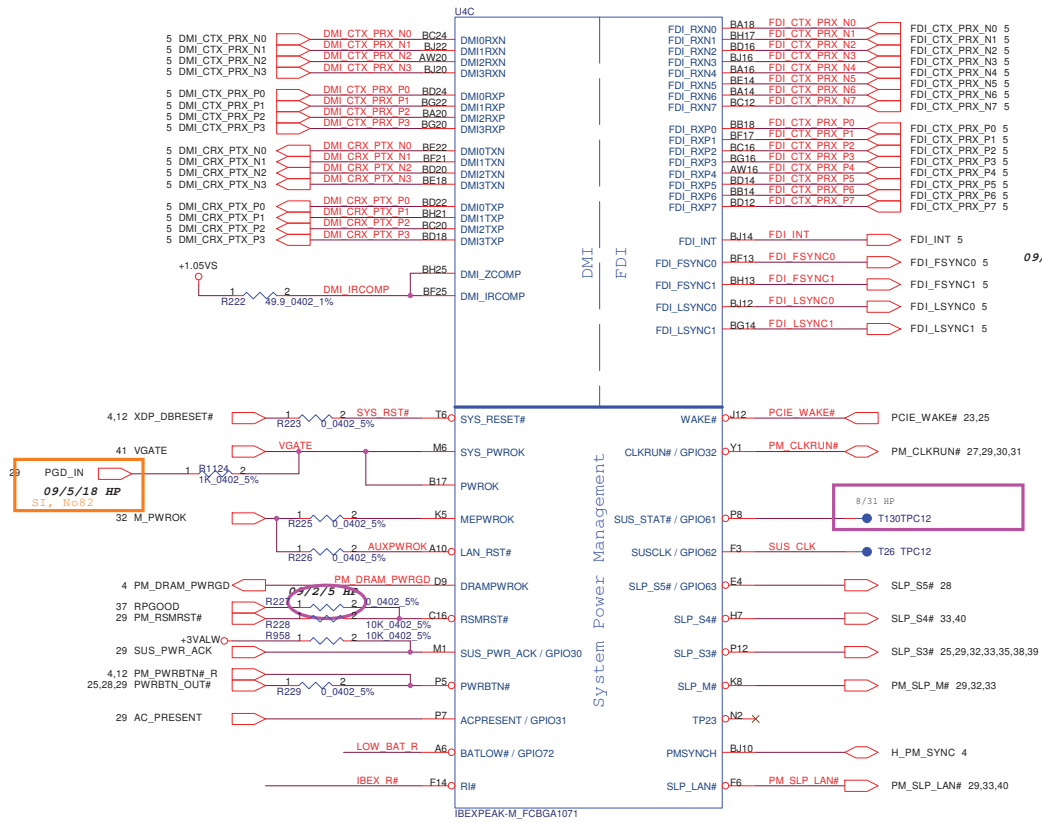


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Title IBEX-M(1/6)-HDA/JTAG/SATA		Rev 0.3
Size Document Number LA-4902P		Date: Wednesday, December 09, 2009 Sheet 12 of 47

8/31/2009 HP

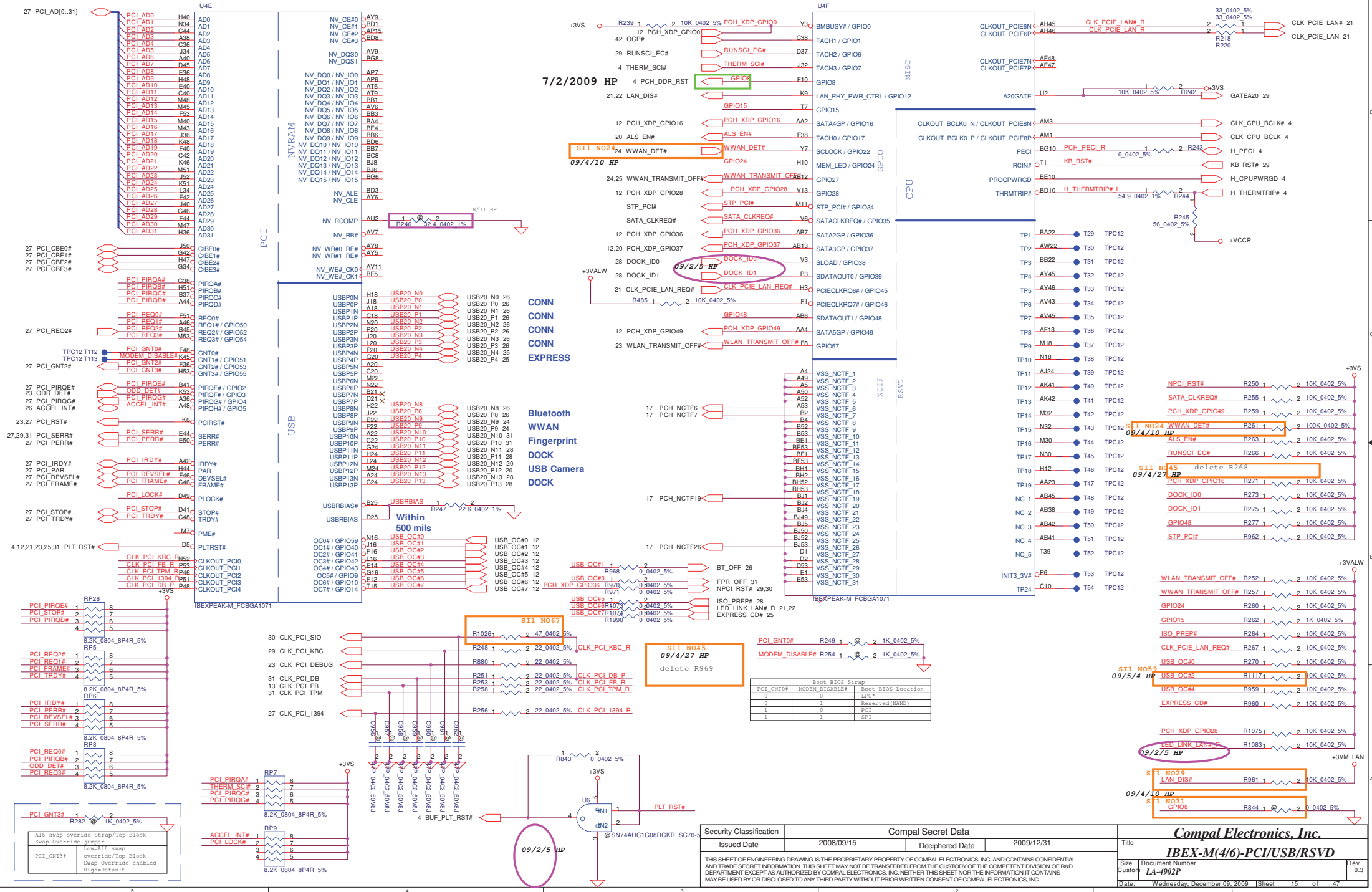


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Issued Date	2008/09/15	Deciphered Date	2009/12/31	IBEX-M(2/6)-PCI-E/SMBUS/CLK	
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Rev	0.3	Date	Wednesday, December 09, 2009	Sheet 14 of 47

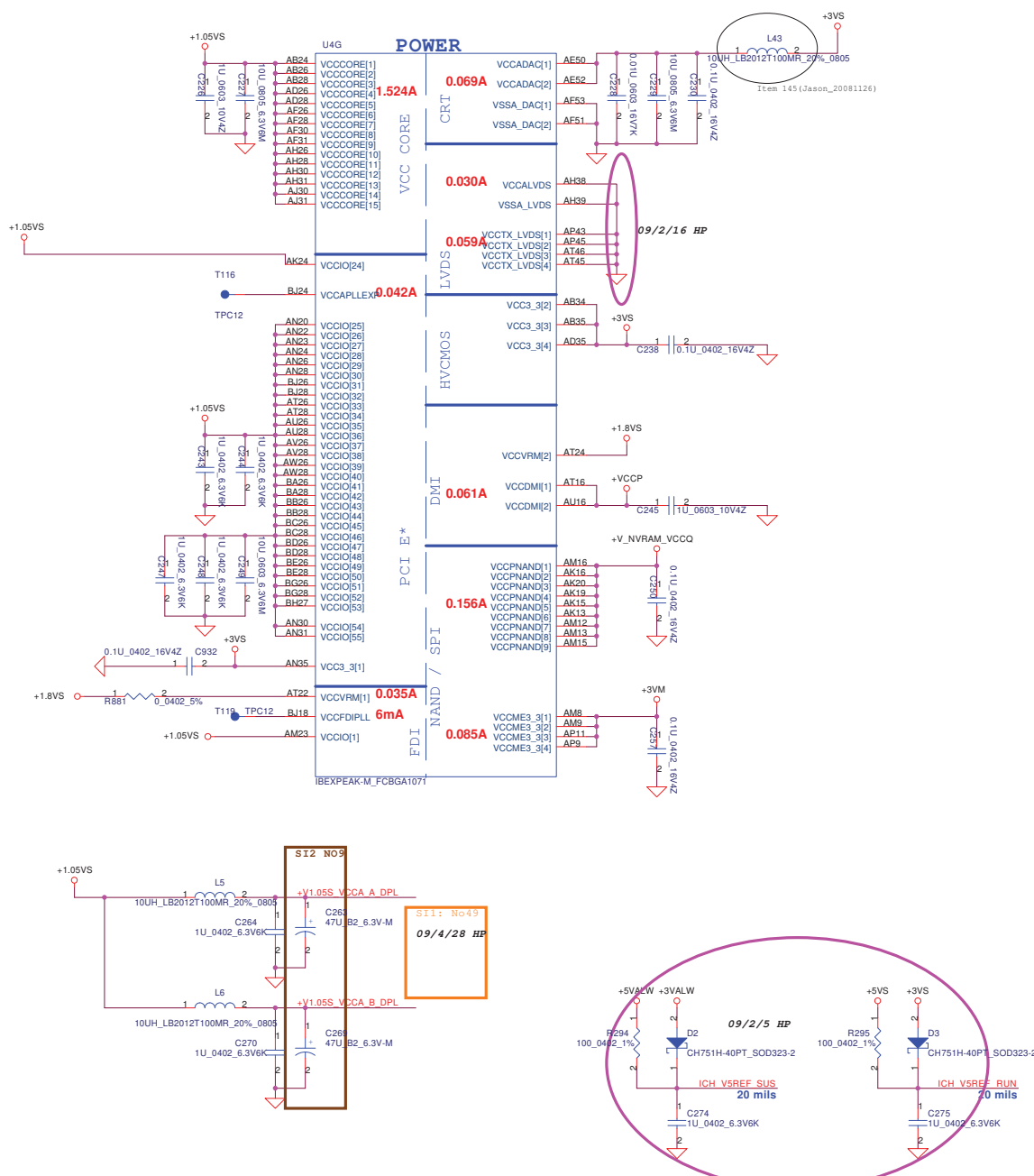
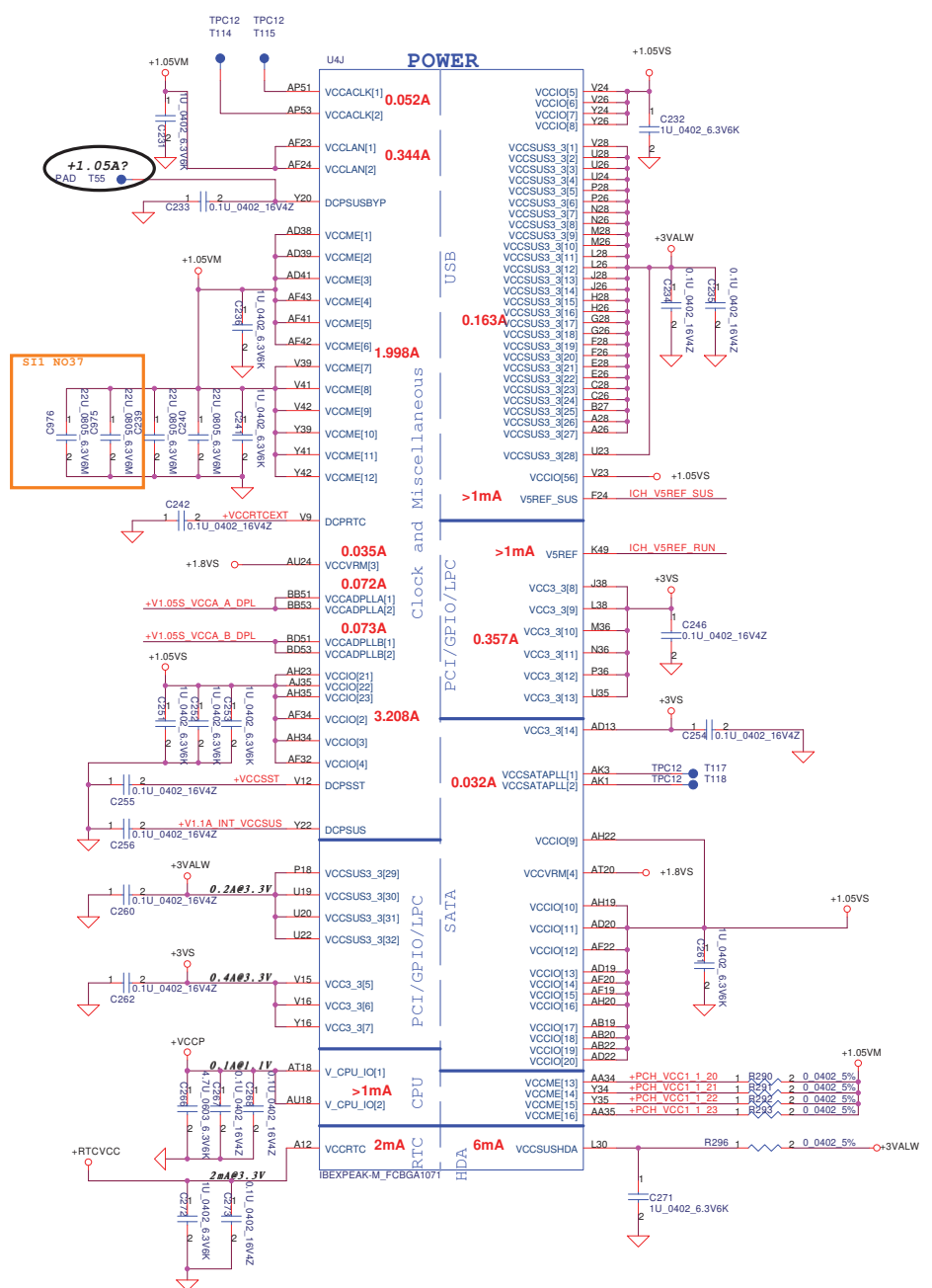
<http://laptop-motherboard-schematic.blogspot.com/>



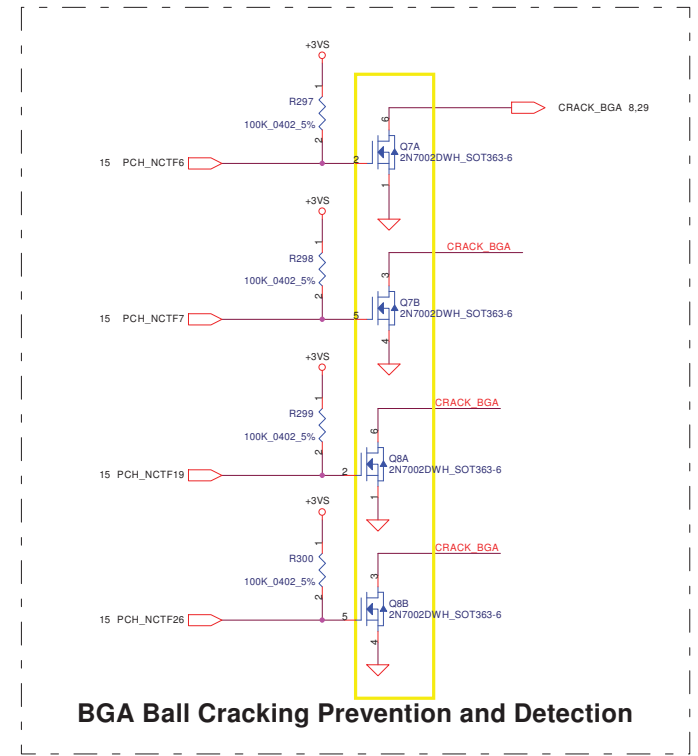
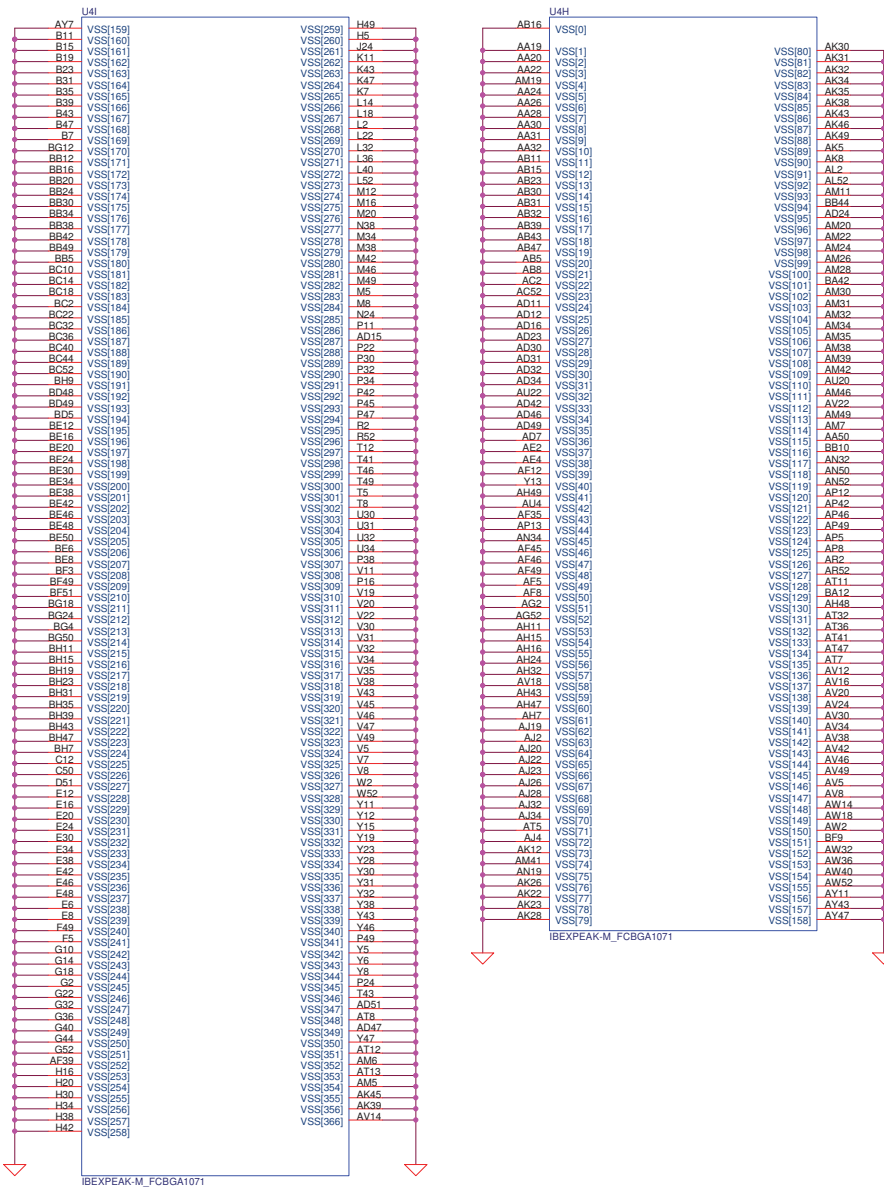
Security Classification	Compal Secret Data	
Issued Date	2008/09/15	Deciphered Date
2009/12/31		

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IBEX-M(4/6)-PCI/USB/RVSD			
Size	Document Number	Rev	
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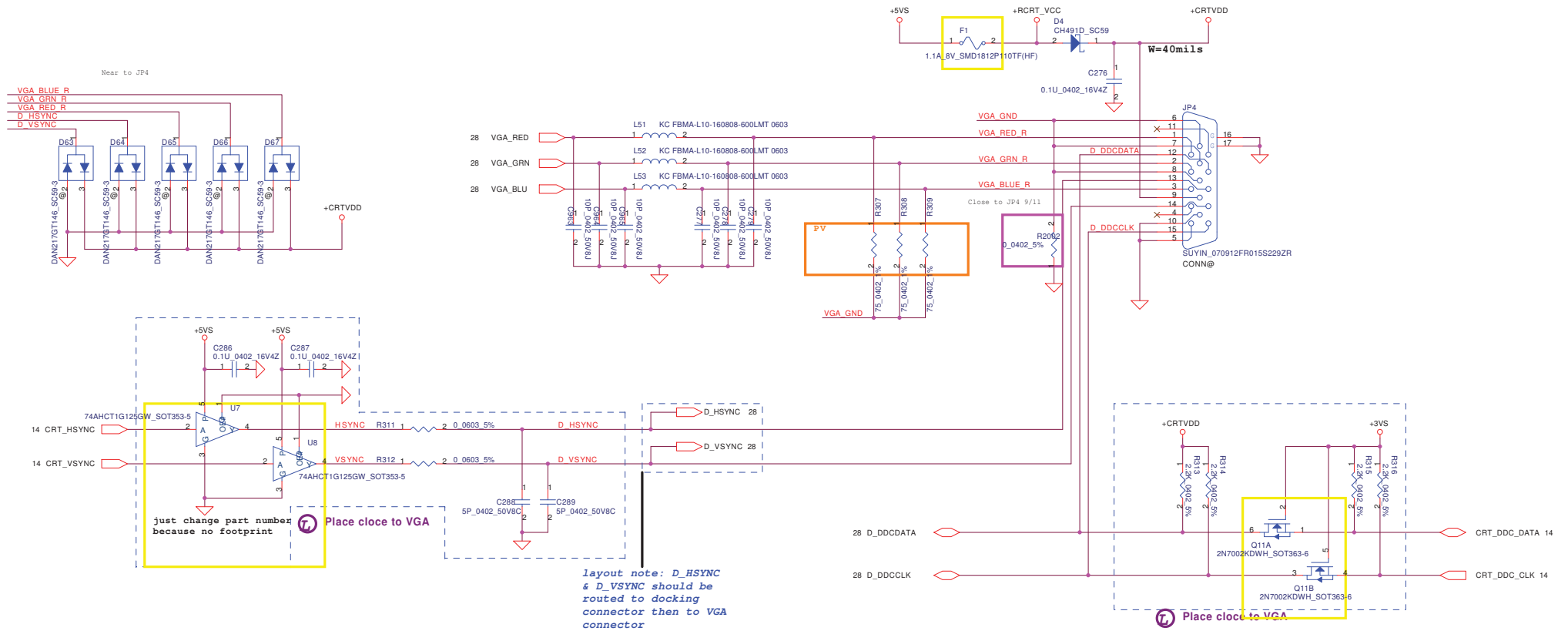


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Size	Document Number	Rev	
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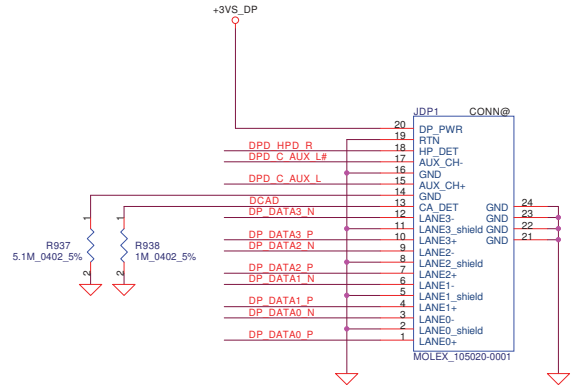
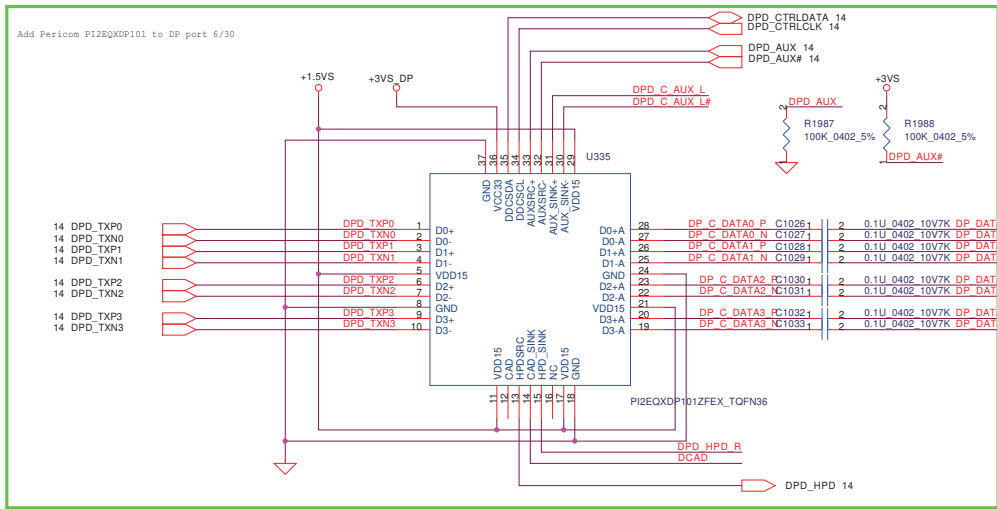
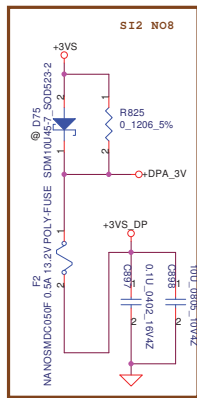
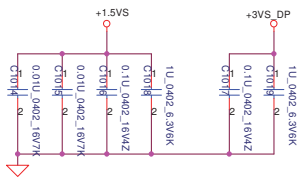


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CRT Connector

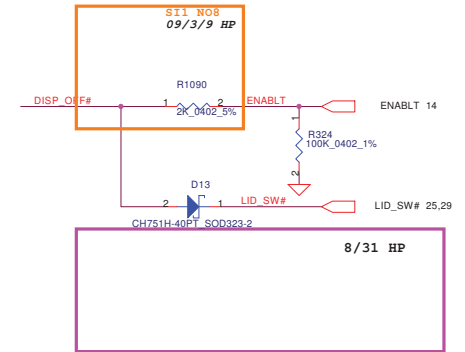
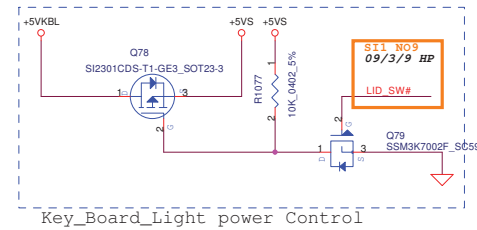
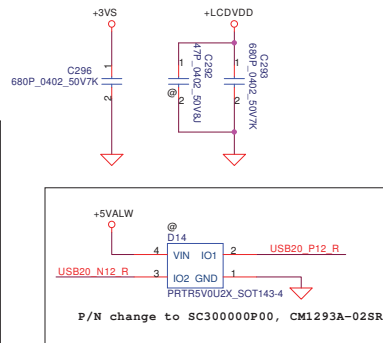
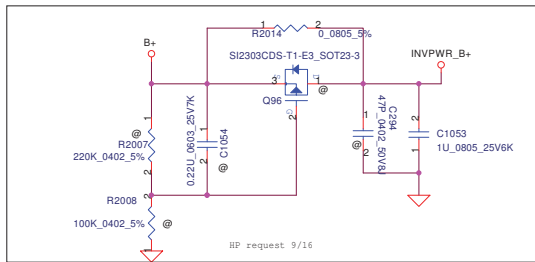


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				0.3
Date: Wednesday, December 03, 2009				Sheet 18 of 47

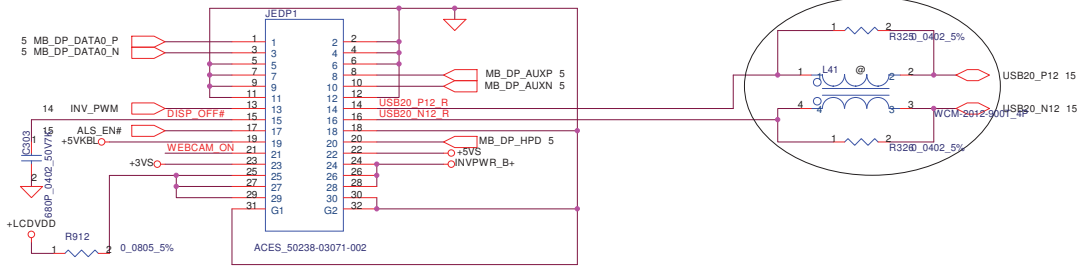


Change connecting eDP to PCH DP 11/24

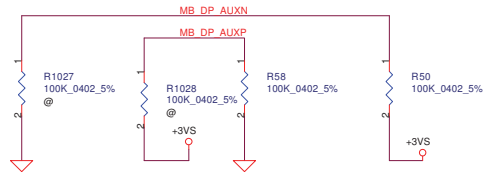
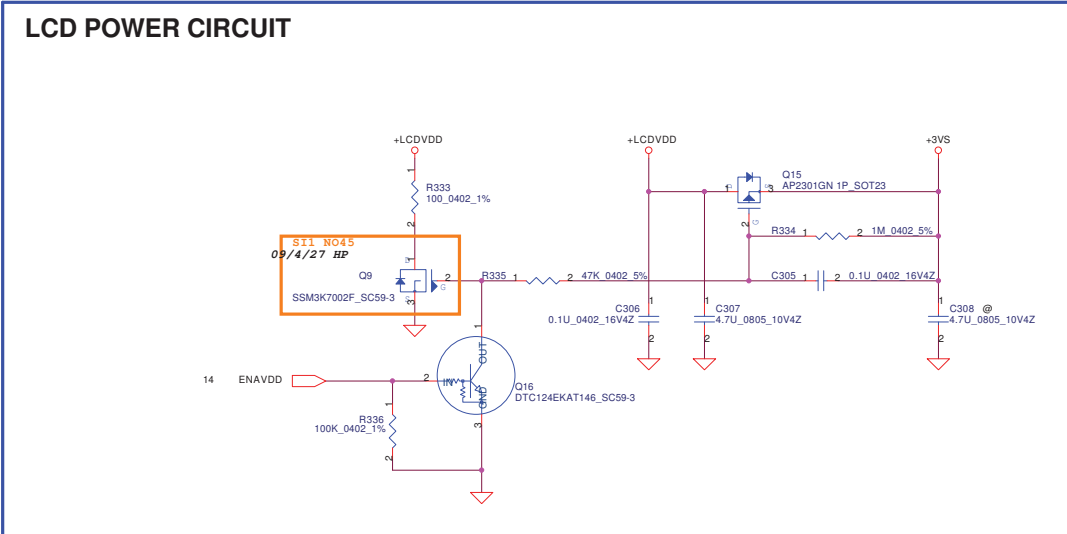
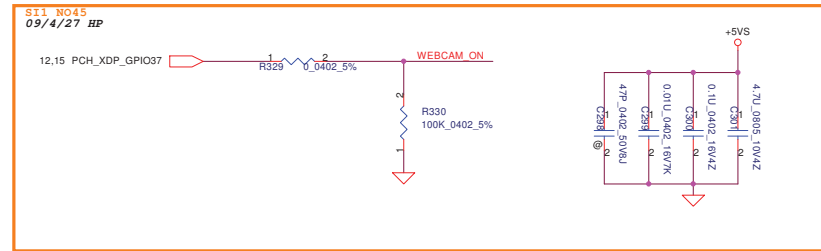
Security Classification	Compal Secret Data		Title	
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Size	Document Number	Rev		0.3
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Date:	Wednesday, December 03, 2009	Sheet	19	of 47



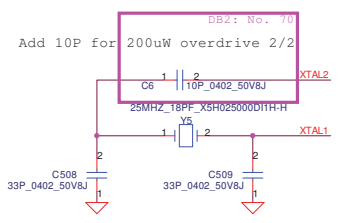
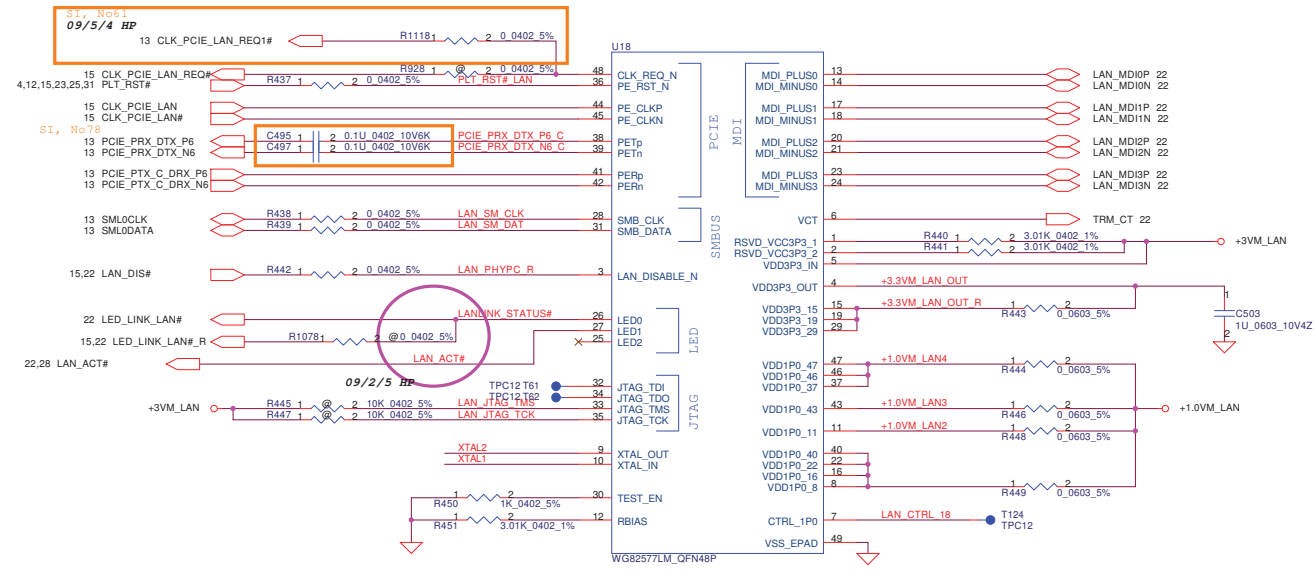
LCD/PANEL BD. CONN.



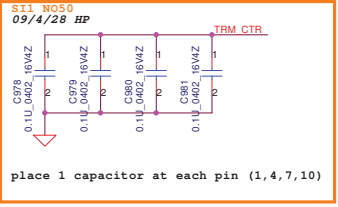
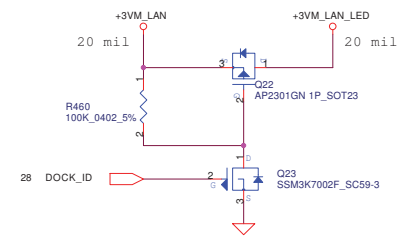
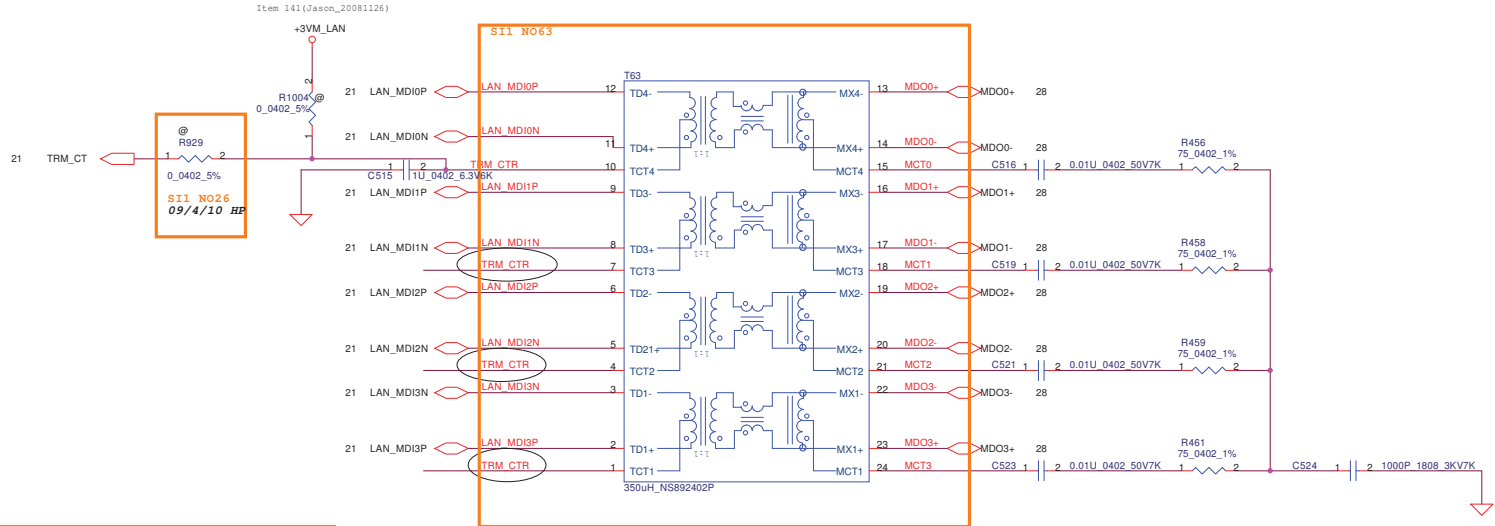
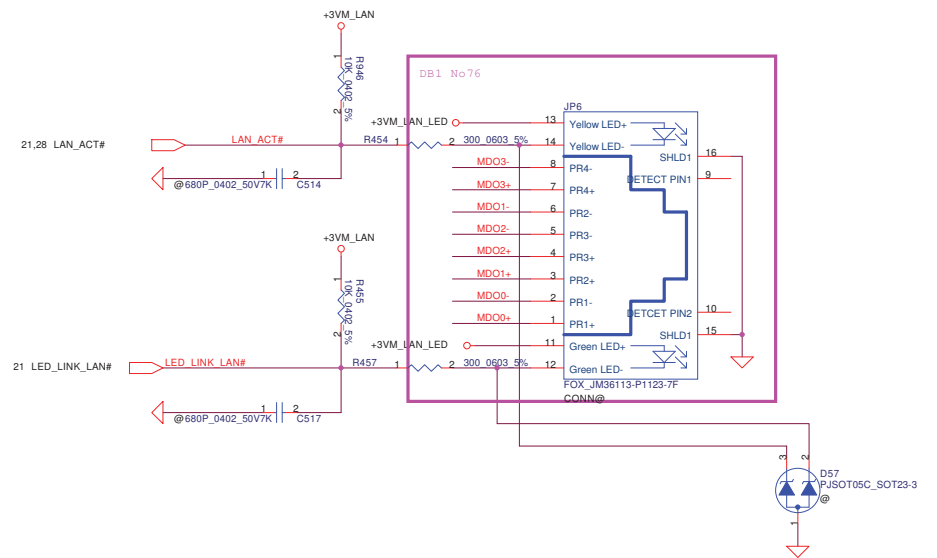
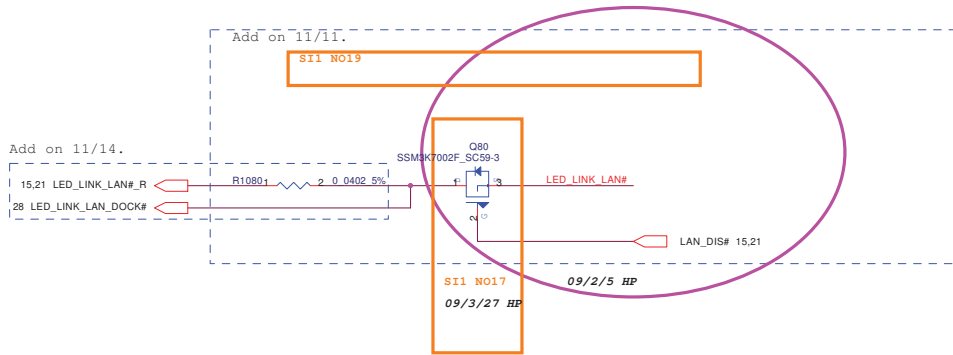
Change eDP LCD connector to 30pin for Coaxial cable 9/13



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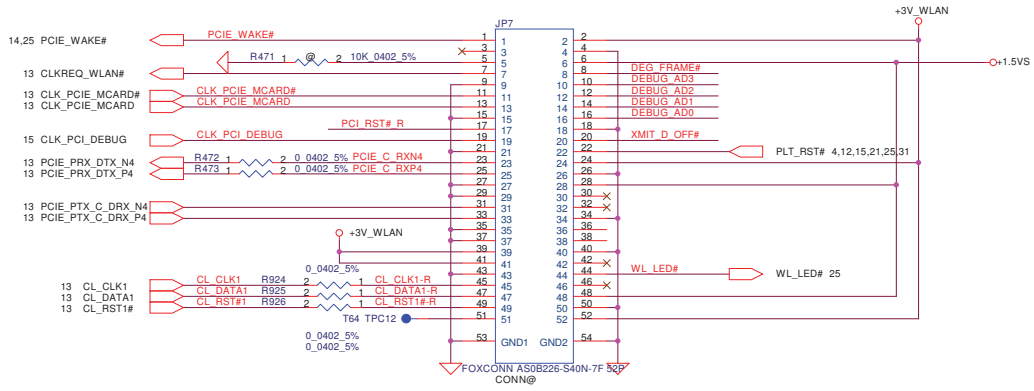
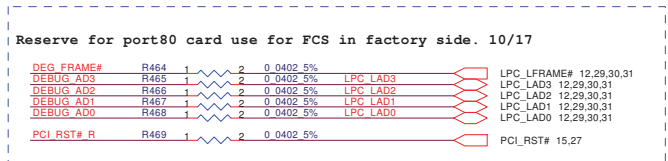
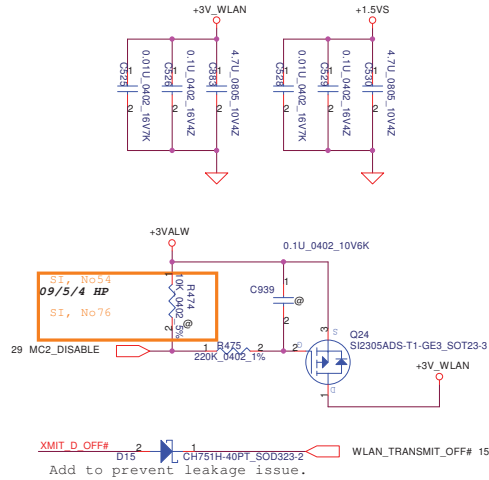


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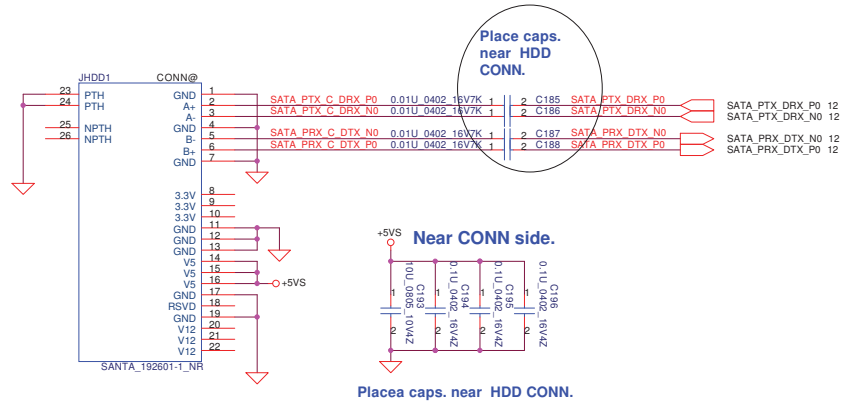


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Size	Document Number	Rev	Date	Sheet	of
	LA-4902P	0.3	Wednesday, December 09, 2009	22	47

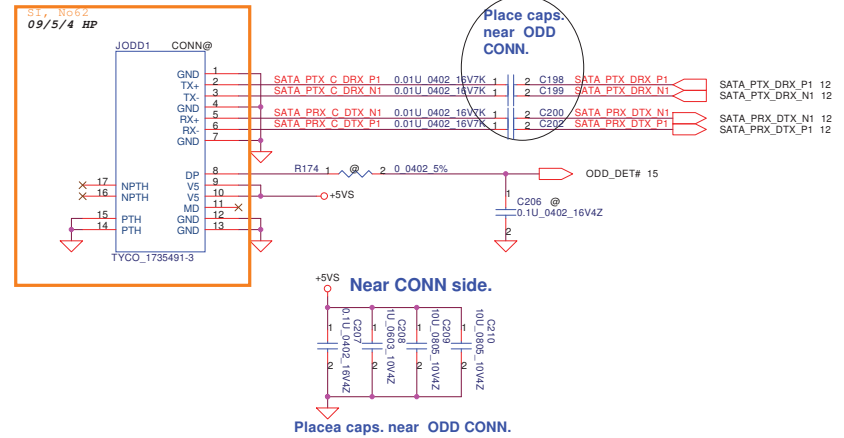
WLAN (Half mini Card)



SATA HDD CONN.

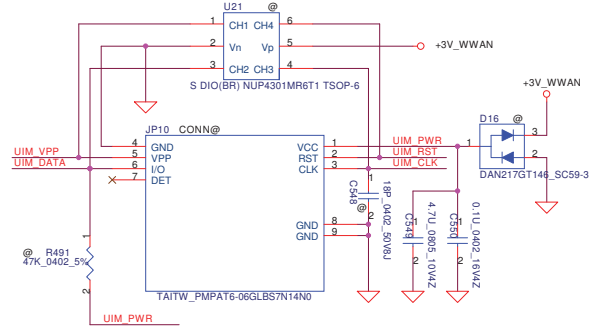
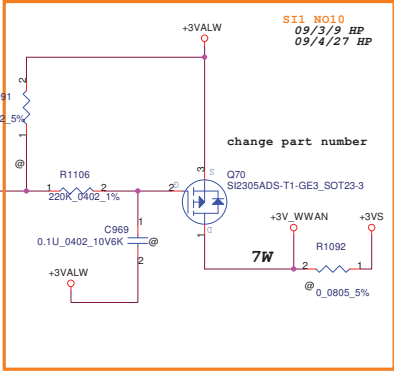
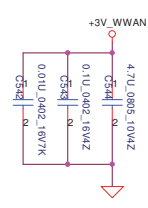
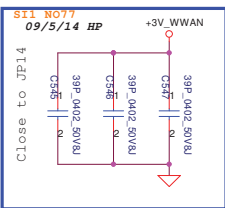
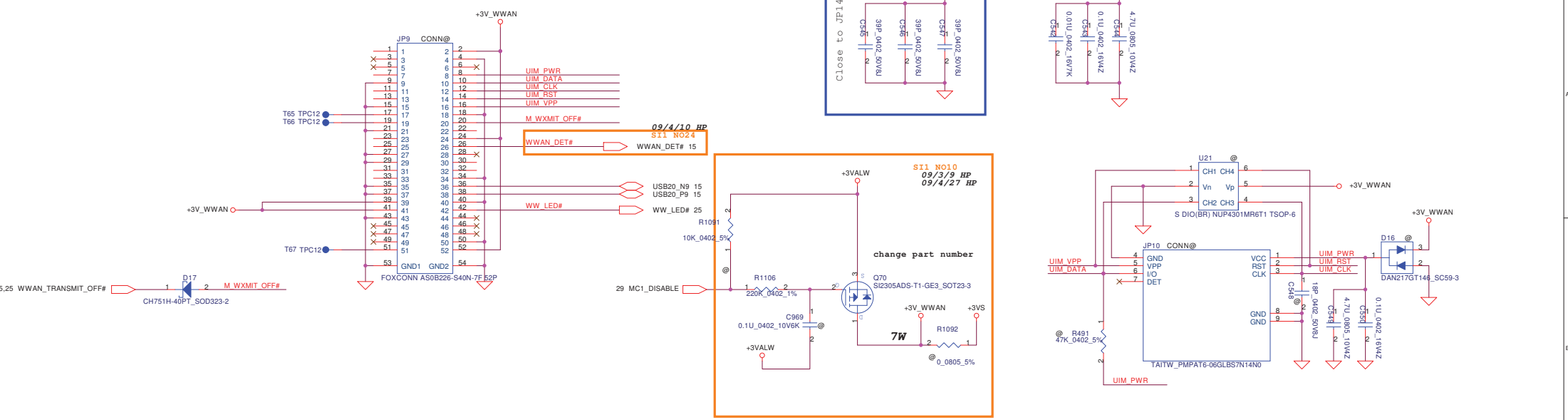


SATA ODD CONN.

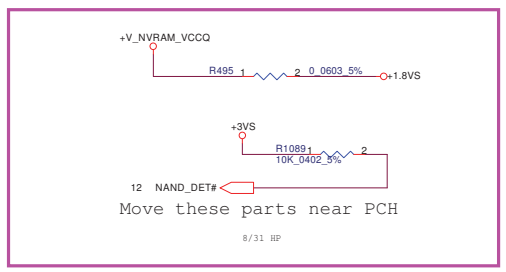


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WWAN (Full mini Card)

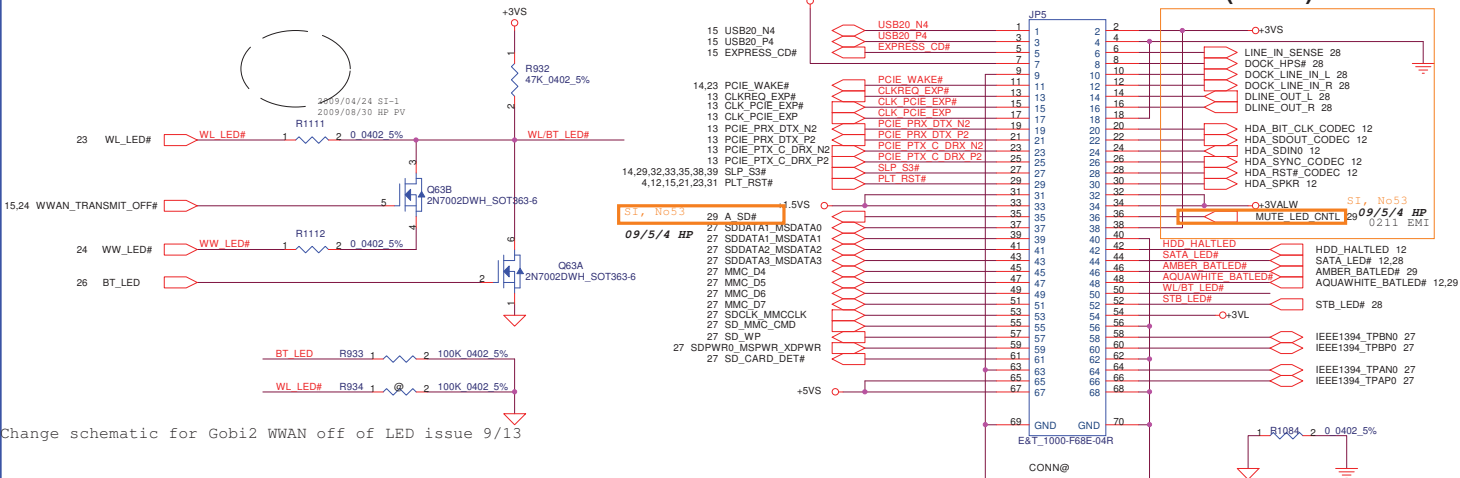


NAND

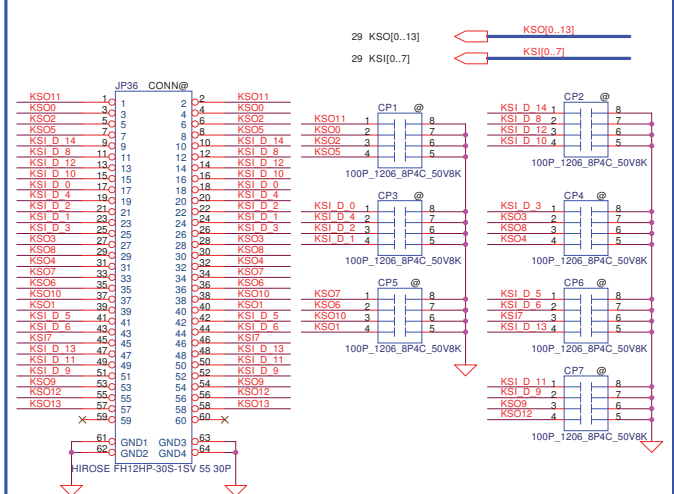


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Issued Date	2008/09/15	Deciphered Date		2009/12/31	WWAN/NAND
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Size	Document Number	Rev		Date	
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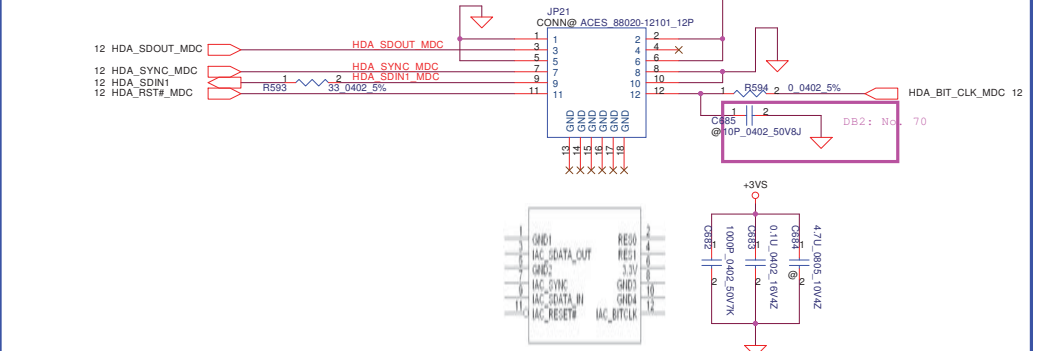
AUDIO BOARD CONNECTOR (MALE)



INT_KBD CONN.



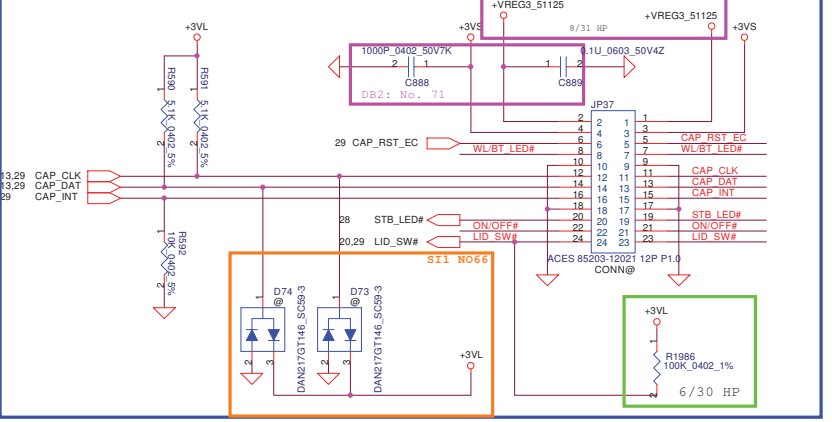
MDC 1.5 Conn.



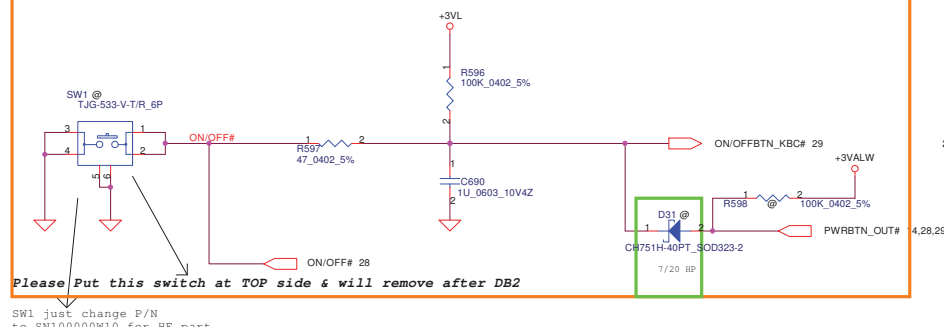
T/P BOARD.



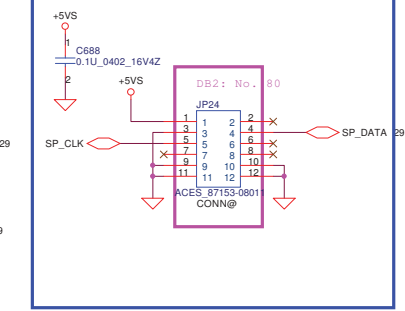
CAP SWITCH BOARD



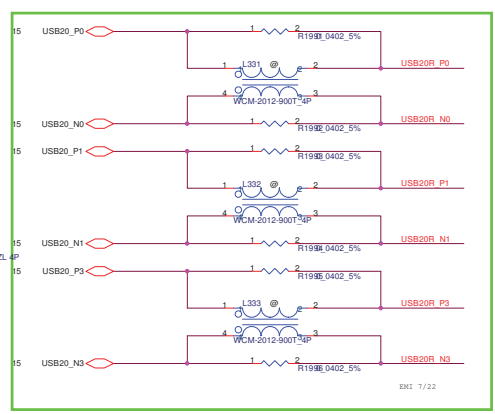
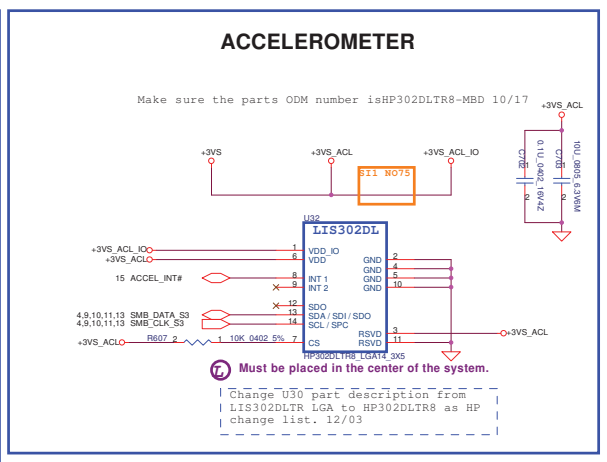
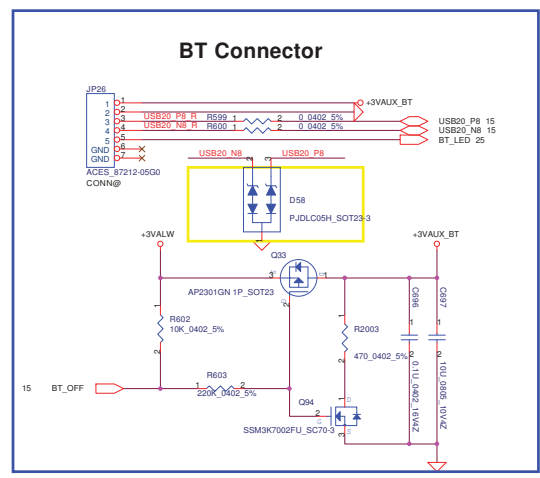
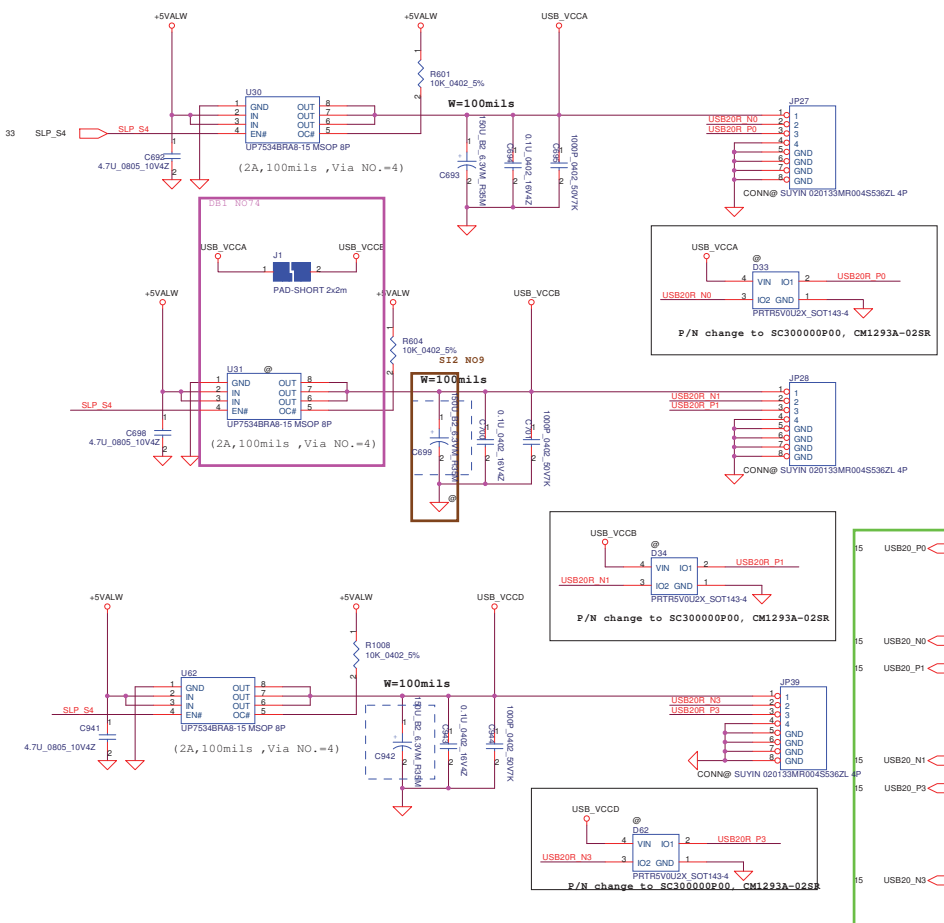
Power Button



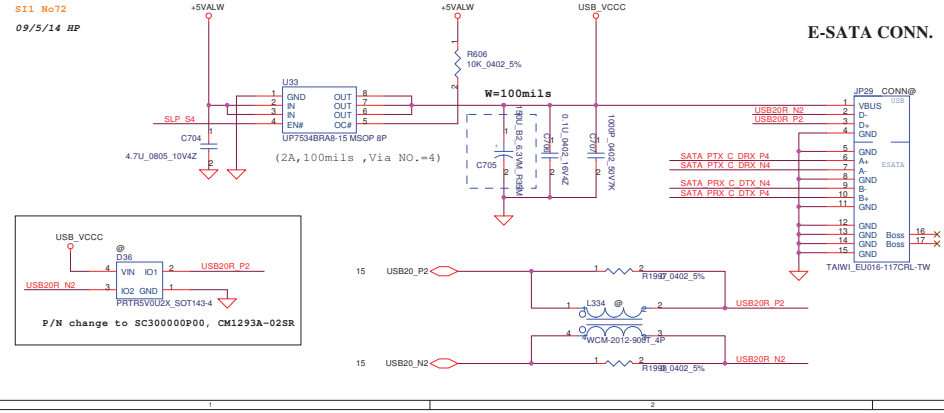
TrackPoint CONN.



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Issued Date	2008/09/15	Deciphered Date	2009/12/31	MDC/KBD/ON OFF/LID	
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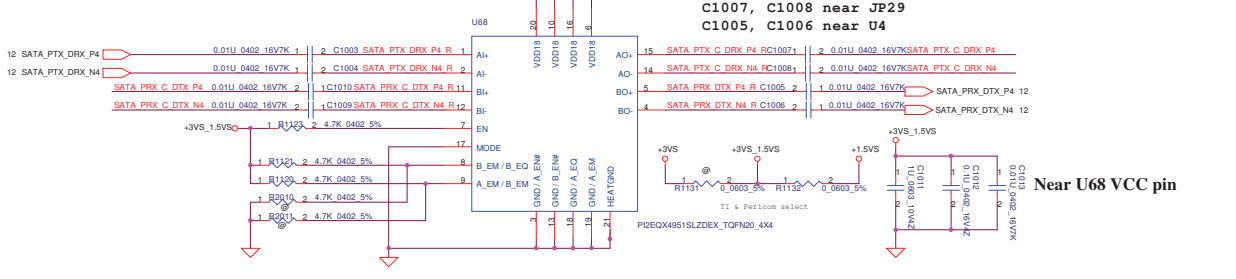


ESATA function

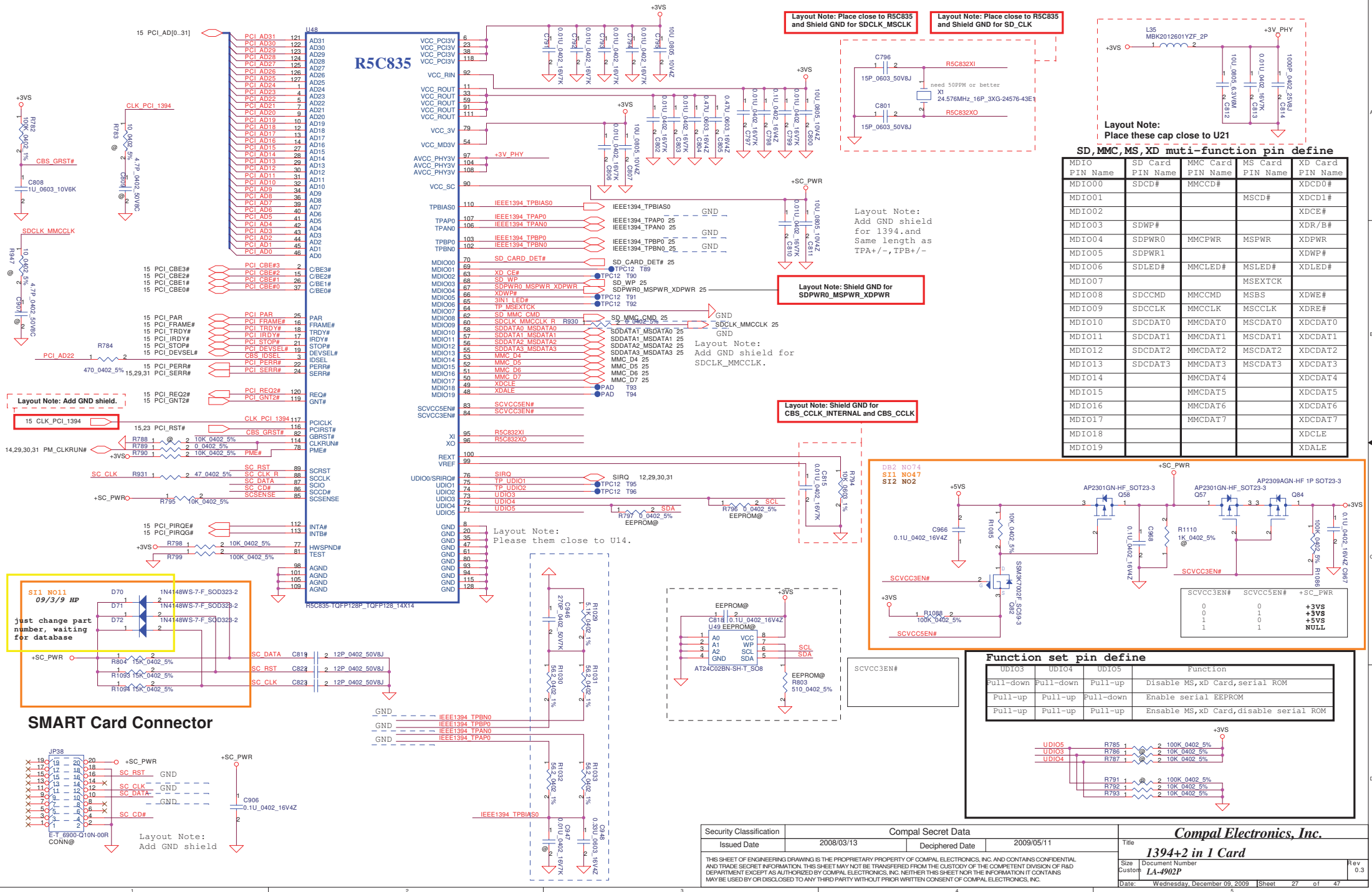


Change TI to Pericom PI3EQX4951ST_PEND
And add 1.5 power rail option 6/30

SATA Redriver

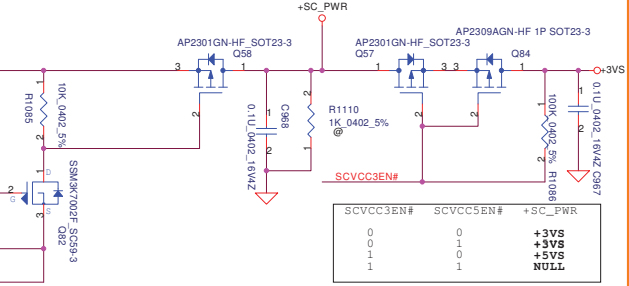


Security Classification	Compal Secret Data		Title Compal Electronics, Inc. USB & BT Connector & Acclerometer
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Date: Wednesday, December 09, 2009 12:28:47			Sheet 26 of 47



SD, MMC, MS, XD multi-function pin define

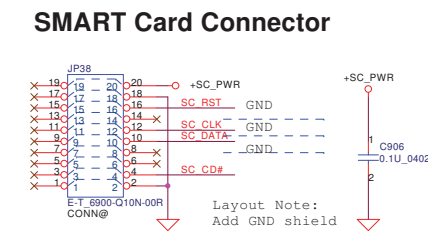
MDIO	SD Card	MMC Card	MS Card	XD Card
PIN Name	PIN Name	PIN Name	PIN Name	PIN Name
MDIO00	SDCD#	MMCCD#	MSCD#	XDCD0#
MDIO01				XDCD1#
MDIO02			XDR/B#	XDCD2#
MDIO03	SDWP#			XDCD3#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLEd#	MSLEd#	XDLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE



Function set pin define

UDIO3	UDIO4	UDIO5	Function
Pull-down	Pull-down	Pull-up	Disable MS, xD Card, serial ROM
Pull-up	Pull-up	Pull-up	Enable serial EEPROM
Pull-up	Pull-up	Pull-up	Enable MS, xD Card, disable serial ROM

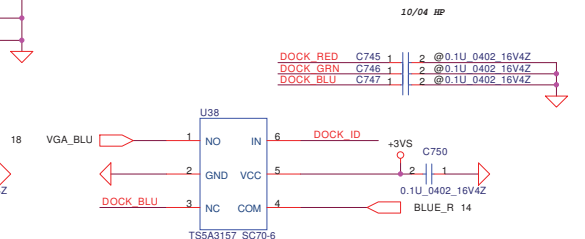
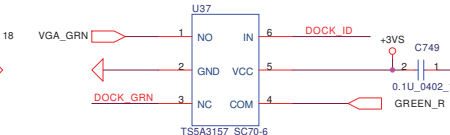
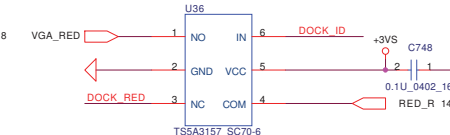
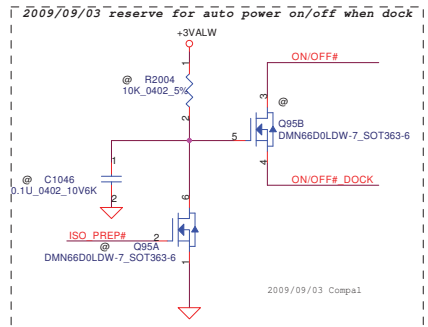
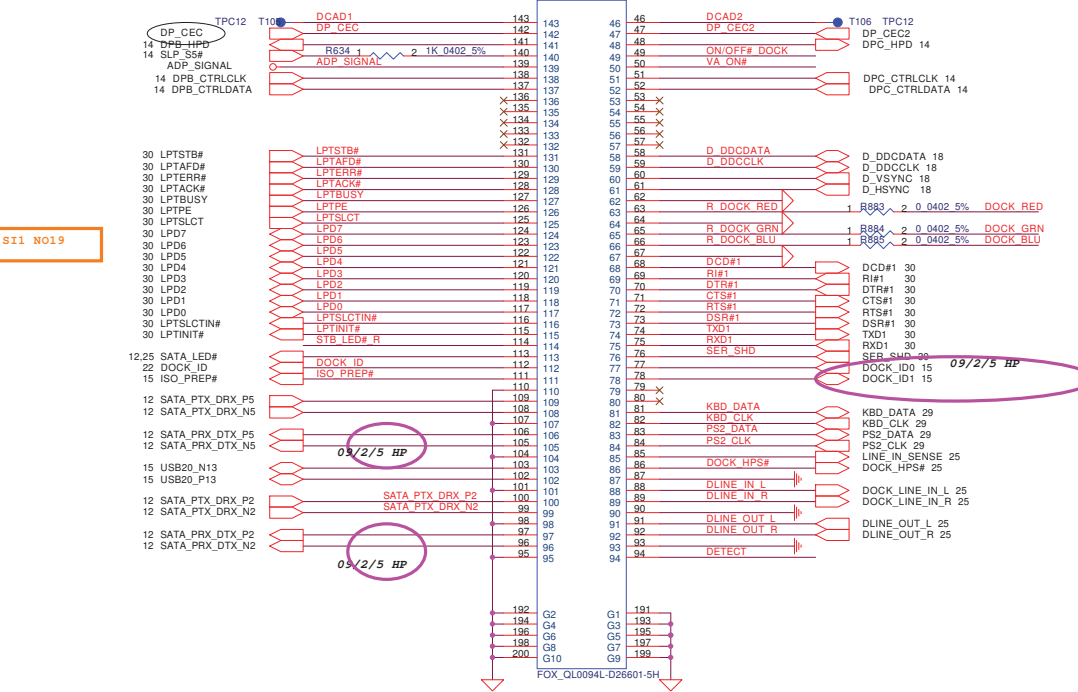
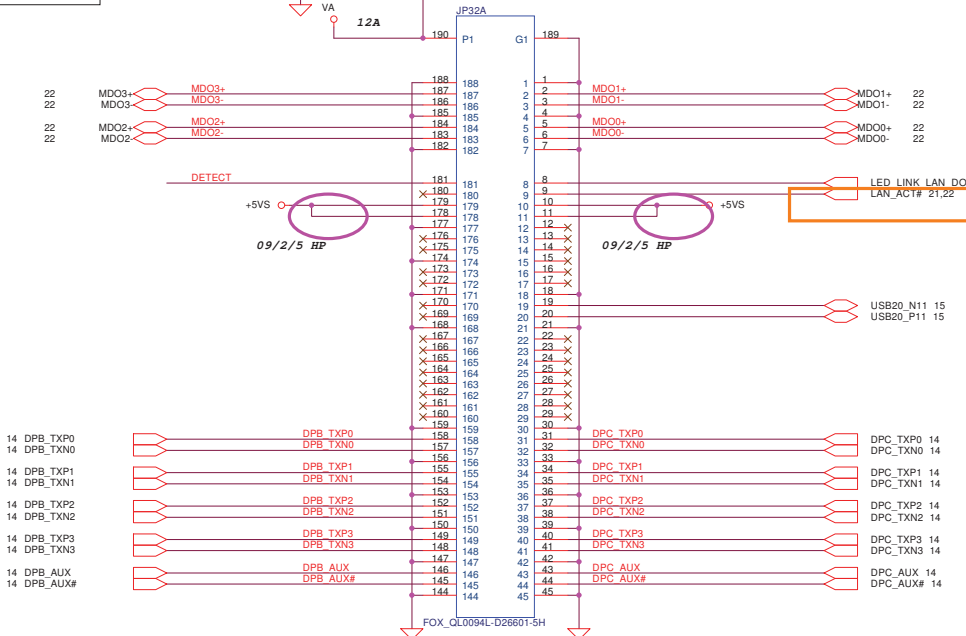
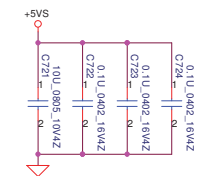
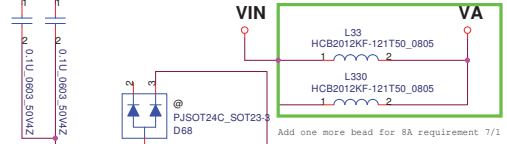
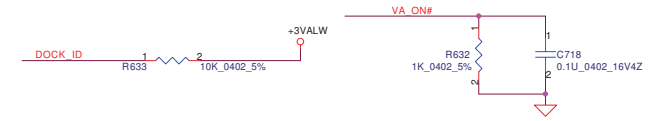
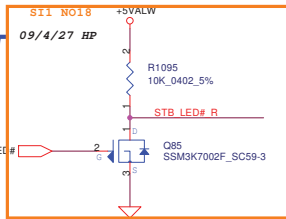
Pin connections for UDIO3, UDIO4, and UDIO5 are shown with pull-up/down resistors (R785, R786, R787, R791, R792, R793).



- (1) PCI Express x1 channels
- (2) PS/2 Interfaces
- (2) USB 2.0 channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface

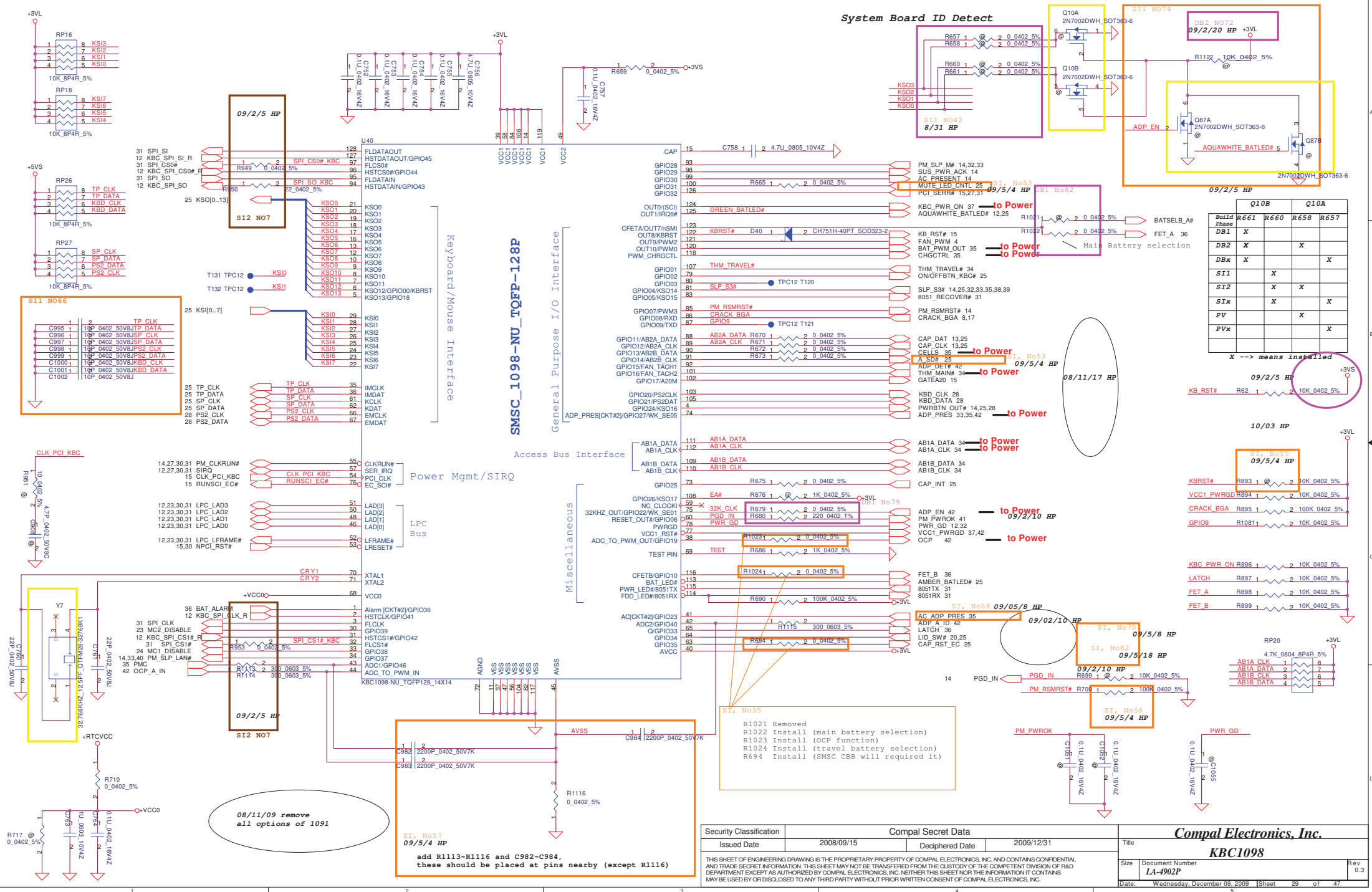
DOCK CONN. 184PIN

DOCKING CONNECT

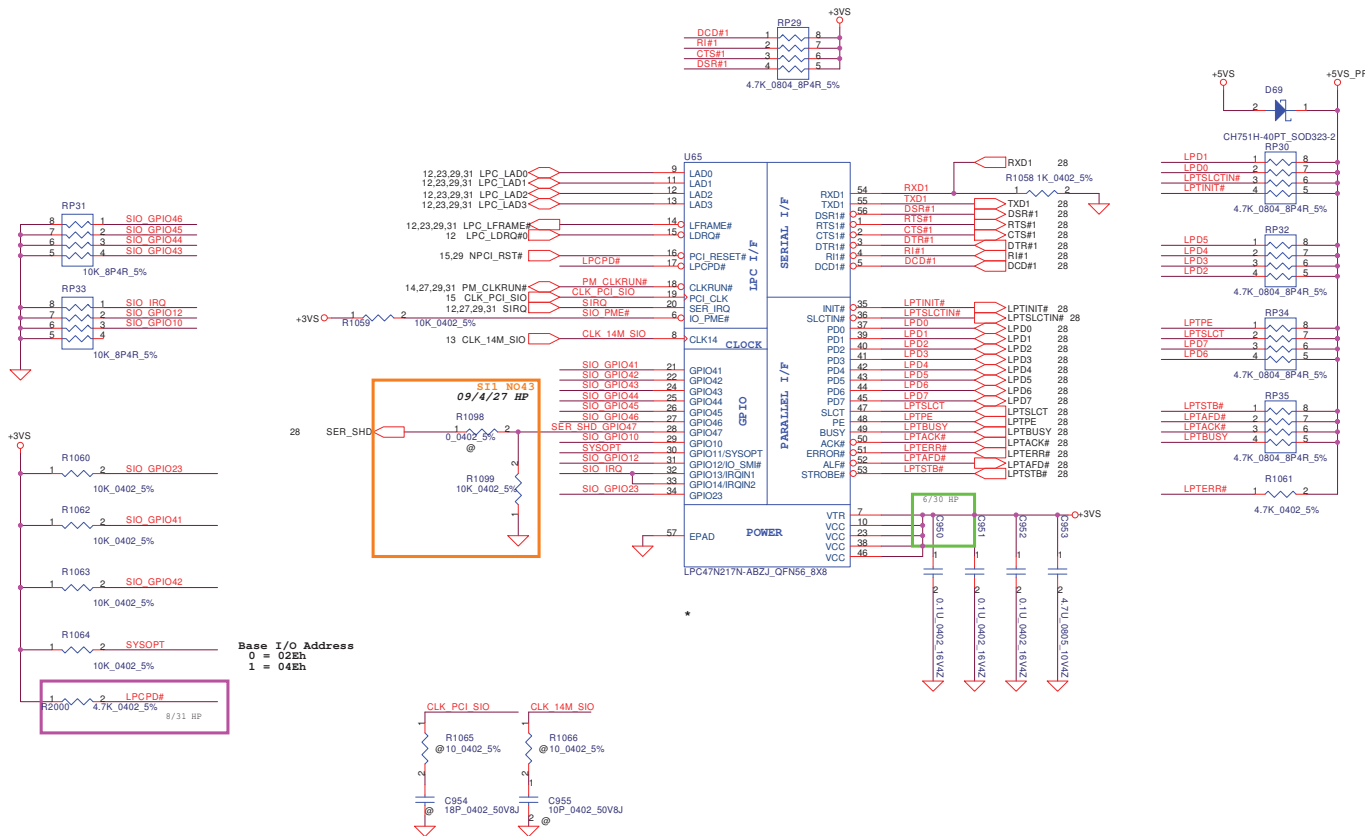


	IN	NC<-->COM	NO<-->COM
L	ON		OFF
H	OFF		ON

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	LA-4902P	0.3		
Date:	Wednesday, December 09, 2009	Sheet	28	of 47



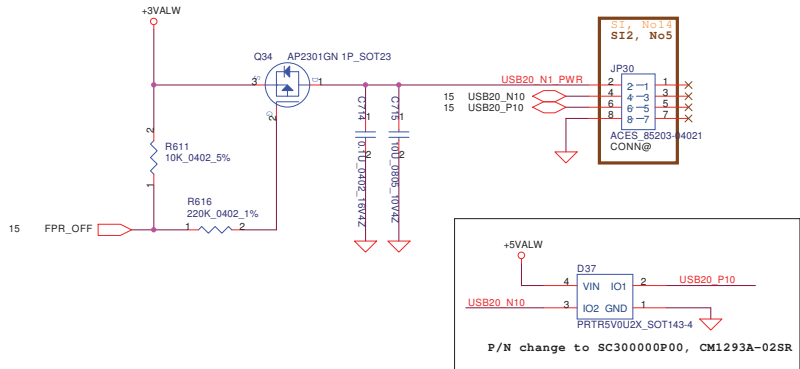
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Date:	Wednesday, December 09, 2009	Sheet	29 of 47



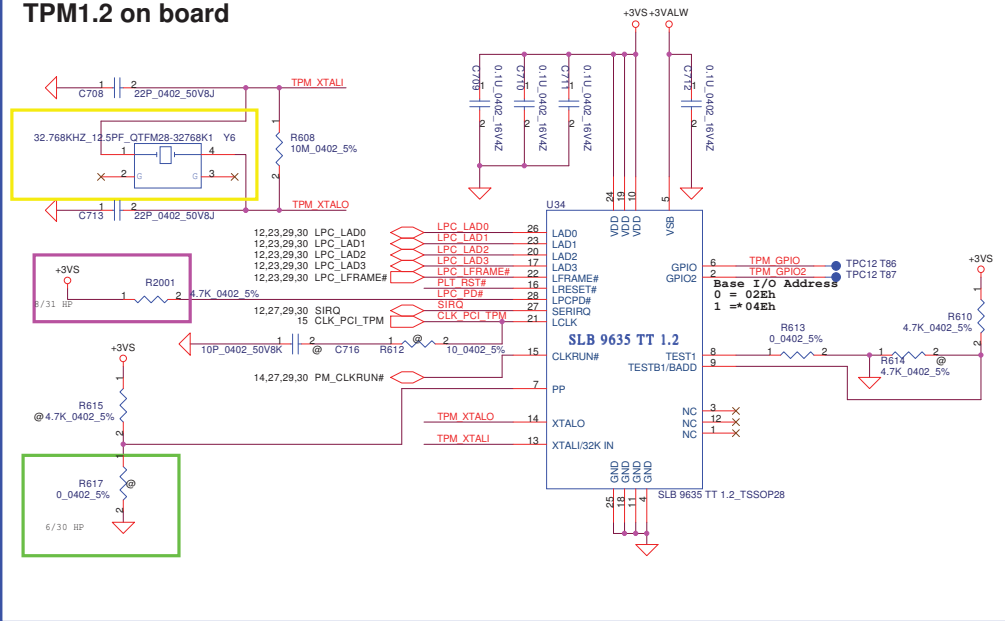
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Date:	Wednesday, December 09, 2009	Sheet	30	of 47

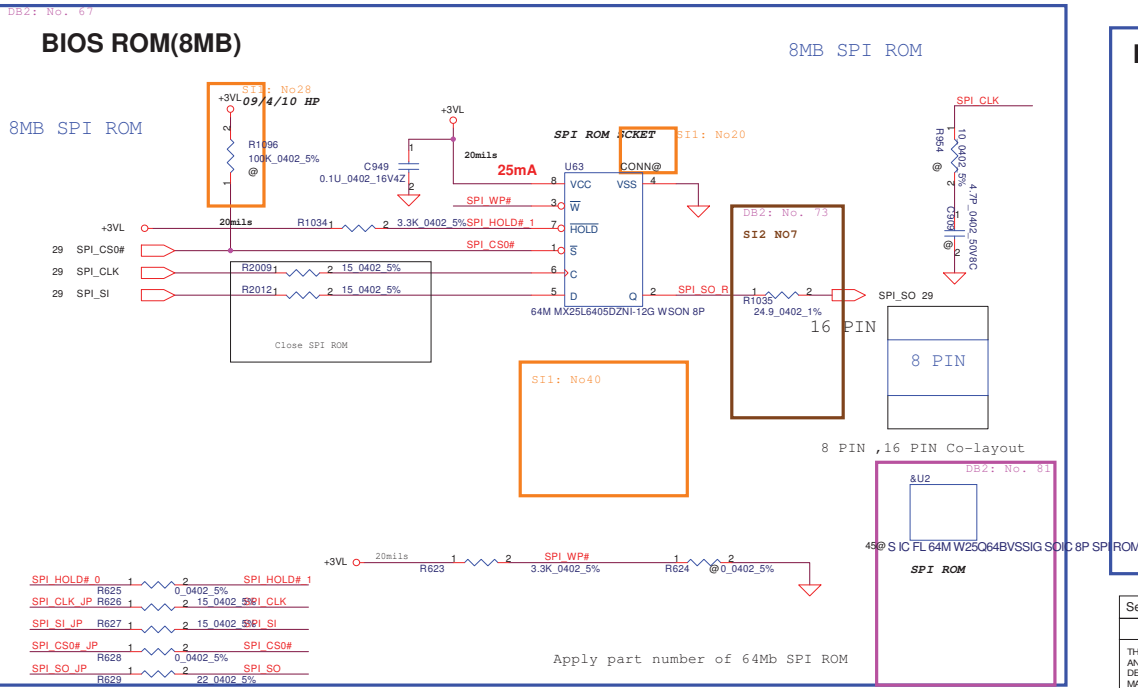
Finger Printer



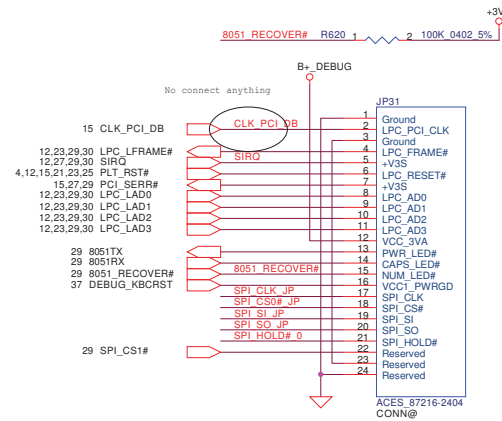
TPM1.2 on board



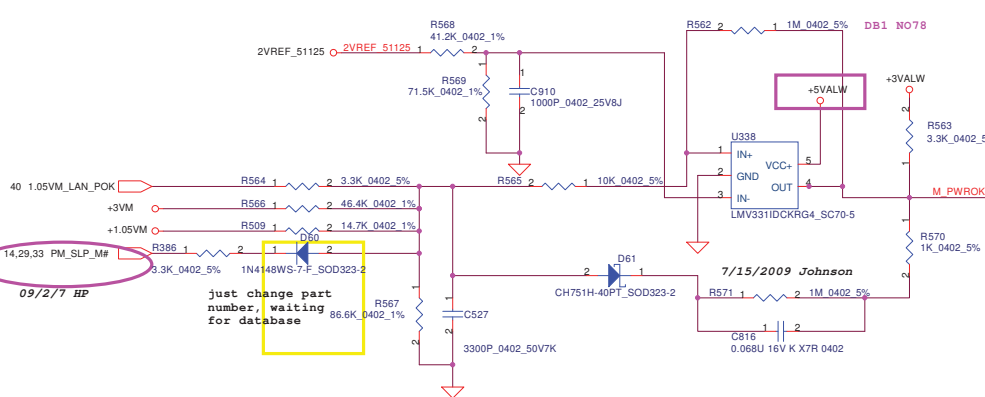
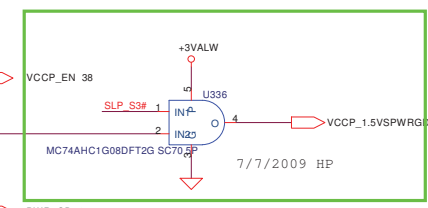
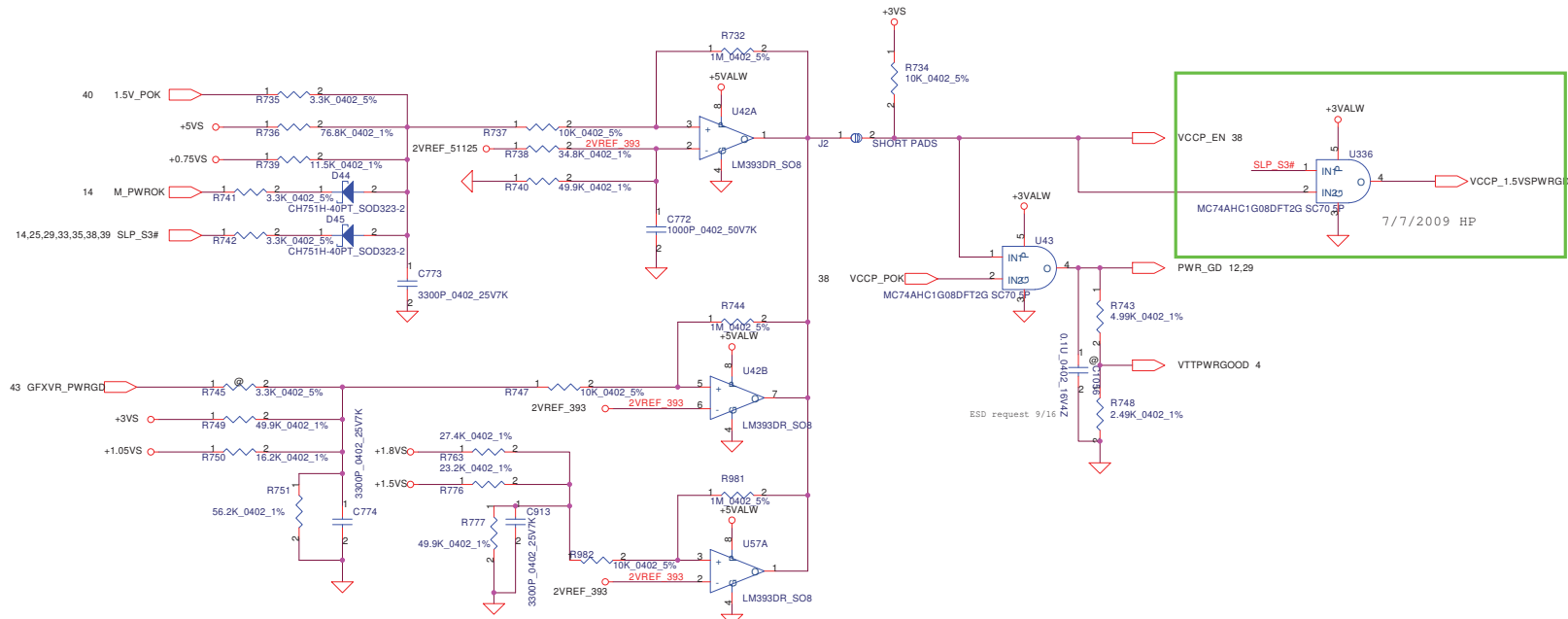
BIOS ROM(8MB)



LPC Debug Port



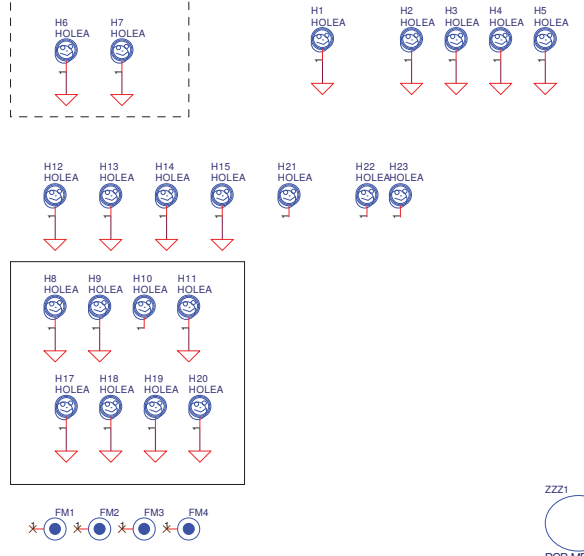
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Issued Date	2008/09/15	Deciphered Date	
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Date: Wednesday, December 09, 2009			Sheet 31 of 47



just change part number, waiting for database

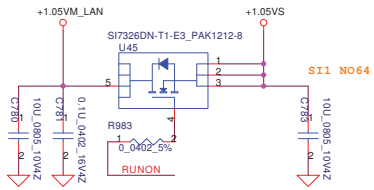
09/2/7 HP

MDC STANDOFF

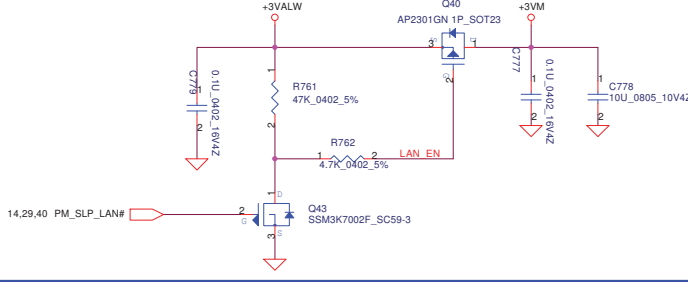


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Size	Document Number	Rev	Date	Sheet	of
	LA-4902P	0.3	Wednesday, December 09, 2009	32	47

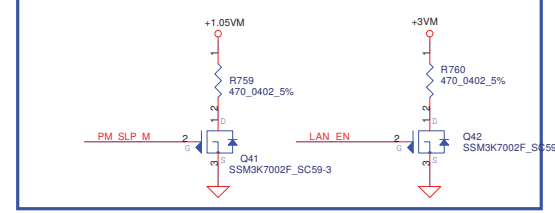
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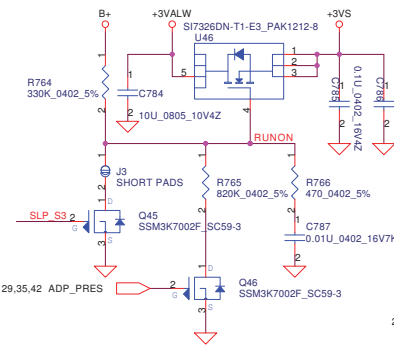
+3VALW to +3VM Transfer



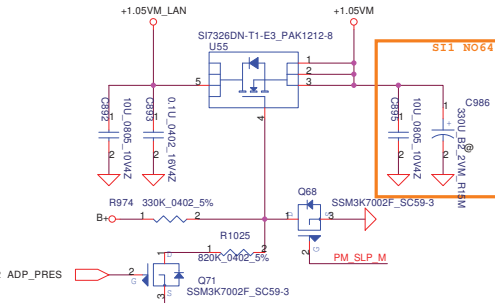
Discharge circuit-2 for V-M



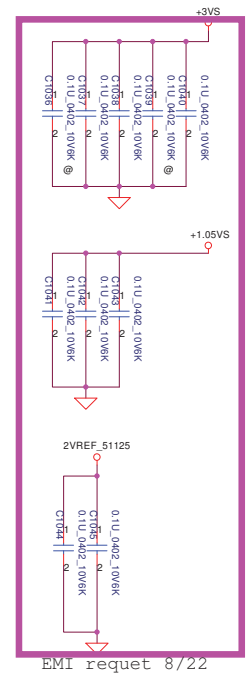
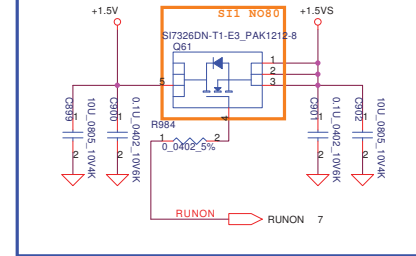
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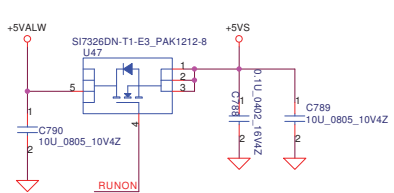
+1.05VM_LAN to +1.05VM Transfer



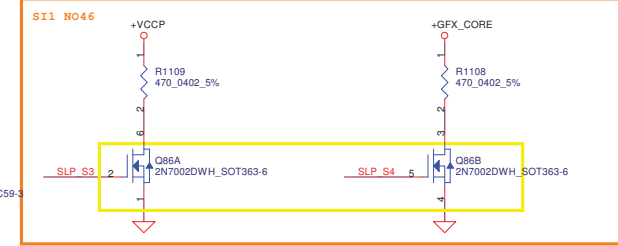
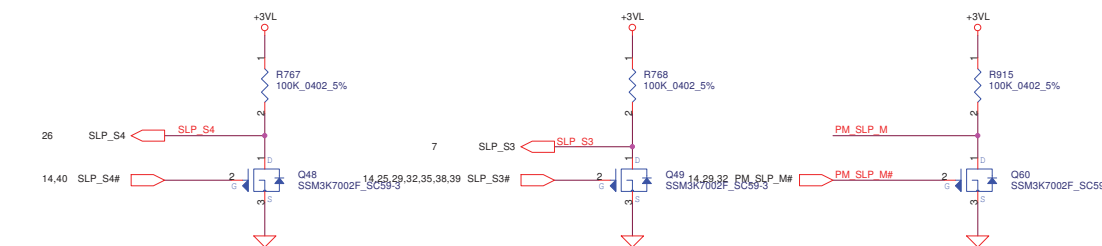
+1.5V to +1.5VS Transfer



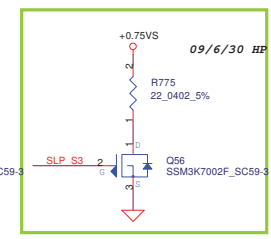
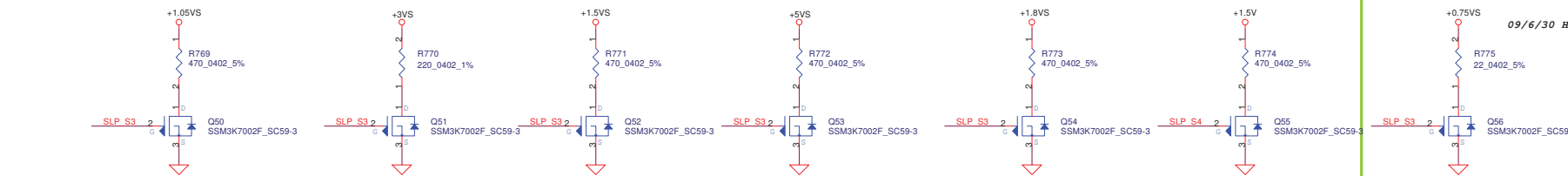
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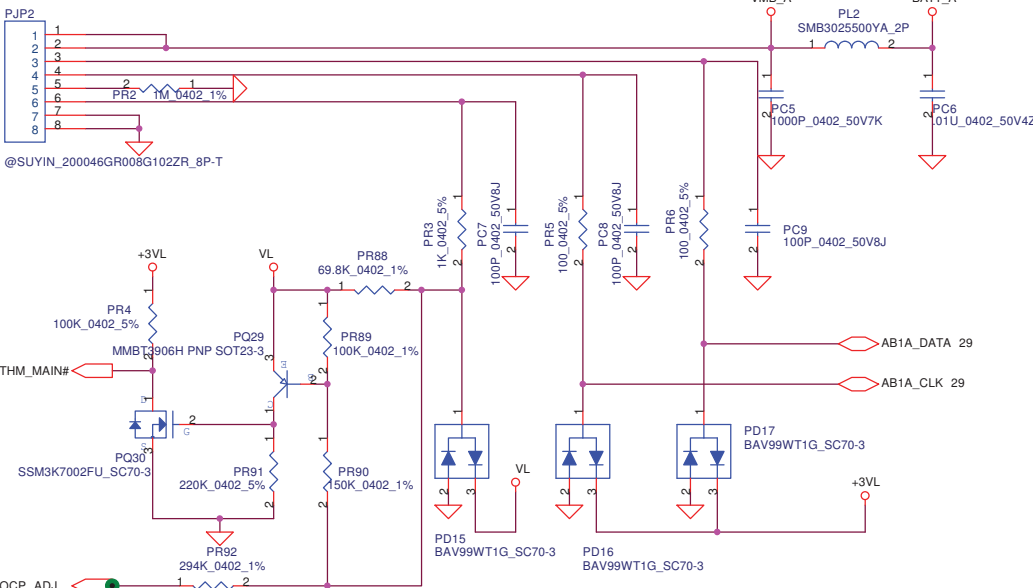
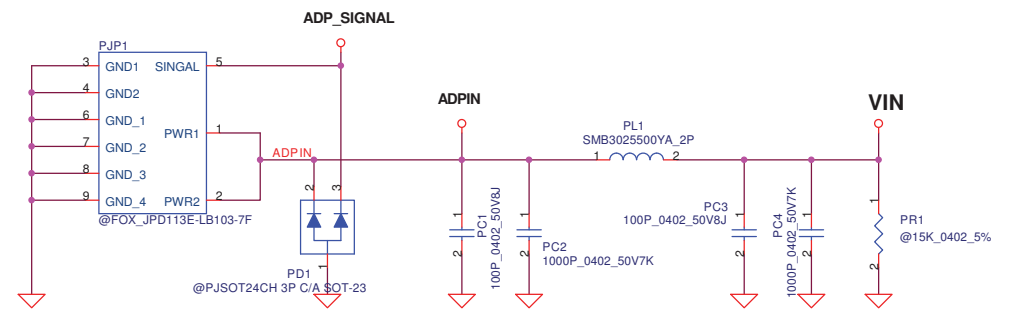
10/17 HP correct it



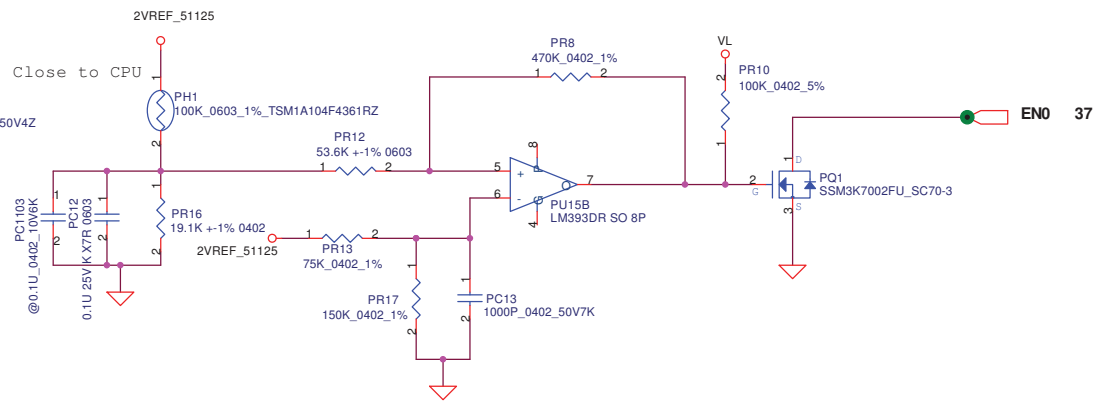
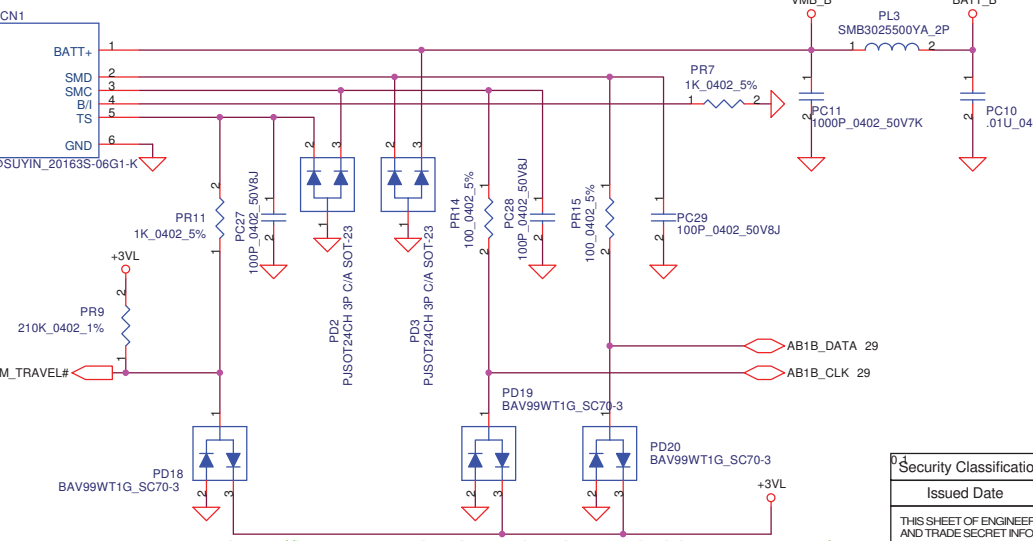
Discharge circuit-1



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Size	Document Number	Rev	Date: Wednesday, December 09, 2009 Sheet 33 of 47		
	LA-4902P	0.3			

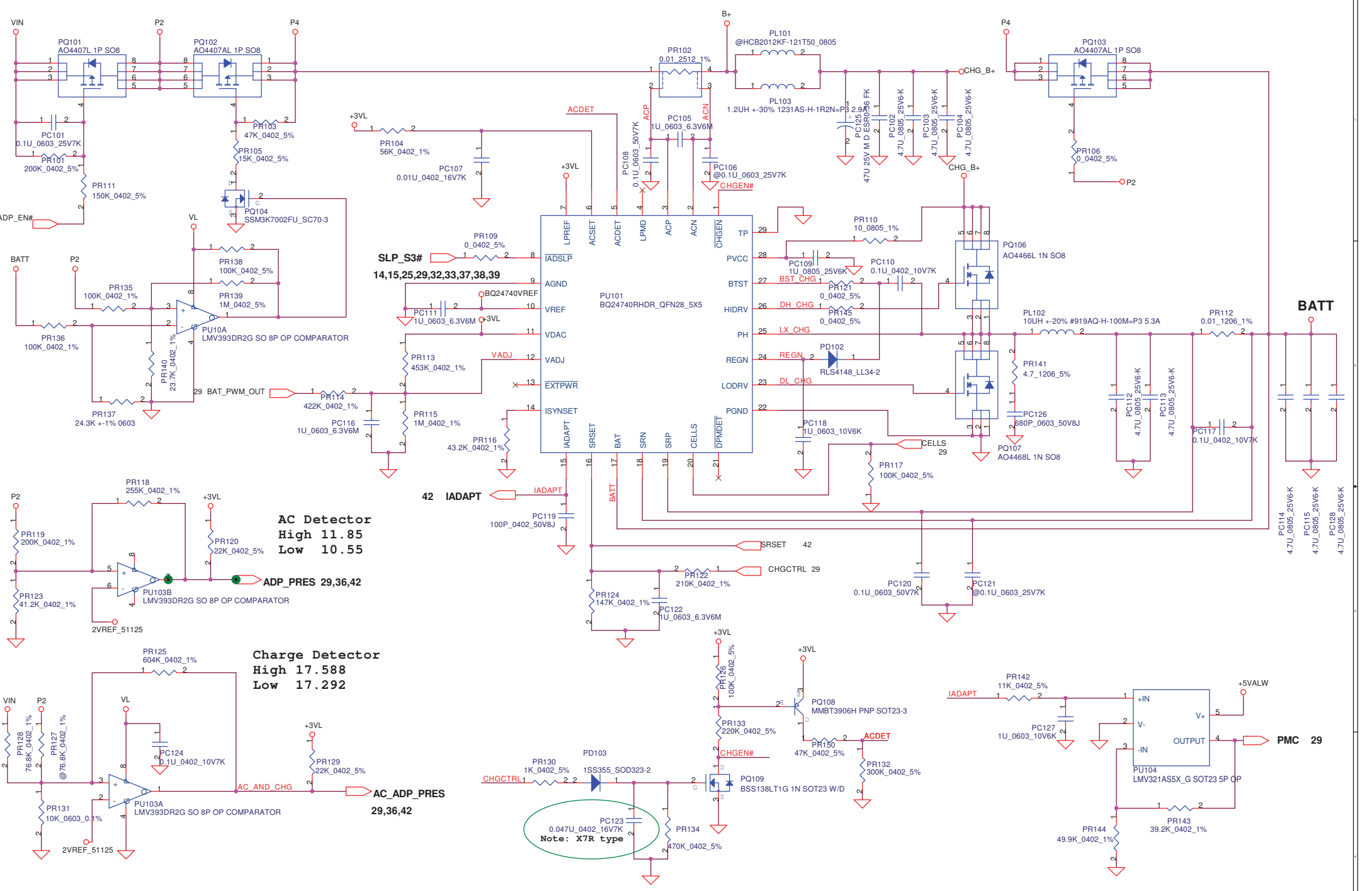


PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 (Need to be checked)



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Date: Wednesday, December 09, 2009				Sheet	34 of 44



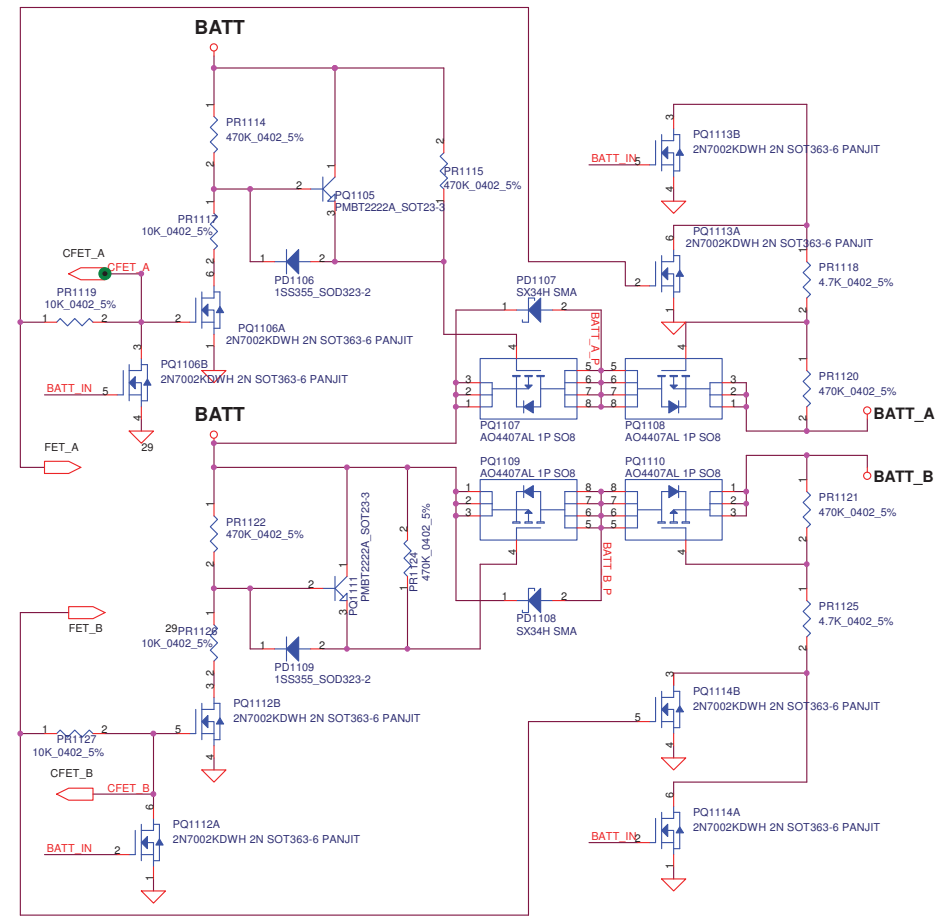
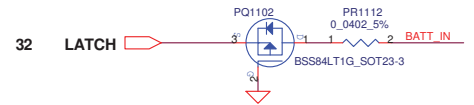
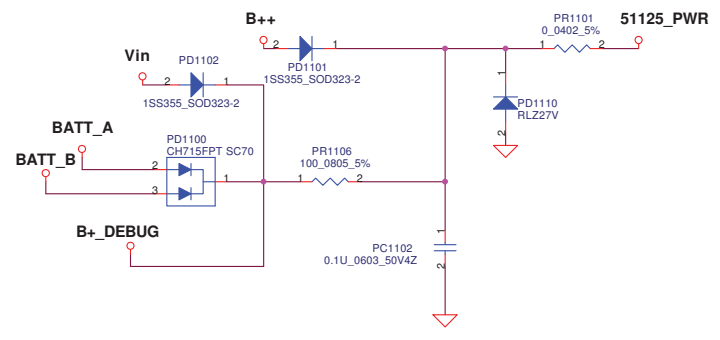
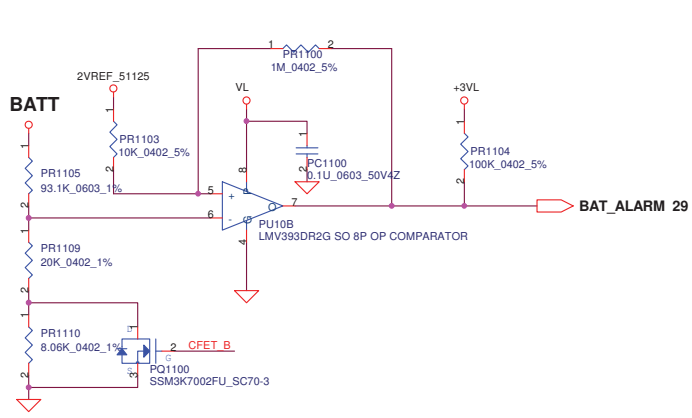
AC Detector
 High 11.85
 Low 10.55

Charge Detector
 High 17.588
 Low 17.292

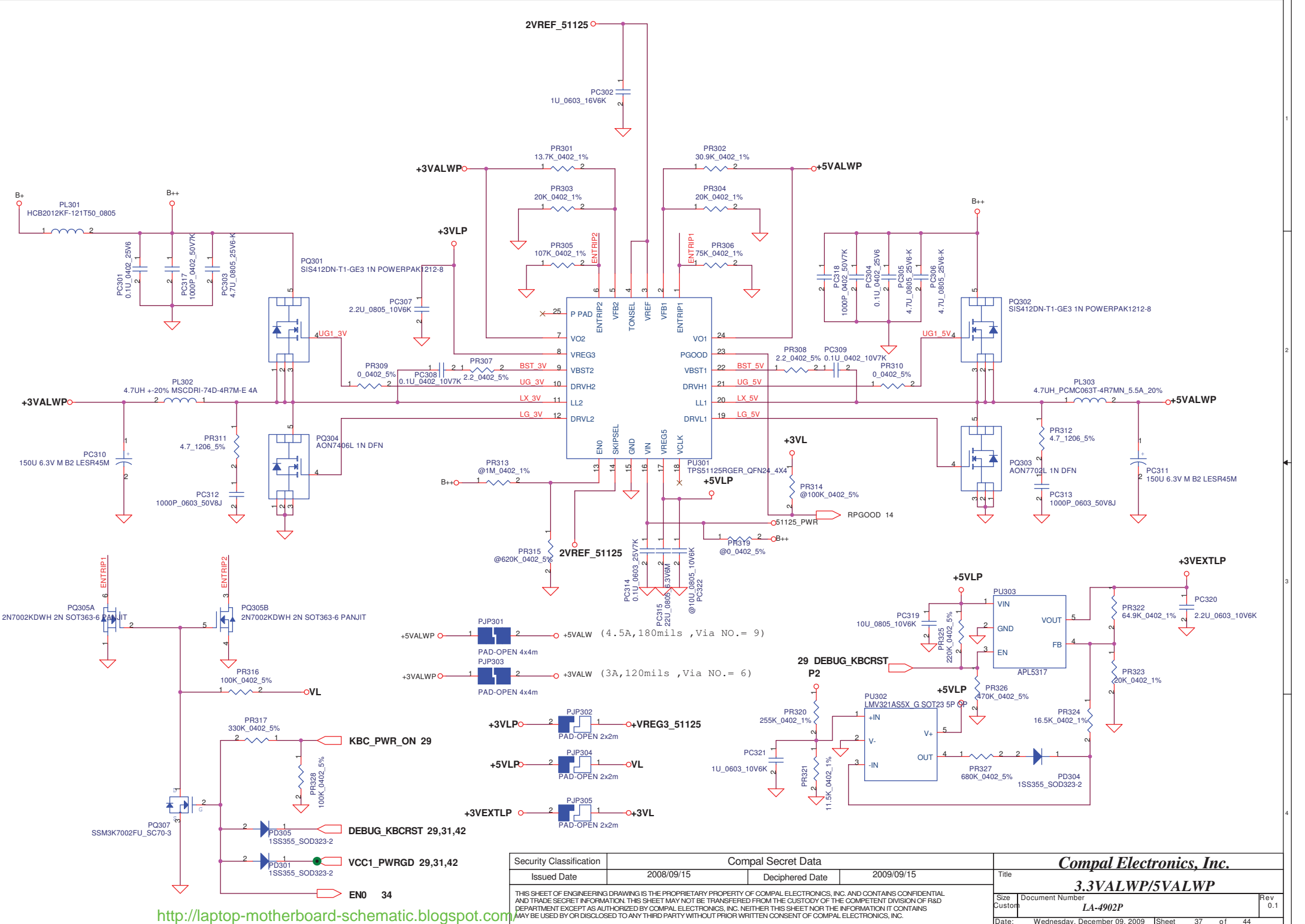
AC AND CHG
 AC_ADAPRES 29,36,42

PC123
 0.047U_0402_16V7K
 Note: X7R type

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Size	Document Number	Date		Sheet	Rev
	LA-4902P	Wednesday, December 09, 2009		35	0.1
				of	44



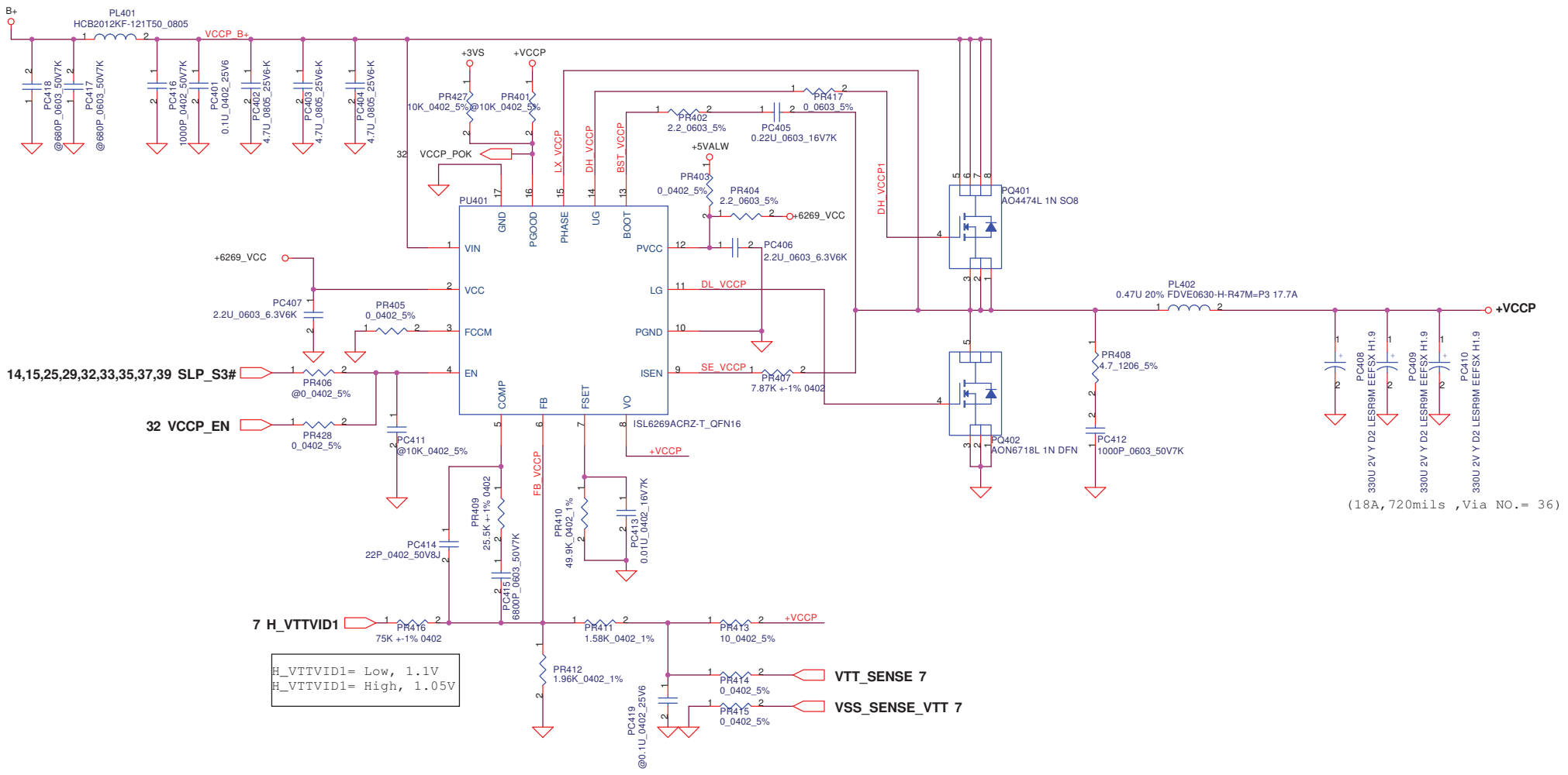
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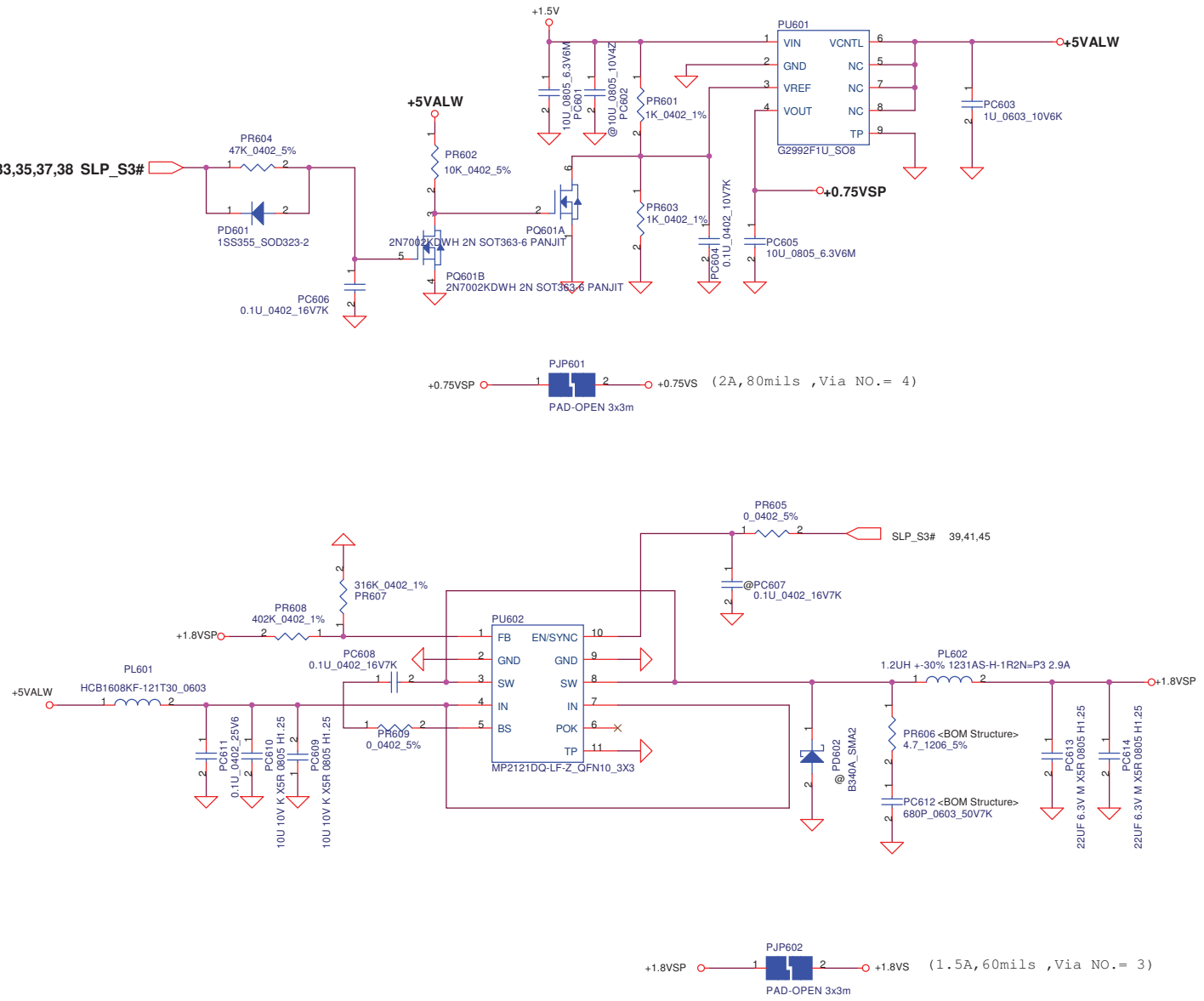
Compal Electronics, Inc.		
3.3VALWP/5VALWP		
Size Custom	Document Number LA-4902P	Rev 0.1
Date:	Wednesday, December 09, 2009	Sheet 37 of 44



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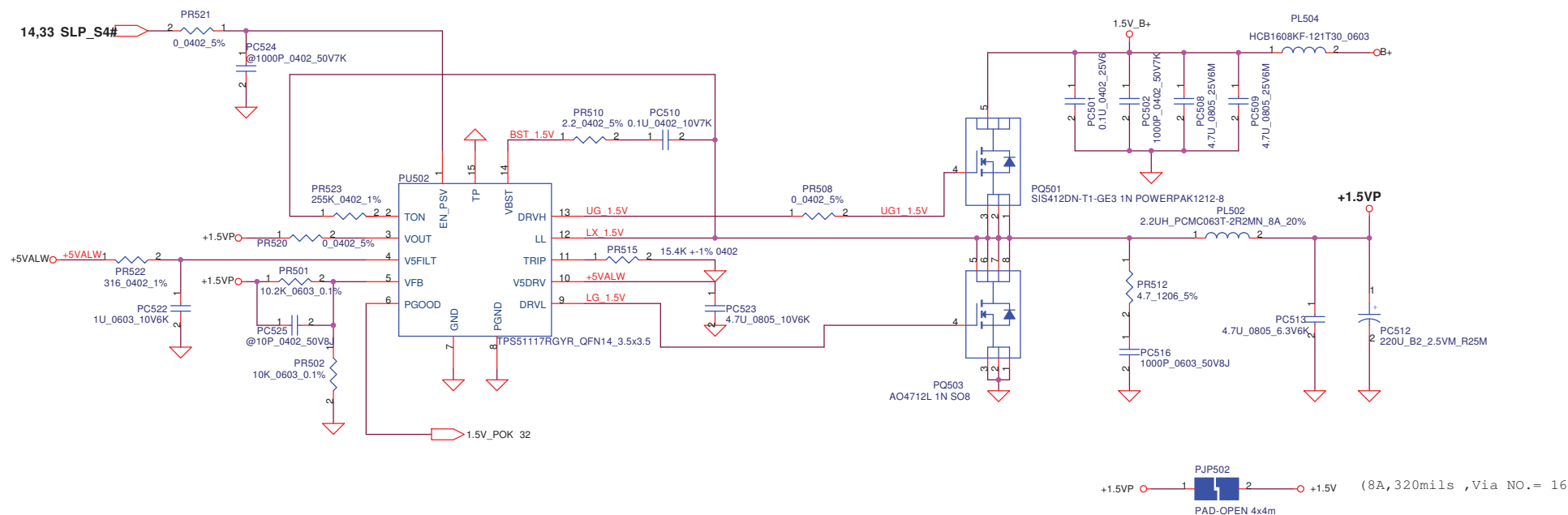
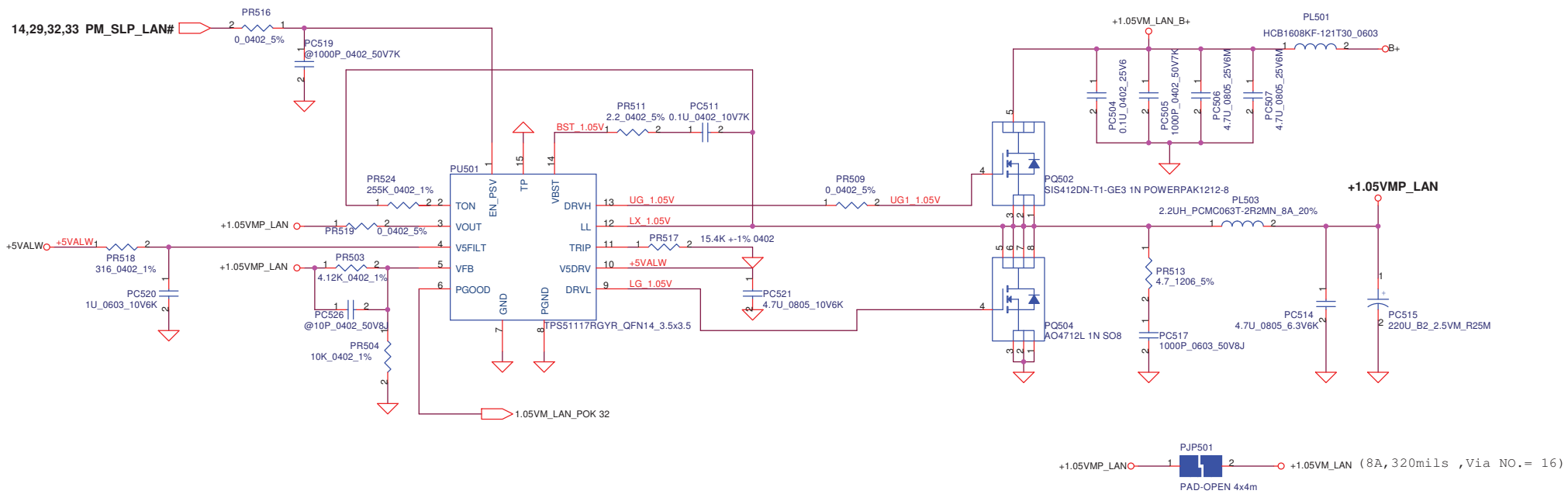
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Size	Document Number			Rev	0.1
				LA-4902P	
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14,15,25,29,32,33,35,37,38 SLP_S3#



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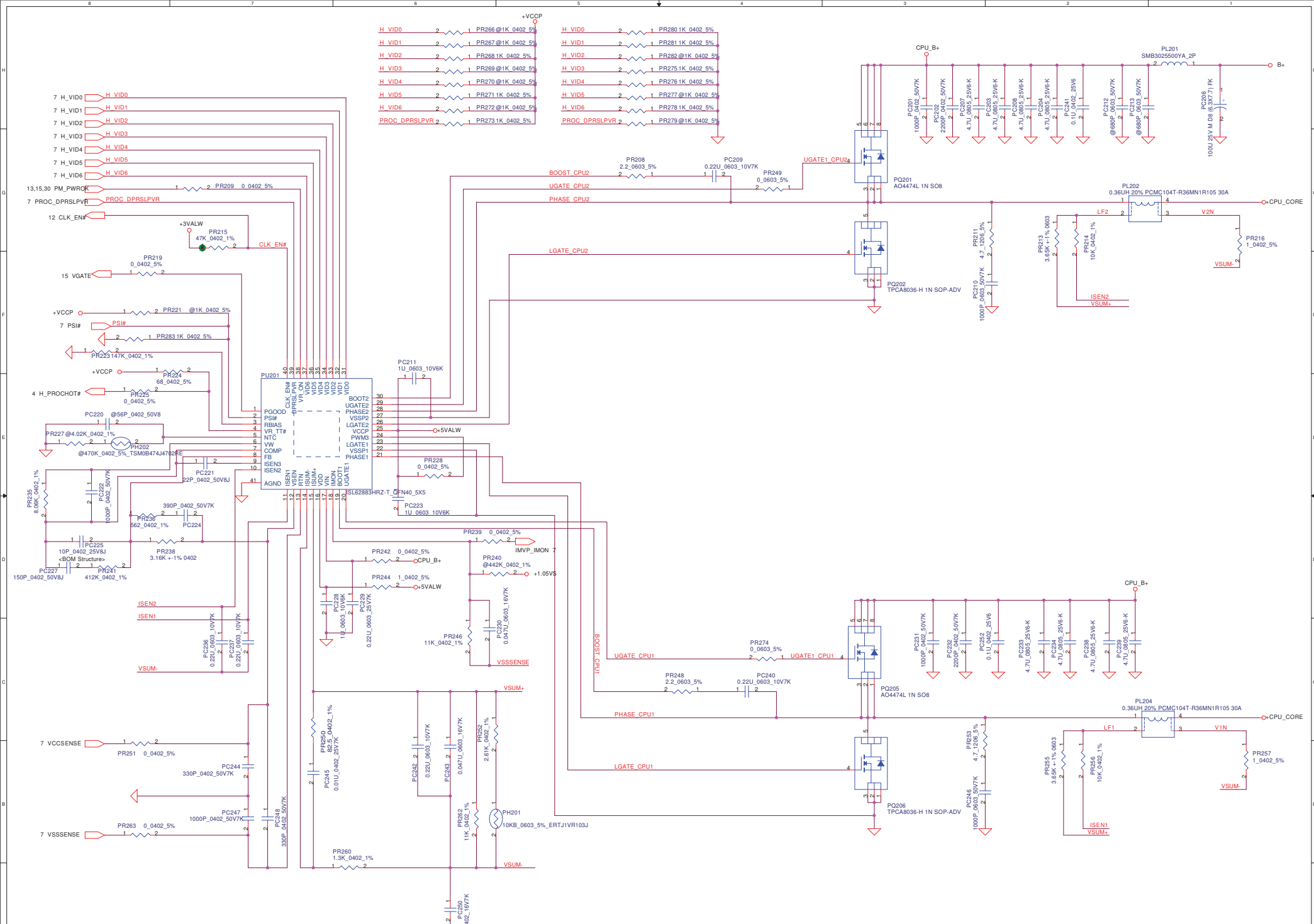
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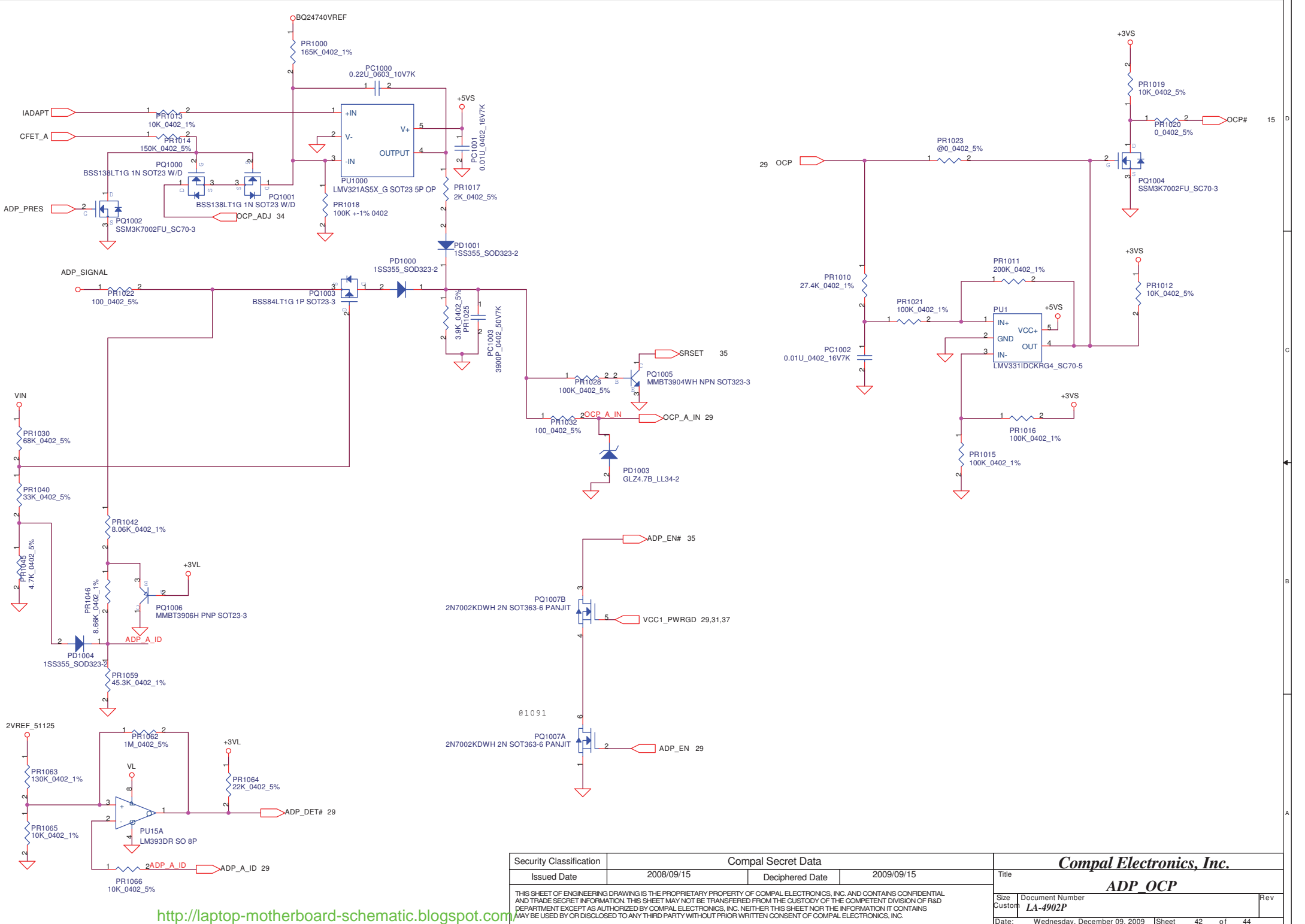
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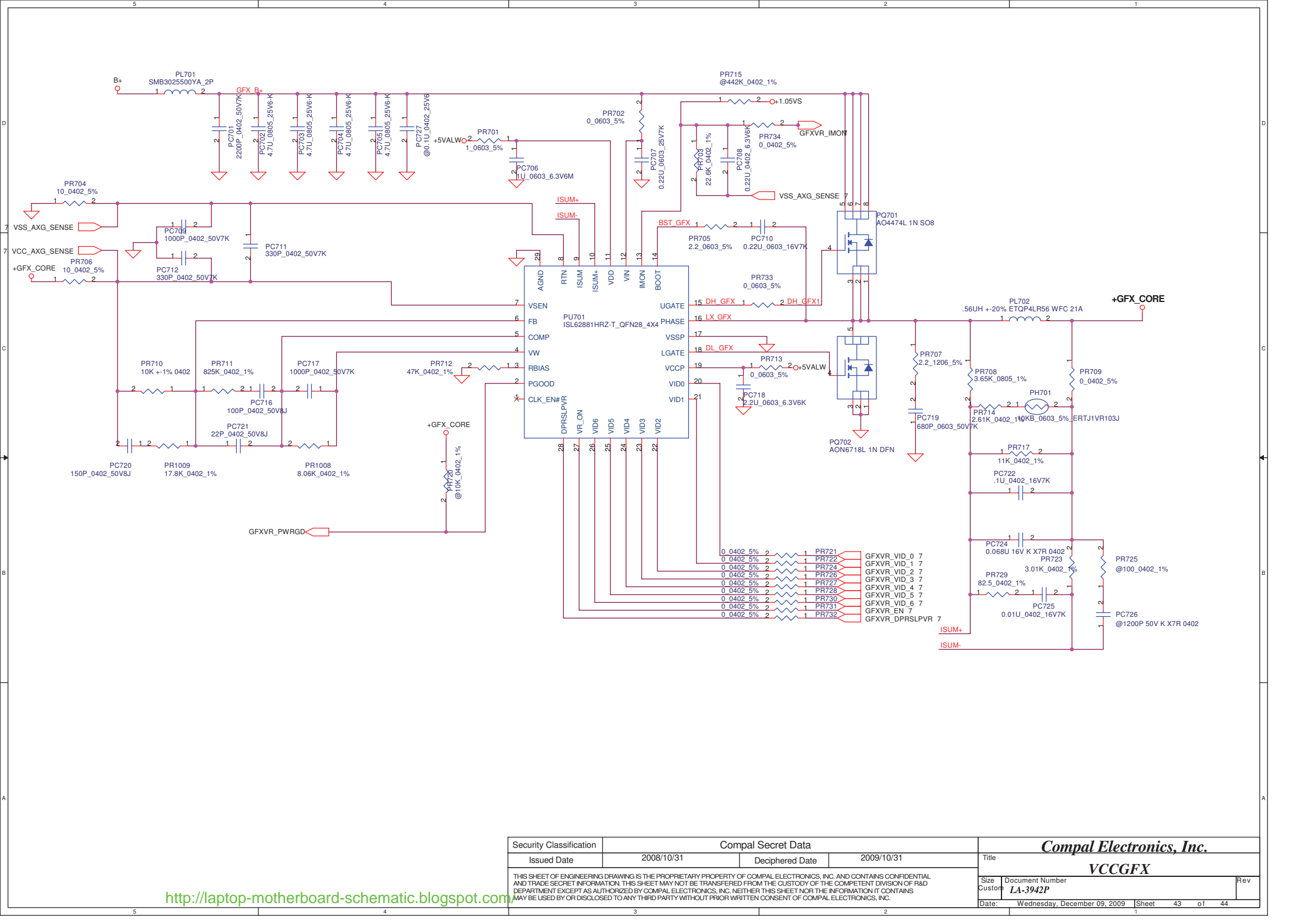
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No1. P21, LED0 and LED1 nets reversed

No2. P16, for HP item 84, R294,R485,C274 value change

No3. P20, due to JEDP1 42pin to 30 pin, redefining the signals, please remember to change footprint, symbol, part number.

No4. P20, JEDP1 change footprint and value

No5. P14,15, delete FCH LVDS signals and USB_5 for LVDS_CAMERA

No6. P21, LED0 and LED1 change back.

No7. P21, HDD/ODD footprint modified.

No8. P20, add 2 pins on JEDP1 by myself, different from database part

No9. P20, use real JEDP1 from database

No10. P12, for HP item 69, delete SMB_DATA_S3, SMB_CLK_S3 and add 2 test points

No11. P14, for HP item 78, install R277

No12. P29, for HP item 82, KB_RST# pull high to +3VS

No13. P4, for HP item 85, uninstall R997 and del R40

No14. P4, for HP item 97, delete R34,R36,R37,R46,R49 and change name of XDP_TDI & XDP_TDO, and short XDP_TDI_M to XDP_TDO_M

No15. P4, for HP item 98, add a series R between pin3 and 5 on U54

No16. P21, for HP item 99, delete C184-C487, C945, R427, R428, R963, Q18

No17. P22, for HP item 100, delete Q80A

No18. P22, for HP item 101, source and Drain of Q80B are swapped and change to a single 2N7002

No20. P12&P29, for HP item 103, change R948, R949, R952, R953, R939, R176, R180, R940 to 0ohm and R950 to 33ohm

No21. P28, for HP item 104, Connect +5VS to JP32 pins 11, 178, 179.

No22. P11, for HP item 105, R141 is connected to +1.05VS

No23. P28, for HP item 106, del R1008 and Q104, replace Q70B with a single 7002

No24. P28, for HP item 107, Delete R635-R638 and short the signals

No25. P28, for HP item 108, Delete C209-C205 and short the signals

No26. P21, for HP item 110, LED0 and LED1 nets reversed again

No27. P22, for HP item 111, Control signal for Q80B_GATE should be LAN_DIS#

No28. P22, for HP item 112, NO INSTALL R967 for ESI silicon

No29. P12, for HP item 113, INSTALL R847 and change to 1Kohm. Connect R847.1 to Q66.1 and remove the GND connection at R847.1.

No30. P12, for HP item 80, install R184 and R190

No31. P15 & P28, for HP item 79, GPIO38 and GPIO39 on U4 connect DOCK_ID0 and DOCK_ID1 to the docking connector pins 77 and 78

No32. P15, for HP item 60, delete R283

No33. P29, for HP item 66, change R504 to K503, change 10K to 0 Ohm, change the Table, add a NOR gate

No34. for No 18, change Q80 Source and Drain pin back.

No35. P32, for HP item 115, change PM_SLP_LAN# to PM_SLP_M# at R386-1

No36. P24, for HP item 116, circuits reconnection because of canceling item 106

No37. P19, for HP item 117, swap DPD_CTRLDATA and DPD_CTRLCLK, AUX connects to CLK and AUX# connects to DATA, add isolation nFET in series with Q74A and Q74B.

No38. P15, add 7 47P_0402 but "0" at every clock of PCI

No39. P12, change RTCVCC source from +VREG3_51125 instead of +3VL

No40. ESD change: (1) 0: D63-D67, D14, D57, D32, D68, D33, D34, D36, D62, D63, D62, D37

No41. ESD change: (2) change P/N: D14, D57, D32, D68, D33, D34, D36, D62, D37

No42. ESD change: (3) affect layout: D14, D33, D34, D36, D62, D37

No43. modify C962 GND disconnection and R70 to GND

No44. modify HP part number, please search "change HF P/N" to know which parts changed.

No45. for Load BOM problems, change some parts as below:
 (1) add CONN#: JCPU1, JP5
 (2) add P/N for dual 2N7002: Q2,Q3,Q7,Q8,Q81
 (3) change P/N: R570, C6, C829, R43, R44, R47

No46. for DRC check,
 (1) P23, delete dummy net of JODD1 pin16, 17
 (2) P28, add intersheet symbol at SMB_CLK_S3 and SMB_DATA_S3
 (3) P21, add a TP at U18.7: LAN_CTRL_18
 (4) P14, delete a dummy net N19910781
 (5) P28, change JP32 pin DCAD net name to DCAD1

No47. for parts forbidden:
 (1) C829 change to SE026104KN0 (2) R800 change to SD028100380
 (3) D68 change to SCA00000E00 (4) C818 change to 0402 SE070104280

No48. EMI concern:
 (1) install C833, C836, C956
 (2) P25, JP25 pin definition changes.
 (3) R931 to 47 ohm
 (4) P18, modify CRT circuits: add L and C, change R places, install C

No49. P29, for HP item 123, Change R680 to 100 ohms, and uninstall R699

No50. P29, delete R886, R887 and relative circuits

No51. P29, delete R892 for BAYCON

No52. P23, change JODD1 pin16, 17 type to avoid from useless net names

No53. HF parts link database: D1

No54. HF parts link database:
 (1) Q78 link SB00000H500
 (2) D16, D63-D67 link SC2AN217020
 (3) D1 link SC2N202U000
 (4) D23-D29 did not link SC2P202U000, just revise manually
 (5) Q57 & Q58 link SB000007H10
 (6) C263 & C269 link SGA202211D0
 (7) lots of 2N7002(Q4, Q23, Q32,Q41,Q42,Q43,Q45,Q46,48,49,50,51, 52,53,54,55,56,60,65,66,68,71,76,79,80) link SB000009080
 (8) T63 link SP050002I10
 (7) U42A, U42B, U44A, U57A link SA003930080

No55. combine power schematics 0212

No56. P29, for HP item 122, Connect D42-2 to VCORE_GP (not PM_PWROK) TEST. change U42,U44,U57 value and footprint LM393DG_S08

before netin
 No57. change U42,U44,U57 link another SA003930080

2/16

No58. P5, for HP item 126, R60 and R61 should be NO INSTALL

No59. P12, for HP item 127, Connect R857.1 to HDD_HALTED_R instead of HDD_HALTED

No60. P9,10, for HP item 128, Connect JDIM1A.199 and JDIMB1.199 to 3VS as Intel reference board

No61. P16, for HP item 131, based on spec, VccTX_LVDS and VCCA_LVD to GND.

No62. P19, for HP item 136, install Q76 and add install R1055 as there must be isolation

No63. P13, for HP item 138, change Gate of Q77 to +3VALV

No64. change Pb-free
 (1)R1058 to SD028100180,
 (2)R1059,1060,1062,1063,1064 to SD028100280
 (3)R615, 1061 to SD028470180
 (4)RP31, RP33 to SD309100280
 (5)RP29, 30, 32,34,35 to SD309470180 --> footprint should keep original
 (6)C950, 951, 952 to SE070104280
 change HF
 (1) SW1 to SN100000W10

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No65. separate GND signals
 (1) P28 and P25, add GNDA and resistors,

No66. P20, change JEDP1 to 24 pin connector, delete LANE[1:3] and EDID, as well as U4 relative signals.
 No67. P31, change SPI ROM back to DB1 design, but mount 8pin, unmount 16pin
 No68. P19, change misunderstand name:DPD_C_AUX/DPD_C_AUX# to DPD_C_AUX_1/DPD_C_AUX_L#

2/19

No69. P5, delete MB_DP_DATA[1:3] N/P for JEDP pin cutting
 No70. C6 and C685 change to SE071100J80 because of Jason's request(vendor doesn't have the original 25V part)
 No71. P25, install C888,C889

2/20

No72. for HP item 66, P29, U66.5 should be connected to 3VL so that KBC can read board before boot and apply necessary fixes.
 No73. for HP item 103, P31, R1035 should be 0ohm
 No74. P27, change SC_PWR circuits for unsurely current

2/23

No74. P26, uninstall U31 and add J1 for cost down
 No75. change some test point footprint to IPC12: T61,T62,T1,T55,T97,T22, and P14 lots of points

2/24

No76. P22, JP6 symbol error, modified!
 No77. P12, add a net name XDP_FN4

2/25

No78. P32, change U44.8 to +5VALV for HP request
 No79. P29, change R680=220 ohms

combine power schematics

No80. P25,
 (1) JP24: redefine the singals of the pins,
 (2) JP25: reverse pin definition

No81.
 (1)U4 change PN to SA00002KV30 for ES2
 (2)P31, &U1, &U2 change to SA000037A00

3/6

No82.
 (1)P29, Firmwave said unmount R1021 and mount R1022
 (2)P4, delete R998 <BOM structure>, otherwise BOM will be error

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No1. for HP item 5, P32, change U44A to U57B and delete U44
No2. for HP item 6, P12&24, connect JP12.17 to U4A.F34 and add 10K pull-up to +3VS for Braidwood detection.
No3. for HP item 7, P4, change PC4 debug ports to CF64 - pin 28, CF65 - pin 30, CF610 - pin 22, and CF611 pin 24
No4. for HP item 11, P20, reverse Q9A
No5. for HP item 12, P13, Change all express clock series terminations from 33ohm to 0ohm, R208, R209, R211, R212, R41 and R59 should be 0ohm
No6. for HP item 14, P12, no install R337, R338, R321 to disable I/Os (D61.0 did not see this)
No7. for HP item 14, P12, unmount R186 and R192 because latest PCH EDS shows that PCH XDP UTAG_RST# is now NO CONNECT on PCH
No8. for HP item 16, P20, change D12 to 2Kohm resistor and remove R322
No9. for HP item 17, P20, Change Q79.2 to L1D_SW#
No10. for HP item 4, P22, source and drain on Q80B should be swapped
No11. for HP item 22, P27, change WWAN power circuits to pFET circuits.
No11. for HP item 22, P27, add ESD Diodes and pullups for the SCCLK, SCIO, SCRST lines on the SC socket
3/16
No12. P14, add RGB name:DAC_RED_R,DAC_GRN_R,DAC_BLU_R
3/19
No13. P29, R593 part number: "space" delete
3/23
No14. P31, reverse JP30 pin definition
No15. P4, change R1082 from 0 ohm to 10K
No16. P14, P18, change R307, R308, R309, R301, R302, R303 from 75ohm to 150ohm
No17. P14, P18, change R307, R308, R309, R301, R302, R303 from 75ohm to 150ohm
No18. P28, add a reversing circuit for STB_LED# to fix the LED bug
No19. P21, P28, delete redundant net LAN_ACT#_DOCK and change it to LAN_ACT#
4/2
No20. P31, revise BIOS connector to CONN@ and unmount &U1
No21. P9, revise "M1@" to "M1@"
No22. P12, revise 0ohm(R868, R869, R870, R871, R872, R1071) from SD034000080 to SD028000080
4/3
No23. P25, modify Power button circuits
4/10
No24. for HP item, P15 and 2# GPIO --> WWAN_DET# and pull high 100K
No25. for HP item, P1, Scruff R51 for SYS_SHDN# and add these 3 to my schematics as C972-974
No26. for HP item, P22, VCI pin U18.6 should be NO CONNECT. R929 uninstall
No27. for HP item, P510, Remove M18 for UMA and make it always installed. UMA will only use M1
No28. for HP item, P41, remove 100Kohm pull up to 3V1 on U63.1
No29. for HP item, P15, LAN_DIS# should pull up to +3VM LAN instead of 3VALW
No30. for HP item, P4, Change R14/R17 to .1K/3R18 per D61.52
No31. for HP item, P16, add NO INSTALL 0ohm to GND on GPIO6 on PCH and remove PULL UP to 3V1W because PCH has an integrated pull up.
No32. for HP item, P13, For UMA:
NO INSTALL: R210, Y4, C222
INSTALL 0ohm resistor in C223
4/14
No33. P14, revise for HP item 13 not mentioned, delete LVD_VREFH and LVD_VREFL to GND
No34. for HP item, P19, Reserve 0.1uF on DDC_EN and DP_EN for concern about noise.
4/21
No35. P29, R1021 Removed
R1022 Install (main battery selection)
R1023 Install (OCP function)
R1024 Install (travel battery selection)
R694 Install (SMSC CBB will required it)
4/22
power schematics updated: CARTIER_UMA_PWR_20090421.DSN
No36. P29, R1021 Removed
No37. for HP item, P16, Add 2x22uF for VCCME (on PCH)
4/22
No38. revise the footprints of T113, I22, I23, I24 from TPC to TPC12
No39. for HP item 14, P14, delete R537, R620 and R621 and add 3 test points.
No40. for HP item, P4, Install R997 and uninstall R444 to change FAN power
4/27
No41. revised for HP item, P28, change name STB_LED#_R
No40. P31, delete U64 and &U1
No41. for HP item 18 and 57, P24, modify WWAN circuits
No42. for HP item 51, P29, change system ID by installing R660 and uninstalling the others
No43. for HP item 54, P30, add uninstalled 0ohm and 10K pull down at SER_SHD
No44. for HP item 46, P9.10, Install a new voltage divider for VREF_CA that is different from VREF_DQ divider
No45. for HP item 61, P15,20, delete R969, R330 R328, C297 R327 R329 Q14 C304 and Q9A, R268, delete WEBCAM_OFF circuits and add WEBCAM_ON circuits.
No46. P33, add +VCCP and +GFX_CORE discharge circuits
4/28
No47. P27, change Smart Card circuits
No48. for HP item 48, P9.10,
(1) add 1 uninstalled 300uF on DIMMB +1.5V,
(2) add 2 10uF on +0.75VS,
(3) delete 4 uninstalled 10uF on +1.5V
(4) unistall 8 0.1uF on +1.5V
No49. for HP item 49, P16, delete R289
No50. for HP item 52, P22, TRM_CRT: add 4 0.1uF
No51. for HP item 56, P24, change caps to 150uF and 22uF, delete the others.
No52. for HP item 61, P20, change sample WWAN/WWAN# LED circuits. uninstall Q62 and Q64
No45. for HP item 61, P20, modify WEBCAM again
4/30
power schematics updated: CARTIER_UMA_PWR_20090429.DSN
5/4
No53. for HP item 62, P25 & 29,
Change A_SD to A_SD# on U40.91U (GPIO14 of KBC).
Change A_SD to A_SD# on JP5.35 (Audio board connector).
Change EAPD to MUTE_LED_CNTL (GPIO31 of KBC).
Change EAPD to MUTE_LED_CNTL on JP5.36 (Audio board connector).
No54. for HP item 64, P23, uninstall R474. The concern is leakage when system is off.
No55. for HP item 65, P29, Uninstall pull-up on KBEST# (R893) as it is not needed.
No56. for HP item 65, P29, change KBEST# from 10K to 100K to reduce current.
No57. for HP item 67, P29, for ADC small input filters, add R1113-R1116 and C982-C984
No58. for HP item 67, P29, for ADC small input filters, add R1113-R1116 and C982-C984
No59. for HP item 70, P18, uninstall R234 for wrong power fail.
No60. for HP item 70, P18, add 10K pull-up to USB_C0#2 as we are not using it.
No60. for HP item 71, P12&24, change net name from BRAID_DET to NAND_DET#
No61. for HP item 72, P13&21, add CLK_PCIE_LAN_REQ1# connected U18.4# to U4B.U4
No62. P23, change JODD1, link database
5/5
No62. P23, JODD1 pin 16,17 change passive
5/6
No63. P22, swap T63 MDI +/- signals
No64. for HP item 15, P33, add 330uF to each of +1.05VS and +1.05VM
No64. for HP item 15, P33, add 330uF to each of +1.05VS and +1.05VM
No64. for HP item 15, P33, add 330uF to each of +1.05VS and +1.05VM
No64. for HP item 15, P33, add 330uF to each of +1.05VS and +1.05VM
No64. for HP item 15, P33, add 330uF to each of +1.05VS and +1.05VM
5/7
power schematics updated: CARTIER_UMA_PWR_20090507.DSN
No65. P8, power team requests 10uF*22 and 22uF*18
No66. according to SMSC AN 18 1 rev 0 12:
(1) add capacitors on PS2 signals
(2) reserve ESD diodes on cap_clk and cap_data
No67. P15, EMI concern: change R1026 to 47 ohm
5/7
No68. for HP item 68, P29, change net name :AC_AND CHG --> AC_ADG_PRES
5/8
No69. for HP item 74, P33, unistall R222
No70. for HP item 74, P33, unistall R222

power schematics updated: CARTIER_UMA_PWR_20090508.DSN
No71. P20, JEDP.20 change to +5VS
5/12
No72. P26, add eSATA connector and redriver circuits
No73. P19, correct Q75B's direction
5/13
No74. P29, cost down, change NOR to dual 2N7002
No75. P26, cost down, delete R605, and short the circuits
No76. P23, from Johnson, we should keep the pull high resistor
because EC will not program the internal pull-high afterwards.
power schematics updated: CARTIER_UMA_PWR_20090513.DSN
5/14
No72. P26, change USB and E-SATA connector and revise this circuit
power schematics updated: CARTIER_UMA_PWR_20090514.DSN
No77. for HP item 75, P24, install C45-C47 39#
No78. P21, c495, c497 CHANGE TO X5R SE095104K80
5/15
No79. P7, delete uninstalled VCCP 47pF * 4 and 10uF * 1 (C41-C44, C46)
power schematics updated: CARTIER_UMA_PWR_20090515.DSN
No80. P33, Q61 change part
5/18
No81. for HP item 22, P27, install D70-72
No82. for HP item 76, P14, 29, 41
(1) add R=1k between PGD_IN and VGATE, and uninstall R237.
(2) remove D42.
(3) remove PR217 and PR230
No83. for HP item 77, P19, uninstall R1076
No84. for HP item 78, P24, install C84-C87 39#
Remove R1051 and R1048 and make the following changes:
Install R1046 (100K) but change R1046.2 to GND
Install R1047 (100K) but change R1047.1 to 3VS
power schematics updated: CARTIER_UMA_PWR_20090518.DSN
No85. P21, change 10uF to 22uF to stabilize voltage
5/19
No86. change HF part:
(1) SA411250130 S IC 74AHCT1G125GW SOT353 5P BUS BUFFER
-> SA00000RY00: U7, U8, (PN change only)
(2) SB000008E00 S TR MMBT3904W NPN SOT323-3
-> SB000008E10: Q1,
(3) SB00000AR00 S TR 2N7002DW T/R7 2N SOT-363-6
-> SB00000AR10: Q2, Q3, Q5, Q7, Q8, Q10, Q63, Q77, Q86, Q87
(4) SB570025280 S TR 2N7002DW-7-F 2N SOT-363
-> SB00000E010: Q11, Q72, Q73, Q74, Q75, Q81
(5) SC2N202U000 S DIO ROW DAN202UGT106 3P C/C SC-70
-> SC60000B00: D1
(6) SCA00000A00 S ZEN ROW PJDLCO5 3P C/A SOT23
-> SCA00000A10: D58
(7) SJ100001V00 S CRYSTAL 32.768KHZ 1TJS125D74A420P
-> SJ100004N00: Y6, Y7
(8) SP04301P120 S FUSE SMD1812P110TF 1.1A 6V UL/CSA/TUV
-> SP04301P140: F1
(9) SC1N4148180 S DIO IN4148WS-7-F SOD-323
-> SC100004P00: D60, D70, D71, D72 (PN change only)
No87. after Gerber out: BOM
(1) change Q70 to SB923050020
(2) link database
JP31(enter myself), C888, R782, R202, R200, R791,
R785, R800, R796, R797, C184, C885, C887, C231,
C232, C236, C241, C243, C244, C247, C248, C251,
C252, C253, C261, C264, C270, C271, C272, C274,
C275, C515, RP16, RP18, RP26, RP27, R787
No88. according to Monji, P13, check R215 to 22 ohm
5/20
No89. U67: Change SA00002ZR0L to SA00002ZR00
for DELL prohibition part
No90. P08,
change MLCC part references for power
team request
(1) 10uF: C103 · C993 · C994 · C988 · C92
C94 · C97 · C116 · C113 · C90
C89 · C98 · C99 · C100 · C101
C102 · C91 · C84 · C96 · C83
C111 · C88
(2) 22uF: the others
(3) change C105 - C108 to SGA00001Q80
SI1 to SI2
5/20
No1. change schematics parts of Q24 and Q70, the same P/N SB923050020
5/25
No3. P27, change R1086 to 100K, R1085 to 10K, delete R1110 like DIS
No3. PCH PN: SA00002KV60; LAN PN: SA00002M040

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5/20
No1. change schematics parts of Q24 and Q70, the same P/N SB923050020

5/25
No2. P27, change R1086 to 100K, R1085 to 10K, delete R1110 like DIS
No3. PCH PN: SA00002KV60; LAN PN: SA00002M040

6/2
No4. P12, change reference name: JBATT1 --> JBAT1
No5. P25 & P31, JP25 and JP30 are reversed(H and V) because of footprint silkscreen problem, remember not to change routing, just change ME pin1

No6. P12, P29, P31, add net names of SPI signals
No7. P12,29,31, change 24.9ohm for SMSC request:R939,R940,R950,R948,R952,R1035

6/18
No8. P19, add 1 fuse on DP power

6/22
No9. P19, as per Johnson's request, for cost down
(1) uninstall C123, C699
(2) change C552 from 150uF to 100uF +0.1uF*2 (not ok)
(3) change C263 and C269 to 100uF (not ok)

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