

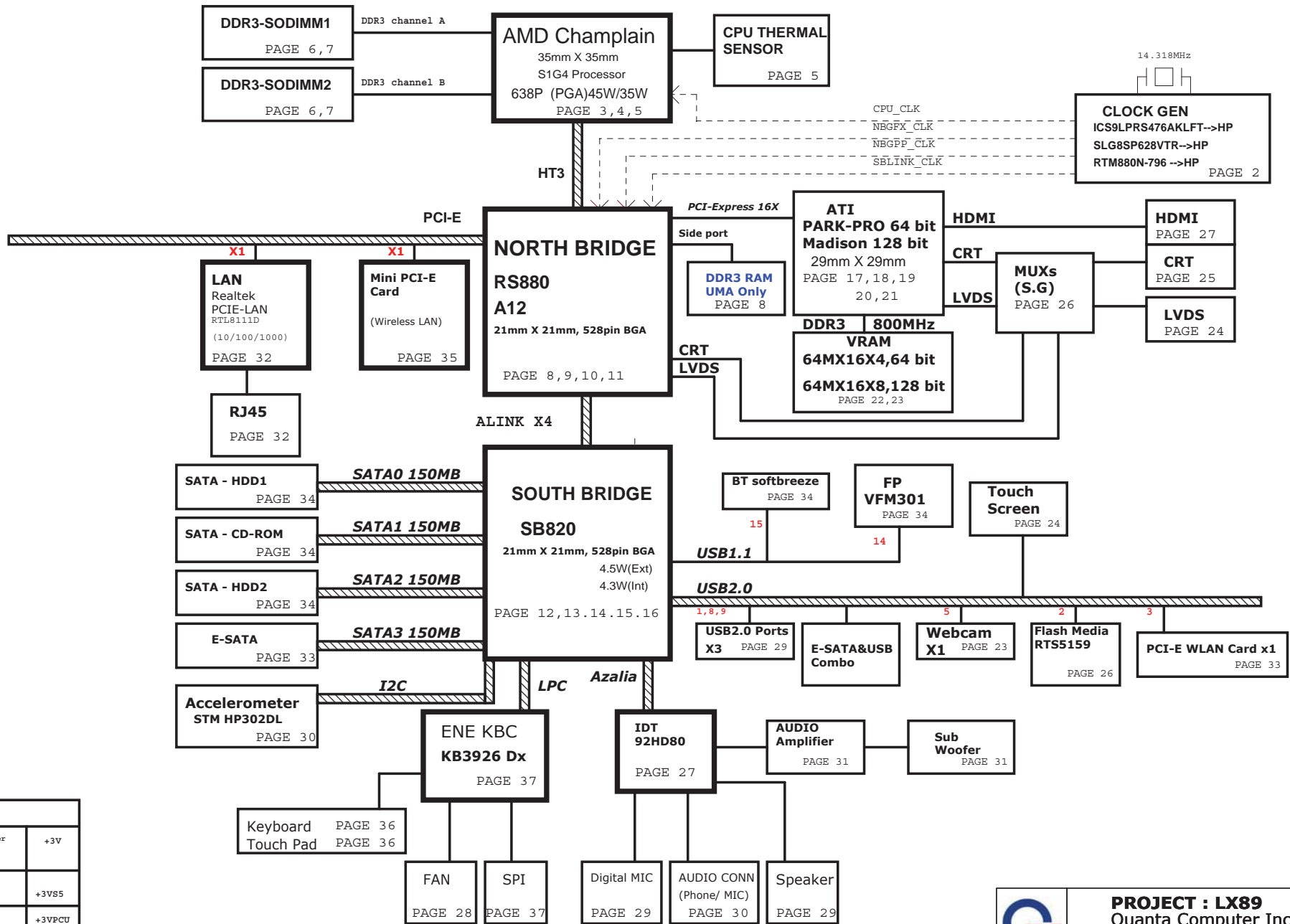
LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : BOT

LX89 SYSTEM DIAGRAM



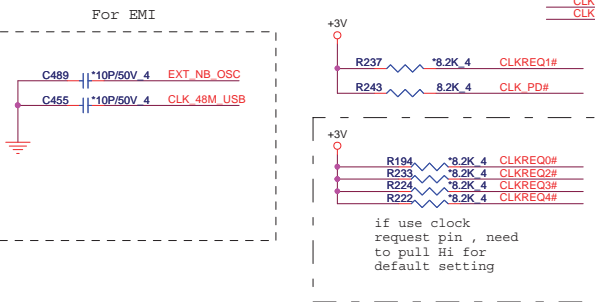
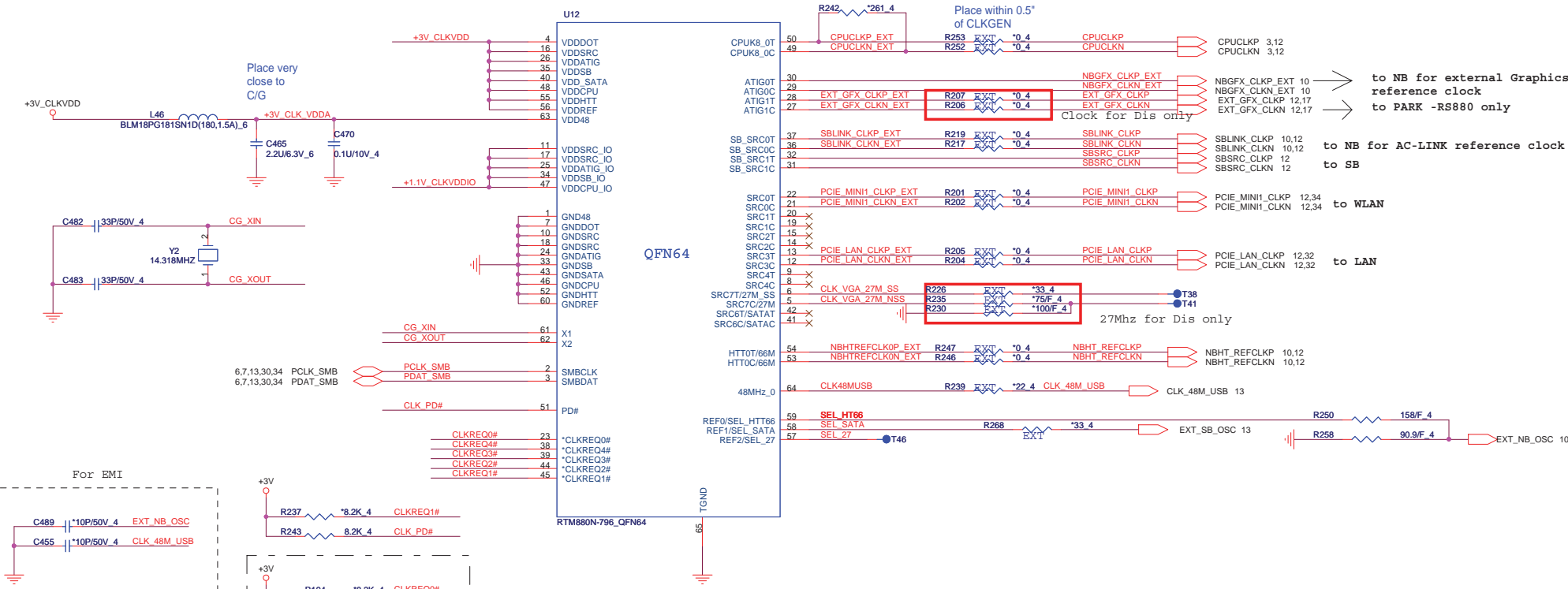
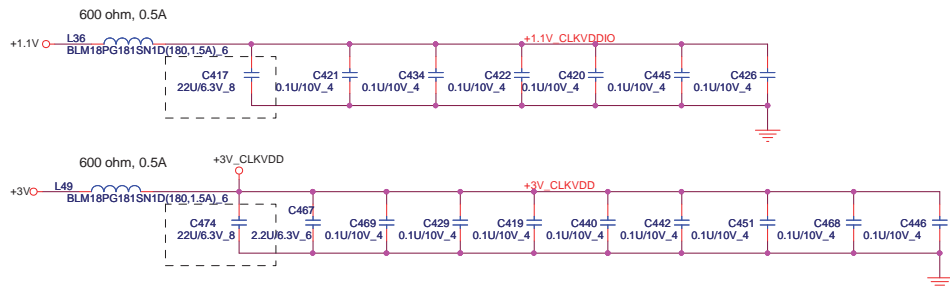
- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Sobson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V



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	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	Block Diagram	
Date: Monday, September 28, 2009	Sheet	1	of 46

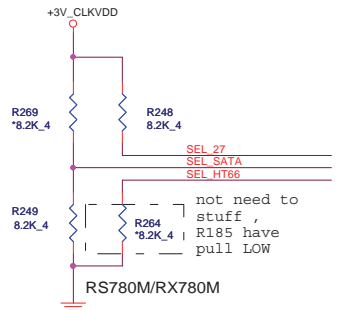


SLG
RTL

SLG8SP628VTR--AL8SP628000
RTM880N-796-- AL000880001

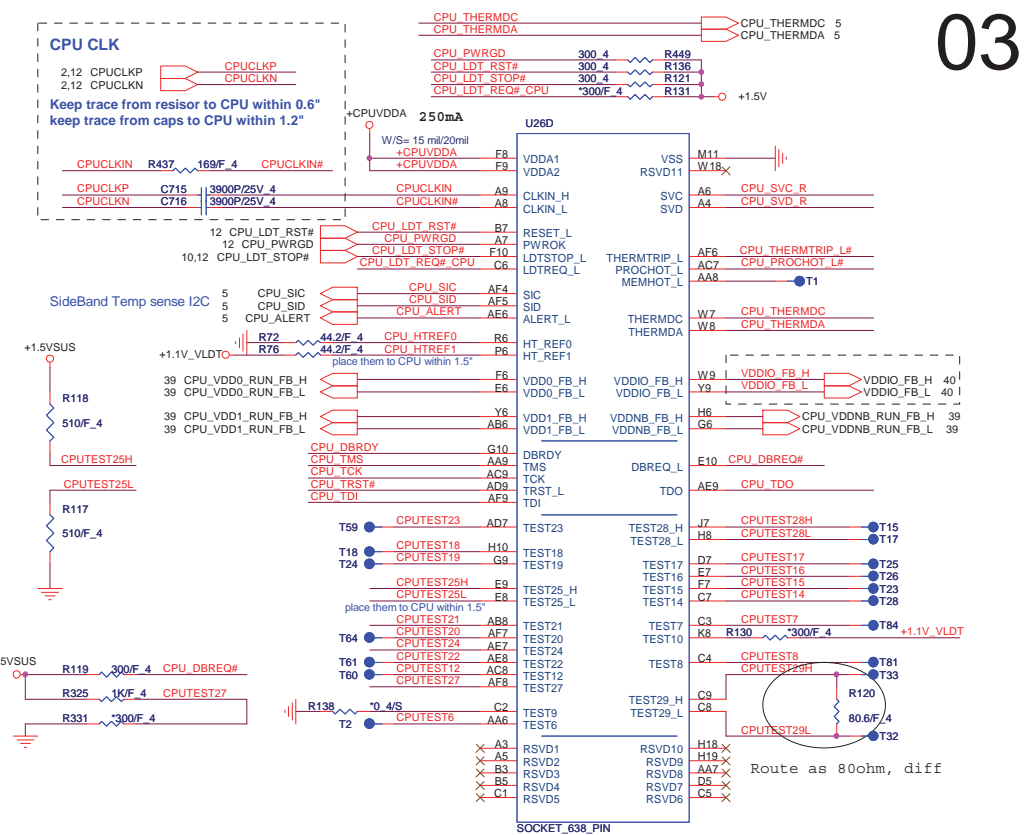
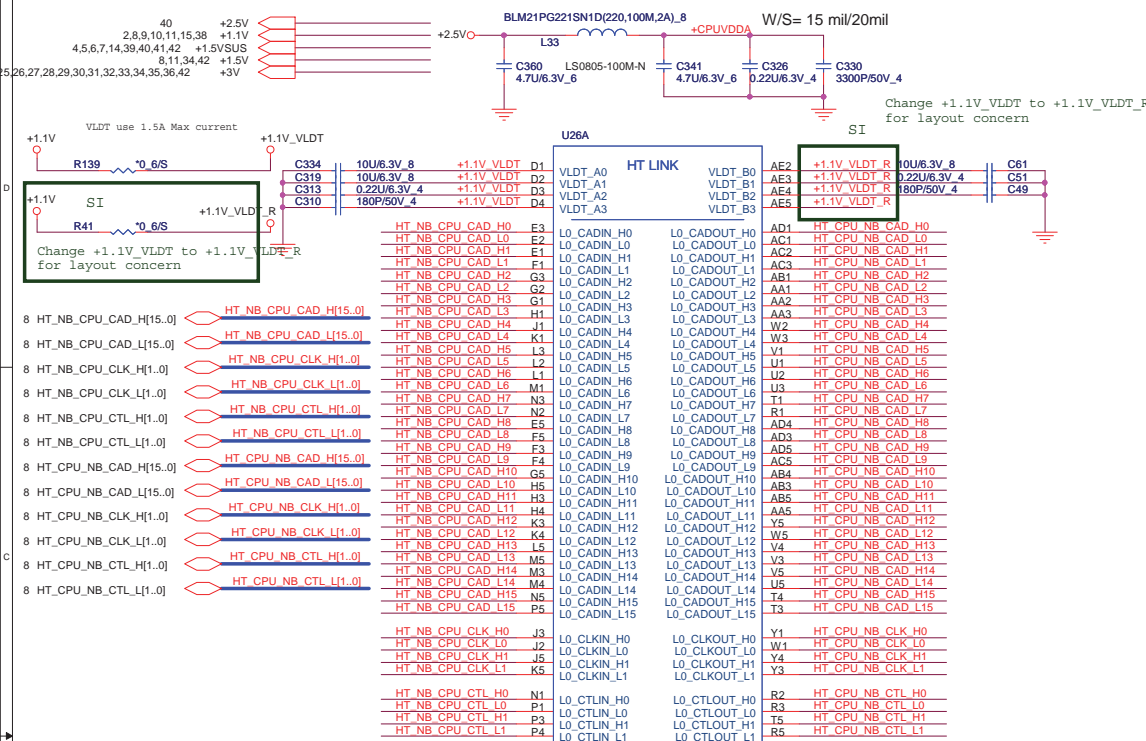
* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



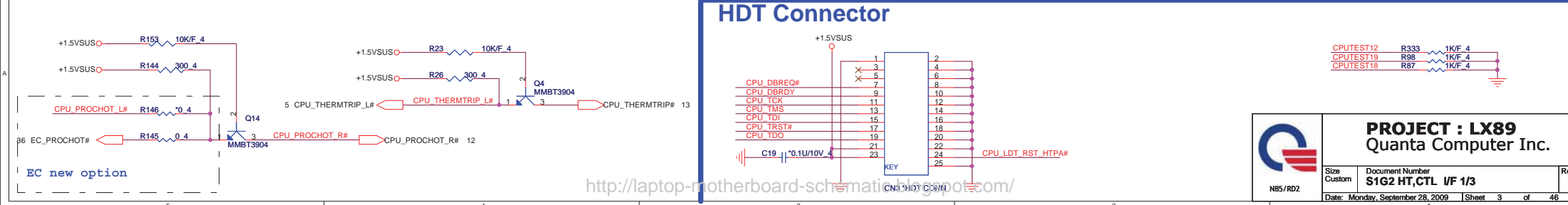
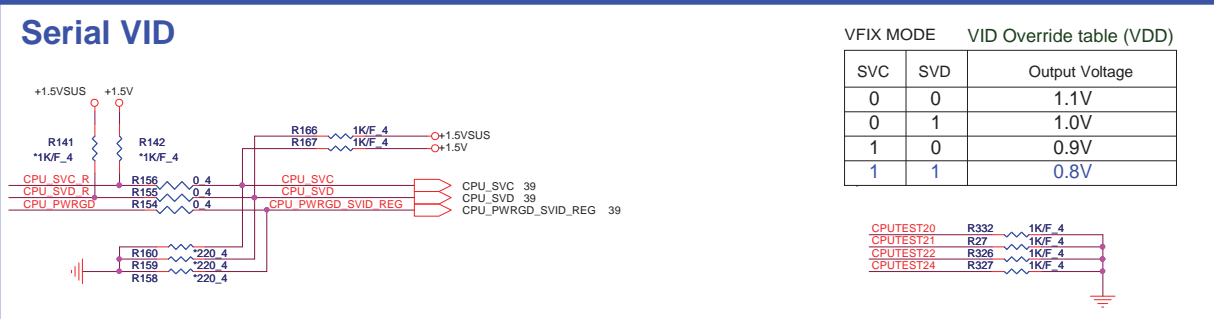
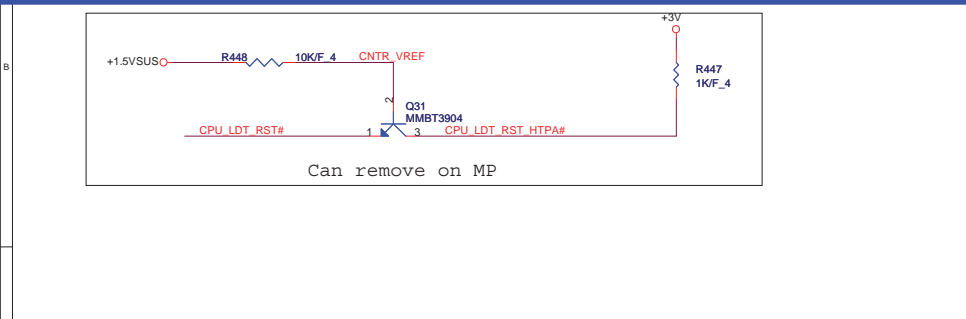
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

not need to stuff, R185 have pull LOW



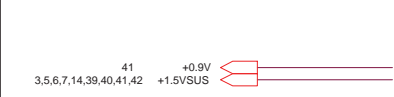
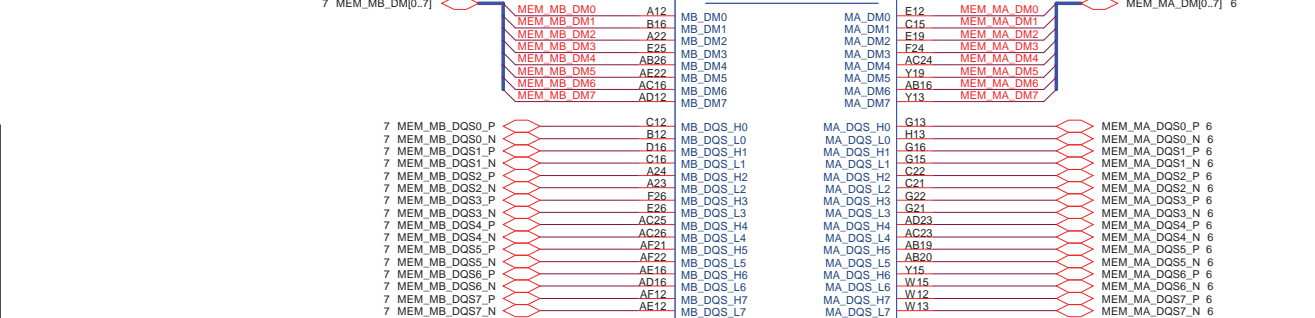
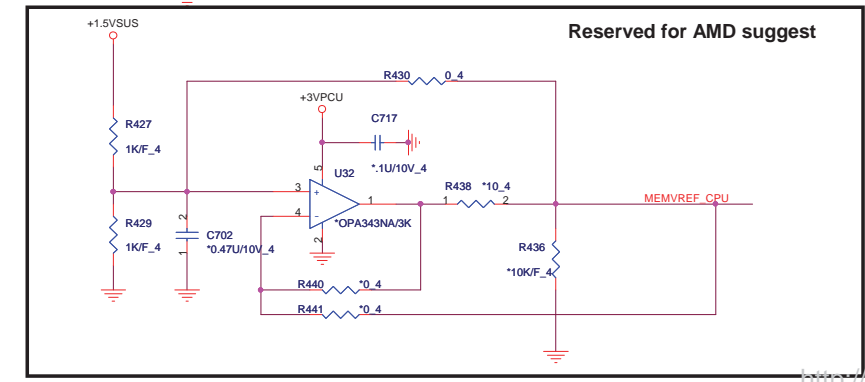
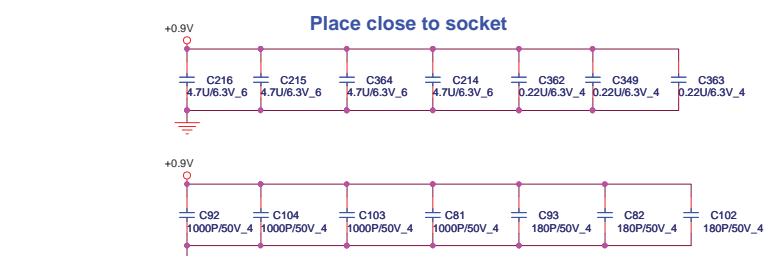
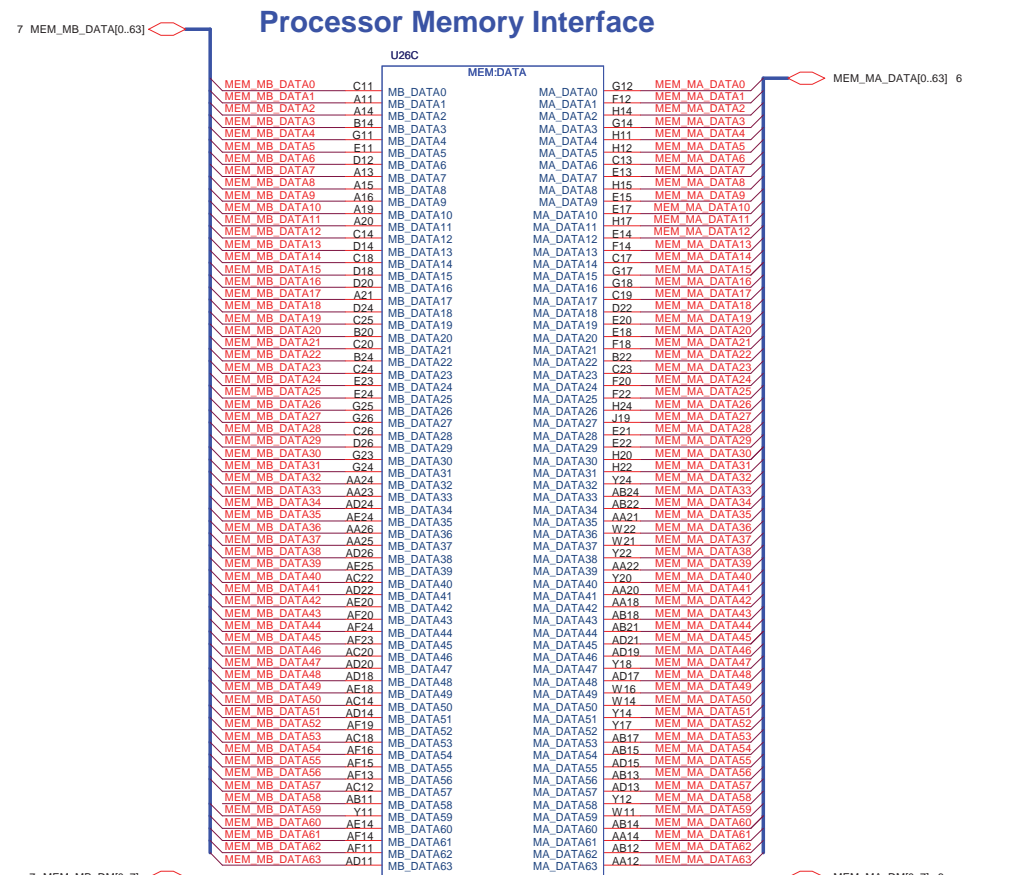
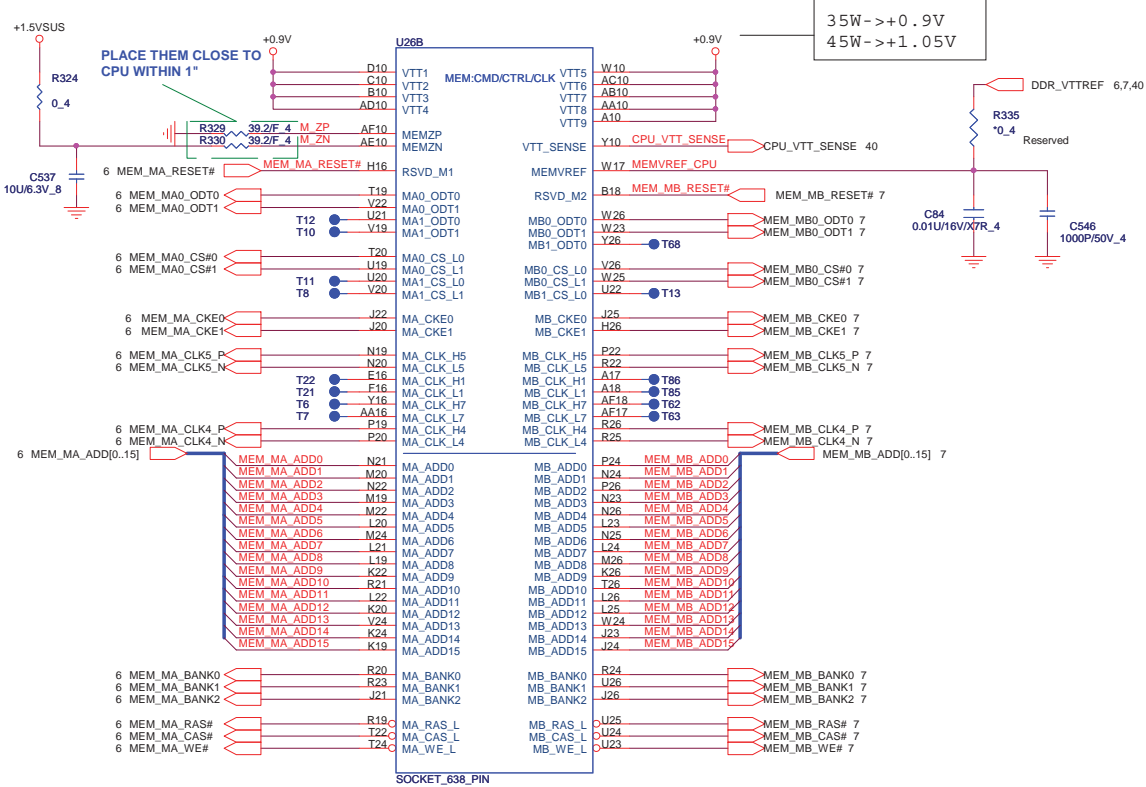
FOX PZ63826-284R-41F
DG0*8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0*8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0*8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

SOCKET_638_PIN



PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number S1G2 HT,CTL VF 1/3 Rev 1A
Date: Monday, September 28, 2009 Sheet 3 of 46

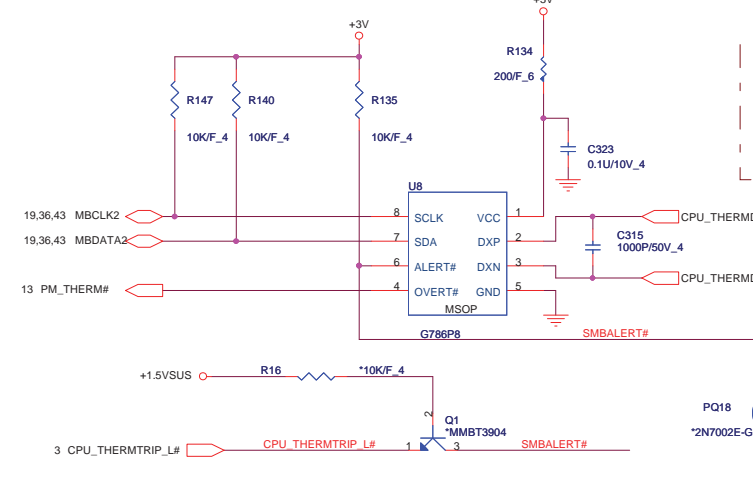
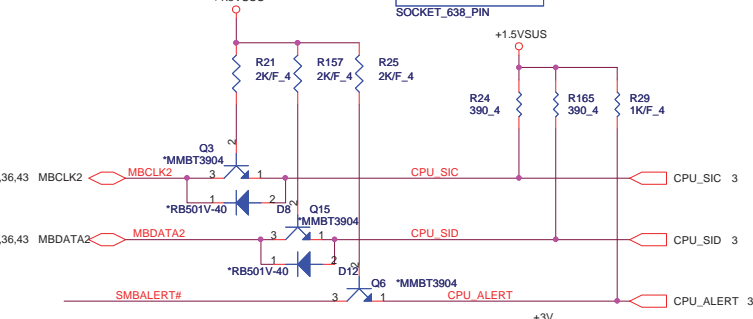
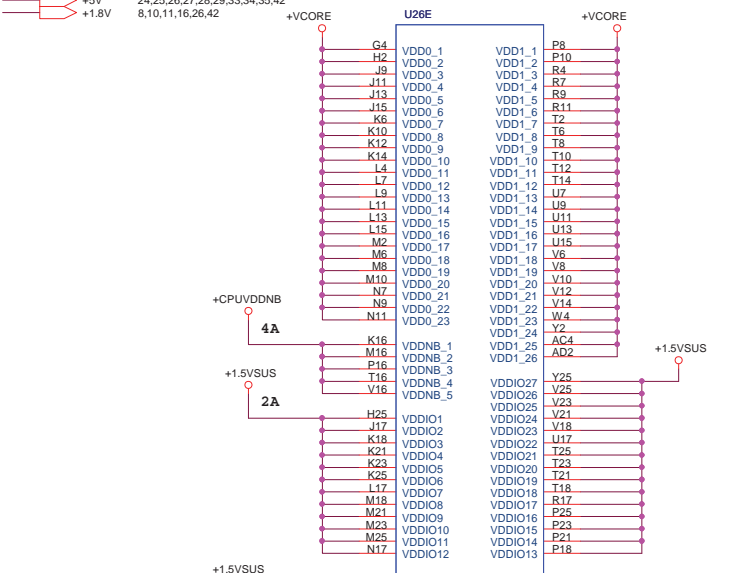


<http://laptop-motherboard-schematic.blogspot.com/>

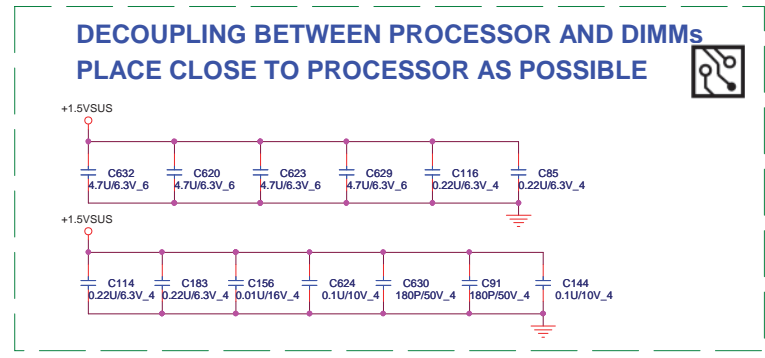
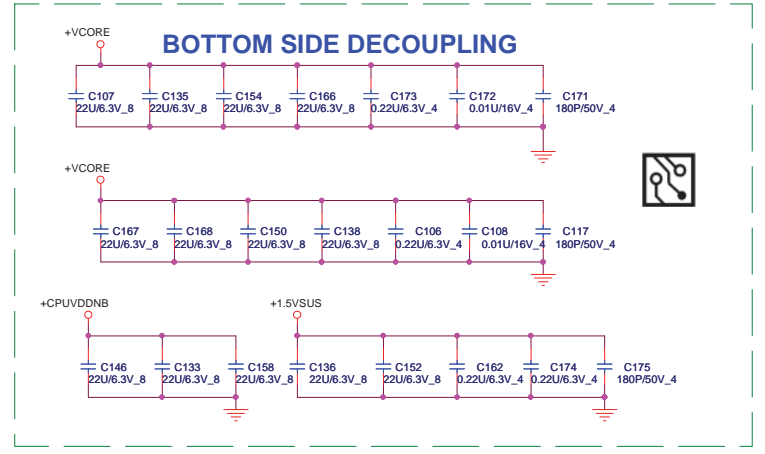
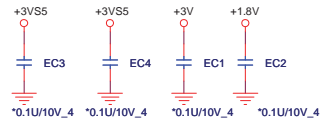
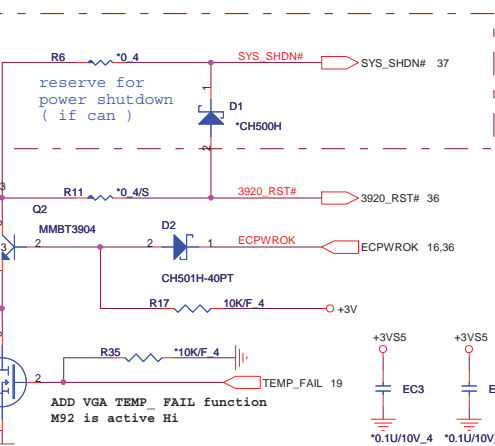
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number S1G2 DDR1 MEMORY I/F 2/3	Rev 1A
Date: Monday, September 28, 2009		Sheet 4 of 46

- +VCORE 39
- +CPUVDDNB 39
- +1.5VSUS 3,4,6,7,14,39,40,41,42
- +3VS5 12,13,14,15,16,42
- +5V 24,25,26,27,28,29,33,34,35,42
- +1.8V 8,10,11,16,26,42



PROCESSOR POWER AND GROUND



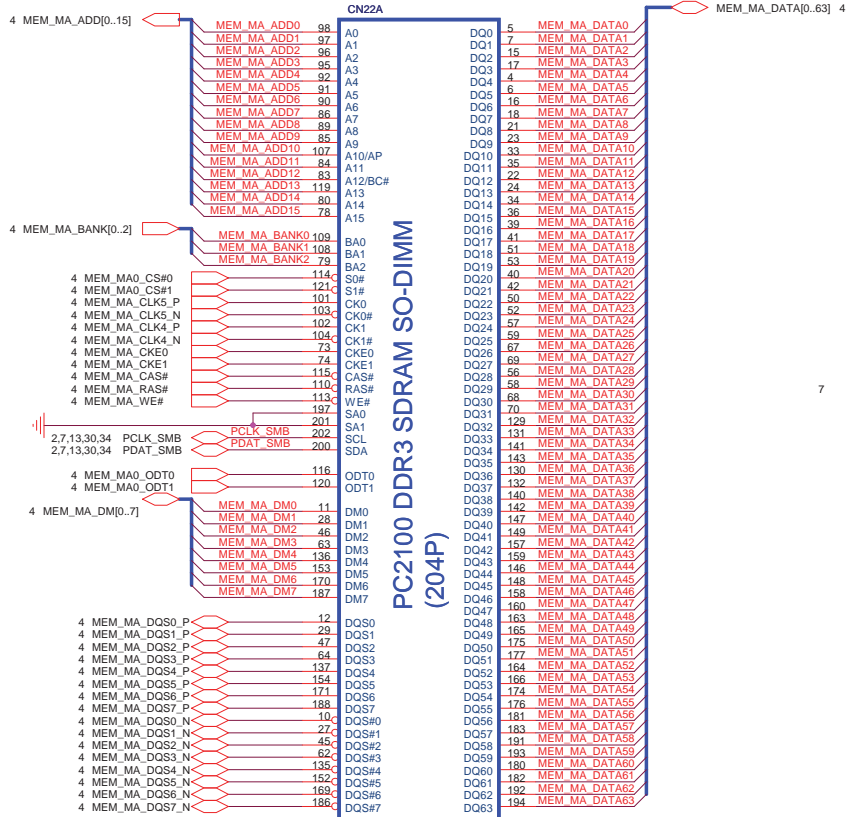
Need Check

For fix HyperTransport nets across plane splits

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	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	S1G2 PWR & GND 3/3	
Date: Monday, September 28, 2009		Sheet 5	of 46

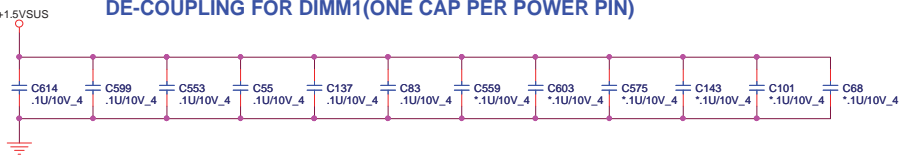
+1.5VSUS 3,4,5,7,14,38,40,41,42
+3V 2,3,5,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 7,40



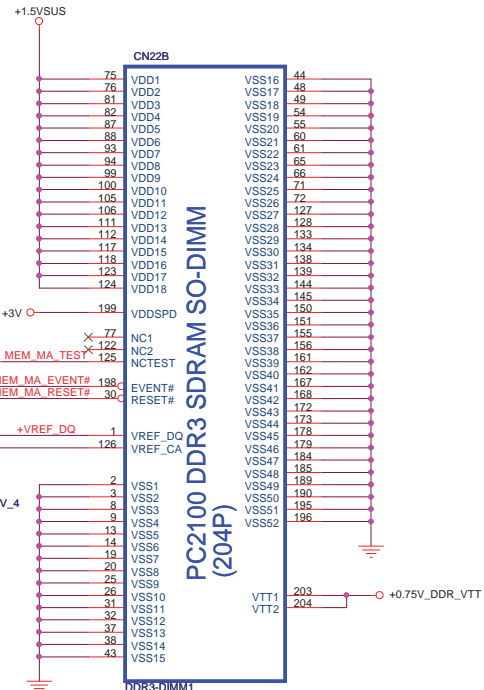
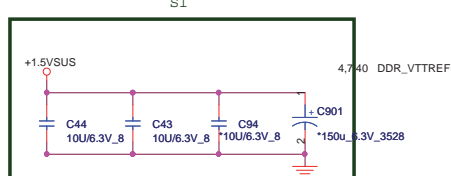
DDR3-DIMM1
H=5.2 footprint: "ddr-c-2013289-204p"
DGMK4000059

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

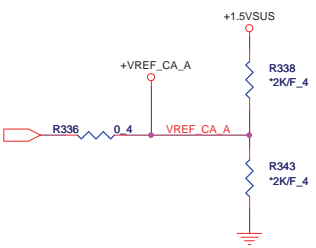
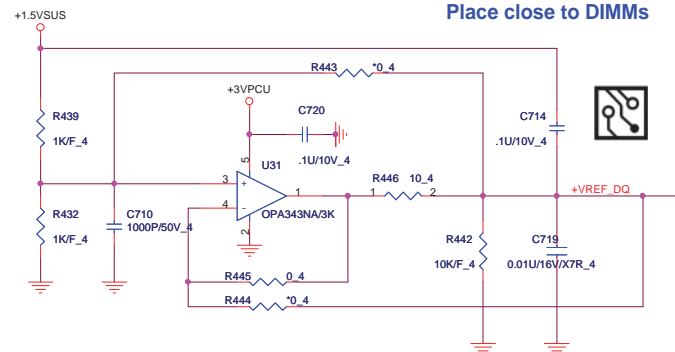


DE-COUPLING FOR DIMM1



H=5.2 footprint: "ddr-c-2013289-204p"
DGMK4000059

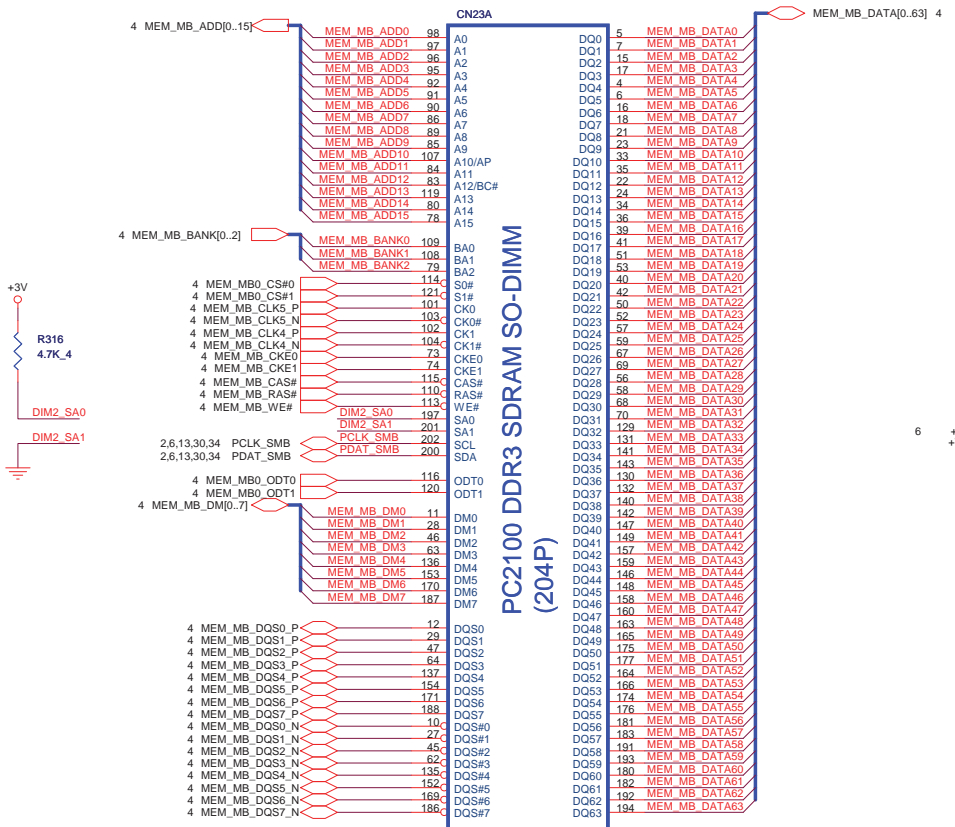
Place close to DIMMs



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	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	DDR3 SODIMMS: A/B CHANNEL	
Date: Monday, September 28, 2009	Sheet 6	of 46	

+1.5VSUS 3,4,5,6,14,39,40,41,42
+3V 2,3,5,6,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 6,40

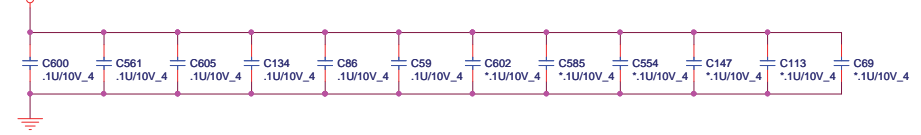


PC2100 DDR3 SDRAM SO-DIMM (204P)

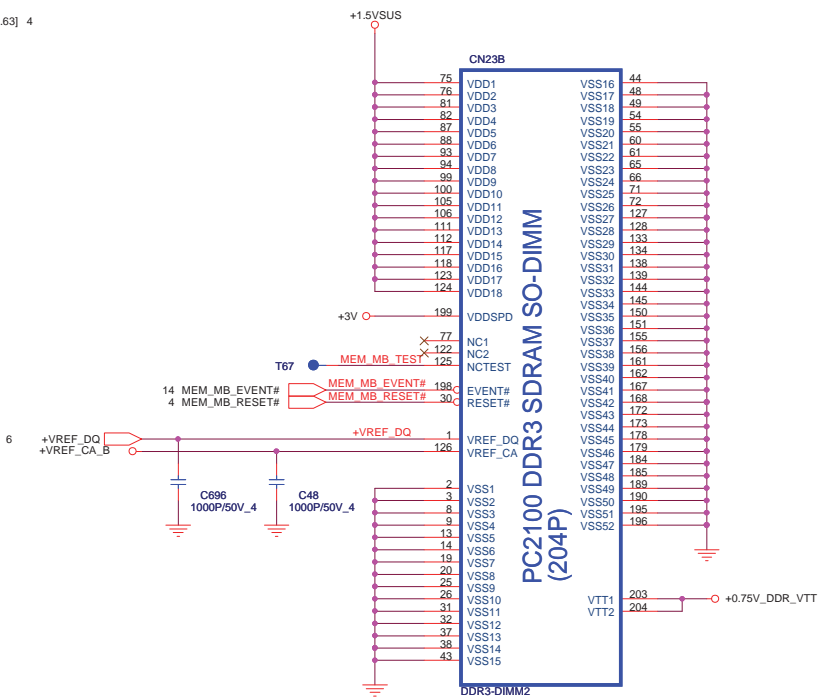
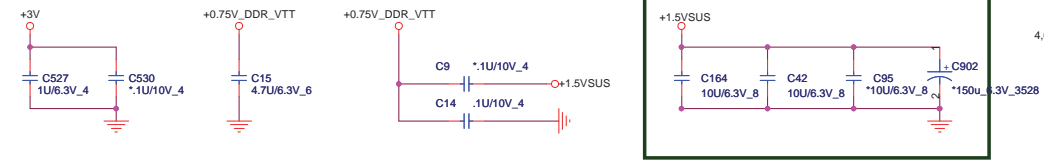
DDR3-DIMM2
H=9.2 footprint: "ddr-c-2013310-204p-1"

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



DE-COUPLING FOR DIMM2



PC2100 DDR3 SDRAM SO-DIMM (204P)

H=9.2 footprint: "ddr-c-2013310-204p-1"
DGMK4000058

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR3 SODIMMS TERMINATIONS		
Date: Monday, September 28, 2009	Sheet 7	of 46



- HT_CPU_NB_CAD_H[15..0] HT_CPU_NB_CAD_H[15..0] 3
- HT_CPU_NB_CAD_L[15..0] HT_CPU_NB_CAD_L[15..0] 3
- HT_CPU_NB_CLK_H[1..0] HT_CPU_NB_CLK_H[1..0] 3
- HT_CPU_NB_CLK_L[1..0] HT_CPU_NB_CLK_L[1..0] 3
- HT_CPU_NB_CTL_H[1..0] HT_CPU_NB_CTL_H[1..0] 3
- HT_CPU_NB_CTL_L[1..0] HT_CPU_NB_CTL_L[1..0] 3
- HT_NB_CPU_CAD_H[15..0] HT_NB_CPU_CAD_H[15..0] 3
- HT_NB_CPU_CAD_L[15..0] HT_NB_CPU_CAD_L[15..0] 3
- HT_NB_CPU_CLK_H[1..0] HT_NB_CPU_CLK_H[1..0] 3
- HT_NB_CPU_CLK_L[1..0] HT_NB_CPU_CLK_L[1..0] 3
- HT_NB_CPU_CTL_H[1..0] HT_NB_CPU_CTL_H[1..0] 3
- HT_NB_CPU_CTL_L[1..0] HT_NB_CPU_CTL_L[1..0] 3

- HT_CPU_NB_CAD_H0 Y25
- HT_CPU_NB_CAD_L0 Y24
- HT_CPU_NB_CAD_H1 V22
- HT_CPU_NB_CAD_L1 V23
- HT_CPU_NB_CAD_H2 V25
- HT_CPU_NB_CAD_L2 V24
- HT_CPU_NB_CAD_H3 U24
- HT_CPU_NB_CAD_L3 U25
- HT_CPU_NB_CAD_H4 T25
- HT_CPU_NB_CAD_L4 T24
- HT_CPU_NB_CAD_H5 P22
- HT_CPU_NB_CAD_L5 P23
- HT_CPU_NB_CAD_H6 P25
- HT_CPU_NB_CAD_L6 P24
- HT_CPU_NB_CAD_H7 N24
- HT_CPU_NB_CAD_L7 N25

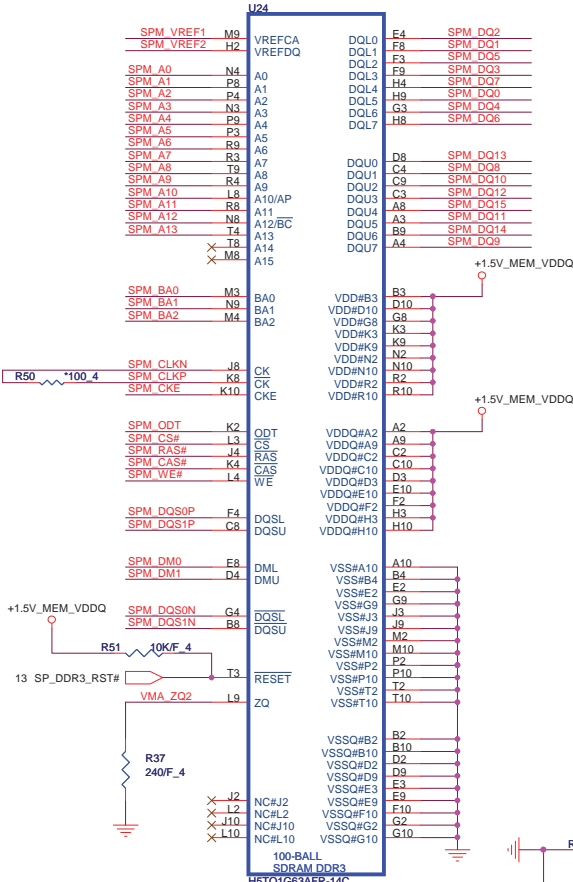
PART 1 OF 6
HYPER TRANSPORT CPU I/F

- D24 HT_NB_CPU_CAD_H0
- D25 HT_NB_CPU_CAD_L0
- E24 HT_NB_CPU_CAD_H1
- E25 HT_NB_CPU_CAD_L1
- F24 HT_NB_CPU_CAD_H2
- F25 HT_NB_CPU_CAD_L2
- F23 HT_NB_CPU_CAD_H3
- F22 HT_NB_CPU_CAD_L3
- H23 HT_NB_CPU_CAD_H4
- H22 HT_NB_CPU_CAD_L4
- J25 HT_NB_CPU_CAD_H5
- J24 HT_NB_CPU_CAD_L5
- K24 HT_NB_CPU_CAD_H6
- K23 HT_NB_CPU_CAD_L6
- K22 HT_NB_CPU_CAD_L7

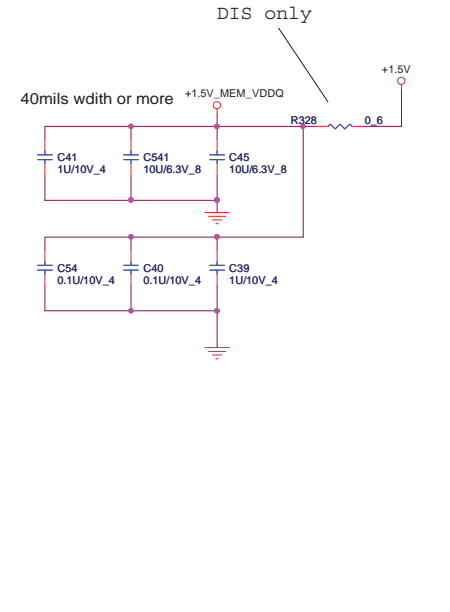
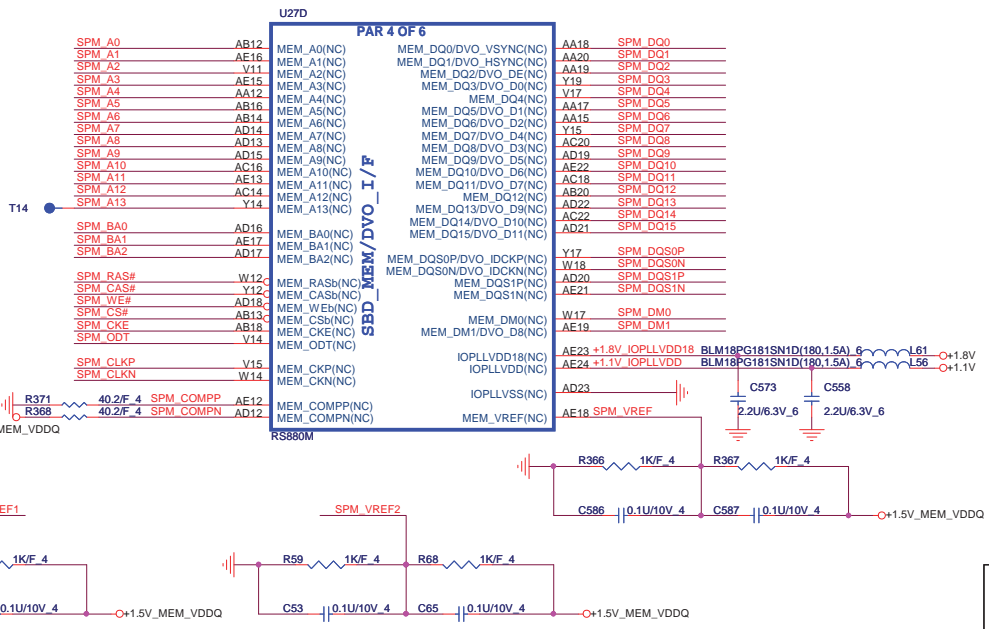
- HT_RXCAD8P D24
- HT_RXCAD8N D25
- HT_RXCAD9P E24
- HT_RXCAD9N E25
- HT_RXCAD10P F24
- HT_RXCAD10N F25
- HT_RXCAD11P F23
- HT_RXCAD11N F22
- HT_RXCAD12P H23
- HT_RXCAD12N H22
- HT_RXCAD13P J25
- HT_RXCAD13N J24
- HT_RXCAD14P K24
- HT_RXCAD14N K23
- HT_RXCAD15P K22
- HT_RXCAD15N K21



signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		



This block is for UMA only, DIS can remove all component



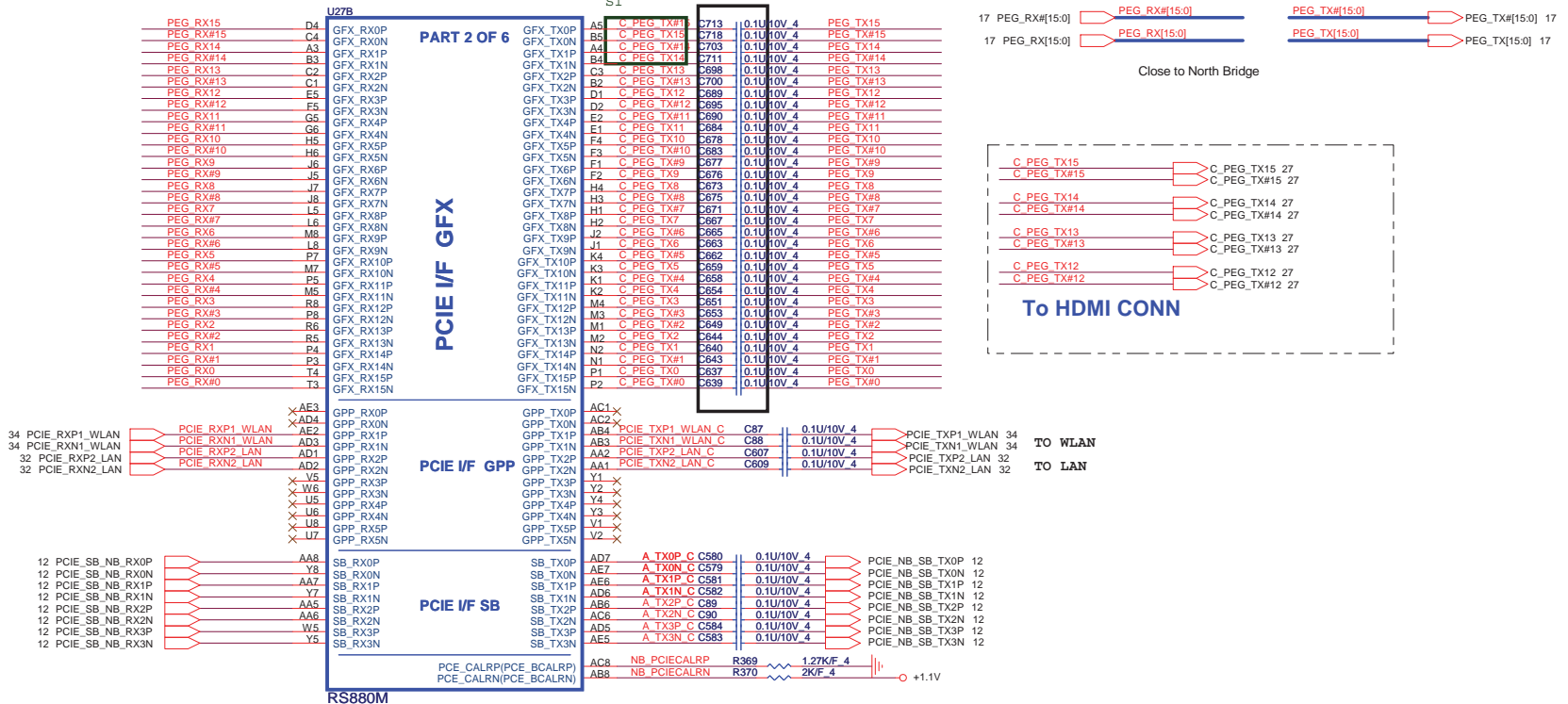
PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number **RS880-HT LINK I/F 1/5** Rev 1A

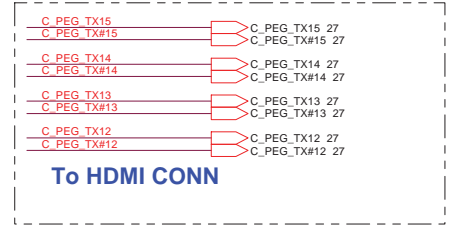
Date: Monday, September 28, 2009 Sheet 8 of 46

UMA Remove All Cap

Swap pin for Layout



Close to North Bridge



RS880M

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



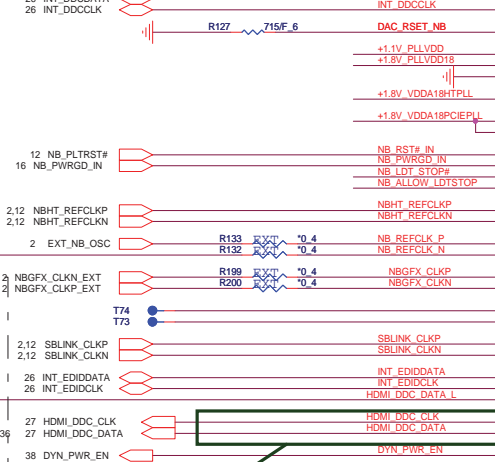
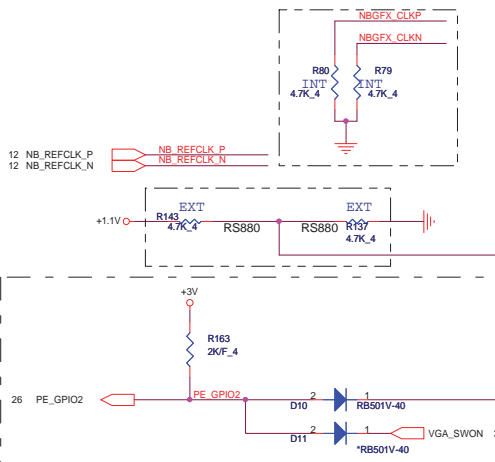
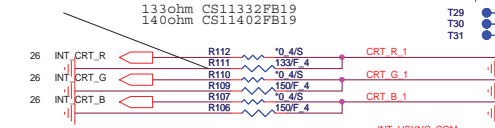
PROJECT : LX89
 Quanta Computer Inc.

Size Custom Document Number **RS880-PCIE I/F 2/5** Rev 1A

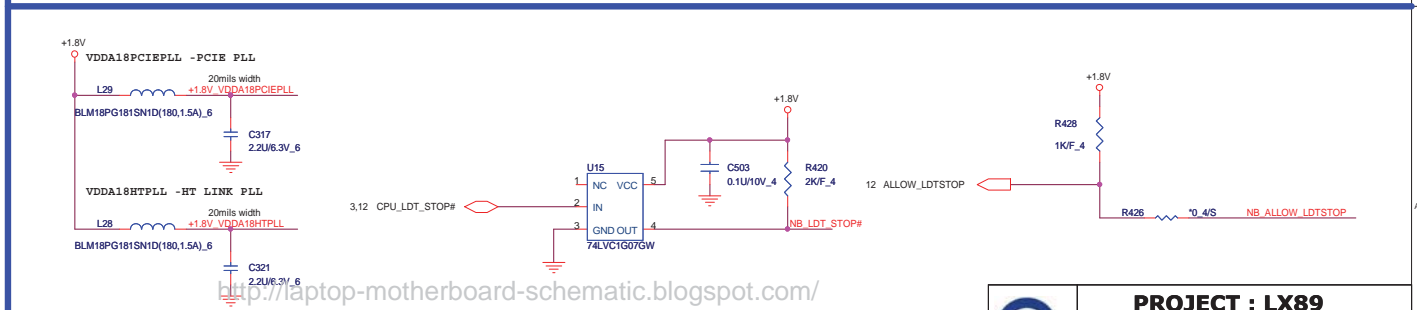
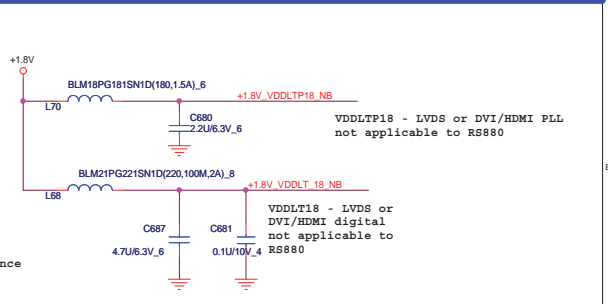
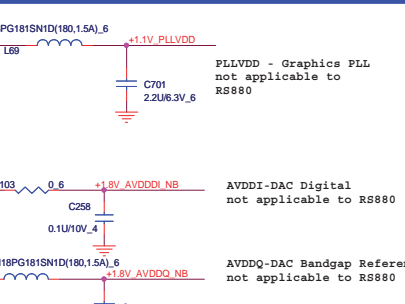
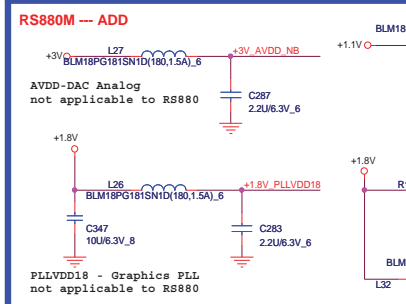
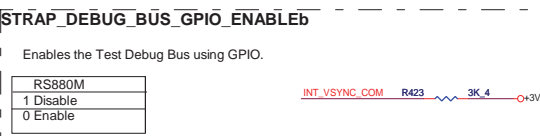
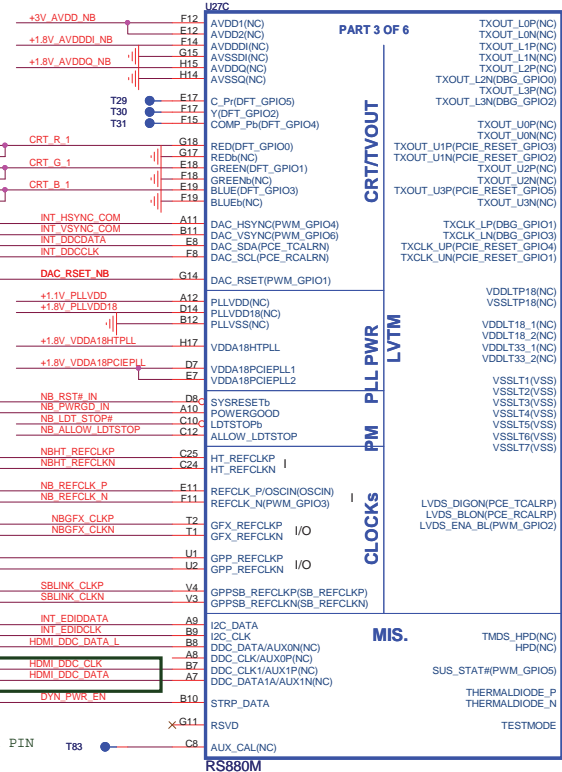
Date: Monday, September 28, 2009 Sheet 9 of 46

+3V 2,3,5,6,7,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
 +1.8V 5,8,11,16,26,42
 +1.1V 2,3,8,9,11,15,38
 +1.5V 3,8,11,34,42

R111 for UMA use 140 ohm
 for DIS+PowerExpress use 133 ohm (AMD)

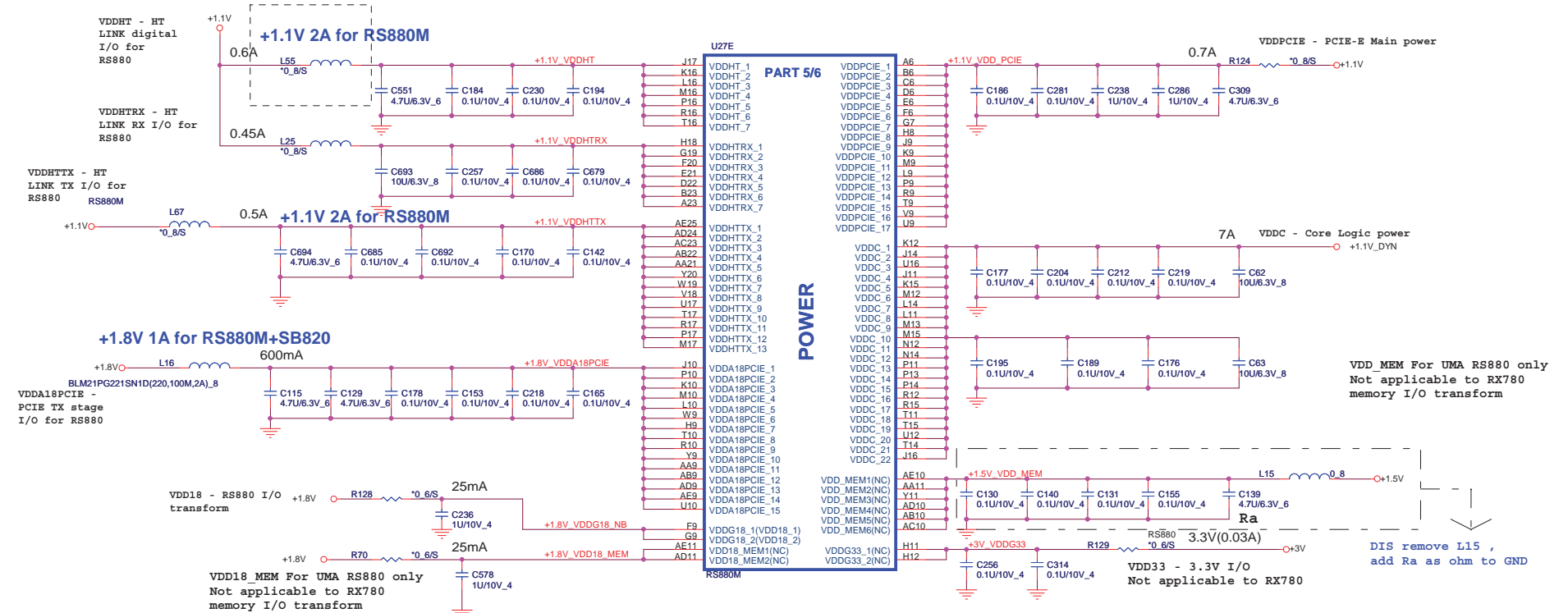
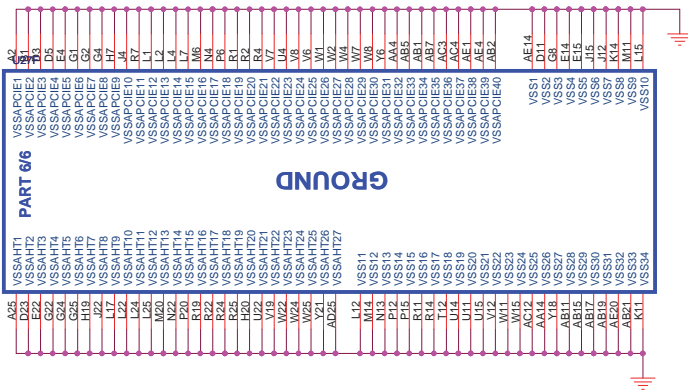


Change HDMI CLK/DATA PIN for AMD recommend



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL18	NC



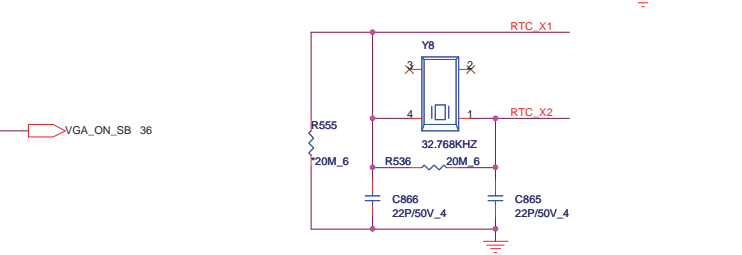
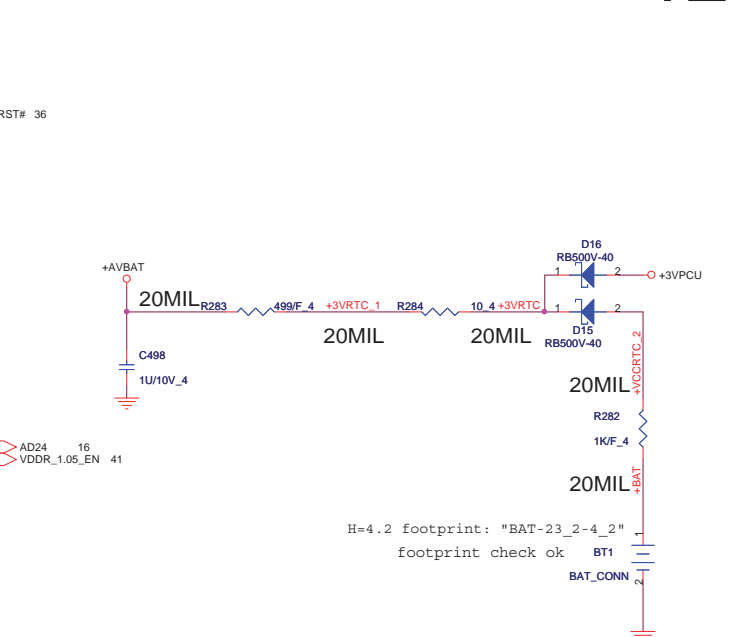
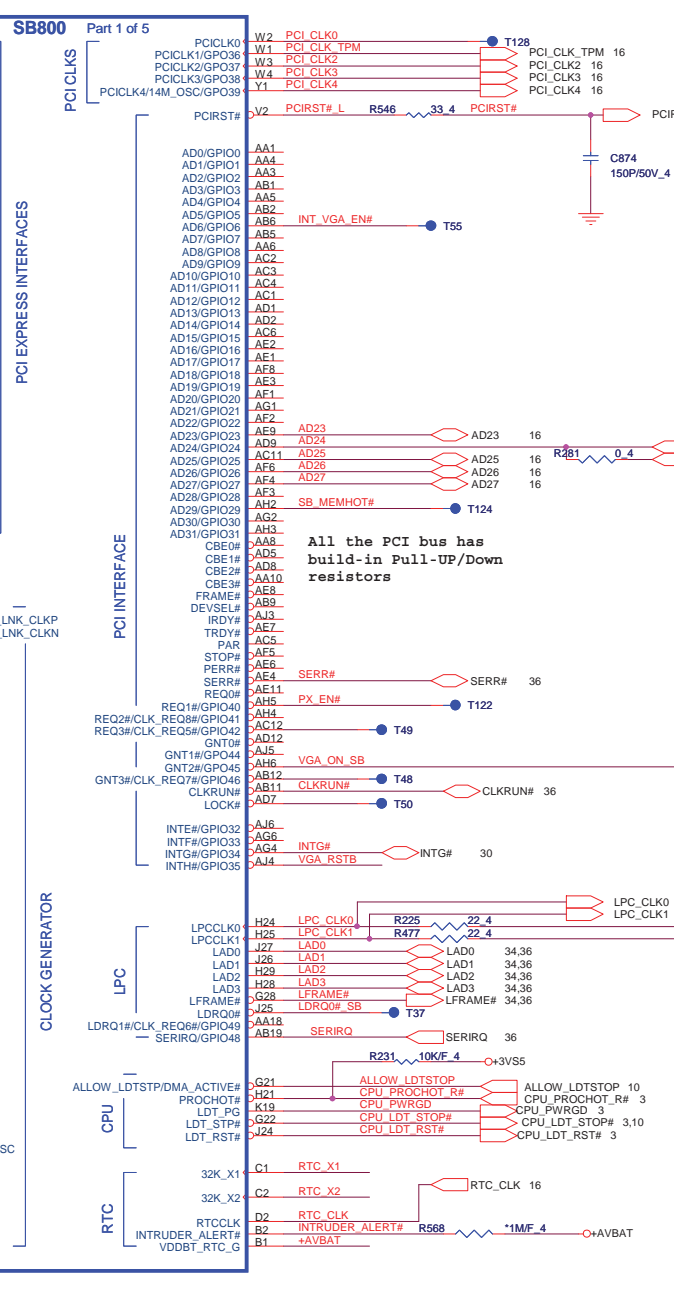
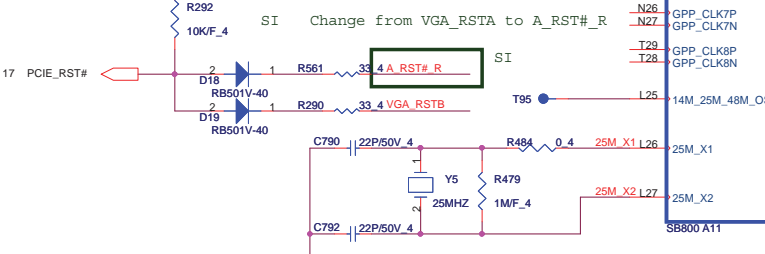
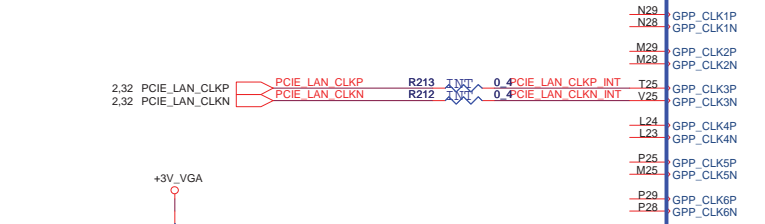
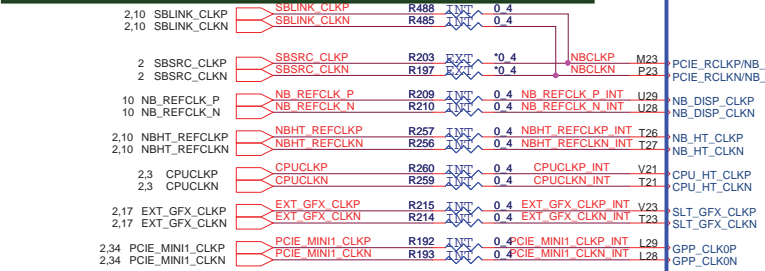
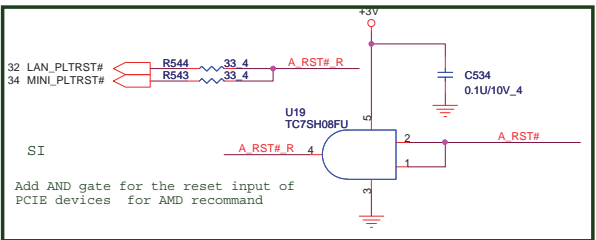
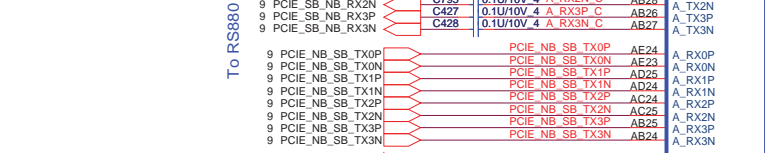
PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number **RS880-POWER5/5** Rev 1A

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+1.1V_PCIE_VDDR 15
+3V_VGA 21,41
+3VS5 5,13,14,15,16,42
+3VPCU 4,6,24,33,35,36,37,38,39,40,41,42,43

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U7007



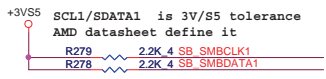
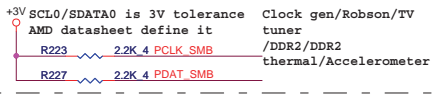
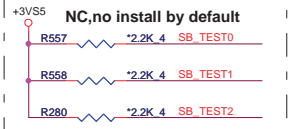
INTRUDER ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

<http://laptop-motherboard-schematic.blogspot.com/>

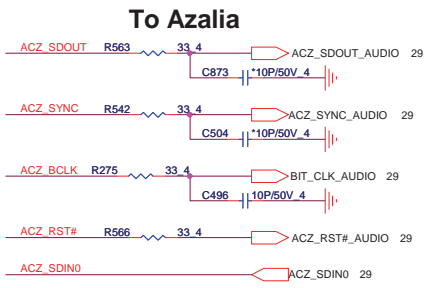
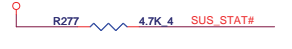
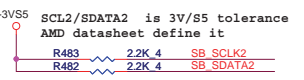
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-PCIE/PCICPU/LPC 1/4	Rev 1A
Date: Monday, September 28, 2009	Sheet 12	of 46

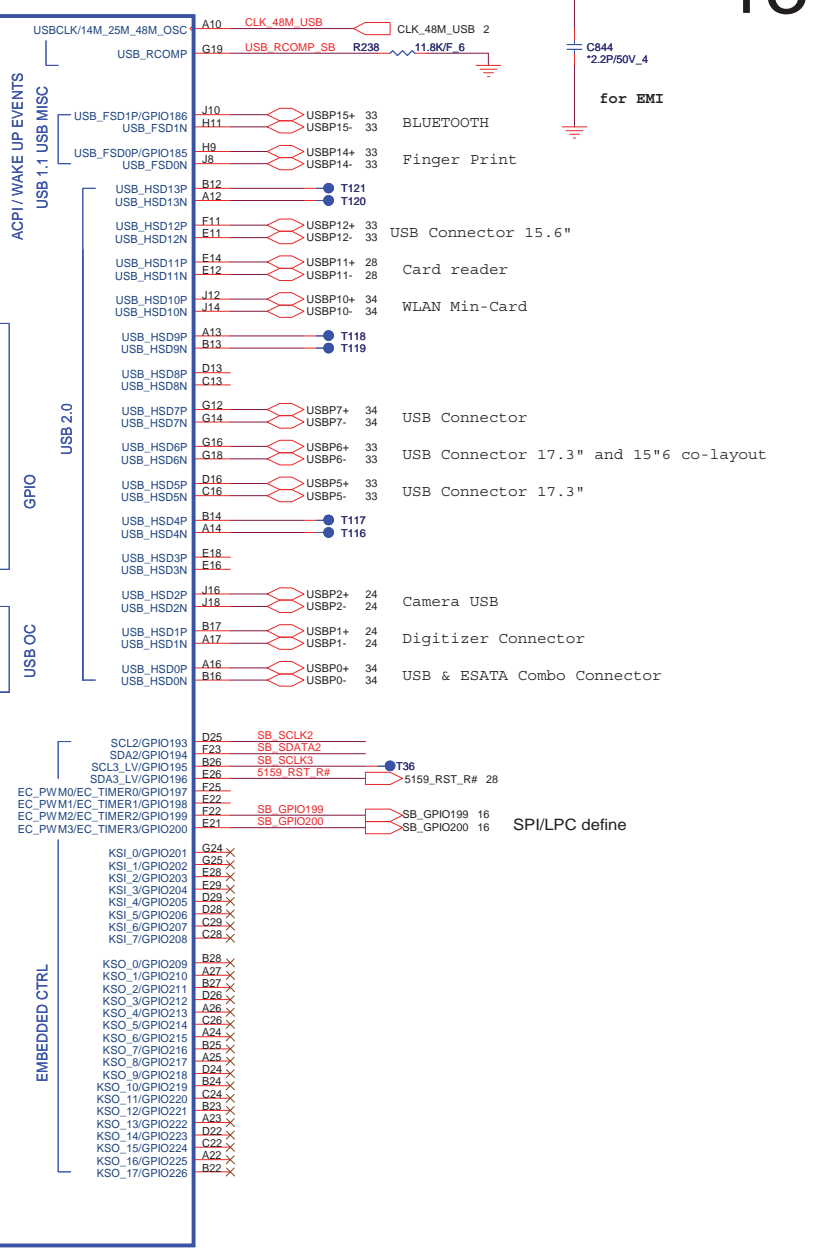
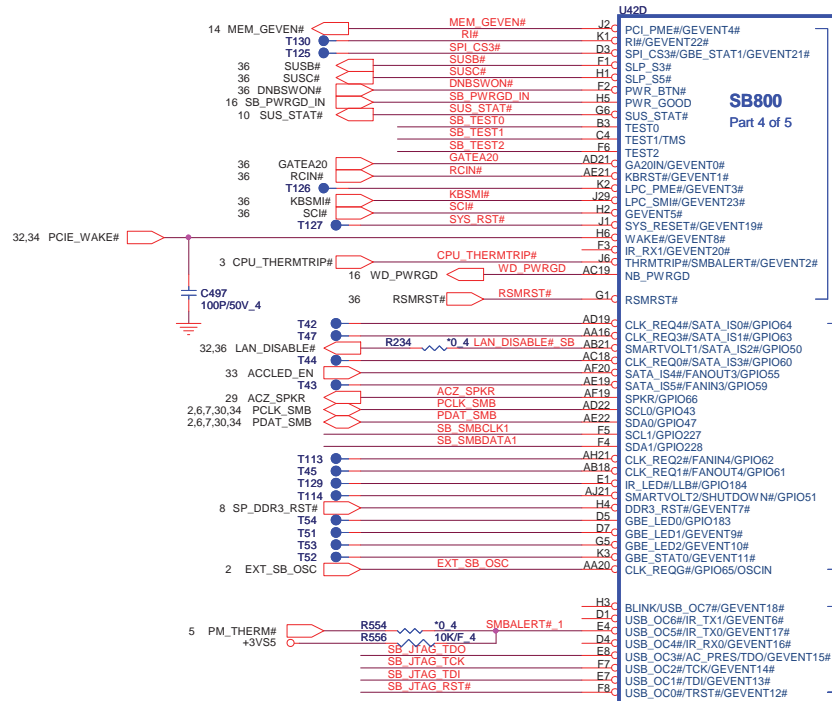
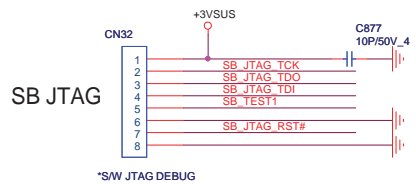
NBS/RD2



remove pull hi
(chip internal
have pull hi)



- +3VSUS 28,33,34,35,41,42
- +3V 2,3,5,6,7,10,11,12,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +3VSS 5,12,14,15,16,42



PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number **SB820-ACPI/USB 2/4** Rev 1A

Date: Monday, September 28, 2009 Sheet 13 of 46

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

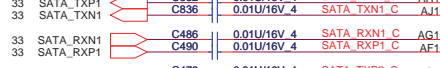
IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY



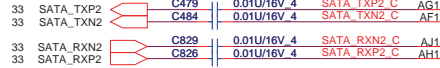
SATA1 HDD



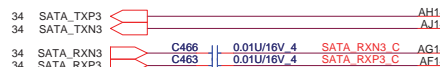
SATA ODD



SATA2 HDD



E-SATA



XTLVDD SATA-- SATA
crystal power

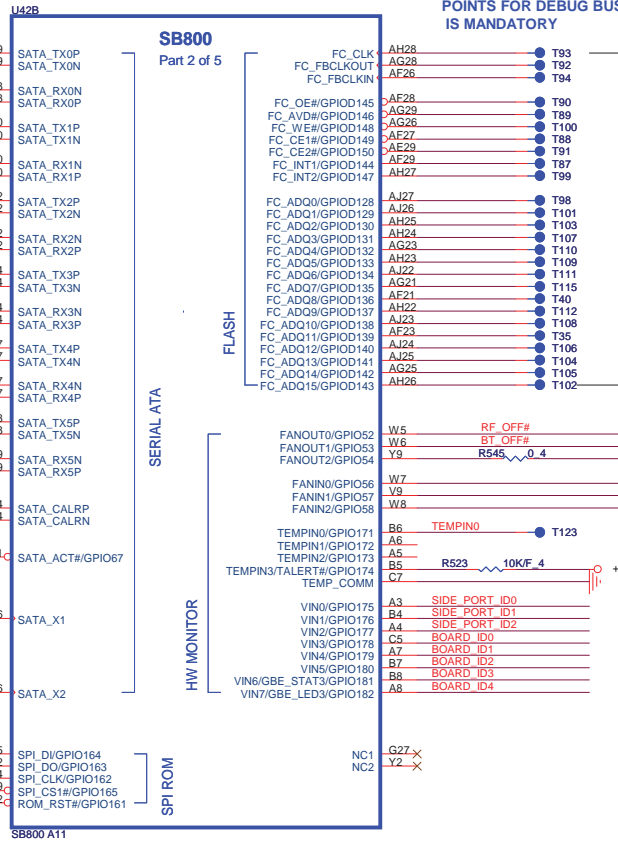
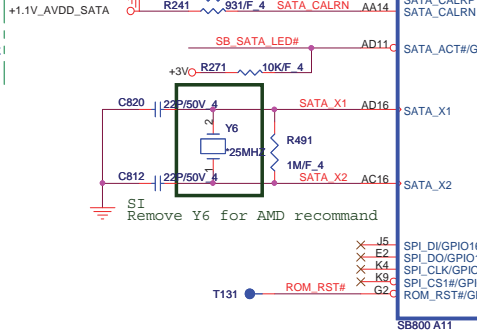
PLVDD SATA--
SATA PLL
POWER



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

NOTE:

R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

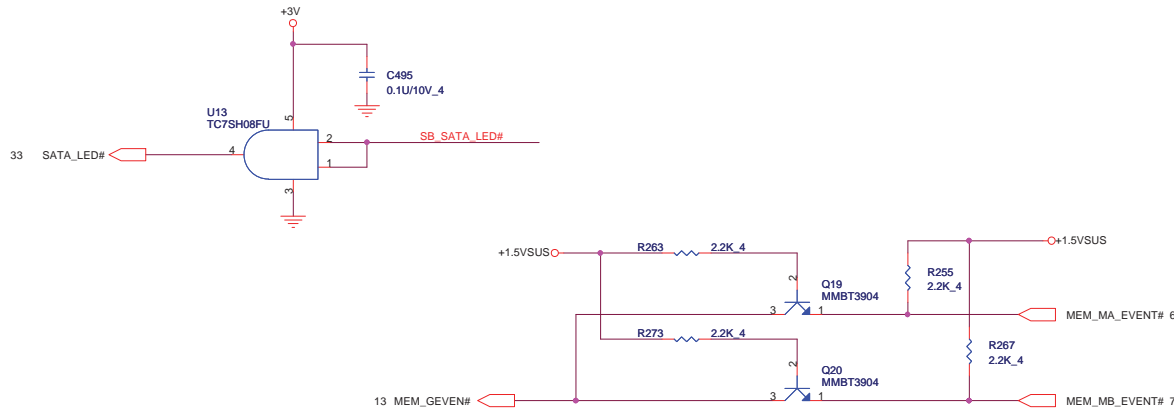


IF USE, power need ready

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port



ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX8 Park
0	0	1	0	0	LX9 Park
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	

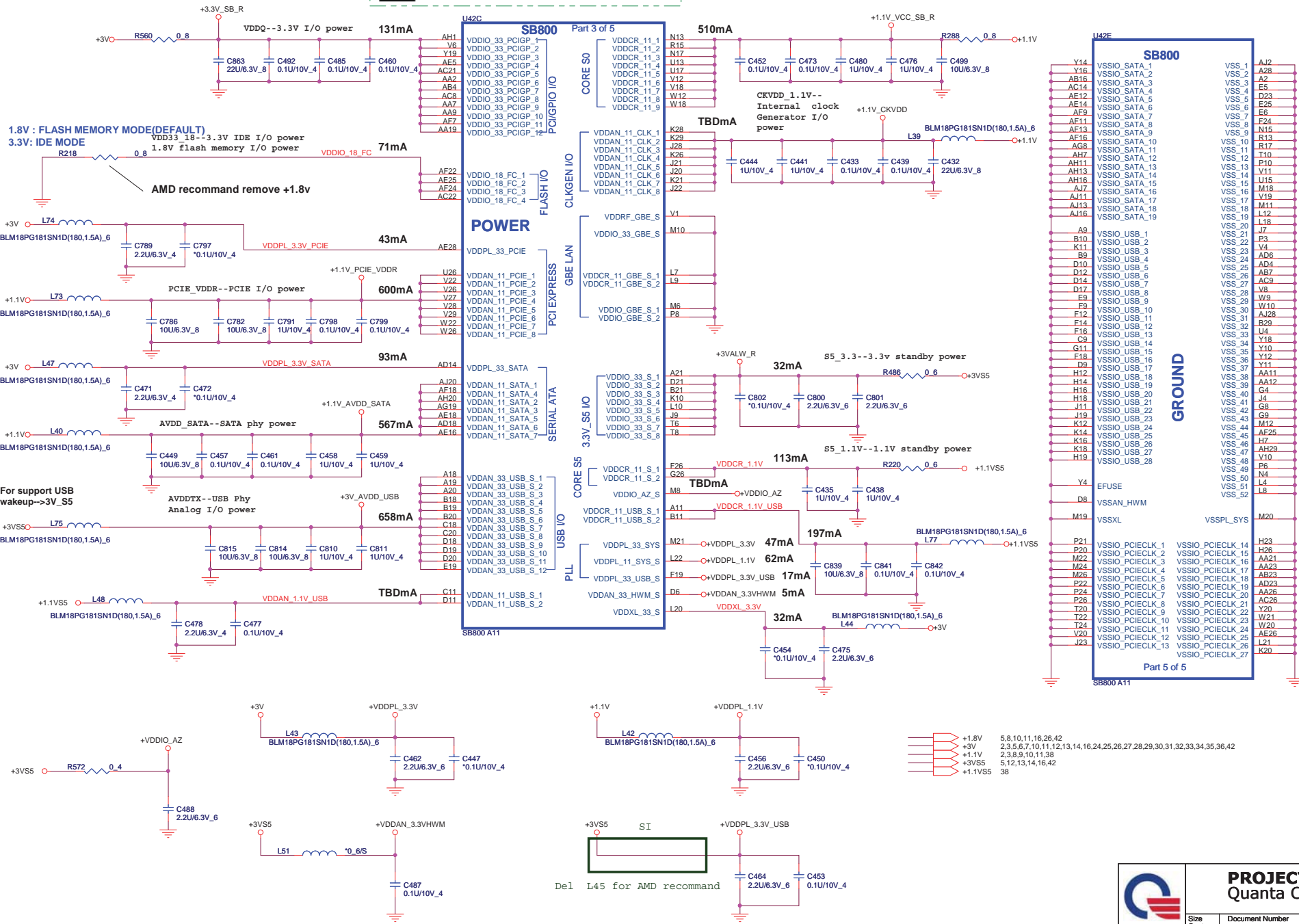


PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-ACPI/GPIO/USB 2J4	Rev 1A
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power



SB800

Part 5 of 5

Y14	VSSIO_SATA_1	VSS_1	A/J2
Y16	VSSIO_SATA_2	VSS_2	A/28
AB16	VSSIO_SATA_3	VSS_3	A/2
AC14	VSSIO_SATA_4	VSS_4	E/5
AE12	VSSIO_SATA_5	VSS_5	D/23
E25	VSSIO_SATA_6	VSS_6	E/6
AF9	VSSIO_SATA_7	VSS_7	F/24
AF11	VSSIO_SATA_8	VSS_8	F/8
AF13	VSSIO_SATA_9	VSS_9	N/15
AF16	VSSIO_SATA_10	VSS_10	R/13
AG8	VSSIO_SATA_11	VSS_11	R/17
AH7	VSSIO_SATA_12	VSS_12	T/10
AH11	VSSIO_SATA_13	VSS_13	P/10
AH13	VSSIO_SATA_14	VSS_14	V/11
AH16	VSSIO_SATA_15	VSS_15	U/15
AH7	VSSIO_SATA_16	VSS_16	M/18
AJ11	VSSIO_SATA_17	VSS_17	V/19
AJ13	VSSIO_SATA_18	VSS_18	M/11
AJ16	VSSIO_SATA_19	VSS_19	M/12
A9	VSSIO_USB_1	VSS_20	L/18
B10	VSSIO_USB_2	VSS_21	J/7
K11	VSSIO_USB_3	VSS_22	P/3
B9	VSSIO_USB_4	VSS_23	V/4
D10	VSSIO_USB_5	VSS_24	A/06
D12	VSSIO_USB_6	VSS_25	A/06
D14	VSSIO_USB_7	VSS_26	A/07
D17	VSSIO_USB_8	VSS_27	A/09
E9	VSSIO_USB_9	VSS_28	W/9
F9	VSSIO_USB_10	VSS_29	W/10
F12	VSSIO_USB_11	VSS_30	A/28
F14	VSSIO_USB_12	VSS_31	W/10
F16	VSSIO_USB_13	VSS_32	A/28
G9	VSSIO_USB_14	VSS_33	Y/18
G11	VSSIO_USB_15	VSS_34	Y/10
F18	VSSIO_USB_16	VSS_35	Y/2
D9	VSSIO_USB_17	VSS_36	Y/2
H12	VSSIO_USB_18	VSS_37	Y/11
H14	VSSIO_USB_19	VSS_38	Y/11
H16	VSSIO_USB_20	VSS_39	A/12
J11	VSSIO_USB_21	VSS_40	G/4
J18	VSSIO_USB_22	VSS_41	G/4
J19	VSSIO_USB_23	VSS_42	J/8
K12	VSSIO_USB_24	VSS_43	J/8
K14	VSSIO_USB_25	VSS_44	G/9
K16	VSSIO_USB_26	VSS_45	M/12
K18	VSSIO_USB_27	VSS_46	A/25
H19	VSSIO_USB_28	VSS_47	A/25
		VSS_48	V/10
		VSS_49	P/6
		VSS_50	N/4
Y4	EFUSE	VSS_51	L/8
D8	VSSAN_HWM	VSS_52	L/8
M19	VSSXL	VSSPLL_SYS	M/20
P21	VSSIO_PCIECLK_1	VSSIO_PCIECLK_14	H/23
P20	VSSIO_PCIECLK_2	VSSIO_PCIECLK_15	H/23
M22	VSSIO_PCIECLK_3	VSSIO_PCIECLK_16	AA/21
M24	VSSIO_PCIECLK_4	VSSIO_PCIECLK_17	AA/23
M26	VSSIO_PCIECLK_5	VSSIO_PCIECLK_18	AB/23
P22	VSSIO_PCIECLK_6	VSSIO_PCIECLK_19	AB/23
P24	VSSIO_PCIECLK_7	VSSIO_PCIECLK_20	AA/26
P26	VSSIO_PCIECLK_8	VSSIO_PCIECLK_21	AC/26
T20	VSSIO_PCIECLK_9	VSSIO_PCIECLK_22	Y/20
T22	VSSIO_PCIECLK_10	VSSIO_PCIECLK_23	W/21
T24	VSSIO_PCIECLK_11	VSSIO_PCIECLK_24	W/20
V20	VSSIO_PCIECLK_12	VSSIO_PCIECLK_25	AE/26
J23	VSSIO_PCIECLK_13	VSSIO_PCIECLK_26	L/21
		VSSIO_PCIECLK_27	K/20

- +1.8V 5,8,10,11,16,26,42
- +3V 2,3,5,6,7,10,11,12,13,14,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +1.1V 2,3,8,9,10,11,38
- +3VSS 5,12,13,14,16,42
- +1.1VSS 38

Del L45 for AMD recommend

PROJECT : LX89
Quanta Computer Inc.

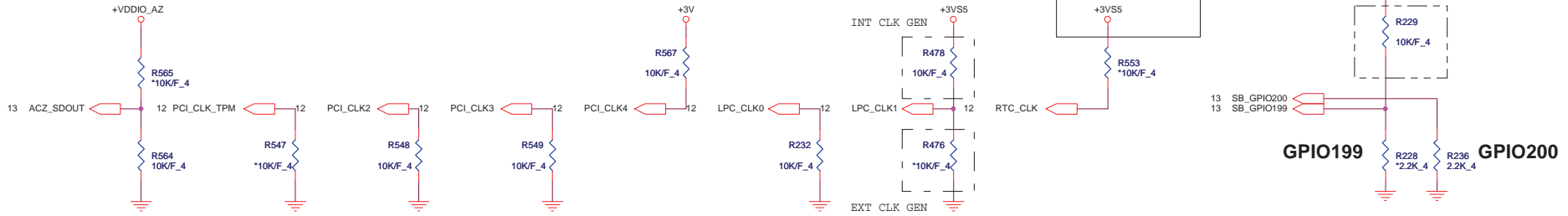
Size Custom	Document Number SB820-PWR/DECOUPLING 4/4	Rev 1A
Date: Monday, September 28, 2009		Sheet 15 of 46

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull Hi 10K , confirm AMD ward this pull Hi not need

- +VDDIO_AZ 15
- +3V 2,3,5,6,7,10,11,12,13,14,15,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +3VS5 5,12,13,14,15,42
- +1.8V 5,8,10,11,26,42



It must ready before RSMRST#

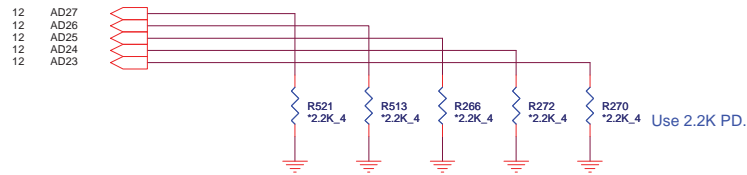
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

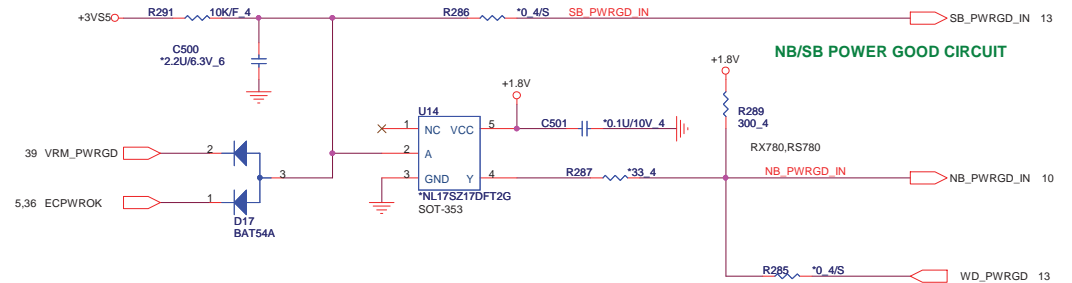
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



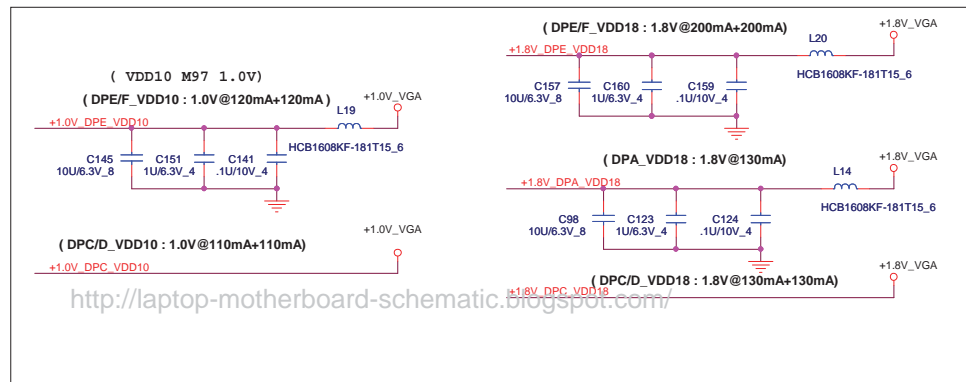
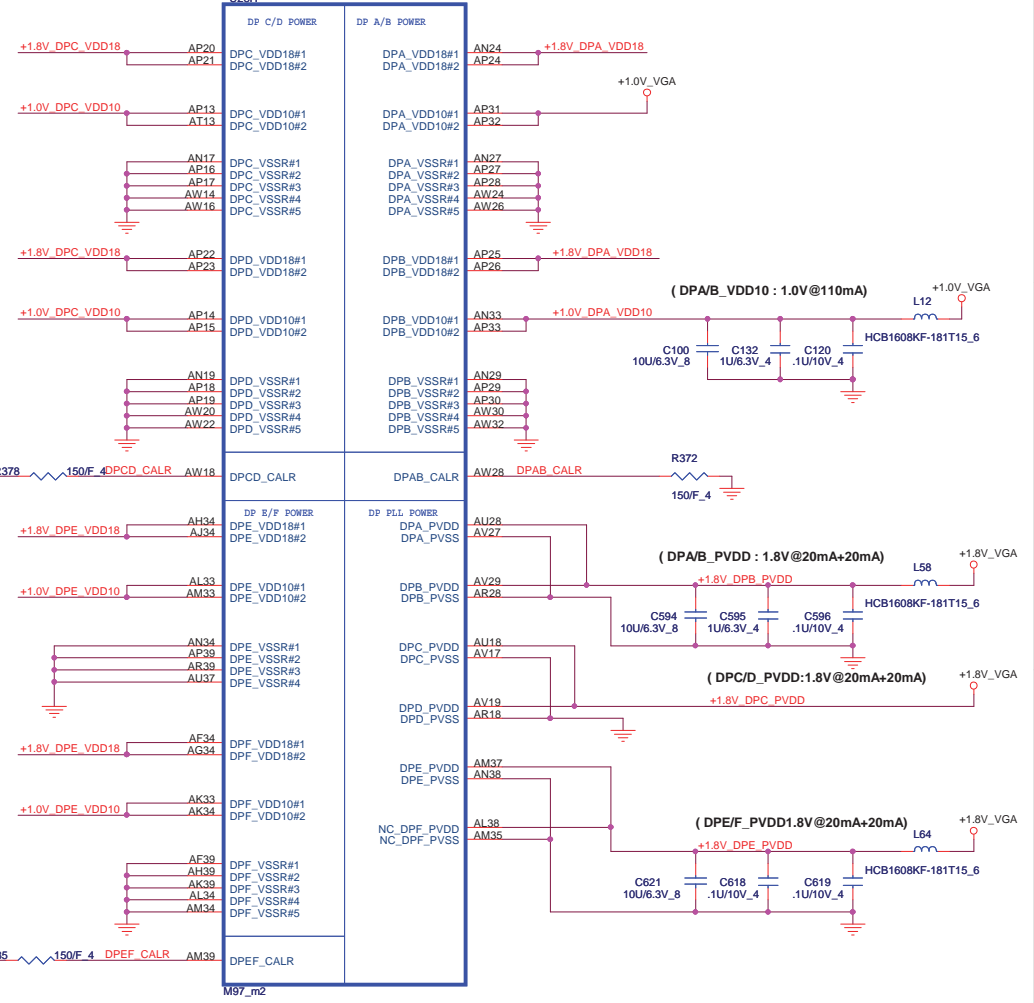
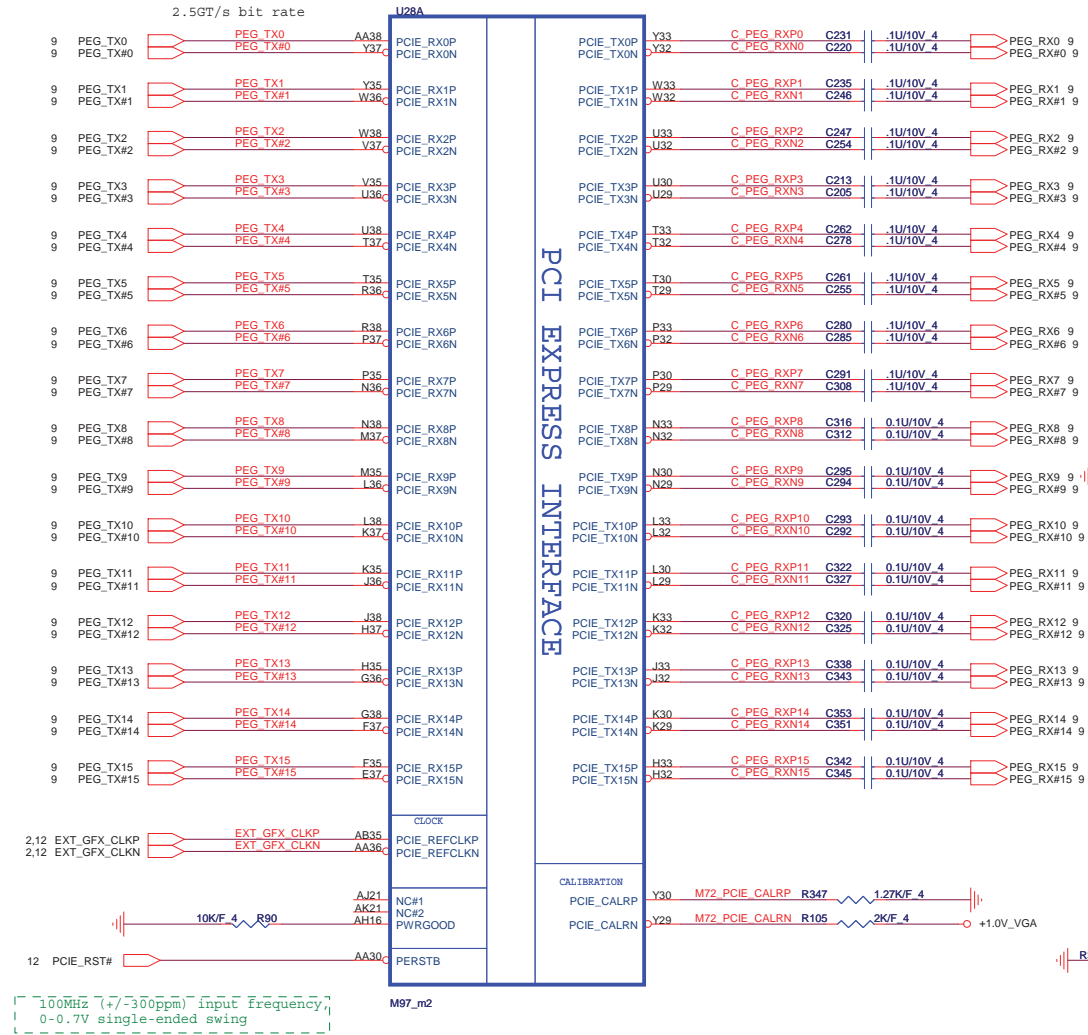
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



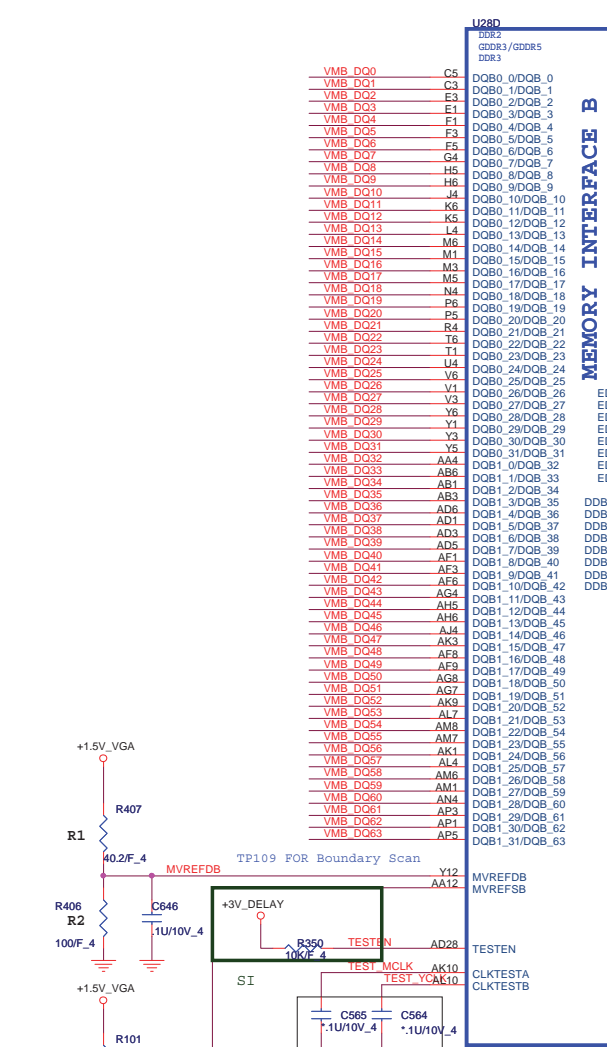
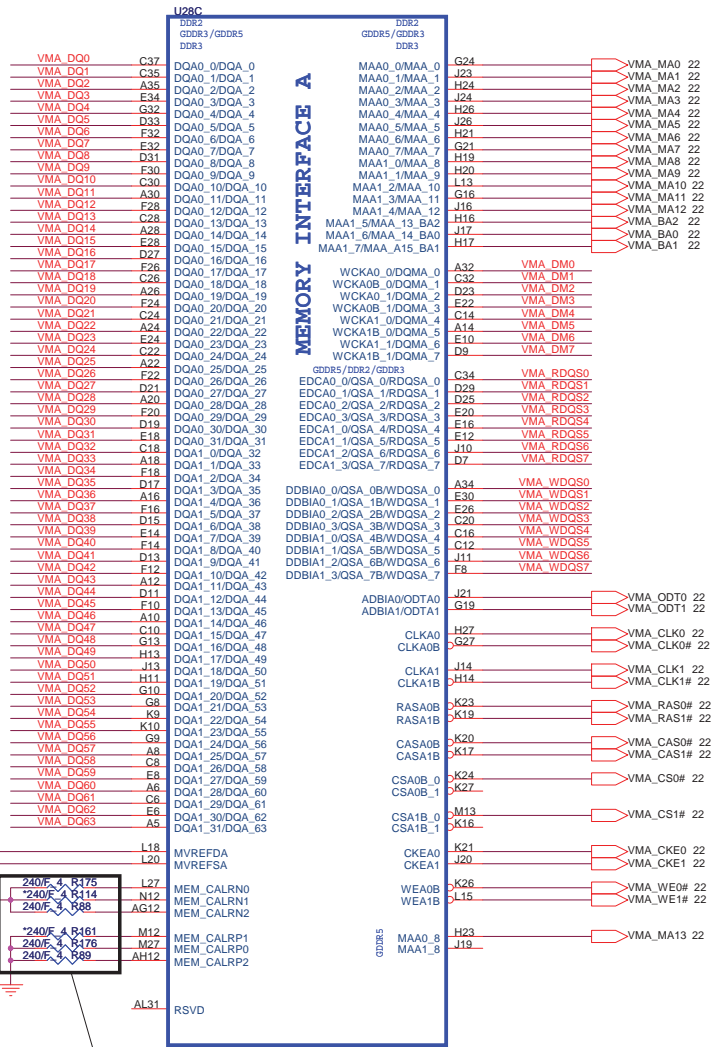
- AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
- ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

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	Quanta Computer Inc.		
	Size Custom	Document Number SB820-STRAPS	
NB5/RD2	Date: Monday, September 28, 2009	Sheet 16 of 46	



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Quanta Computer Inc.

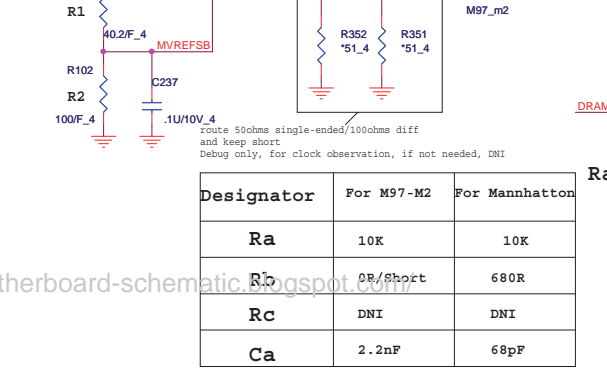
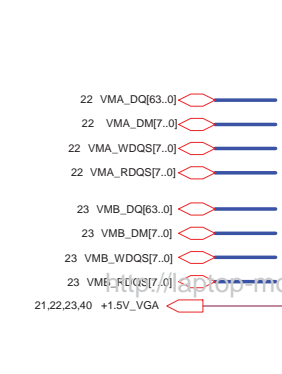
Size Custom	Document Number ATI Park/Madison (PCI E I/F) 1/5	Rev 1A
NB5/RDZ	Date: Monday, September 28, 2009	Sheet 17 of 46



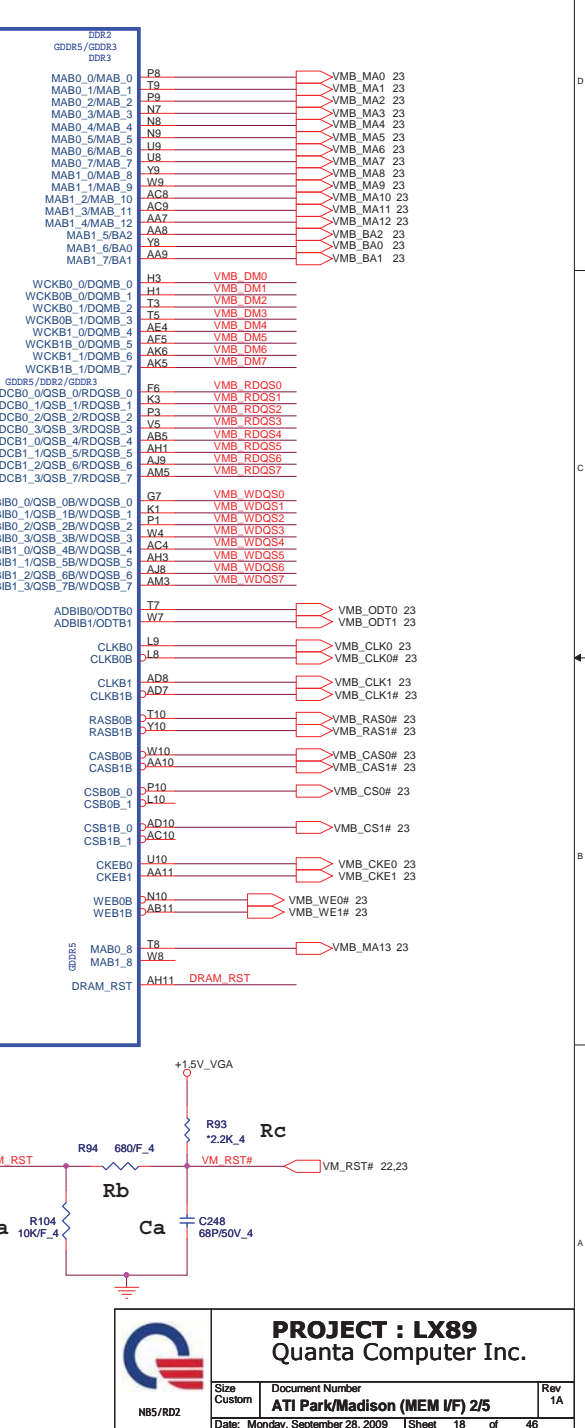
	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
R1	40.2R	40.2R	40.2R
R2	100R	100R	100R



Designator	For M97-M2	For Manhattan
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF

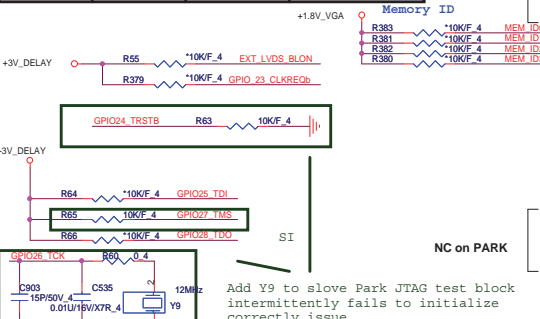


PROJECT : LX89
Quanta Computer Inc.

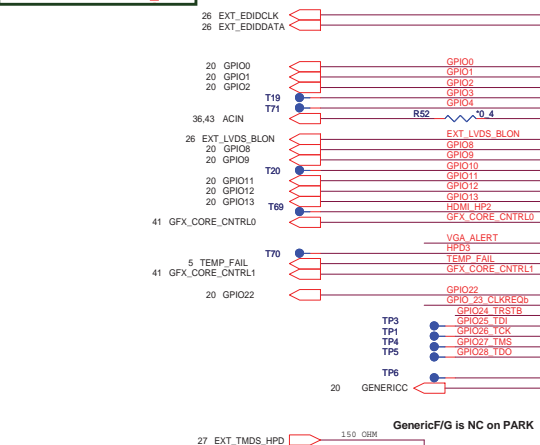
Size Custom Document Number **ATI Park/Madison (MEM VF) 2/5** Rev 1A
 Date: Monday, September 28, 2009 Sheet 16 of 46

MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0010		Reserved	
0011		Reserved	
0100		Reserved	
0101		Reserved	
0110		Reserved	
0111		Reserved	
1000		Reserved	
1001		Reserved	
1010		Reserved	
1011		Reserved	
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	

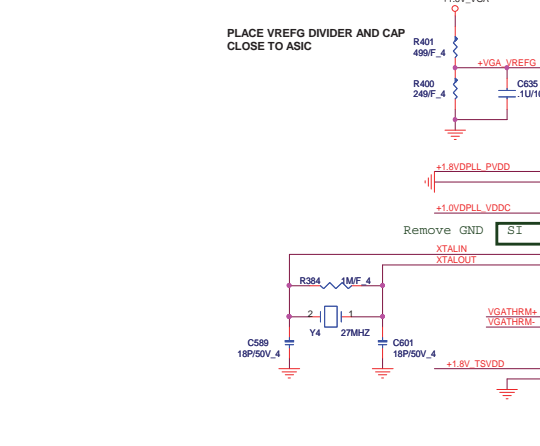
NC on PARK



NC on PARK



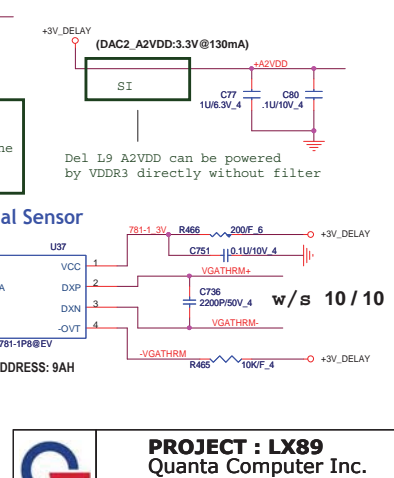
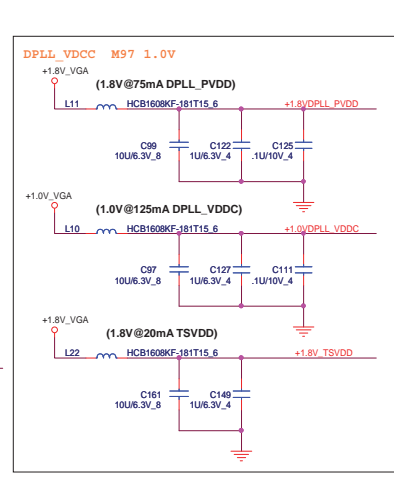
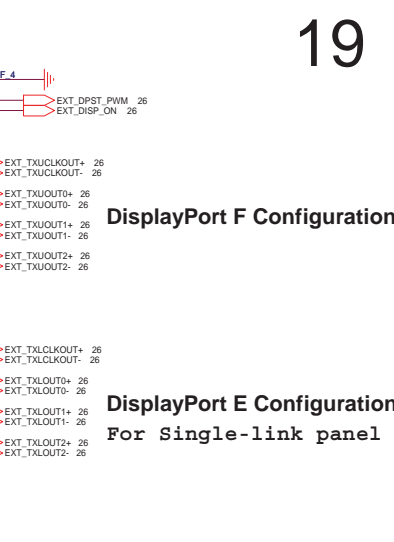
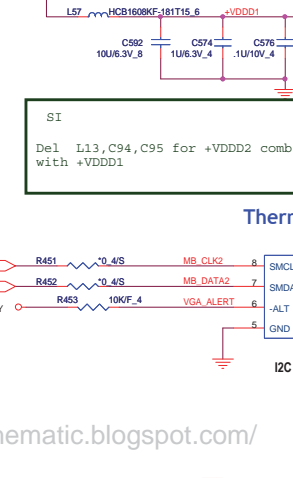
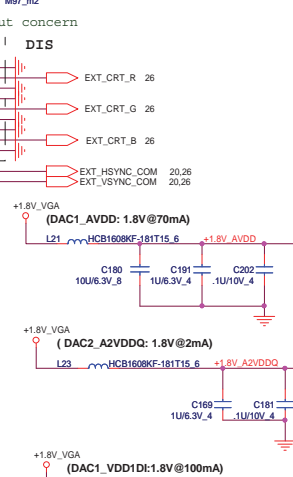
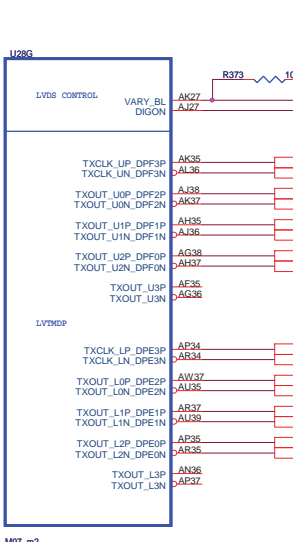
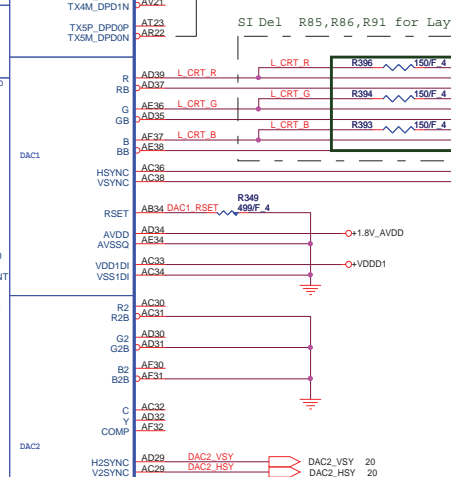
Generic/F/G is NC on PARK



MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0010		Reserved	
0011		Reserved	
0100		Reserved	
0101		Reserved	
0110		Reserved	
0111		Reserved	
1000		Reserved	
1001		Reserved	
1010		Reserved	
1011		Reserved	
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	

MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0010		Reserved	
0011		Reserved	
0100		Reserved	
0101		Reserved	
0110		Reserved	
0111		Reserved	
1000		Reserved	
1001		Reserved	
1010		Reserved	
1011		Reserved	
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	

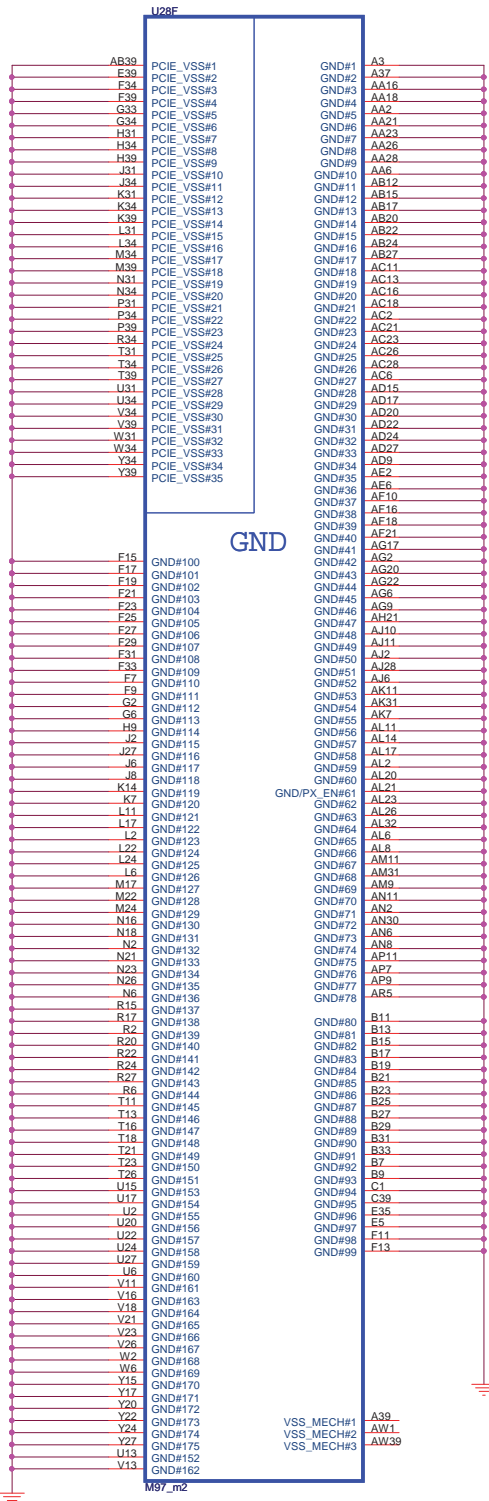
MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0010		Reserved	
0011		Reserved	
0100		Reserved	
0101		Reserved	
0110		Reserved	
0111		Reserved	
1000		Reserved	
1001		Reserved	
1010		Reserved	
1011		Reserved	
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	



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Quanta Computer Inc.

Size: Custom
 Document Number: AT1 Park/Madison (DISPLAY) 3/5
 Date: Monday, September 28, 2009
 Sheet: 19 of 46

http://www.park-madison.com/schematic-blogspot.com/



Memory Aperture size fix 256M

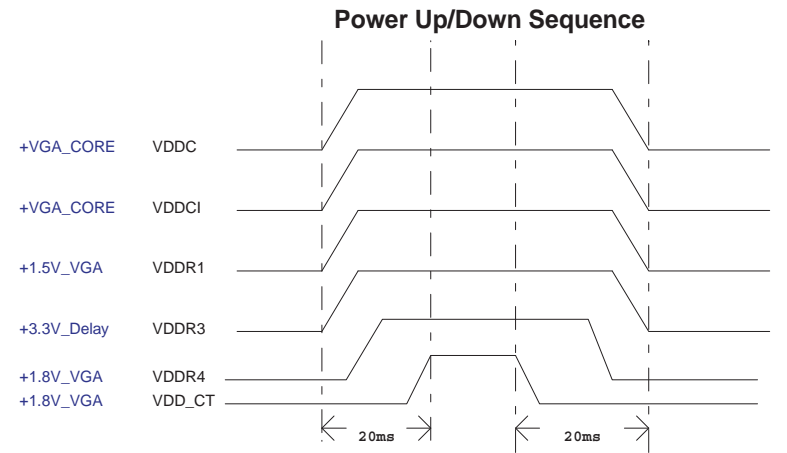
GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	1	0
0	32M	0	1
0	512M	1	0
0	1G	0	1
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

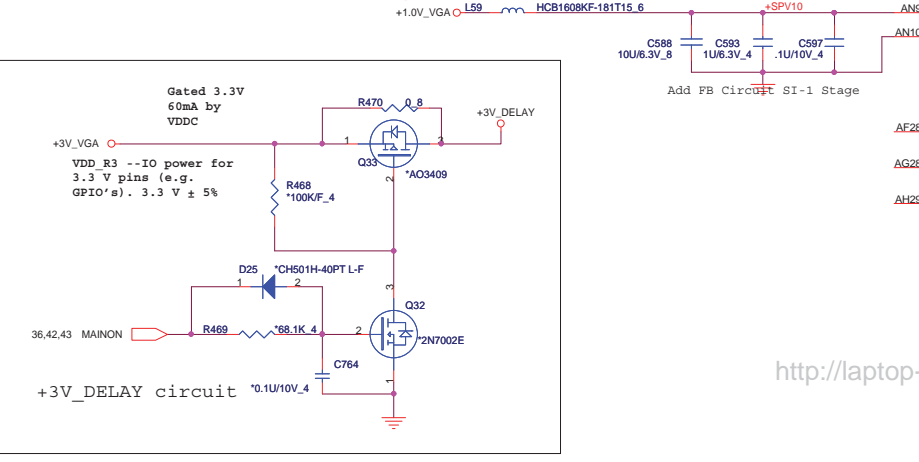
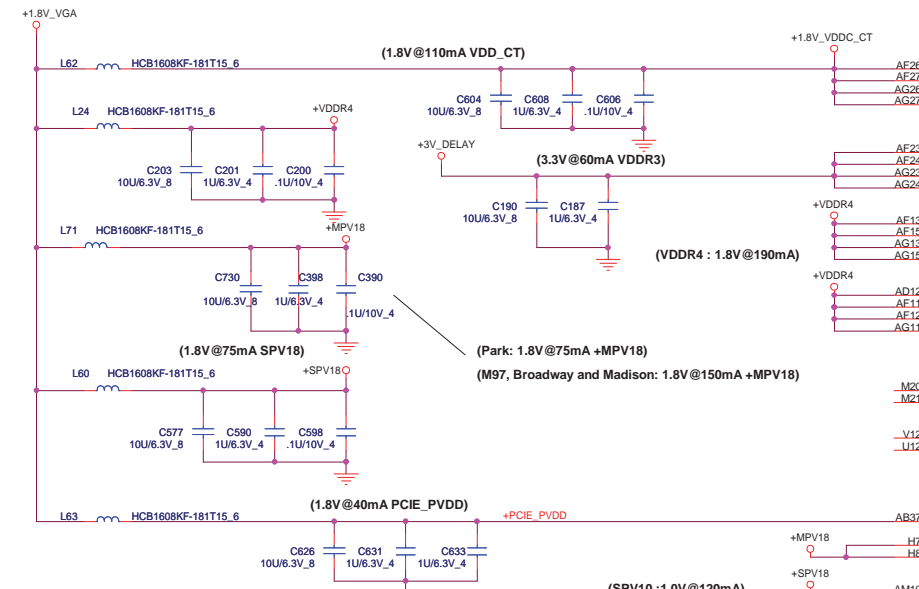
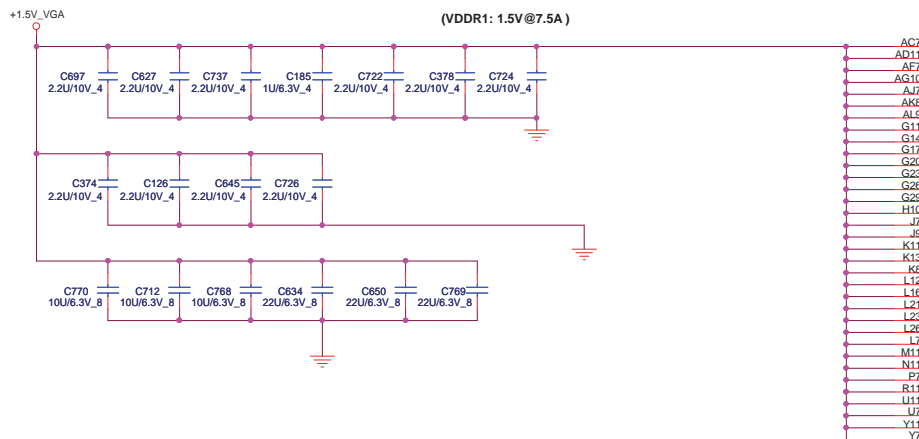
<http://laptop-motherboard-schematic.blogspot.com/>

CONFIGURATION STRAPS			RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 - Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 - Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO{13:11}	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERIC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERIC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

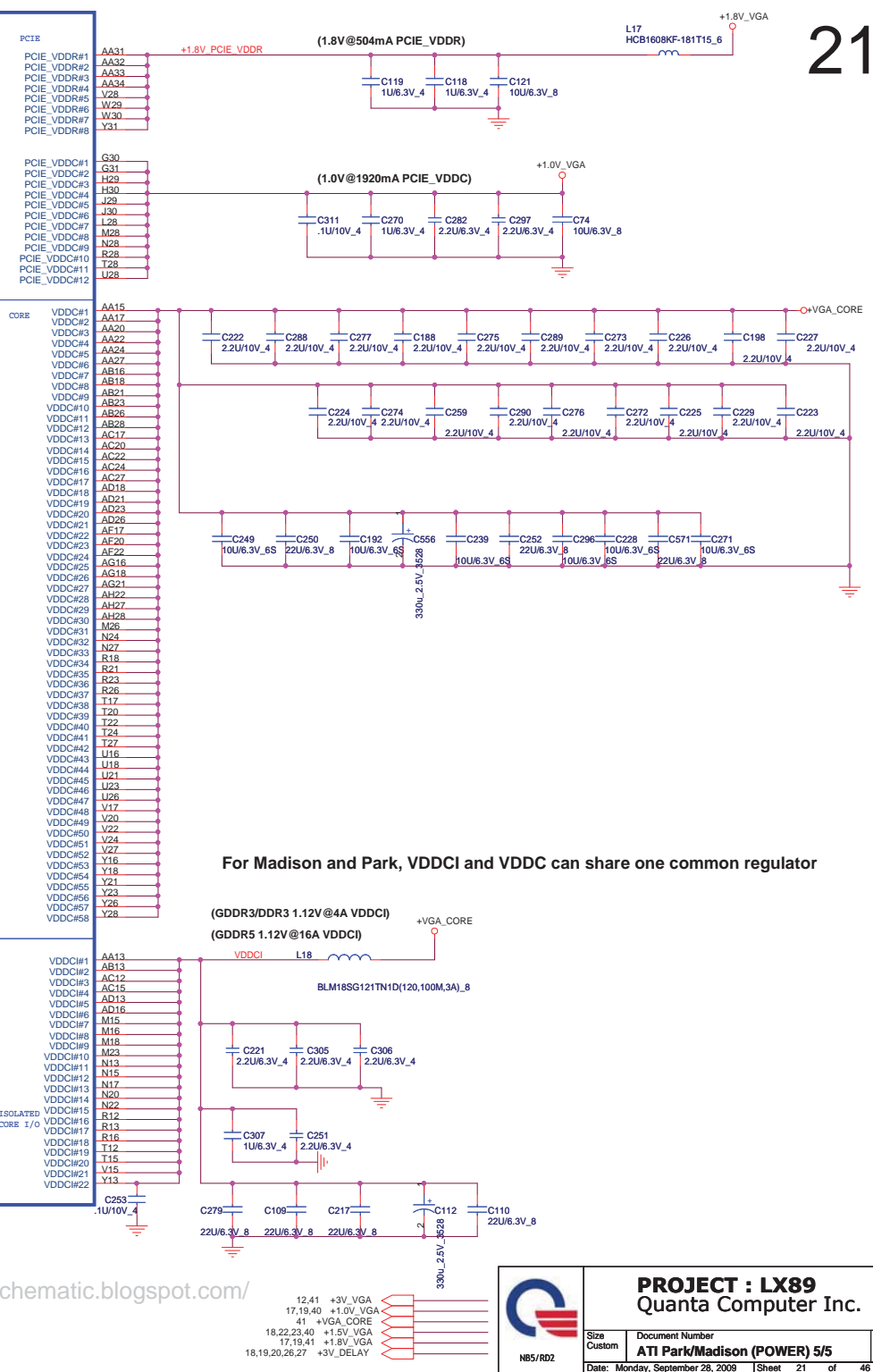


	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Date: Monday, September 28, 2009	Document Number ATI Park/Madison(GND&Str&Ther)4/5



MEM I/O	
AC7	VDDR1#1
AD11	VDDR1#2
AF7	VDDR1#3
AG10	VDDR1#4
AJ7	VDDR1#5
AK8	VDDR1#6
AL9	VDDR1#7
G11	VDDR1#8
G14	VDDR1#9
G17	VDDR1#10
G20	VDDR1#11
G23	VDDR1#12
G26	VDDR1#13
G29	VDDR1#14
H10	VDDR1#15
J7	VDDR1#16
J9	VDDR1#17
K11	VDDR1#18
K13	VDDR1#19
K8	VDDR1#20
L12	VDDR1#21
L16	VDDR1#22
L21	VDDR1#23
L23	VDDR1#24
L26	VDDR1#25
L7	VDDR1#26
M11	VDDR1#27
N11	VDDR1#28
P7	VDDR1#29
R11	VDDR1#30
U11	VDDR1#31
U7	VDDR1#32
Y11	VDDR1#33
Y7	VDDR1#34
LEVEL TRANSLATION	
AF26	VDD_CT#1
AF27	VDD_CT#2
AG26	VDD_CT#3
AG27	VDD_CT#4
I/O	
AF23	VDDR3#1
AF24	VDDR3#2
AG23	VDDR3#3
AG24	VDDR3#4
+VDDR4	
AE13	VDDR4#4
AE15	VDDR4#5
AG13	VDDR4#7
AG15	VDDR4#8
+VDDR4	
AD12	VDDR4#1
AE11	VDDR4#2
AE12	VDDR4#3
AG11	VDDR4#6
-M20	NC_VDDRHA
-M21	NC_VSSRHA
-Y12	NC_VDDRHB
-U12	NC_VSSRHB
PLL	
AB37	PCIE_PVDD
MPV18	
H7	MPV18#1
H8	MPV18#2
SPV18	
AM10	SPV18
AN9	SPV10
AN10	SPVSS
VOLTAGE SENSE	
AF28	FB_VDDC
AG28	FB_VDDCI
AH29	FB_GND
M97_m2	

POWER



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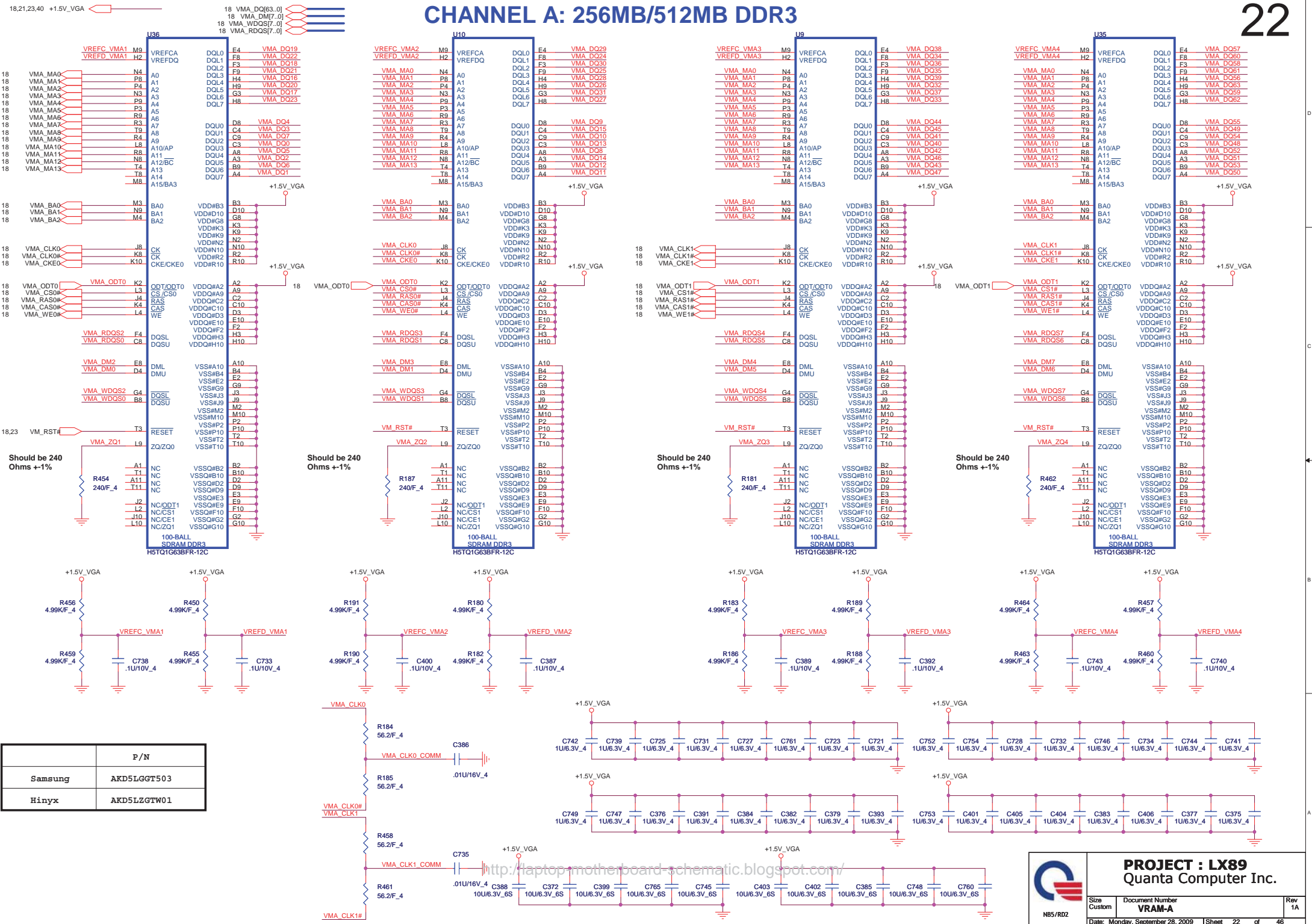
PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number **ATI Park/Madison (POWER) 5/5** Rev 1A

Date: Monday, September 28, 2008 Sheet 21 of 46



CHANNEL A: 256MB/512MB DDR3



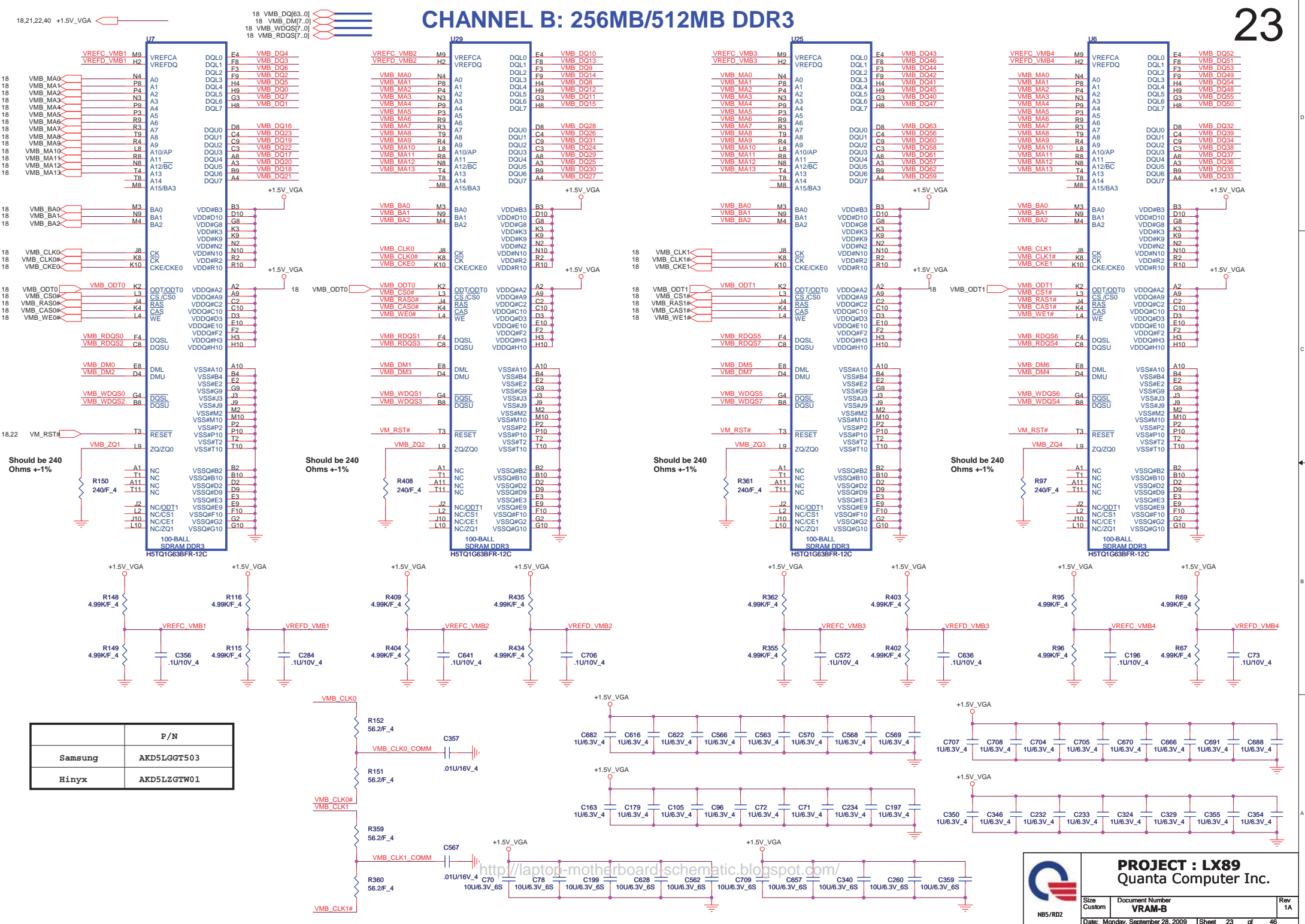
	P/N
Samsung	AKD5LGGT503
Hynix	AKD5LZGTW01


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PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number VRAM-A	Rev 1A
Date: Monday, September 28, 2009		
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CHANNEL B: 256MB/512MB DDR3



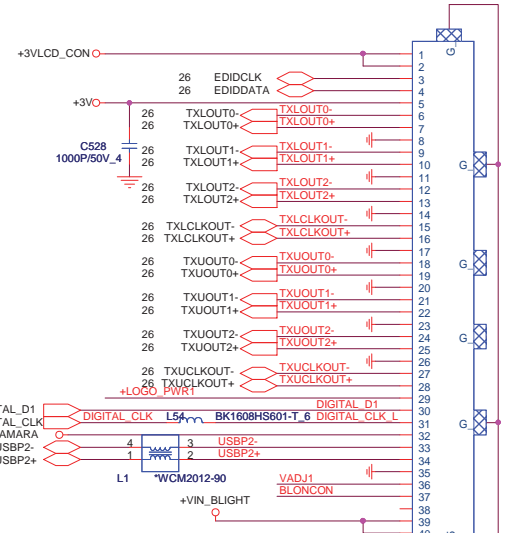
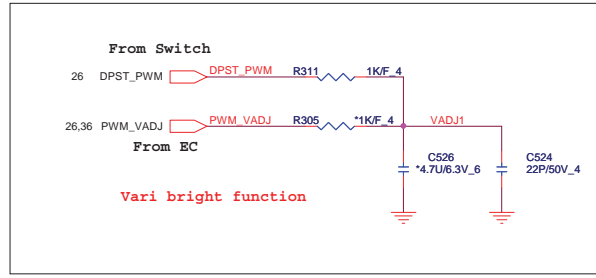
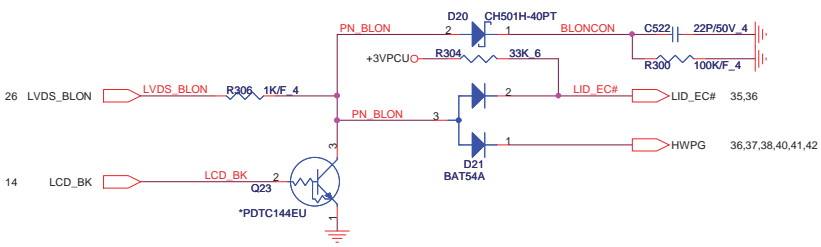
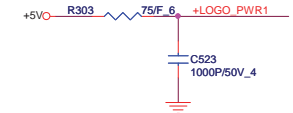
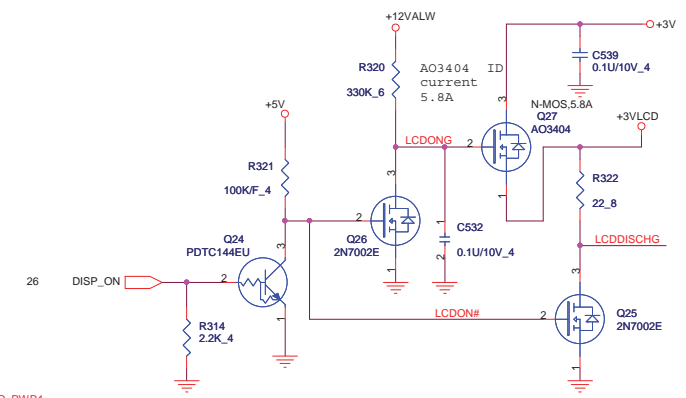
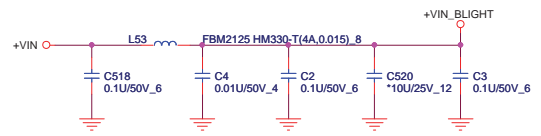


PROJECT : LX89
Quanta Computer Inc.

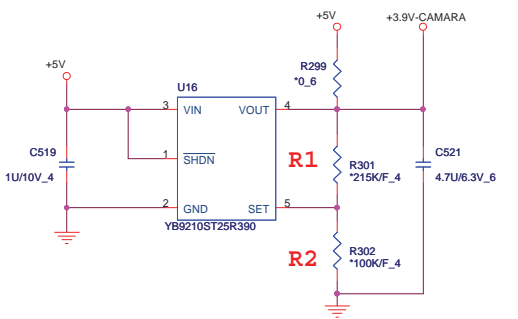
Size Custom	Document Number VRAM-B	Rev 1A
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<http://laptop-motherboard-schematic.blogspot.com/>

+VIN	31,37,38,39,40,41,42,43
+12VALW	33,35,40,41,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY	18,19,20,21,26,27
+5V	25,26,27,28,29,33,34,35,42

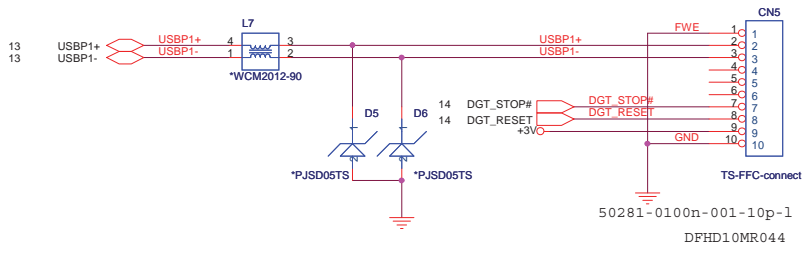


CAMERA POWER



$V_{out} = 1.25 (1 + R1/R2)$

Digitizer Connector



$V_{out} = 1.25 (1 + R1/R2)$

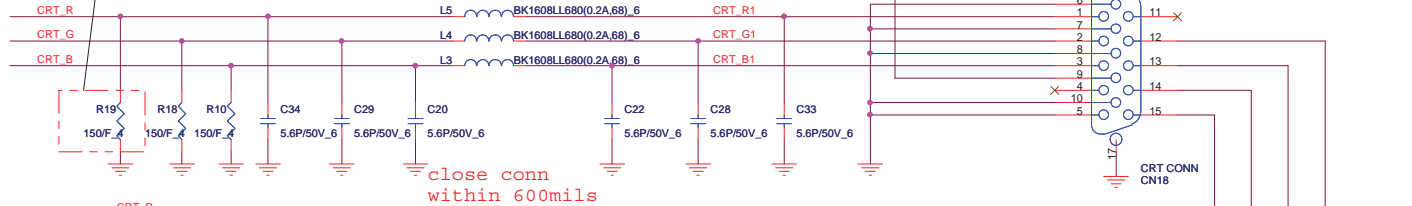
<http://laptop-motherboard-schematic.blogspot.com/>

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number		
LCD CONN			
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CRT PORT

+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,42
 +5V 24,26,27,28,29,33,34,35,42
 +3V_DELAY 18,19,20,21,26,27

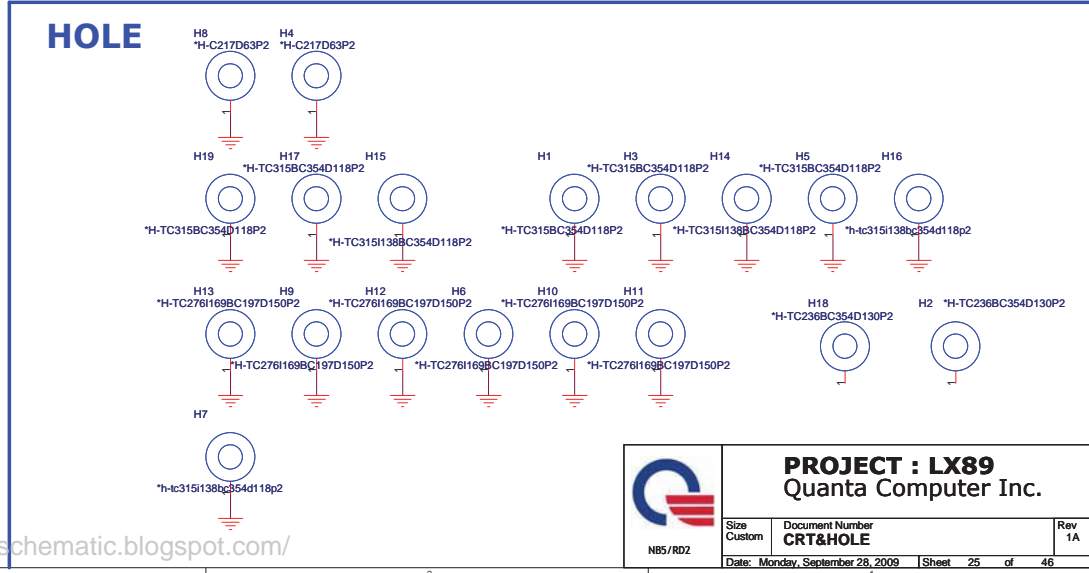
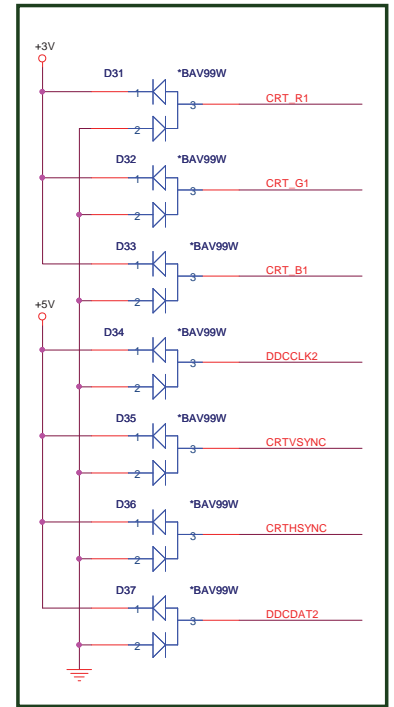
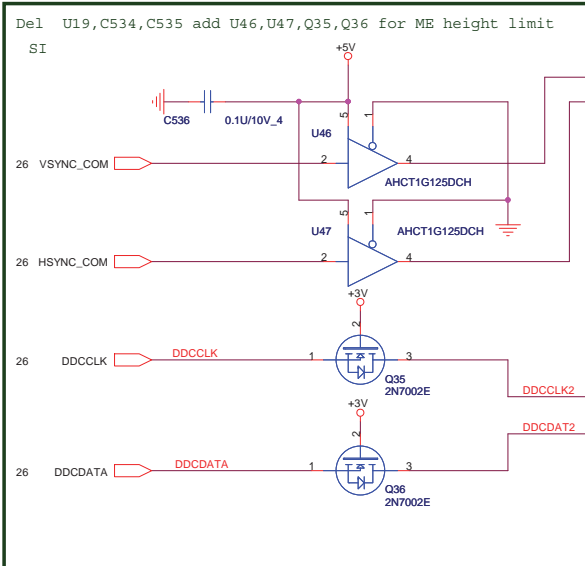
R19 for UMA use 140 ohm
 for DIS+PowerExpress use 150 ohm (AMD)



26 CRT_R
 26 CRT_G
 26 CRT_B

close conn
 within 600mils

SI Add D31-D37 for ME height limit

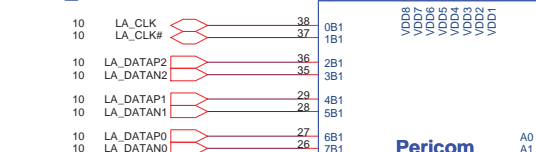


<http://laptop-motherboard-schematic.blogspot.com/>

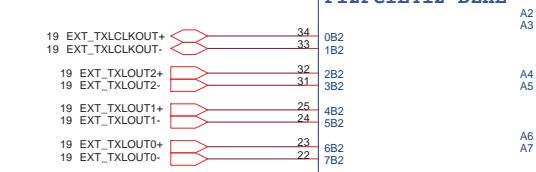
PROJECT : LX89 Quanta Computer Inc.		
Size Custom	Document Number CRT&HOLE	Rev 1A
Date: Monday, September 28, 2009 Sheet 25 of 46		

For Single-link panel

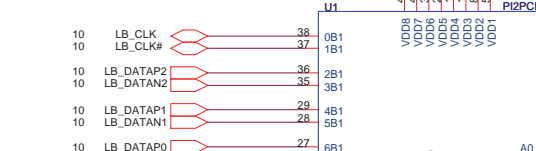
IGPU_Channel-A



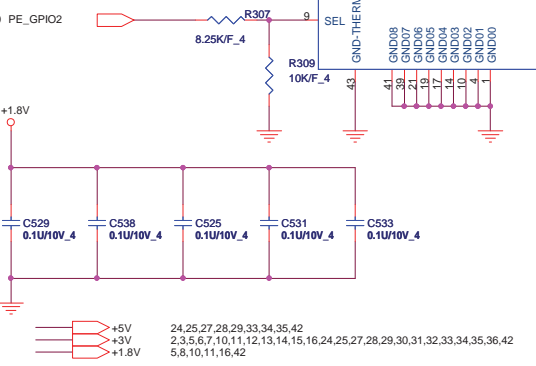
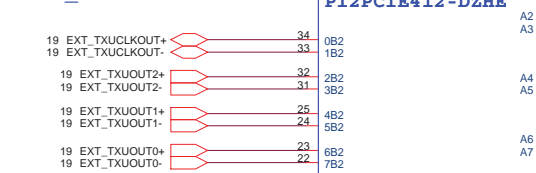
DGPU_Channel-A



IGPU_Channel-B

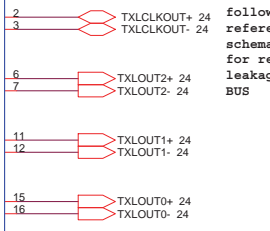


DGPU_Channel-B



LVDS Channel Switch

SELx	Ay
HIGH	B2
LOW	B1

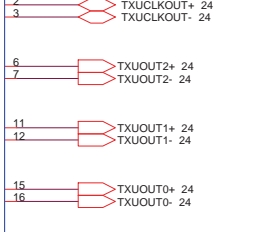


SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

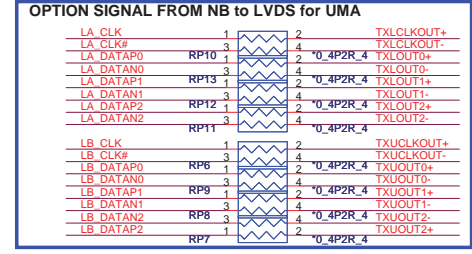


LVDS Channel Switch

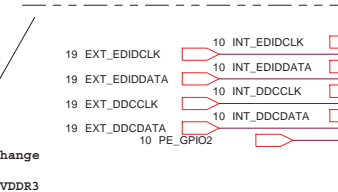
SELx	Ay
HIGH	B2
LOW	B1



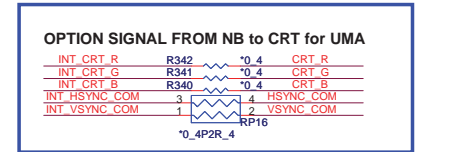
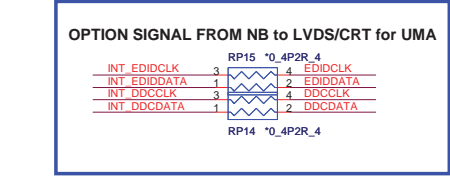
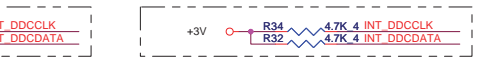
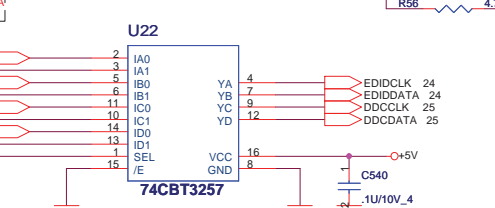
SEL	FUNCTION
HIGH	DGPU
LOW	IGPU



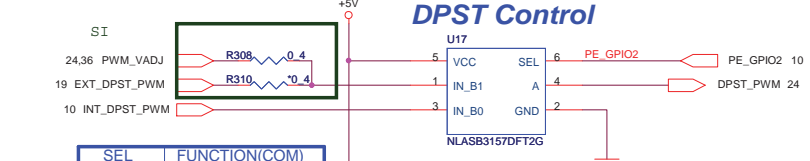
LVDS/CRT DDC Switch



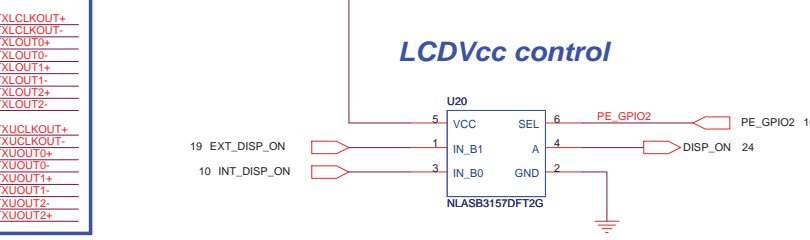
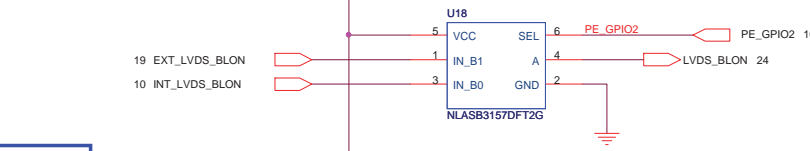
VGA Switch



DIS Change Vari bright function from EC control



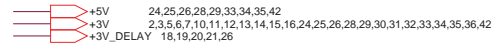
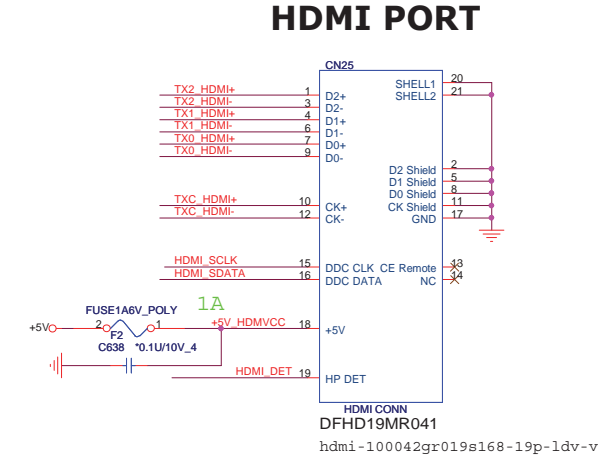
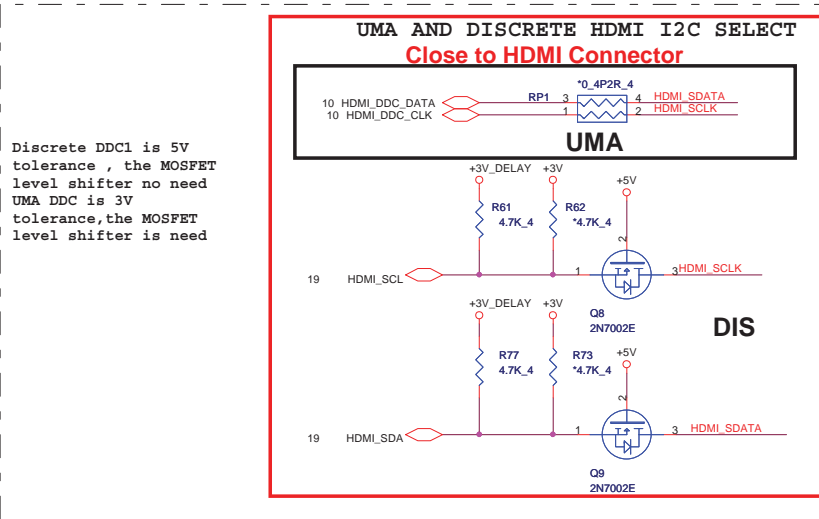
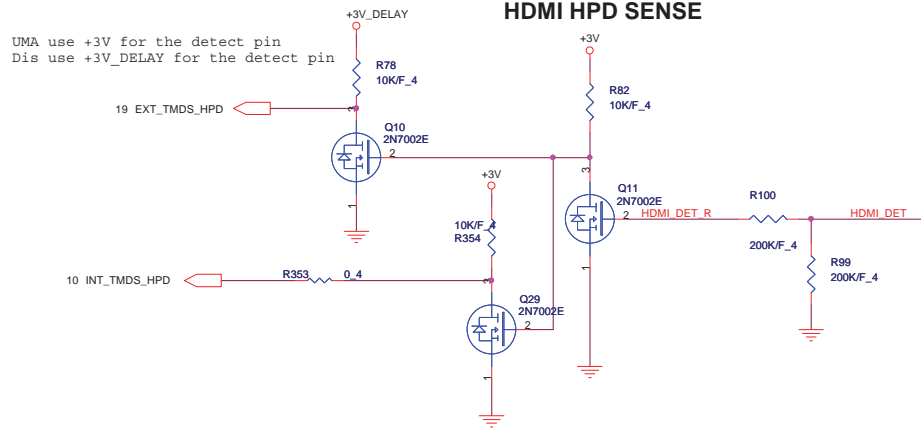
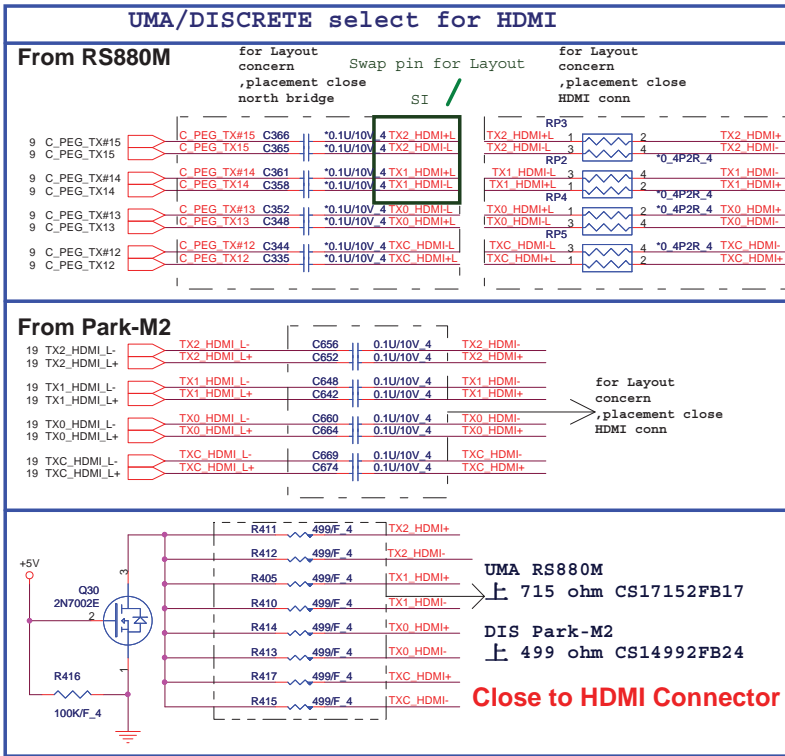
SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A



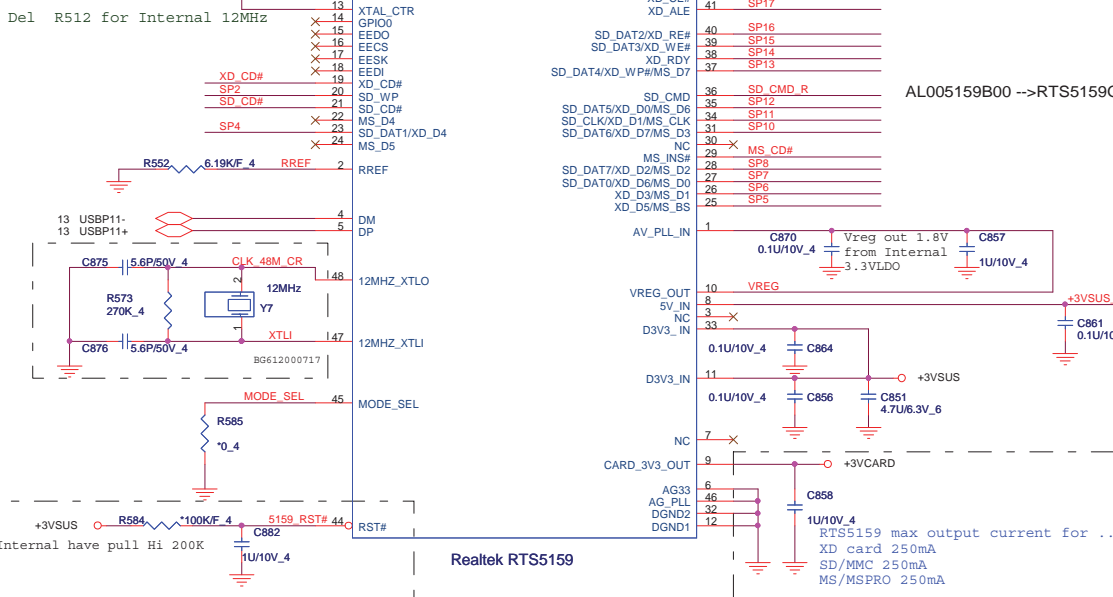
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PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number LVDS/CRT Hyper_switch	Rev 1A
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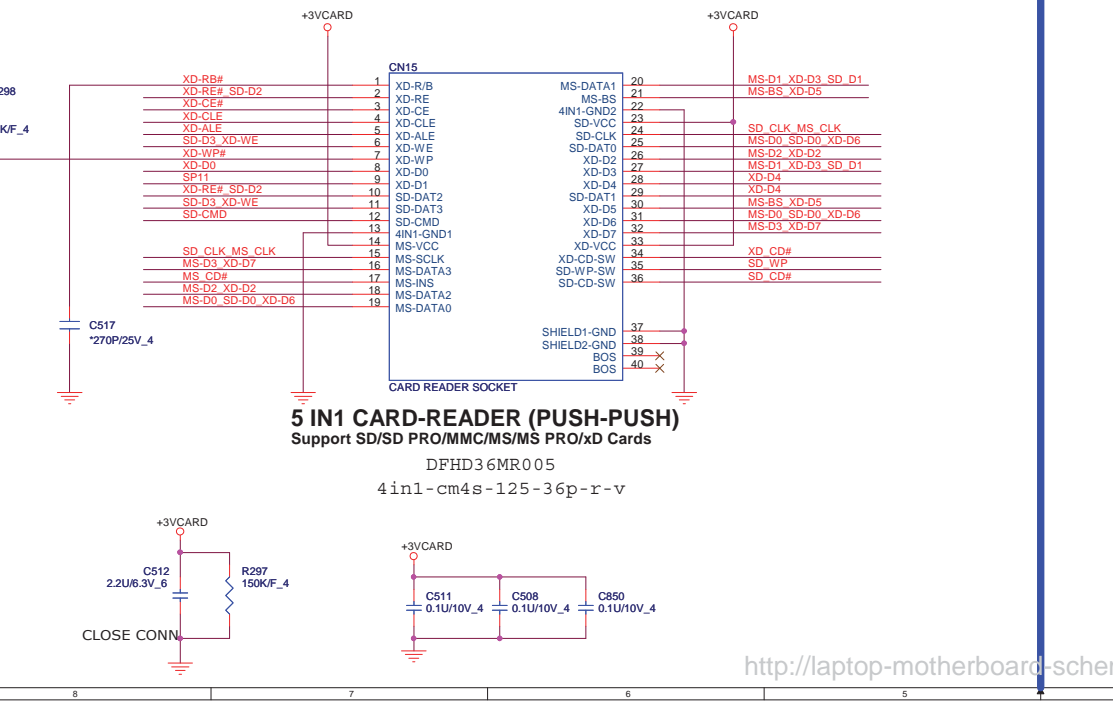
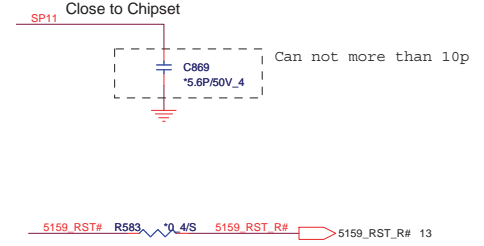
XTAL control pin for 12Mhz crystal or 48Mhz clk in



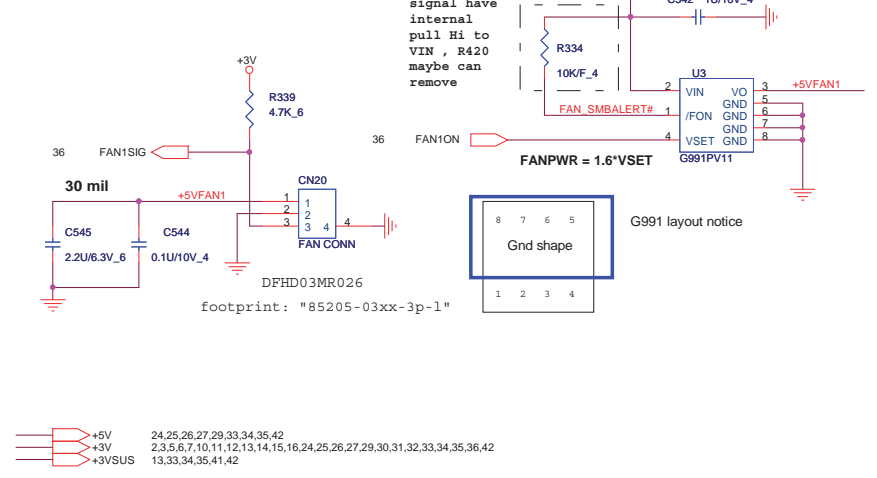
Note:

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5	MS_BS	XD D5
SP6	MS_D1	XD D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9	MS_INSB	
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD D0
SP13	SD_DAT4	XD WP#
SP14		XD RB#
SP15	SD_DAT3	XD WB#
SP16	SD_DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

SP7	R528	0.4	MS-D0	SD-D0	XD-D6
SP6	R524	0.4	MS-D1	XD-D3	SD-D1
SP8	R531	0.4	MS-D2	XD-D2	
SP16	R579	0.4	XD-RE#	SD-D2	
SP5	R522	0.4	MS-BS	XD-D5	
SP15	R578	0.4	SD-D3	XD-WE	
SP11	R569	0.4	SD-CLK	MS-CLK	
SP2	R511	0.4	SD_WP		
SP13	R576	0.4	XD-WP#		
SP19	R582	0.4	XD-CLE		
SP4	R510	0.4	XD-D4		
SP10	R537	0.4	MS-D3	XD-D7	
SP14	R577	0.4	XD-RB#		
SP12	R570	0.4	XD-D0		
SP17	R590	0.4	XD-ALE		
SP18	R581	0.4	XD-CE#		
SD_CMD R	R571	0.4	SD-CMD		



CPU FAN

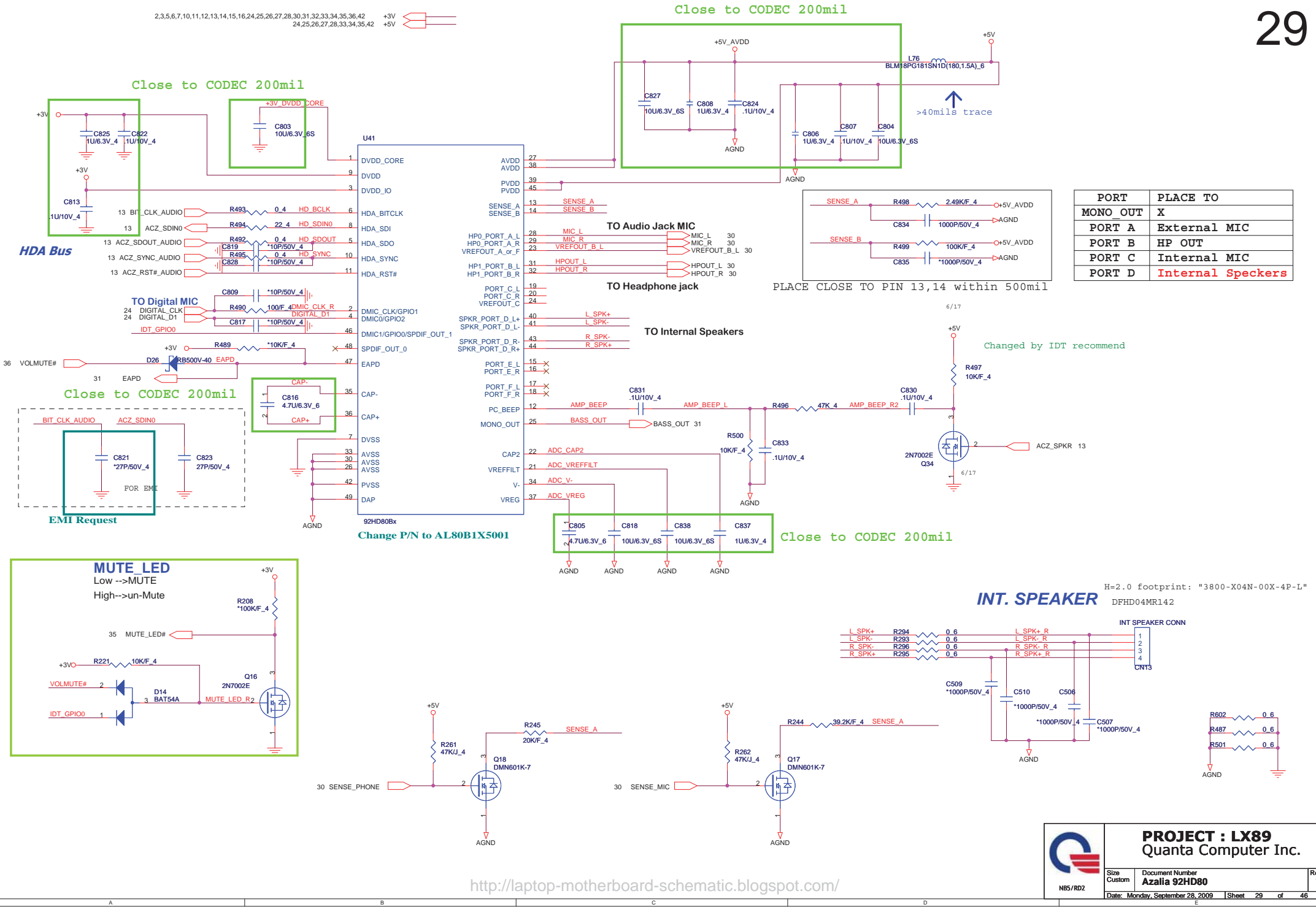


- +5V 24,25,26,27,29,33,34,35,42
- +3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,29,30,31,32,33,34,35,36,42
- +3VSUS 13,33,34,35,41,42

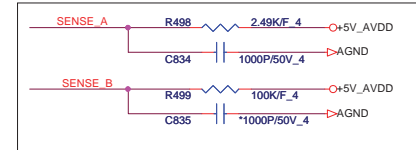
<http://laptop-motherboard-schematic.blogspot.com/>

PROJECT : LX89
Quanta Computer Inc.

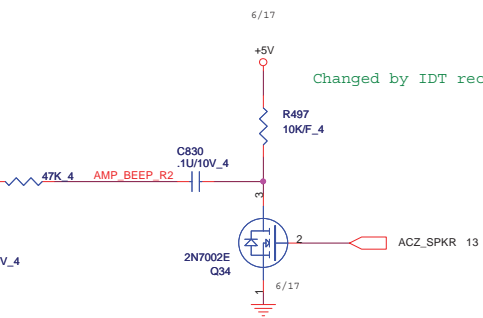
Size Custom	Document Number	Rev 1A
NB5/RD2	RTS5159&CPU FAN	
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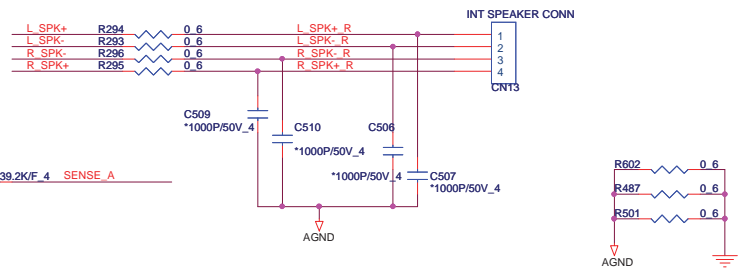
PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speakers



PLACE CLOSE TO PIN 13,14 within 500mil



H=2.0 footprint: "3800-X04N-00X-4P-L"
DFHD04MR142

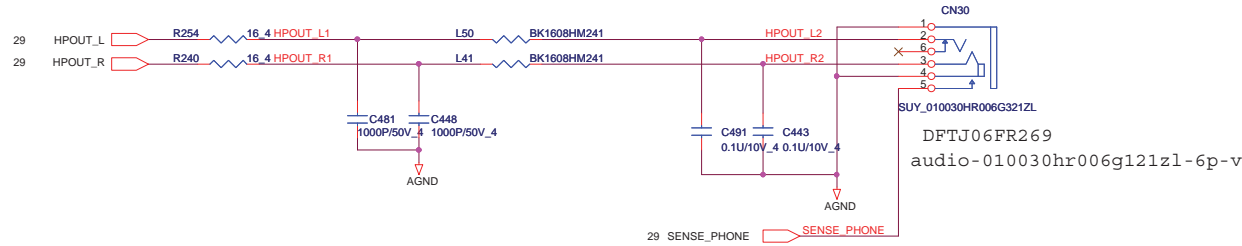


	PROJECT : LX89	
	Quanta Computer Inc.	
Size Custom	Document Number Azalia 92HD80	Rev 1A
NB5/RD2	Date: Monday, September 28, 2009	Sheet 29 of 46

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

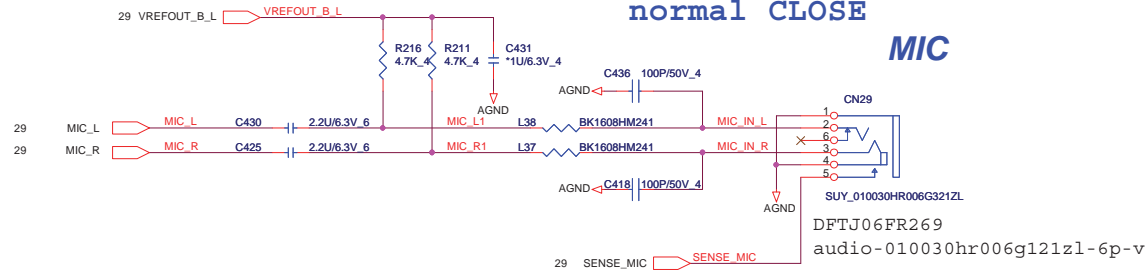
33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

normal CLOSE Line out



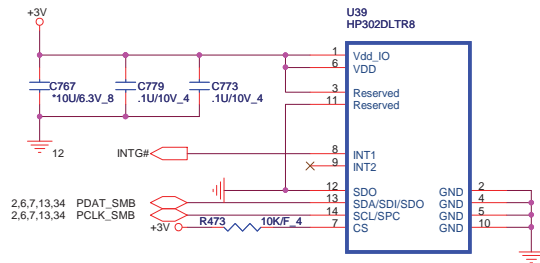
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

normal CLOSE MIC

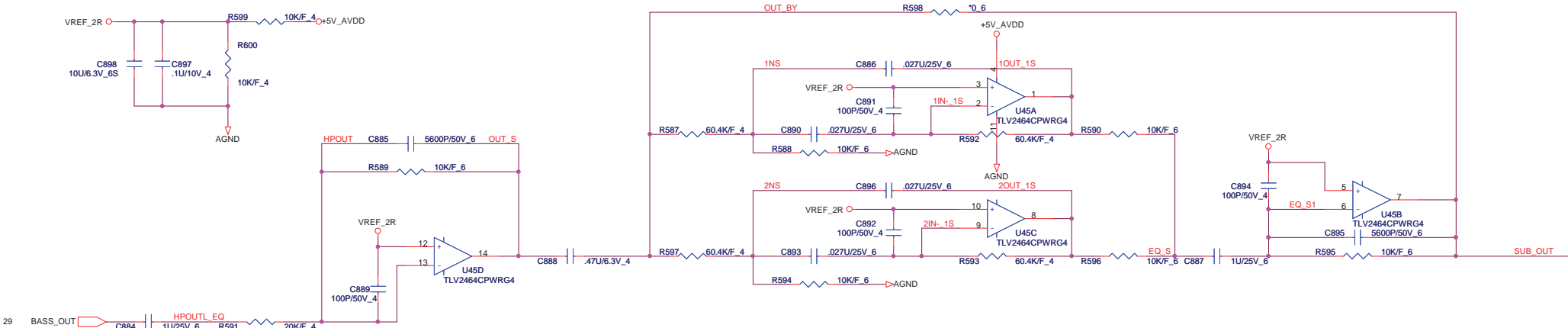


Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low

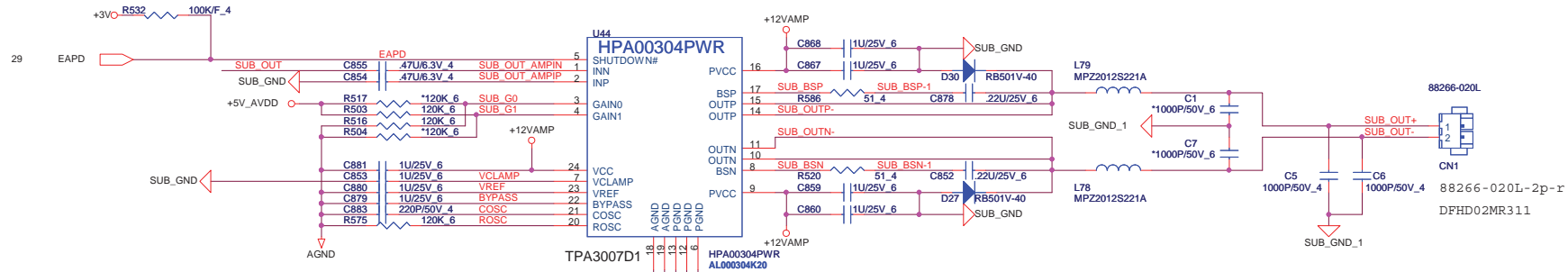


EQ FOR SUBWOOFER



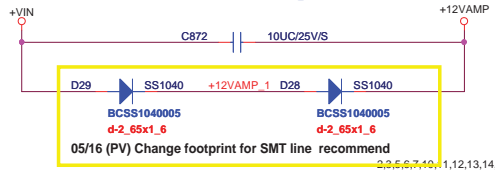
MODEL	UP7
R9402	60.4K/F_6
R9403	60.4K/F_6
R9407	60.4K/F_6
R9408	60.4K/F_6
C5144	0.027U/25V_6
C5146	0.027U/25V_6
C5148	0.027U/25V_6
C5153	0.027U/25V_6

5/27: NA for subwofer function



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

Sub-Woofer power



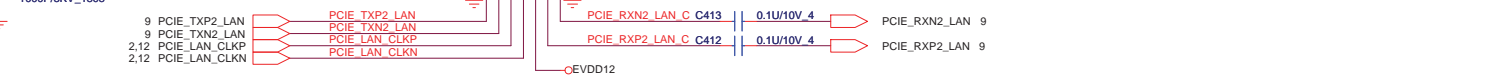
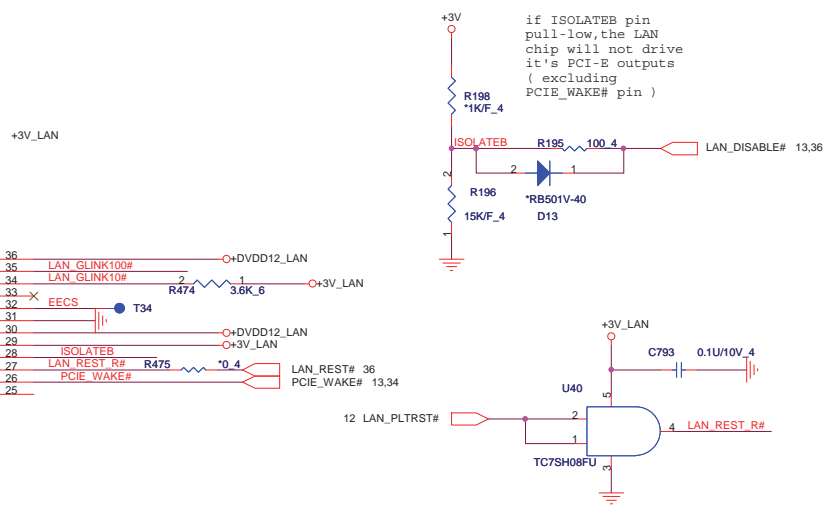
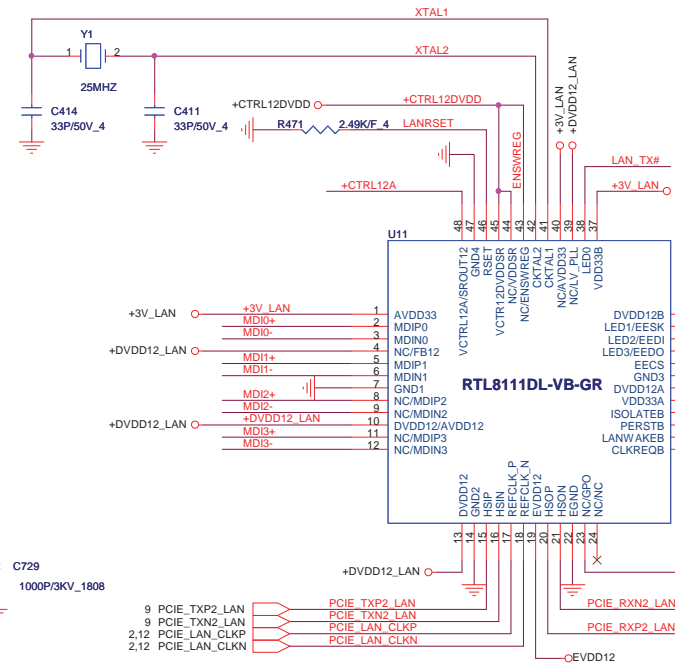
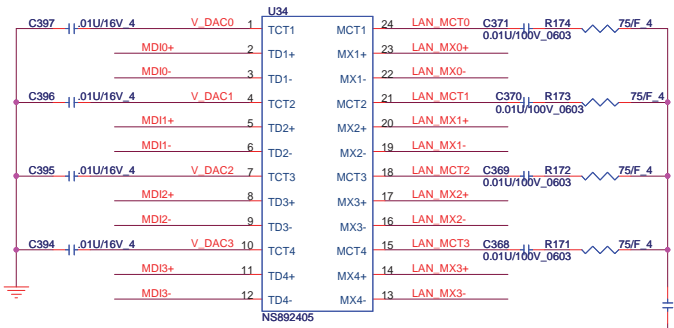
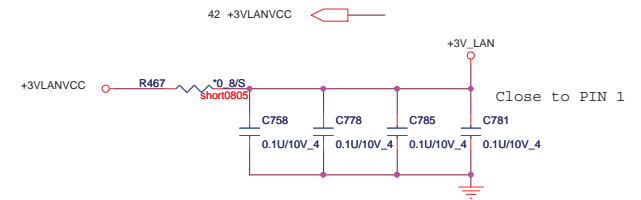
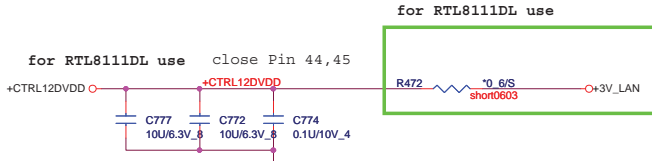
- +3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42
- +5V_AVDD 29
- +VIN 24,37,38,39,40,41,42,43

<http://laptop-motherboard-schematic.blogspot.com/>

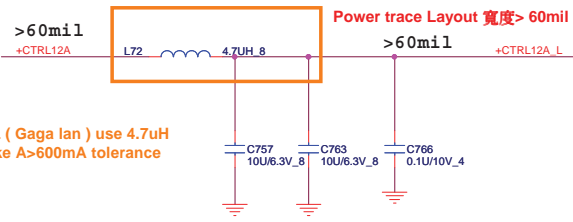
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SUBWOOFER (EQ & AMP.)	Rev 1A
Date: Monday, September 28, 2009 Sheet 31 of 46		

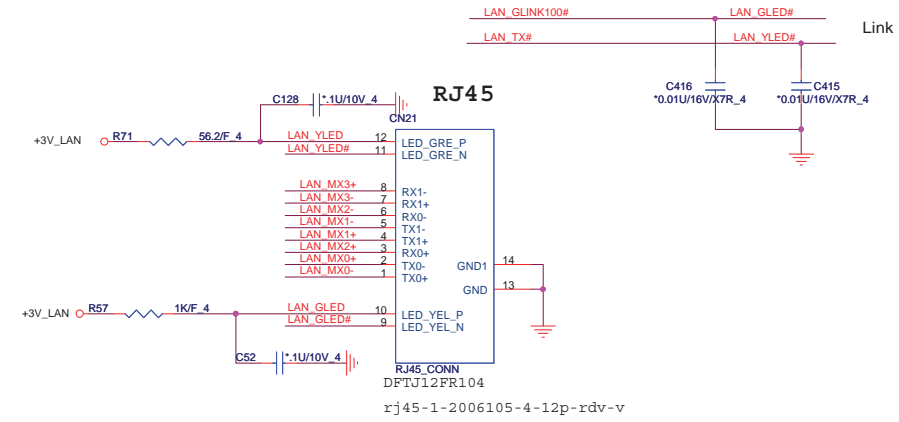
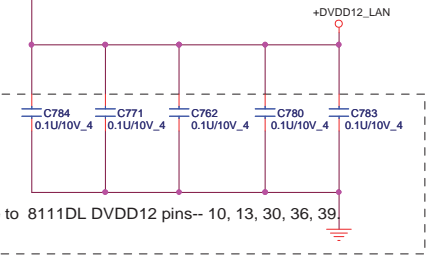
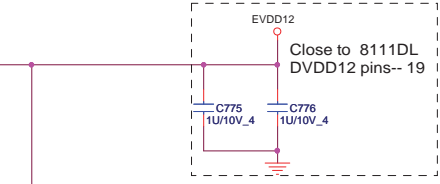
T : Stuffed for RTL8111DL(10/100/1000)



NS892402:GIGABIT DB0AT9LAN05

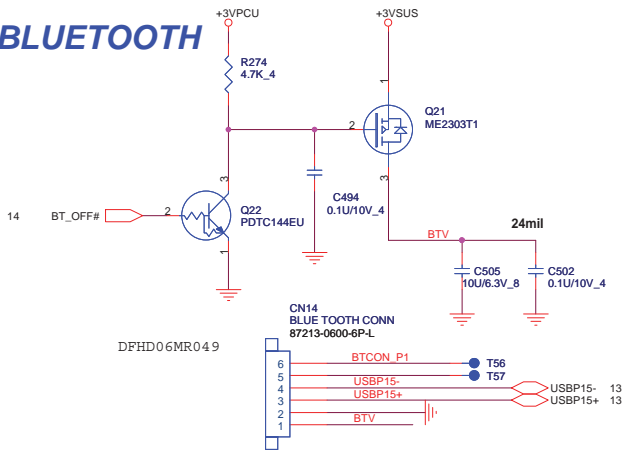


L149
RTL8111DL (Gaga lan) use 4.7uH
power choke A>600mA tolerance
±15%

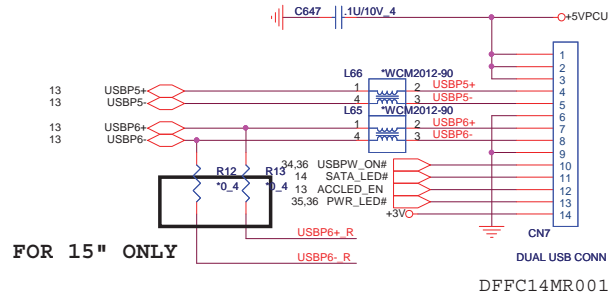


			PROJECT : LX89 Quanta Computer Inc.	
Size	Document Number	Rev		
Custom	RTL8111DL/RJ45	1A		
Date: Monday, September 28, 2009	Sheet 32	of 46		

BLUETOOTH

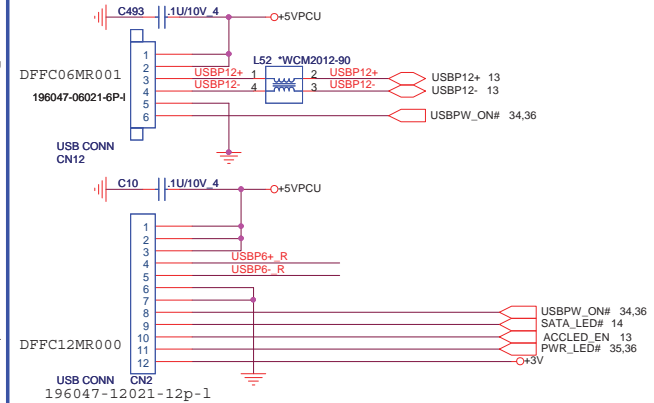


RIGHT SIDE USBX2 for 17"



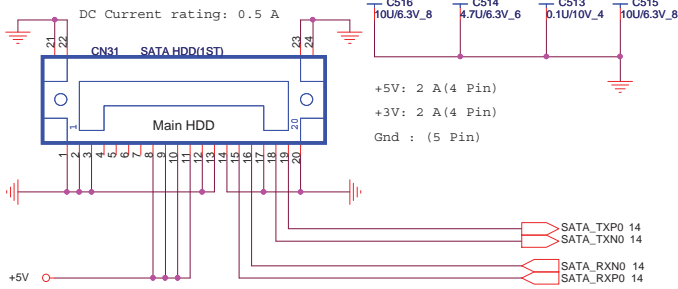
FOR 15" ONLY

RIGHT SIDE USBX2 for 15"



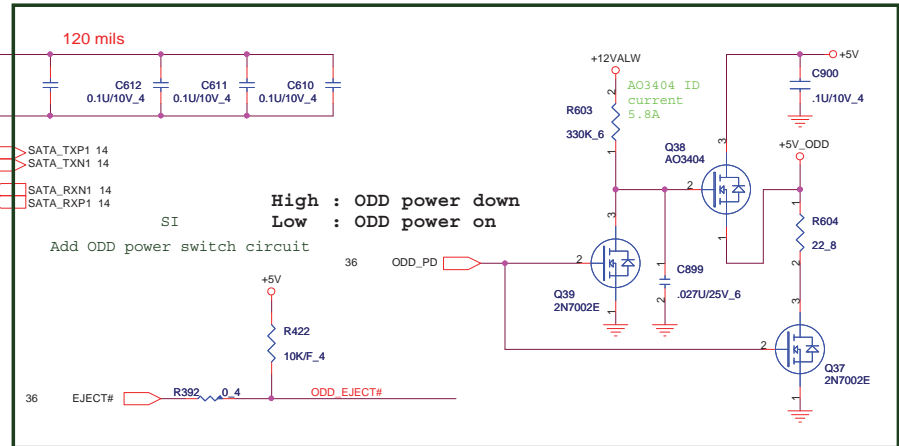
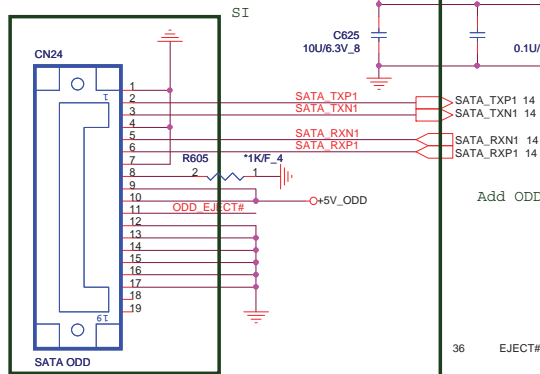
SATA HDD CONNECTOR

H=2.6 Footprint: "GS12201-1011-9F-20P-L"
DFHD20MR023



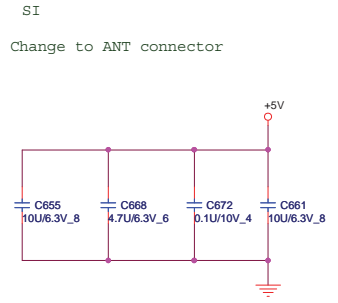
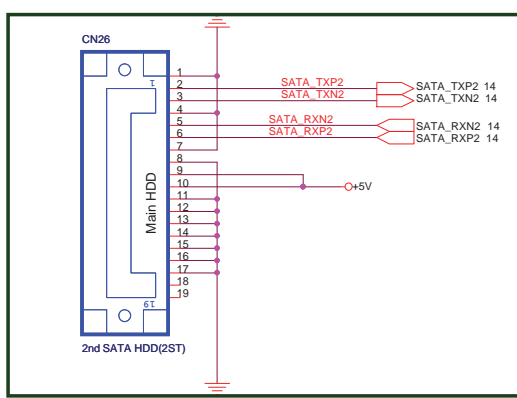
SATA CD-ROM

Change to ANT connector



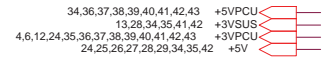
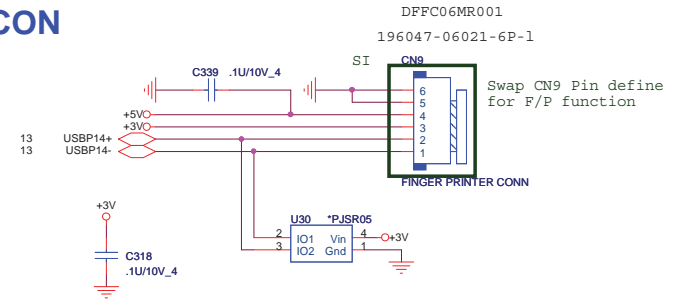
SATA_2 HDD CONNECTOR FOR 17.3"

+5V: 2 A(4 Pin)
Gnd : (5 Pin)



USB Fingerprint CON

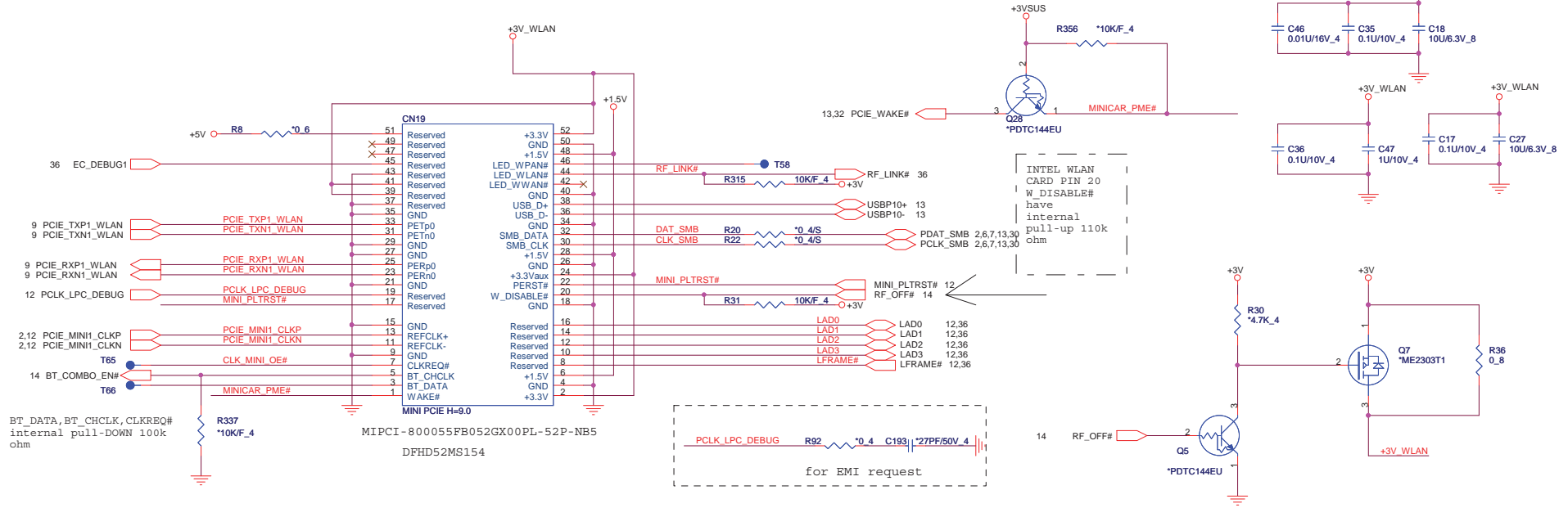
1. SYSTEM GND
2. SYSTEM GND
3. LED PWR(+5V)
4. USB PWR(+3V)
5. USB1.1+
6. USB1.1-



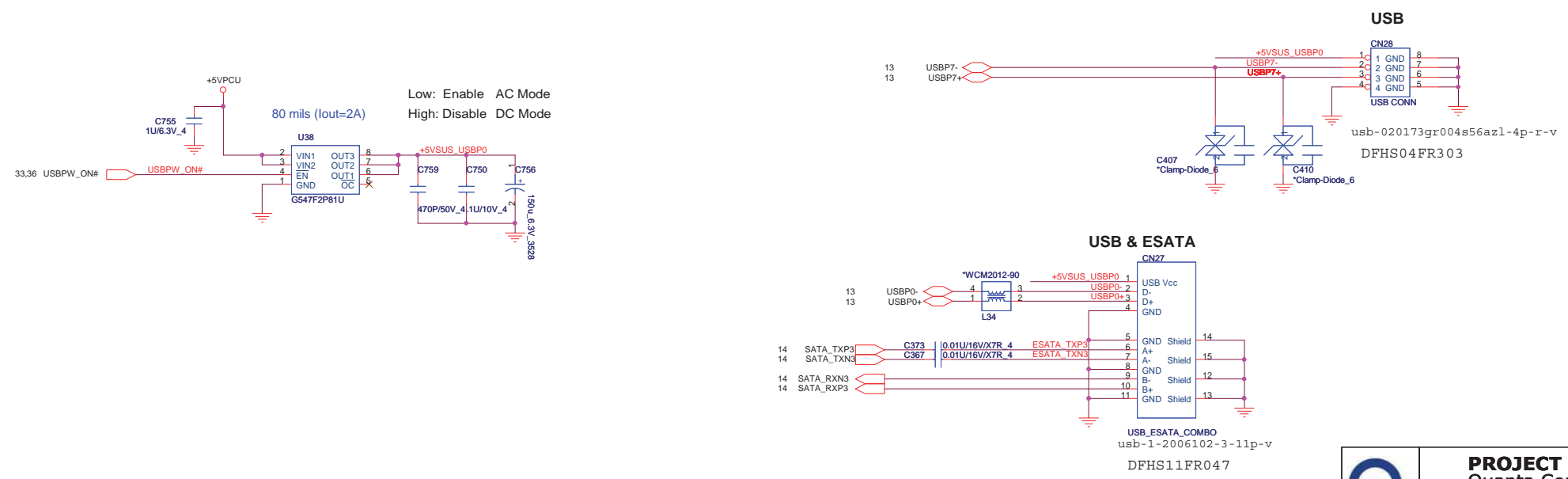
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number BT/FP/USBX2/SATA HDDX2/ODD	Rev 1A
Date: Monday, September 28, 2009	Sheet 33 of 46	

Mini PCI-E Card WLAN

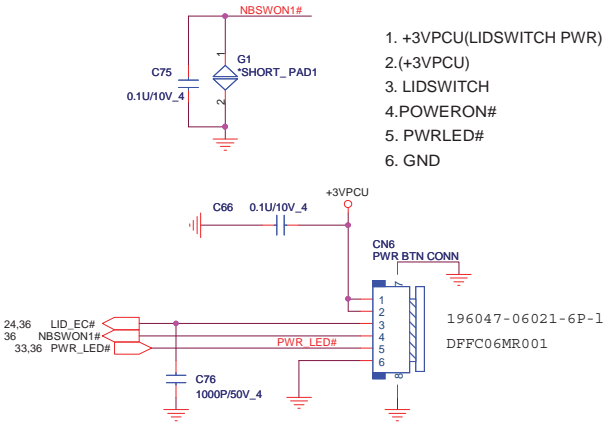


USB2.0 X 1 and E-SATA/USB2.0 COMBO

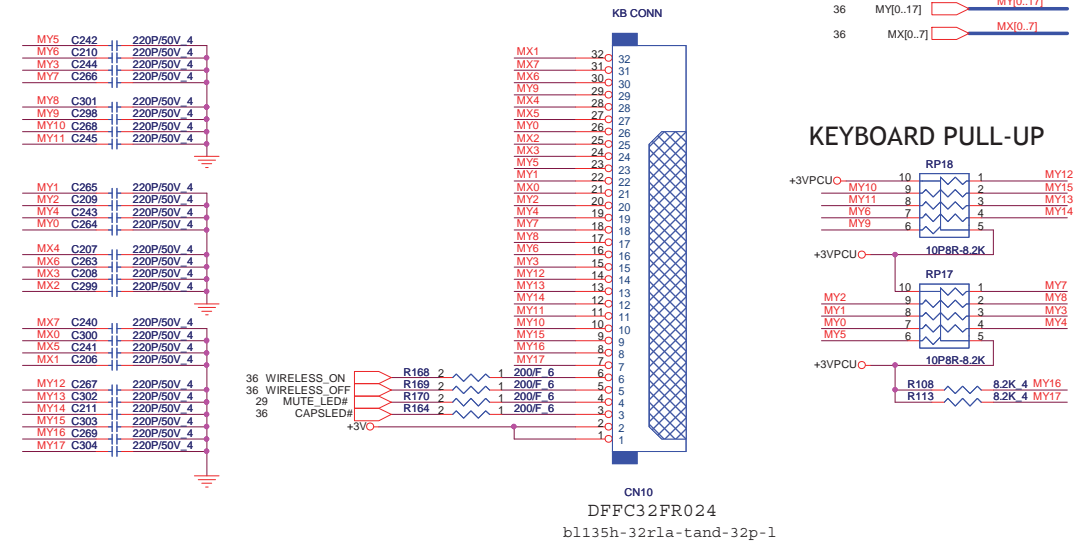


			PROJECT : LX89 Quanta Computer Inc.	
Date: Monday, September 28, 2009			Sheet 34	of 46

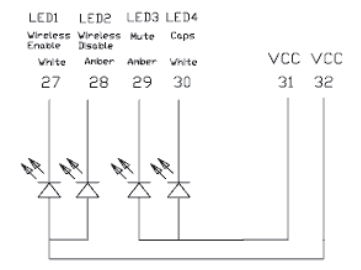
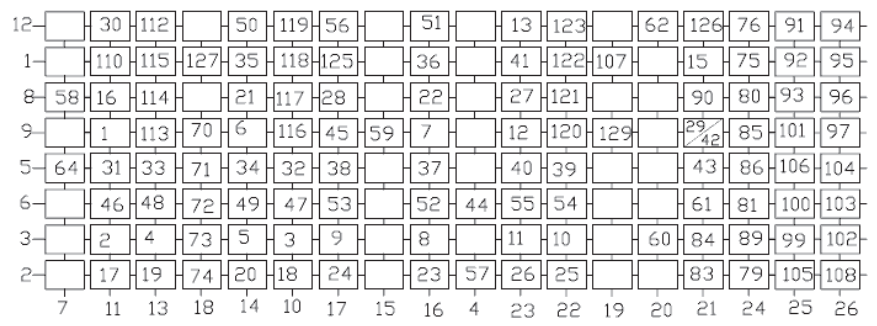
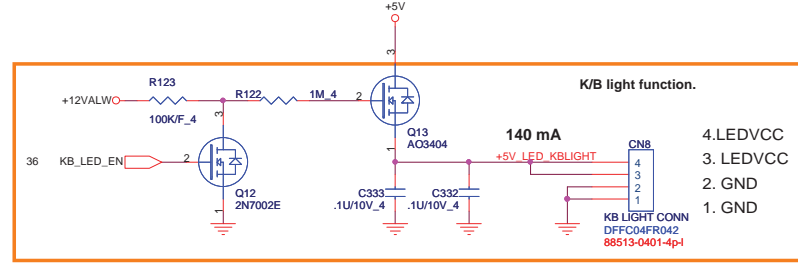
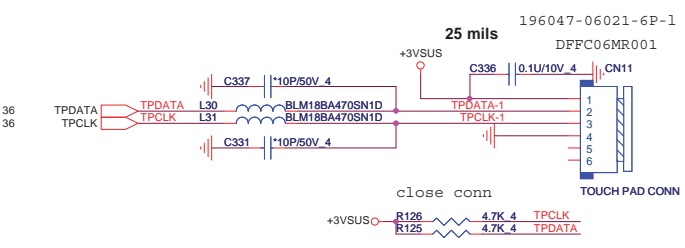
POWER BUTTON CONNECT



KEYBOARD Con.

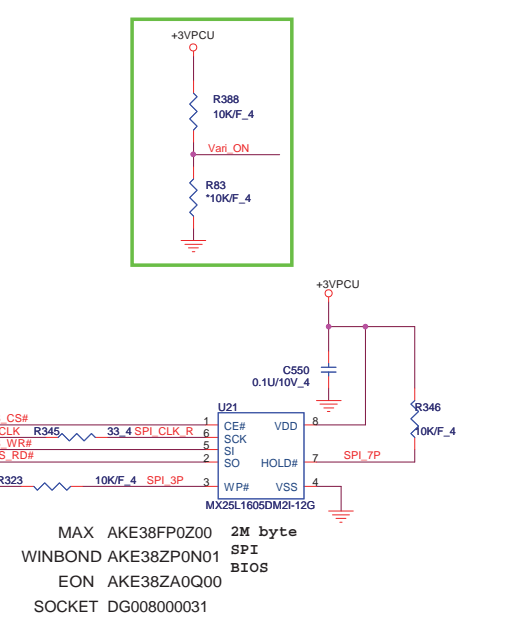
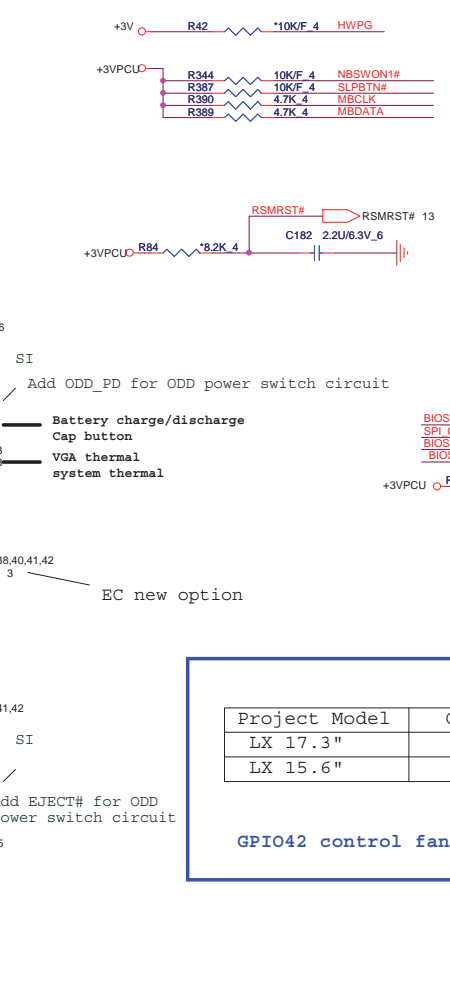
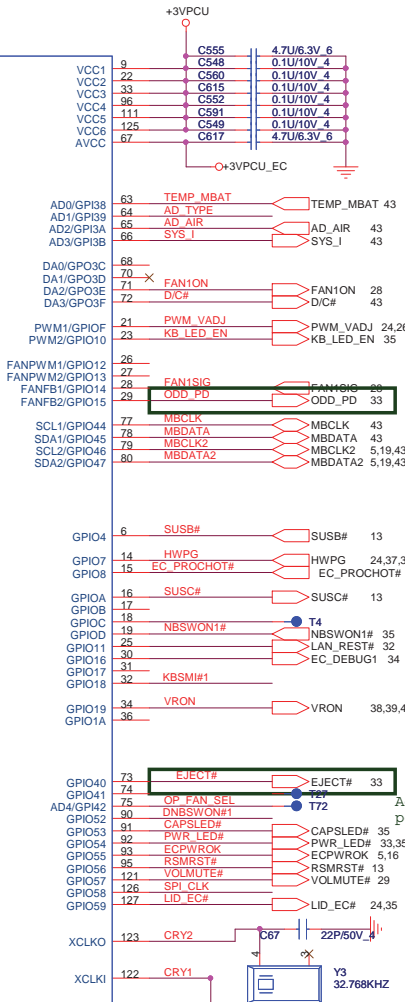
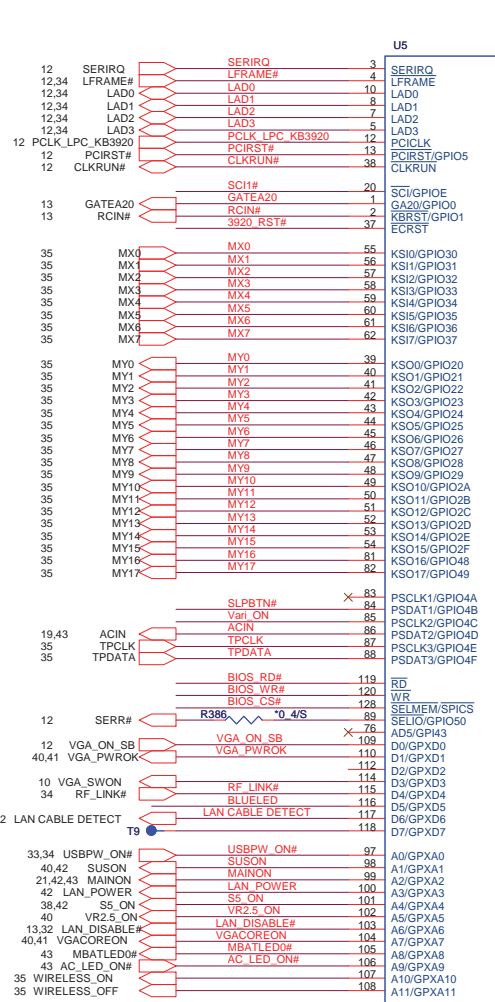


TOUCH PAD CONN



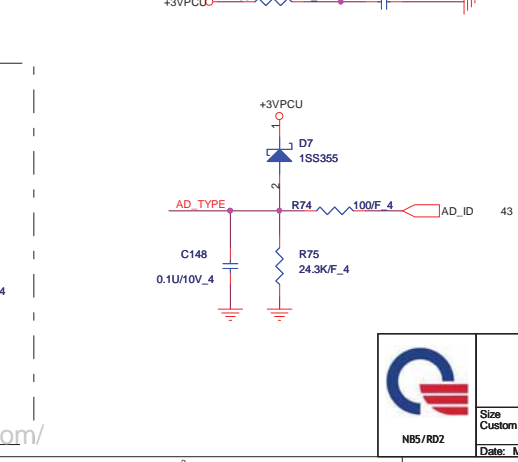
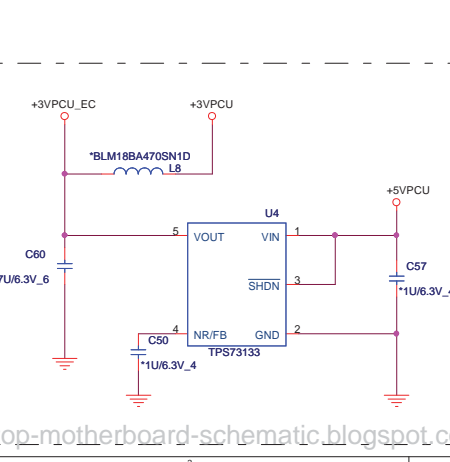
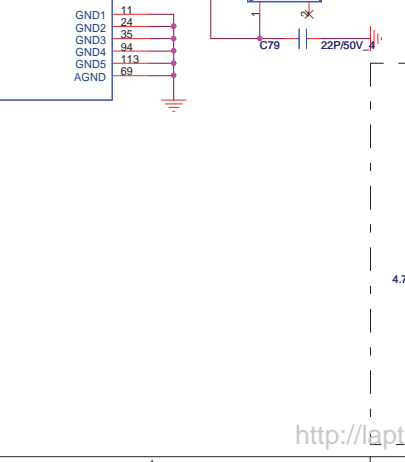
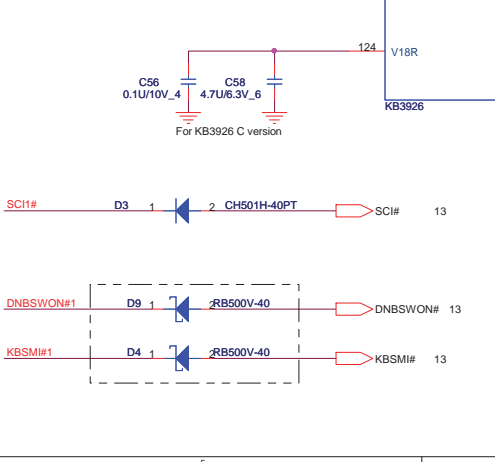
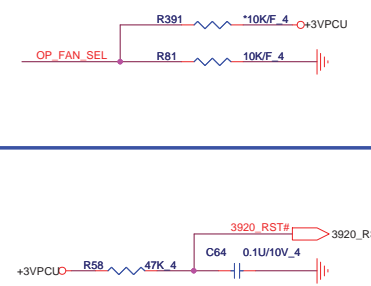
<http://laptop-motherboard-schematic.blogspot.com/>

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number LED/KEYBOARD/SW_BOARD	
Date: Monday, September 28, 2009		Sheet 35 of 46	



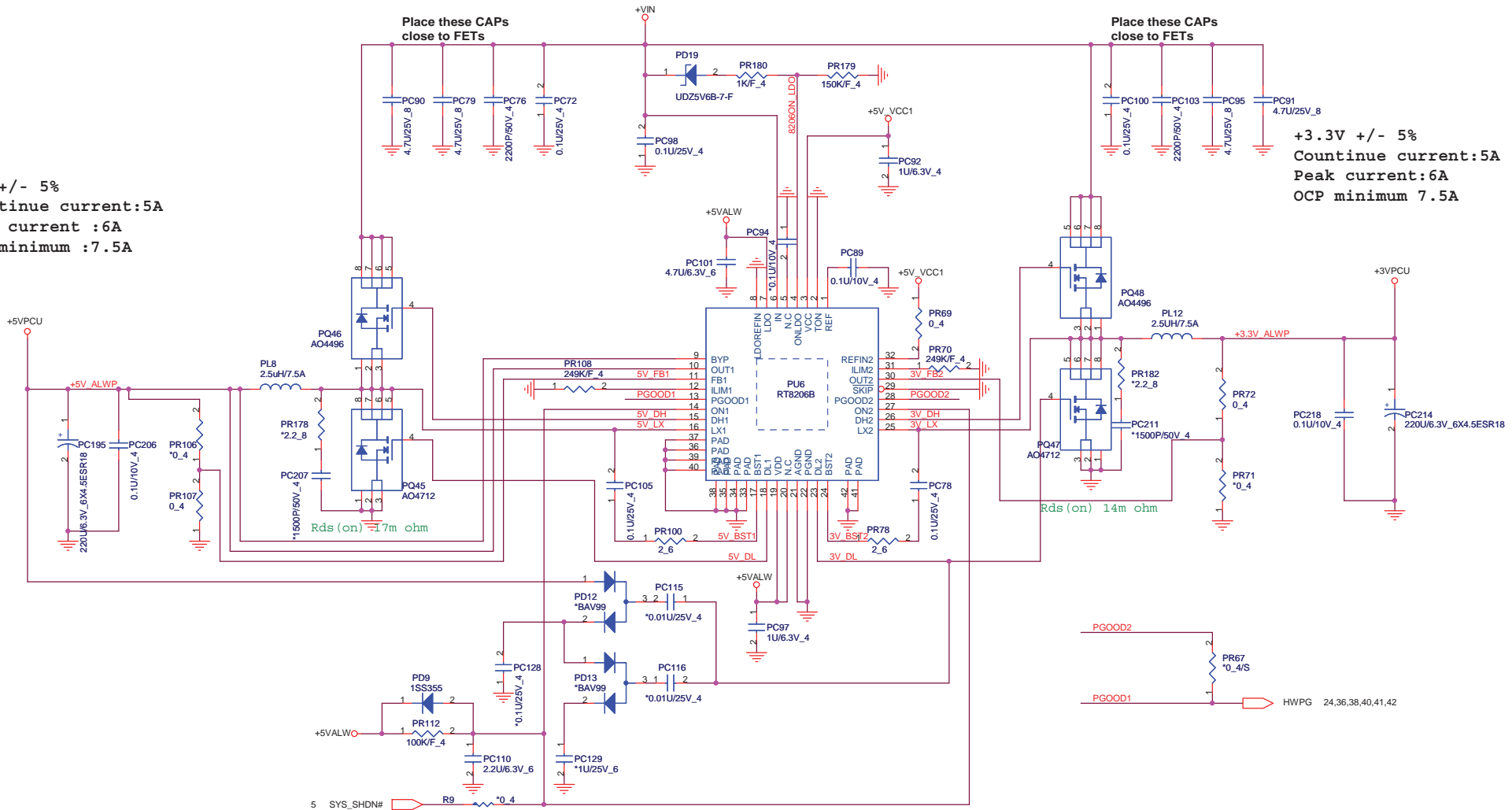
Project Model	GPIO42
LX 17.3"	High
LX 15.6"	Low

GPIO42 control fan table



+5V +/- 5%
 Countinue current:5A
 Peak current :6A
 OCP minimum :7.5A

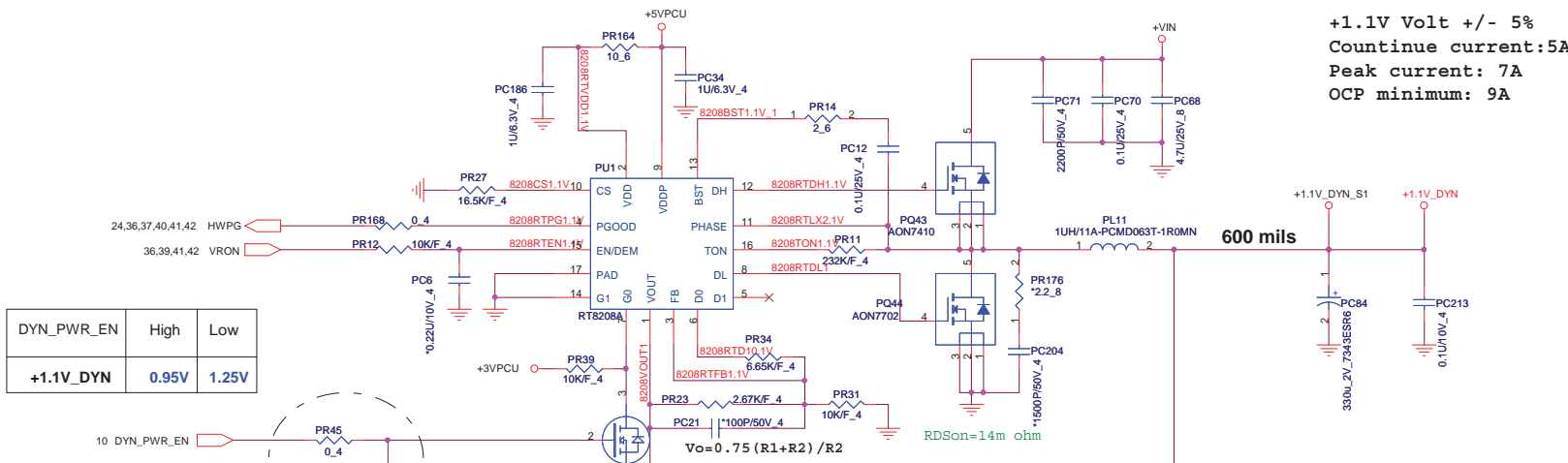
+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A



- +VIN 24,31,38,39,40,41,42,43
- +3VPCU 4,6,12,24,33,35,36,38,39,40,41,42,43
- +5VPCU 33,34,36,38,39,40,41,42,43

<http://laptop-motherboard-schematic.blogspot.com/>

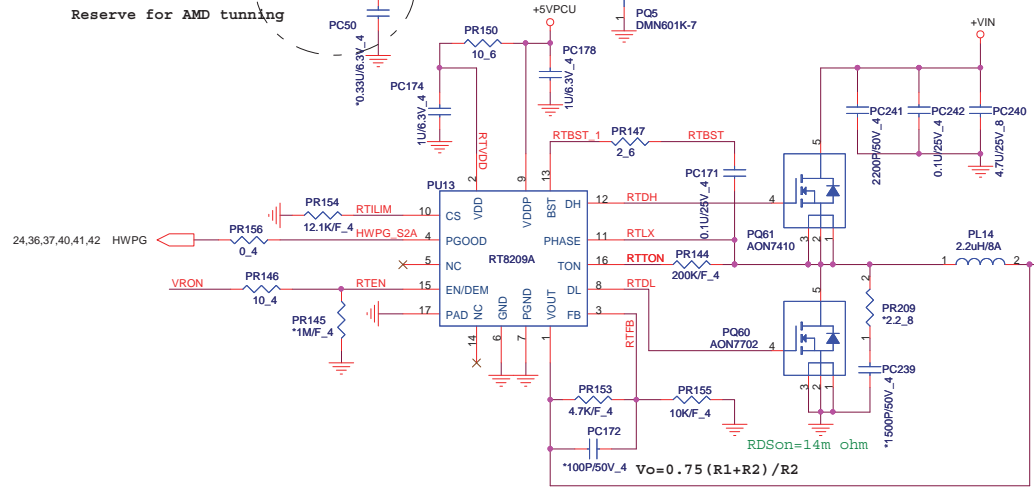
	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Size Custom	Document Number +5V/+3V (RT8206B)
Date: Monday, September 28, 2009 Sheet 37 of 46		



+1.1V Volt +/- 5%
 Countinue current:5A
 Peak current: 7A
 OCP minimum: 9A

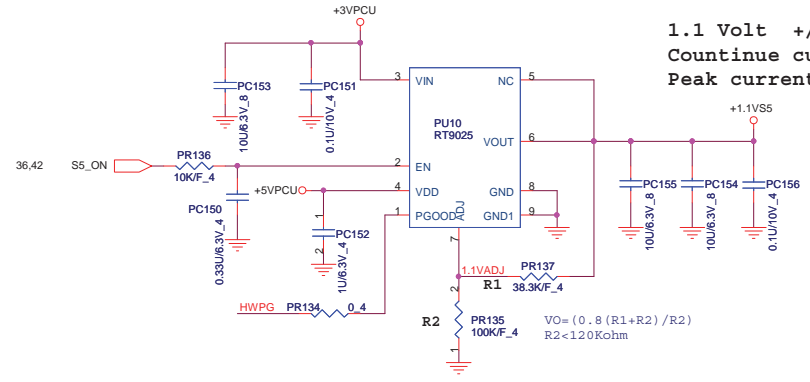
DYN_PWR_EN	High	Low
+1.1V_DYN	0.95V	1.25V


Reserve for AMD tuning



+1.1V Volt +/- 5%
 Countinue current:5A
 Peak current: 7A
 OCP minimum: 9A

1.1 Volt +/- 5%
 Countinue current:0.2A
 Peak current:0.5A



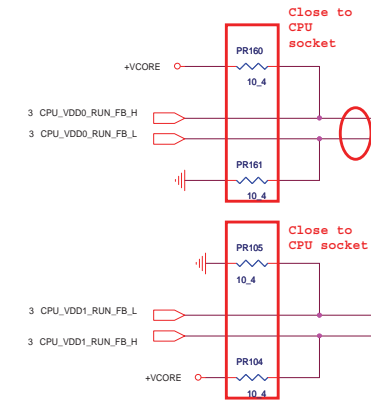
 <p>NBS/RD2</p>	<p>PROJECT : LX89 Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number VGA Core/+1.8VGF1.0VGF</p>	<p>Rev 1A</p>
	<p>Date: Monday, September 28, 2009</p>		<p>Sheet 38 of 46</p>

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

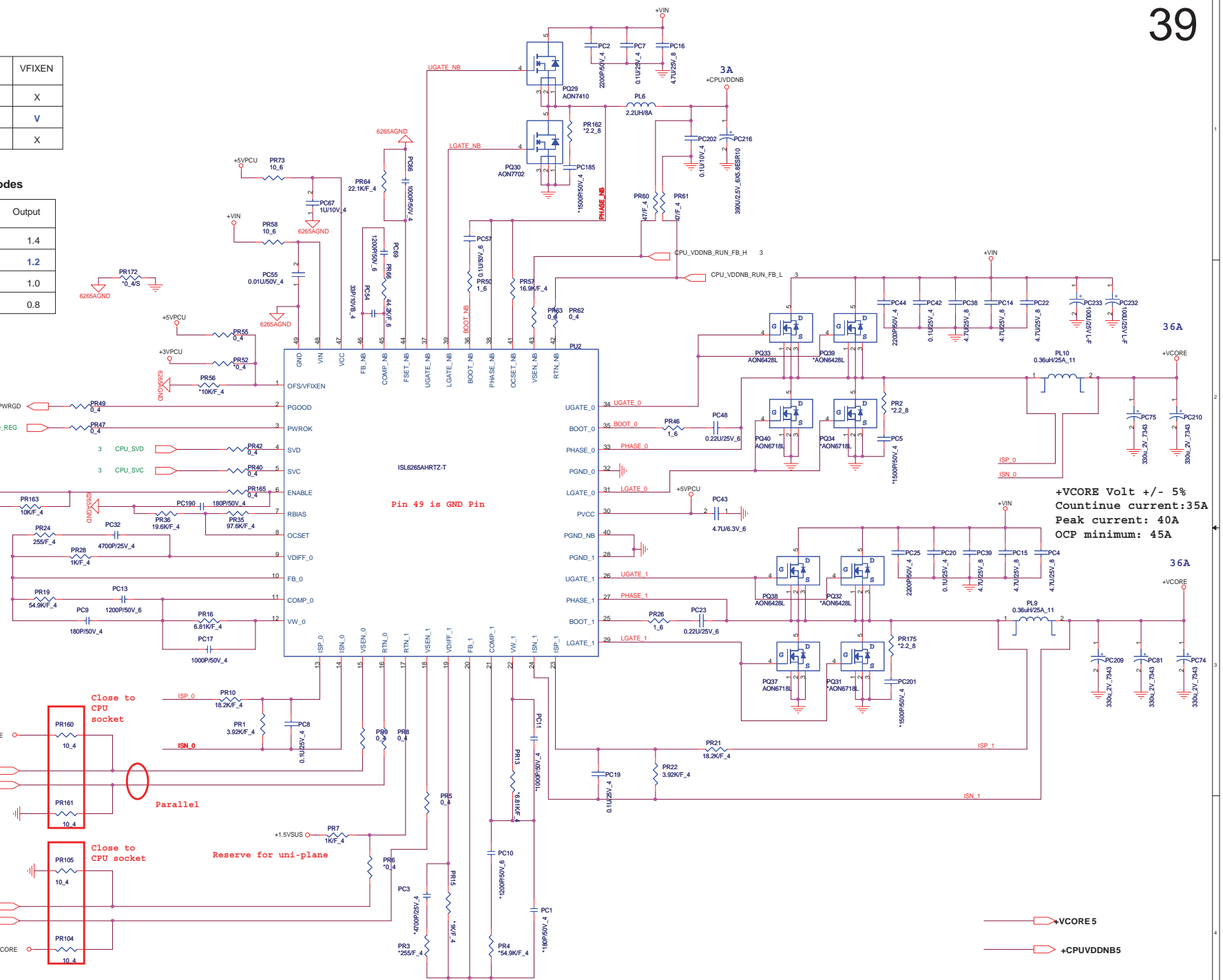
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

- 16 VRM_PWRGD
- 3 CPU_PWRGD_SVID_REG
- 3 CPU_SVD
- 3 CPU_SVC
- 36.38.41.42 VRON



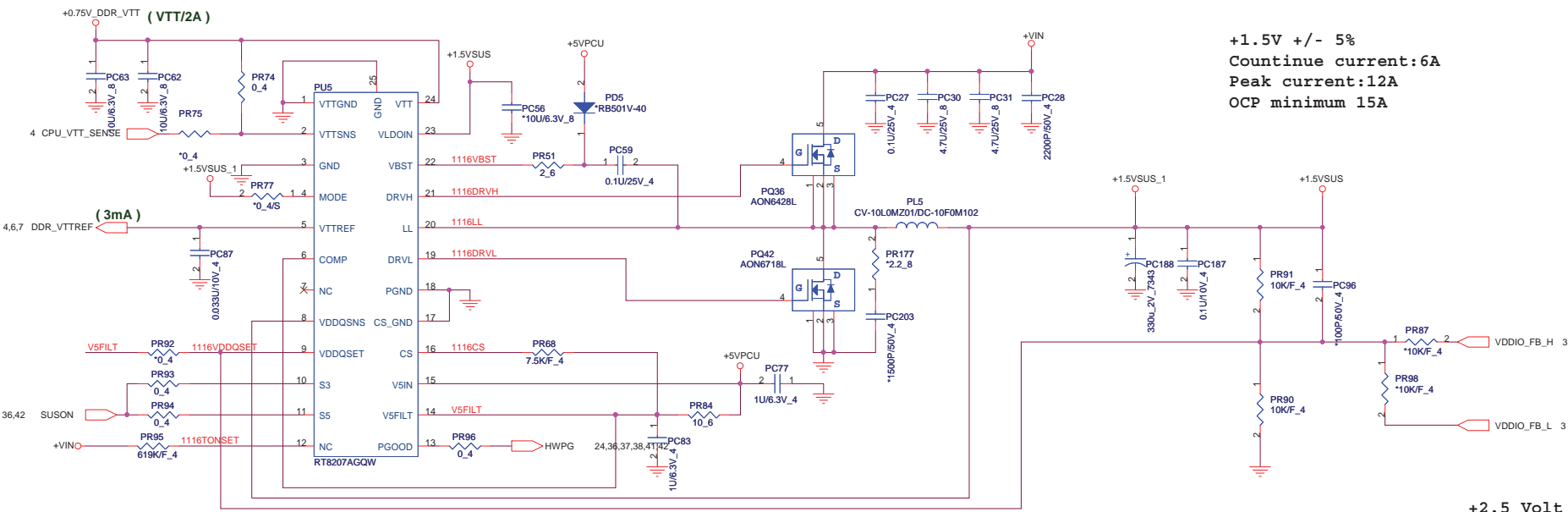
Pin 49 is GND Pin

<http://laptop-motherboard-schematic.blogspot.com/>



+V CORE Volt +/- 5%
 Countinue current: 35A
 Peak current: 40A
 OCP minimum: 45A

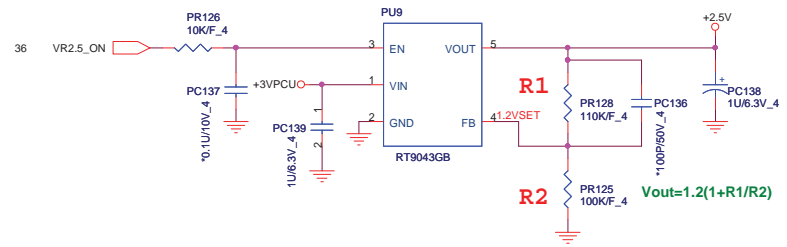




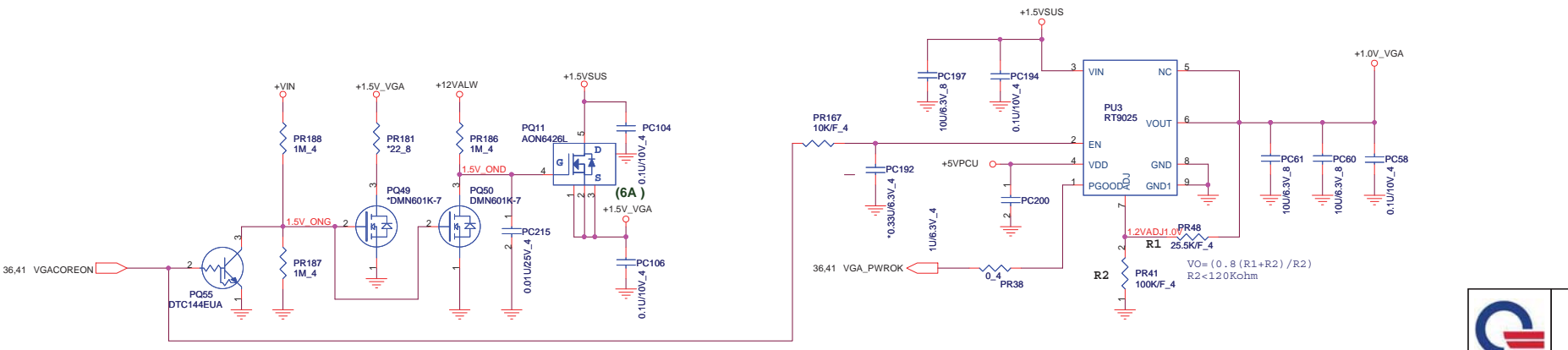
+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

4.6.7 DDR_VTTREF (3mA)


+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA



+1.0V +/- 5%
Countinue current:1.5A
Peak current:3A

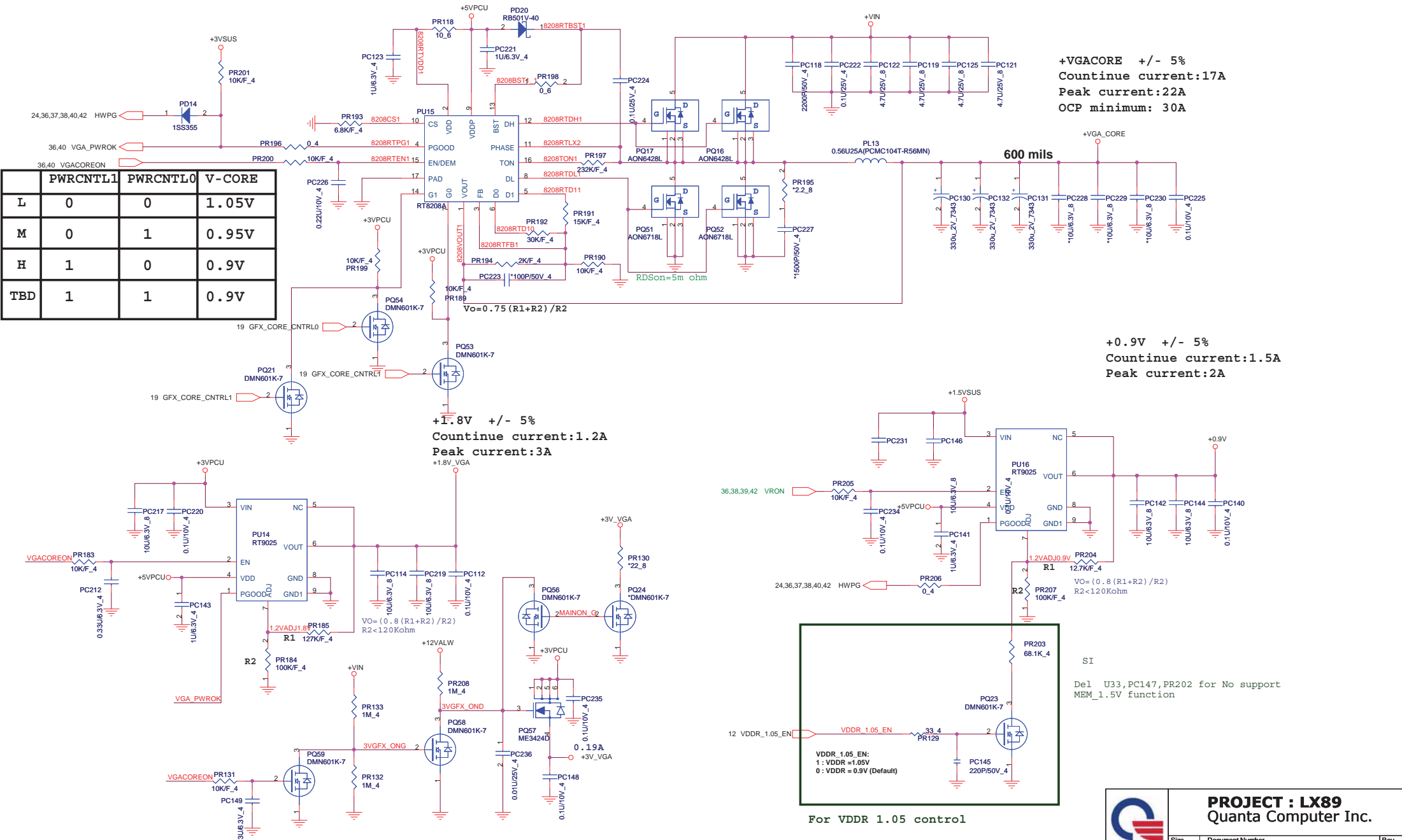


<http://laptop-motherboard-schematic.blogspot.com/>

 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number DDR3 (RT8207) Date: Monday, September 28, 2009	Rev 1A Sheet 40 of 46

VGA Core

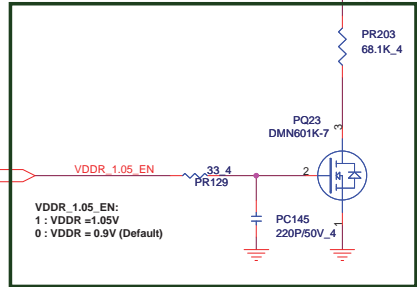
	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V



+VGA_CORE +/- 5%
 Countinue current:17A
 Peak current:22A
 OCP minimum: 30A

+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

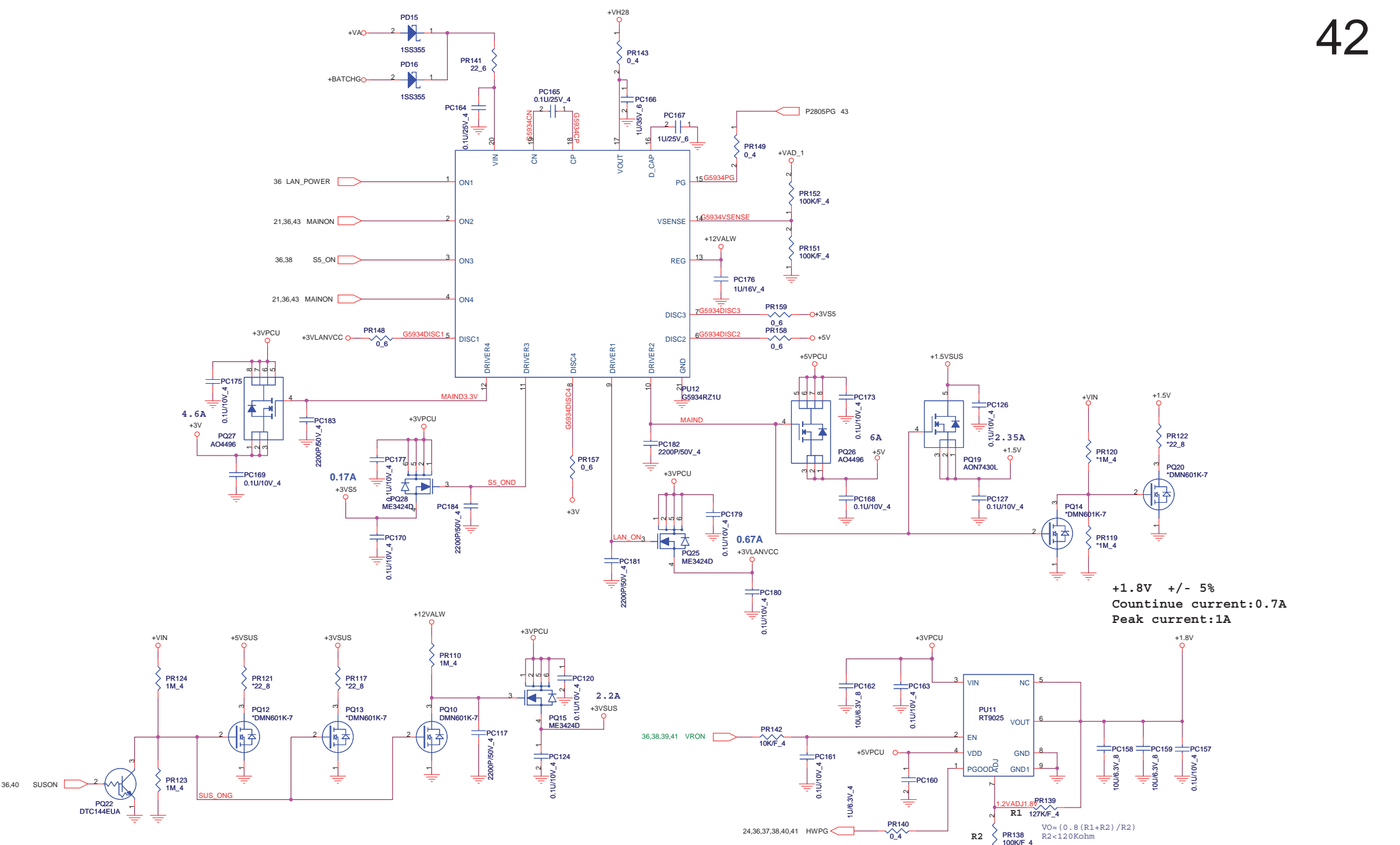
+1.8V +/- 5%
 Countinue current:1.2A
 Peak current:3A



For VDDR 1.05 control

SI
 Del U33,PC147,PR202 for No support
 MEM_1.5V function

	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number +VGA_CORE (RT8208/1.8V)	Rev 1A
Date: Monday, September 28, 2009		Sheet 41 of 46




+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

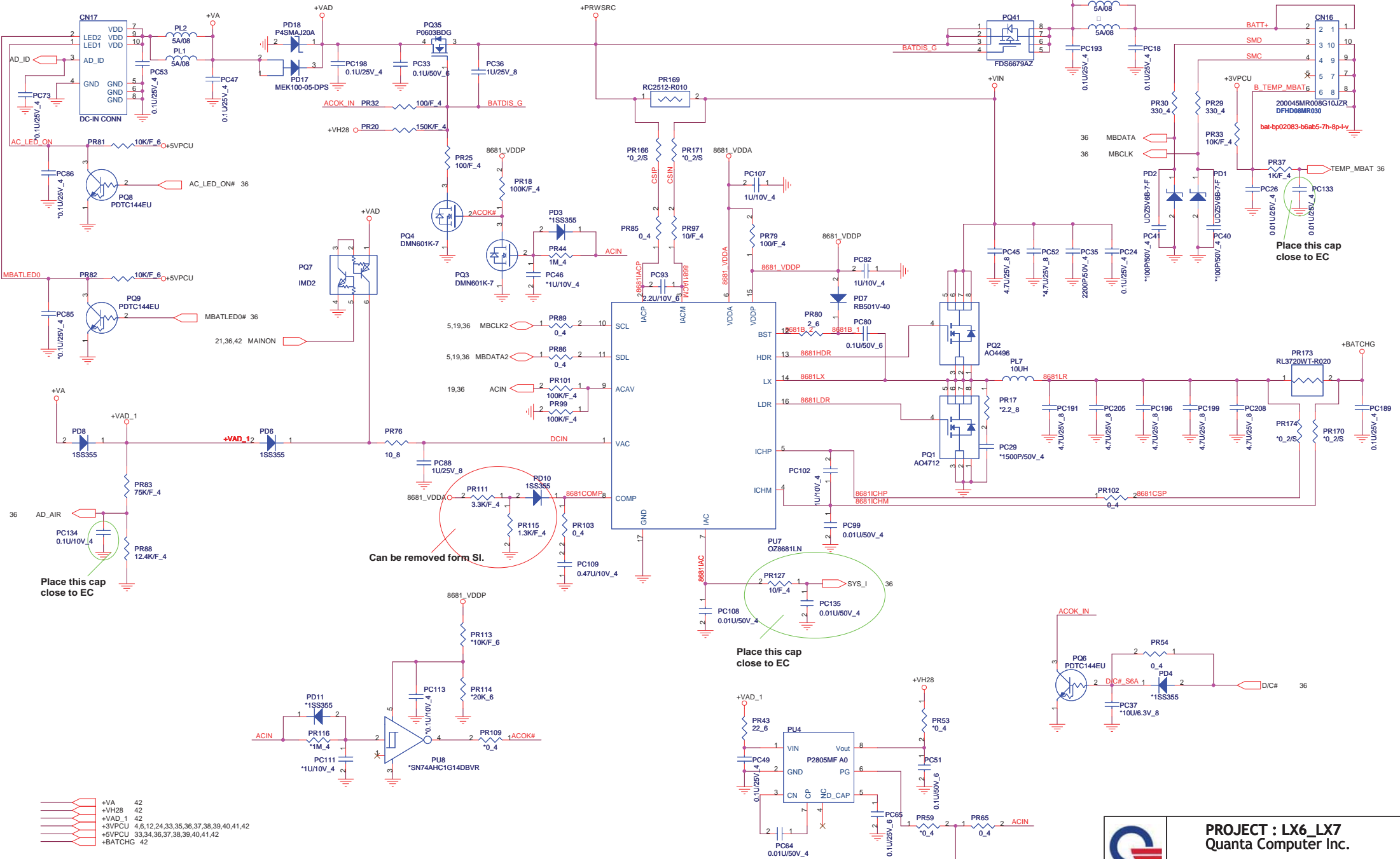
$$V_O = (0.8 (R1 + R2) / R2)$$

$$R2 < 1.20Kohm$$

<http://laptop-motherboard-schematic.blogspot.com/>

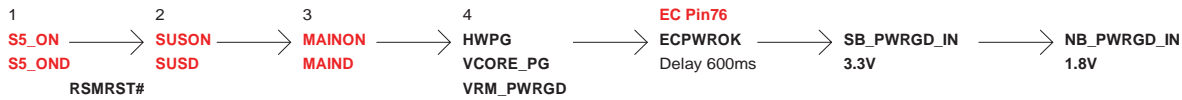
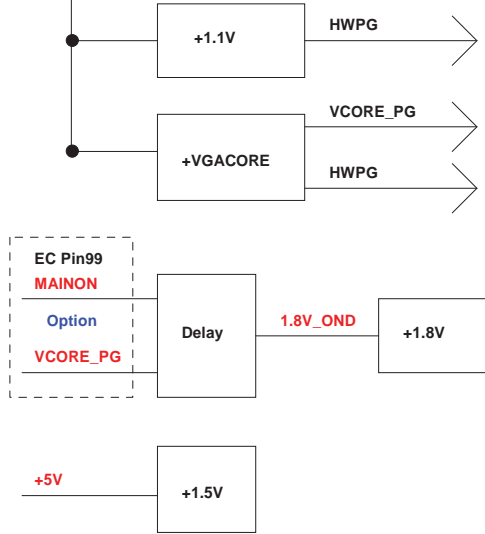
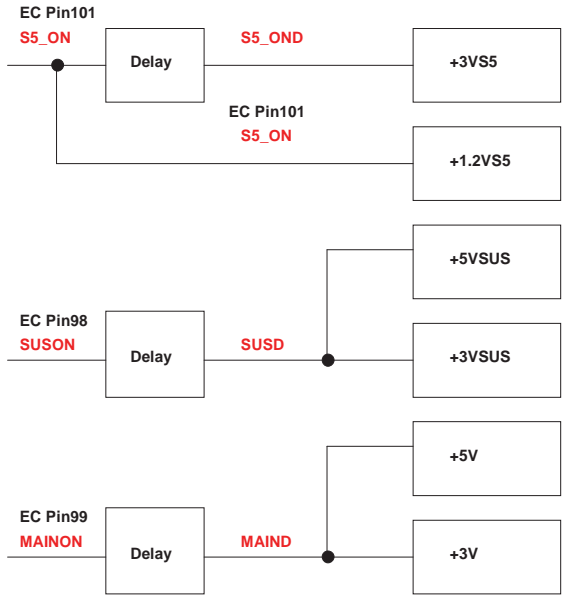
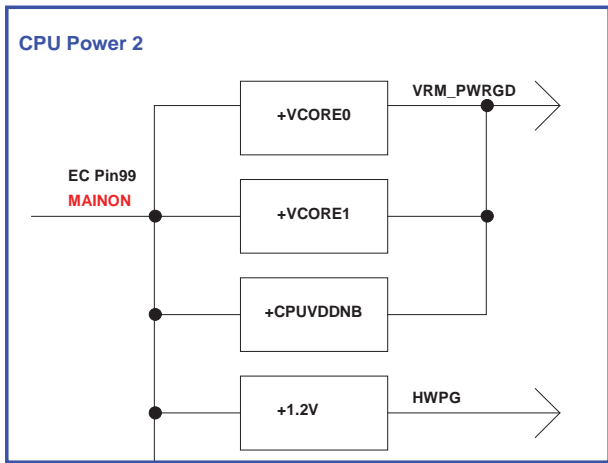
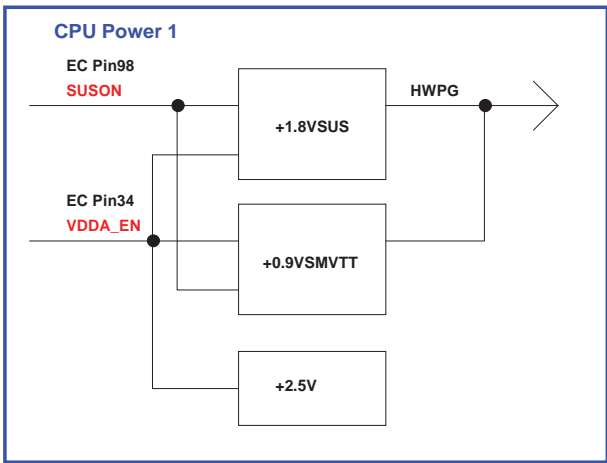
 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number Dis-charge IC (P2806)	Rev 1A
Date: Monday, September 28, 2009 Sheet 42 of 46		

TOP DC JACK
65W/90W
20346-100n-1-10p-1dv



<http://laptop-motherboard-schematic.blogspot.com/>

	PROJECT : LX6_LX7		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number Charger (BQ24704)		
Date: Monday, September 28, 2009	Sheet 43	of 46	



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT