

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel
Crestline_PM+ICH8-M core logic

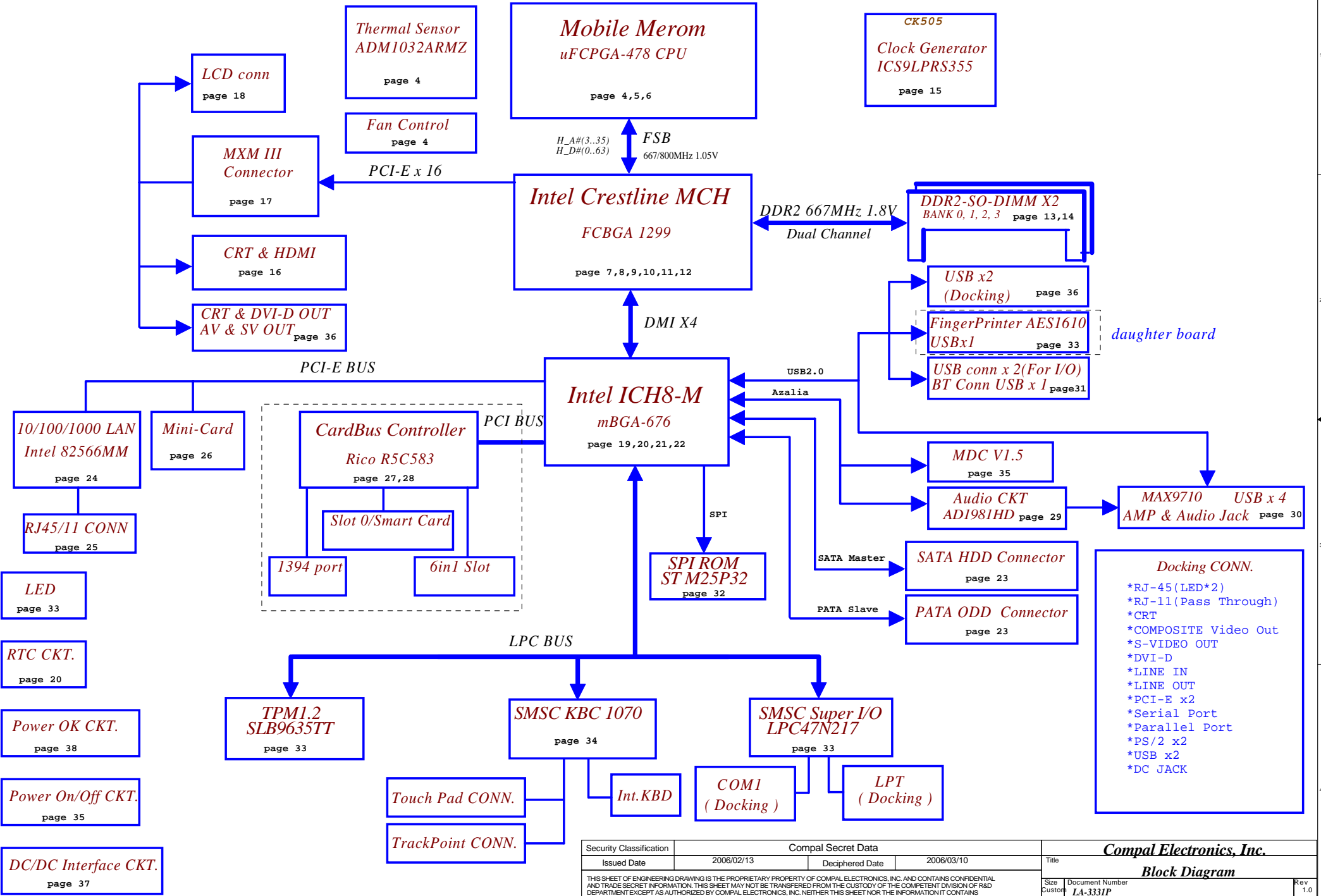
2007-05-15

REV:1.0



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				Date:	Tuesday, May 15, 2007	Sheet 2 of 59

- Docking CONN.**
- *RJ-45(LED*2)
 - *RJ-11(Pass Through)
 - *CRT
 - *COMPOSITE Video Out
 - *S-VIDEO OUT
 - *DVI-D
 - *LINE IN
 - *LINE OUT
 - *PCI-E x2
 - *Serial Port
 - *Parallel Port
 - *PS/2 x2
 - *USB x2
 - *DC JACK

Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+3VM +1.25VM +1.05VM	+5V +1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP
s0	○	○	○	○	○
s1	○	○	○	○	○
s3	○	○	○	○	✗
s5 S4/AC	○	○	○	✗	✗
s5 S4/ Battery only	○	✗	✗	✗	✗
s5 S4/AC & Battery don't exist	✗	✗	✗	✗	✗

○ MEANS ON ✗ MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	M/B
1	Finger Printer
2	M/B
3	On Audio Board
4	On Audio Board
5	On Audio Board
6	Blut Tooth
7	Docking
8	On Audio Board
9	Docking

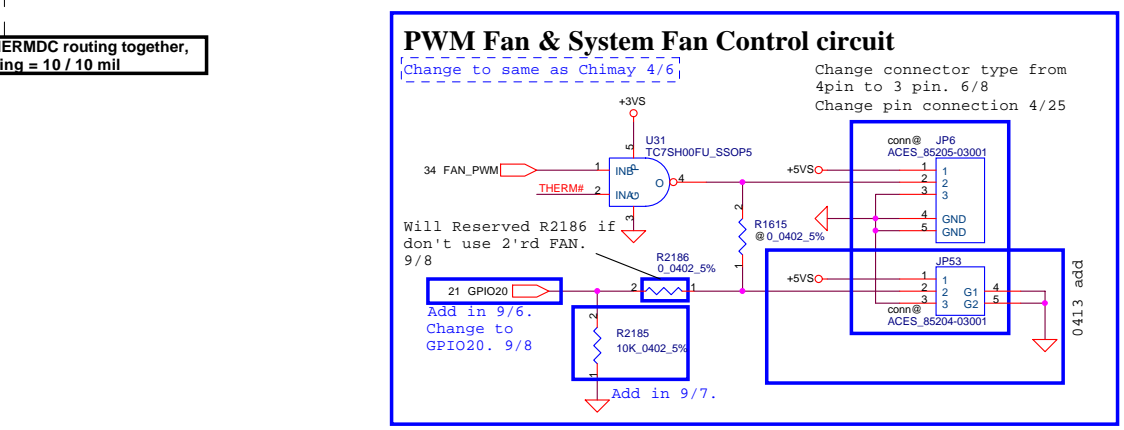
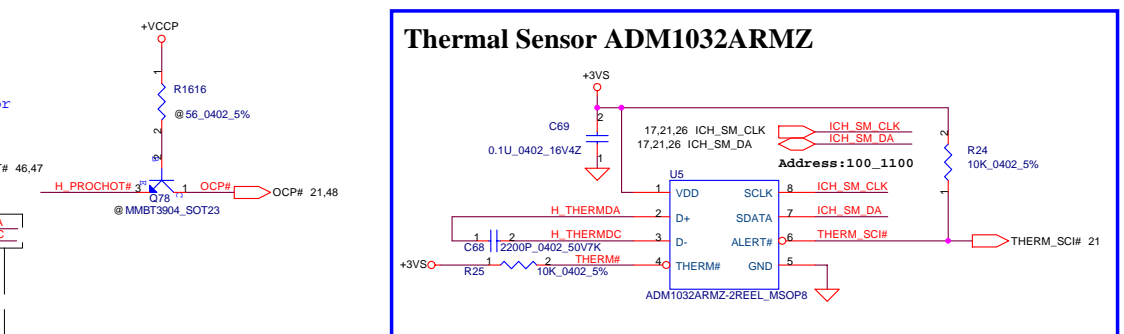
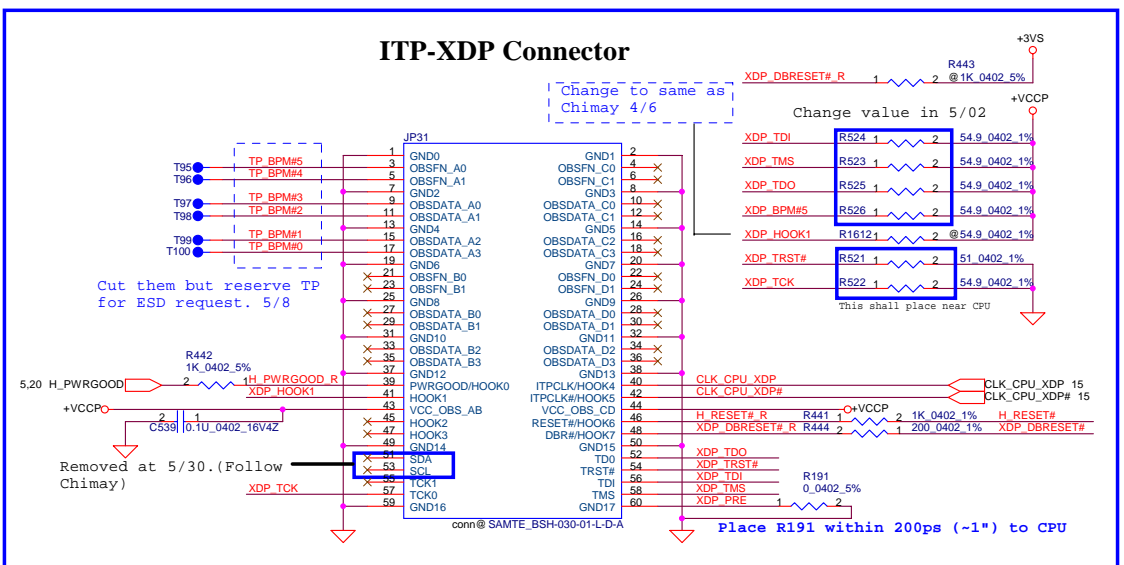
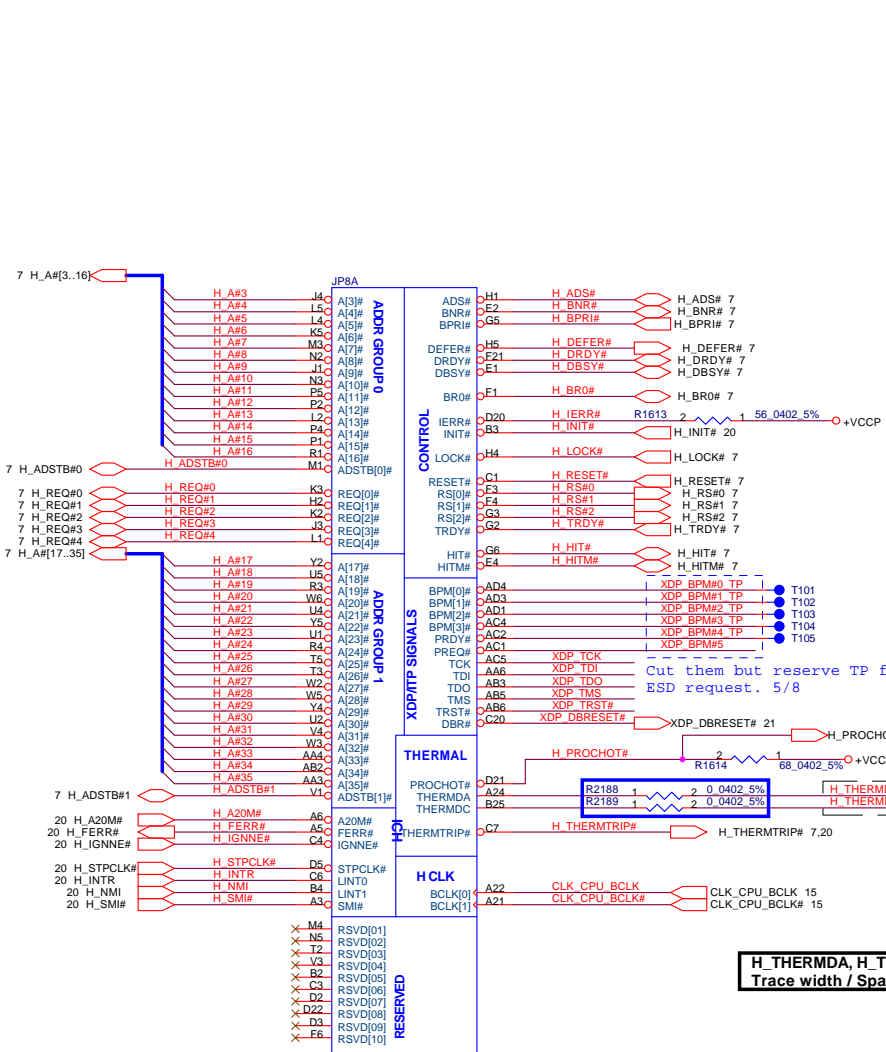
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass storage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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				1.0
				Notes List

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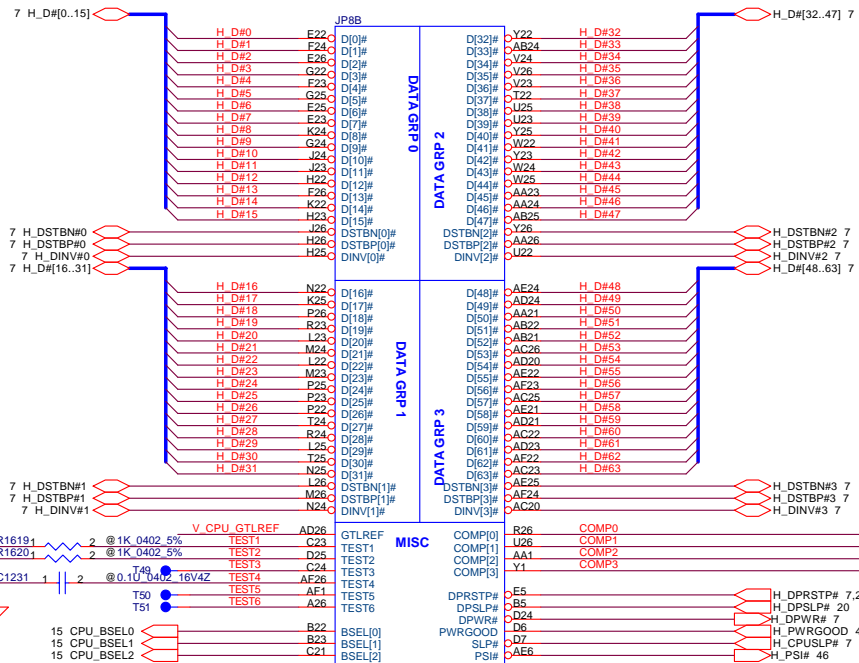
Notes List

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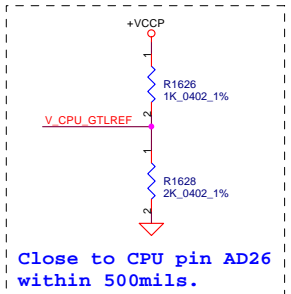
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

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				Merom(1/3)-AGTL+XDP	
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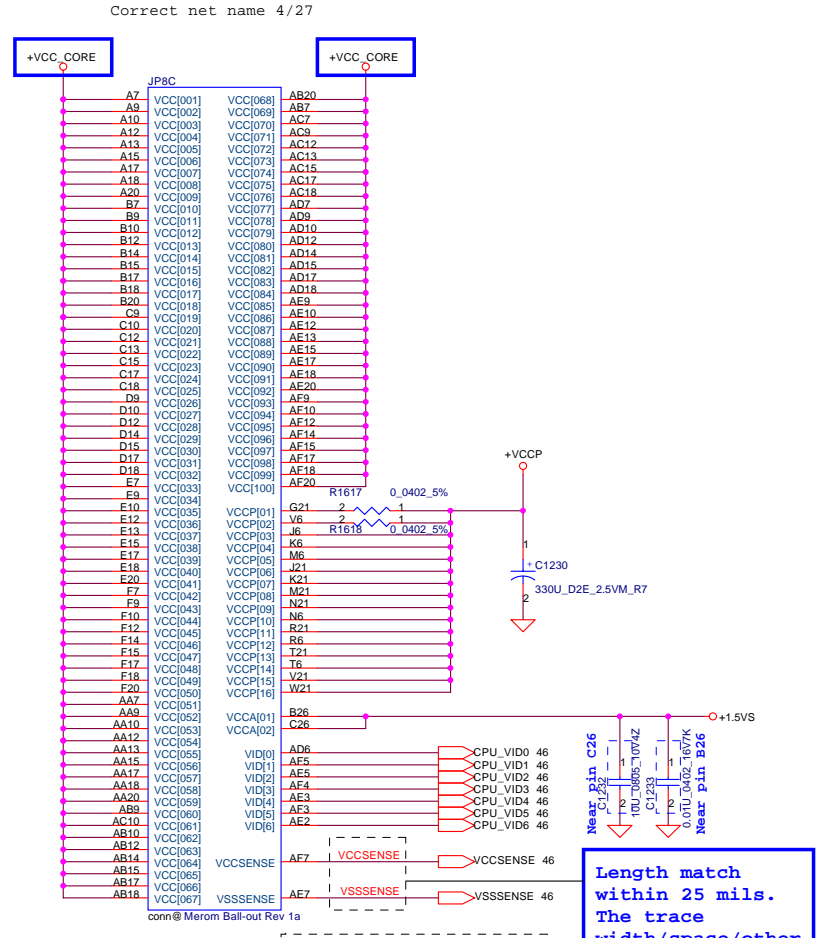
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

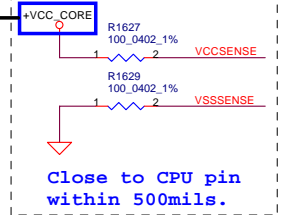


Close to CPU pin AD26 within 500mils.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Correct net name 6/16

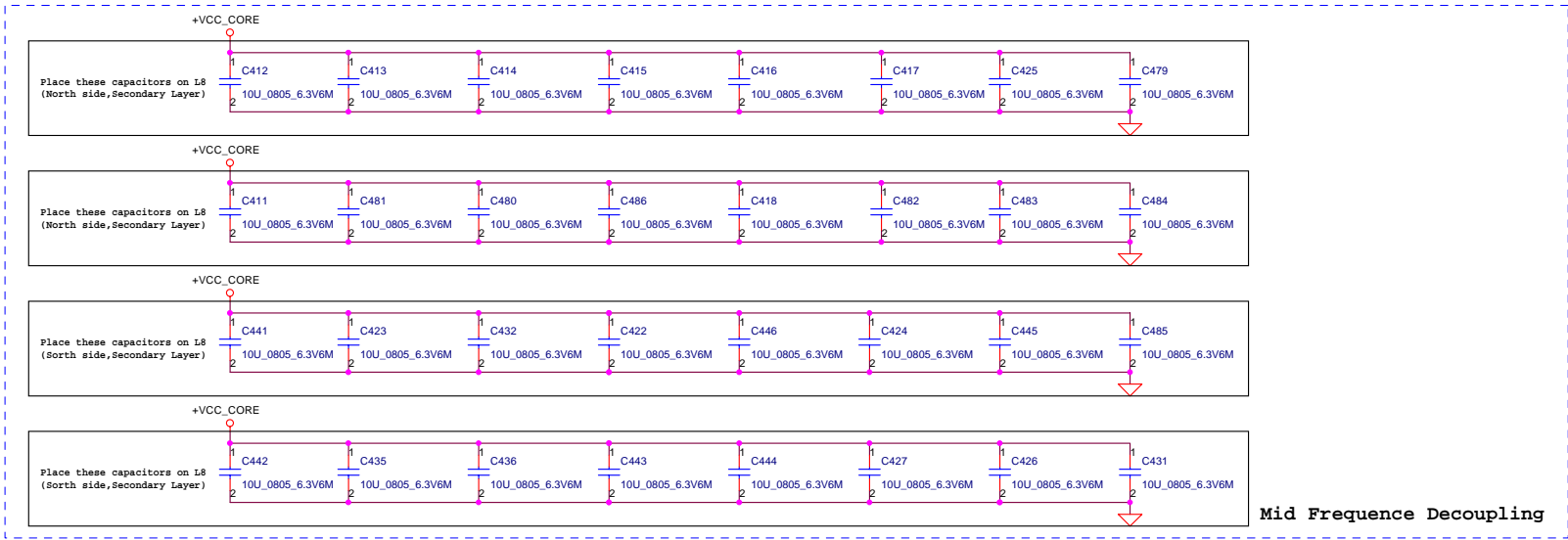


Close to CPU pin within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

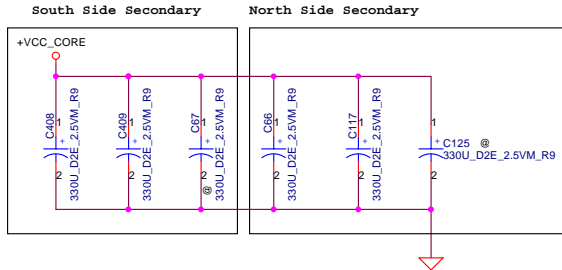
JP8D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D16	VSS[030]	AA11
D19	VSS[031]	AA14
D23	VSS[032]	AA16
D26	VSS[033]	AA19
E3	VSS[034]	AA22
E6	VSS[035]	AA25
E8	VSS[036]	AB1
F11	VSS[037]	AB4
F14	VSS[038]	AB8
F16	VSS[039]	AB11
F19	VSS[040]	AB13
E21	VSS[041]	AB16
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F8	VSS[044]	AB26
F11	VSS[045]	AC3
F13	VSS[046]	AC6
F16	VSS[047]	AC8
F19	VSS[048]	AC11
F2	VSS[049]	AC14
F22	VSS[050]	AC16
F25	VSS[051]	AC19
G4	VSS[052]	AC21
G1	VSS[053]	AC24
G23	VSS[054]	AD2
G26	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD16
J2	VSS[060]	AD19
J5	VSS[061]	AD22
J22	VSS[062]	AD25
J25	VSS[063]	AE1
K1	VSS[064]	AE4
K4	VSS[065]	AE8
K23	VSS[066]	AE11
K26	VSS[067]	AE14
L3	VSS[068]	AE16
L6	VSS[069]	AE19
L21	VSS[070]	AE23
L24	VSS[071]	AE26
M2	VSS[072]	A2
M5	VSS[073]	AF6
M22	VSS[074]	AF8
M25	VSS[075]	AF11
N1	VSS[076]	AF13
N4	VSS[077]	AF16
N23	VSS[078]	AF19
N26	VSS[079]	AF21
P3	VSS[080]	A25
	VSS[081]	AF25
	VSS[082]	
	VSS[083]	
	VSS[084]	
	VSS[085]	
	VSS[086]	
	VSS[087]	
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	VSS[162]	
	VSS[163]	

conn@Merom Ball-out Rev 1a

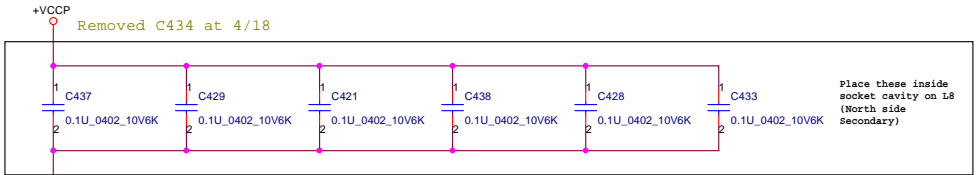


Mid Frequency Decoupling

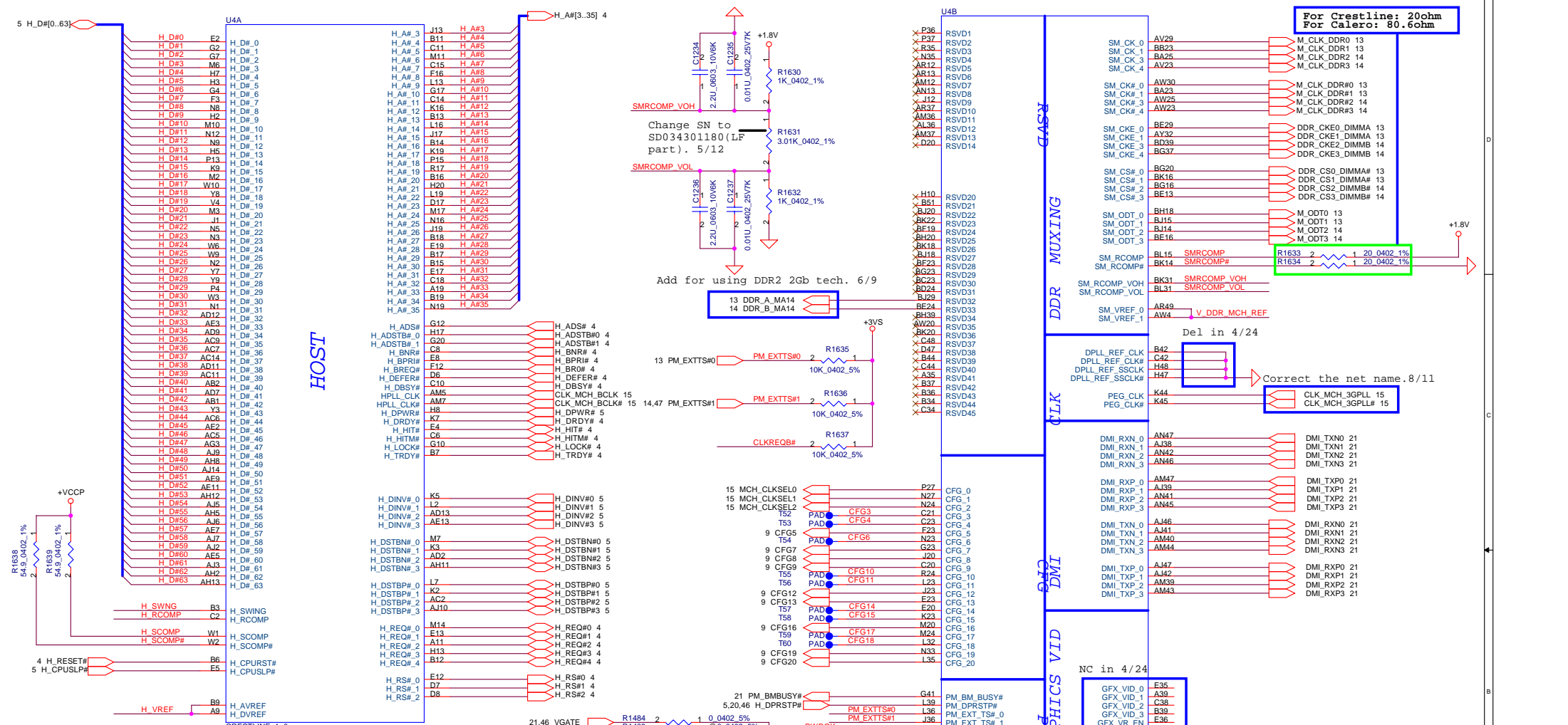
No install C67, C125 at 2007/03/23.



ESR <= 1.5m ohm
Capacitor > 1980uF



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For Crestline: 20ohm
For Calero: 80.6ohm

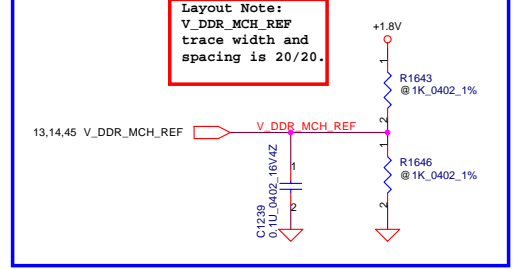
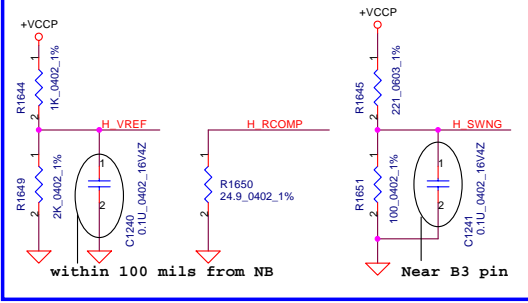
Change SN to
SD034301180 (L#
part.) 5/12

Add for using DDR2 2Gb tech. 6/9

Reserve R2134 for Crestline A0.
Install R2134 from Crestline B0.

Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

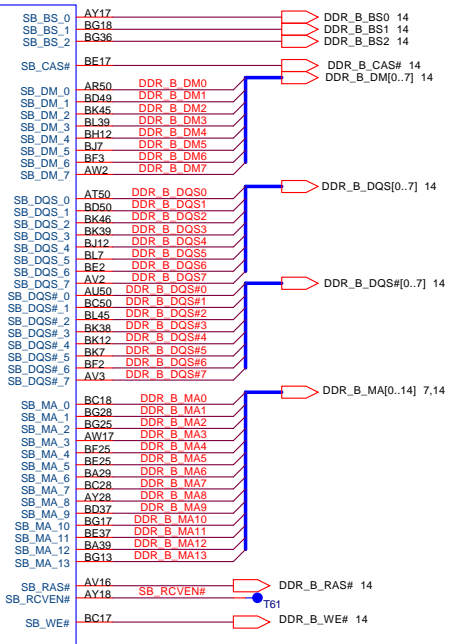
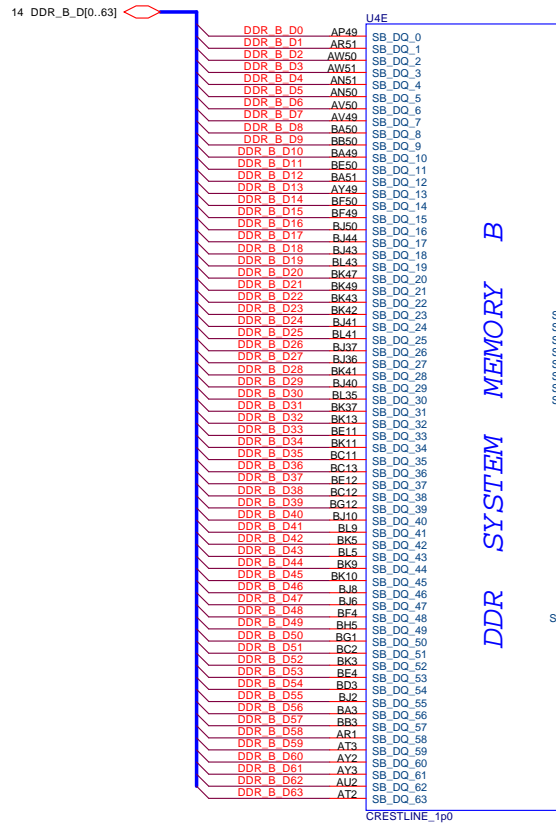
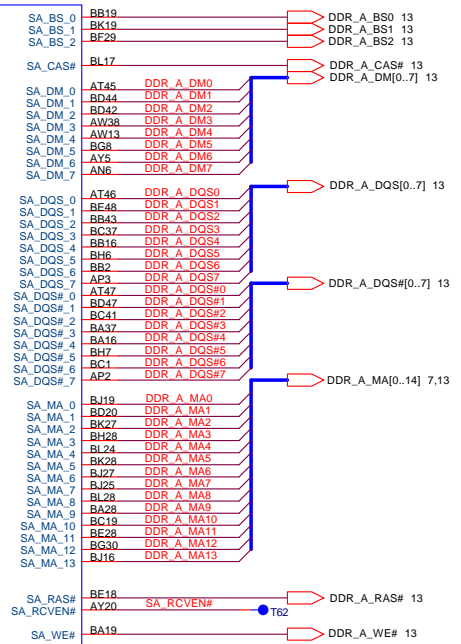
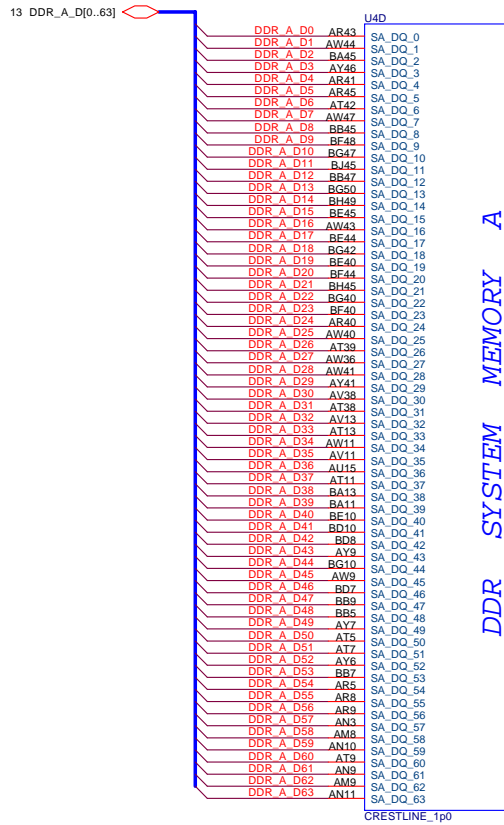
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 18/20



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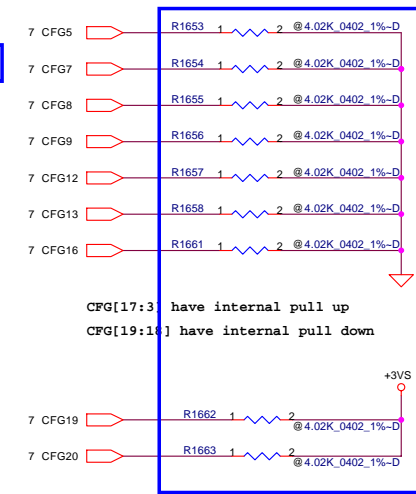
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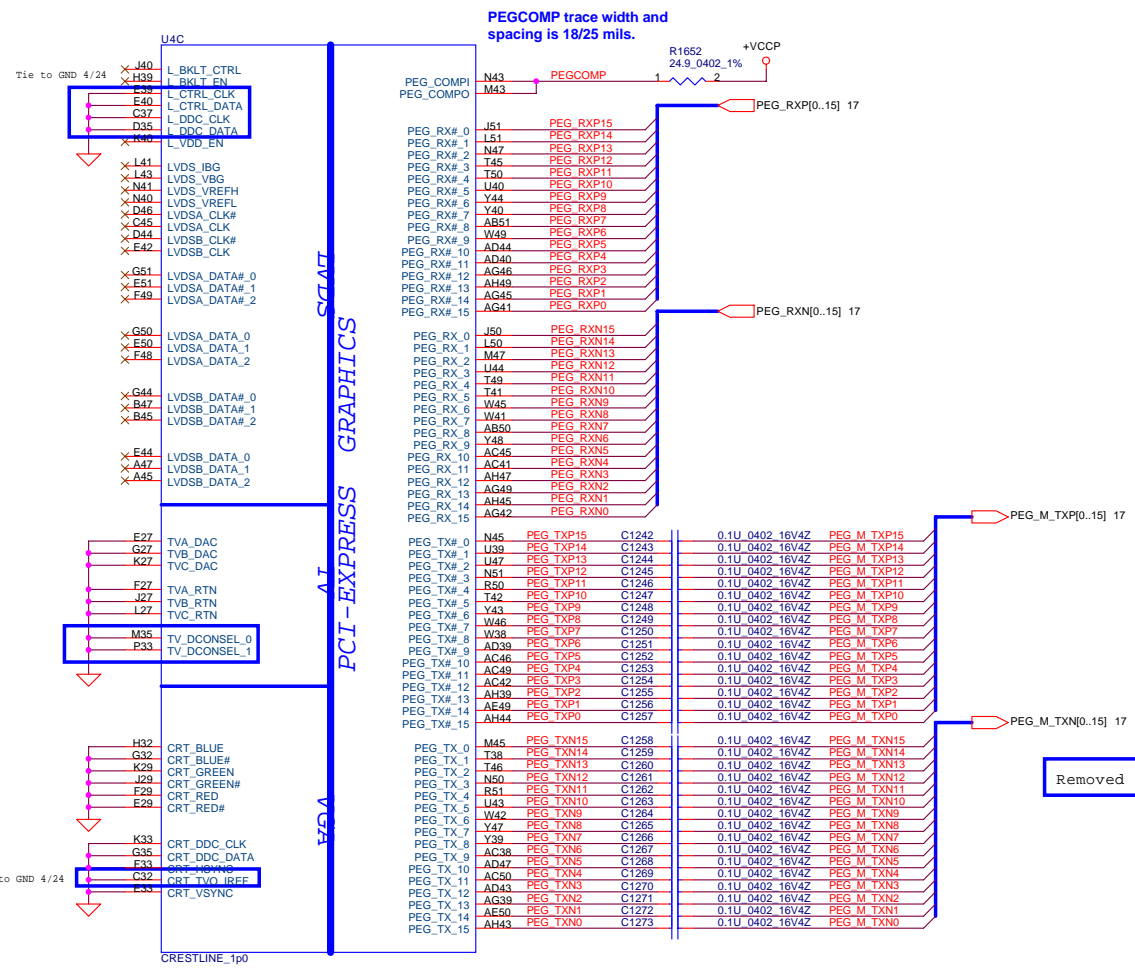
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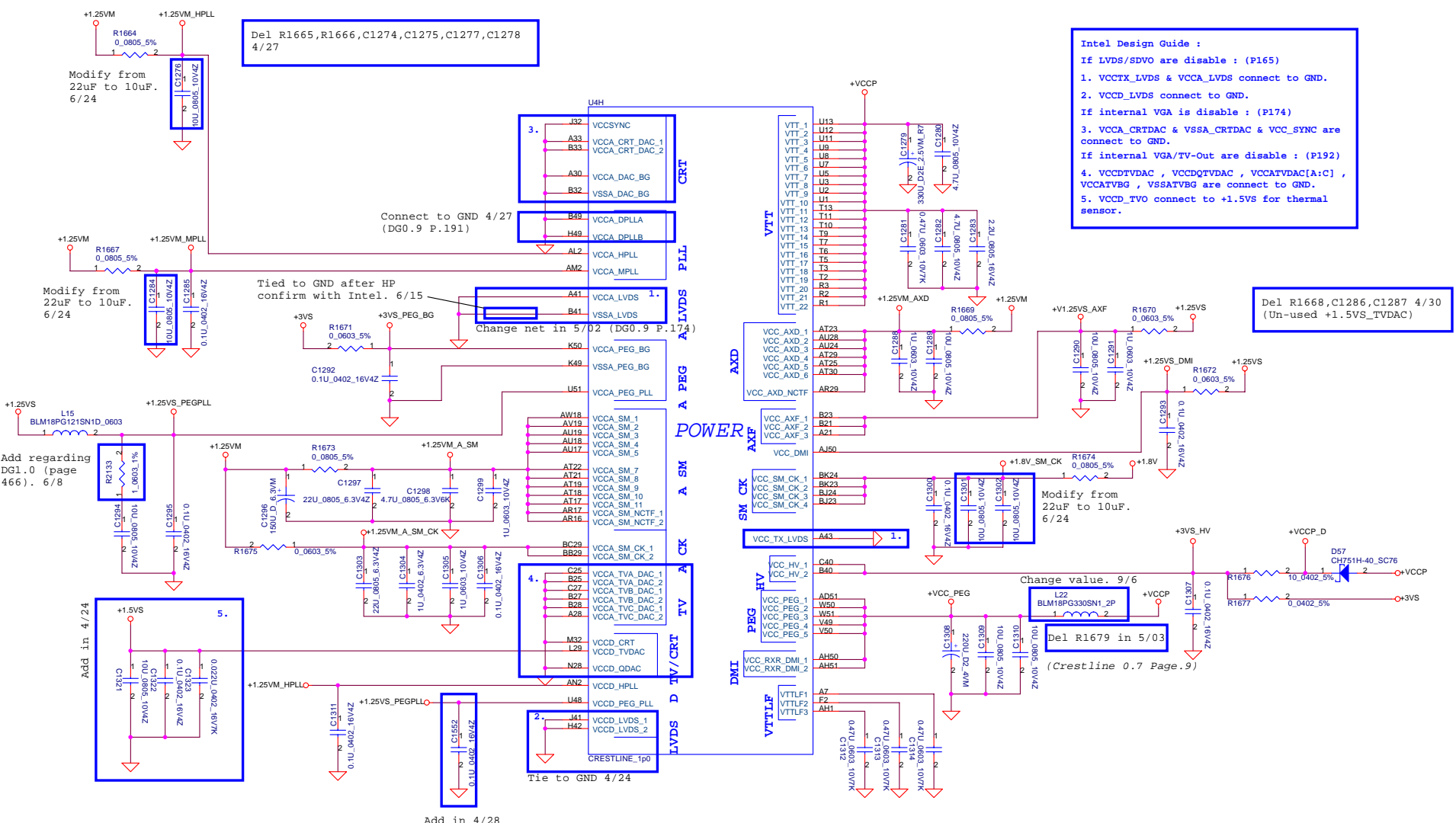
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



Change Value form 2.2K to 4.02K.





Modify from 22uF to 10uF. 6/24

Modify from 22uF to 10uF. 6/24

Add regarding DG1.0 (page 466). 6/8

Add in 4/24

Add in 4/28

Del R1665, R1666, C1274, C1275, C1277, C1278 4/27

Connect to GND 4/27 (DG0.9 P.191)

Tied to GND after HP confirm with Intel. 6/15

Change net in 5/02 (DG0.9 P.174)

Intel Design Guide :
 If LVDS/SDVO are disable : (P165)
 1. VCCTX_LVDS & VCCA_LVDS connect to GND.
 2. VCCD_LVDS connect to GND.
 If internal VGA is disable : (P174)
 3. VCCA_CRTDAC & VSSA_CRTDAC & VCC_SYNC are connect to GND.
 If internal VGA/TV-Out are disable : (P192)
 4. VCCDTV DAC, VCCDQTV DAC, VCCATV DAC[A:C], VCCATV BG, VSSATV BG are connect to GND.
 5. VCCD_TVO connect to +1.5VS for thermal sensor.

Del R1668, C1286, C1287 4/30 (Un-used +1.5VS_TVDAC)

Modify from 22uF to 10uF. 6/24

Change value. 9/6
 Del R1679 in 5/03 (Crestline 0.7 Page.9)

POWER

AXD AXF

SM CK

SM CK

PEG HV

DMIT

LVDS D TV/CRT TV

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

LVDS

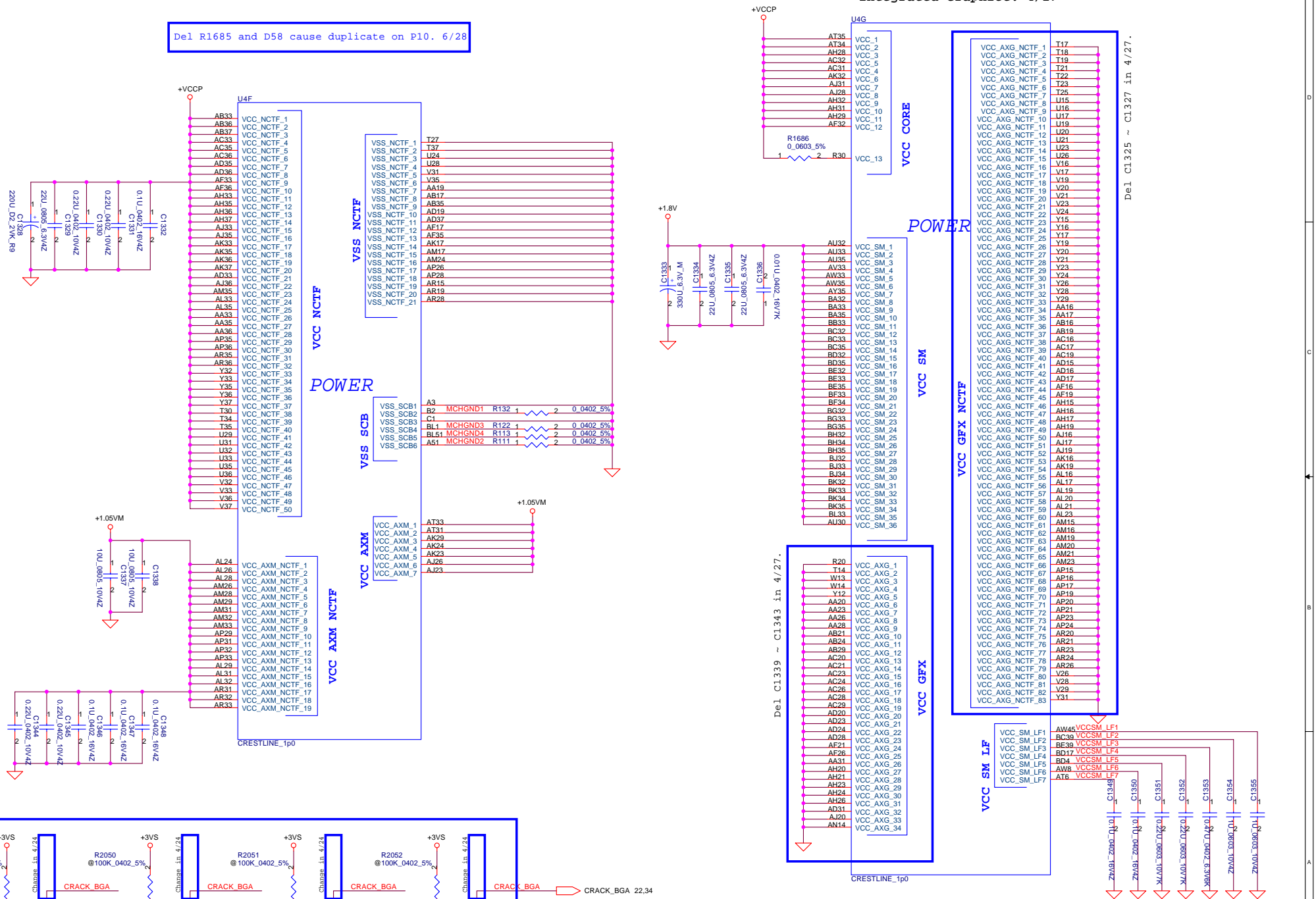
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Compal Electronics, Inc.
 CRESTLINE(4/6)-PWR

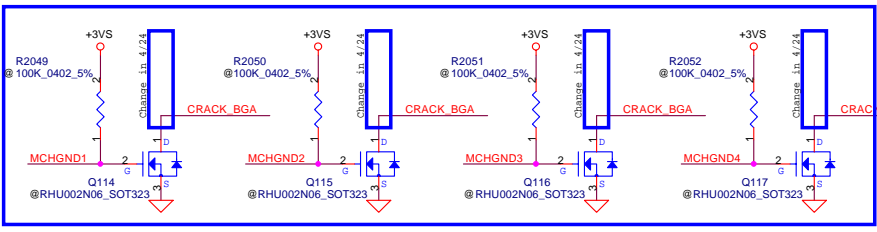
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Del R1685 and D58 cause duplicate on P10. 6/28



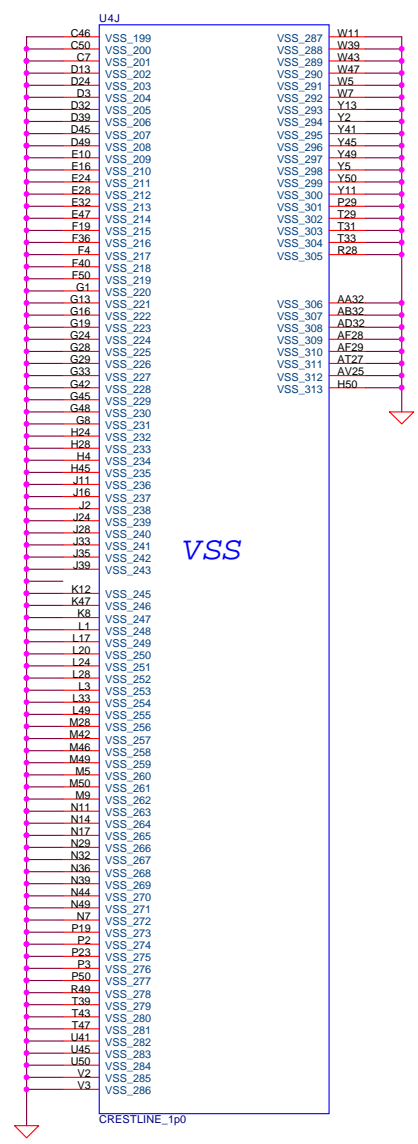
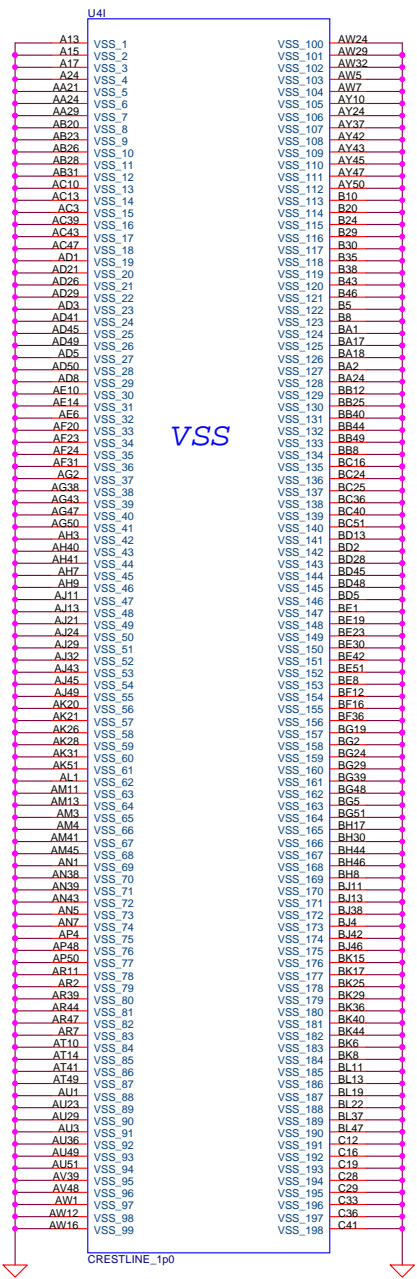
Add in 4/21
Remove in 5/02



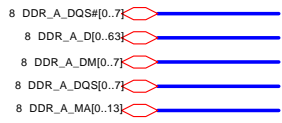
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Issued Date	2006/02/13	Deciphered Date
		2006/03/10

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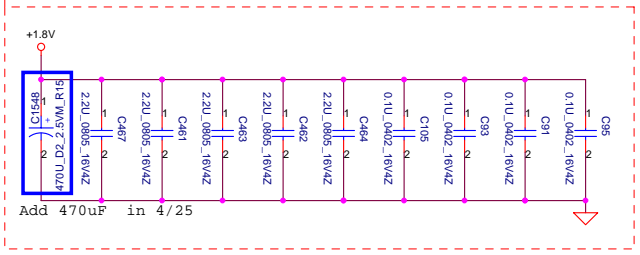
Compal Electronics, Inc.		
CRESTLINE((5/6)-PWR/GND		
Title	Document Number	Rev
	LA-3331P	1.0
Date:	Tuesday, May 15, 2007	Sheet 11 of 59



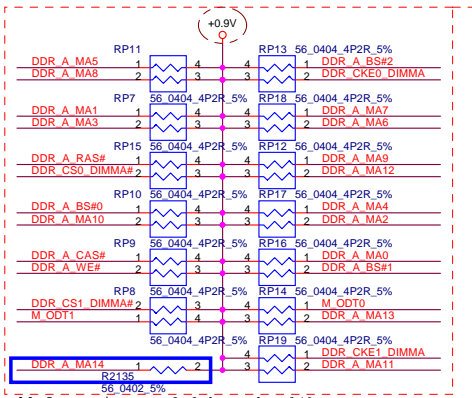
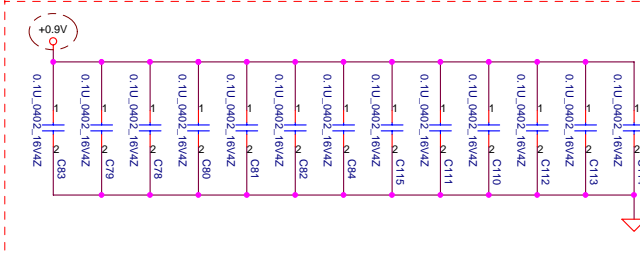
Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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Date:	Tuesday, May 15, 2007	Sheet	12 of 59	



Layout Note:
Place near JP9

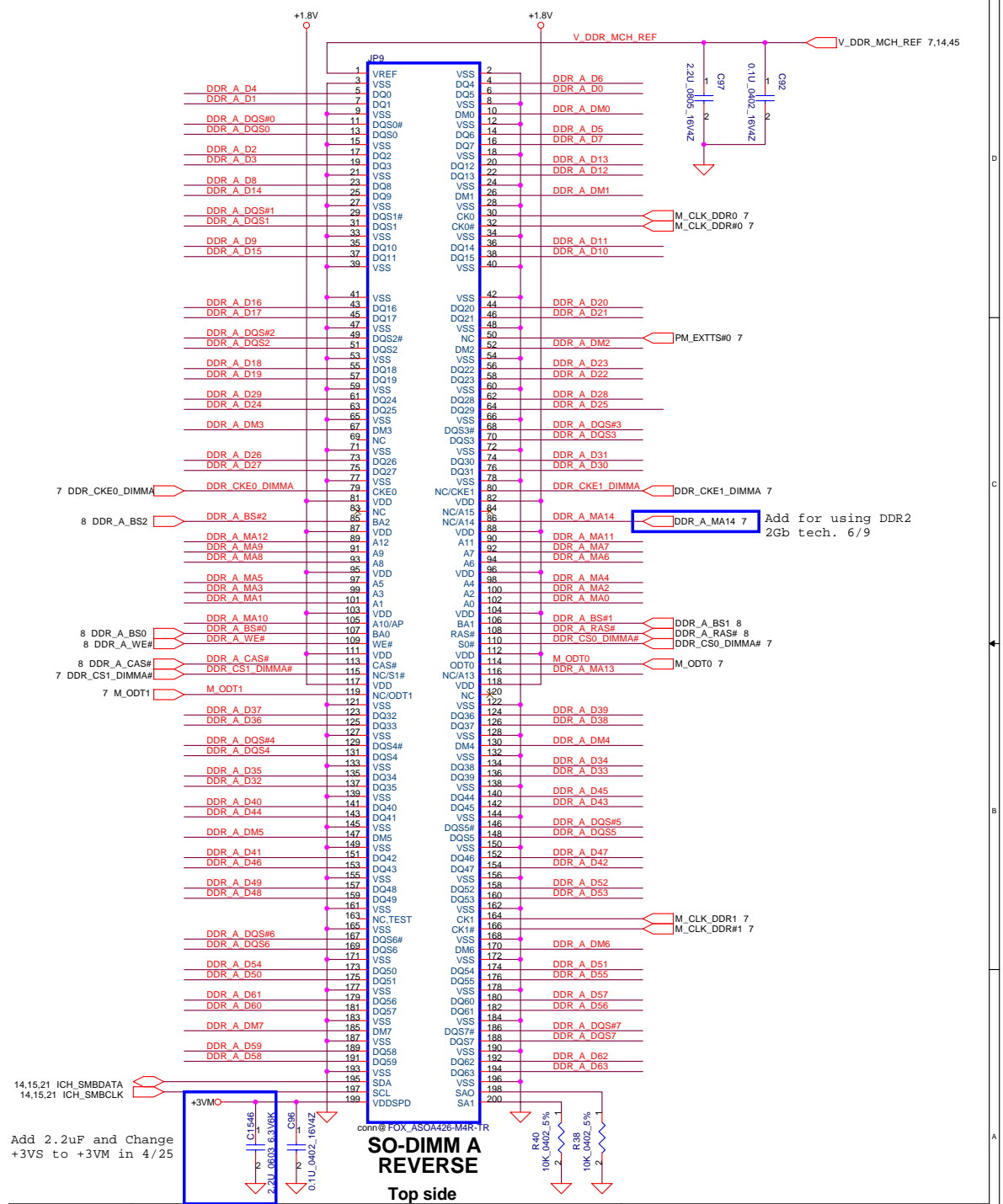


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP9, all trace length Max=1.5"

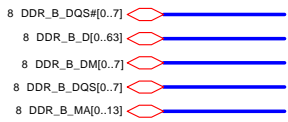
Add for using DDR2 2Gb Tech. 6/9



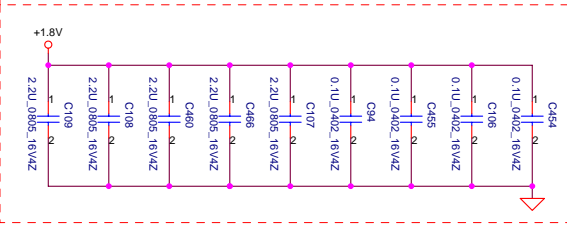
Add 2.2uF and Change +3VS to +3VM in 4/25

Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10

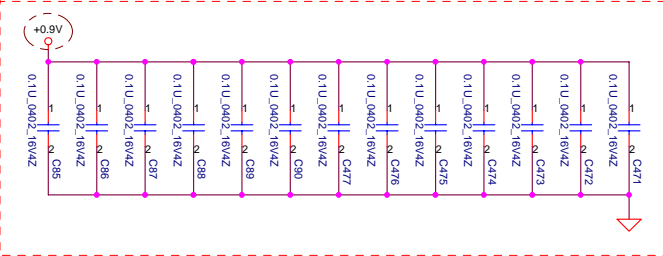
Title		Compal Electronics, Inc.	
		DDR2-SODIMM SLOT1	
Size	Document Number	Rev	
Custom	LA-3331P	1.0	



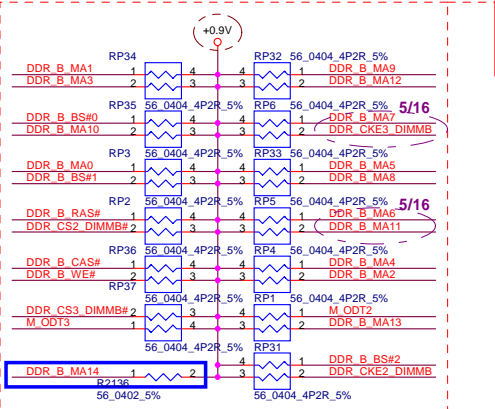
Layout Note:
Place near JP34



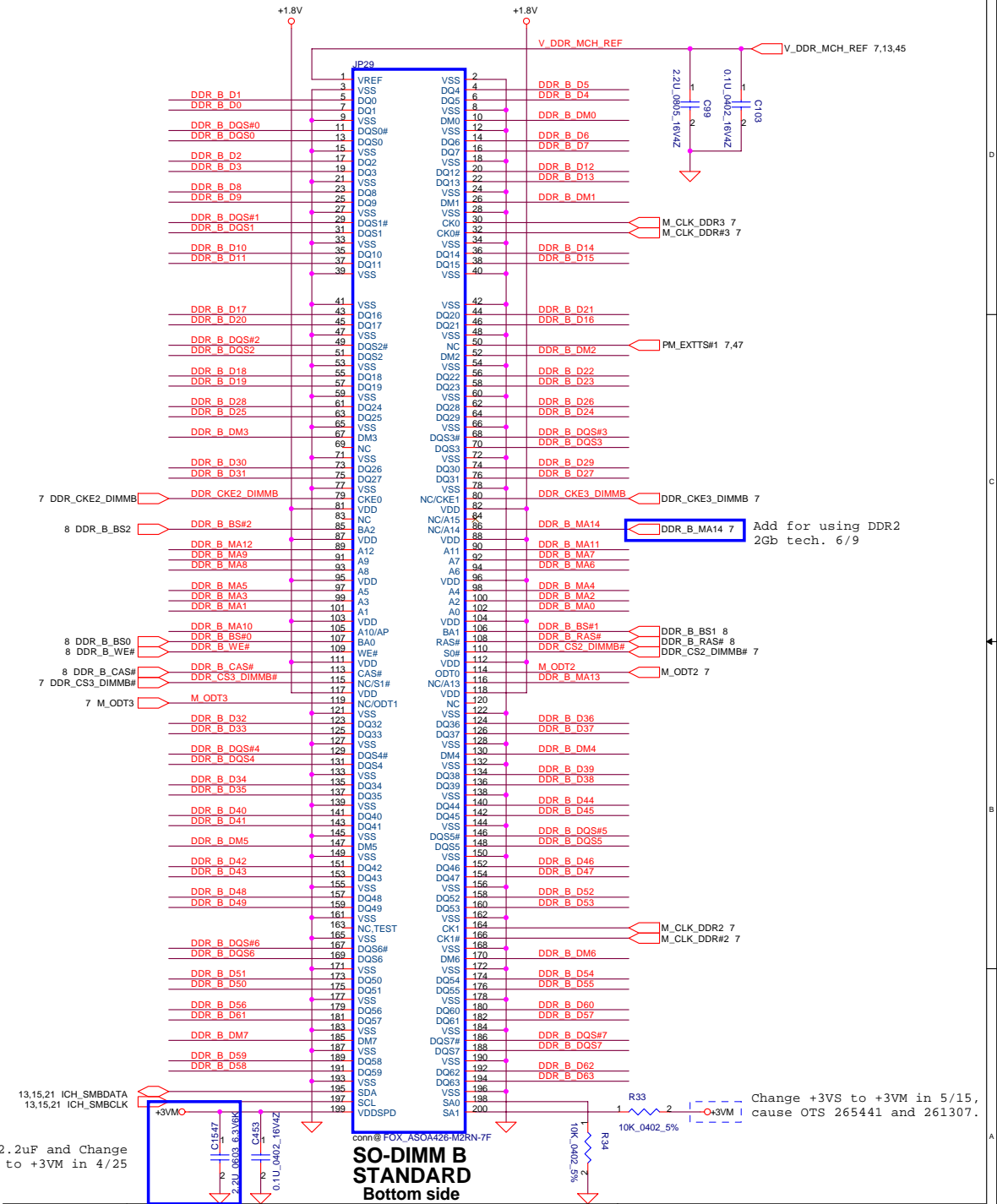
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



Add For using DDR2 2Gb tech. 6/9



Add 2.2uF and Change +3VS to +3VM in 4/25

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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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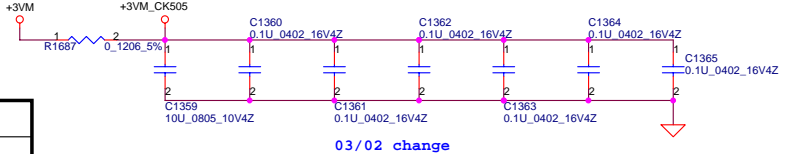
Title			
Compal Electronics, Inc.			
DDR2-SODIMM SLOT2			
Size	Document Number	Rev	
	LA-331P	1.0	
Date:	Tuesday, May 15, 2007	Sheet	14 of 59

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1694	R1716	R1734			
*(Default)	Yes	R1689	R1696	R1705	R1719	R1726	R1737
	No	R1689	R1696	R1734	R1737		
667MHz	Yes	R1689	R1696	R1734	R1737		
	No	R1694	R1705	R1716	R1719	R1726	
800MHz	Yes			R1734	R1737		
	No	R1689	R1694	R1696	R1705	R1716	R1726 R1719

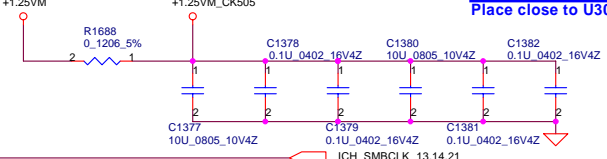
Removed C1366~C1368 4/30 (Same as Chimay)



03/02 change

Install R1688 4/28

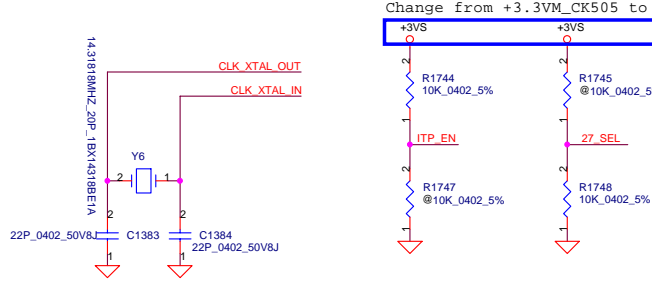
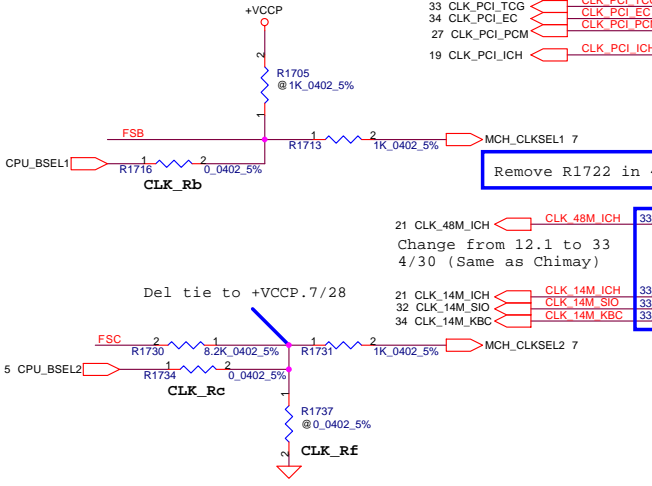
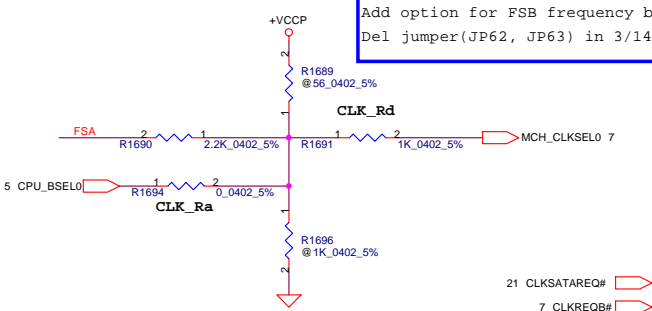
Del Q79 in 5/19.



Place close to U30

Add option for FSB frequency by jumper.11/08

Del jumper(JP62, JP63) in 3/14.



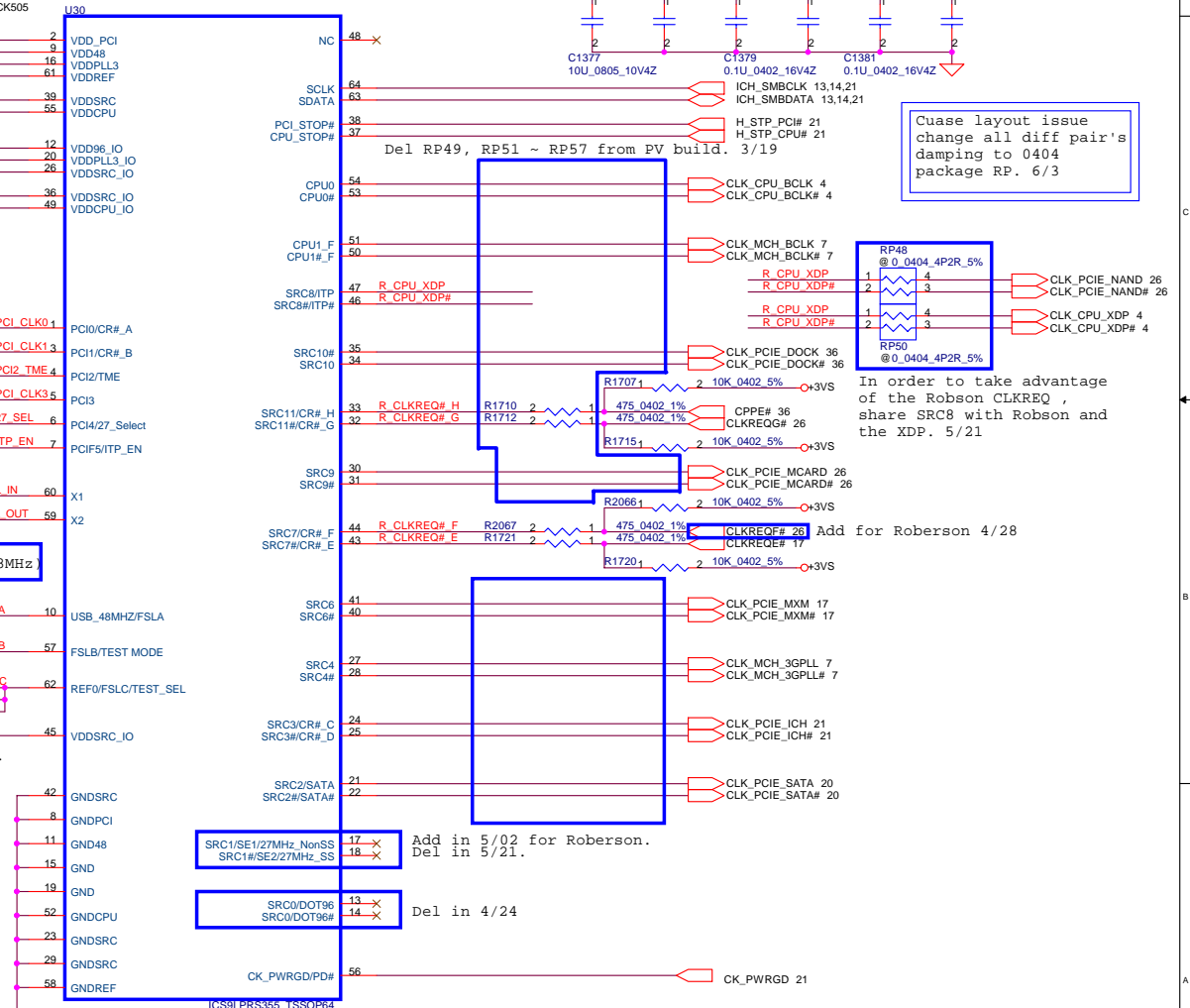
Remove R1722 in 4/24. (Richo don't need 48MHz)

Change from 12.1 to 33 4/30 (Same as Chimay)

Del tie to +VCCP.7/28

Modify at 5/14.

Change from +3.3VM_CK505 to +3VS. 6/9



Cause layout issue change all diff pair's damping to 0404 package RP. 6/3

In order to take advantage of the Robson CLKREQ, share SRC8 with Robson and the XDP. 5/21

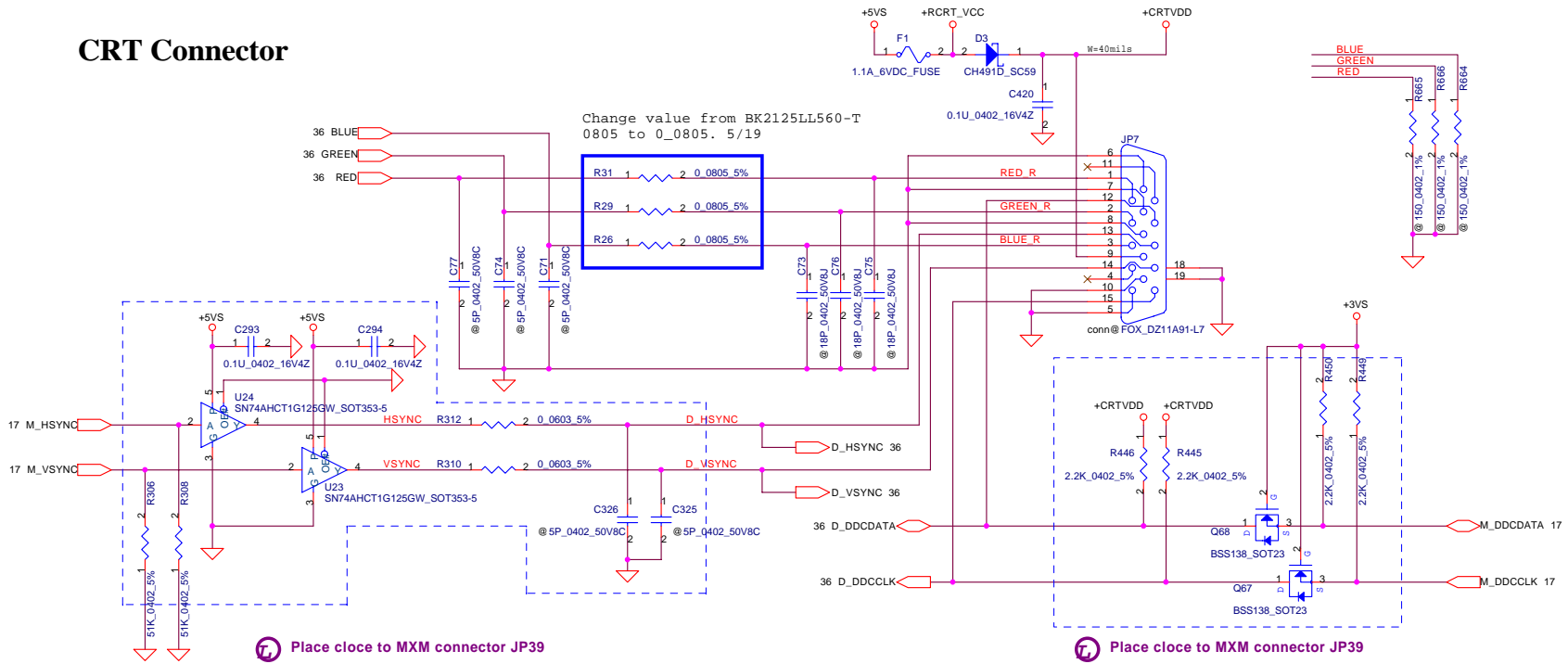
Add for Roberson 4/28

Add in 5/02 for Roberson. Del in 5/21.

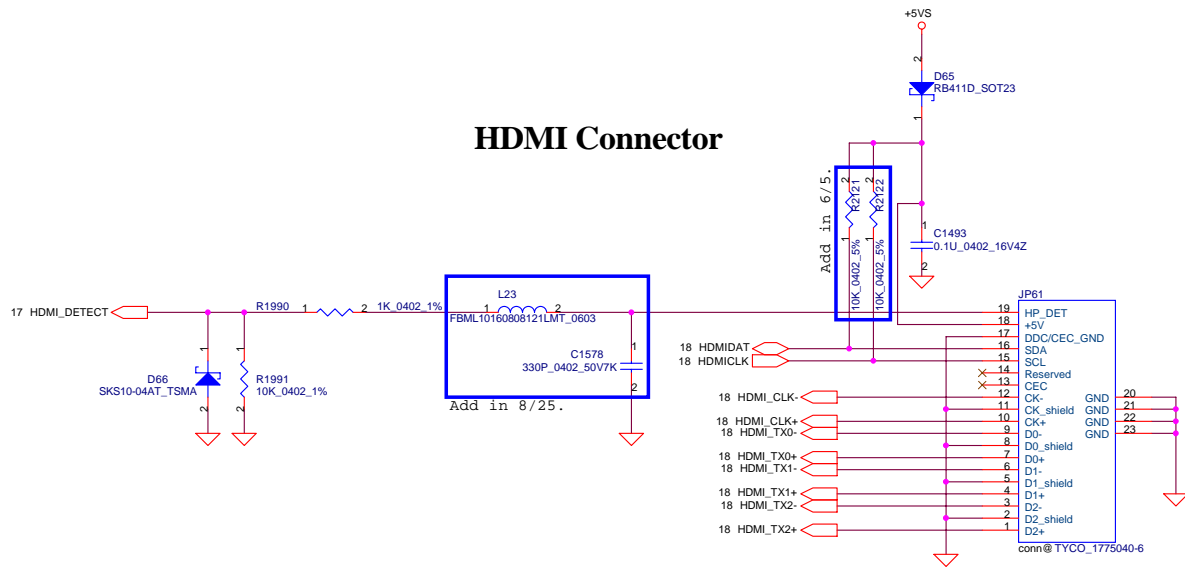
Del in 4/24

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	CLOCK GENERATOR	
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Size	Document Number	Date	Tuesday, May 15, 2007	Sheet	15 of 59
	LA-333IP				Rev 1.0

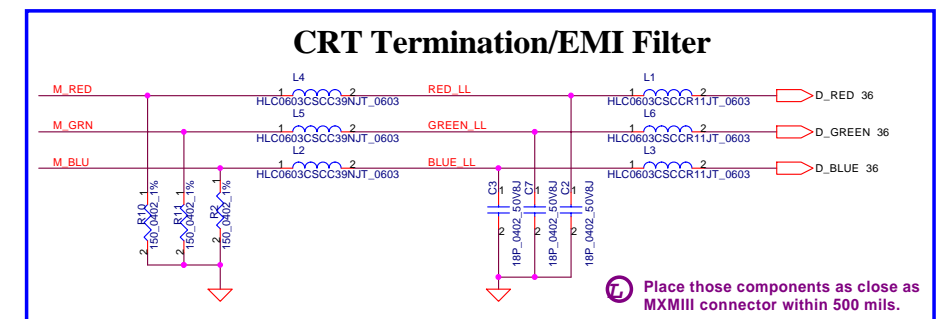
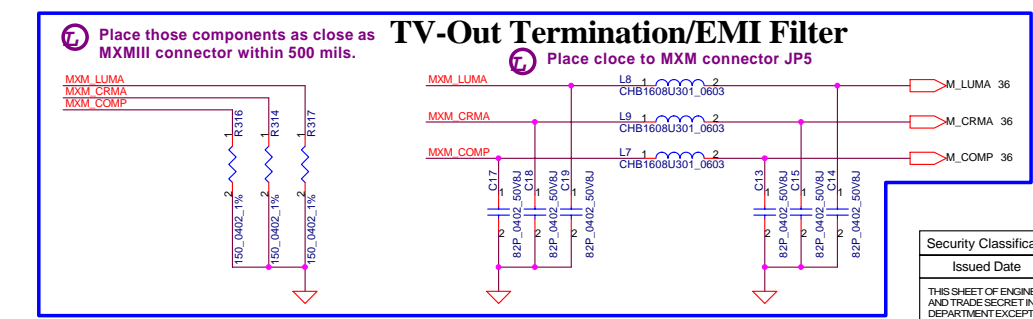
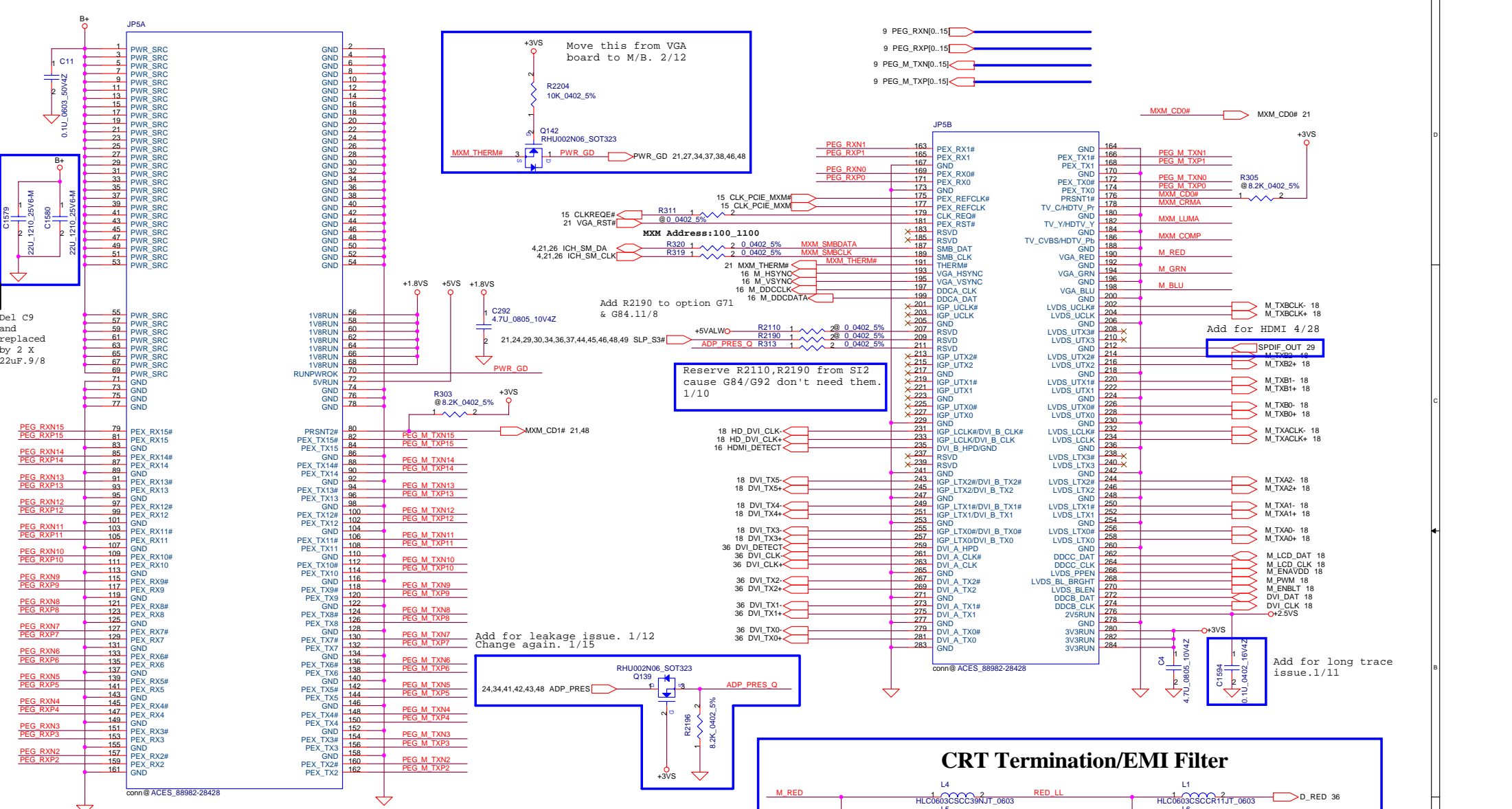
CRT Connector



HDMI Connector

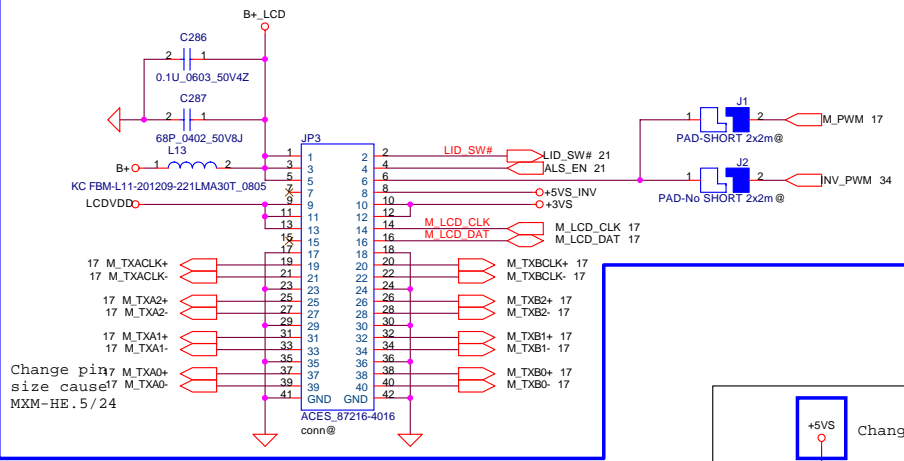


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			Date:	LA-333IP	1.0
			Tuesday, May 15, 2007	Sheet	16 of 59

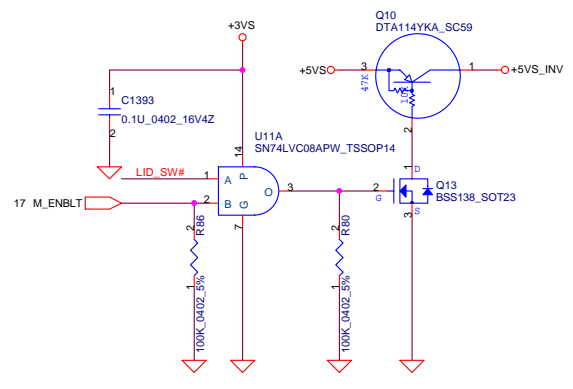
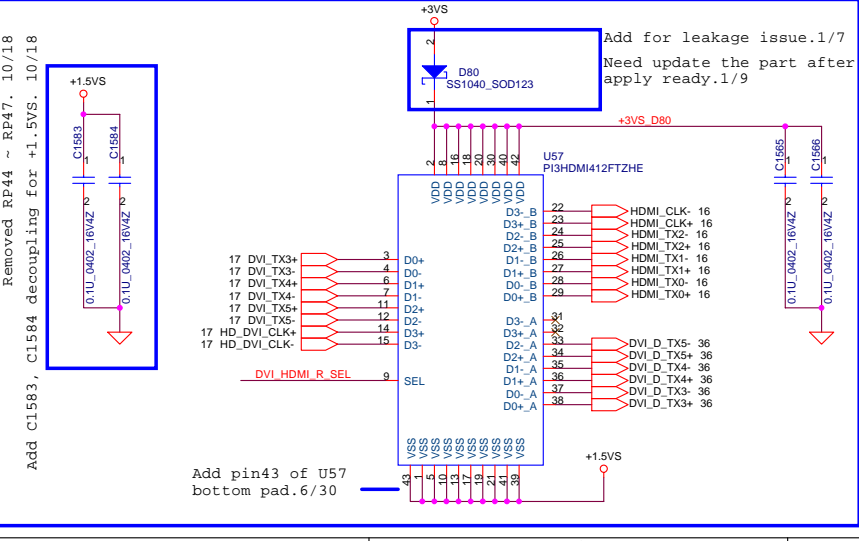
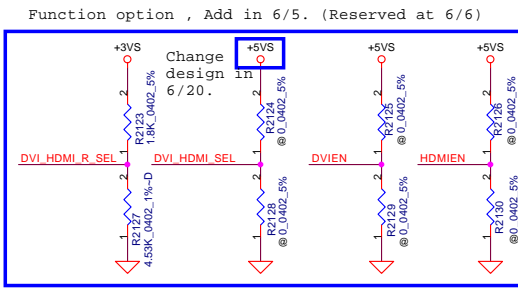
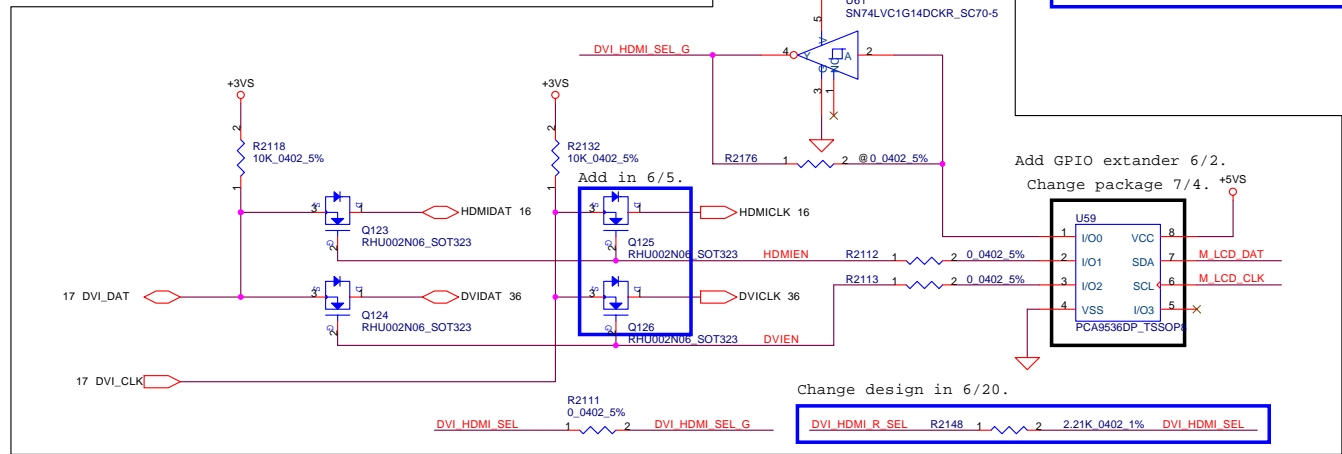
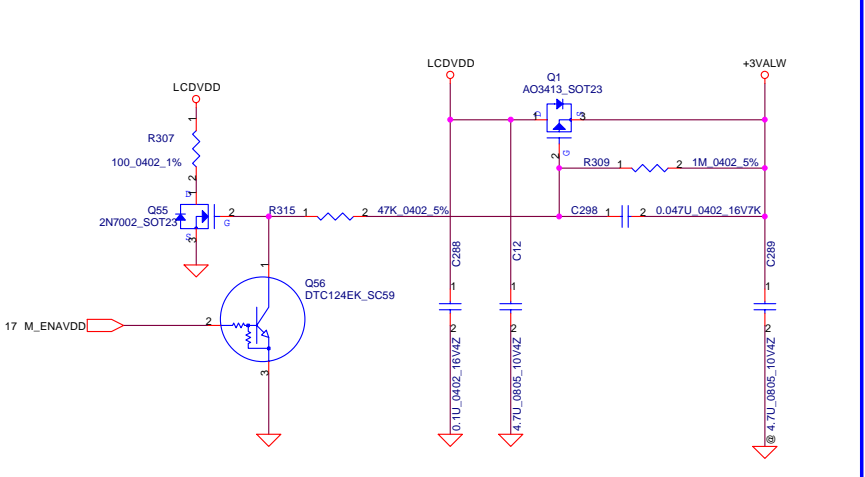


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Date:	Tuesday, May 15, 2007	Sheet	17	of	59
Size	Document Number	Rev			
	LA-333IP	1.0			

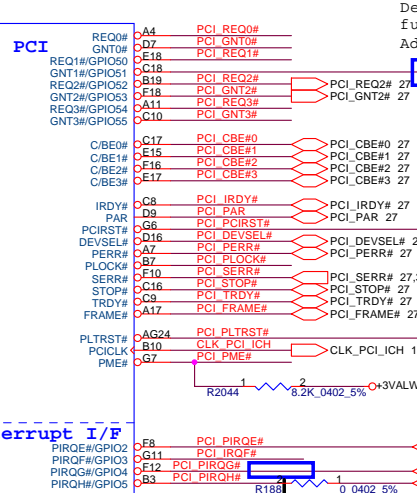
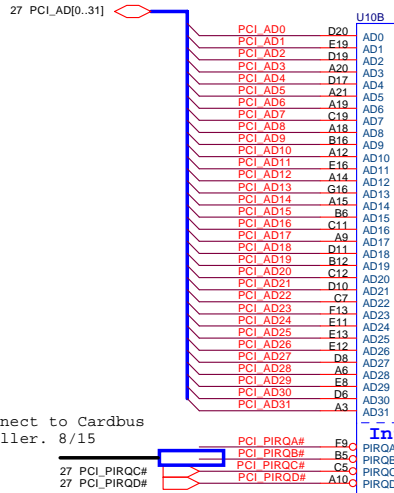
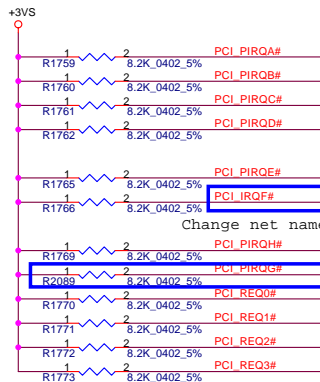
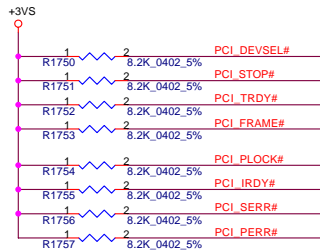
MXM LVDS CONN



LCD POWER CIRCUIT



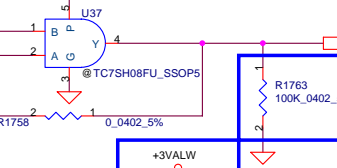
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	LCD CONN & Q-Switch & GPIO Ext.
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Date:	Tuesday, May 15, 2007	Sheet	18	of 59



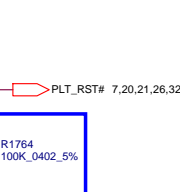
Del Modem disable function in 6/21. Add in 6/15.



Change design to same as Chimay. 5/10



Change design to same as Chimay. 5/10



Change design to same as Chimay. 5/10

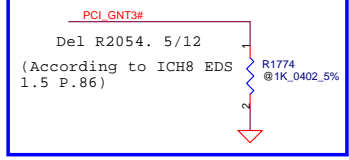
Change design to same as Chimay 5/5. Change design, move LANLINK_STATUS# to GPIO1. Connect to Richo chip. 8/15

Change net name. 5/10

This pin is OD pin, so add PU. 5/16
Reserved R2089 6/2
Installed R2089. 6/5

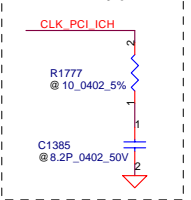
Removed R1767, R2053 5/5.

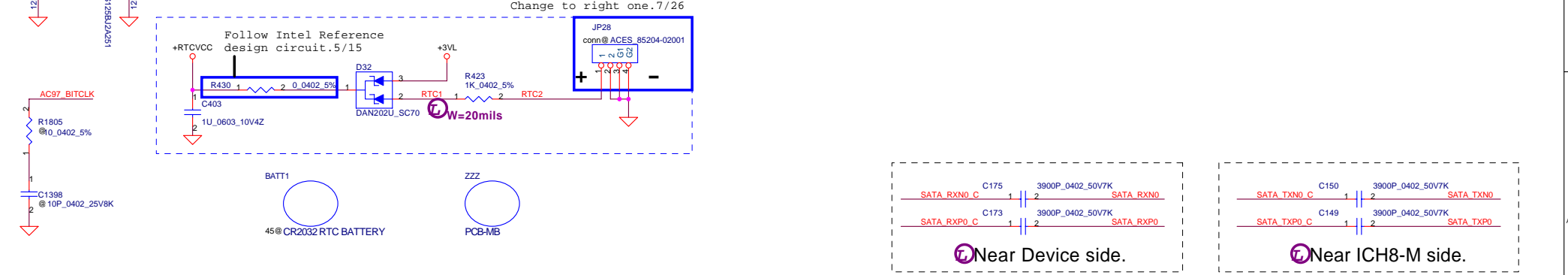
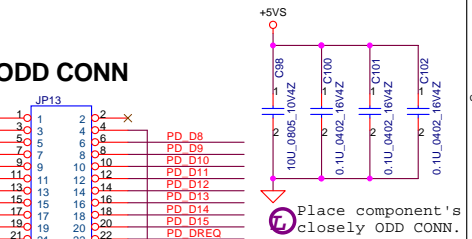
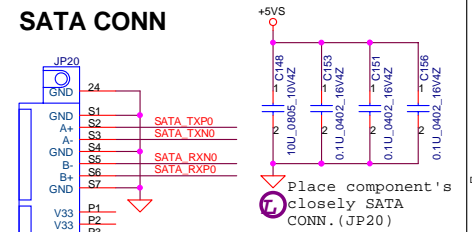
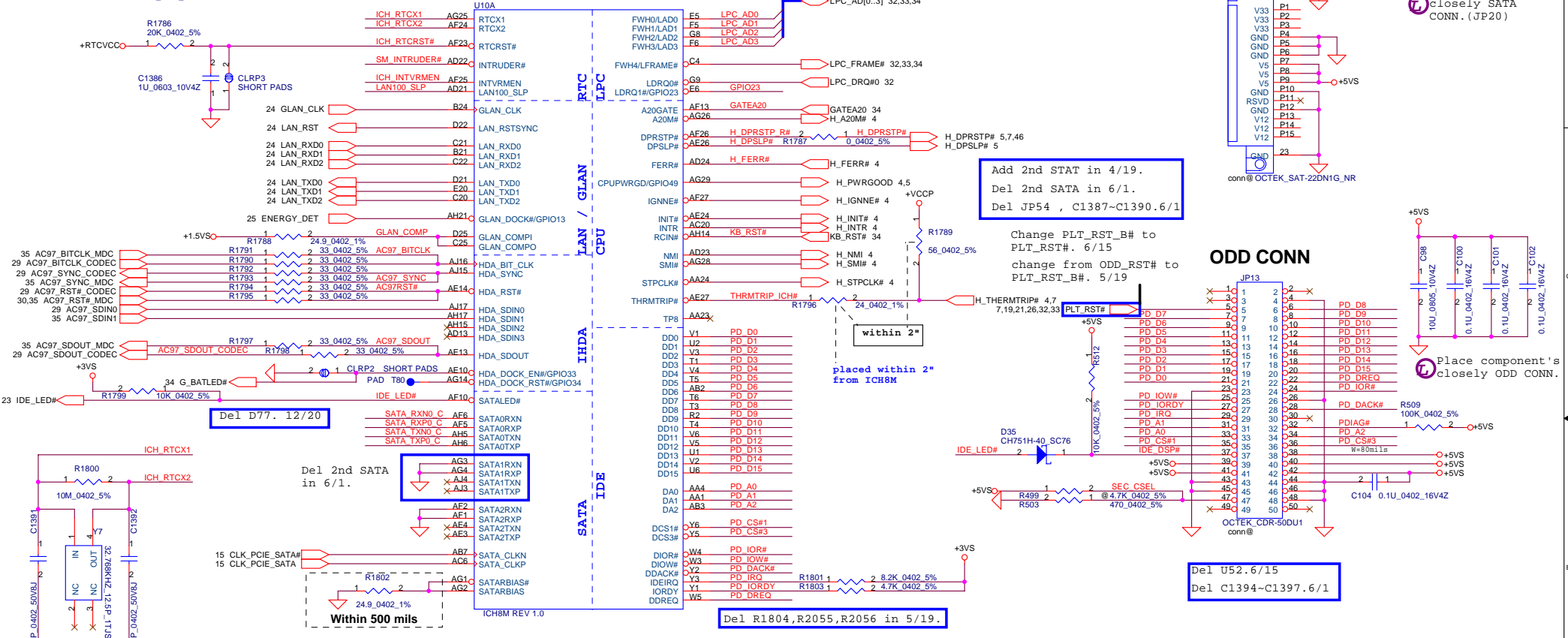
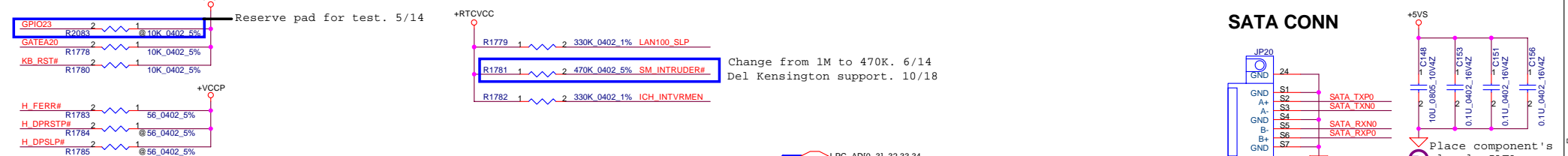
A16 swap override Strap
Low= A16 swap override Enable
High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

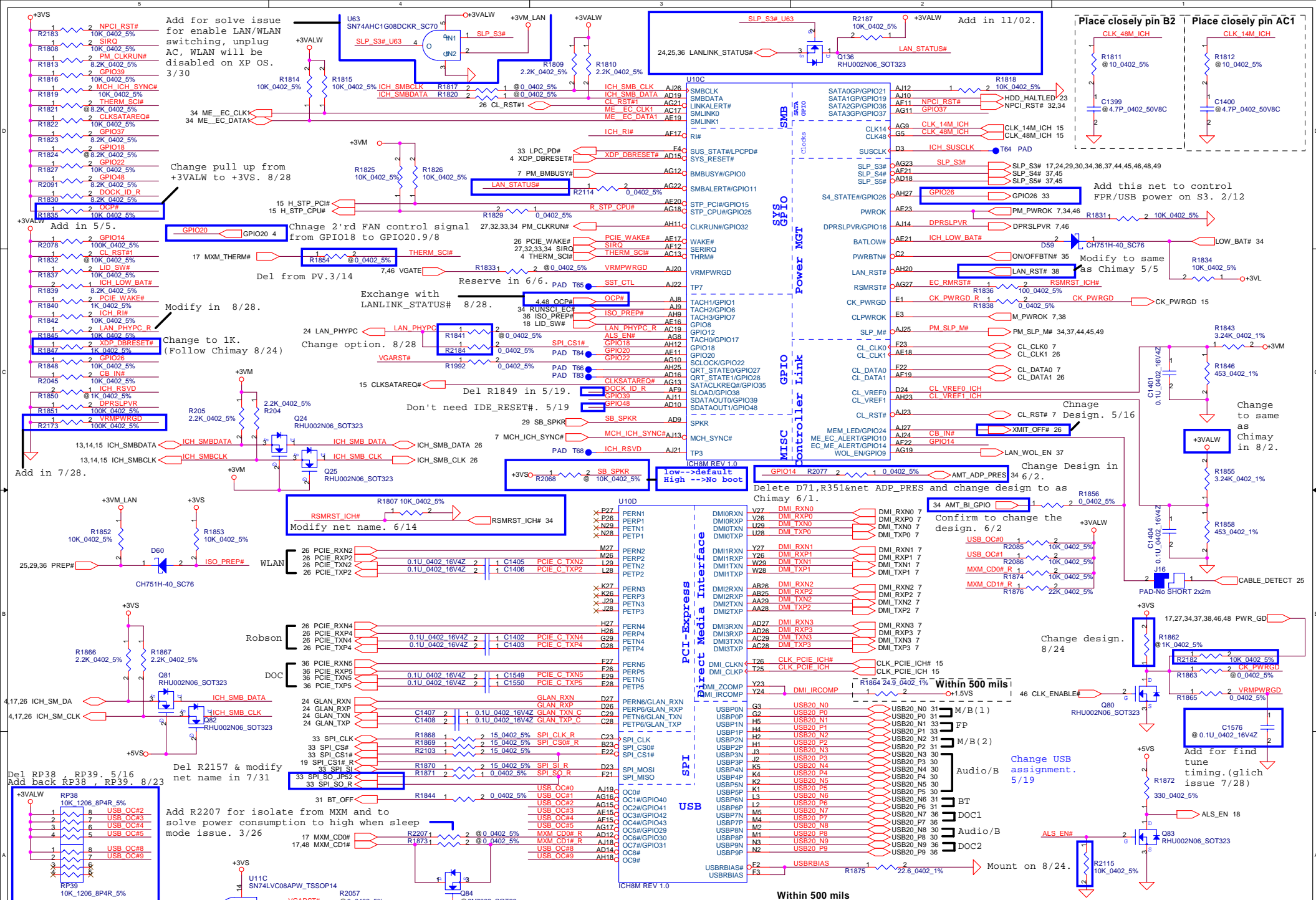
Place closely pin B10





XOR CHAIN ENTRANCE STRAP:RSVD

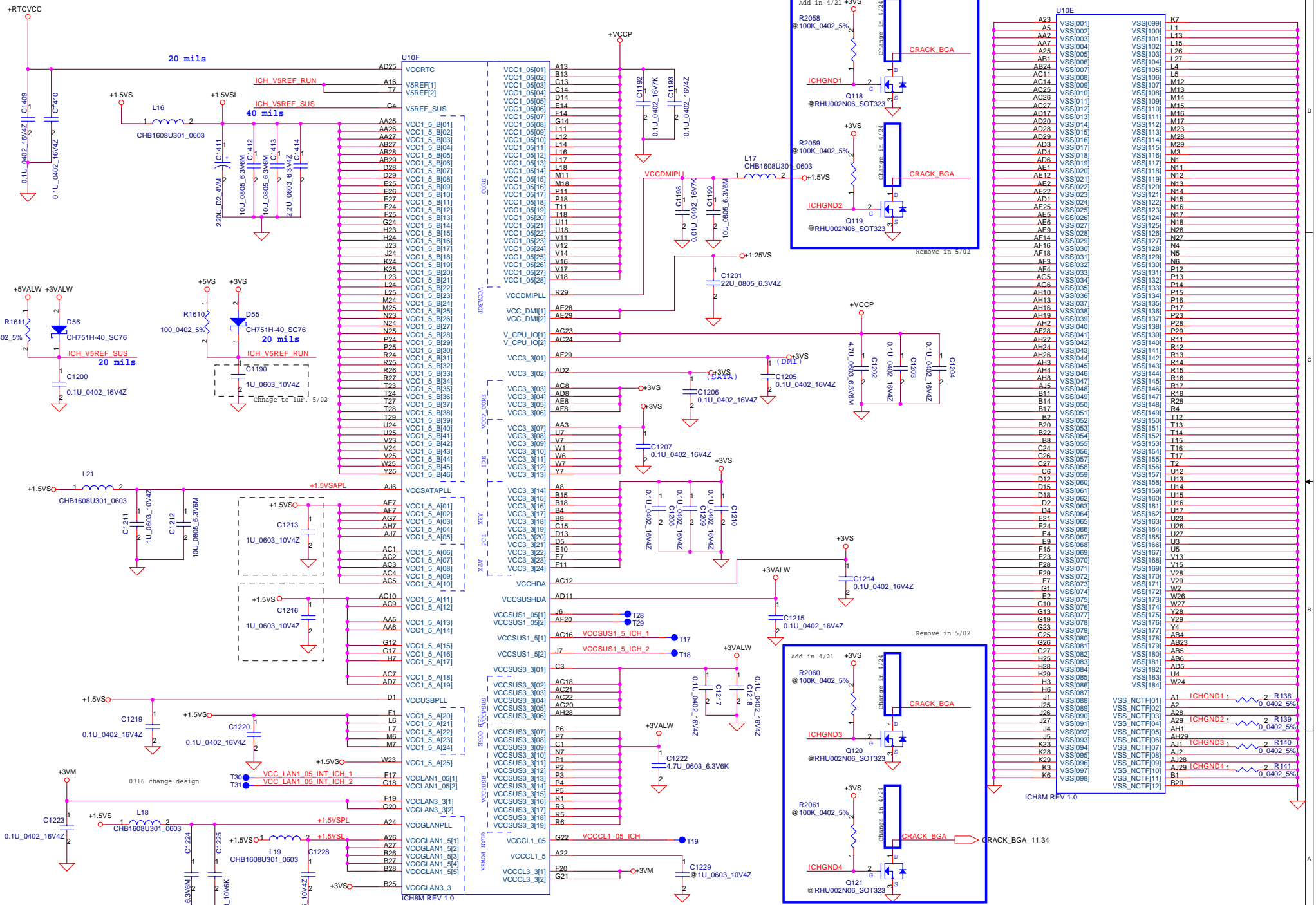
Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	ICH8(2/4) LAN,HD,IDE,LPC
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Size	Document Number	Rev	Date	
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Issued Date	2006/02/13	Deciphered Date
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Compal Electronics, Inc.		
ICH8(3/4) PM,USB,GPIO		
Size	Document Number	Rev
Custom	LA-331P	1.0
Date:	Tuesday, May 15, 2007	Sheet 21 of 59

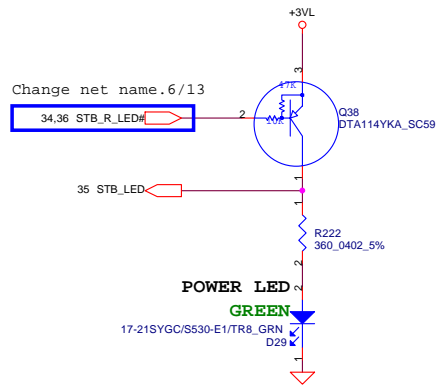
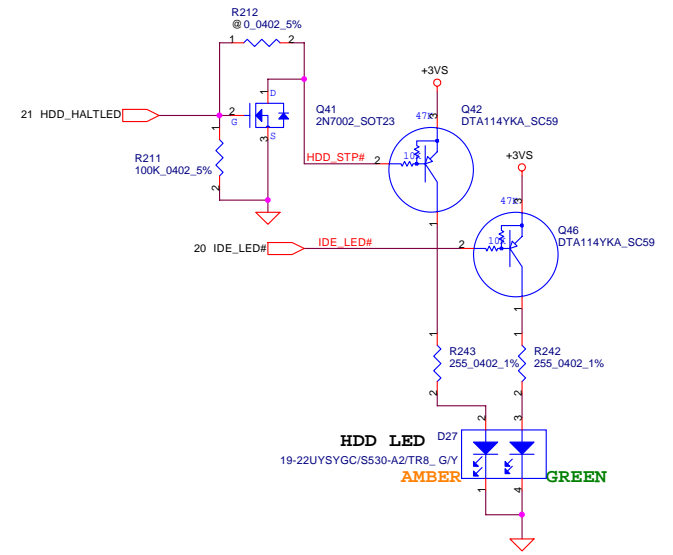
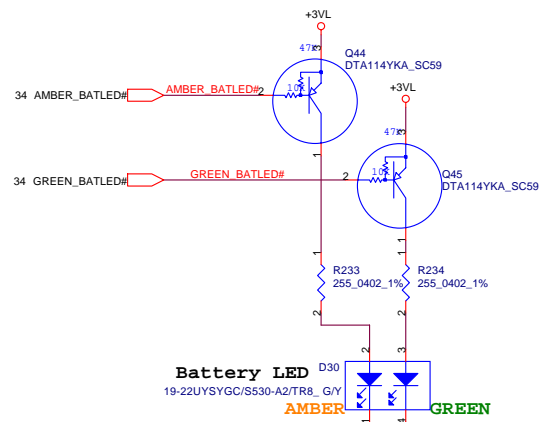
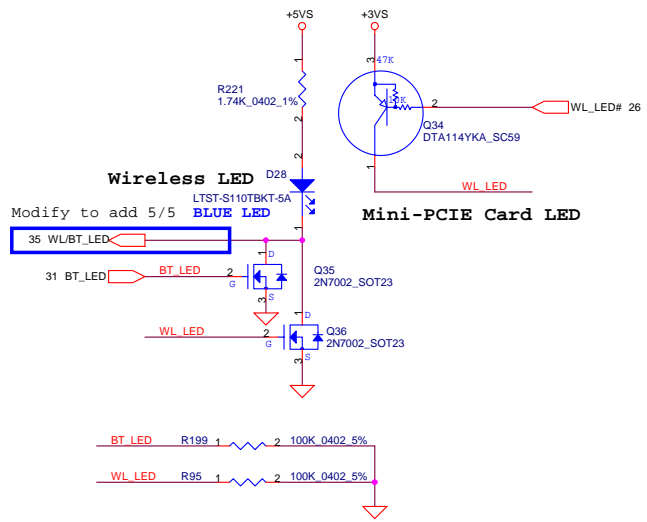
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		2006/03/10

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Title		
Compal Electronics, Inc.		
ICH8(4/4) POWER&GND		
Size	Document Number	Rev
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Del R2109. 6/14
 Add the kill circuit. 5/25
 Update design. 5/14
 Reserved Space for Kensington 4/27
 Removed Kensington 10/18.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Title			Compal Electronics, Inc.	
Size			LEDS & Kensington	
Custom	Document Number	Rev		
	LA-333IP	1.0		
Date:	Tuesday, May 15, 2007	Sheet	23	of 59

ACBS support :
Mount Q85, R2072.
Remove Q87, Q88, R1877

Remove Q90 and C1436 ~ C1440. 3/28

Follow Design Guide in 6/11.

Change design 5/01 (Follow Chimay)
Change design. 5/14(Intel check result)

EMI request to add for 150MHz/200MHz
issue close to U25.1/4

Add in 5/17.(Follow DG P.430)

Cause something wrong , add 1V
supply back. 5/14

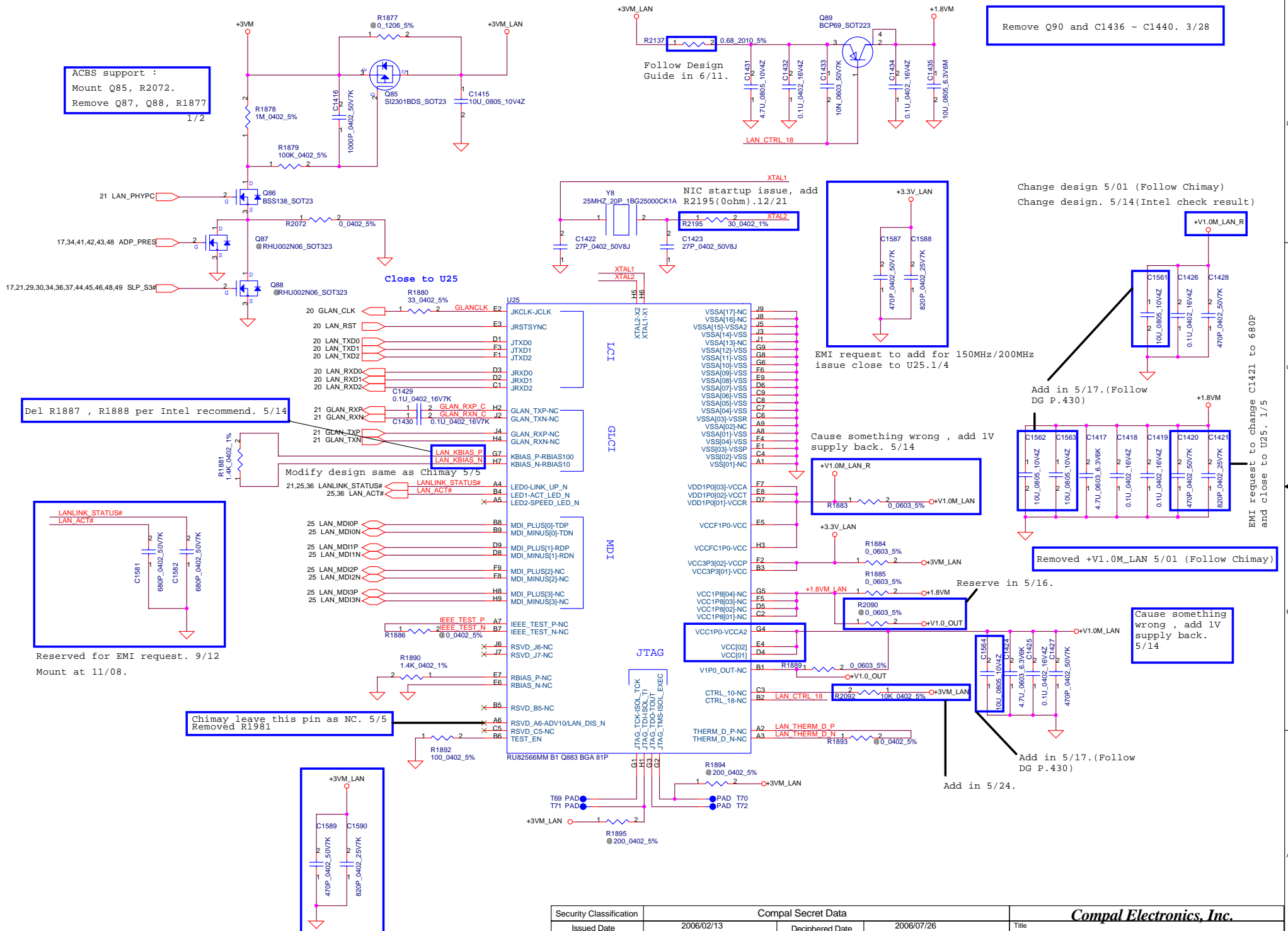
Removed +V1.0M_LAN 5/01 (Follow Chimay)

Cause something wrong , add 1V
supply back. 5/14

Add in 5/17.(Follow DG P.430)

Add in 5/24.

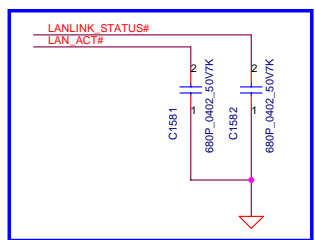
EMI request to change C1421 to 680P
and close to U25. 1/5



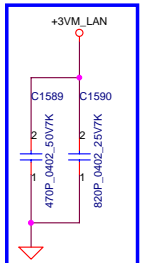
Del R1887 , R1888 per Intel recommend. 5/14

Modify design same as Chimay 5/5

Chimay leave this pin as NC. 5/5
Removed R1981

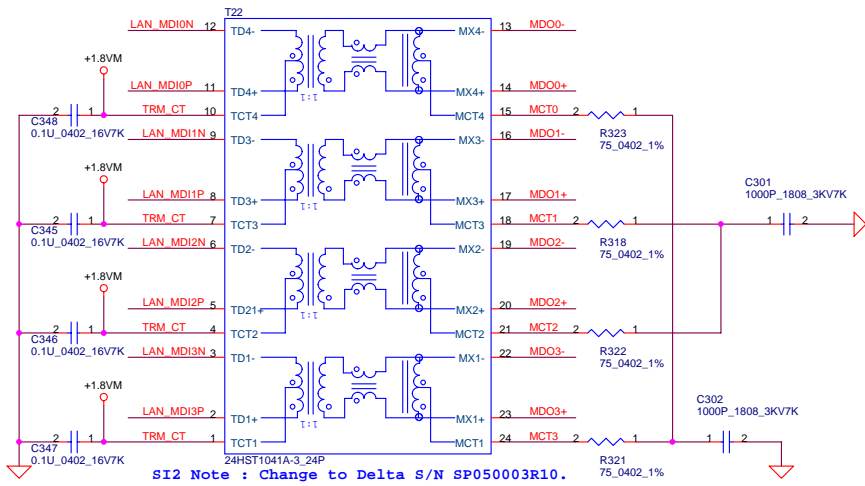


Reserved for EMI request. 9/12
Mount at 11/08.

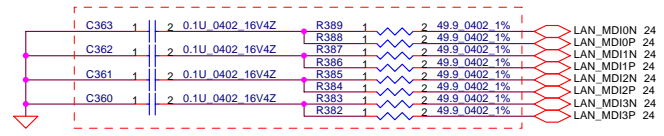


EMI request to add for 150MHz/200MHz
issue close to R1894.1/4

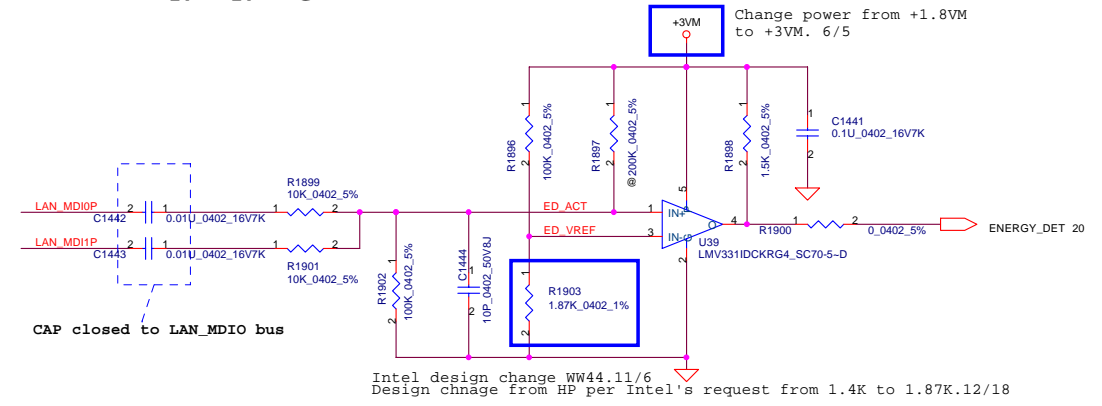
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Compal Electronics, Inc.
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Size	Document Number	Date	Sheet	Rev
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Layout Notice : Place termination as close as Intel 82566 as possible

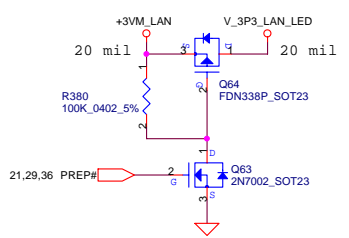
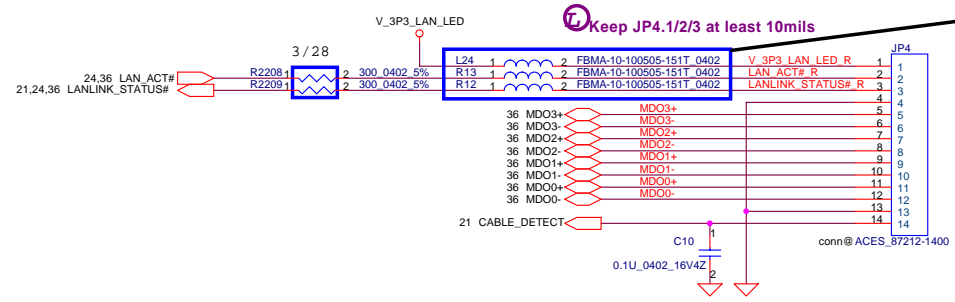


LAN ENERGY DET



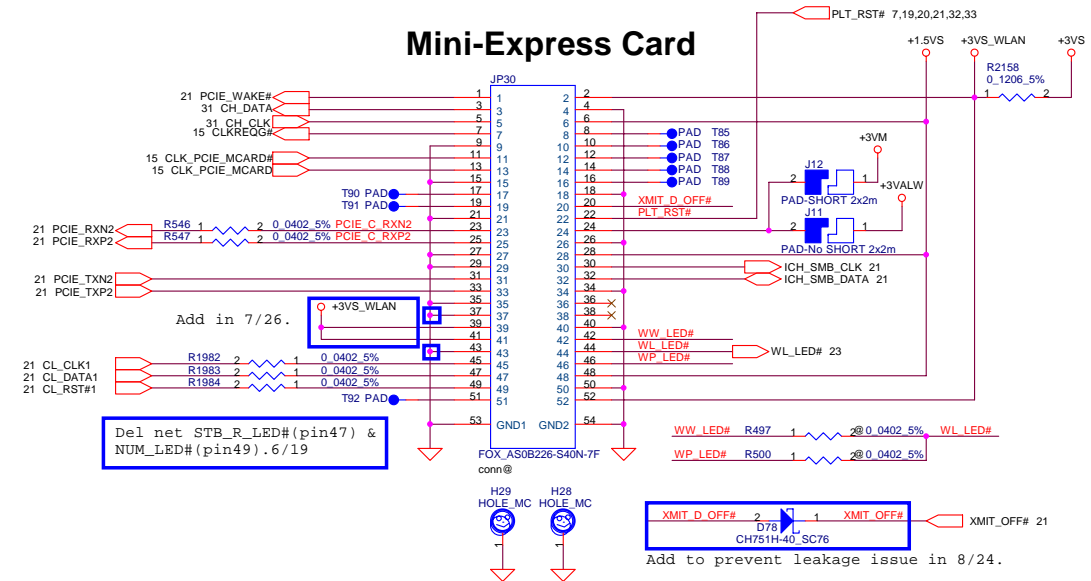
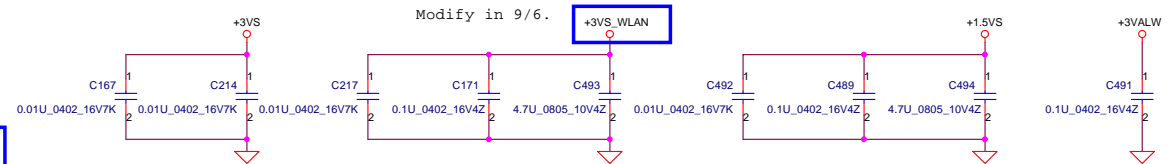
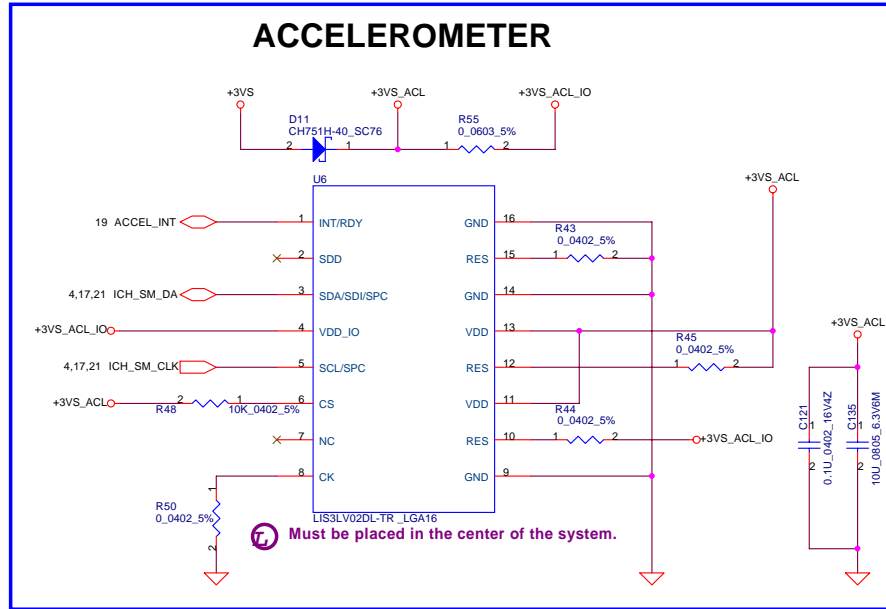
To RJ-45 CONN.

- EMI request :
1. Add L24 and C1591.
 2. Change R12~R13 to FBMA-10-100505-151T_0402.
 3. Add R2208, R2209 to have current limit for E-star. 3/28



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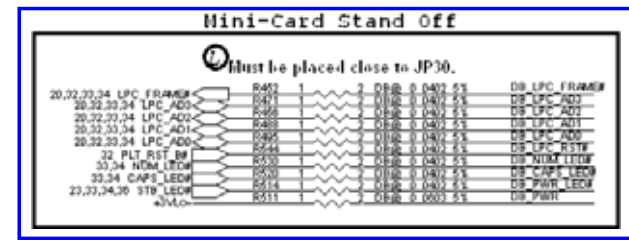
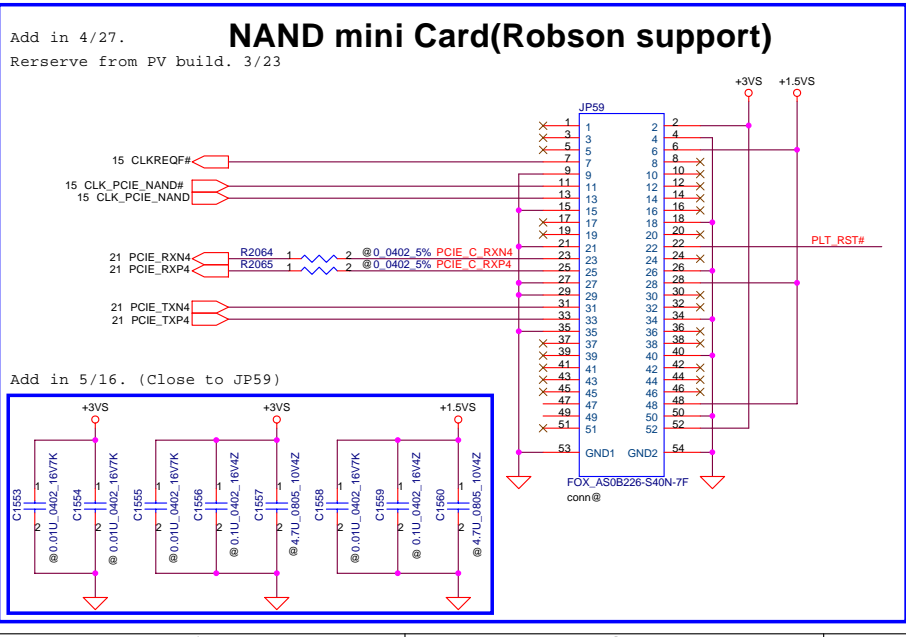
Change U6 to same as Chimay. 7/27



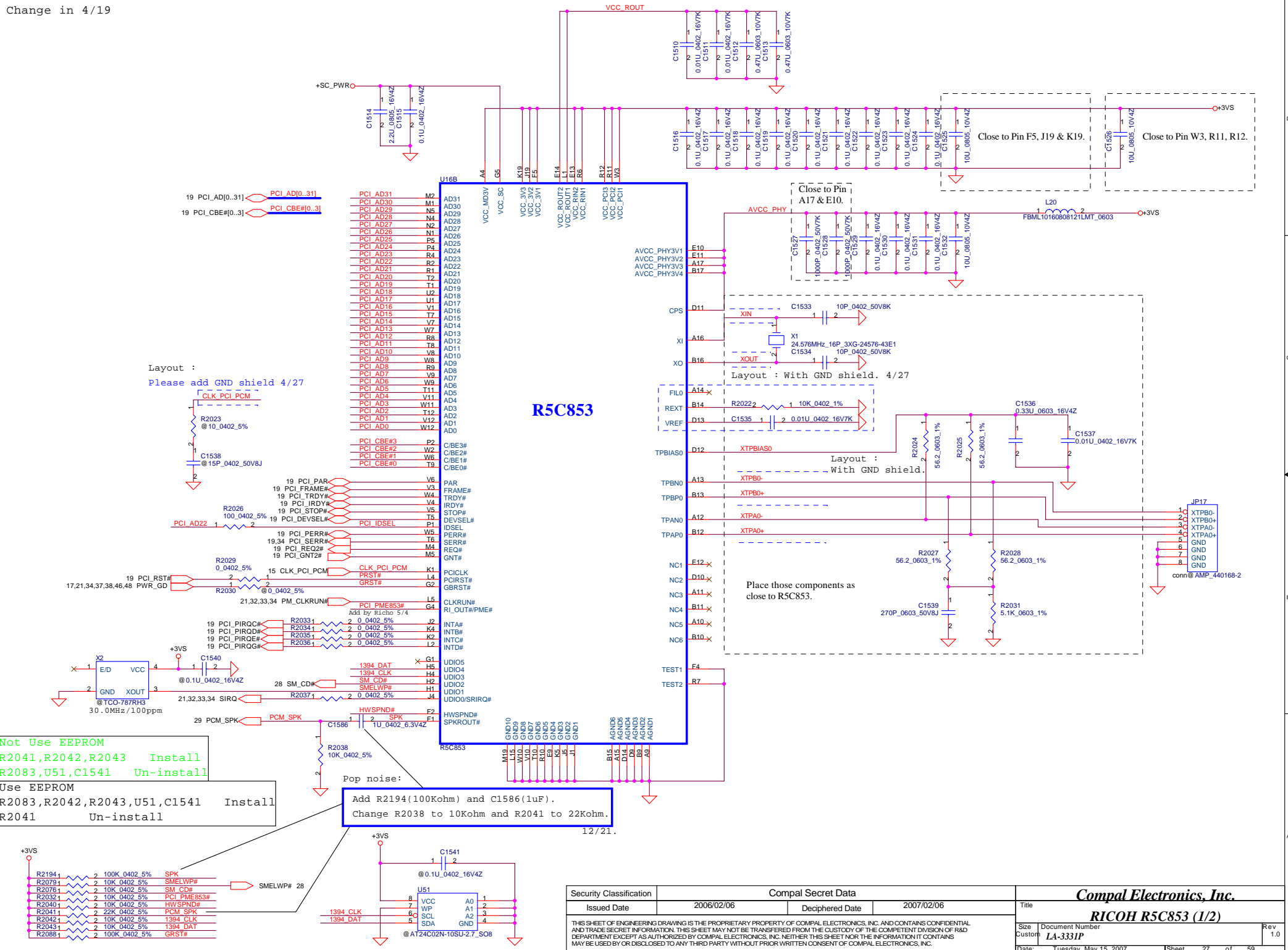
Change Design , Del R92 , R104 , R112 , Q17. 5/16

Del +3VL from JP30 pin 45. 6/15
Del net of JP30 pin 8, 10, 12, 14, 16, 17, 19, 51. 6/15

Del resistors & bypass all net as shown in below picture. 5/24



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Layout :
Please add GND shield 4/27

R5C853

Not Use EEPROM
R2041, R2042, R2043 Install
R2083, U51, C1541 Un-install

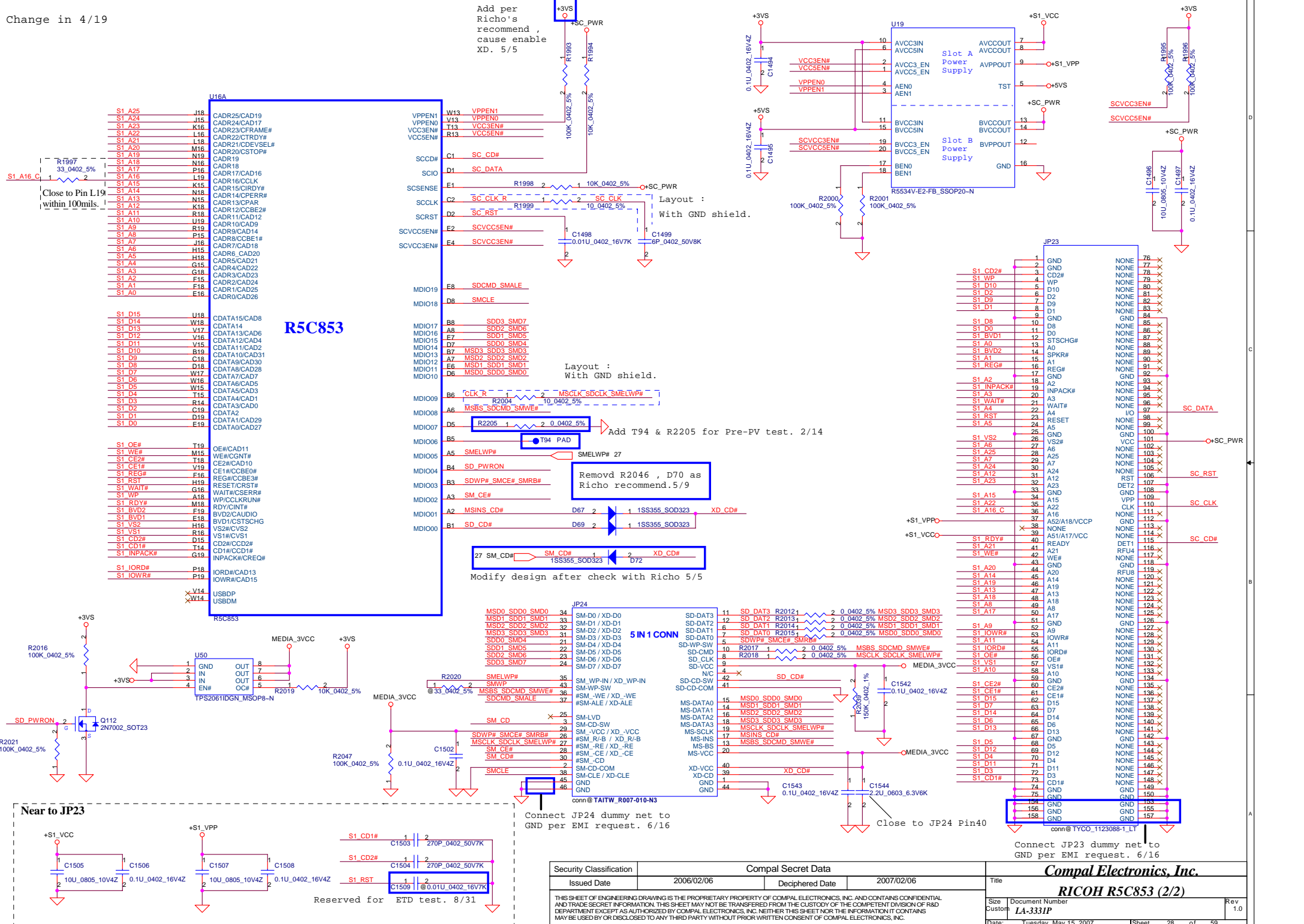
Use EEPROM
R2083, R2042, R2043, U51, C1541 Install
R2041 Un-install

Pop noise:
Add R2194(100Kohm) and C1586(1uF).
Change R2038 to 10Kohm and R2041 to 22Kohm.

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		2007/02/06

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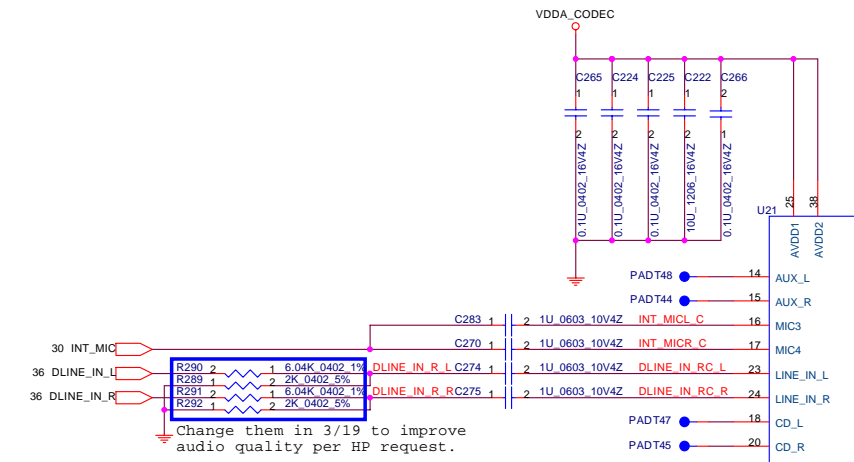
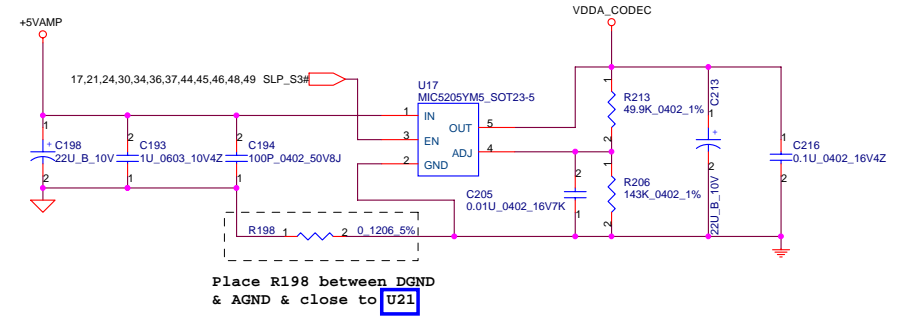
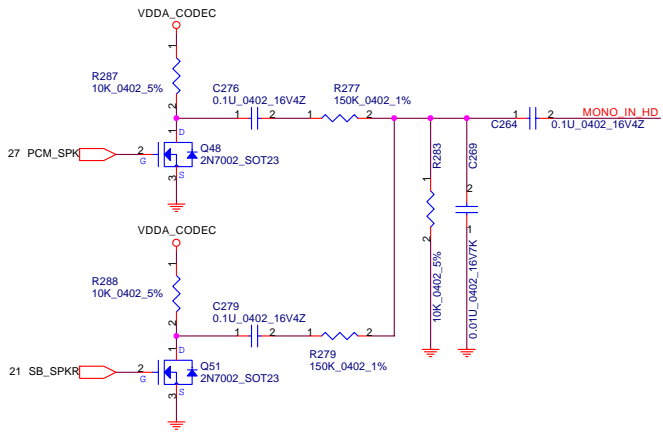
Compal Electronics, Inc.		
RICOH R5C853 (1/2)		
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Security Classification	Compal Secret Data	
Issued Date	2006/02/06	Deciphered Date
		2007/02/06

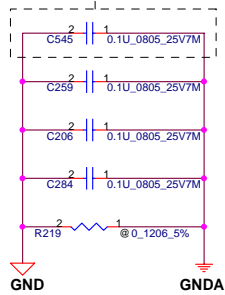
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Compal Electronics, Inc.			Tuesday, May 15, 2007		
RICOH R5C853 (2/2)			Sheet 28 of 59		
Size	Document Number	Rev			
Custom	LA-333IP	1.0			

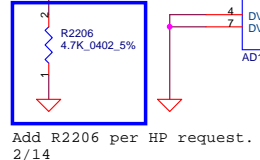


Change them in 3/19 to improve audio quality per HP request.

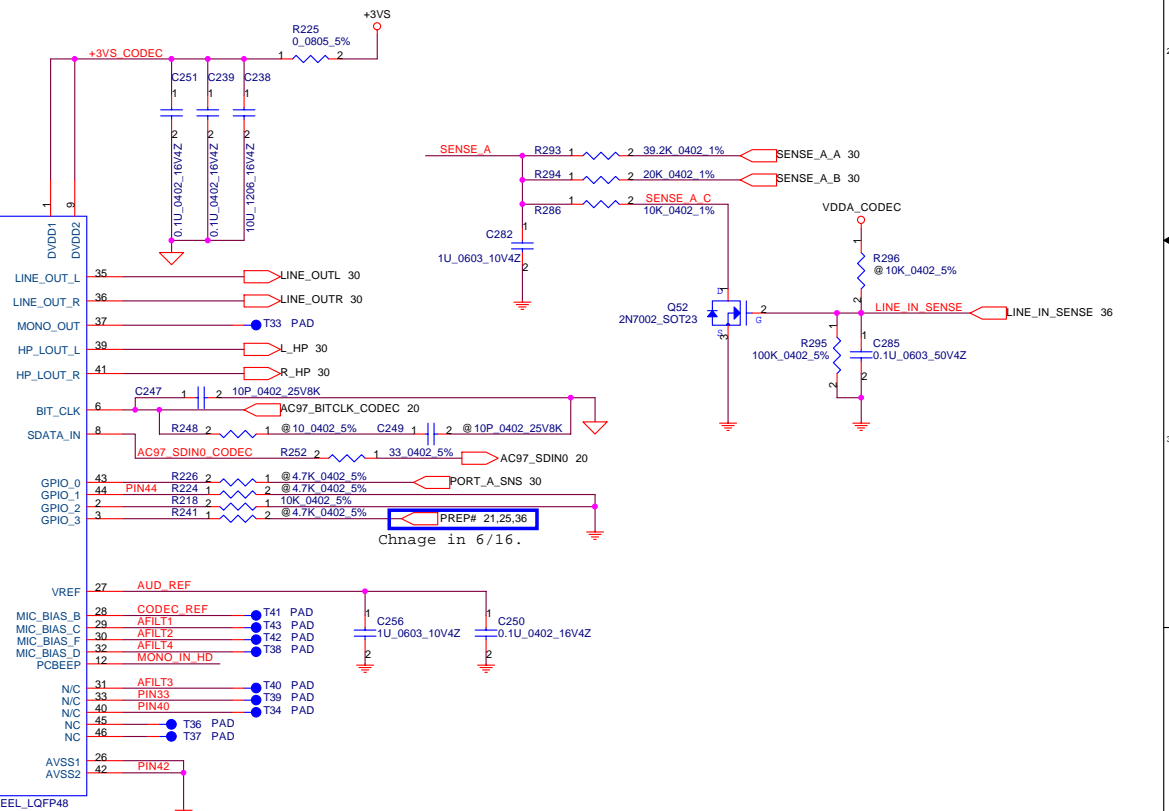
Place close to U14



Add for HDMI to MXM Conn 4/27



Add R2206 per HP request. 2/14

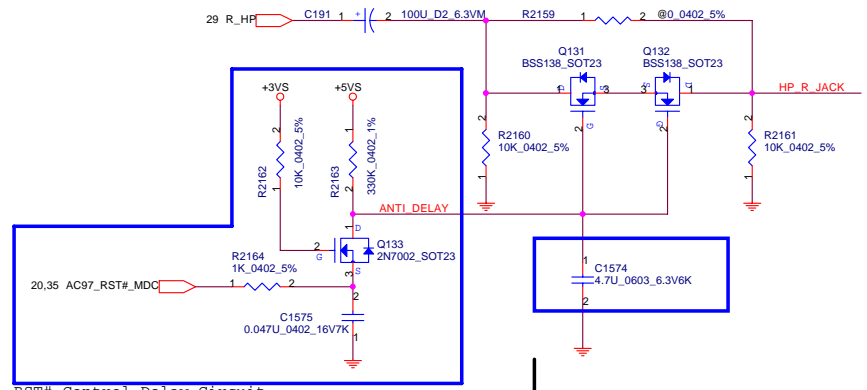
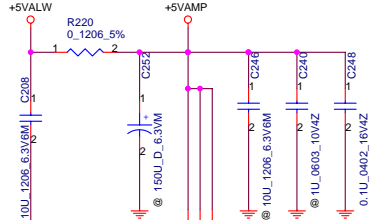
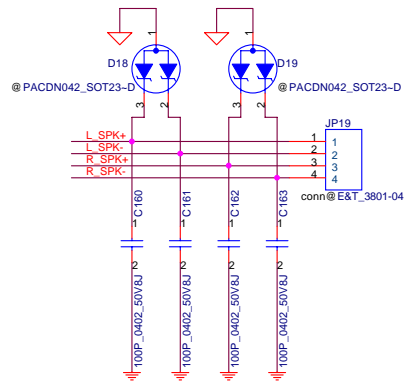


Chnage in 6/16.

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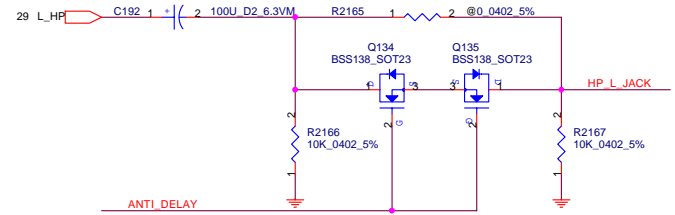
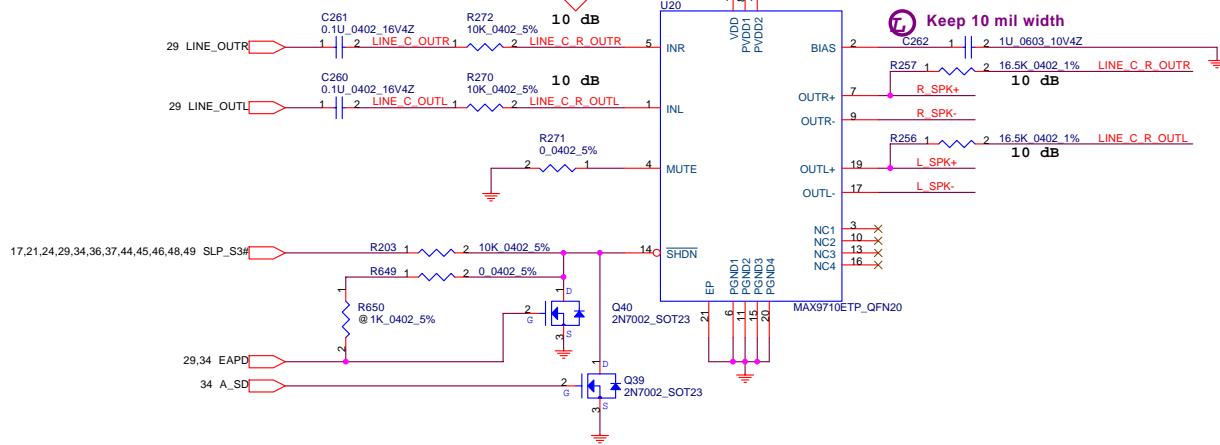
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Compal Electronics, Inc.			
AC97 CODEC AD1981HD			
Size	Document Number	Rev	
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AMP. FOR INTERNAL SPEAKER

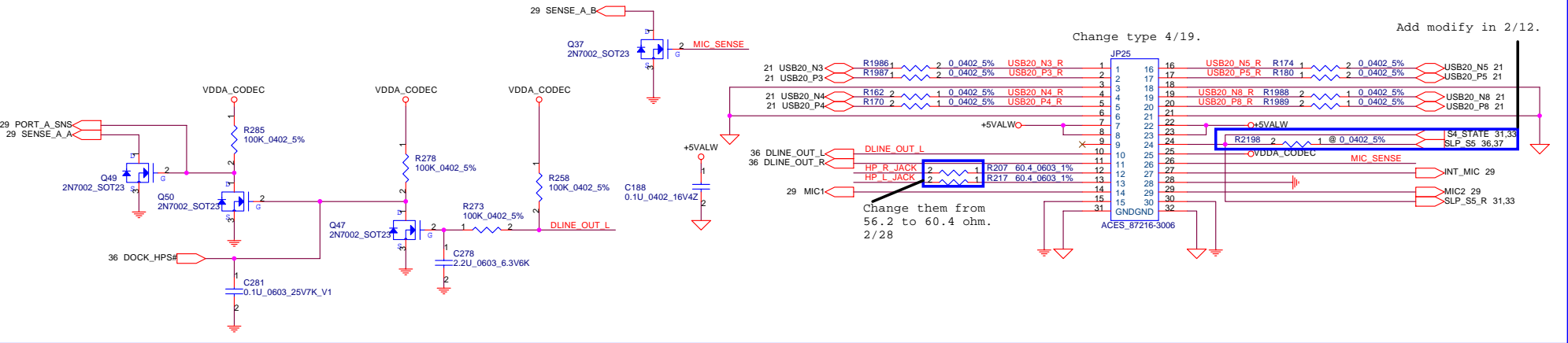


RST# Control Delay Circuit

ANTI POP Circuit (Add in 7/26)



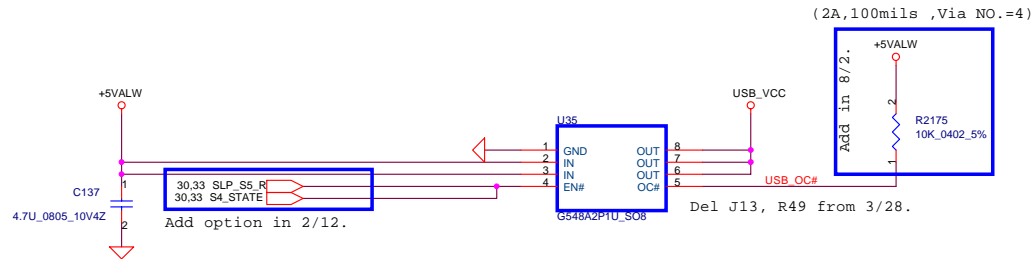
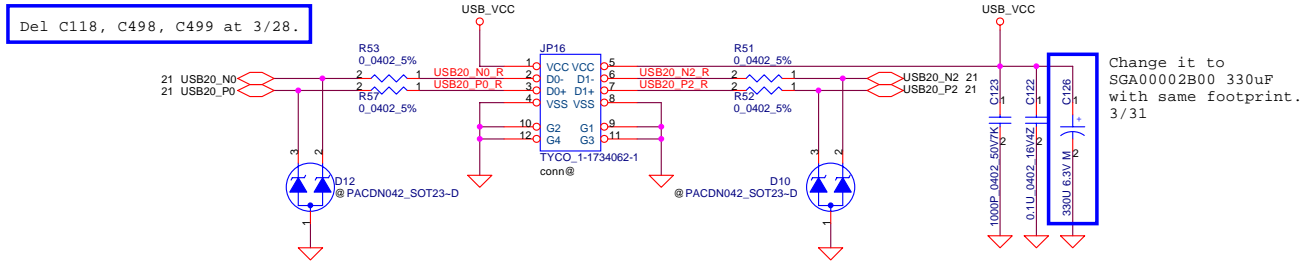
To Audio / USB Board CONN



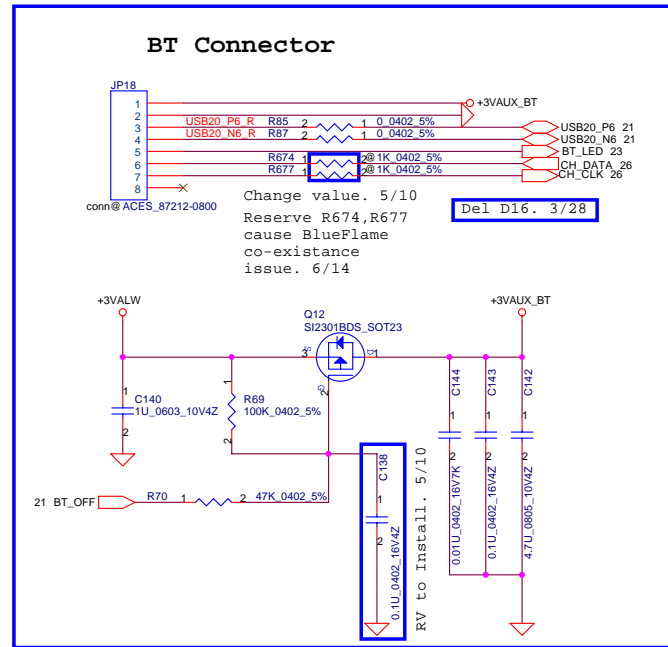
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		AMP & Audio Jack	
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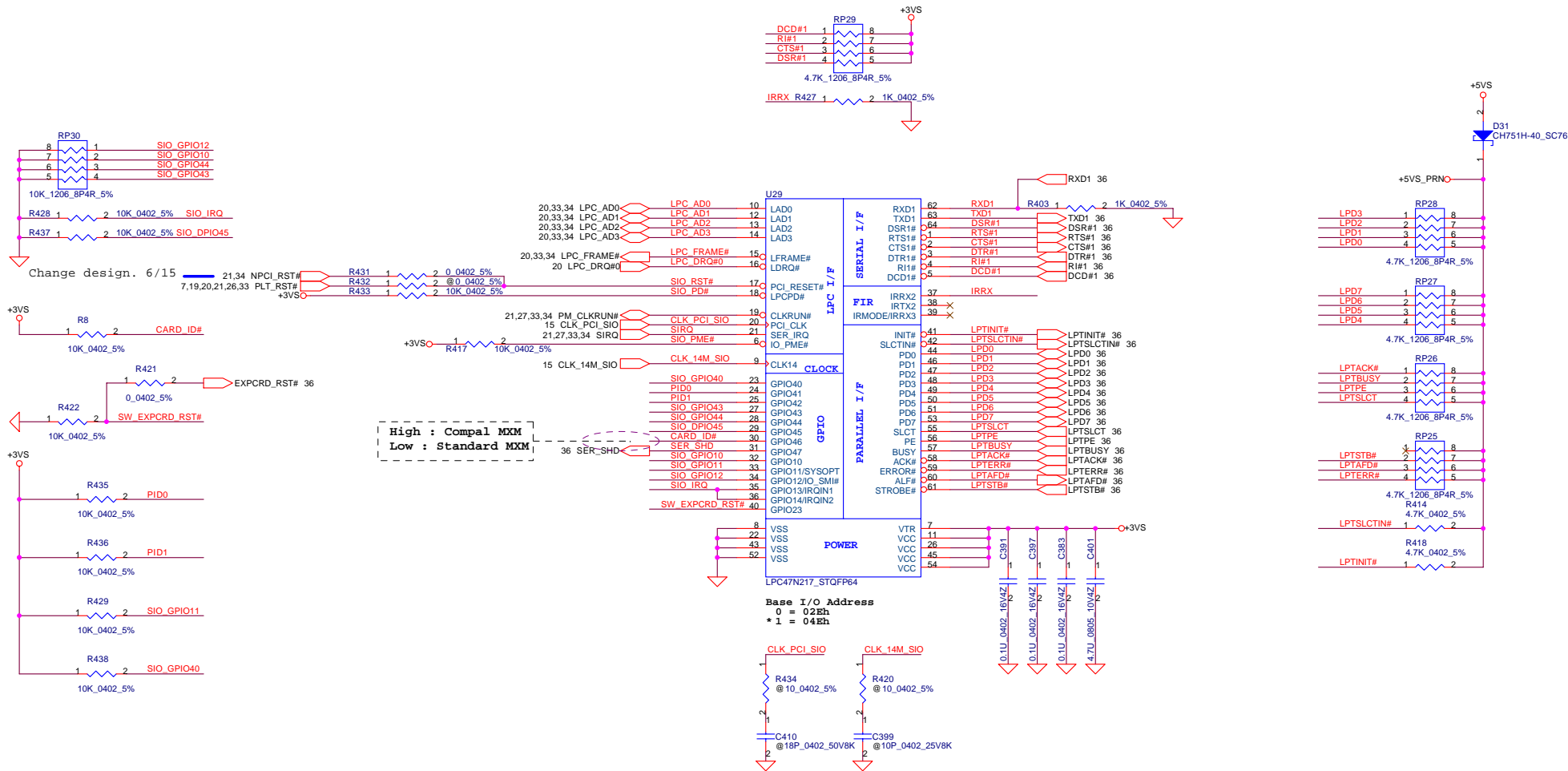
USB CONNECTOR 1



BT Connector



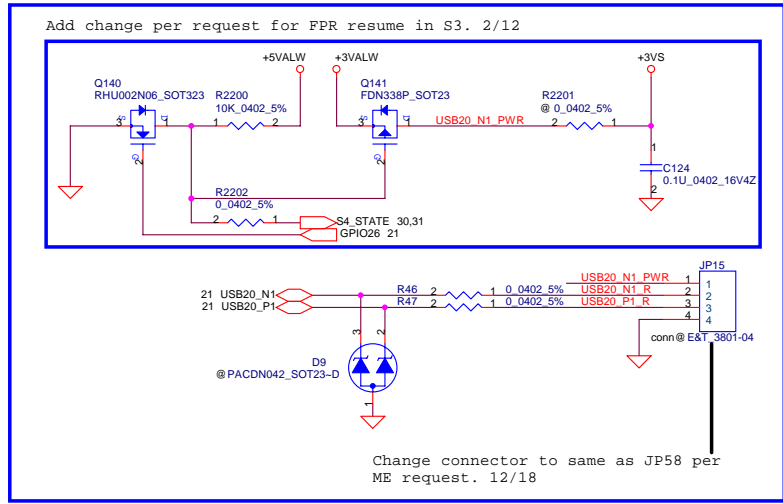
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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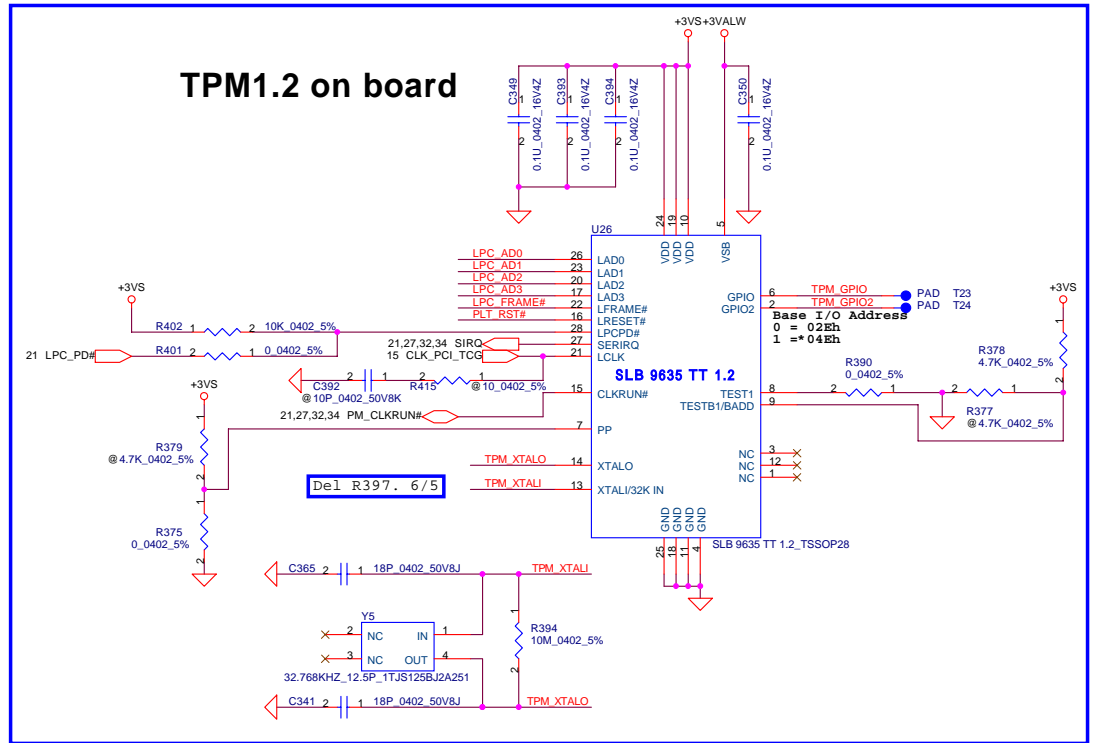
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SUPER I/O LPC47N217			
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Finger printer

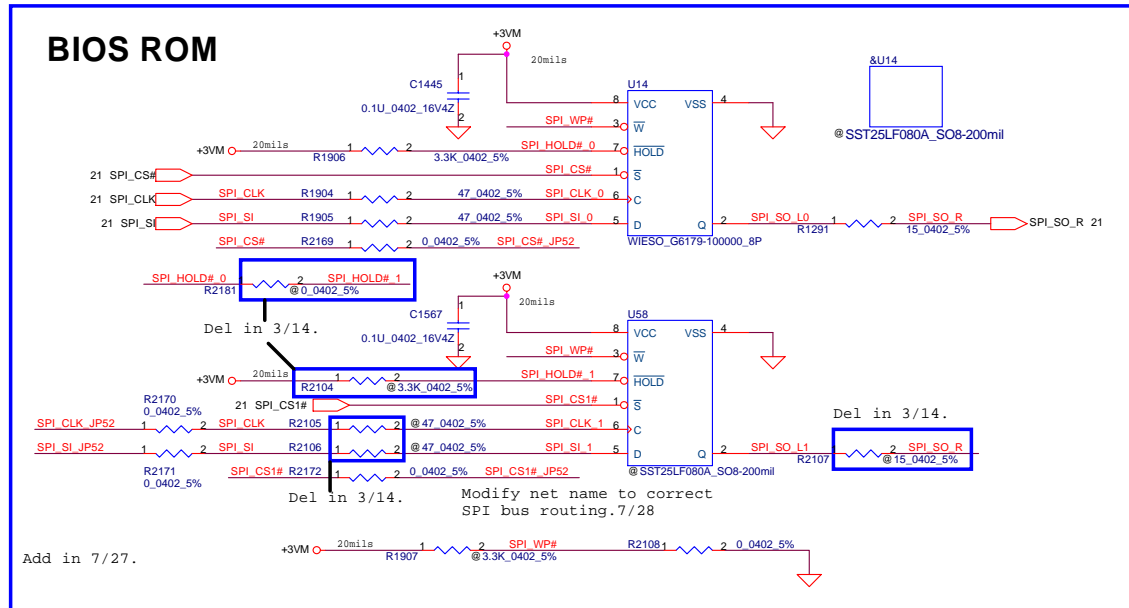


TPM1.2 on board

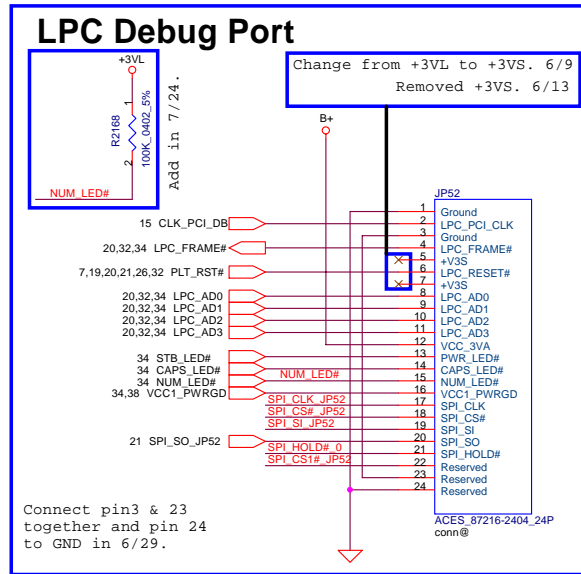


Change SPI ROM to 8Mbit(SA00001JX00) from SI2.

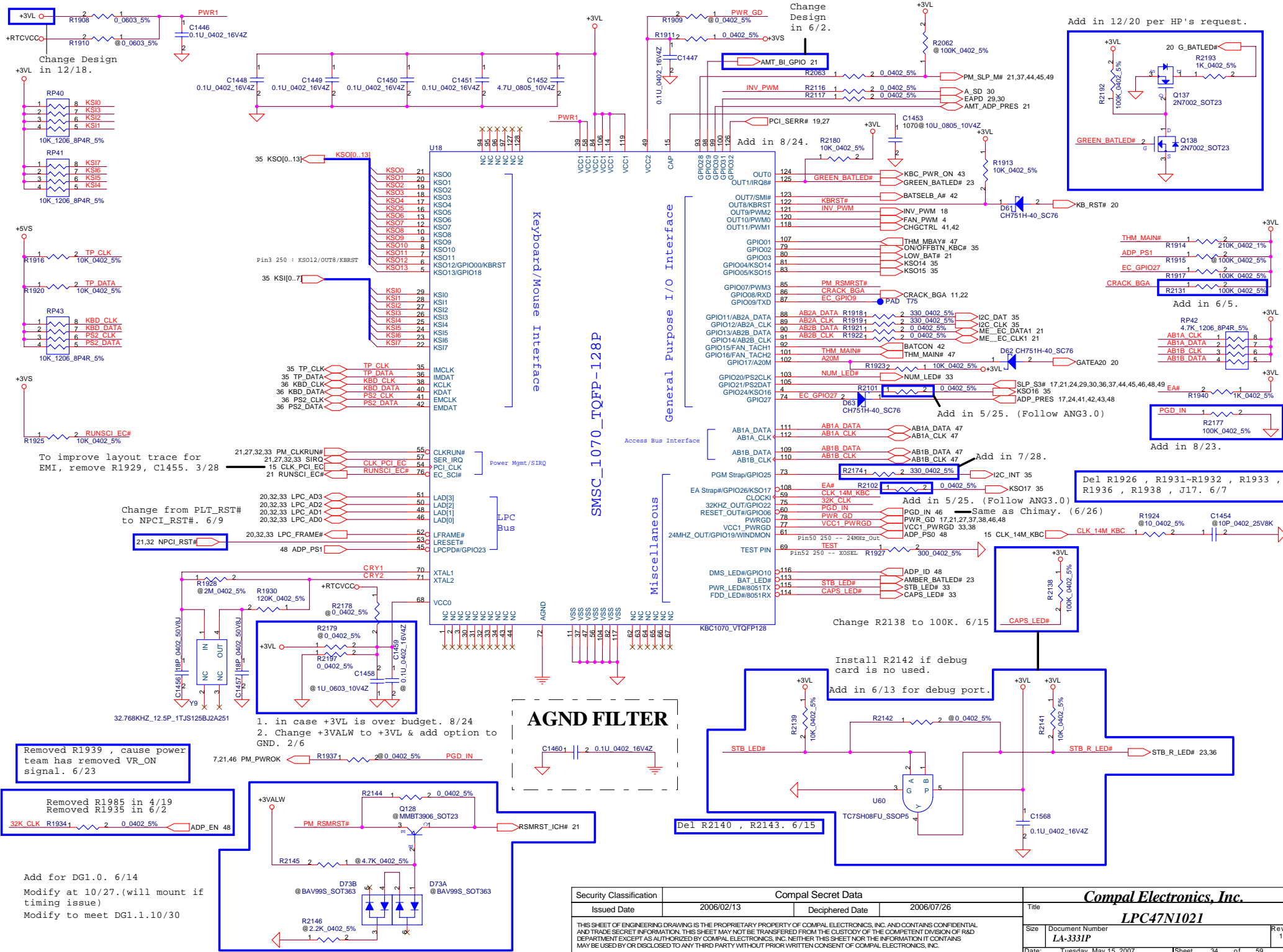
BIOS ROM



LPC Debug Port



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	TCG/BIOS ROM/PS2/SW LPC DEBUG
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To improve layout trace for EMI, remove R1929, C1455. 3/28

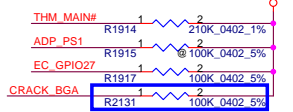
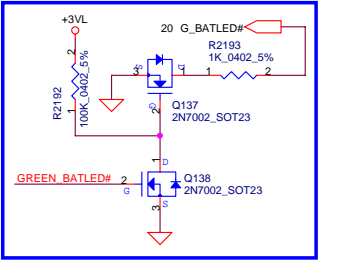
Change from PLT_RST# to NPCI_RST#. 6/9

Removed R1939, cause power team has removed VR_ON signal. 6/23

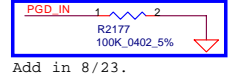
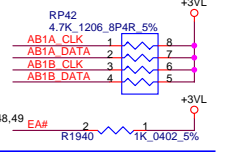
Removed R1985 in 4/19
Removed R1935 in 6/2

Add for DG1.0. 6/14
Modify at 10/27.(will mount if timing issue)
Modify to meet DG1.1.10/30

Add in 12/20 per HP's request.



Add in 6/5.



Add in 8/23.

Del R1926, R1931-R1932, R1933, R1936, R1938, J17. 6/7

Change R2138 to 100K. 6/15

Install R2142 if debug card is no used.
Add in 6/13 for debug port.

Del R2140, R2143. 6/15

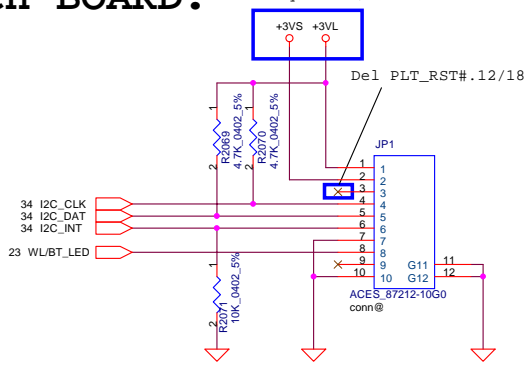
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LPC47N1021

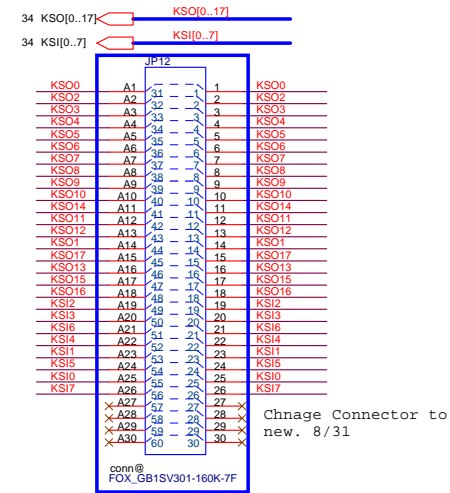
LA-333IP

SWITCH BOARD.

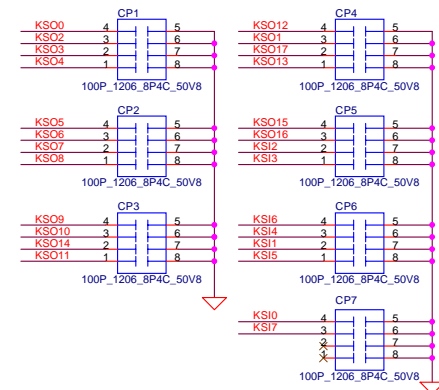
Modify at 10/5.



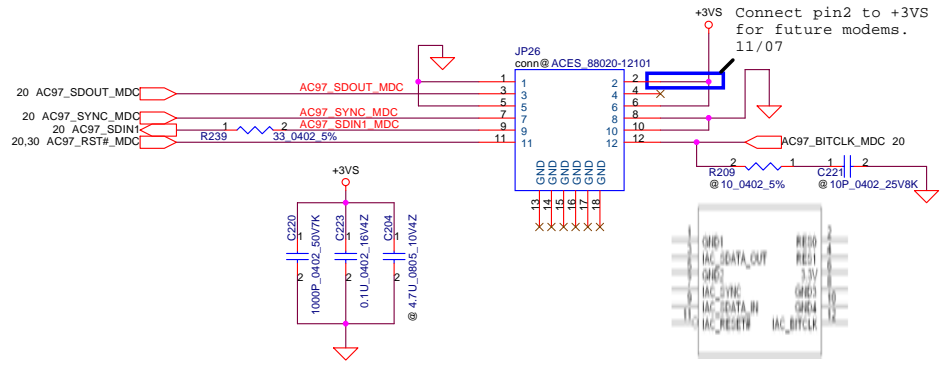
INT_KBD CONN.



Update to 18x8 angelfire keyboard matrix

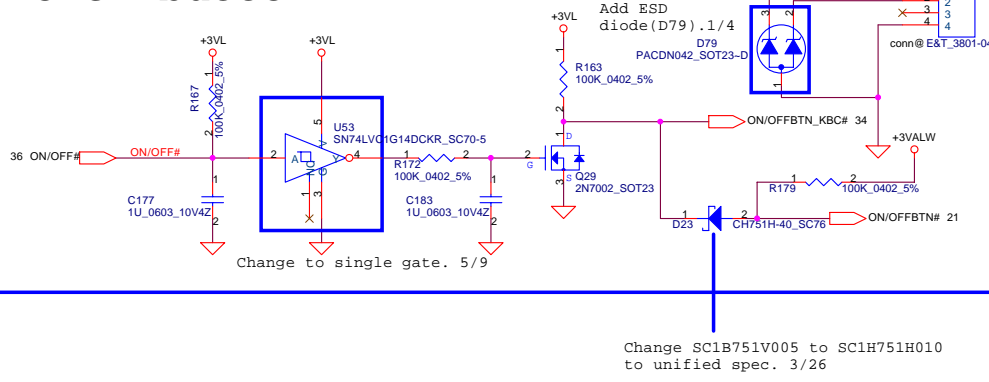


MDC 1.5 Conn.

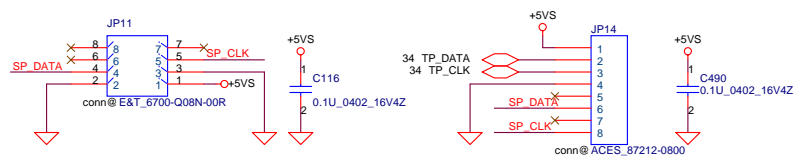


Del Modem disable function(Del R2147). 6/21.

Power button

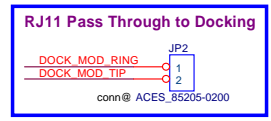


TrackPoint CONN. T/P BOARD.

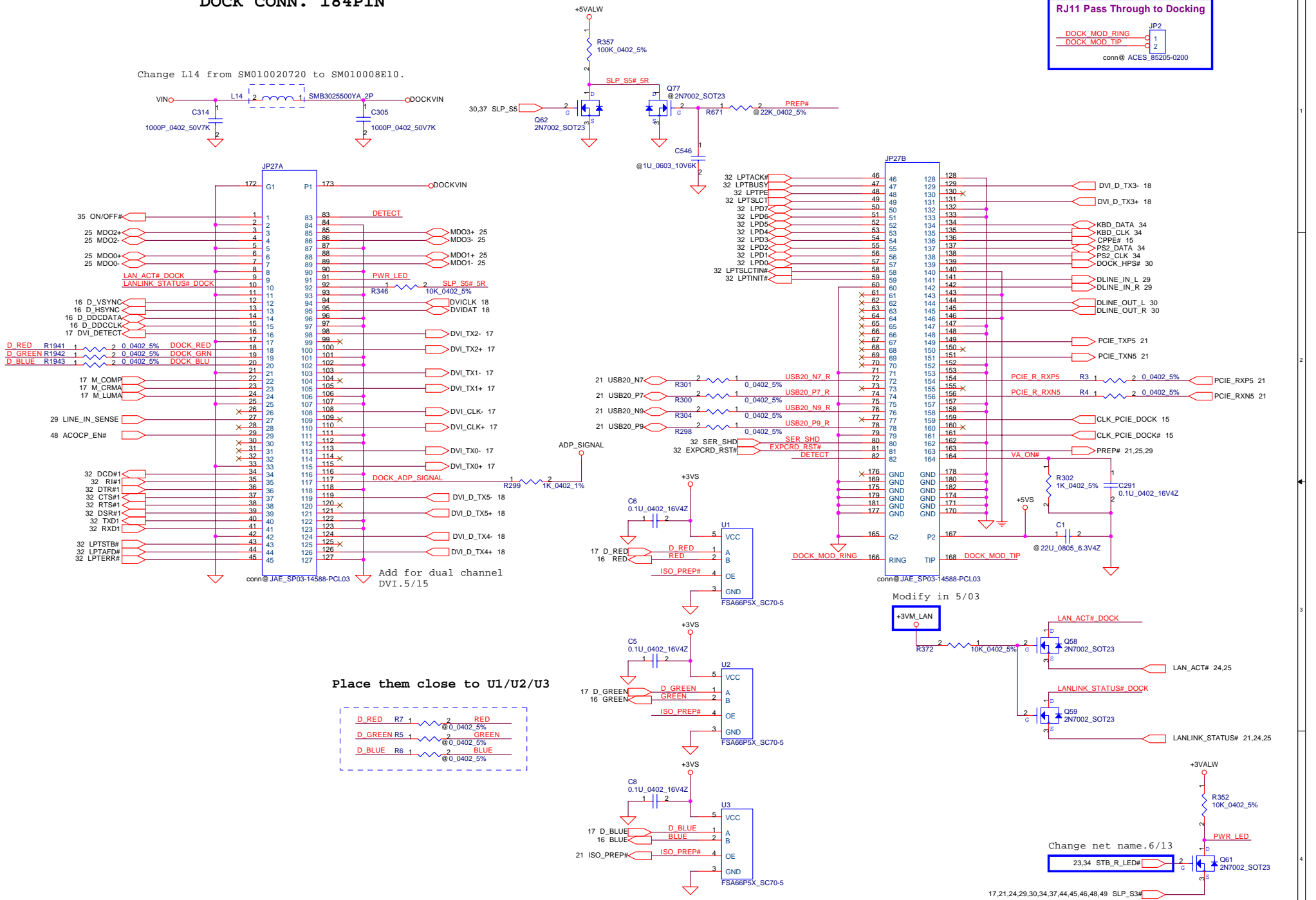


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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title
				MDC/KBD/ON OFF/LID
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				Document Number
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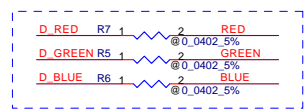
DOCK CONN. 184PIN



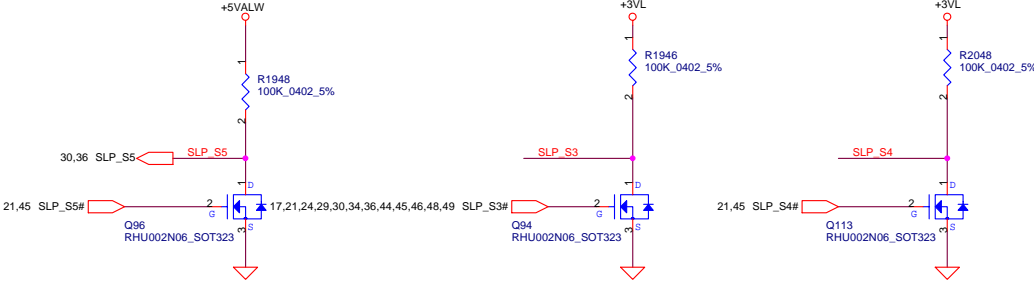
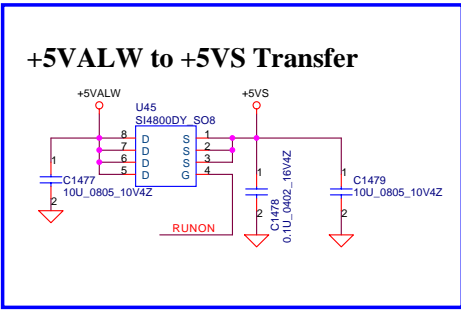
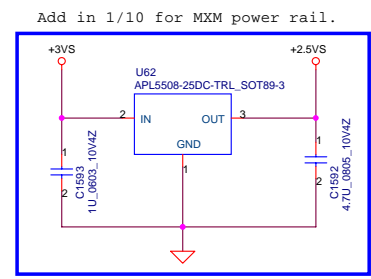
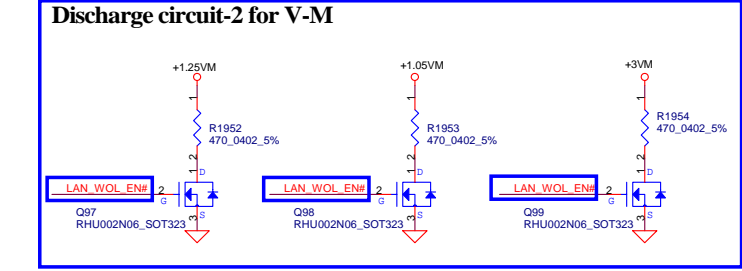
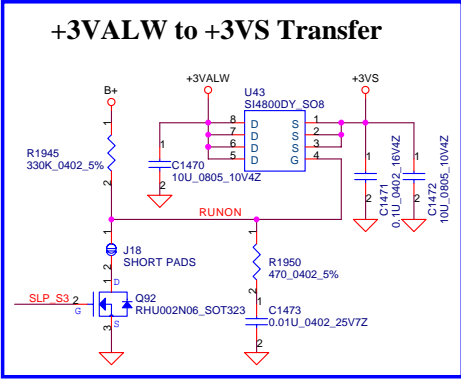
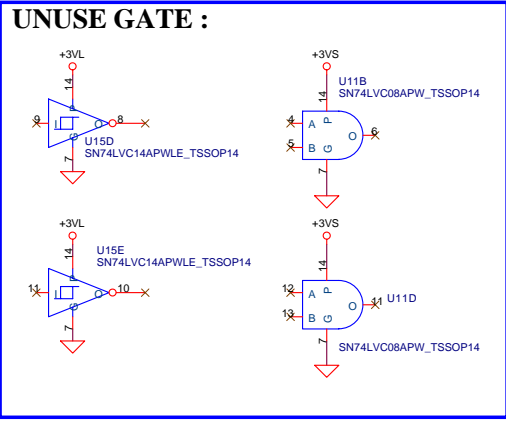
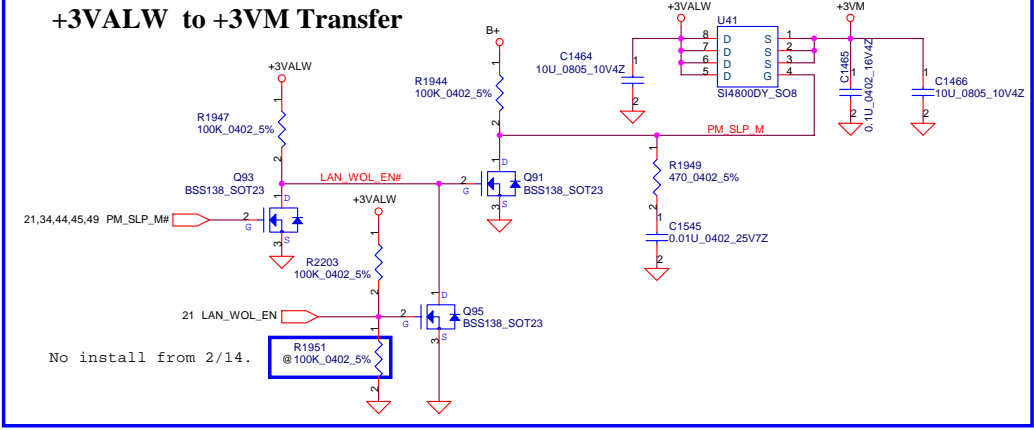
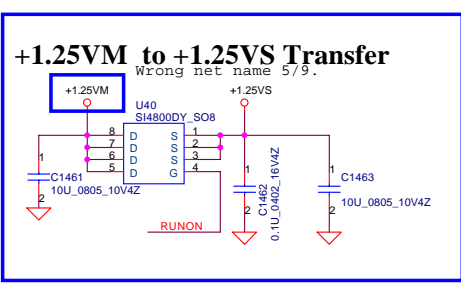
Change L14 from SM010020720 to SM010008E10.



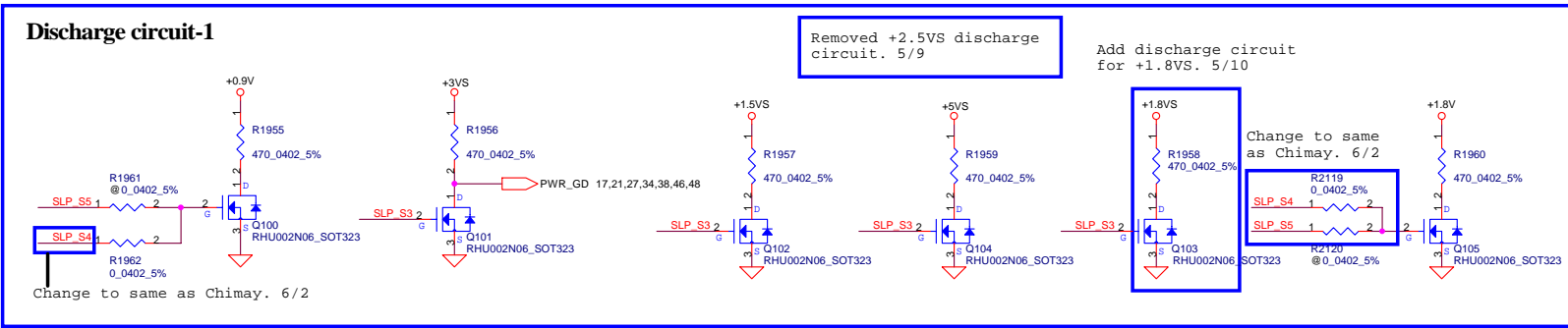
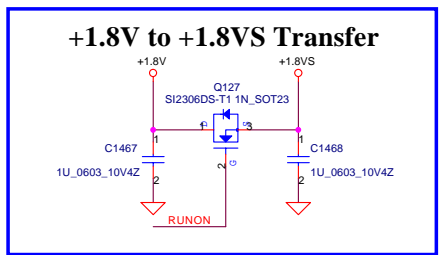
Place them close to U1/U2/U3



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Size	Document Number	Date		Sheet	Rev
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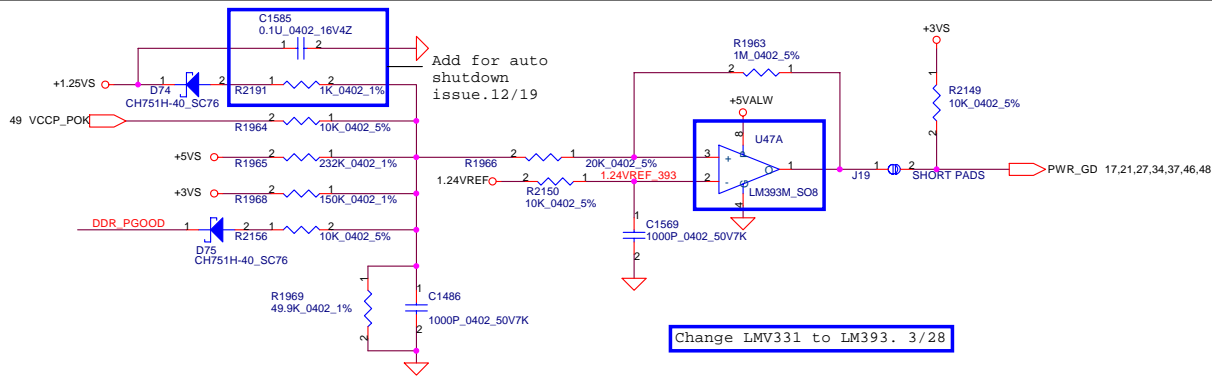


Change U42 to Q , cause no need such power consumption of +1.8VS. 6/9

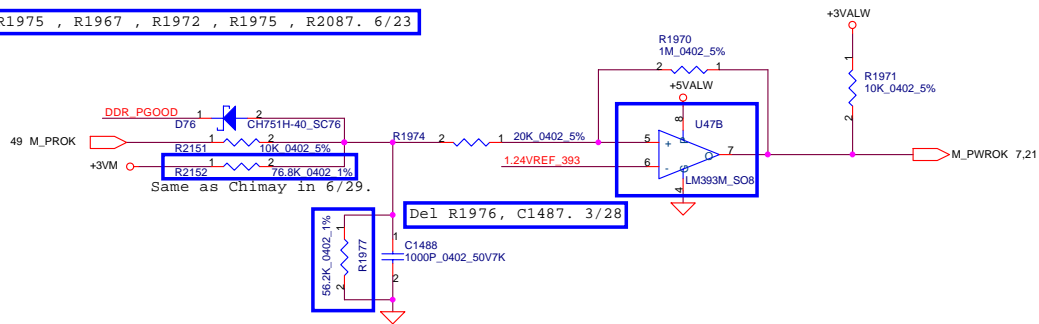


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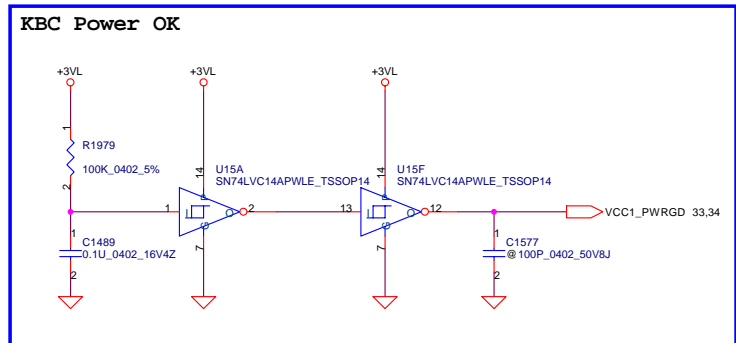
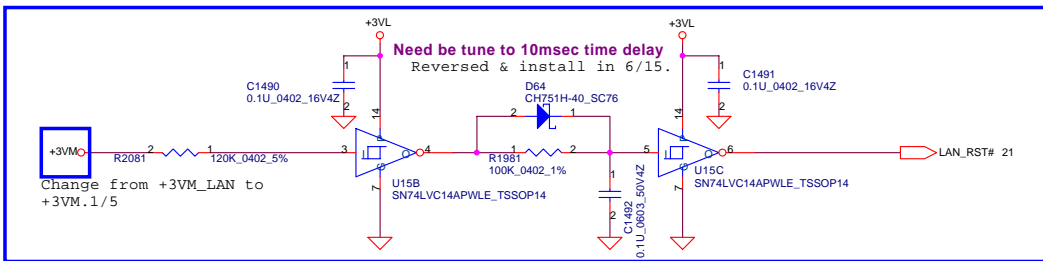
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Compal Electronics, Inc.			
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Size	Document Number	Rev	
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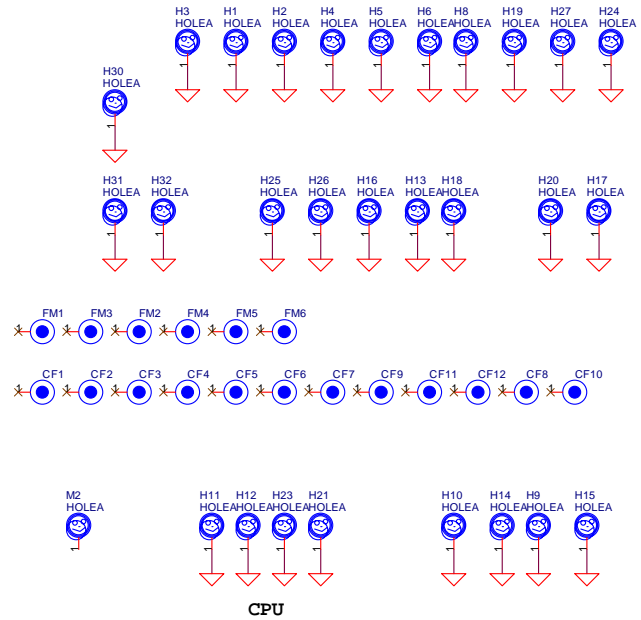
Del R1975 , R1967 , R1972 , R1975 , R2087. 6/23



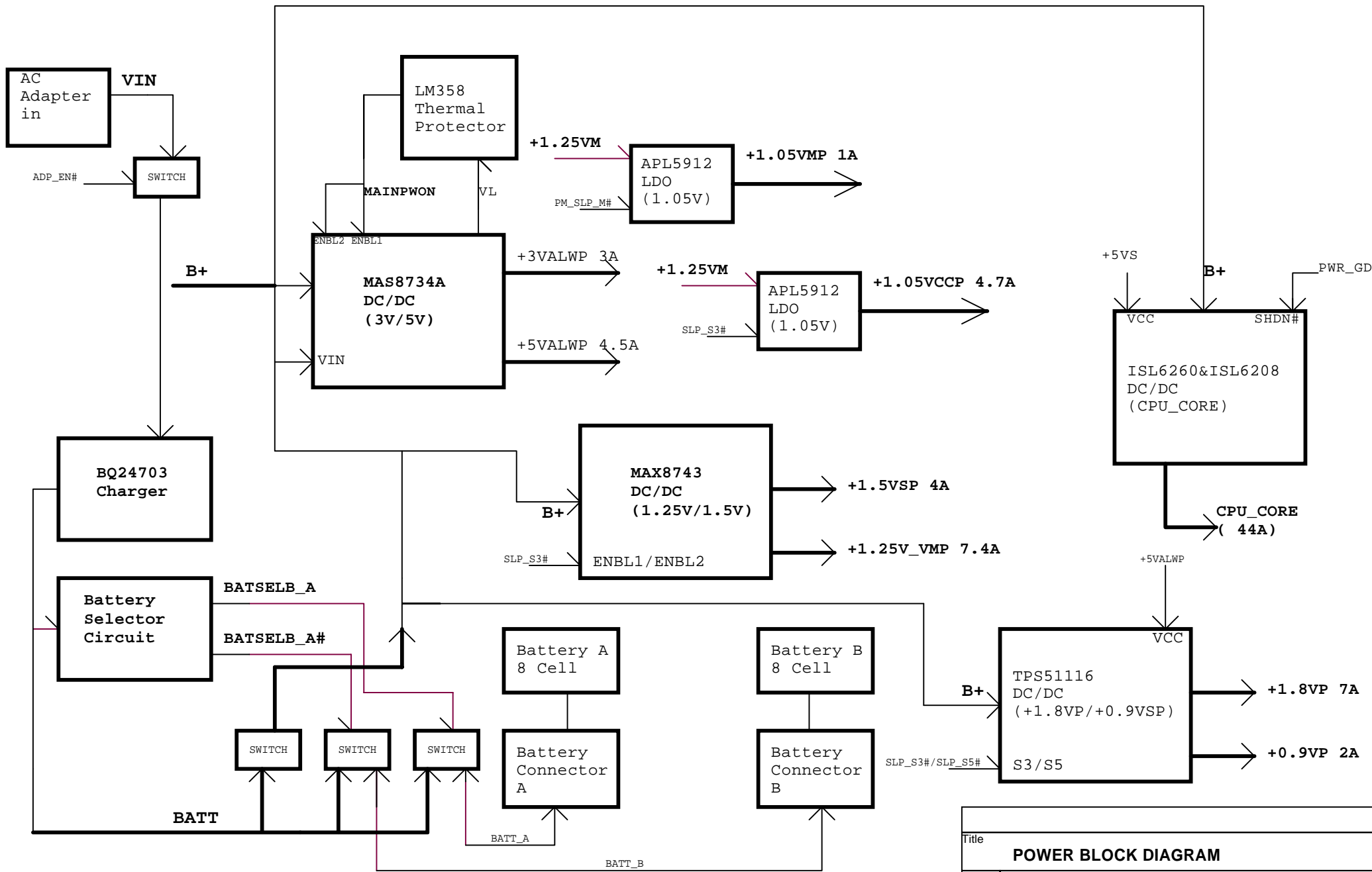
Change to same as Chimay (Del R2080 , R1980 , R2082. 6/23
Modify to same as Chimay 5/5



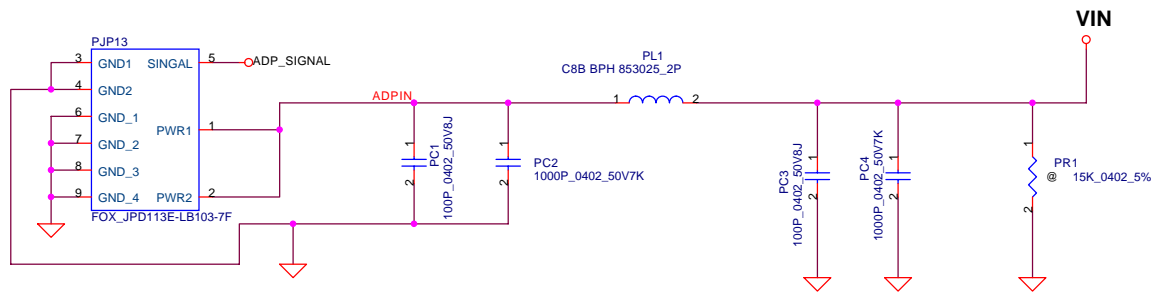
Del U54 and connect to U15. 12/19
Del Q106 and connect to U15, del R1978 and reserve C1577.



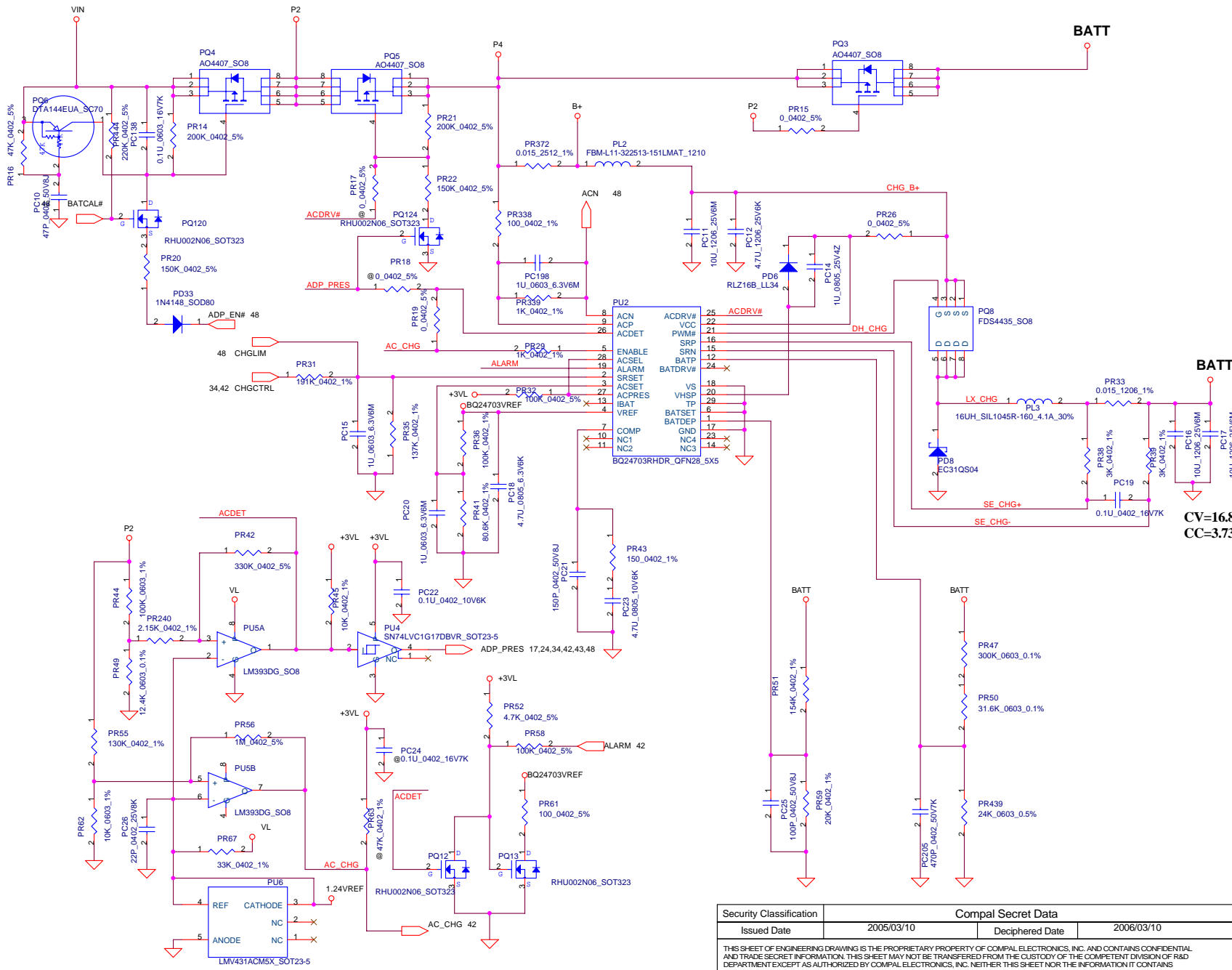
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Title		
POWER BLOCK DIAGRAM		
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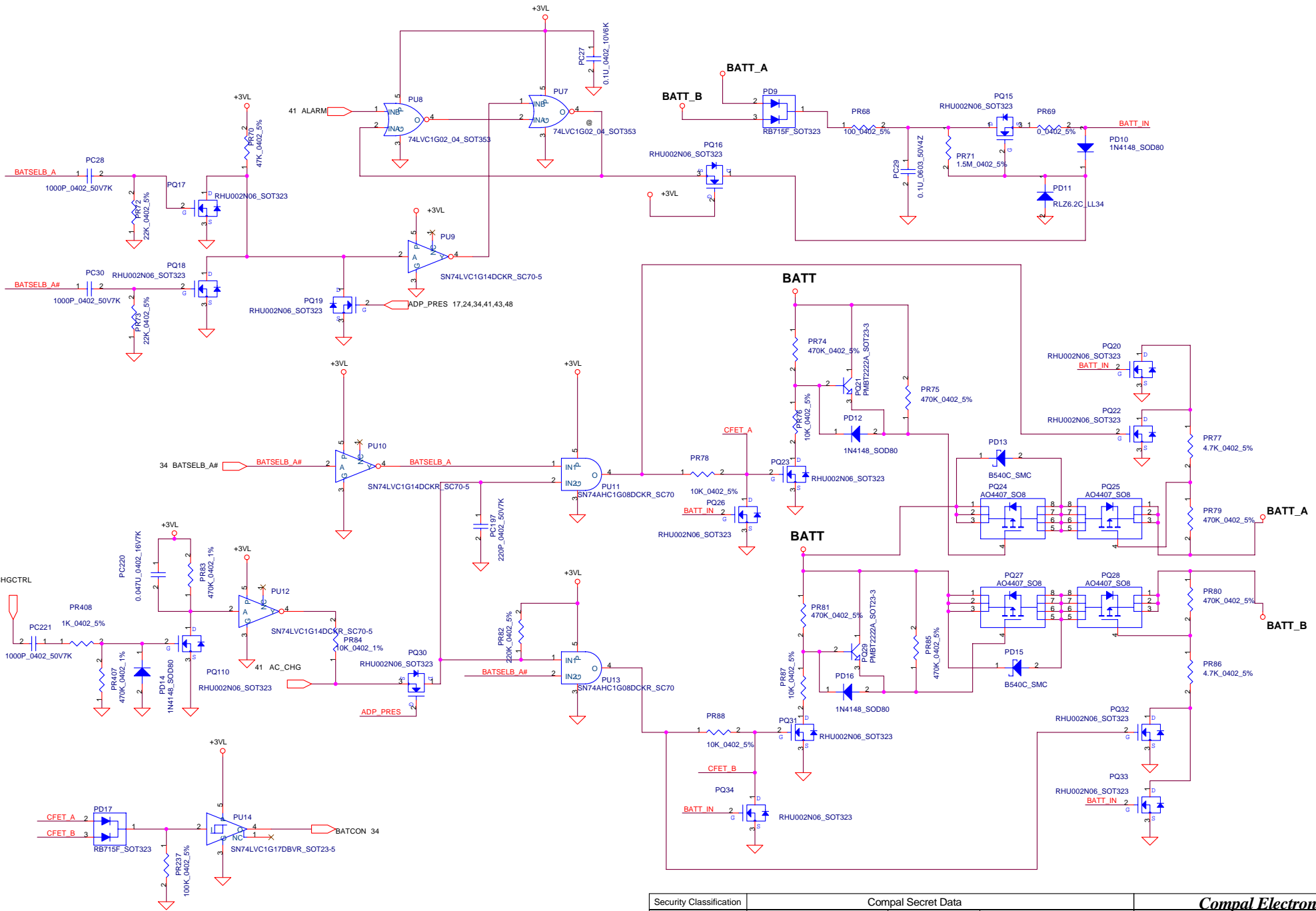
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CV=16.8V (8 CELLS LI-ION)
 CC=3.73A when duty for CHGCTRL is 100%

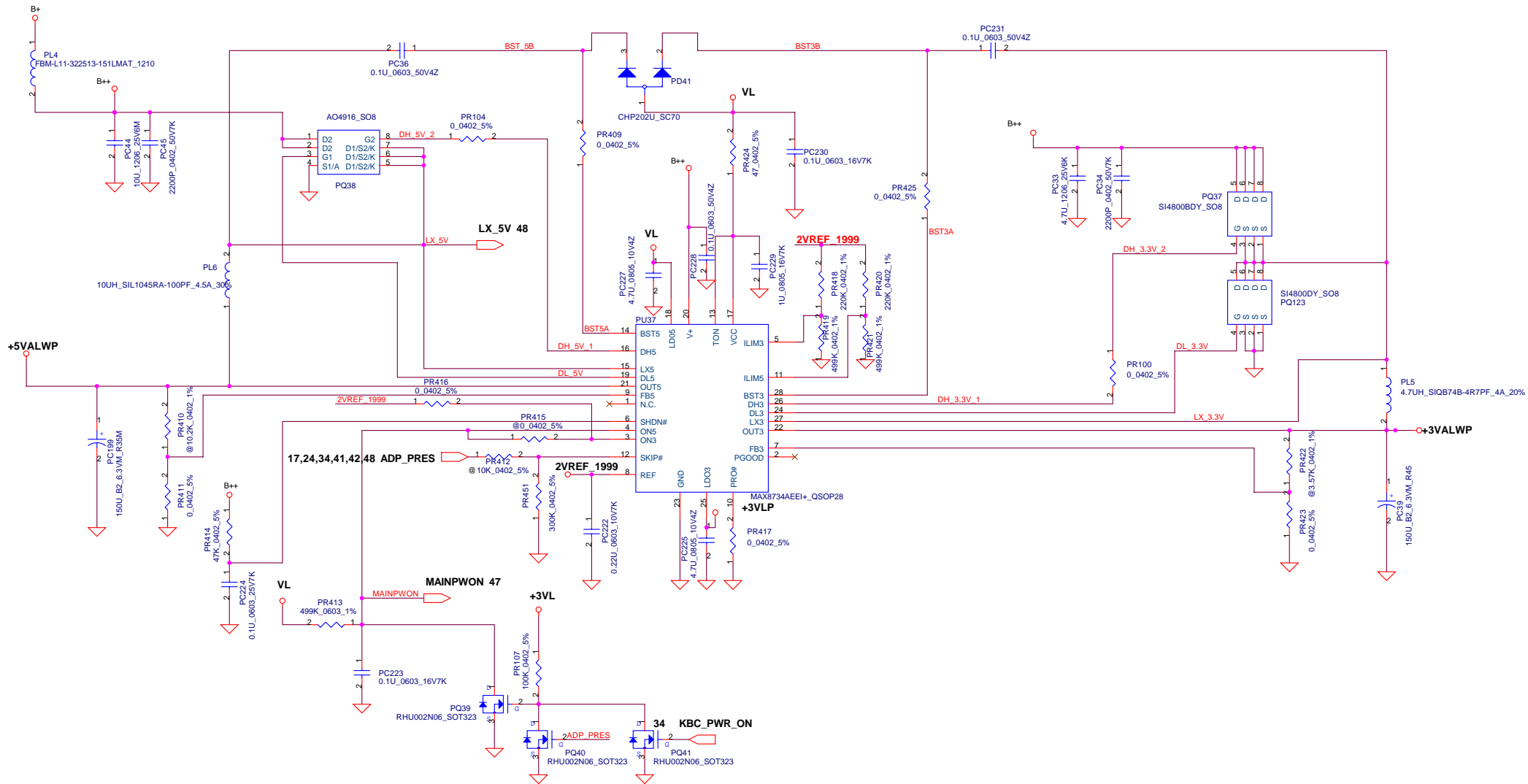
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Compal Electronics, Inc.		
Charger		
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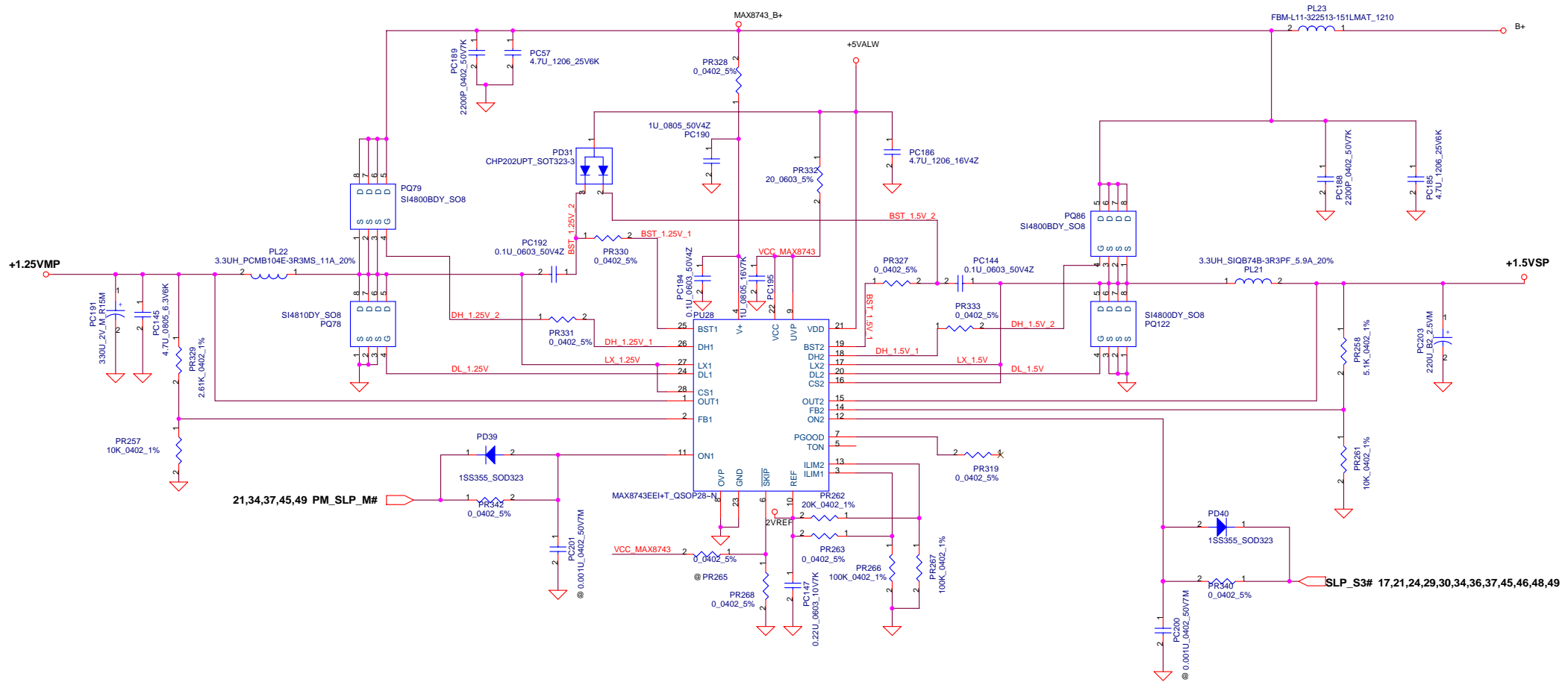
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Compal Electronics, Inc.		
Battery selector		
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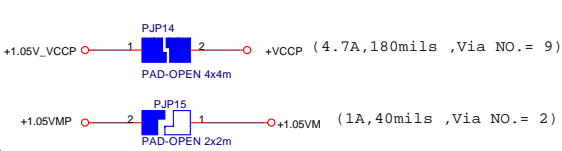
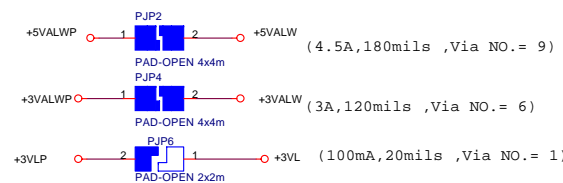
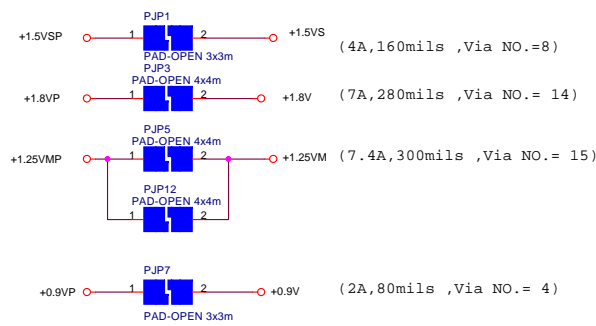


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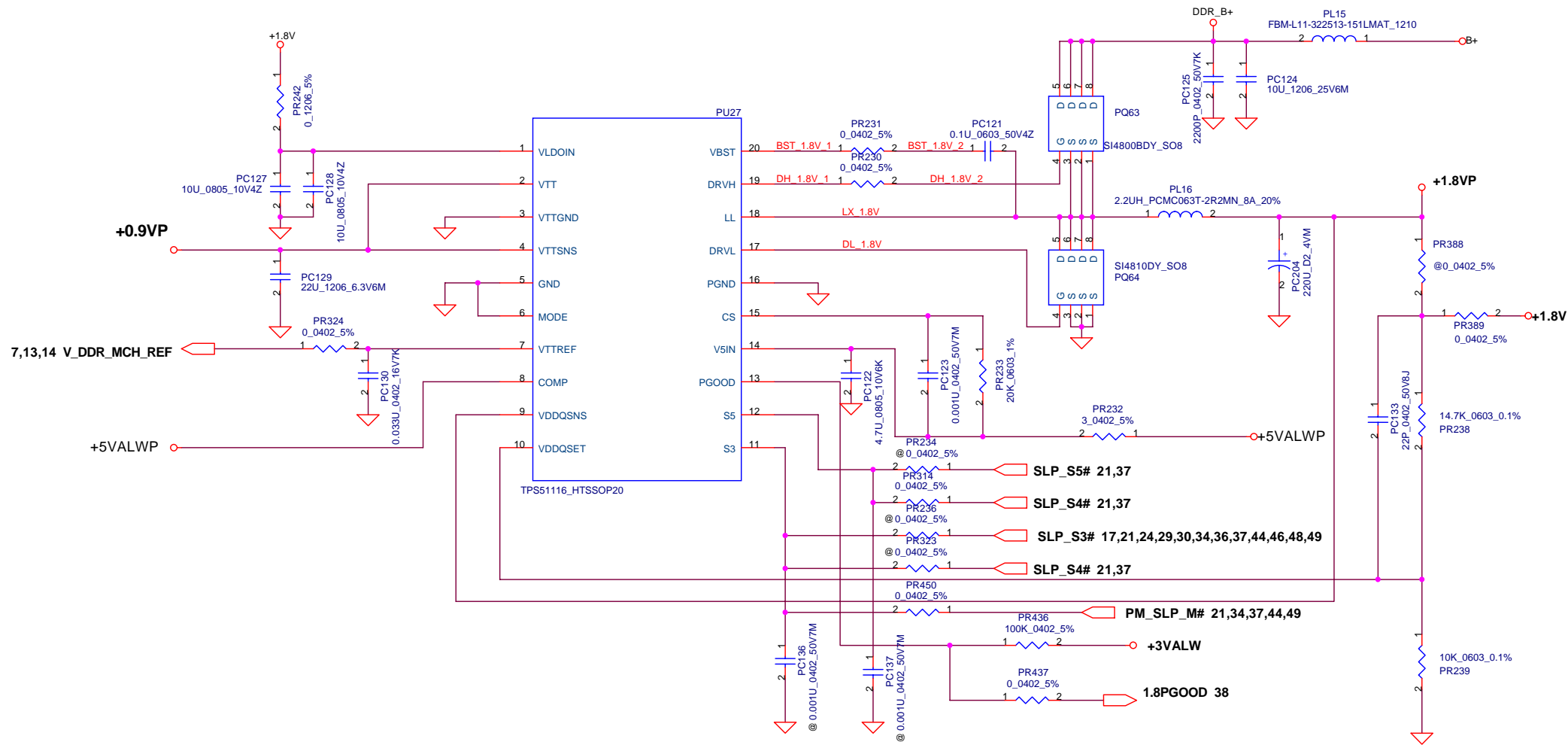
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Size	Document Number	Rev	
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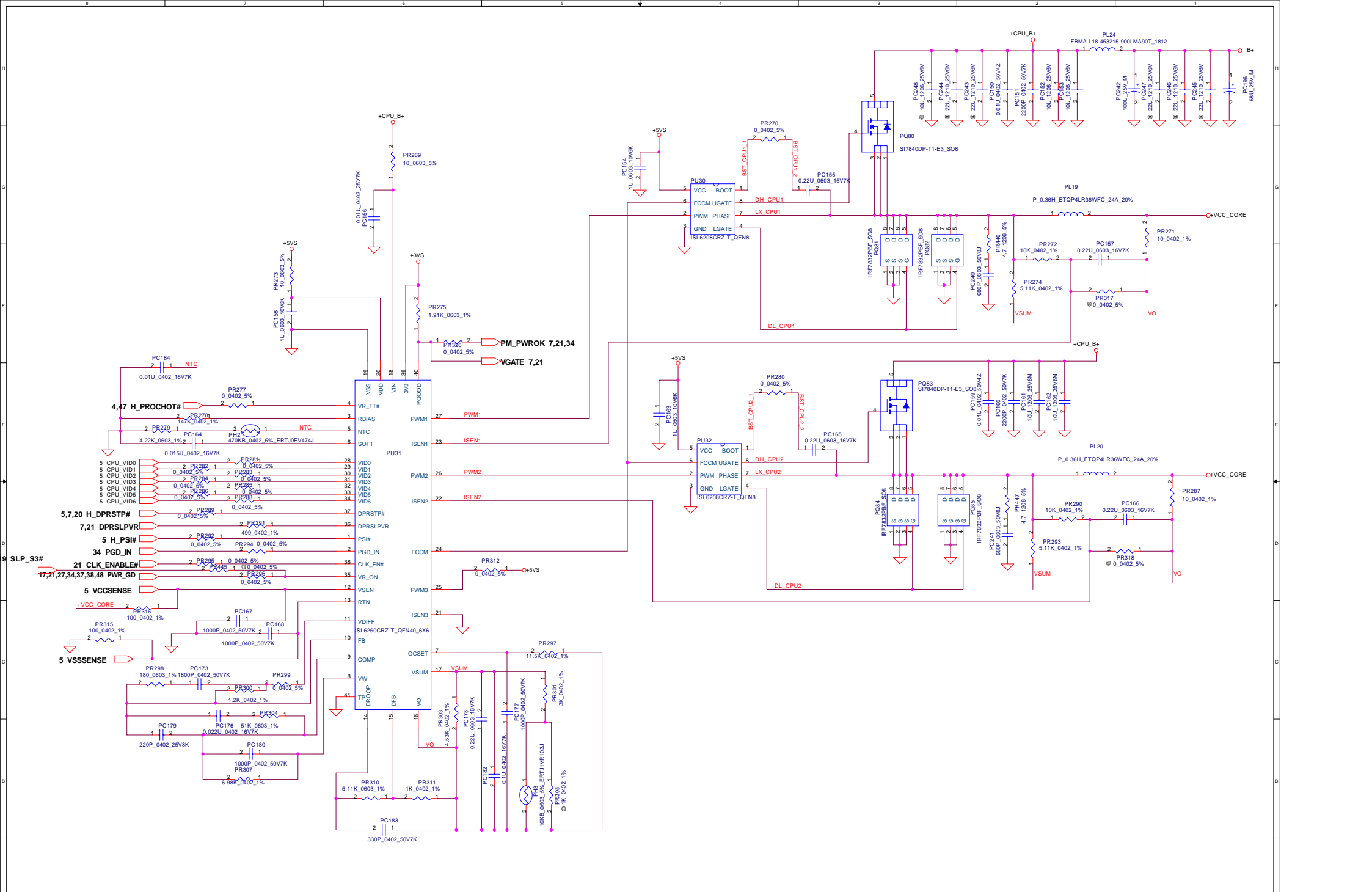
1.5VSP/+1.25VMP



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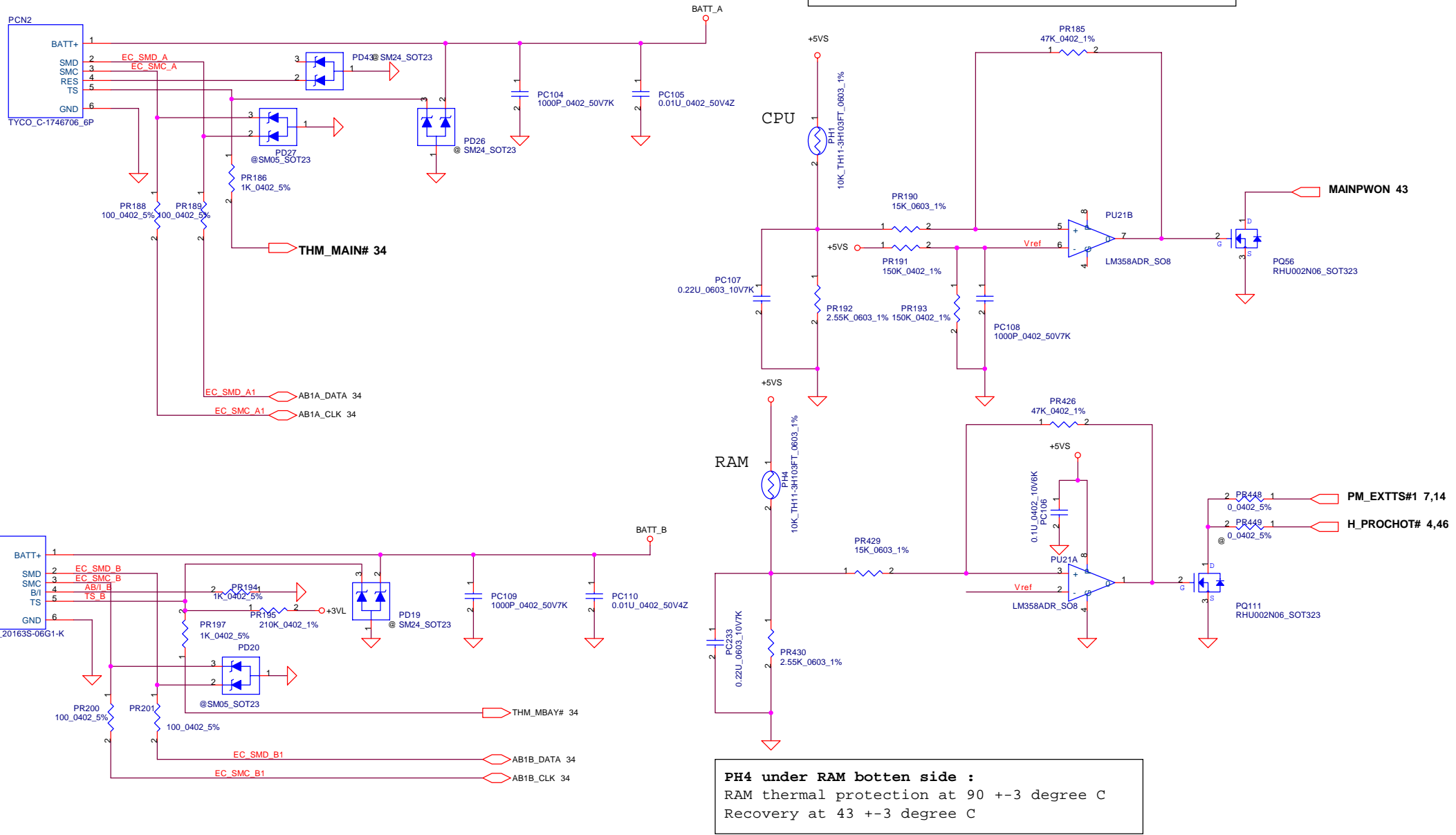


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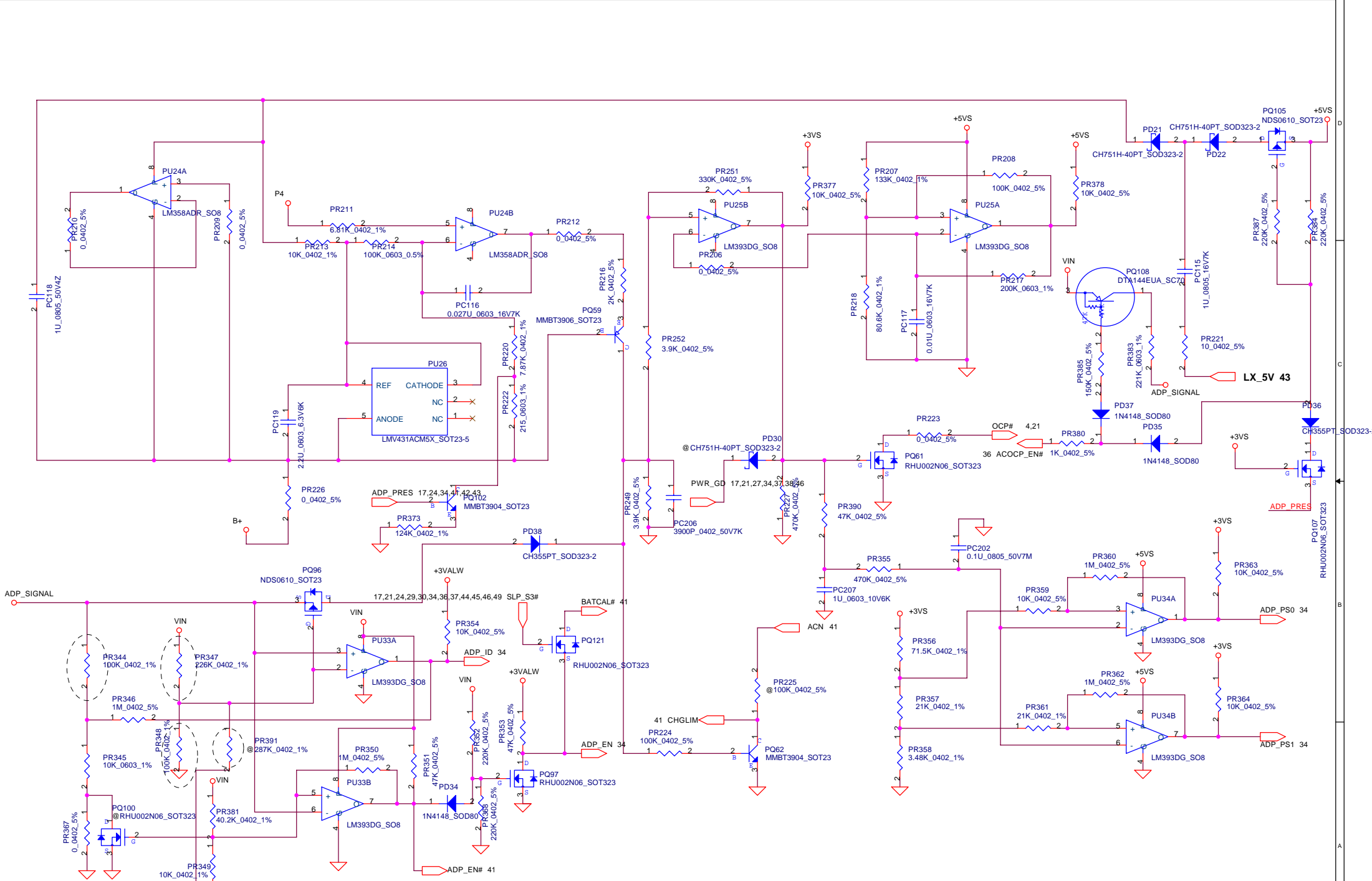
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PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 43 +-3 degree C



PH4 under RAM botten side :
 RAM thermal protection at 90 +-3 degree C
 Recovery at 43 +-3 degree C

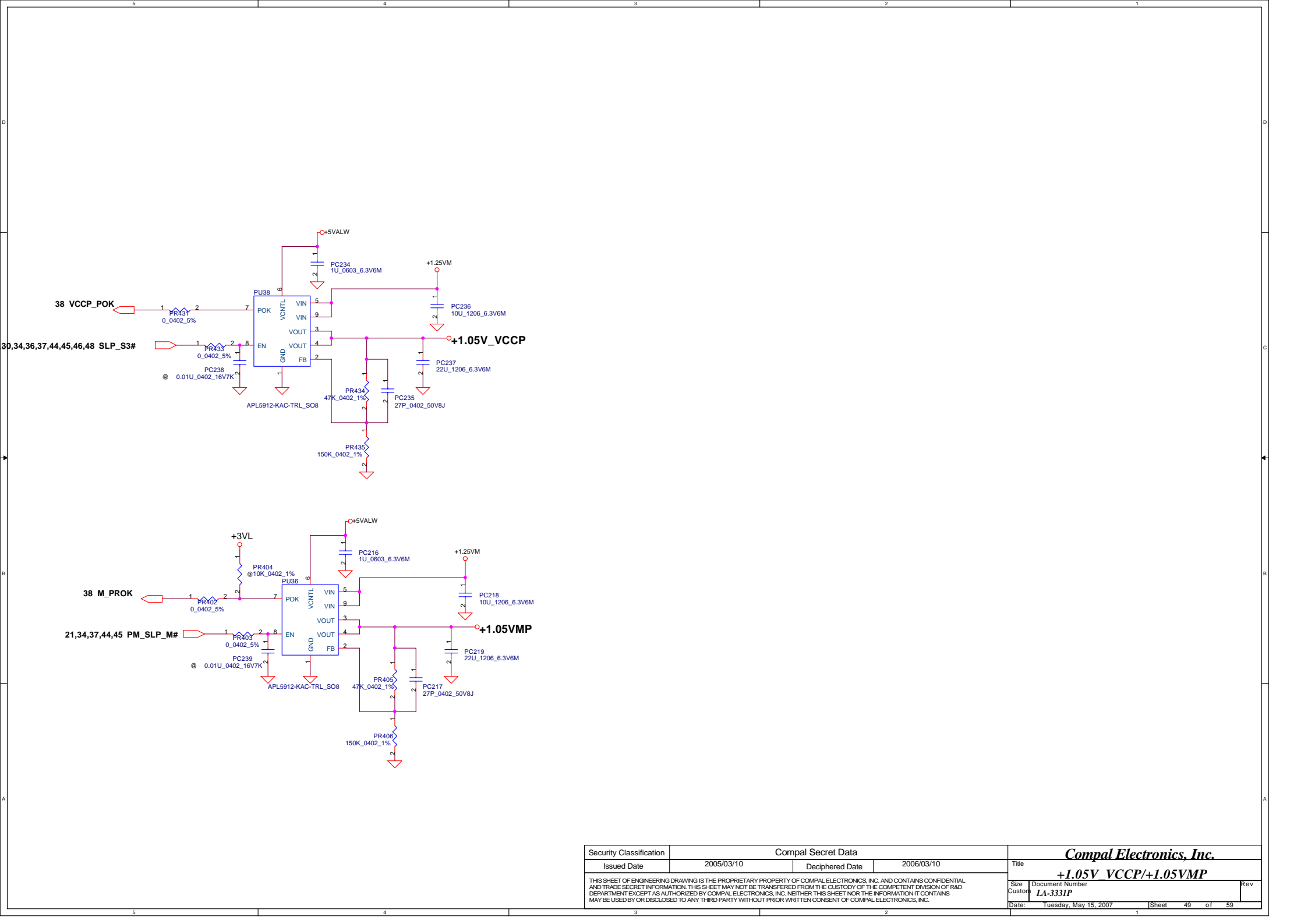
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				BATTERY CONN	



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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Charger	5/9	HP	Remove PQ91,PD32,PR376	Remove PQ91,PD32,PR376	Rev.
2	42	Battery Selector	5/9	HP	Modify battery selector design.	PU12 Change from SN74LVC1G17DBVR_SOT23-5 to SN74LVC1G14DCKR_SC70-5 Add new location PC220 as 0.047uF Add new location PC221 as 1000PF Add new location PR407 as 470K ohm. Add new location PR408 as 1K ohm.	
3	43	3.3VALW/5VALW	5/9	HP	Modify 3.3VALW/5VALW solution	Change solution from TPS51020 to MAX8734A	
4	44	2.5VALW/1.5VS/ 1.05VCCP	5/9	Compal	Remove 2.5VALW, H/W no need!	Remove PU20, PC72, PC73	
5	47	BATTERY CONN	5/9	Compal Thermal team	Add RAM thermal protection schematic.	Add new location PH4,PC233,PR430,PR429,PR426,PQ111	
6	48	ADP_OCP	5/9	HP	Modify ADP_OCP design	Delete PR379,PQ103,PQ104,PR386,PR382,PQ106	
7	43	3.3VALW/5VALW	5/9	Compal	Modify 3.3VALW/5VALW location for layout.	Swap location PC33, PC44 Swap location PC34, PC45 Swap location PQ37, PQ38, PL5 PL6, PR100, PR104, PC39 , PC199.	
8	44	1.25VM/1.5VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution	
9	49	1.05V_VCCP/ 1.05VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution.	
10	45	1.8V/0.9VS	6/2	HP	HP request to follow Chimay.	Modify 1.8V/0.9VS schematic.	
11	41	Charger	6/6	HP	HP request!	Modify Charger schematic.	
12	42	Battery selector	6/6	HP	HP request!	Modify selector schematic.	
13	47	BATTERY CONN	6/6	HP	HP request!	Modify main battery power in schematic.	
14	45	1.8V/0.9VS	6/7	HP	At S3 mode, 0.9V need exist, so connect PR242 to 1.8V	Modify PR242 connect to 1.8V	
15	46	CPU_CORE	6/21	HP	HP request.	Modify PU31.35 pin connect to SLP_S3#, originally is connect to VR_ON.	

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	41	Charger	5/9	HP	Change PQ114 to BSS138.	Change PQ114 to BSS138.	
17	47	BATTERY CONN	9/7	Compal	Intel Document for the DDR Module Thermal Diode design	Change the PQ111.1 connection from H_PROCHOT# to PM_EXTTS#1	
18	43/44		11/1	Compal	Dual N MOSFET has failure rate at other project, to reduce Dual N MOS useage.	Change 3V, 1.5V solution, to single N Mos FET solution.	
19	41	Charger	03/29	Compal	Reserve some components for EPA.	Reserve PR21, PR22, PQ124 and PR19.	
20			03/30	Compal	DFx request modify footprint to prevent shift issue.	Modify PD10,PD12,PD14,PD16,PD33,PD34,PD35,PD37(SC11N414880) footprint from SOD80 to LL34.	
21			04/02	Compal	For Energy star	Uninstall Uninstall PR1, PR17 and PR18.And install PR19,PR21,PR22,PQ124.	
22			04/02	Compal	For ADP OCP setting.	Change PC116 from 0.22U_0603_16V_X7R to 0.027U_0603_16V_X7R.	
23			04/02	Compal	For ADP OCP setting.	Change PR222 from 422 ohm 1% to 215 ohm 1%.	
24			04/02	Compal	For ADP OCP setting.	Change PC117 form 0.027U_0603_16V_X7R to 0.01U_0603_16V_X7R.	
25			04/02	Compal	For ADP OCP setting.	Change PR217 from 604K_0603_1% to 200K_0603_1%	

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	26	Mini Express Card	7/3	Compal	H28 & H29 size different.	Change H28 size to same as H29.	0.2
2	24	GIGA LAN	7/4	Compal	BOM Leverage to Chimay.	Chnage Y8 to 25MHz_20P_1BG25000CK1A (Same as Chimay)	0.2
3	18	GPIO Extender	7/4	Compal	Use wrong package with BOM (U59).	Correct the package.	0.2
4	34	Capacitive I2C	7/27	HP		Change R1918, R1919 & add R2174 to 330 ohm.	0.2
5	15	FSB SEL	7/27	HP	No good for layout quality.	Del R1719, R1726.	0.2
6	20	RTC Conn	7/26	Compal	Wrong Package	Change JP28 from SP02000D000 to SP02000D700.	0.2
7	33	NUM_LED#	7/25	Compal	System auto re-boot	Add R2168 pull up to 3VL.	0.2
8	30	Head Phone	7/26	HP	ANTI-POP noise	Add circuit for this issue	0.2
9	26	WLAN	7/27	HP		Add R2158 connect to +3VS and connect to JP30 pin 2,39,41,52 , pin37,43 connect to GND.	0.2
10	18	Quick Switch	7/26	Compal	Wrong package for PCB foot print (U57).	Correct the package.	0.2
11	21	CPU Clock	7/28	Compal/HP	VRMPWRGD has glich to cause wrong CPU clk.	Add R2173 & reserve C1576.	0.2
12	18	Quick Switch	7/28	Compal	Channel A & B will twist togeter as current layout.	Swap Channel A & B on schematic.	0.2
13	06	VCCP	8/1	Compal		Delete C1570 ~ C1573	0.2
14	21	CL_VREF1_ICH	8/2	Compal	Wrong pull high to +3VM.(R1855)	Change pull up to +3VALW.	0.2
15	31	USB	8/2	Compal	No pull up resistor for USB power switch OC pin.	Add R2175 and pull up to +5VALW.	0.2
16	18	Quick Switch	8/3	HP		Add U61 and Reserved R2176 for Q-switch select pin.	0.2
17	38	Power Good	8/4	Compal	VCC1_PWRGD has glich when power on.	Reserve C1577 on PWRGD to GND.	0.2
18	21	Power Good	8/7	Compal	CLK_ENABLE# has glich when power on.	Change R1862 from 330ohm to 1K ohm.	0.2
19	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
20	27	CardBus Controller	8/15.	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
2	27	CardBus Controller	8/15	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3
3	21	USB	8/23	Compal	System easy hang-up when plug USB2.0 device.	Separate from pull up resistor of U10 for these pins.	0.3
4	34	PGD_IN	8/23	HP	Leverage Chimay SI schematic.	Add R2177(100K) pull down to GND.	0.3
5	34	EC VCC0(PIN 68)	8/24	HP	+3VL may over budget.	Add R2178, R2179(RV) for option the power source.	0.3
6	34	EC	8/24	HP	Leverage Chimay SI schematic.	Add D77, R2180 and connect D77 pin2 to U10 pinAE10.	0.3
7	33	SPI ROM	8/24	HP	Debug card asserts hold, can't assert both SPI ROM.	Add R2181 to connect SPI_HOLD#0 and SPI_HOLD#1.	0.3
8	26	MINI Card	8/24	HP	May leakage issue from WLAN card.	Add D78 to prevent this issue.	0.3
9	21	Power Sequency	8/24	HP	There is a shoot when power on of this pin.	Reserve R1862 and add R2182(10K) pull up to PWR_GD.	0.3
10	21	GPIO26	8/24	HP	Default is input can't floating.	Add a pull up R2183(10K) to +3VS.	0.3
11	21	GPIO17	8/24	HP	Default is input can't floating.	Make R2115 from RV to mount.	0.3
12	21	STP_CPU#	8/24	HP	Can't into C3 status.	Mount R1829.	0.3
13	21	XDP_DBRESET#	8/24	HP	Leverage Chimay SI schematic.	Change R1847 to 1K.	0.3
14	21	SPI_CS1#	8/24	HP	Only need one 4MB BIOS chip.	Add R2184(0 ohm) for BOM option.	0.3
15	17	MXM-HE	8/24	HP	Need High performace VGA card.	Chnage MXM-III to MXM-HE.	0.3
16	17	HDMI	8/25	HP	BOM change.	Change R1990 to 1K, R1991 to 10K and add L23, C1578.	0.3
17	21	GPIO12	8/28	HP	Add BOM option for SPI_CS1#.	Change connect of R1845.2 from LAN_PHYPC to LAN_PHYPC_R.	0.3
18	21	GPIO1 & GPIO11	8/28	HP	Net Change.	Exchnage OCP#(To GPIO1)&LANLINK_STATUS#(To GPIO11)	0.3
19	28	Card bus ETD test	8/31	HP	May some issue with ETD test.	Reserved C1509.	0.3
20	35	KBD Connector	8/31	HP	To meet HP 2007 platform defined.	Chnage JP12 from 26pin to 30pin.	0.3
21	10	L22	9/6	HP	BLM18PG221SN1 impedence is 221ohm@100MHZ.	BLM18PG330SN1 impedence is 33ohm@100MHZ.	0.3
22	26	Wireless LAN	9/6	HP	Connect C217, C171, C493 to wrong power.	Connect C217, C171, C493 from +3VS to +3VS_WLAN.	0.3
23	07	CRESTLINE	9/6	HP	Change Chip version from A0 to B0.	Mount R2134.	0.3
24	04, 21	Second FAN	9/7	Compal	Thermal team ask to add control for second FAN.	Add R2185, R2186 and use GPIO20 to control FAN.	0.3
25	17	MXM power B+	9/8	Compal	Delete C9 cause not enough space to placement.	ADD C1579, C1580(1210 size) to replace C9.	0.3
26	24	LAN Connector	9/12	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	ADD C1581, C1582(0402 size) per EMI request.	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	20, 34	BATTERY LED	10/2	HP	GREEN_BATLED# keep high when AC/DC exist.	Change connection between SB & EC.	0.4
2	21	SM Bus	10/3	Compal	SM Bus connection is not correct.	Correct connection of SM bus and reserved R1817, R1820.	0.4
3	35	Function Connector	10/5	HP	Wireless LED always on.	Make change of JP1, pin1-> +3VL, pin2 -> +3VS.	0.4
4	20, 23	Kensington support	10/18	HP	Removed Kensington support.	Remove JP60, Q122, R2084.	0.4
5	18	Quick-Switch	10/18	Nvidia	We will change Quick switch to PI3HDMI412FT-A	Don't need pull up, removed RP44 ~ RP47.	0.4
6	18	Quick-Switch	10/18	HP	Don't have decoupling for U57 1.5VS.	Add C1583, C1584.	0.4
7	34	KBC Debug port	10/18	HP	Don't need use JP55, JP56 for debug.	Removed JP55, JP56 from S11.	0.4
8	34	RUMRST# timing	10/18	HP	It may don't need these circuit.	Reserve them at S11.(Install R2144, RV : Q128, D73, R2145~2146)	0.4
9	34	RUMRST# timing	10/18	HP	It different to desgn guide 1.1.	Change R2145 to 4.7k, pull up to +3VALW and connect to Q128 base pin.	0.4
10	34	VCC1 Power	11/02	HP	Chnage Design.	Chnage VCC1 power option to +3VALW or +RTCVCC.	0.4
11	21	LANSTATUS#	11/02	HP	System auto power on after plug AC in.	Add Q136 to isolation U10 directly link to NIC, and add PU R2187.	0.4
12	31	USB Switch	11/03	Compal	Don't need dual layout for USB power switch.	Remove U7, U36.	0.4
13	30	Audio	11/03	HP	To pass Vista test of Audio.	Change R207, R217 from 15ohm to 56.2ohm.	0.4
14	25	LAN	11/06	Intel	Intel Santa Rosa Platform Message of the WW44	Change R1903 from 3.92Kohm to 1.4Kohm.	0.4
15	24	LAN Connector	11/06	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	Mount C1581, C1582 --> 680pF(0402).	0.4
16	17	MXM Connector	11/08	HP	Need BOM option of SLP_S3# for use G71 or G84.	Add R2190(0ohm).	0.4
17	4	Thermal Senser	11/08	HP	Abita will chnage to new Thermal senser in the future.	Add R2188, R2189(0ohm).	0.4
18	35	MDC	11/08	HP	Implement new MDC future.	Connect JP26.2 to +3VS.	0.4
19	15	FSB Freq Selecter	11/09	HP	Need HW option for 667MHz or 800MHZ	Add JP62, JP63 and install R1689,R1696,R1705,R1737 and reserve R1694,R1716,R1734.	0.4
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21	37	M-Power discharge	11/10	Compal	It's wrong connection of discharge control circuit.	Correct Q97, Q98, Q99 pin2 connect to LAN_WOL_EN#.	0.4
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	FP Connector	12/18	Compal	ME ask to change FP connector.	Change FP connector(JP15) to same as JP58.	0.5
2	34	KBC	12/18	HP	System can't power on.(PWR1 connect to +3VALW)	PWR1 will modify connect to +3VL(R1908.2).	0.5
3	35	PLTRST/CBB	12/18	HP	Capacitive Button Board may not need PLTRST.	Disconnect PLT_RST# from JP1.3.	0.5
4	38	KBC Power good	12/19	HP	VCC1_PWRGD have glitch when plug AC/DC power.	Del U54, Q106 and R1978, replace by U15.	0.5
5	25	LAN ENERGY DET	12/19	Intel	Intel request chnage value of R1903.	Change R1903 from 1.4K to 1.87Kohm.	0.5
6	38	PWR_GD	12/19	HP	Ripple noise to cause system auto shutdown issue.	Add C1585(0.1uF) and R2191(1Kohm).	0.5
7	34	KBC	12/20	HP	Current design may possible to damage the KBC.	Change design to add Q137, Q138(2N7002) and R2192(100Kohm), R2193(1Kohm).	0.5
8	27	Card bus Controller	12/21	Compal	There is pop noise when plug some PCMCIA card.	Add R2194 and C1586 and change value for R2038 and R2041.	0.5
9	24	NIC	12/21	Intel	82566MM may have start-up issue with Crystal.	Modify layout and add R2195(0ohm).	0.5
10	24	ACBS	01/02	Intel	To enable iAMT and support ACBS.	Mount Q85 and R2072 but remove Q87~Q88 and R1877.	0.5
11	35	Power Buttom	01/04	Compal	ESD test is not good for Switch board.	Add ESD diode(D79) to M/B and add ME solution.	0.5
12	24	NIC	01/05	Compal	EMI test is fail from NIC.	Add C1587~C1590, L24 and change C1421 to 820pF, R12~R13 to FBMA-10-100505-151T.	0.5
13	38	LAN Reset	01/05	HP	HP request to modify.	Change this power rail from +3VM_LAN to +3VM.	0.5
14	18	Quick-Switch	01/07	HP	There is leakage issue of Q-Switch.	Add D80 for this issue.	0.5
15	37	MXM	01/10	HP	MXM board need external +2.5VS power rail.	Add U62, C1592, C1593 for this issue.	0.5
16	37	MXM	01/11	HP	2.5VS for MXM is too long.	Reserve C1594(0.1uF) close to pin.	0.5
17	37	MXM	01/12	HP	Leakage issue from MXM pin211(ADP_PRES)	Add Q139(RHU002N06) & R2196(8.2K).	0.5
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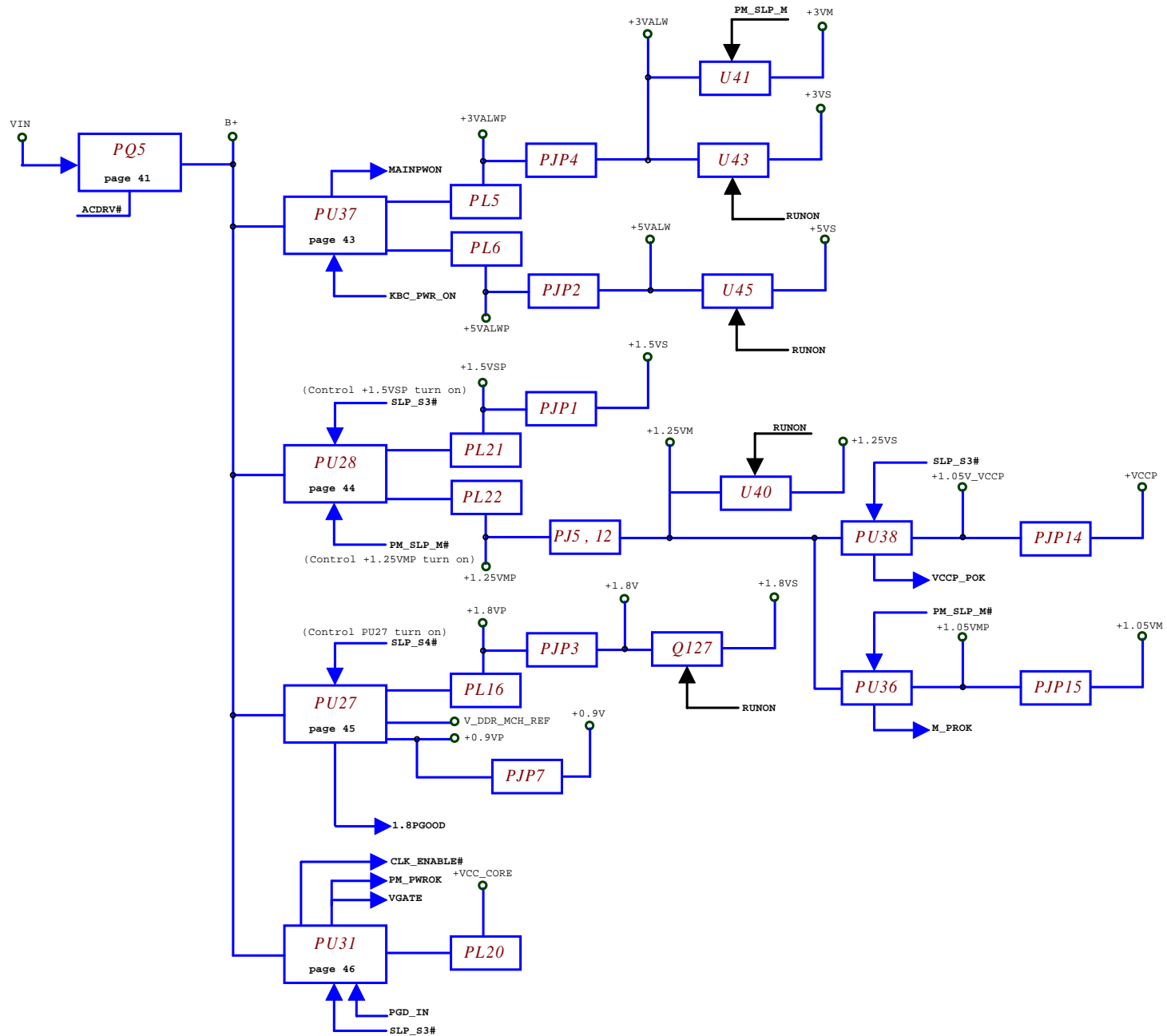
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	USB Connector	02/07	Compal	Not need 40 pin connector for USB/Audio connector.	Change JP25 from 40pin to 30pin.	0.6
2	34	KBC VCC0	02/07	Compal	Can't power on and AC power LED always light.	Change R2179 connect to +3VL, and add option R2197 to GND.	0.6
3	33	FPR/USB S3/S4	02/12	HP	Change control method for FPR/USB power in S3/S4.	Add R2198, R2200~R2202, Q140~Q141.	0.6
4	37	WOL control	02/14	HP	Add 100K pull up for LAN_WOL_EN.	Add R2203(100Kohm).	0.6
5	29	SPDIF	02/14	HP	HP request to add 4.7K pull down on SPDIF out.	Add R2206(4.7Kohm).	0.6
6	29	Card reader	02/14	HP	Need reserve some test point.	Add R2205(0ohm) and T94.	0.6
7	17	MXM thermal pin	02/14	HP	Isolation MXM_THERM# and PWR_GD use MOSFET.	Add Q142 and R2204 for the modify.	0.6
8	30	USB Connector	02/28	HP	Couple mV over the 150mV GS limits.	Change R207, R217 from 56.2 ohm to 60.4 ohm.	0.6
9	21	THERM_SCI#	02/28	HP	HP request to design change.	Remove R1854 from BOM list.	0.6
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	15	Clock Gen	03/19	HP	Remove Ohm damping of differential clock pair.	Remove RP49, RP51~RP57, reserve RP48.	0.8
2	15	FSB selector	03/19	HP	Remove FSB selection function. Remove JP62, JP63, Reserve R1689, R1696, R1705, R1737, install R1694, R1716, R1734.		0.8
3	29	Audio Codec	03/19	HP	To improve audio quality of docking.	Change R290~R291 to 6.04K and R289, R292 to 2K.	0.8
4	20	GPU Thermal	03/19	HP	Design change for MXM board.	Reserve R1854.	0.8
5	26	NAND Card	03/23	HP	Don't need this function for MP.	Reserve R2064, R2065, C1553 ~ C1560.	0.8
6	21	OC6#/GPIO30	03/23	HP	This pin is not long use for MXM.	Reserve R2207 for isolation.	0.8
7	38	POK CKT	03/28	Compal	For schematic leverage to Chimay.	Change LMV331(U47,U48) to LM393(U47), and remove R1976, C1487	0.8
8	24	NIC power	03/28	Compal	Don't need +V1.0M_LAN power regulator.	Remove Q90, C1436 ~ C1440.	0.8
9	31	USB Port	03/28	Compal	To correct schematic and make layout smooth.	Remove C118, C498, C499, R49 and change C126 to 330uF.	0.8
10	31	BT	03/28	Compal	To make layout smoothly.	Remove D16.	0.8
11	34	KBC Clock	03/28	Compal	To make layout smoothly and EMI request.	Remove R1929, C1455.	0.8
12	21	LAN/WLAN Switch	03/30	HP	Unplug AC, WLAN will be disabled on XP OS.	Add U63 for solve leakage issue of enable ACBS.	0.8
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	NB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q114~Q117, R2049~R2052, install R111, R113, R122, R132.	1.0
2	22	SB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q118~Q121, R2058~R2061, install R138~R141.	1.0
3	22	Audio Codec	05/02	HP	To improve ICH_V5REF_RUN of SB.	Change C1190 from 0.1uF to 1uF.	1.0
4	36	Easy crack issue	05/14	HP	To prevent crack issue for L14	Change L14 material to SM010008E10.	1.0
5	14	DDR DIMM B	5/15	HP	To solve OTS issue OTS 265441 and 261307.	Change R33 pin2 connect to +3VM.	1.0
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