



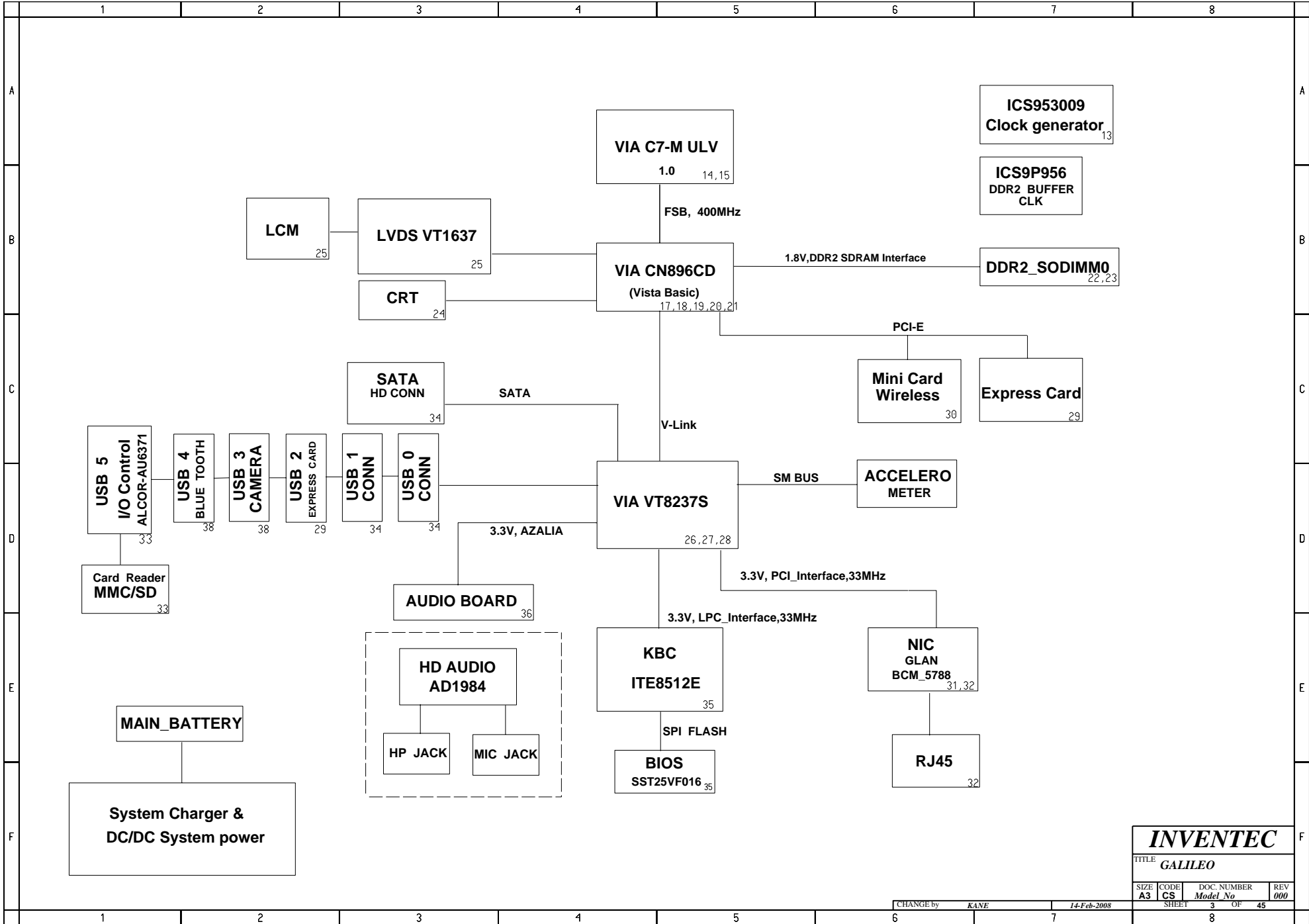
## TABLE OF CONTENTS

PAGE	PAGE
1. COVER PAGE	23.DDR2 PULL UP TERMINATOR
2. INDEX	24.CRT
3. BLOCK DIAGRAM	25.LCM CONN & LVDS TRANSMITTER
4. POWER SEQUENCE BLOCK	26.S/B VT8237S 1
5. CHARGER & OCP	27.S/B VT8237S 2
6. SELECT & BATTERY CONN	28.S/B VT8237S 3
7. SYSTEM POWER (3V/5V)	29.EXPRESS CARD
8. SYSTEM POWER (1.5V/1.8V)	30.MINICARD CONN ( WIRELESS LAN )
9. CPU CORE POWER	31.LAN CONTROLLER 1
10.VCCP / 0.9V	32.LAN CONTROLLER 2 & RJ45
11-12. POWER SLEEP	33.CARD READER
13.CLOCK GENERATOR & ICS9P956	34.USB & SATA CONN & ACCELEROMETER
14.CPU VIA C7-M ULV -1	35.KBC
15.CPU VIA C7-M ULV -2	36.KEYBOARD CONN
16.FAN & THERMAL CONTROLLER	37.SWITCH & LED (MB)
17.N/B VN896CD 1	38.BLUETOOTH CONN & CAMERA
18.N/B VN896CD 2	39.EMI CAP
19.N/B VN896CD 3	
20.N/B VN896CD 4	
21.N/B VN896CD 5	
22.DDR2 DIMMO	

**INVENTEC**

TITLE *GALILEO*

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
CHANGE by <i>KANE</i>		30-Oct-2007	SHEET <b>2</b> OF <b>45</b>



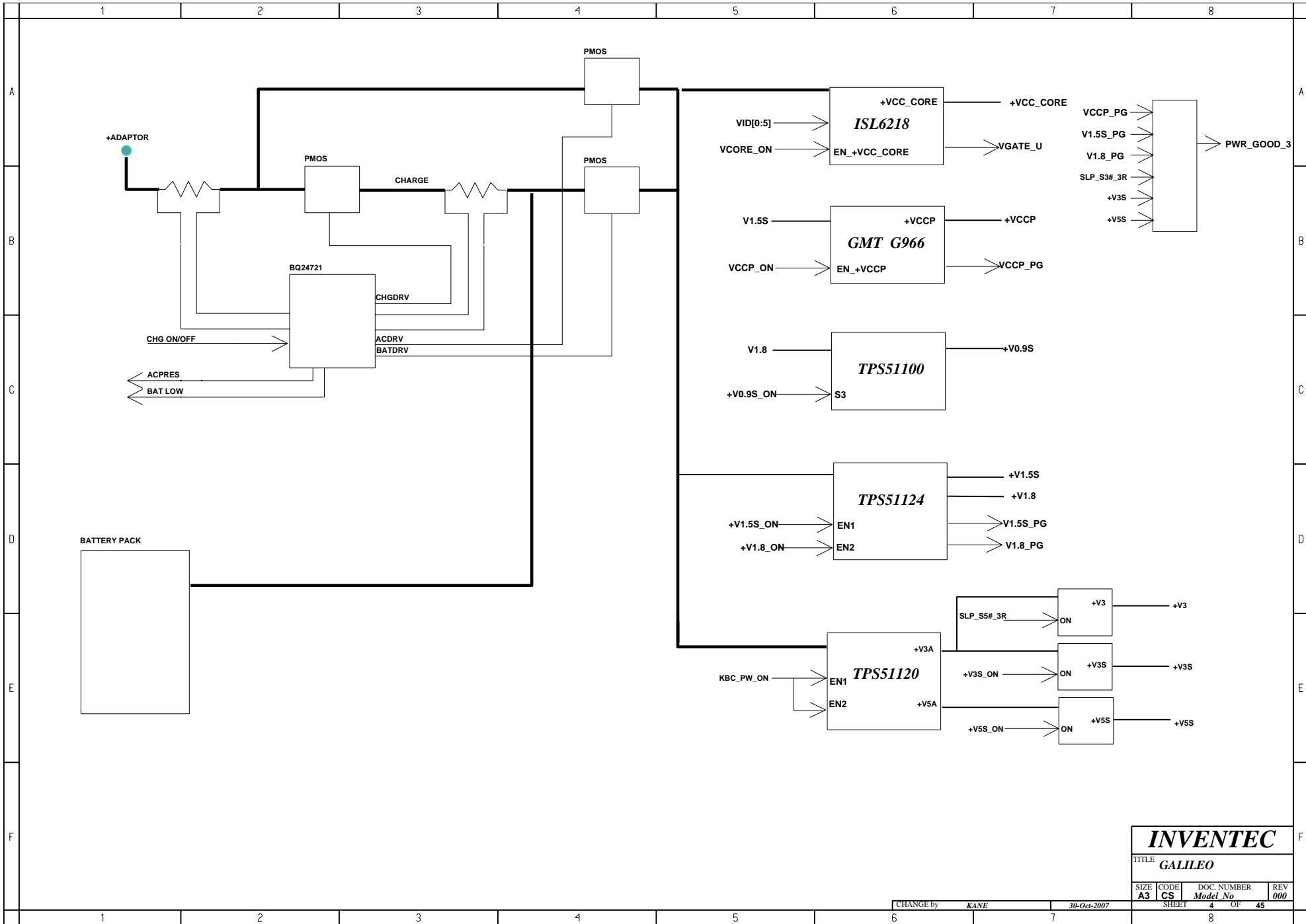
**INVENTEC**

TITLE GALILEO

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
-------------------	-------------------	--------------------------------	-------------------

CHANGE by *KANE* 14-Feb-2008

SHEET 3 OF 45



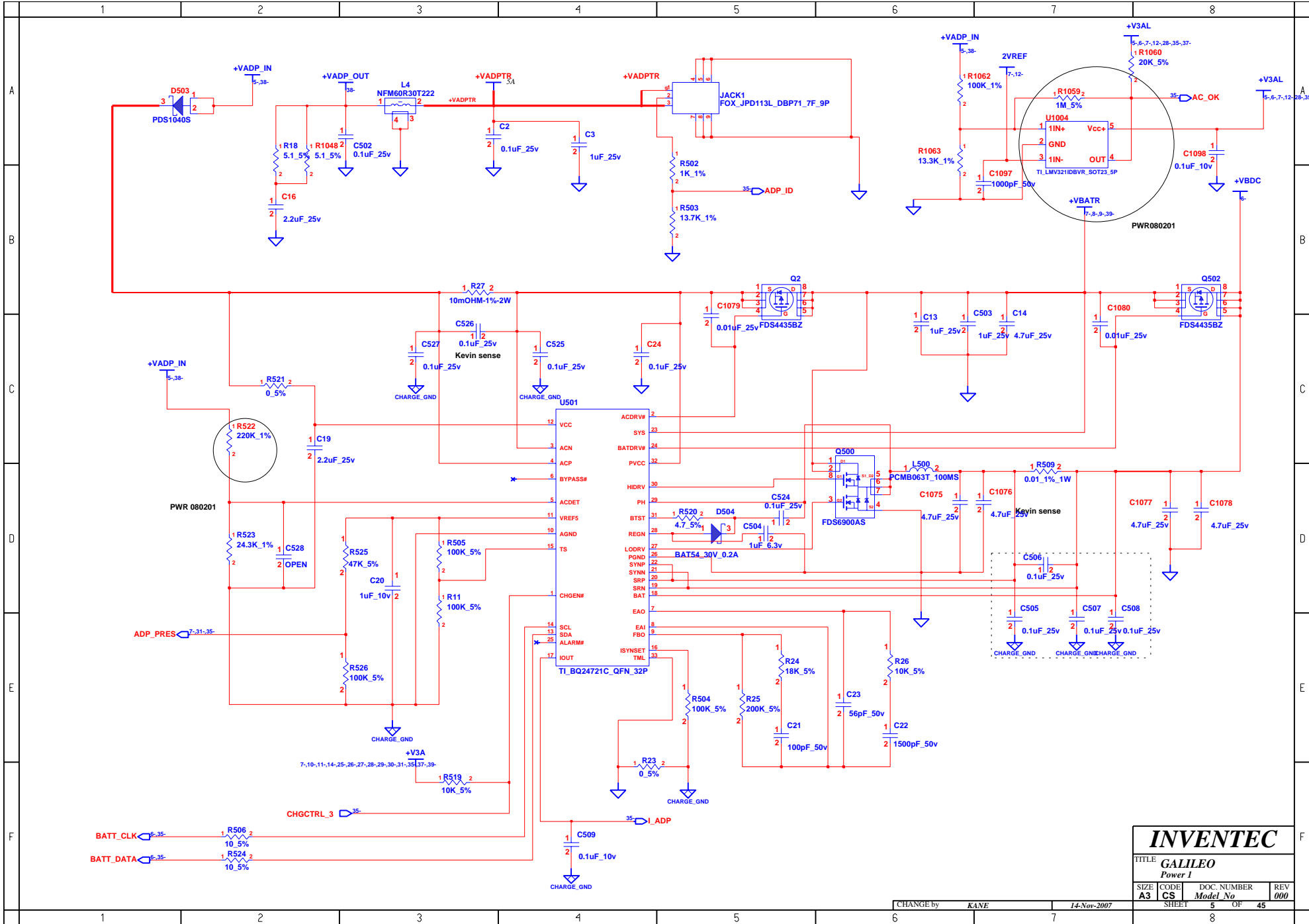
**INVENTEC**

TITLE **GALILEO**

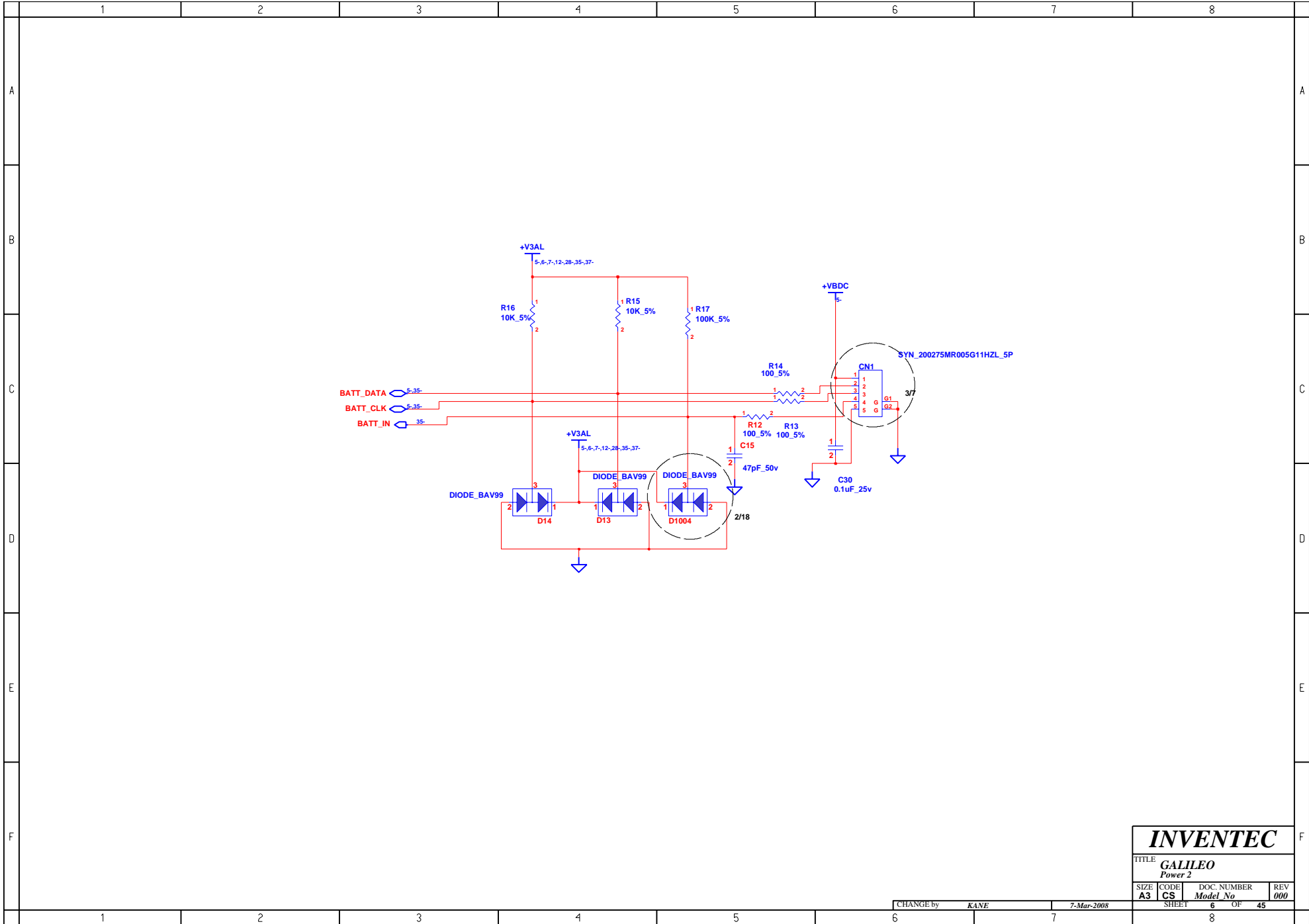
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000

CHANGE by *KANE* 30-Oct-2007

SHEET 4 OF 45



<b>INVENTEC</b>			
TITLE <b>GALILEO</b> <i>Power 1</i>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000
CHANGE by		14-Nov-2007	
KANE		SHEET 5 OF 45	

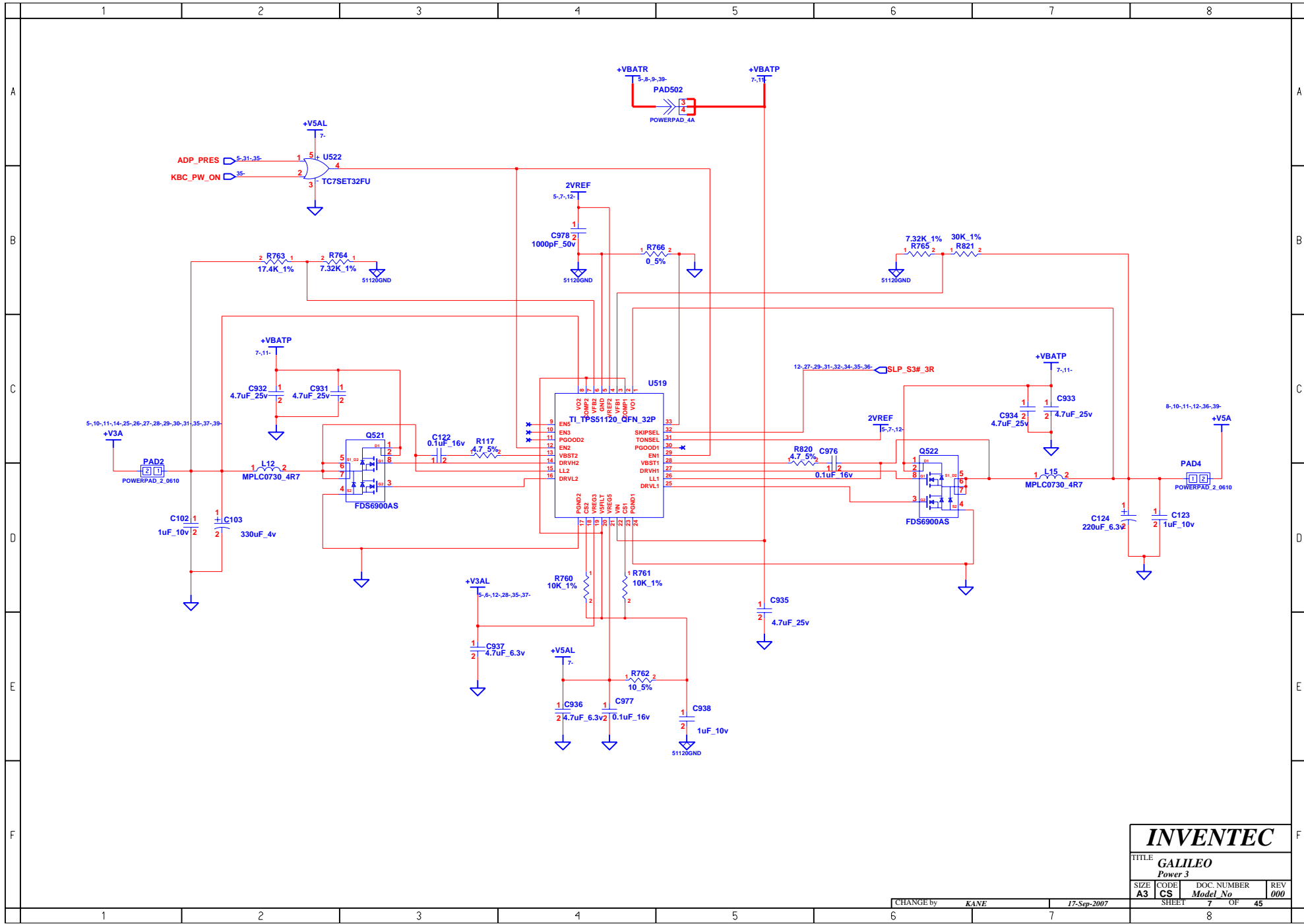


**INVENTEC**

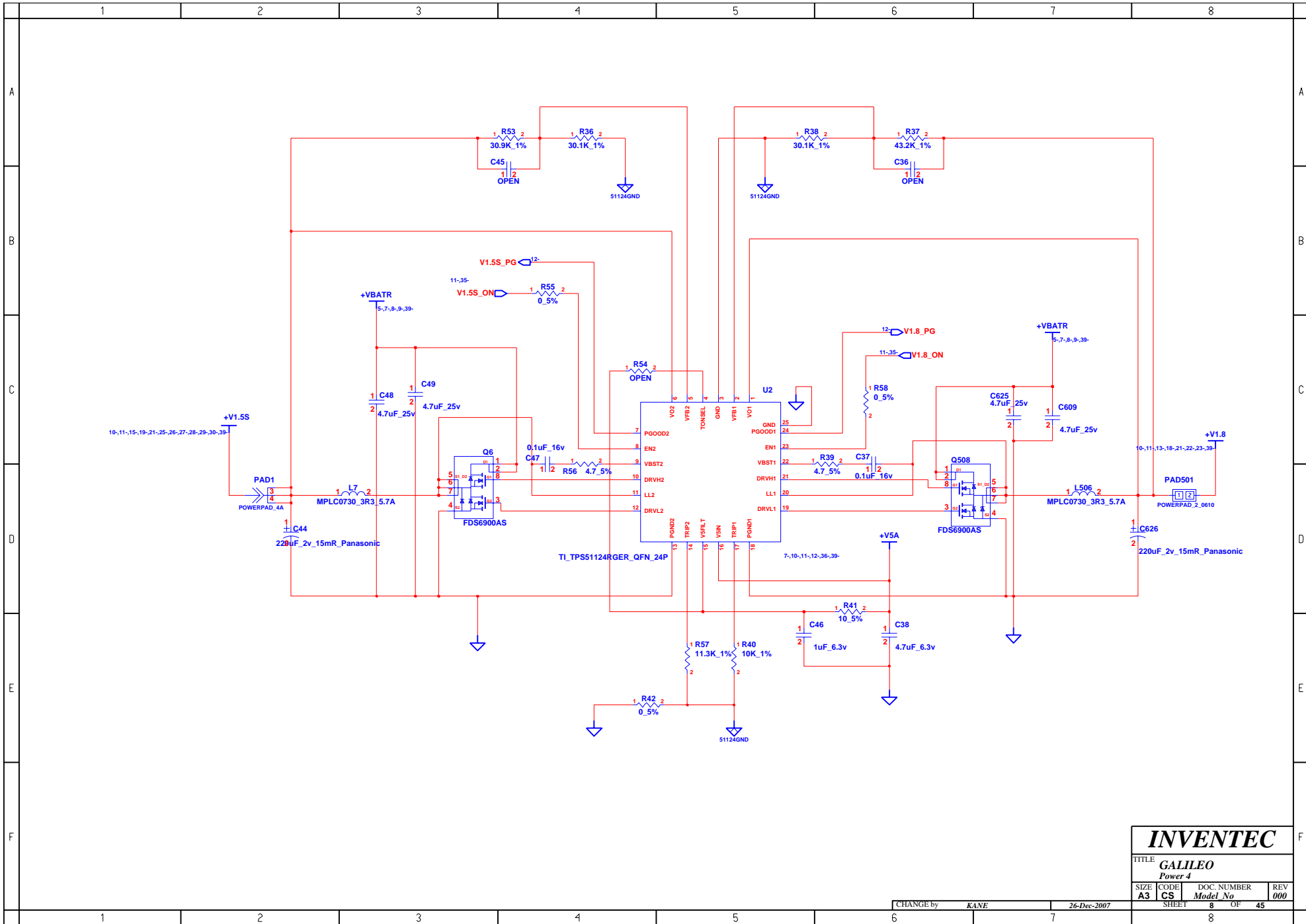
TITLE			
GALILEO			
Power 2			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000

CHANGE by KANE 7-Mar-2008

SHEET 6 OF 45



<b>INVENTEC</b>			
TITLE <b>GALILEO</b> <i>Power 3</i>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
CHANGE by <b>KANE</b>		17-Sep-2007	
SHEET <b>7</b>		OF <b>45</b>	



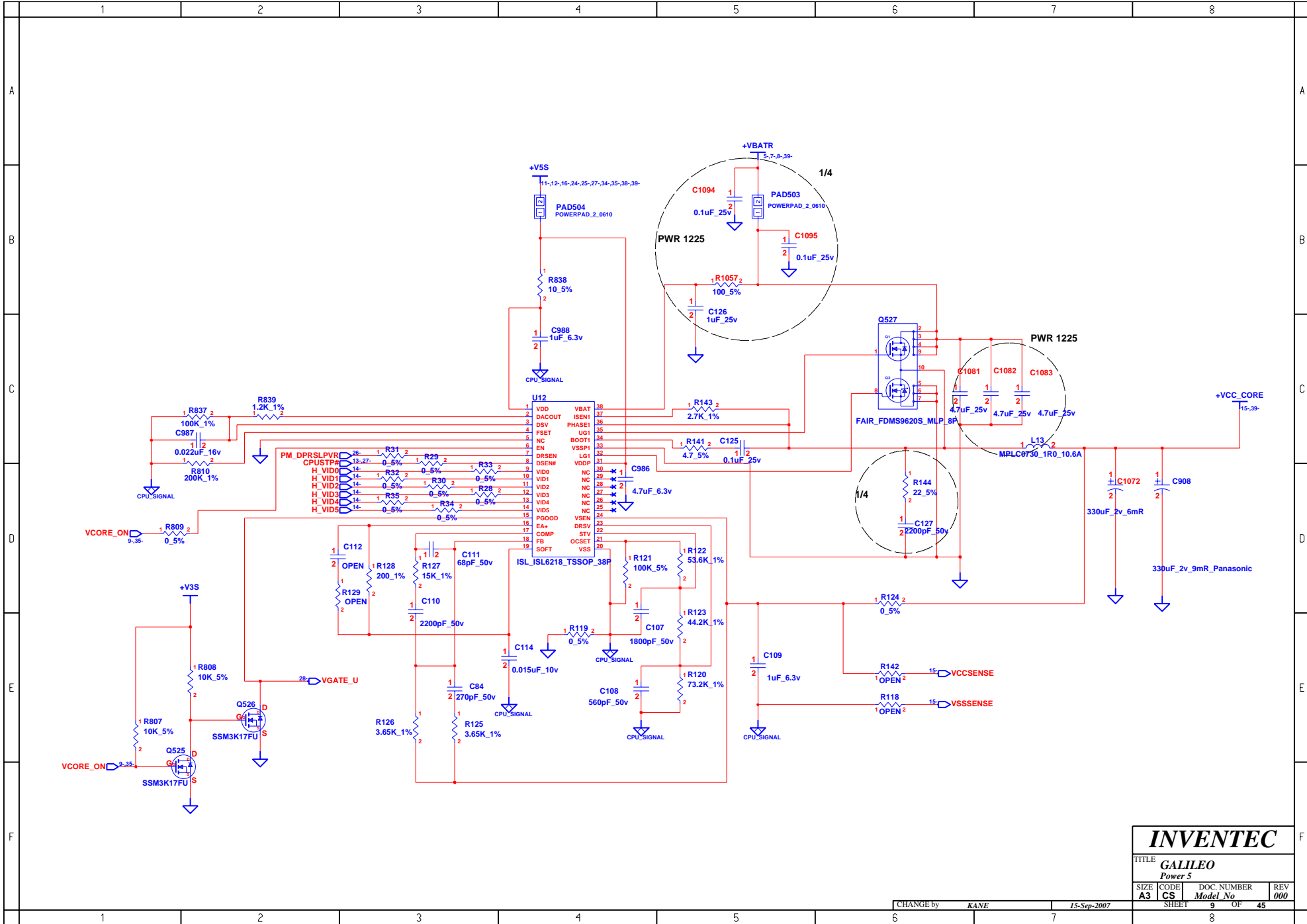
# INVENTEC

TITLE **GALILEO**  
**Power 4**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000

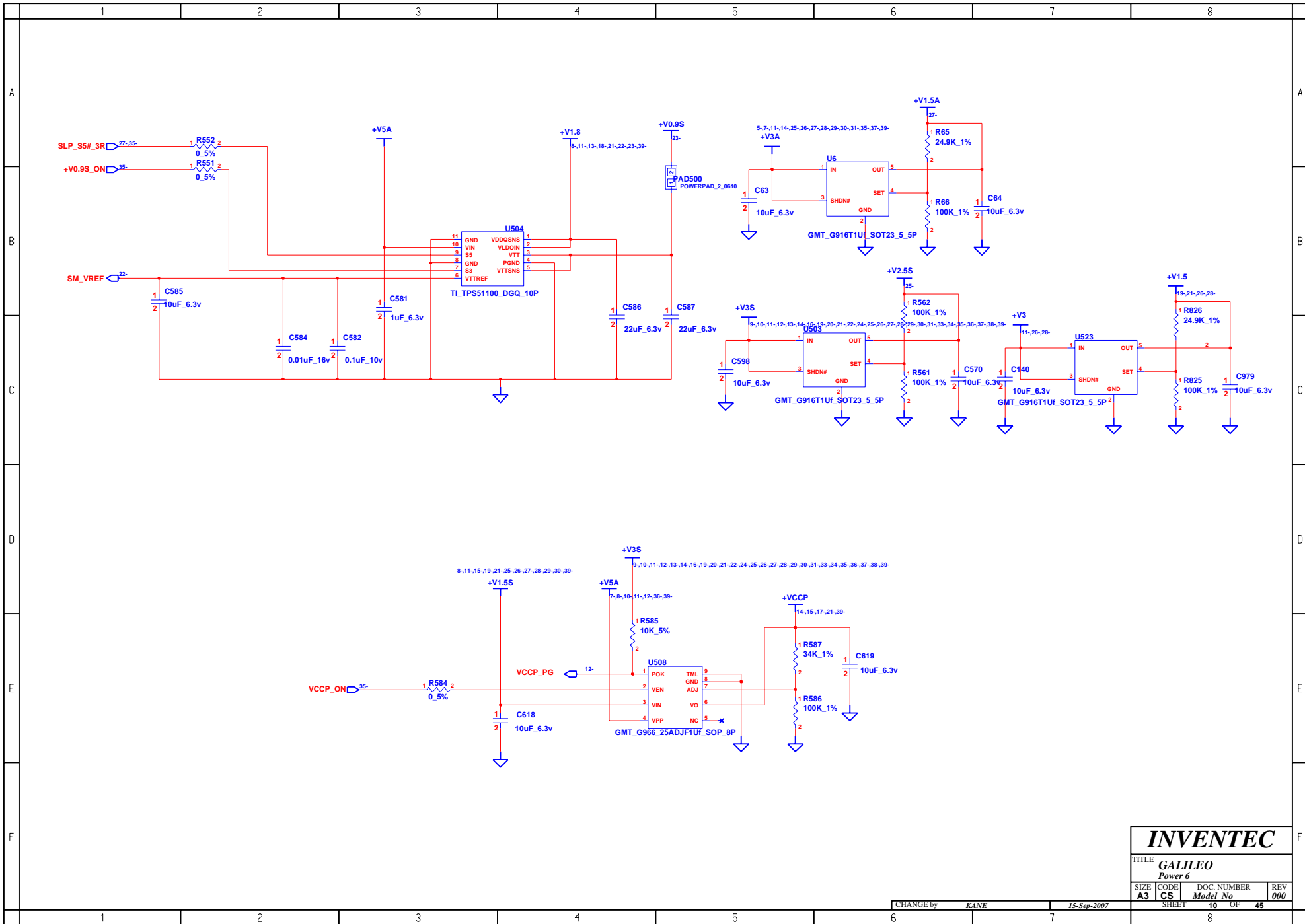
CHANGE by **KANE** 26-Dec-2007  
 SHEET 8 OF 45





# INVENTEC

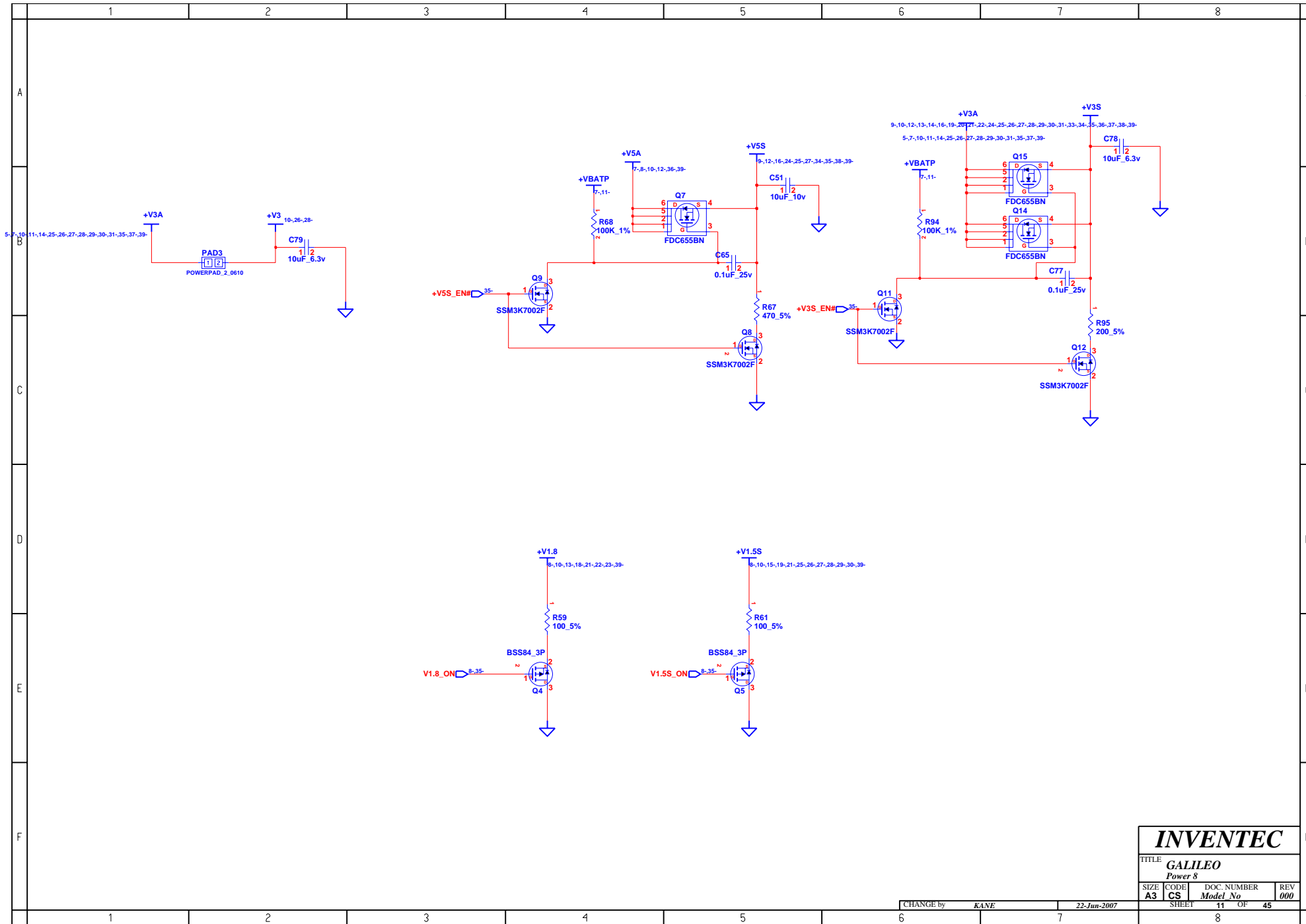
TITLE			
GALILEO			
Power 5			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000



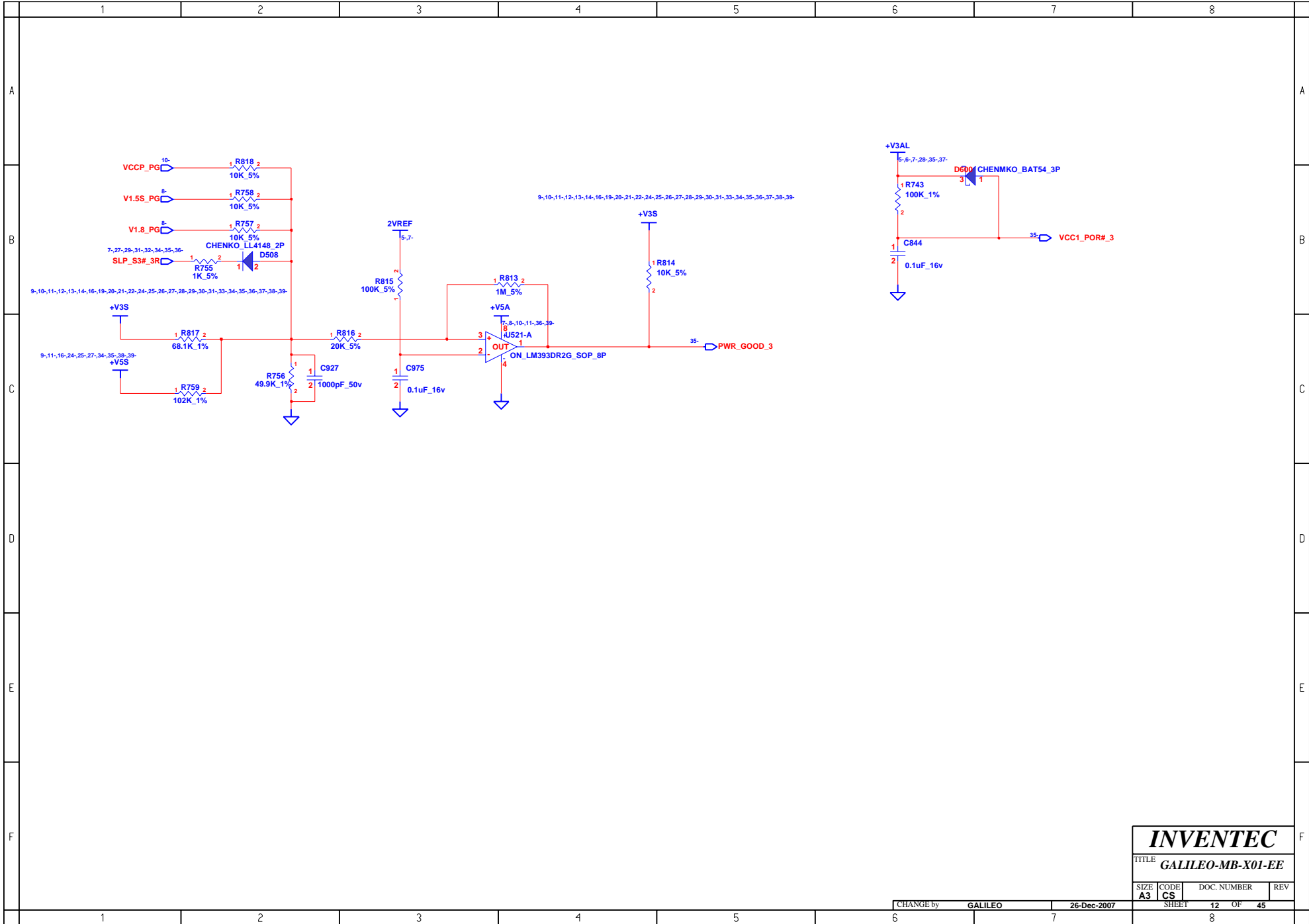
# INVENTEC

TITLE			
GALILEO			
Power 6			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000
CHANGE by		SHEET	
KANE		10 OF 45	

15-Sep-2007



<b>INVENTEC</b>			
TITLE <b>GALILEO</b>			
Power 8			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000
CHANGE by KANE		22-Jun-2007	SHEET 11 OF 45



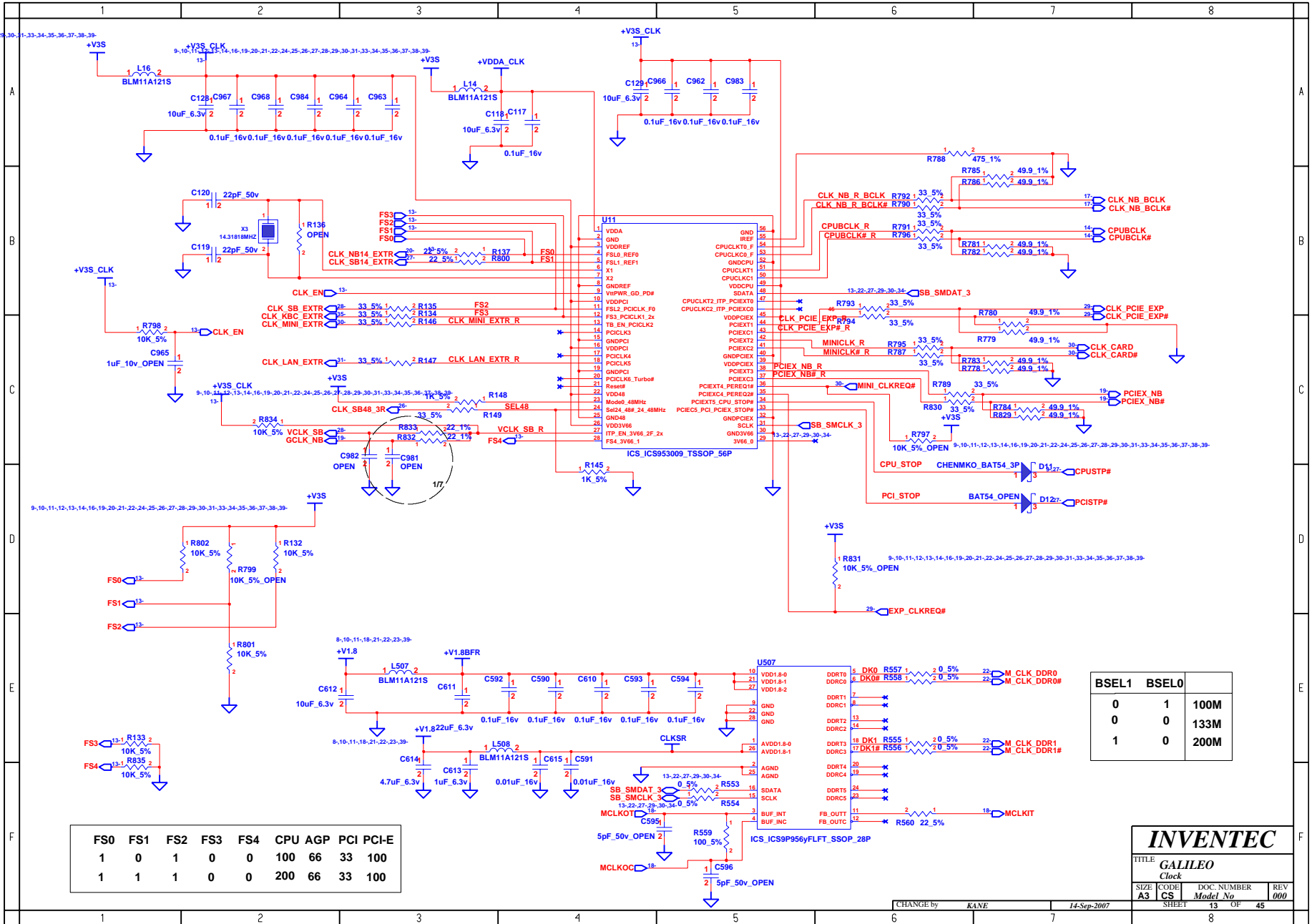
**INVENTEC**

TITLE GALILEO-MB-X01-EE

SIZE A3	CODE CS	DOC. NUMBER 12 OF 45	REV
------------	------------	-------------------------	-----

CHANGE by GALILEO 26-Dec-2007

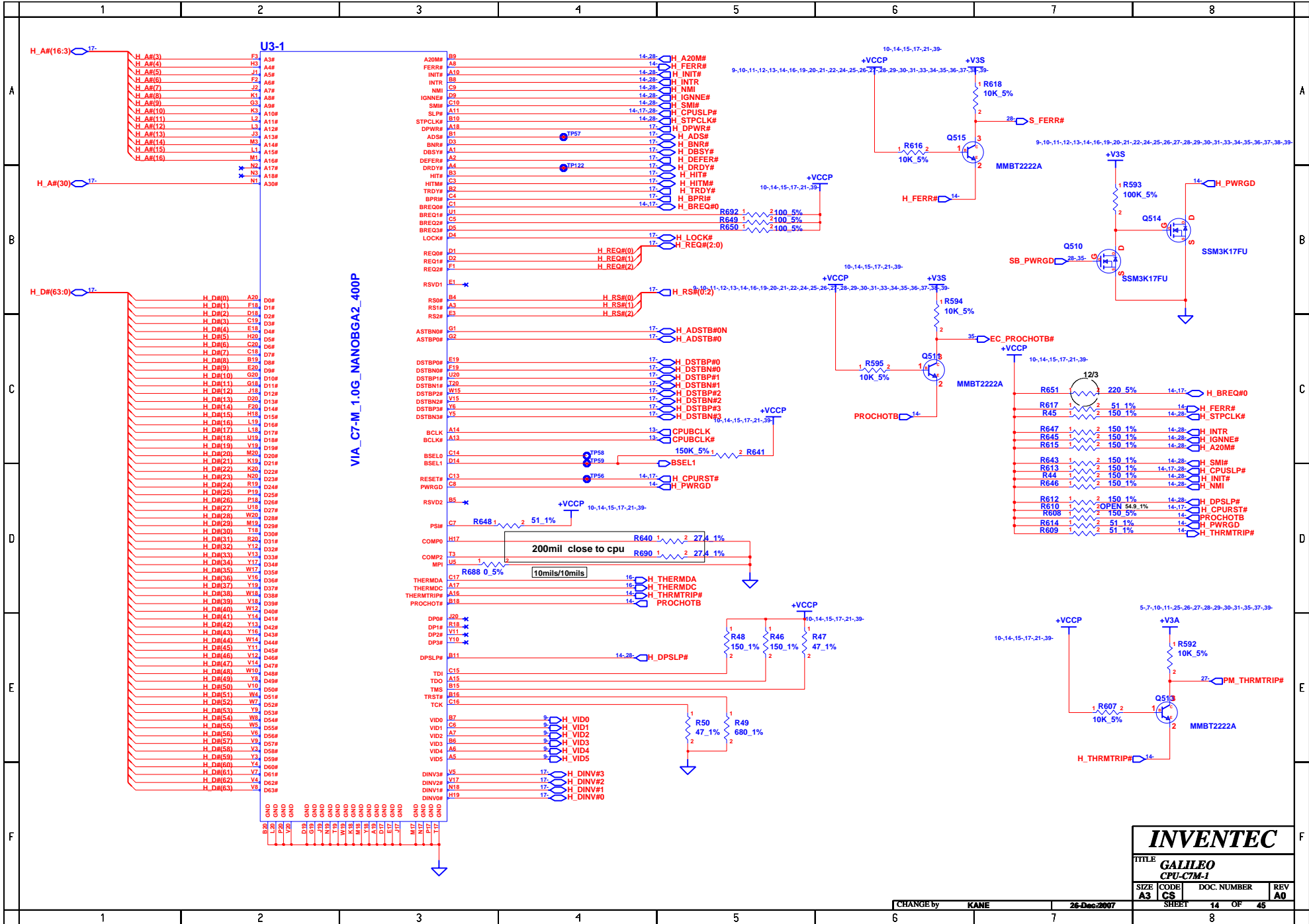
SHEET 8

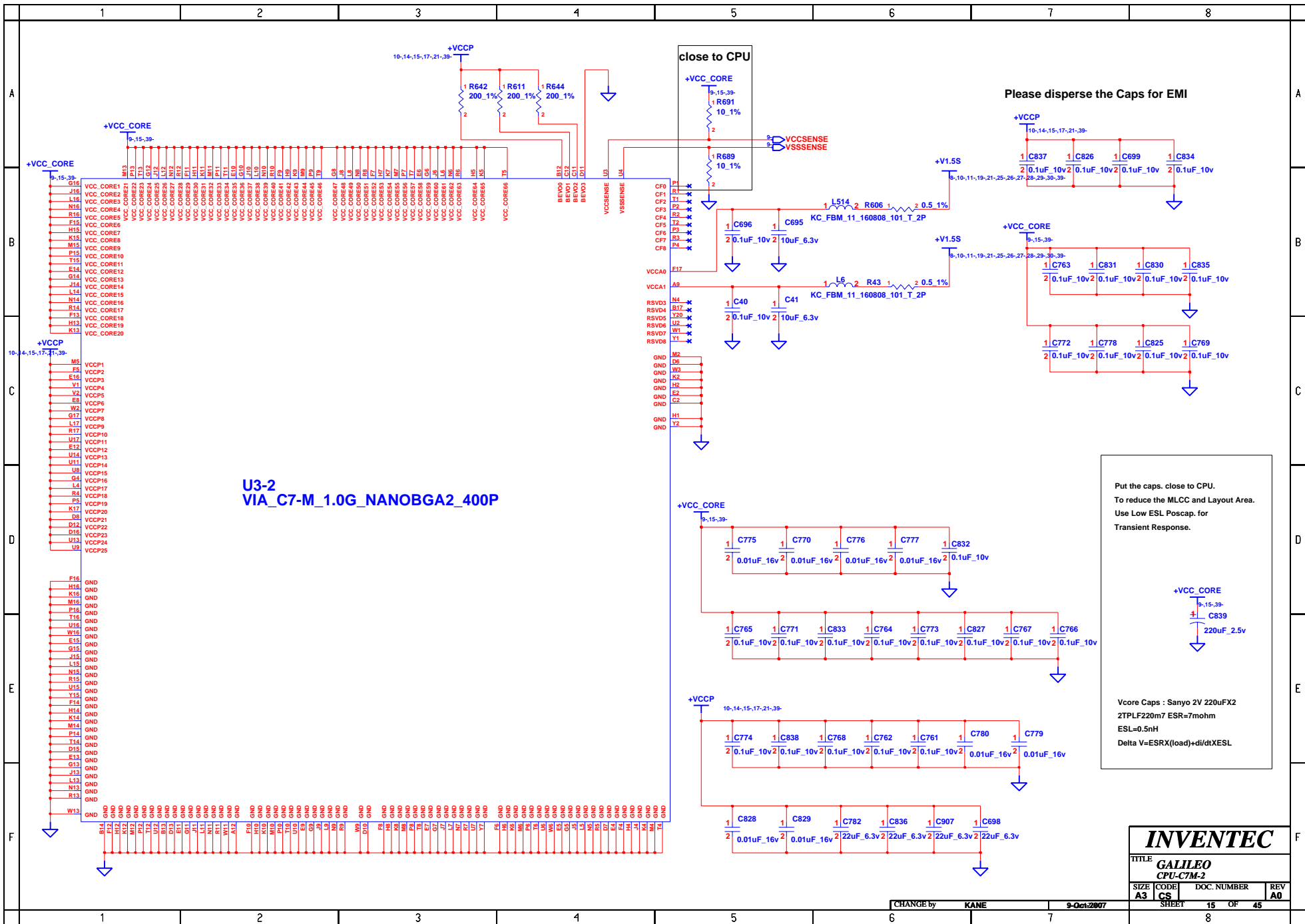


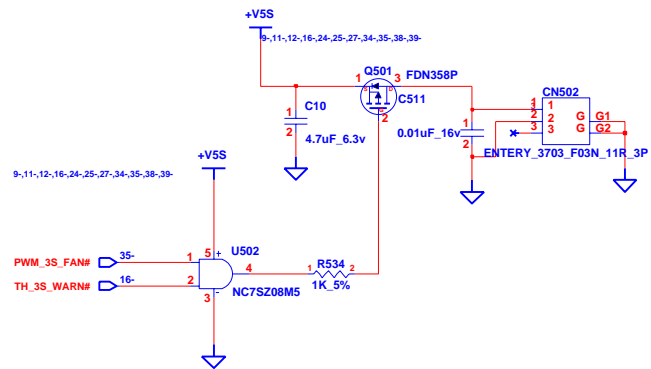
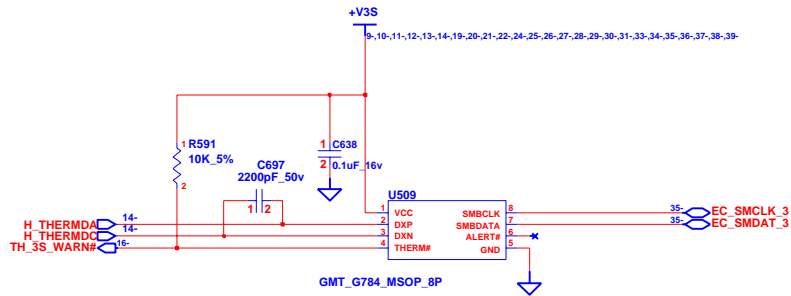
FS0	FS1	FS2	FS3	FS4	CPU	AGP	PCI	PCI-E
1	0	1	0	0	100	66	33	100
1	1	1	0	0	200	66	33	100

BSEL1	BSEL0	
0	1	100M
0	0	133M
1	0	200M

<b>INVENTEC</b>			
TITLE GALILEO			
Clock			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV 000
SHEET 13		OF 45	





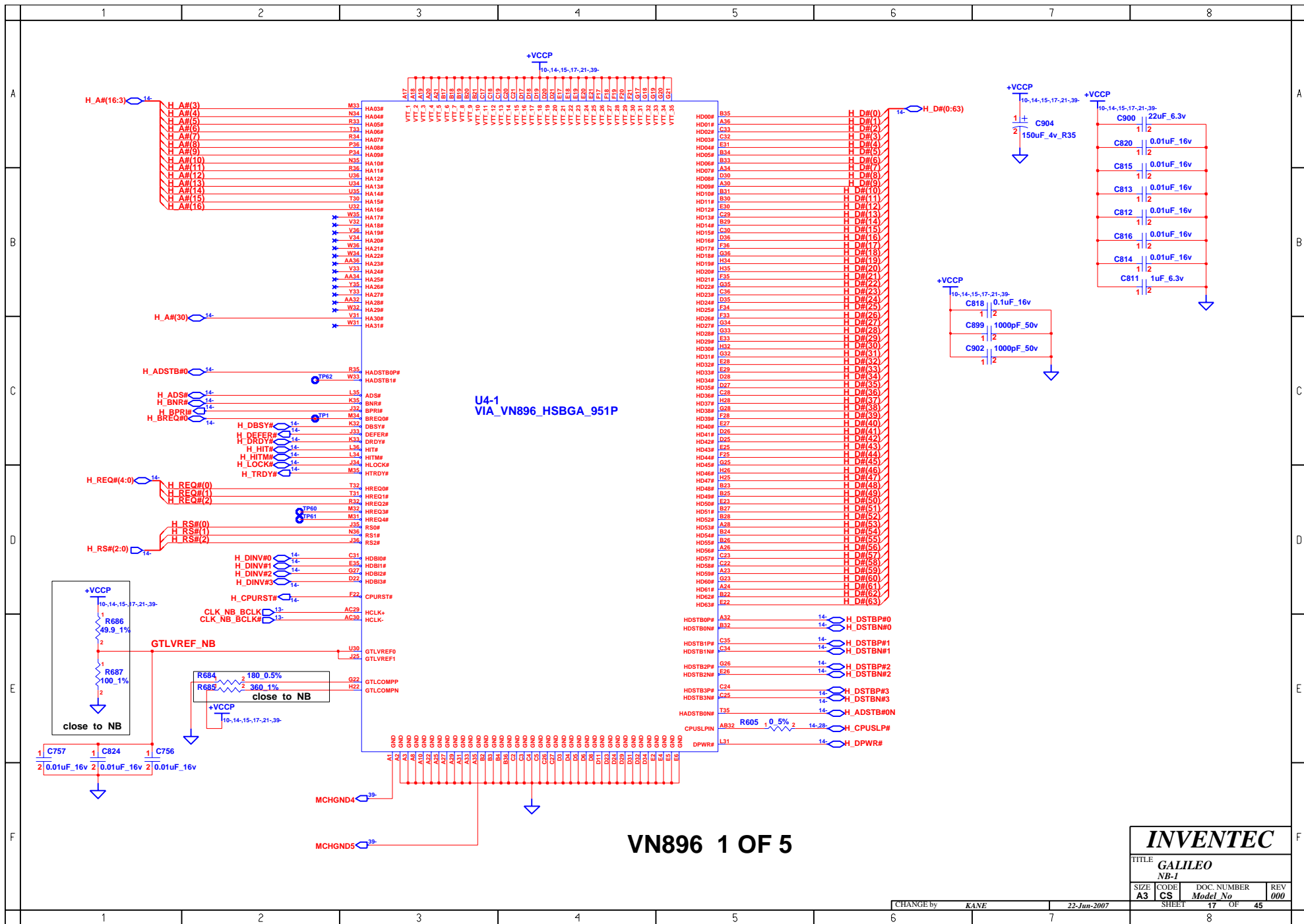


# INVENTEC

TITLE			
GALILEO			
Fan And Thermal			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000
SHEET		16	OF 45

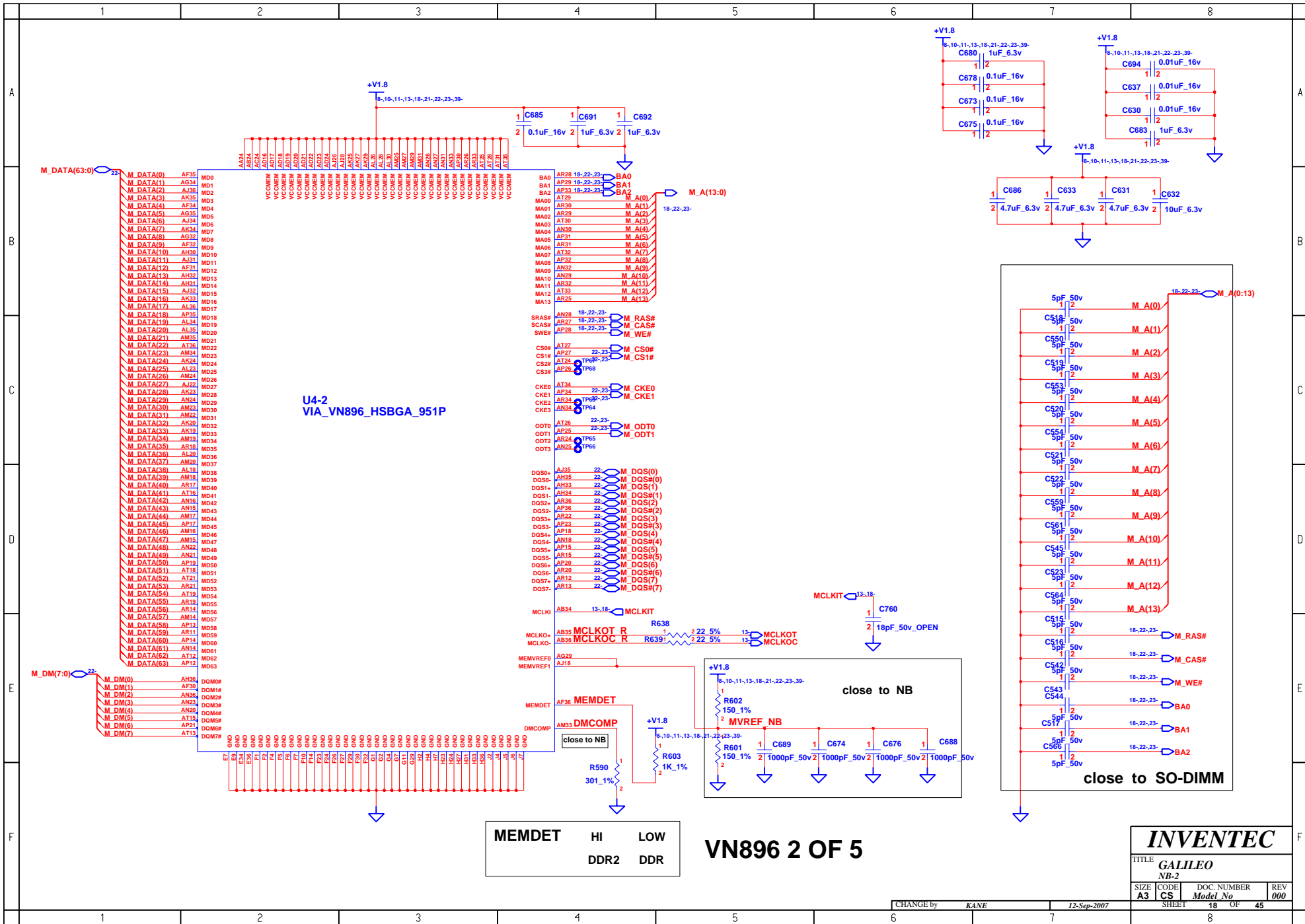
CHANGE by KAANE





VN896 1 OF 5

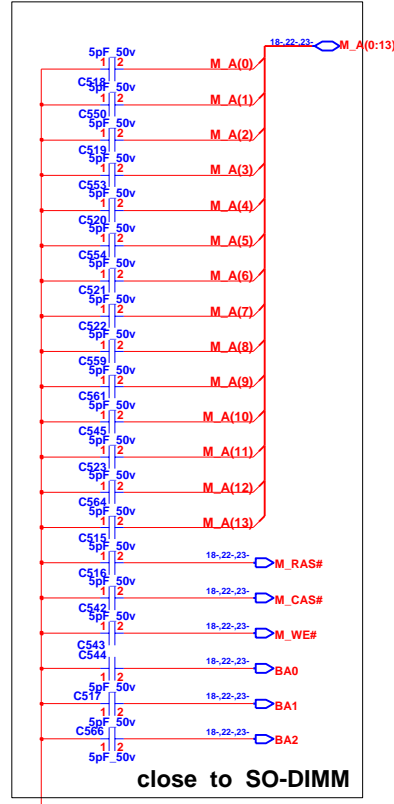
<b>INVENTEC</b>			
TITLE GALILEO			
NB-1			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV 000
CHANGE by KANE		22-Jun-2007	SHEET 17 OF 45



U4-2  
VIA\_VN896\_HSBGA\_951P

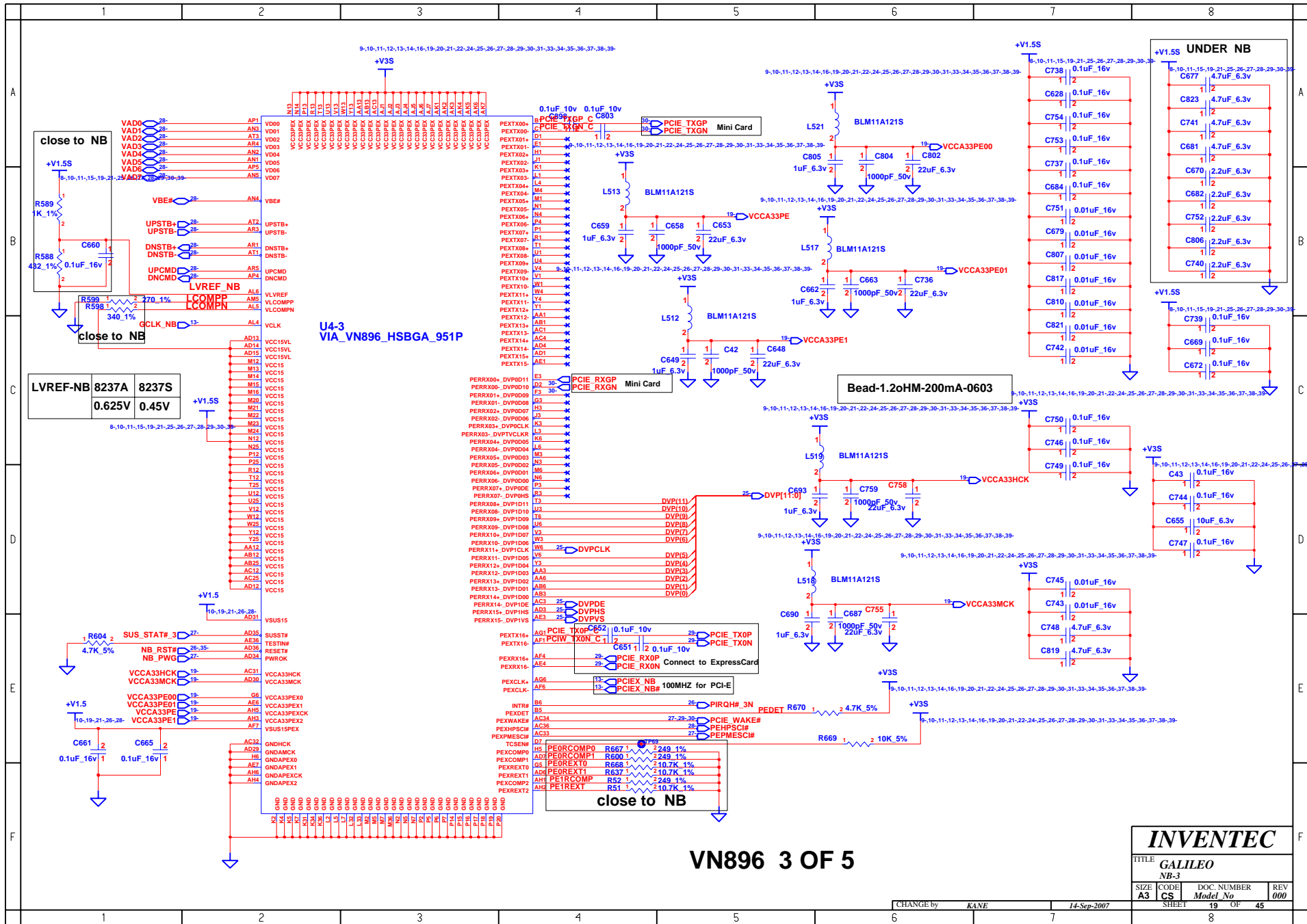
MEMDET HI LOW  
DDR2 DDR

VN896 2 OF 5



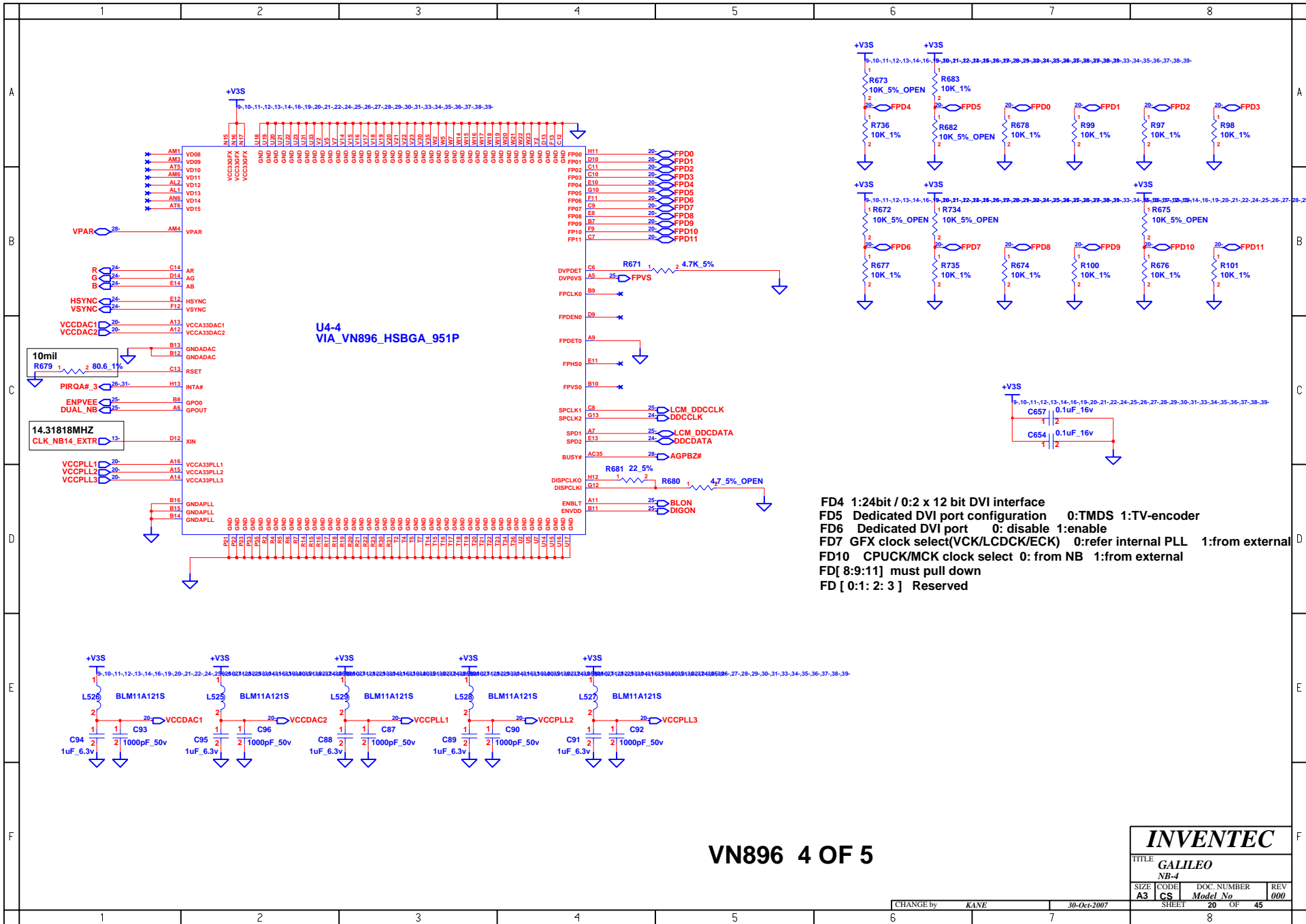
INVENTEC

TITLE			
GALILEO			
NB-2			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000
CHANGE by		12-Sep-2007	
KANE		SHEET 18 OF 45	



VN896 3 OF 5

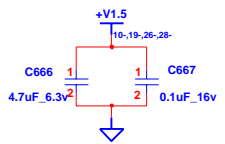
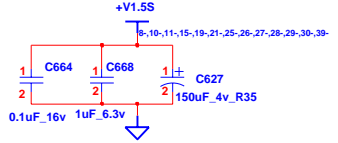
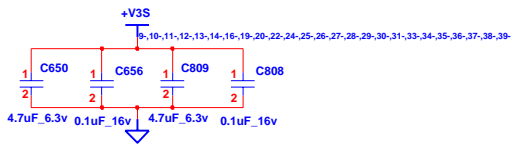
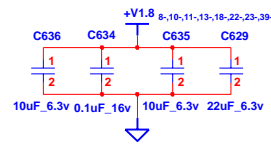
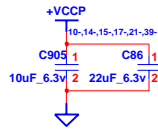
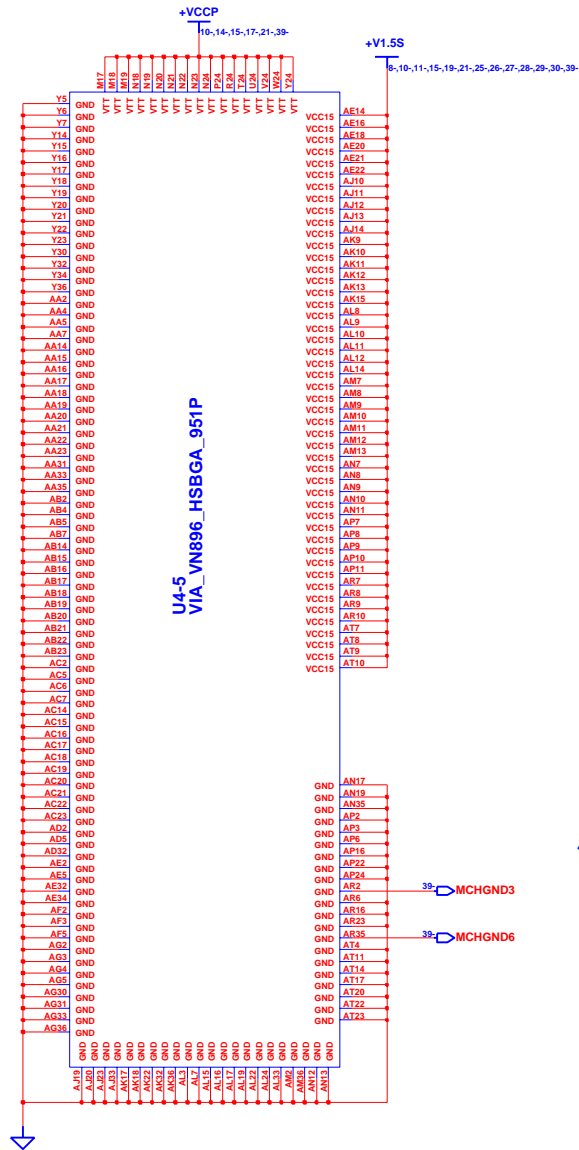
<b>INVENTEC</b>			
TITLE GALILEO			
NB-3			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV 000
CHANGE by		NAME	14-Sep-2007
SHEET 19		OF 45	



FD4 1:24bit / 0:2 x 12 bit DVI interface  
 FD5 Dedicated DVI port configuration 0:TMD5 1:TV-encoder  
 FD6 Dedicated DVI port 0: disable 1:enable  
 FD7 GFX clock select(VCK/LCDCK/ECK) 0:refer internal PLL 1:from external  
 FD10 CPUCK/MCK clock select 0: from NB 1:from external  
 FD[ 8:9:11] must pull down  
 FD [ 0:1: 2: 3 ] Reserved

VN896 4 OF 5

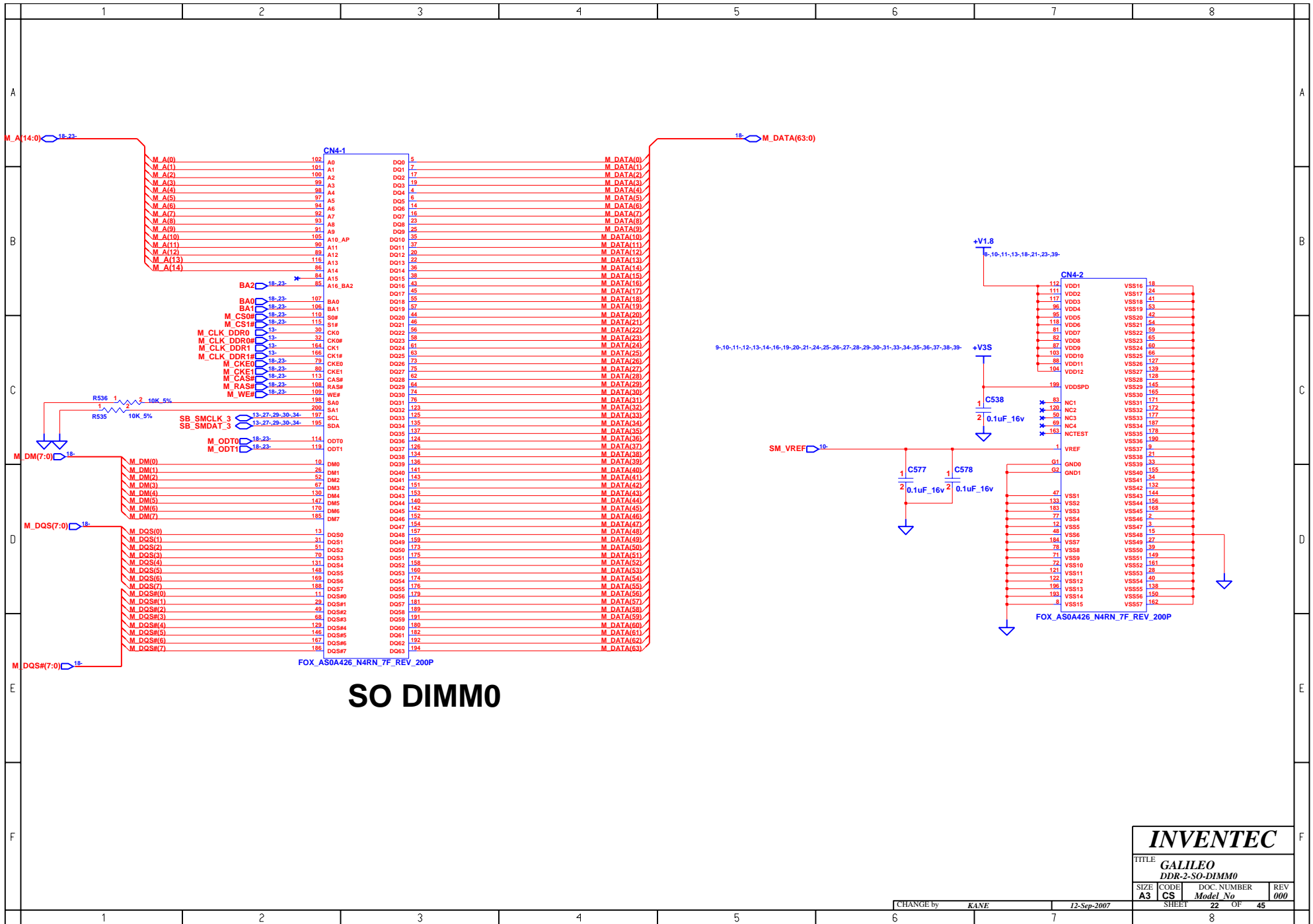
<b>INVENTEC</b>			
TITLE GALILEO			
NB-4			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV 000
CHANGE by KANE		30-Oct-2007	SHEET 20 OF 45



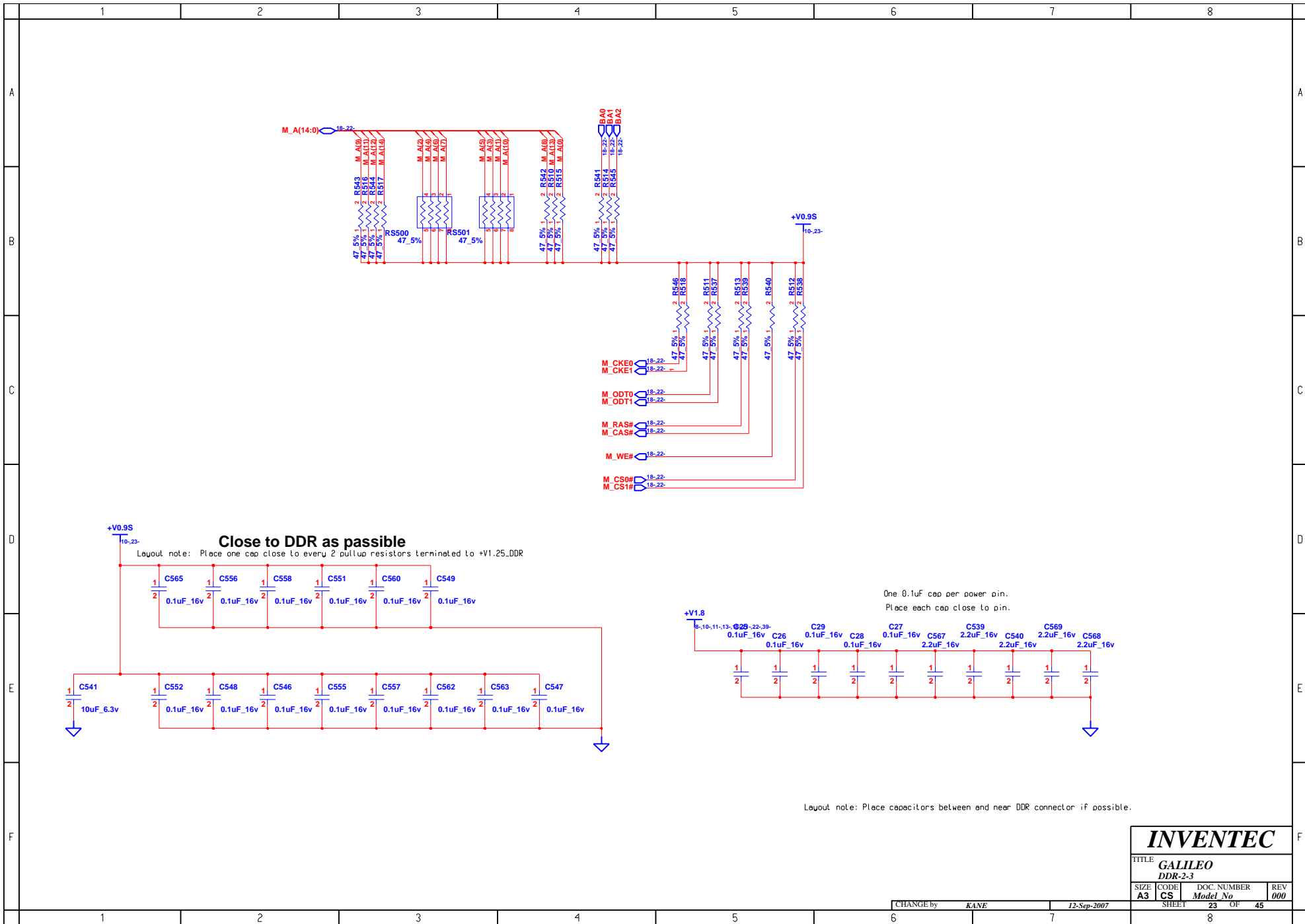
39 MCHGND3  
39 MCHGND6

# VN896 5 OF 5

<b>INVENTEC</b>			
TITLE <b>GALILEO</b>			
NB-5			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>000</b>
CHANGE by <b>KANE</b>		18-Jul-2007	SHEET <b>21</b> OF <b>45</b>



<b>INVENTEC</b>			
TITLE <b>GALILEO</b>			
DDR-2-SO-DIMM0			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>000</b>
CHANGE by <b>KAWE</b>		12-Sep-2007	
SHEET <b>22</b>		OF <b>45</b>	



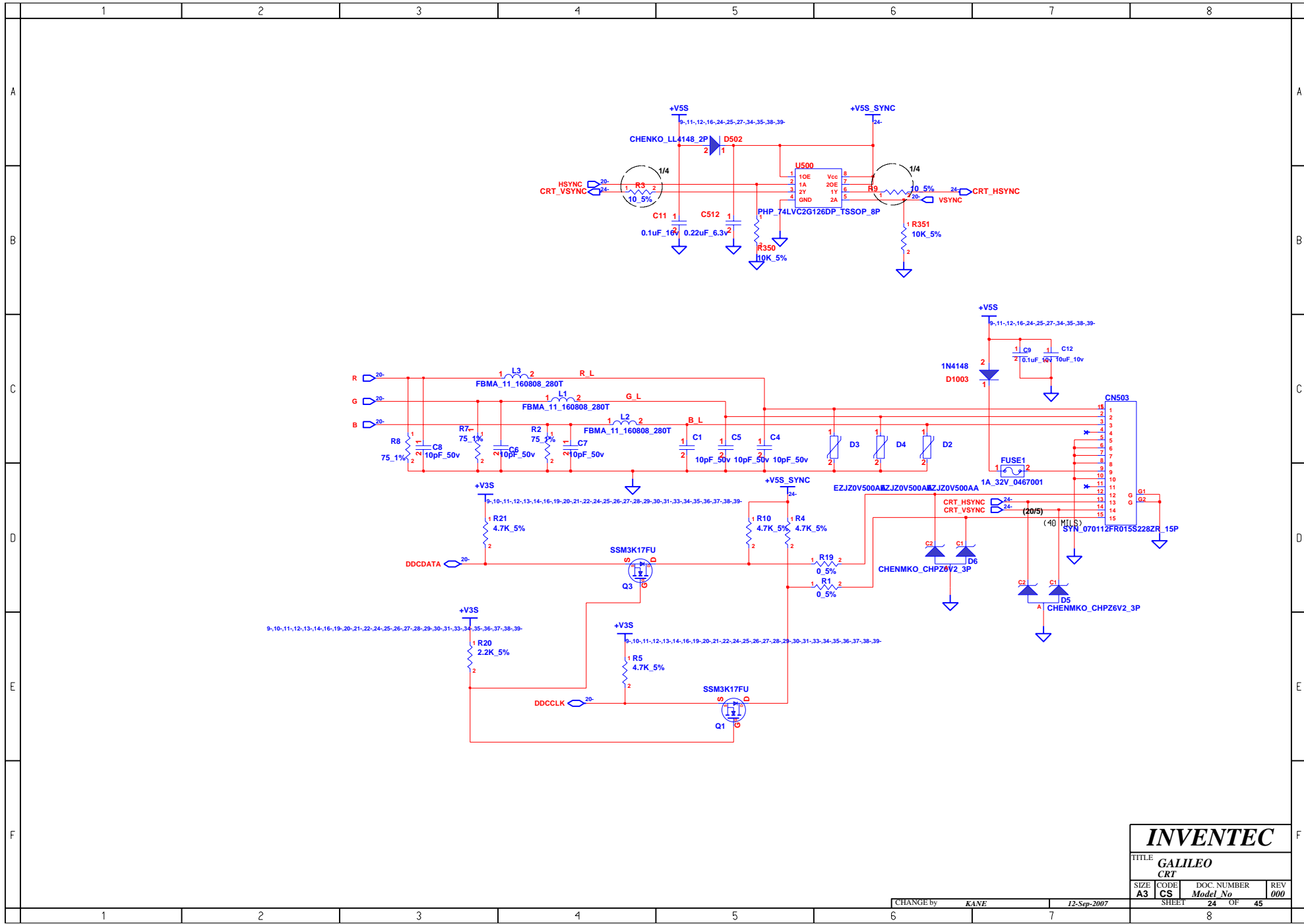
**Close to DDR as possible**

Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25\_DDR

One 0.1uF cap per power pin.  
Place each cap close to pin.

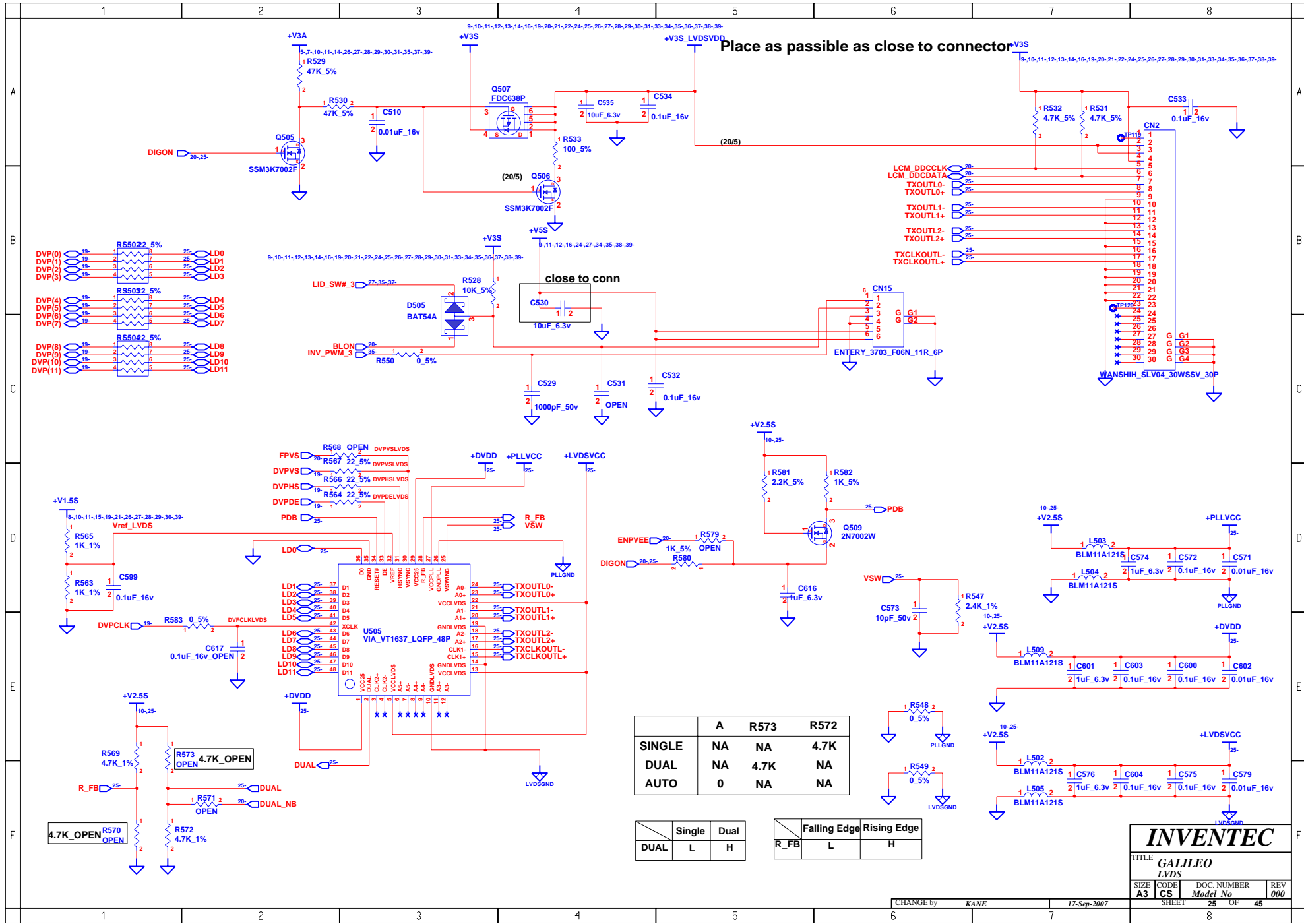
Layout note: Place capacitors between and near DDR connector if possible.

<b>INVENTEC</b>			
TITLE <b>GALILEO DDR-2-3</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
CHANGE by <b>KANE</b>		12-Sep-2007	
SHEET <b>23</b> OF <b>45</b>			



<b>INVENTEC</b>			
TITLE <b>GALILEO CRT</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>000</b>
CHANGE by <b>KANE</b>		12-Sep-2007	
SHEET <b>24</b>		OF <b>45</b>	





	A	R573	R572
SINGLE	NA	NA	4.7K
DUAL	NA	4.7K	NA
AUTO	0	NA	NA

	Single	Dual		Falling Edge	Rising Edge	
DUAL	L	H		R_FB	L	H

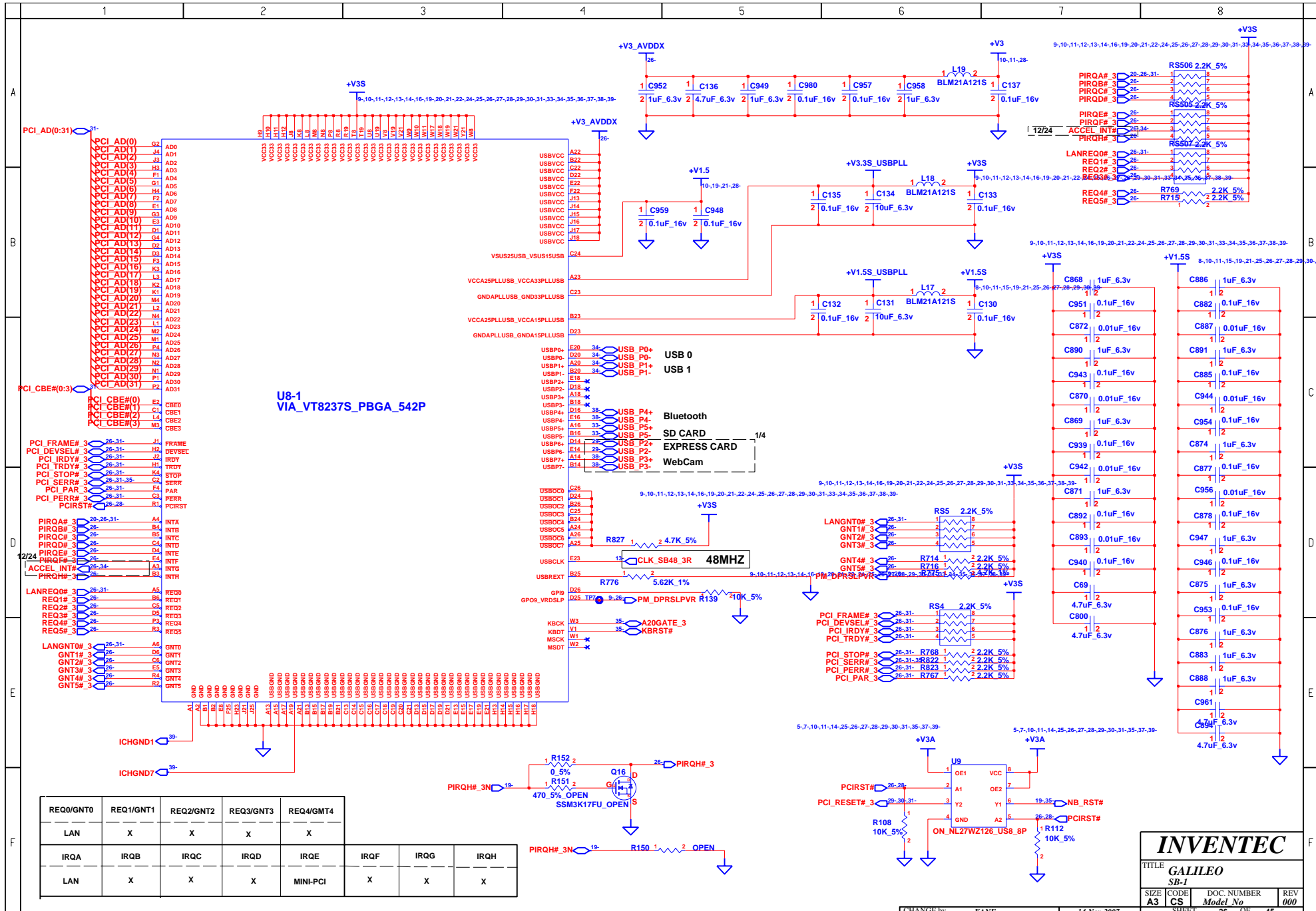
**INVENTEC**

TITLE: GALILEO LVDS

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000

SHEET 25 OF 45

CHANGE by KANE 17-Sep-2007



- PCI\_AD(0:31)
- PCI\_AD(0) G2 AD0
  - PCI\_AD(1) J4 AD1
  - PCI\_AD(2) J3 AD2
  - PCI\_AD(3) H3 AD3
  - PCI\_AD(4) F1 AD4
  - PCI\_AD(5) H4 AD5
  - PCI\_AD(6) G1 AD6
  - PCI\_AD(7) F2 AD7
  - PCI\_AD(8) E1 AD8
  - PCI\_AD(9) E3 AD9
  - PCI\_AD(10) G3 AD10
  - PCI\_AD(11) D1 AD11
  - PCI\_AD(12) G4 AD12
  - PCI\_AD(14) D2 AD13
  - PCI\_AD(15) F3 AD14
  - PCI\_AD(16) K3 AD15
  - PCI\_AD(17) L3 AD16
  - PCI\_AD(18) L4 AD17
  - PCI\_AD(19) K1 AD18
  - PCI\_AD(20) M4 AD19
  - PCI\_AD(21) L2 AD20
  - PCI\_AD(22) N4 AD21
  - PCI\_AD(23) L1 AD22
  - PCI\_AD(24) N1 AD23
  - PCI\_AD(25) M2 AD24
  - PCI\_AD(26) P4 AD25
  - PCI\_AD(27) N3 AD26
  - PCI\_AD(28) N2 AD27
  - PCI\_AD(29) N1 AD28
  - PCI\_AD(30) P1 AD29
  - PCI\_AD(31) P2 AD30

- PCI\_CBE#(0:3)
- PCI\_CBE#(0) E2 CBE0
  - PCI\_CBE#(1) C1 CBE1
  - PCI\_CBE#(2) L4 CBE2
  - PCI\_CBE#(3) M3 CBE3

- PCI\_FRAME# 3 J1 FRAME
- PCI\_DEVSEL# 3 J2 DEVSEL
- PCI\_IRDY# 3 J3 IRDY
- PCI\_TRDY# 3 J4 TRDY
- PCI\_STOP# 3 K4 STOP
- PCI\_SERR# 3 G2 SERR
- PCI\_PAR# 3 F4 PAR
- PCI\_PERR# 3 C3 PERR
- PCIRST# 2 R1 PCIRST

- PIRQA# 3 A4 INTX
- PIRQB# 3 B4 INTB
- PIRQC# 3 B5 INTC
- PIRQD# 3 G4 INTD
- PIRQE# 3 E4 INTE
- PIRQF# 3 D4 INTF
- ACCEL\_INT# 2 A3 INTG
- PIRQH# 3 B3 INTH

- LANREQ0# 3 A5 REQ0
- REQ1# 3 B6 REQ1
- REQ2# 3 C6 REQ2
- REQ3# 3 D6 REQ3
- REQ4# 3 P3 REQ4
- REQ5# 3 R3 REQ5

- LANGNT0# 3 A6 GNT0
- GNT1# 3 D6 GNT1
- GNT2# 3 C6 GNT2
- GNT3# 3 E5 GNT3
- GNT4# 3 R4 GNT4
- GNT5# 3 B2 GNT5

REQ0/GNT0	REQ1/GNT1	REQ2/GNT2	REQ3/GNT3	REQ4/GNT4	IRQA	IRQB	IRQC	IRQD	IRQE	IRQF	IRQG	IRQH
LAN	X	X	X	X								
IRQA	IRQB	IRQC	IRQD	IRQE	IRQF	IRQG	IRQH					
LAN	X	X	X	MINI-PCI	X	X	X					

**INVENTEC**

TITLE GALILEO  
SB-1

SIZE A3	CODE CS	DOC. NUMBER Model No	REV 000
---------	---------	----------------------	---------

CHANGE by KANE 14-Nov-2007 SHEET 26 OF 45



**GPIOA GPIOA**  
 LL: 100MHz  
 LH: 133MHz  
 HL: 200MHz  
 HH: Auto (166MHz can be obtained) \*

**GPIOB = IOQ Depth**  
 L: 8 Level \*  
 H: 1 Level

**GPIOD = AGTL + internal Pullups**  
 L: Enable \*  
 H: Disable

**PDA(0) = Vlink compensation**  
 L: Auto mode  
 H: Manual mode \*

**PDA(1) = V4-Lite Capability**  
 L: Disable \*  
 H: Enable

**PDA(2) = V4 Capability**  
 L: Disable \*  
 H: Enable

**PDCS3\_3 = V-Link reference**  
 L: 0.75 (8251) \*  
 H: 0.9V (8237)

**PDDACK\_3**  
 V-Link 4X mode  
 L: Auto mode  
 H: Manual mode \*

**PDCS1\_3**  
 SATA Stagger Spin Up  
 L: Disable  
 H: Enable \*

**ACSYNC**  
 LPC FWH command  
 L: Enable  
 H: Disable \*

**ACSDO**  
 Auto Reboot  
 L: Enable  
 H: Disable \*

**PCISTP#**  
 100MHz Vlink clock  
 L: Enable  
 H: Disable \*

**SEEDI**  
 LAN shadow EEPROM  
 L: Disable \*  
 H: Enable

**PCSPKR\_SB\_3**  
 CPU FREQ Strapping  
 L: Enable  
 H: Disable \*

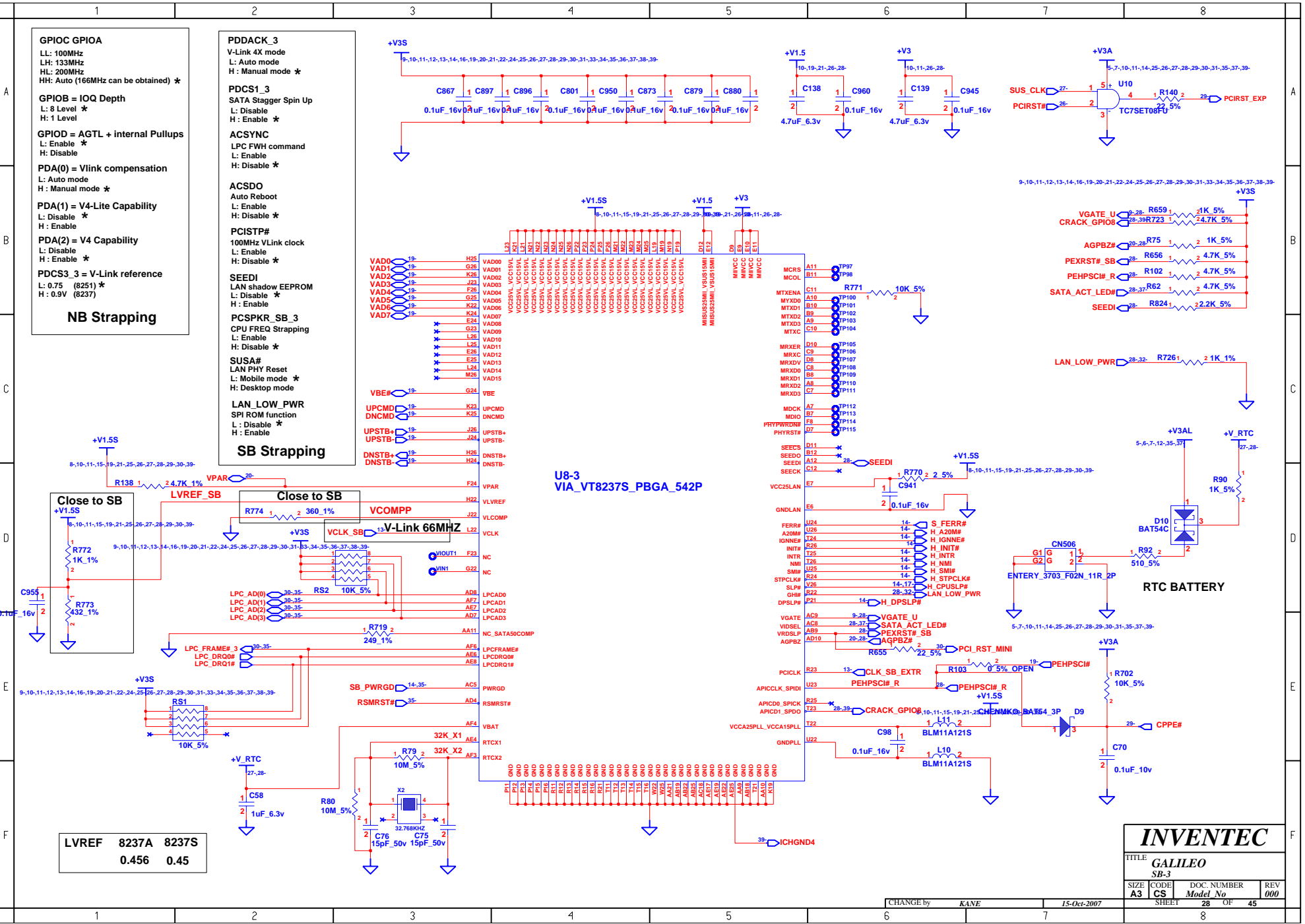
**SUSA#**  
 LAN PHY Reset  
 L: Mobile mode \*  
 H: Desktop mode

**LAN\_LOW\_PWR**  
 SPI ROM function  
 L: Disable \*  
 H: Enable

**NB Strapping**

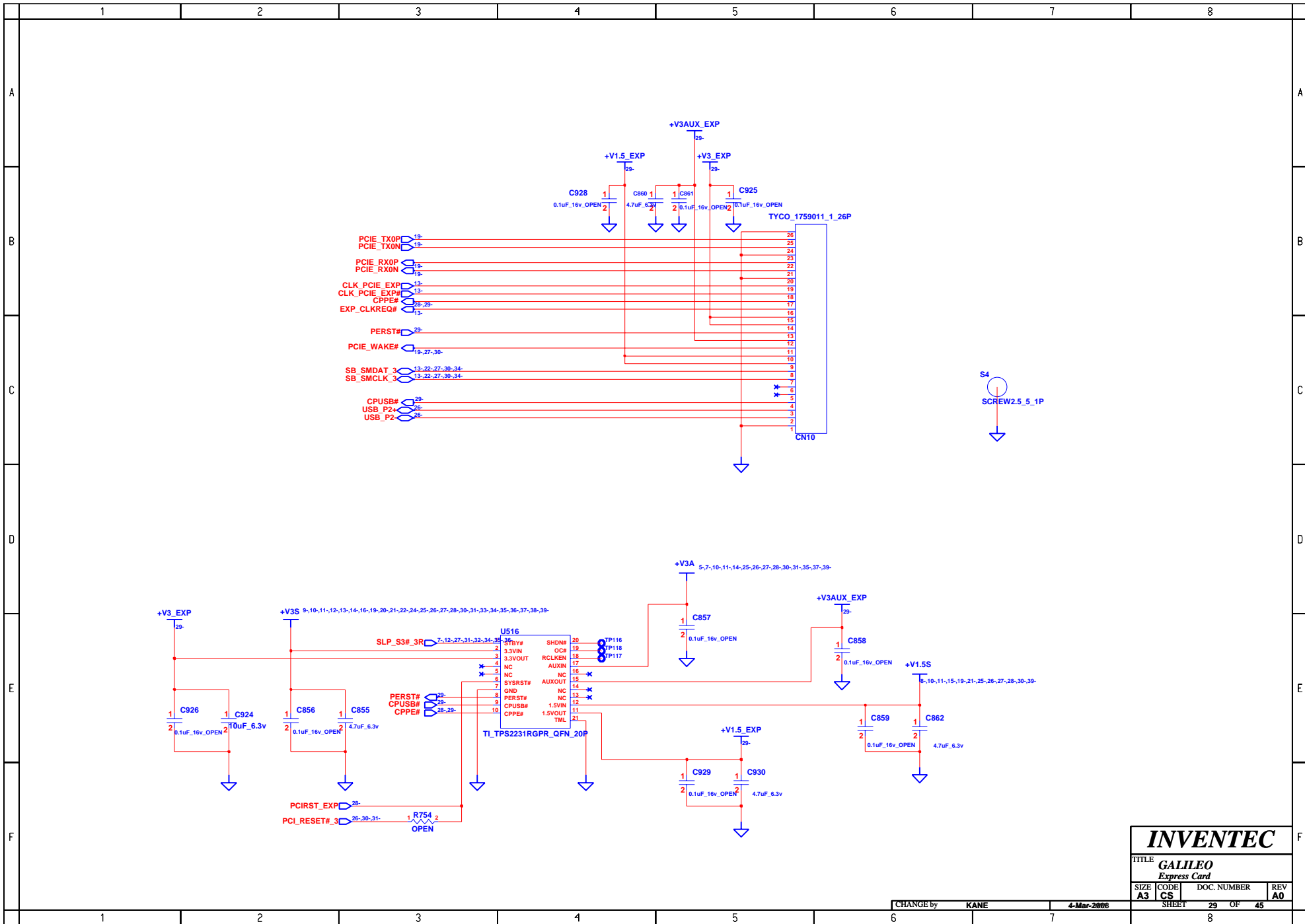
**SB Strapping**

**U8-3 VIA\_VT8237S\_PBGA\_542P**

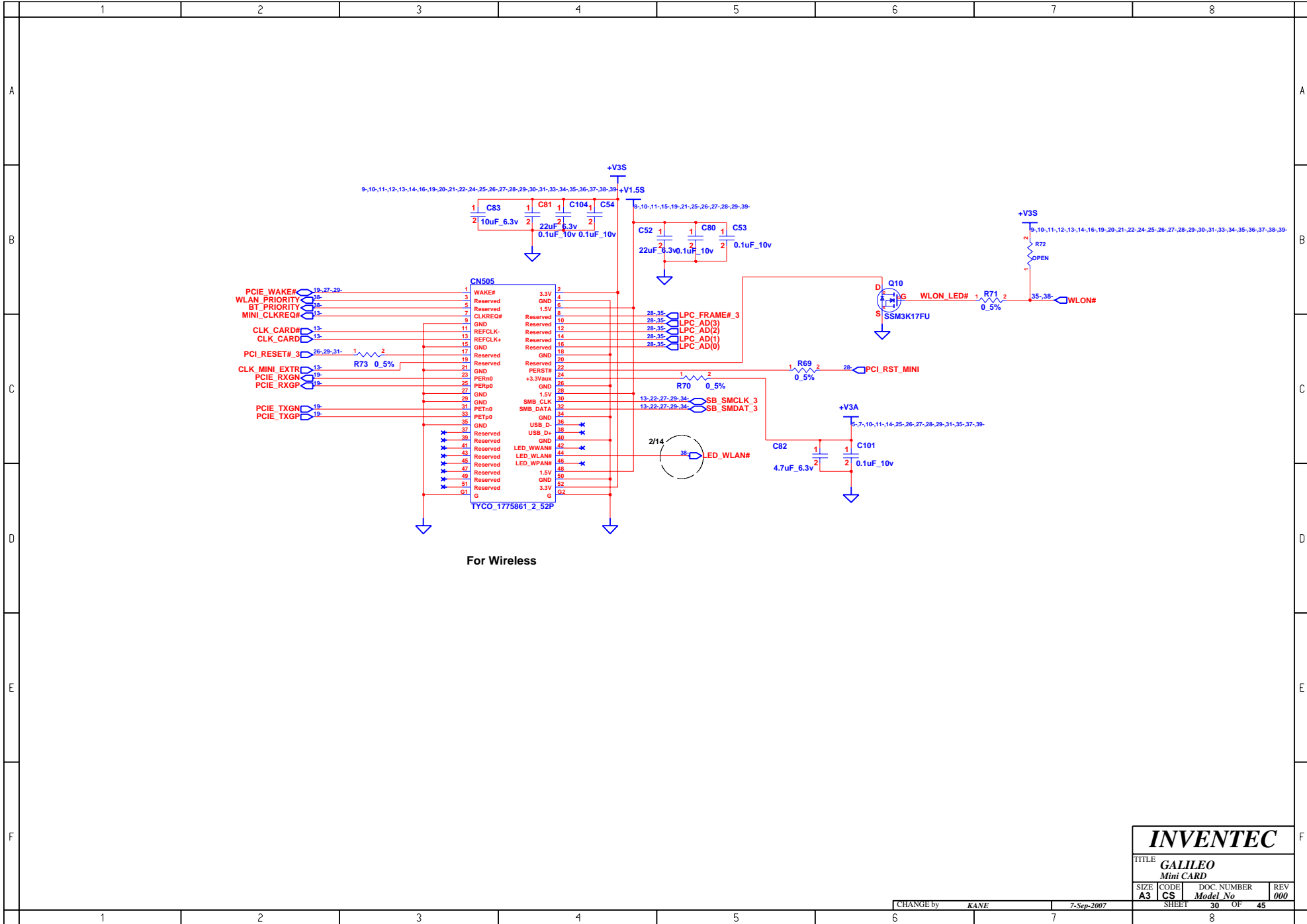


LVREF	8237A	8237S
	0.456	0.45

<b>INVENTEC</b>			
TITLE GALILEO			
SB-3			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000



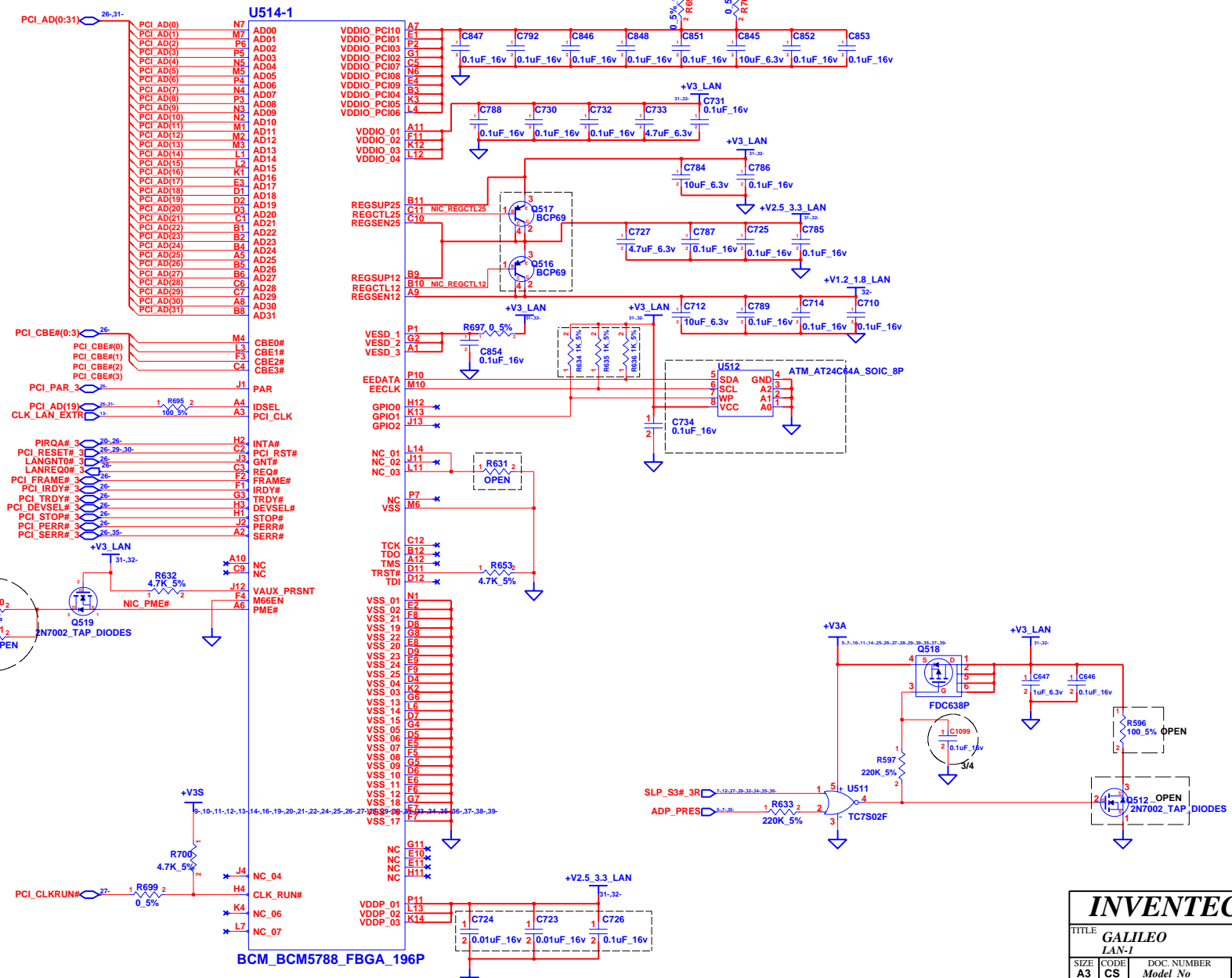
<b>INVENTEC</b>			
TITLE <b>GALILEO</b> <i>Express Card</i>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER 29 OF 45	REV <b>A0</b>
CHANGE by <b>KANE</b>		4-Mar-2008	
SHEET		29 OF 45	



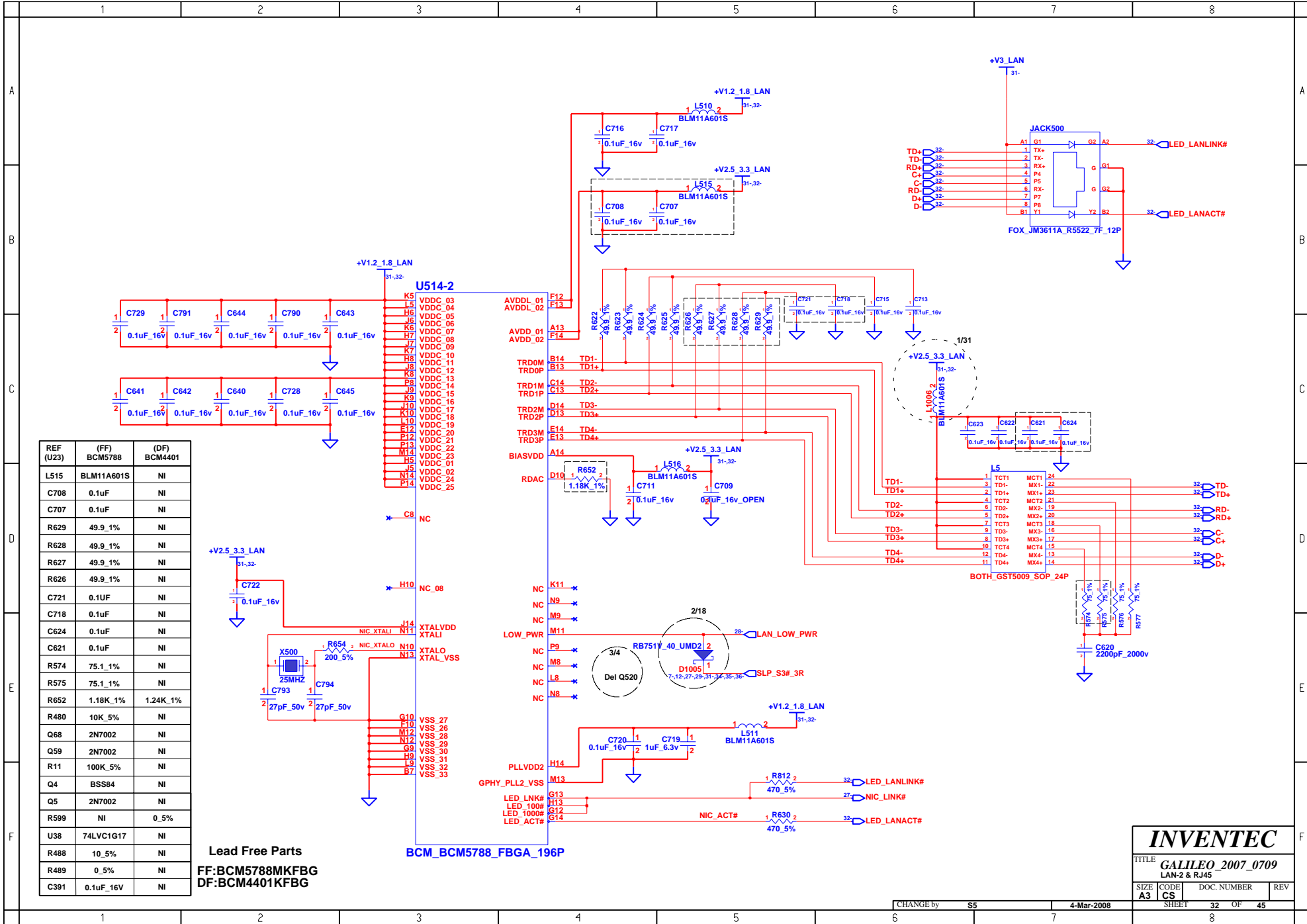
<b>INVENTEC</b>			
TITLE <i>GALILEO</i> <i>Mini CARD</i>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
CHANGE by <i>KANE</i>		7-Sep-2007	
SHEET <b>30</b>		OF <b>45</b>	

REF (U23)	(FF) BCM5788	(DF) BCM4401
R698	NI	0.5%
R701	0.5%	NI
Q517	BCP69	NI
Q516	BCP69	NI
R634	1K_5%	NI
R635	1K_5%	NI
R636	1K_5%	NI
U512	AT24C64A	NI
U30	NI	AT93C46A
R631	NI	0.5%
C724	0.01uF_16V	NI
C723	0.01uF_16V	NI
C726	0.01uF_16V	NI

**Lead Free Parts**  
**FF:BCM5788MKFBG**  
**DF:BCM4401KFBG**



<b>INVENTEC</b>				
TITLE: GALILEO LAN-1				
SIZE: A3	CODE: CS	DOC. NUMBER: Model No	REV: 000	
CHANGE by: KANE		4-Mar-2008		
SHEET: 31			OF: 45	



REF (U23)	(FF) BCM5788	(DF) BCM4401
L515	BLM11A601S	NI
C708	0.1uF	NI
C707	0.1uF	NI
R629	49.9_1%	NI
R628	49.9_1%	NI
R627	49.9_1%	NI
R626	49.9_1%	NI
C721	0.1uF	NI
C718	0.1uF	NI
C624	0.1uF	NI
C621	0.1uF	NI
R574	75.1_1%	NI
R575	75.1_1%	NI
R652	1.18K_1%	1.24K_1%
R480	10K_5%	NI
Q68	2N7002	NI
Q59	2N7002	NI
R11	100K_5%	NI
Q4	BSS84	NI
Q5	2N7002	NI
R599	NI	0_5%
U38	74LVC1G17	NI
R488	10_5%	NI
R489	0.5%	NI
C391	0.1uF_16V	NI

Lead Free Parts  
 FF:BCM5788MFKFBG  
 DF:BCM4401KFBG

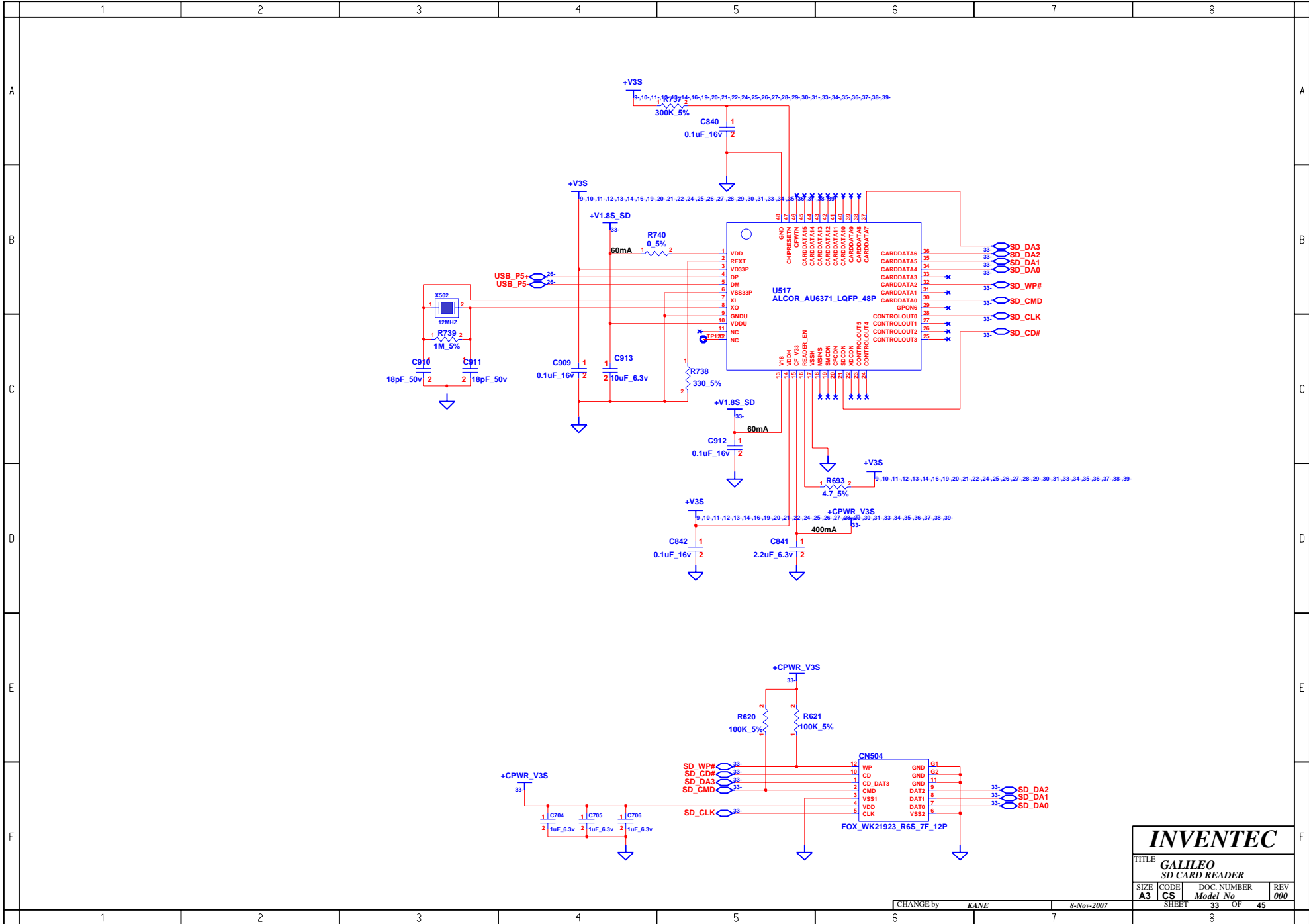
BCM\_BCM5788\_FPGA\_196P

# INVENTEC

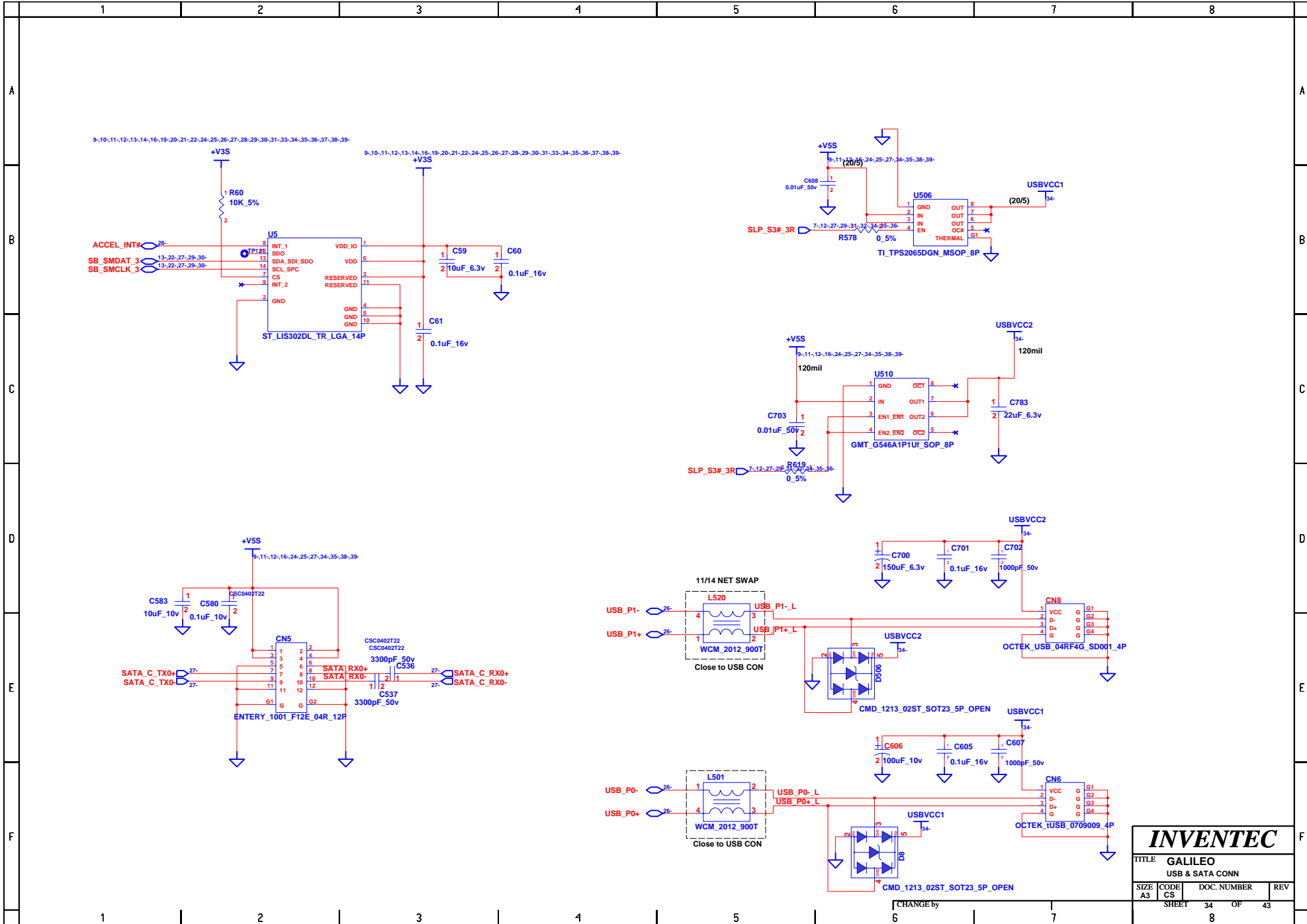
TITLE GALILEO\_2007\_0709  
 LAN-2 & RJ45

SIZE	CODE	DOC NUMBER	REV
A3	CS		



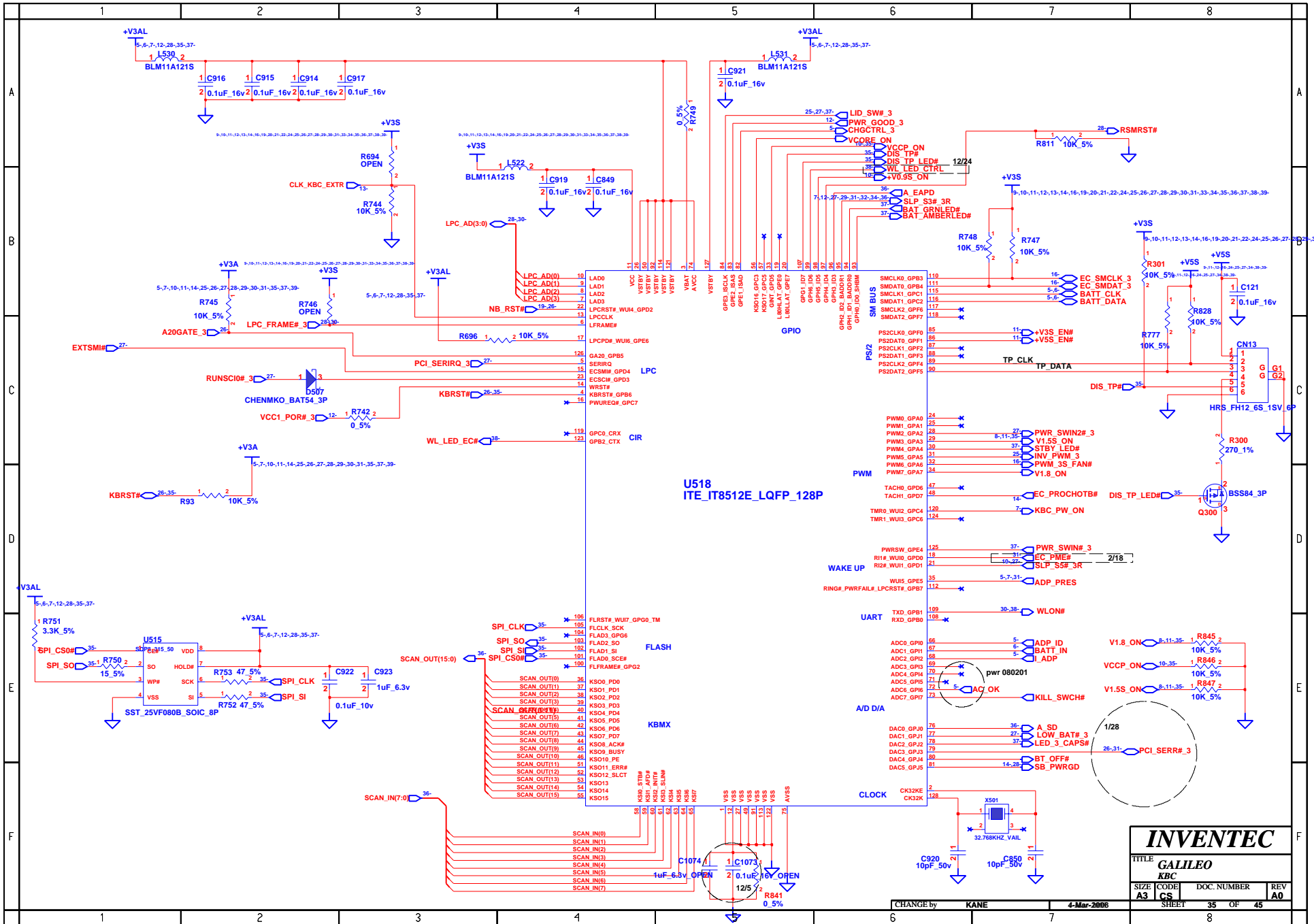


<b>INVENTEC</b>			
TITLE <b>GALILEO SD CARD READER</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>000</b>
CHANGE by <b>KANE</b>		8-Nov-2007	
SHEET <b>33</b> OF <b>45</b>		8	



<b>INVENTEC</b>			
TITLE GALILEO USB & SATA CONN			
SIZE A3	CODE CS	DOC. NUMBER 34 OF 43	REV 8

CHANGE by 6 7



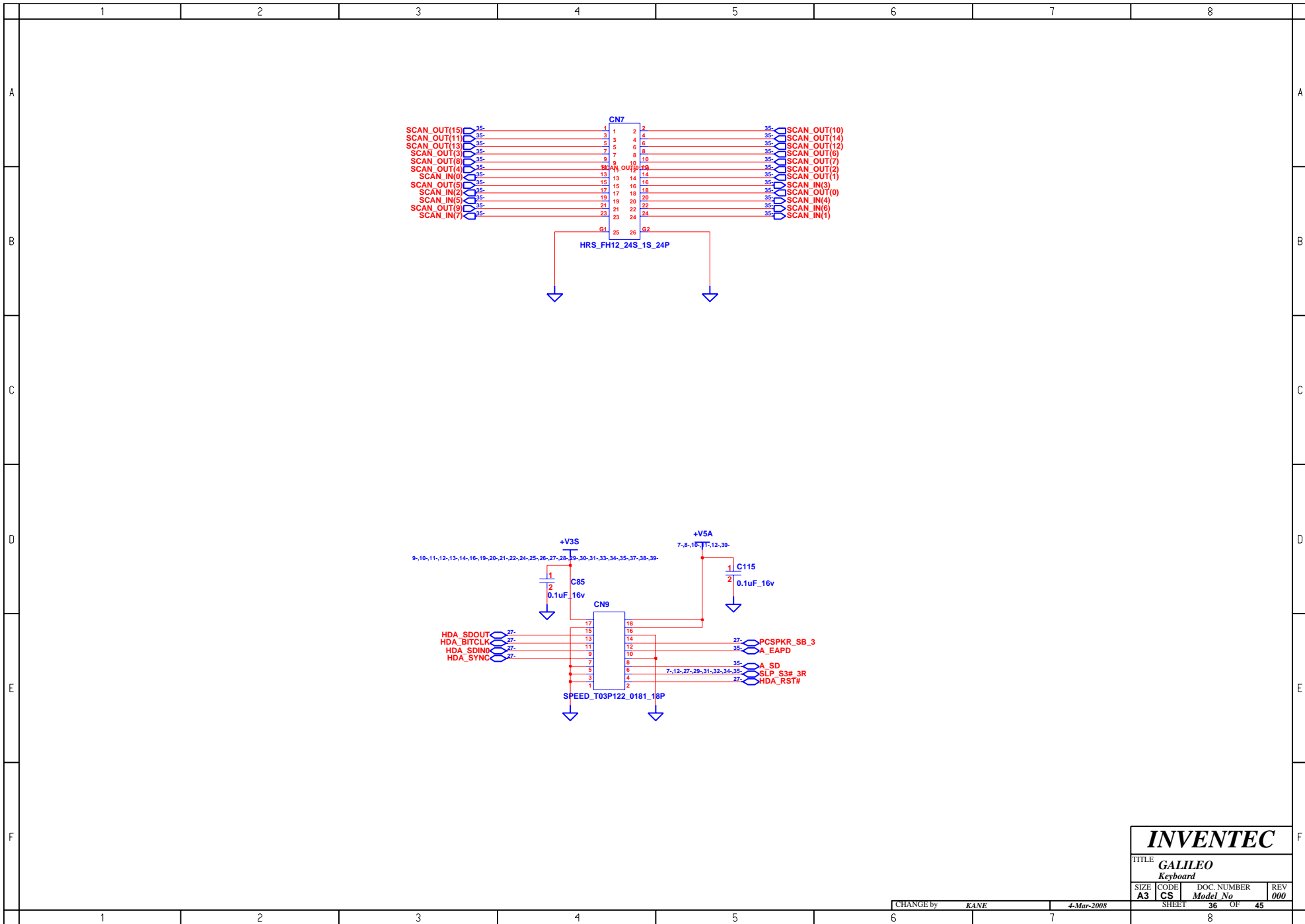
**INVENTEC**

TITLE: GALILEO  
KBC

SITE A3	CODE CS	DOC. NUMBER 35 OF 45	REV A0
---------	---------	----------------------	--------

CHANGE by: KANE 4-Mar-2008

SHEET 8

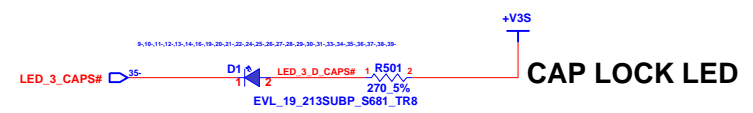
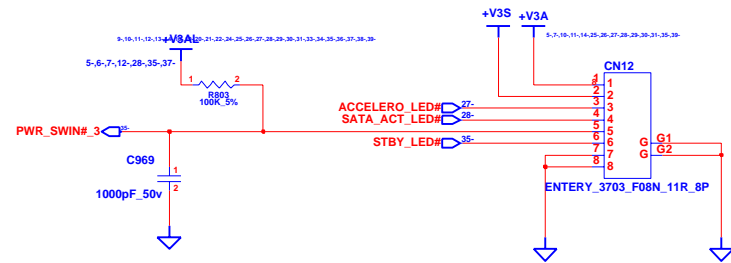
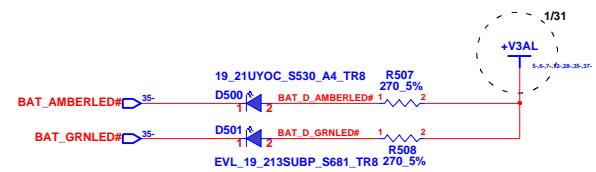
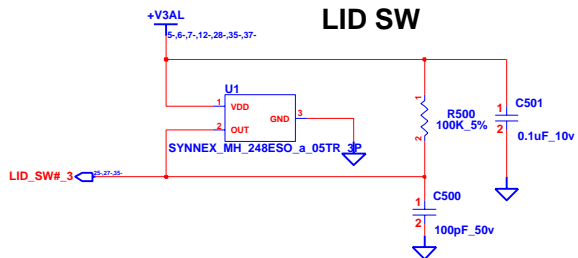


**INVENTEC**

TITLE			
GALILEO			
Keyboard			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	000

CHANGE by *KANE* 4-Mar-2008

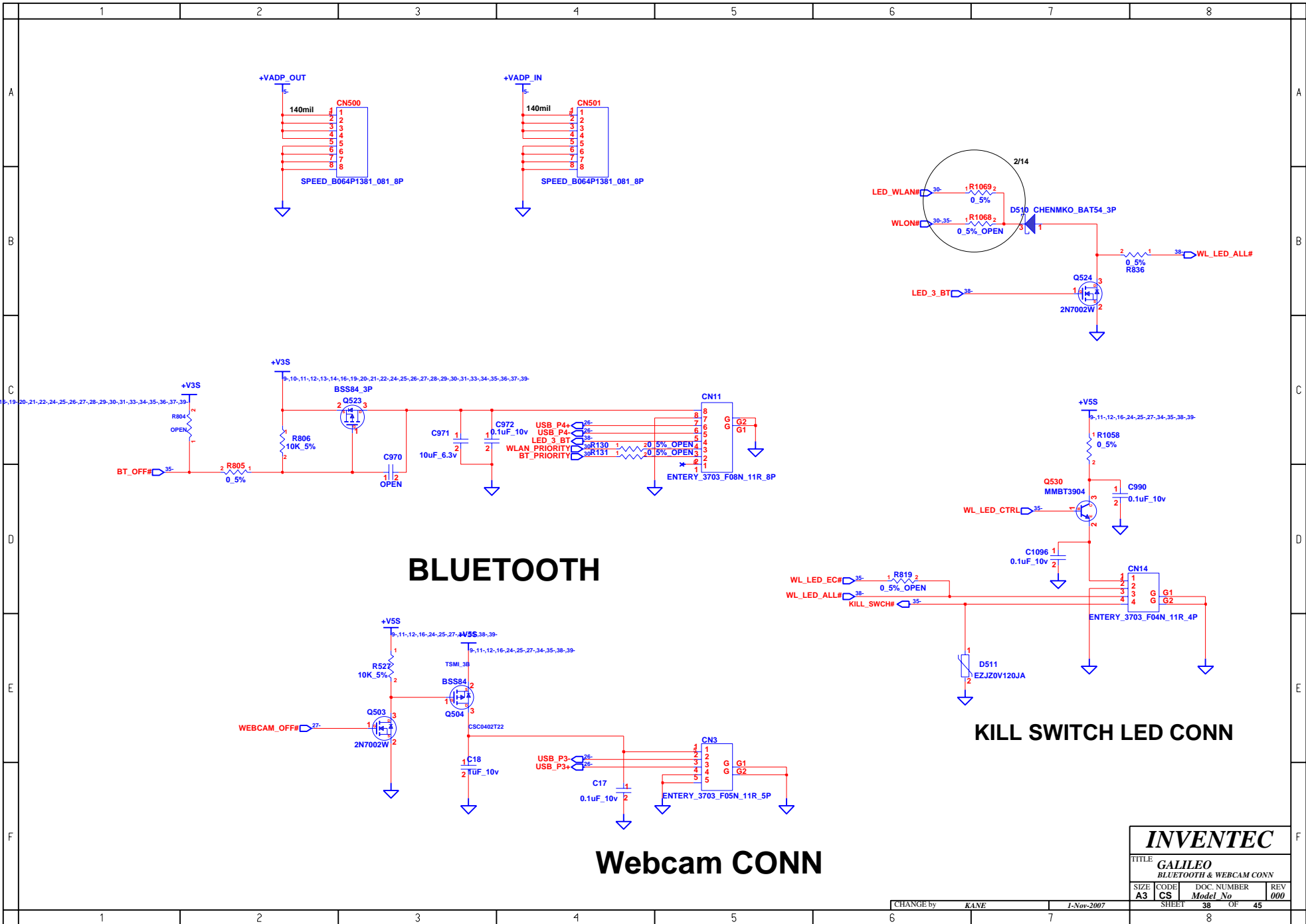
SHEET 36 OF 45



<b>INVENTEC</b>			
TITLE GALILEO-MB-X01-EE			
Button Board			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	37 OF 45	

CHANGE by GALILEO 4-Mar-2008

SHEET 37 OF 45

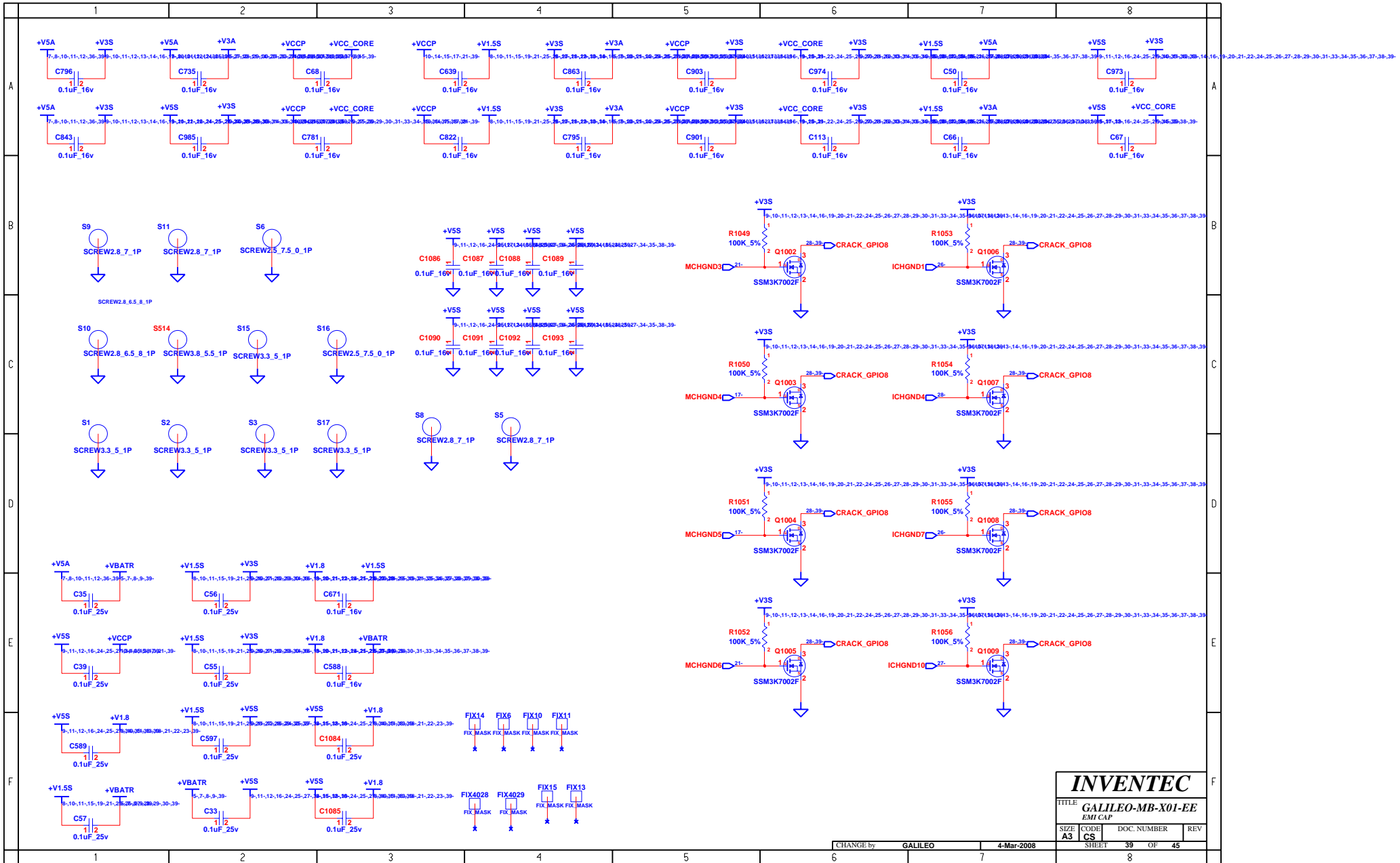


# BLUETOOTH

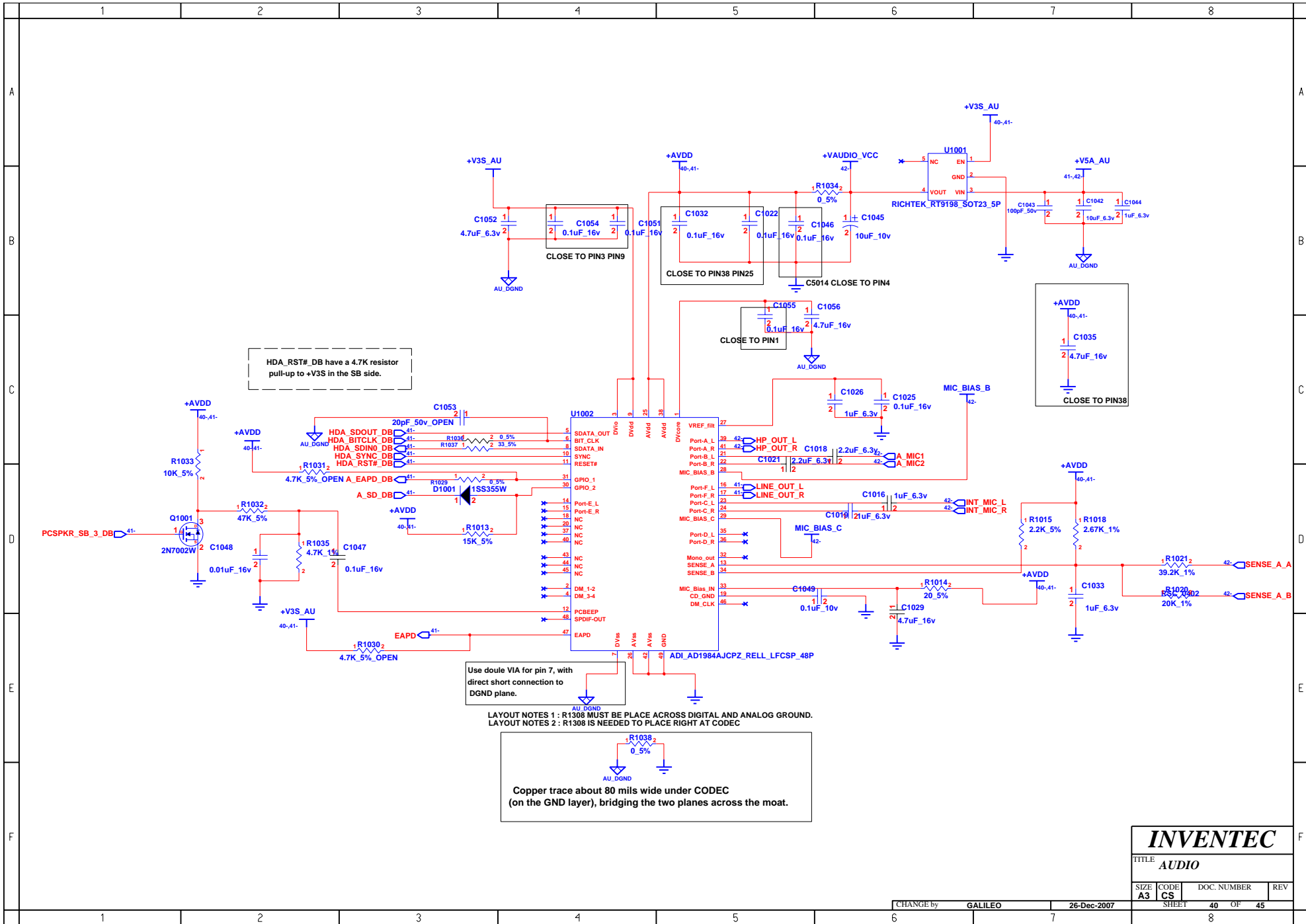
# Webcam CONN

# KILL SWITCH LED CONN

<b>INVENTEC</b>				
TITLE: GALILEO BLUETOOTH & WEBCAM CONN				
SIZE: A3	CODE: CS	DOC. NUMBER: Model No	REV: 000	
CHANGE by: KAWE		1-Nov-2007		
SHEET: 38		OF: 45		



<b>INVENTEC</b>			
TITLE: GALILEO-MB-X01-EE			
EMI CAP			
SIZE	CODE	DOC. NUMBER	REV
A3	CS		
CHANGE by: GALILEO		4-Mar-2008	
SHEET 39		OF 45	
		8	



# INVENTEC

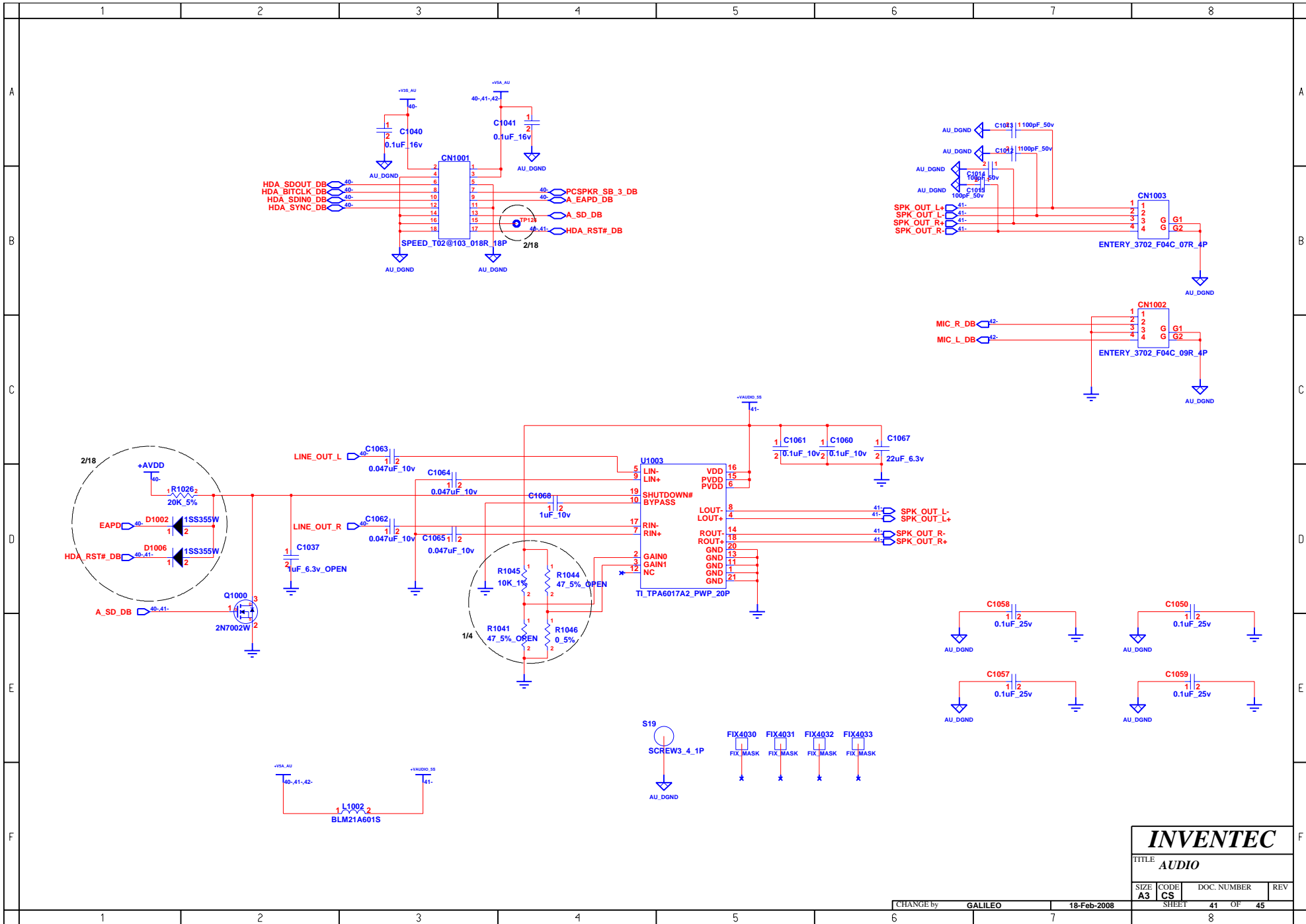
TITLE AUDIO

SIZE	CODE	DOC. NUMBER	REV
A3	CS		

CHANGE by GALILEO 26-Dec-2007

SHEET	OF	45
1	40	



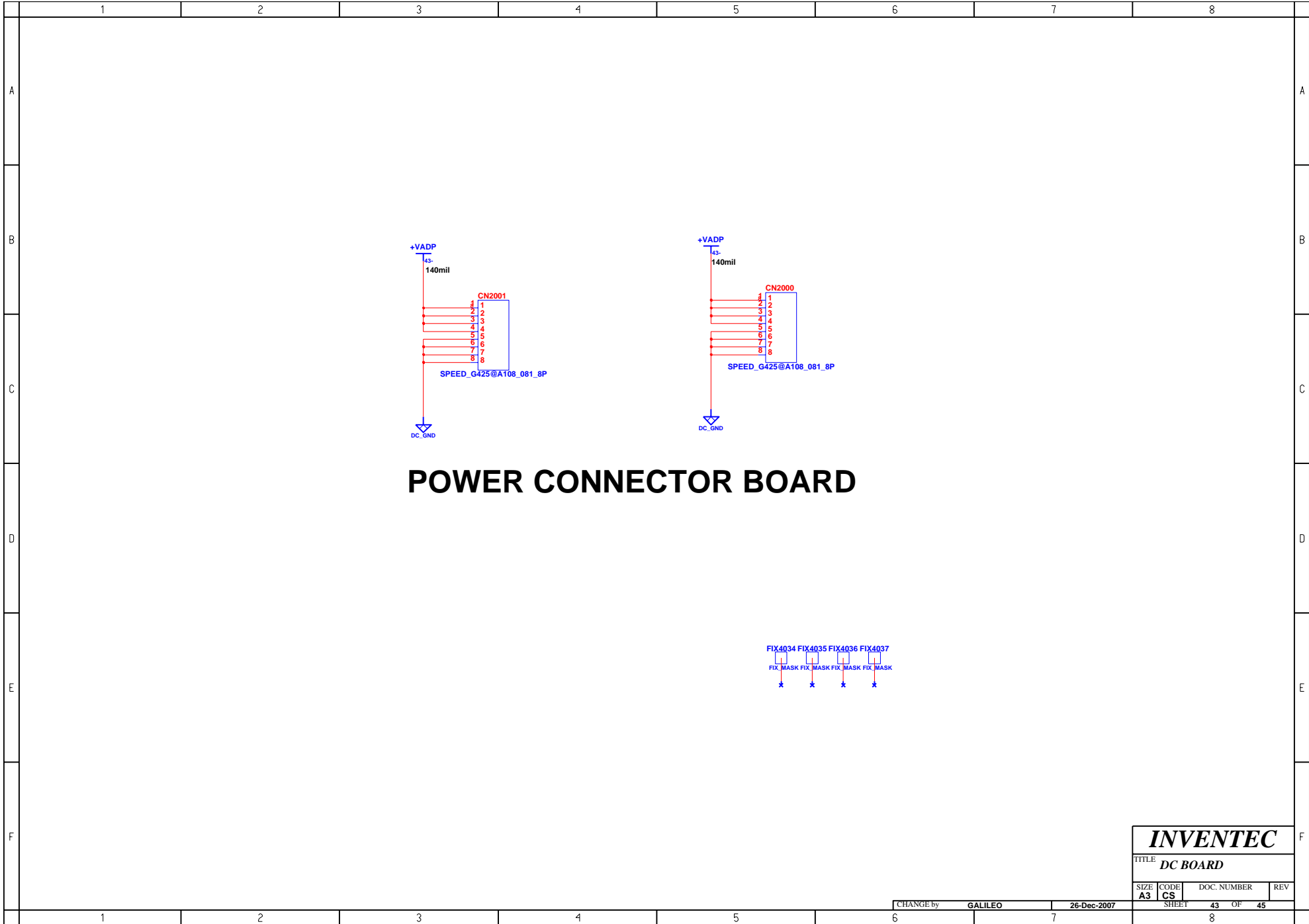


# INVENTEC

TITLE  
**AUDIO**

SIZE	CODE	DOC. NUMBER	REV
A3	CS		





# POWER CONNECTOR BOARD

FIX4034 FIX4035 FIX4036 FIX4037  
 MASK FIX MASK FIX MASK FIX MASK  
 \* \* \* \*

**INVENTEC**

TITLE **DC BOARD**

SIZE	CODE	DOC. NUMBER	REV
A3	CS		

CHANGE by GALILEO 26-Dec-2007

SHEET 43 OF 45

8

## VERSION DB TO SI

10/30

- PAGE 8 --- change R57 to 11.3K
- PAGE 9 --- Add R28-R35 (0 ohm\_5%)
- PAGE 9 --- Add C1072 (330uF\_OPEN) . Add a POWERPAD
- PAGE 11 --- Delete R17( 47ohm) , R15 (100K), C17 (0.1uF\_25V)
- PAGE 11 --- Delete Q753, Q748(NMOS), Q4 (PMOS)
- PAGE 11 --- Add a PAD and connects +V3A and +V3
- PAGE 14 --- Q510, Q514 change to NMOS (SSM3K17FU)
- PAGE 28 --- change R659 to 1K
- PAGE 28 --- change SEEDI from GND to +V3S
- PAGE 34 --- change C700,C606 to 150uF\_6.3V
- PAGE 20 --- change R673 to OPEN, change R736 to 10K\_1%
- PAGE 35 --- change U515 to SST25V080B (1M FLASH)
- PAGE 38 --- change pin1 from +V3A to +V3S

11/1

- PAGE 25 --- Add CN15 (6 pin connector) for LVDS
- PAGE 38 --- change CN14 to 4pin connector

11/2

- PAGE 41 --- change 8 pin connector to 4pin connector\*2 for SPK and MIC
- PAGE 28 --- Delete R89 ; change D10 to BAT54C
- PAGE 28 --- Change R90 to 1K ohm ; change R92 to 510 ohm.

11/5

- PAGE 30 --- Add Q20(PMOS), change R23 to R1047(100K)
- PAGE 37 --- Delete D509
- PAGE 24 --- Add D1003

11/6

- PAGE 25 --- change pin 3,4 and pin 5,6 of CN15
- PAGE 5 --- add R1048
- PAGE 5 --- change c24 to 0.1UF
- PAGE 5 --- change C16 to 2.2uF
- PAGE 35 --- change KBRST#, A20GATE pull high to +V3A

11/7

- PAGE 6 --- R12 change to 100ohms
- PAGE 6 --- add D1006
- PAGE 6 --- add D1007
- PAGE 6 --- change C15 47PF

11/8

- PAGE 27 --- change ACCELERO\_LED# pull high to +V3A

11/9

- PAGE 38 --- LED\_3 WLAN change to WLON#
- PAGE 38 --- Delete U520, KILL\_SWCH#. R805 change to 0 ohm
- PAGE 34 --- ACCEL\_INT# change to ACCEL\_INT#\_L
- PAGE 30 --- CN505 pin 44 NC. Delete U7, R71 change to 0 ohm
- PAGE 27 --- Delete R115, R81 . Add Q303, R307.
- PAGE 27 --- SMCLK, SMDAT change pull high to +V3S
- PAGE 13 --- C981, C982 change to 15pF

11/14

- PAGE 34 --- C606 change to 100uF\_10V (Low ESR)
- PAGE 34 --- C700 change to 150uF\_6.3V (Low ESR)
- PAGE 39 --- Del S1
- PAGE 34 --- SWAP L520 D+ D-
- PAGE 41 --- CHANGE CN1002 TO 6012B0239001 (BLACK)
- PAGE 32 --- SWAP LED\_LANACT# & LED\_LANLINK#
- PAGE 27 --- CHANGE R81 ,R115 TO 0402 TYPE

11/16

- PAGE 5 --- D503 change to PDS1040S
- PAGE 9 --- C987 change to 22nF ; R128 change to 200ohm
- PAGE 24 --- C11 change to 0.1uF\_6.3V ; C512 change to 0.22uF\_6.3V
- PAGE 24 --- R3,R9 change to 33ohm ; R5, R21 change to 4.7Kohm
- PAGE 24 --- U500 change to 74LVC2G126DP
- PAGE 24 --- Q1,Q3 change to SSM3K17FU
- PAGE 24 --- Add R350,R351 (10Kohm) ; Add R121 (100Kohm)
- PAGE 24 --- D502 change to LL4148
- PAGE 24 --- Delete R6,R22 (10ohm)
- PAGE 24 --- Change R1,R19 to 0 ohm ; R4,R10 change to 4.7Kohm

11/19

- PAGE 31 --- R698, R701 change size to 0805
- PAGE 41 --- C1050,C1057,C1058,C1059 change to 1000pF\_50V

11/21

- PAGE 12 --- Delete U513, C918, R741
- PAGE 12 --- Add D600 (CHENMDO\_BAT54\_3P)
- PAGE 39 --- S14 change to SCREW3.8\_5.5 size
- PAGE 41 --- S18,S19 change to SCREW3\_4 size

## VERSION SI TO SI-2

11/26

- PAGE 27 --- R110, R111 change to 4.7K\_5% and pull high to +V3A
- PAGE 27 --- Add Q17(2N7002DW)
- PAGE 27 --- Add R6 (4.7K\_5%)
- PAGE 28 --- WL\_OFF# change to WL\_OFF
- PAGE 30 --- Q20 Change to NMOS (2N7002W)
- PAGE 30 --- WL\_OFF# change to WL\_OFF
- PAGE 35 --- U518 change to IT8512E

12/3

- PAGE 25 --- change CN15 pin name
- PAGE 24 --- change CN503 (6012B0244701)
- PAGE 23 --- change C539,C540,C567,C568,C569 (6010B0075501)
- PAGE 14 --- R651 change to 220\_5%
- PAGE 5 --- change C3 (6010B067601)
- PAGE 30 --- Delete Q13,Q20,R1047
- PAGE 30 --- +V3S\_WL change to +V3S
- PAGE 11 --- R67 change to 470 ohm(60130B4710ZT)
- PAGE 11 --- R95 change to 200 ohm(6013A0051201)
- PAGE 25 --- R583 change to 0 ohm(60130B0000ZT)
- PAGE 30 --- C83 change to 10 uF(6010B0044901)

12/4

- PAGE 9 --- delete PAD505

12/5

- PAGE 35 --- add C989(0.1uF),C990(1uF),R841(0 ohm)
- PAGE 34 --- change CN8
- PAGE 39 --- add S1

12/7

- PAGE 34 --- change CN5
- PAGE 39 --- Add Q1002-Q1009(SSM3k7002)
- PAGE 39 --- Add R1049-R1056(100Kohm)

## VERSION SI-2 TO PV

12/21

- PAGE 6 --- CN1 change geometry
- PAGE 27 --- +VBATR change to +V3S
- PAGE 27 --- Delete Q303 , R307
- PAGE 29 ---U516 change geometry
- PAGE 40 ---U1002 change geometry
- PAGE 37 ---U1 change to MH248ES0

12/24

- PAGE 39 --- S14 change to S514
- PAGE 27 --- R6 pin1 change pull high to +V5S
- PAGE 35 --- Add a signal (WL\_LED\_CTRL) from U518 pin99
- PAGE 38 --- Add Q530 , C990
- PAGE 26 --- Pin A3(INTG#) connect to ACCEL\_INT#
- PAGE 27 --- Pin AE2(GPIO) connect to NIC\_LINK#.
- PAGE 28 --- NC Pin R25
- PAGE 34 --- CN6,CN8 update geometry
- PAGE 27 --- Pin AB1 connect to SMBALT#

12/25

- PAGE 5 --- Del C31,C32,C105,C106
- PAGE 5,9 --- Add C1075,C1076,C1077,C1078,C1081,C1082,C1083
- PAGE 9 --- Add C1079,C1080
- PAGE 9 --- Add R1057

12/27

- PAGE 34 --- CN5 change to 1001-F12E-04R
- PAGE 36 --- CN9 change to T03P122-0181
- PAGE 41 --- CN1001(24pin) change to 18 pin

1/4

- PAGE 9 --- Add 0.1uF capacitor in PAD503's pin1,2
- PAGE 9 --- Add C1049,C1050,R144,C127
- PAGE 26 --- Change USB port
- PAGE 42 --- C1011,C1010 change to 470uF
- PAGE 39 --- Add C1084-C1093. (10 pcs capacitor)
- PAGE 40 --- EMI capacitor change to 0.1uF\_25V
- PAGE 35 --- V1.8\_ON add 10Kohm to DGND
- PAGE 41 --- Add R1045, R1046 ; Del R1041, R1044
- PAGE 42 --- C1038,C1066 change to 100uF\_6.3V
- PAGE 42 --- Change MIC net name

1/7

- PAGE 13 --- R833,R832 change to 22ohm ; Delete C981,C982
- PAGE 38 --- Q530(NMOS change to BJT) ; Add C1096, R1085
- PAGE 38 --- R1085 pin 1 connect to +V5S
- PAGE 41 --- Delete C1037

1/8

- PAGE 35 --- V1.5S\_ON, VCCP\_ON connect 10Kohm to GND

**INVENTEC**

TITLE  
History

SIZE	CODE	DOC. NUMBER	REV
A3	CS	44 OF 45	

CHANGE by GALILEO 4-Feb-2008

SHEET 44 OF 45

**VERSION PV TO PVR**

---

- 1/28 1. PAGE 35 --- U518 PIN 79 connects to PCI\_SERR#\_3  
 1/31 1. PAGE 32 --- L5 power +V2.5\_3.3\_LAN add BLM11A601S  
       2. PAGE 37 --- D500 and D501 power change to +V3AL  
 2/12 1. PAGE 27 --- U1005 and R1067 for the Sub# buffer  
       2. PAGE 32 --- R1066 for the SLP\_S3#\_3R pull high  
 2/14 1. PAGE30 --- Add a signal "LED\_WLAN#" at CN505 pin 44  
       2. PAGE38 --- Add R1069 and connect to LED\_WLAN#  
 2/18 1. PAGE35 --- Add a signal "EC\_PME#" at pin 18  
       2. PAGE31 --- Add 0 ohm resistor, and 0ohm\_OPEN connect to EC\_PME#  
       3. PAGE6 --- Add a diode D1004  
       4. PAGE32 --- Add a diode D1005  
       5. PAGE41 --- Del SLP\_S3#\_3R\_DB and add a test point.  
       6. PAGE41 --- Add a diode D1006 and connect to HDA\_RST#\_DB  
       7. PAGE41 --- R1026 pin1 change to connects +AVDD  
       8. PAGE27 --- Add Q1010. R22

**VERSION PVR TO MV**

---

- 3/4 1. PAGE 31 --- Add C1099  
       2. PAGE 31 --- OPEN the R596, Q512  
       3. PAGE 31 --- Del Q520

<b>INVENTEC</b>			
TITLE GALILEO-6050A217490A-MB-A02-power			
SIZE A3	CODE CS	DOC. NUMBER 45 OF 45	REV
CHANGE by GALILEO		4-Mar-2008	SHEET 8