

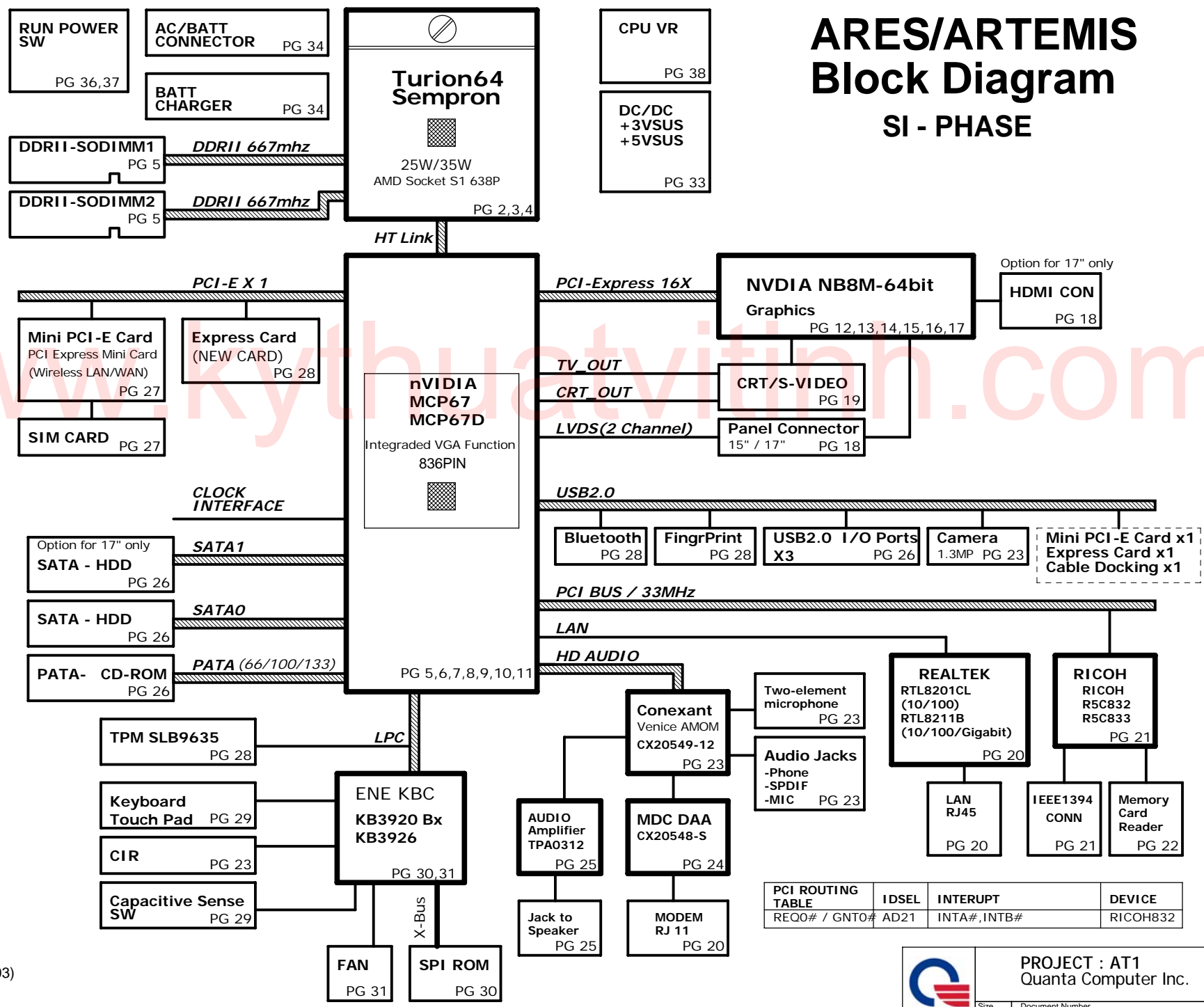
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

ARES/ARTEMIS

Block Diagram

SI - PHASE



- Cable Docking**
- TV_OUT
 - VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PG 31

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%, OTHER IS 0402
 V=Y5V,U=Y5U,R=X5R,S=X6S,
 X=X7R,G=COG,O=NPO

EXAMPLE

10R=10ohm(0402)
 10A=10ohm(0603)
 10B=10ohm(0805)
 10C=10ohm(1206)
 10/F=10ohm(0402 and 1%)

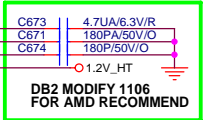
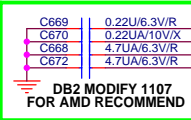
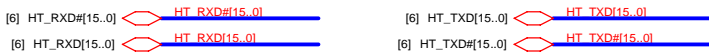
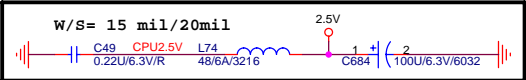
EXAMPLE

0.1U/16V/R=0.1U/16V/X5R(0402)
 0.47UA/10V/X=0.47U/10V/X7R(0603)
 10UB/10V/U=10U/10V/Y5U(0805)

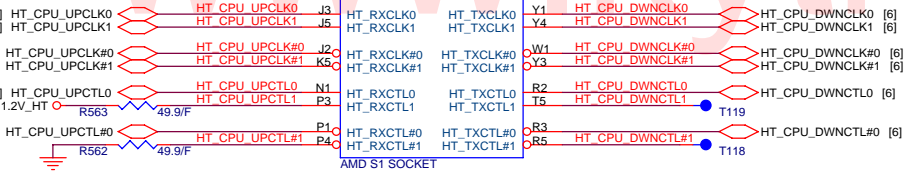
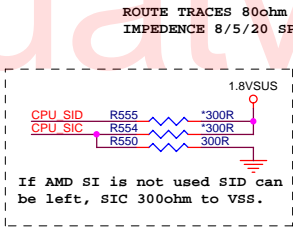
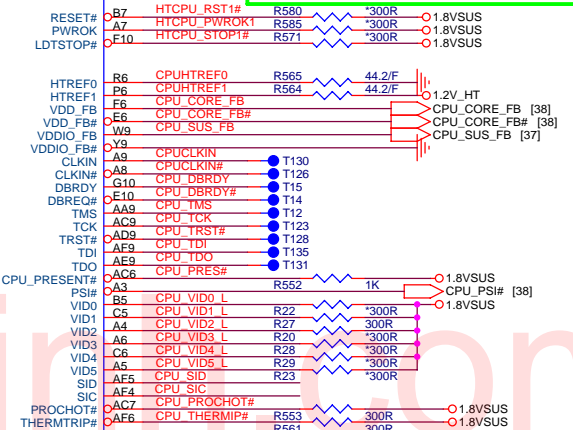
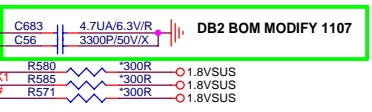
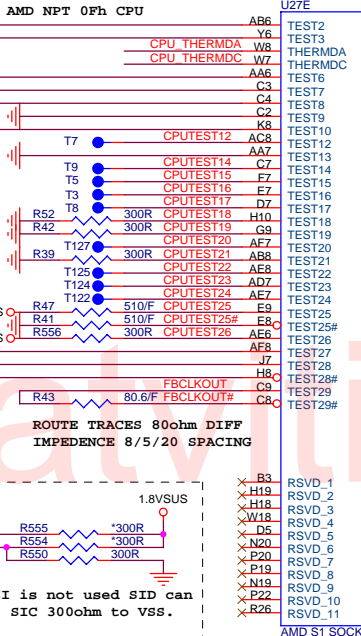
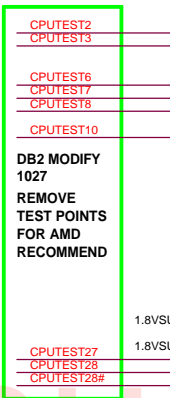
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number BLOCK DIAGRAM	Rev C2A
Date: Friday, December 29, 2006	Sheet 1 of 40	

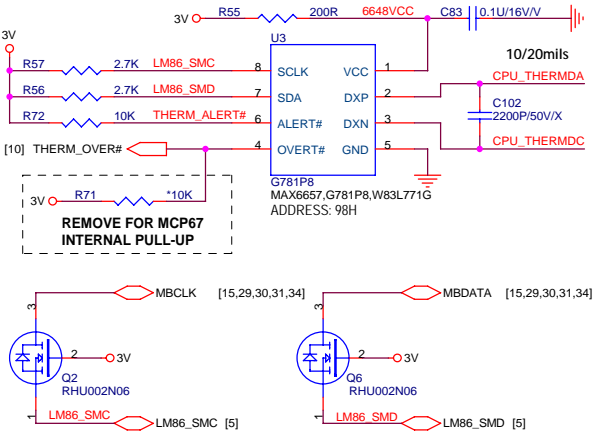


TEST PU/PL MUST FOLLOW ERRATA 133 REVISION GUIDE FROM AMD NPT 0Ph CPU



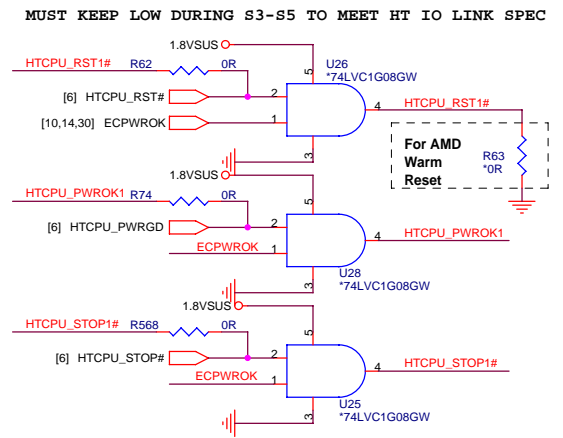
HT_RXCTL1/HT_RXCL#1 MUST <1.5" FROM CPU PIN

CPU THERMAL SENSOR & CONTROL



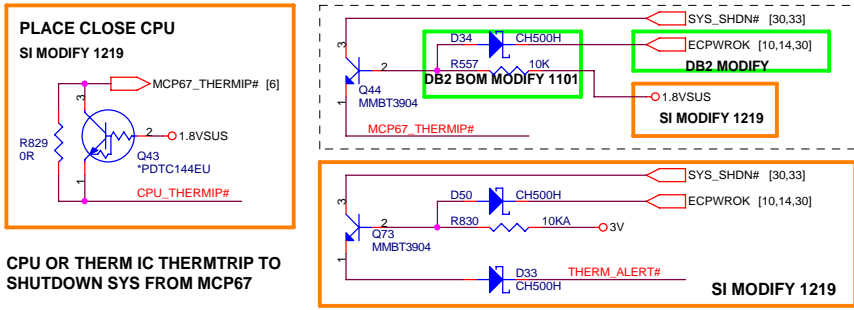
MBCLK/MBDATA NEED PU TO 3VPCU

HT LINK CONTROL LEVEL SHIFTER



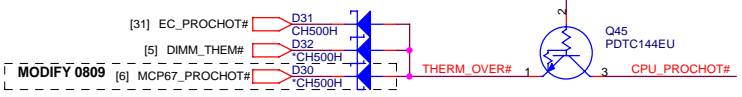
FOLLOW AMD AND NVIDIA RECOMMEND 0904

OVER TEMP CONTROL

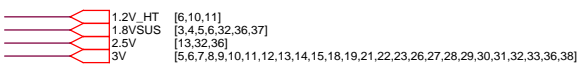


CPU OR THERM IC THERMTRIP TO SHUTDOWN SYS FROM MCP67

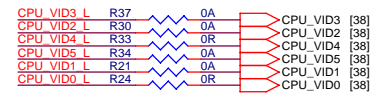
CPU PROCHOT INPUT FROM THERMAL IC OR SODIMM SENSOR



MODIFY 0809



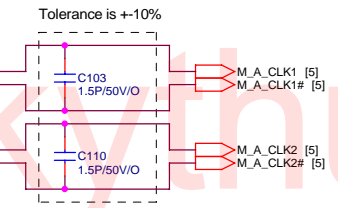
NEED TO CONFIRM NVIDIA FOR THE USAGE CONNECTION TO SB



PROJECT : AT1 Quanta Computer Inc. Size Custom Document Number CPU (HT_I/F_CTL) Rev C2A Date: Friday, December 29, 2006 Sheet 2 of 40

U27B

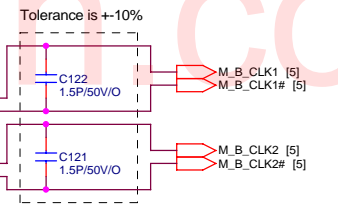
M A DQ63	AA12	MA_DATA[63]	MA_DM[7]	Y13	M A DQM7
M A DQ62	AB12	MA_DATA[62]	MA_DM[6]	AB16	M A DQM6
M A DQ61	AA14	MA_DATA[61]	MA_DM[5]	Y19	M A DQM5
M A DQ60	AB14	MA_DATA[60]	MA_DM[4]	AC24	M A DQM4
M A DQ59	W11	MA_DATA[59]	MA_DM[3]	F24	M A DQM3
M A DQ58	Y12	MA_DATA[58]	MA_DM[2]	E19	M A DQM2
M A DQ57	AD13	MA_DATA[57]	MA_DM[1]	C15	M A DQM1
M A DQ56	AB13	MA_DATA[56]	MA_DM[0]	E12	M A DQM0
M A DQ55	AD15	MA_DATA[55]			
M A DQ54	AB15	MA_DATA[54]			
M A DQ53	AB17	MA_DATA[53]			
M A DQ52	Y17	MA_DATA[52]			
M A DQ51	Y14	MA_DATA[51]	MA_DQS[7]	W12	M A DQS7
M A DQ50	W14	MA_DATA[50]	MA_DQS[6]	Y15	M A DQS6
M A DQ49	W16	MA_DATA[49]	MA_DQS[5]	AB19	M A DQS5
M A DQ48	AD17	MA_DATA[48]	MA_DQS[4]	AD23	M A DQS4
M A DQ47	Y18	MA_DATA[47]	MA_DQS[3]	G22	M A DQS3
M A DQ46	AD19	MA_DATA[46]	MA_DQS[2]	G16	M A DQS2
M A DQ45	AD21	MA_DATA[45]	MA_DQS[1]	G13	M A DQS1
M A DQ44	AB21	MA_DATA[44]	MA_DQS[0]	G13	M A DQS0
M A DQ43	AB18	MA_DATA[43]	MA_DQS[7]	W13	M A DQS#7
M A DQ42	AA18	MA_DATA[42]	MA_DQS[6]	W15	M A DQS#6
M A DQ41	AA20	MA_DATA[41]	MA_DQS[5]	AB20	M A DQS#5
M A DQ40	Y20	MA_DATA[40]	MA_DQS[4]	AC23	M A DQS#4
M A DQ39	AA22	MA_DATA[39]	MA_DQS[3]	G21	M A DQS#3
M A DQ38	Y22	MA_DATA[38]	MA_DQS[2]	G21	M A DQS#2
M A DQ37	W21	MA_DATA[37]	MA_DQS[1]	G15	M A DQS#1
M A DQ36	W22	MA_DATA[36]	MA_DQS[0]	H13	M A DQS#0
M A DQ35	AA21	MA_DATA[35]			
M A DQ34	AB22	MA_DATA[34]			
M A DQ33	AB24	MA_DATA[33]			
M A DQ32	Y24	MA_DATA[32]			
M A DQ31	H22	MA_DATA[31]			
M A DQ30	H20	MA_DATA[30]			
M A DQ29	E22	MA_DATA[29]			
M A DQ28	E21	MA_DATA[28]			
M A DQ27	J19	MA_DATA[27]			
M A DQ26	H24	MA_DATA[26]			
M A DQ25	F22	MA_DATA[25]			
M A DQ24	F20	MA_DATA[24]			
M A DQ23	C23	MA_DATA[23]			
M A DQ22	B22	MA_DATA[22]			
M A DQ21	F18	MA_DATA[21]			
M A DQ20	E18	MA_DATA[20]			
M A DQ19	E20	MA_DATA[19]			
M A DQ18	D22	MA_DATA[18]			
M A DQ17	C19	MA_DATA[17]			
M A DQ16	G18	MA_DATA[16]			
M A DQ15	G17	MA_DATA[15]			
M A DQ14	C17	MA_DATA[14]			
M A DQ13	F14	MA_DATA[13]			
M A DQ12	E14	MA_DATA[12]			
M A DQ11	H17	MA_DATA[11]			
M A DQ10	E17	MA_DATA[10]			
M A DQ9	E15	MA_DATA[9]			
M A DQ8	H15	MA_DATA[8]			
M A DQ7	E13	MA_DATA[7]			
M A DQ6	C13	MA_DATA[6]			
M A DQ5	H12	MA_DATA[5]			
M A DQ4	H11	MA_DATA[4]			
M A DQ3	G14	MA_DATA[3]			
M A DQ2	H14	MA_DATA[2]			
M A DQ1	F12	MA_DATA[1]			
M A DQ0	G12	MA_DATA[0]			



TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

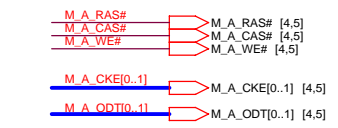
U27C

M B DQ63	AD11	MB_DATA[63]	MB_DM[7]	AD12	M B DQM7
M B DQ62	AE11	MB_DATA[62]	MB_DM[6]	AC16	M B DQM6
M B DQ61	AE14	MB_DATA[61]	MB_DM[5]	AE22	M B DQM5
M B DQ60	AE14	MB_DATA[60]	MB_DM[4]	AB26	M B DQM4
M B DQ59	Y11	MB_DATA[59]	MB_DM[3]	E25	M B DQM3
M B DQ58	AB11	MB_DATA[58]	MB_DM[2]	A22	M B DQM2
M B DQ57	AC12	MB_DATA[57]	MB_DM[1]	B16	M B DQM1
M B DQ56	AE13	MB_DATA[56]	MB_DM[0]	A12	M B DQM0
M B DQ55	AE15	MB_DATA[55]			
M B DQ54	AE16	MB_DATA[54]			
M B DQ53	AC18	MB_DATA[53]			
M B DQ52	AE19	MB_DATA[52]			
M B DQ51	AD14	MB_DATA[51]	MB_DQS[7]	AF12	M B DQS7
M B DQ50	AC14	MB_DATA[50]	MB_DQS[6]	AE16	M B DQS6
M B DQ49	AE18	MB_DATA[49]	MB_DQS[5]	AF21	M B DQS5
M B DQ48	AD18	MB_DATA[48]	MB_DQS[4]	AC25	M B DQS4
M B DQ47	AD20	MB_DATA[47]	MB_DQS[3]	F26	M B DQS3
M B DQ46	AC20	MB_DATA[46]	MB_DQS[2]	A24	M B DQS2
M B DQ45	AE23	MB_DATA[45]	MB_DQS[1]	D16	M B DQS1
M B DQ44	AE24	MB_DATA[44]	MB_DQS[0]	C12	M B DQS0
M B DQ43	AE20	MB_DATA[43]	MB_DQS[7]	AD12	M B DQS#7
M B DQ42	AE20	MB_DATA[42]	MB_DQS[6]	AD16	M B DQS#6
M B DQ41	AD22	MB_DATA[41]	MB_DQS[5]	AF22	M B DQS#5
M B DQ40	AC22	MB_DATA[40]	MB_DQS[4]	AC26	M B DQS#4
M B DQ39	AE25	MB_DATA[39]	MB_DQS[3]	E26	M B DQS#3
M B DQ38	AD26	MB_DATA[38]	MB_DQS[2]	A23	M B DQS#2
M B DQ37	AA25	MB_DATA[37]	MB_DQS[1]	C16	M B DQS#1
M B DQ36	AA26	MB_DATA[36]	MB_DQS[0]	B12	M B DQS#0
M B DQ35	AE24	MB_DATA[35]			
M B DQ34	AD24	MB_DATA[34]			
M B DQ33	AA23	MB_DATA[33]			
M B DQ32	AA24	MB_DATA[32]			
M B DQ31	G24	MB_DATA[31]			
M B DQ30	G23	MB_DATA[30]			
M B DQ29	D26	MB_DATA[29]			
M B DQ28	C26	MB_DATA[28]			
M B DQ27	G26	MB_DATA[27]			
M B DQ26	G25	MB_DATA[26]			
M B DQ25	C25	MB_DATA[25]			
M B DQ24	E23	MB_DATA[24]			
M B DQ23	C24	MB_DATA[23]			
M B DQ22	B24	MB_DATA[22]			
M B DQ21	C20	MB_DATA[21]			
M B DQ20	B20	MB_DATA[20]			
M B DQ19	D20	MB_DATA[19]			
M B DQ18	D24	MB_DATA[18]			
M B DQ17	A21	MB_DATA[17]			
M B DQ16	D20	MB_DATA[16]			
M B DQ15	D18	MB_DATA[15]			
M B DQ14	C18	MB_DATA[14]			
M B DQ13	D14	MB_DATA[13]			
M B DQ12	C14	MB_DATA[12]			
M B DQ11	A20	MB_DATA[11]			
M B DQ10	A19	MB_DATA[10]			
M B DQ9	A16	MB_DATA[9]			
M B DQ8	A15	MB_DATA[8]			
M B DQ7	A13	MB_DATA[7]			
M B DQ6	D12	MB_DATA[6]			
M B DQ5	E11	MB_DATA[5]			
M B DQ4	G11	MB_DATA[4]			
M B DQ3	B14	MB_DATA[3]			
M B DQ2	A14	MB_DATA[2]			
M B DQ1	A11	MB_DATA[1]			
M B DQ0	C11	MB_DATA[0]			

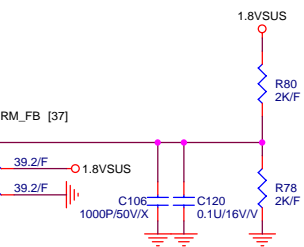
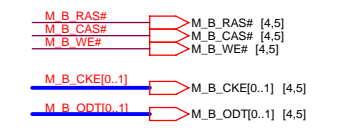


TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

- [5] M_A_DQ[0..63] <-> M_A_DQ[0..63]
- [4..5] M_A_A[0..15] <-> M_A_A[0..15]
- [5] M_A_DQM[0..7] <-> M_A_DQM[0..7]
- [5] M_A_DQS[0..7] <-> M_A_DQS[0..7]
- [5] M_A_DQS#[0..7] <-> M_A_DQS#[0..7]
- [4..5] M_A_BA[0..2] <-> M_A_BA[0..2]
- [4..5] M_A_CS#[0..3] <-> M_A_CS#[0..3]



- [5] M_B_DQ[0..63] <-> M_B_DQ[0..63]
- [4..5] M_B_A[0..15] <-> M_B_A[0..15]
- [5] M_B_DQM[0..7] <-> M_B_DQM[0..7]
- [5] M_B_DQS[0..7] <-> M_B_DQS[0..7]
- [5] M_B_DQS#[0..7] <-> M_B_DQS#[0..7]
- [4..5] M_B_BA[0..2] <-> M_B_BA[0..2]
- [4..5] M_B_CS#[0..3] <-> M_B_CS#[0..3]



M_VREF : W = 20MIL AND SPACE = 20MIL

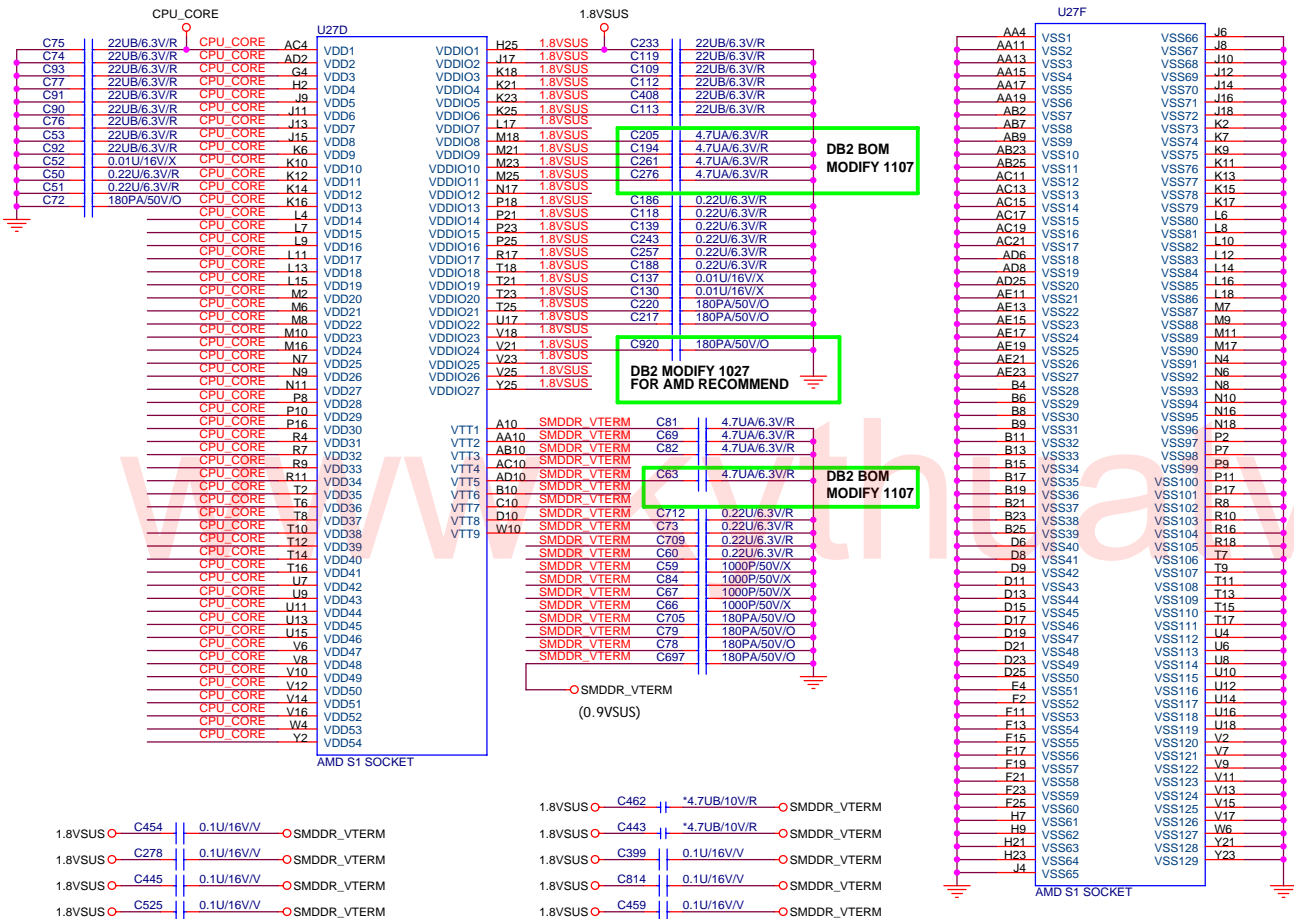
NBS/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Rev C2A

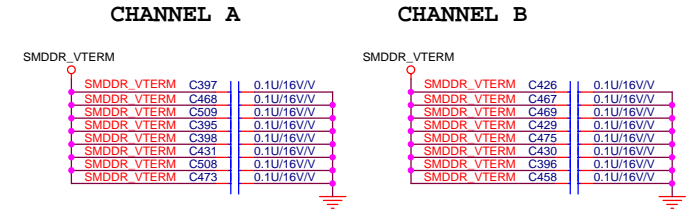
Size Custom	Document Number CPU (MEM_I/F)	Rev C2A
Date: Friday, December 29, 2006		Sheet 3 of 40

CPU POWER PLANE AND BY PASS CAP



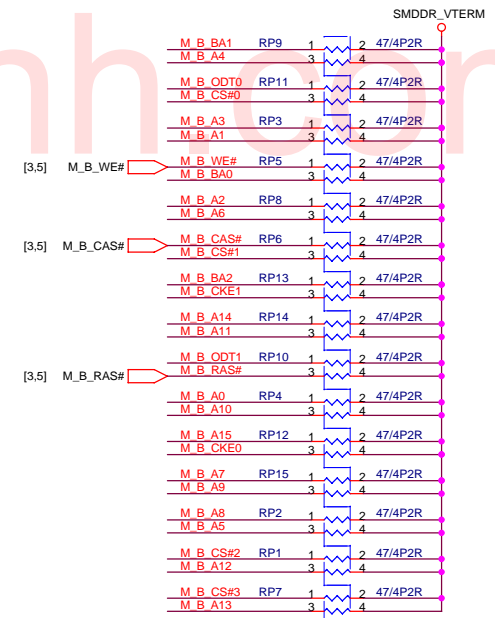
DDR2 TERMINATION BYPASS CAP

04

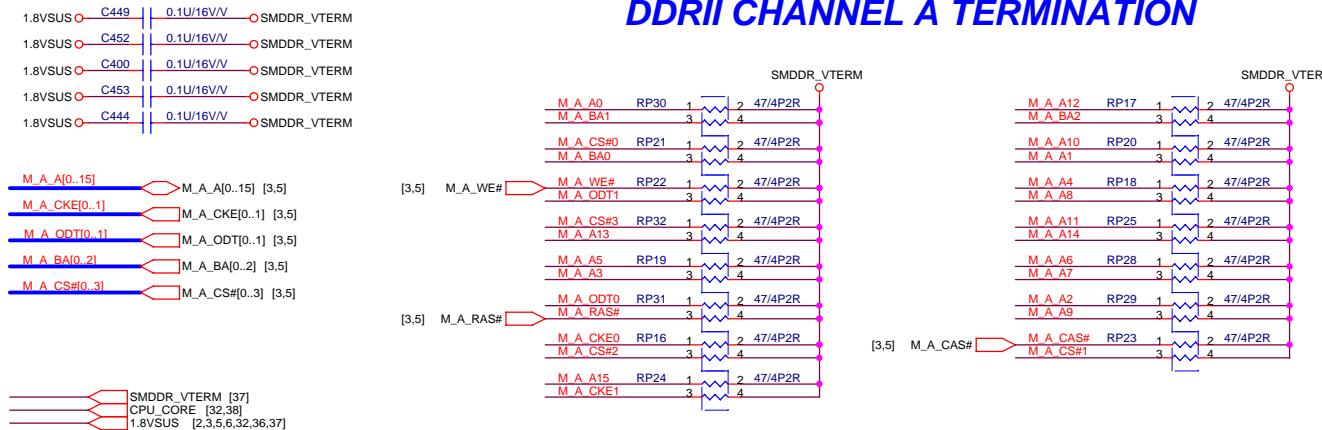



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDRR_VTERM

DDRII CHANNEL B TERMINATION



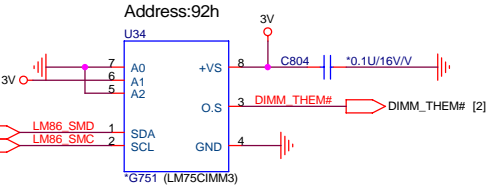
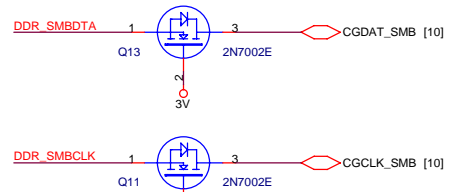
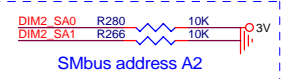
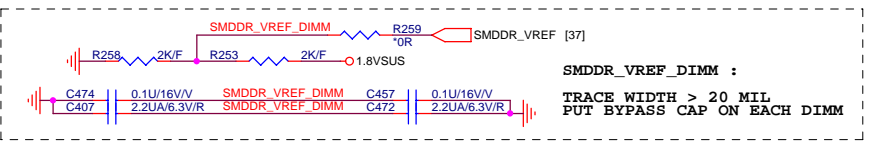
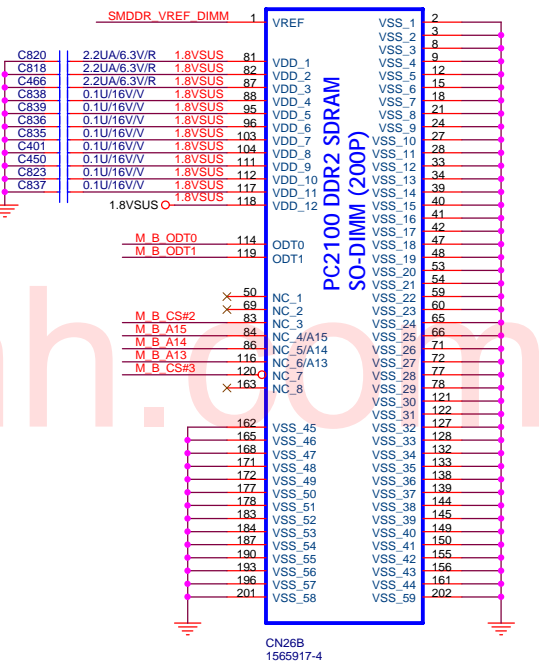
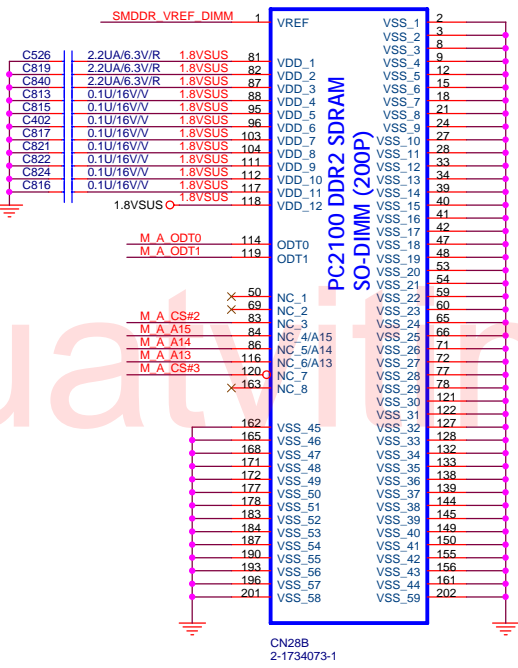
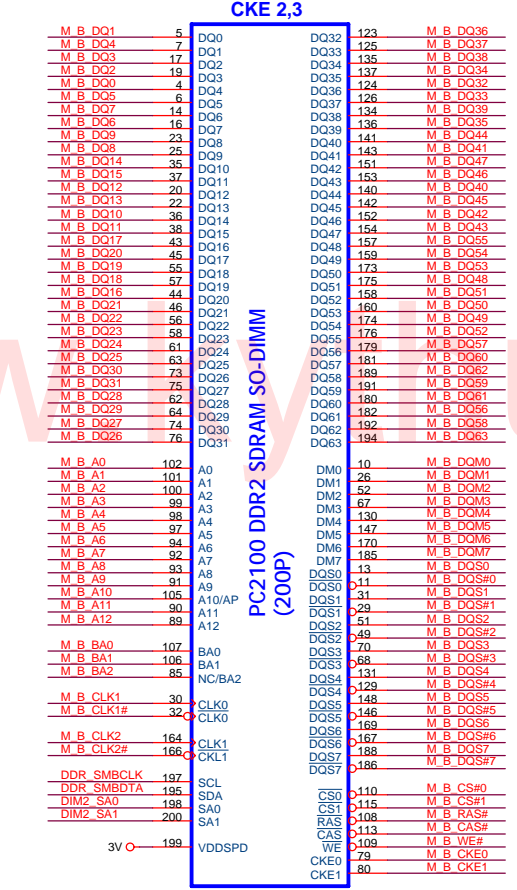
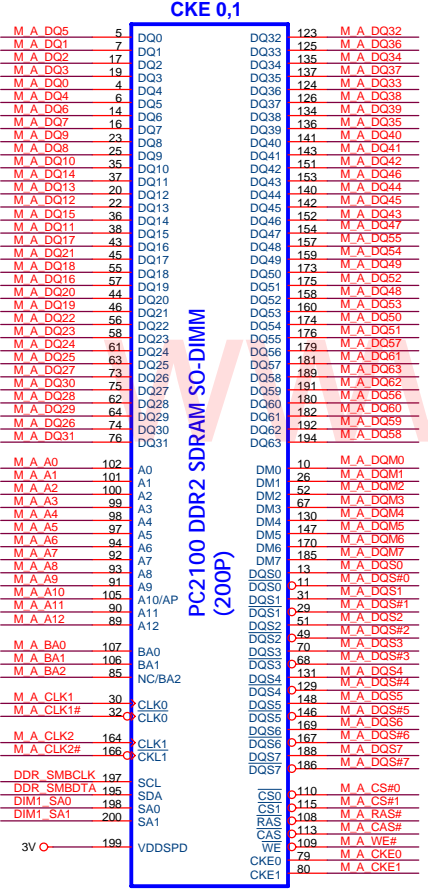
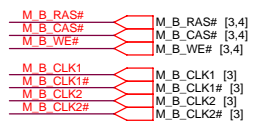
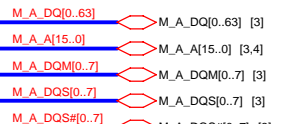
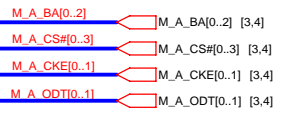
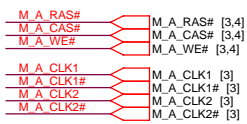
DDRII CHANNEL A TERMINATION



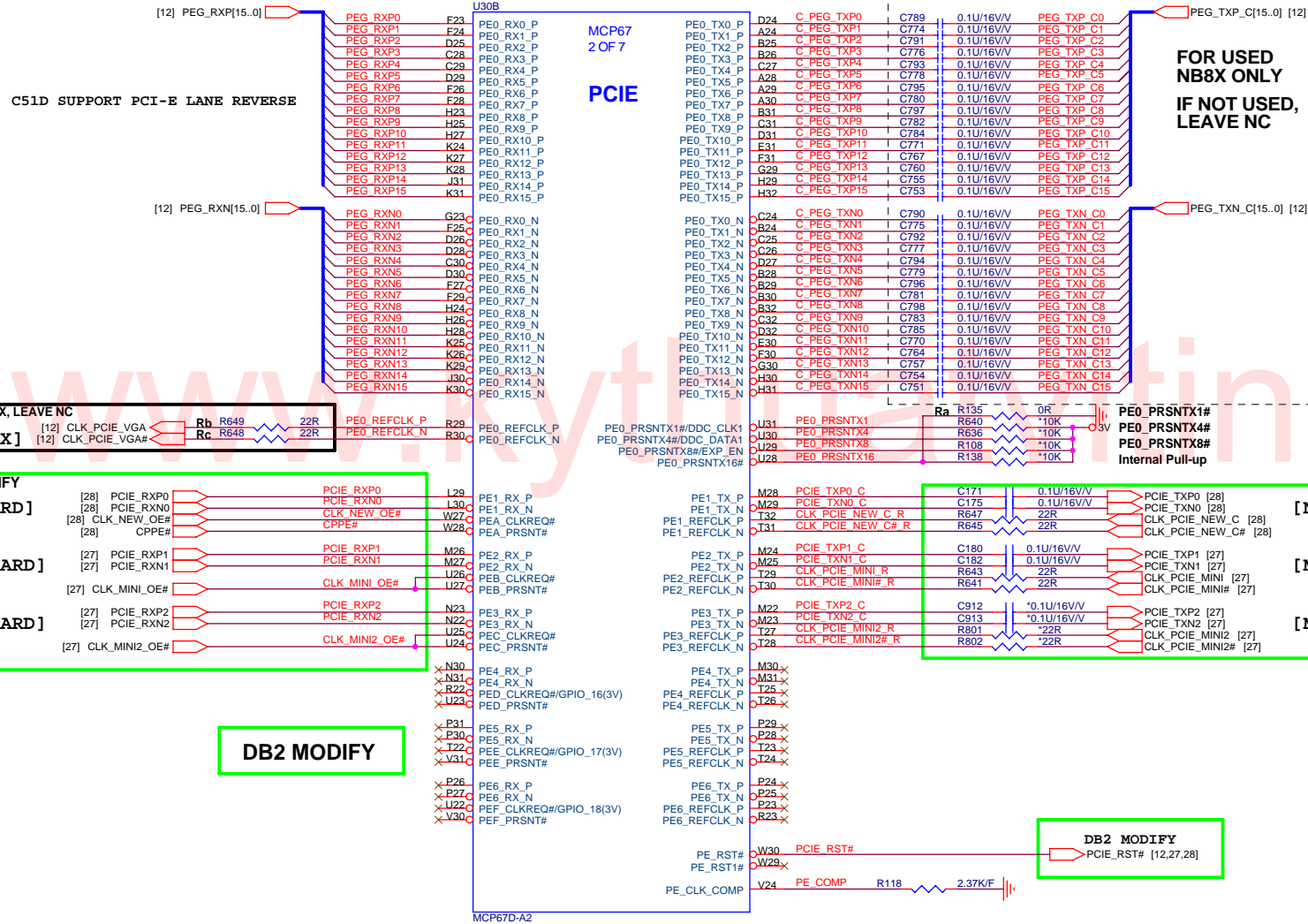


PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number CPU (POWER,GND),DDR2_TERM	Rev C2A
Date: Friday, December 29, 2006 Sheet 4 of 40		



PROJECT : AT1
Quanta Computer Inc.
Size Custom Document Number DDR SO-DIMMx2 (200P) Rev C2A
Date: Friday, December 29, 2006 Sheet 5 of 40

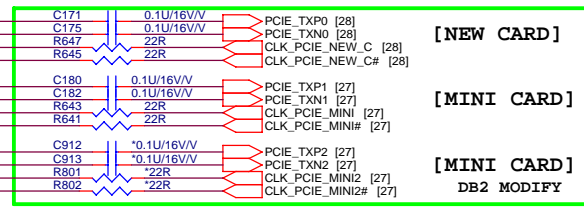
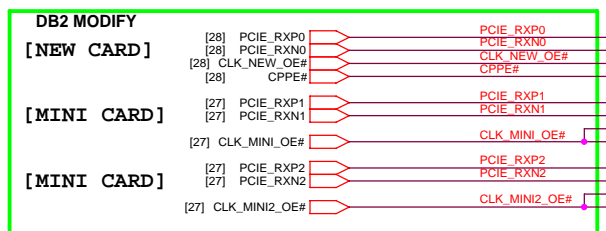


MCP67D & MCP67M DIFFERENCE TABLE

LOCATION	MCP67M (UMA)	MCP67M (DISCRETE)	MCP67D (DISCRETE)
Ra	NC	0R	0R
Rb Rc	NC NC	22R 22R	22R 22R

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	NC

IF NOT USED NB8X, LEAVE NC
 [G7xM/NB8X] [12] CLK_PCIE_VGA# Rb R649 22R PE0_REFCLK_P R29 PE0_REFCLK_P
 [12] CLK_PCIE_VGA# Rc R648 22R PE0_REFCLK_N R30 PE0_REFCLK_N

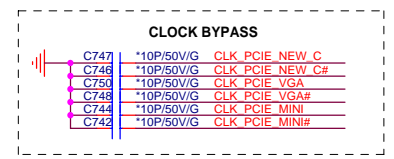
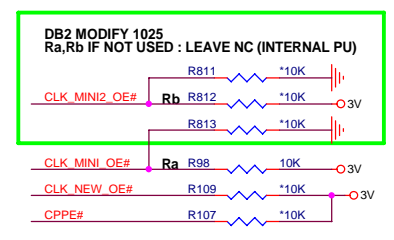


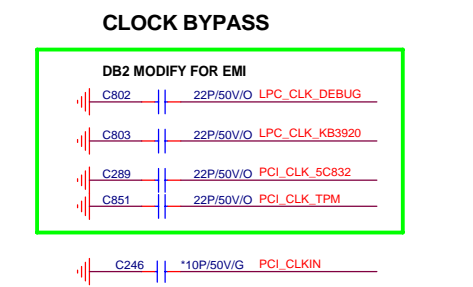
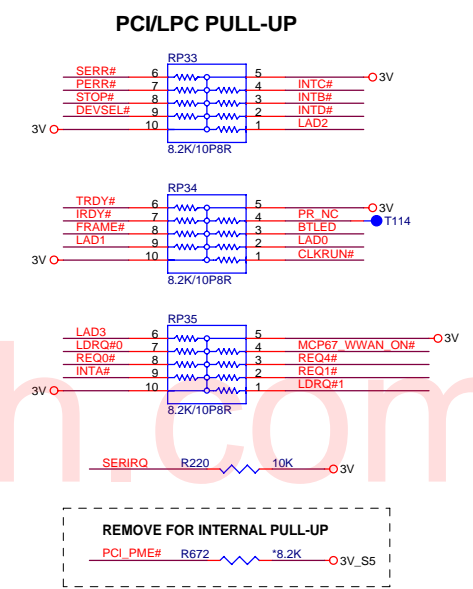
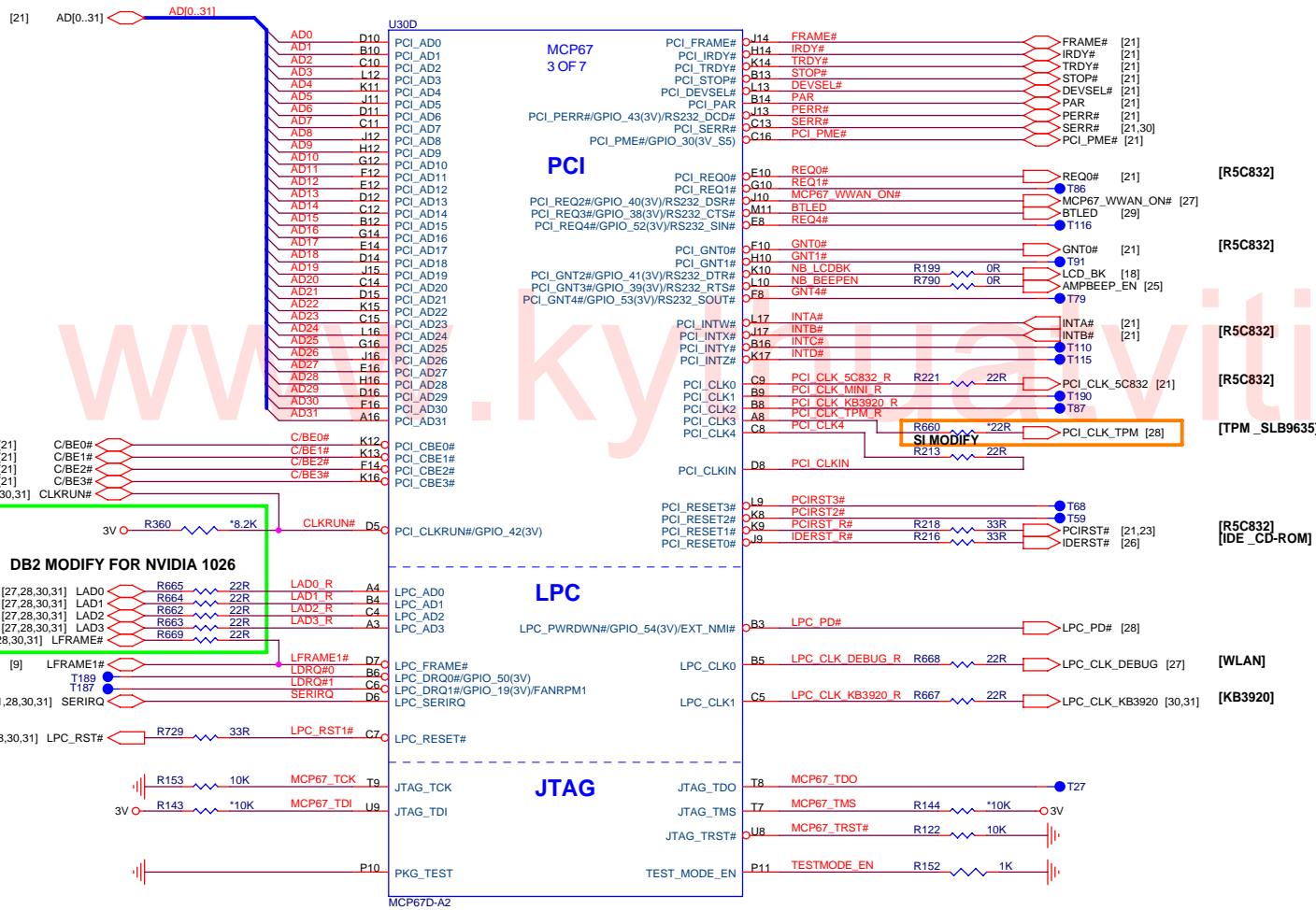
DB2 MODIFY

- N30 PE4_RX_P
- N31 PE4_RX_N
- R22 PE4_CLKREQ#/GPIO_16(3V)
- U23 PE4_PRSNT#
- P31 PE5_RX_P
- P30 PE5_RX_N
- T22 PE5_CLKREQ#/GPIO_17(3V)
- T24 PE5_PRSNT#
- P28 PE6_RX_P
- P27 PE6_RX_N
- U22 PEF_CLKREQ#/GPIO_18(3V)
- V30 PEF_PRSNT#

DB2 MODIFY

- W30 PCIE_RST#
- W29 PE_RST#
- V24 PE_COMP R118 2.37K/F

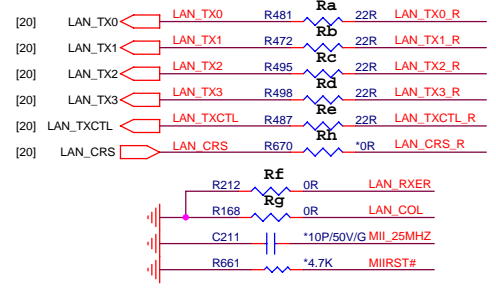




3V
3V_S5

[2,5,6,7,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
[9,10,11,20,28,30,32,33,37]

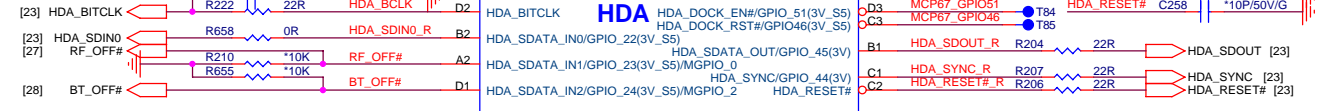
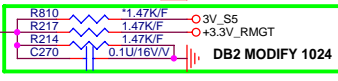
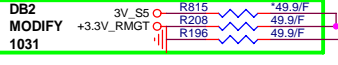
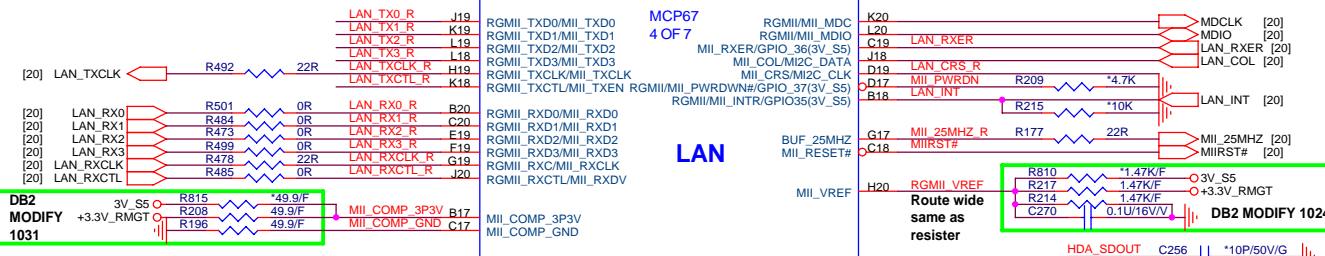
10/100 - GIAG LAN STUFF OPTION



MODIFY 0824

	10/100	GTGA
Ra	0R	22R
Rb	0R	22R
Rc	0R	22R
Rd	0R	22R
Re	0R	22R
Rf	0R	22R
Rg	NC	0R
Rh	NC	0R

U30E



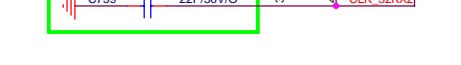
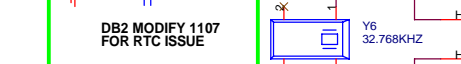
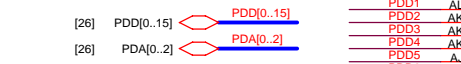
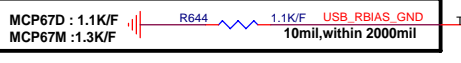
[USB CONN]

[Bluetooth module]

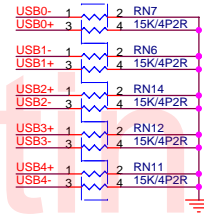
[Port Docking]

[PCI-E MINI Card]

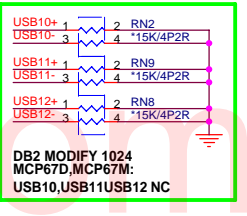
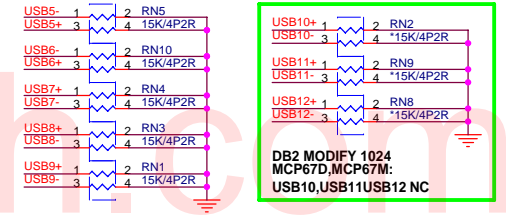
[FINGER PRINT]



MODIFY 0823



USB PULL-DOWN



MCP67 STRAPPING

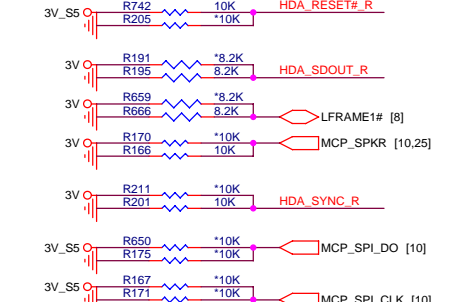
HDA RESET# (LAN)	
0	MIL
4	RGMIU (DEFAULT)

HDA SDOUT R (LFRAM1# (BIOS))	
00	LPC (DEFAULT)
01	PCI BIOS
10	SPI BIOS
11	RESERVED (SPI)

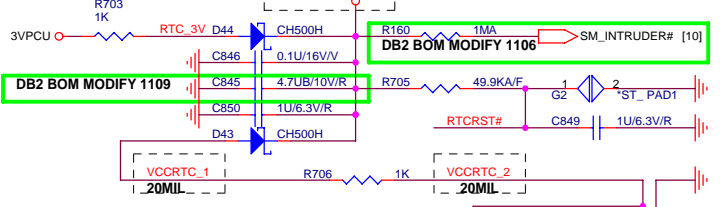
HDA SYNC R (SIO CLOCK)	
0	14.318MHz (DEFAULT)
1	24MHz

SPI DO, SPI CLK (SPI CLOCK)	
00	31MHz
01	42MHz
10	25MHz
11	1MHz

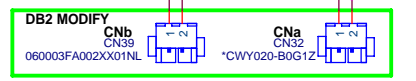
MODIFY 0824



RTC



BATTERY HOLDER TYPE	
CNa	USED BATTERY 2P CONNECTOR
CNb	USED BATTERY HOLDER

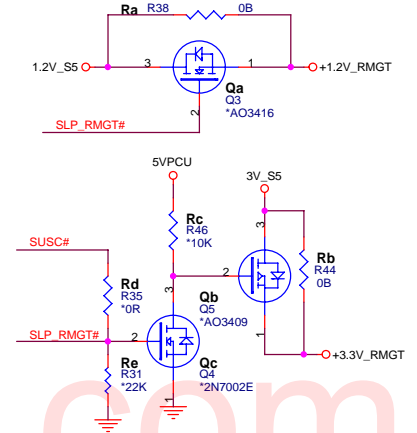


PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MCP67 (LAN,HDA,USB,ATA,RTC)	Rev C2A
Date: Friday, December 29, 2006		Sheet 9 of 40

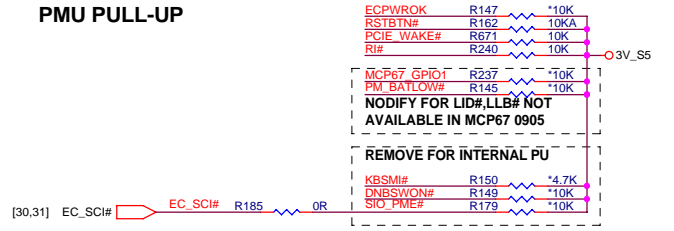
- +3.3V_RMGT [10,11]
- 3V [2,5,6,7,8,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
- 3V_S5 [8,10,11,20,28,30,32,33,37]
- 3VPCU [14,18,28,29,30,31,33,34,35]

CORE POWER CIRCUIT FOR SLEEP MODE MCP67M SUPPORT ONLY



	MCP67M UMA	MCP67D DISCRETE
Ra	NC	STUFF
Rb	NC	STUFF
Rc	STUFF	NC
Rd	NC	NC
Re	STUFF	NC
Qa	STUFF	NC
Qb	STUFF	NC
Qc	STUFF	NC

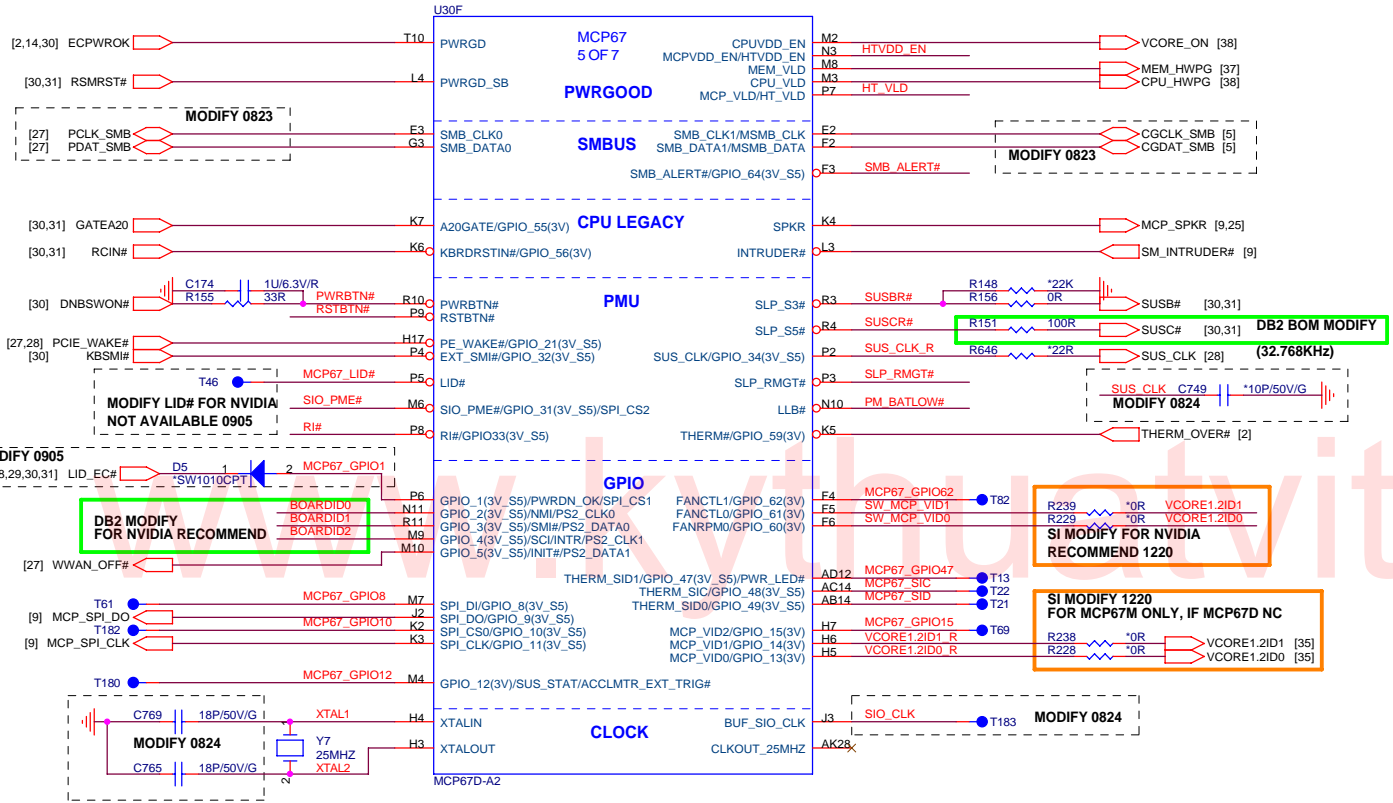
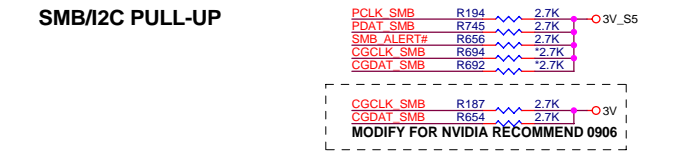
PMU PULL-UP



CPU LEGACY PULL-UP

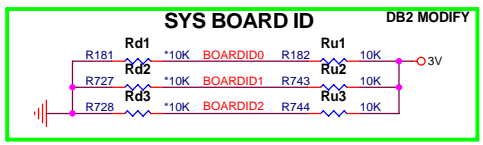


SMB/I2C PULL-UP

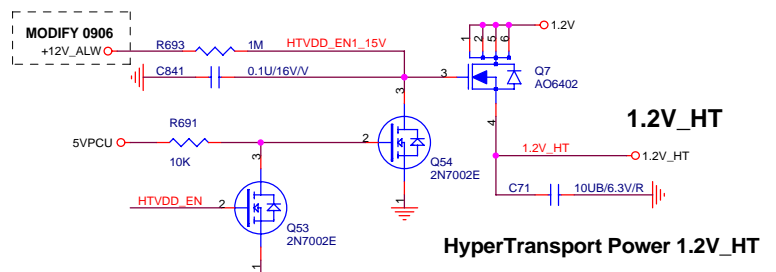
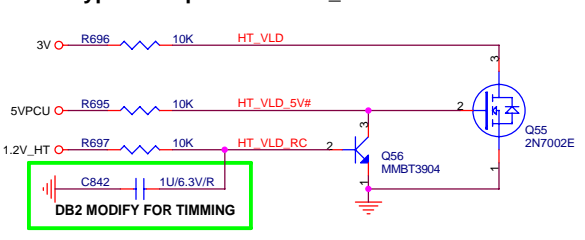


SKU (BOARD ID)	AT1A (DISCRETE)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (DISCRETE)	AT2A (UMA)
Board ID	010	X00	X00	111	X01
ID0 STUFF	Rd1	Rd1	Rd1	Ru1	Ru1
ID1 STUFF	Ru2	Rd2	Rd2	Ru2	Rd2
ID2 STUFF	Rd3			Ru3	

Board ID :	0/1	0/1	0/1
DIFINE	RESERVE / RESERVE	UMA / DISCRETE	AT1 / AT2



HyperTransport Link 1.2 V_HT Power Valid

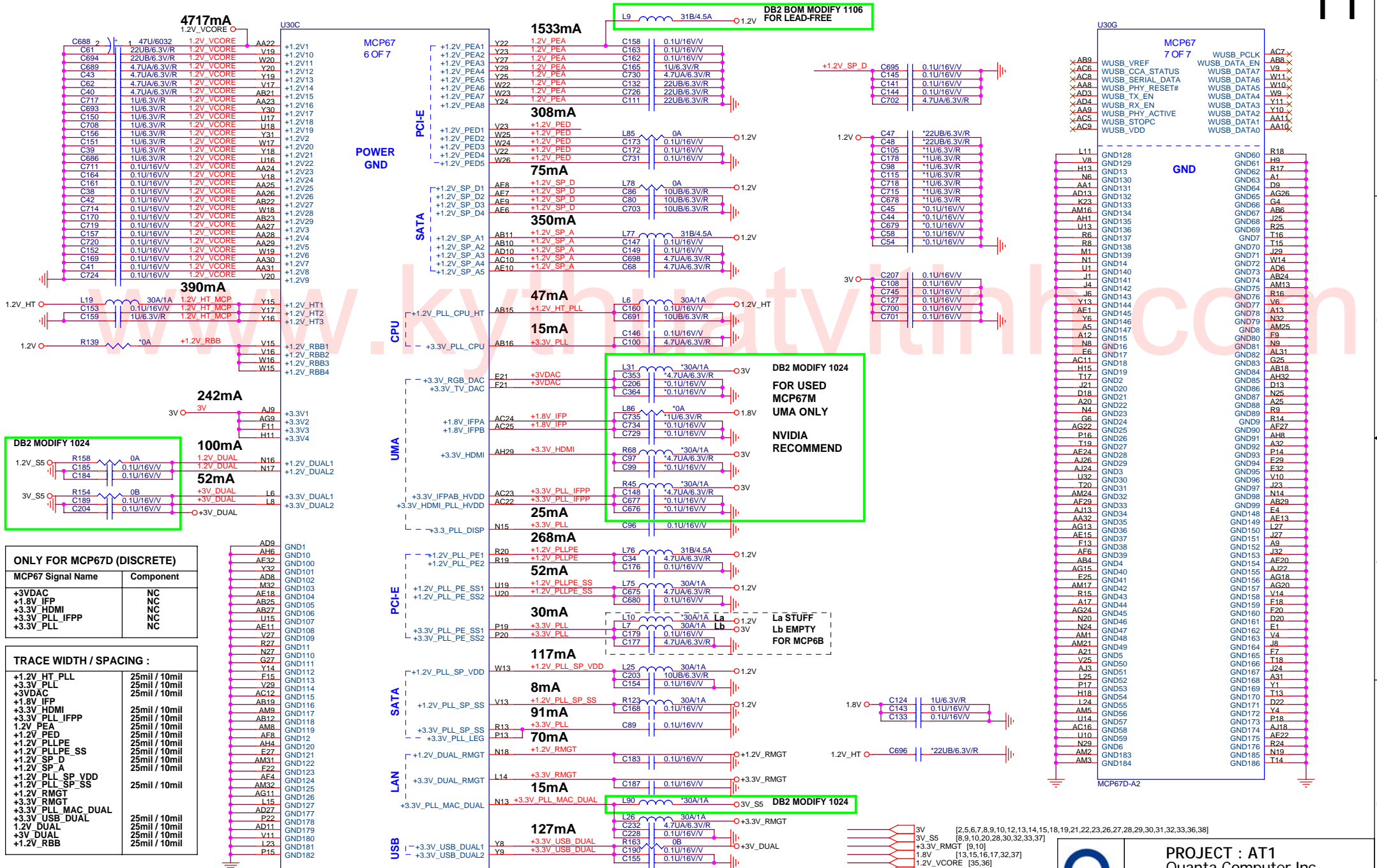


- +1.2V_RMGT [11]
- 1.2V_S5 [11,32,35]
- 1.2V_HT [2,6,11]
- 1.2V [11,12,13,15,36]
- +3.3V_RMGT [9,11]
- 3V_S5 [2,5,6,7,8,9,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
- 5VPCU [23,33,34,35,36,37,38]
- +12V_ALW [18,32,33]

PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MCP67 (PG,SMB,PMU,GPIO,CLK)	Rev C2A
Date: Friday, December 29, 2006	Sheet 10	of 40

MCP67 POWER PLANE/GND & BYPASS



ONLY FOR MCP67D (DISCRETE)

MCP67 Signal Name	Component
+3VDAC	NC
+1.8V_IFP	NC
+3.3V_HDMI	NC
+3.3V_PLL_IFPP	NC
+3.3V_PLL	NC

TRACE WIDTH / SPACING :

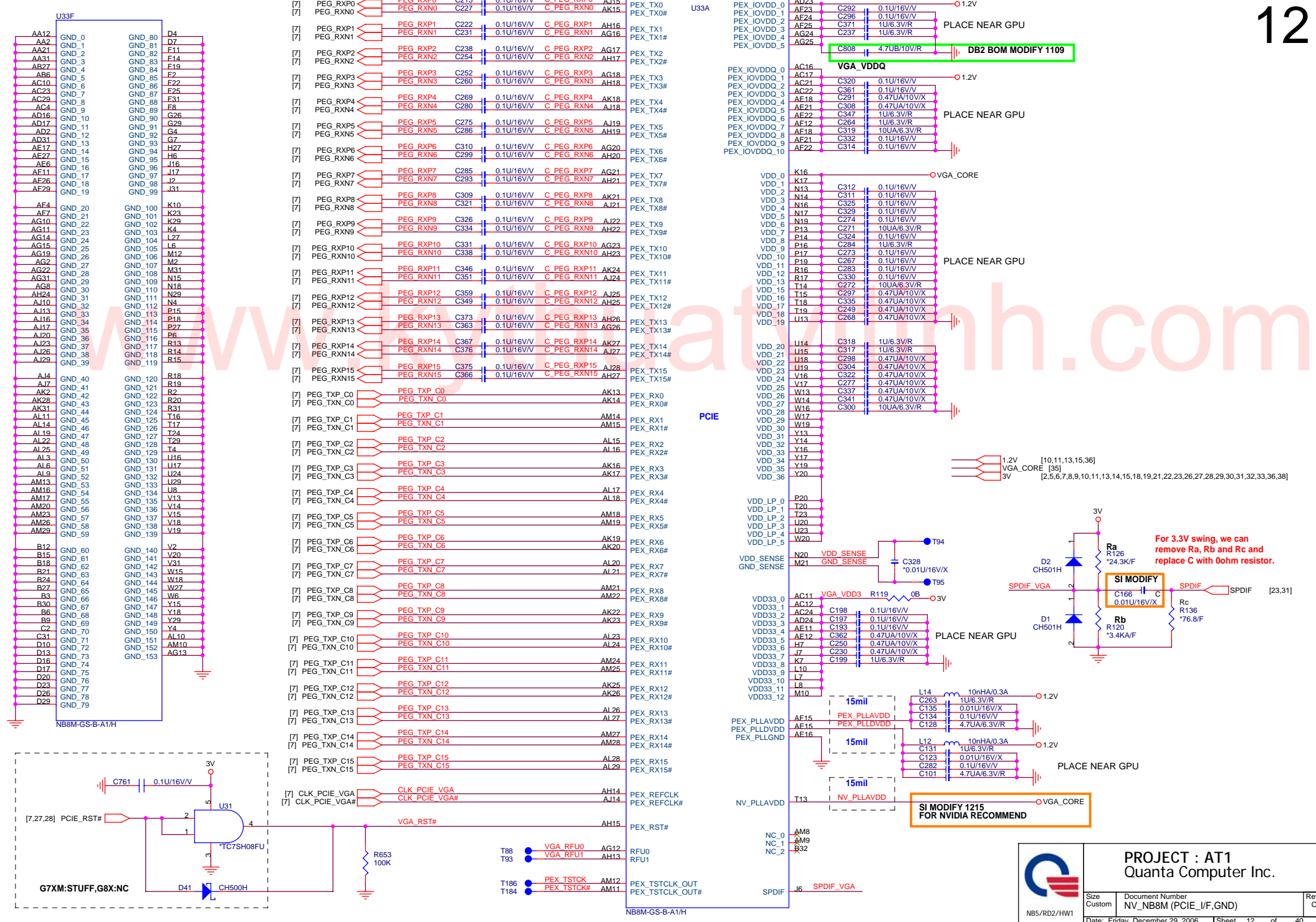
+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	25mil / 10mil
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
+1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	25mil / 10mil
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	25mil / 10mil
+3.3V_RMGT	25mil / 10mil
+3.3V_PLL_MAC_DUAL	25mil / 10mil
+3.3V_USB_DUAL	25mil / 10mil
+1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil



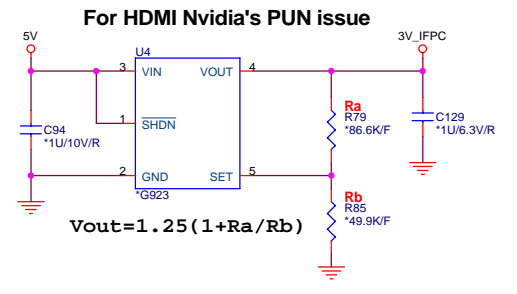
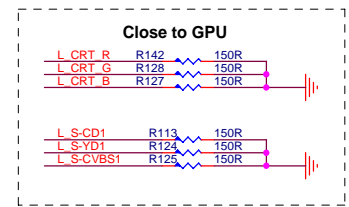
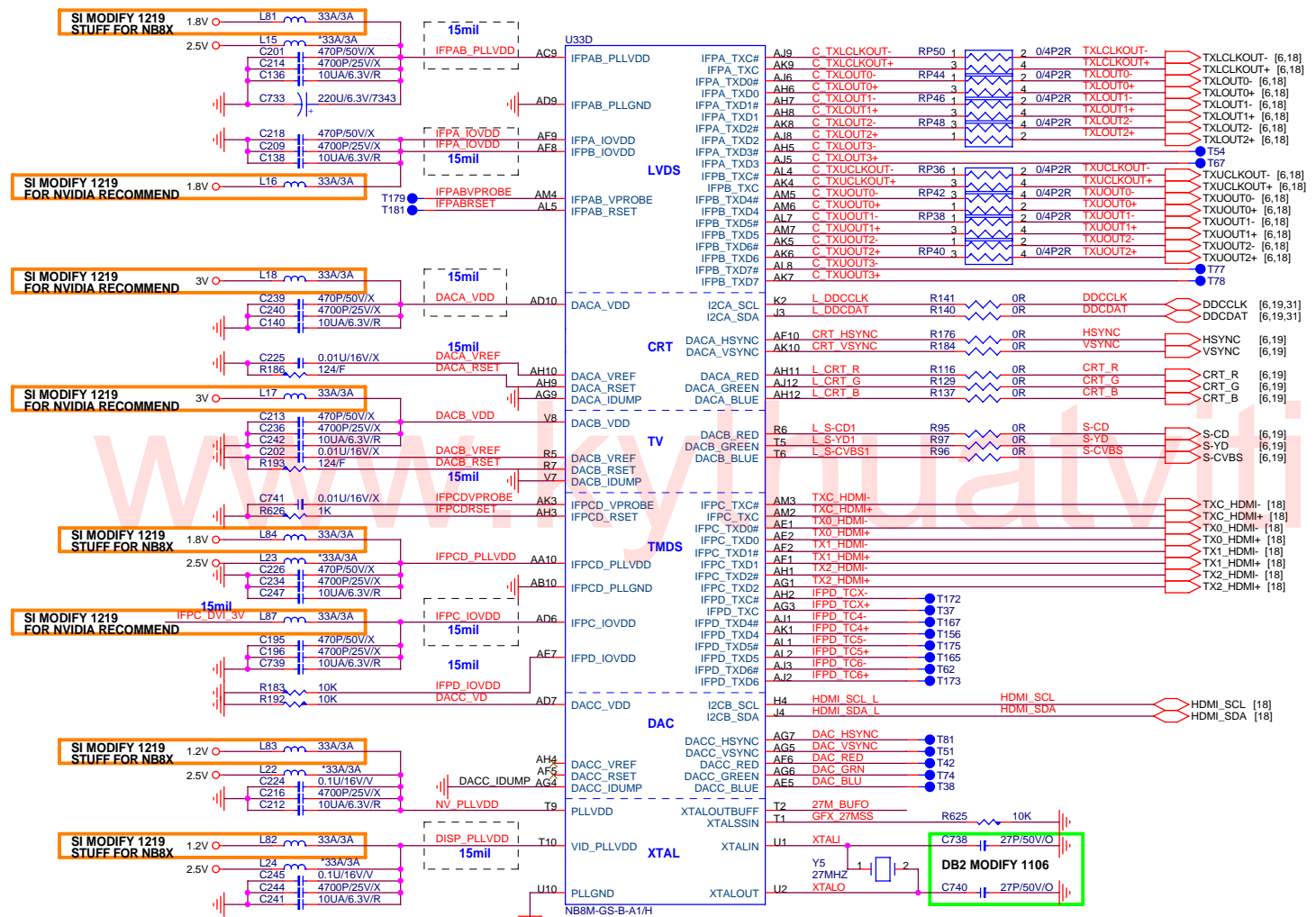
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MCP67 (POWER,GND)	Rev C2A
Date: Friday, December 29, 2006	Sheet 11 of 40	

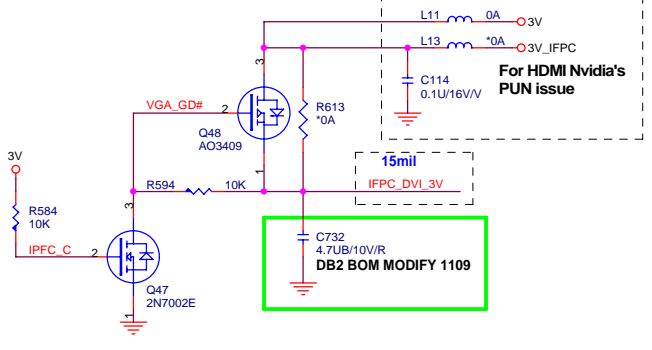
- 3V [2,5,6,7,8,9,10,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
- 3V_S5 [8,9,10,20,28,30,32,33,37]
- +3.3V_RMGT [9,10]
- 1.8V [13,15,16,17,32,37]
- 1.2V_VCORE [35,36]
- 1.2V_HT [10,12,13,15,36]
- 1.2V_HT [2,6,10]
- 1.2V_S5 [10,32,35]
- +1.2V_RMGT [10]



	PROJECT : AT1 Quanta Computer Inc.		
	Size Custom	Document Number NV_NB8M (PCI_E_I/F,GND)	Rev C2A
Date: Friday, December 29, 2006			Sheet 12 of 40



FOR IFPC VDD LEAKAGE CIRCUIT

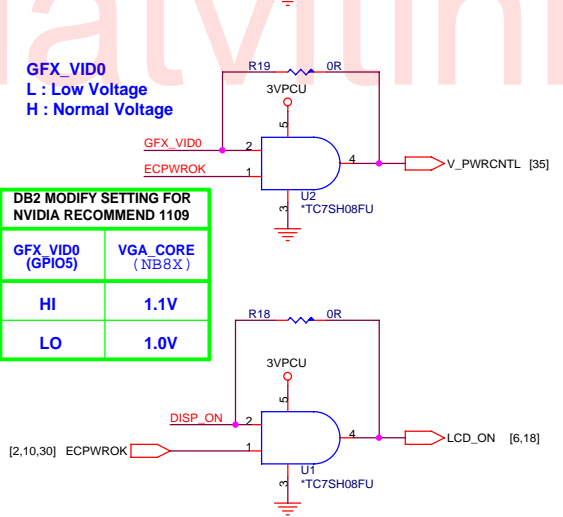
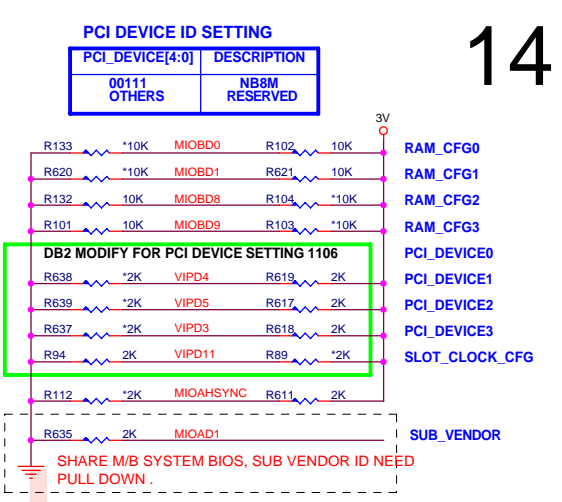
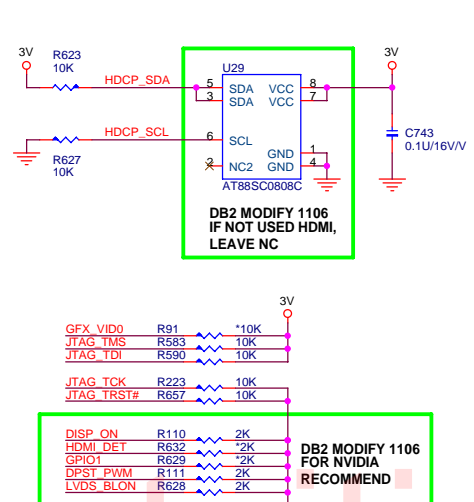
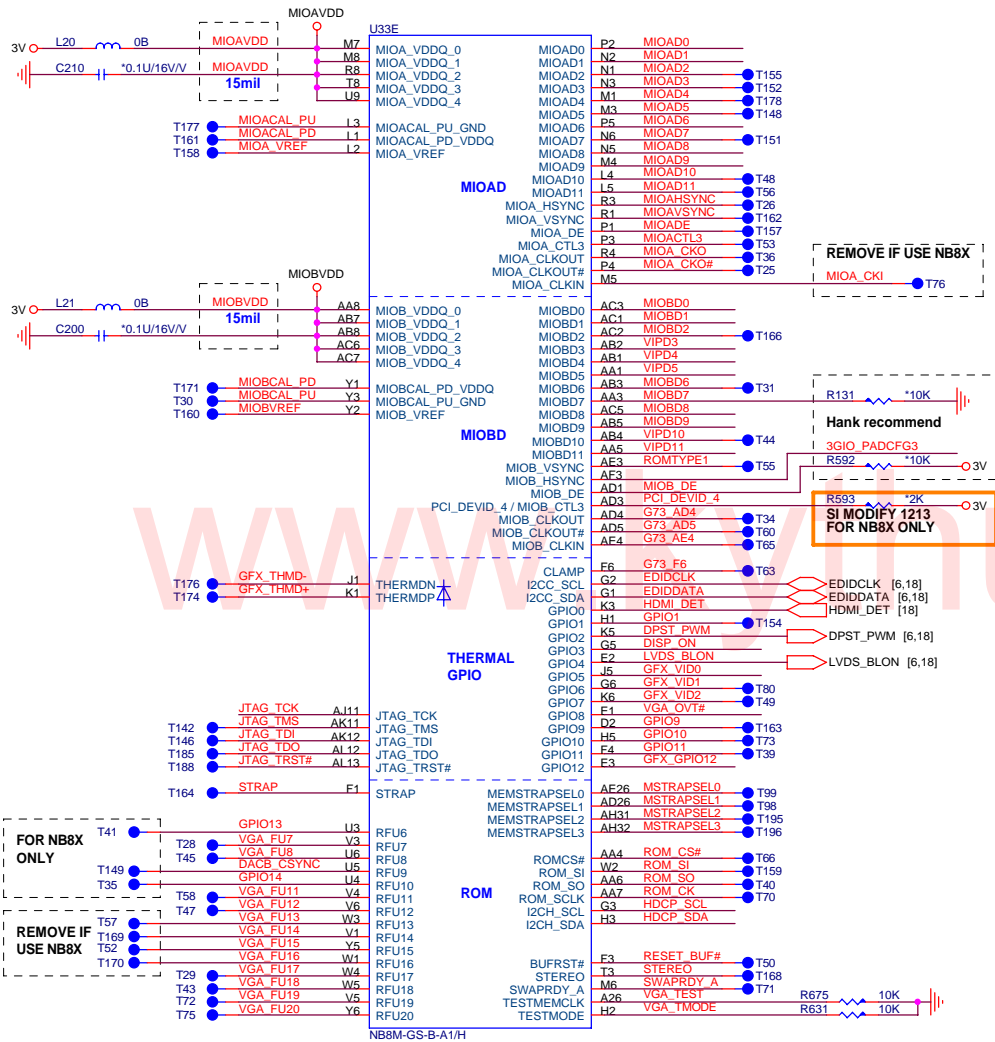


1.2V	[10,11,12,15,36]
1.8V	[11,15,16,17,32,37]
2.5V	[2,32,36]
3V	[2,5,6,7,8,9,10,11,12,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
5V	[18,19,22,23,25,26,27,28,29,31,32,33,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number NV_NB8M (LVDS,CRT,TV,HDMI)	Rev C2A
Date: Friday, December 29, 2006	Sheet 13 of 40	

NBS/RD2/HW1

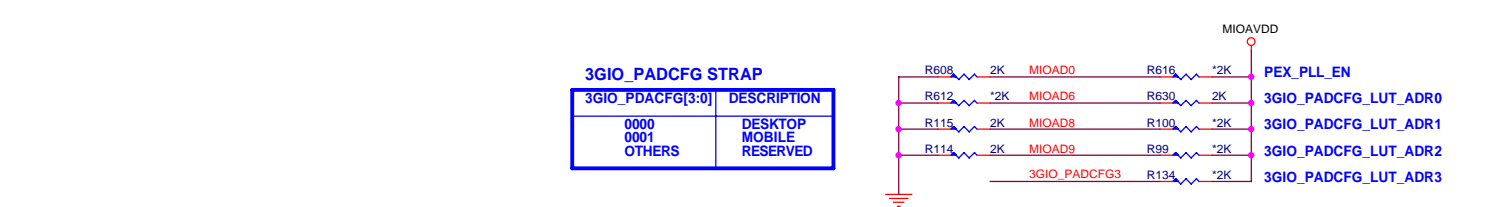
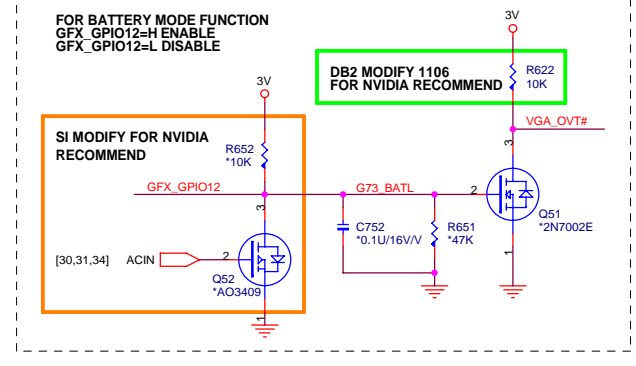


NB8X 64bit VRAM Configuration Table

RAM_CFG3[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infinion
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infinion
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

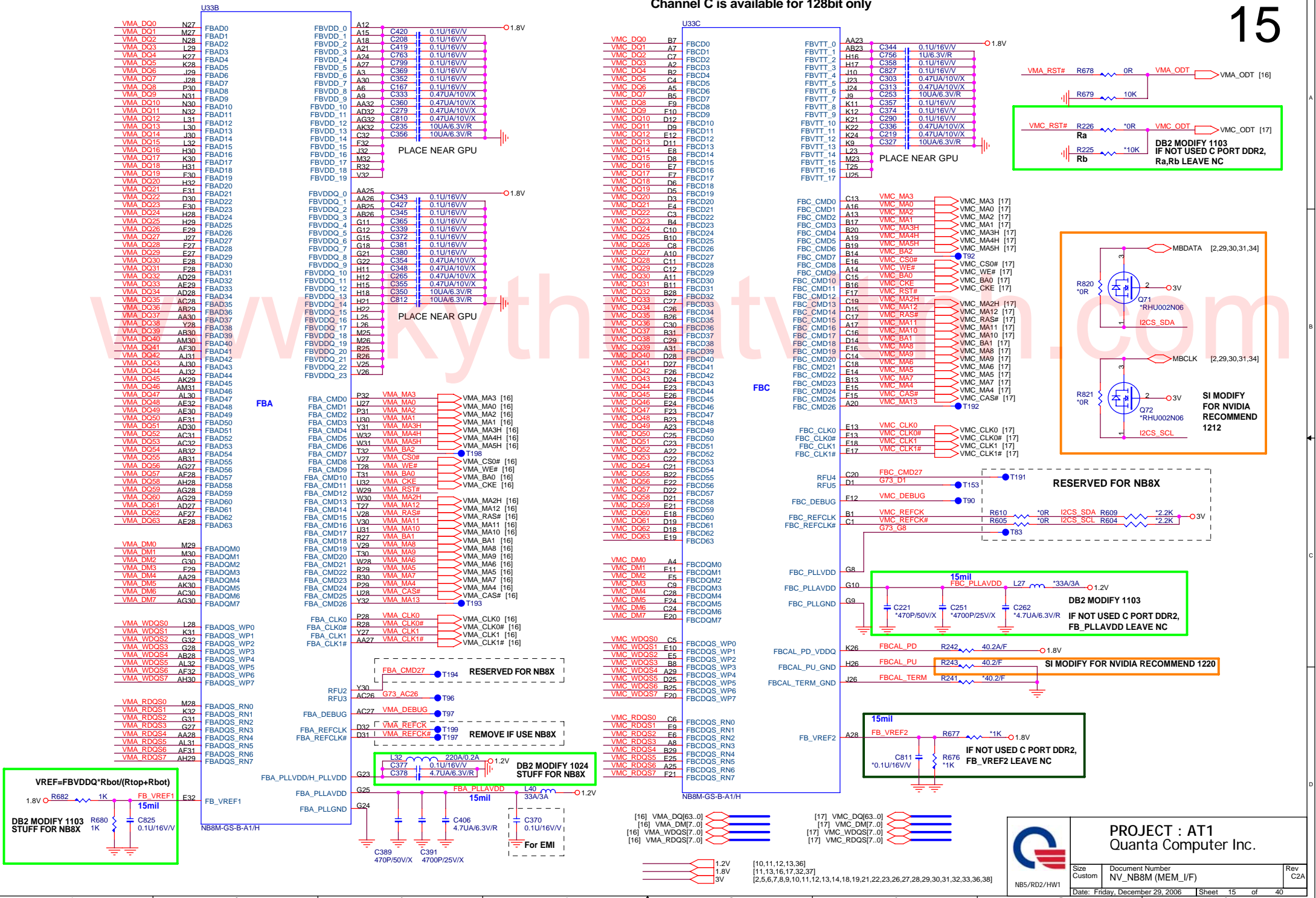
NB8X 128bit VRAM Configuration Table

RAM_CFG3[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infinion
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infinion
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infinion
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



3V [2,5,6,7,8,9,10,11,12,13,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU [9,18,28,29,30,31,33,34,35]

Channel C is available for 128bit only



VMA_RST# R678 *0R VMA_ODT VMA_ODT [16]
 R679 *10K
 VMC_RST# R226 *0R VMC_ODT VMC_ODT [17]
 R225 *10K
**DB2 MODIFY 1103
 IF NOT USED C PORT DDR2,
 Ra,Rb LEAVE NC**

MBDATA [2,29,30,31,34]
 R820 *0R
 Q71 *RHU002N06
 I2CS_SDA
 MBCLK [2,29,30,31,34]
 R821 *0R
 Q72 *RHU002N06
 I2CS_SCL
SI MODIFY FOR NVIDIA RECOMMEND 1212

RESERVED FOR NB8X
 C20 FBC_CMD27
 D1 G73_D1
 T153
 T191
 F12 VMC_DEBUG
 T90
 B1 VMC_REFCK
 C1 VMC_REFCK#
 R610 *0R I2CS_SDA R609 *2.2K
 R605 *0R I2CS_SCL R604 *2.2K
 G73_G8
 T83

15mil
 FBC_PLLAVDD L27 *33A/3A
 0.1.2V
 C221 *470P/50V/X
 C251 *4700P/25V/X
 C262 *4.7UA/6.3V/R
**DB2 MODIFY 1103
 IF NOT USED C PORT DDR2,
 FB_PLLAVDD LEAVE NC**

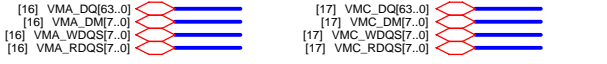
15mil
 FB_VREF2 R677 *1K
 0.1.8V
 C811 *0.1U/16V/V
 R676 *1K
**IF NOT USED C PORT DDR2,
 FB_VREF2 LEAVE NC**

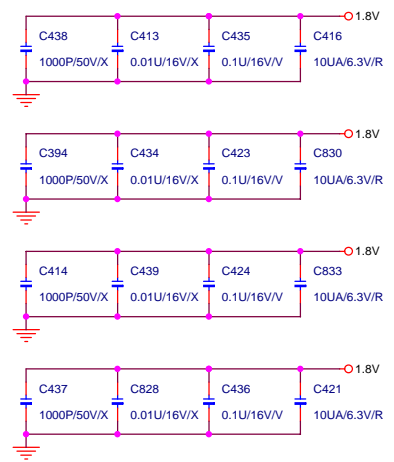
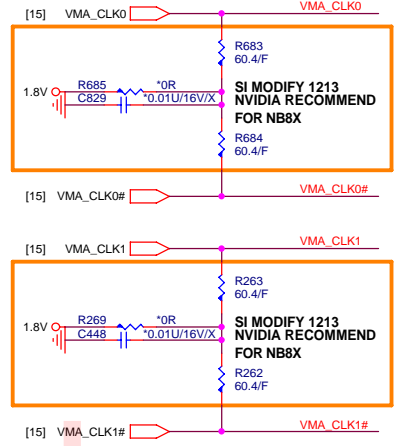
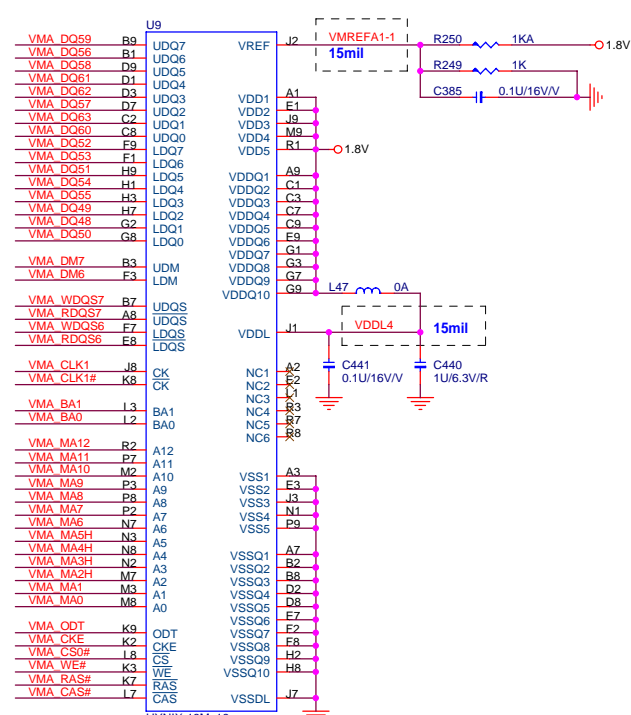
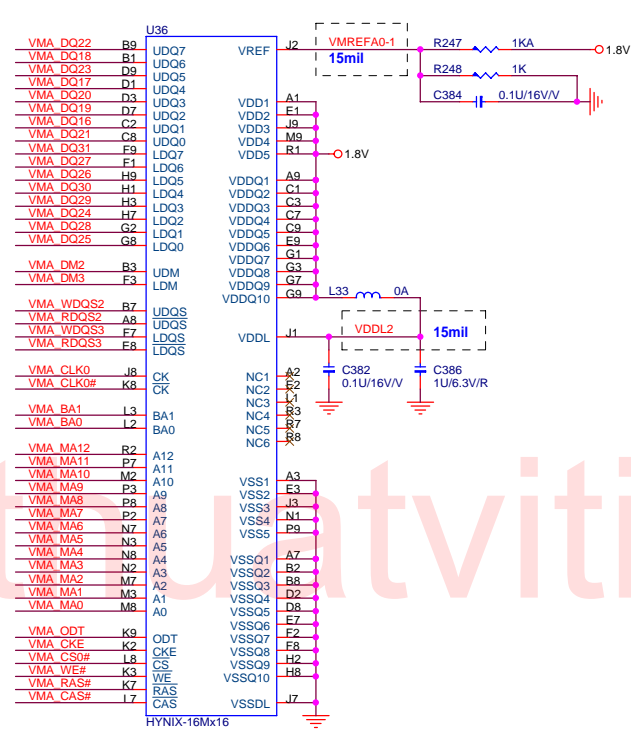
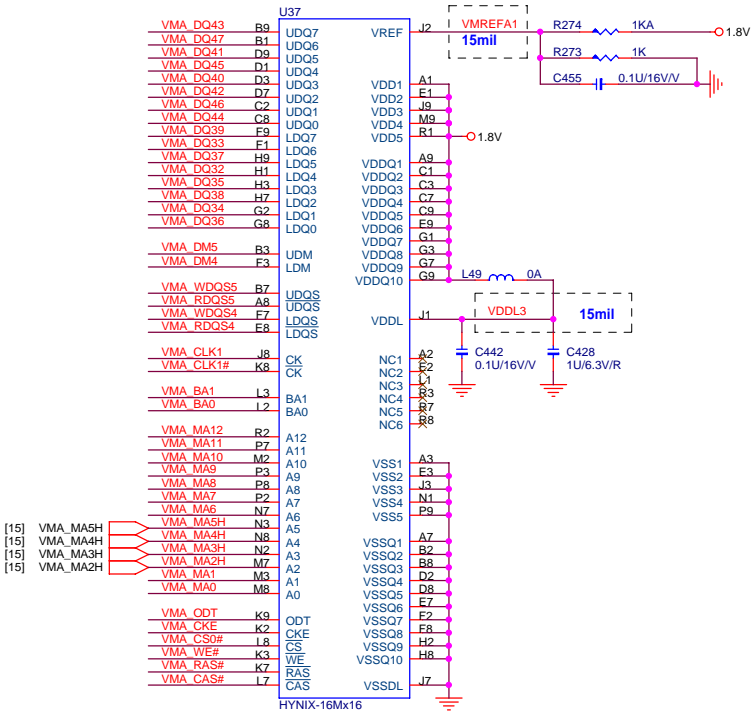
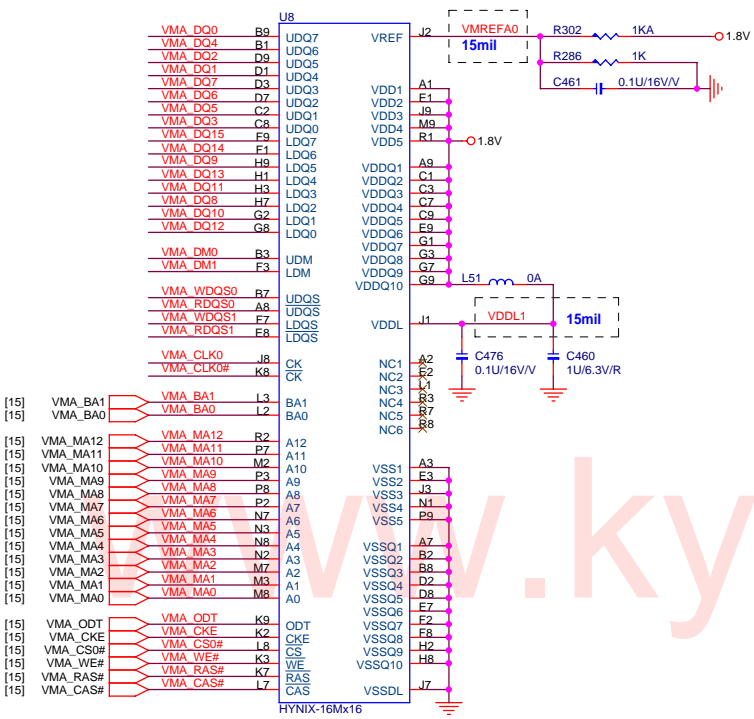
VREF=FBVDDQ*(Rbo/(Rtop+Rbot))
 1.8V R682 *1K
 FB_VREF1
 15mil
 R680 1K
 C825 0.1U/16V/V
**DB2 MODIFY 1103
 STUFF FOR NB8X**

RESERVED FOR NB8X
 FBA_CMD27 T194
 Y30 G73 AC26 T96
 AC26

REMOVE IF USE NB8X
 D32 VMA_REFCK T199
 D31 VMA_REFCK# T197

L32 220A/0.2A
 C377 0.1U/16V/V
 C378 4.7UA/6.3V/R
 0.1.2V
**DB2 MODIFY 1024
 STUFF FOR NB8X**



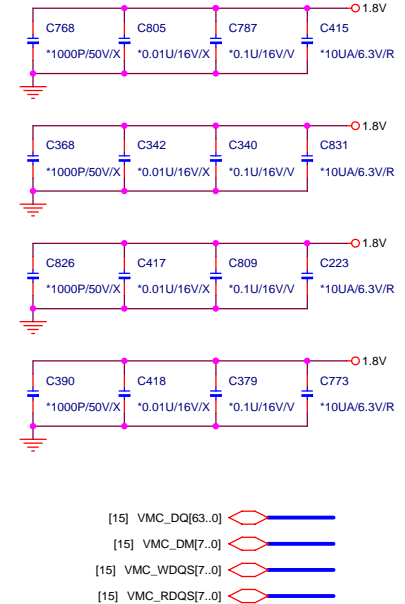
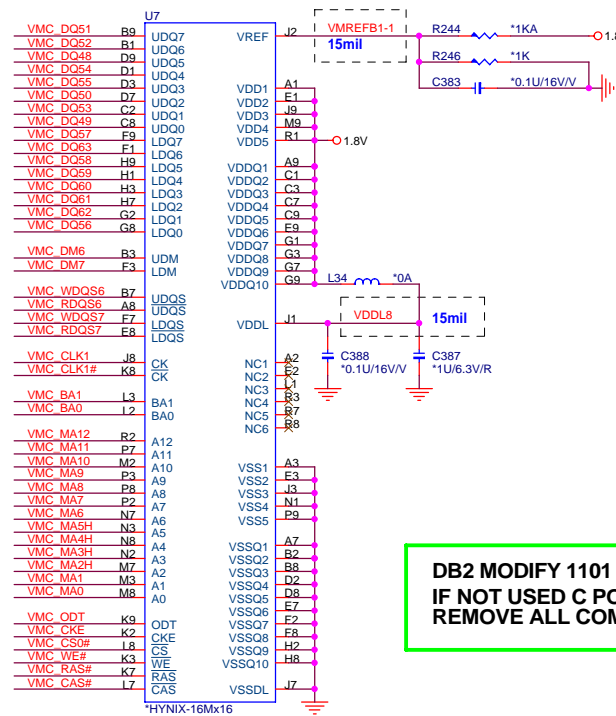
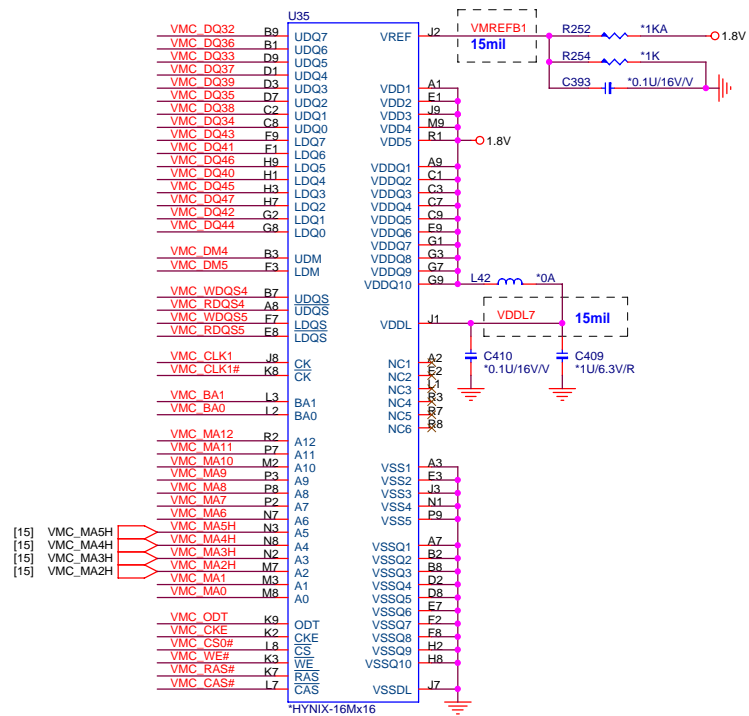
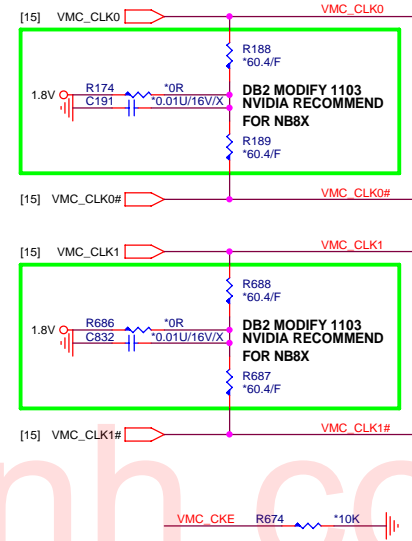
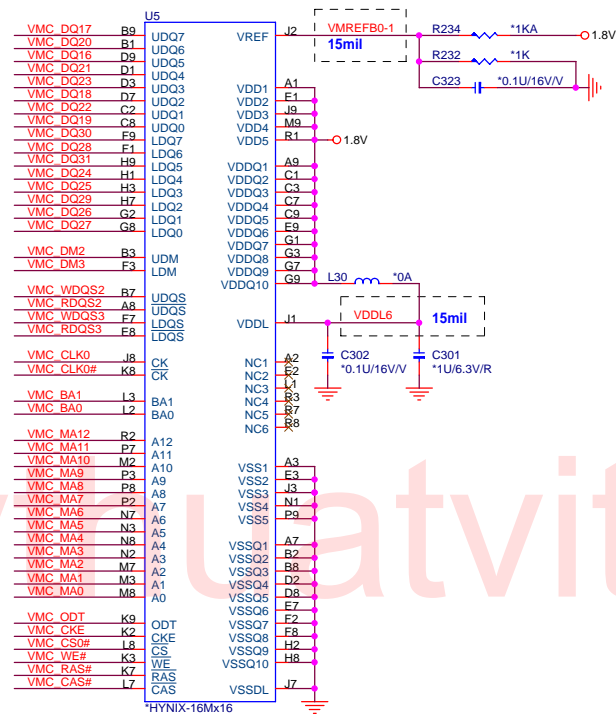
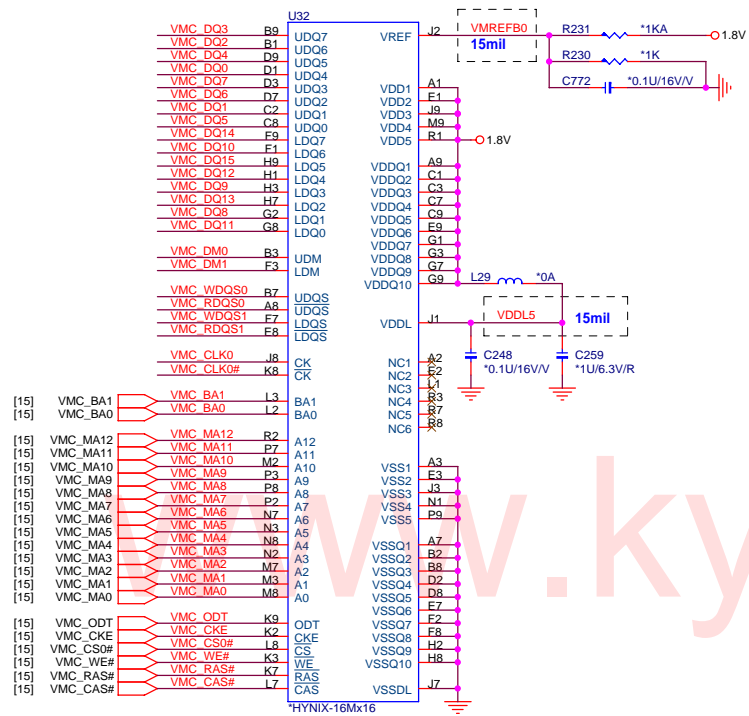


HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25_1.8V)
 INFINEON-16Mx16 : AKD5JG-T*08 (HYB18T256161AFL25)
 SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)



PROJECT : AT1
 Quanta Computer Inc.

Size Custom	Document Number NV_NB8M VRAM-1(GDDR2 BGA84)	Rev C2A
Date: Friday, December 29, 2006	Sheet 16 of 40	



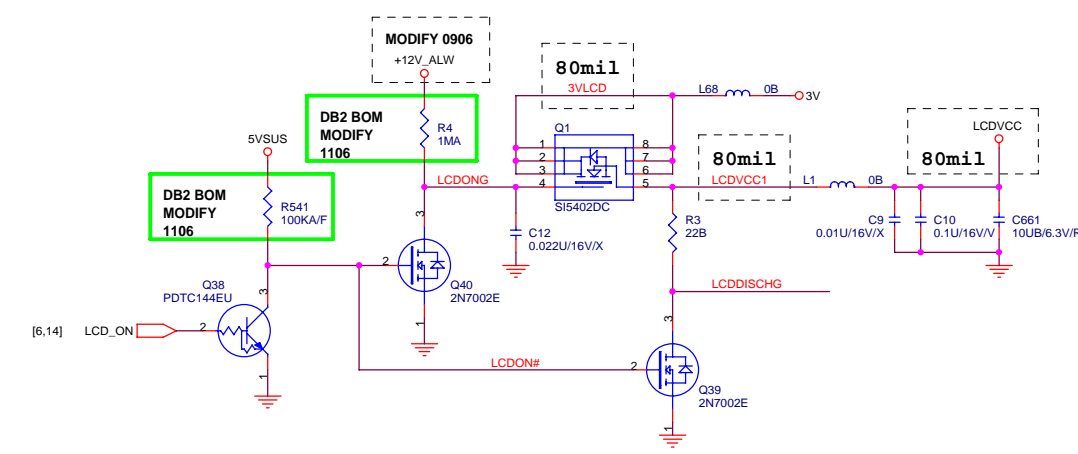
**DB2 MODIFY 1101
IF NOT USED C PORT DDR2,
REMOVE ALL COMPONENTS**

HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25_1.8V)
INFINEON-16Mx16 : AKD5JG-T*08 (HYB18T256161AFL25)
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)

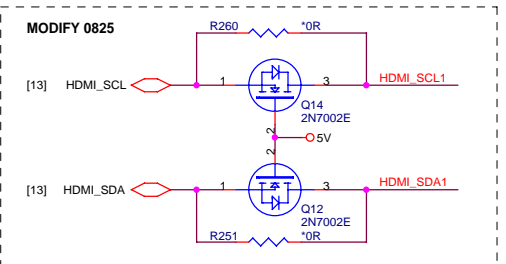
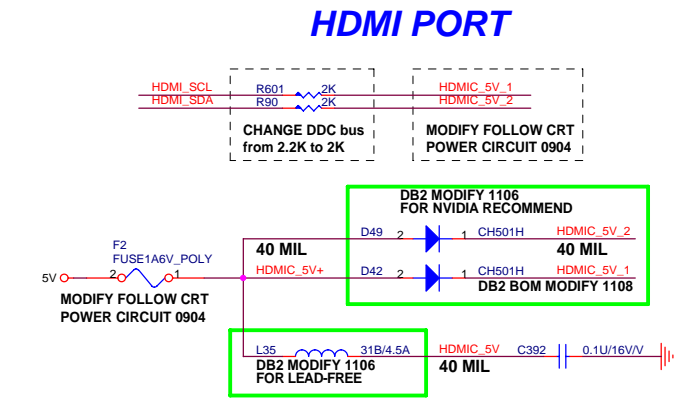
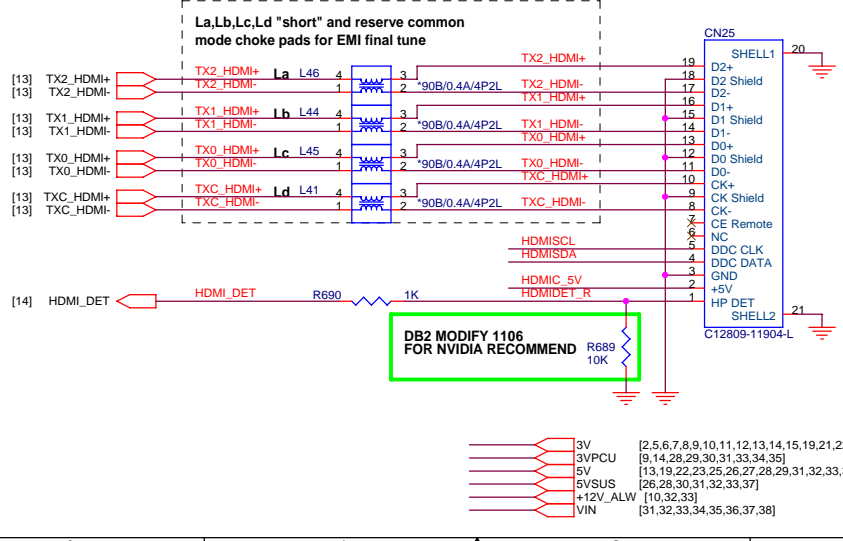
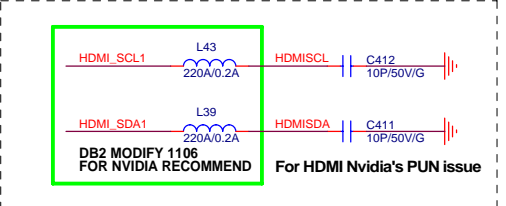
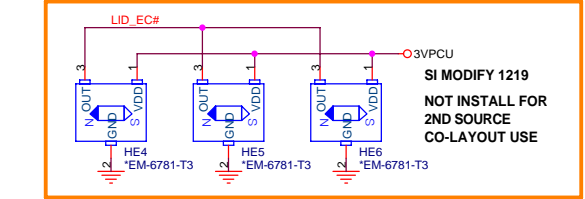
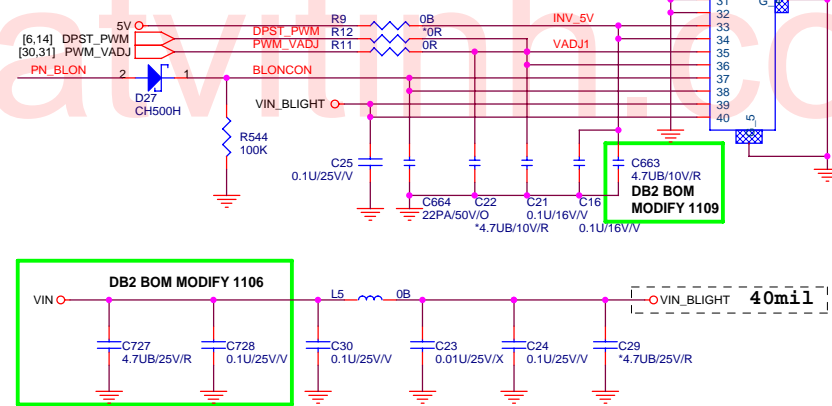
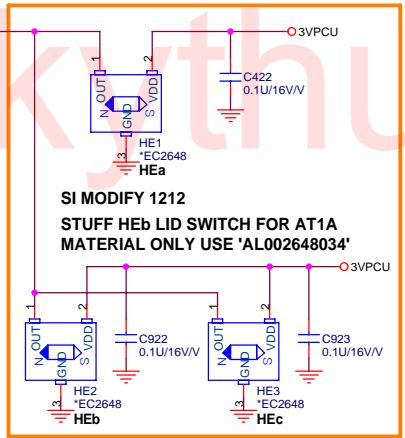
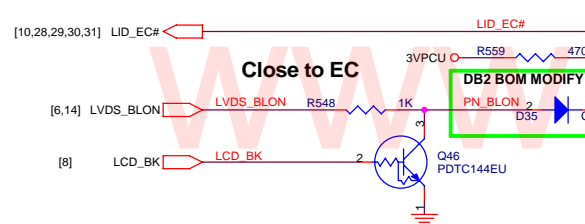
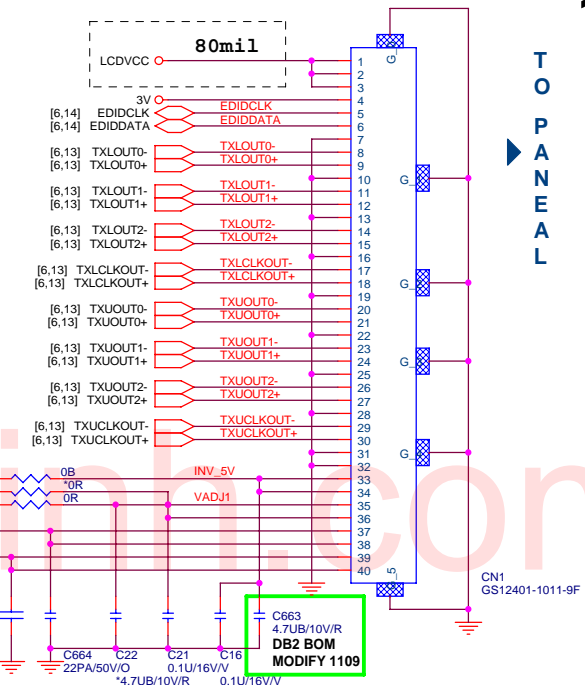
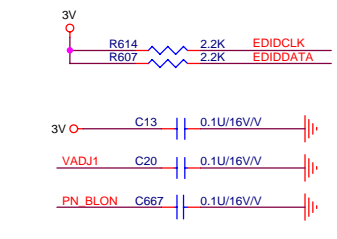
**PROJECT : AT1
Quanta Computer Inc.**

Size Custom	Document Number NV_NB8M VRAM-2(GDDR2 BGA84)	Rev C2A
Date: Friday, December 29, 2006	Sheet 17	of 40

T O P A N E A L



LCD CONNECTOR

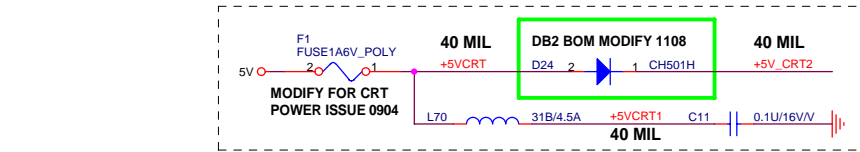
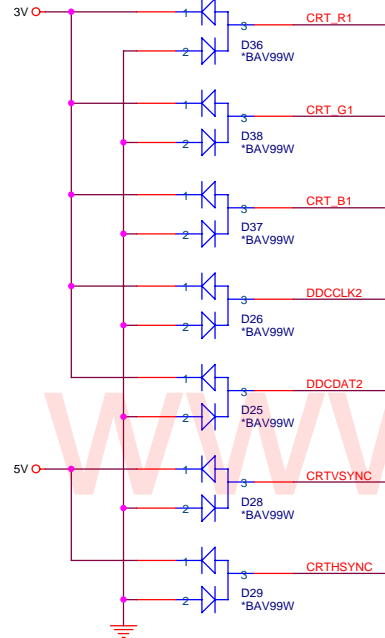


3V	[2,5,6,7,8,9,10,11,12,13,14,15,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU	[9,14,28,29,30,31,33,34,35]
5V	[13,19,22,23,25,26,27,28,29,31,32,33,36,38]
5VSUS	[26,28,30,31,32,33,37]
+12V_ALW	[10,32,33]
VIN	[31,32,33,34,35,36,37,38]

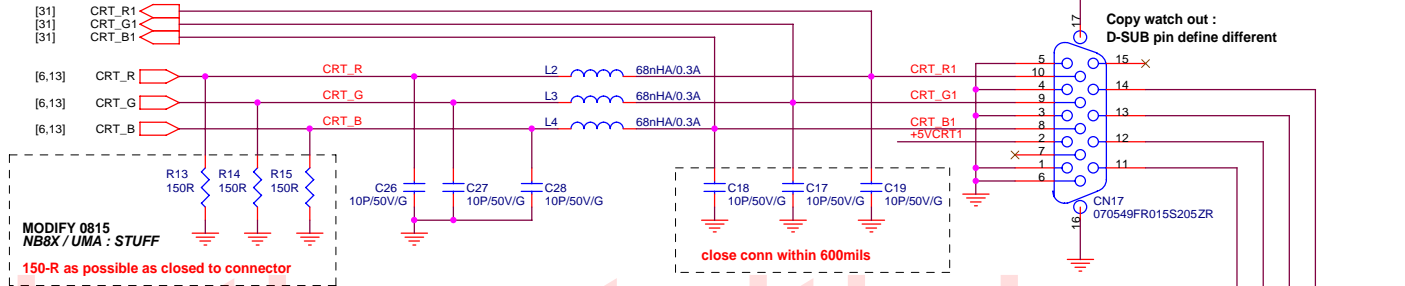


PROJECT : AT1
Quanta Computer Inc.

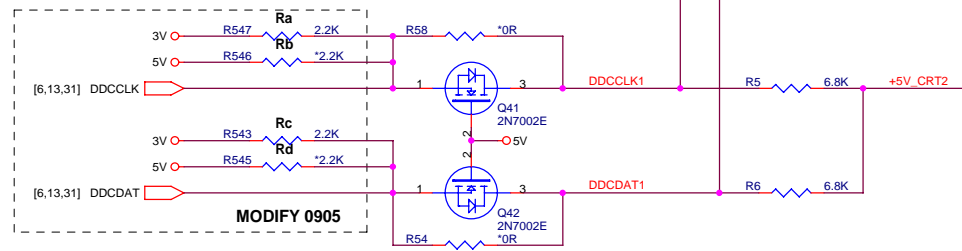
Size Custom	Document Number LCD,HDMI,LID_SW	Rev C2A
Date: Friday, December 29, 2006		Sheet 18 of 40



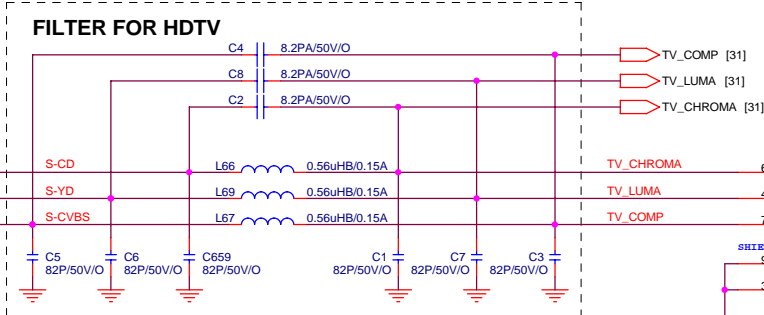
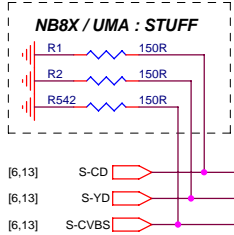
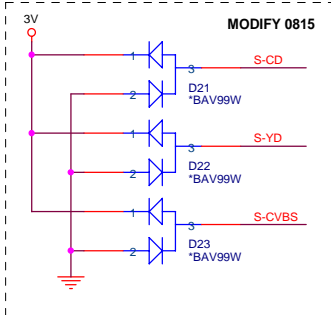
CRT PORT



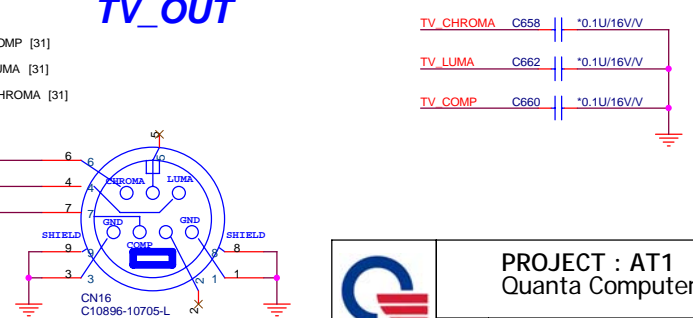
NB8X & MCP67M DIFFERENCE		
LOCATION	NB8X (DISCRETE)	MCP67M (UMA)
Ra	2.2K	NC
Rb	NC	2.2K
Rc	2.2K	NC
Rd	NC	2.2K



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,21,22,23,26,27,28,29,30,31,32,33,36,38]
 5V [13,18,22,23,25,26,27,28,29,31,32,33,36,38]

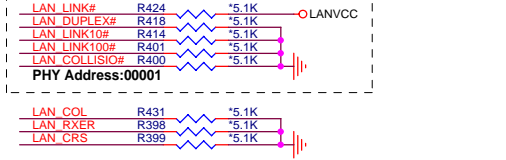
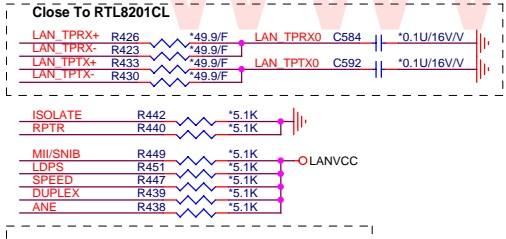
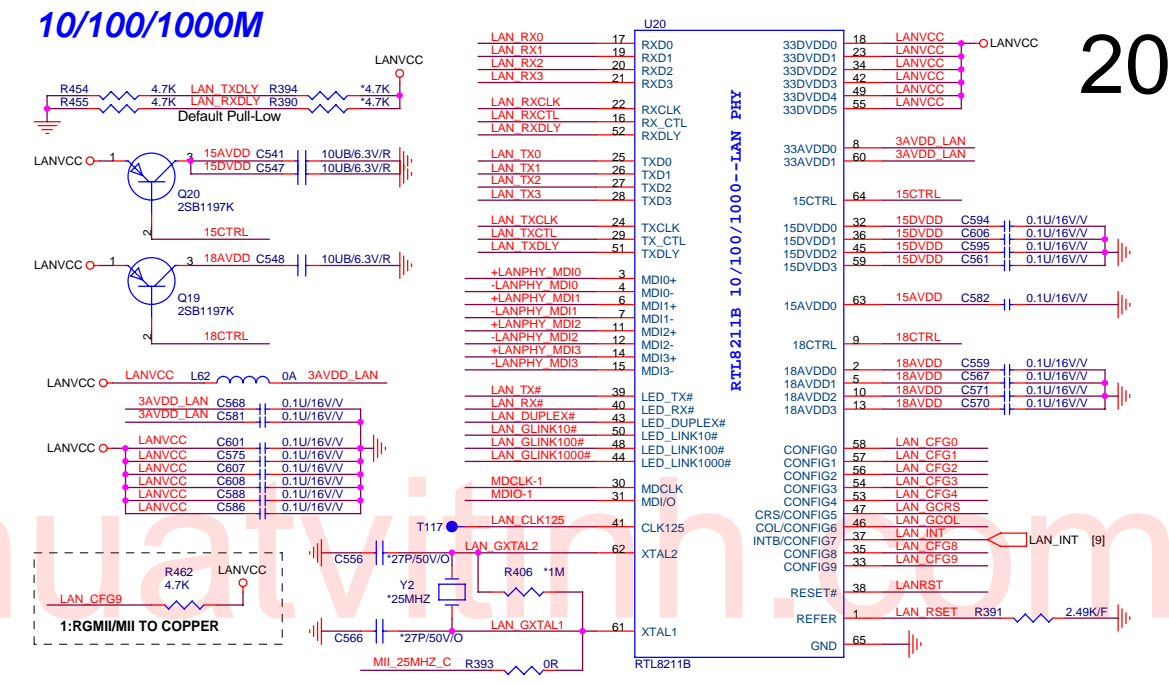
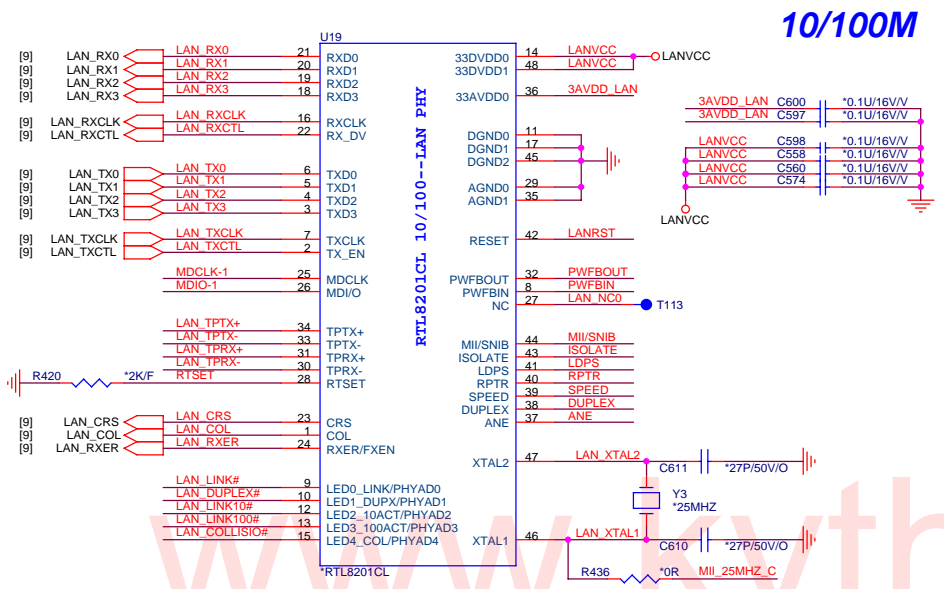


TV_OUT

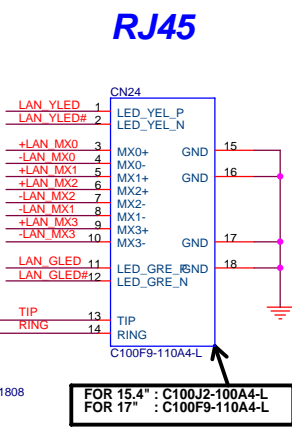
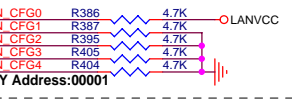
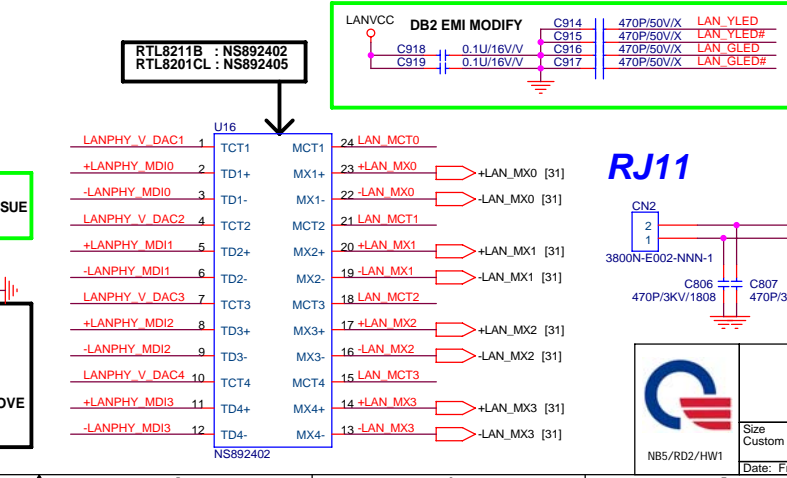
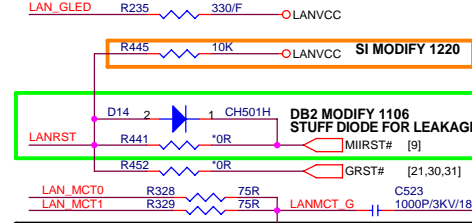
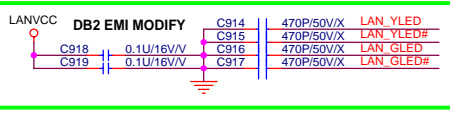
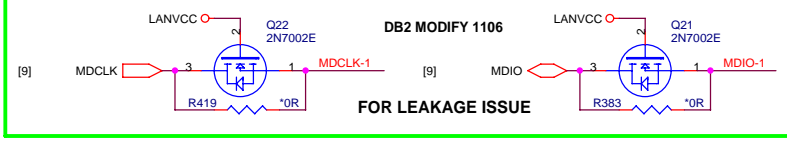
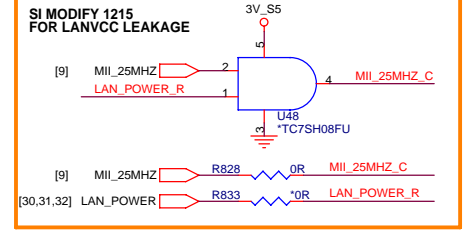
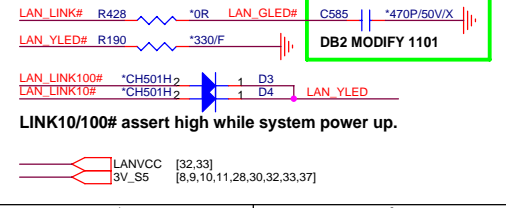
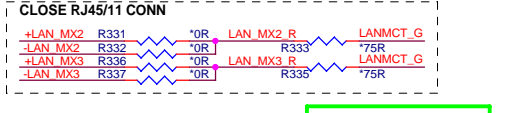
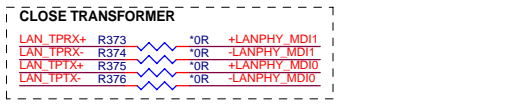


PROJECT : AT1
 Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev C2A
Date: Friday, December 29, 2006		Sheet 19 of 40



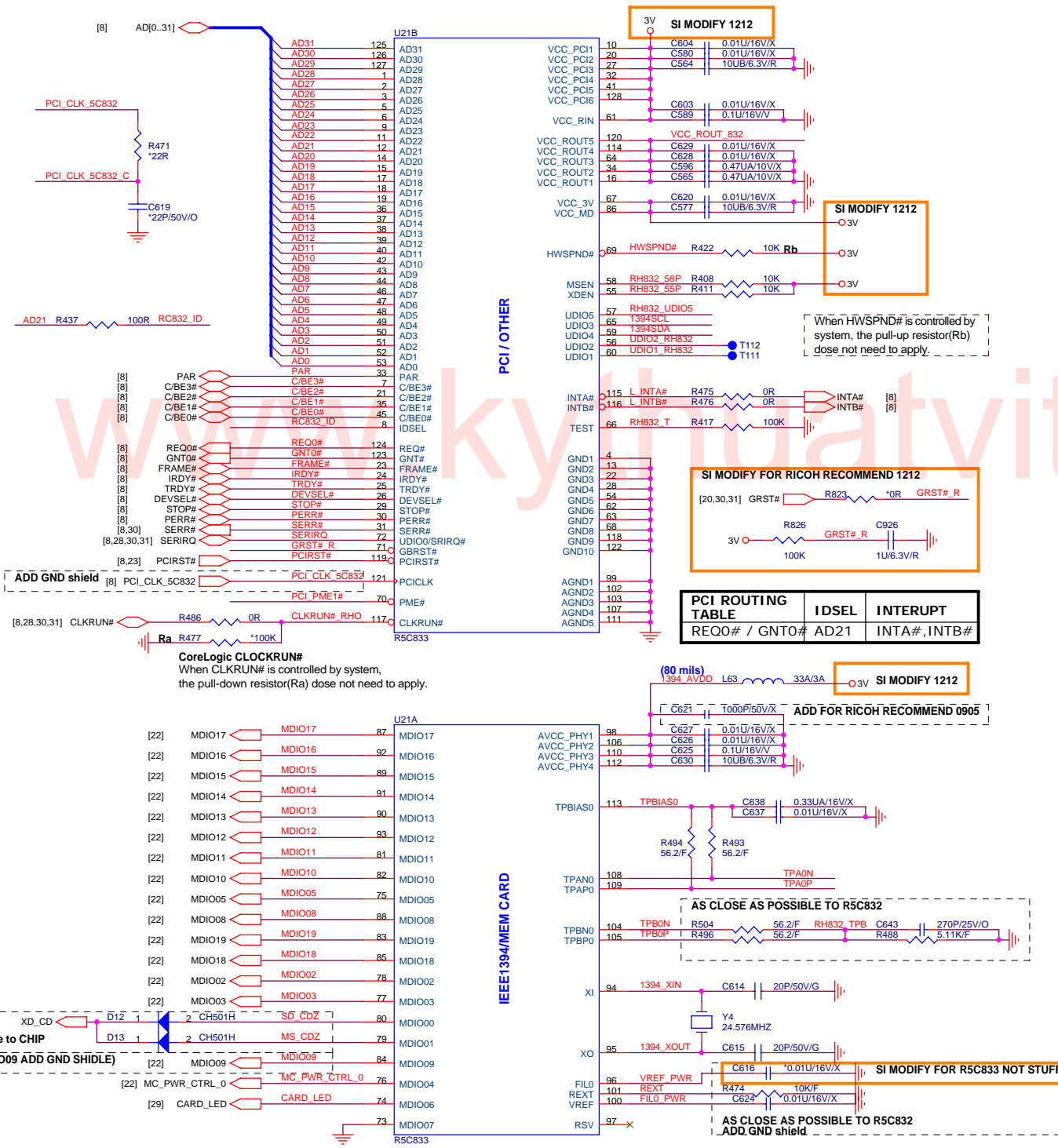
LAN_COL	1	Default	RTL8201B LED
LAN_RXER_R	1	Default	RTL8201CL LED
LAN_CRIS	0	Default	Fiber Mode
LAN_CRIS	0	Default	Ensure operating at normal mode



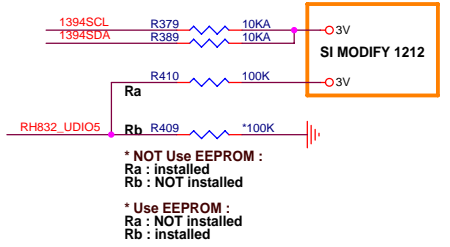
PROJECT : AT1
Quanta Computer Inc.

Size Custom Document Number RTL8211B,8201CL,RJ45,RJ11 Rev C2A

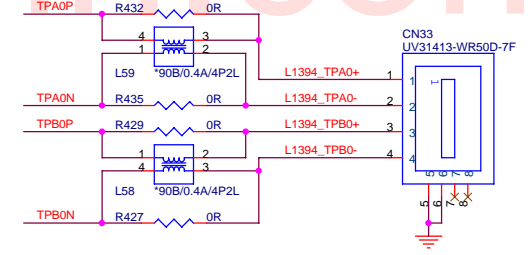
Date: Friday, December 29, 2006 Sheet 20 of 40



Serial EEPROM

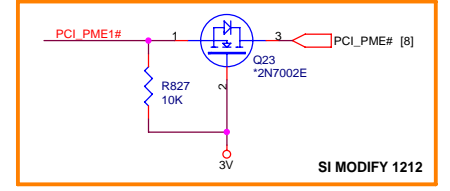


AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



- *TPA/TPA#, TPB/TPB# pair trace : As close as possible.
- *TPA/TPA#, TPB/TPB# pair trace : Same length electrically. And layout with shields.
- *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

- SD_CDZ [22]
- MS_CDZ [22]



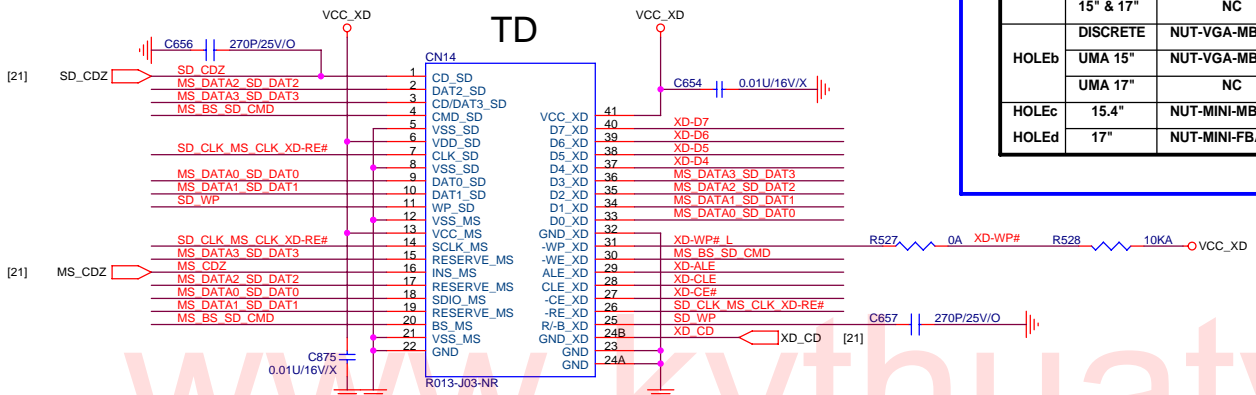
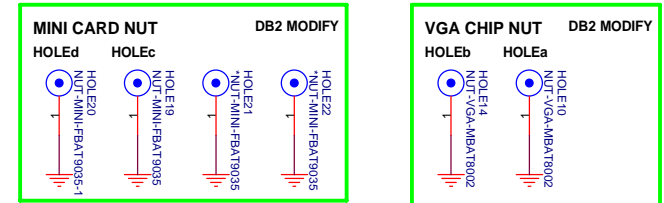
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number R5C832V00, 1394 PORT	Rev C2A
Date: Friday, December 29, 2006	Sheet 21	of 40

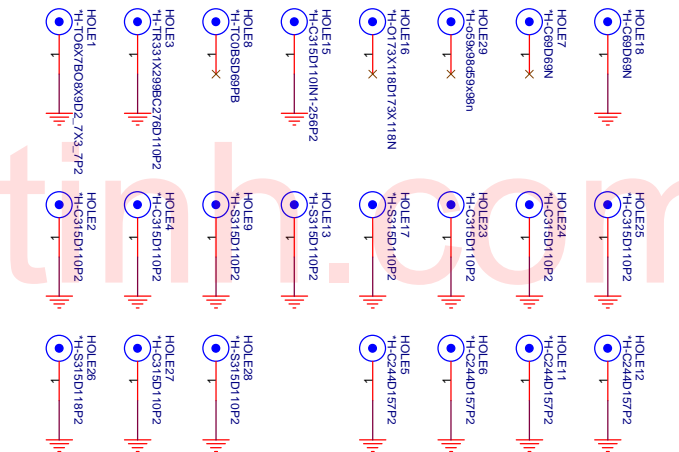
4 IN1 CARD READER XD,MMC/SD,MS/MP

15.4" & 17" AND DISCRETE & UMA		
HOLES	STATUS	NUT
HOLEa	DISCRETE	NUT-VGA-MBAT8002
	15" & 17"	NC
HOLEb	DISCRETE	NUT-VGA-MBAT8002
	UMA 15"	NUT-VGA-MBAT8002
	UMA 17"	NC
HOLEc	15.4"	NUT-MINI-MBAT8004
HOLEd	17"	NUT-MINI-FBAT9035

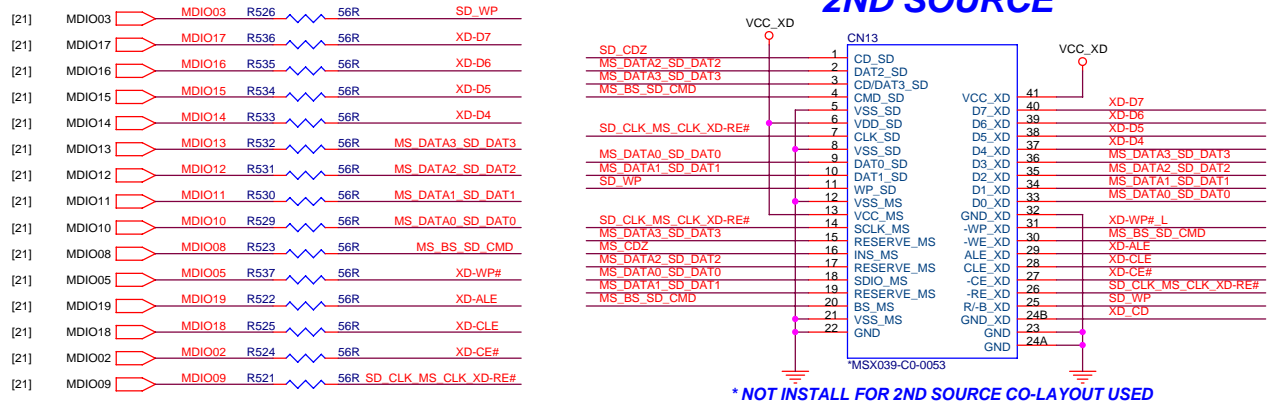
SCREW HOLE



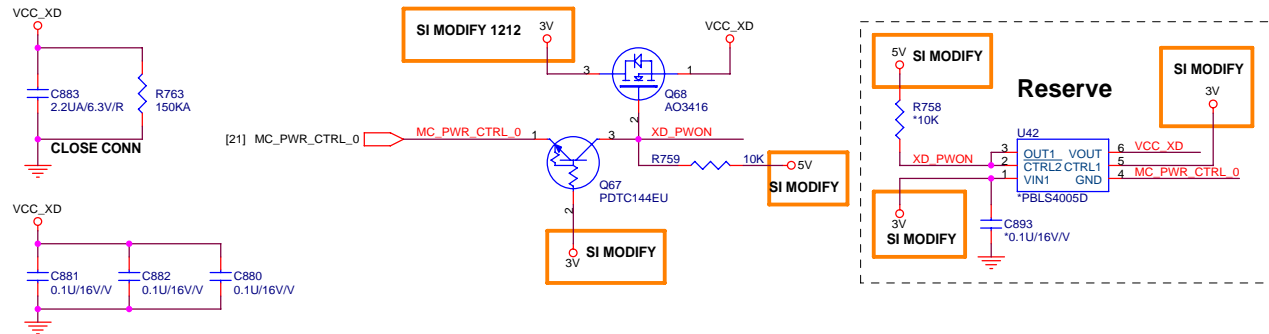
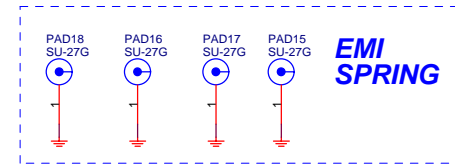
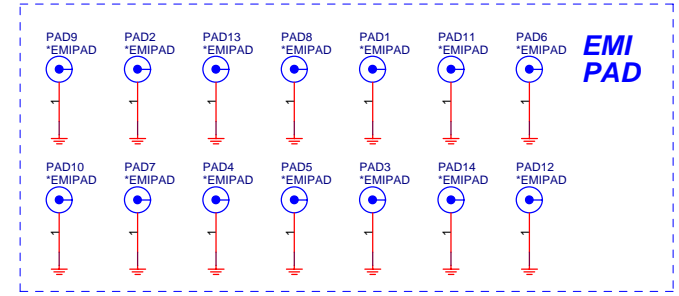
Note: Need to add WP# and CD# pad for Proconn



2ND SOURCE



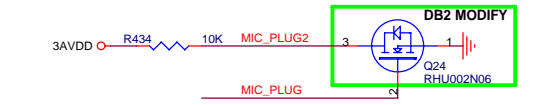
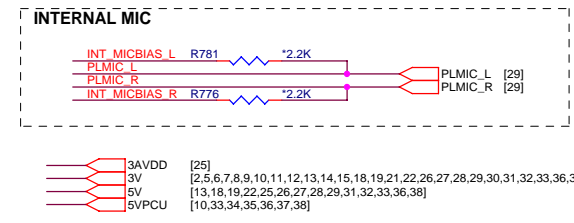
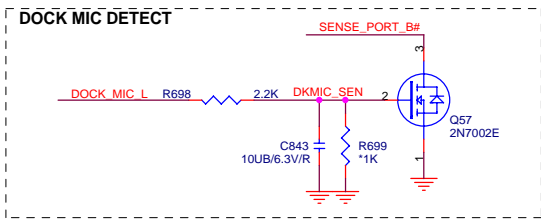
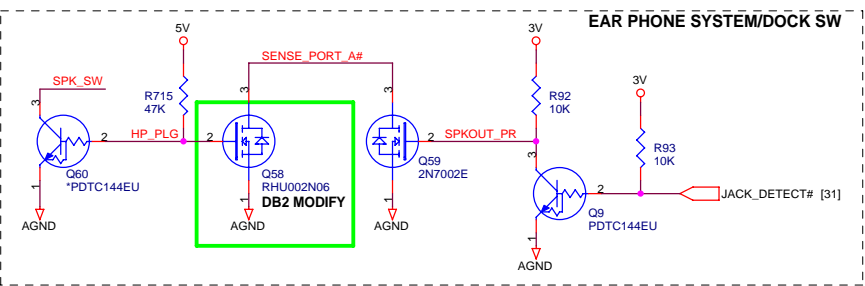
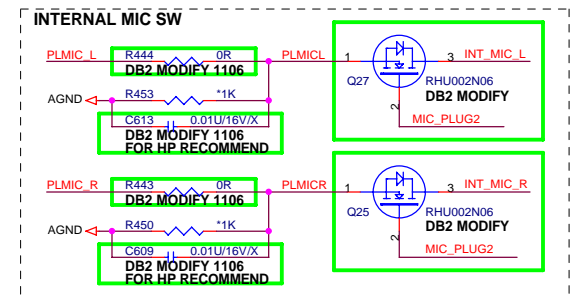
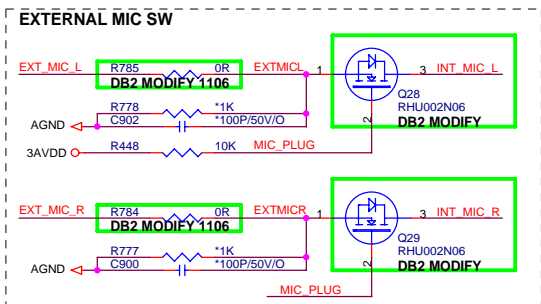
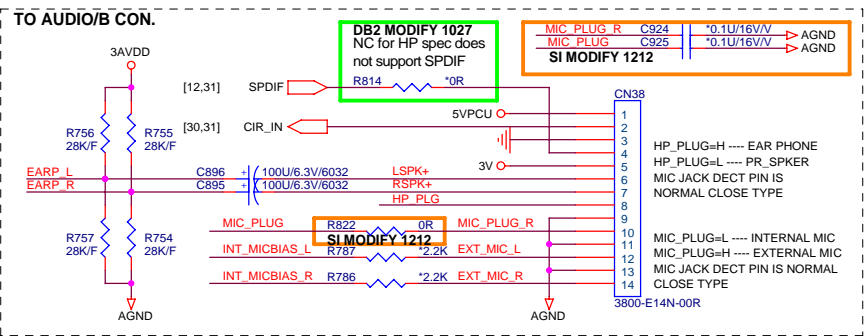
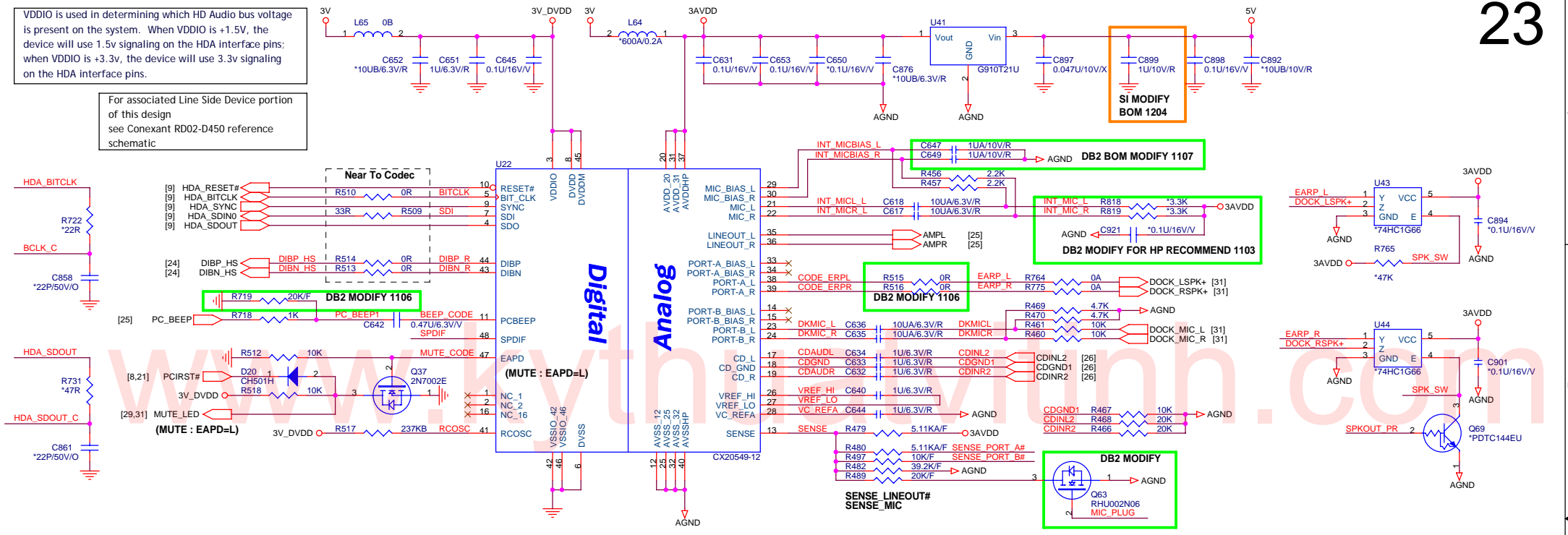
* NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED



[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,23,26,27,28,29,30,31,32,33,36,38]
[13,18,19,23,25,26,27,28,29,31,32,33,36,38]

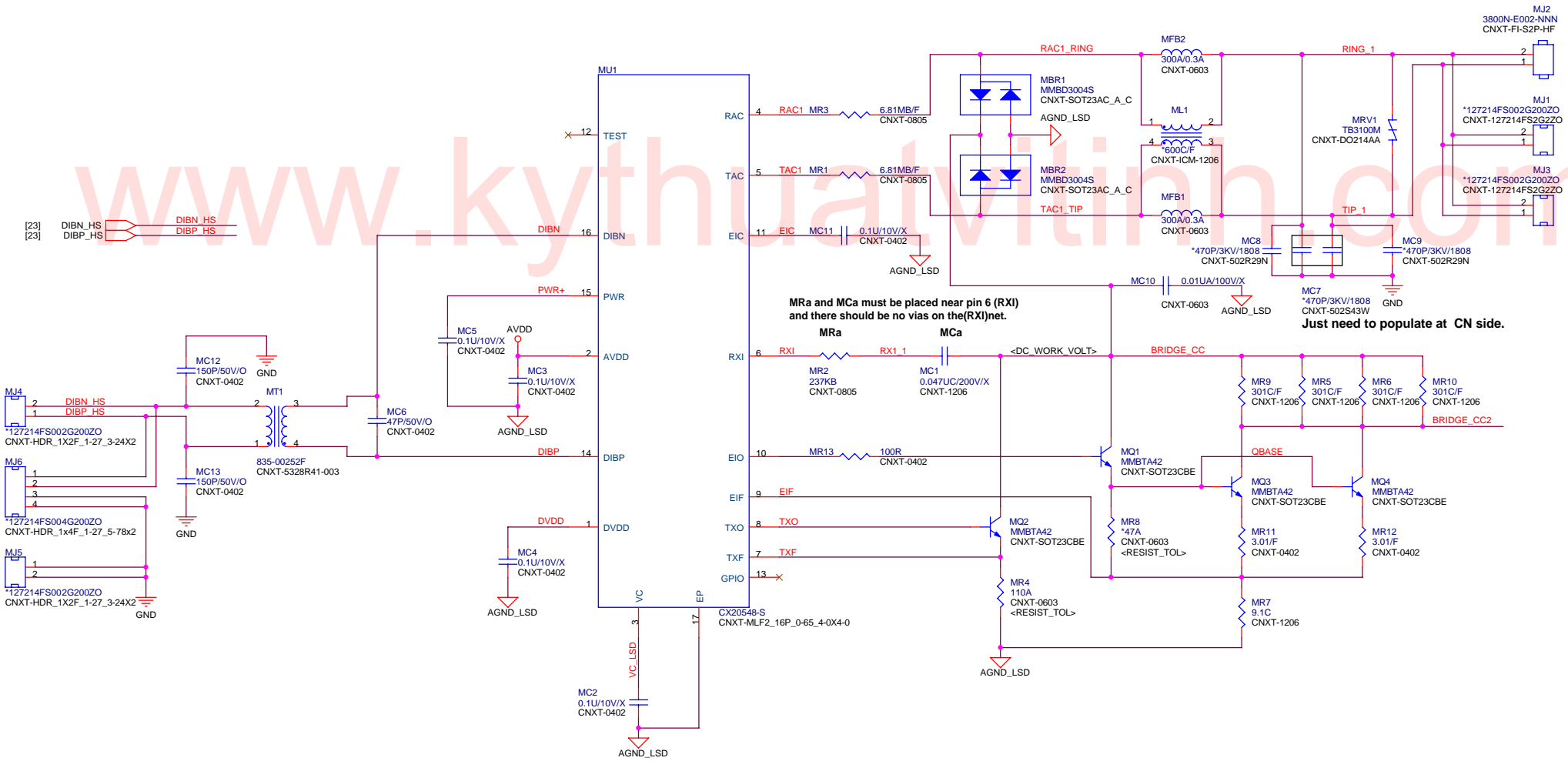
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.


For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

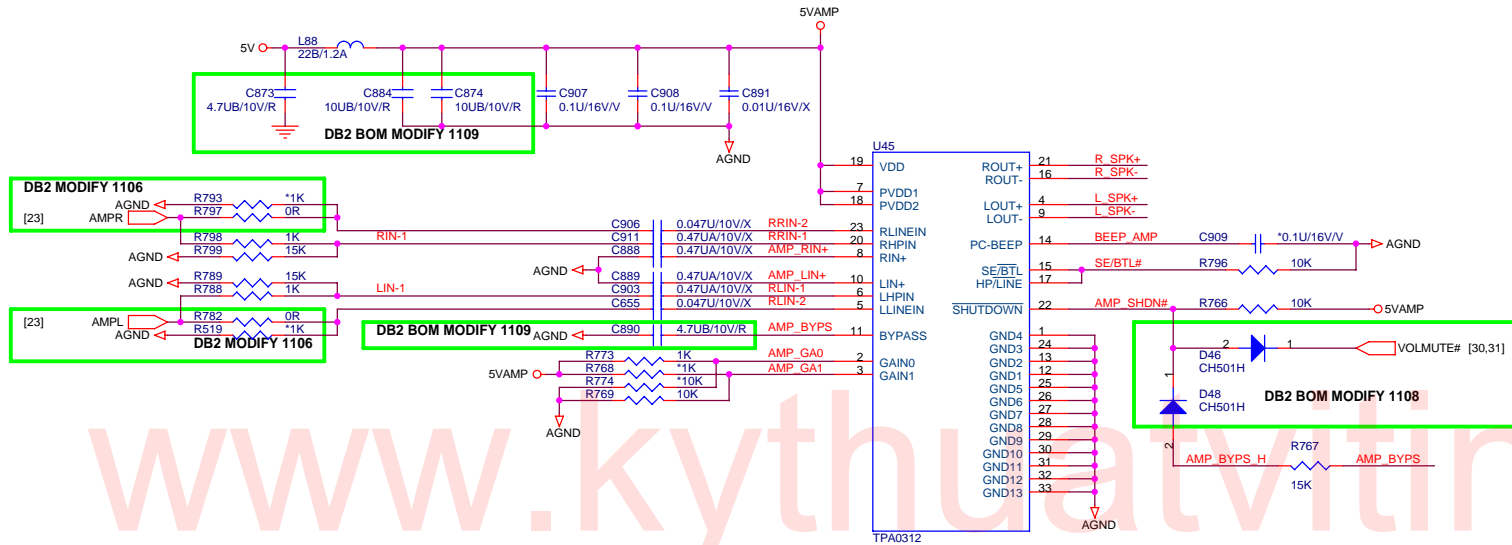


	PROJECT : AT1 Quanta Computer Inc.	
	Size Custom Document Number HDA_CX20549-12_AUDIO_BOARD Date: Friday, December 29, 2006	Rev C2A Sheet 23 of 40

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



 NBS/RD2/HW1	PROJECT : AT1 Quanta Computer Inc.	
	Size Custom Date: Friday, December 29, 2006	Document Number MODEM(DAA)_CX20548-S

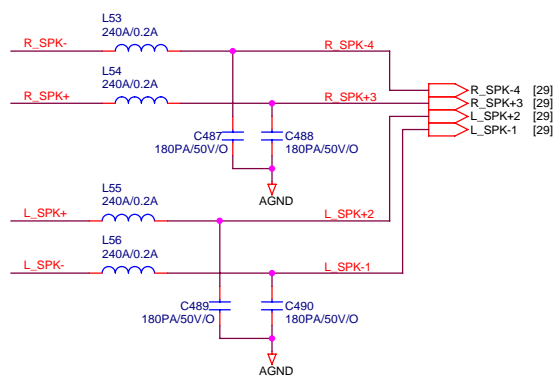


0312 Gain Table

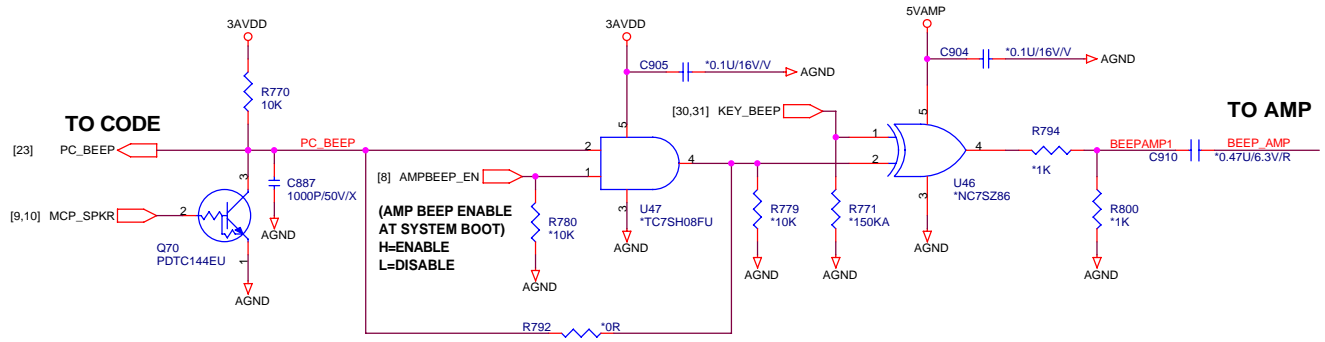
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

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INT. SPEAKER



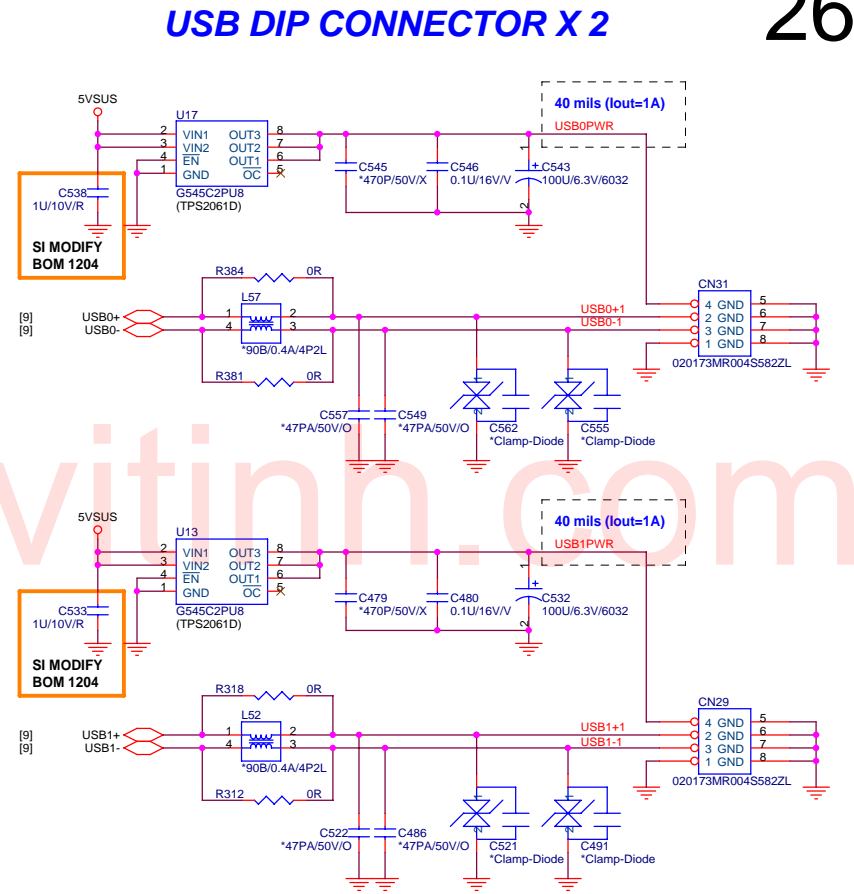
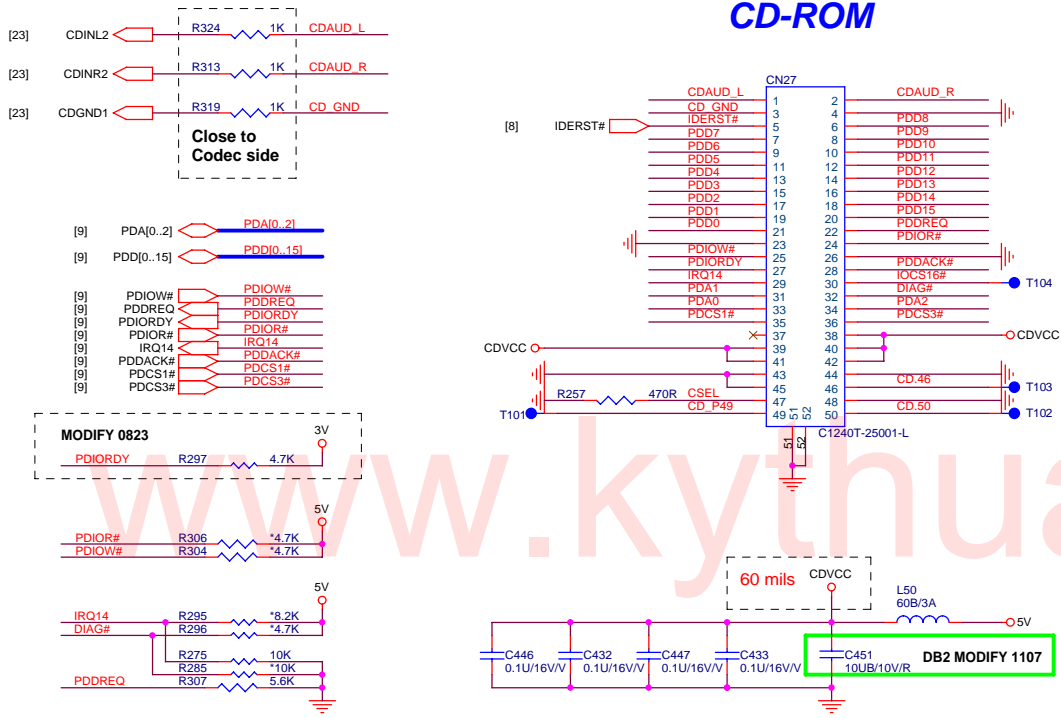
PCSPK BEEP



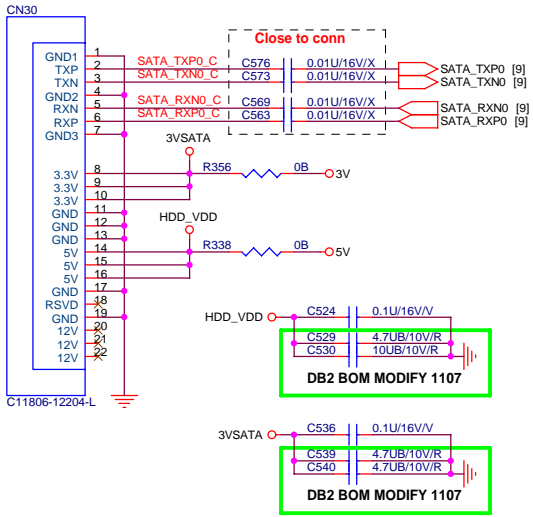
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA0312	Rev C2A
Date: Friday, December 29, 2006		Sheet 25 of 40

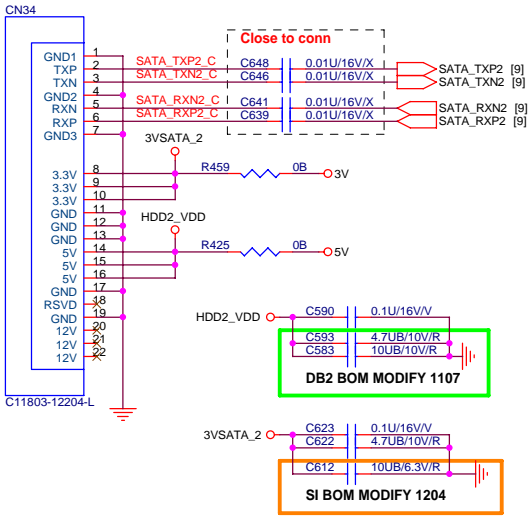
3AVDD [23] (13,18,19,22,23,26,27,28,29,31,32,33,36,38)
5V



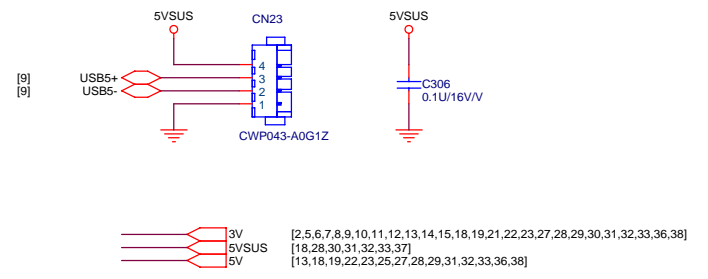
SATA_1 CONNECTOR



For 17" W Second HDD SATA_2 CONNECTOR

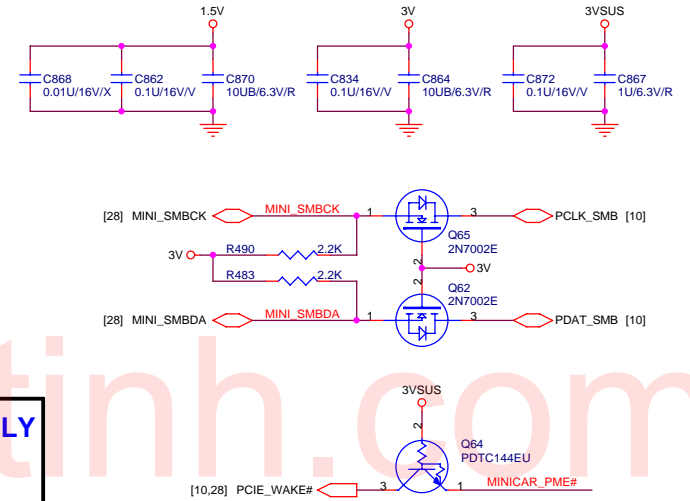
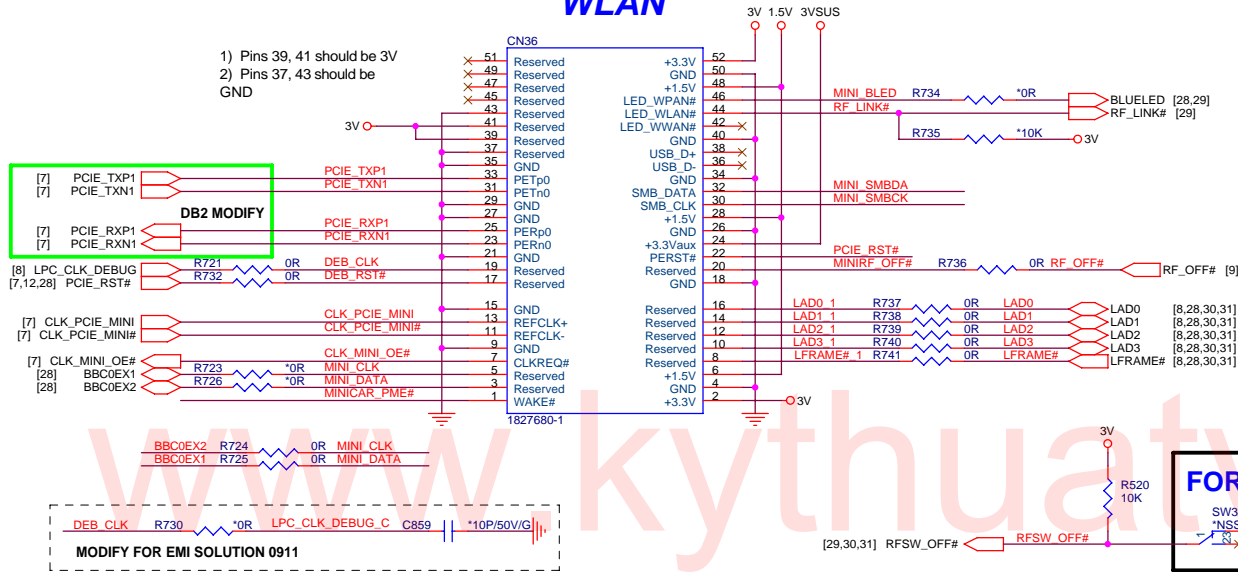


USB WIRE TO DC BOARD X 1

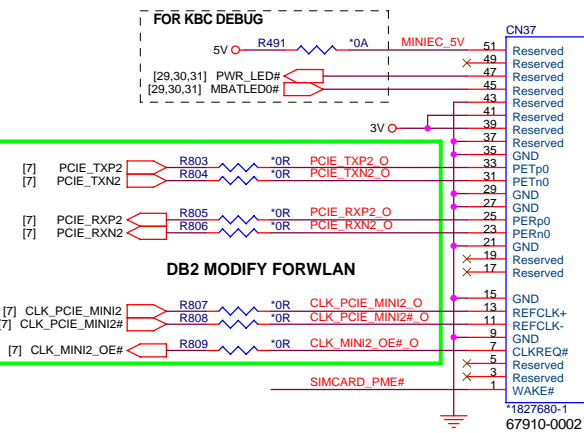
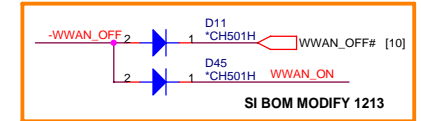
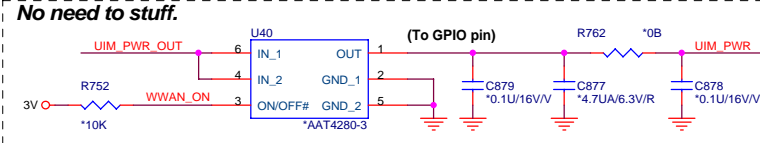
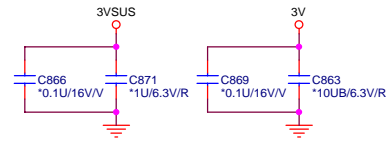


	PROJECT : AT1	
	Quanta Computer Inc.	
	Size Custom	Document Number SATA HDDx2,CD-ROM,USBx3
Date: Friday, December 29, 2006		Sheet 26 of 40

Mini PCI-E Card 1 WLAN



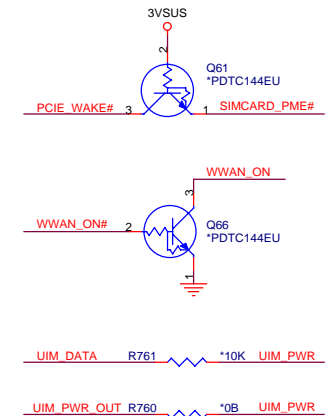
Mini PCI-E Card 2 (WWAN/SIM) FOR 15.4" ONLY (RESERVE)



FOR 17" SW BOARD



SI MODIFY 1213 FOR WLAN

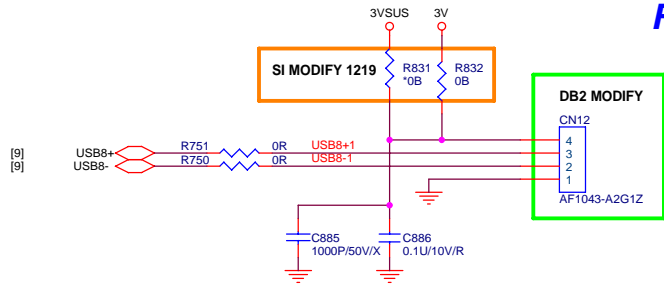


1.5V	[28,31,32,36]
3V	[2,3,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,28,29,30,31,32,33,36,38]
3VSUS	[28,29,32,33]
5V	[13,18,19,22,23,25,26,28,29,31,32,33,36,38]

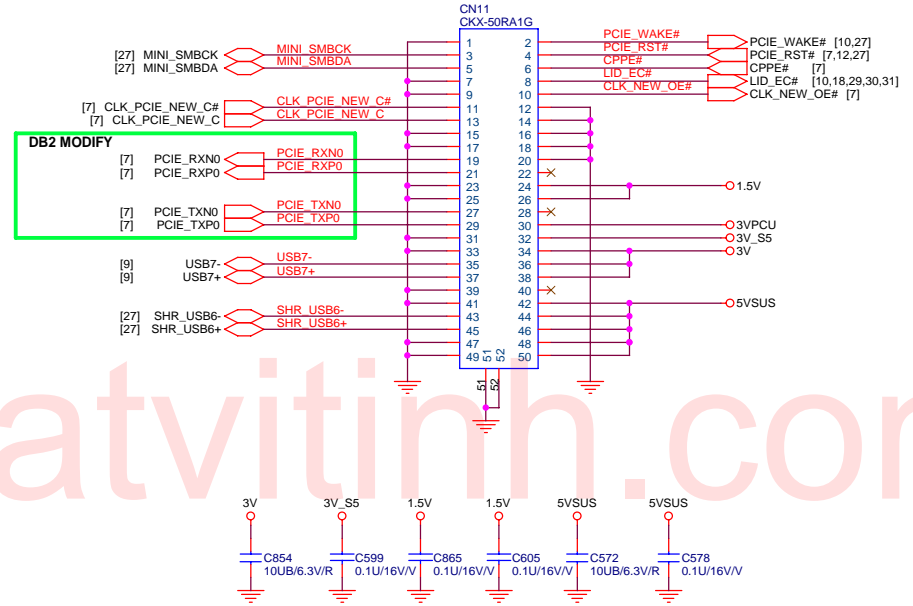
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MINI CARDx2 (WLAN,WWAN,SIM)	Rev C2A
Date: Friday, December 29, 2006	Sheet 27	of 40

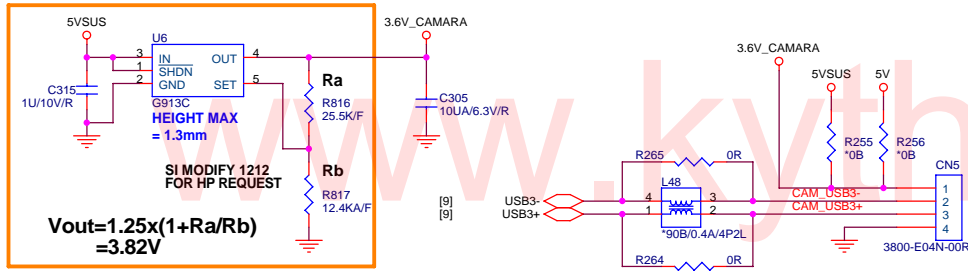
FINGER PRINT



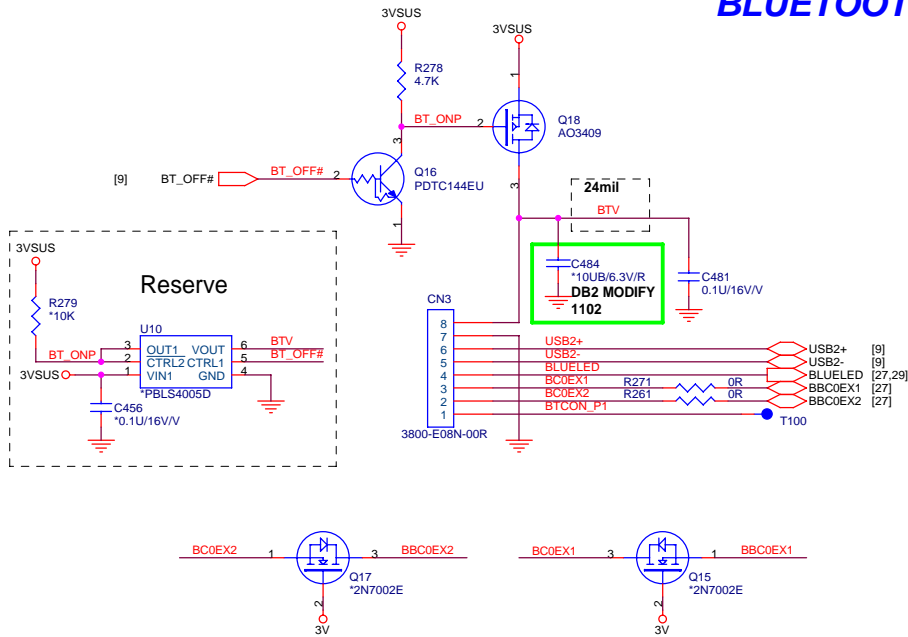
NEW CARD



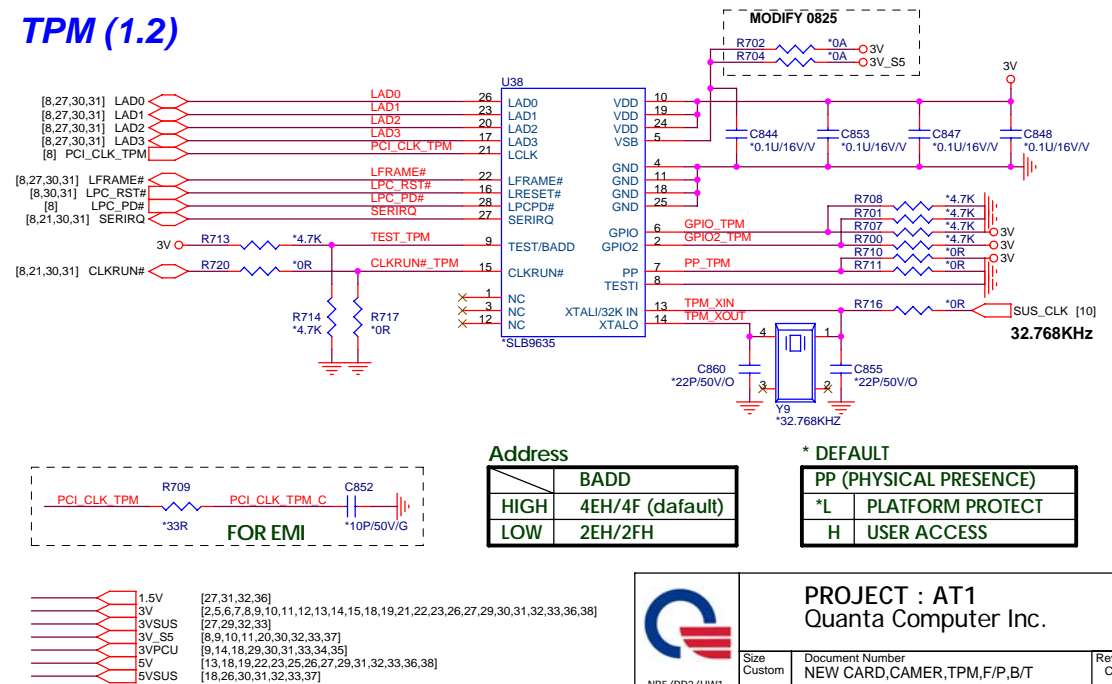
CAMERA



BLUETOOTH



TPM (1.2)



Address

	BADD
HIGH	4EH/4F (default)
LOW	2EH/2FH

* DEFAULT

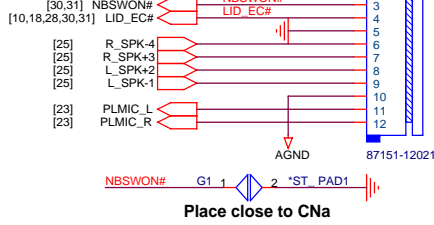
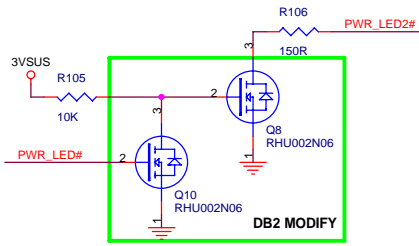
PP (PHYSICAL PRESENCE)	
*L	PLATFORM PROTECT
H	USER ACCESS



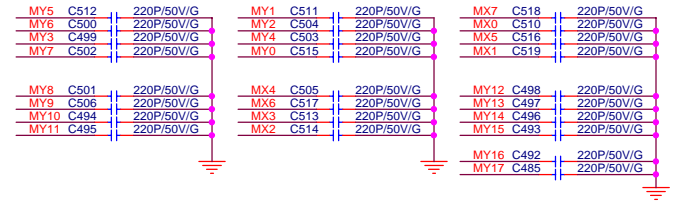
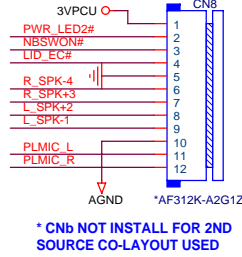
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number NEW_CARD,CAMER,TPM,F/P,B/T	Rev C2A
Date: Friday, December 29, 2006	Sheet 28	of 40

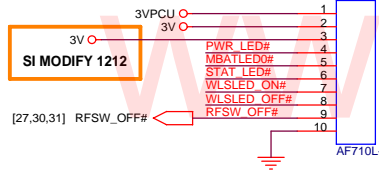
FOR POWER ON AND INTERNAL SPK / MIC SW BOARD



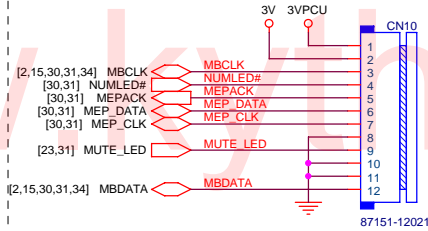
2ND SOURCE



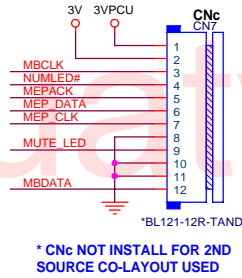
FOR 17" LED AND WIRLESS SW BOARD



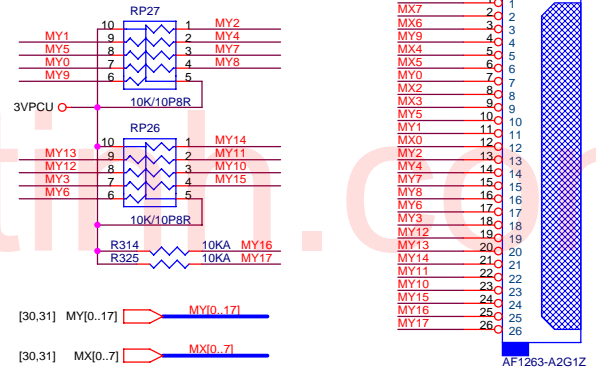
FOR QLB SW BOARD



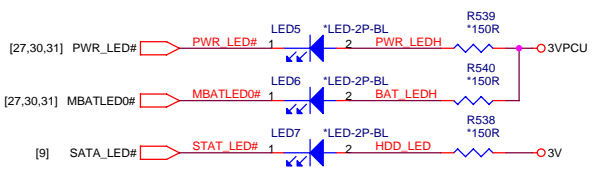
2ND SOURCE



KEYBOARD PULL-UP



STUFF FOR 15.4" LED USED

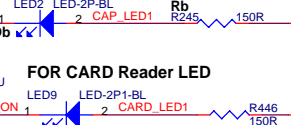
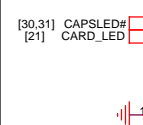


FOR 15.4" LCD : STUFF LEDa, Ra

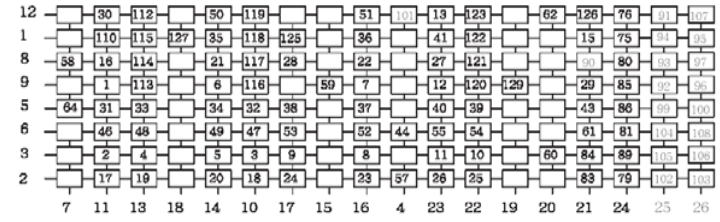
STUFF FOR 15.4" CAPS LOCK LED

FOR 17" LCD : STUFF LEDb, Rb

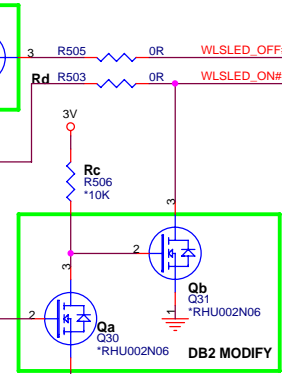
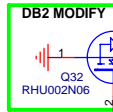
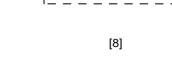
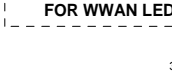
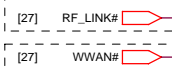
STUFF FOR 17" CAPS LOCK LED



FOR CARD Reader LED



FOR WLAN LED



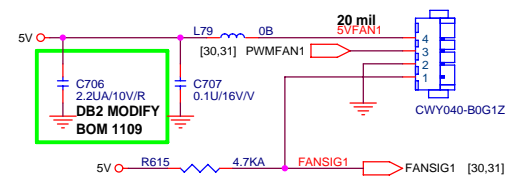
STUFF FOR 15.4" LED



FOR LED DRIVING ISSUE

STUFF	Rc, Qa, Qb, LEDc
NC	Rd

FAN CONNECTOR

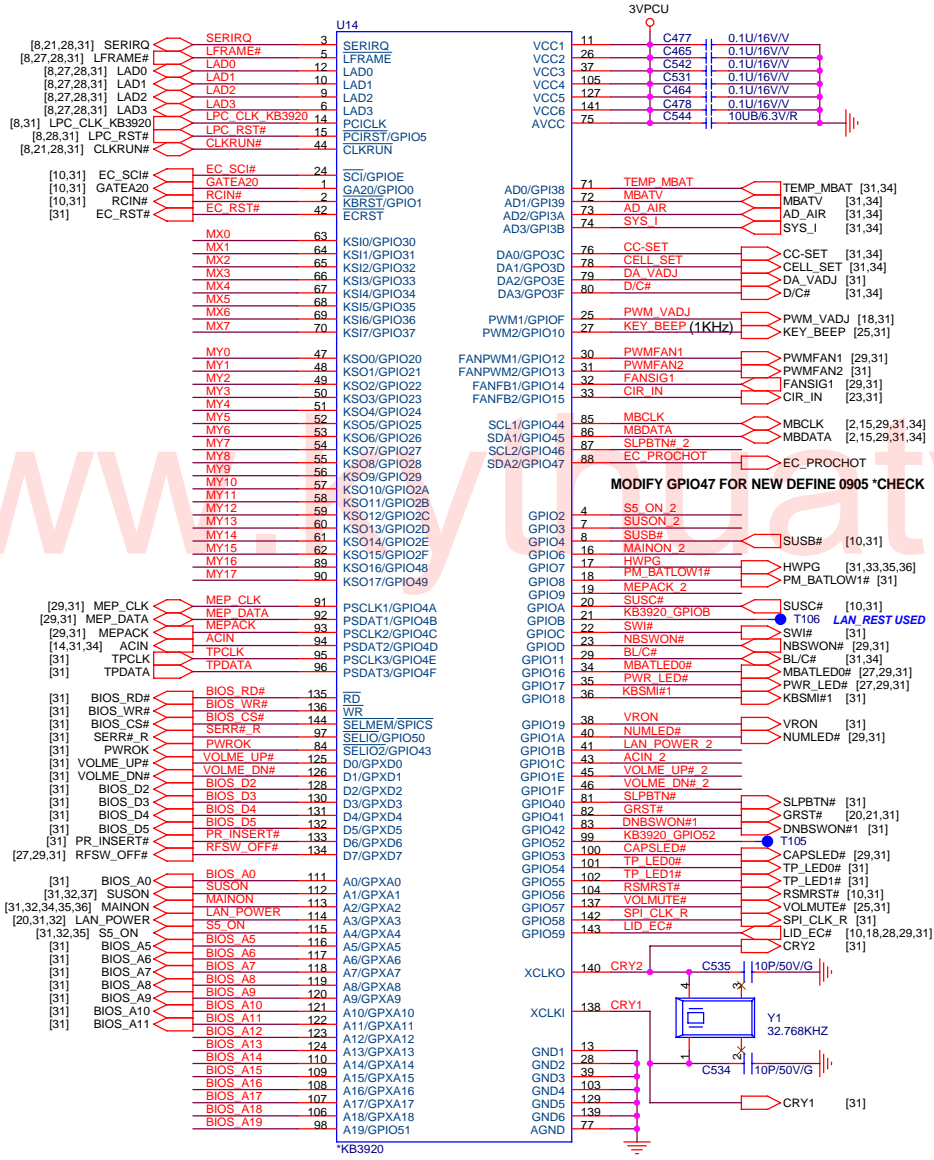


PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number KB,FAN,LED,SW (PWR,QLB,LED)	Rev C2A
Date: Friday, December 29, 2006	Sheet 29	of 40

- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,30,31,32,33,36,38]
- 3VSUS [27,28,32,33]
- 3VPCU [9,14,18,28,30,31,33,34,35]
- 5V [13,18,19,22,23,25,26,27,28,31,32,33,36,38]

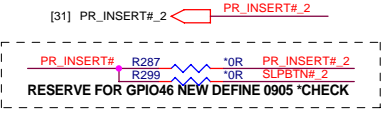
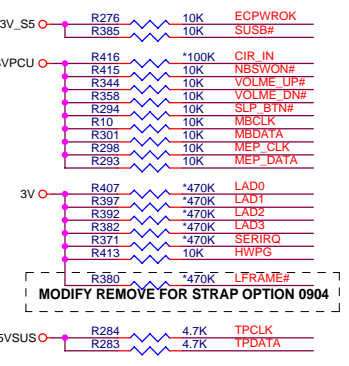
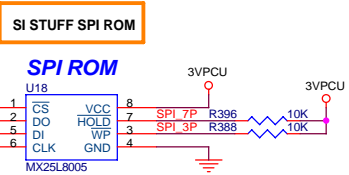
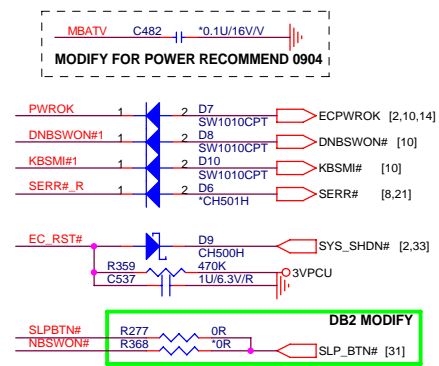
EC - KB3920



STRAP PIN (*INTERNAL PULL-UP)

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal training	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode

DB2 MODIFY



- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,31,32,33,36,37]
- 3V_S5 [8,9,10,11,20,28,32,33,37]
- 3VPCU [9,14,18,28,29,31,33,34,35]
- 5VSUS [18,26,28,31,32,33,37]

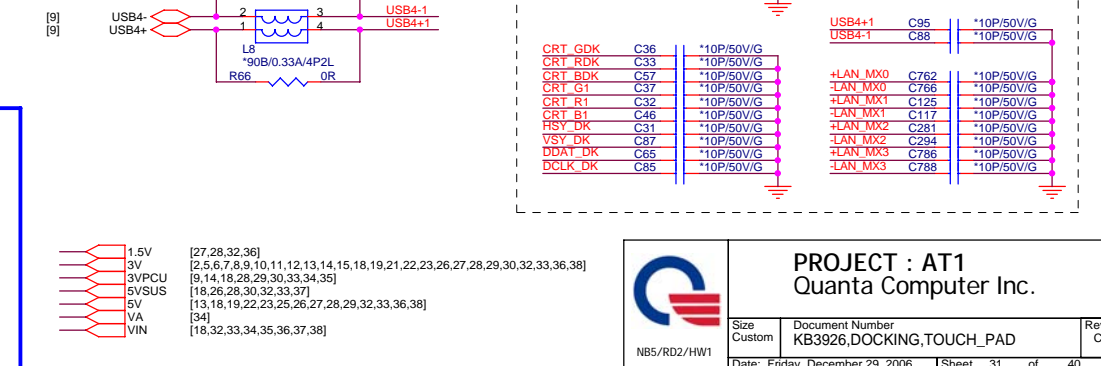
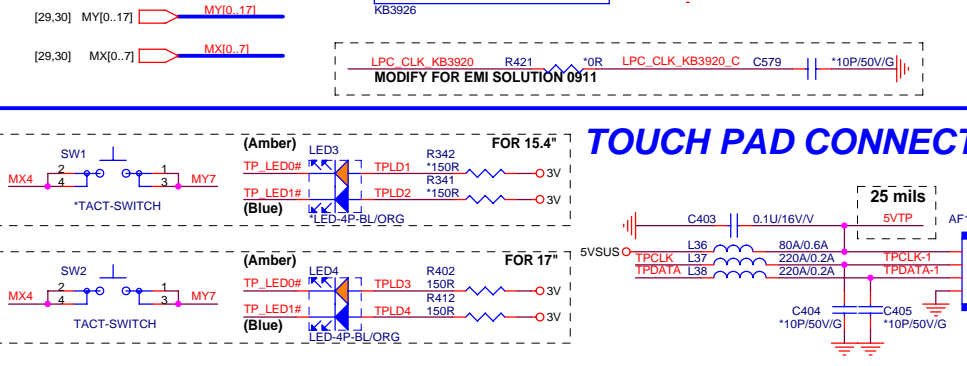
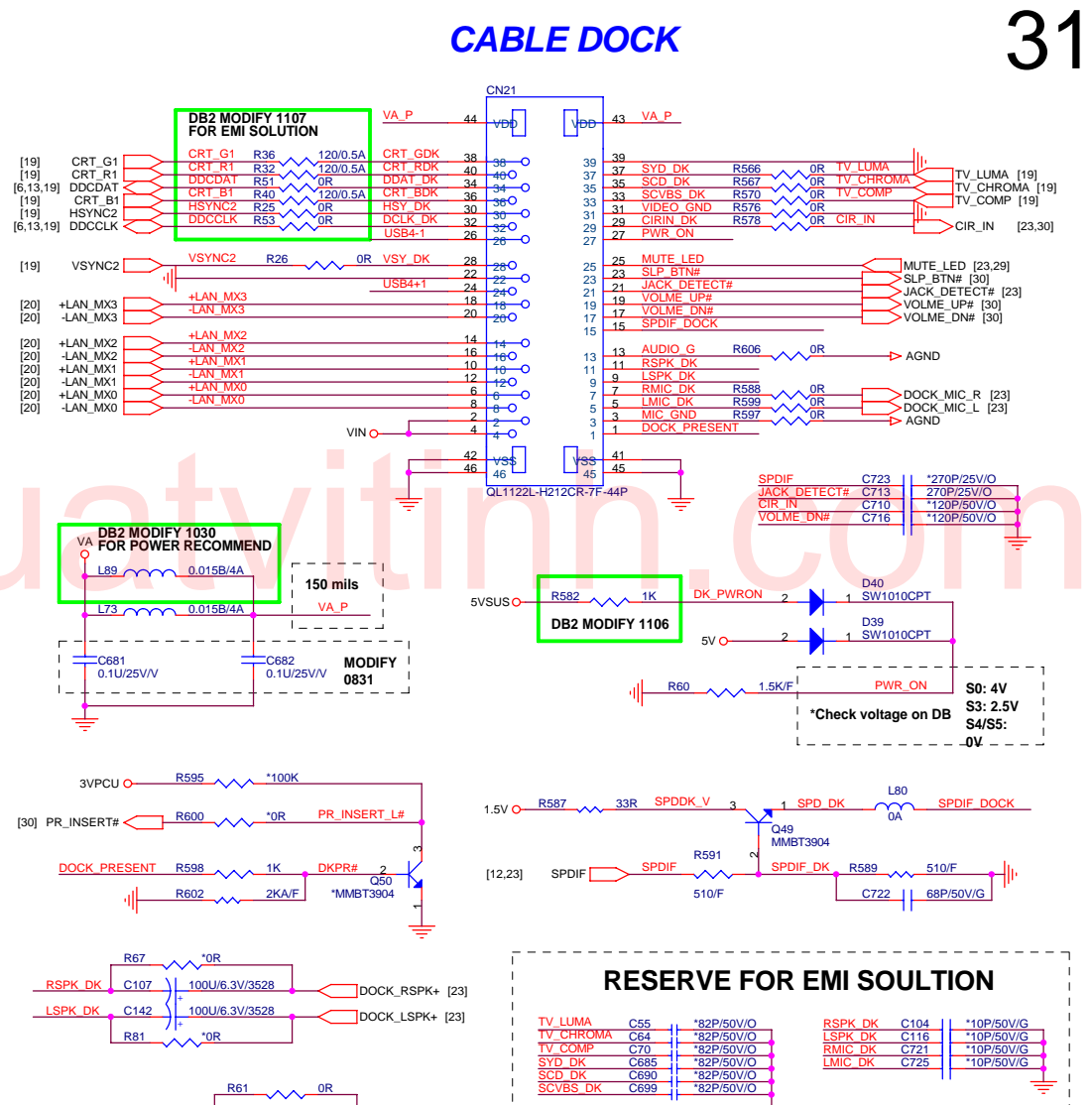
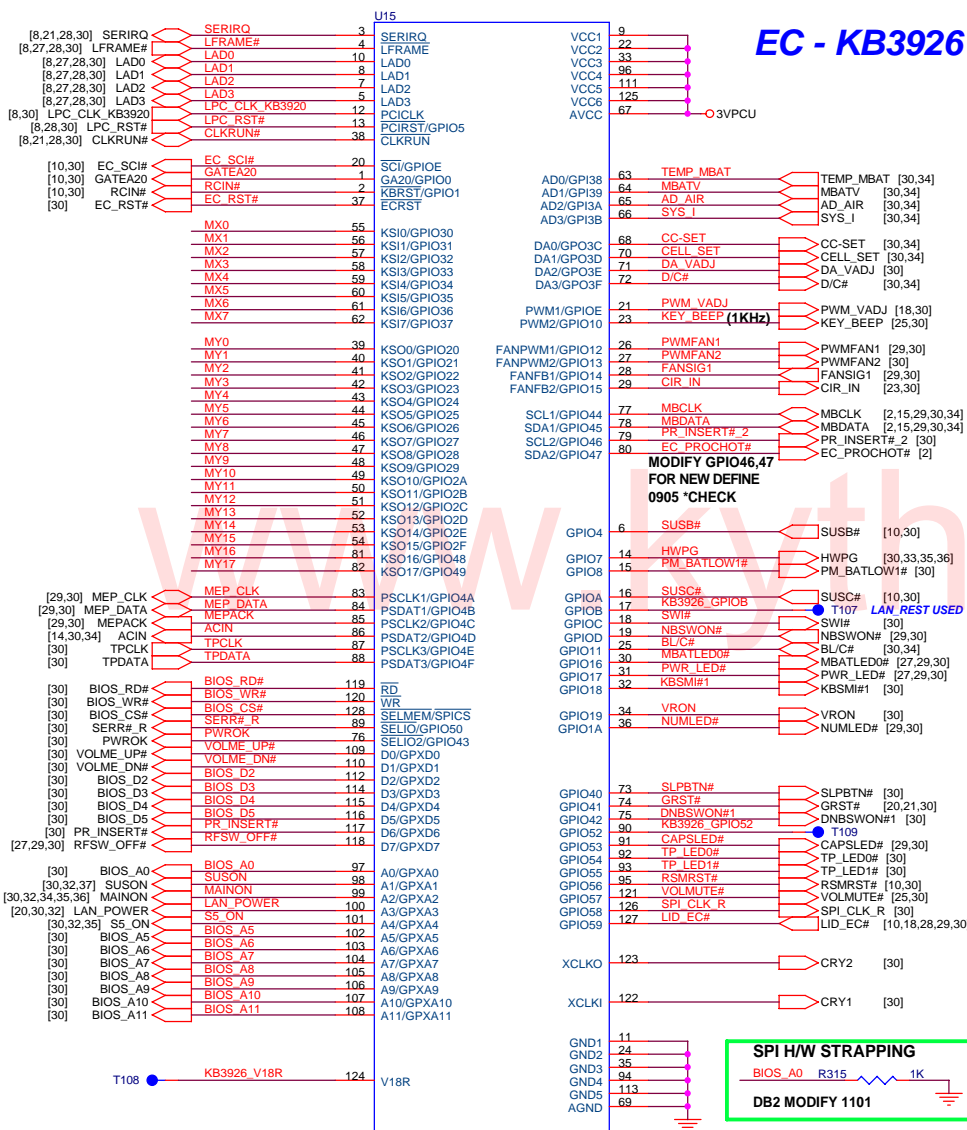
PROJECT : AT1
Quanta Computer Inc.

Size Custom Document Number KB3920_SPI_ROM Rev C2A

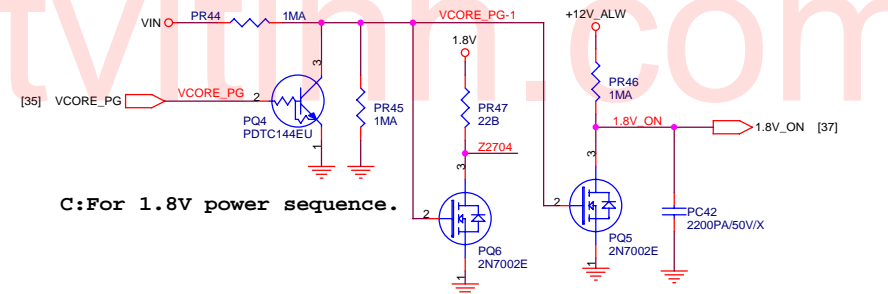
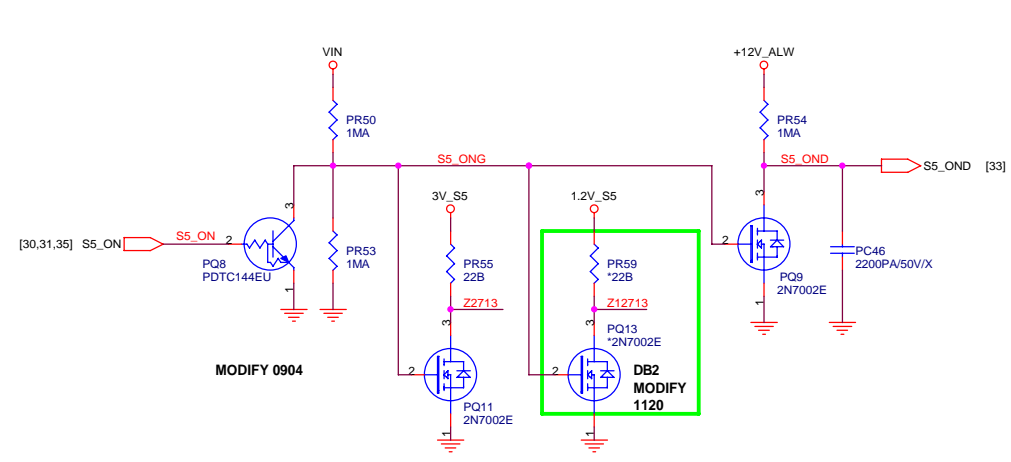
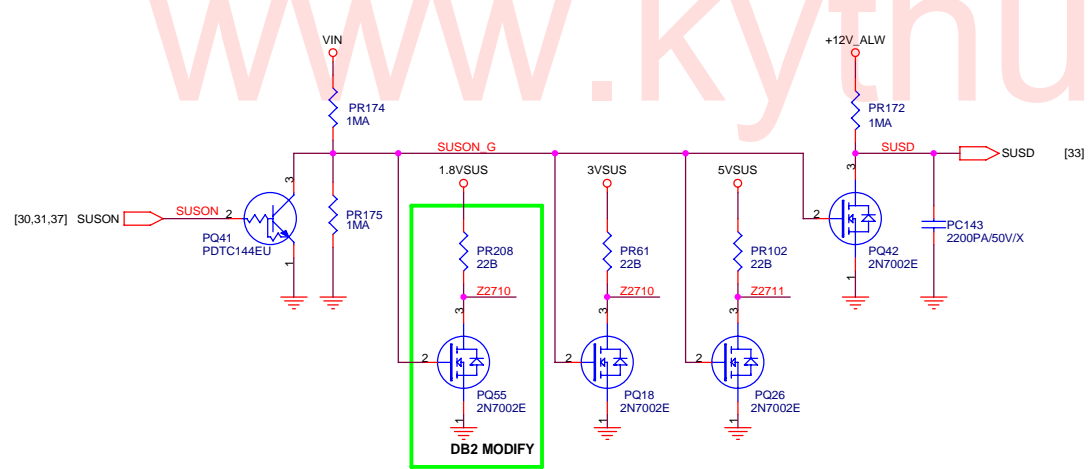
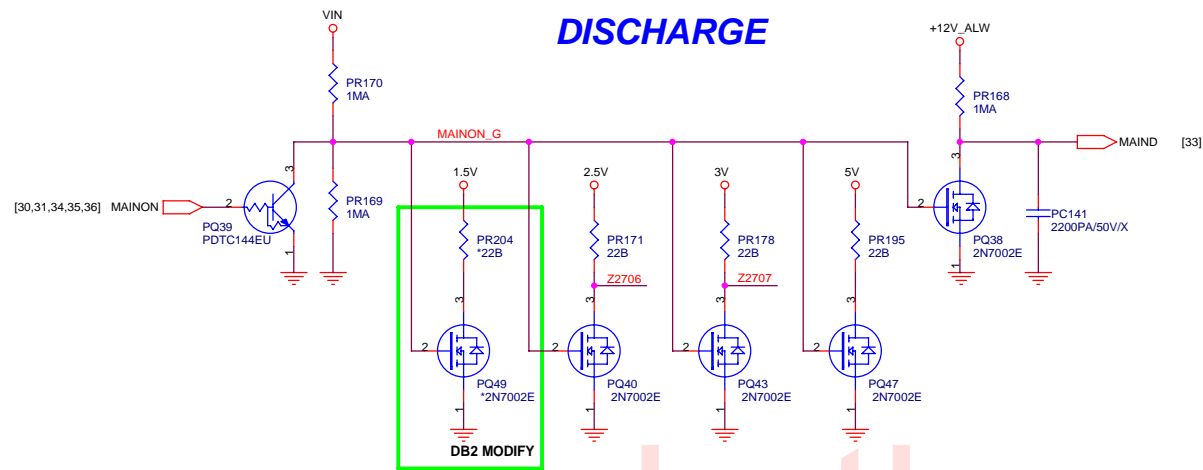
Date: Friday, December 29, 2006 Sheet 30 of 40

EC - KB3926

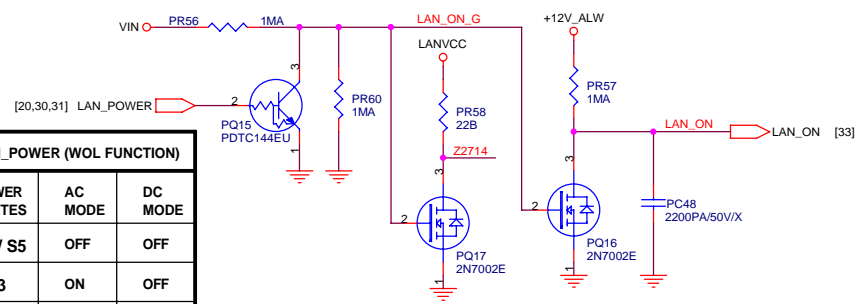
CABLE DOCK



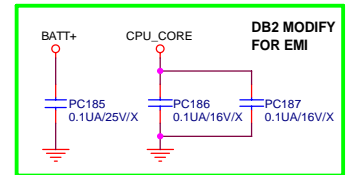
DISCHARGE



C:For 1.8V power sequence.



LAN_POWER (WOL FUNCTION)		
POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON



- CPU_CORE [4,38]
- 1.2V_S5 [10,11,35]
- 1.5V [27,28,31,36]
- 1.8V [11,13,15,16,17,37]
- 1.8VSUS [2,3,4,5,6,36,37]
- 2.5V [2,13,36]
- LANVCC [20,33]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
- 3VSUS [27,28,29,33]
- 3V_S5 [8,9,10,11,20,28,30,33,37]
- 5V [13,18,19,22,23,25,26,27,28,29,31,33,36,38]
- 5VSUS [18,26,29,30,31,33,37]
- +12V_ALW [10,18,33]
- VIN [18,31,33,34,35,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number DISCHARGE	Rev C2A
Date: Friday, December 29, 2006		
Sheet 32 of 40		

DC/DC 3VPCU/ 5VPCU/ +12V_ALW

TOPN: OUT1/OUT2
 GND=400KHz/500KHz
 REF = 400KHz/300KHz
 VCC5=200KHz/300KHz

5 Volt +/- 5%
5VPCU
C/C:8A
P/C:10A

Place these CAPS close to FETs

Place these CAPS close to FETs

3.3 Volt +/- 5%
3VPCU
C/C:8A
P/C:10A

Vout=0.7*(Ra+Rb)/Rb
Rb around 49.9k

I_lim*MOSFET (RDSON) = V_ILIM (mV) / 10
V_ILIM (mV) = 5uA * R_ILIM

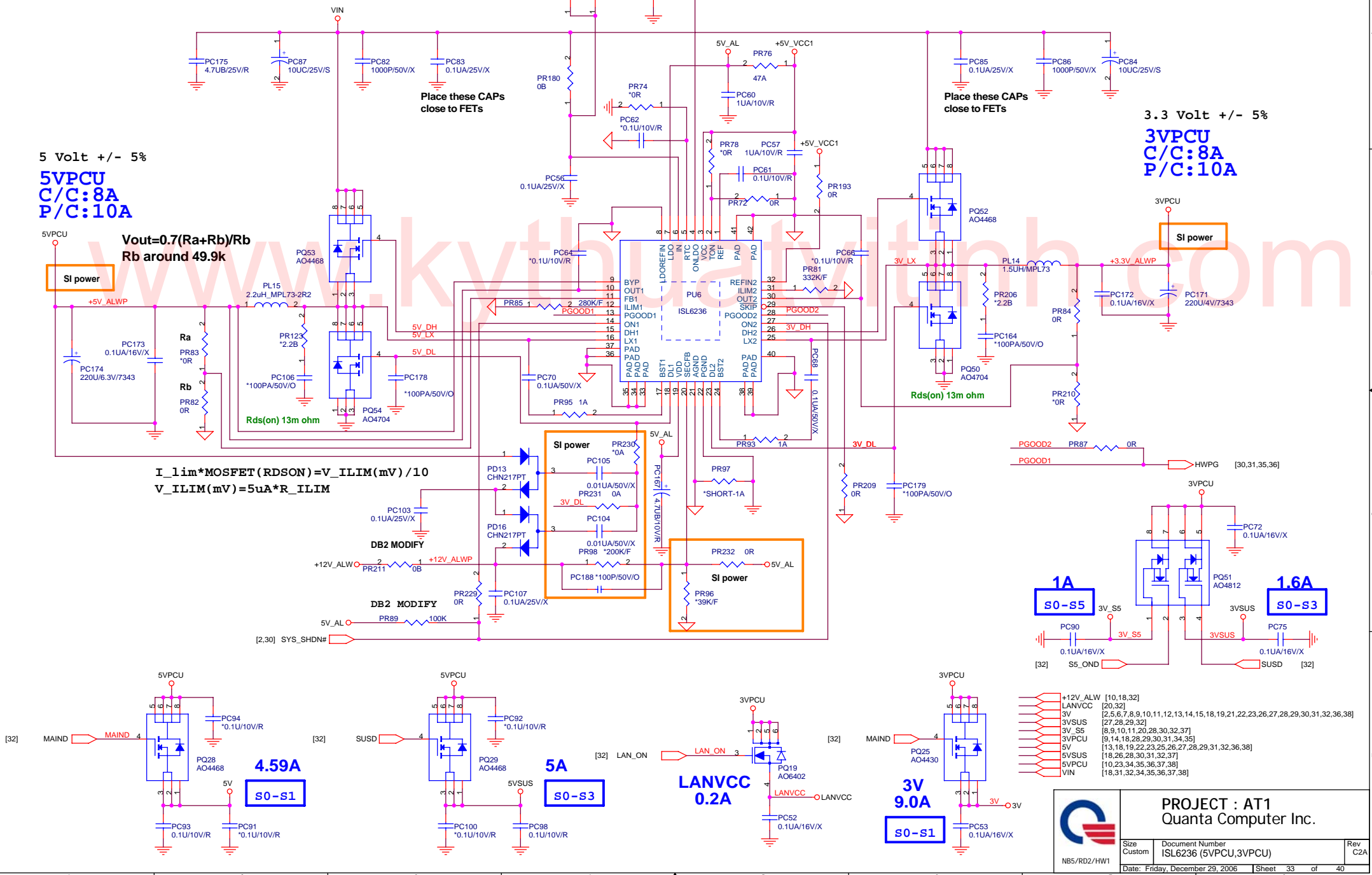
DB2 MODIFY

DB2 MODIFY

+12V_ALW	[10,18,32]
LANVCC	[20,32]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS	[27,28,29,32]
3V_S5	[8,9,10,11,20,28,30,32,37]
3VPCU	[9,14,18,28,29,30,31,34,35]
3V	[13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS	[18,26,28,30,31,32,37]
5VPCU	[10,23,34,35,36,37,38]
VIN	[18,31,32,34,35,36,37,38]

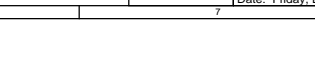
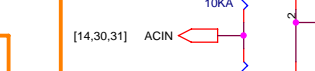
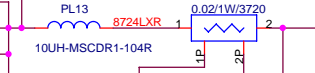
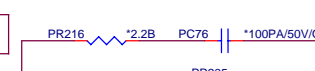
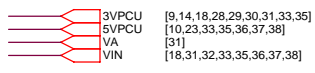
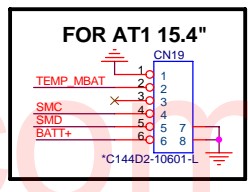
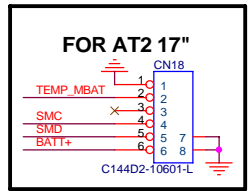
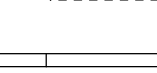
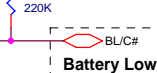
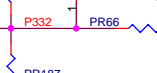
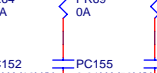
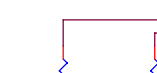
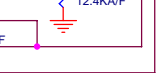
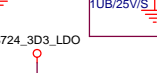
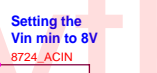
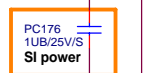
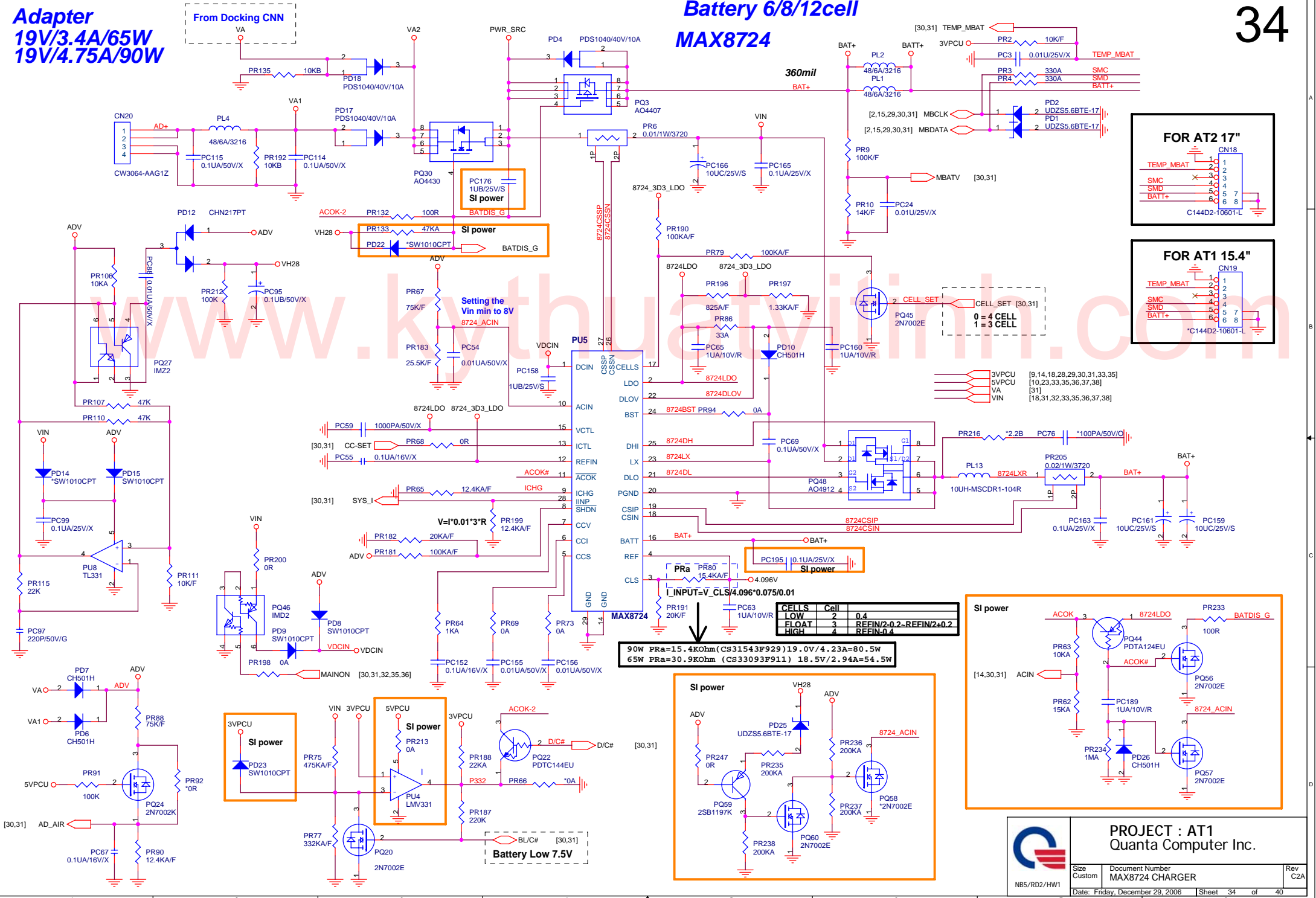
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6236 (5VPCU,3VPCU)	C2A
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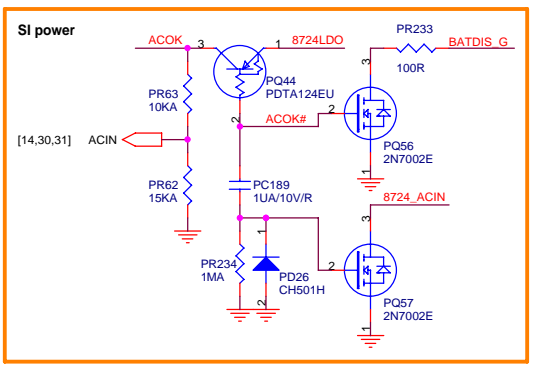
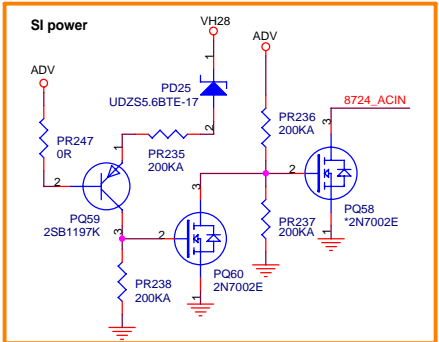
Adapter
19V/3.4A/65W
19V/4.75A/90W

Battery 6/8/12cell
MAX8724



CELLS	Cell
LOW	2
FLOAT	3
HIGH	4

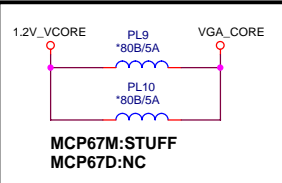
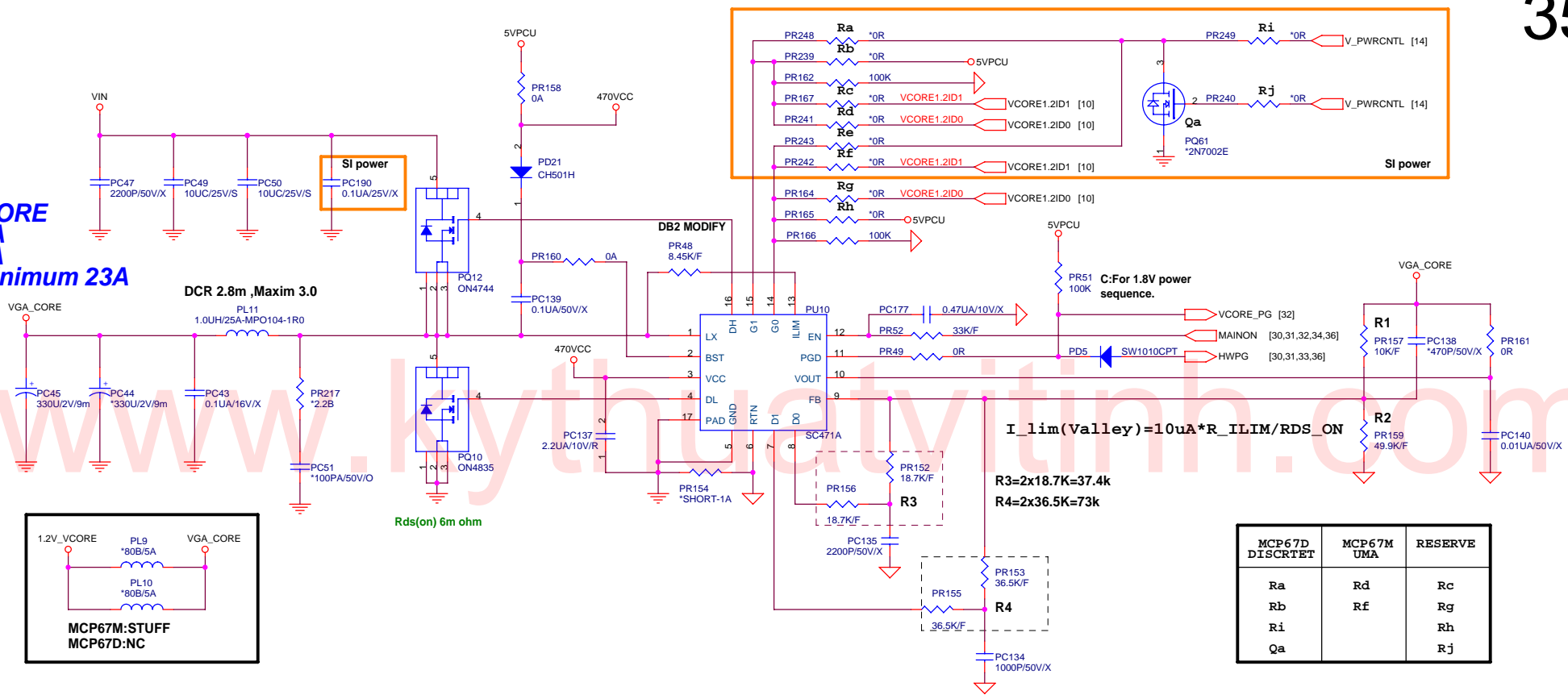
$90W P_{ra}=15.4K\Omega m (CS31543F929) 19.0V/4.23A=80.5W$
 $65W P_{ra}=30.9K\Omega m (CS33093F911) 18.5V/2.94A=54.5W$



PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MAX8724 CHARGER	Rev C2A
Date: Friday, December 29, 2006	Sheet 34	of 40

VGA_CORE
C/C:12A
P/C:15A
OCP minimum 23A



Rds(on) 6m ohm

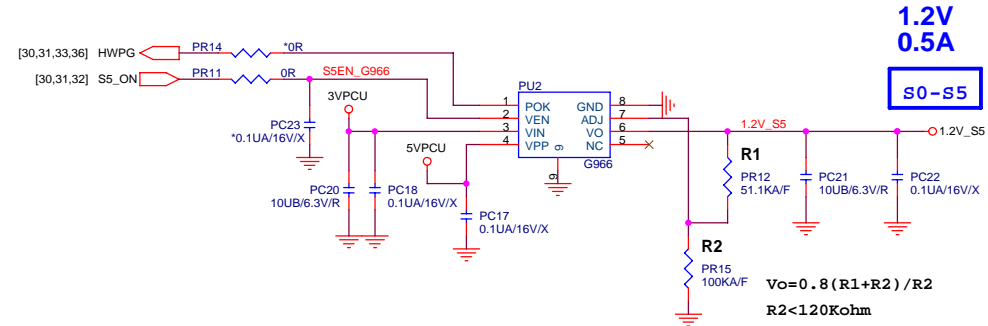
$I_{lim}(\text{Valley}) = 10\mu\text{A} * R_{ILIM} / R_{DS_ON}$

$R3 = 2 * 18.7\text{K} = 37.4\text{k}$

$R4 = 2 * 36.5\text{K} = 73\text{k}$

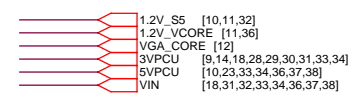
MCP67D DISCRETET	MCP67M UMA	RESERVE
Ra	Rd	Rc
Rb	Rf	Rg
Ri		Rh
Qa		Rj

INPUTS		OUTPUTS			VGA_CORE
G0	G1	OD1	OD2	OD3	
0	0	$0.75 * (1 + R1/R2 + R1/R3 + R1/R4)$			1.2V
0	1	$0.75 * (1 + R1/R2 + R1/R3)$			1.1V
1	0	$0.75 * (1 + R1/R2 + R1/R4)$			1.0V
1	1	$0.75 * (1 + R1/R2)$			0.9V



GFX_VID0
H: Normal Voltage
L: Low Voltage

VGACORECTL	NB8X	R2	R3/PR294	PR1293/PR295
HI	1.2V	CS43012FB10	NA	Mounted
LO	1.XV			

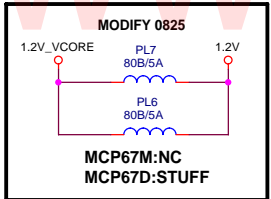


PROJECT : AT1
Quanta Computer Inc.

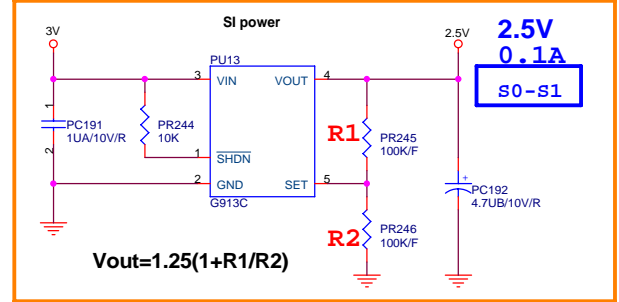
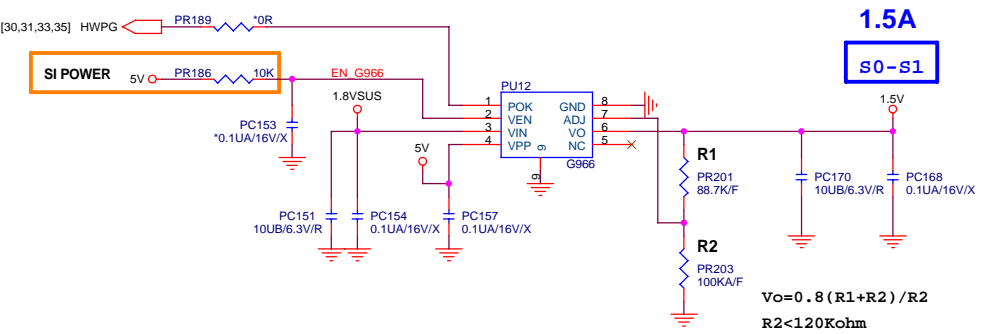
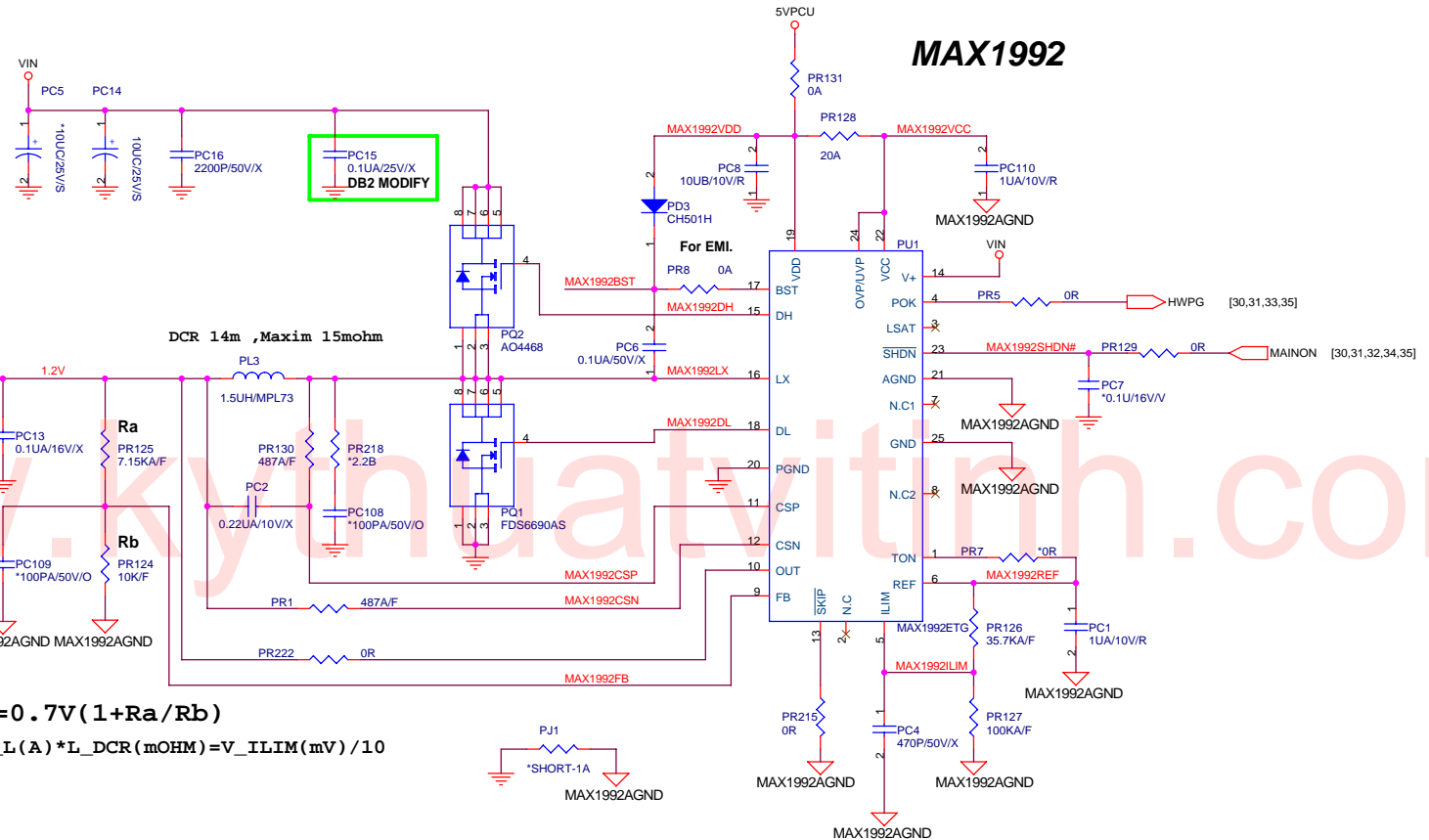
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MAX1992

S0-S1
1.2V
C/C:6A
P/C:8A
OCP minimum 10A



$V_{out} = 0.7V(1 + R_a/R_b)$
 $V_{cs} = I_L(A) * L_{DCR}(mOHM) = V_{ILIM}(mV) / 10$



- 1.2V_VCORE [11,35]
- 1.2V [10,11,12,13,15]
- 1.5V [27,28,31,32]
- 1.8VSUS [2,3,4,5,6,32,37]
- 2.5V [2,13,32]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,38]
- 5V [13,18,19,22,23,25,26,27,28,29,31,32,33,38]
- 5VPCU [10,23,33,34,35,37,38]
- VIN [18,31,32,33,34,35,37,38]

S0-S3

1.8VSUS
C/C:12A
P/C:15.2A
OCP minimum 25A

1.8 Volt +/-5%

DCR 2.8m ,Maxim 3.0

51116_V5IN PR119
0R
Fix 1.8V Output

$Ra = (V_{out} - 0.75) / 0.75 * Rb$
Rb value from 100K to 300K ohm

Rds(on) 4.2m ohm

S0-S3

SMDDR_VTERM
1.53A / 0.9V

SI MODIFY FOR POWER SEQUENCE 1211

0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

S0-S3

SMDDR_VTERM
0.9V
?A

0.9v/1.2A

1.8V
4.75A
S0-S1

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_TRIP (mV) = R_TRIP (Kohm) * 10 (uA)$
 $I_OCP = V_trip / Rds_on + I_Ripple / 2$

VDDQSET	VDDQ (V)	VTREF and Vtt	Note
GND	2.5	V_ vddqsns / 2	DDR
V5IN	1.8	V_ vddqsns / 2	DDR2
FB	adjustable	V_VDDQSNS / 2	1.5V < VDDQ < 3V

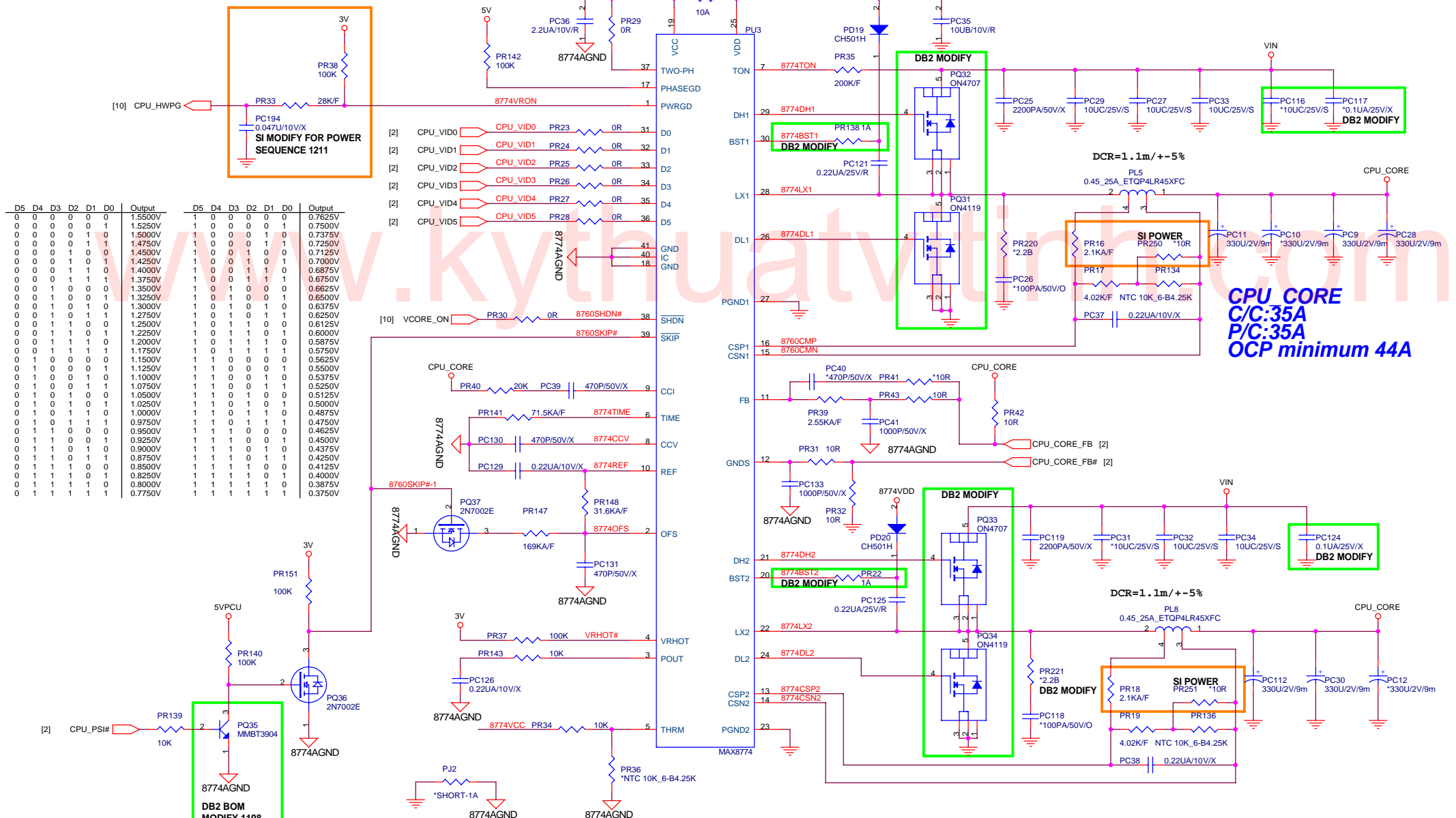
- SMDDR_VTERM [4]
- 1.8V [11,13,15,16,17,32]
- 1.8VSUS [2,3,4,5,6,32,36]
- 3V_S5 [8,9,10,11,20,28,30,32,33]
- 5VSUS [18,26,28,30,31,32,33]
- 5VPCU [10,23,33,34,35,36,38]
- VIN [18,31,32,33,34,35,36,38]

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CPU_CORE MAX8774


Slew rate=(12.5mVus)*(71.5K/R_TIME)
 VFB=V_VID+0.125(VREF-VOFS)
 VRHOT is low when VTHRM below 1.5V
 Tsw=16.26pF(R_TON+6.5K)ohm
 CCV CAP=470pF*(2/total phase)*300kHz/fsw



D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	0	1	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	0	1.4750V	1	0	0	1	0	0	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	1	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	0	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	0	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	1	0	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	1	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V

CPU_CORE
C/C:35A
P/C:35A
OCP minimum 44A

- CPU_CORE [4,32]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36]
- 5V [13,18,19,22,23,25,26,27,28,29,31,32,33,36]
- 5VPCU [10,23,33,34,35,36,37]
- VIN [18,31,32,33,34,35,36,37]



NBS/RD2/HWI

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