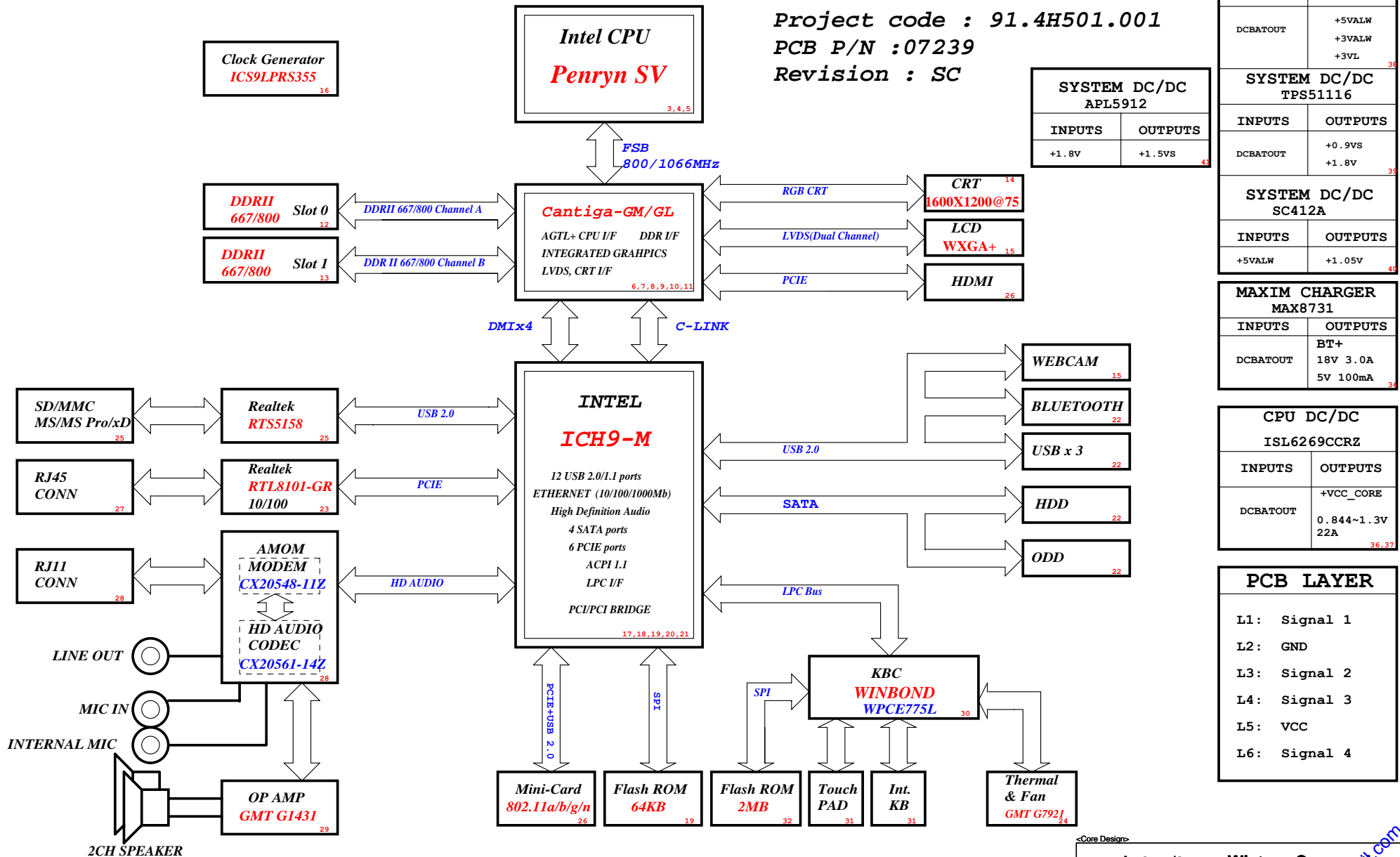


Warrior Intel UMA Block Diagram

Project code : 91.4H501.001
 PCB P/N : 07239
 Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
+5VALW	+1.05V

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC ISL6269CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCIe Routing page 19

LANE1	LAN
LANE2	MiniCard WLAN

USB Table page 19

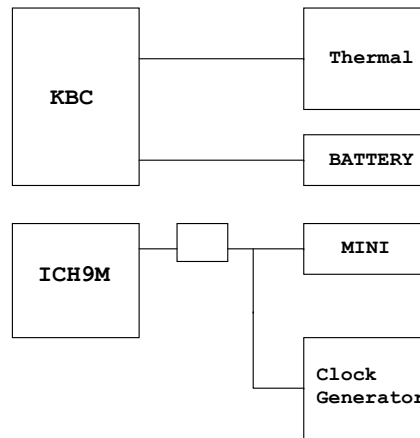
USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLEPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

SMBus



Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG6 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default)
CFG9	PCIe Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect... 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

<Core Design>

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Table of Content	
Size A3	Document Number
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Date: Friday, January 04, 2008	Rev SC
Sheet 2	of 42

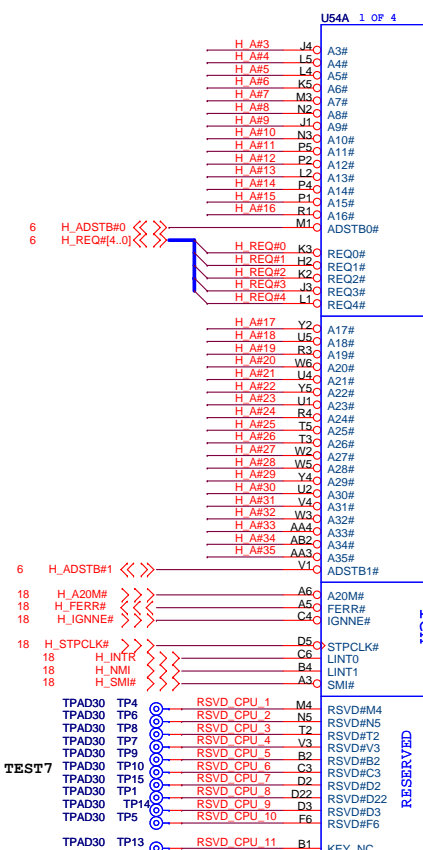
A

B

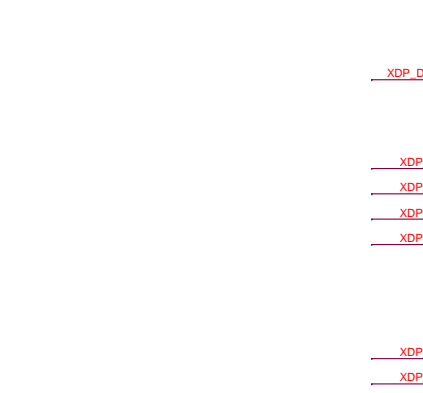
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D

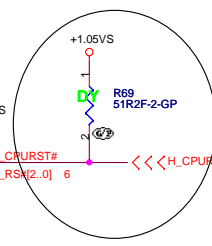
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BGA479-SK16-GPU4 62.10079.001

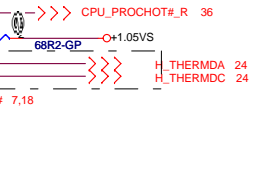


Reserve for ITP, when install ITP connector, install R2.

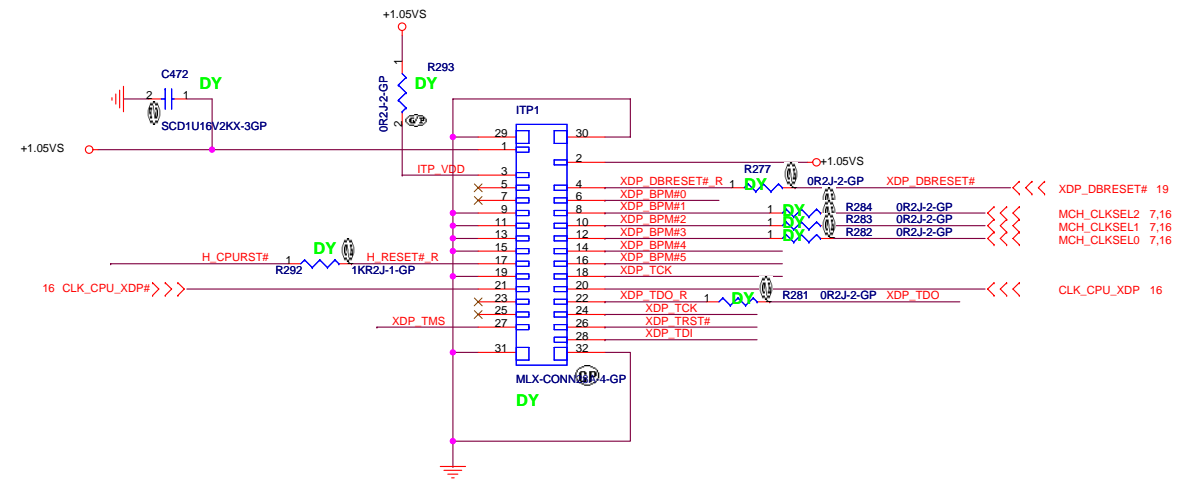


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Connect to V Core 4/23 Houston



ITP Connector



<Core Design> Place R310 with in 200ps (~1") to CPU

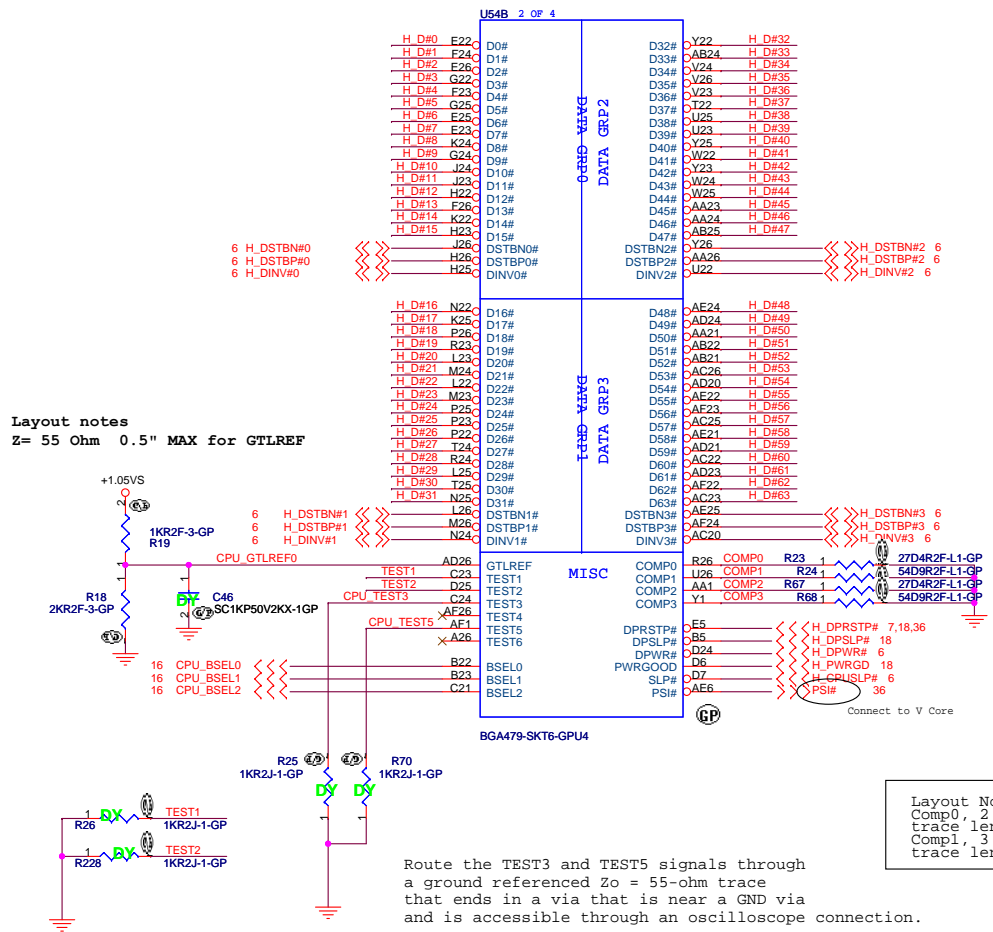
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Title: CPU (1 of 2)

Size: Document Number: Warrior Rev: SC

Date: Monday, January 07, 2008 Sheet: 3 of 42

H_DINV#[3..0] <<>>H_DINV#[3..0] 6
 H_DSTBN#[3..0] <<>>H_DSTBN#[3..0] 6
 H_DSTBP#[3..0] <<>>H_DSTBP#[3..0] 6
 H_D#[63..0] <<>>H_D#[63..0] 6



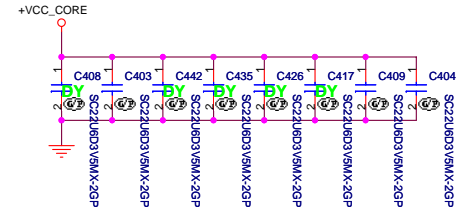
Layout notes
 Z= 55 Ohm 0.5" MAX for GTLREF

Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

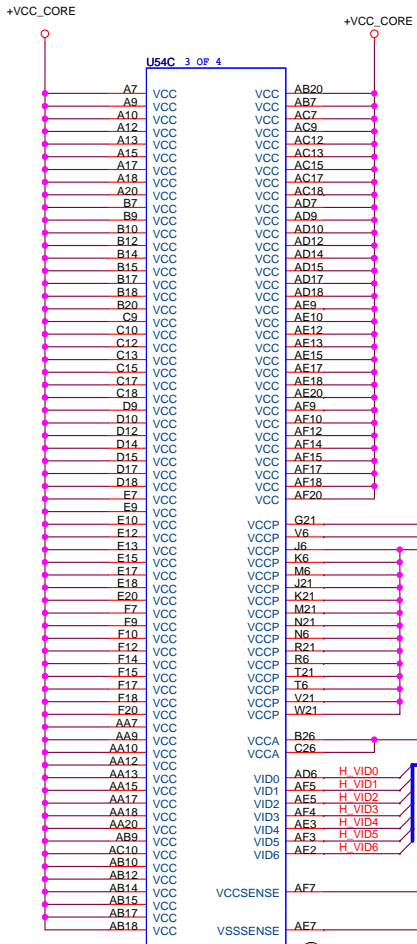
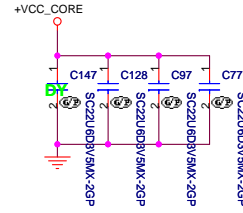
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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Title	
CPU (3 of 2)	
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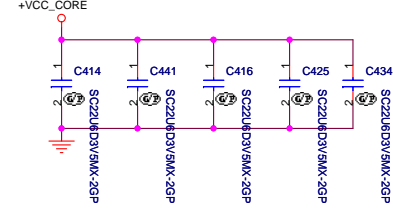
Please these inside socket cavity on L8(North side Secondary)



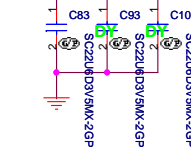
Please these outside socket cavity on L8(North side Secondary)



Please these inside socket cavity on L8(South side Secondary)

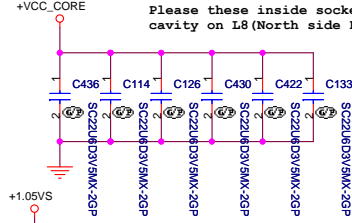


+VCC_CORE

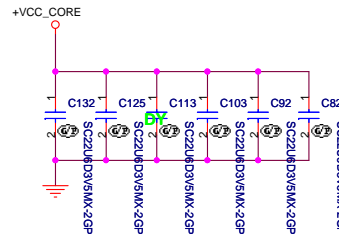


Please these outside socket cavity on L8(South side Secondary)

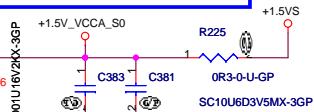
Please these inside socket cavity on L8(North side Primary)



Please these inside socket cavity on L8(South side Primary)



layout note: "1D5V VCCA_S0" as short as possible



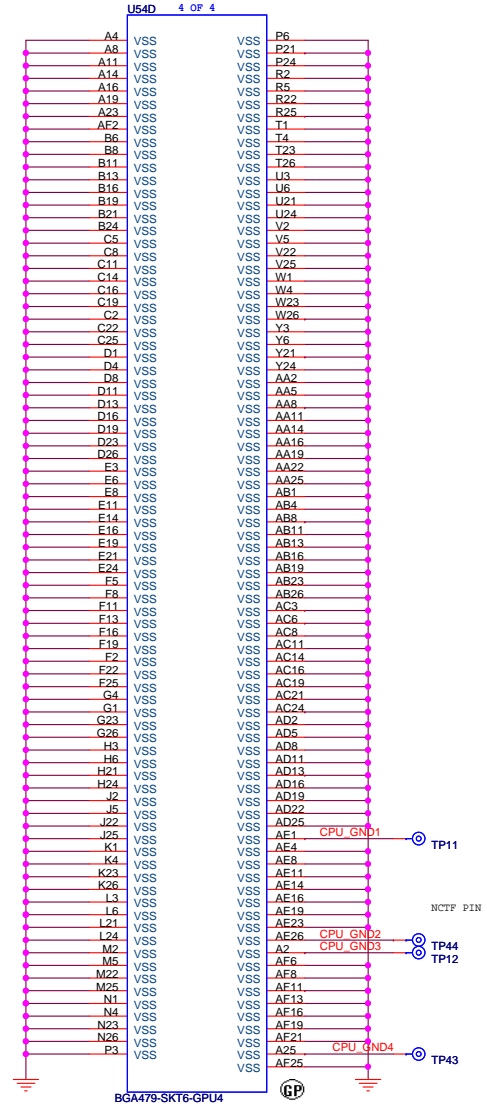
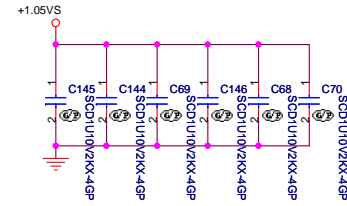
Layout Note: Place as close as possible to the CPU VCCA pin.



Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

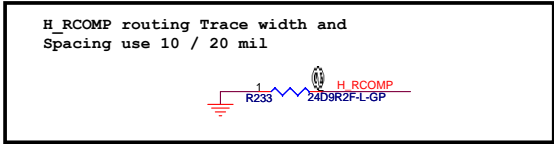
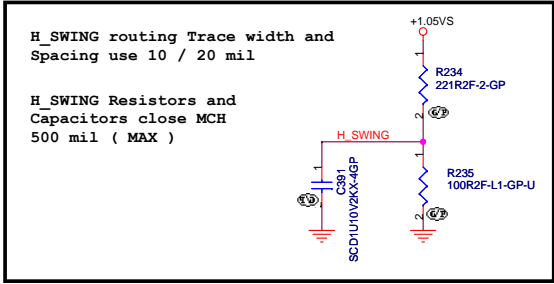
Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)

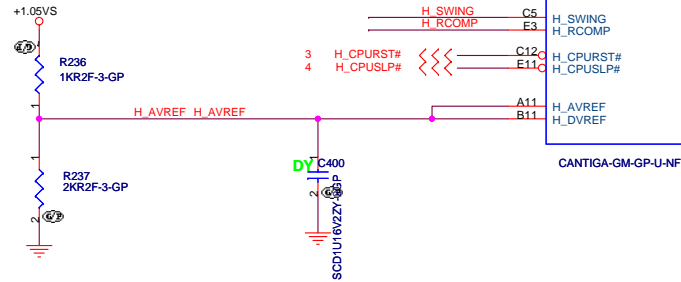


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Size	Document Number	Rev	SC
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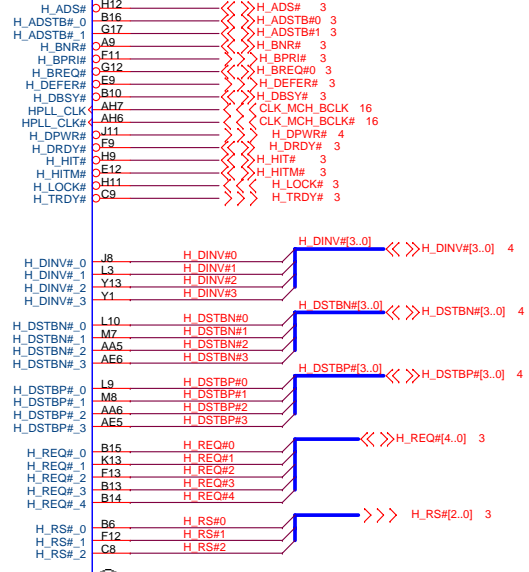


Place them near to the chip (< 0.5")



H_D#0	F2	H_D#_0	H_A#_3	A14	H_A#3
H_D#1	G3	H_D#_1	H_A#_4	C15	H_A#4
H_D#2	F8	H_D#_2	H_A#_5	F16	H_A#5
H_D#3	E6	H_D#_3	H_A#_6	H13	H_A#6
H_D#4	G2	H_D#_4	H_A#_7	C18	H_A#7
H_D#5	H6	H_D#_5	H_A#_8	M16	H_A#8
H_D#6	H2	H_D#_6	H_A#_9	J13	H_A#9
H_D#7	F6	H_D#_7	H_A#_10	E16	H_A#10
H_D#8	D4	H_D#_8	H_A#_11	R16	H_A#11
H_D#9	H3	H_D#_9	H_A#_12	N17	H_A#12
H_D#10	M3	H_D#_10	H_A#_13	M13	H_A#13
H_D#11	M9	H_D#_11	H_A#_14	E17	H_A#14
H_D#12	J1	H_D#_12	H_A#_15	F17	H_A#15
H_D#13	J2	H_D#_13	H_A#_16	G20	H_A#16
H_D#14	N12	H_D#_14	H_A#_17	B19	H_A#17
H_D#15	J6	H_D#_15	H_A#_18	J16	H_A#18
H_D#16	L2	H_D#_16	H_A#_19	E20	H_A#19
H_D#17	R2	H_D#_17	H_A#_20	H16	H_A#20
H_D#18	N9	H_D#_18	H_A#_21	J20	H_A#21
H_D#19	M5	H_D#_19	H_A#_22	L17	H_A#22
H_D#20	M5	H_D#_20	H_A#_23	A17	H_A#23
H_D#21	J3	H_D#_21	H_A#_24	B17	H_A#24
H_D#22	N2	H_D#_22	H_A#_25	L16	H_A#25
H_D#23	R1	H_D#_23	H_A#_26	C21	H_A#26
H_D#24	N5	H_D#_24	H_A#_27	J17	H_A#27
H_D#25	N6	H_D#_25	H_A#_28	H20	H_A#28
H_D#26	P13	H_D#_26	H_A#_29	B18	H_A#29
H_D#27	N8	H_D#_27	H_A#_30	K17	H_A#30
H_D#28	L7	H_D#_28	H_A#_31	B20	H_A#31
H_D#29	N10	H_D#_29	H_A#_32	F21	H_A#32
H_D#30	M3	H_D#_30	H_A#_33	K21	H_A#33
H_D#31	Y3	H_D#_31	H_A#_34	L20	H_A#34
H_D#32	AD14	H_D#_32	H_A#_35		
H_D#33	Y6	H_D#_33	H_ADSTB#_0	B16	H_ADSTB#_0
H_D#34	Y10	H_D#_34	H_ADSTB#_1	G17	H_ADSTB#_1
H_D#35	Y12	H_D#_35	H_BNRP#_0	A9	H_BNRP#_0
H_D#36	Y14	H_D#_36	H_BPRIP#_0	E11	H_BPRIP#_0
H_D#37	Y7	H_D#_37	H_BREQ#_0	G12	H_BREQ#_0
H_D#38	W2	H_D#_38	H_DEFER#_0	E9	H_DEFER#_0
H_D#39	A8	H_D#_39	H_DBSY#_0	B10	H_DBSY#_0
H_D#40	Y9	H_D#_40	HPLL_CLK#_0	AH7	CLK_MCH_BCLK#_0
H_D#41	AA13	H_D#_41	HPLL_CLK#_1	AH6	CLK_MCH_BCLK#_1
H_D#42	AA9	H_D#_42	H_DPWR#_0	J11	H_DPWR#_0
H_D#43	AA11	H_D#_43	H_DRDY#_0	E9	H_DRDY#_0
H_D#44	AD10	H_D#_44	H_HIT#_0	E12	H_HIT#_0
H_D#45	AD13	H_D#_45	H_HITM#_0	C11	H_HITM#_0
H_D#46	AE12	H_D#_46	H_LOCK#_0	C11	H_LOCK#_0
H_D#47	AE8	H_D#_47	H_TRDY#_0	C9	H_TRDY#_0
H_D#48	AE2	H_D#_48			
H_D#49	AD8	H_D#_49			
H_D#50	AA3	H_D#_50			
H_D#51	AD3	H_D#_51			
H_D#52	AD7	H_D#_52			
H_D#53	AE14	H_D#_53			
H_D#54	AE3	H_D#_54			
H_D#55	AC1	H_D#_55			
H_D#56	AE3	H_D#_56			
H_D#57	AE3	H_D#_57			
H_D#58	AC3	H_D#_58			
H_D#59	AE11	H_D#_59			
H_D#60	AE8	H_D#_60			
H_D#61	AG2	H_D#_61			
H_D#62	AD6	H_D#_62			
H_D#63		H_D#_63			

HOST



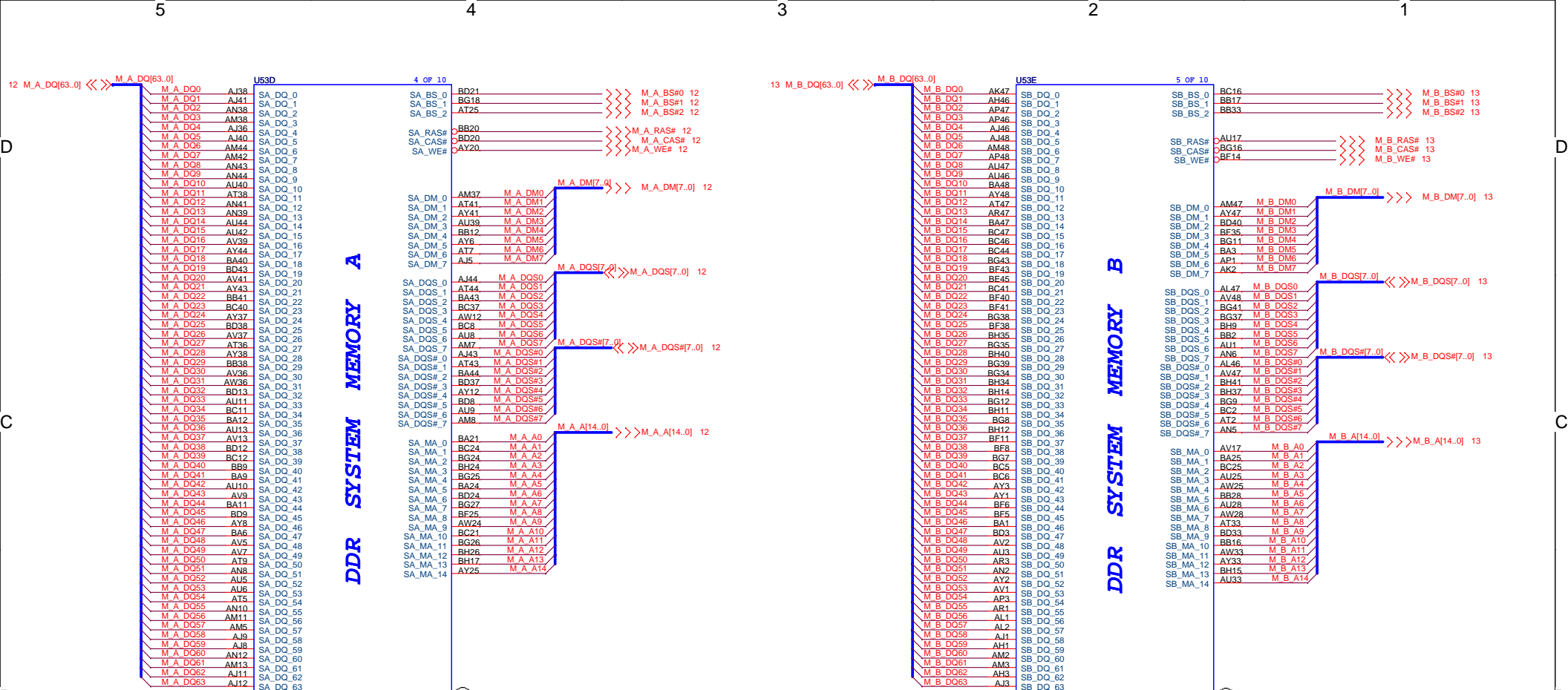
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 Taipei Hsein 221, Taiwan, R.O.C.

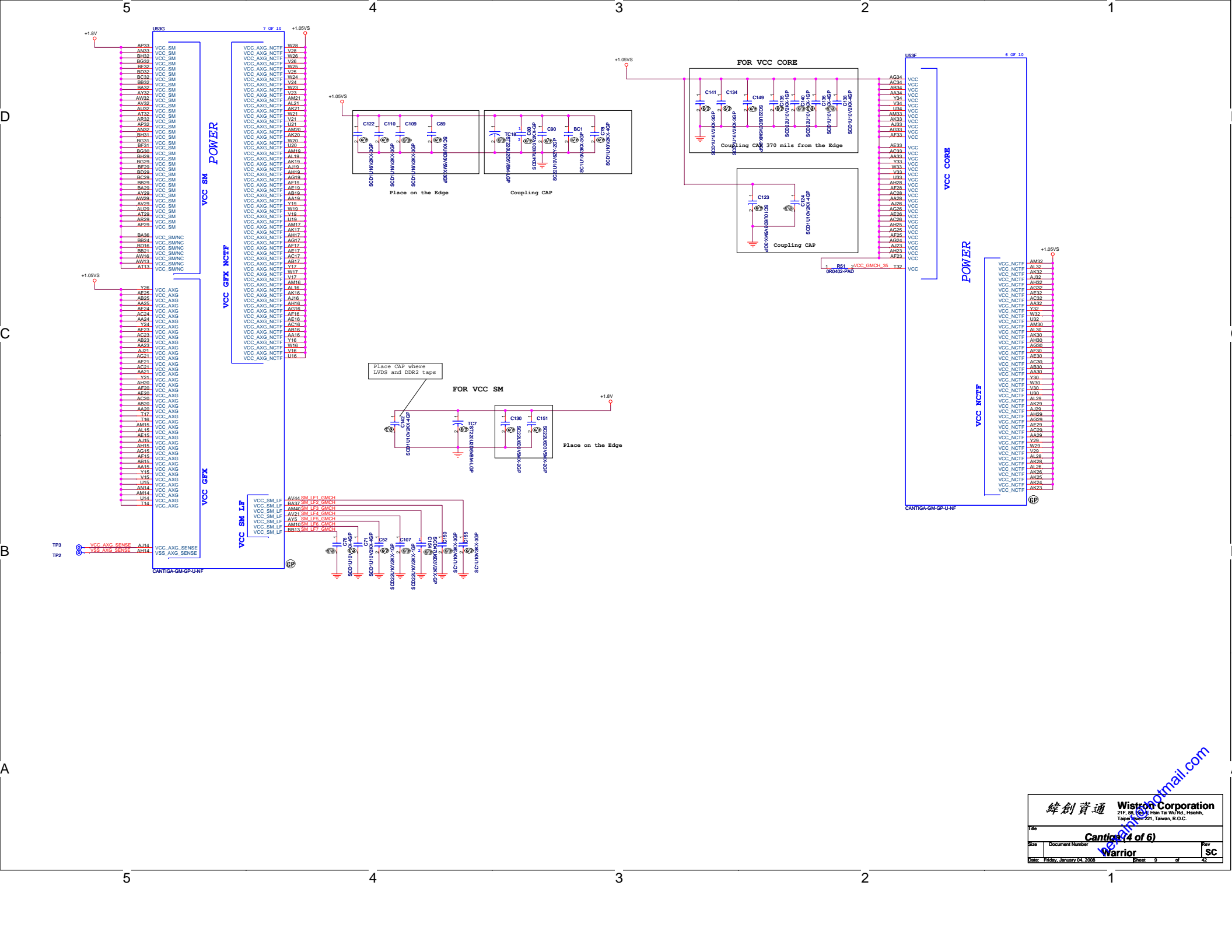
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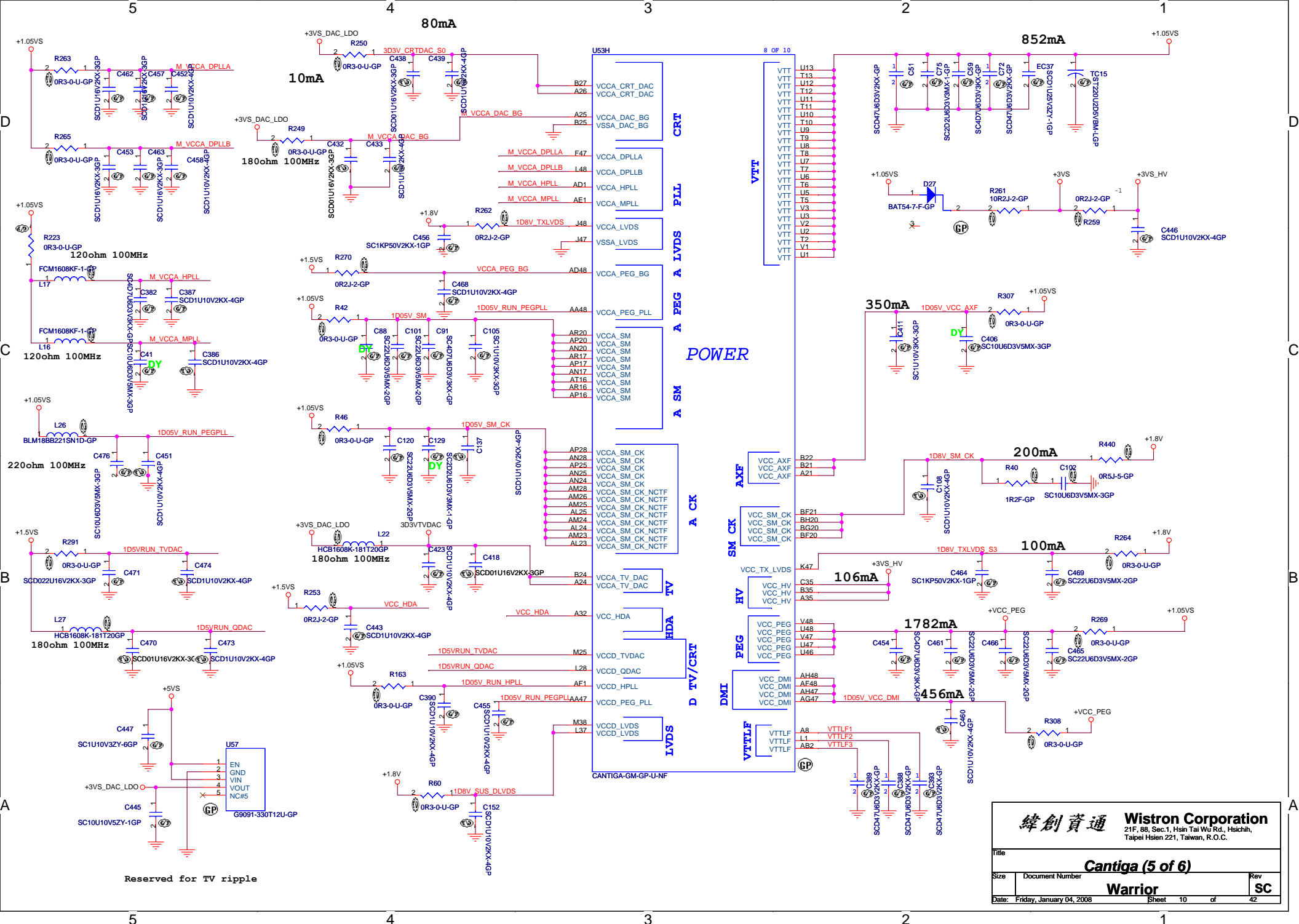
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Date: Monday, January 07, 2008 Sheet 6 of 42



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Size	Document Number		Rev
	Warrior		SC
Date:	Monday, January 07, 2008	Sheet	8 of 42





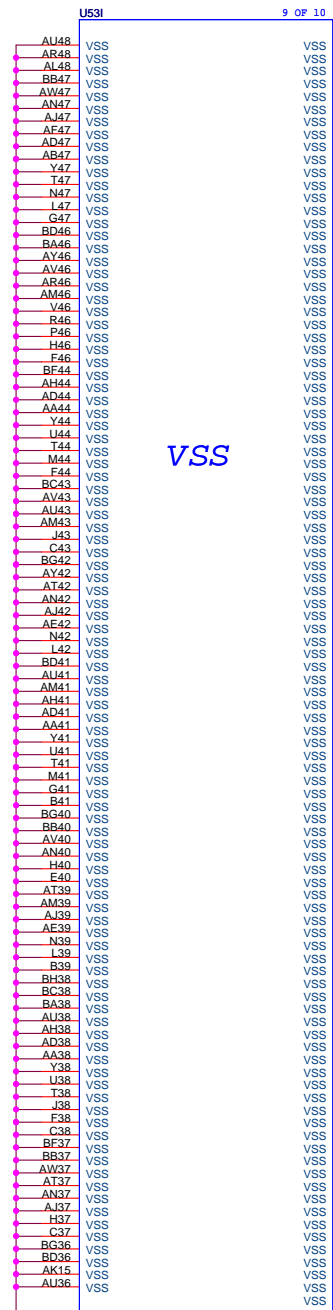
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 Taipei Hsien 221, Taiwan, R.O.C.

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Size: _____ Document Number: _____ Rev: _____

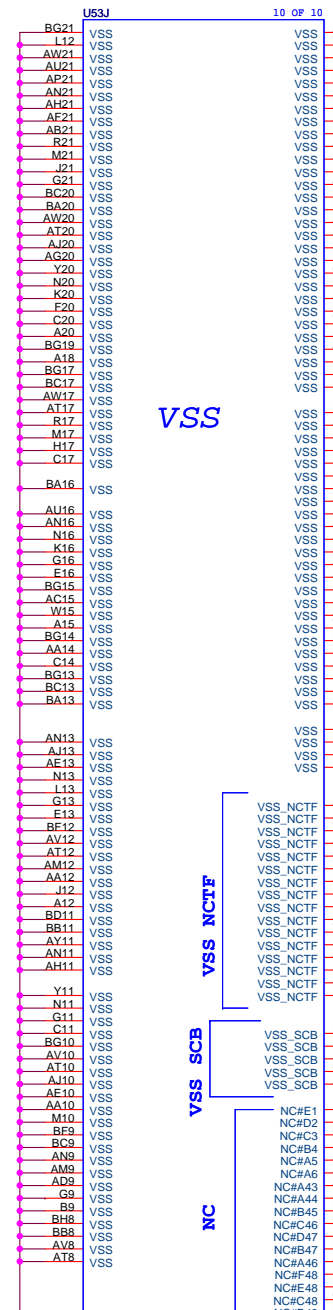
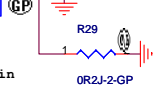
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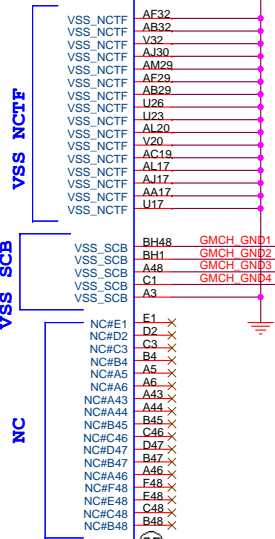


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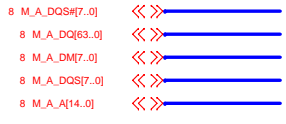
Modification AJ6 to reserved Pin



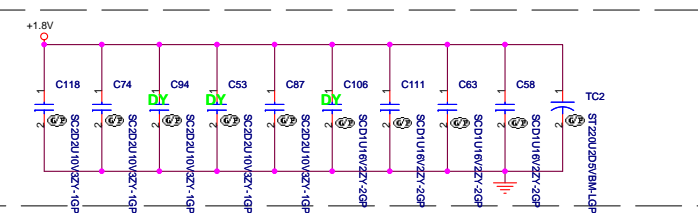
CANTIGA-GM-GP-U-NF



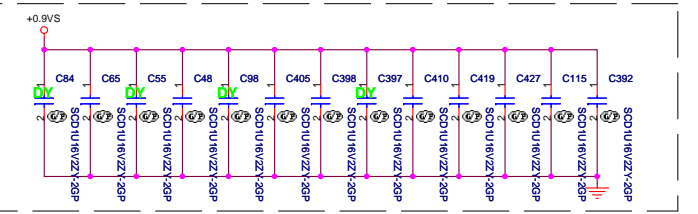
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Cantiga (6 of 6)			
Size:	Document Number:	Rev: SC	
Date:	Friday, January 04, 2008	Sheet:	11 of 42



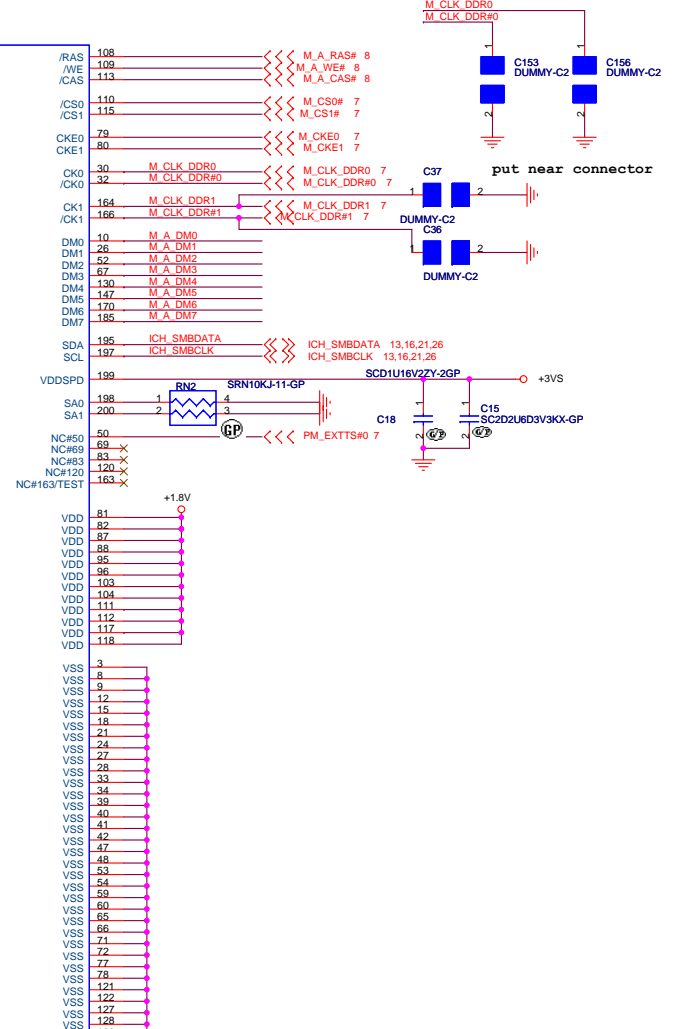
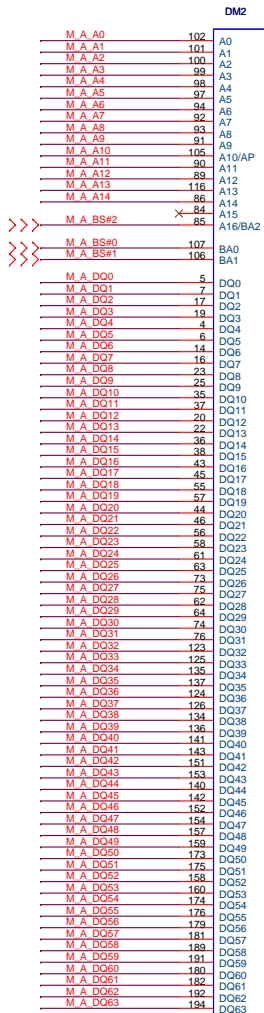
Layout Note:
Place near DM1



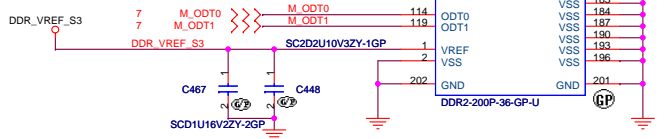
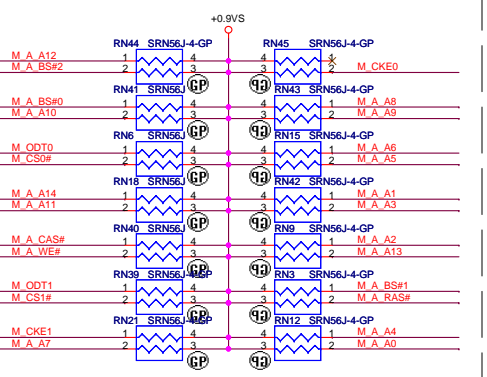
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



8 M_A_BS#2
8 M_A_BS#0
8 M_A_BS#1



Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"



DM2 use 62.10017.E11

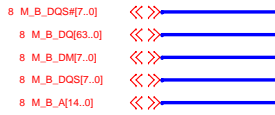
<Core Design>

緯創資通 **Wistron Corporation**
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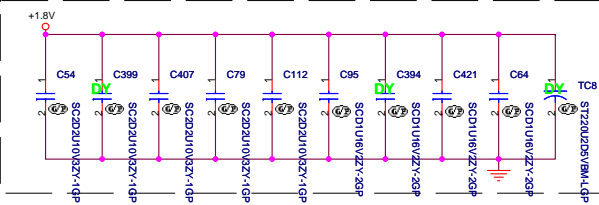
Title: **DDR2-SODIMM SLOT1**

Size: Document Number
Customer: **Warrior** Rev: **SC**

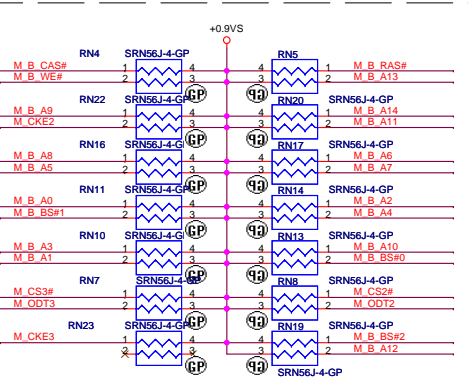
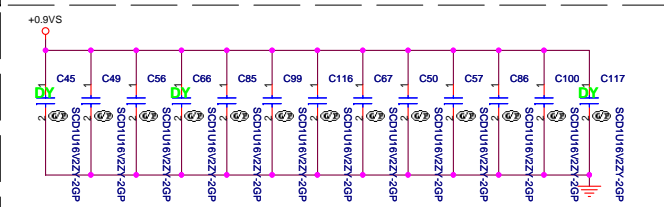
Date: Monday, January 07, 2008 Sheet 12 of 42



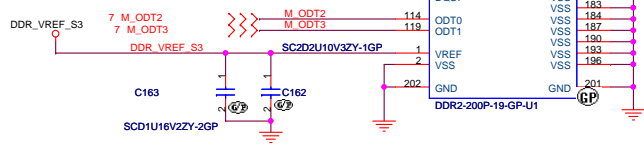
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

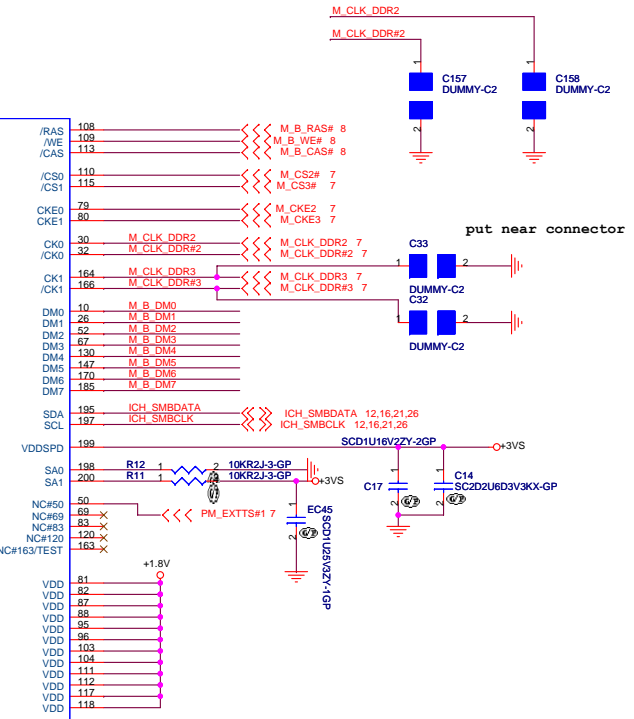


Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



DM1 use 62.10017.B51

M_B_A0	102	A0
M_B_A1	101	A1
M_B_A2	100	A2
M_B_A3	99	A3
M_B_A4	98	A4
M_B_A5	97	A5
M_B_A6	94	A6
M_B_A7	92	A7
M_B_A8	93	A8
M_B_A9	91	A9
M_B_A10	105	A10/AP
M_B_A11	90	A11
M_B_A12	89	A12
M_B_A13	116	A13
M_B_A14	86	A14
M_B_A15	84	A15
M_B_BS#2	85	A16/BA2
M_B_BS#0	107	BA0
M_B_BS#1	106	BA1
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	17	DQ2
M_B_DQ3	19	DQ3
M_B_DQ4	6	DQ4
M_B_DQ5	4	DQ5
M_B_DQ6	14	DQ6
M_B_DQ7	20	DQ7
M_B_DQ8	23	DQ8
M_B_DQ9	25	DQ9
M_B_DQ10	35	DQ10
M_B_DQ11	37	DQ11
M_B_DQ12	20	DQ12
M_B_DQ13	22	DQ13
M_B_DQ14	38	DQ14
M_B_DQ15	38	DQ15
M_B_DQ16	43	DQ16
M_B_DQ17	45	DQ17
M_B_DQ18	55	DQ18
M_B_DQ19	57	DQ19
M_B_DQ20	44	DQ20
M_B_DQ21	46	DQ21
M_B_DQ22	56	DQ22
M_B_DQ23	58	DQ23
M_B_DQ24	61	DQ24
M_B_DQ25	63	DQ25
M_B_DQ26	73	DQ26
M_B_DQ27	75	DQ27
M_B_DQ28	62	DQ28
M_B_DQ29	64	DQ29
M_B_DQ30	74	DQ30
M_B_DQ31	76	DQ31
M_B_DQ32	123	DQ32
M_B_DQ33	125	DQ33
M_B_DQ34	135	DQ34
M_B_DQ35	137	DQ35
M_B_DQ36	124	DQ36
M_B_DQ37	126	DQ37
M_B_DQ38	134	DQ38
M_B_DQ39	136	DQ39
M_B_DQ40	141	DQ40
M_B_DQ41	143	DQ41
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M_B_DQ43	153	DQ43
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M_B_DQ52	158	DQ52
M_B_DQ53	160	DQ53
M_B_DQ54	174	DQ54
M_B_DQ55	176	DQ55
M_B_DQ56	179	DQ56
M_B_DQ57	181	DQ57
M_B_DQ58	189	DQ58
M_B_DQ59	191	DQ59
M_B_DQ60	180	DQ60
M_B_DQ61	182	DQ61
M_B_DQ62	192	DQ62
M_B_DQ63	194	DQ63
M_B_DQS#0	11	DQS0
M_B_DQS#1	29	DQS1
M_B_DQS#2	49	DQS2
M_B_DQS#3	68	DQS3
M_B_DQS#4	129	DQS4
M_B_DQS#5	146	DQS5
M_B_DQS#6	167	DQS6
M_B_DQS#7	188	DQS7
M_B_DQS#0	13	DQS0
M_B_DQS#1	31	DQS1
M_B_DQS#2	70	DQS2
M_B_DQS#3	70	DQS3
M_B_DQS#4	131	DQS4
M_B_DQS#5	148	DQS5
M_B_DQS#6	169	DQS6
M_B_DQS#7	188	DQS7
M_ODT2	114	ODT0
M_ODT3	119	ODT1
M_ODT0		
M_ODT1		



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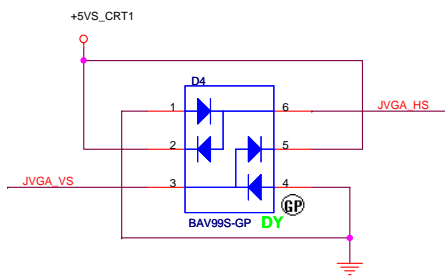
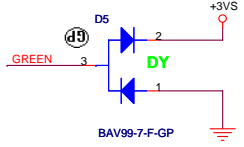
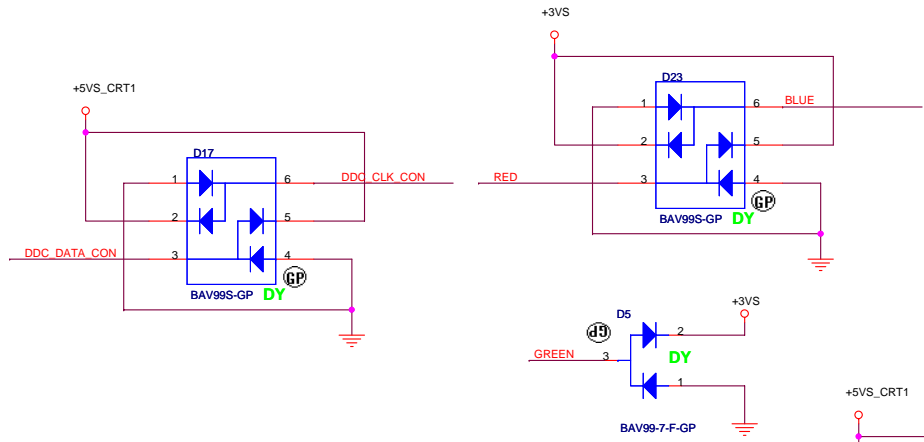
DDR2-SODIMM SLOT2

Warrior

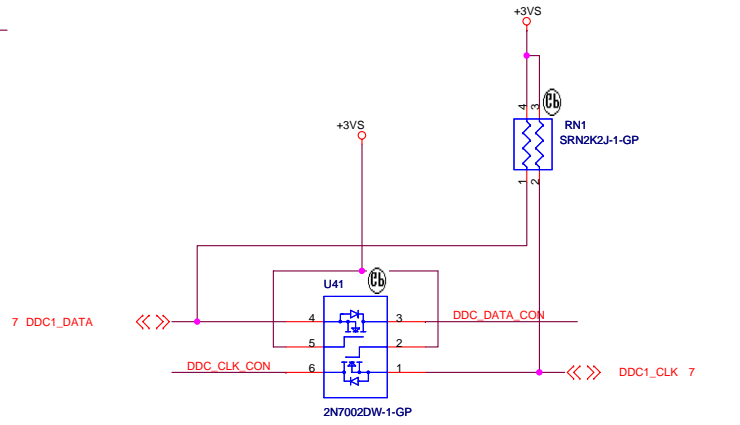
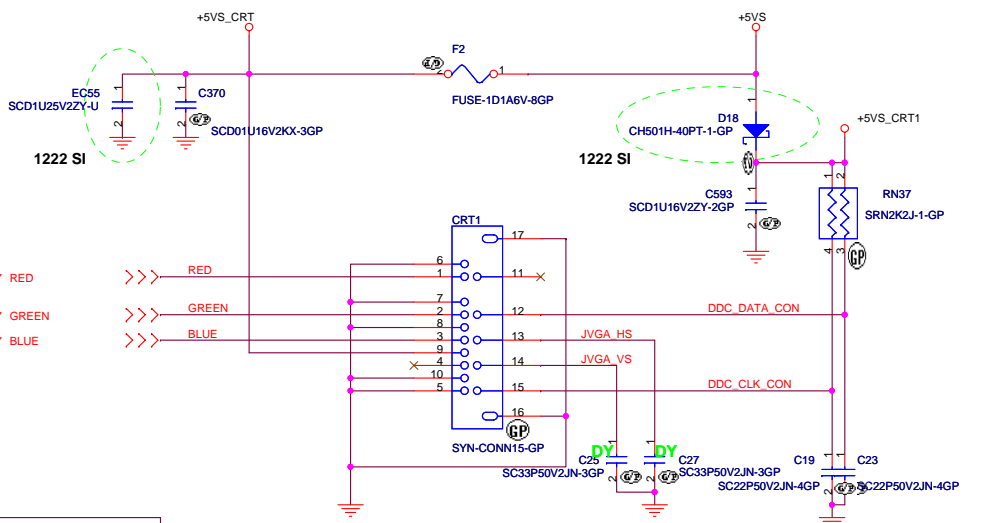
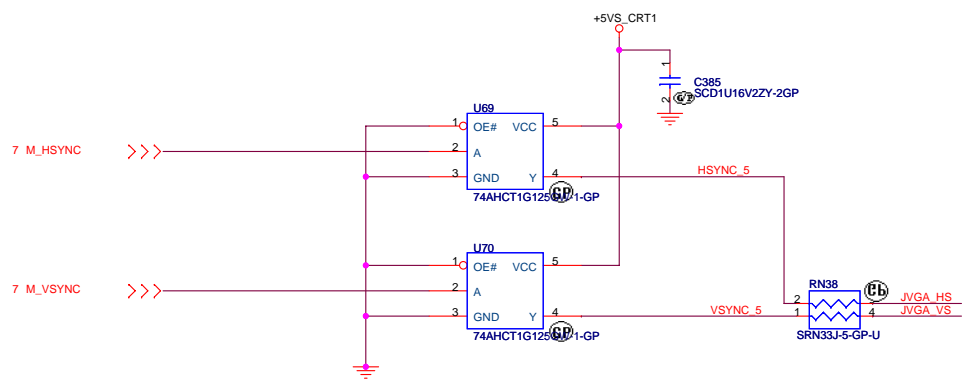
Monday, January 07, 2008

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CRT I/F & CONNECTOR



Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



5V @ ext. CRT side

<Core Design>

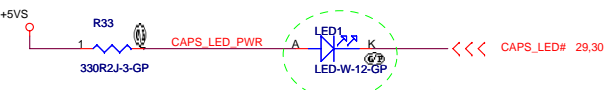
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size A3 Document Number **Warrior** Rev **SC**

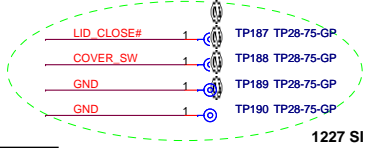
Date: Monday, January 07, 2008 Sheet 14 of 42

LCD / INVERTER INTERFACE / CAMERA

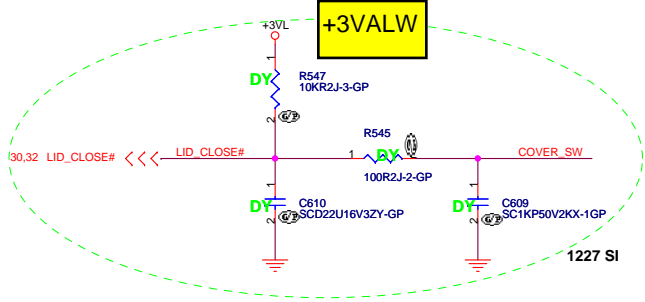


White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70

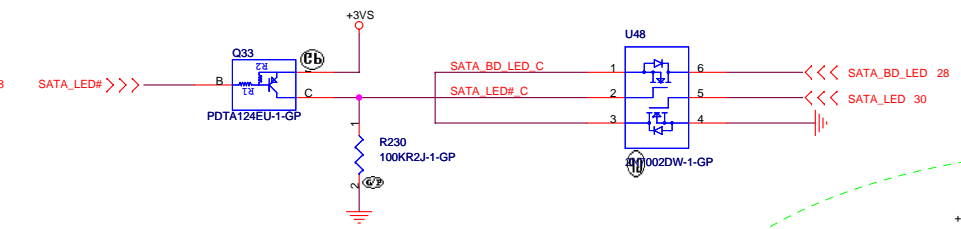
1218 SI



1227 SI



1227 SI



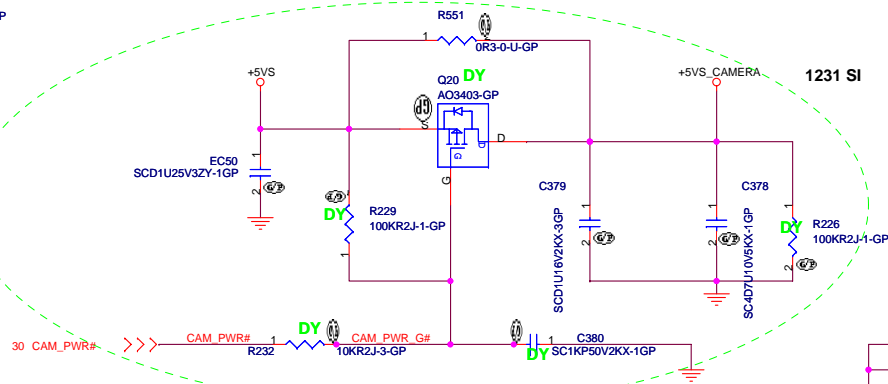
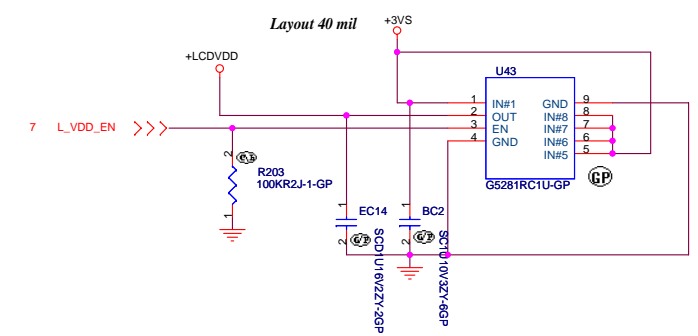
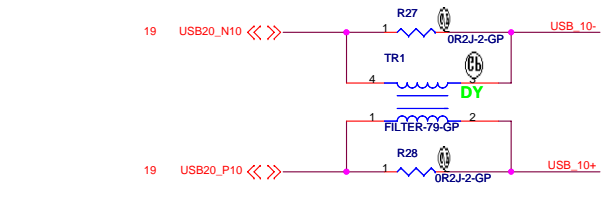
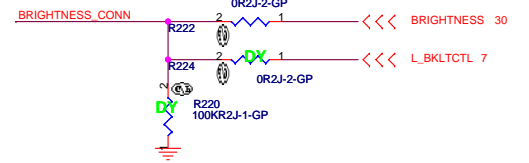
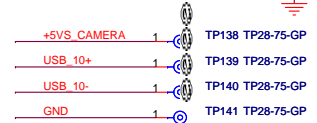
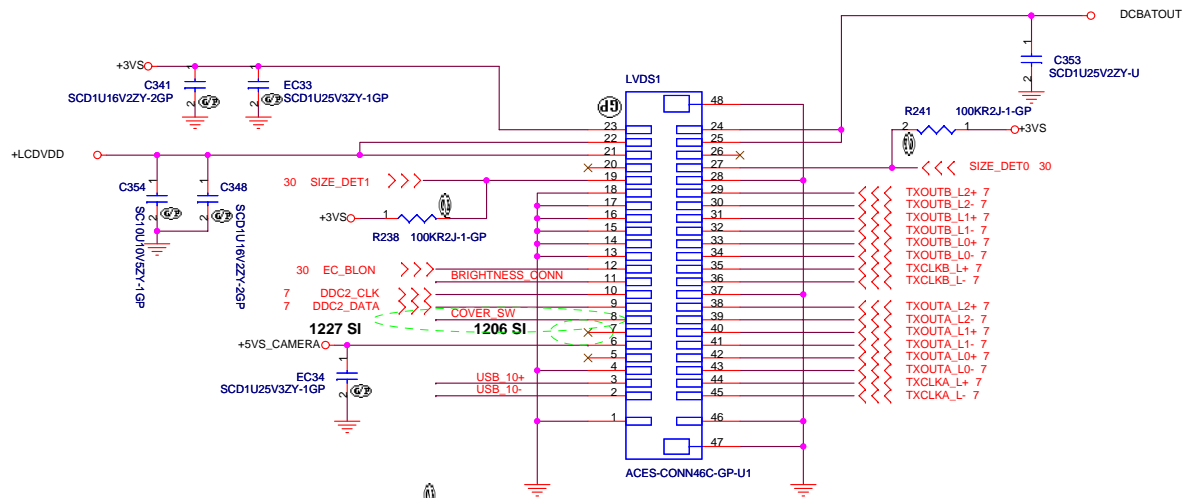
SATA_LED# >>> SATA_LED# C

SATA_BD_LED_C

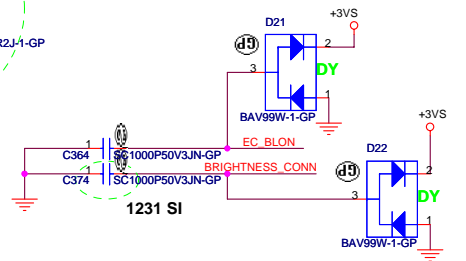
SATA_LED# C

SATA_LED 28

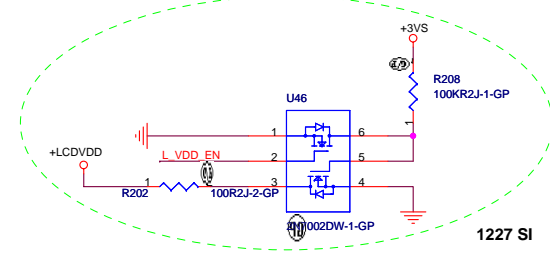
SATA_LED 30



1231 SI



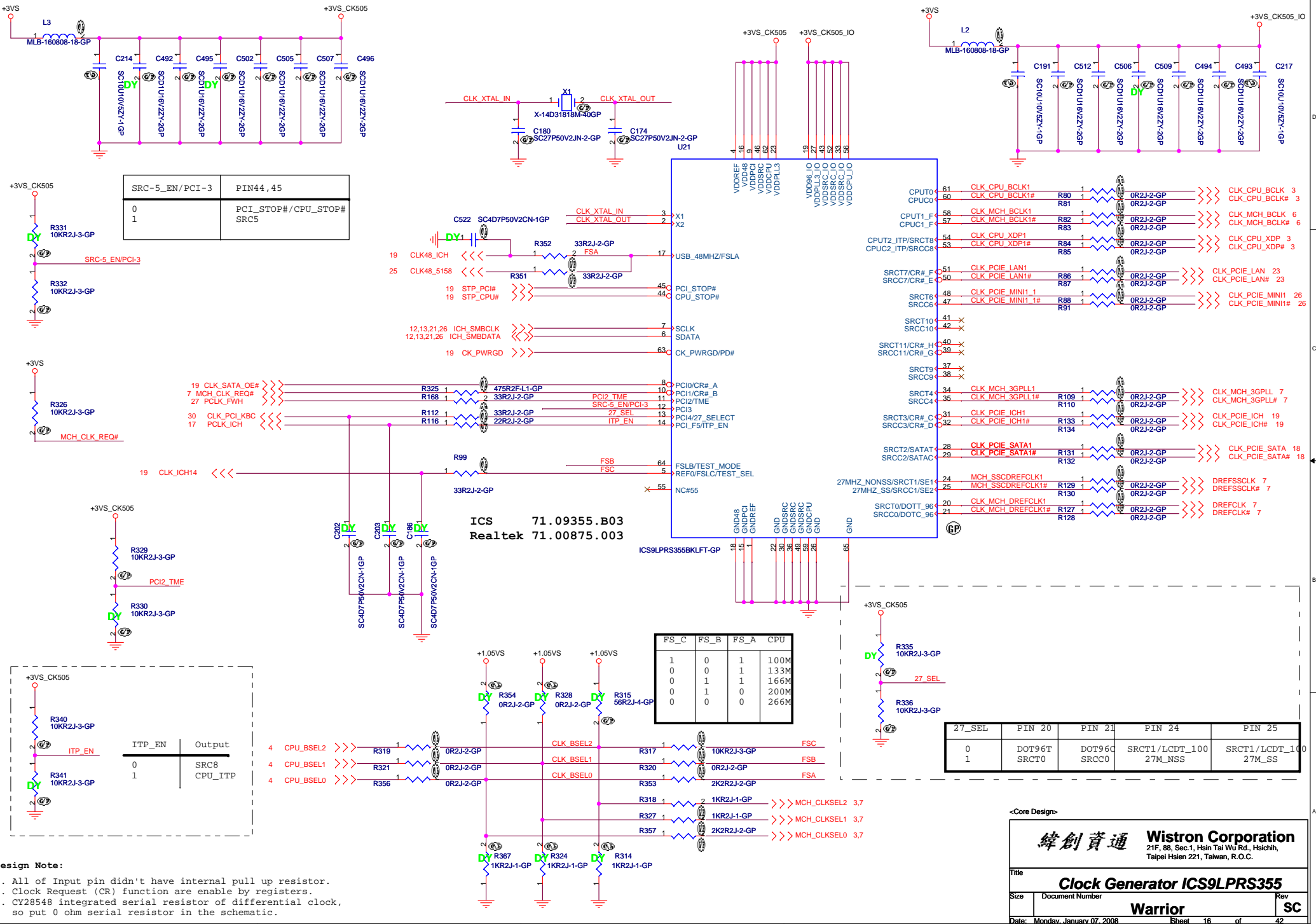
1231 SI



1227 SI

<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih Taipei Hsien 221, Taiwan, R.O.C.			
Title	LCD/Inverter Connector/CAM/LED		
Size	Document Number		
A3			
Date:	Monday, January 07, 2008	Sheet	15 of 42
Warrior		SC	



SRC-5_EN/PCI-3	PIN44, 45
0	PCI_STOP#/CPU_STOP#
1	SRC5

Signal	Pin	Function
19 CLK_SATA_OE#	8	PCI0/CR#_A
7 MCH_CLK_REQ#	10	PCI1/CR#_B
27 PCLK_FWH	11	PCI2/TME
30 CLK_PCI_KBC	12	PCI3
17 PCLK_ICH	13	PCI4/27_SELECT
	14	ITP_EN

ITP_EN	Output
0	SRC8
1	CPU_ITP

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	SRCT0	27M_NSS	SRCT1/LCDDT_100
1		SRCC0		SRCT1/LCDDT_10

Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

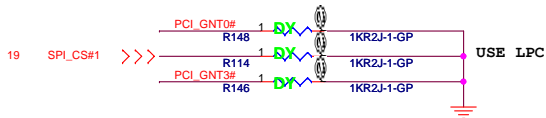
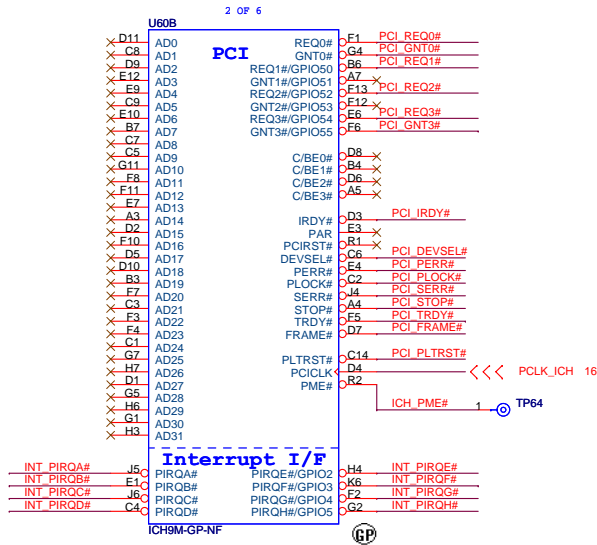
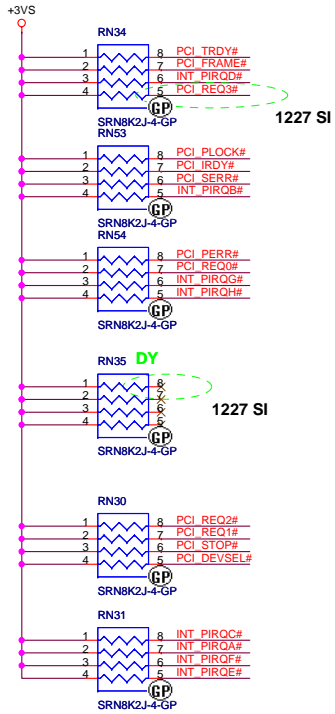
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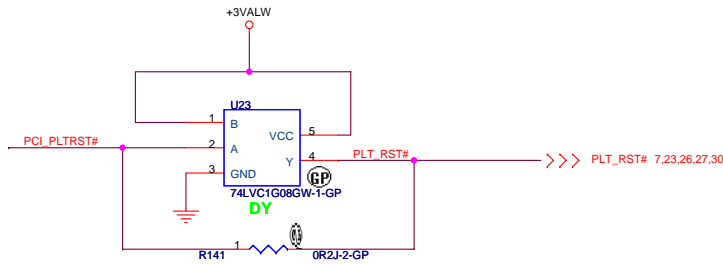
Title: **Clock Generator ICS9LPRS355**

Size: Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 16 of 42

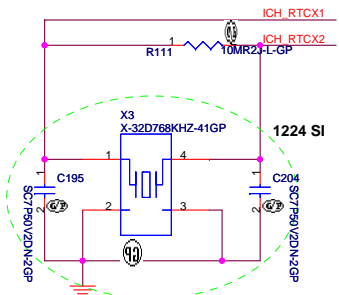


BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

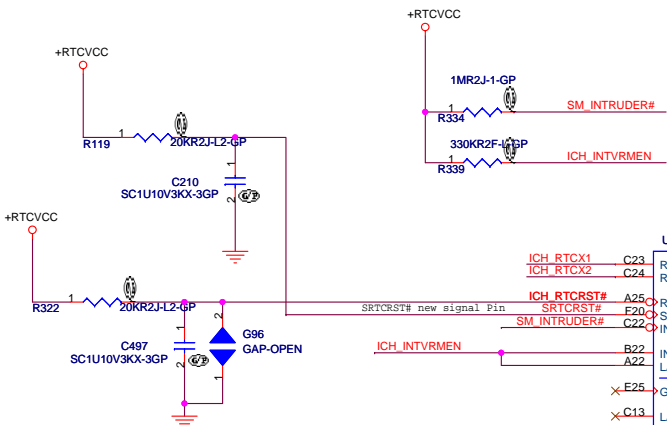


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichang Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ICH9-M (1 of 5)			
Size	Document Number	Rev	SC
Date:	Monday, January 07, 2008	Sheet	42

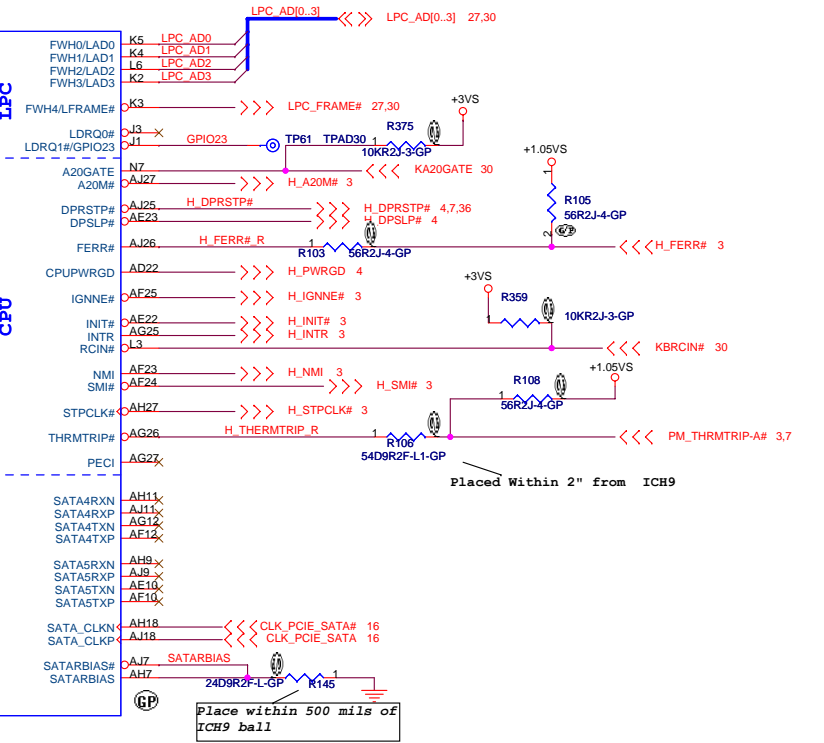
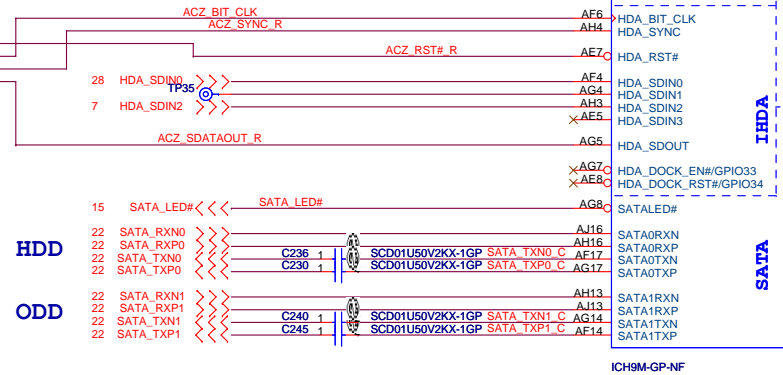
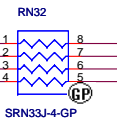


82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm



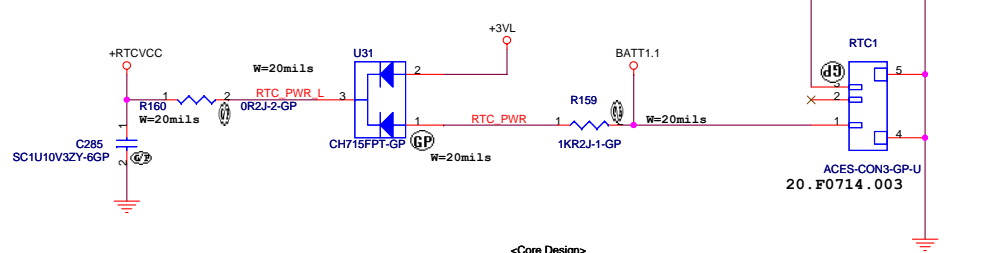
GLAN_COMP place within 500 mil of ICH9M

7.28 HDA_RST#_CODEC
7.28 HDA_BITCLK_CODEC
7.28 HDA_SYNC_CODEC
7.28 HDA_SDOUT_CODEC



Placed Within 2" from ICH9

Place within 500 mils of ICH9 ball



integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

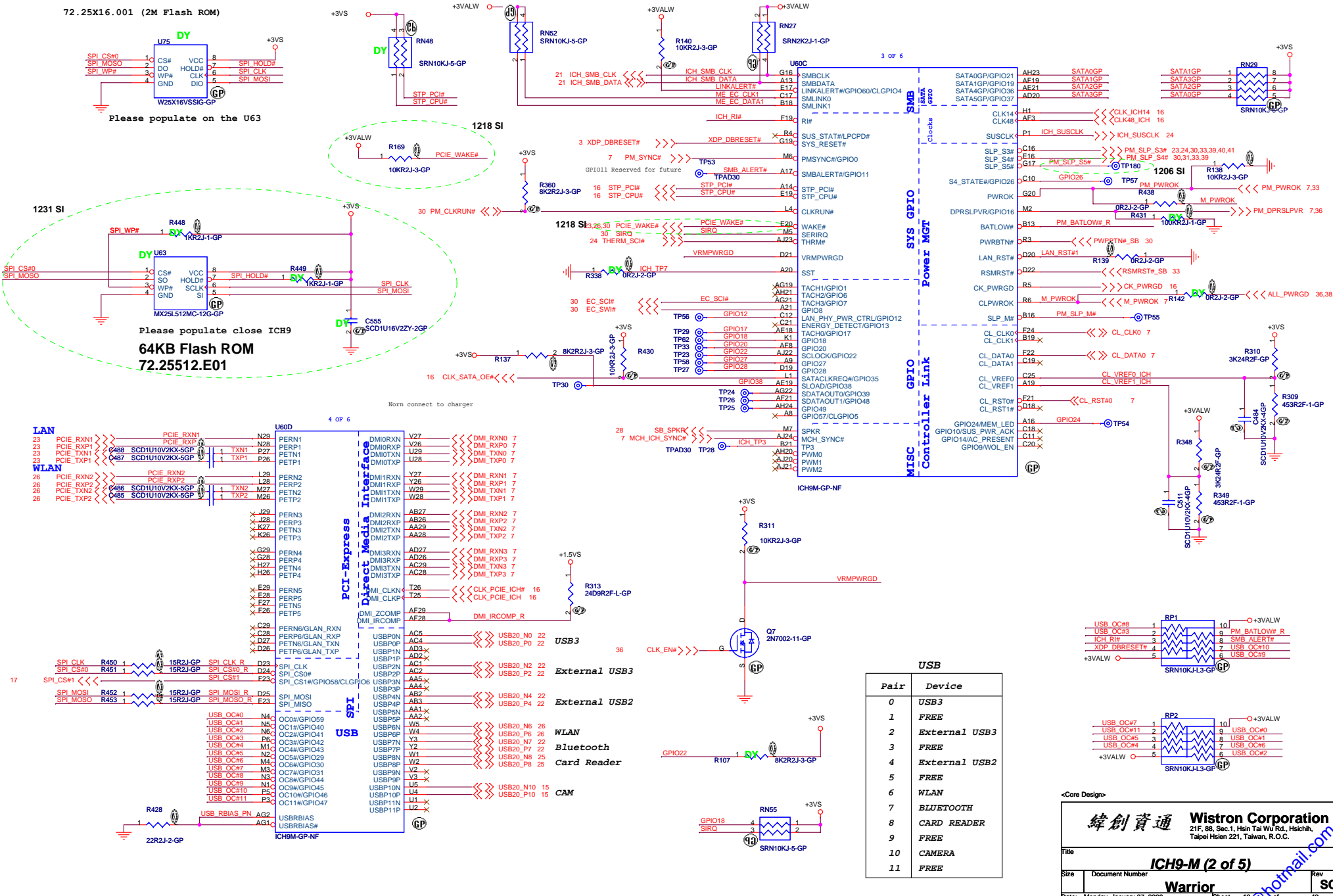
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File: **ICH9-M (2 of 5)**

Size: Document Number **Warrior** Rev **SC**

Date: Monday, January 07, 2008 Sheet 18 of 42



Please populate on the U63

Please populate close ICH9
64KB Flash ROM
72.25512.E01

USB

Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD READER
9	FREE
10	CAMERA
11	FREE

<Core Design>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **ICH9-M (2 of 5)**

Size: Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 18 of 42

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5 OF 6

AA26	VSS	H5
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	AC22
AA23	VSS	K28
AB28	VSS	K29
AB29	VSS	L13
AB4	VSS	L15
AB5	VSS	L2
AC17	VSS	L26
AC26	VSS	L27
AC27	VSS	L5
AC3	VSS	L7
AD1	VSS	M12
AD10	VSS	M13
AD12	VSS	M14
AD13	VSS	M15
AD14	VSS	M16
AD17	VSS	M17
AD18	VSS	M23
AD21	VSS	M28
AD28	VSS	M29
AD29	VSS	N11
AD4	VSS	N12
AD5	VSS	N13
AD6	VSS	N14
AD7	VSS	N15
AD9	VSS	N16
AE12	VSS	N17
AE13	VSS	N18
AE14	VSS	N26
AE16	VSS	N27
AE17	VSS	P12
AE2	VSS	P13
AE20	VSS	P14
AE24	VSS	P15
AE3	VSS	P16
AE4	VSS	P17
AE6	VSS	P2
AE9	VSS	P23
AF13	VSS	P28
AF16	VSS	P29
AF18	VSS	P4
AF22	VSS	P7
AH26	VSS	R11
AF26	VSS	R12
AF27	VSS	R13
AF5	VSS	R14
AF7	VSS	R15
AF9	VSS	R16
AG13	VSS	R17
AG16	VSS	R18
AG18	VSS	R28
AG20	VSS	T12
AG23	VSS	T13
AG31	VSS	T14
AG6	VSS	T15
AG9	VSS	T16
AH12	VSS	T17
AH14	VSS	T23
AH17	VSS	B26
AH19	VSS	U12
AH2	VSS	U13
AH22	VSS	U14
AH25	VSS	U15
AH28	VSS	U16
AH5	VSS	U17
AH8	VSS	AD23
AJ12	VSS	U26
AJ14	VSS	U27
AJ17	VSS	U3
AJ8	VSS	V1
B11	VSS	V13
B14	VSS	V15
B17	VSS	V23
B2	VSS	V28
B20	VSS	V29
B23	VSS	V4
B5	VSS	V5
B6	VSS	W26
C26	VSS	W27
C27	VSS	W3
E11	VSS	Y1
E14	VSS	Y28
E18	VSS	Y29
E2	VSS	Y4
E21	VSS	Y5
E24	VSS	AG28
E5	VSS	AH6
E8	VSS	AF2
F16	VSS	B25
F28	VSS	
F29	VSS	A1
G12	VSS	A2
G14	VSS	A28
G18	VSS	A29
G21	VSS	AH1
G24	VSS	AH29
G26	VSS	AJ1
G27	VSS	AJ2
G8	VSS	AJ28
H2	VSS	AJ29
H23	VSS	B1
H28	VSS	B29
H29	VSS	

ICH9M-GP-NF

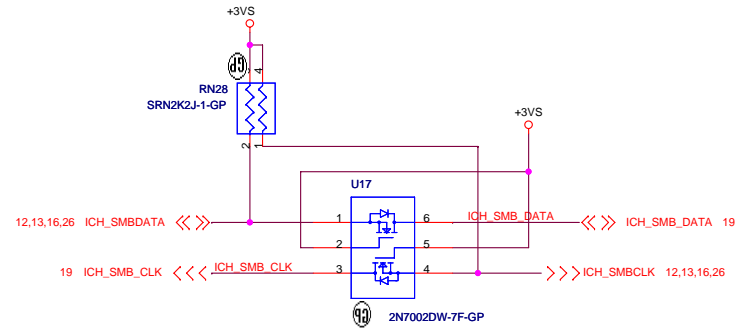
ICH_GND1 TP60

ICH_GND2 TP51

ICH_GND3 TP63

ICH_GND4 TP52

NCTF PIN



SMBUS

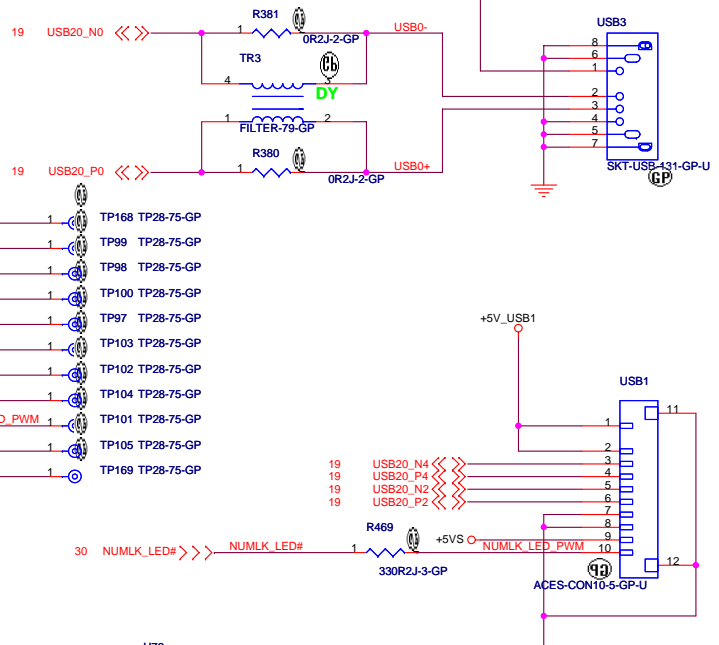
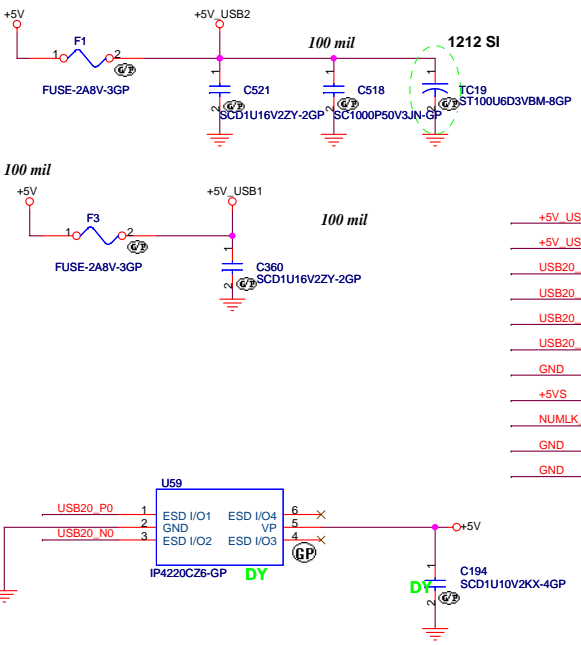
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (4 of 4)

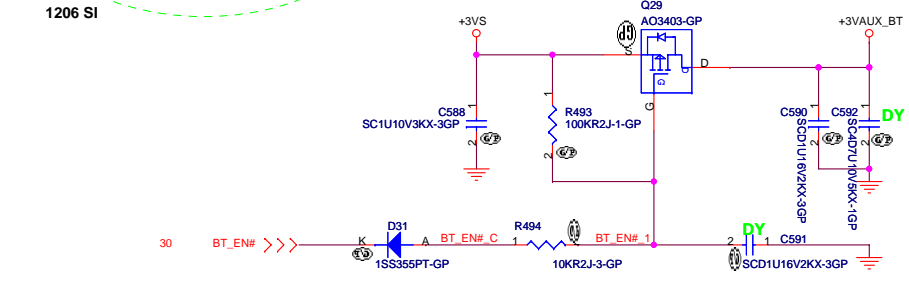
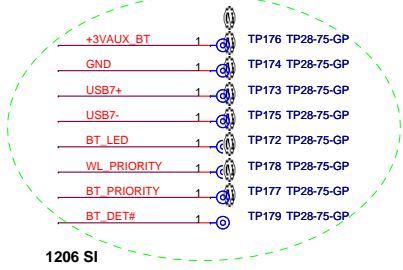
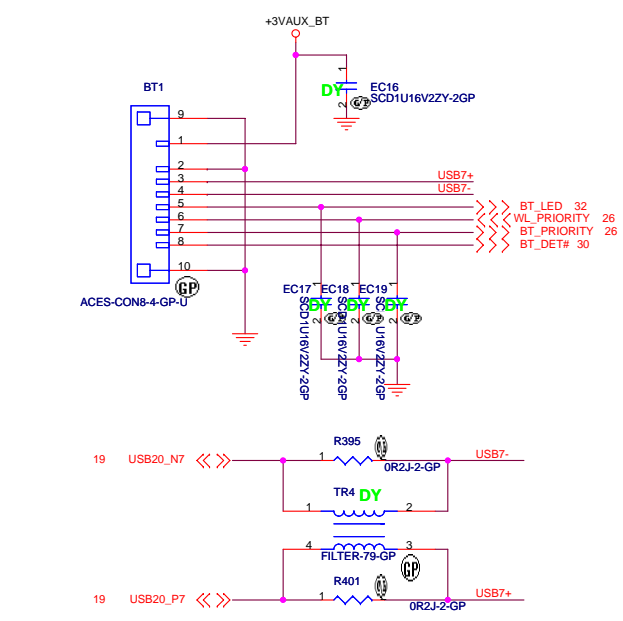
Size: Document Number: Rev: SC

Date: Monday, January 07, 2008 Sheet 21 of 42

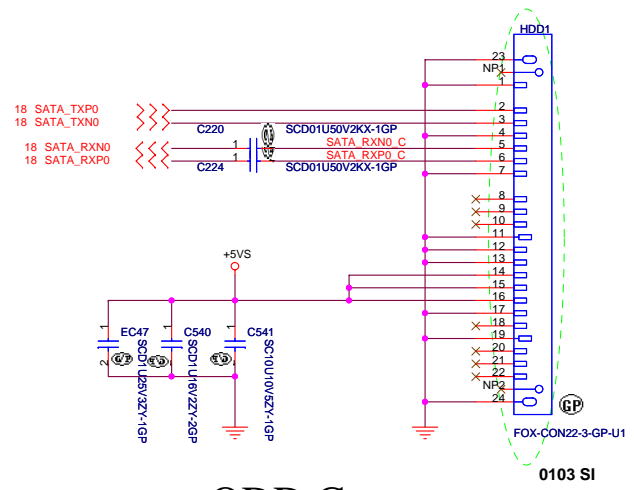
USB PORT



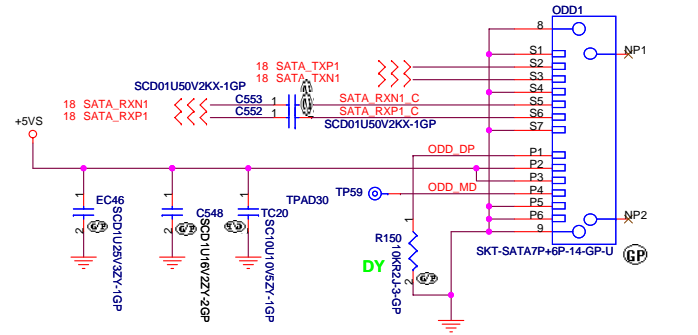
BLUETOOTH



SATA HD Connector



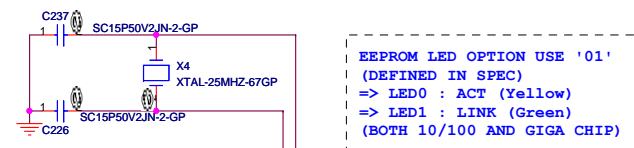
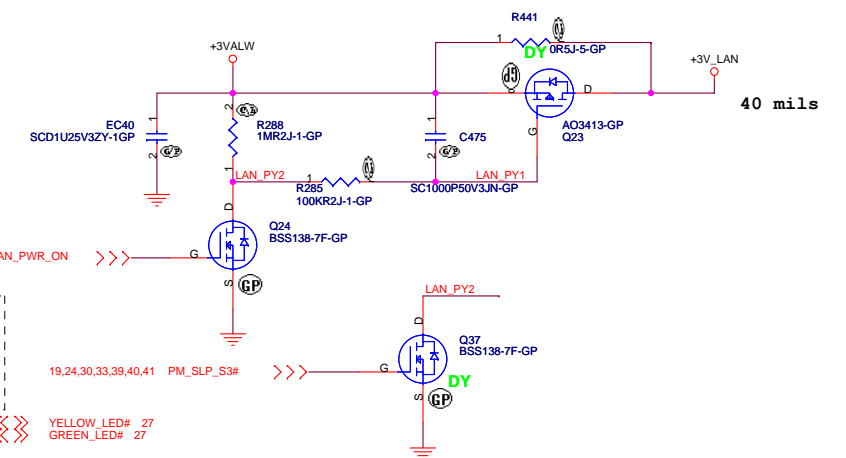
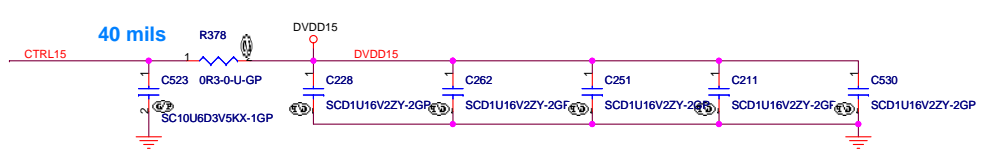
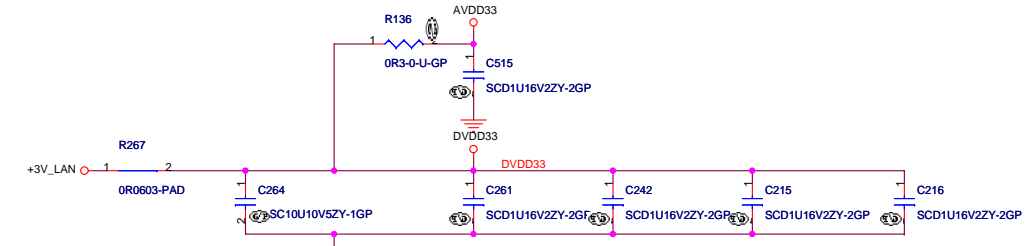
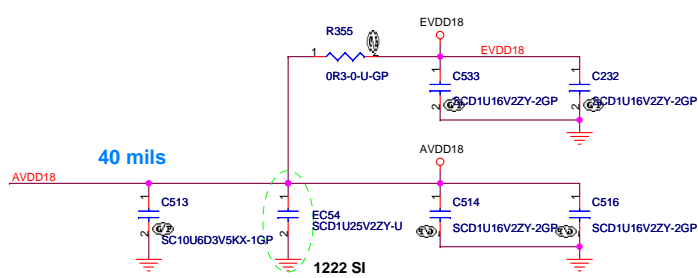
ODD Connector



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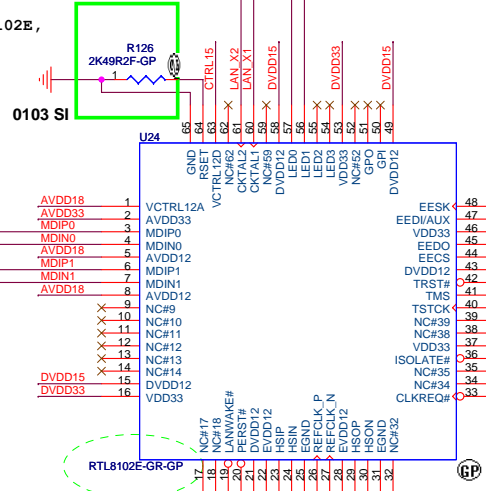
緯創資通 Wistron Corporation
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File		
HDD/CDROM/USB/BT		
Size	Document Number	Rev
A3		SC
Date: Monday, January 07, 2008		Sheet 22 of 42

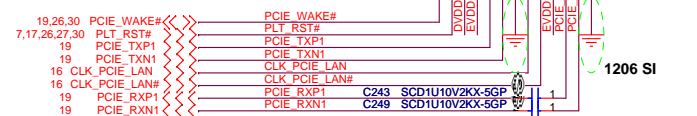
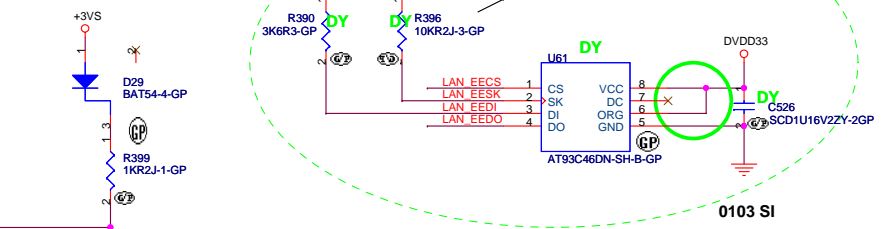
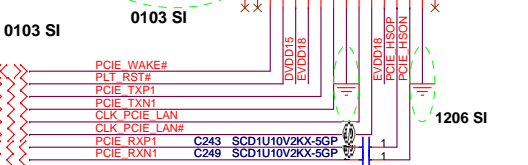
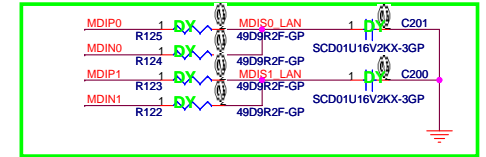


EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 AND GIGA CHIP)

R548 should be 2.49K 1% ohm for 8102E,
R548 should be 2K 1% for 8101E.



8101E use this circuit, 8102E dummy this circuit



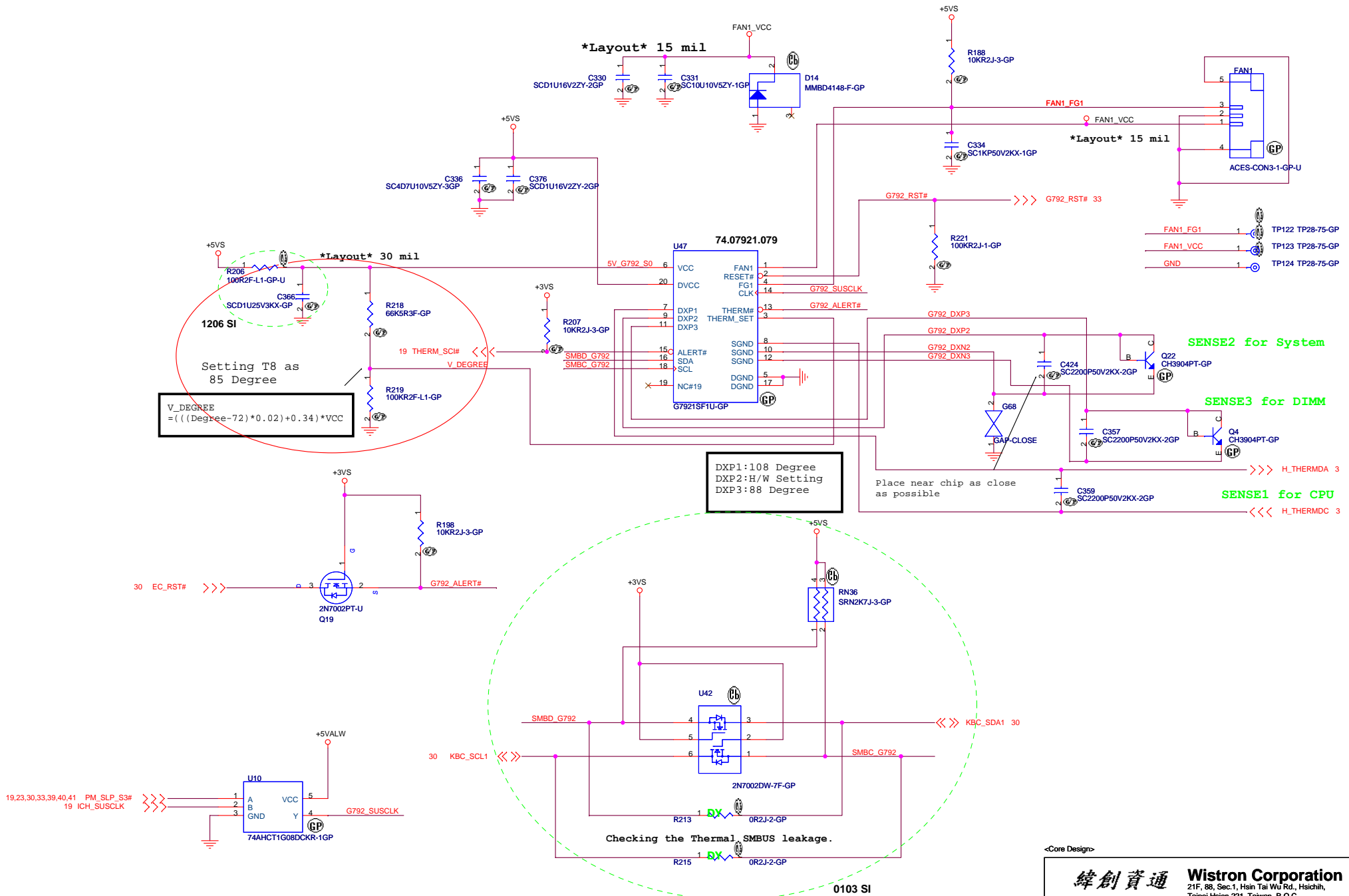
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8101E**

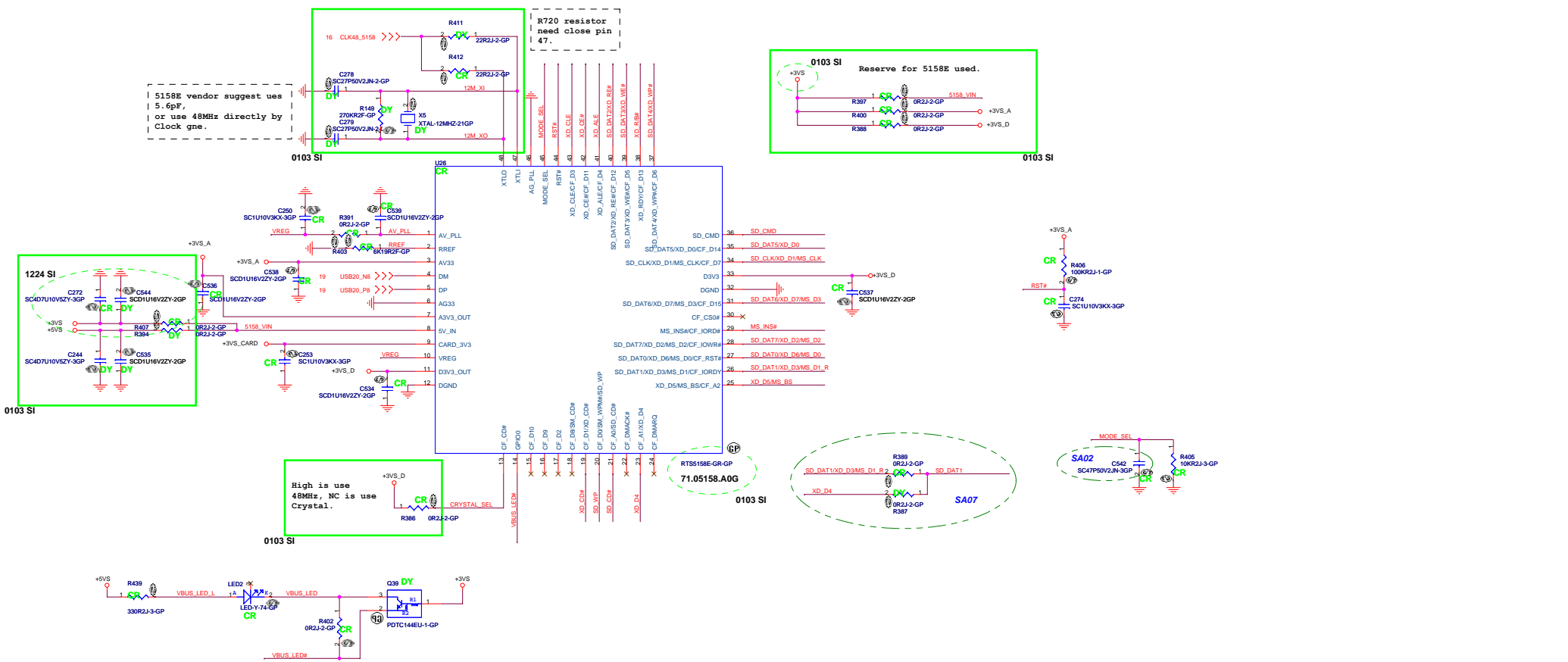
Size: A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet: 23 of 42

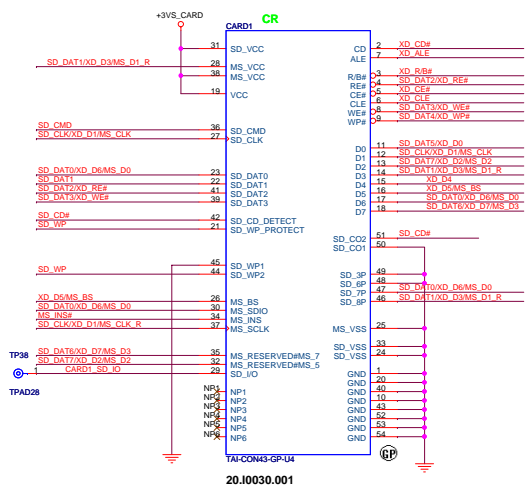
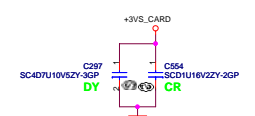
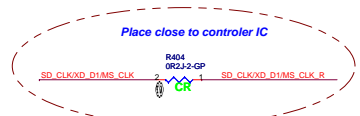


<Core Design>

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Title		
Thermal/Fan Controller		
Size	Document Number	Rev
Custom		SC
Date: Monday, January 07, 2008	Sheet 24 of 42	

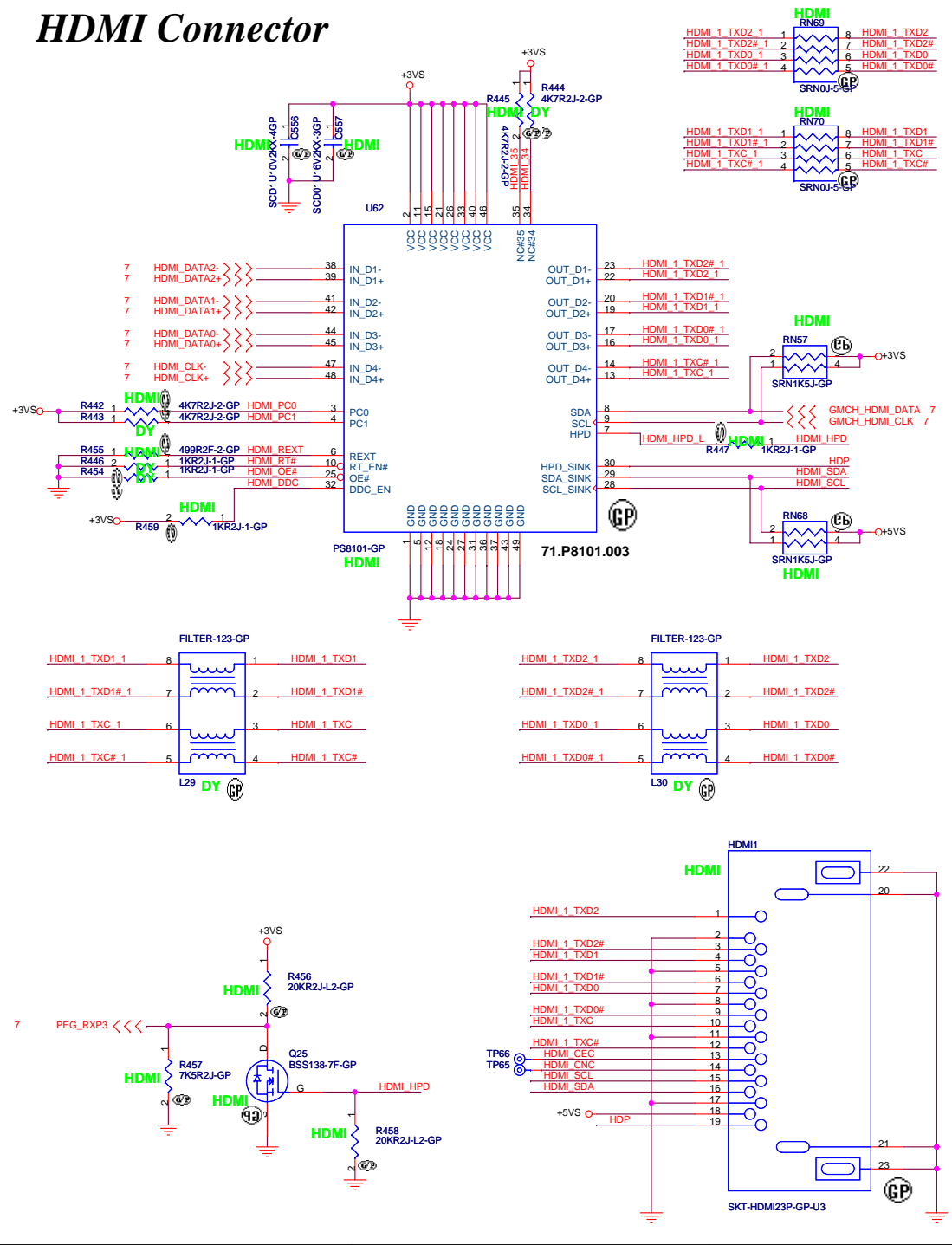


4 IN 1 CARD-READER (SD/SD IO/MMC/MMC.0/MS/MS PRO/XD)

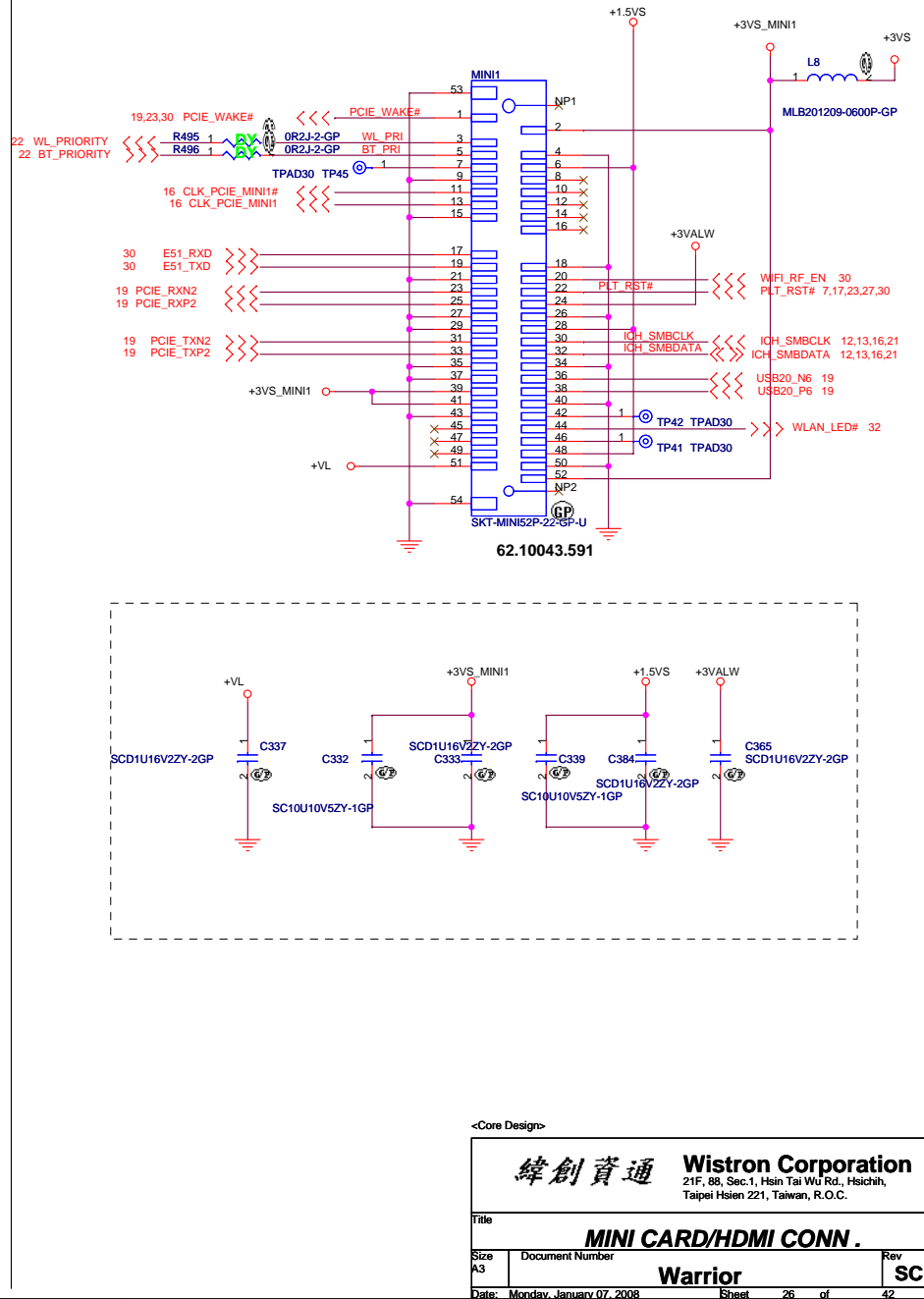


緯創資通 Wistron Corporation
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USB Card Reader Controller - RTS5158
 Date: Monday, January 07, 2008 Sheet 26 of 42

HDMI Connector



Mini Card Connector1(802.11a/b/g)

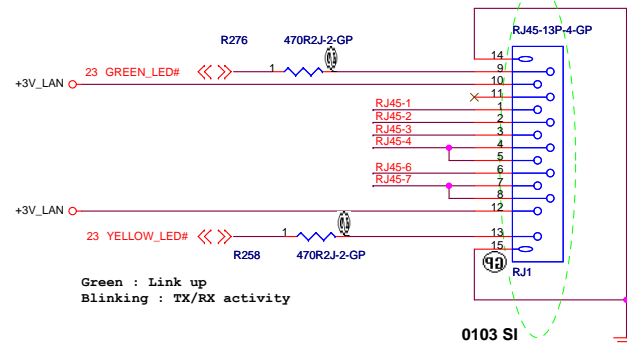
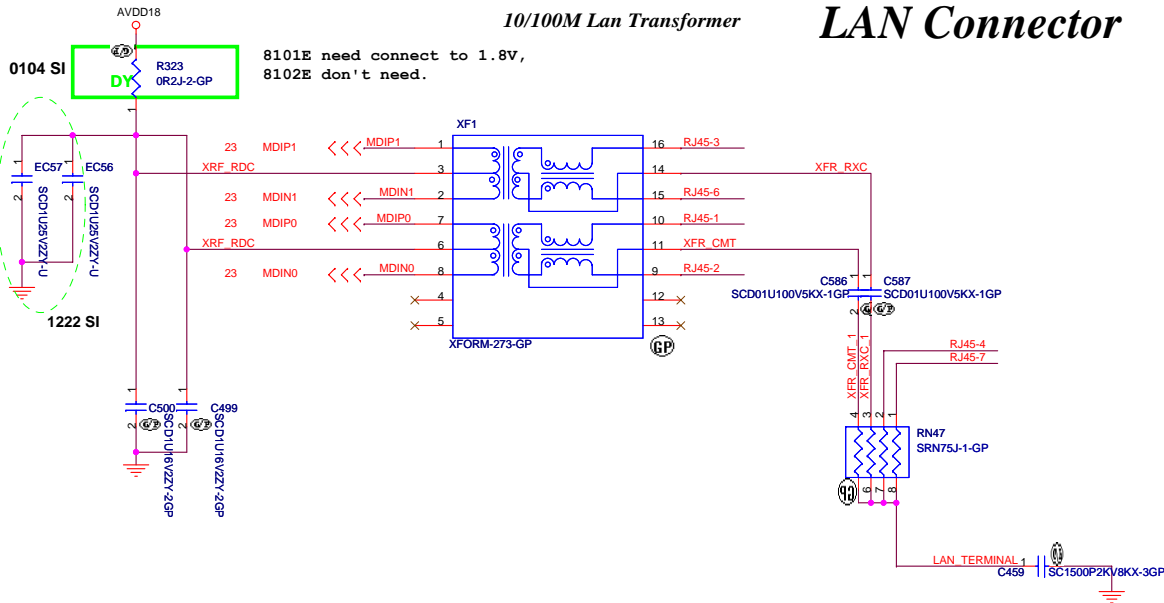


10/100M Lan Transformer

LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil across pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



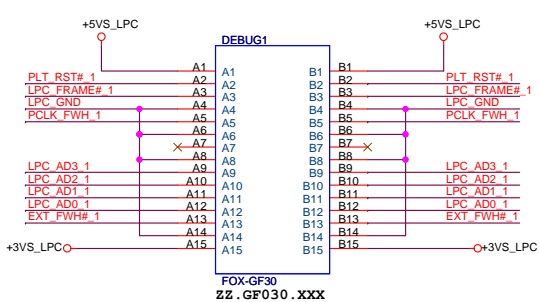
Remark:
Add trace width to 20mils for RJ1 pin4, 5 and pin 7, 8.

Golden Finger for Debug Board

TOP VIEW (A)

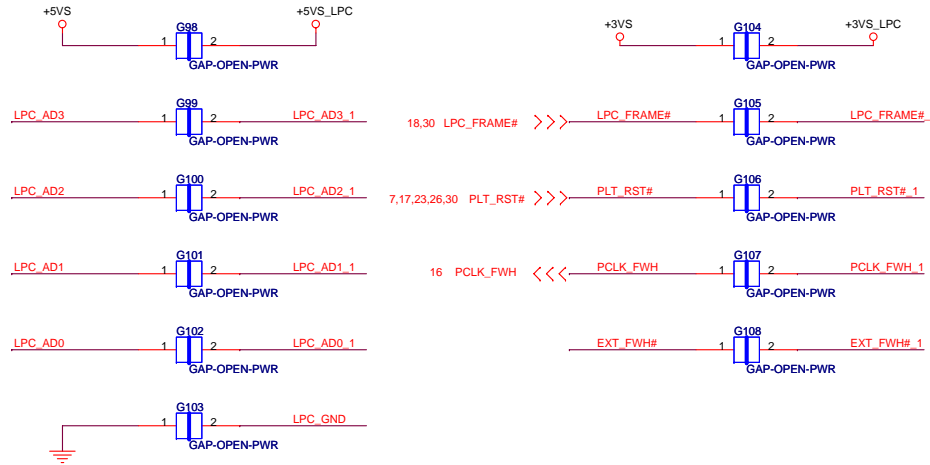
A15 (B1)
A14 (B2)
:
:
:
A2 (B14)
A1 (B15)

BOTTOM VIEW (B)



Please put near board edge.

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



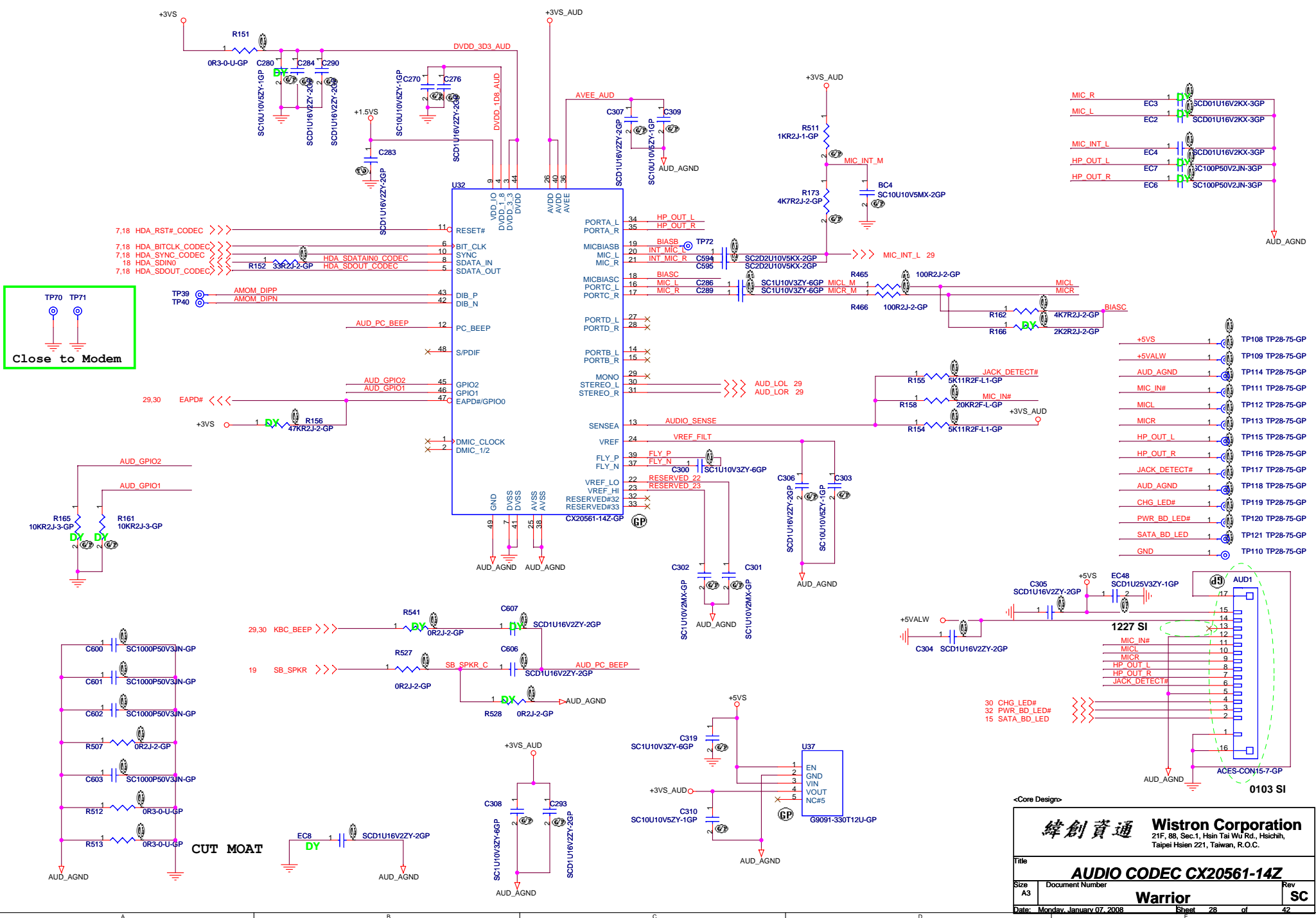
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21F, 88, Sec.1, Hsin Tai Wu Rd., Keelung,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN/Debug**

Size A3 Document Number **Warrior** Rev **SC**

Date: Monday, January 07, 2008 Page 27 of 42



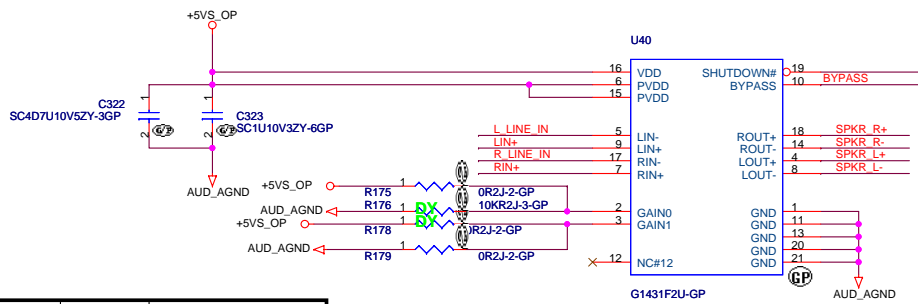
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 Taipei Hsien 221, Taiwan, R.O.C.

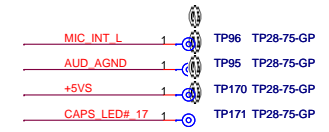
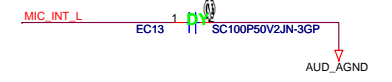
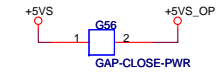
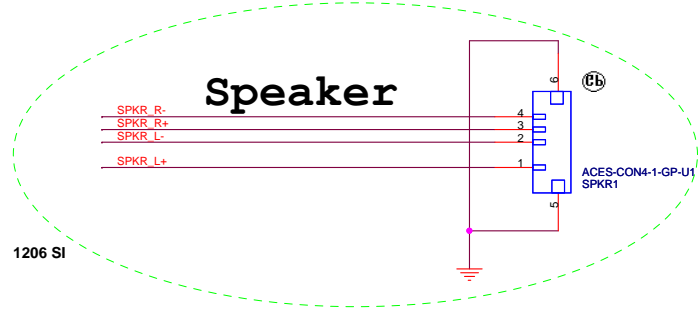
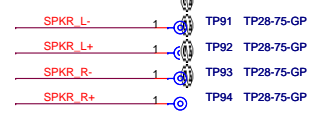
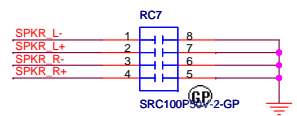
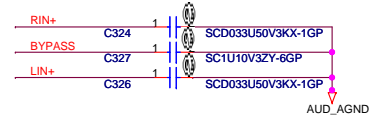
Title: **AUDIO CODEC CX20561-14Z**

Size A3 Document Number **Warrior** Rev **SC**

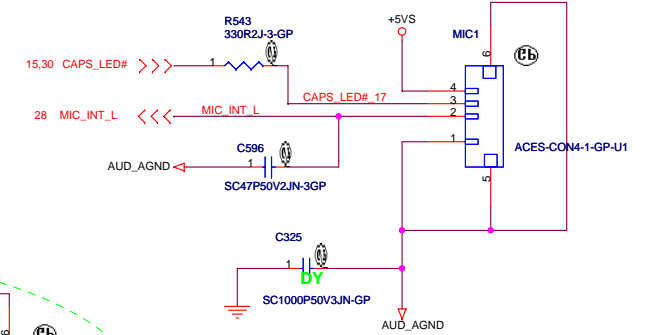
Date: Monday, January 07, 2008 Sheet 28 of 42



GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



MIC



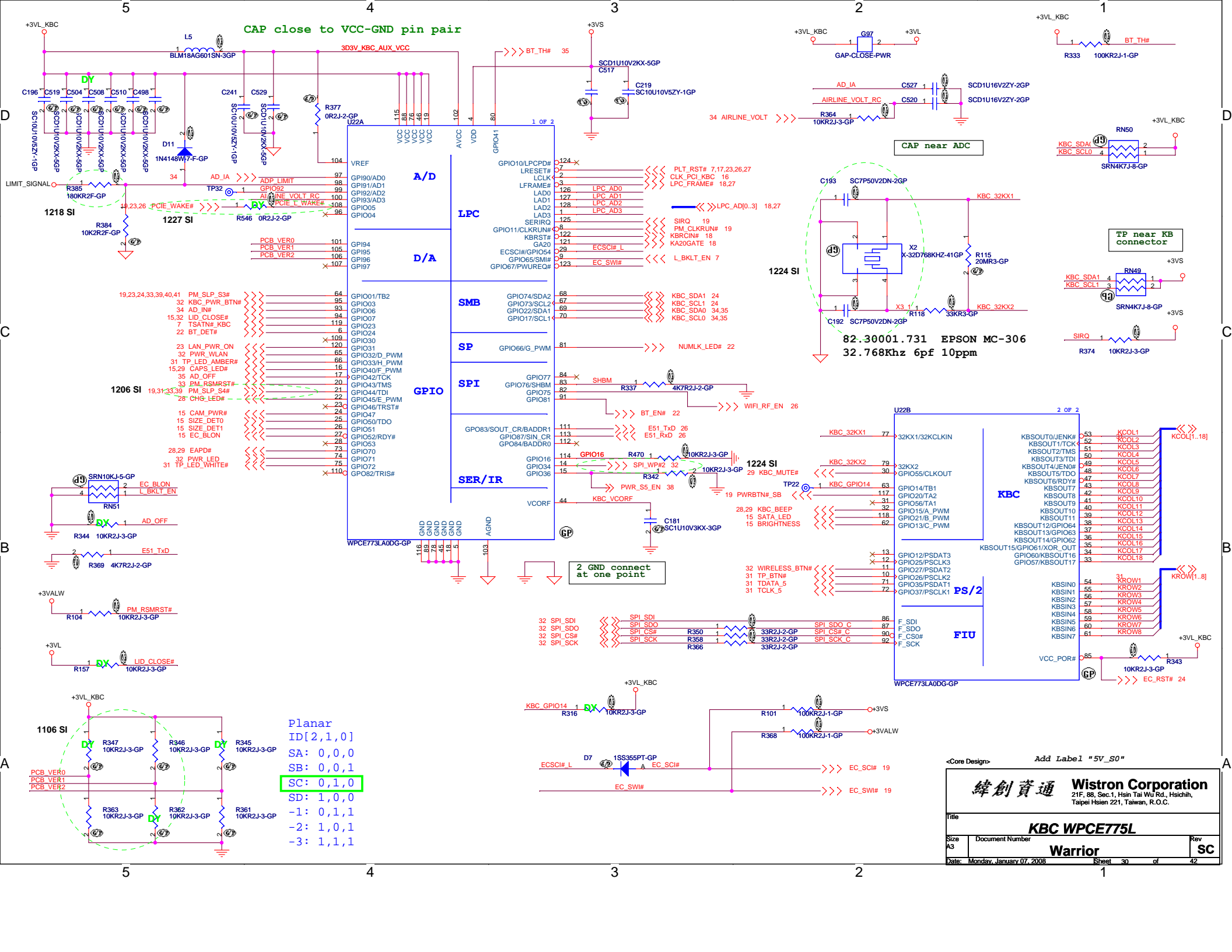
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/SPEAKER**

Size: A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Page: 29 of 42



CAP close to VCC-GND pin pair

CAP near ADC

2 GND connect at one point

Planar ID[2,1,0]

SA:	0,0,0
SB:	0,0,1
SC:	0,1,0
SD:	1,0,0
-1:	0,1,1
-2:	1,0,1
-3:	1,1,1

<Core Design> Add Label "5V_S0"

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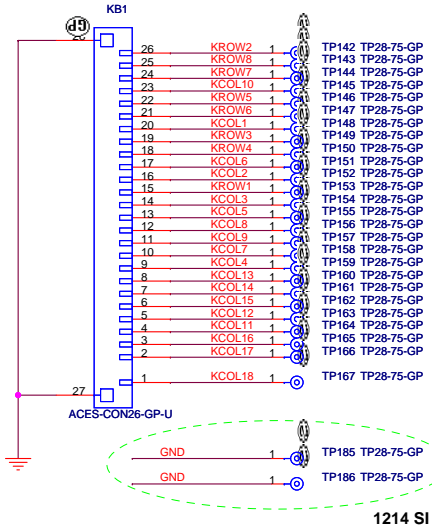
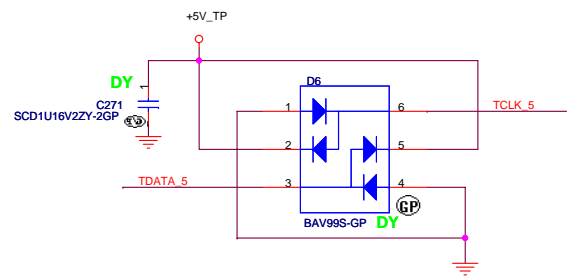
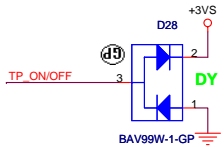
KBC WPCE775L		Rev
Size A3	Document Number	SC
Warrior		Sheet 30 of 42
Date: Monday, January 07, 2008		

Internal Keyboard Connector

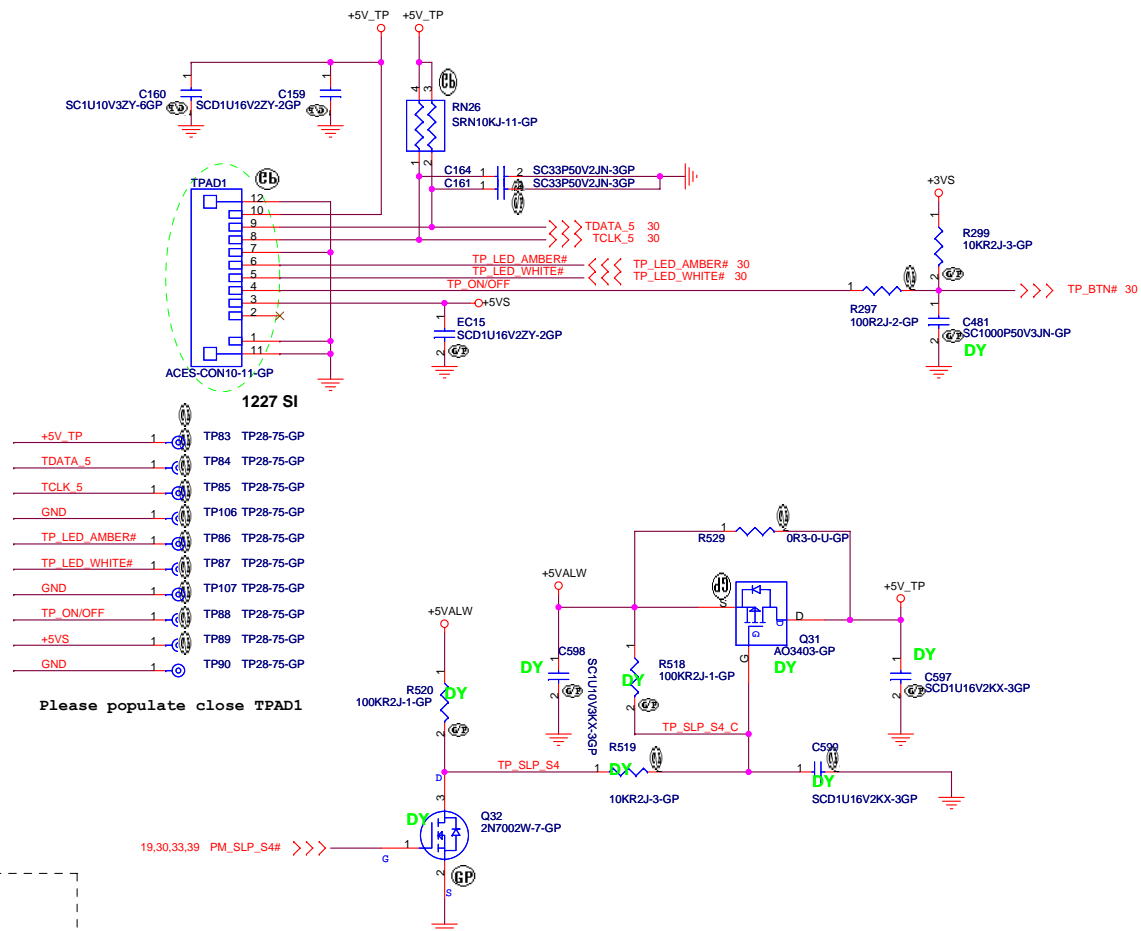
30 KROW[1..8] <<<< 
 30 KCOL[1..18] <<<< 

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

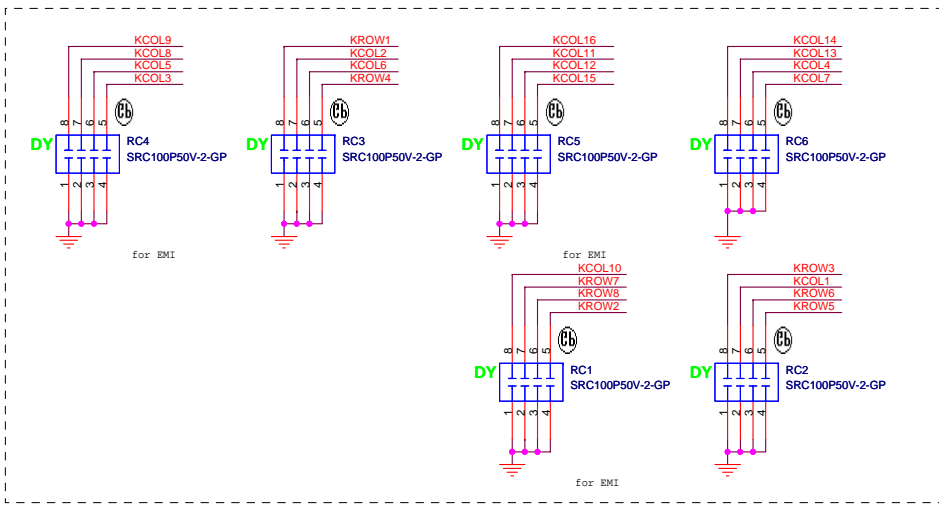


TouchPad Connector



- +5V_TP 1 TP83 TP28-75-GP
- TDATA_5 1 TP84 TP28-75-GP
- TCLK_5 1 TP85 TP28-75-GP
- GND 1 TP106 TP28-75-GP
- TP_LED_AMBER# 1 TP86 TP28-75-GP
- TP_LED_WHITE# 1 TP87 TP28-75-GP
- GND 1 TP107 TP28-75-GP
- TP_ON/OFF 1 TP88 TP28-75-GP
- +5V_S 1 TP89 TP28-75-GP
- GND 1 TP90 TP28-75-GP

Please populate close TPAD1



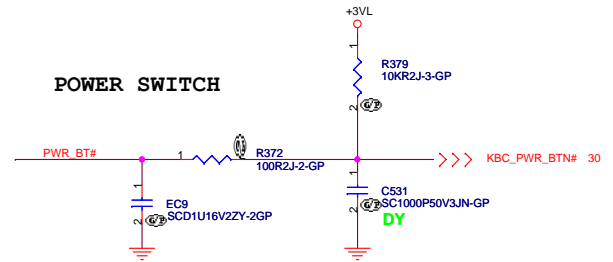
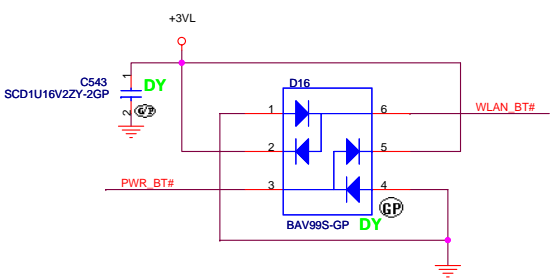
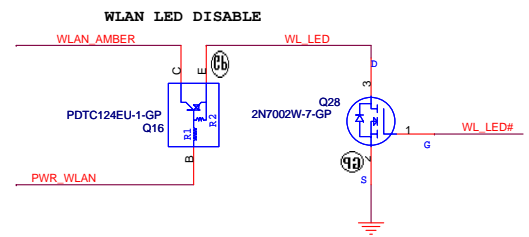
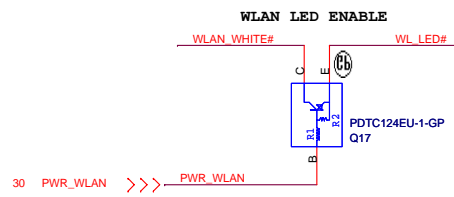
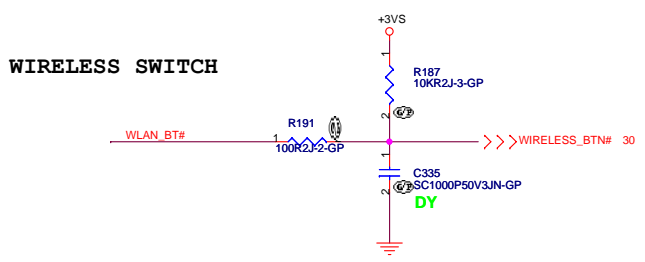
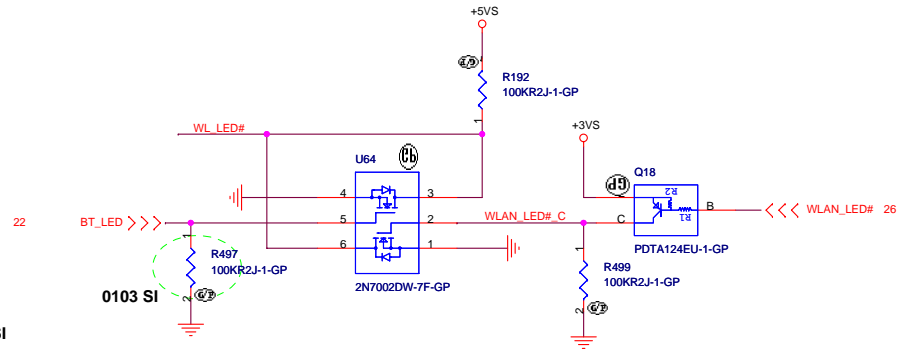
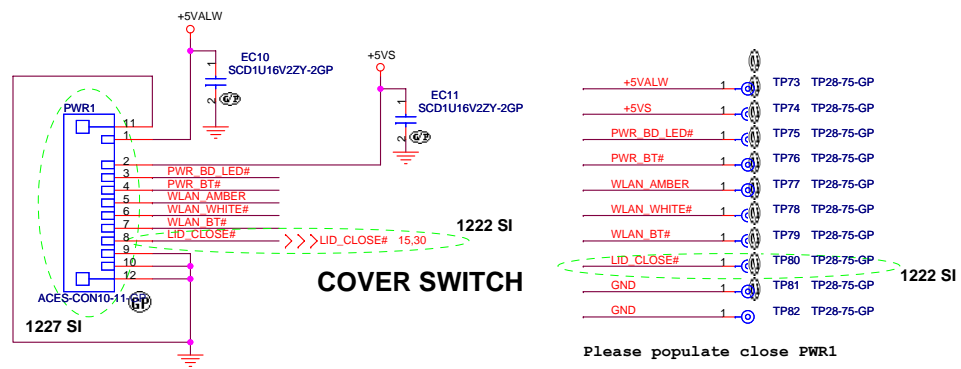
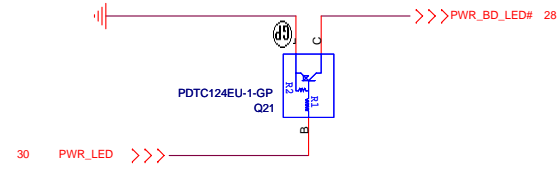
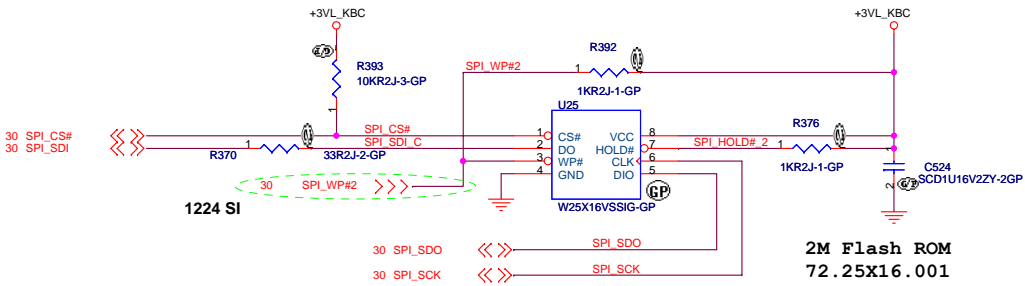
<Core Design>

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Title: **KeyBoard-CONN**

Size A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 39 of 42



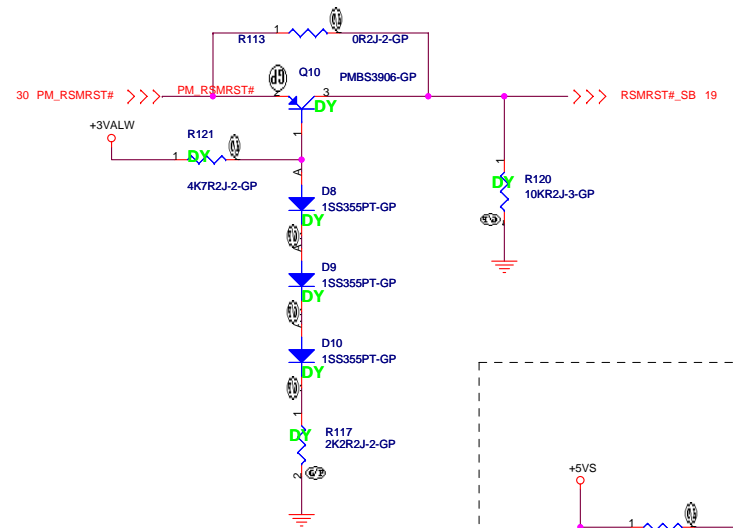
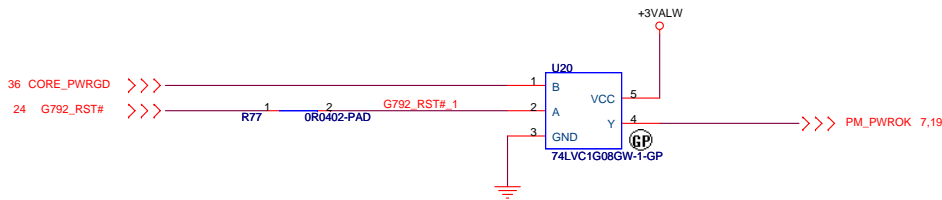
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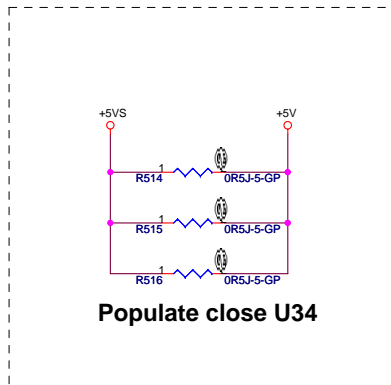
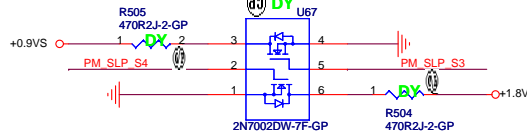
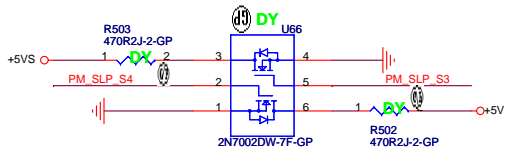
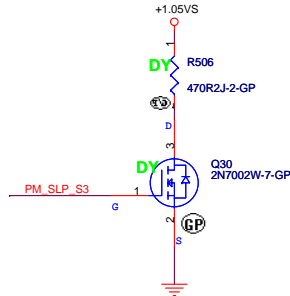
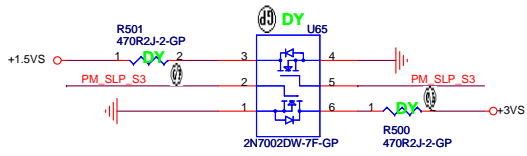
Title: **FWH and CONN.**

Size A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 32 of 42



Discharge Circuit

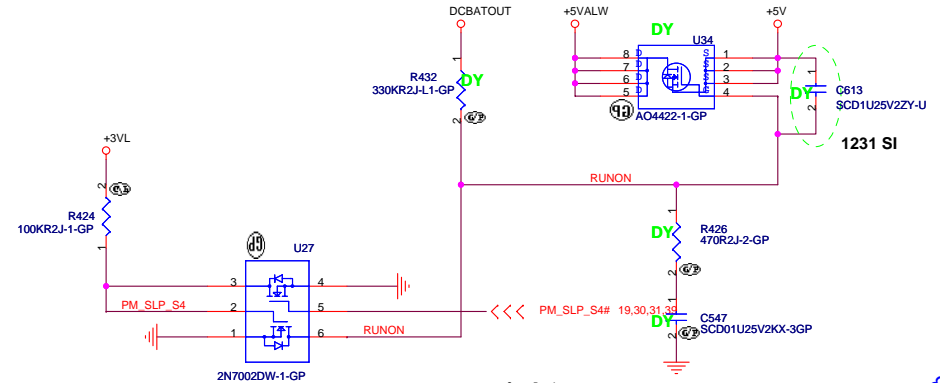
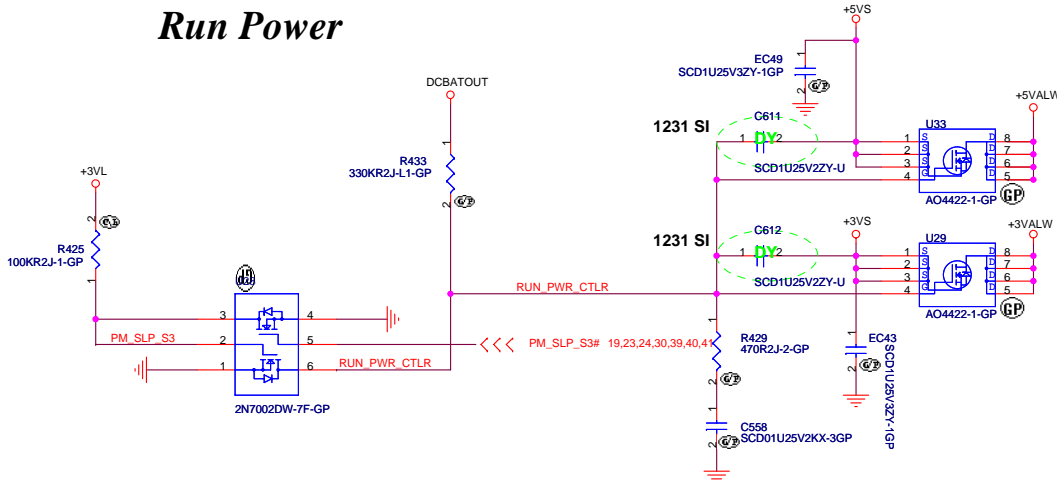


Populate close U34

+5VALW to +5VS Transfer +3VALW to +3VS Transfer

+5VALW to +5V Transfer

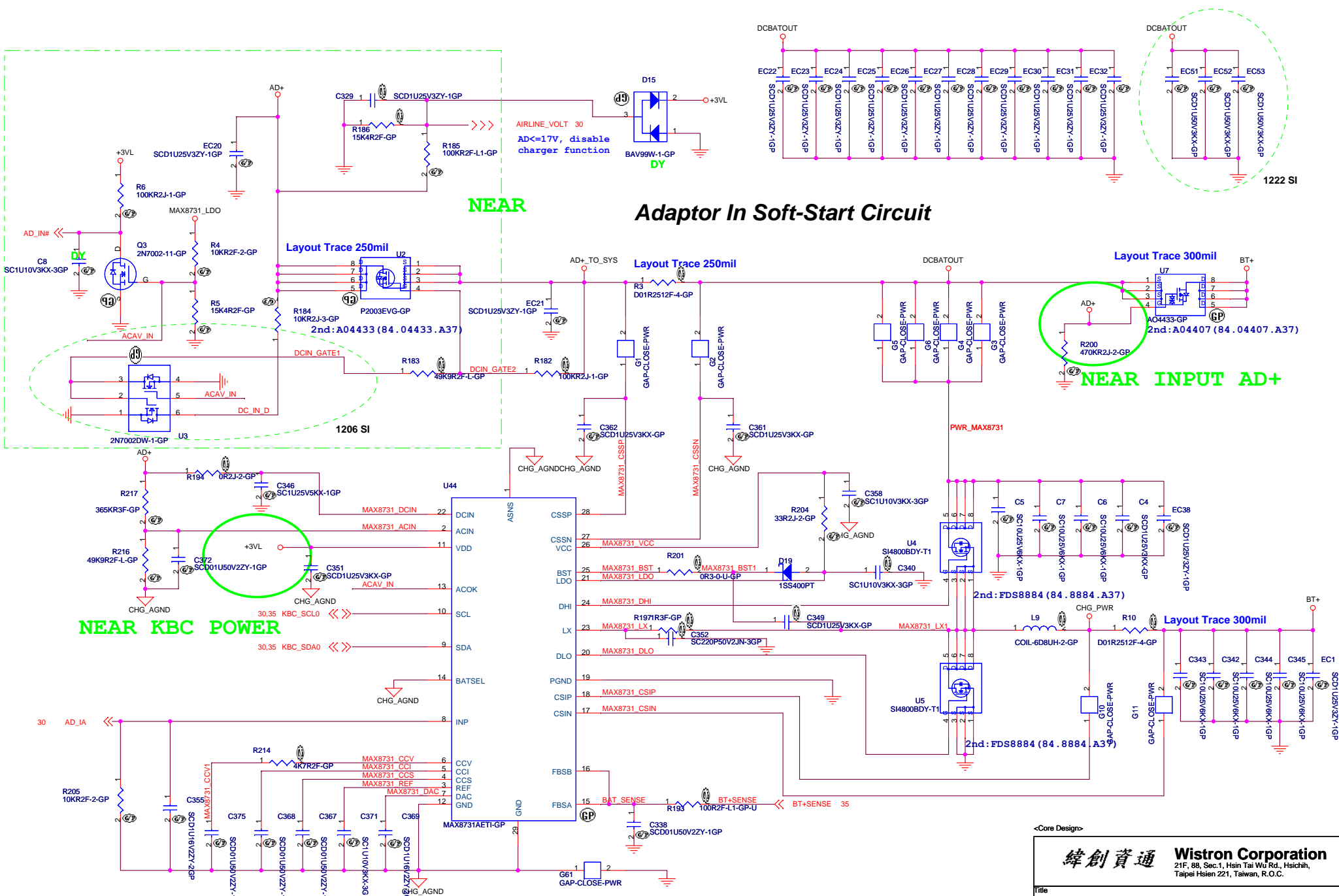
Run Power



<Core Design>

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 21F, 88, Sec.1, Hsin Tai Wu Rd, Neihu, Taipei Hsien 221, Taiwan, R.O.C.

Title	PWRPLANE	
Size	Document Number	Rev
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Date: Monday, January 07, 2008	Sheet 33 of 42	



Adaptor In Soft-Start Circuit

NEAR

NEAR INPUT AD+

NEAR KBC POWER

Need Check MAXIM Sming Use MAX8731 or MAX8731A

<Core Design>

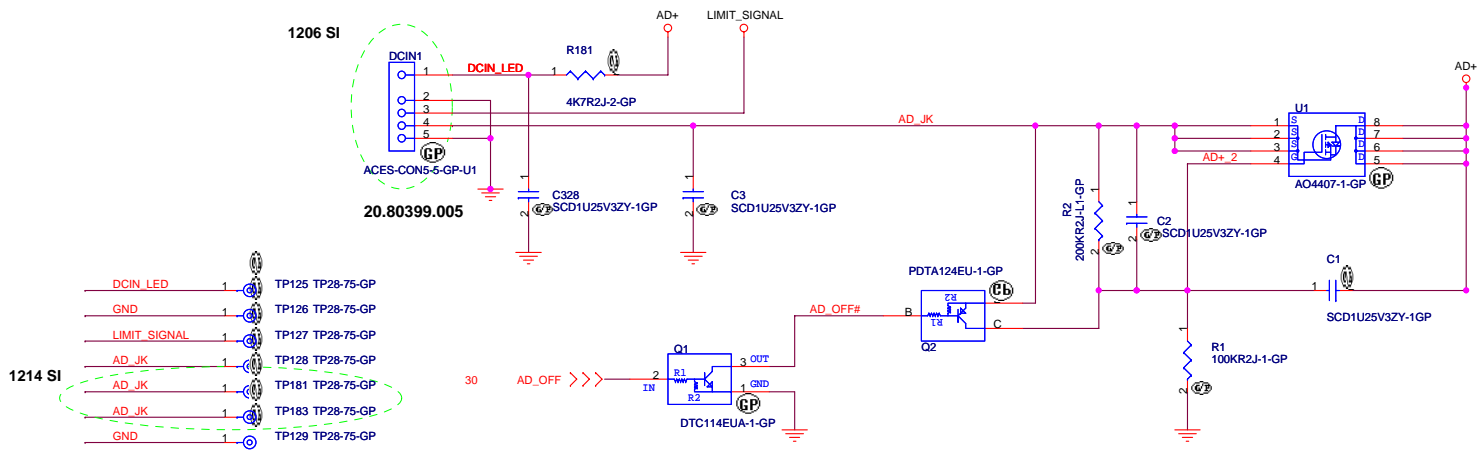
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731ETI**

Size: A3 Document Number: **Warrior** Rev: **SC**

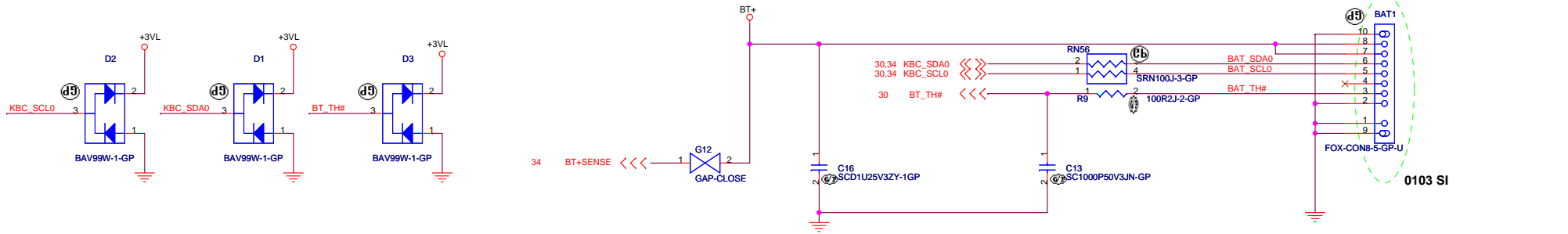
Date: Monday, January 07, 2008 Sheet 34 of 42

Adaptor in to generate DCBATOUT



- 1206 SI
- DCIN1 1
 - DCIN1 2
 - DCIN1 3
 - DCIN1 4
 - DCIN1 5
- ACES-CON5-5-GP-U1
- 20.80399.005
- 1214 SI
- DCIN_LED 1 TP125 TP28-75-GP
 - GND 1 TP126 TP28-75-GP
 - LIMIT_SIGNAL 1 TP127 TP28-75-GP
 - AD_JK 1 TP128 TP28-75-GP
 - AD_JK 1 TP181 TP28-75-GP
 - AD_JK 1 TP183 TP28-75-GP
 - GND 1 TP129 TP28-75-GP

BATTERY CONNECTOR



- 0103 SI
- BAT1 10
 - BAT1 8
 - BAT1 7
 - BAT1 6
 - BAT1 5
 - BAT1 4
 - BAT1 3
 - BAT1 2
 - BAT1 1
 - BAT1 9
- FOX-CON8-5-GP-U
- 1214 SI
- BT+ 1 TP182 TP28-75-GP
 - BT+ 1 TP130 TP28-75-GP
 - BT+ 1 TP131 TP28-75-GP
 - GND 1 TP132 TP28-75-GP
 - GND 1 TP133 TP28-75-GP
 - BAT_SDA0 1 TP134 TP28-75-GP
 - BAT_SCL0 1 TP135 TP28-75-GP
 - BAT_TH# 1 TP136 TP28-75-GP
 - GND 1 TP137 TP28-75-GP

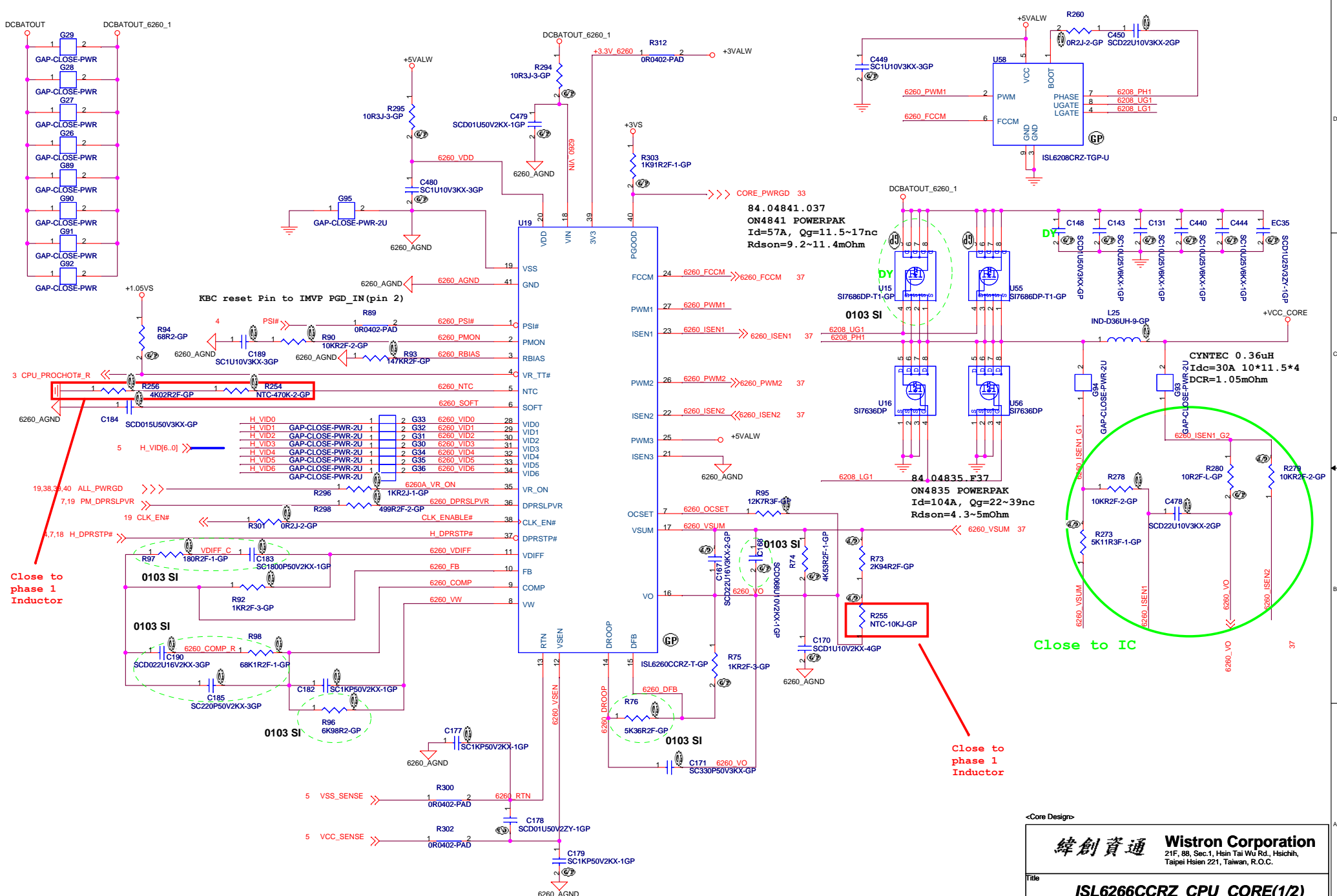
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Keelung, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size: A3 Document Number: **Warrior** Rev: **SC**

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Close to phase 1 Inductor

Close to IC

Close to phase 1 Inductor

<Core Design>

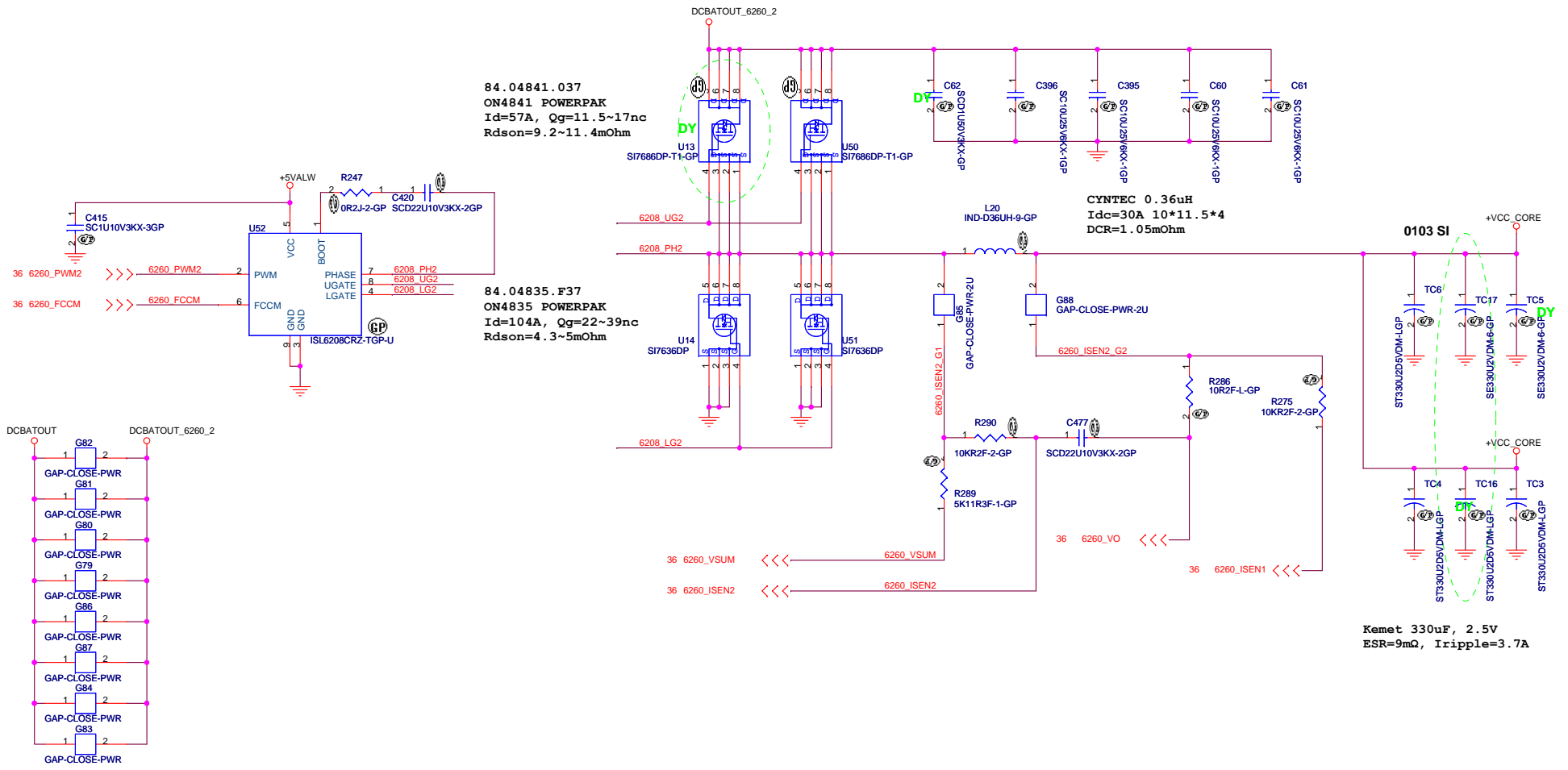
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6266CCRZ CPU CORE(1/2)**

Size A3 Document Number Rev

Warrior SC

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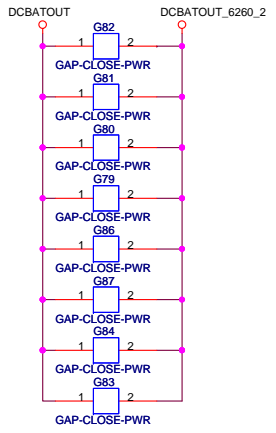
84.04841.037
ON4841 POWERPAK
 Id=57A, Qg=11.5~17nc
 Rdson=9.2~11.4mOhm

84.04835.F37
ON4835 POWERPAK
 Id=104A, Qg=22~39nc
 Rdson=4.3~5mOhm

CYNTEC 0.36uH
 Idc=30A 10*11.5*4
 DCR=1.05mOhm

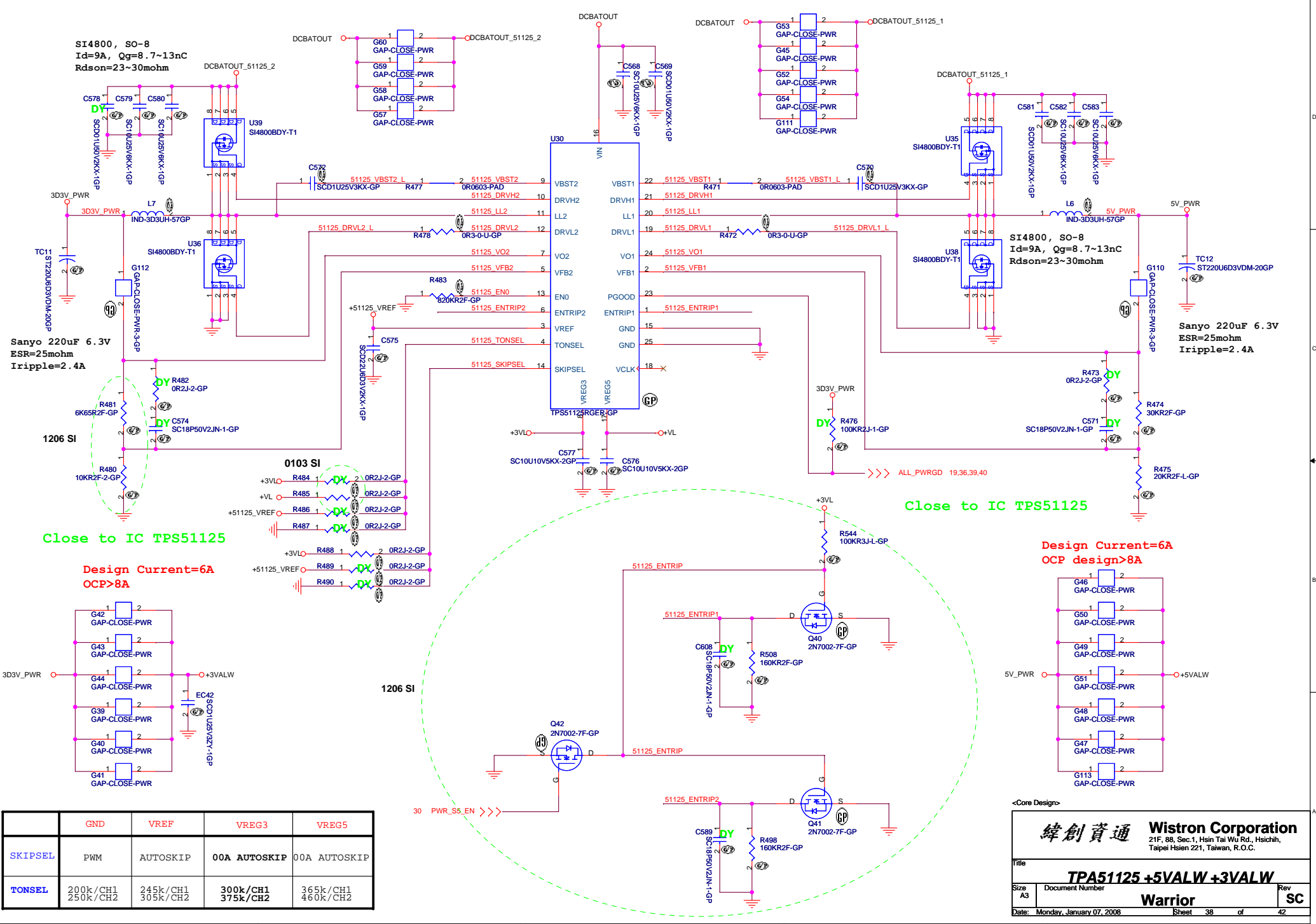
0103 SI

Kemet 330uF, 2.5V
 ESR=9mΩ, Iripple=3.7A



<Core Design>

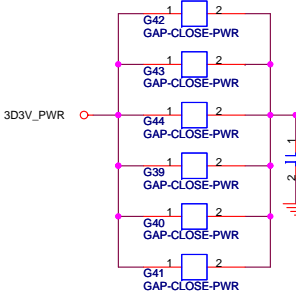
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title ISL6260CCRZ CPU CORE(2/2)	
Size A3	Document Number Warrior
Date Monday, January 07, 2008	Rev SC
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SI4800, SO-8
 Id=9A, Qg=8.7~13nC
 Rdson=23~30mohm

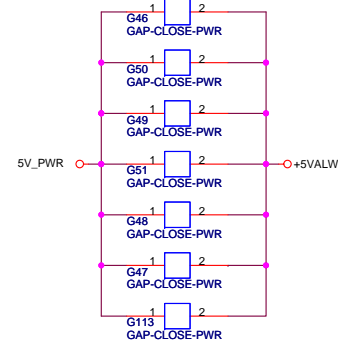
Sanyo 220uF 6.3V
 ESR=25mohm
 Iripple=2.4A

Design Current=6A
 OCP>8A



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Design Current=6A
 OCP design>8A



<Core Design>

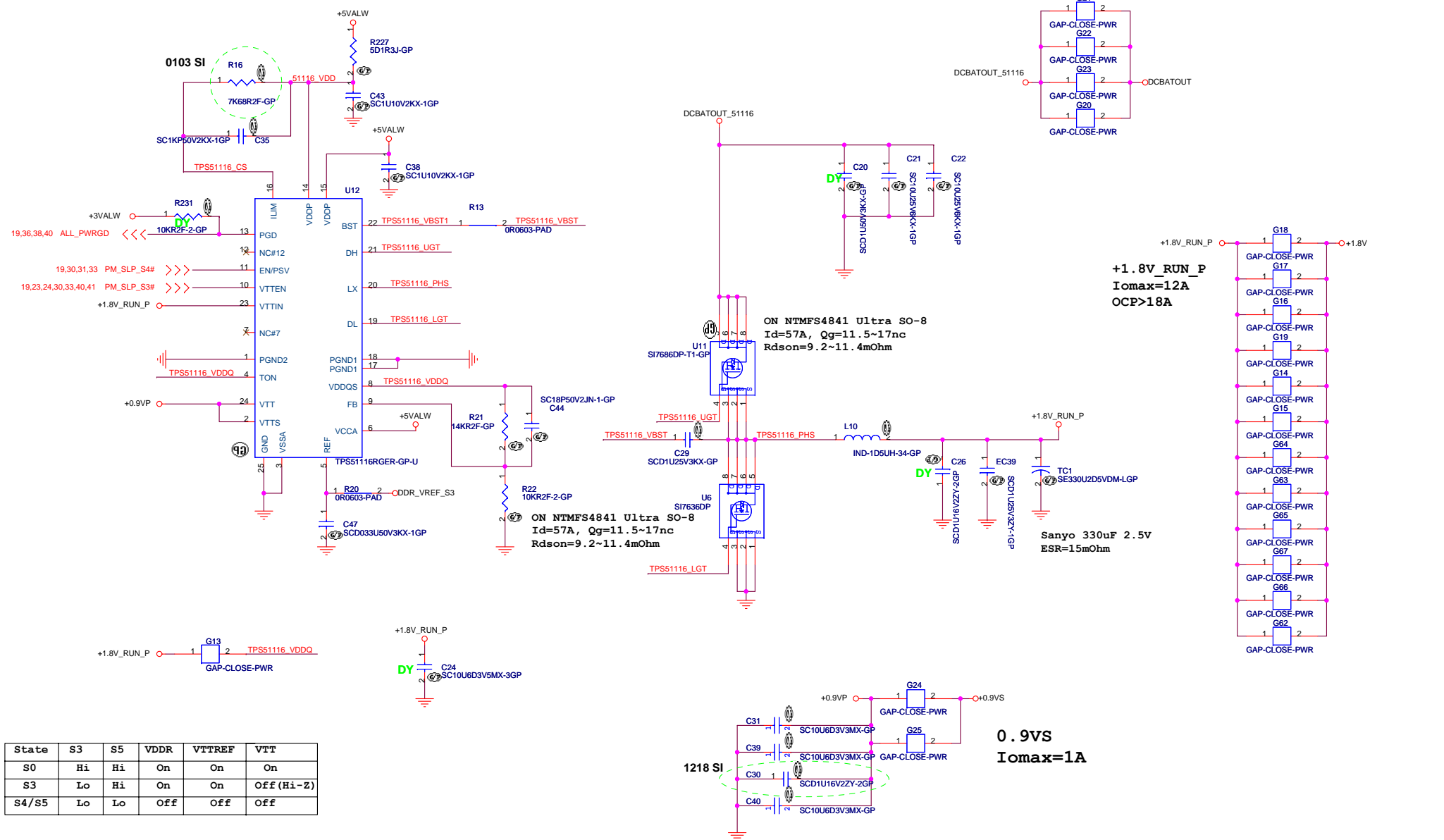
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPA51125 +5VALW +3VALW**

Size A3 Document Number **Warrior** Rev **SC**

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TI TPS51116 for 1D8V and 0D9V



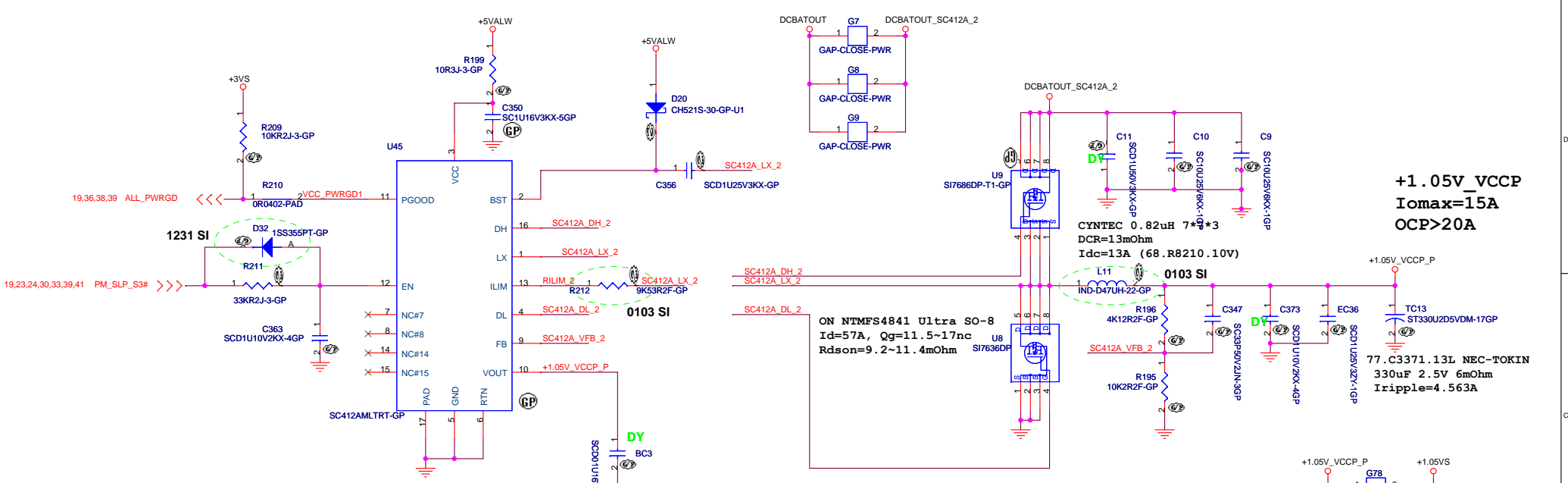
<Core Design>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 1D8V/0D9V**

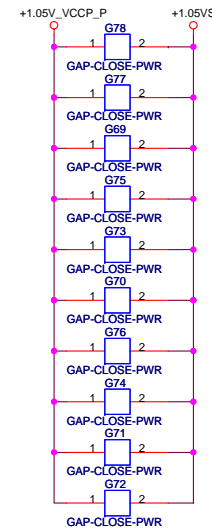
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+1.05V_VCCP
I_{omax}=15A
OCP>20A

Close to IC SC412A



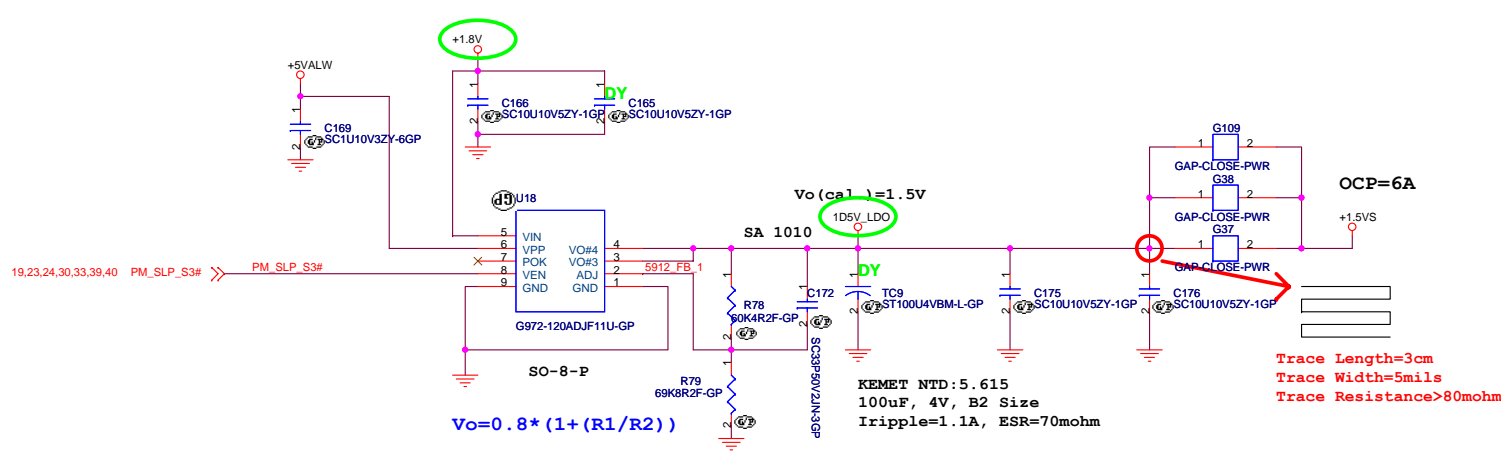
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SC412A +1.05VS**

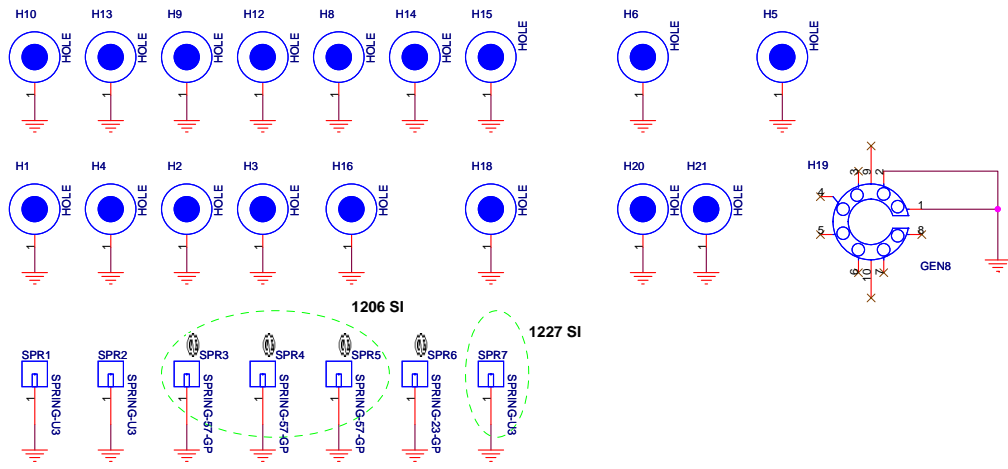
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<Core Design>

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GMT 1D5V LDO			
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SPR1-2: 34.40U07.001
SPR3-5: 34.42T14.002
SPR6 : 34.39S07.003
SPR7 : 34.40U07.001

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MISC
Size A3	Document Number Warrior
Date: Monday, January 07, 2008	Rev SC