

2010.04.07 MV Schematic

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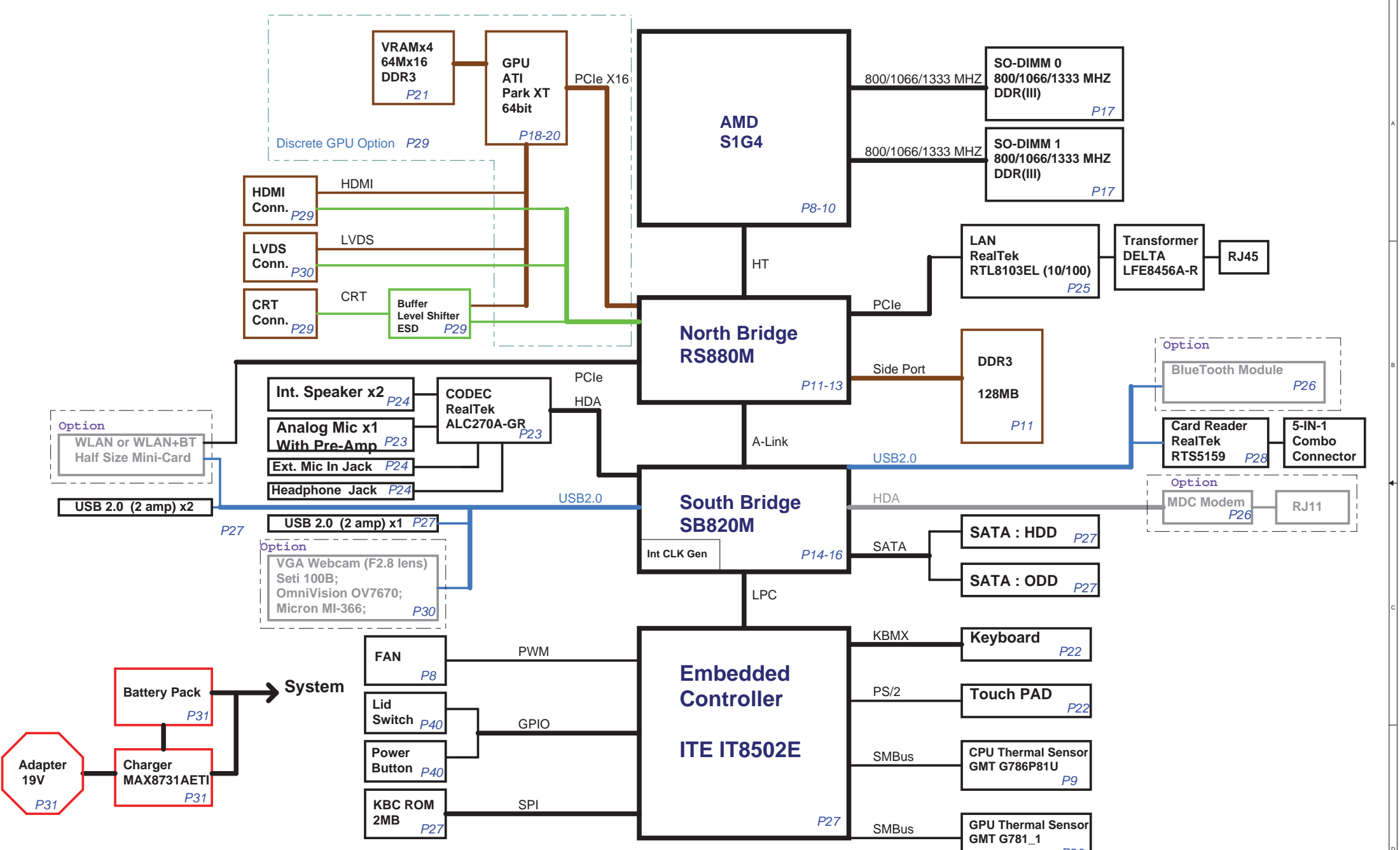
Daughter Board

P40 -- Power Board / USB Board / SW Board

P. Leader	Check by	Design by

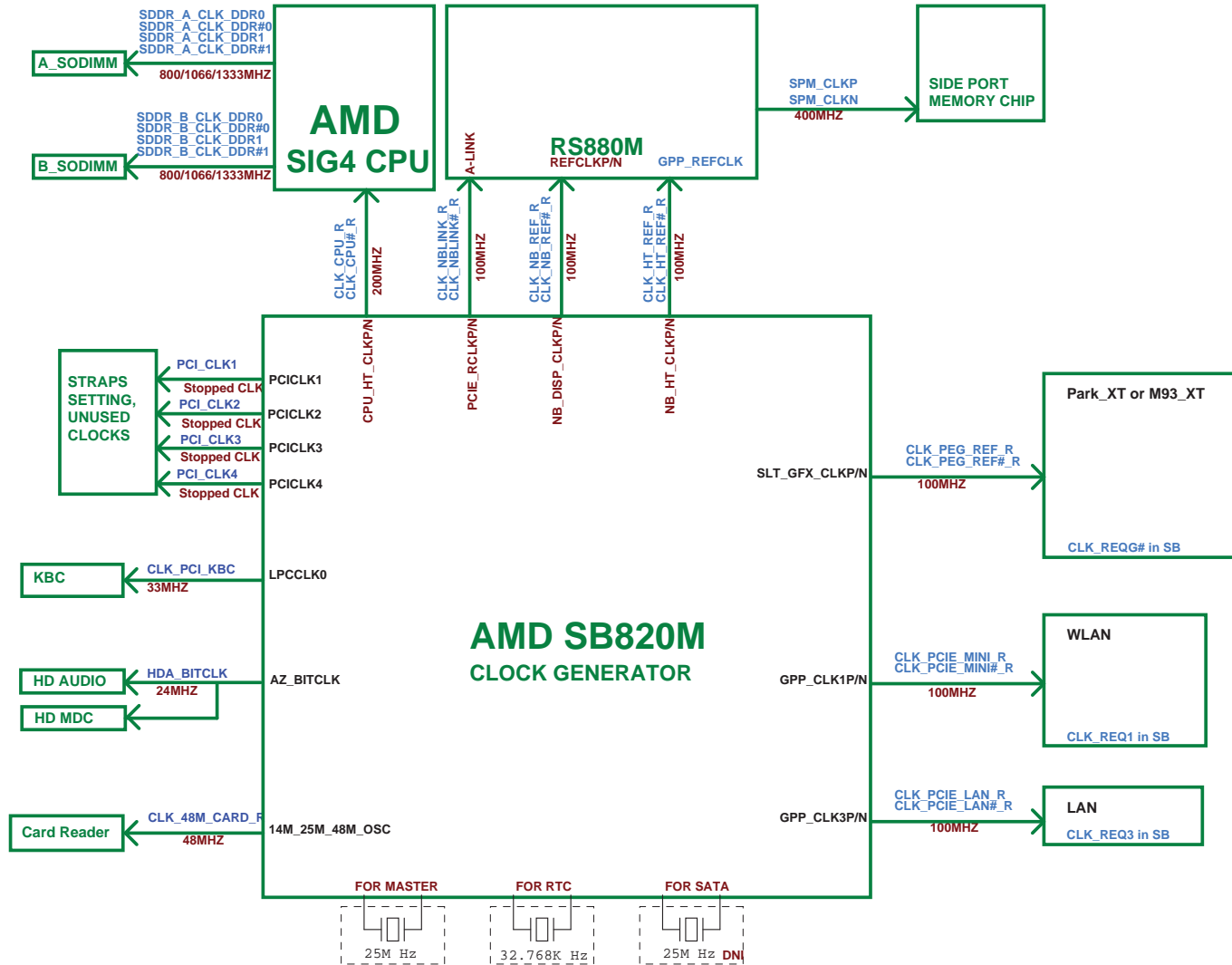
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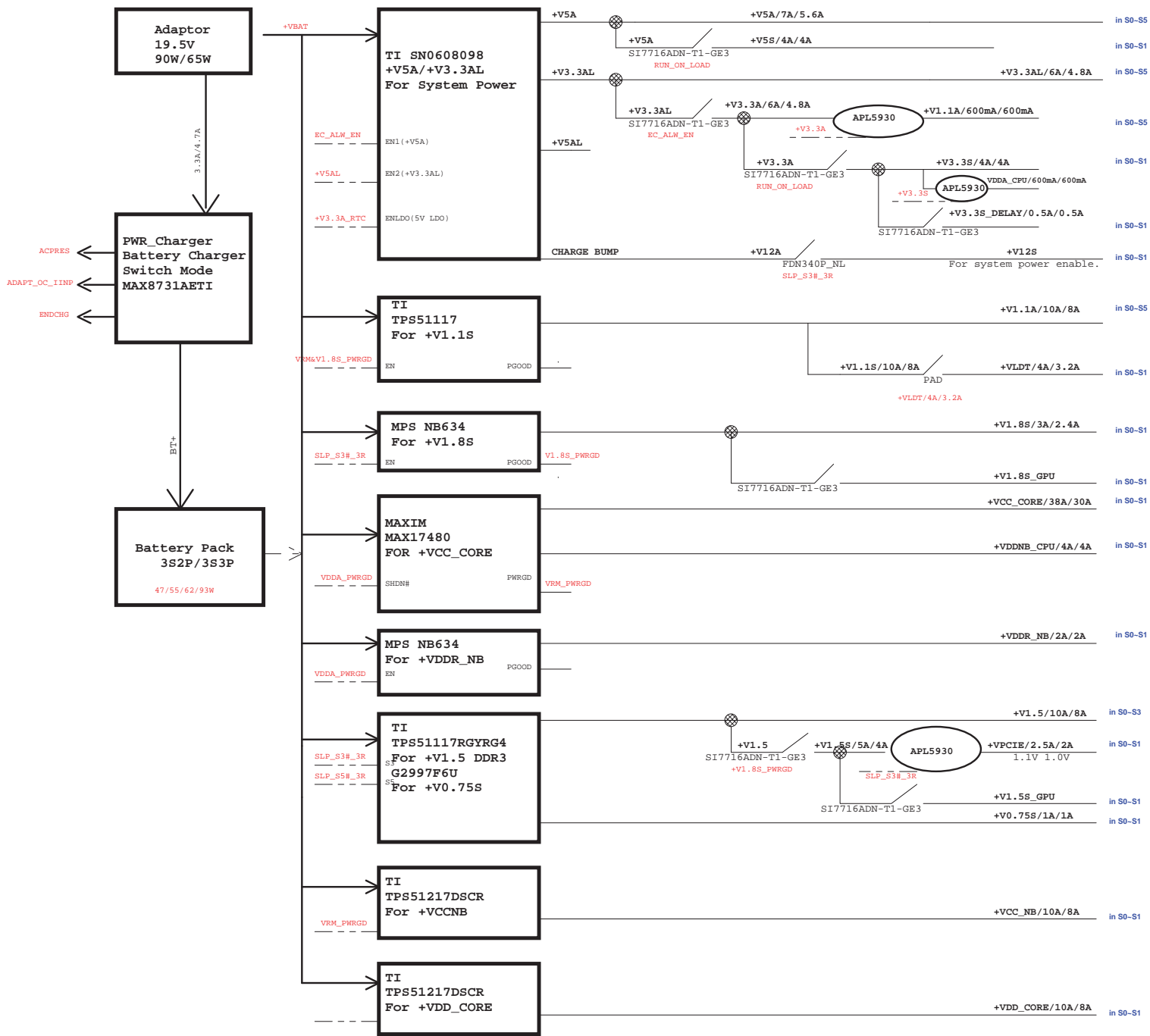


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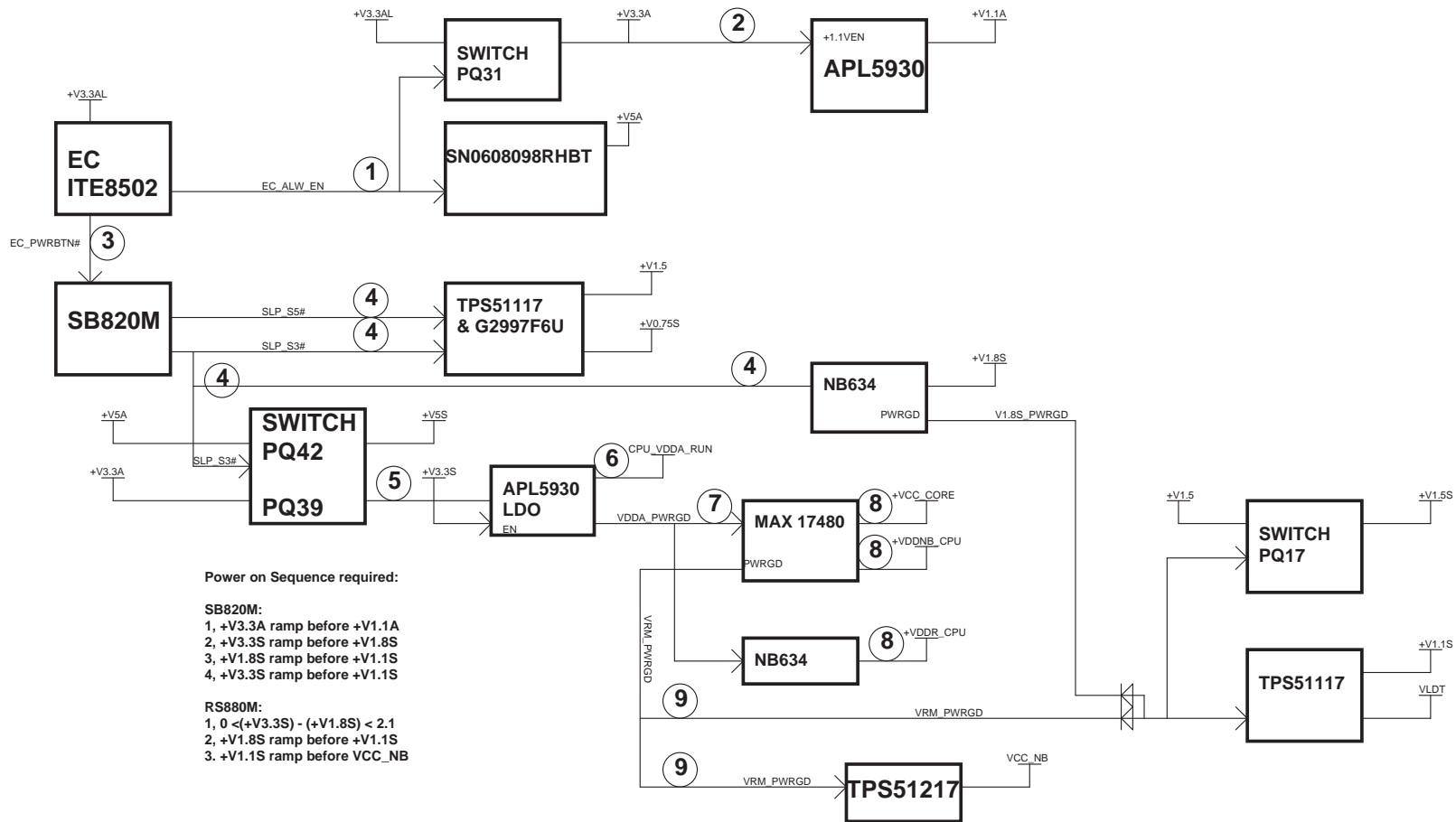
INTERNAL CLOCK MODE

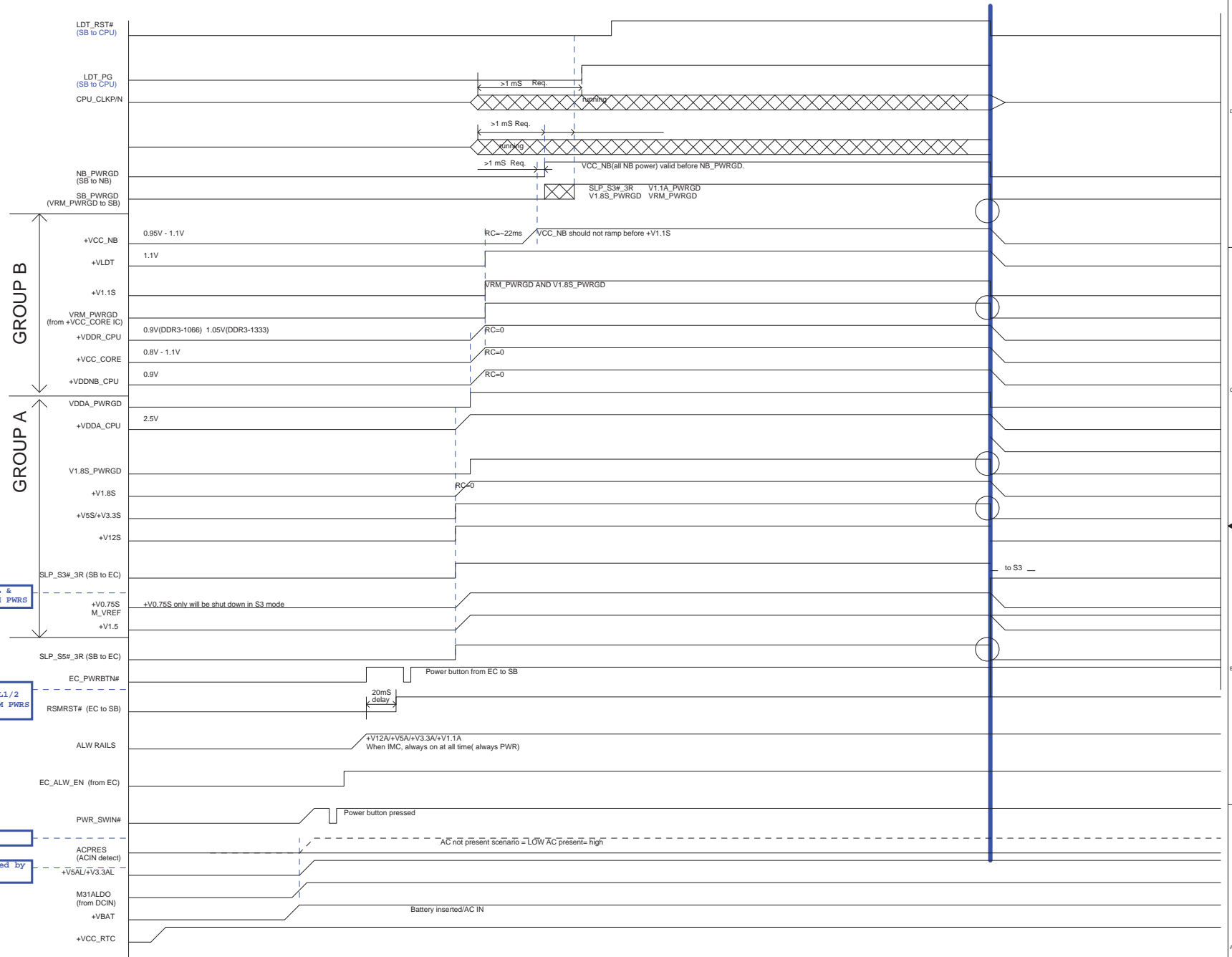


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GROUP B

GROUP A

CPU MEM CTL & DDR3 SODIMM PWRS

CPU_THM/SB/SB_SCL1/2 SB_KB/SPI/LPC ROM PWRS

KBC is ready

KBC is powered by +V3.3AL

Power on Sequence required:

SB820:

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

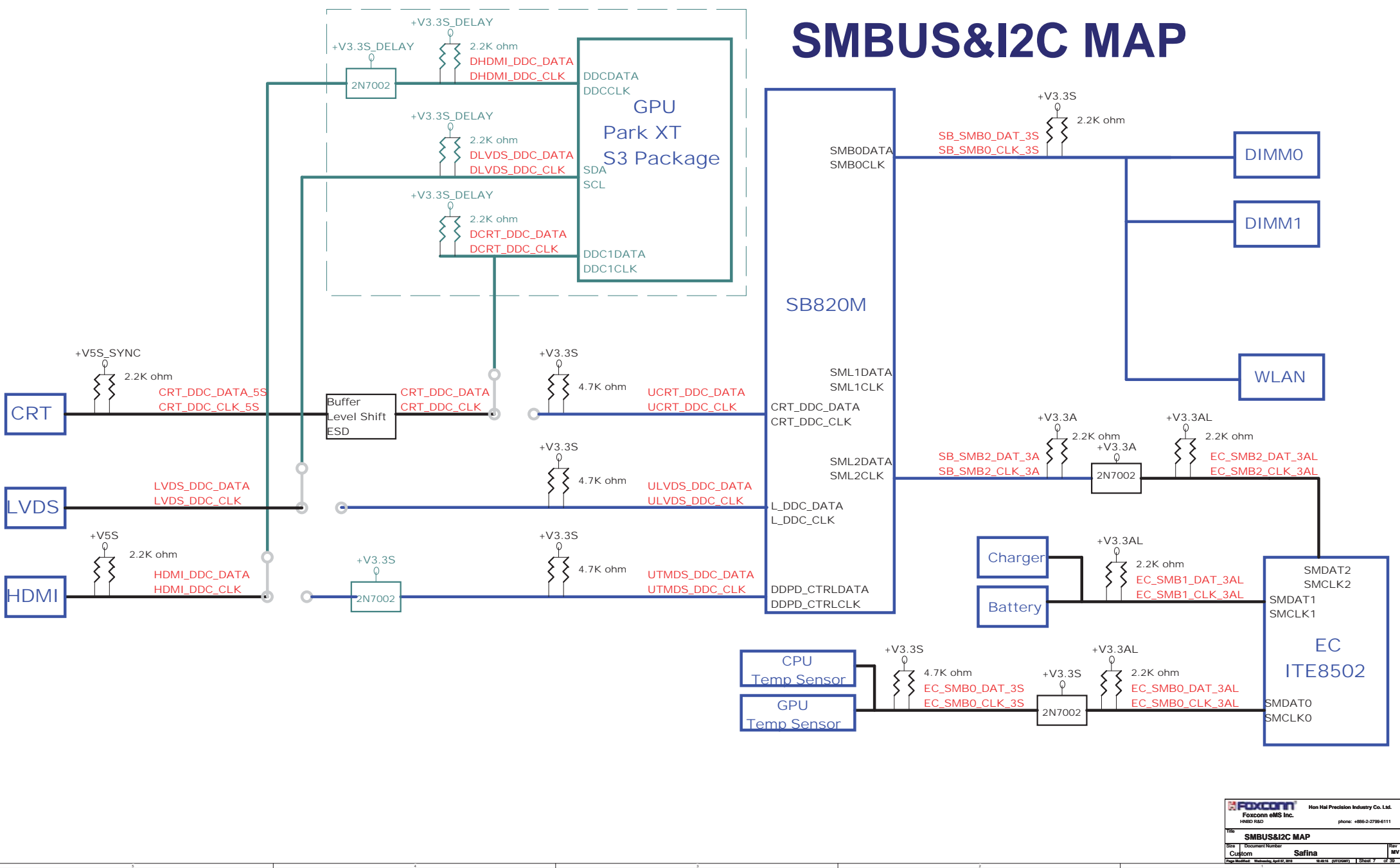
RS880M:

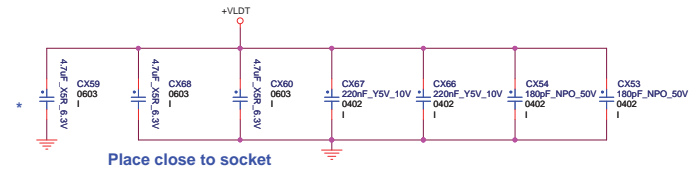
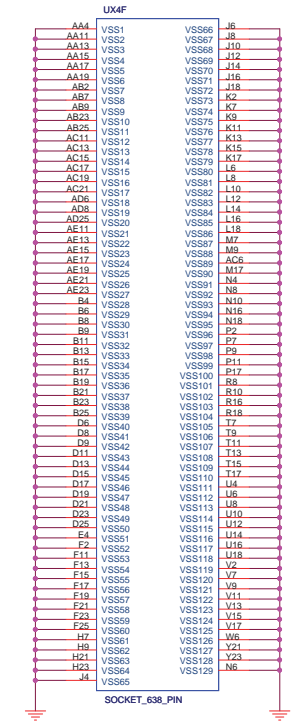
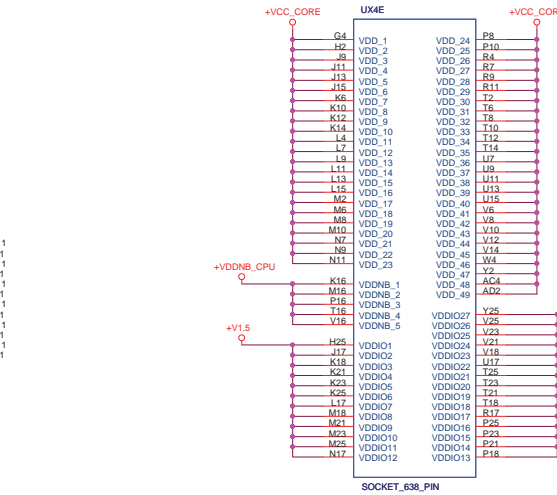
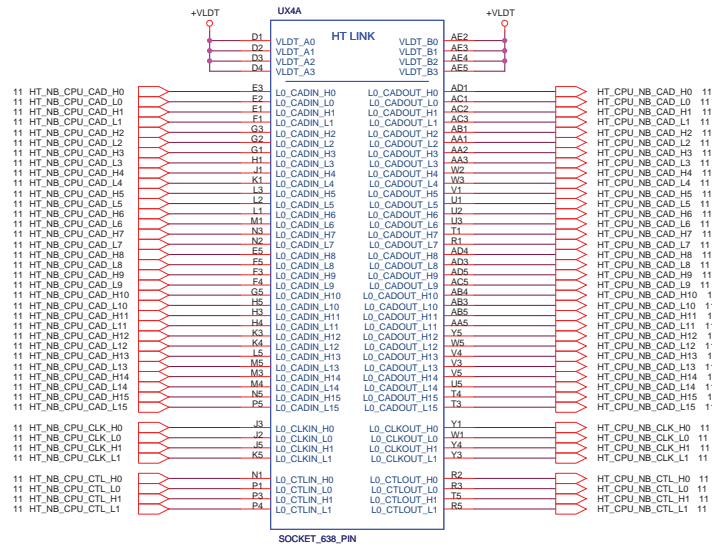
- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC_NB

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		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNSD R&D	
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Title: POWER SEQUENCY TIMING			
Size:	Document Number:	Rev:	MV
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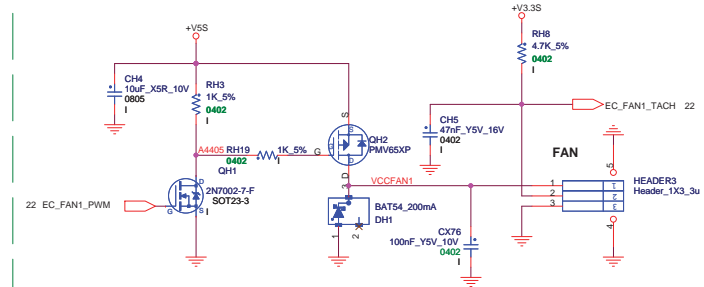
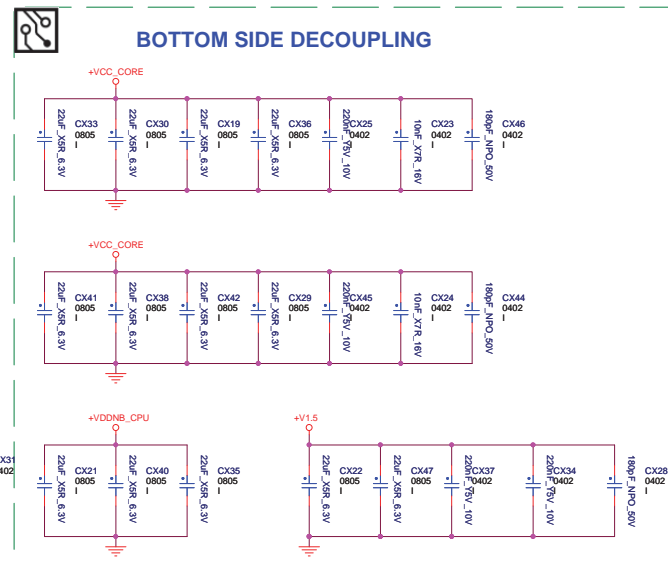
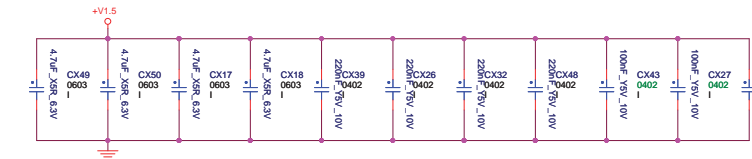
SMBUS&I2C MAP





* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE

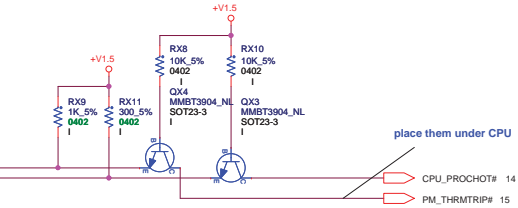
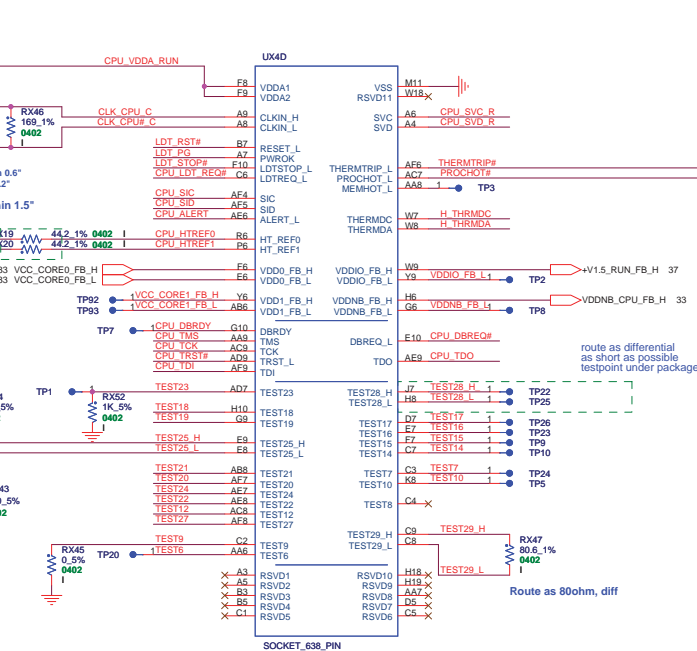
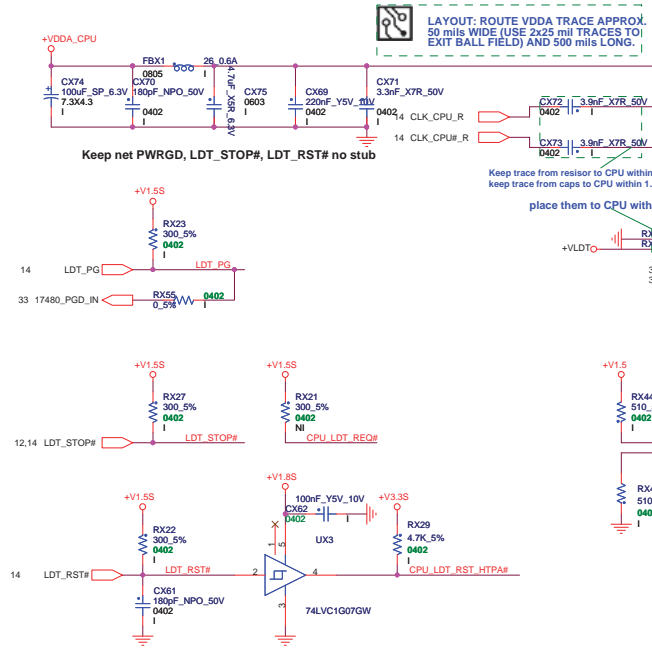


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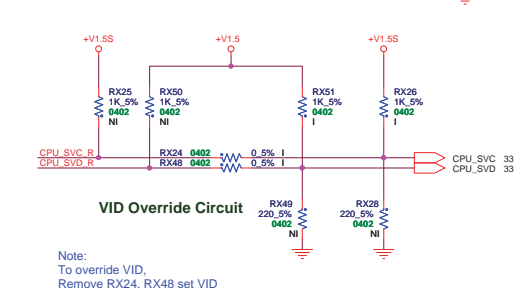
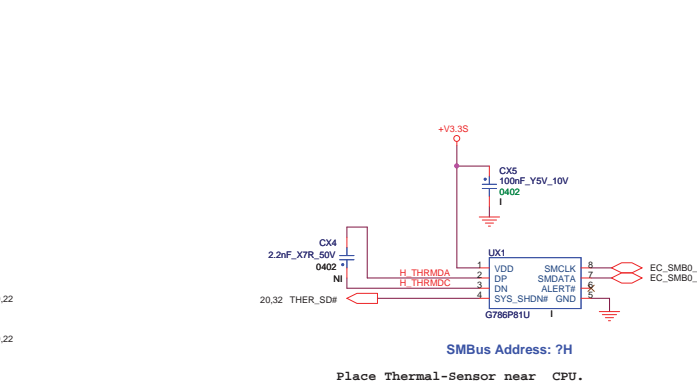
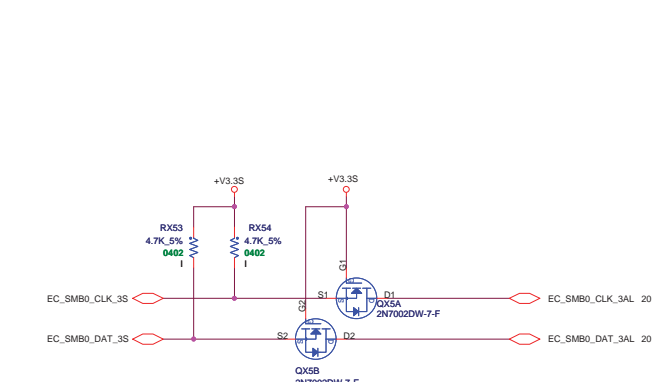
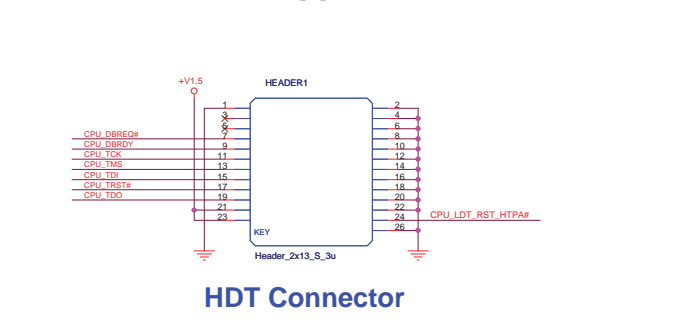
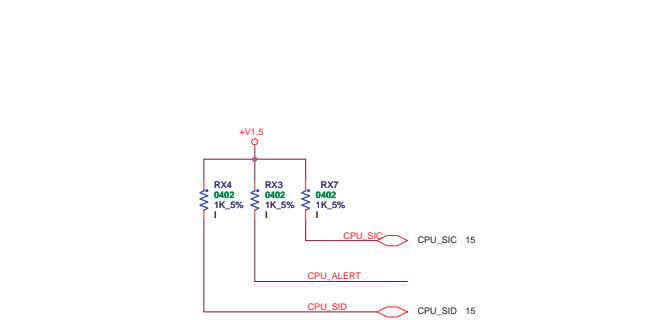
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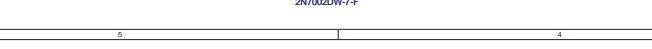


Thermdc and Thermda should be routed away to VRM, crystal, etc. Customer should follow the MBDG. However, Guam is using TSI so this does not apply to Guam.



SVC		SVD		BOOT VOLTAGE(VDD)	
		(CPU)RST_PROG	(CPU)RST_PROG	(CPU)RST_PROG	(CPU)RST_PROG
		=VCC(GND)	=OPEN	=VCC(GND)	=OPEN
0	0	1.1	1.1		
0	1	1.0	1.2		
1	0	0.9	1.0		
1	1	0.8	0.8		

VID OVERRIDE TABLE (VDD)



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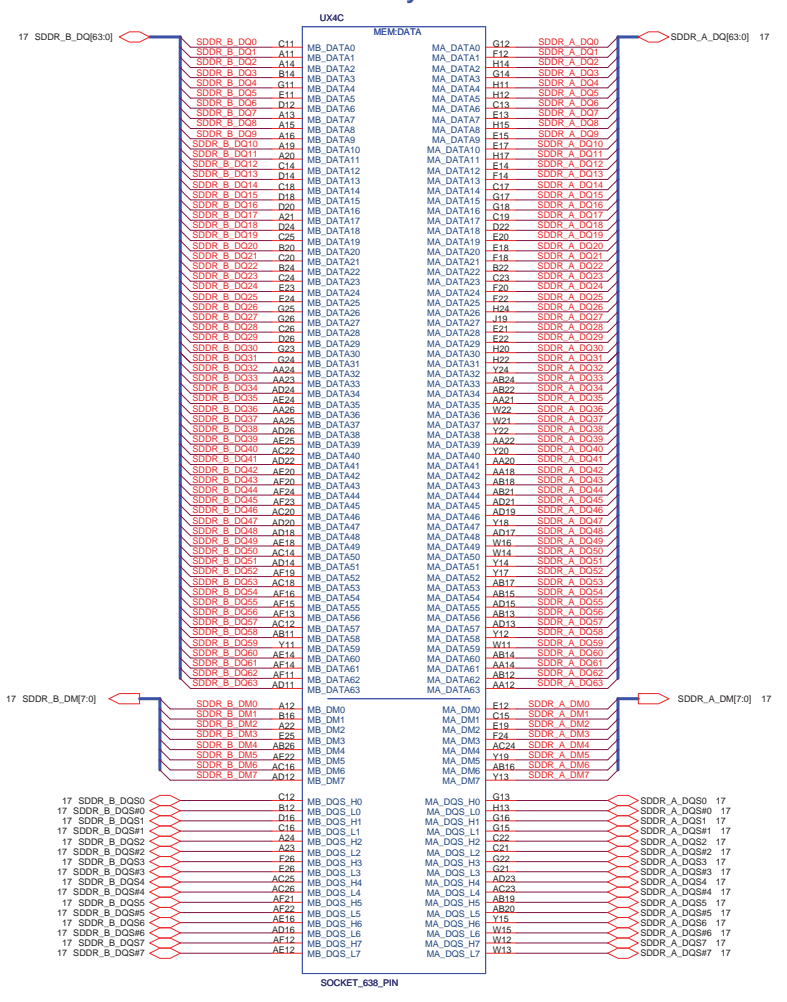
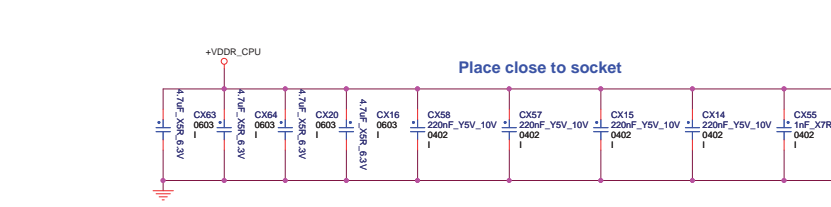
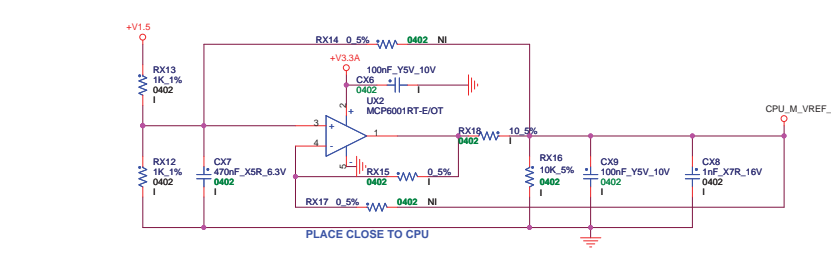
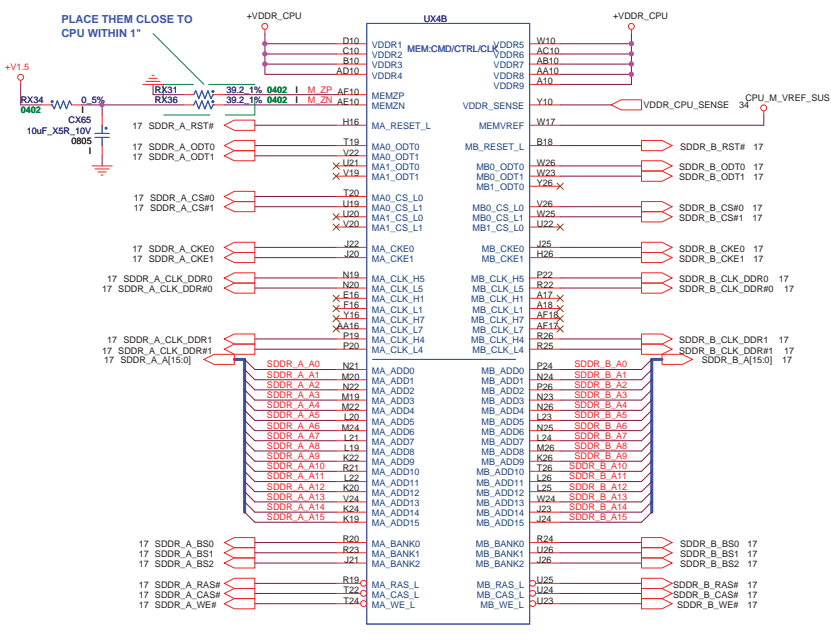
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Title: **S1G4 CTRL & DEBUG**

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Processor Memory Interface

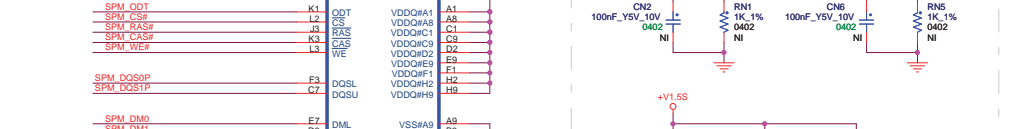
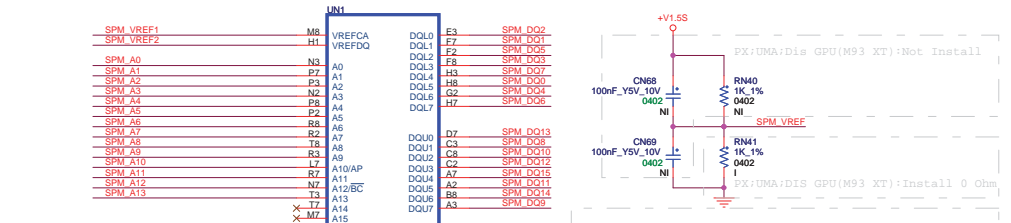
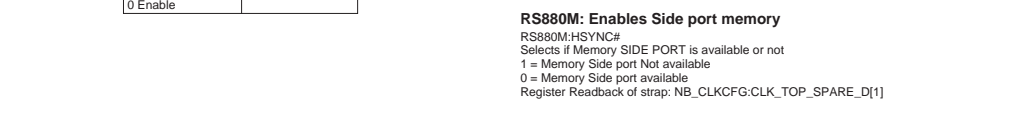
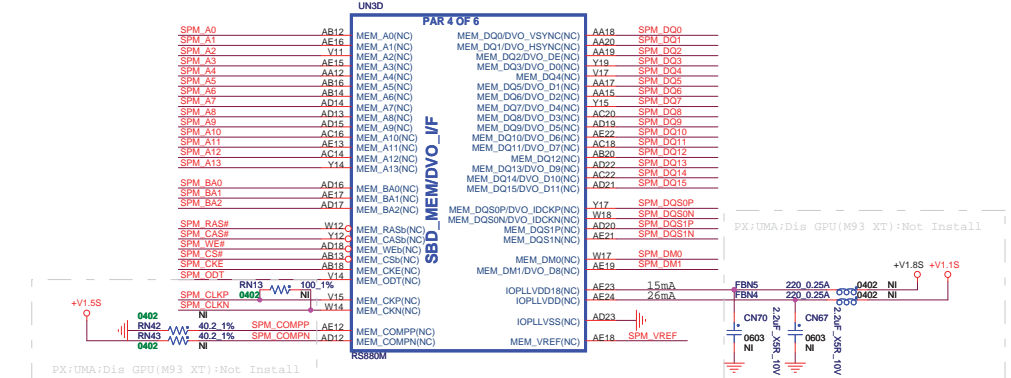
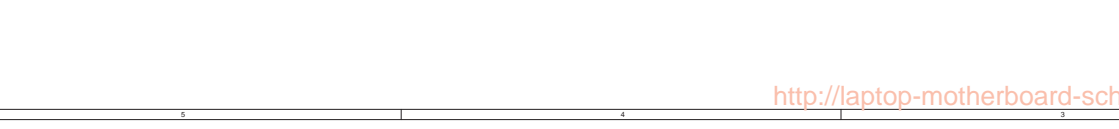
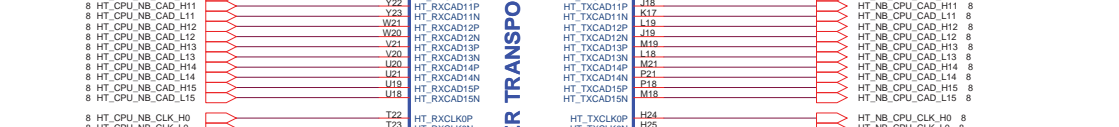
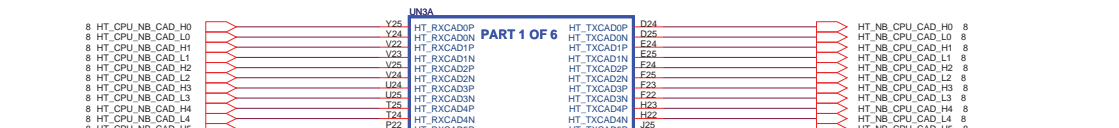
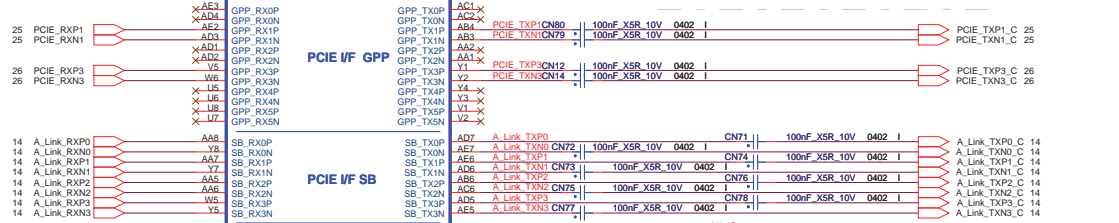
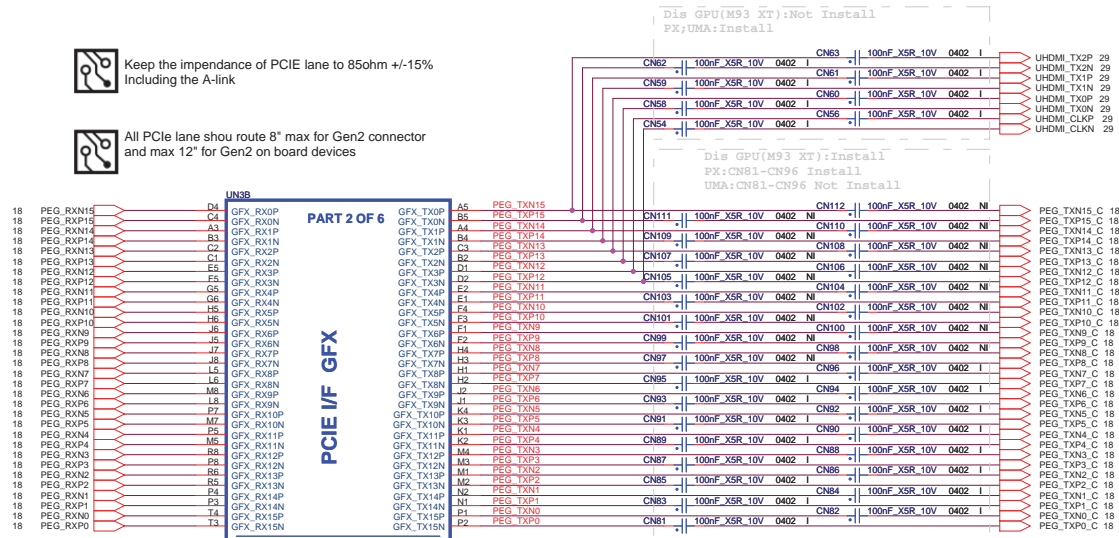




Keep the impedance of PCIe lane to 85ohm +/-15% including the A-link



All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices

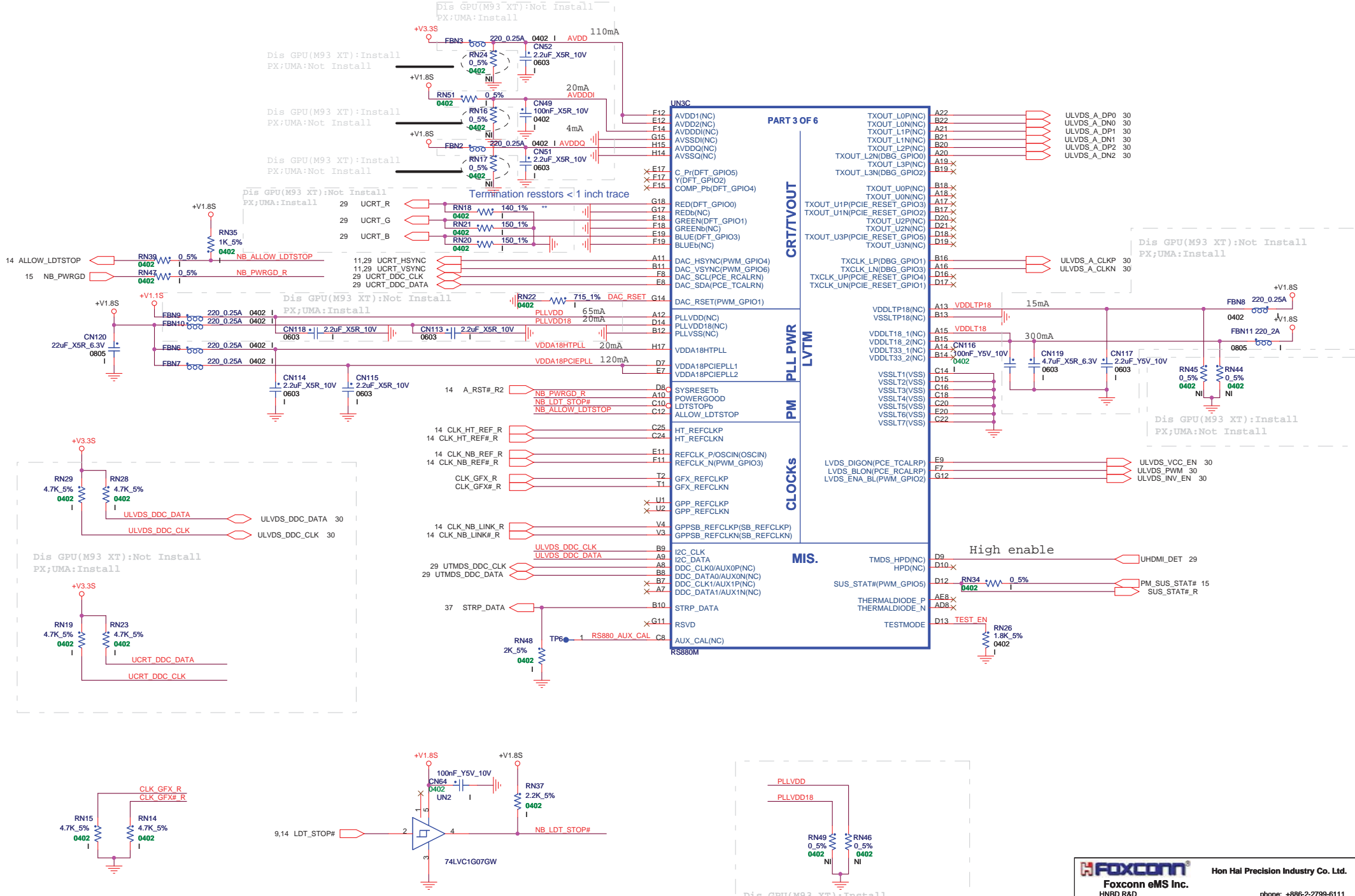


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Rev
RS880M-PCIE/HT LINK/SPMEM

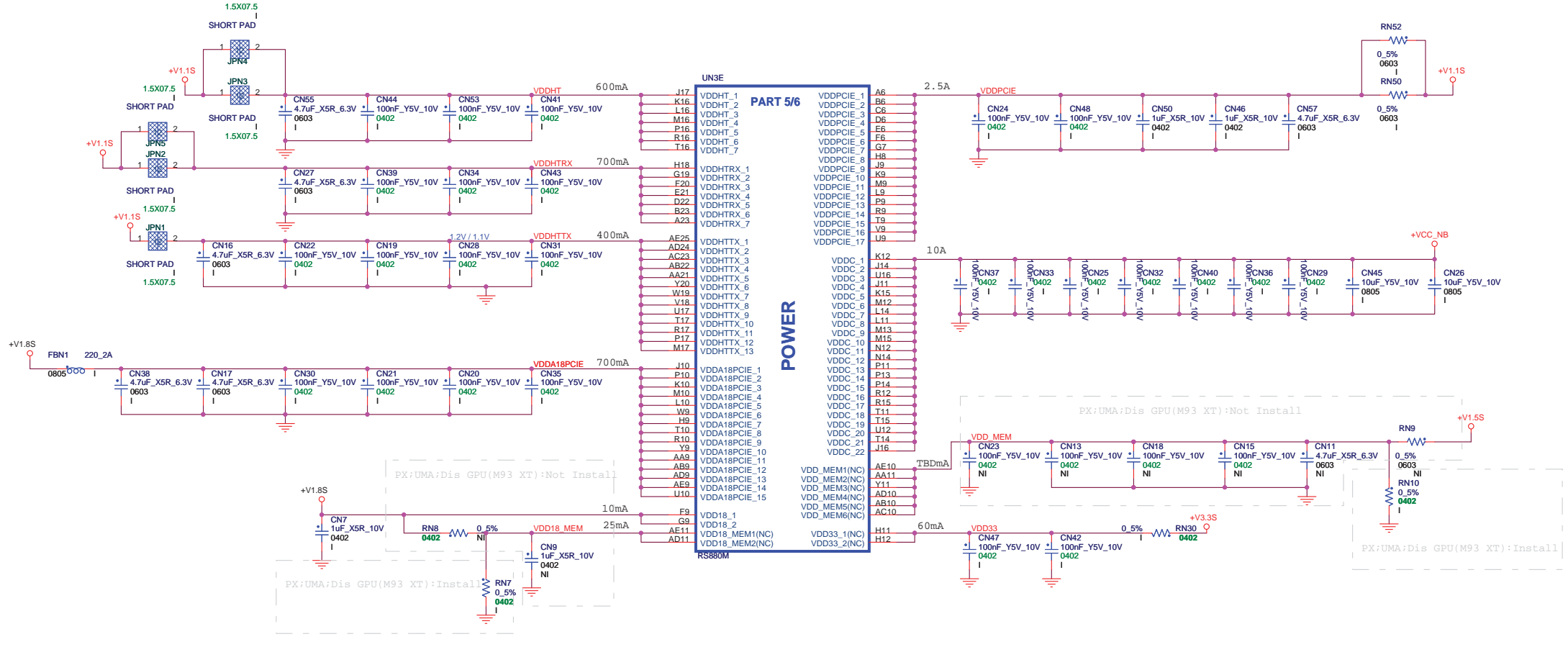
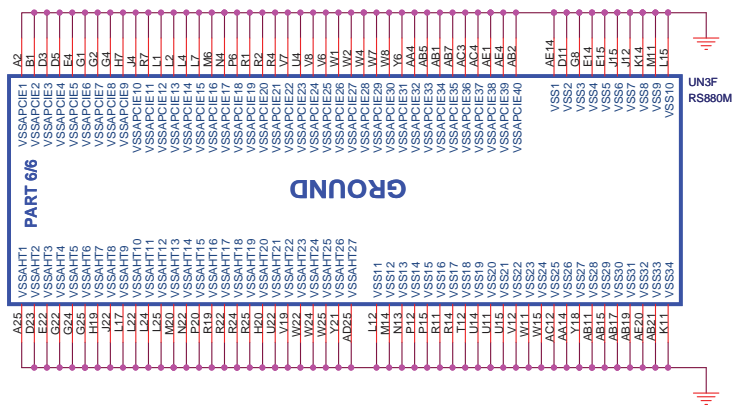
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Title			
RS880M-SYSTEM I/F			
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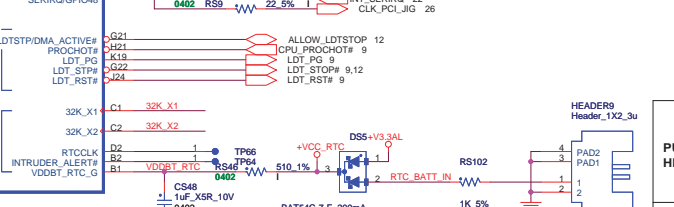
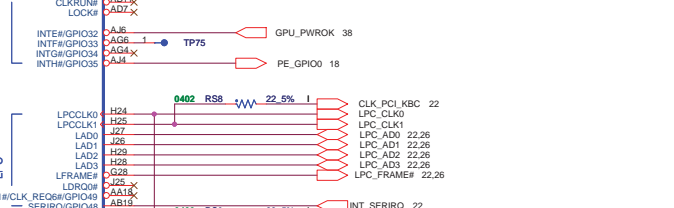
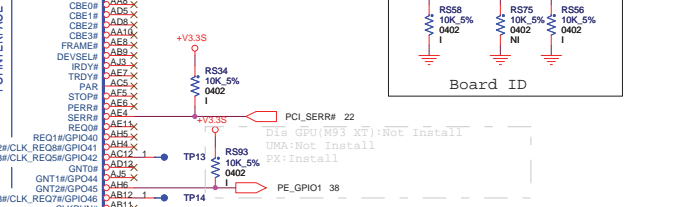
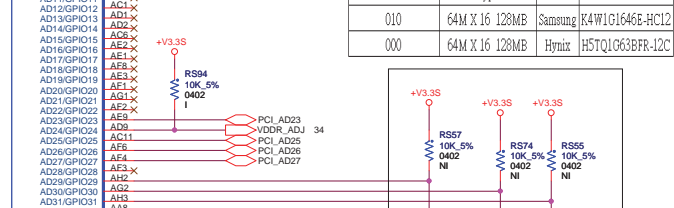
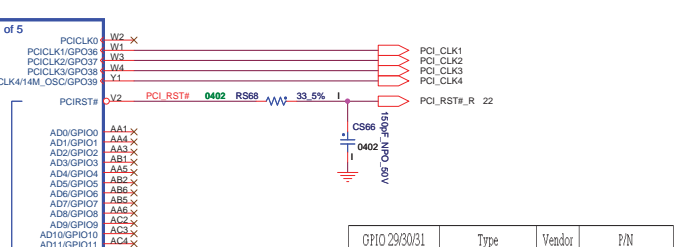
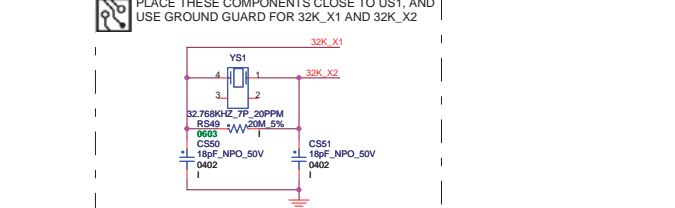
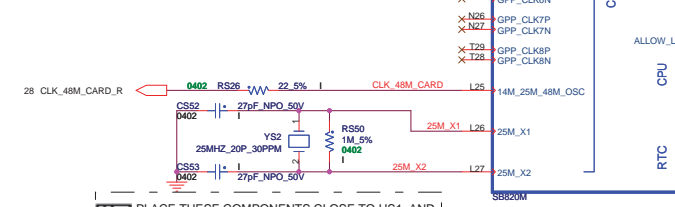
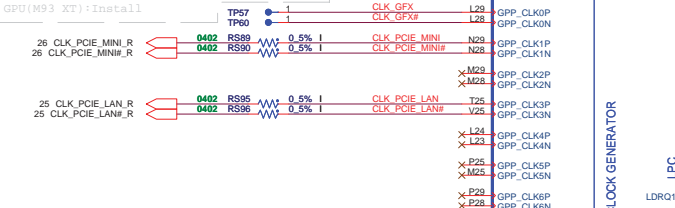
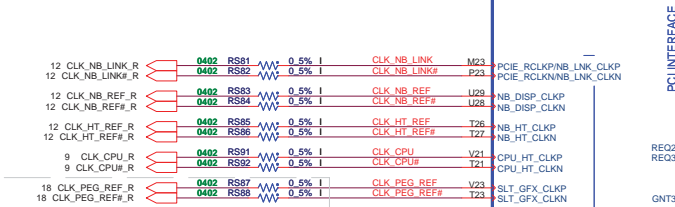
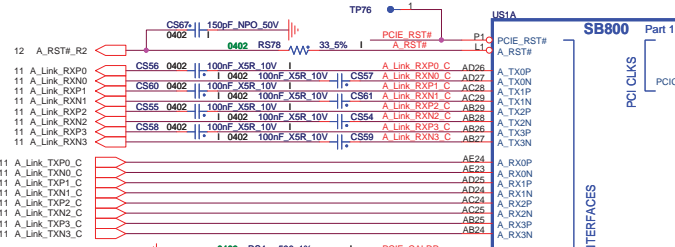
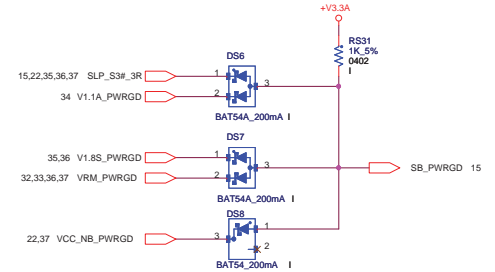
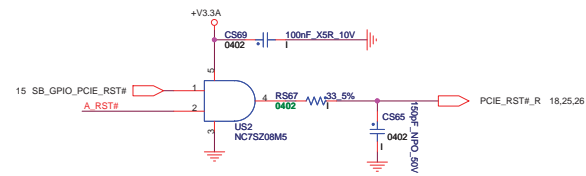
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Title: **RS880M-POWER**

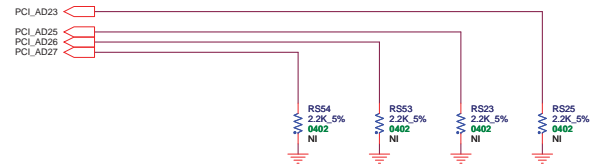
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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US1

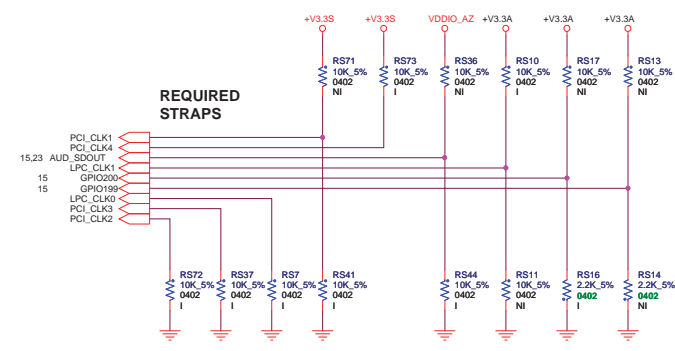


DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE PCI MEM BOOT

REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L,L = LPC ROM (Default) L,L = FWH ROM	

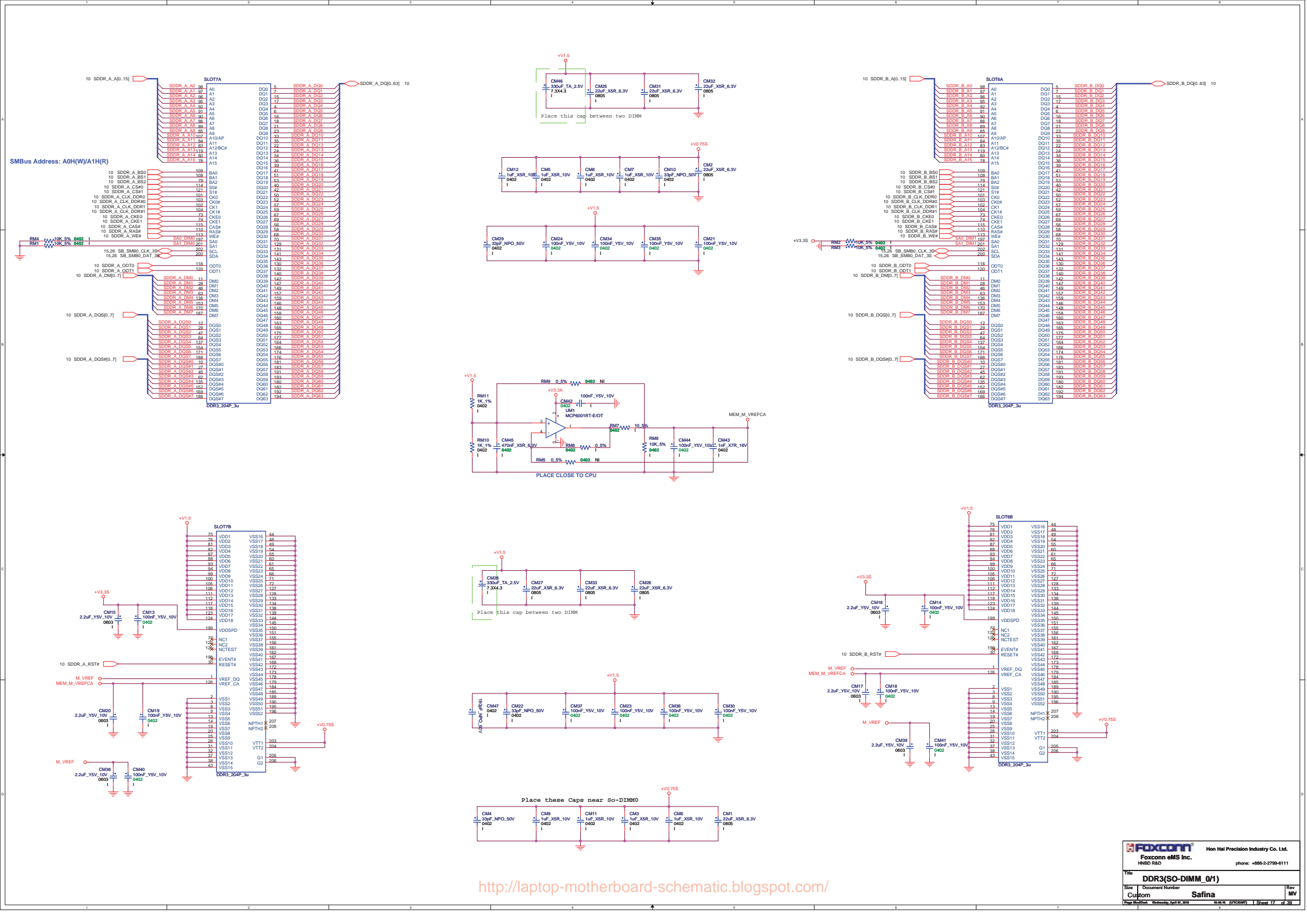
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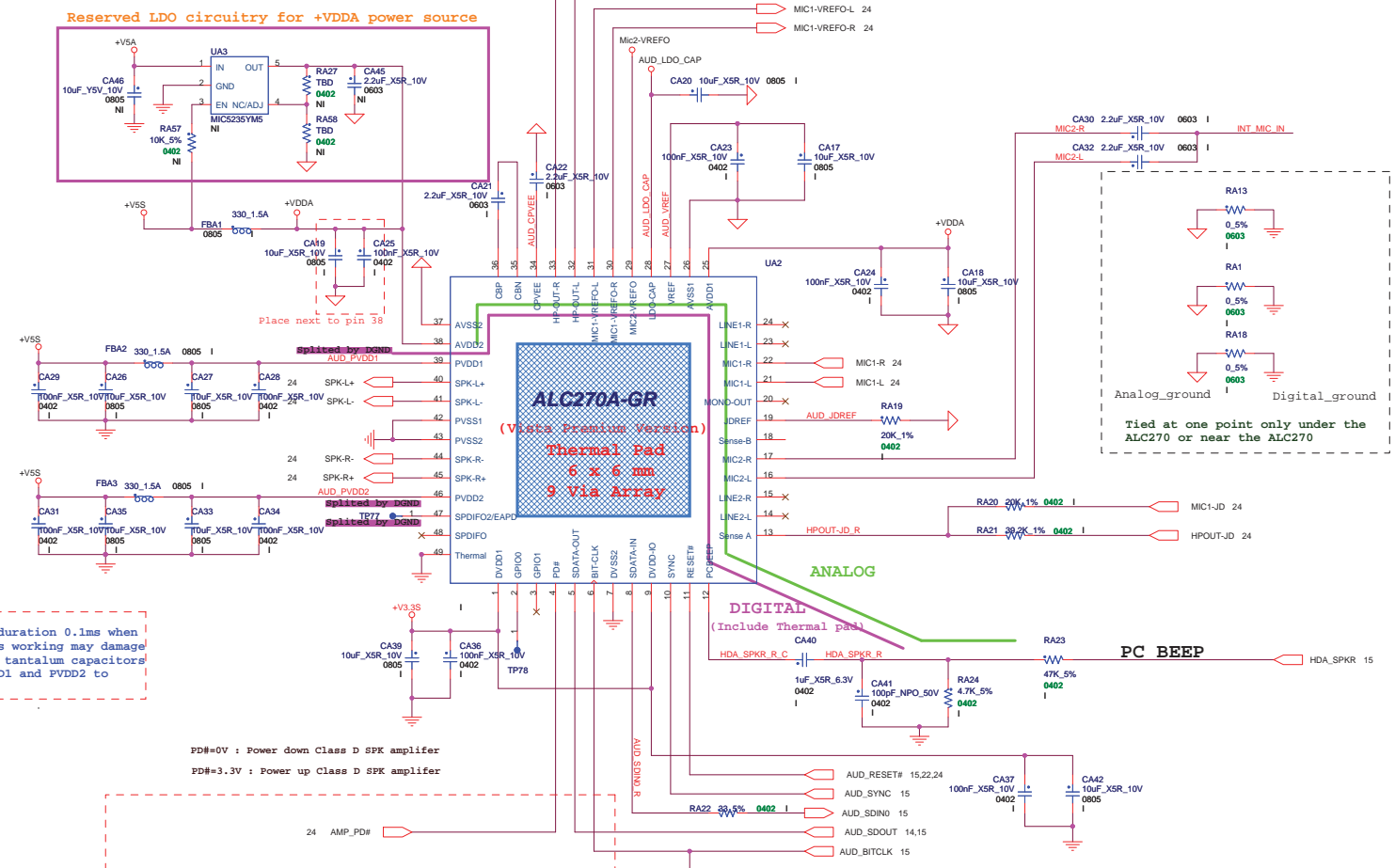
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Foxconn eMS Inc.
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Title: **SB820M-PCIE/CPU/LPC/STRAP**

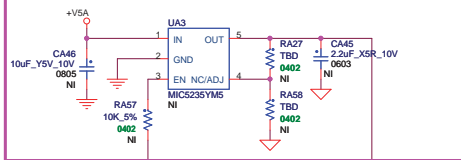
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Reserved LDO circuitry for +VDDA power source



Place next to pin 38

Splitted by DDD

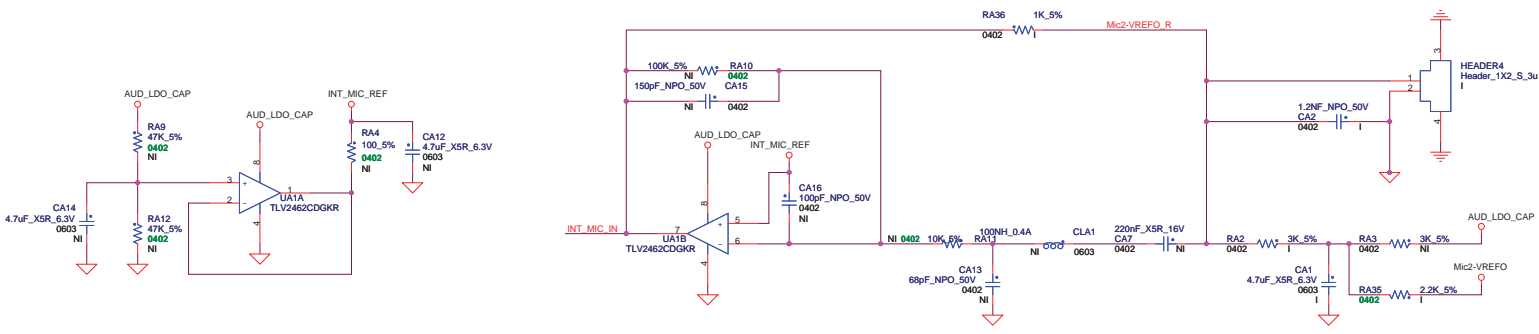
Splitted by DDD

Splitted by DDD

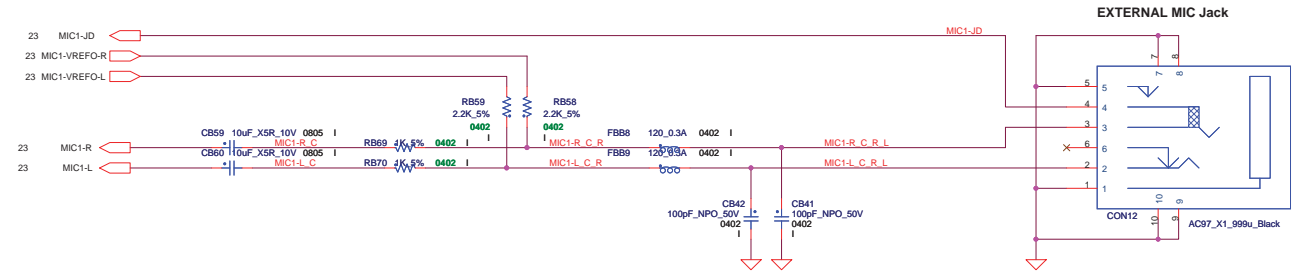
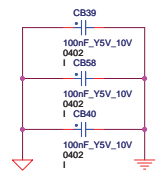
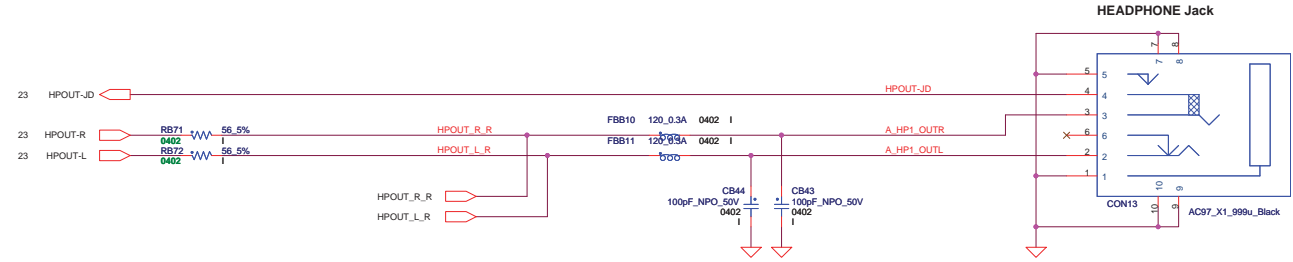
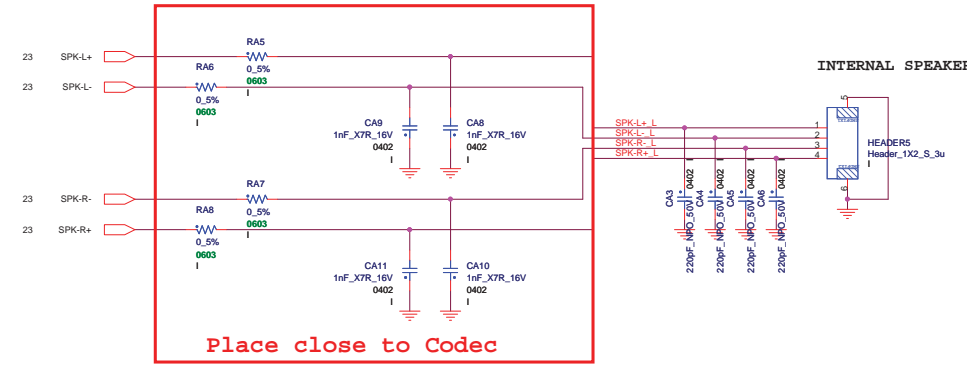
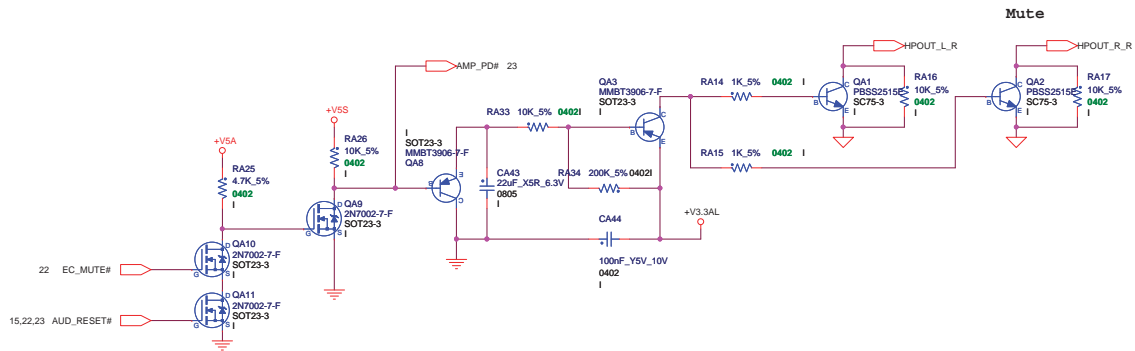
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

PD# = 0V : Power down Class D SPK amplifier
PD# = 3.3V : Power up Class D SPK amplifier

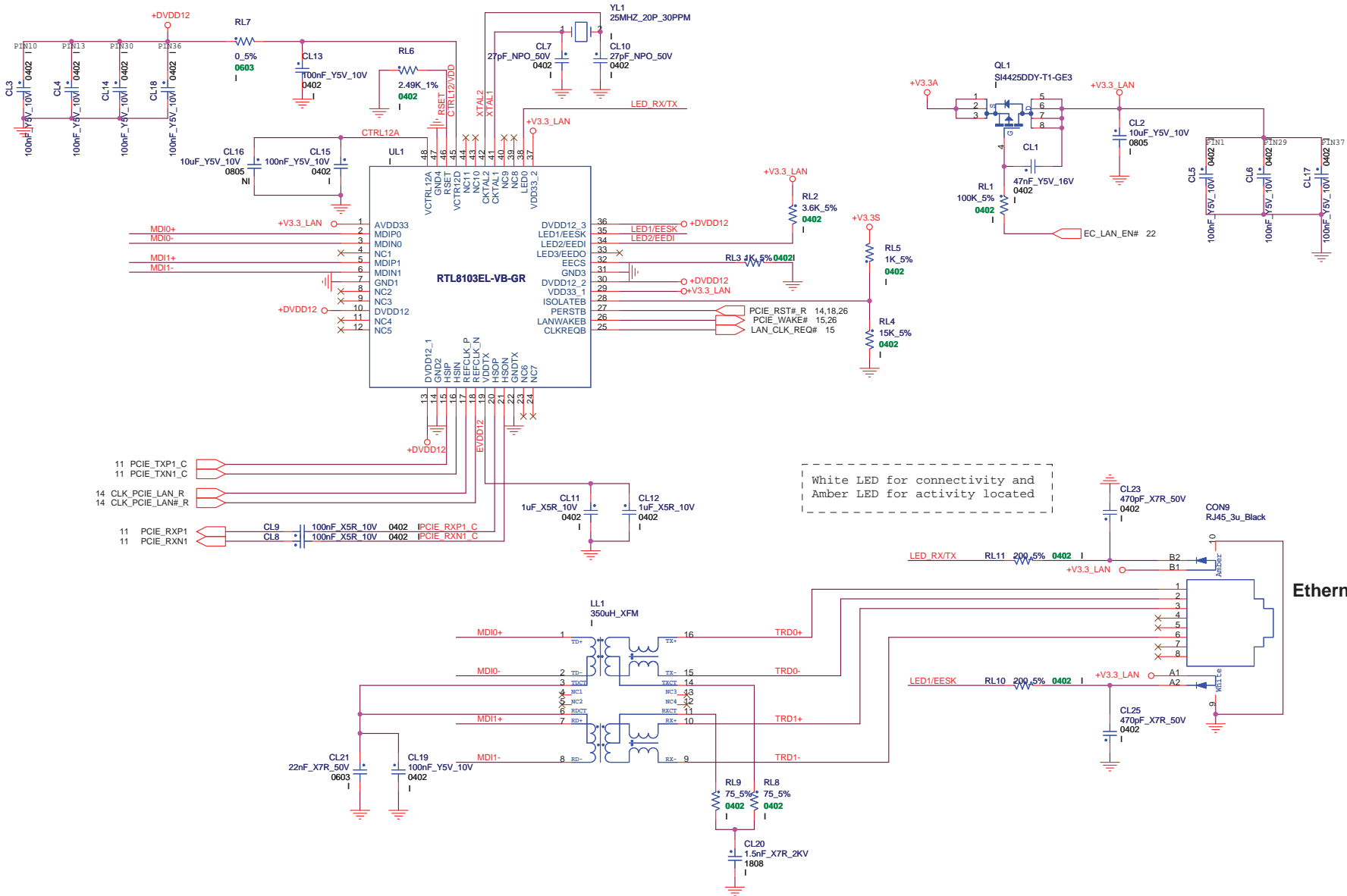
<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)



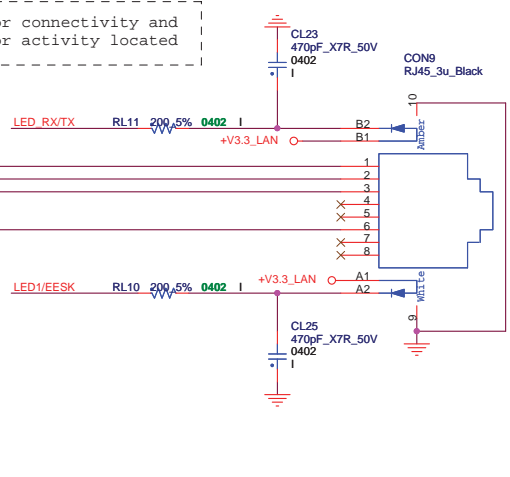
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Size	Document Number			Rvw
Custom	Safina			MV
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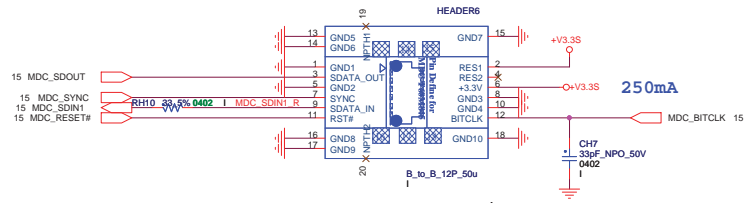
<http://laptop-motherboard-schematic.blogspot.com/>



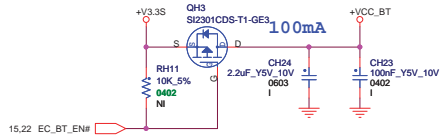
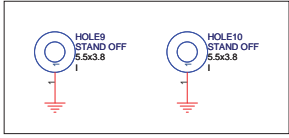
White LED for connectivity and Amber LED for activity located



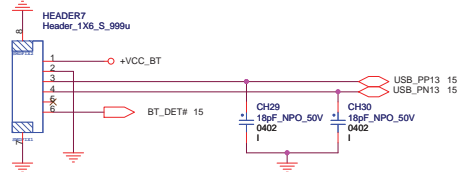
Ethernet



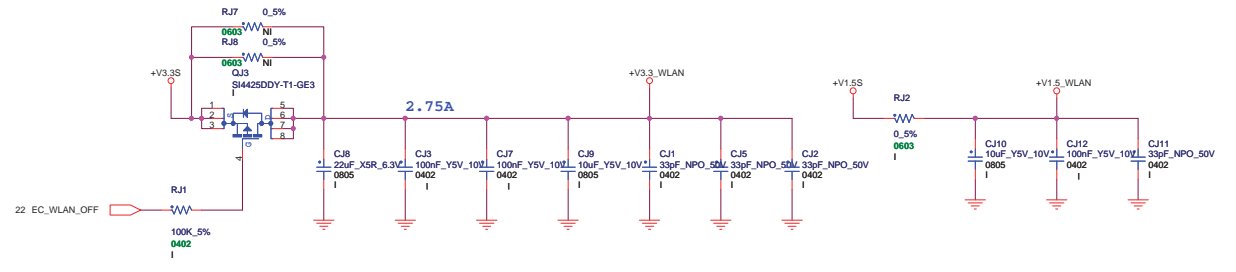
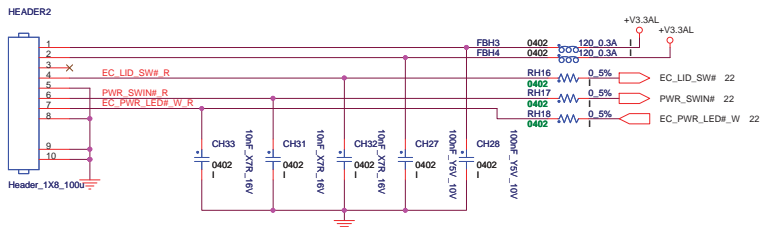
MDC CONN. Option



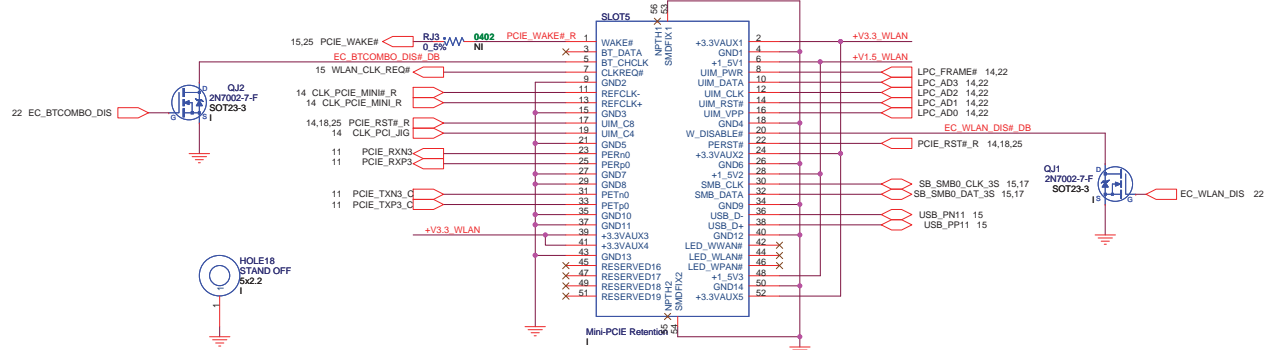
Bluetooth CONN.



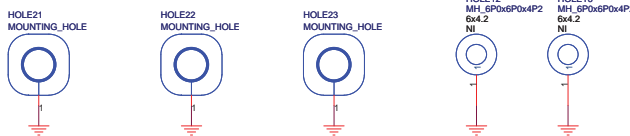
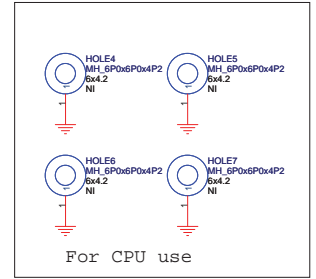
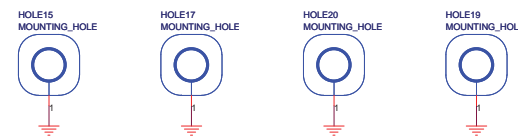
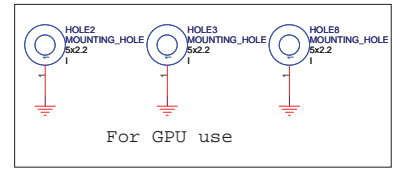
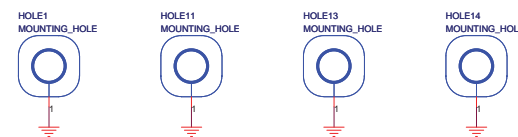
PWR Board CONN.



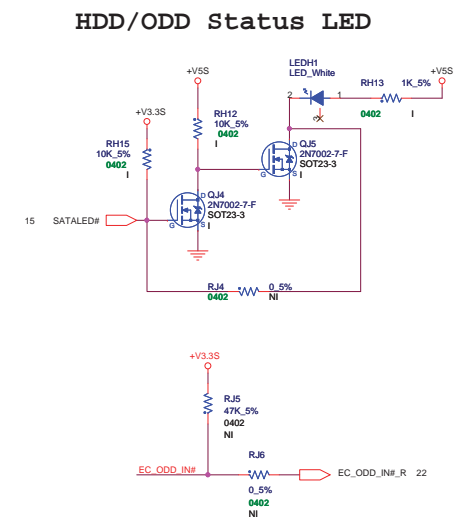
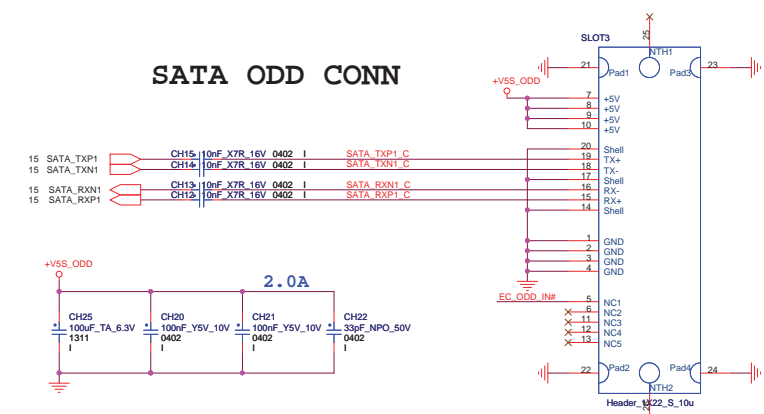
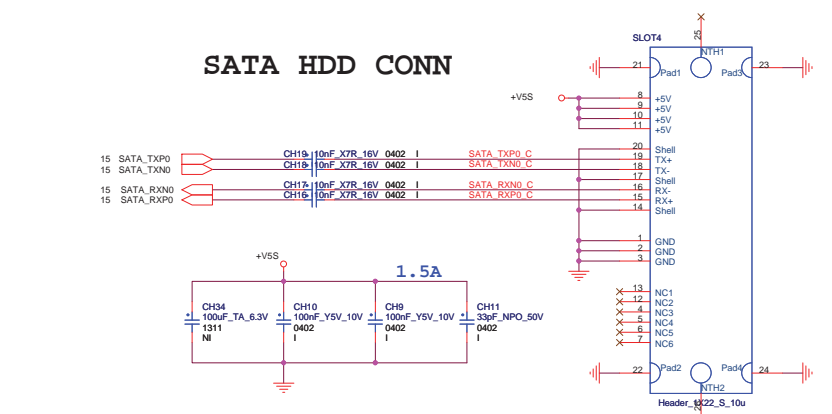
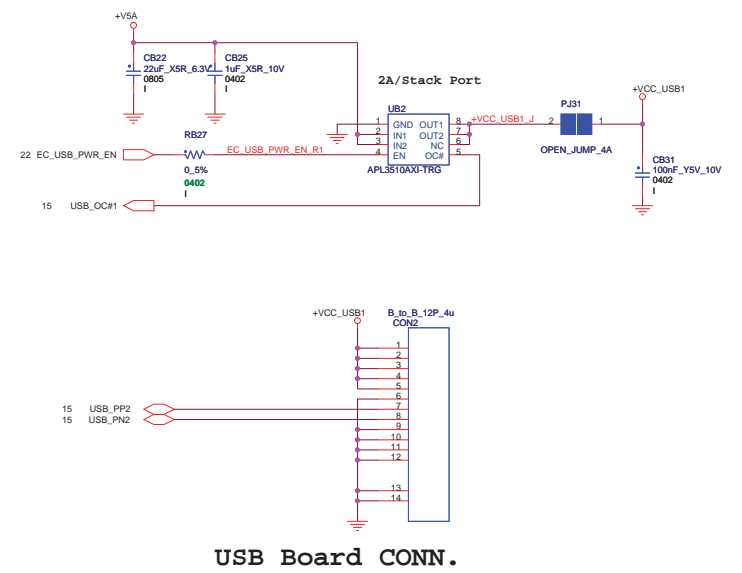
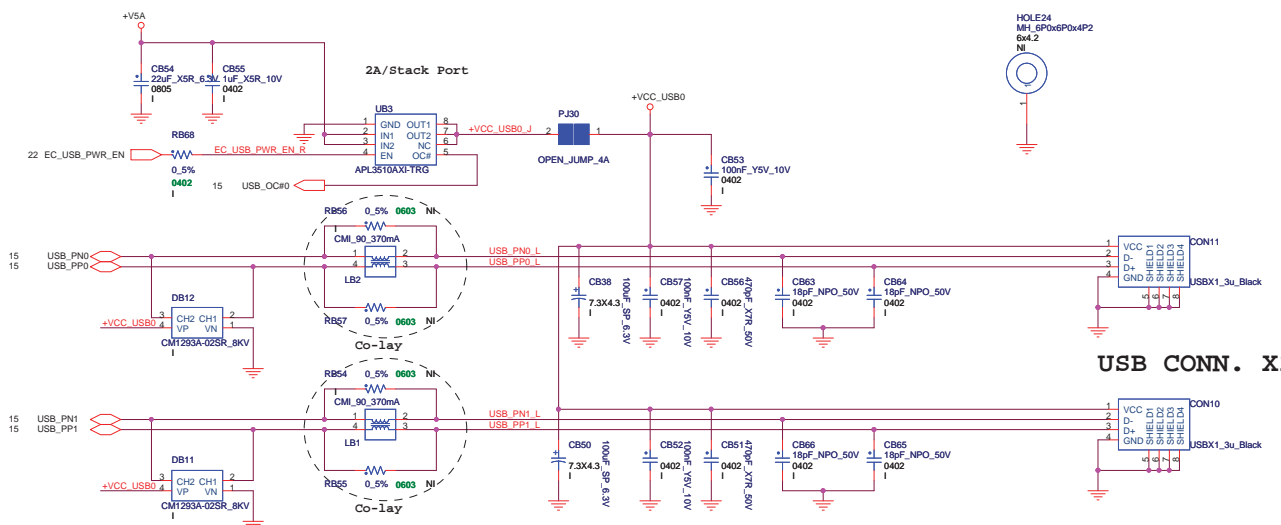
+1.5V=>0.5A Peak/0.375A Normal
+3.3Vaux=>2.75A Peak/1.1A Normal



Half Mini Card for WLAN



Mounting HOLE



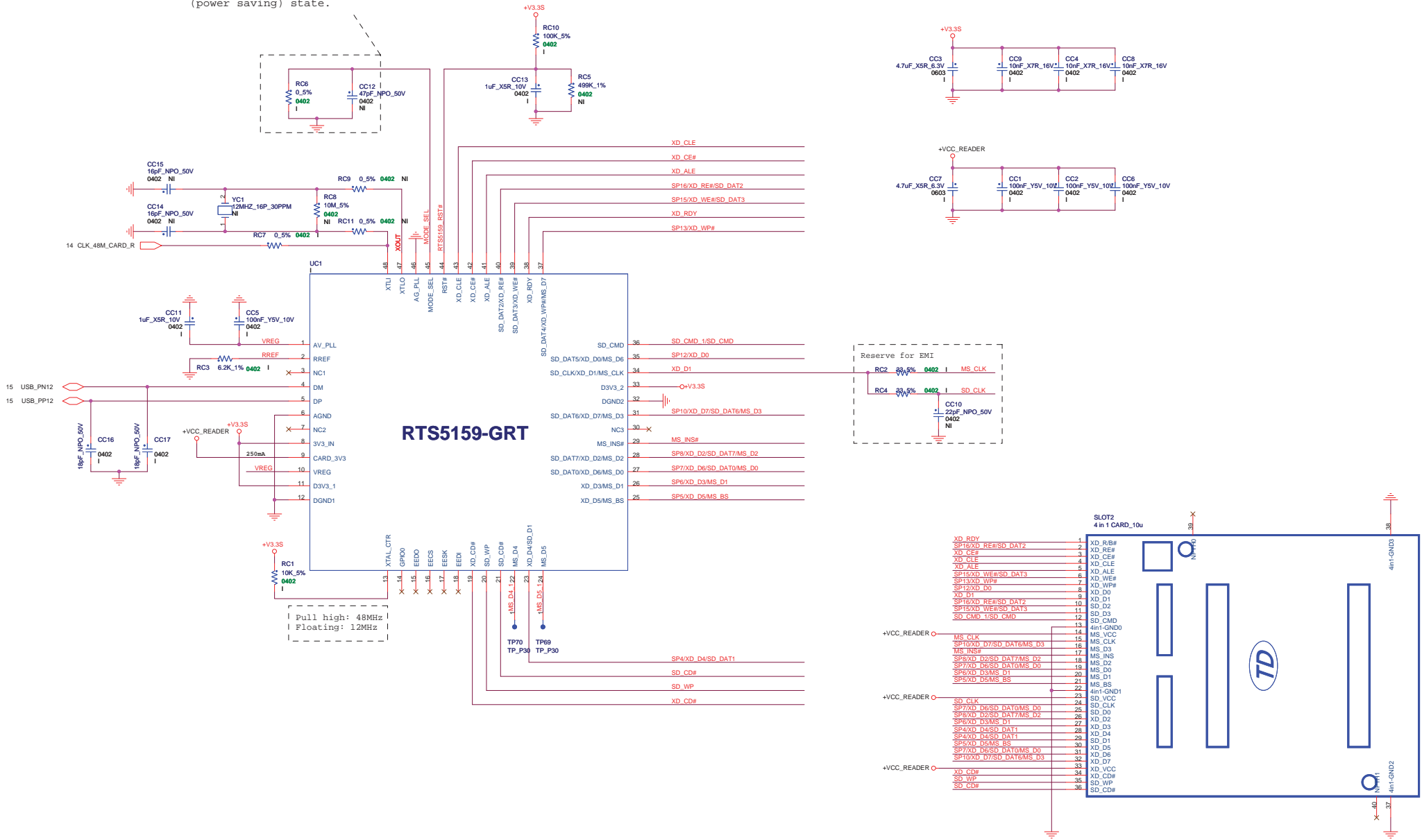
Power pin current
max. 1300 mA (less 2ms)

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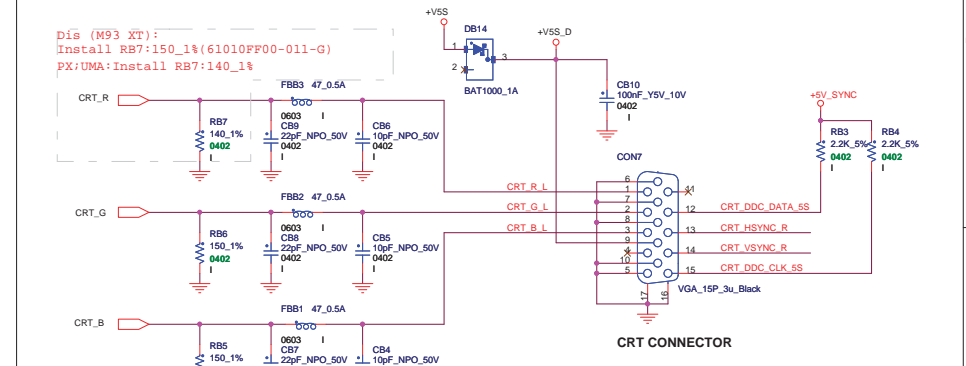
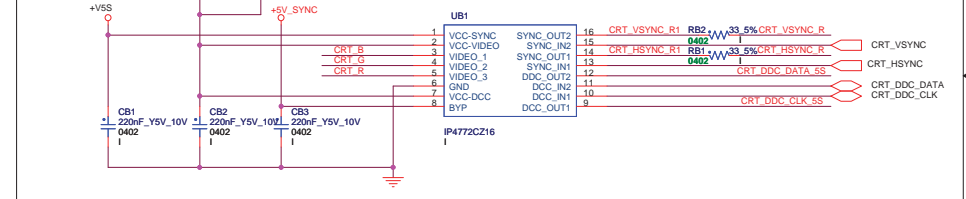
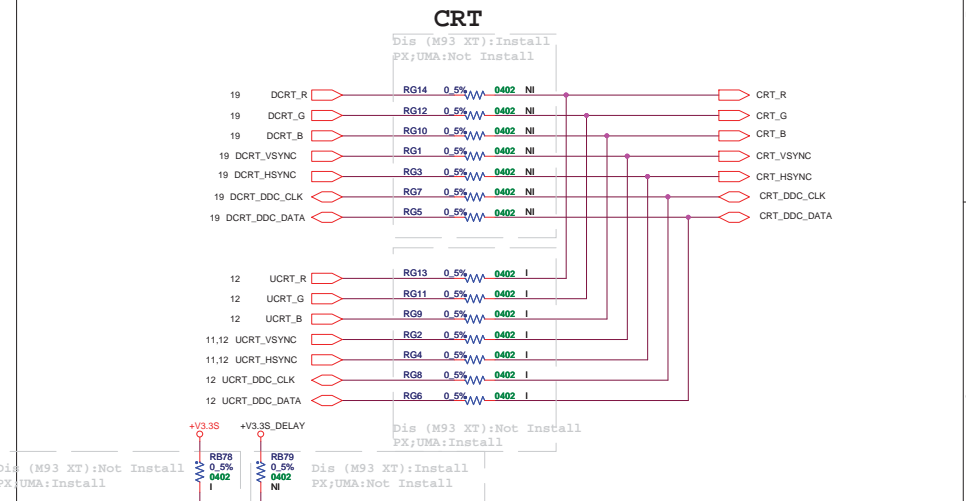
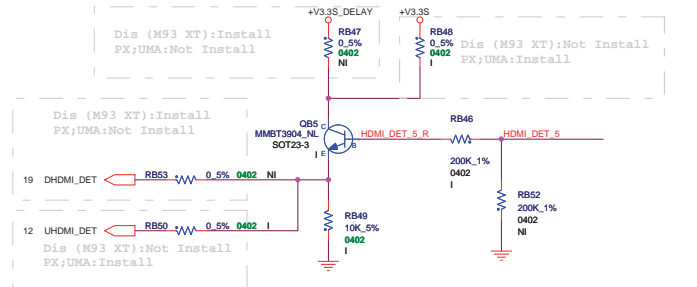
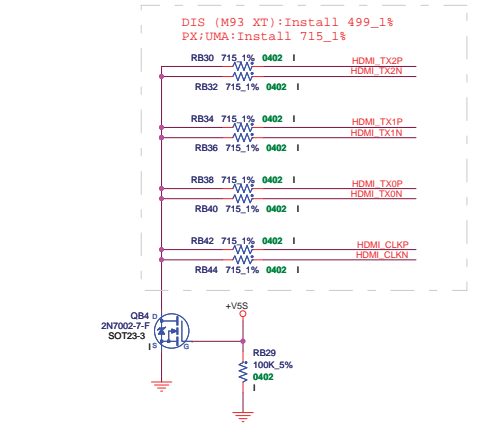
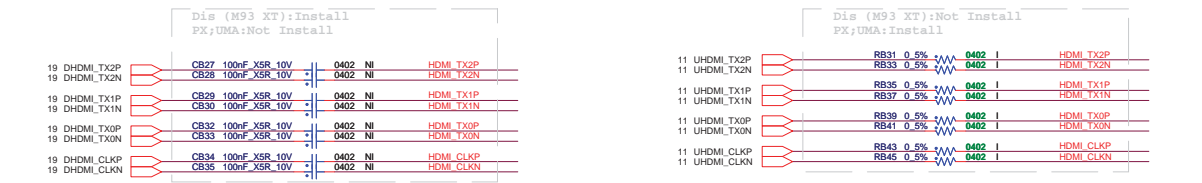
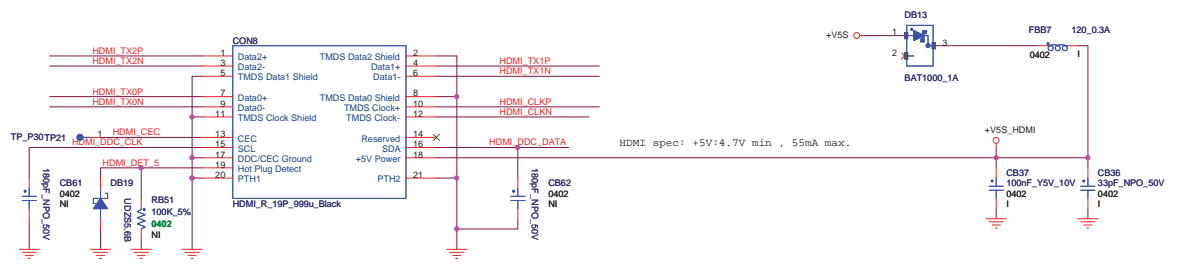
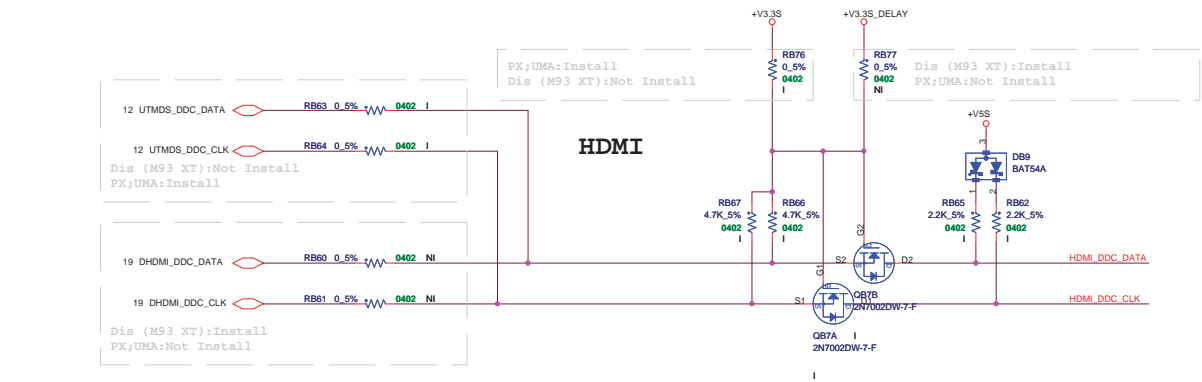
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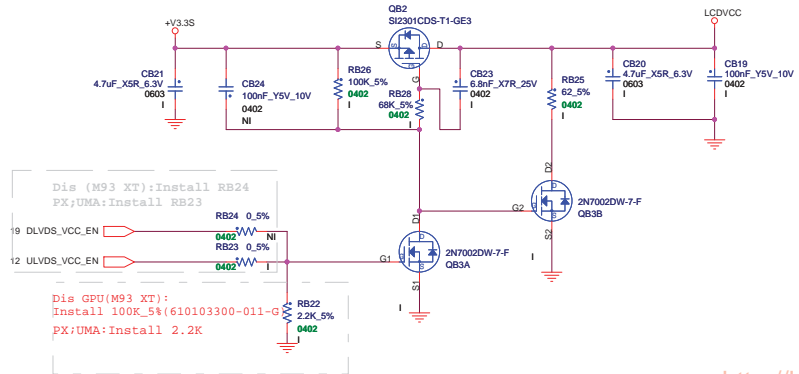
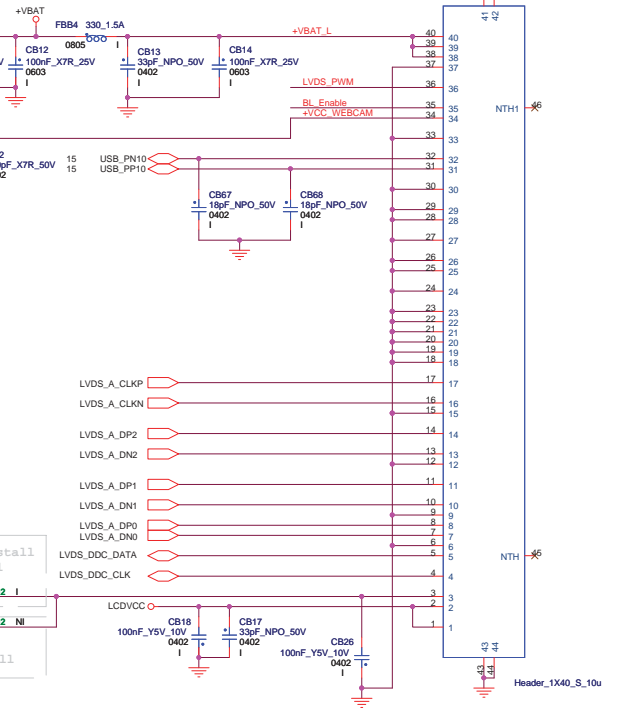
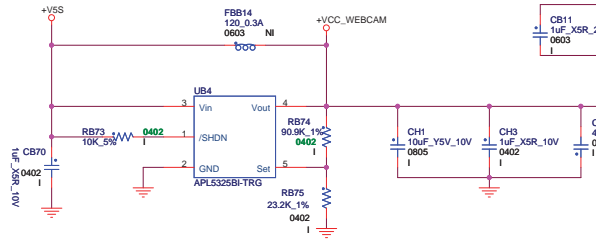
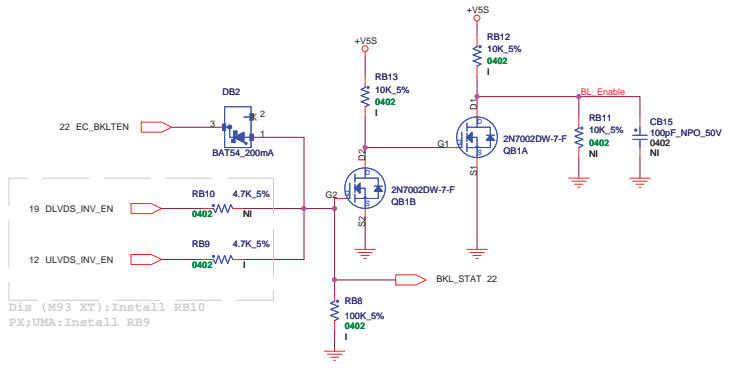
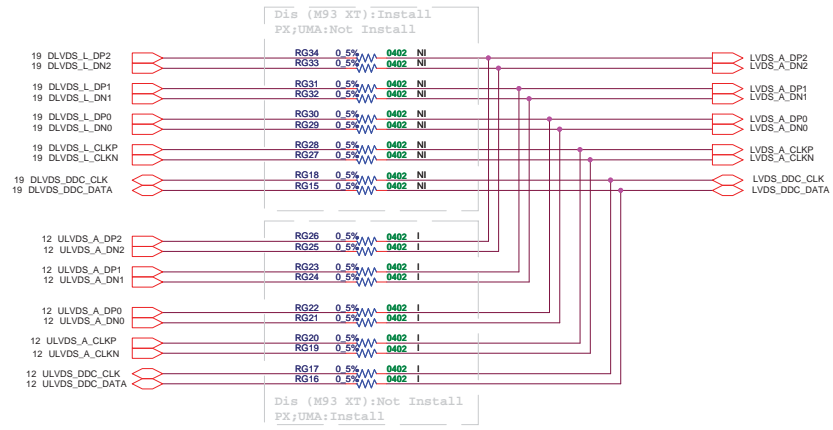
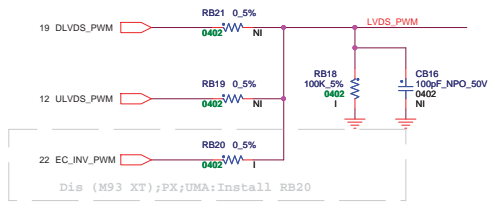
Title	USB2/USB DB CONN./SATA CONN.	
Size	Document Number	Rev
Custom	Safina	MV
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D3 mode: (R:0 ohm ; C:NC)
 If user remove memory card from
 socket, RTS5159 will terminate
 USB bus connection and enter D3
 (power saving) state.



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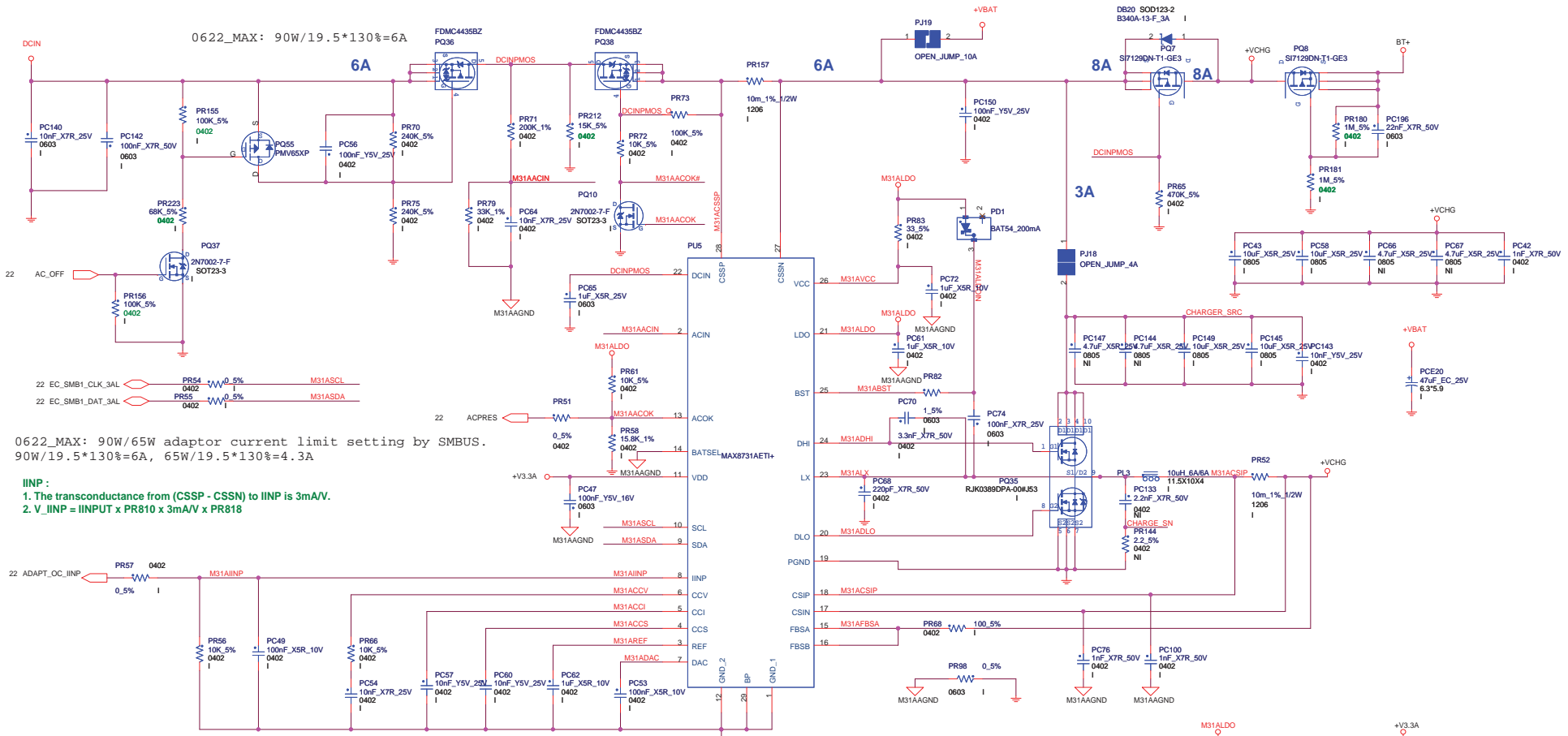




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Title LVDS&Webcam		Rev Mv
Size Custom	Document Number Safina	
Page Modified: Wednesday, April 07, 2010 18:48:16 (UTC+08:00)		Sheet 30 of 39

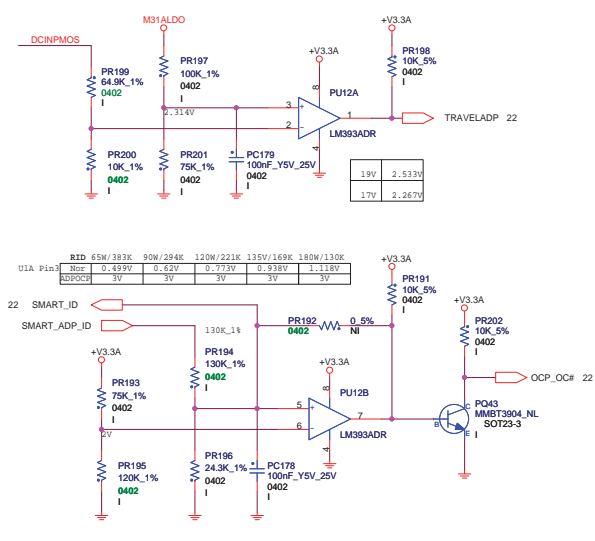
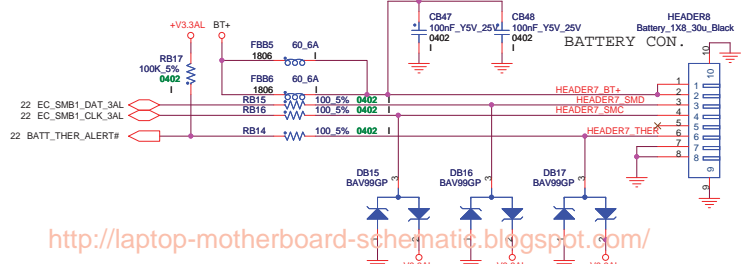
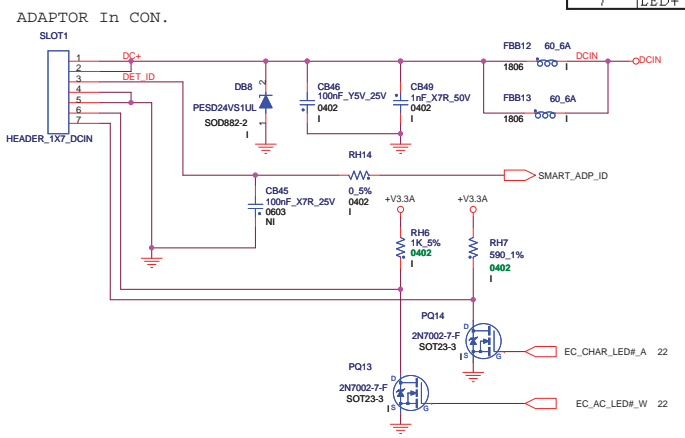


0622_MAX: 90W/65W adaptor current limit setting by SMBUS.
 $90W/19.5 \times 130\% = 6A$, $65W/19.5 \times 130\% = 4.3A$

- IINP :**
- The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 - $V_IINP = IINP \times PR810 \times 3mA/V \times PR818$

Pin No	Pin Define	AWG	Color
1	DC+	22	Red
2	DC+	22	Red
3	Detect (ID)	28	White
4	Detect (ID)	22	Black
5	DC-	22	Black
6	LED-	28	Black
7	LED+	28	yellow

Pin No.	Symbol	Comments
1	B ATT+	Batt+, Battery Positive Terminal.
2	B ATT+	Batt+, Battery Positive Terminal.
3	SMD	SMBus data interface I/O pin..
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



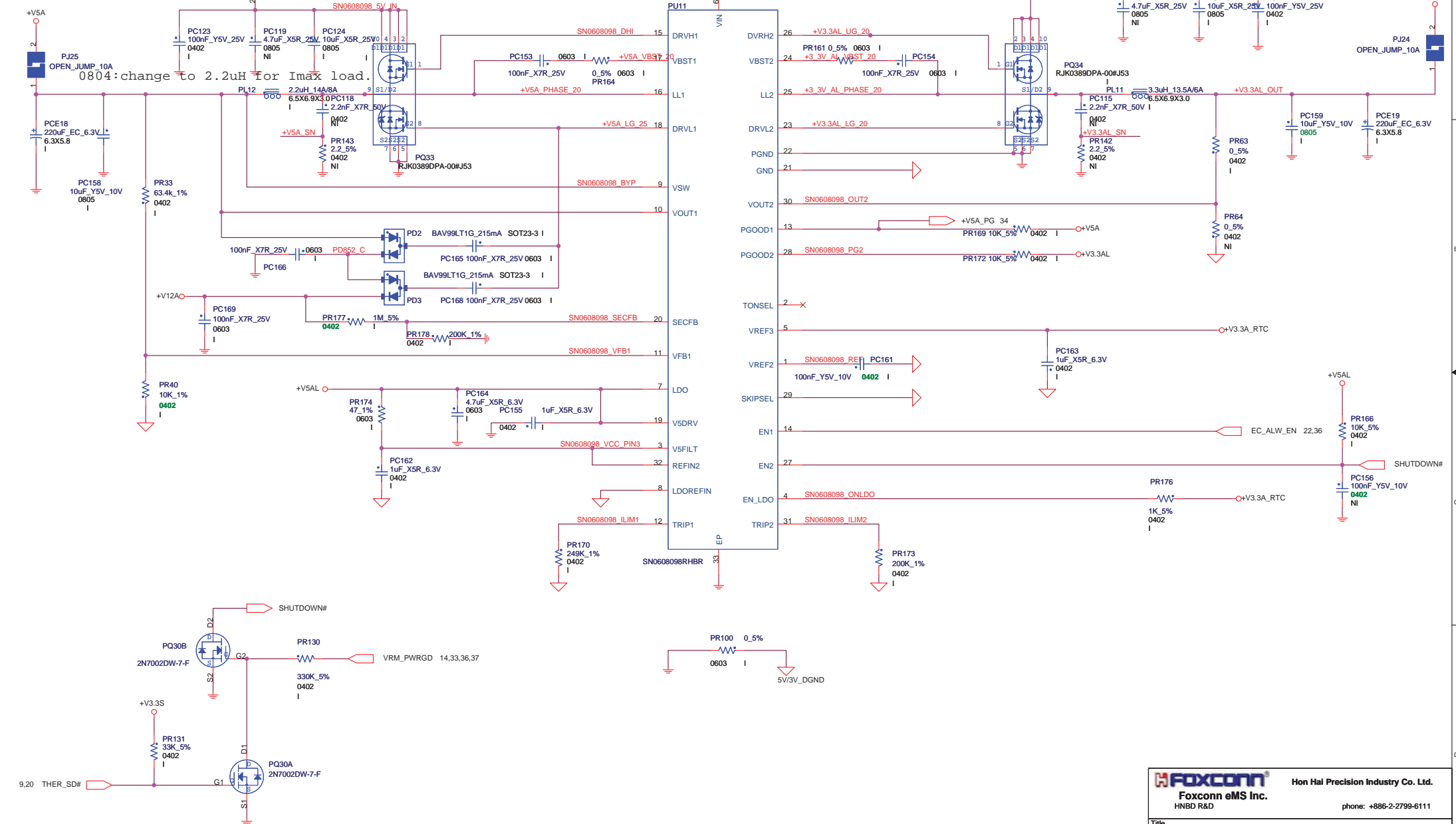
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Title: **PWR_Charger MAX8731AETI**
 Size: Document Number
 Custom: Safina
 Page Modified: Wednesday, April 07, 2010 18:16 (UTC+8) Sheet 31 of 39

+V5A/7A/5.6A

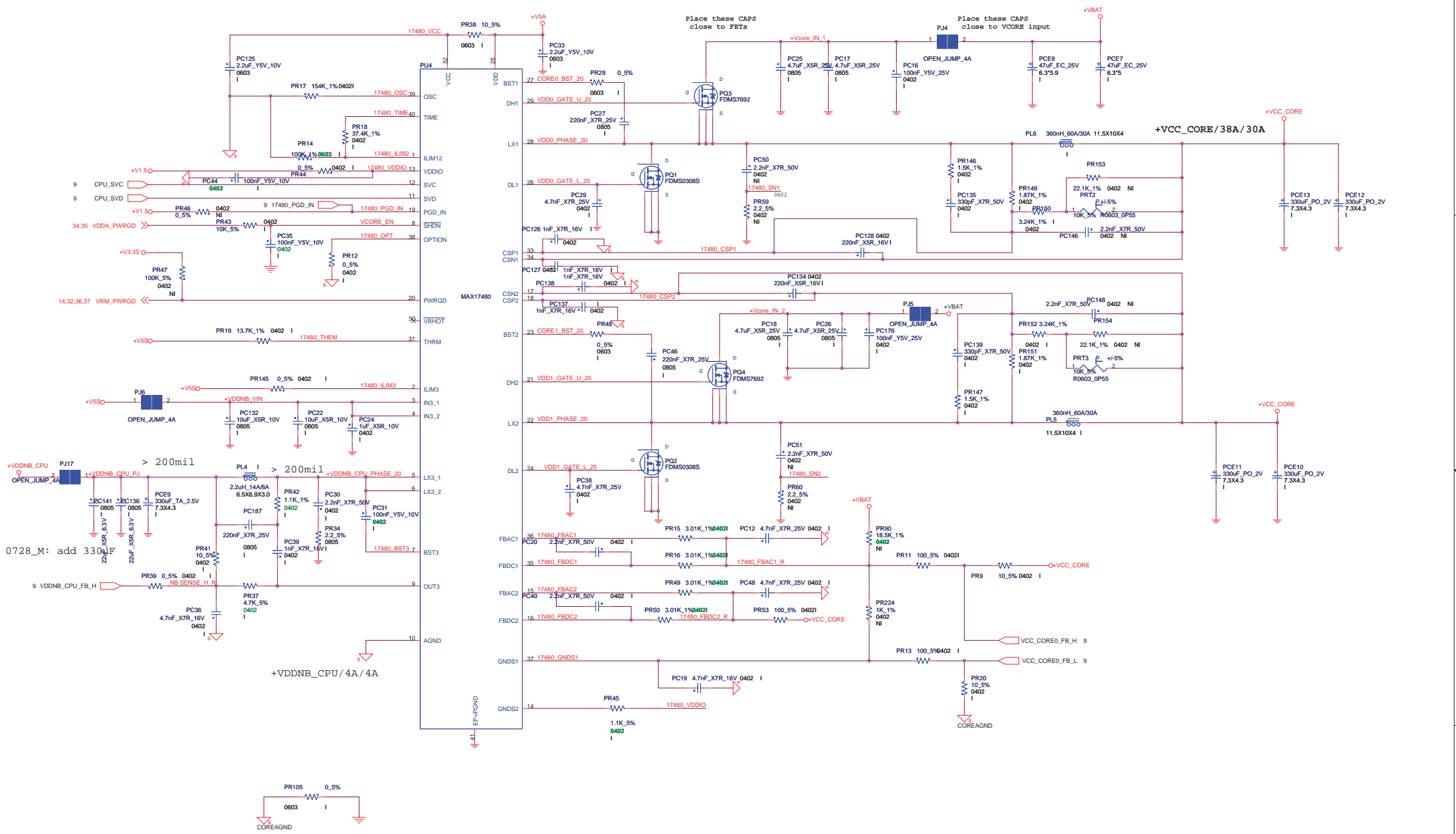
+V3.3A/6/4.8A



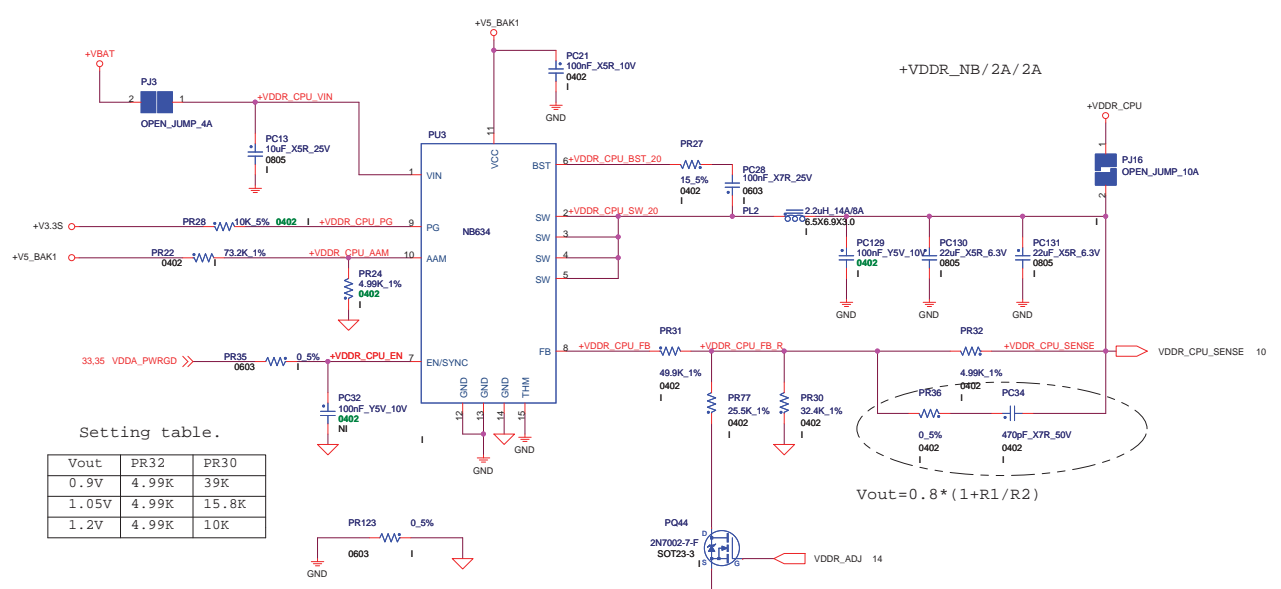
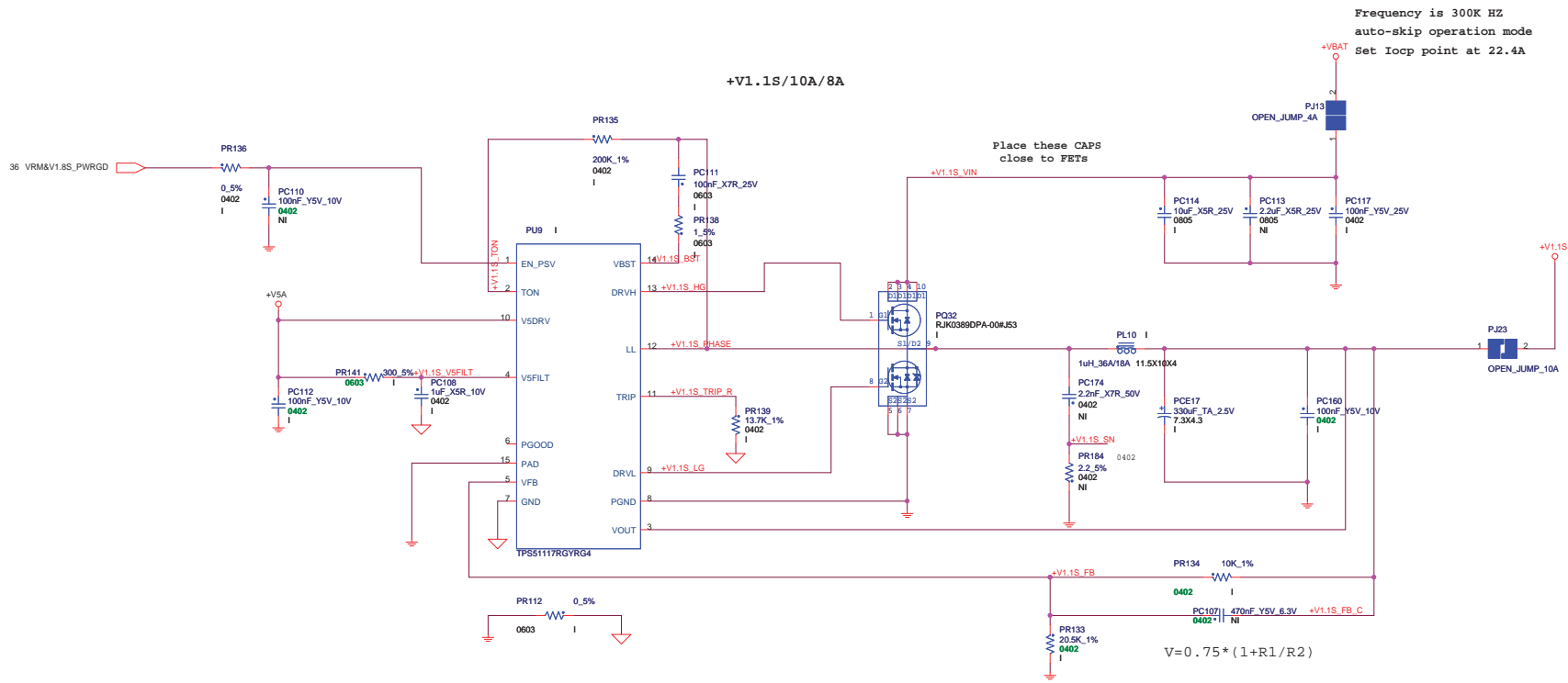
0804:change to 2.2uH for I_{max} load.

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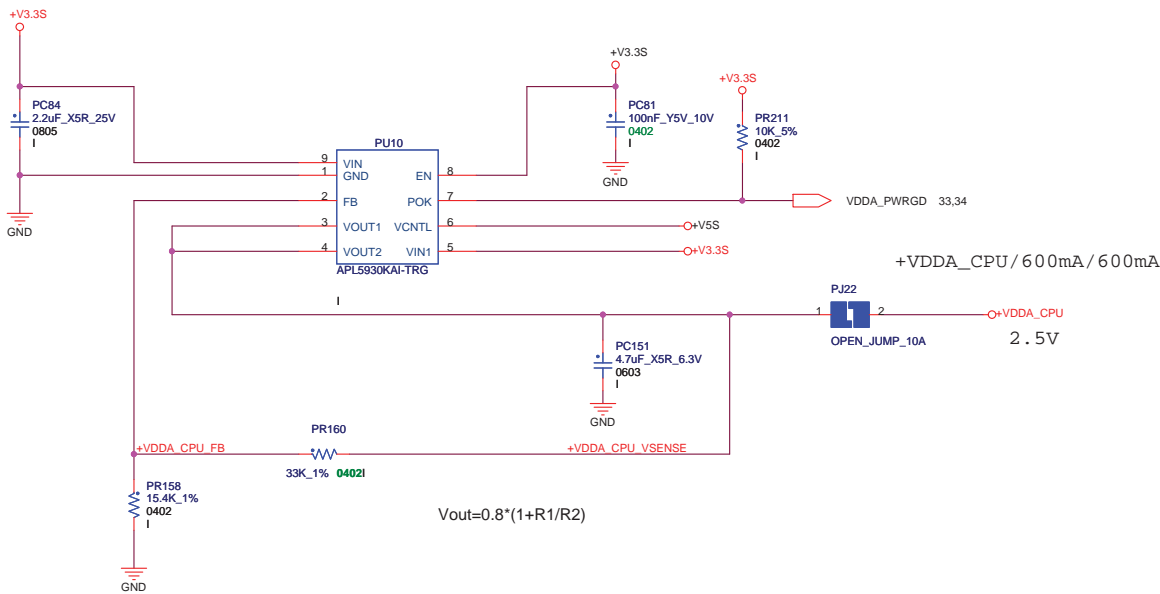
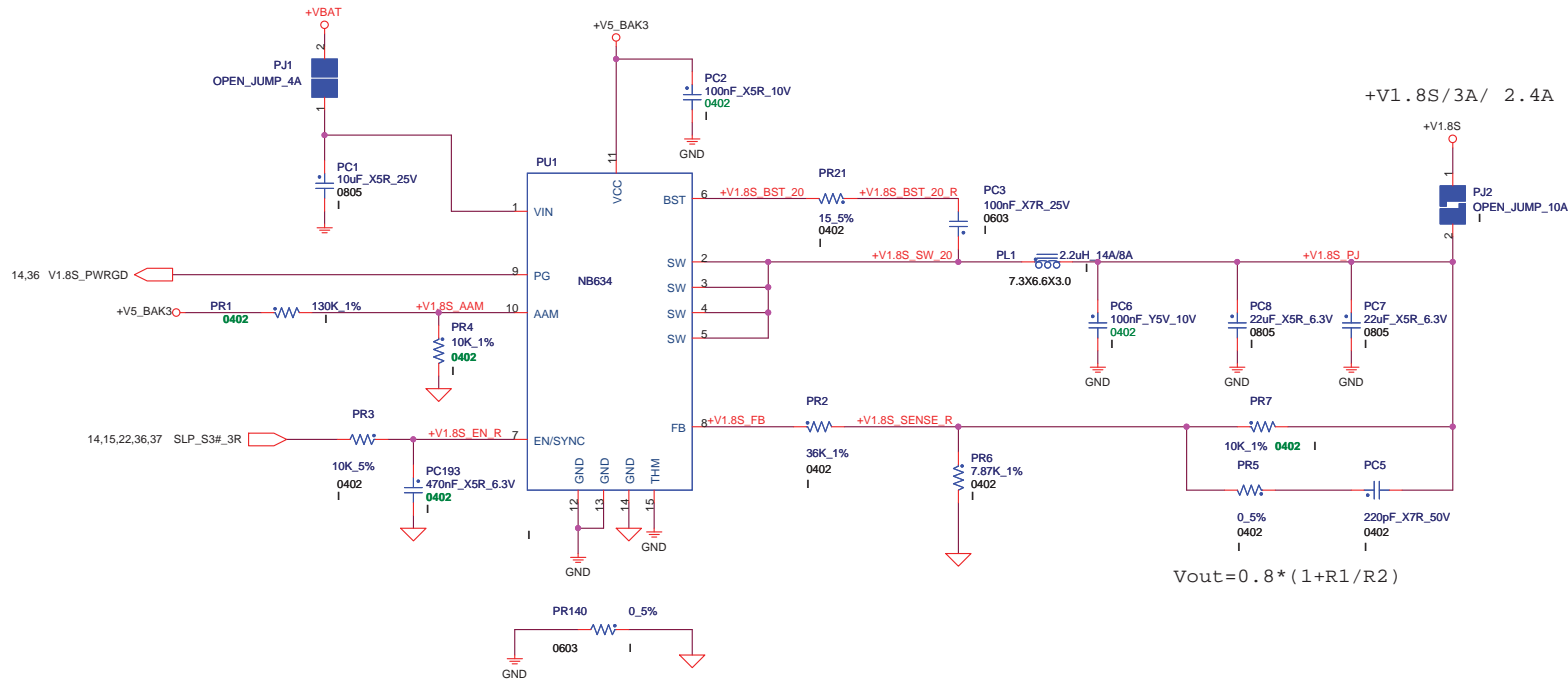
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Size Custom	Document Number Safina	Rev MV	
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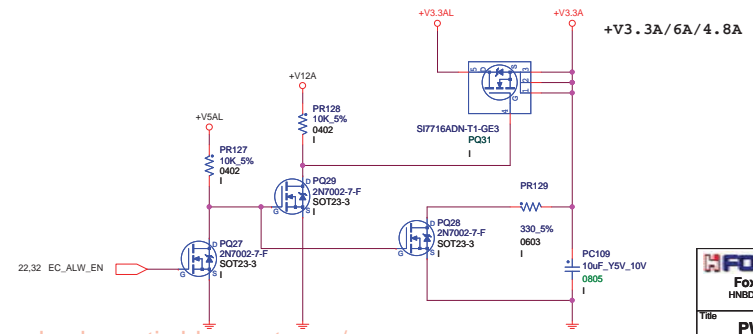
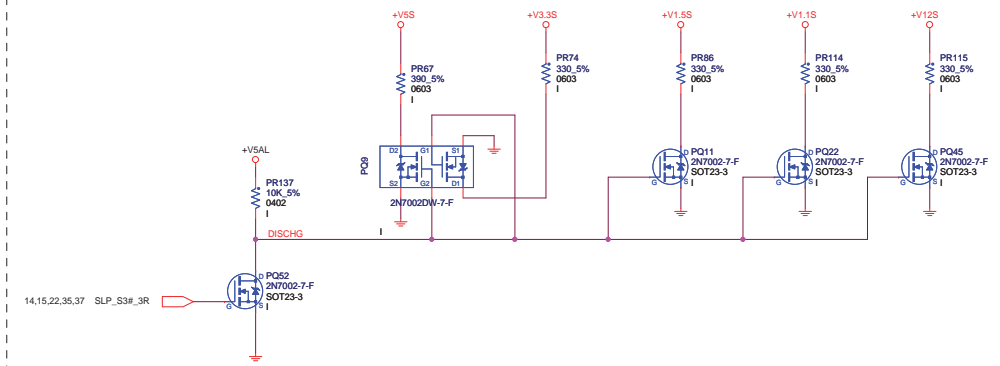
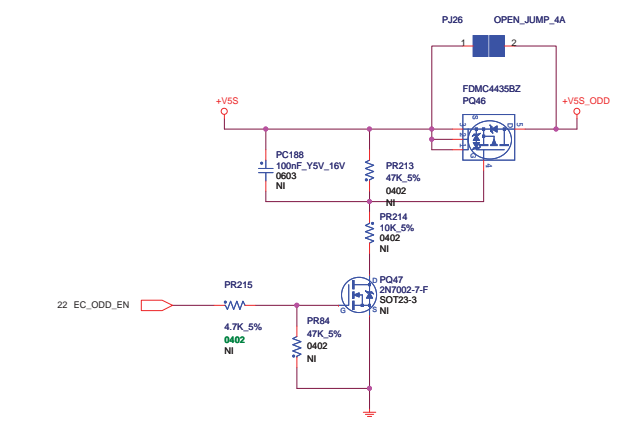
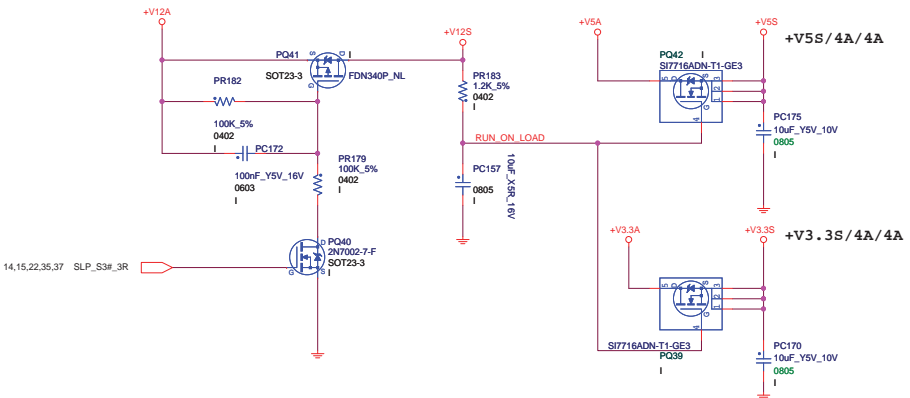
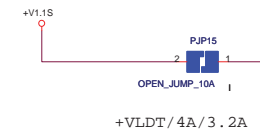
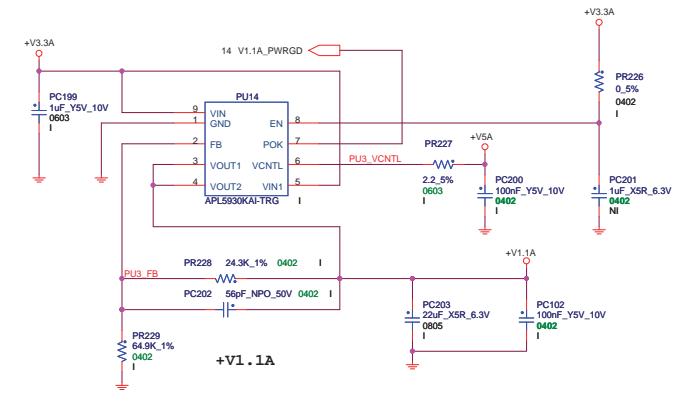
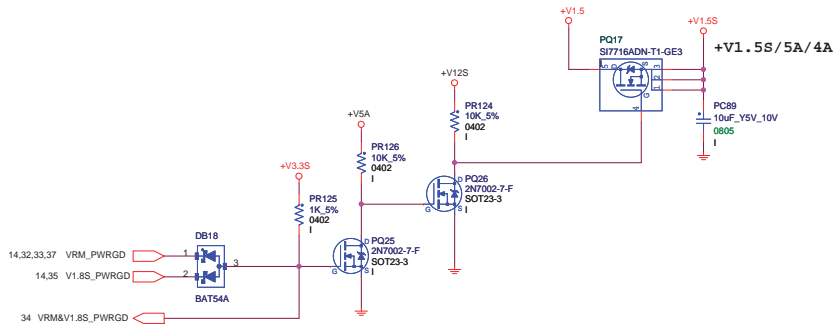
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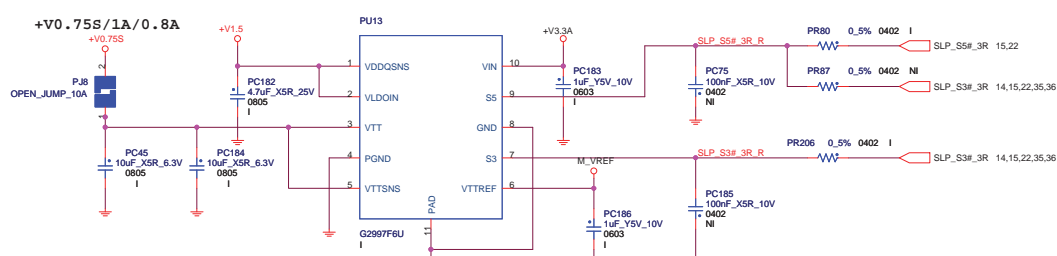
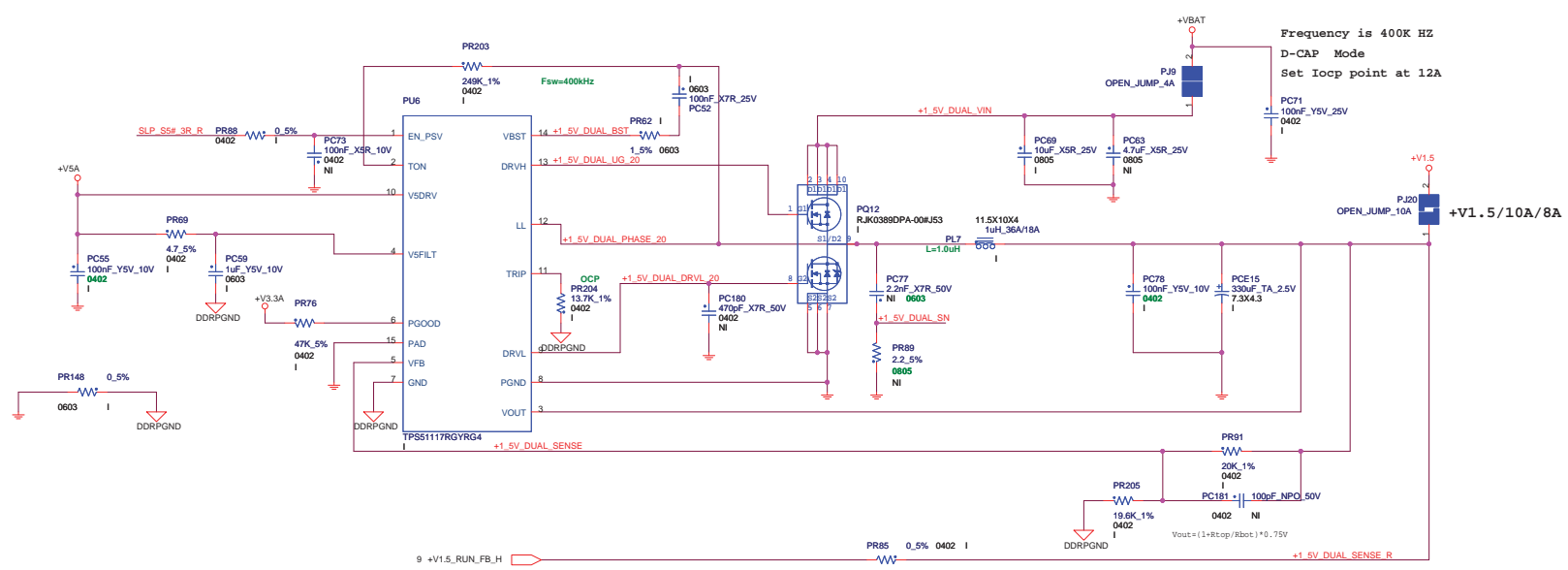
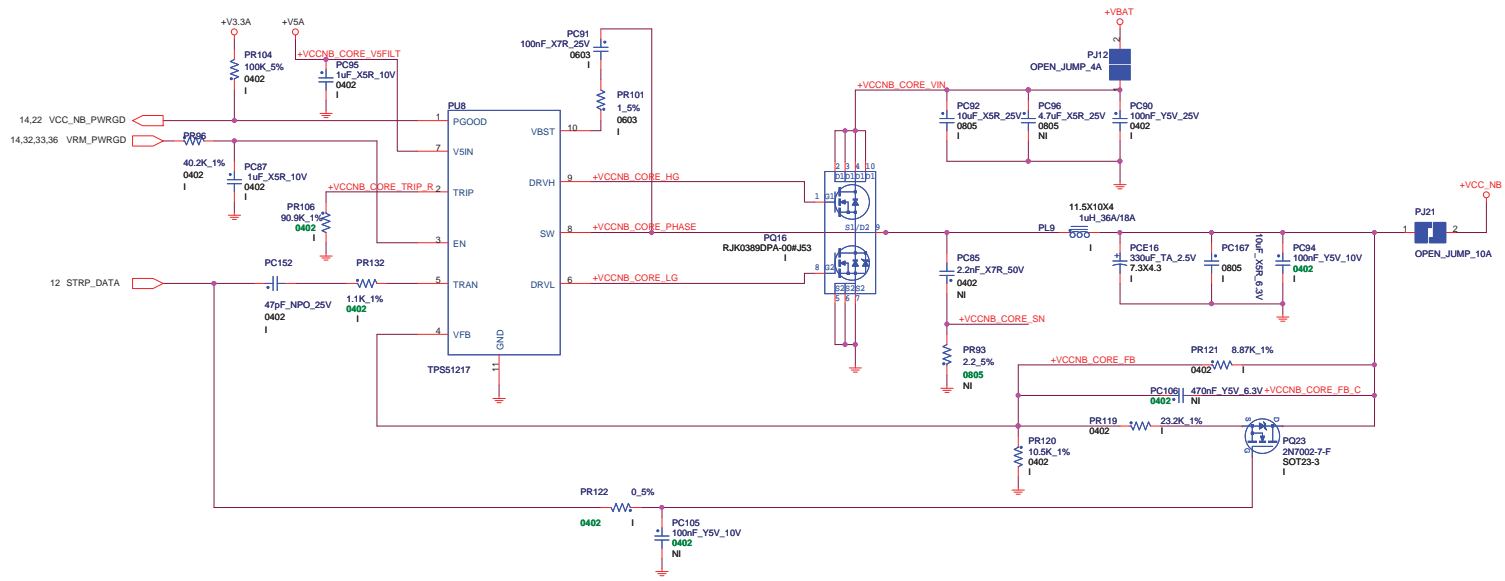
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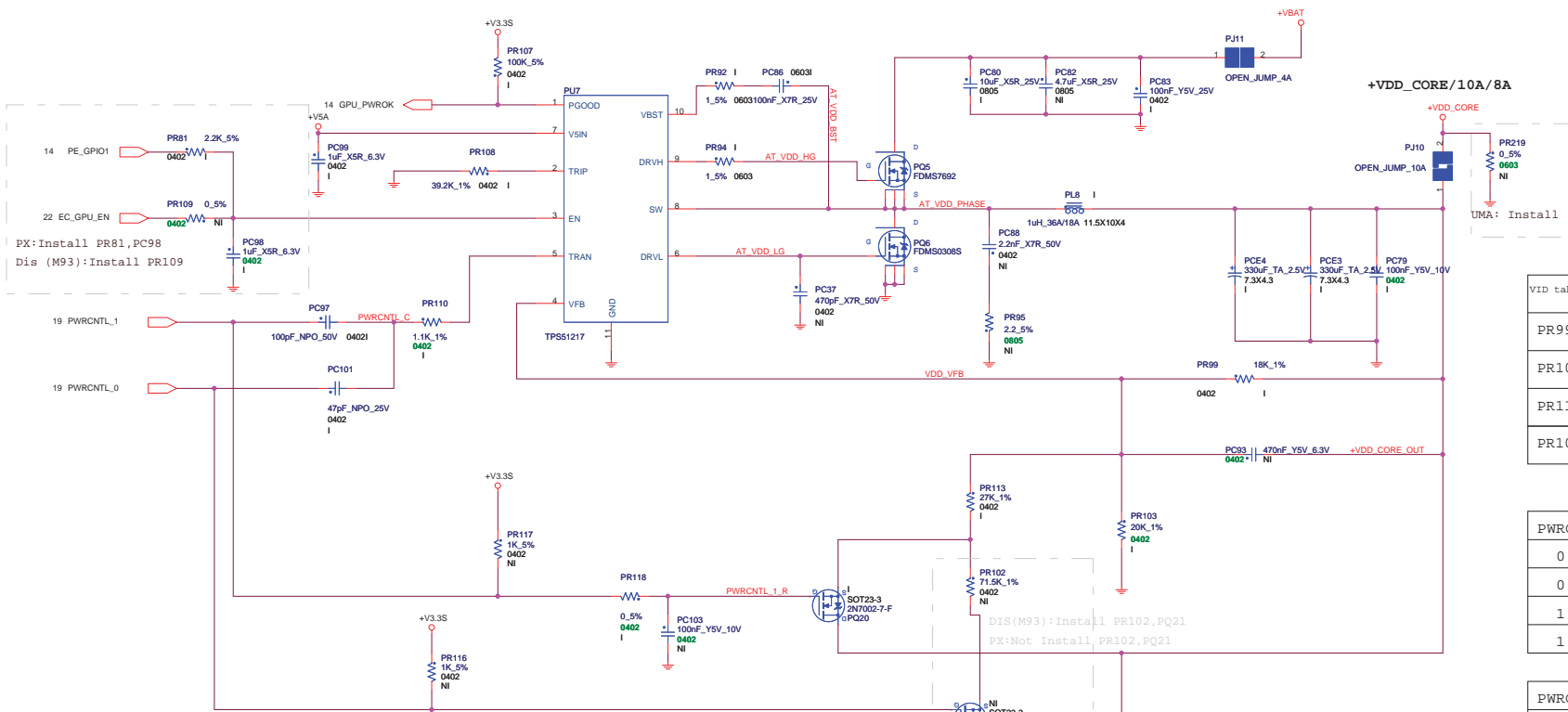
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Frequency is 400K HZ
 D-CAP Mode
 Set Iocp point at 12A

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Title +VCCNB & 1.5VDDR3 +0.75V		Rev MV	
Size Custom	Document Number Safina	Page Modified: Wednesday, April 07, 2010 18:48:18 (UTC+08:00) Sheet 37 of 39	



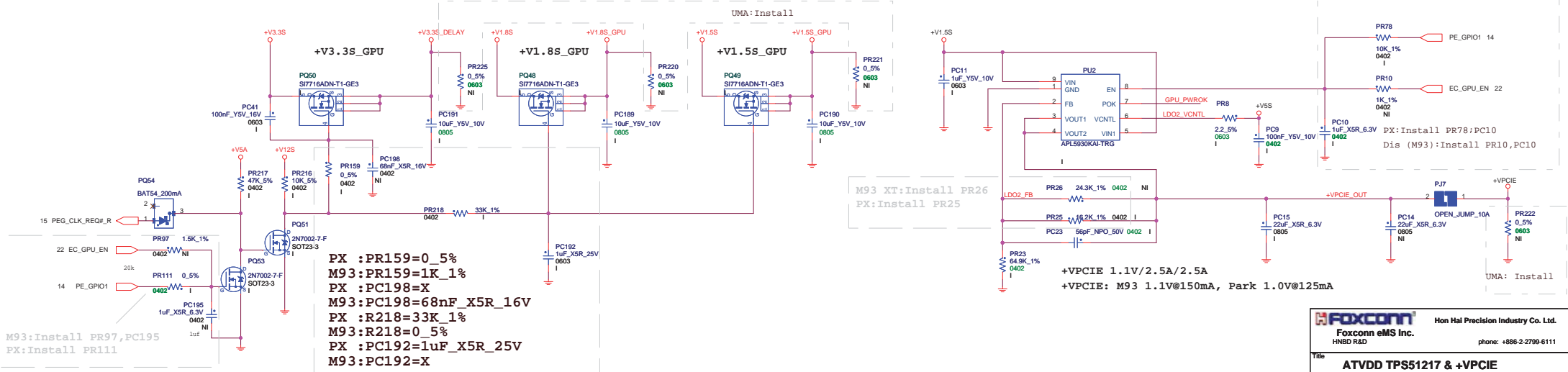
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PR103	20K_1% (610114H00-011-G)	20K_1% (610114H00-011-G)
PR113	28.7K_1% (61011B400-012-G)	27K_1% (610117200-012-G)
PR102	71.5K_1% (611008700-011-G)	N/A

PWRCNTL_1	PWRCNTL_0	M93_XT_S3
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	Park_XT_S3
0	1.12V
1	0.9V

Dis (M93);PX:Install
UMA:Not Install

$$V = 0.6 * (1 + R1/R2)$$

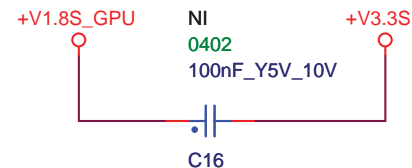
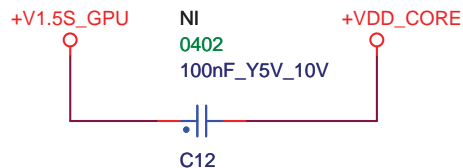
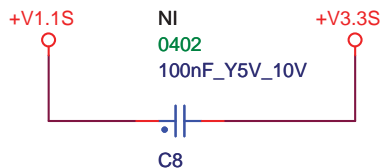
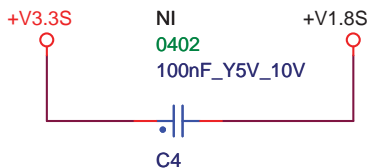
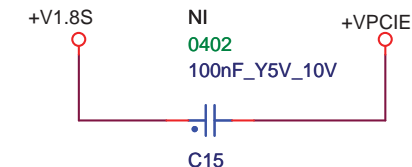
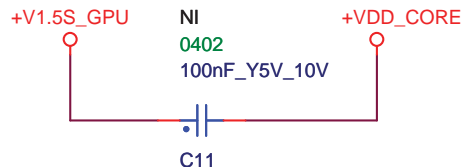
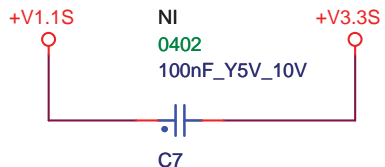
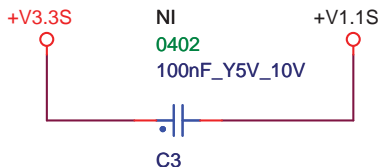
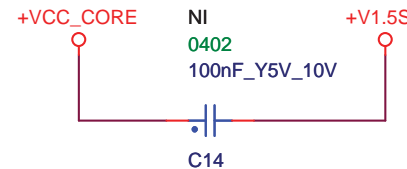
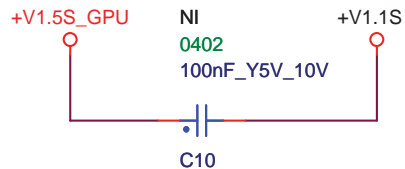
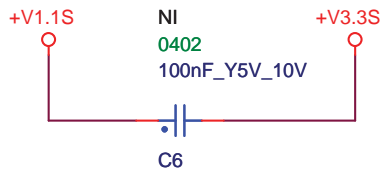
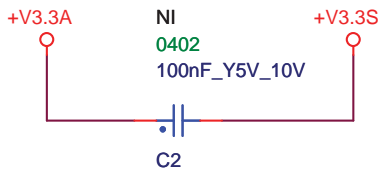
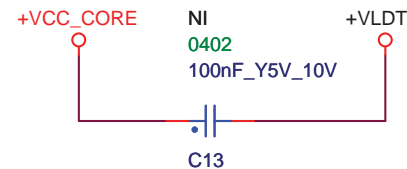
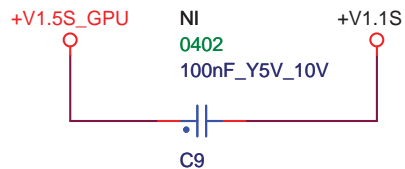
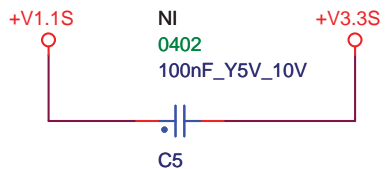
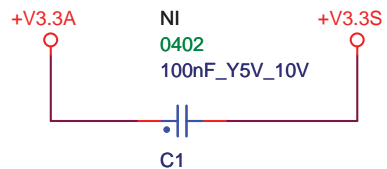


PX :PR159=0_5%
M93:PR159=1K_1%
PX :PC198=X
M93:PC198=68nF_X5R_16V
PX :R218=33K_1%
M93:R218=0_5%
PX :PC192=1uF_X5R_25V
M93:PC192=X

M93 XT:Install PR26
PX:Install PR25

+VPCIE 1.1V/2.5A/2.5A
+VPCIE: M93 1.1V@150mA, Park 1.0V@125mA

M93:Install PR97,PC195
PX:Install PR111



Only for 6 layer M/B use



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Title

SYSTEM BLOCK DIAGRAM

Size

Document Number

Rev

A

Safina

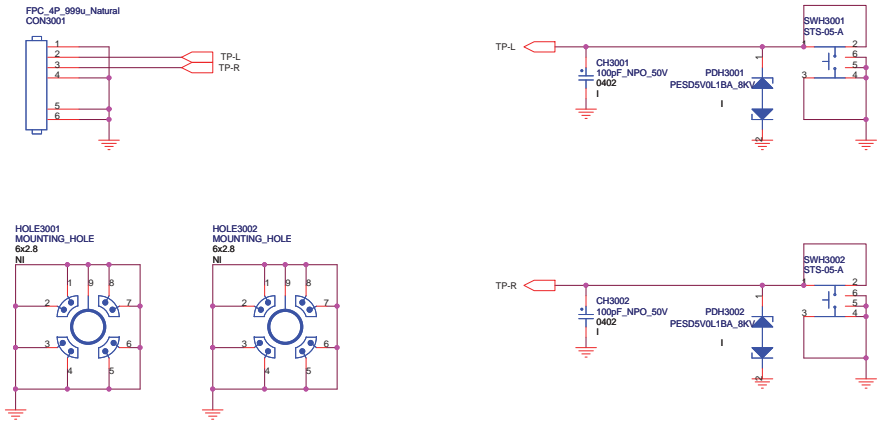
MV

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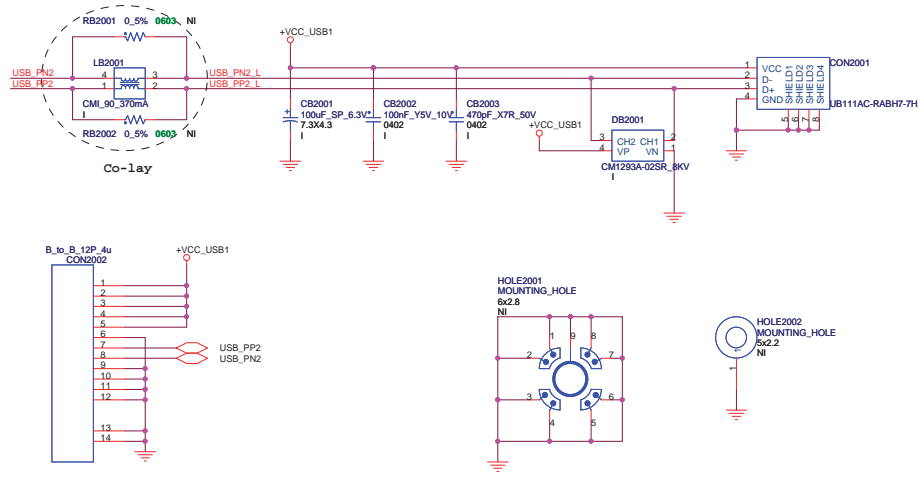
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18:49:16 (UTC/GMT)

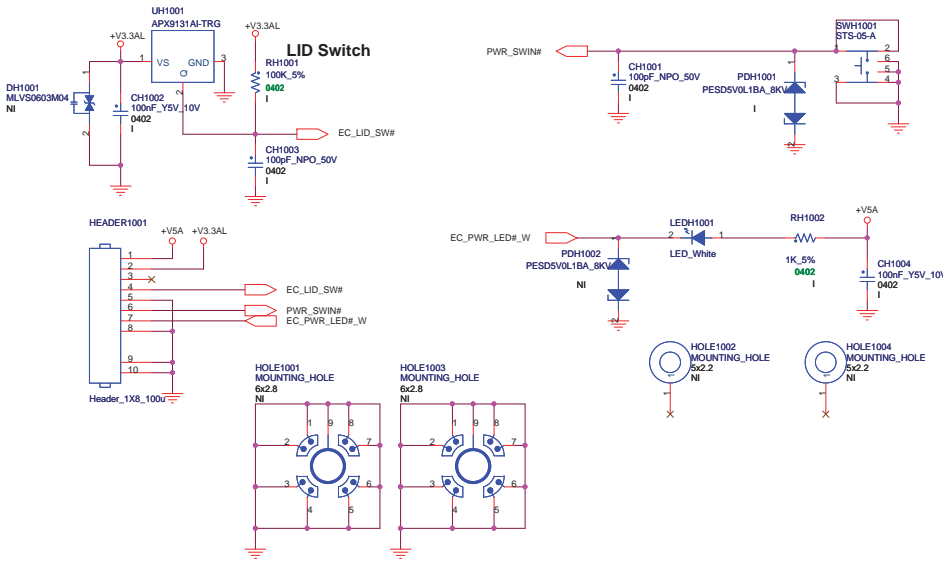
Sheet 39 of 39



SW Board



USB Board



Power Board

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Title: SW Board & USB Board & Power Board			
Size:	Document Number:	Safina	Rev: S1
C			
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