

# Compal confidential

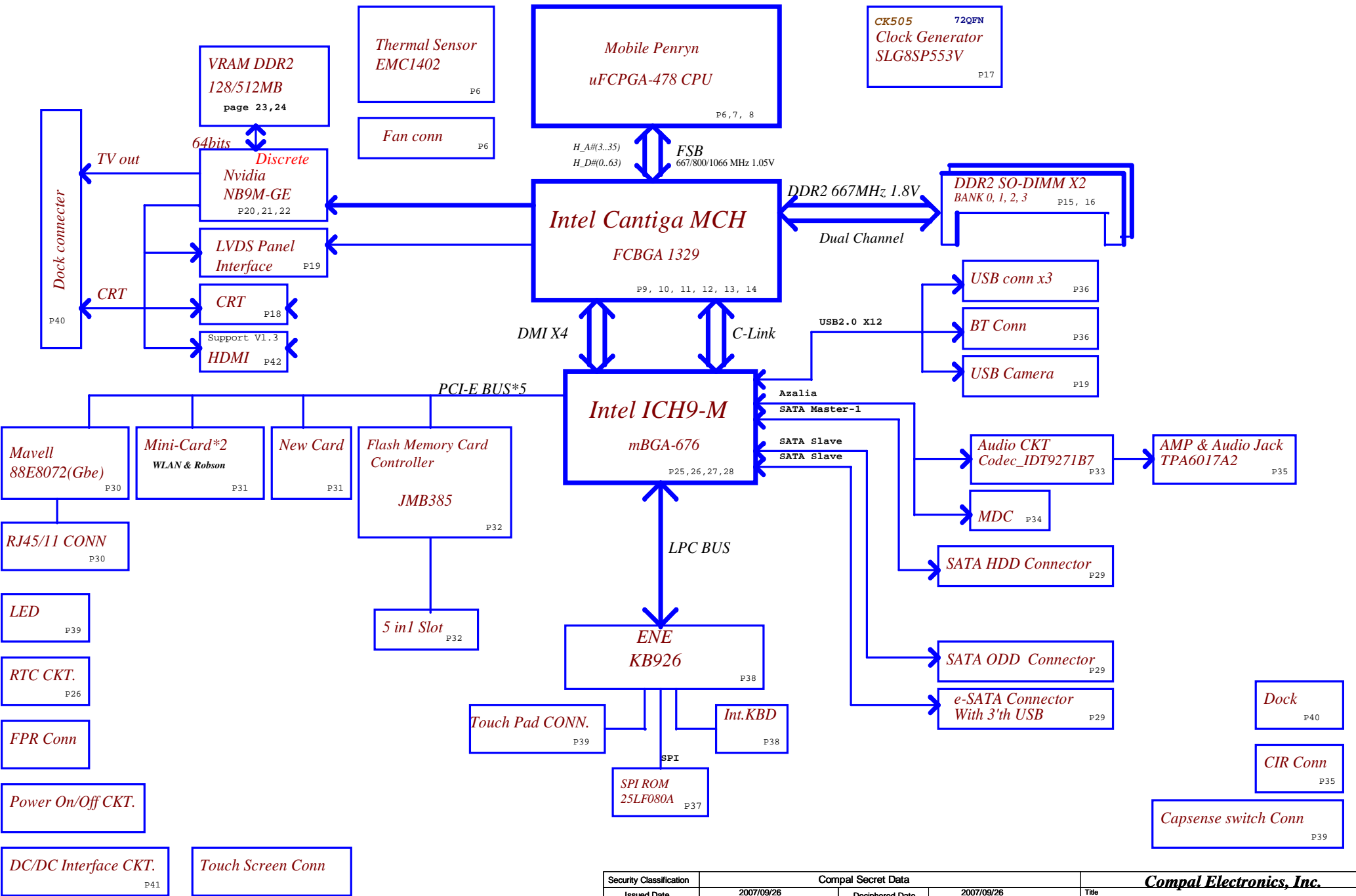
## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_PM+ICH9-M core logic

2007-09-16

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				Montevina Consumer discrete	0.1	
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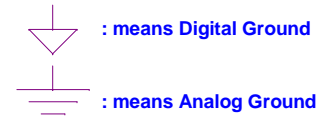
### Voltage Rails

O MEANS ON

X MEANS OFF

power plane \ State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### Symbol Note :



@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

### USB assignment:

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card
- USB-10 X
- USB-11 X

### PCIe assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 New Card
- PCIe-5 Card reader
- PCIe-6 GLAN (Marvell)

### SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	V	V	V
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	X

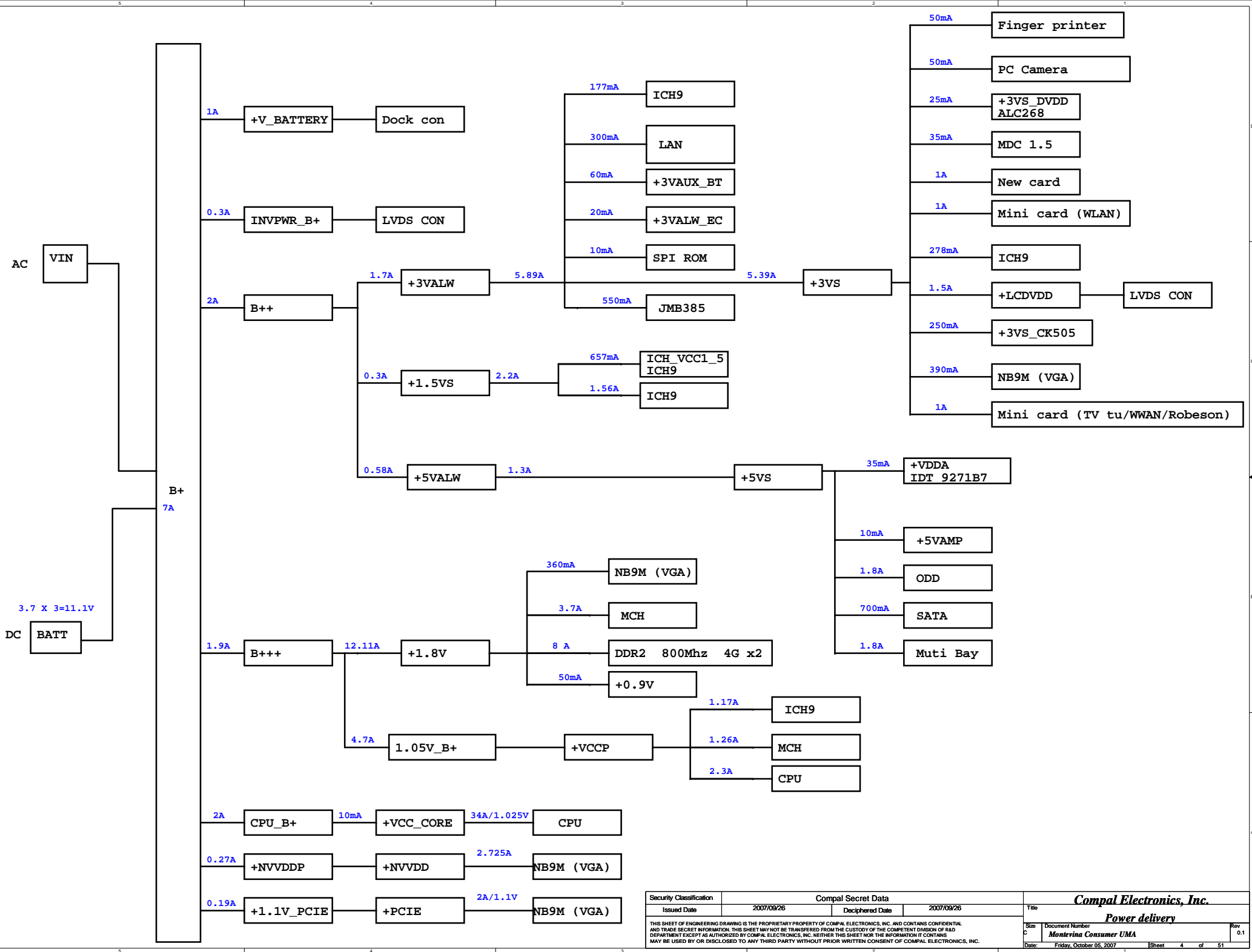
### NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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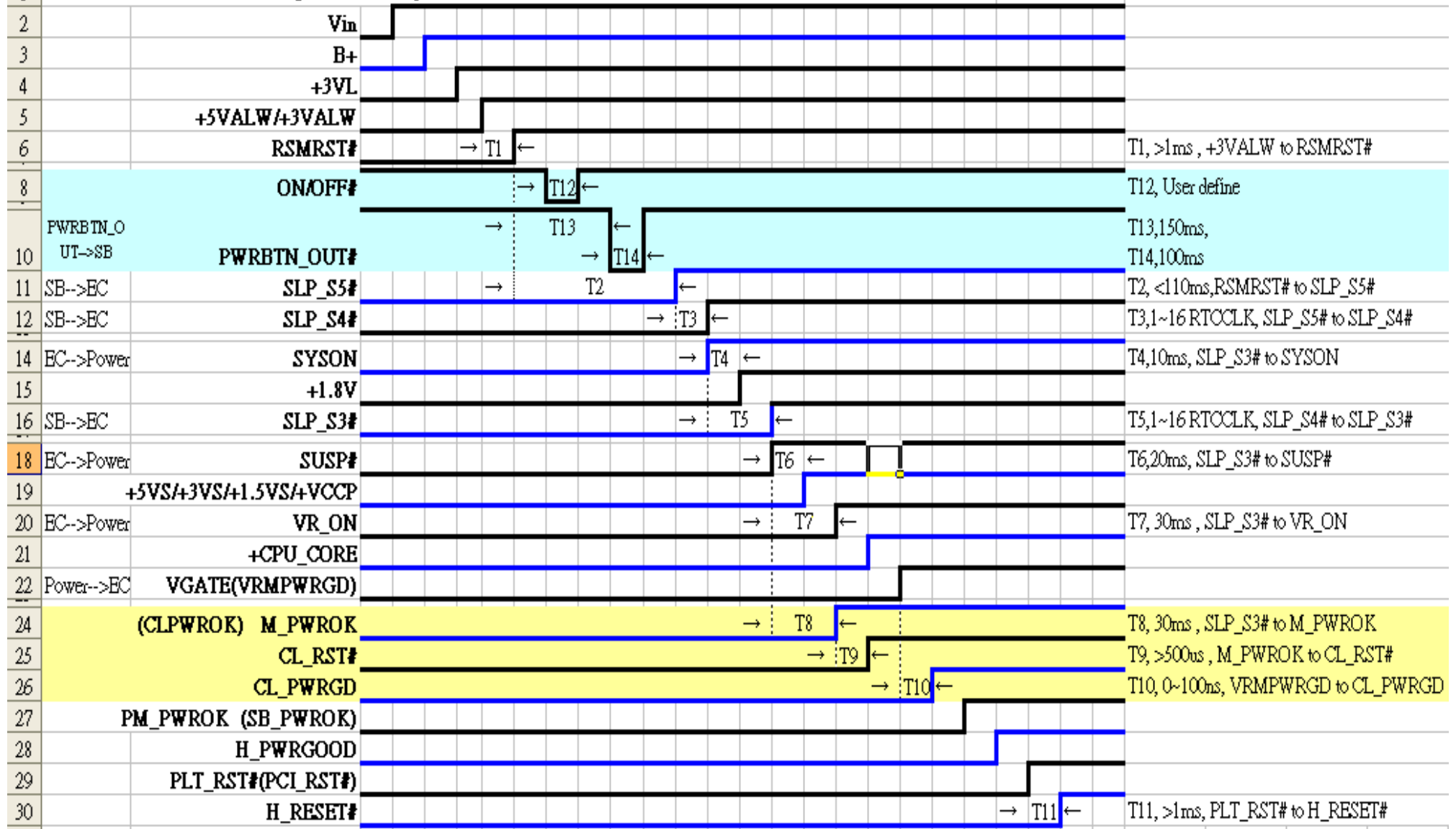


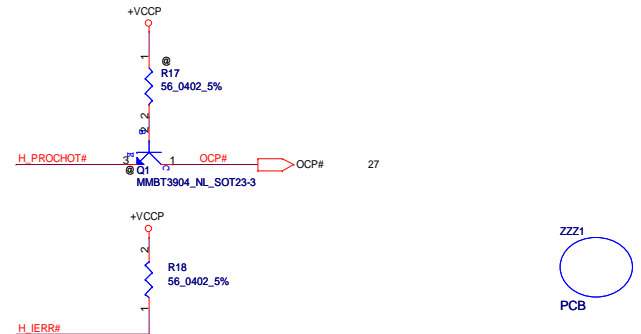
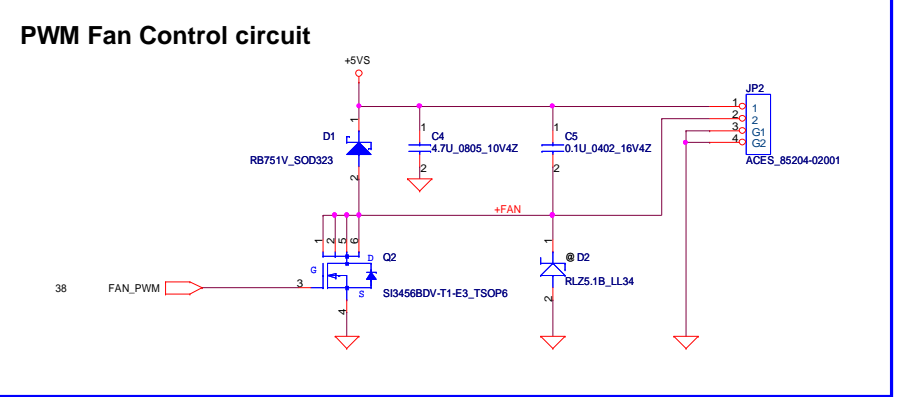
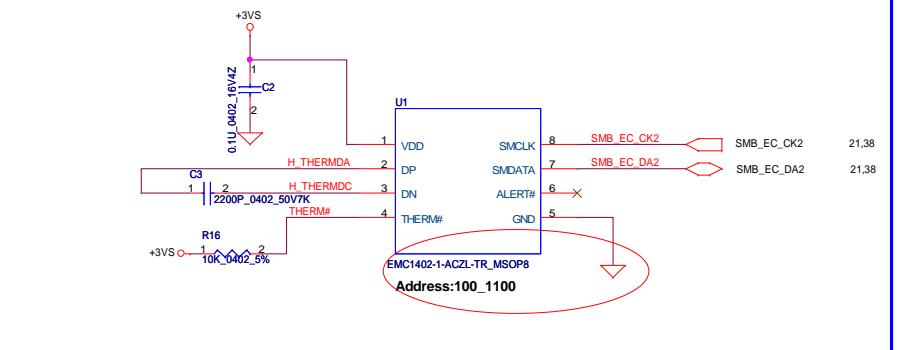
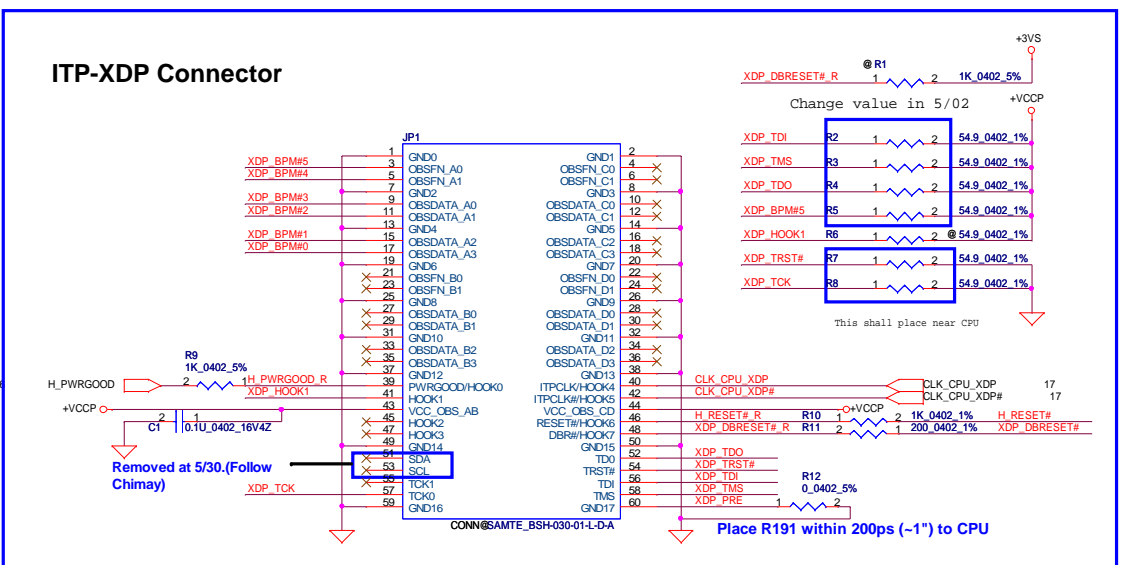
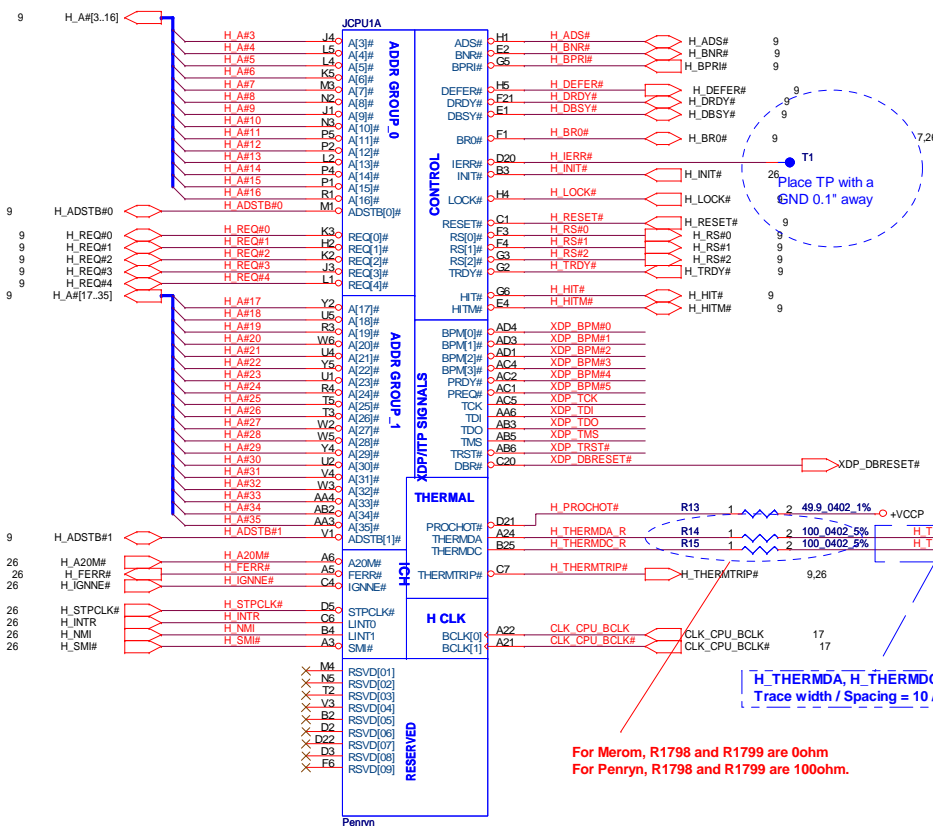
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<b>Compal Electronics, Inc.</b>	
<b>Power delivery</b>	
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# JAL50 power sequence AC mode

96.09.03.



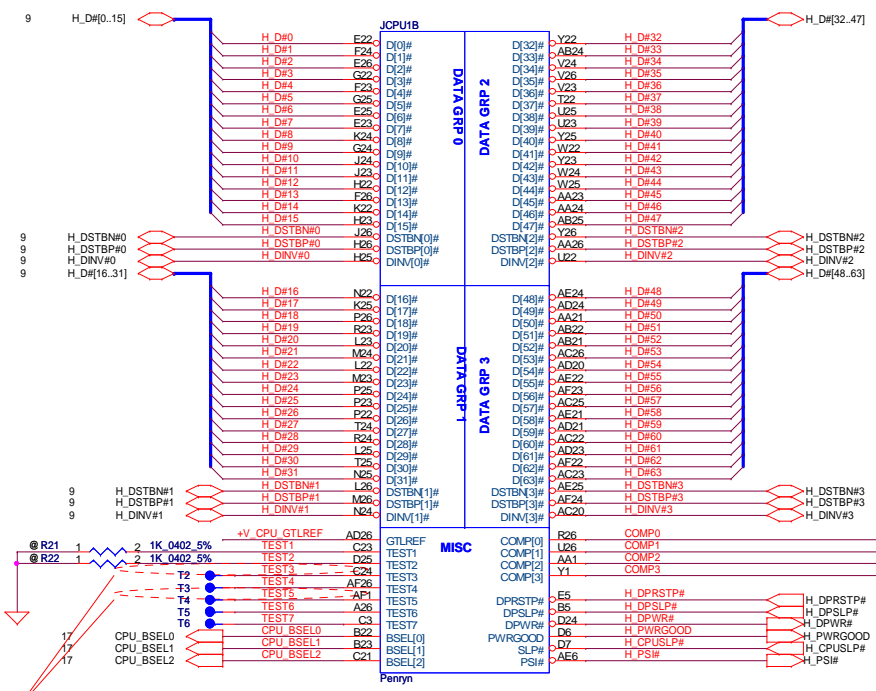


H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

For Merom, R1798 and R1799 are 0ohm  
For Penryn, R1798 and R1799 are 100ohm.

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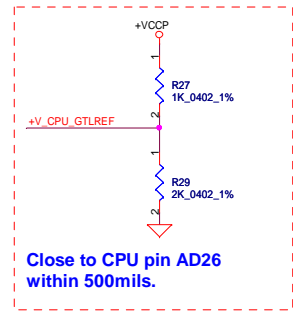
Compal Electronics, Inc.		
Penryn(1/3)-AGTL+/ITP-XDP		
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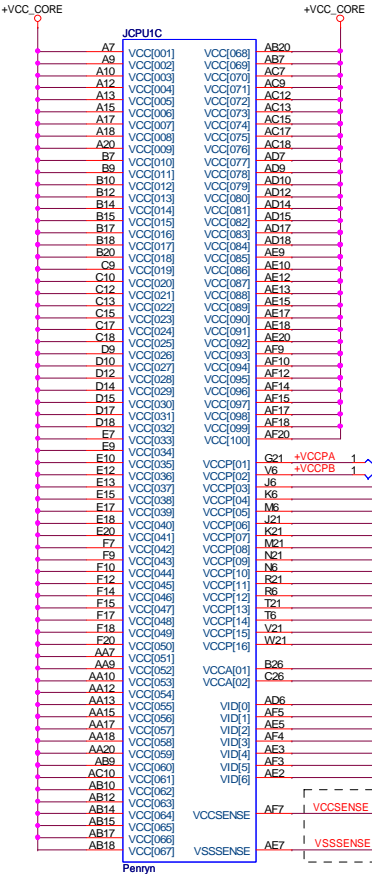
\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

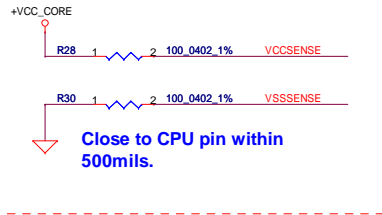
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 207/725.



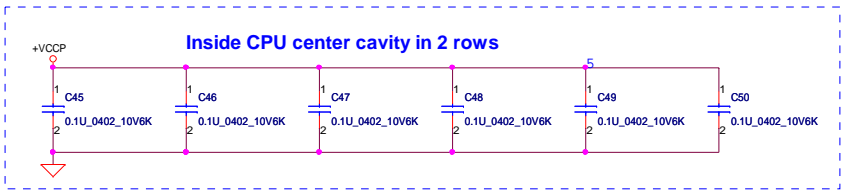
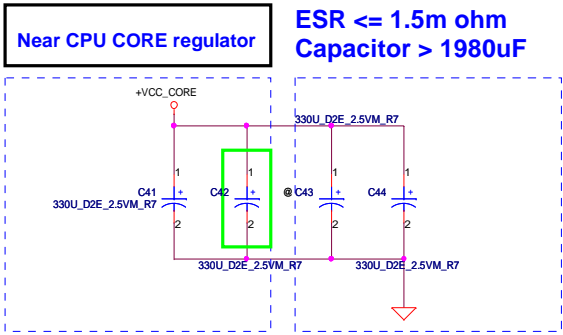
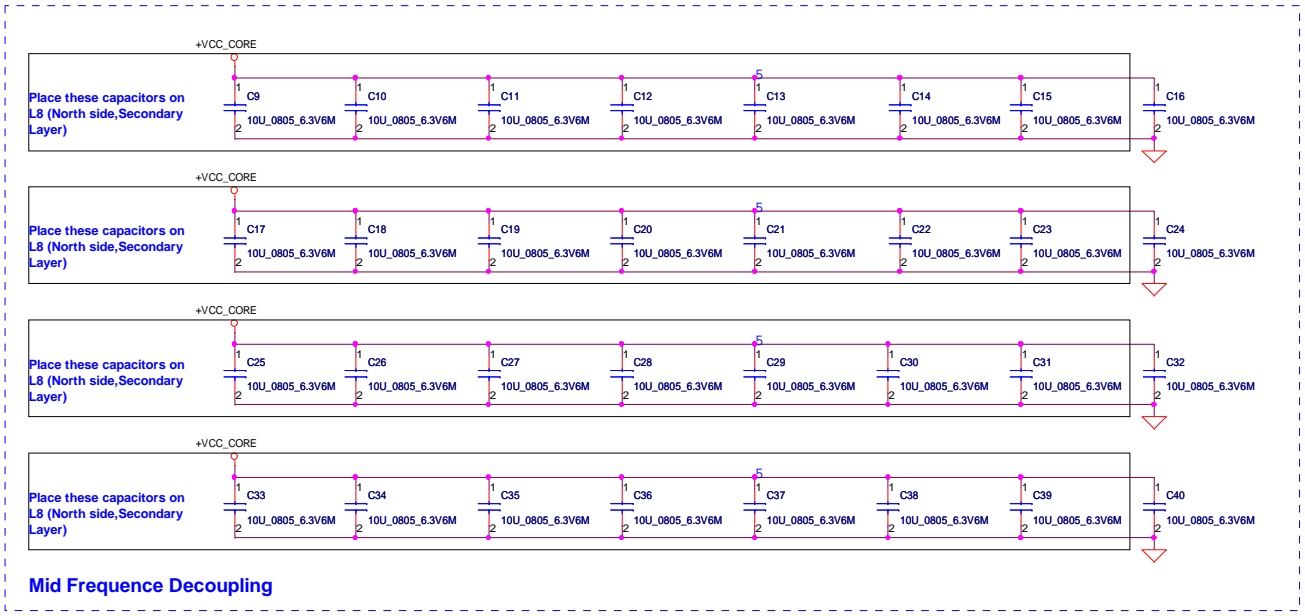
Close to CPU pin within 500mils.

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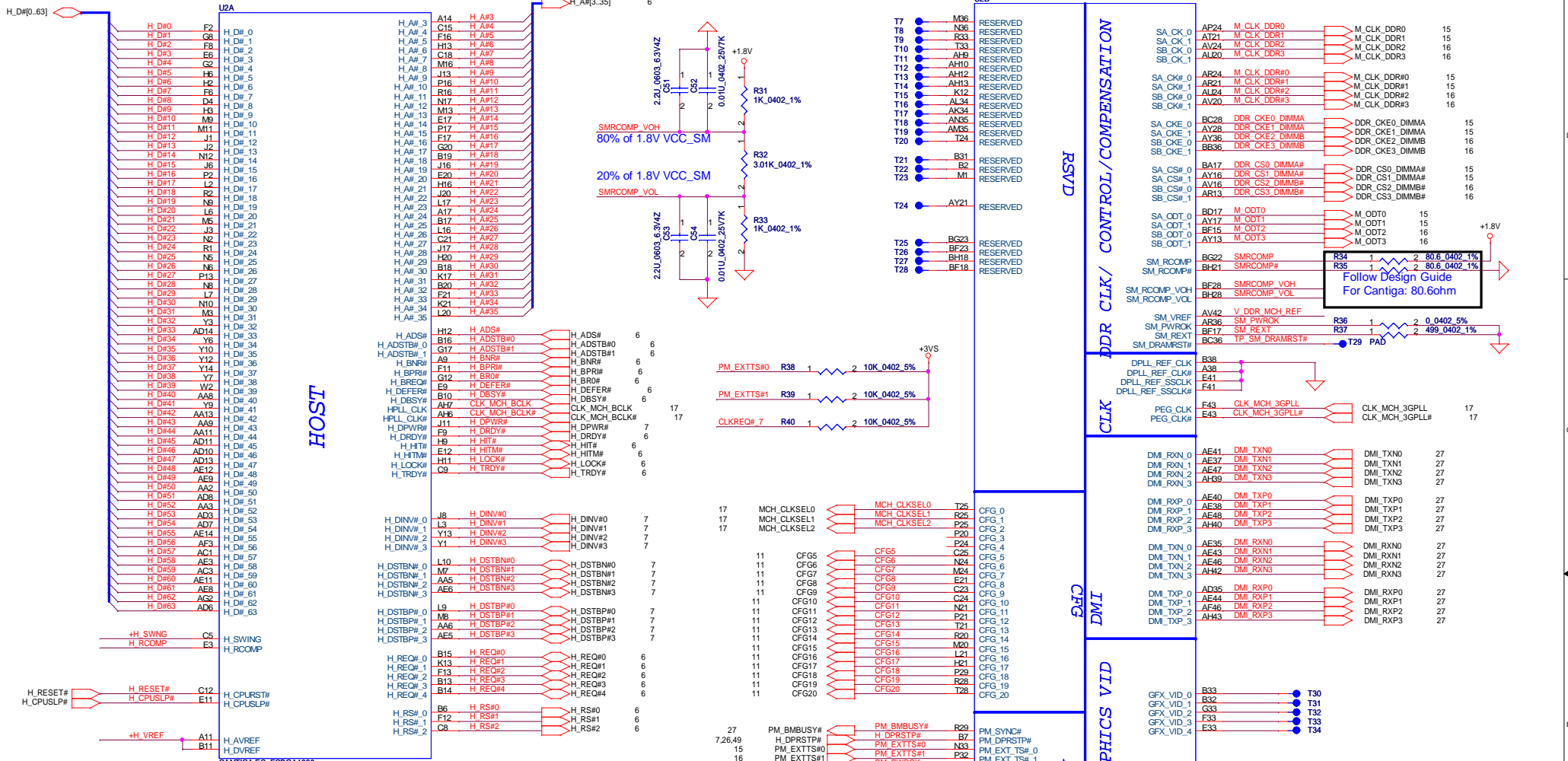
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Penryn(2/3)-AGTL+/ICP-XDP		
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JCPU10		
A4	VSS1001	VSS1002
A8	VSS1003	VSS1004
A11	VSS1005	VSS1006
A14	VSS1007	VSS1008
A16	VSS1009	VSS1010
A19	VSS1011	VSS1012
A23	VSS1013	VSS1014
A27	VSS1015	VSS1016
B2	VSS1017	VSS1018
B6	VSS1019	VSS1020
B8	VSS1021	VSS1022
B11	VSS1023	VSS1024
B13	VSS1025	VSS1026
B16	VSS1027	VSS1028
B19	VSS1029	VSS1030
B21	VSS1031	VSS1032
B24	VSS1033	VSS1034
C5	VSS1035	VSS1036
C8	VSS1037	VSS1038
C11	VSS1039	VSS1040
C14	VSS1041	VSS1042
C16	VSS1043	VSS1044
C19	VSS1045	VSS1046
C2	VSS1047	VSS1048
C22	VSS1049	VSS1050
C25	VSS1051	VSS1052
D1	VSS1053	VSS1054
D4	VSS1055	VSS1056
D8	VSS1057	VSS1058
D11	VSS1059	VSS1060
D13	VSS1061	VSS1062
D16	VSS1063	VSS1064
D19	VSS1065	VSS1066
D23	VSS1067	VSS1068
D26	VSS1069	VSS1070
E3	VSS1071	VSS1072
E6	VSS1073	VSS1074
E8	VSS1075	VSS1076
E11	VSS1077	VSS1078
E14	VSS1079	VSS1080
E16	VSS1081	VSS1082
E19	VSS1083	VSS1084
E21	VSS1085	VSS1086
E24	VSS1087	VSS1088
F5	VSS1089	VSS1090
F8	VSS1091	VSS1092
F11	VSS1093	VSS1094
F13	VSS1095	VSS1096
F16	VSS1097	VSS1098
F19	VSS1099	VSS1100
F2	VSS1101	VSS1102
F22	VSS1103	VSS1104
F25	VSS1105	VSS1106
G4	VSS1107	VSS1108
G1	VSS1109	VSS1110
G23	VSS1111	VSS1112
G26	VSS1113	VSS1114
H3	VSS1115	VSS1116
H6	VSS1117	VSS1118
H11	VSS1119	VSS1120
H24	VSS1121	VSS1122
J2	VSS1123	VSS1124
J5	VSS1125	VSS1126
J22	VSS1127	VSS1128
J25	VSS1129	VSS1130
K1	VSS1131	VSS1132
K4	VSS1133	VSS1134
K23	VSS1135	VSS1136
K26	VSS1137	VSS1138
L3	VSS1139	VSS1140
L6	VSS1141	VSS1142
L21	VSS1143	VSS1144
L24	VSS1145	VSS1146
M2	VSS1147	VSS1148
M5	VSS1149	VSS1150
M22	VSS1151	VSS1152
M25	VSS1153	VSS1154
N1	VSS1155	VSS1156
N4	VSS1157	VSS1158
N23	VSS1159	VSS1160
N26	VSS1161	VSS1162
P3	VSS1163	VSS1164

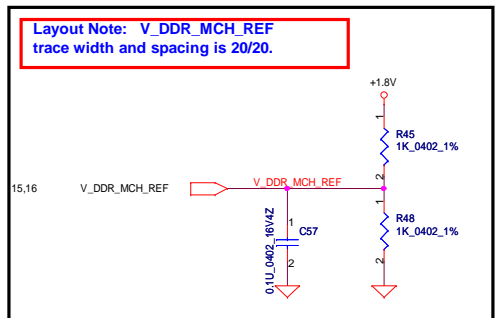
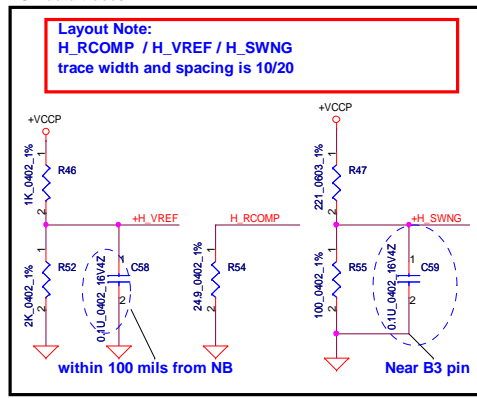


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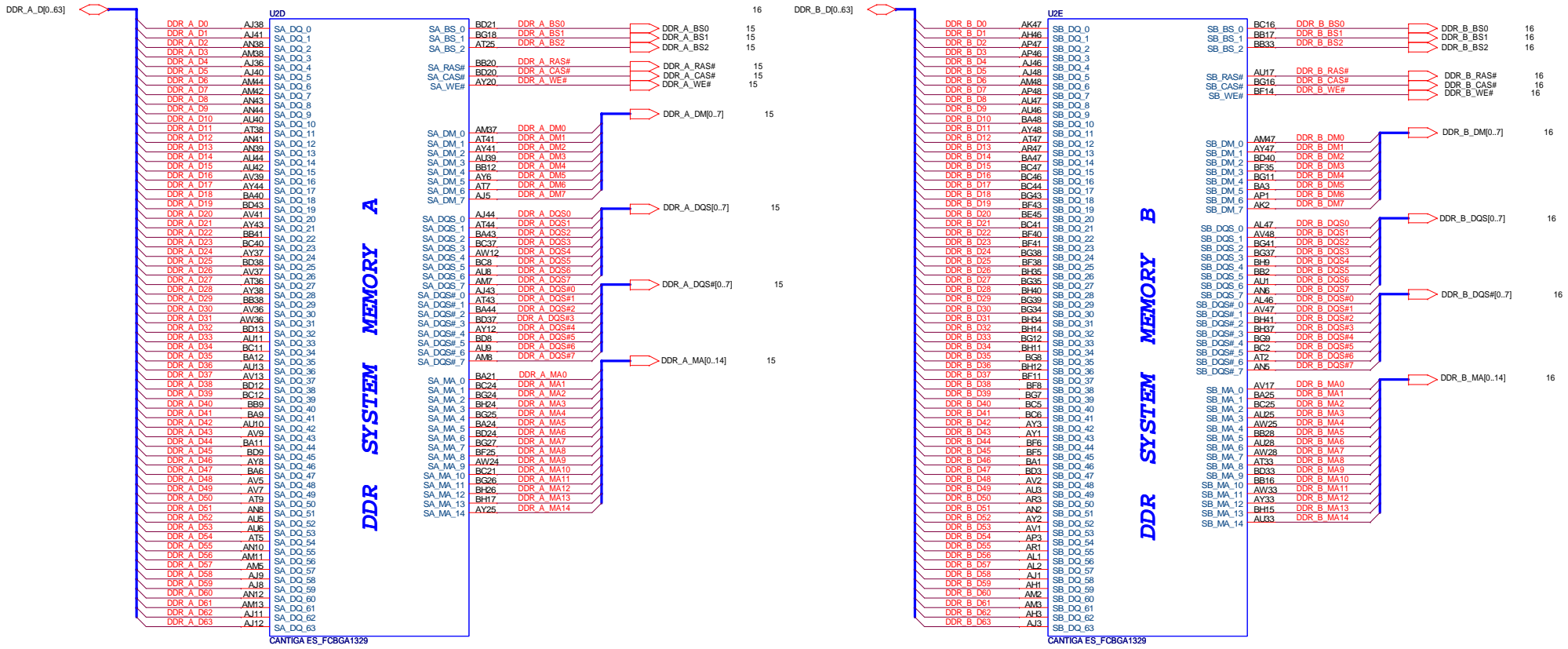




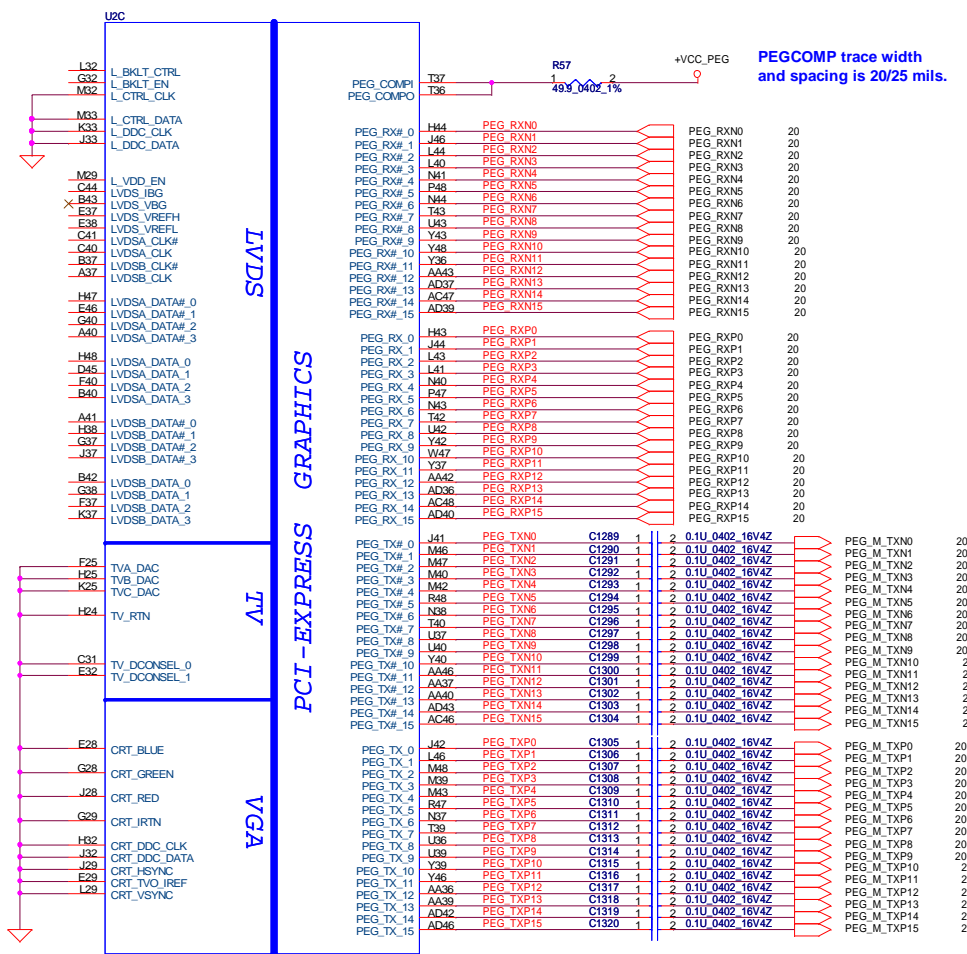
**Layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



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<p>Compal Electronics, Inc. Cantiga (I/6)-AGTL/DMI/DDR</p>			<p>Montevina Consumer Discrete</p>	
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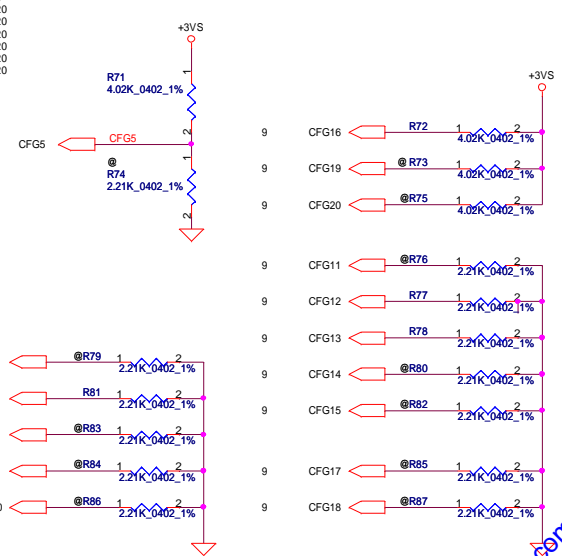


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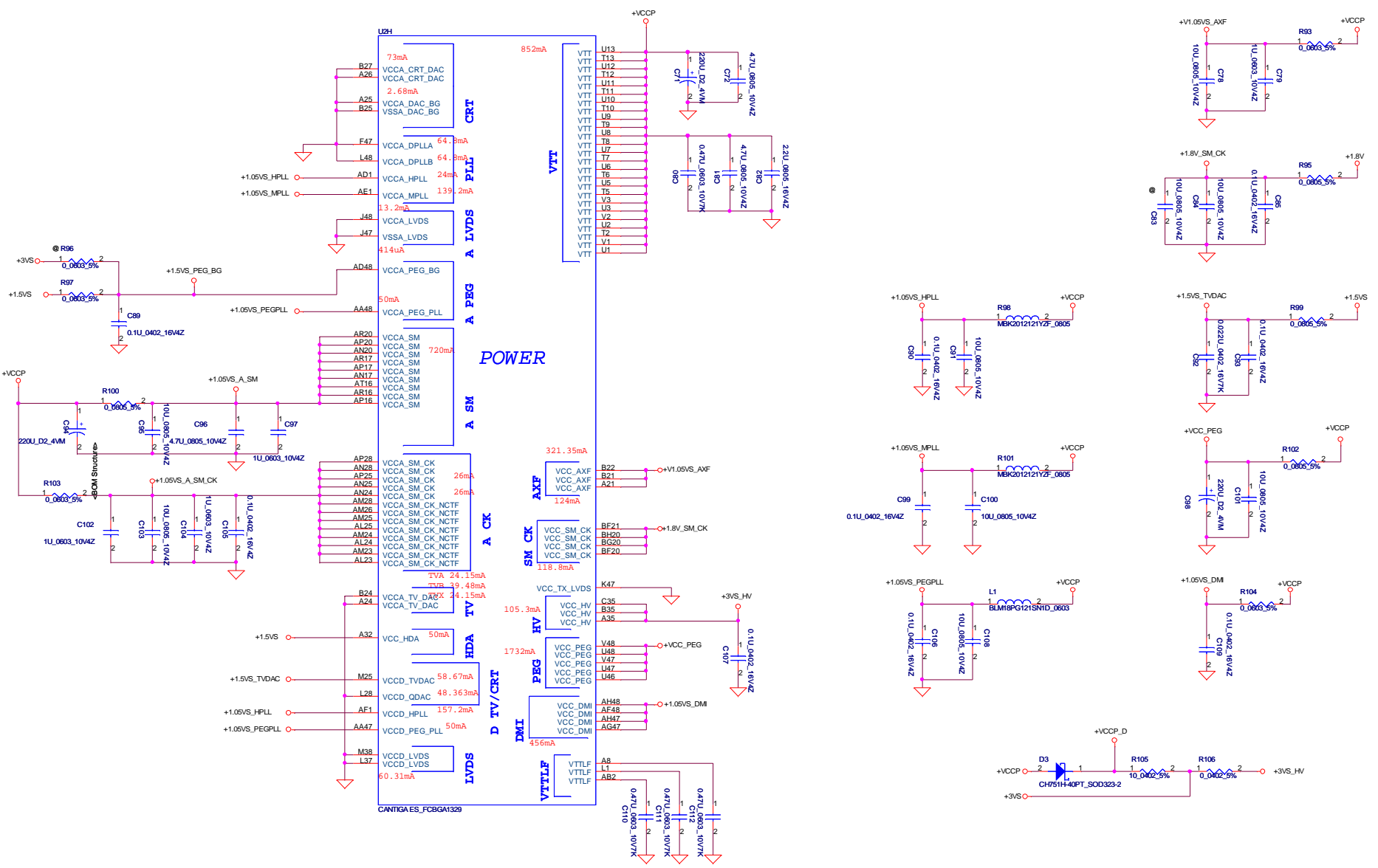


### Strap Pin Table

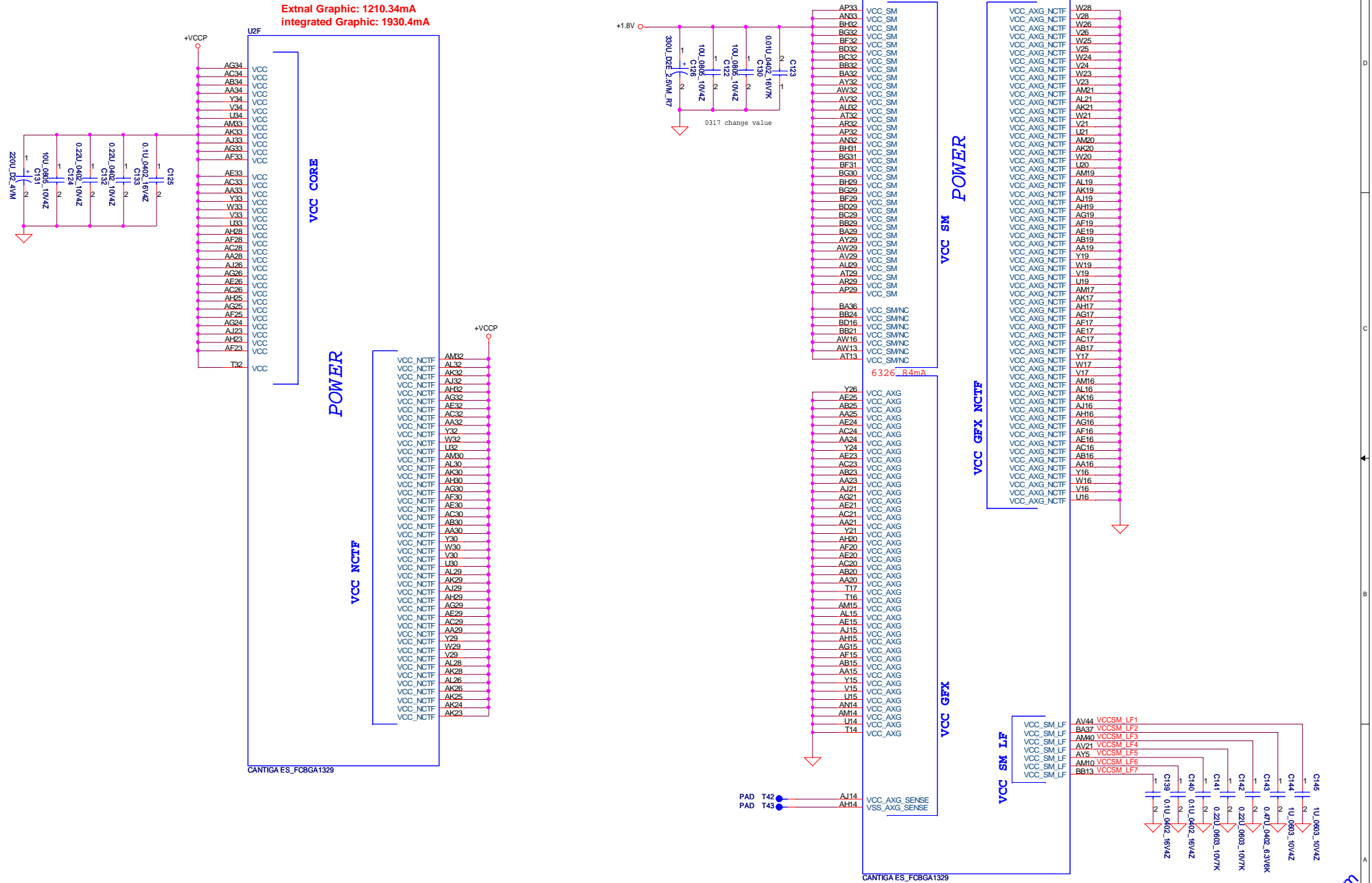
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



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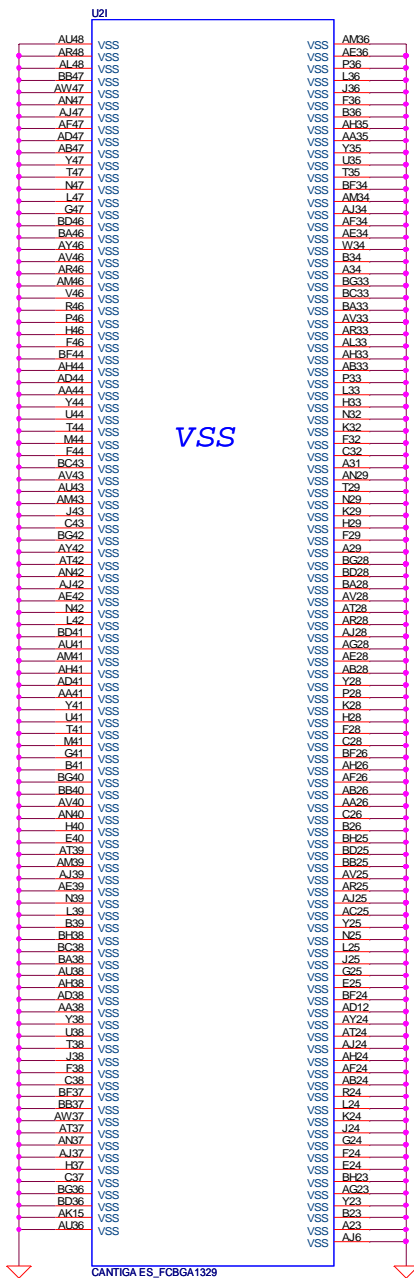


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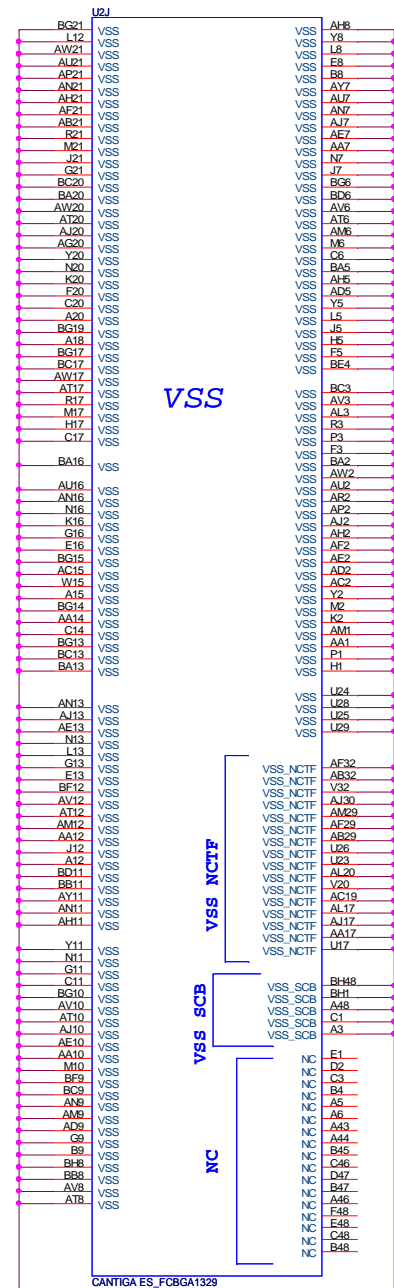


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Cantiga(5/6)-PWR/GND		
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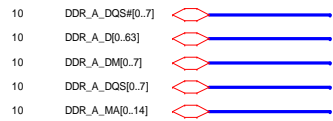


CANTIGA\_ES\_FCBGA1329

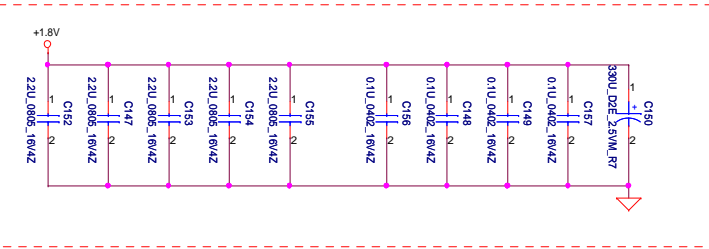


CANTIGA\_ES\_FCBGA1329

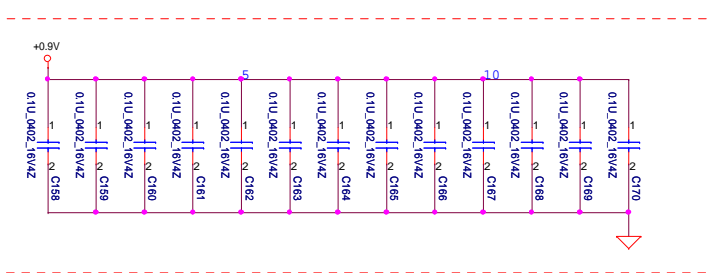
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Size Custom	Document Number	Rev		0.1	
Date:	Friday, October 05, 2007	Sheet	14	of	51



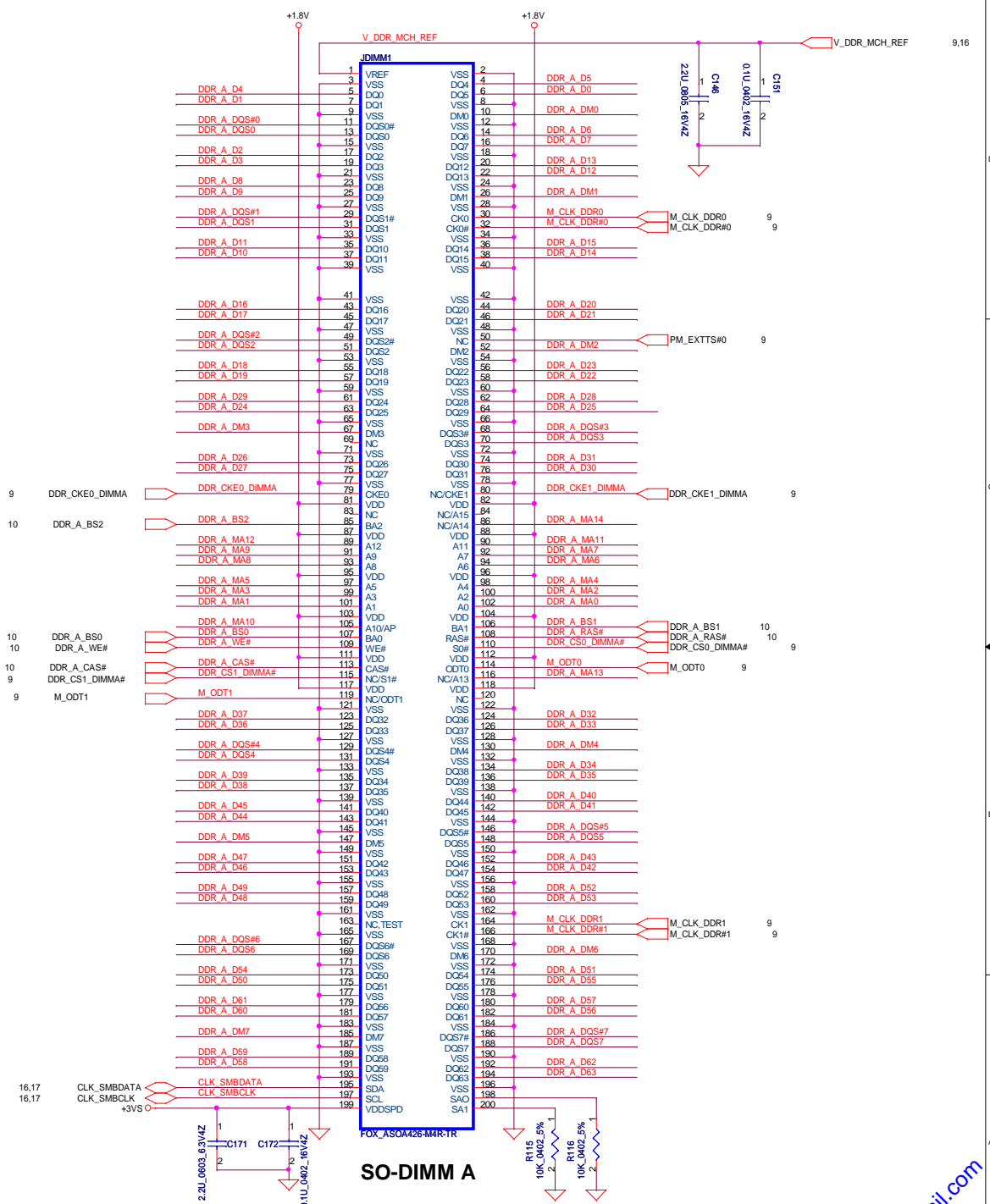
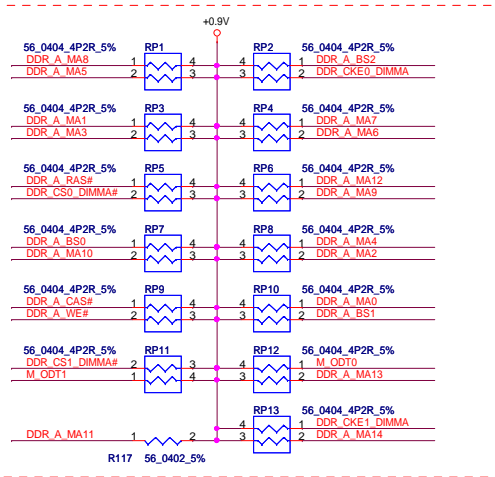
**Layout Note:**  
Place near JP3



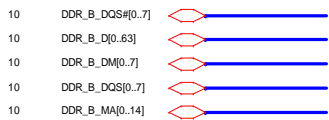
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V5



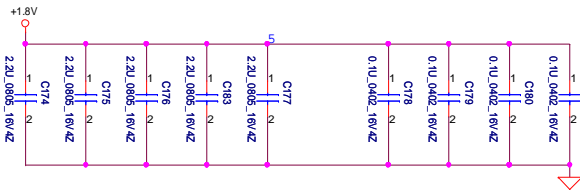
**Layout Note:**  
Place these resistor closely JP3, all trace length Max=1.5"



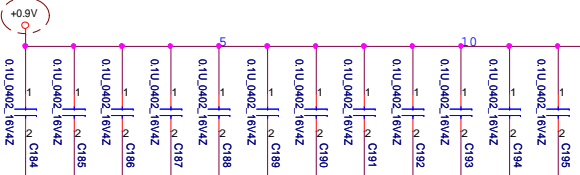
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Issued Date	2007/09/26	Deciphered Date	2007/09/26
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			Rev: 0.1



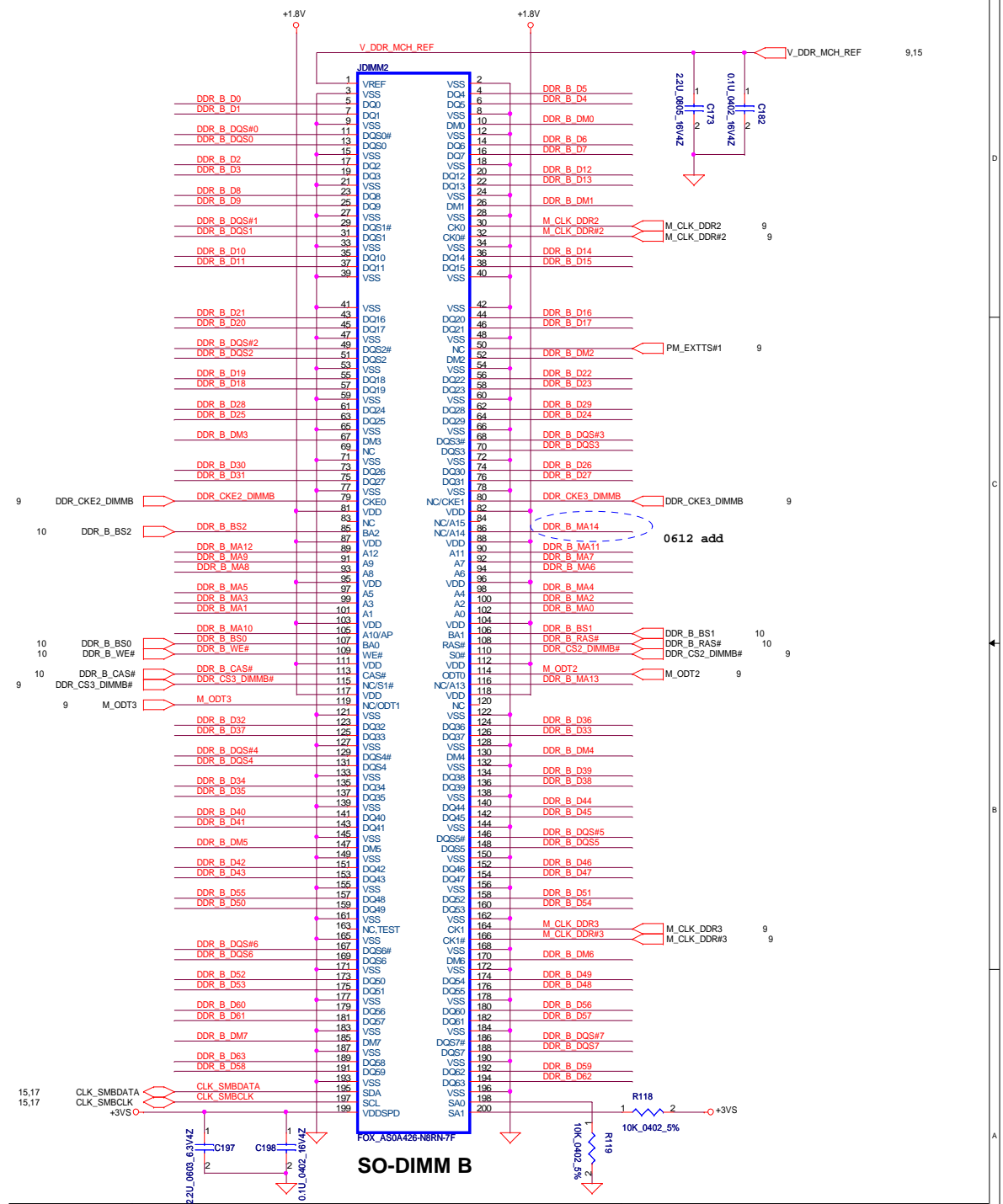
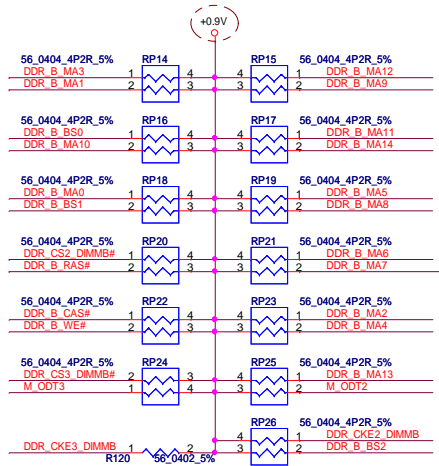
**Layout Note:**  
Place near JP19



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP3, all trace length Max=1.5"

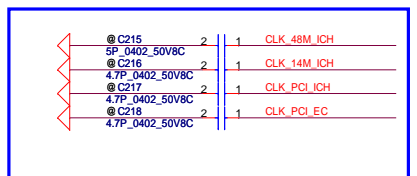
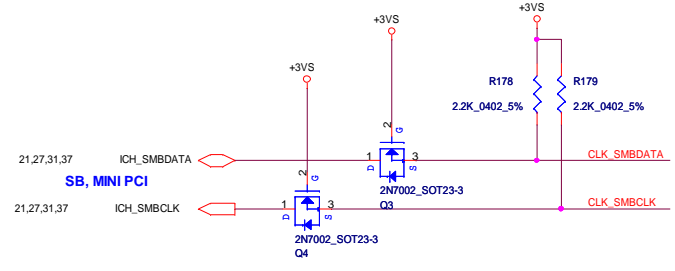
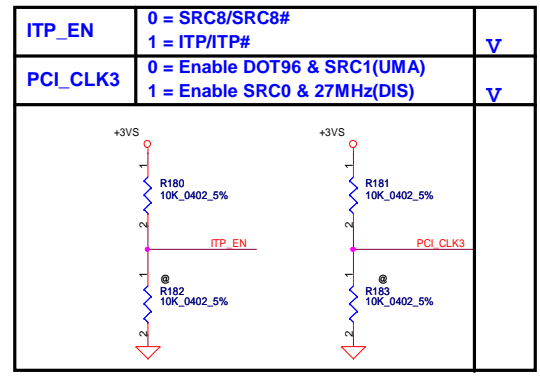
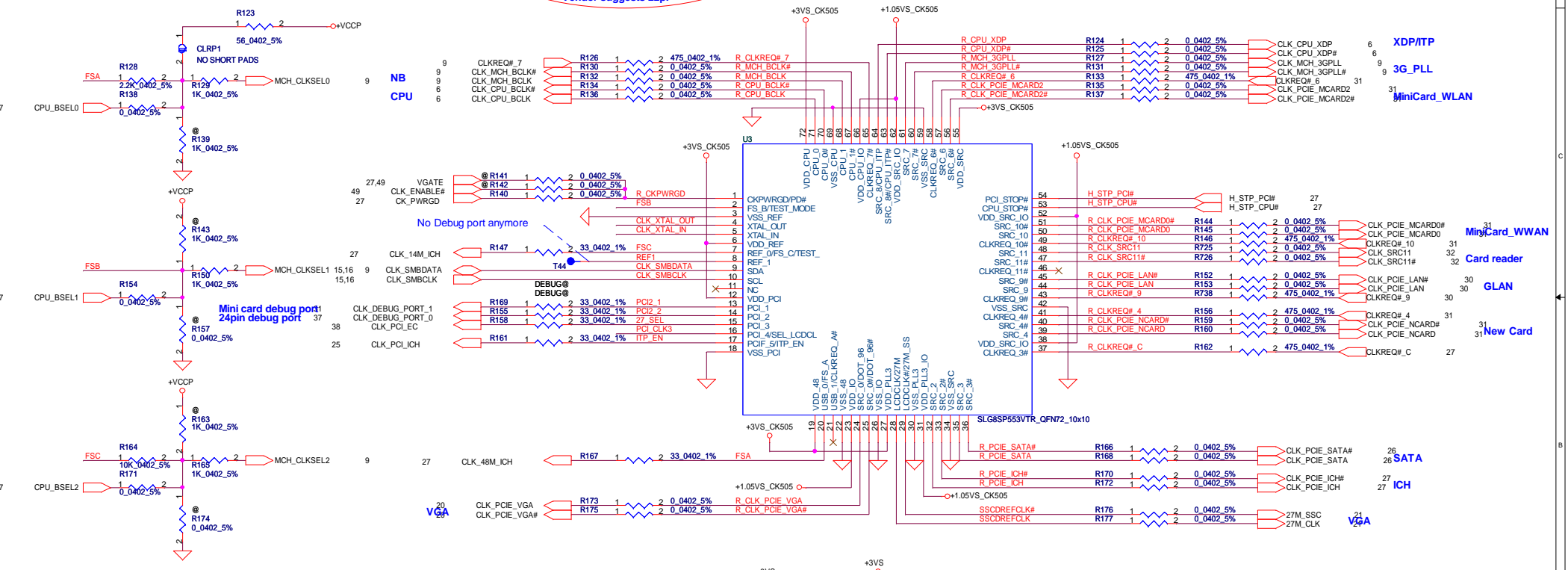
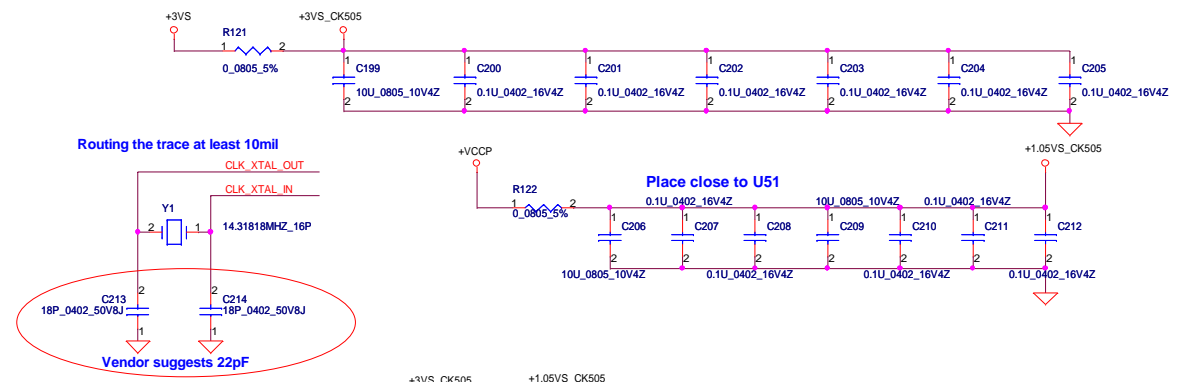


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Date:	Friday, October 05, 2007	Sheet	16 of 51

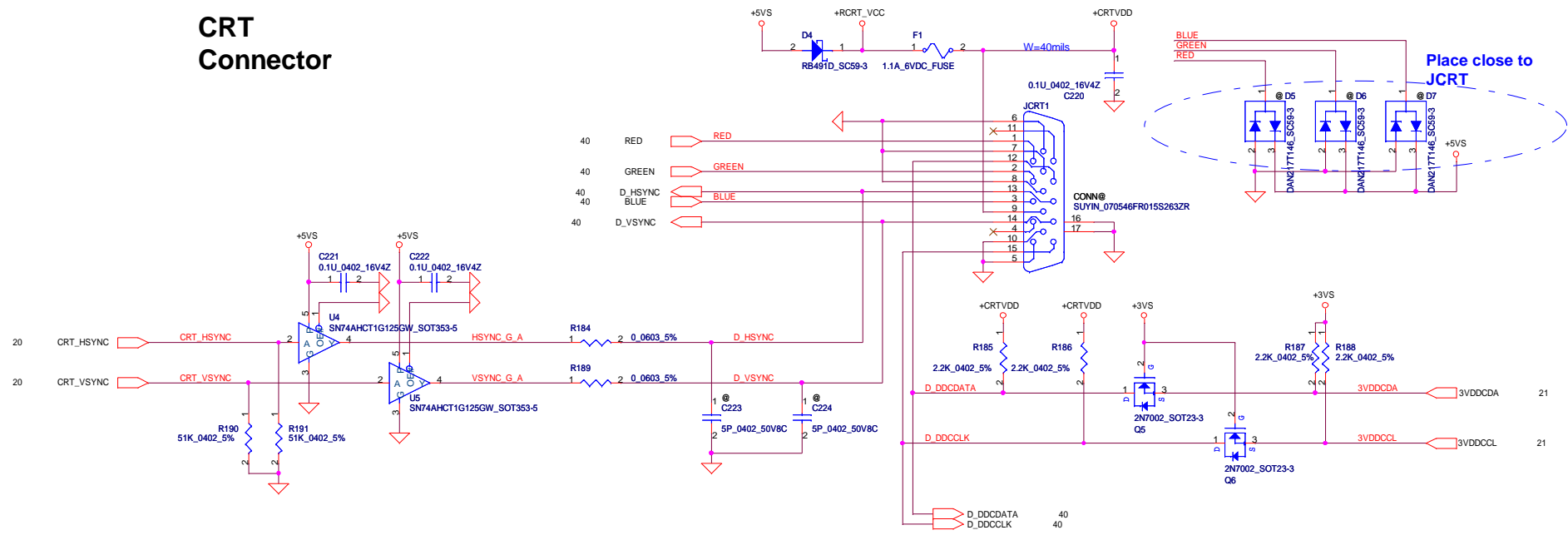


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

**Reserved**

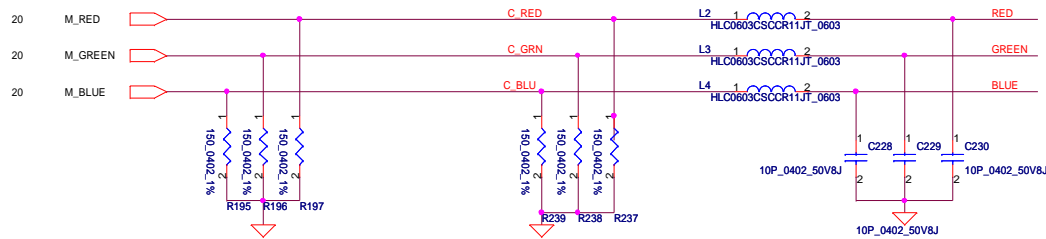


# CRT Connector

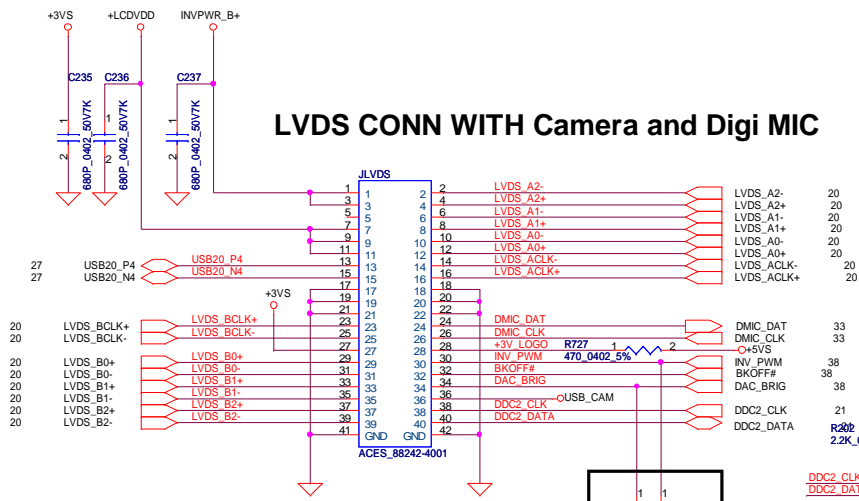


## CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

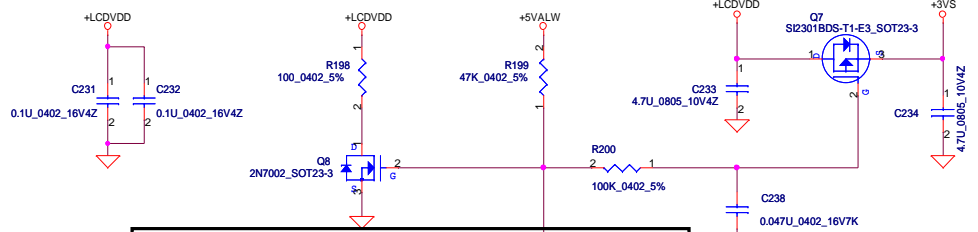


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Size		Document Number		Montevina Consumer Discrete		Rev
Date:		Friday, October 05, 2007		Sheet		18 of 51



**LVDS CONN WITH Camera and Digi MIC**

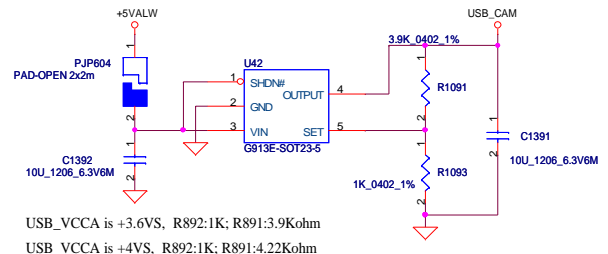
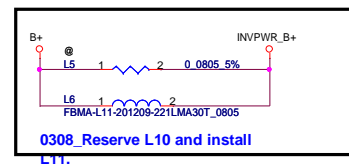
0308\_Install all cap for EMI request.



**Limited Current < 1A**

Avoid Panel display garbage after power on.

ENAVDD circuit with MOSFET Q9 (2N7002\_SOT23-3), resistor R201 (100K\_0402\_5%), and capacitor C239 (0.22U\_0803\_10V7K).

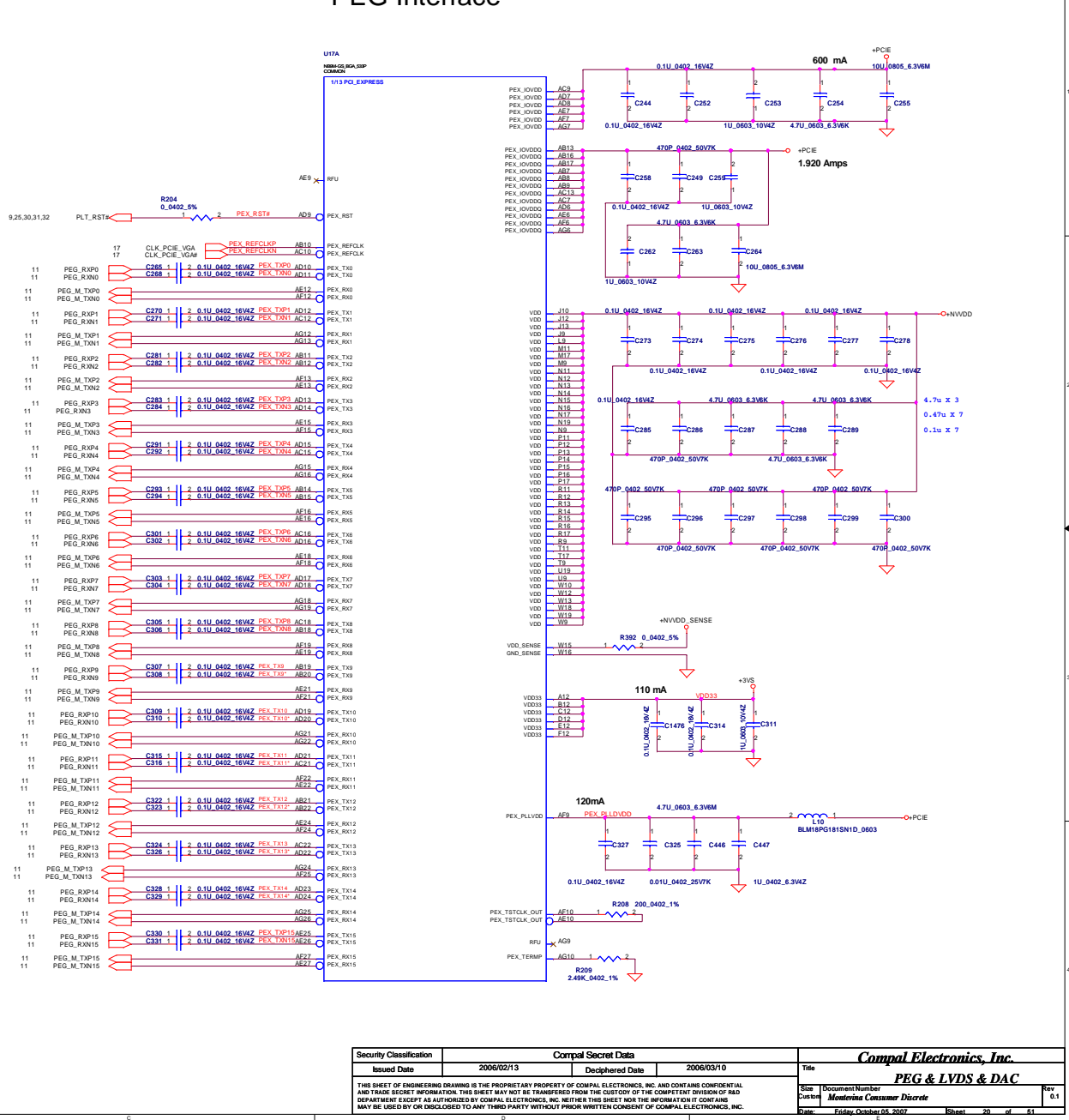
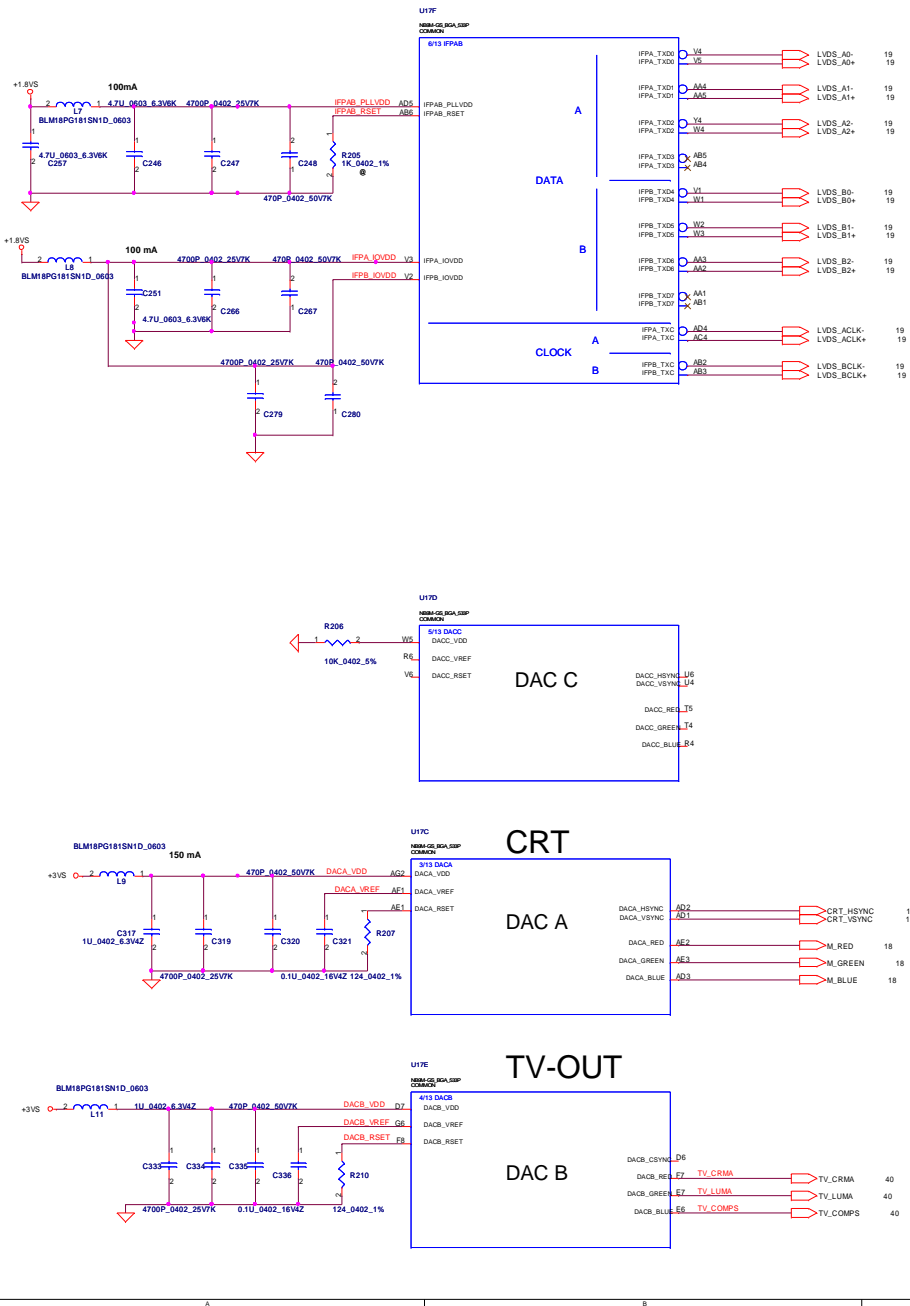


USB\_VCCA is +3.6V, R892:1K; R891:3.9Kohm  
 USB\_VCCA is +4V, R892:1K; R891:4.22Kohm

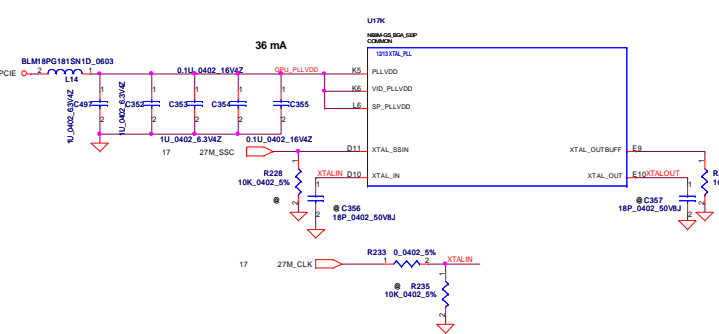
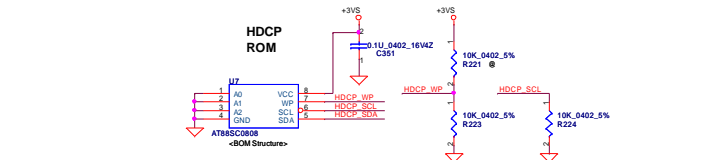
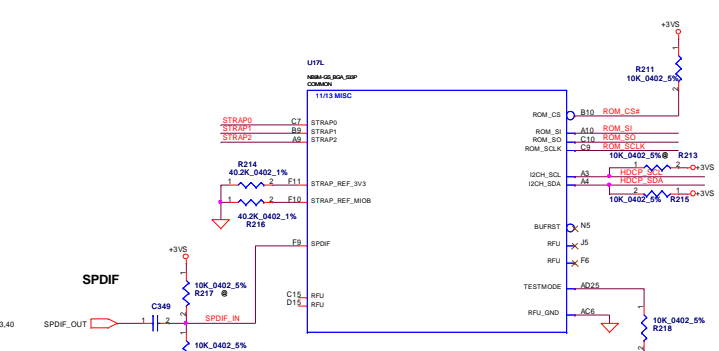
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# LVDS & DAC Interface

# PEG Interface

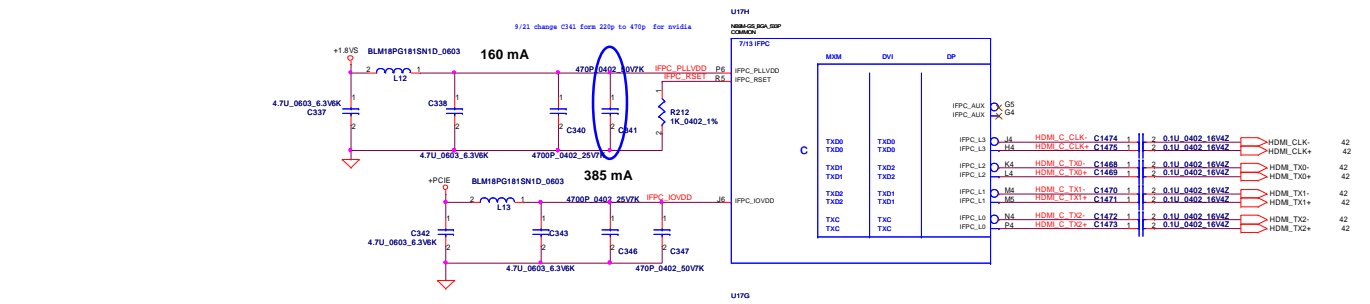
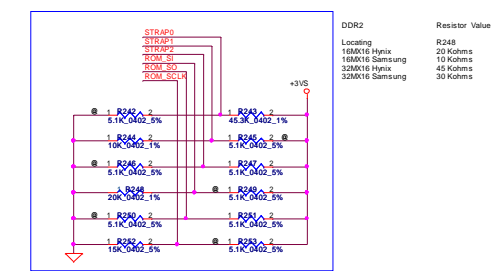


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Size	Customer		Rev
L10	Montevina Consumer Discrete		0.1
Date:	Friday, October 08, 2005	Sheet	50 of 51



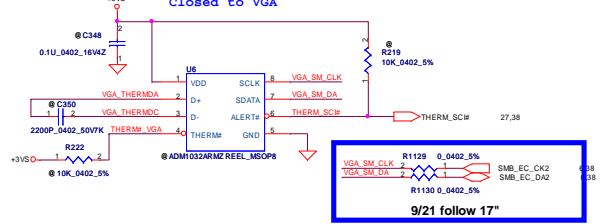
### Straps

MULTI LEVEL STRAPS

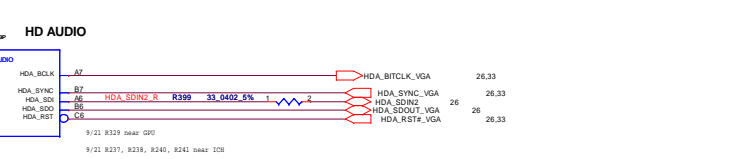
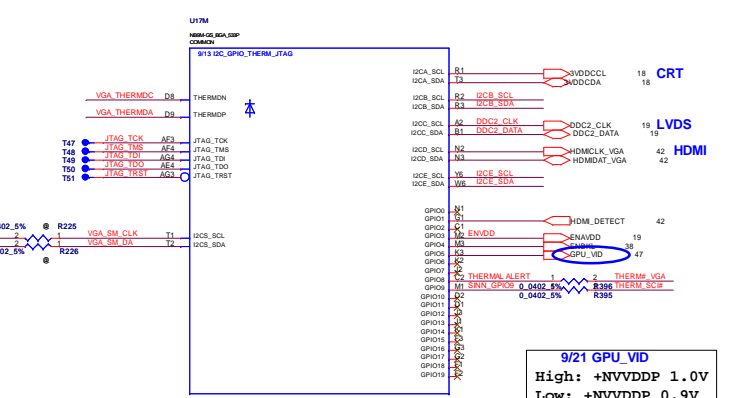
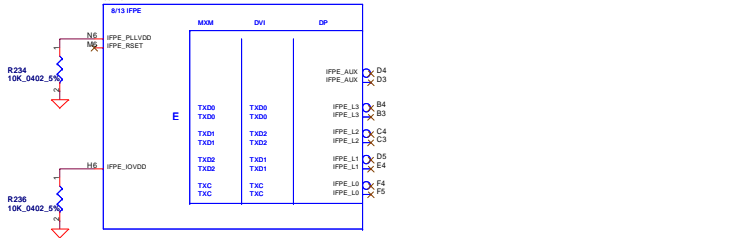


### VGA Thermal Sensor ADM1032ARMZ

Closed to VGA



GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC0
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



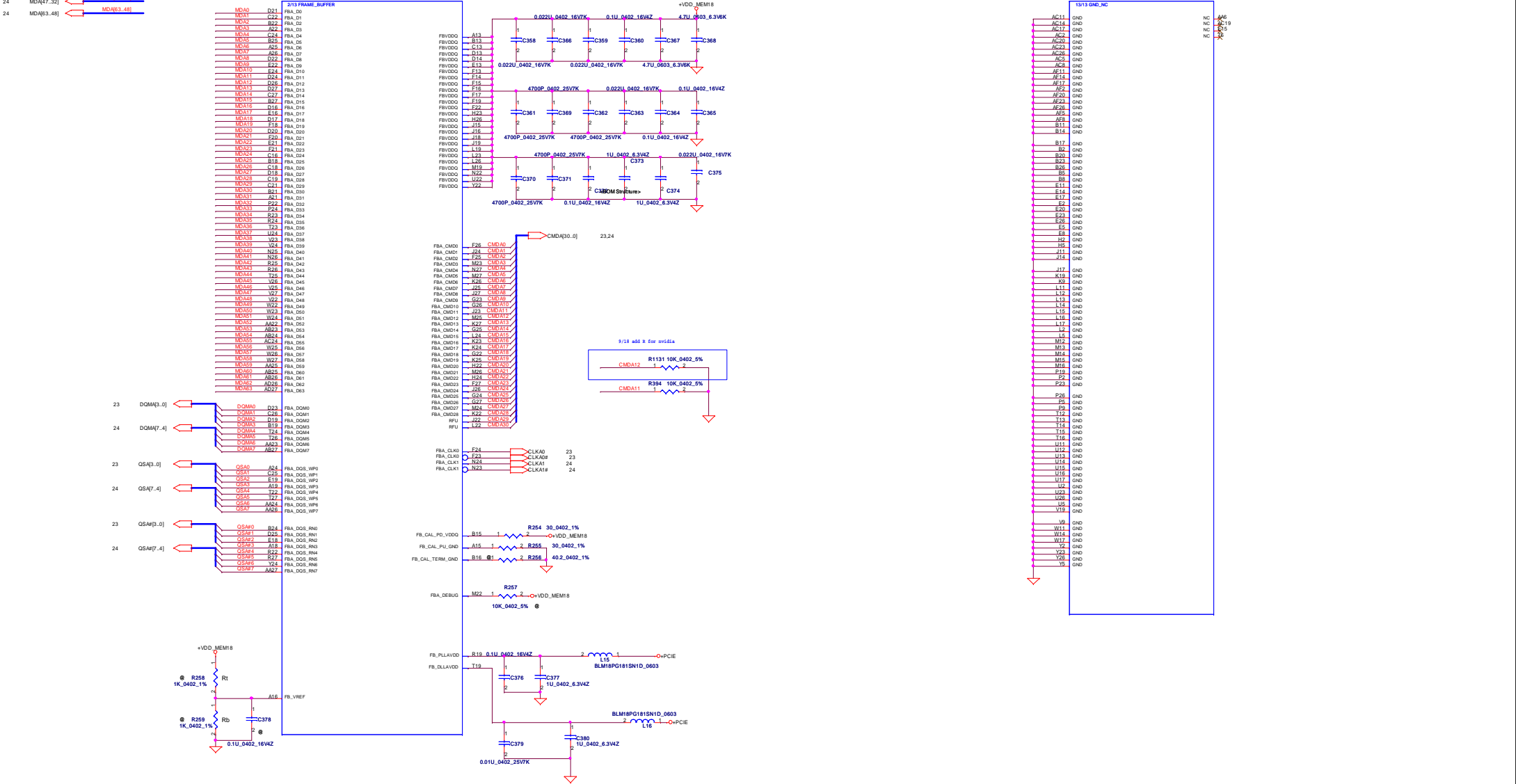
9/21 GPU\_VID  
High: +NVVDDP 1.0V  
Low: +NVVDDP 0.9V

Security Classification	Compal Secret Data	Deciphered Date	2006/03/10
Issued Date	2006/02/13		
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<p>Security Classification</p>		<p>Deciphered Date</p>	
<p>Issued Date</p>		<p>2006/03/10</p>	
<p>Compal Electronics, Inc.</p>			
<p>Straps &amp; HDMI</p>			
Docu	Docu	Docu	Docu
Customer	Customer	Customer	Customer
Date	Monday, October 08, 2007	ISheet	21 of 51

hexain@hotmail.com

# VRAM Interface

- 23 MDA[15..0] ← MDA[15..0]
- 23 MDA[31..16] ← MDA[31..16]
- 24 MDA[47..32] ← MDA[47..32]
- 24 MDA[63..48] ← MDA[63..48]

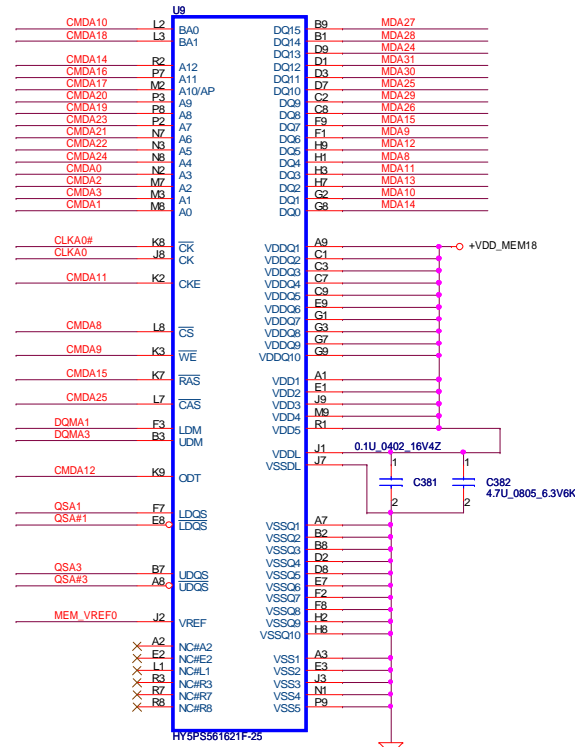
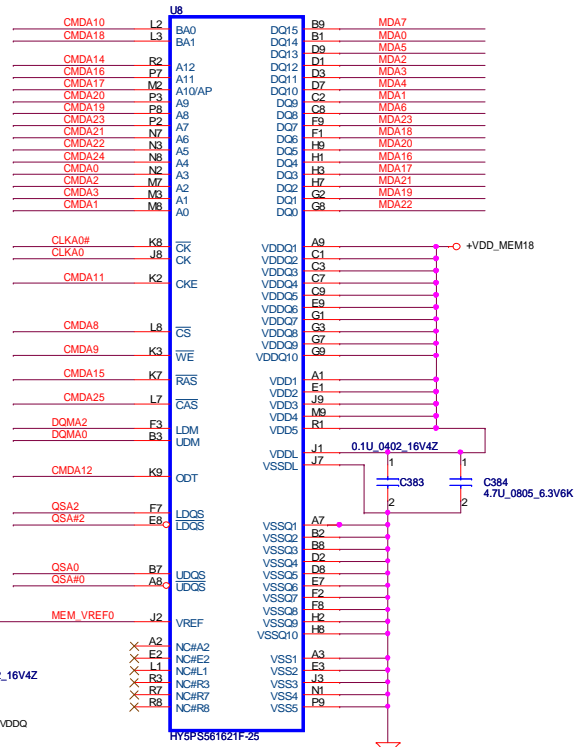
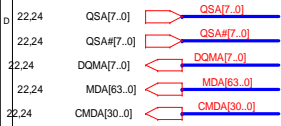


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			<b>VRAM / GND</b>
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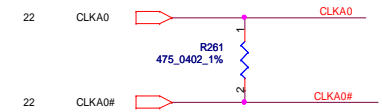
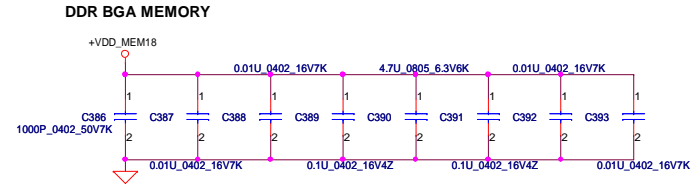
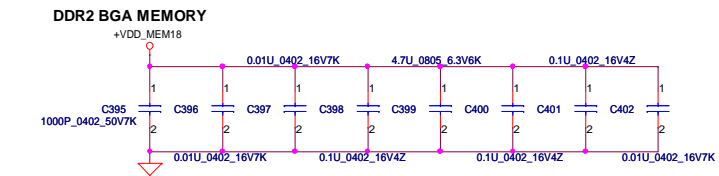
# VRAM DDR2 chips (256MB & 128MB)

32Mx16 DDR2 400MHz \*4==>256MB

16Mx16 DDR2 400MHz\*4==>128MB



Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

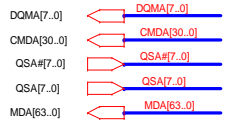


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Date: Monday, October 08, 2007				Sheet 7 of 16

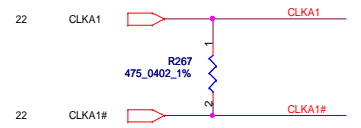
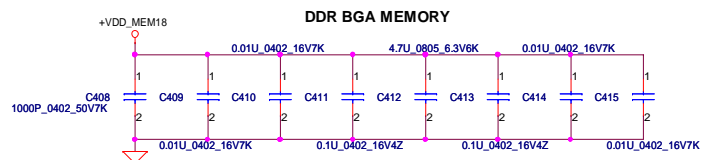
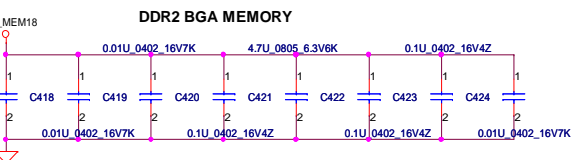
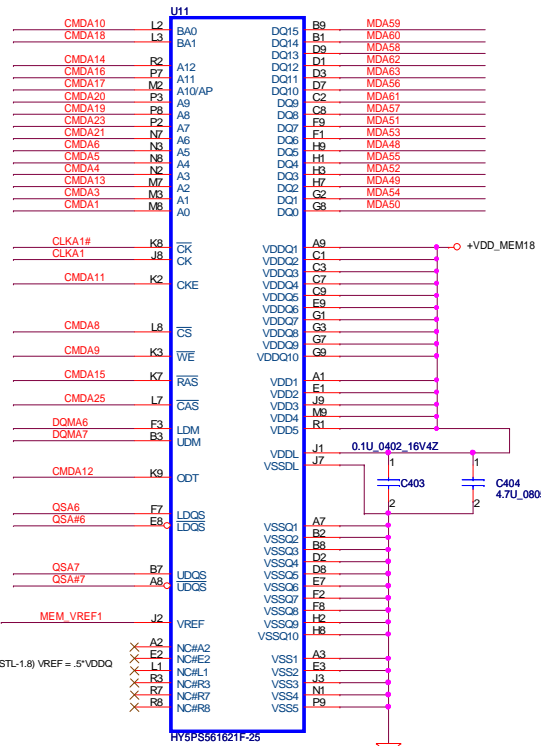
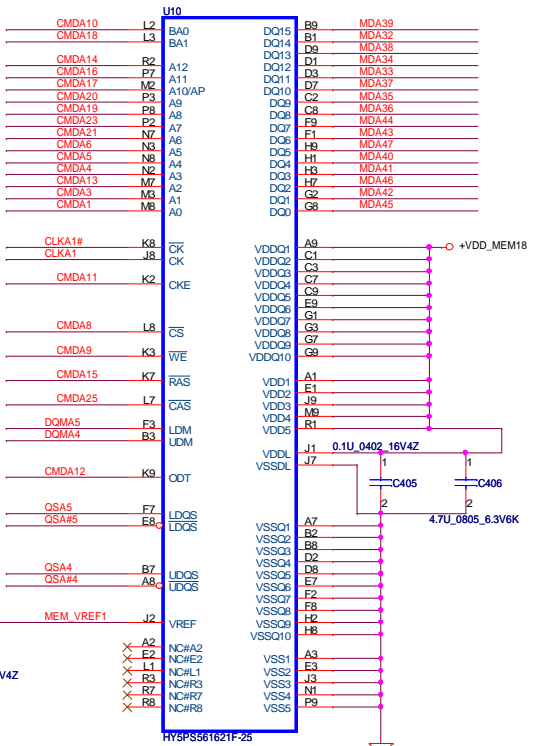
# VRAM DDR2 chips (256MB & 128MB)

32Mx16 DDR2 400MHz \*4==>256MB

16Mx16 DDR2 400MHz\*4==>128MB

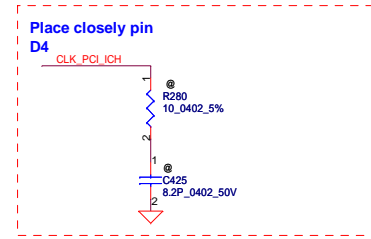
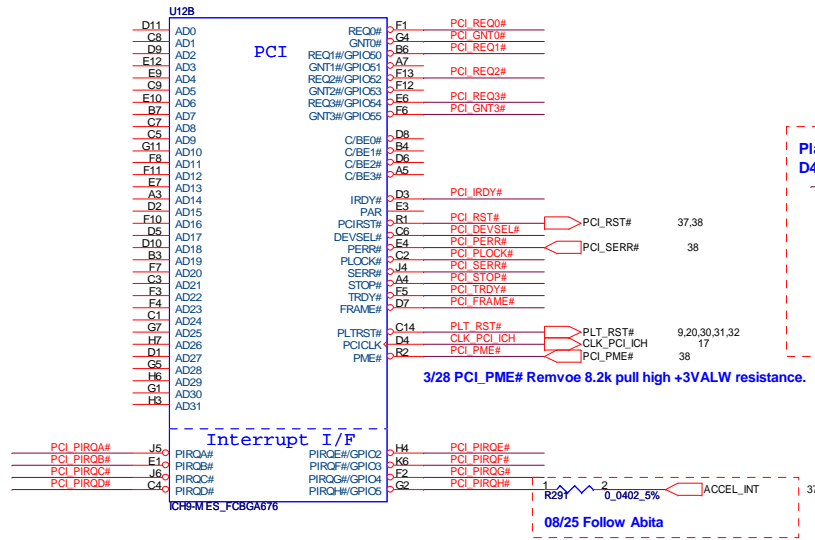
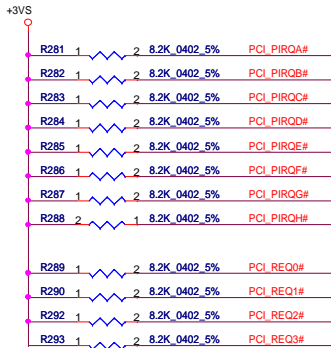
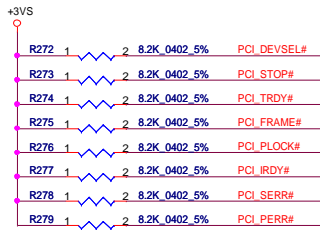


Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



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Date: Monday, October 08, 2007				Sheet 8 of 16





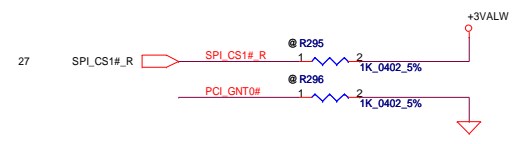
**A16 swap override Strap**

PCI_GNT3#	Low = A16 swap override Enable High = Default *
-----------	--

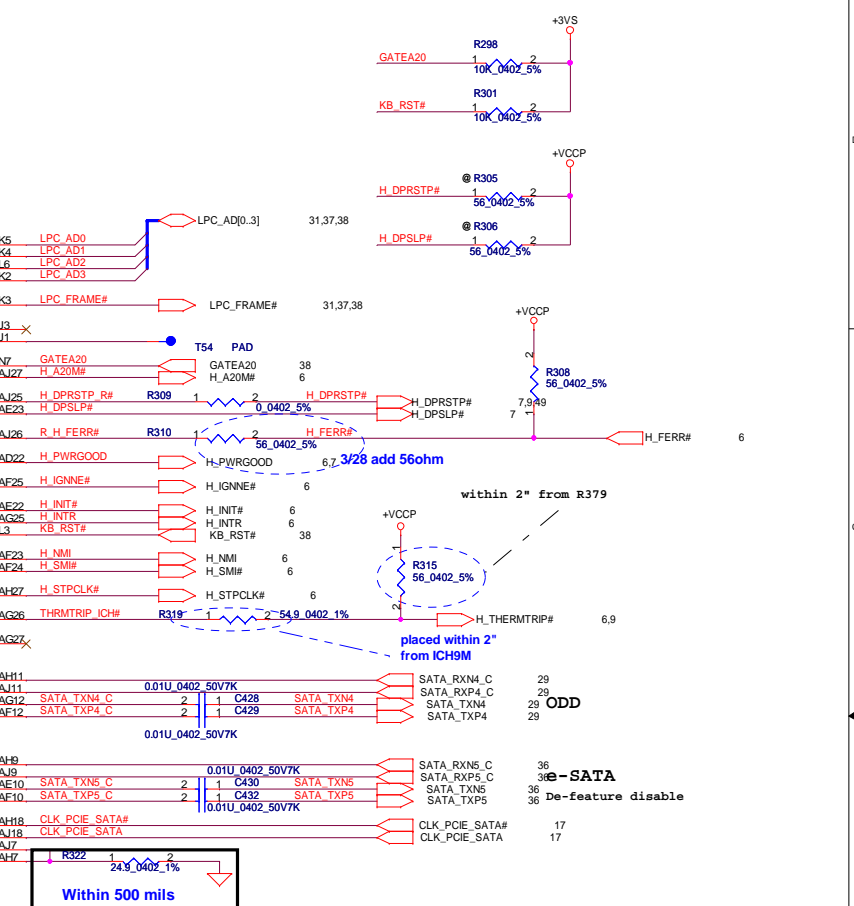
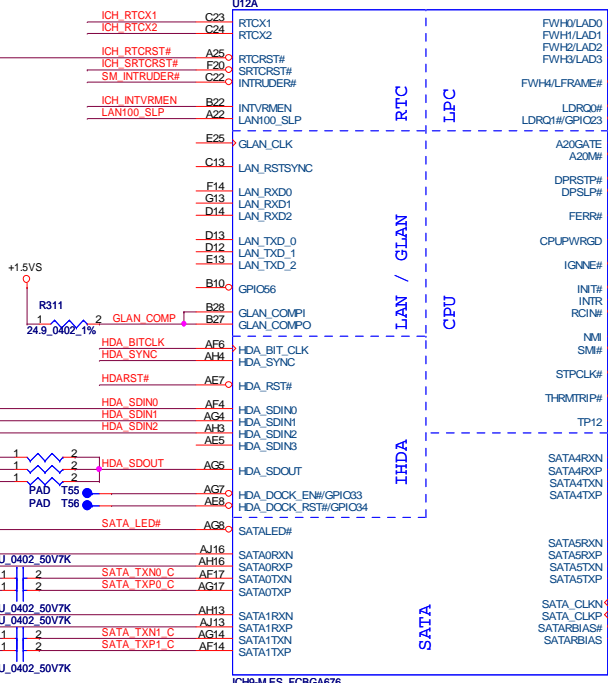
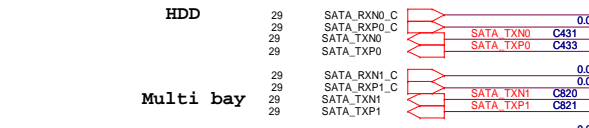
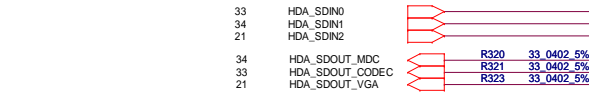
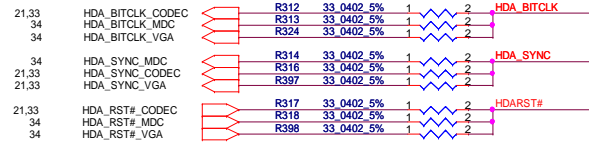
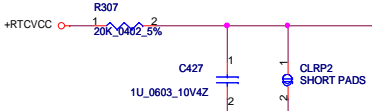
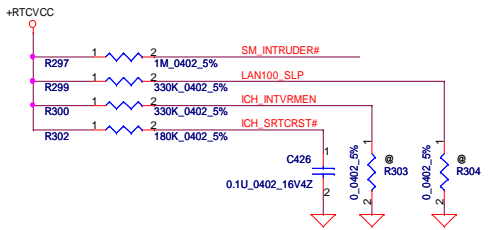


**Boot BIOS Strap**

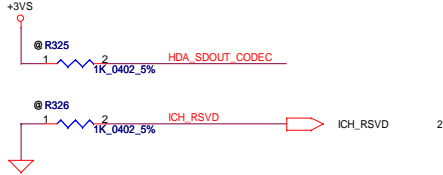
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



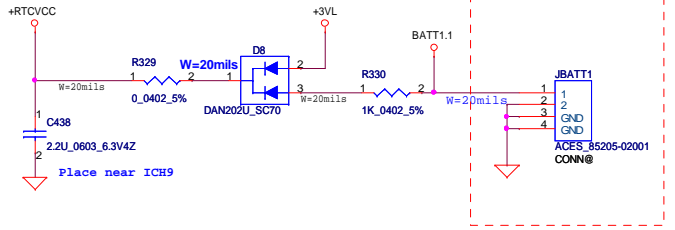
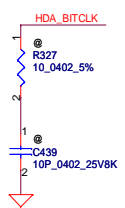
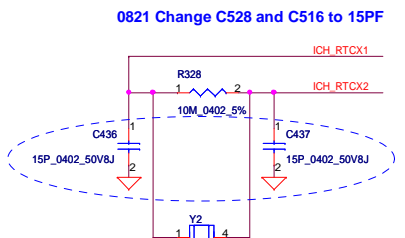
<b>ICH8M Internal VR Enable Strap</b> (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
<b>ICH_INTVRMEN</b>	Low = Internal VR Disabled High = Internal VR Enabled(Default)
<b>ICH8M LAN100 SLP Strap</b> (Internal VR for VccLAN1.05 and VccCL1.05)	
<b>ICH_LAN100_SLP</b>	Low = Internal VR Disabled High = Internal VR Enabled(Default)



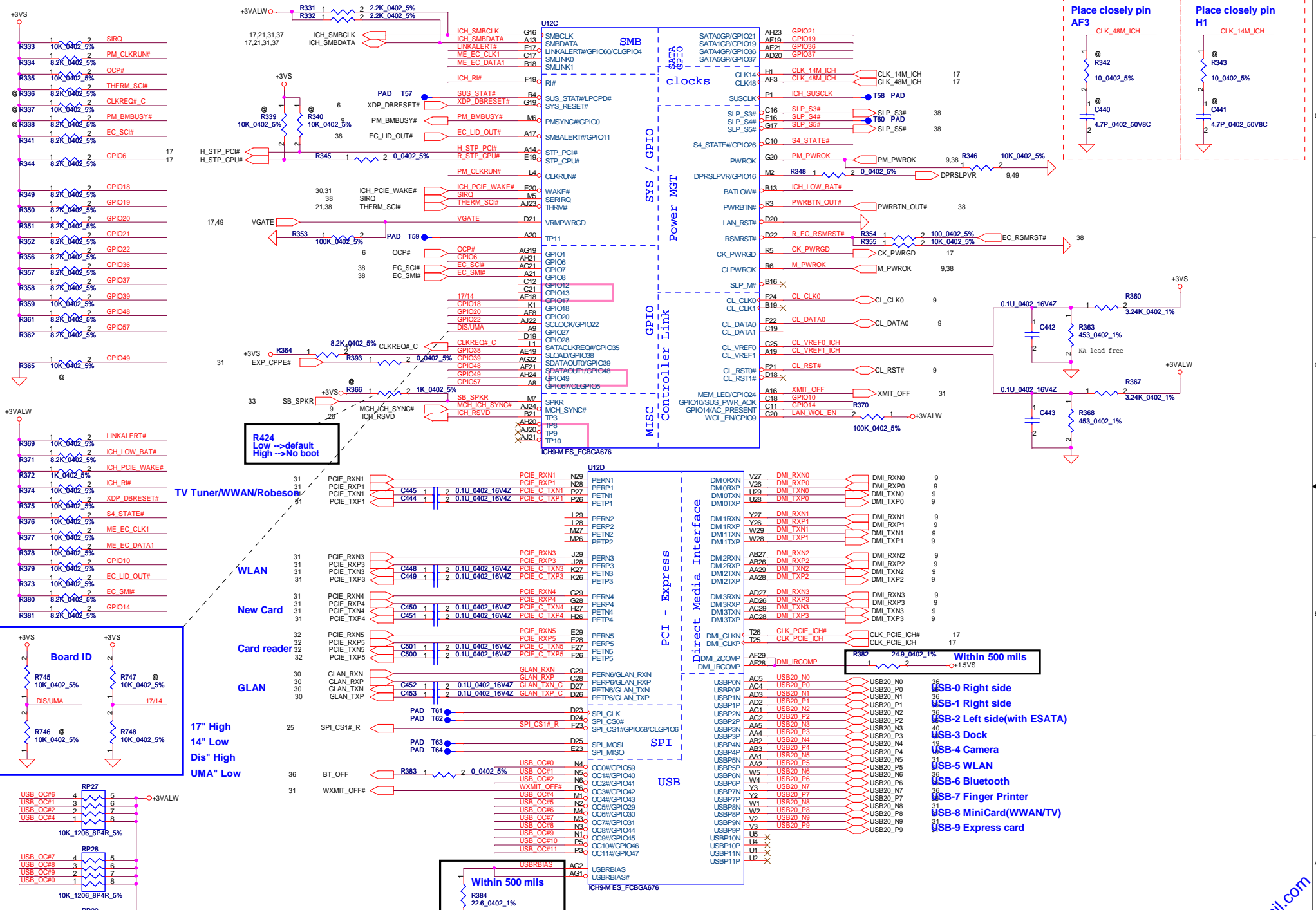
**XOR CHAIN ENTRANCE STRAP:RSVD**



ICH_RSVD	HDA_SDOUT_CODEC
0	0
0	1
1	0
1	1



<b>Security Classification</b>	<b>Compal Secret Data</b>		<b>Title</b>	
<b>Issued Date</b>	2007/09/26	<b>Deciphered Date</b>	2007/09/26	<b>Compal Electronics, Inc.</b>
<b>ICH9(2/4) LAN,HD,IDE,LPC</b>				
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	Custom	Montevina Consumer Discrete	0.1	
<b>Date:</b>	Monday, October 08, 2007	<b>Sheet</b>	26	<b>of</b> 51

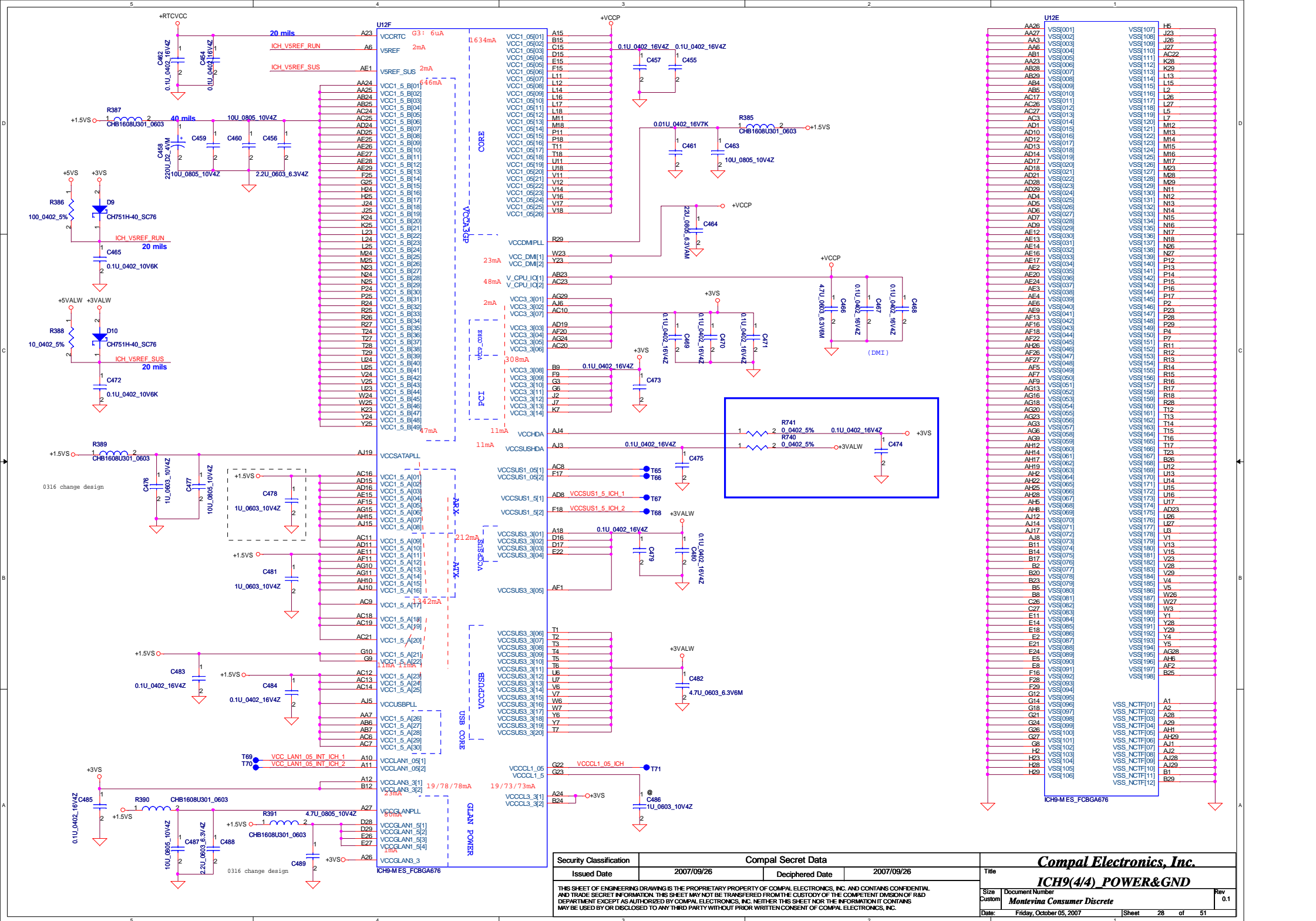


Security Classification	Compal Secret Data	
Issued Date	2007/09/26	Deciphered Date
		2007/09/26

Compal Electronics, Inc.		
Title		
ICH9(3/4) DMI,USB,GPIO,PCIE		
Size	Document Number	Rev
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Date:	Monday, October 08, 2007	Sheet 27 of 51

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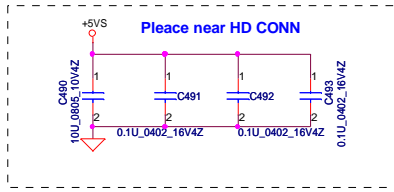
http://www.compalelectronics.com



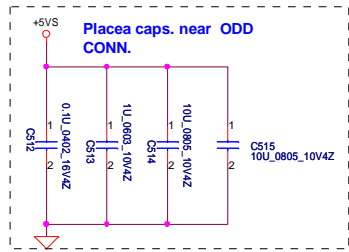
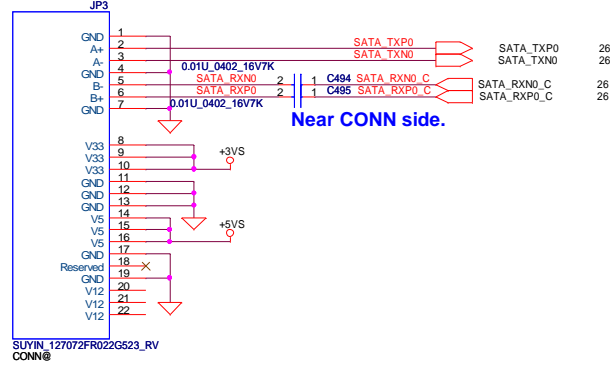
Security Classification	Compal Secret Data	
Issued Date	2007/09/26	Deciphered Date
		2007/09/26

<b>Compal Electronics, Inc.</b>		
<b>ICH9(4) POWER&amp;GND</b>		
Size Custom	Document Number <b>Montevina Consumer Discrete</b>	Rev <b>0.1</b>
Date:	Friday, October 05, 2007	Sheet 28 of 51

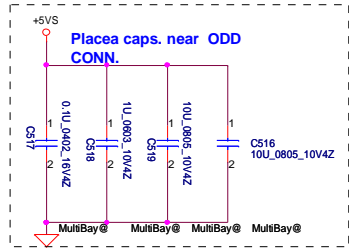
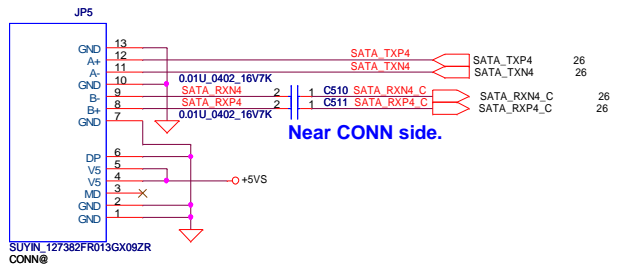
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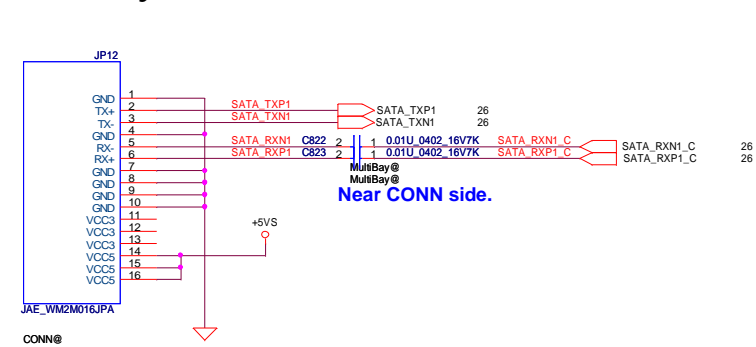
### HDD Connector



### CD-ROM Connector



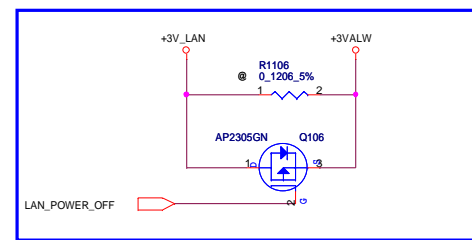
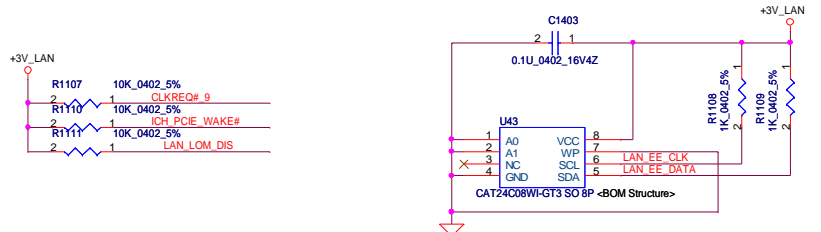
### Multi Bay Connector



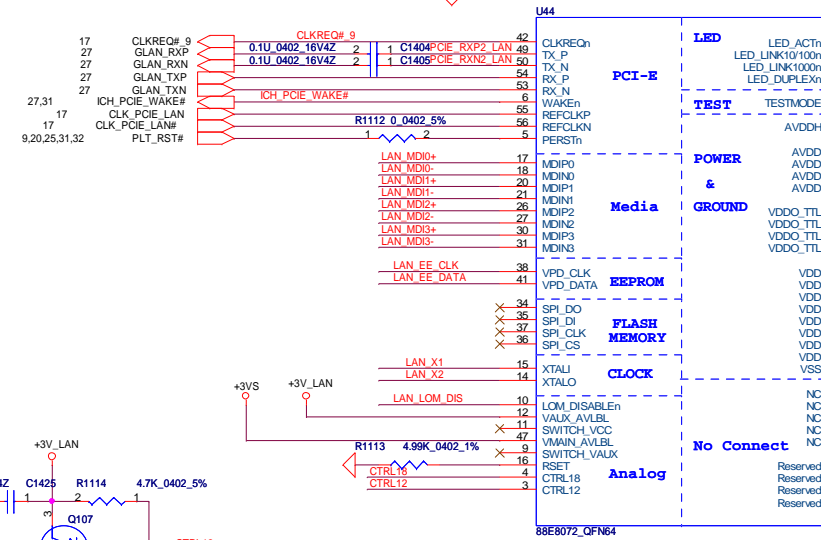
Security Classification	Compal Secret Data		
Issued Date	2007/09/26	Deciphered Date	2007/09/26
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<b>HDD &amp; CDROM</b>		
Size Custom	Document Number <b>Montevina Consumer Discrete</b>	Rev 0.1
Date:	Monday, October 08, 2007	Sheet 29 of 51

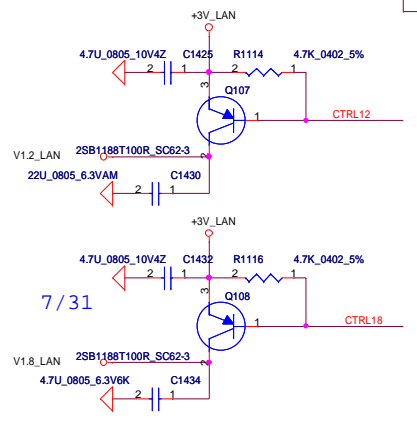
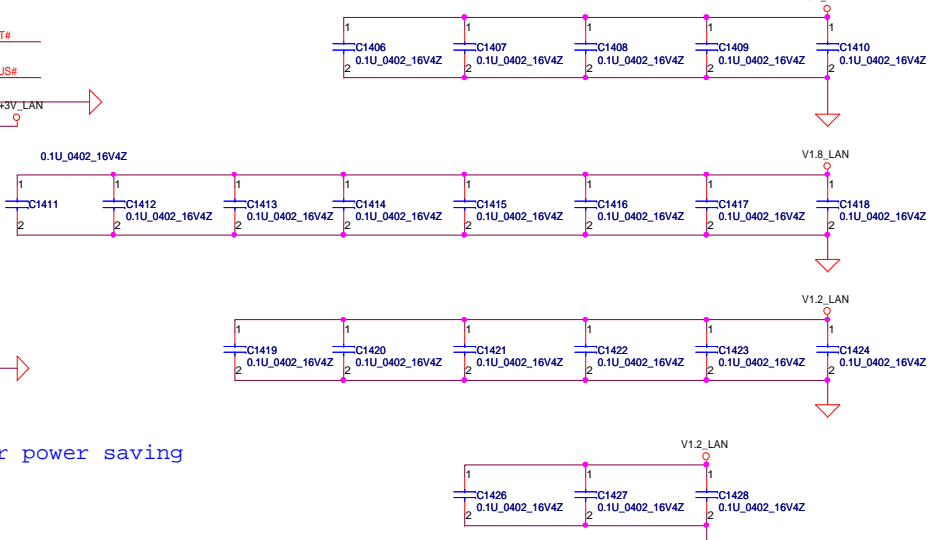
http://www.compal.com



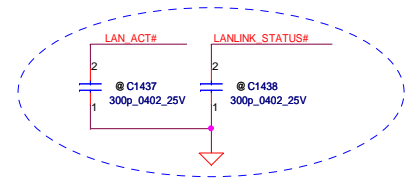
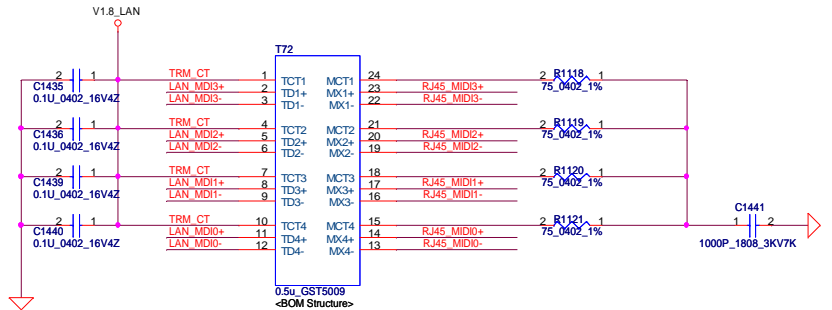
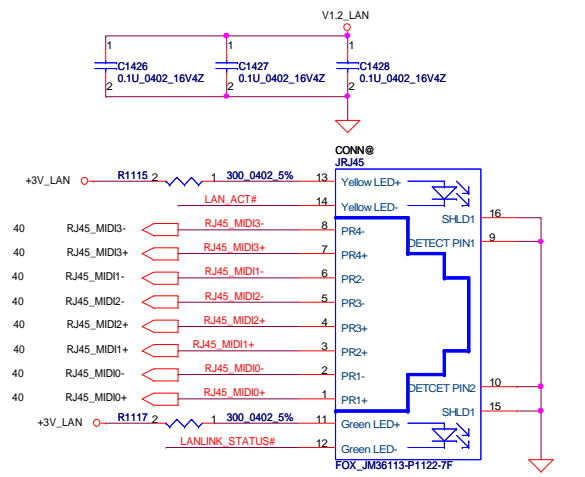
Turn off power when S3. 06/14



for power saving



7/31

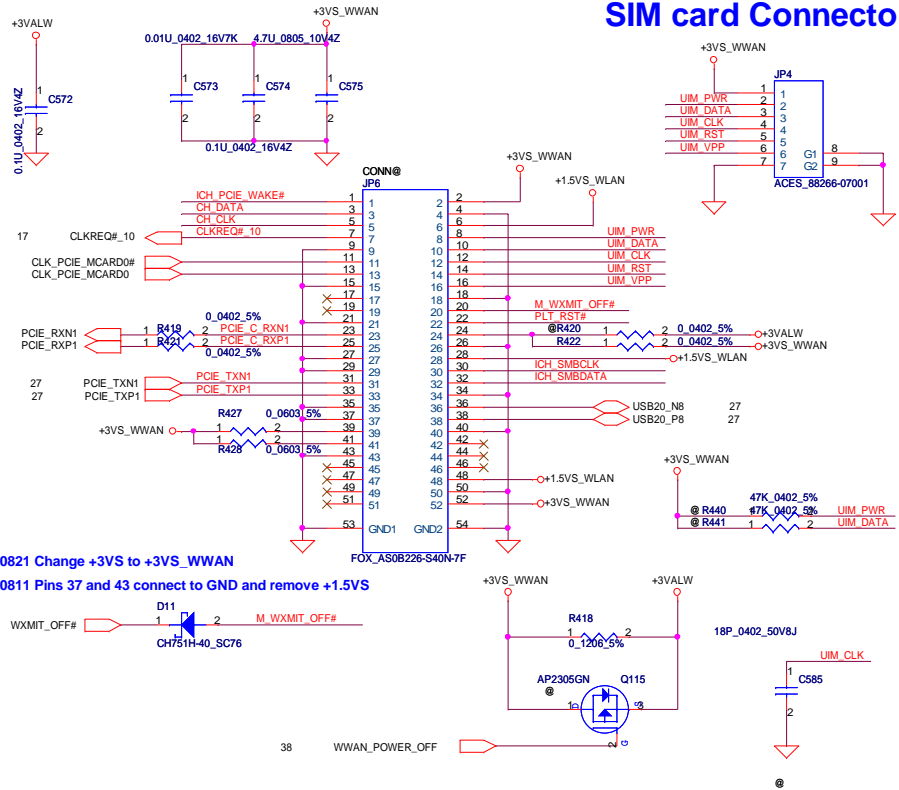


1115 EMI REQUEST

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<p><b>Compal Electronics, Inc.</b></p> <p><b>LAN-88E8072</b></p>				
Size	Document Number	Rev		
	LA-3821P	0.1		
Date:	Friday, October 05, 2007	Sheet	30	of 51

# Mini Card 0--TV tuner/WWAN/Robson

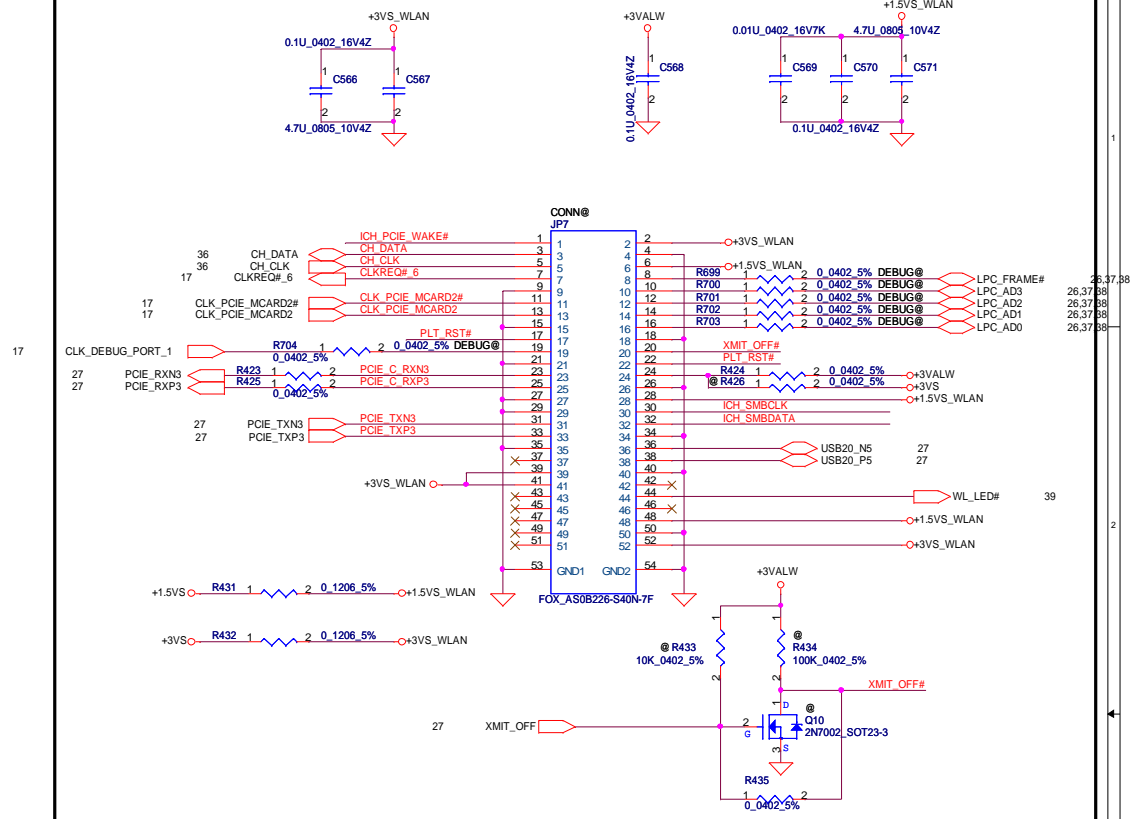
## SIM card Connector



0821 Change +3VS to +3VS\_WWAN

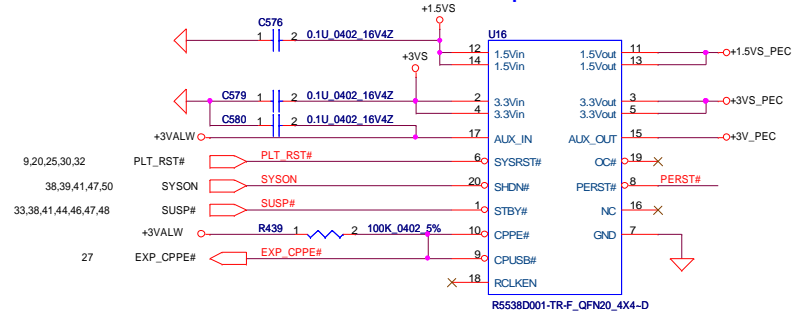
0811 Pins 37 and 43 connect to GND and remove +1.5V

# Mini Card 2---WLAN



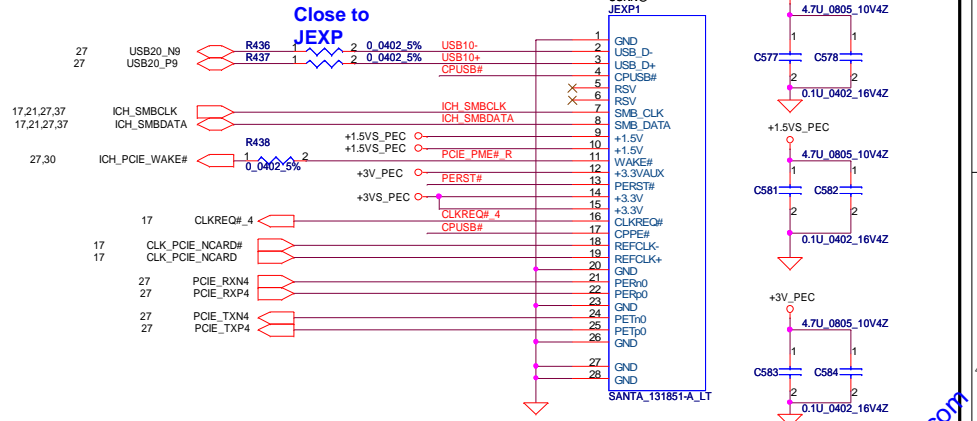
# New Card

## Express Card Power Switch



internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low

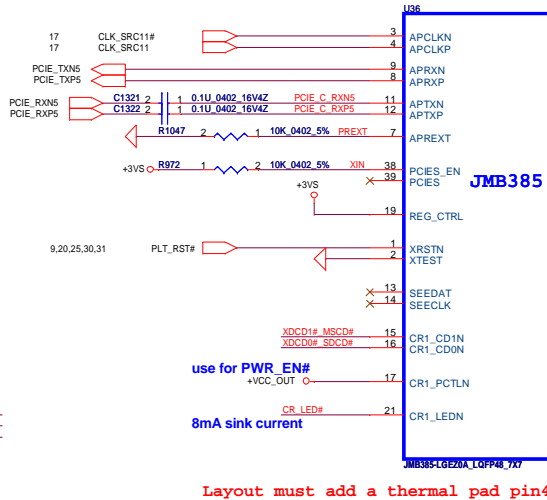
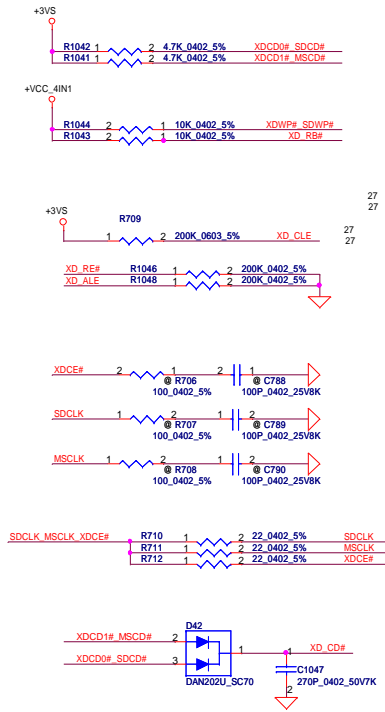
## Near to Express Card slot.



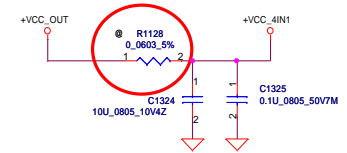
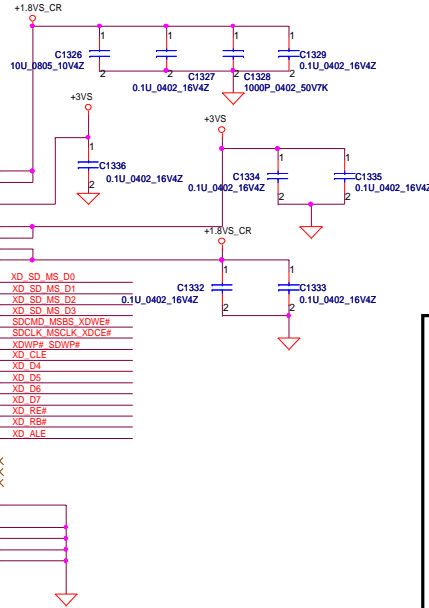
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Issued Date	2007/09/26	Deciphered Date
		2007/09/26

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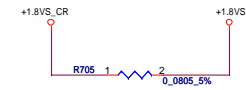
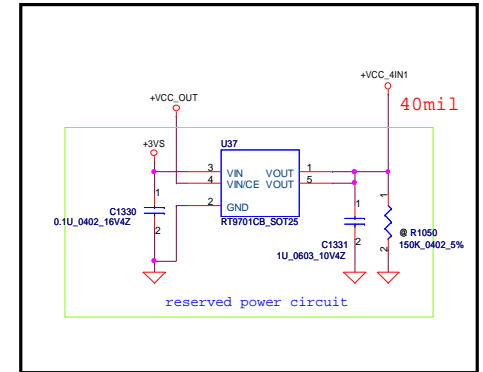
Title		
WLAN, WWAN, New Card		
Size	Document Number	Rev
	Montevina Consumer Discrete	0.1
Date:	Friday, October 05, 2007	Sheet 31 of 51



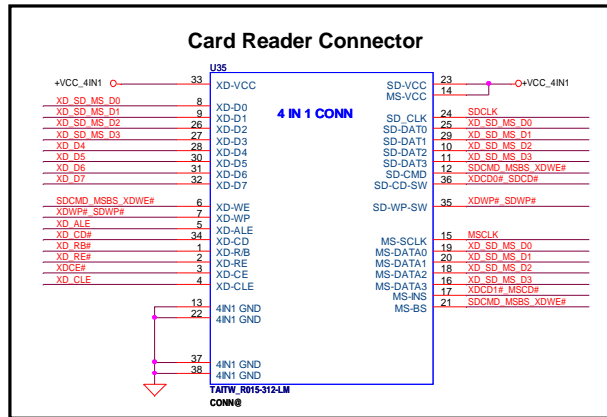
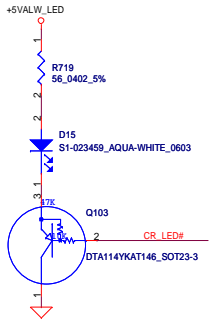
Layout must add a thermal pad pin49



Use 0603 type and over 20 mils trace width on both side



White LED: VF=3V, IF = 5mA, Res = 56ohm

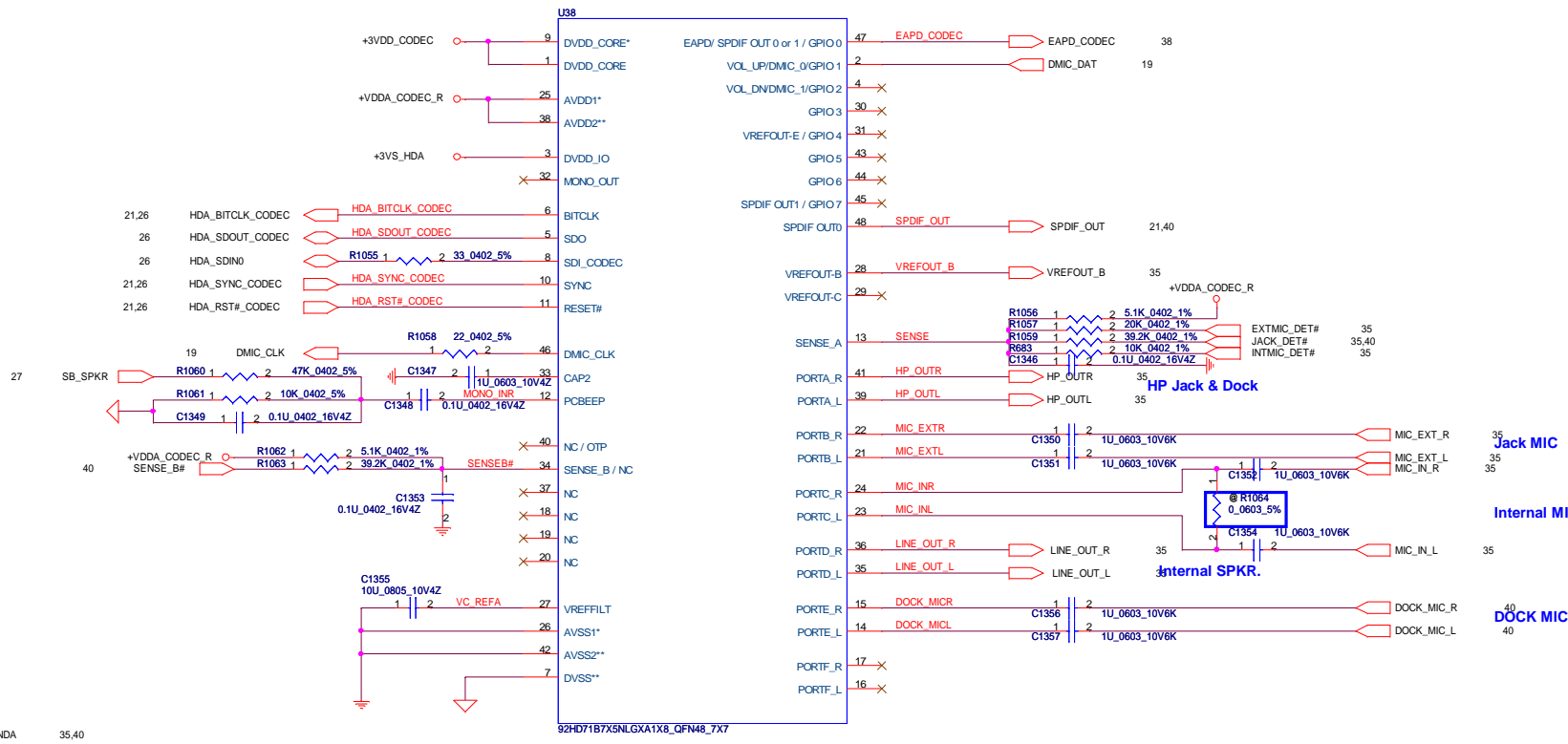
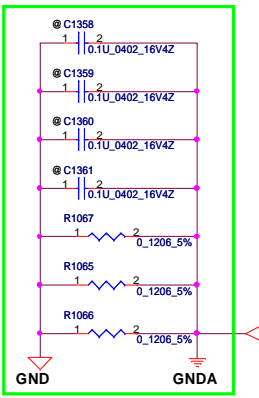
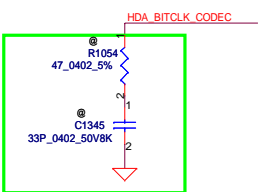
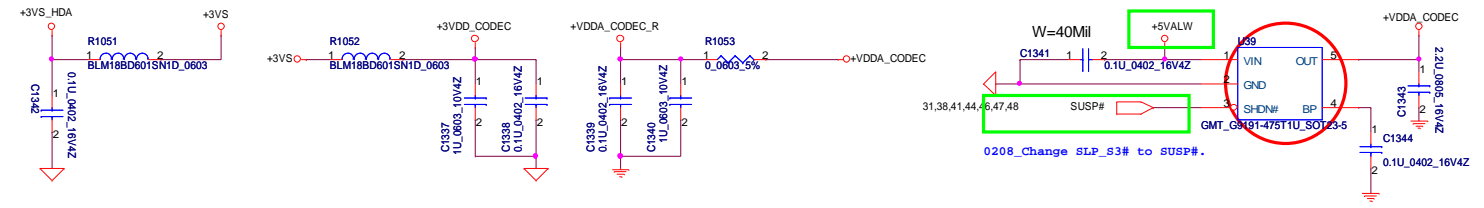


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Date: Friday, October 05, 2007				Sheet 32 of 51	



**CODEC POWER**

(4.75V)  
300mA

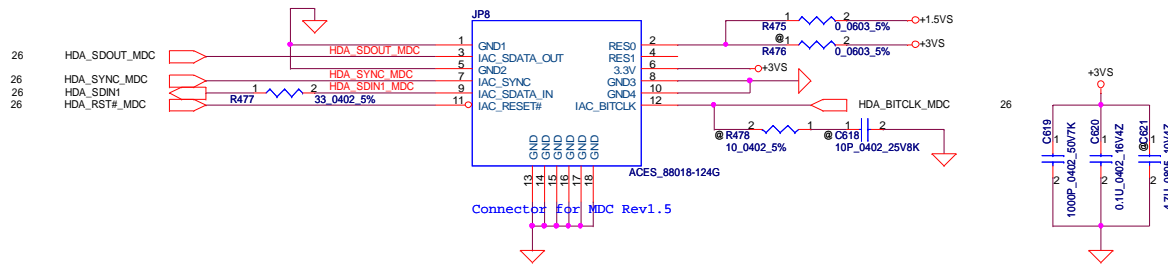


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

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				Montevina Consumer UMA	
				Date:	Friday, October 05, 2007
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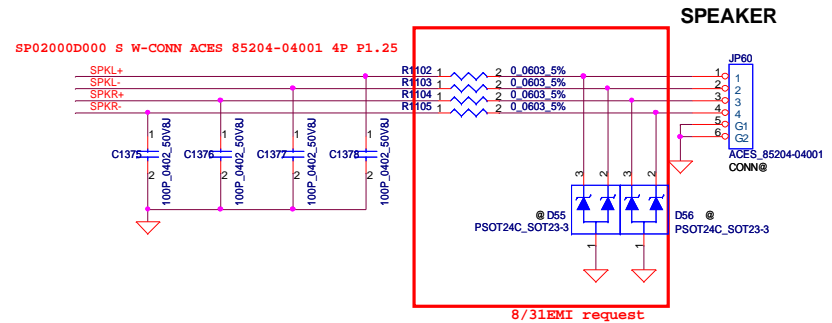
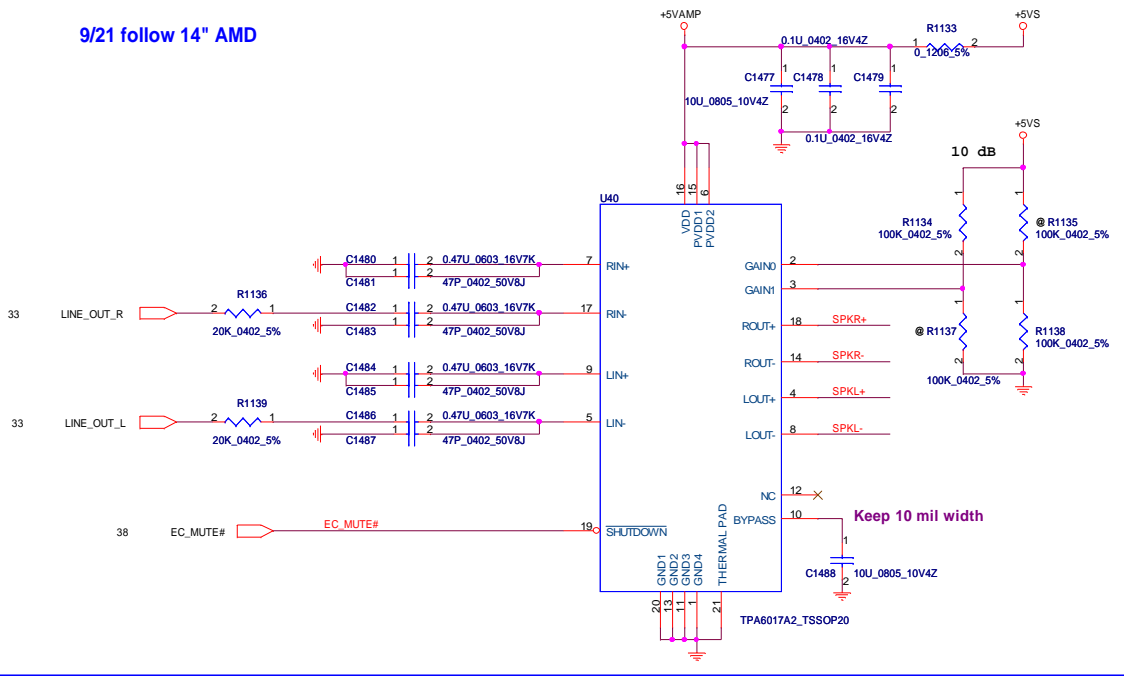
mailto:hotmail.com

# MDC 1.5 Conn.

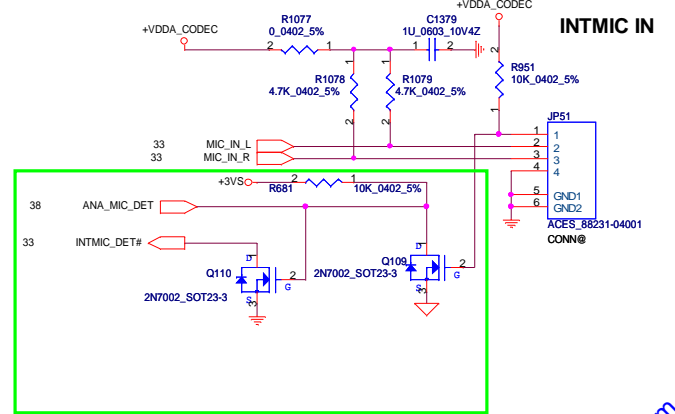
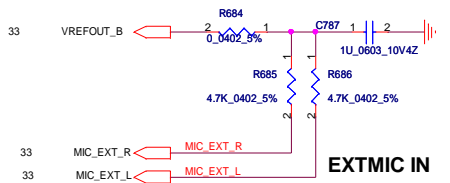
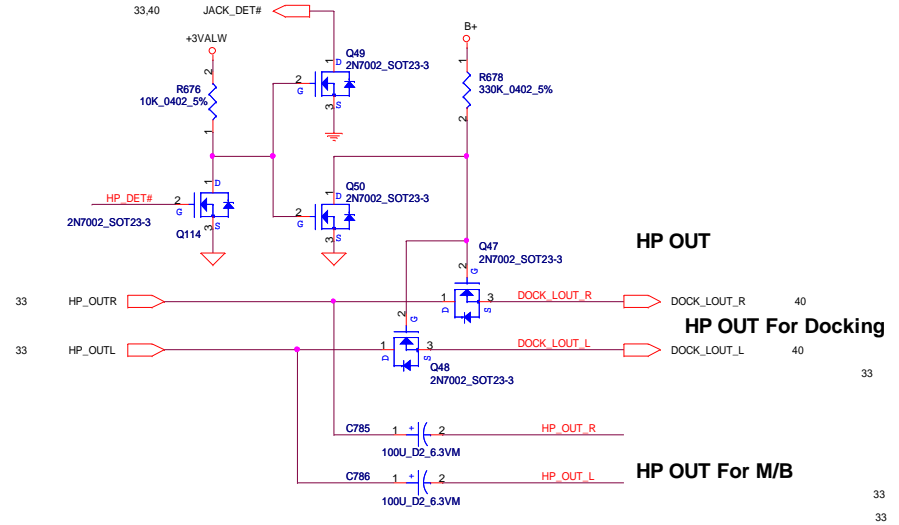
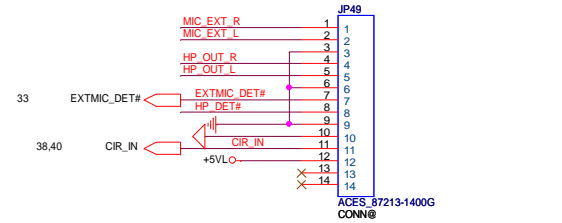


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9/21 follow 14" AMD

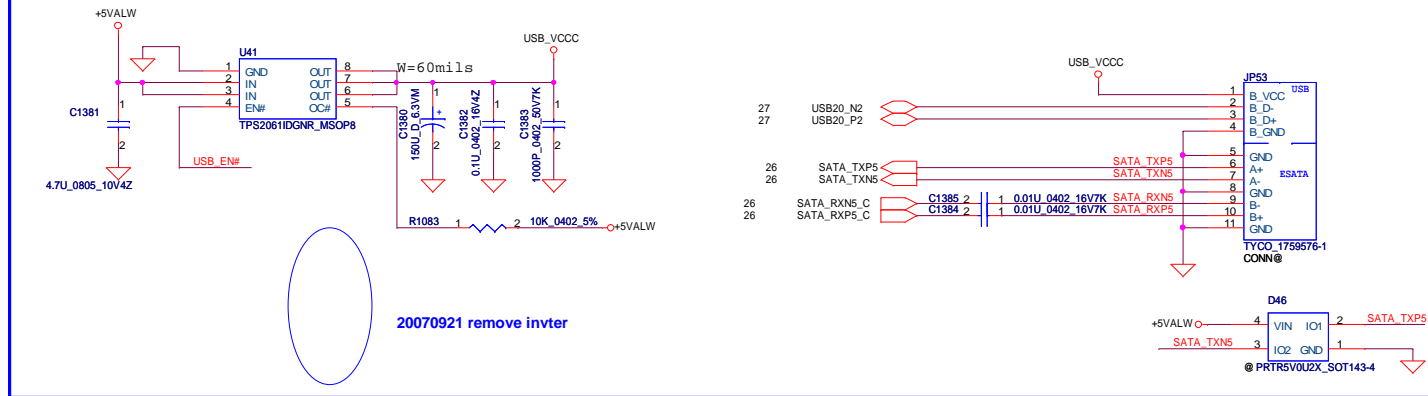


Audio/B & CIR

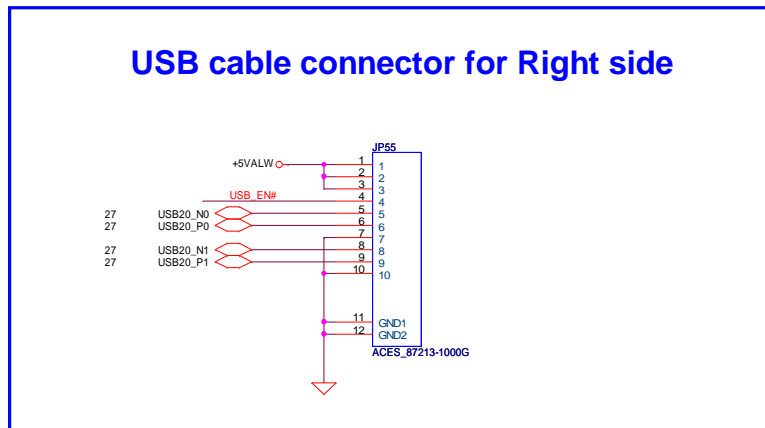


Security Classification		Compal Secret Data		Title	
Issued Date	2007/09/26	Deciphered Date	2007/09/26	AMP & Audio Jack	
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				Custom	Montevina Consumer Discrete
				Date:	Friday, October 05, 2007
				Sheet	35 of 51

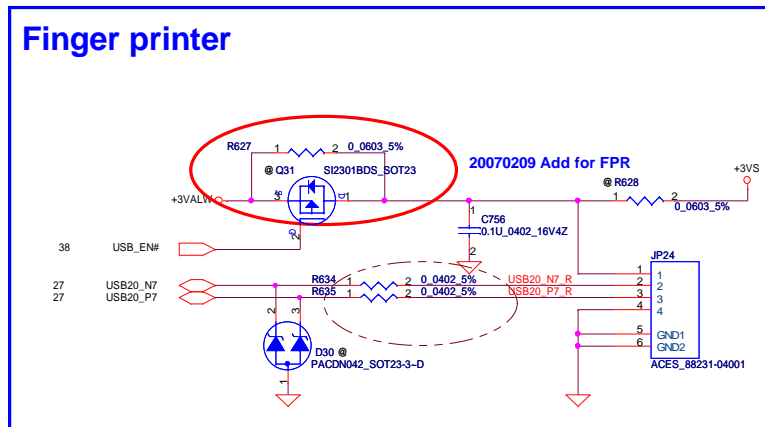
## Left side ESATA/USB combination Connector



## USB cable connector for Right side

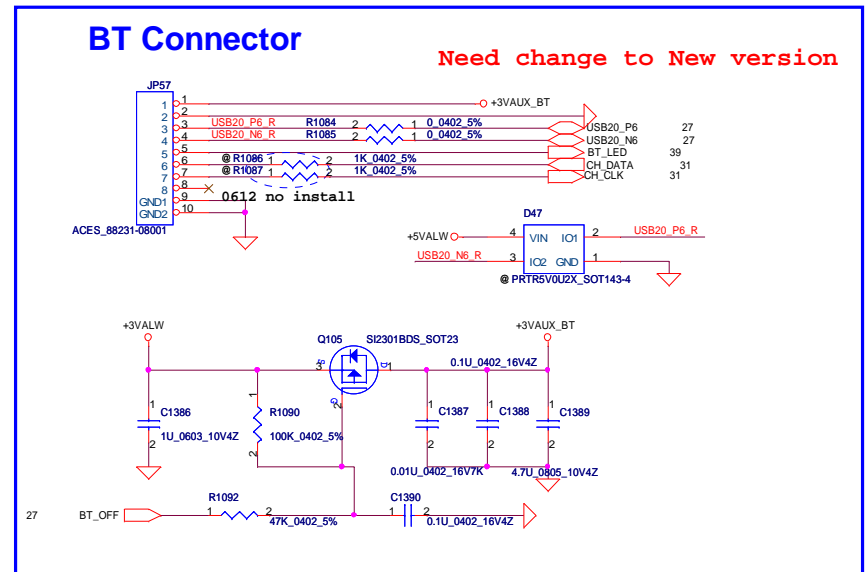


## Finger printer

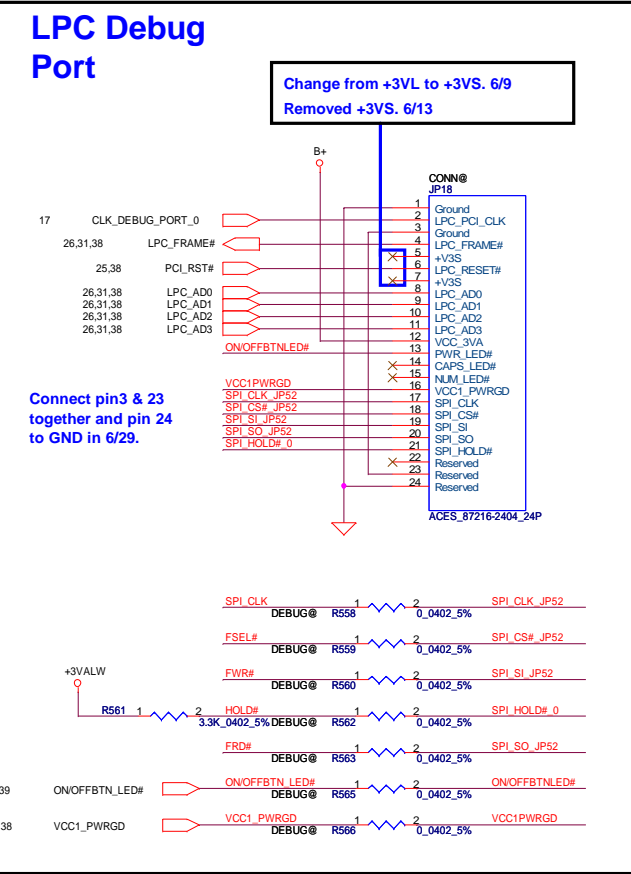
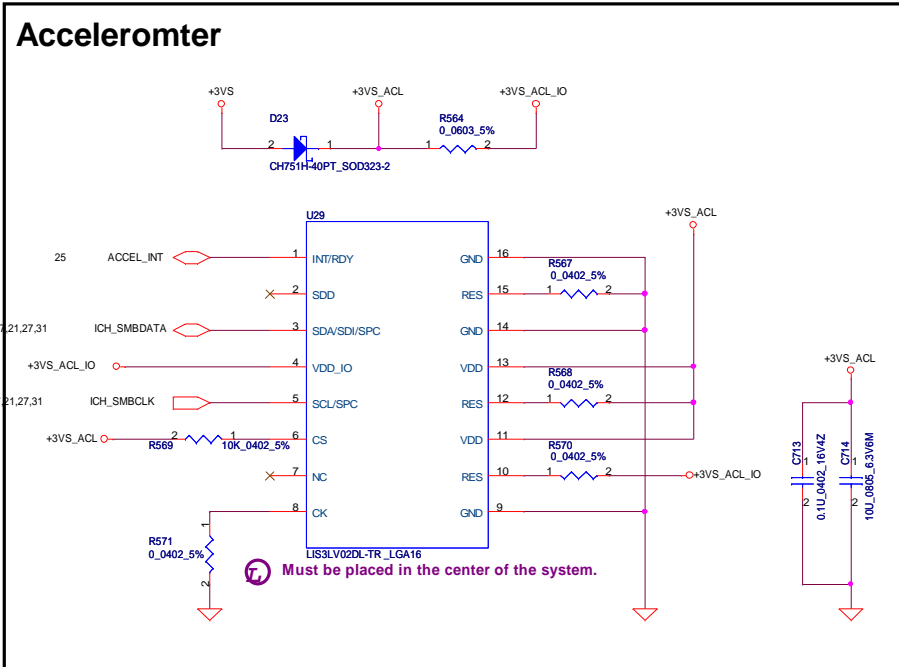
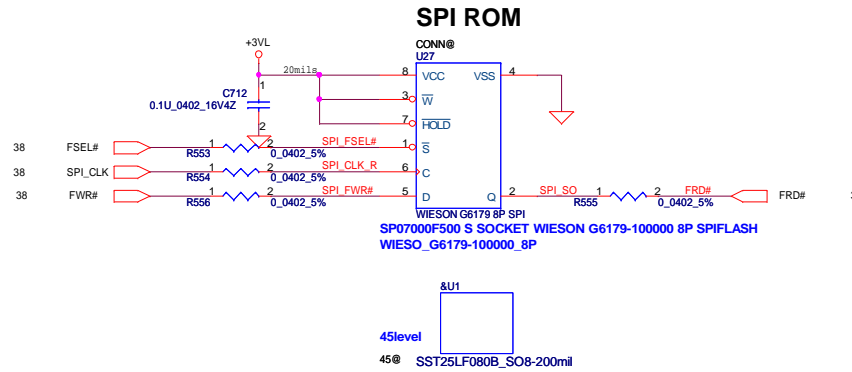
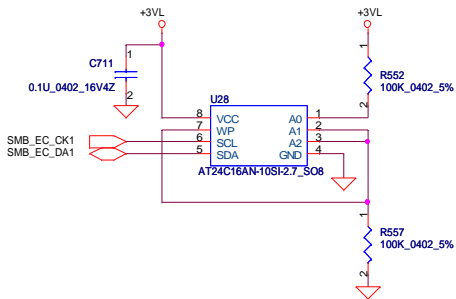


## BT Connector

Need change to New version

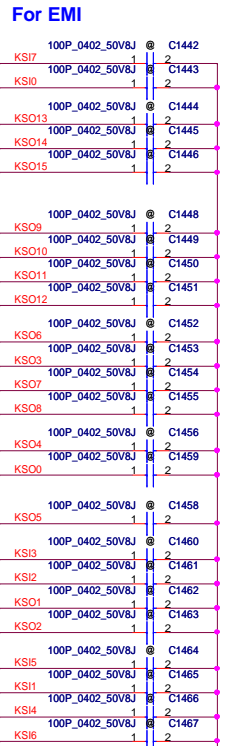
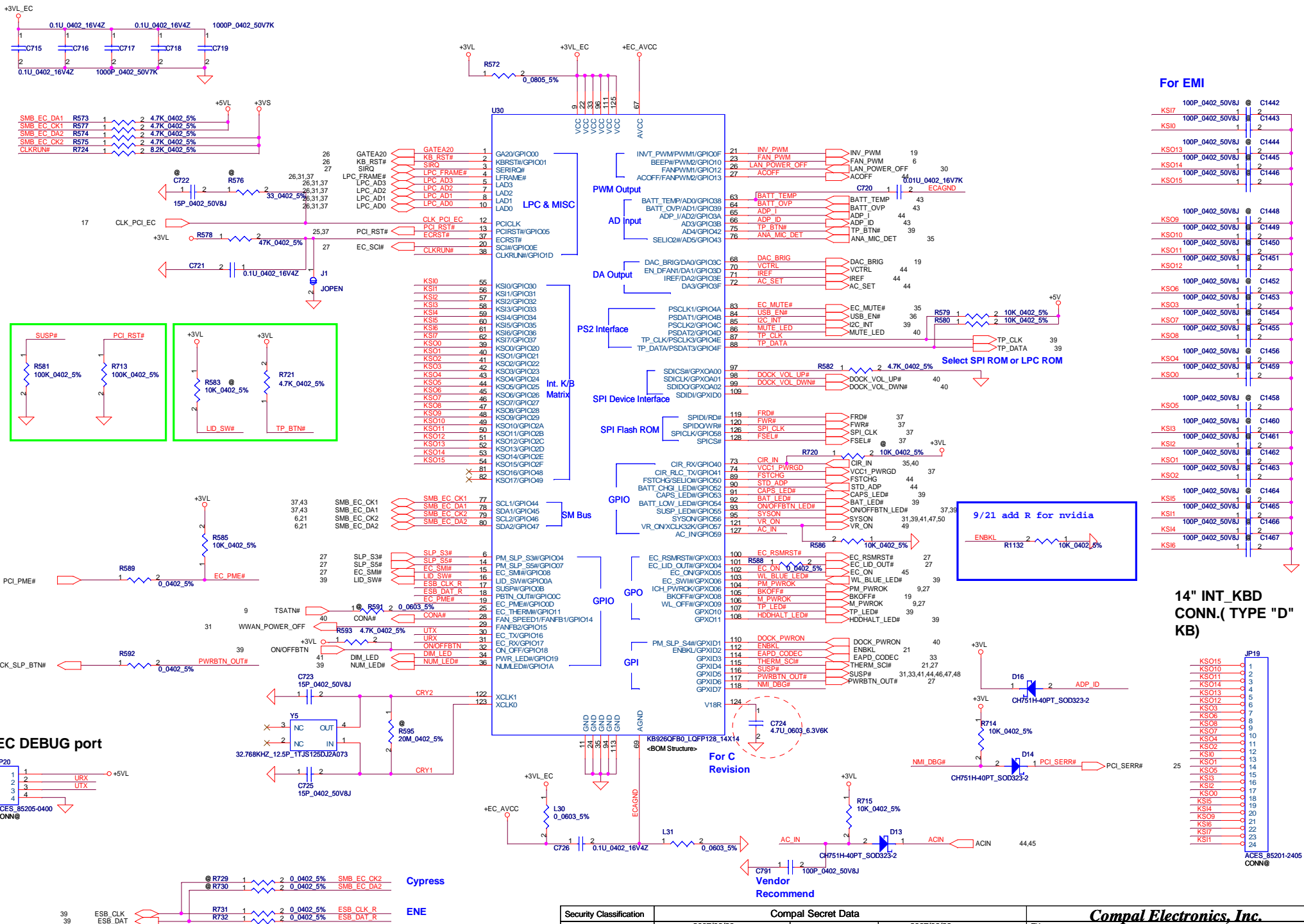


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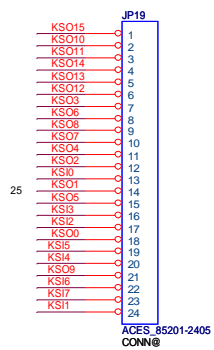


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Size			<b>BIOS ROM</b>	
Document Number			<b>Montevina Consumer Discrete</b>	
Date:	Friday, October 05, 2007	Sheet	37	of 51

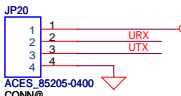


**14" INT\_KBD CONN.( TYPE "D" KB)**



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EC KB926/KB Conn.		0.1	
Size	Document Number	Montevina Consumer Discrete	
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**EC DEBUG port**



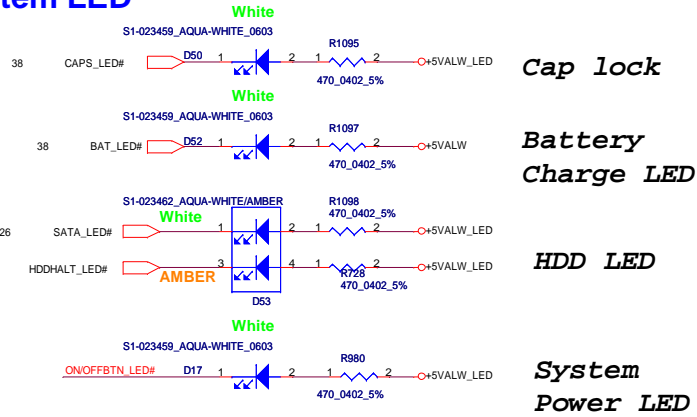
**Cypress**

**ENE**

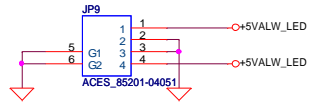
**For C Revision**

**Vendor Recommend**

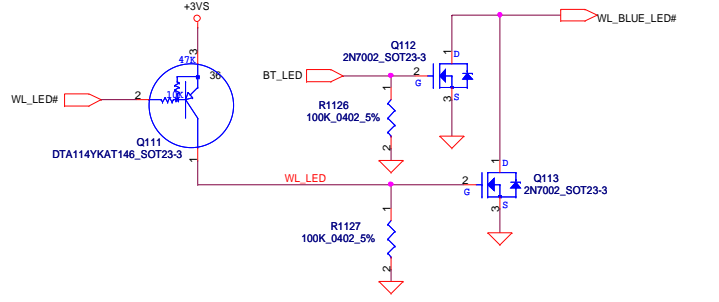
# System LED



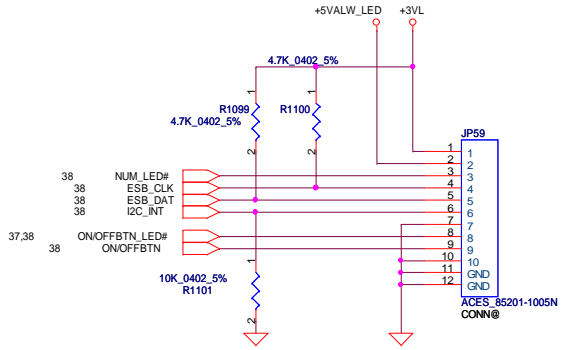
# Keyboard backlight Conn



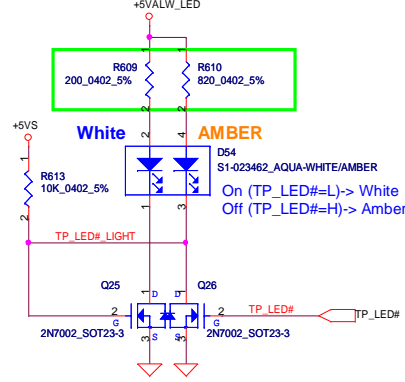
# Mini card LED



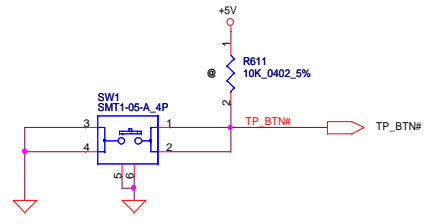
# Capacitor Sensor Conn



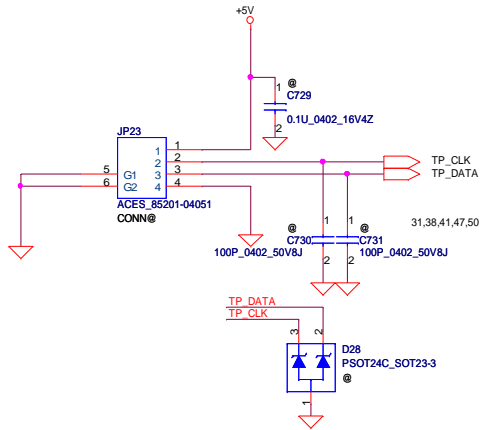
# TouchPAD ON/OFF LED



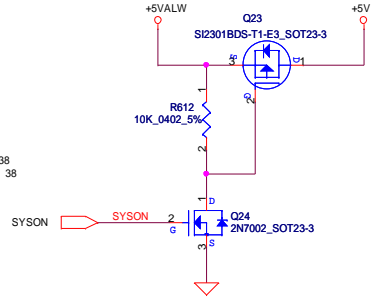
# TP ON/OFF



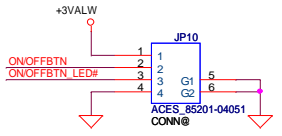
# T/P Board



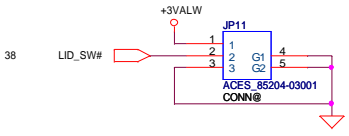
# T/P Power



# ON/OFF Button Connector

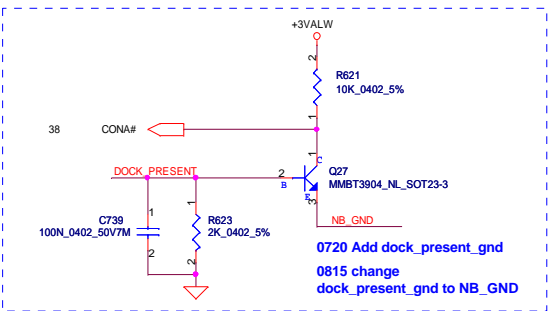
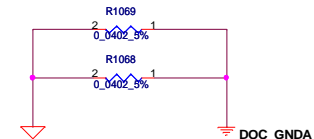
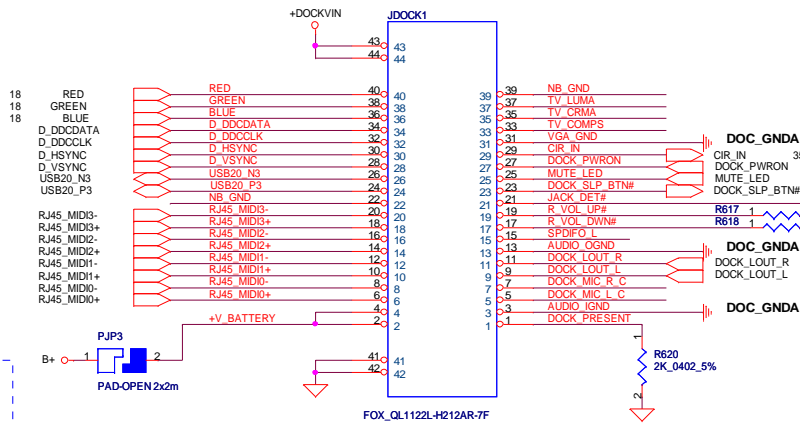


# Reed Switch Connector

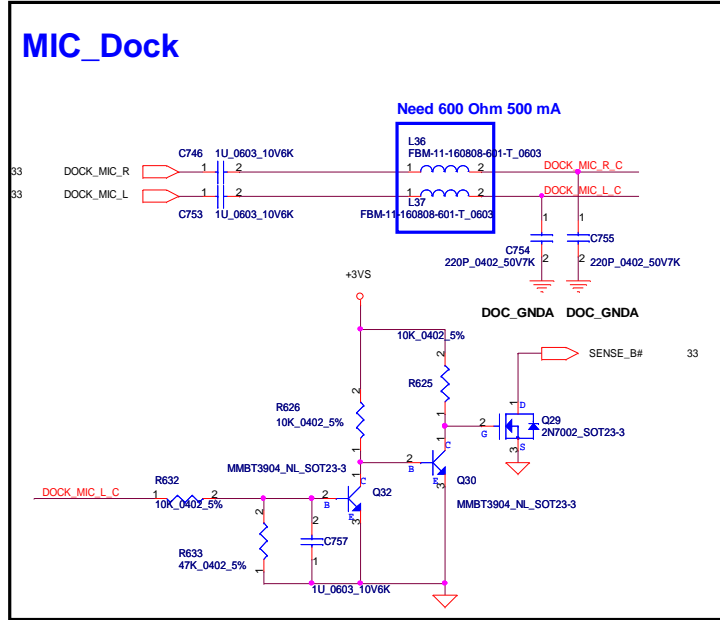
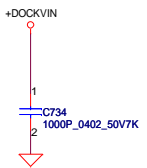
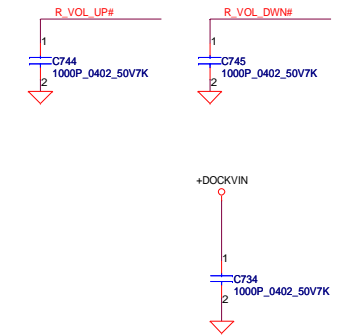
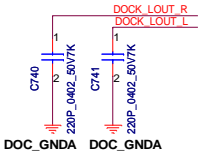
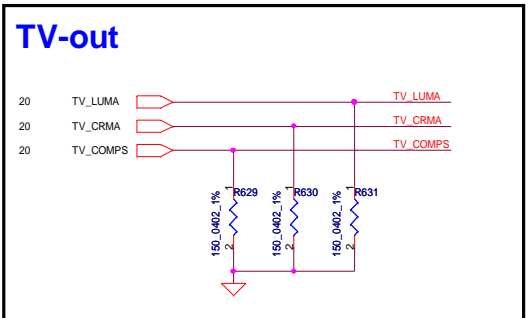
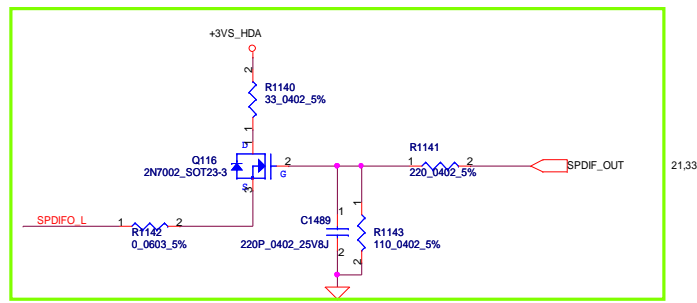


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# Atlas/ Saturn Dock



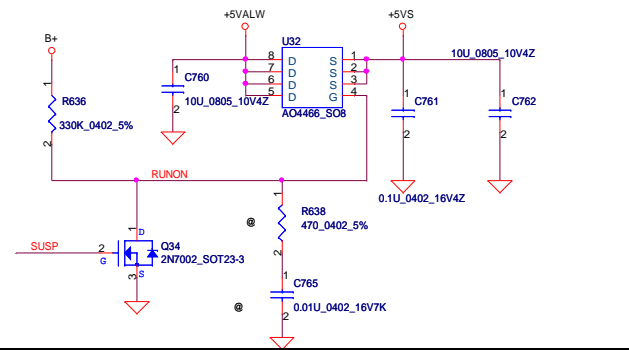
need change to reverse type connector



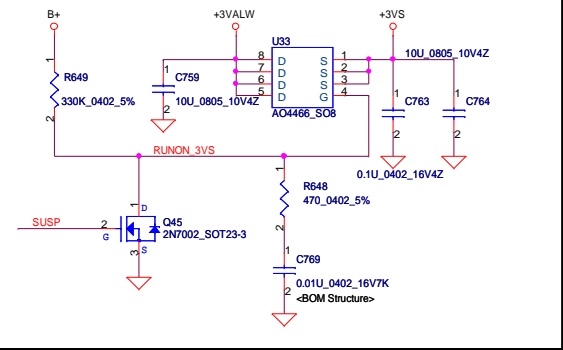
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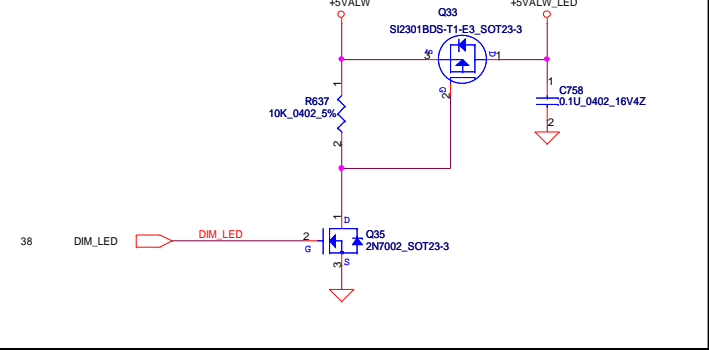
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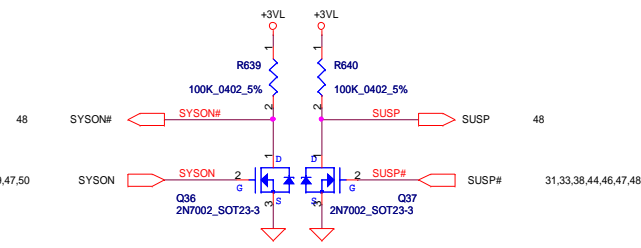
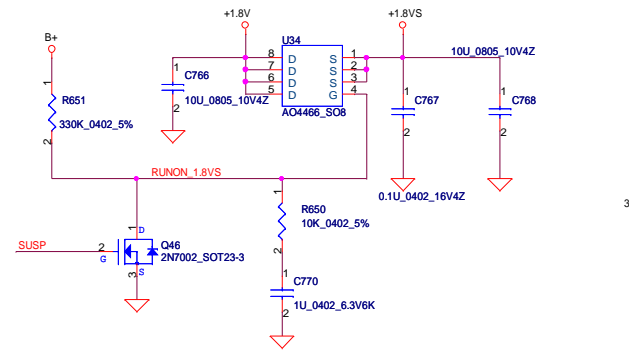
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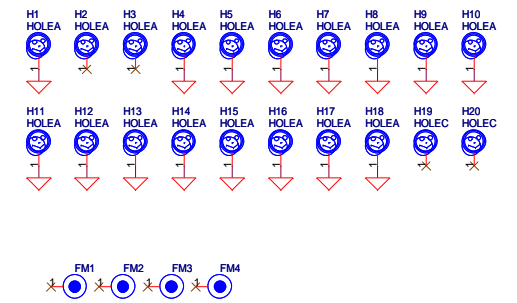
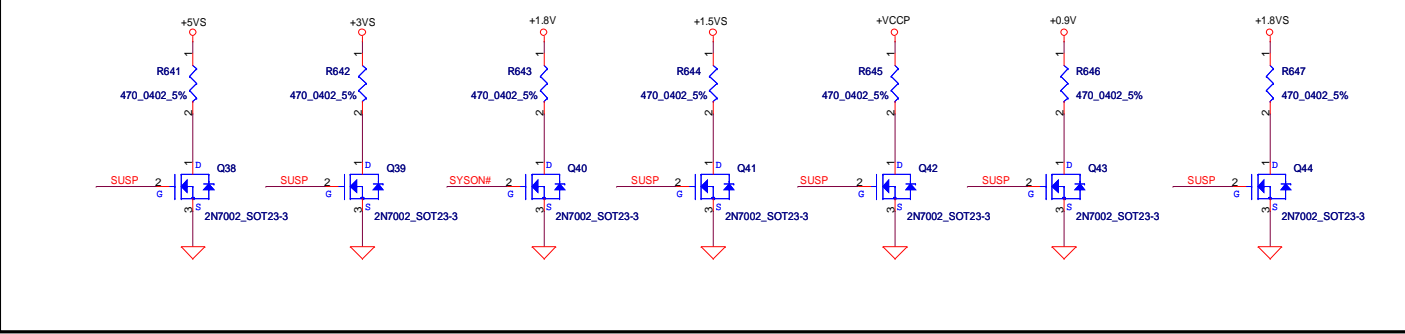
### DIM LED



### +1.8V to +1.8VS Transfer

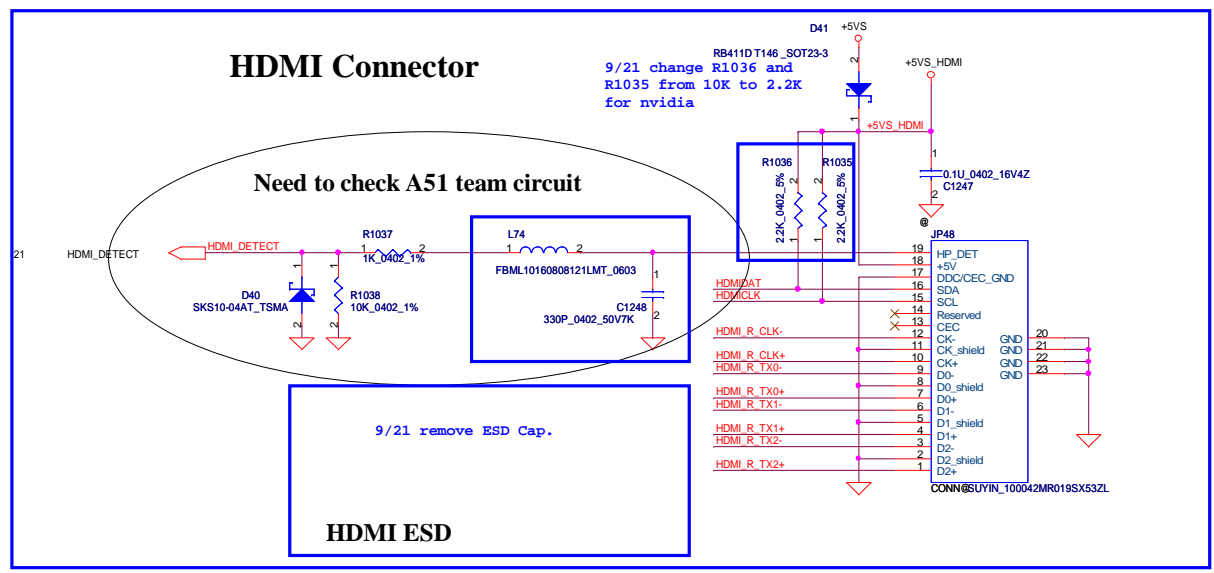
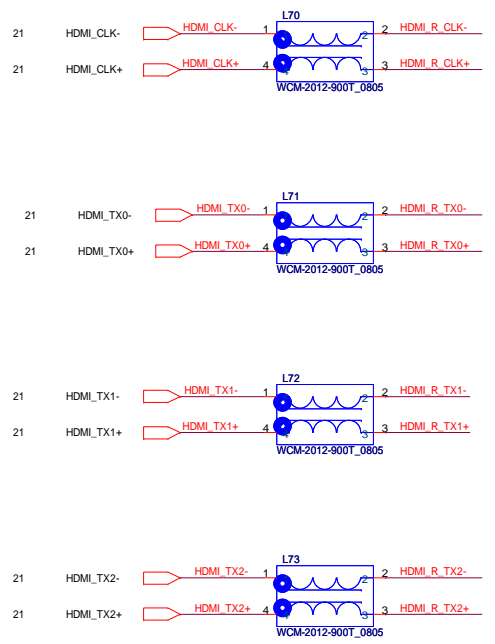
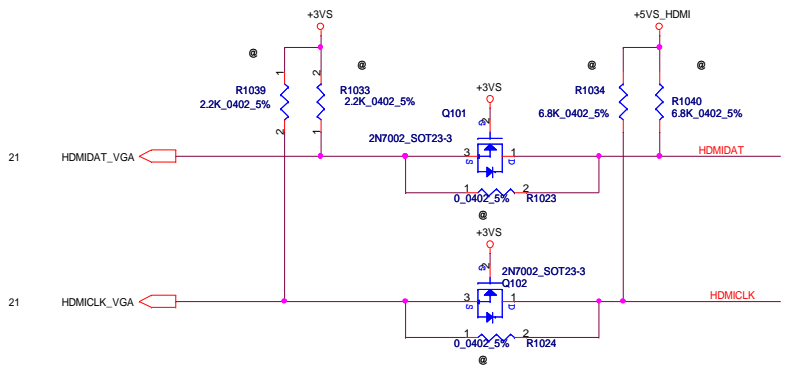


### Discharge circuit

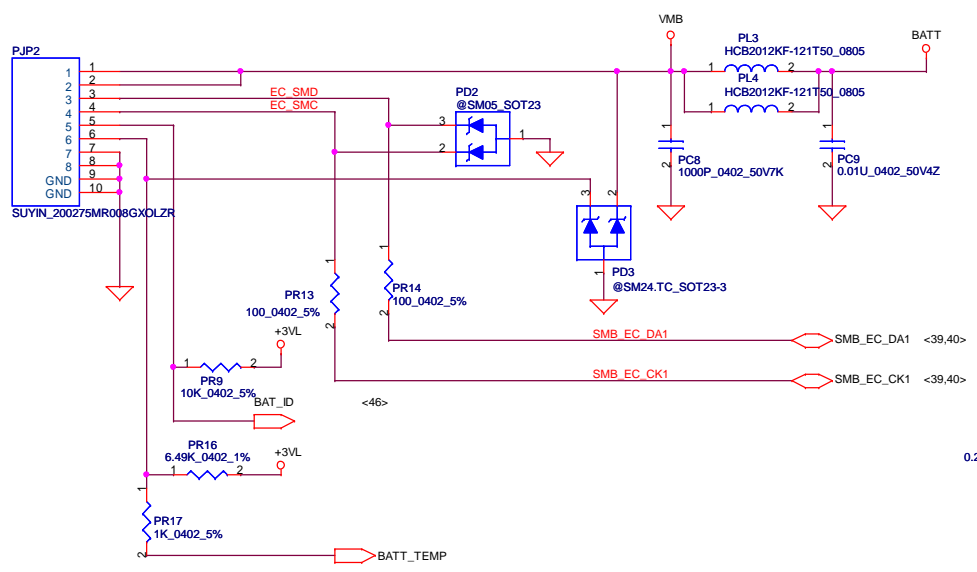
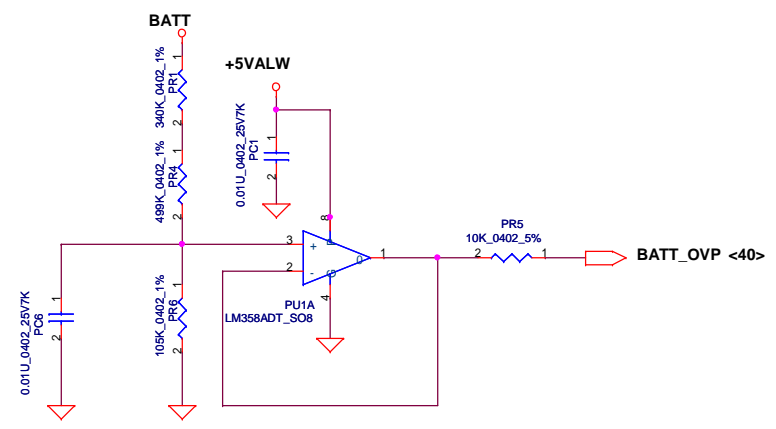
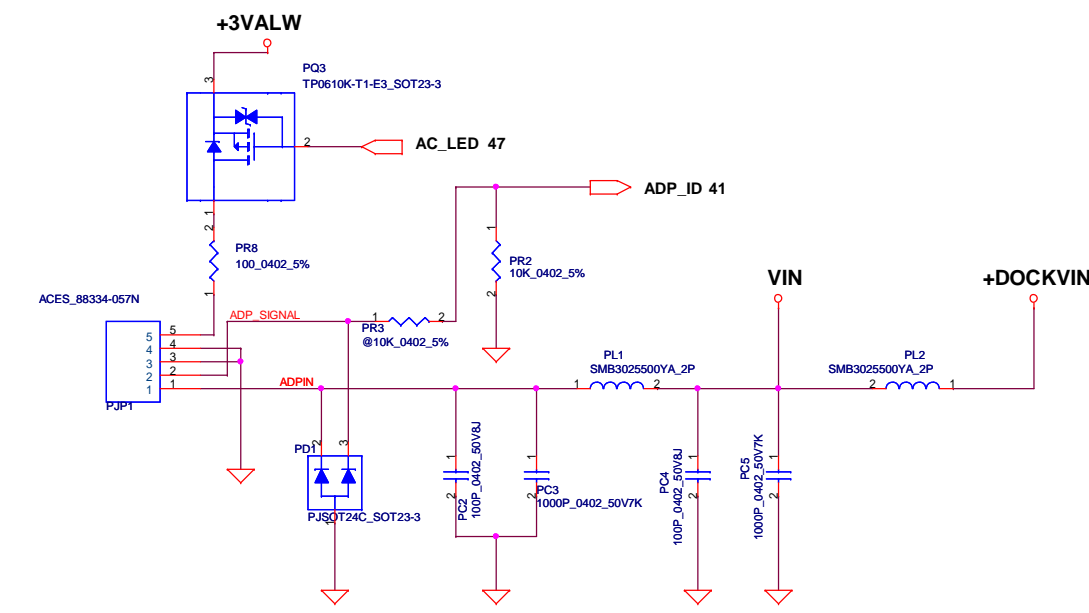


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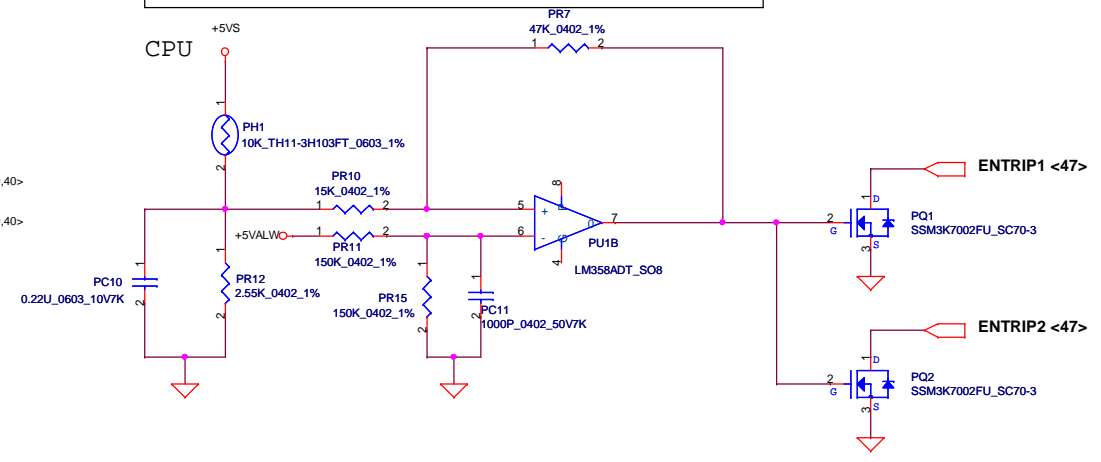
netmail@hmail.com



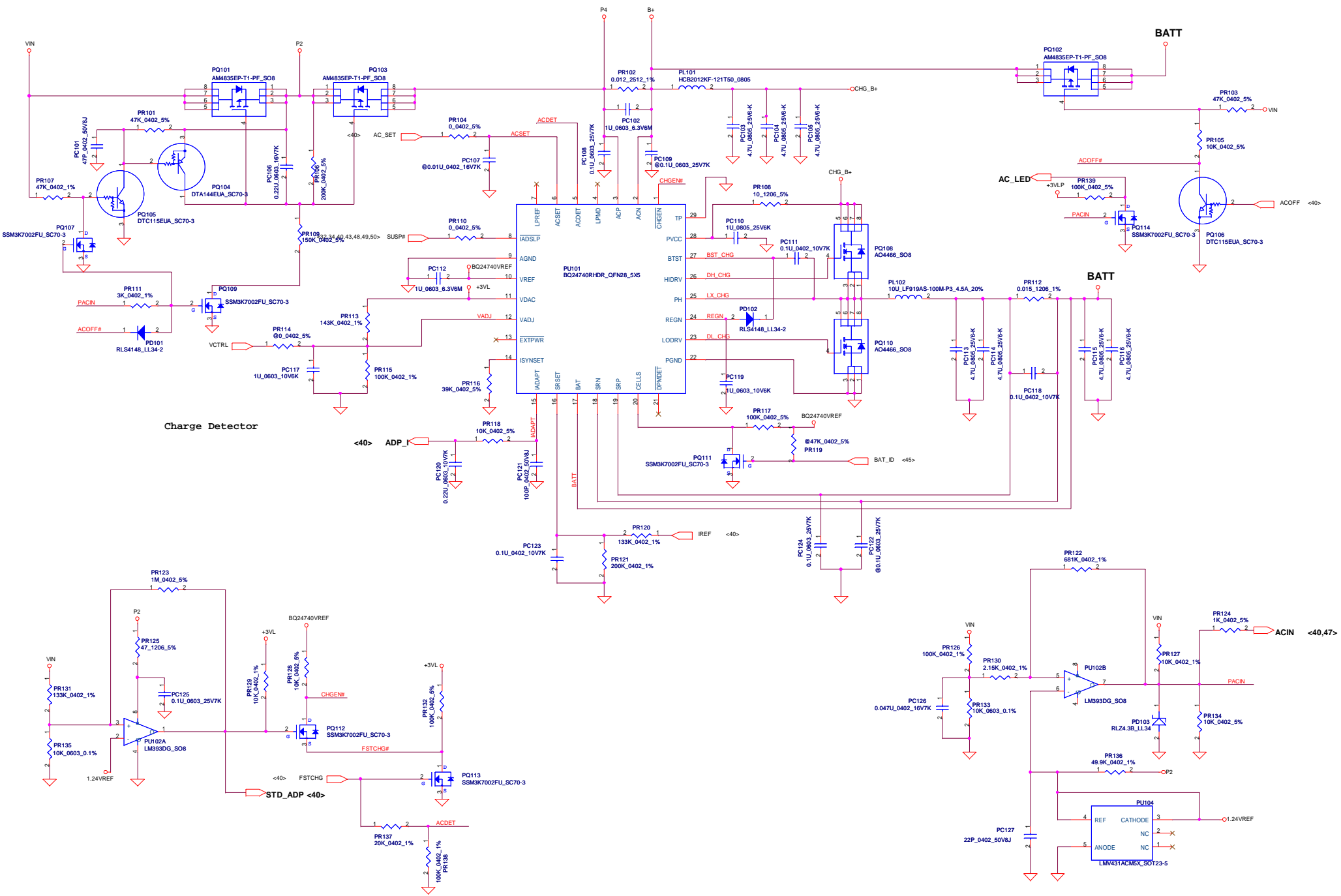
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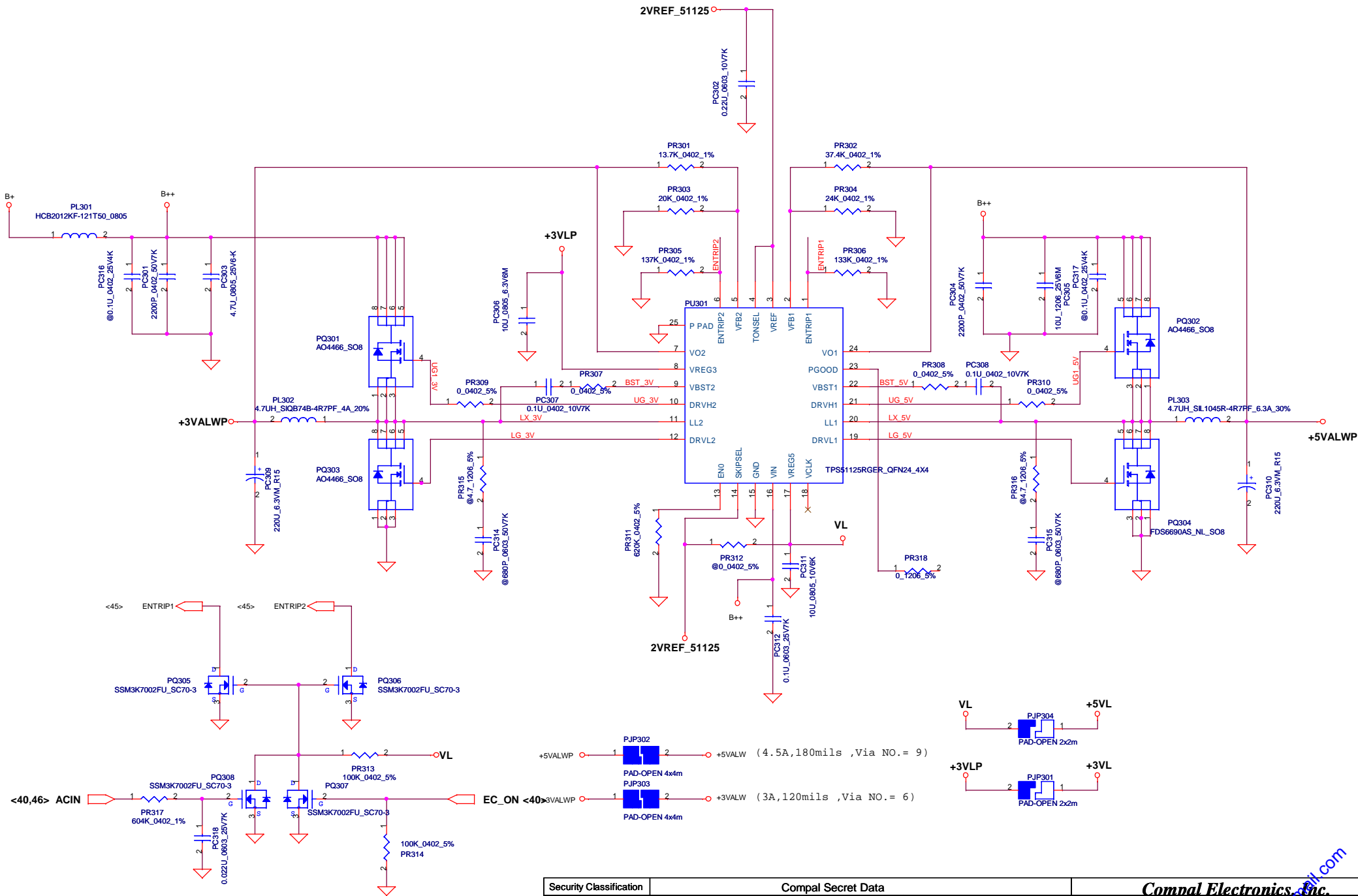
PH1 under CPU bottom side :  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 47 +/-3 degree C



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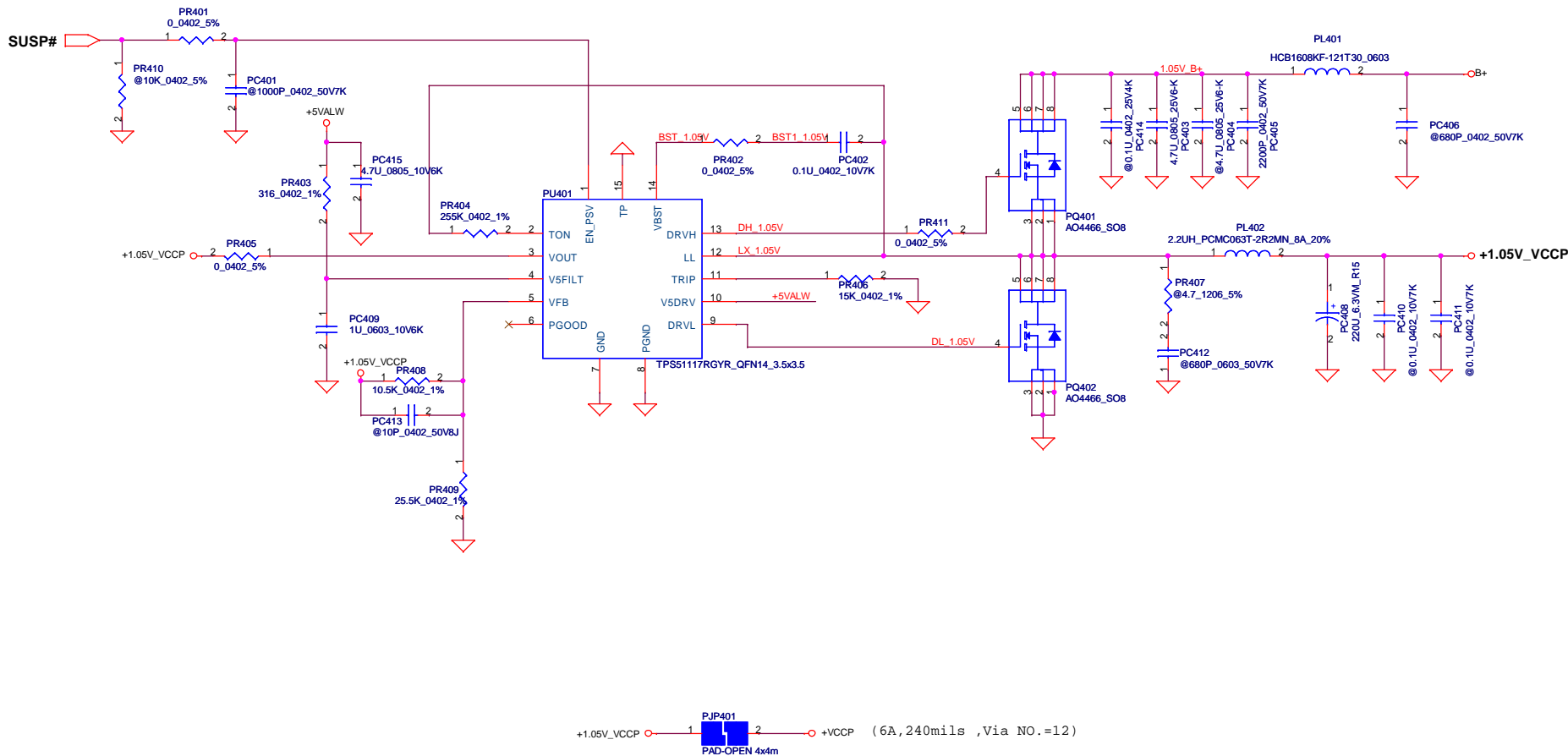


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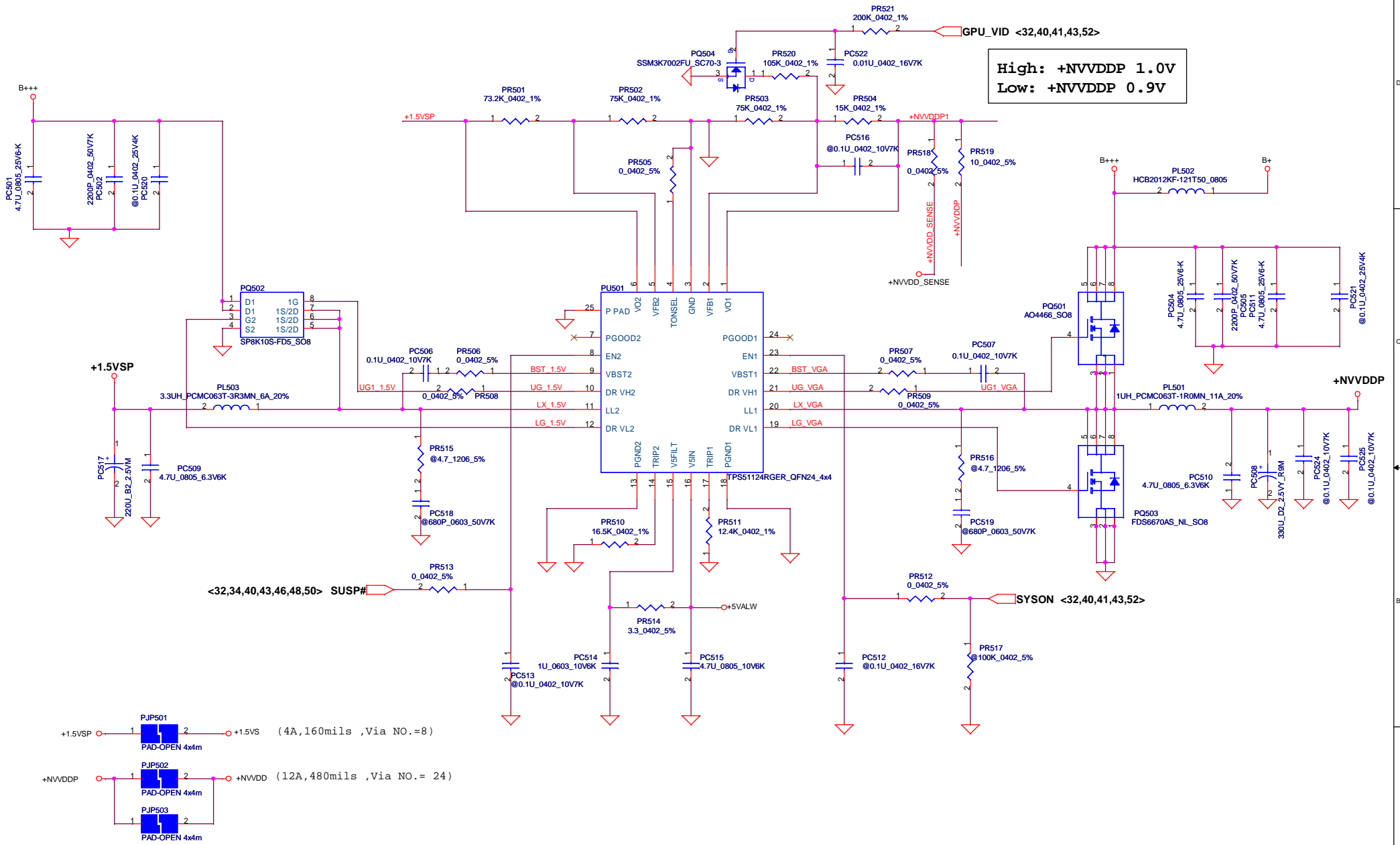
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+1.05V\_VCCP 1 PJP401 2 +VCCP (6A,240mils ,Via NO.=12)  
PAD-OPEN 4x4m

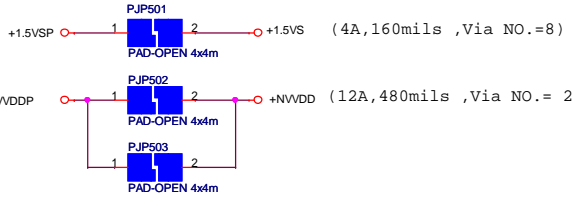
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				Date:	Friday, October 05, 2007
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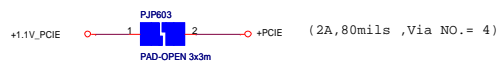
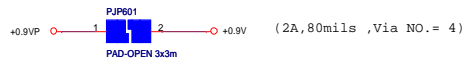
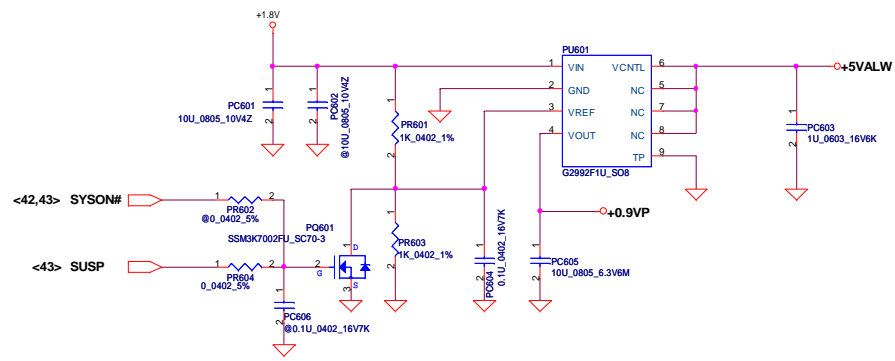
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Low: +NVVDDP 0.9V

<32,34,40,43,46,48,50> SUSP#

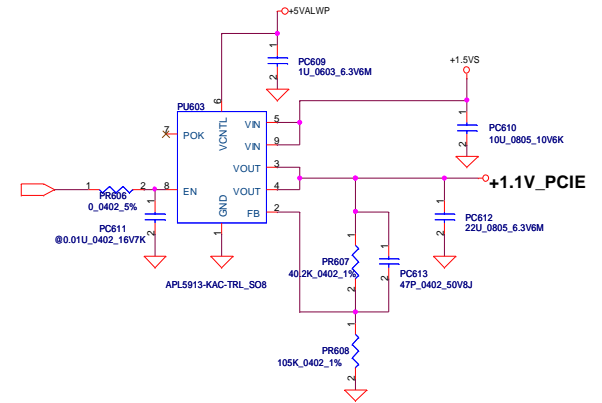
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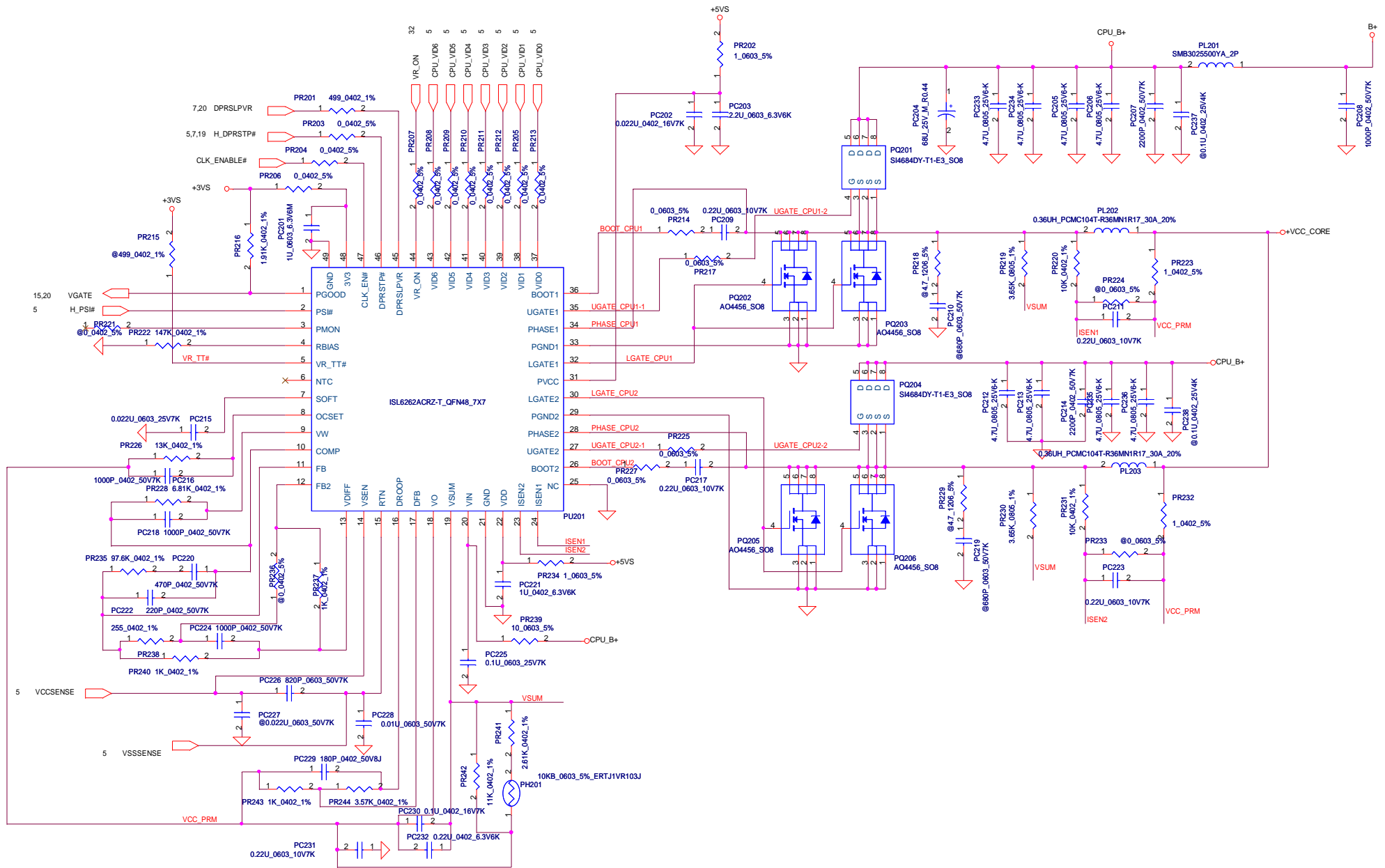


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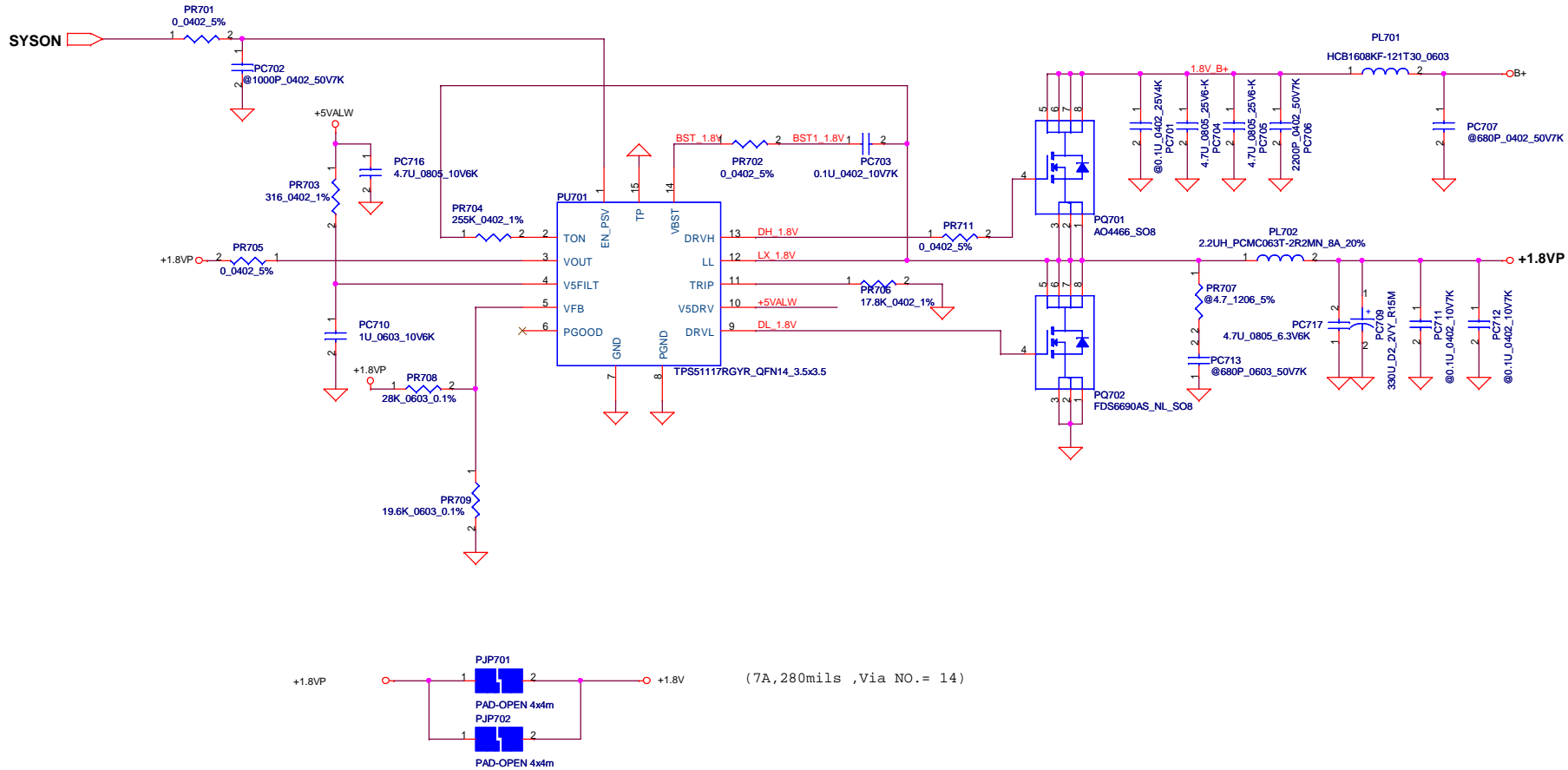




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