QT8 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 7,8
DDRII-SODIMM2 PAGE 7,8
DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E
PCI-Express 16X

NORTH BRIDGE
RX781 / RS780MN
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

ATI M82-S for Discrete only
64 Bit,DDR2*4
M82-SCE A11
PAGE 17,18,19 20,21,22

Side port
256mb RAM for UMA only PAGE 8

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

Cable Docking PAGE 37
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

X1 LAN
Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN)
PAGE 31,32

X1 Express Card (NEW CARD) PAGE 33

X3 Mini PCI-E Card (Wireless LAN/TV TUNNER) PAGE 36

RJ45 PAGE 31

ALINK X4

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

USB2.0
1,8,9 USB2.0 Ports X3 PAGE 30
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2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30
3 Flash Media for UMA only RTS5158 PAGE 25
Touch Screen for Discrete only

SATA0,1 150MB
TWO SATA - HDD PAGE 33

SATA0 150MB
SATA - CD-ROM PAGE 33

SATA4 150MB
E-SATA PAGE 30

PCIE BUS
JMICRON JMD380 for Discrete only PAGE 27

Azalia
IDT 92HD71B7 PAGE 27
AUDIO Amplifier TPA6017A2 PAGE 28
MDC CONN PAGE 29
IEEE1394 connect for Discrete only PAGE 26
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LPC

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Touch Pad PAGE 34
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Capacitive Sense SW PAGE 34

ENE KBC
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SYSTEM CHARGER(ISL6251A) PAGE 44
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DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
VGACORE(1.1V~1.2V)Oz8118 PAGE 42
CPU CORE ISL6265A PAGE 40

SMBUS TABLE

SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, February 19, 2008 Sheet 1 of 45

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653,R656,R612 STUFF	R653,R656,R612 NC	To M82-S 27Mhz - RX780 only

+1.2V L49 BLM18PG181SN1D(180,1.5A)_6 60 ohm, 0.5A
600 ohms@100Mhz
C523 10U/6.3V_8 C518 C496 C527 C521 C476 C515 0.1U/10V_4
+1.2V_CLKVDDIO

DCR: 0.5 ohm
600 ohms@100Mhz
+3V L51 BLM18PG181SN1D(180,1.5A)_6 +3V_CLKVDD 60 ohm, 0.5A
C541 10U/6.3V_8 C468 C473 C512 C522 C508 C500 C474 C471 C469 0.1U/10V_4
+3V_CLKVDD

+3V_CLKVDD L42 BLM18PG181SN1D(180,1.5A)_6 +3V_CLK_VDDA
C464 10U/6.3V_8 C482 C470 0.1U/10V_4
Place very close to C/G

U10A SLG8SP626VTR

49	VDDA	CPUKG0T_LPRS	56 CPUCLKP
48	GNDA	CPUKG0C_LPRS	55 CPUCLKN
62	VDDREF	ATIG0T_LPRS	33 NBGFX_CLKP
66	GNDREF	ATIG0C_LPRS	32 NBGFX_CLKN
		ATIG1T_LPRS	31 EXT_GFX_CLKP
		ATIG1C_LPRS	30 EXT_GFX_CLKN
		ATIG2T_LPRS	26
		ATIG2C_LPRS	25
69	VDD48	SB_SRC0T_LPRS	40 PCIE_MINI2_CLKP
29	VDDATIG	SB_SRC0C_LPRS	39 PCIE_MINI2_CLKN
54	VDDCPU	SB_SRC1T_LPRS	35 CLK_PCIE_CARD
61	VDDHTT	SB_SRC1C_LPRS	34 CLK_PCIE_CARD#
38	VDDSB_SRC		
17	VDDSRC		
44	VDDSATA		
3	VDDDOT		
53	VDDCPU_IO	SRC0T_LPRS	23 NBGPP_CLKN_R
28	VDDATIG_IO	SRC0C_LPRS	22 NBGPP_CLKN_L
37	VDDSB_SRC_IO	SRC1T_LPRS	21 PCIE_NEW_CLKP
12	VDDSRC_IO1	SRC1C_LPRS	20 PCIE_NEW_CLKN
18	VDDSRC_IO2	SRC2T_LPRS	16 PCIE_MINI1_CLKP
		SRC2C_LPRS	15 PCIE_MINI1_CLKN
		SRC3T_LPRS	14 SBLINK_CLKP
		SRC3C_LPRS	13 SBLINK_CLKN
		SRC4T_LPRS	10 SBSRC_CLKP
		SRC4C_LPRS	9 SBSRC_CLKN
		SRC5T_LPRS	8 PCIE_LAN_CLKP
		SRC5C_LPRS	7 PCIE_LAN_CLKN
72	GND48	SRC6T/SATAT_LPRS	46
27	GNDATIG1	SRC6C/SATAC_LPRS	45
6	GNDDOT	SRC7T_LPRS/27Mhz_SS	5 CLK_VGA_27M_SS
52	GNDCPU	SRC7C_LPRS/27Mhz_NS	4 CLK_VGA_27M_NSS
58	GNDHTT		
47	GNDSATA		
36	GNDSB_SRC		
11	GNDSRC1		
19	GNDSRC2		
67	X1	HTT0T/66M_LPRS	60
68	X2	HTT0C/66M_LPRS	59 NBHTREFCLK0P
		48MHz_0	71 NBHTREFCLK0N
		48MHz_1	70 CLK48MUSB
57	PD#	REF0/SEL_HTT66	65 SEL_HT66
		REF1/SEL_SATA	64 SEL_SATA
1	SMBCLK	REF2/SEL_27	63 SEL_27
2	SMBDAT		
		CLKREQ0#	24 CLKREQ0#
		CLKREQ1#	51 EXT_NWD_CLK_REQ#
		CLKREQ2#	50 CLKREQ2#
		CLKREQ3#	43 CLKREQ3#
		CLKREQ4#	42 CLKREQ4#
41	SB_SRC_SLOW#		

Place within 0.5" of CLKGEN
R196 *261_4
Del RP for TP on PV
RP43 RP54 RP53 RP48 RP55 RP51 RP49 RP47 RP45 RP44 4 2 3 *0_4P2R_4
CPUCLKP 3
CPUCLKN 3
NBGFX_CLKP 10
NBGFX_CLKN 10
EXT_GFX_CLKP 17
EXT_GFX_CLKN 17
to NB for external Graphics reference clock
to M82-S -RX780 only
T196 T84
PCIE_MINI2_CLKP 36
PCIE_MINI2_CLKN 36
CLK_PCIE_CARD 26
CLK_PCIE_CARD# 26
to TV TUNER CARD
to PCIE-CARD READER
Del RP52 for NBGPP CLK
T59 T62
PCIE_NEW_CLKP 33
PCIE_NEW_CLKN 33
PCIE_MINI1_CLKP 36
PCIE_MINI1_CLKN 36
SBLINK_CLKP 10
SBLINK_CLKN 10
SBSRC_CLKP 12
SBSRC_CLKN 12
PCIE_LAN_CLKP 31
PCIE_LAN_CLKN 31
to EPRESS CARD
to WLAN
to NB for AC-LINK reference clock
to SB
to PCIE-LAN
SI-1 Modified --remove to ROBSON
R527 33_4 OSC_SPREAD
R515 75/F_4
R490 100/F_4
OSC_SPREAD 18
EVGA-XTALI 18
SSIN - for M82 - 3.3V level input
X_TALIN --for M82 -1.8V level input
R193 R194 R201 R192 0_4 33_4
NBHT_REFCLKP 10
NBHT_REFCLKN 10
CLK_48M_CR 25
CLK_48M_USB 13
T58 T167
EXT_NWD_CLK_REQ# 33

C466 33P/50V_4 CG_XIN
Y2 14.318MHZ
C465 33P/50V_4 CG_XOUT
CG_XIN CG_XOUT CLK_PD#
can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/S0 power level
6,7,13,28,36 PCLK_SMB
6,7,13,28,36 PDAT_SMB
PCLK_SMB PDAT_SMB
14 CHIPSET_PCIE_SLOW_SB# D17 *CH501H-40PT L-F SB_SRC_SLOW#
when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

R186 Ra 158/F_4
R184 1 2 90.9/F_4 Rb
EXT_NB_OSC 10

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

THERMAL GND
73 eGND73
74 eGND74
75 eGND75
77 eGND77
76 eGND76
78 eGND78
U10B SLG8SP626VTR

C952 C953 C954 C955 C956 *10P/50V_4
EXT_NB_OSC CLK_48M_USB CLK_48M_CR EVGA-XTALI OSC_SPREAD
SI-1 modified -- reserve for EMT

+3V
R756 R757 R758 R759 *8.2K_4
CLKREQ0# CLKREQ2# CLKREQ3# CLKREQ4#
if use clock request pin , need to pull Hi for default sttting

ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

+3V_CLKVDD
R189 *8.2K_4 R195 8.2K_4
SEL_27 SEL_SATA SEL_HT66
R203 8.2K_4 R202 *8.2K_4
RS780M/RX780M

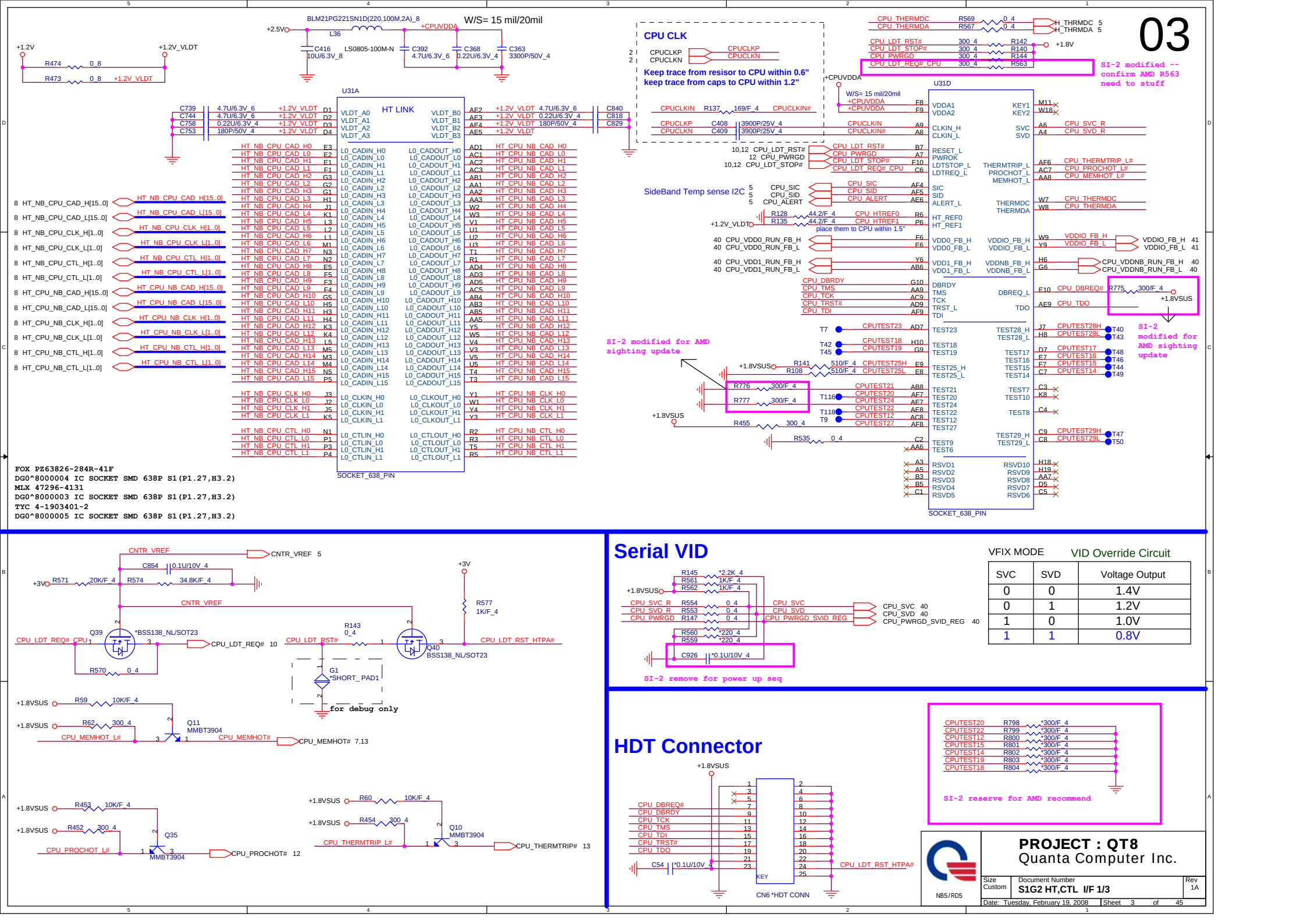
+3V
EXT_NWD_CLK_REQ# 8.2K_4 R219
CLK_PD# 8.2K_4 R204
SB_SRC_SLOW# 8.2K_4 R261

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

Date: Tuesday, February 19, 2008 Sheet 2 of 45


03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
HT LINK
SideBand Temp sense I2C
SI-2 modified -- confirm AMD R563 need to stuff
SI-2 modified for AMD sighting update
SI-2 modified for AMD sighting update
place them to CPU within 1.5"
U31A
U31D
SOCKET_638_PIN
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
Serial VID
SI-2 remove for power up seq
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
HDT Connector
SI-2 reserve for AMD recommend
for debug only
PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 1A
Date: Tuesday, February 19, 2008
Sheet 3 of 45

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

U31B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

750 mA

U31C

MEM:DATA

SOCKET_638_PIN

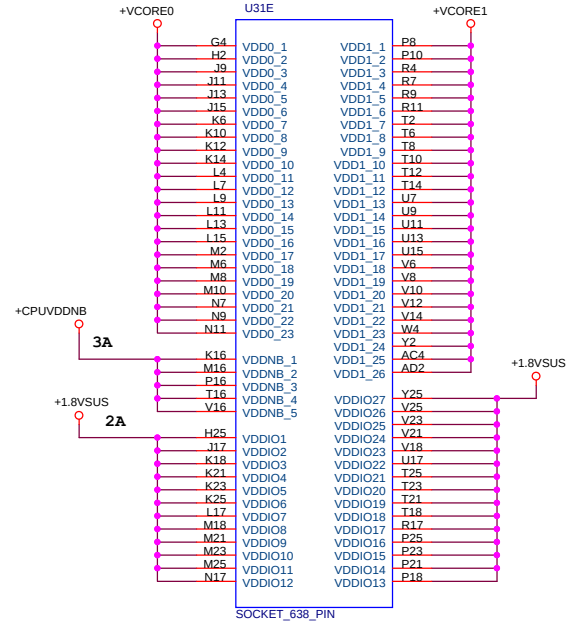
Place close to socket

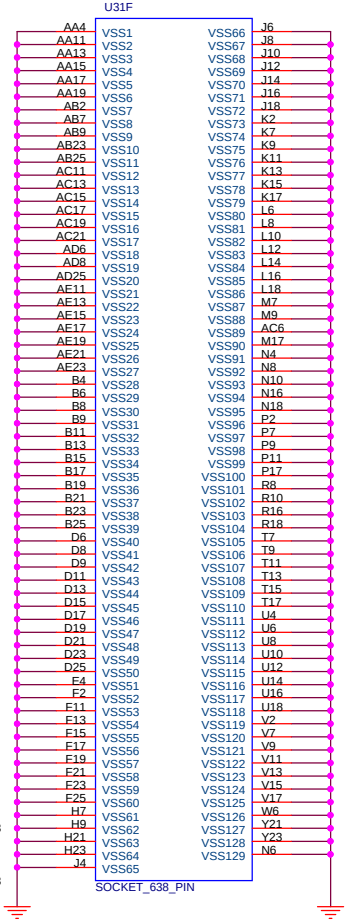
Close to CPU within 1500 mils

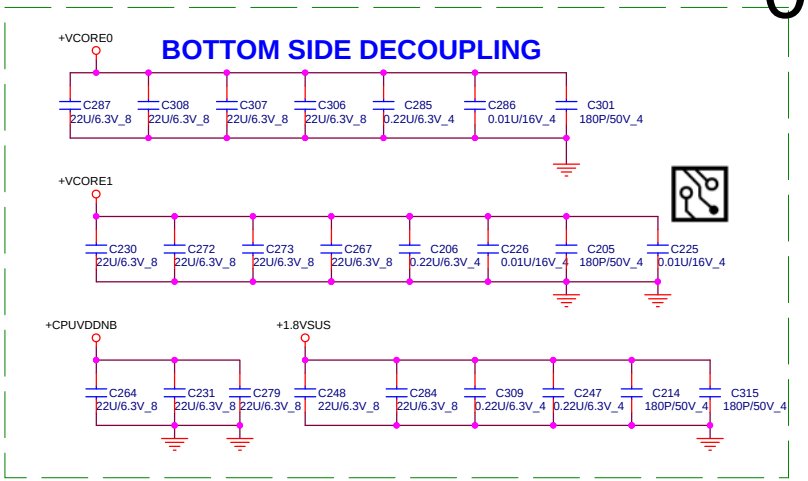
PROJECT :	QT8
Quanta Computer Inc.	
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 4 of 45

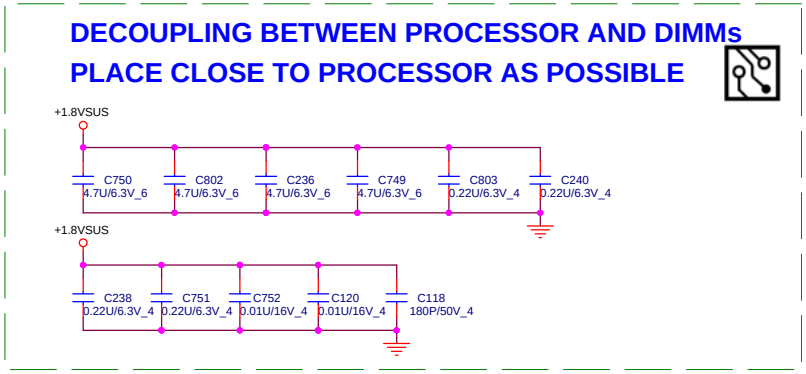
NB5/RD5

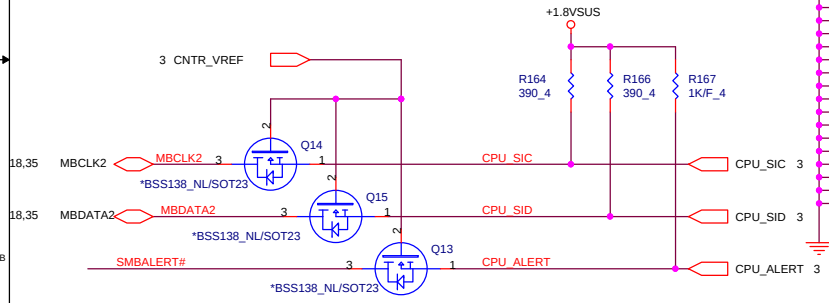
PROCESSOR POWER AND GROUND

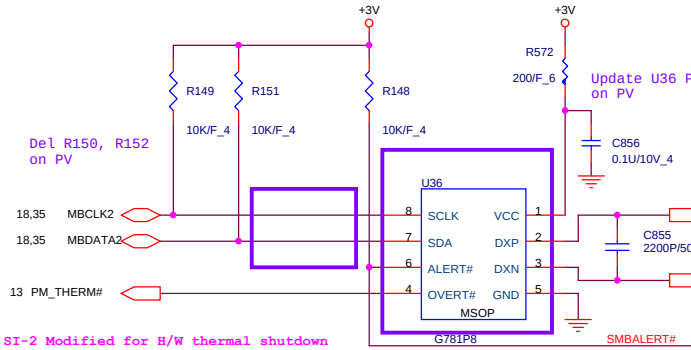


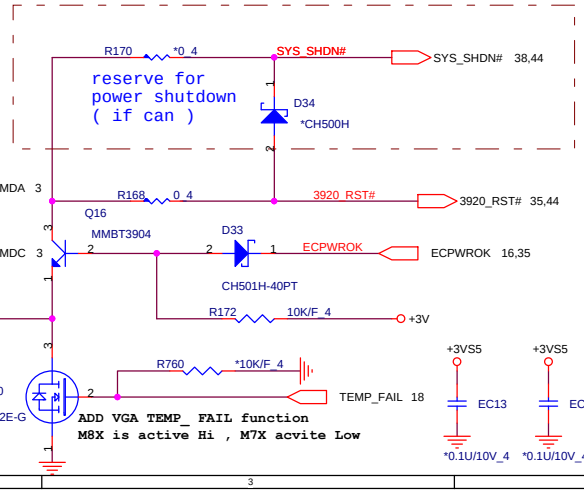


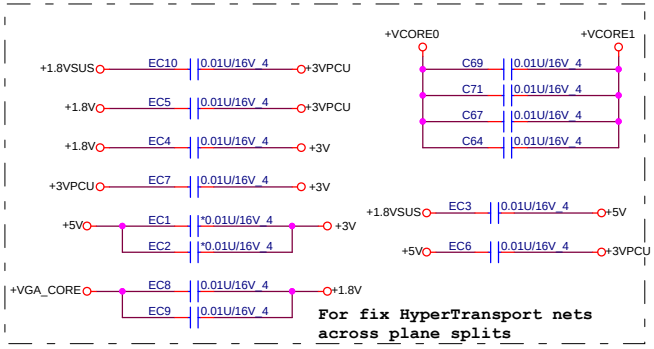


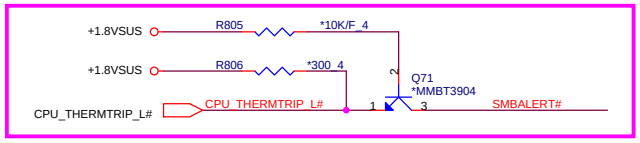


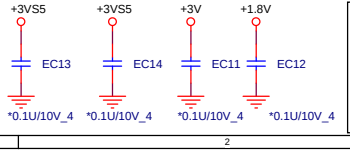




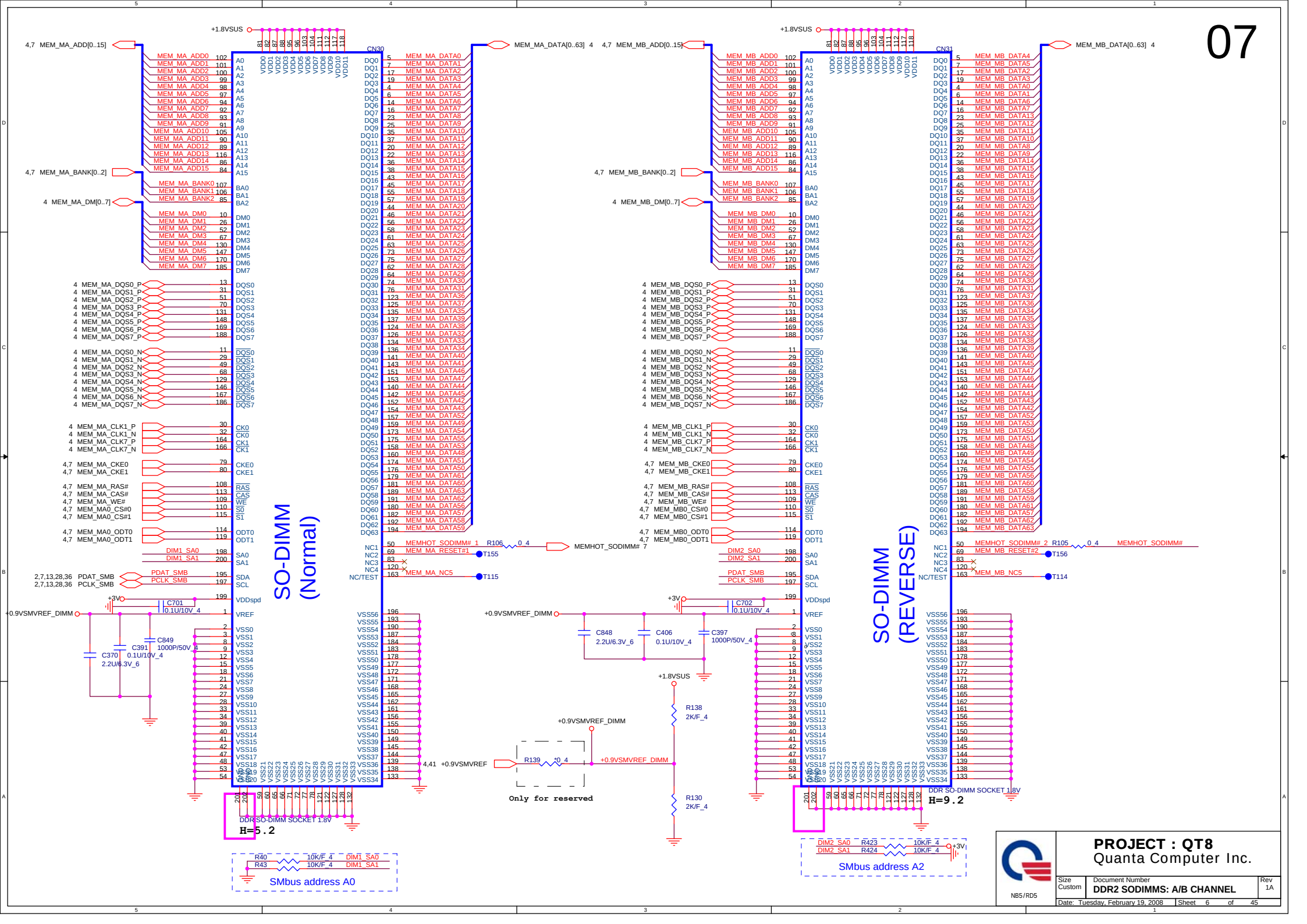








	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: **S1G2 PWR & GND 3/3**	Rev: 1A
NB5/RD5	Date: Tuesday, February 19, 2008	Sheet 5 of 45


SO-DIMM (Normal)
SO-DIMM (REVERSE)
CN30
CN31
+1.8VSUS
+3V
+0.9VSMVREF_DIMM
4,7 MEM_MA_ADD[0..15]
4,7 MEM_MA_BANK[0..2]
4 MEM_MA_DM[0..7]
MEM_MA_DATA[0..63] 4
4,7 MEM_MB_ADD[0..15]
4,7 MEM_MB_BANK[0..2]
4 MEM_MB_DM[0..7]
MEM_MB_DATA[0..63] 4
MEMHOT_SODIMM# 1
MEMHOT_SODIMM# 7
MEMHOT_SODIMM# 2
MEM_MA_RESET#1
MEM_MB_RESET#2
MEM_MA_NC5
MEM_MB_NC5
T155
T115
T156
T114
R106 0_4
R105 0_4
2,7,13,28,36 PDAT_SMB
2,7,13,28,36 PCLK_SMB
C701 0.1U/10V_4
C702 0.1U/10V_4
C370 2.2U/6.3V_6
C391 0.1U/10V_4
C849 1000P/50V_4
C848 2.2U/6.3V_6
C406 0.1U/10V_4
C397 1000P/50V_4
R138 2K/F_4
R130 2K/F_4
R139 0_4
4,41 +0.9VSMVREF
Only for reserved
DDR SO-DIMM SOCKET 1.8V
H=5.2
H=9.2
R40 10K/F_4 DIM1_SA0
R43 10K/F_4 DIM1_SA1
SMbus address A0
DIM2_SA0 R423 10K/F_4
DIM2_SA1 R424 10K/F_4
SMbus address A2
NB5/RD5
PROJECT : QT8
Quanta Computer Inc.
Size Custom
Document Number
DDR2 SODIMMS: A/B CHANNEL
Rev 1A
Date: Tuesday, February 19, 2008
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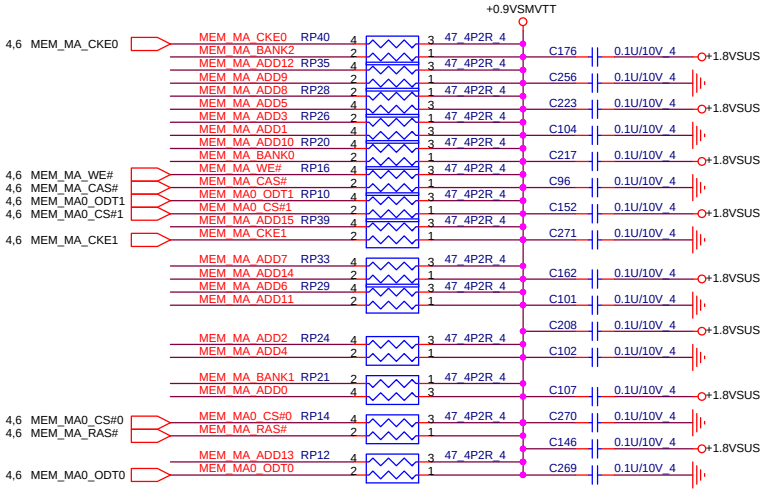
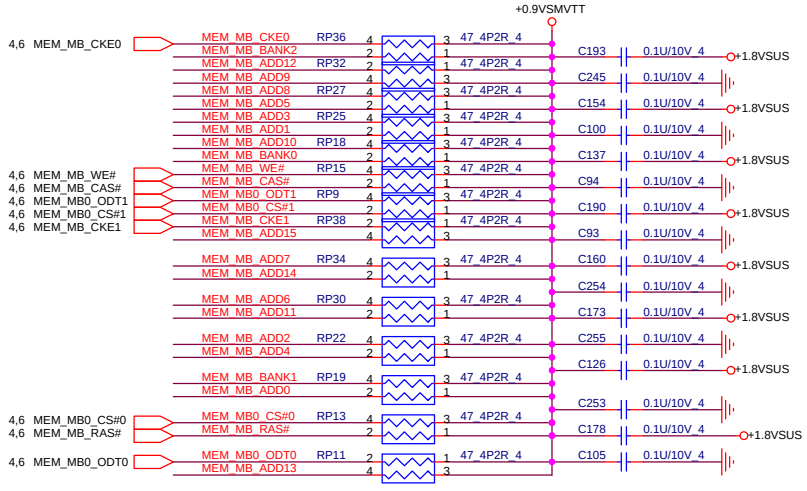
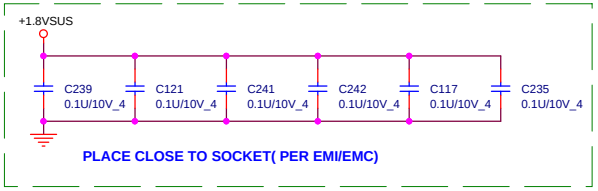
4,6 MEM_MA_ADD[0..15] — MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] — MEM_MA_BANK[0..2]

4,6 MEM_MB_ADD[0..15] — MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] — MEM_MB_BANK[0..2]

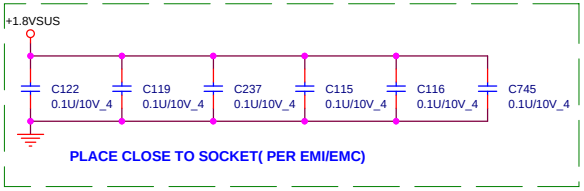


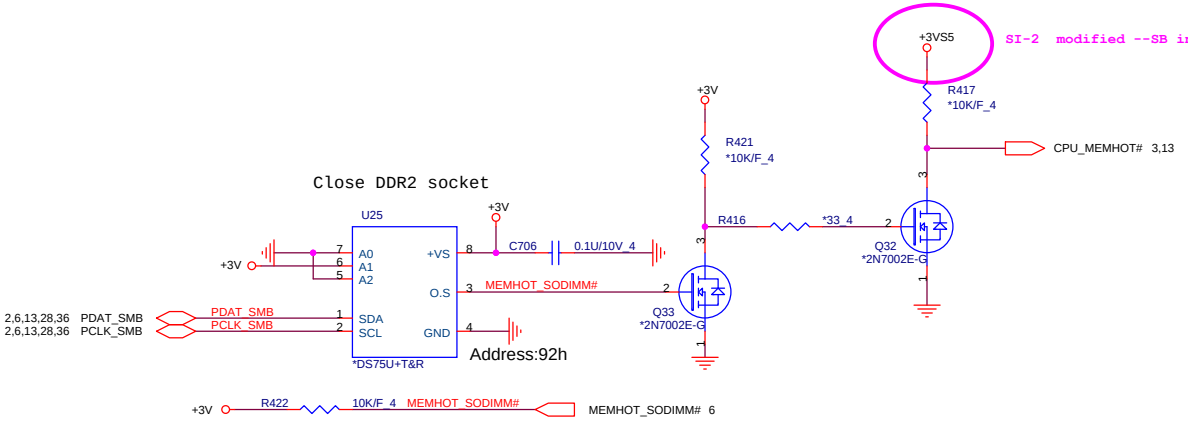


PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



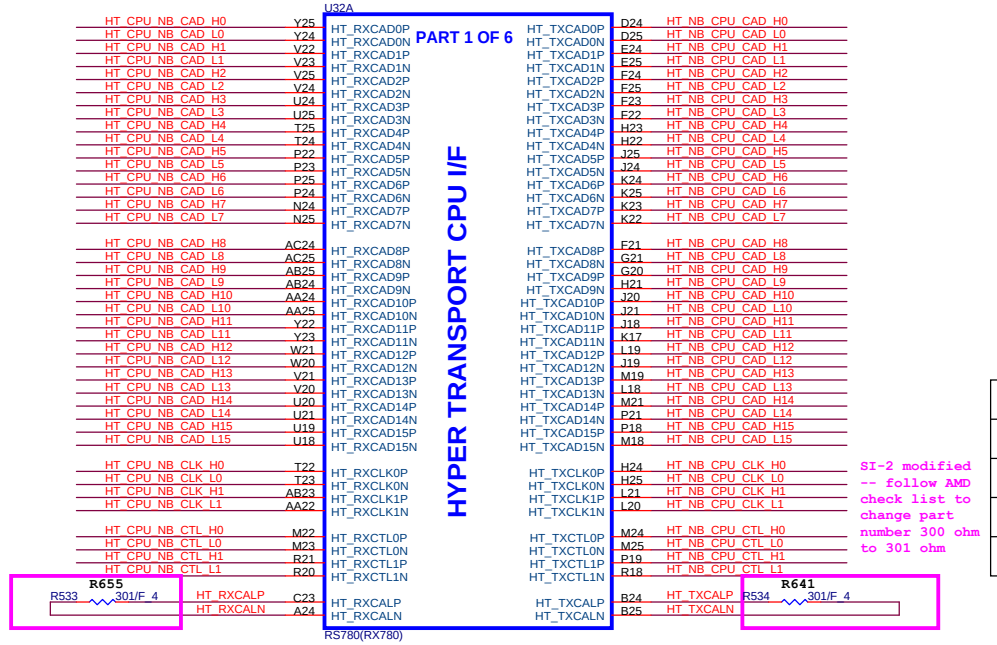


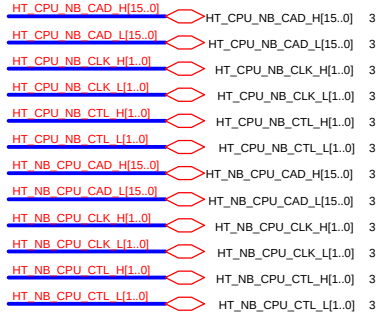
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

NB5/RD5

Date: Tuesday, February 19, 2008 | Sheet 7 of 45



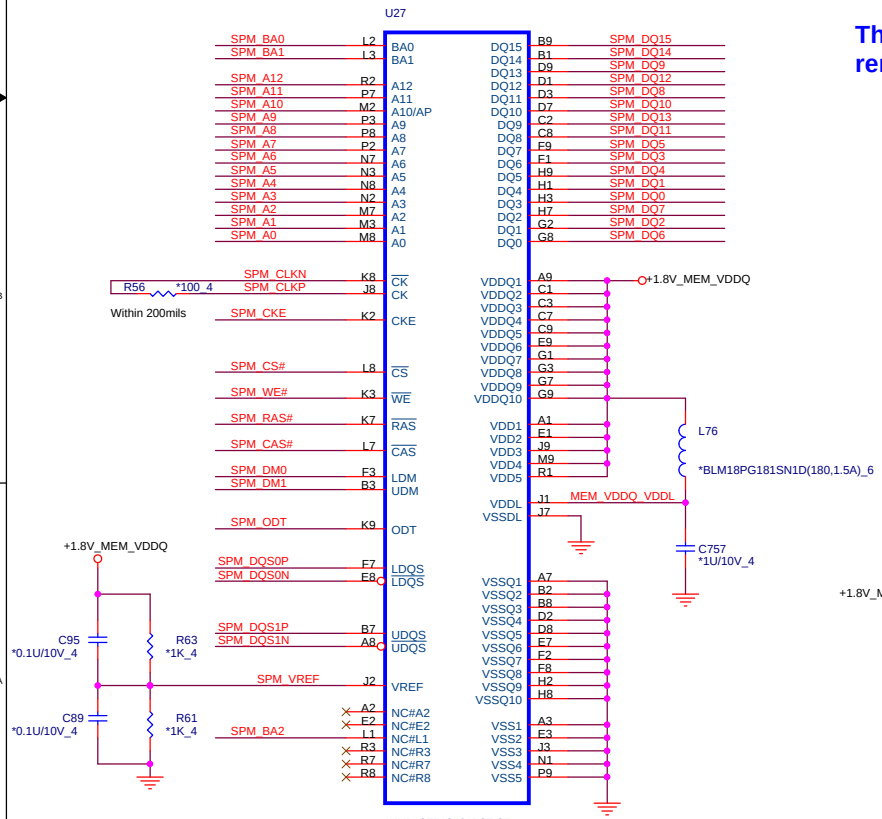


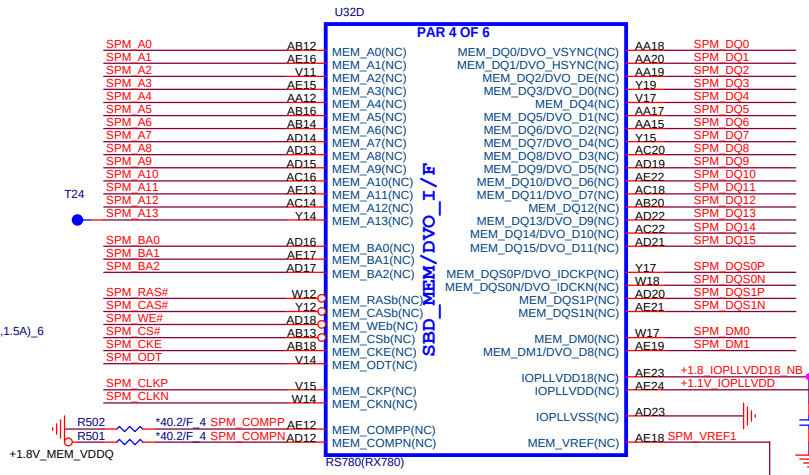
signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

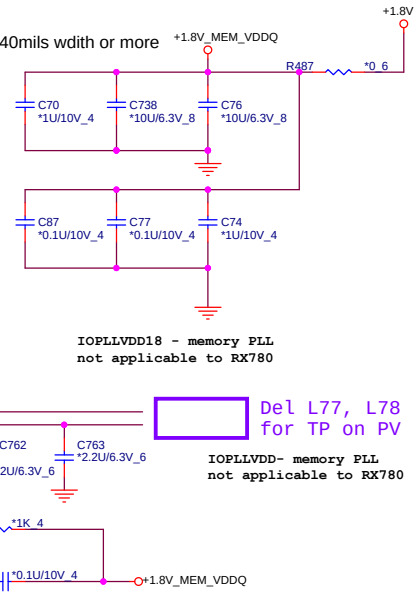
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

This block is for UMA RS780 only , RX780 can remove all component







PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A

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NB5/RD5

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NB5/RD5

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RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
3,12 CPU_LDT_RST# — R157 *0_4 — NB_RST# IN
RS780
12 NB_PLTRST# — R160 0_4
North Bridge RESET

R109 for UAM use 140 ohm

U32C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
18,24 CRT_R — R446 *0_4, R109 *150/F_4 — CRT_R_1 — G18
18,24 CRT_G — R445 0_4, R110 *150/F_4 — CRT_G_1 — G17, F18
18,24 CRT_B — R444 0_4, R111 *150/F_4 — CRT_B_1 — F18, F19
18,19,24 HSYNC_COM — R549 *0_4 — HSYNC_INT — A11
18,19,24 VSYNC_COM — R540 *0_4 — VSYNC_INT — B11
18,24 DDCDATA — R133 *0_4 — DDCDATA_INT — E8
18,24 DDCCLK — R134 *0_4 — DDCCLK_INT — F8
R119 *715/F_6 — DAC_RSET_NB — G14

PLL PWR
+1.1V_PLLVDD — A12
+1.8V_PLLVDD18 — D14, B12
+1.8V_VDDA18HTPLL — H17
+1.8V_VDDA18PCIEPLL — D7, E7

PM
16 NB_PWRGD_IN — NB_RST#_IN — D8
NB_PWRGD_IN — A10
NB_LDT_STOP# — C10
NB_ALLOW_LDTSTOP — C12

CLOCKS
2 NBHT_REFCLKP — NBHT_REFCLKP — C25
2 NBHT_REFCLKN — NBHT_REFCLKN — C24
2 EXT_NB_OSC — R117 0_4 — NB_REFCLK_P — E11
NB_REFCLK_N — F11
+1.1V — R125 4.7K_4, R120 4.7K_4 — RS780 RS780
2 NBGFX_CLKP — NBGFX_CLKP — T2
2 NBGFX_CLKN — NBGFX_CLKN — T1
Del NBGPP CLK
T168 — NBGPP_CLKP — U1
T169 — NBGPP_CLKN — U2
2 SBLINK_CLKP — SBLINK_CLKP — V4
2 SBLINK_CLKN — SBLINK_CLKN — V3

I/O
GFX_REFCLKP, GFX_REFCLKN
GPP_REFCLKP, GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)

MIS.
18,23 EDIDDATA — R547 *0_4 — NB_I2C_DATA — A9
18,23 EDIDCLK — R546 *0_4 — NB_I2C_CLK — B9
23 HDMI_DDC_DATA — R537 *0_4 — HDTV_DET — B8
23 HDMI_DDC_CLK — R544 *0_4 — RS740_DFT_GPIO0 — A8
RS740_DFT_GPIO1 — B7
T161, T158 — A7
39 DYN_PWR_EN — R27 0_4 STRP_DATA — B10
G11
T164 — RS780_AUX_CAL — C8

RS780 only
+3V — R536 4.7K_4 HDTV_DET
R539 4.7K_4 NB_I2C_DATA
R538 4.7K_4 NB_I2C_CLK

+3V_AVDD_NB — F12
+1.8V_AVDDDI_NB — F12, F14
+1.8V_AVDDQ_NB — G15, H15, H14
S-CD1 — E17, F17, F15
C_Pr(DFT_GPIO5), Y(DFT_GPIO2), COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0), REDb(NC), GREEN(DFT_GPIO1), GREENb(NC), BLUE(DFT_GPIO3), BLUEb(NC)
DAC_HSYNC(PWM_GPIO4), DAC_VSYNC(PWM_GPIO6), DAC_SDA(PCE_TCALRN), DAC_SCL(PCE_RCALRN)
DAC_RSET(PWM_GPIO1)
PLLVDD(NC), PLLVDD18(NC), PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1, VDDA18PCIEPLL2
SYSRESETb, POWERGOOD, LDTSTOPb, ALLOW_LDTSTOP
HT_REFCLKP, HT_REFCLKN
REFCLK_P/OSCIN(OSCIN), REFCLK_N(PWM_GPIO3)
I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)

TXOUT_L0P(NC) A22 — LA_DATAP0 — LA_DATAP0 23
TXOUT_L0N(NC) B22 — LA_DATAN0 — LA_DATAN0 23
TXOUT_L1P(NC) A21 — LA_DATAP1 — LA_DATAP1 23
TXOUT_L1N(NC) B21 — LA_DATAN1 — LA_DATAN1 23
TXOUT_L2P(NC) B20 — LA_DATAP2 — LA_DATAP2 23
TXOUT_L2N(DBG_GPIO0) A20 — LA_DATAN2 — LA_DATAN2 23
TXOUT_L3P(NC) A19 — LA_DATAP3 — T159
TXOUT_L3N(DBG_GPIO2) B19 — LA_DATAN3 — T157
TXOUT_U0P(NC) B18 — LB_DATAP0 — LB_DATAP0 23
TXOUT_U0N(NC) A18 — LB_DATAN0 — LB_DATAN0 23
TXOUT_U1P(PCIE_RESET_GPIO3) A17 — LB_DATAP1 — LB_DATAP1 23
TXOUT_U1N(PCIE_RESET_GPIO2) B17 — LB_DATAN1 — LB_DATAN1 23
TXOUT_U2P(NC) D20 — LB_DATAP2 — LB_DATAP2 23
TXOUT_U2N(NC) D21 — LB_DATAN2 — LB_DATAN2 23
TXOUT_U3P(PCIE_RESET_GPIO5) D18 — LB_DATAP3 — T163
TXOUT_U3N(NC) D19 — LB_DATAN3 — T160
TXCLK_LP(DBG_GPIO1) B16 — LA_CLK — LA_CLK 23
TXCLK_LN(DBG_GPIO3) A16 — LA_CLK# — LA_CLK# 23
TXCLK_UP(PCIE_RESET_GPIO4) D16 — LB_CLK — LB_CLK 23
TXCLK_UN(PCIE_RESET_GPIO1) D17 — LB_CLK# — LB_CLK# 23
VDDLTP18(NC) A13 — +1.8V_VDDLTP18_NB — B13
VSSLTP18(NC)
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB — B15
VDDLT18_2(NC)
VDDLT33_1(NC) A14 — +3V_VDLT33_NB — B14
VDDLT33_2(NC)
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

RS780 only
LVDS_DIGON(PCE_TCALRP) E9 — R132 *0_4 — DISP_ON — DISP_ON 19,23
LVDS_BLON(PCE_RCALRP) E7 — R126 *0_4 — LVDS_BLON — LVDS_BLON 18,23
LVDS_ENA_BL(PWM_GPIO2) G12 — R118 *0_4 — DPST_PWM — DPST_PWM 19,23
R121 *1.27K/F_4
R127 *1.27K/F_4
For RX780 only

TMDS_HPD(NC) D9 — TMDS_HPD0 — R545 *0_4 — TMDS_HPD 18,23
HPD(NC) D10 — TMDS_HPD1 — T162
UMA only
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB — R131 0_4 — SUS_STAT# 13
THERMALDIODE_P AE8 — R_NB_THRMDA — T136
THERMALDIODE_N AD8 — R_NB_THRMDC — T135
TESTMODE D13 — TEST_EN — R541 1.82K/F_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
RX780
RS780_AUX_CAL — R543 3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
VSYNC_COM — R124 3K_4 — +3V

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
HSYNC_COM — R129 3K_4 — +3V
R136 *3K_4

For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA — R548 10K/F_4 — +VDDG_NB
R558 *10K/F_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780
RX780
S-CD1 — R810 *3K_4
Reserved only

RX780 -->NC / RS780 --- ADD

+3V — L35 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB — C340 2.2U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V — BLM18PG181SN1D(180,1.5A)_6 L82 — +1.1V_PLLVDD — C842 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V — L33 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18 — C405 10U/6.3V_8, C333 2.2U/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V — R107 0_6 — +1.8V_AVDDDI_NB — C321 2.2U/6.3V_6
AVDDI-DAC Digital not applicable to RX780

BLM18PG181SN1D(180,1.5A)_6 L34 — +1.8V_AVDDQ_NB — C349 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V — BLM18PG181SN1D(180,1.5A)_6 L83 — +1.8V_VDDLTP18_NB — C841 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

BLM21PG221SN1D(220,100M,2A)_8 L85 — +1.8V_VDDLT_18_NB — C846 4.7U/6.3V_6, C838 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

+1.8V — L32 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDA18PCIEPLL (20mils width) — C358 2.2U/6.3V_6
VDDA18PCIEPLL -PCIE PLL

+1.8V — L31 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDA18HTPLL (20mils width) — C356 2.2U/6.3V_6
VDDA18HTPLL -HT LINK PLL

RS780 Q37 BSS138_NL/SOT23
+1.8V — R556 4.7K_4 — +VDDG_NB
3,12 CPU_LDT_STOP# — NB_LDT_STOP#
R555 *0_4
RX780

RS780 Q38 BSS138_NL/SOT23
+1.8V — R557 4.7K_4 — +VDDG_NB
3 CPU_LDT_REQ# — R568 0_4 — NB_ALLOW_LDTSTOP
12 ALLOW_LDTSTOP — R564 *0_4
RX780

RX780 +1.8V — R566 *0_6 — +VDDG_NB
RS780 +3V — R565 0_6

+3V — L84 *BLM21PG221SN1D(220,100M,2A)_8 — +3V_VDLT33_NB — C844 *2.2U/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

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Quanta Computer Inc.
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PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V 2A for RS780M

+1.1V 0.6A L72 BLM21PG221SN1D(220,100M,2A)_8 +1.1V_VDDHT

C770 4.7U/6.3V_6, C274 0.1U/10V_4, C313 0.1U/10V_4, C280 0.1U/10V_4

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A L81 BLM21PG221SN1D(220,100M,2A)_8 +1.1V_VDDHTRX

C847 4.7U/6.3V_6, C323 0.1U/10V_4, C843 0.1U/10V_4, C839 0.1U/10V_4

+1.2V 2A for RS780M+SB700

+1.2V L12 BLM21PG221SN1D(220,100M,2A)_8 0.5A +1.2V_VDDHTTX

+1.35V L13 BLM21PG221SN1D(220,100M,2A)_8

C124 4.7U/6.3V_6, C195 0.1U/10V_4, C194 0.1U/10V_4, C249 0.1U/10V_4, C199 0.1U/10V_4

+1.35V for A1-1 chip bug , A1-2 can remove

VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.8V 1A for RS780M+SB700

+1.8V L22 BLM21PG221SN1D(220,100M,2A)_8 600mA +1.8V_VDDA18PCIE

C188 4.7U/6.3V_6, C175 4.7U/6.3V_6, C258 0.1U/10V_4, C209 0.1U/10V_4, C302 0.1U/10V_4, C234 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V R122 0_6 0.005A C317 1U/10V_4 +1.8V_VDDG18_NB

+1.8V R499 0_6 0.005A C769 1U/10V_4 +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

U32E

PART 5/6

POWER

RS780(RX780)

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE 0.7A R542 0_8 +1.1V

C275 0.1U/10V_4, C337 0.1U/10V_4, C318 1U/10V_4, C328 1U/10V_4, C845 4.7U/6.3V_6

VDDC - Core Logic power

7A +1.1V_DYN

C251 0.1U/10V_4, C292 0.1U/10V_4, C297 0.1U/10V_4, C303 0.1U/10V_4, C59 10U/6.3V_8

C281 0.1U/10V_4, C278 0.1U/10V_4, C250 0.1U/10V_4, C60 10U/6.3V_8

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+1.8V_VDD_MEM 1.8V(0.15A) L23 BLM21PG221SN1D(220,100M,2A)_8 +1.8V

C192 0.1U/10V_4, C179 0.1U/10V_4, C172 0.1U/10V_4, C216 0.1U/10V_4, C153 4.7U/6.3V_6

+3V_VDDG33 R123 RS780 0_6 3.3V(0.03A) +3V

C336 0.1U/10V_4, C329 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

NB5/RD5

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Quanta Computer Inc.

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PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

SB700
Part 1 of 5
U37A

PCIE_PVDD-- PCIE PLL POWER

Del R639, R640, R641, R642 on PV

change D21, D20 type for PV

All the PCI bus has build-in Pull-UP/Down resistors

100MHZ

SI-2 mofified for satify -- remove R560 , add R796 ,R797

SI-2 Modified-- for power leakage issue

Del R783 for TP on PV

SI-2 Modified-- Add GPIO pin for control D3E wake up (need low 1ms for Jmicron request)

R589 change to 10 ohm on PV

If CPU have pull Hi ,this pin should be not need

PV-1 Modified -- change to pull hi to 3VS5 for power leakage issue

SI-1 Modified - for EMI

SI-2 modified -- for EMI suggestion

SI-2 Modified--reserve

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

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NC only ,Can't be install

+3VSUS
R297 *2.2K_4 SB_TEST0
R240 *2.2K_4 SB_TEST1
R287 *2.2K_4 SB_TEST2

+3VSUS
R289 *10K/F_4 SWI#

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R245 2.2K_4 PCLK_SMB
R253 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3VS5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R648 *2.2K_4 SB_SMBCLK1
R649 *2.2K_4 SB_SMBDATA1

remove pull hi (chip internal have pull hi)

+3VS5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R222 *2.2K_4 SB_SCLK2
R227 *2.2K_4 SB_SDATA2

+3V
R276 4.7K_4 SUS_STAT#
G4
2 1 SYS_RST#
*SHORT_ PAD1

+3VS5
R763 2.2K_4 DNBSWON#

U37D
SB700
Part 4 of 5

33 NEWCARD_DETECT
T211
T99
35 SUSB#
35 SUSC#
35 DNBSWON#
16 SB_PWRGD_IN
10 SUS_STAT#
R271 *0_4
R191 *0_4
R233 *0_4
NEWCARD_DETECT
RI#
SLP_S2
SUSB#
SUSC#
DNBSWON#
SB_PWRGD_IN
SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0

SI-2 modified add D3E function

35 GATEA20
35 RCIN#
35 SCI#
35 KBSMI#
T109
GATEA20
RCIN#
SCI#
KBSMI#
GEVENT5#
SYS_RST#
PCIE_WAKE#
31,33,36 PCIE_WAKE#
35 SWI#
3 CPU_THERMTRIP#
16 WD_PWRGD
R211 *0_4
R786 0_4
SWI#
SB_THERMTRIP#
WD_PWRGD

35 RSMRST#
R284 *0_4 RSMRST#

SI-2 modified -- Change lan disable control from SB to EC SB reserve

T63
T194
31,35 LAN_DISABLE#
R217 *0_4
SATA_IS1
LAN_DISABLE# SB
SB_NWD_CLK_REQ#
T222

27,28 ACZ_SPKR
2,6,7,28,36 PCLK_SMB
2,6,7,28,36 PDAT_SMB
R302 *0_4
ACZ_SPKR
PCLK_SMB
PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1

T69
T75
35 PM_BATLOW#
PM_BATLOW#
SES_INT
T72
26 D3E_SCI#

D3E_SCI# from Gevent5# change to Gevent7# on PV

SI-2 modified Del D35

3,7 CPU_MEMHOT#
5 PM_THERM#
+3VS5
R275 *0_4
R279 *10K/F_4
CPU_MEMHOT# IN
SMBALERT# 1
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_R
ACZ_SDIN1_R
T98
T209
16 ACZ_RST#
ACZ_SYNC
ACZ_RST#

HD audio interface is 3.385 voltage

+3VS5
R592 22K_4 HDD_AUX_RST#

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

USB 1.1
USB 2.0

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

SB700

CLK_48M_USB
CLK_48M_USB 2
USB_RCOMP_SB
R267 11.8K/F_6

C554 *2.2P/50V_4

for EMI & del R268 change 2.2P

T101
T199
T91
T93

USBP11+ 36
USBP11- 36
TV Min-Card

USBP10+ 36
USBP10- 36
WLAN Min-Card

USBP9+ 30
USBP9- 30
USB Connector

USBP8+ 30
USBP8- 30
USB Connector

USBP7+ 33
USBP7- 33
NEW CARD

USBP6+ 30
USBP6- 30
FINGERPRINT

USBP5+ 30
USBP5- 30
BLUETOOTH

USBP4+ 37
USBP4- 37
Docking

USBP3+
USBP3-
USB card reader or Touch screen

USBP2+ 30
USBP2- 30
Carama USB

USBP1+ 30
USBP1- 30
E-SATA and USB Connector

USBP0+ 30
USBP0- 30
USB Connector

SB_SCLK2
SB_SDATA2
SB_SCLK3
T64
SB_SDATA3
T70
SB_GPIO16
SB_GPIO17
SB_GPIO16 16
SB_GPIO17 16
SPI/LPC define

+3VS5
R764 2K/04
+3V
33,36 SCLK_WLAN
PCLK_SMB
Q66
2N7002EPT

+3VS5
R765 2K/04
+3V
33,36 SDATA_WLAN
PDAT_SMB
2N7002EPT Q67

To Azalia

ACZ_SDOUT R644 33_4 ACZ_SDOUT_AUDIO 27
C908 *10P/50V_4
ACZ_SYNC R290 33_4 ACZ_SYNC_AUDIO 27
C569 *10P/50V_4
ACZ_BCLK R646 33_4 BIT_CLK_AUDIO 27
C910 10P/50V_4
ACZ_RST# R296 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0_R R295 0_4 ACZ_SDIN0 27

SI-2 Modified --for EMI suggestion

To Modem Board

ACZ_SDOUT R645 33_4 ACZ_SDOUT_AUDIO_MDC 29
C909 *10P/50V_4
ACZ_SYNC R292 33_4 ACZ_SYNC_AUDIO_MDC 29
C577 *10P/50V_4
ACZ_BCLK R647 33_4 BIT_CLK_AUDIO_MDC 29
C911 10P/50V_4
ACZ_RST# R293 33_4 ACZ_RST#_AUDIO_MDC 29
ACZ_SDIN1_R R286 0_4 ACZ_SDIN1 29

SB JTAG

CN16
+3VSUS
C462 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

SI-2 Modified -- discrete remove RP56

CLOSE TO SB
USBP3-
USBP3+
RP50 *0_4P2R_4
USBP6_CR- 25
USBP6_CR+ 25
UMA

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size Custom
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SATA PORT 0,1,2,3 can support AHCI mode

SATA1

SATA ODD

E-SATA

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

U37B

SB700

Part 2 of 5

SERIAL ATA

SATA_TX0P / SATA_TX0N — AD9 / AE9
SATA_RX0N / SATA_RX0P — AB10 / AC10
SATA_TX1P / SATA_TX1N — AE10 / AD10
SATA_RX1N / SATA_RX1P — AD11 / AE11
SATA_TX2P / SATA_TX2N — AB12 / AC12
SATA_RX2N / SATA_RX2P — AE12 / AD12
SATA_TX3P / SATA_TX3N — AD13 / AE13
SATA_RX3N / SATA_RX3P — AB14 / AC14
SATA_TX4P / SATA_TX4N — AE14 / AD14
SATA_RX4N / SATA_RX4P — AD15 / AE15
SATA_TX5P / SATA_TX5N — AB16 / AC16
SATA_RX5N / SATA_RX5P — AE16 / AD16
SATA_CAL — V12
SATA_X1 — Y12
SATA_X2 — AA12
SATA_ACT#/GPIO67 — W11

SATA PWR

PLLVDD_SATA — AA11
XTLVDD_SATA — W12

ATA 66/100/133

IDE_IORDY AA24 — T231
IDE_IRQ AA25 — T232
IDE_A0 Y22 — T233
IDE_A1 AB23 — T234
IDE_A2 Y23 — T235
IDE_DACK# AB24 — T236
IDE_DRQ AD25 — T237
IDE_IOR# AC25 — T238
IDE_IOW# AC24 — T239
IDE_CS1# Y25 — T240
IDE_CS3# Y24 — T241

IDE_D0/GPIO15 AD24 — T242
IDE_D1/GPIO16 AD23 — T243
IDE_D2/GPIO17 AE22 — T244
IDE_D3/GPIO18 AC22 — T245
IDE_D4/GPIO19 AD21 — T246
IDE_D5/GPIO20 AE20 — T247
IDE_D6/GPIO21 AB20 — T248
IDE_D7/GPIO22 AD19 — T249
IDE_D8/GPIO23 AE19 — T250
IDE_D9/GPIO24 AC20 — T251
IDE_D10/GPIO25 AD20 — T252
IDE_D11/GPIO26 AE21 — T253
IDE_D12/GPIO27 AB22 — T254
IDE_D13/GPIO28 AD22 — T255
IDE_D14/GPIO29 AE23 — T256
IDE_D15/GPIO30 AC23 — T257

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

SPI_DI/GPIO12 G6 — T100
SPI_DO/GPIO11 D2 — T219
SPI_CLK/GPIO47 D1 — T218
SPI_HOLD#/GPIO31 E4 — T111
SPI_CS#/GPIO32 E3 — T220

LAN_RST#/GPIO13 U15 — R265 0_4 — BT_OFF# 30
ROM_RST#/GPIO14 J1 — ROM_RST# — T215

HW MONITOR

FANOUT0/GPIO3 M8 — SB_FANOUT0 — T96
FANOUT1/GPIO48 M5 — SB_FANOUT1 — T97
FANOUT2/GPIO49 M7 — CHIPSET_PCIE_SLOW_SB# 2

FANIN0/GPIO50 P5 — SB_FANTACH0 — T104
FANIN1/GPIO51 P8 — SB_FANTACH1 — T92
FANIN2/GPIO52 R8 — PORT_80_PWR_DWN — T95

TEMP_COMM C6 — TEMP_COMM — T208
TEMPIN0/GPIO61 B6 — TEMPIN0 — T202
TEMPIN1/GPIO62 A6 — TEMPIN1 — T203
TEMPIN2/GPIO63 A5 — MB_THRMDA_SB — T207
TEMPIN3/TALERT#/GPIO64 B5 — T259

VIN0/GPIO53 A4 — R216 0_4 — ACCLED_EN 29
VIN1/GPIO54 B4 — BT_COMBO_EN# 36
VIN2/GPIO55 C4
VIN3/GPIO56 D4 — BOARD_ID0
VIN4/GPIO57 D5 — BOARD_ID1
VIN5/GPIO58 D6 — BOARD_ID2
VIN6/GPIO59 A7 — BOARD_ID3
VIN7/GPIO60 B7 — BOARD_ID4

Del R220 for TP on PV

Del WAN off# and R597 on PV

AVDD F6 — 5mA — +3V_VDD_HWM — L52 0_6 — +3VS5
AVSS G7

C571 *0.1U/10V_4
C572 *2.2U/6.3V_6

AVDD--H/W monitor Analog power

SI-2 modified -- for fix +3V power leakage in S5 mode

SATA PORT 4,5 are only support IDE mode

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE :
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

R361 1K/F_4 — R264 — SATA_RBIAS_PN — V12

PLVDD_SATA-- SATA PLL POWER

+3V — R382 10K/F_4 — +1.2V_PLLVDD_SATA

XTLVDD_SATA-- SATA crystal power

C534 27P/50V_4 — Y4 25MHZ — R262 10M_6 — C517 27P/50V_4 — SATA_X1 / SATA_X2

SB_SATA_LED# — W11

SI-2 modified -- SB internal pull Hi to 3VS5 , modified to same power rail with SB

+3VS5 — R221 10K/F_4 BOARD_ID0 — R229 *10K/F_4
R247 *10K/F_4 BOARD_ID1 — R248 *10K/F_4
R225 *10K/F_4 BOARD_ID2 — R228 *10K/F_4
R230 *10K/F_4 BOARD_ID3 — R242 *10K/F_4
R596 *10K/F_4 BOARD_ID4 — R600 *10K/F_4

+3V — C655 0.1U/10V_4 — U20 TC7SH08FU — 29 SATA_LED# — SB_SATA_LED#

SI-2 modified for SATA LED fail issue

+1.2V — (1.2V @ 60mA) — L47 BLM18PG181SN1D(180,1.5A)_6 — +1.2V_PLLVDD_SATA — 77mA
C524 1U/10V_4 — C550 0.1U/10V_4

+3V — (3.3V @ 1.2mA) — L46 BLM18PG181SN1D(180,1.5A)_6 — +3V_XTLVDD_SATA — 1mA
C539 1U/10V_4

Place near ball

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Del R285 for TP on PV

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

POWER

SB700 Part 3 of 5

U37C

VDDQ--3.3V I/O power — 0.8A

+3V → C576 100U/6.3V_3528 → C557 10U/6.3V_8, C560 1U/10V_4, C573 1U/10V_4, C565 1U/10V_4, C547 1U/10V_4, C553 1U/10V_4, C574 1U/10V_4

VDDQ_1 L9, VDDQ_2 M9, VDDQ_3 T15, VDDQ_4 U9, VDDQ_5 U16, VDDQ_6 U17, VDDQ_7 V8, VDDQ_8 W7, VDDQ_9 Y6, VDDQ_10 AA4, VDDQ_11 AB5, VDDQ_12 AB21 — PCI/GPIO I/O

VDD-- S/B CORE power — 604mA

+1.2V_VCC_SB_R → R590 *0_8 → +1.2V_S5 (For SB700 issue(6/22) A1-1 chip bug use A1-2 chip can remove)

VDD_1 L15, VDD_2 M12, VDD_3 M14, VDD_4 N13, VDD_5 P12, VDD_6 P14, VDD_7 R11, VDD_8 R15, VDD_9 T16 — CORE S0

C533 1U/10V_4, C545 1U/10V_4, C538 1U/10V_4, C532 1U/10V_4, C467 10U/6.3V_8

R198 0_8 → +1.2V

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power — 0.45A

+3V → R226 0_8; +1.8V → R751 *0_8 → +VDD33_18

C486 10U/6.3V_8, C501 1U/10V_4, C487 1U/10V_4, C497 1U/10V_4, C488 1U/10V_4

VDD33_18_1 Y20, VDD33_18_2 AA21, VDD33_18_3 AA22, VDD33_18_4 AE25 — IDE/FLSH I/O

CKVDD_1.2V-- Internal clock Generator I/O power — 286mA

+1.2V_CKVDD

CKVDD_1.2V_1 L21, CKVDD_1.2V_2 L22, CKVDD_1.2V_3 L24, CKVDD_1.2V_4 L25 — CLKGEN I/O

C505 2.2U/6.3V_6, C489 0.1U/50V_6, C475 0.1U/50V_6, C478 2.2U/6.3V_6

L43 BLM18PG181SN1D(180,1.5A)_6 → +1.2V

PCIE_VDDR--PCIE I/O power — 844mA

+1.2V_PCIE_VDDR; +1.2V → L89 BLM18PG181SN1D(180,1.5A)_6

C477 10U/6.3V_8, C502 1U/10V_4, C484 1U/10V_4, C504 1U/10V_4, C492 1U/10V_4, C483 1U/10V_4

PCIE_VDDR_1 P18, PCIE_VDDR_2 P19, PCIE_VDDR_3 P20, PCIE_VDDR_4 P21, PCIE_VDDR_5 R22, PCIE_VDDR_6 R24, PCIE_VDDR_7 R25 — A-LINK I/O

S5_3.3--3.3v standby power

+3VALW_R → 0.01A → R604 0_6 (Change to 0603) → +3VS5

C875 0.1U/10V_4, C570 0.1U/10V_4, C876 10U/6.3V_8

S5_3.3V_1 A17, S5_3.3V_2 A24, S5_3.3V_3 B17, S5_3.3V_4 J4, S5_3.3V_5 J5, S5_3.3V_6 L1, S5_3.3V_7 L2 — 3.3V_S5 I/O

S5_1.2V--1.2V standby power — 0.22A

S5_1.2V_1 G2, S5_1.2V_2 G4 — CORE S5

C903 0.1U/10V_4, C901 0.1U/10V_4 → +1.2V_S5

Del R661 for TP on PV

AVDD_SATA--SATA phy power — 0.2A

+1.2V_AVDD_SATA; +1.2V → L92 BLM18PG181SN1D(180,1.5A)_6

C888 10U/6.3V_8, C880 0.1U/10V_4, C884 0.1U/10V_4, C883 1U/10V_4, C881 1U/10V_4

AVDD_SATA_1 AA14, AVDD_SATA_4 AB18, AVDD_SATA_2 AA15, AVDD_SATA_3 AA17, AVDD_SATA_5 AC18, AVDD_SATA_6 AD17, AVDD_SATA_7 AE17 — SATA I/O

0.2A

USB_PHY_1.2V_1 A10, USB_PHY_1.2V_2 B10 — CORE S5 → +1.2V_USB_PHY_R

For support USB wakeup-->3V_S5
AVDDTX--USB Phy Analog I/O power — 0.2A

+3V_AVDD_USB; +3VS5 → L91 BLM18PG181SN1D(180,1.5A)_6

C889 10U/6.3V_8, C882 10U/6.3V_8, C878 0.1U/10V_4, C886 0.1U/10V_4

C528 1U/10V_4, C537 1U/10V_4, C885 1U/10V_4, C511 0.1U/10V_4, C510 0.1U/10V_4, C879 0.1U/10V_4, C536 0.1U/10V_4

AVDDTX_0 A16, AVDDTX_1 B16, AVDDTX_2 C16, AVDDTX_3 D16, AVDDTX_4 D17, AVDDTX_5 E17, AVDDRX_0 F15, AVDDRX_1 F17, AVDDRX_2 F18, AVDDRX_3 G15, AVDDRX_4 G17, AVDDRX_5 G18 — USB I/O

V5_VREF--PCI 5V TOLERANCE

V5_VREF AE7 ← +5V_VREF — 4mA → R621 1K/F_4 → +5V

AVDDCK_3.3V J16 ← +3V_AVDDCK — 7mA

AVDDCK_1.2V K17 ← +1.2V_AVDDCK — 44mA

AVDDC E9 ← +3V_AVDDC — 16mA

C898 1U/10V_4

D36 CH501H-40PT → +3V

PLL

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R616 0_6 → +1.2V_USB_PHY_R

C890 0.1U/10V_4, C891 0.1U/10V_4, C892 10U/6.3V_8

AVDDC--USB Analog PLL power

+3VS5 → L50 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDC

C546 0.1U/10V_4, C540 10U/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L45 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDDCK

C509 2.2U/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L48 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDCK

C516 2.2U/6.3V_6

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U37E

AVSS_SATA_1 T10, AVSS_SATA_2 U10, AVSS_SATA_3 U11, AVSS_SATA_4 U12, AVSS_SATA_5 V11, AVSS_SATA_6 V14, AVSS_SATA_7 W9, AVSS_SATA_8 Y9, AVSS_SATA_9 Y11, AVSS_SATA_10 Y14, AVSS_SATA_11 Y17, AVSS_SATA_12 AA9, AVSS_SATA_13 AB9, AVSS_SATA_14 AB11, AVSS_SATA_15 AB13, AVSS_SATA_16 AB15, AVSS_SATA_17 AB17, AVSS_SATA_18 AC8, AVSS_SATA_19 AD8, AVSS_SATA_20 AE8

AVSS_USB_1 A15, AVSS_USB_2 B15, AVSS_USB_3 C14, AVSS_USB_4 D8, AVSS_USB_5 D9, AVSS_USB_6 D11, AVSS_USB_7 D13, AVSS_USB_8 D14, AVSS_USB_9 D15, AVSS_USB_10 E15, AVSS_USB_11 F12, AVSS_USB_12 F14, AVSS_USB_13 G9, AVSS_USB_14 H9, AVSS_USB_15 H17, AVSS_USB_16 J9, AVSS_USB_17 J11, AVSS_USB_18 J12, AVSS_USB_19 J14, AVSS_USB_20 J15, AVSS_USB_21 K10, AVSS_USB_22 K12, AVSS_USB_23 K14, AVSS_USB_24 K15

PCIE_CK_VSS_1 H18, PCIE_CK_VSS_2 J17, PCIE_CK_VSS_3 J22, PCIE_CK_VSS_4 K25, PCIE_CK_VSS_5 M16, PCIE_CK_VSS_6 M17, PCIE_CK_VSS_7 M21, PCIE_CK_VSS_8 P16

AVSSC F9, AVSSCK L17

VSS_1 A2, VSS_2 A25, VSS_3 B1, VSS_4 D7, VSS_5 F20, VSS_6 G19, VSS_7 H8, VSS_8 K9, VSS_9 K11, VSS_10 K16, VSS_11 L4, VSS_12 L7, VSS_13 L10, VSS_14 L11, VSS_15 L12, VSS_16 L14, VSS_17 L16, VSS_18 M6, VSS_19 M10, VSS_20 M11, VSS_21 M13, VSS_22 M15, VSS_23 N4, VSS_24 N12, VSS_25 N14, VSS_26 P6, VSS_27 P9, VSS_28 P10, VSS_29 P11, VSS_30 P13, VSS_31 P15, VSS_32 R1, VSS_33 R2, VSS_34 R4, VSS_35 R9, VSS_36 R10, VSS_37 R12, VSS_38 R14, VSS_39 T11, VSS_40 T12, VSS_41 T14, VSS_42 U4, VSS_43 U14, VSS_44 V6, VSS_45 Y21, VSS_46 AB1, VSS_47 AB19, VSS_48 AB25, VSS_49 AE1, VSS_50 AE24

PCIE_CK_VSS_9 P23, PCIE_CK_VSS_10 R16, PCIE_CK_VSS_11 R19, PCIE_CK_VSS_12 T17, PCIE_CK_VSS_13 U18, PCIE_CK_VSS_14 U20, PCIE_CK_VSS_15 V18, PCIE_CK_VSS_16 V20, PCIE_CK_VSS_17 V21, PCIE_CK_VSS_18 W19, PCIE_CK_VSS_19 W22, PCIE_CK_VSS_20 W24, PCIE_CK_VSS_21 W25

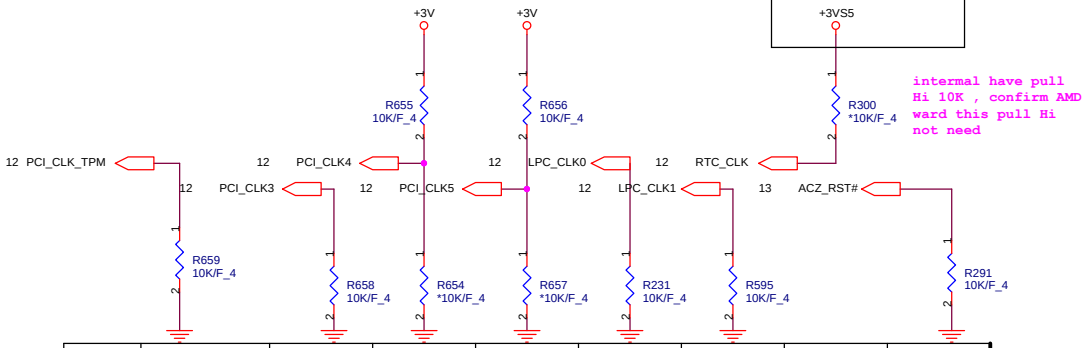
GROUND

PROJECT : QT8	
Quanta Computer Inc.	
Size: Custom	Document Number: SB700-PWR/DECOUPLING 4/4
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 15 of 45
NB5/RD5	

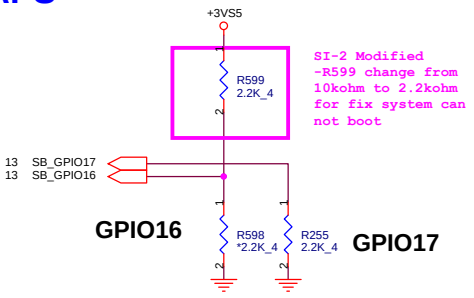
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



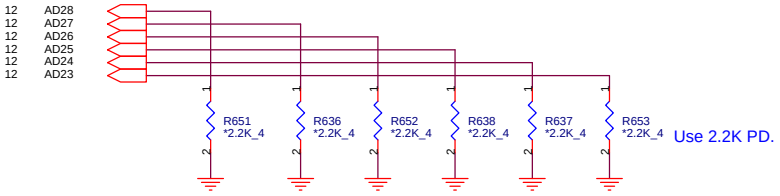
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

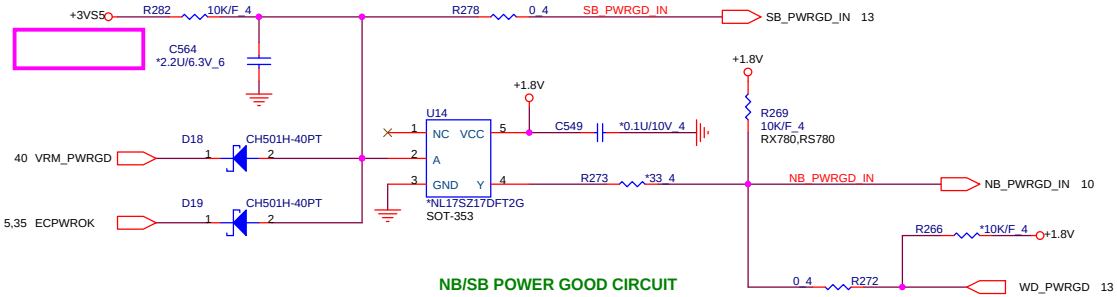


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove +3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

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IC CTRL(632P) 216-0707001-00(BGA)
VGA P/N : AJ070700T00

2.5Gb/s bit rate

PART 1 OF 6

PCI-EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AC30	PCIE_RX0P	PCIE_TX0P	AA28	C_PEG_RXP0	C163	0.1U/10V_4	PEG_RX0	9
9	PEG_TX#0	PEG_TX#0	AC31	PCIE_RX0N	PCIE_TX0N	AA27	C_PEG_RXN0	C156	0.1U/10V_4	PEG_RX#0	9
9	PEG_TX1	PEG_TX1	AC29	PCIE_RX1P	PCIE_TX1P	AA25	C_PEG_RXP1	C167	0.1U/10V_4	PEG_RX1	9
9	PEG_TX#1	PEG_TX#1	AB29	PCIE_RX1N	PCIE_TX1N	AA24	C_PEG_RXN1	C170	0.1U/10V_4	PEG_RX#1	9
9	PEG_TX2	PEG_TX2	AB31	PCIE_RX2P	PCIE_TX2P	Y28	C_PEG_RXP2	C180	0.1U/10V_4	PEG_RX2	9
9	PEG_TX#2	PEG_TX#2	AB30	PCIE_RX2N	PCIE_TX2N	Y27	C_PEG_RXN2	C196	0.1U/10V_4	PEG_RX#2	9
9	PEG_TX3	PEG_TX3	AA31	PCIE_RX3P	PCIE_TX3P	Y25	C_PEG_RXP3	C164	0.1U/10V_4	PEG_RX3	9
9	PEG_TX#3	PEG_TX#3	AA30	PCIE_RX3N	PCIE_TX3N	Y24	C_PEG_RXN3	C157	0.1U/10V_4	PEG_RX#3	9
9	PEG_TX4	PEG_TX4	W30	PCIE_RX4P	PCIE_TX4P	V28	C_PEG_RXP4	C218	0.1U/10V_4	PEG_RX4	9
9	PEG_TX#4	PEG_TX#4	W31	PCIE_RX4N	PCIE_TX4N	V27	C_PEG_RXN4	C204	0.1U/10V_4	PEG_RX#4	9
9	PEG_TX5	PEG_TX5	W29	PCIE_RX5P	PCIE_TX5P	V25	C_PEG_RXP5	C203	0.1U/10V_4	PEG_RX5	9
9	PEG_TX#5	PEG_TX#5	V29	PCIE_RX5N	PCIE_TX5N	V24	C_PEG_RXN5	C187	0.1U/10V_4	PEG_RX#5	9
9	PEG_TX6	PEG_TX6	V31	PCIE_RX6P	PCIE_TX6P	T28	C_PEG_RXP6	C220	0.1U/10V_4	PEG_RX6	9
9	PEG_TX#6	PEG_TX#6	V30	PCIE_RX6N	PCIE_TX6N	T27	C_PEG_RXN6	C224	0.1U/10V_4	PEG_RX#6	9
9	PEG_TX7	PEG_TX7	U31	PCIE_RX7P	PCIE_TX7P	T25	C_PEG_RXP7	C243	0.1U/10V_4	PEG_RX7	9
9	PEG_TX#7	PEG_TX#7	U30	PCIE_RX7N	PCIE_TX7N	T24	C_PEG_RXN7	C252	0.1U/10V_4	PEG_RX#7	9
9	PEG_TX8	PEG_TX8	P30	PCIE_RX8P	PCIE_TX8P	P28	C_PEG_RXP8	C276	0.1U/10V_4	PEG_RX8	9
9	PEG_TX#8	PEG_TX#8	P31	PCIE_RX8N	PCIE_TX8N	P27	C_PEG_RXN8	C268	0.1U/10V_4	PEG_RX#8	9
9	PEG_TX9	PEG_TX9	P29	PCIE_RX9P	PCIE_TX9P	P25	C_PEG_RXP9	C259	0.1U/10V_4	PEG_RX9	9
9	PEG_TX#9	PEG_TX#9	N29	PCIE_RX9N	PCIE_TX9N	P24	C_PEG_RXN9	C246	0.1U/10V_4	PEG_RX#9	9
9	PEG_TX10	PEG_TX10	N31	PCIE_RX10P	PCIE_TX10P	M28	C_PEG_RXP10	C289	0.1U/10V_4	PEG_RX10	9
9	PEG_TX#10	PEG_TX#10	N30	PCIE_RX10N	PCIE_TX10N	M27	C_PEG_RXN10	C277	0.1U/10V_4	PEG_RX#10	9
9	PEG_TX11	PEG_TX11	M31	PCIE_RX11P	PCIE_TX11P	M25	C_PEG_RXP11	C290	0.1U/10V_4	PEG_RX11	9
9	PEG_TX#11	PEG_TX#11	M30	PCIE_RX11N	PCIE_TX11N	M24	C_PEG_RXN11	C296	0.1U/10V_4	PEG_RX#11	9
9	PEG_TX12	PEG_TX12	K30	PCIE_RX12P	PCIE_TX12P	L28	C_PEG_RXP12	C288	0.1U/10V_4	PEG_RX12	9
9	PEG_TX#12	PEG_TX#12	K31	PCIE_RX12N	PCIE_TX12N	L27	C_PEG_RXN12	C295	0.1U/10V_4	PEG_RX#12	9
9	PEG_TX13	PEG_TX13	K29	PCIE_RX13P	PCIE_TX13P	L25	C_PEG_RXP13	C330	0.1U/10V_4	PEG_RX13	9
9	PEG_TX#13	PEG_TX#13	J29	PCIE_RX13N	PCIE_TX13N	L24	C_PEG_RXN13	C324	0.1U/10V_4	PEG_RX#13	9
9	PEG_TX14	PEG_TX14	J31	PCIE_RX14P	PCIE_TX14P	J28	C_PEG_RXP14	C325	0.1U/10V_4	PEG_RX14	9
9	PEG_TX#14	PEG_TX#14	J30	PCIE_RX14N	PCIE_TX14N	J27	C_PEG_RXN14	C331	0.1U/10V_4	PEG_RX#14	9
9	PEG_TX15	PEG_TX15	H31	PCIE_RX15P	PCIE_TX15P	G28	C_PEG_RXP15	C304	0.1U/10V_4	PEG_RX15	9
9	PEG_TX#15	PEG_TX#15	H30	PCIE_RX15N	PCIE_TX15N	G27	C_PEG_RXN15	C316	0.1U/10V_4	PEG_RX#15	9

Clock

2	EXT_GFX_CLKP	EXT_GFX_CLKP	AD29
2	EXT_GFX_CLKN	EXT_GFX_CLKN	AD30

PCIE_REFCLKP
PCIE_REFCLKN

100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing

SM BUS

NC_SMBCLK		AC28
NC_SMBDATA		AC27

12	PCIE_RST#	R71	0_4	AG25

PERSTB

Calibration

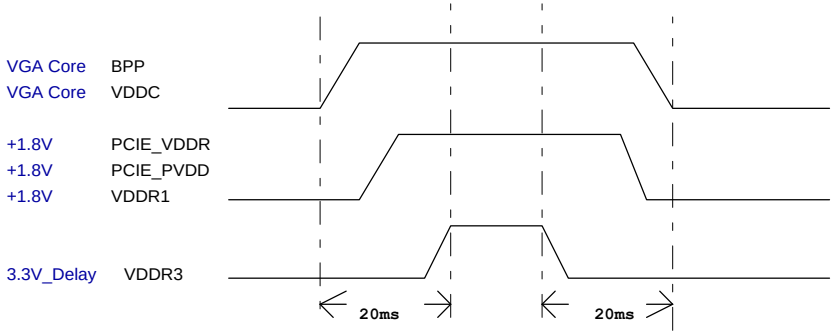
PCIE_CALRN	AF25	M72_PCIE_CALRN	R74	2K/F_4	+1.1V_PCIE_VDDC	
PCIE_CALRP	AE25	M72_PCIE_CALRP	R70	1.27K/F_4		

1.27K for M82-S

NC_1	AE23	
NC_2	AH30	

M72-S/M82-S
U29A

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_PCIE_Interface	1A

NB5/RD5

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R100 1K/F_4 GPIO_24_JMODE — NA- M62S,M71S PD 1K- M72S

R522 10K/F_4 ROMCS# — GPIO22(ROMCS#) PD without external VBIOS ROM

R87 10K/F_4 BBEN — NA - M64/M62, M71 BBEN- M66 BBEN(10K PD)- M76

R95 10K/F_4 TEMP_FAIL — NA- M62S,M71S PU to 3.3V- M72S

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161B2F-20
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16-500MHZ	H5PS5162FFR-20L
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-HC20
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

U29B PART 2 OF 6 — INTEGRATED TMDS/DP PORT

TXCM_DPA0P / TXCP_DPA0N — TXC_HDMI_L- / TXC_HDMI_L+ — TXC_HDMI_L- 23, TXC_HDMI_L+ 23

TX0M_DPA1P / TX0P_DPA1N — TX0_HDMI_L- / TX0_HDMI_L+ — TX0_HDMI_L- 23, TX0_HDMI_L+ 23

TX1M_DPA2P / TX1P_DPA2N — TX1_HDMI_L- / TX1_HDMI_L+ — TX1_HDMI_L- 23, TX1_HDMI_L+ 23

TX2M_DPA3P / TX2P_DPA3N — TX2_HDMI_L- / TX2_HDMI_L+ — TX2_HDMI_L- 23, TX2_HDMI_L+ 23

Remove 180R SHUNT RESISTOR for M82-S from AMD Jackson confirm

DPA_PVDD / DPB_PVDD — +1.8V_TPVDD
DP/TMDS PLL Power (Link A)
DP/TMDS PLL Power (Link B)
1.8 V ± 3%

DPA_VDDR / DPB_VDDR — DPA_B_VDDR
DP/TMDS Transmitter Power (Link A)
DP/TMDS Transmitter Power (Link B)
1.1 V ± 3%

DVALID, PSYNC_NEW — 19 PSYNC

DVPCNTL_MVP_0, DVPCNTL_MVP_1, DVPCNTL_0, DVPCNTL_1, DVPCNTL_2, DVPCLK

DVPDATA_0 … DVPDATA_23 — EXT TMDS DVO

GPIO_0 … GPIO_28_TDO — GENERAL PURPOSE I/O

GEN_A, GEN_B, GEN_C, GEN_D_HPD4, GEN_E, VREFG

DPLL_PVDD, DPLL_PVSS, PCIE_PVDD, MPVDD, MPVSS, DPLL_VDDC — PLL & XTAL

XTALIN, XTALOUT

TESTEN, PLLTEST — TEST

TS_FDO — THERMAL — DPLUS, DMINUS

M72-S/M82-S

ENABLE HD AUDIO (M8X-M)

R488 *0_4 — VIP_3 — VIP_3 19

M82-S

R476 0_4 150 OHM — DPA_VSSR_2

TMDS_HPD — TMDS_HPD 10,23

R485 *100K/F_4, R463 150/F_4, R449 0_4 — CRT_R 10,24

R462 150/F_4, R448 0_4 — CRT_G 10,24

R461 150/F_4, R447 0_4 — CRT_B 10,24

Del R481, R482, R483, R68, R464, R486 for TP on PV

HSYNC_COM 10,19,24 — VSYNC_COM 10,19,24

R484 499/F_4 — RSET

+1.8V_A2VDD_Q — AVDD

AVDD
DAC1 Analog Power
Dedicated power for DAC1.
1.8 V ± 5%

VDD1DI
DAC1 Digital Power.
1.8 V ± 5%

A2VDD
DAC2 Analog Power.
3.3 V ± 5%

A2VDDQ
DAC2 Band Gap (clean) power supply.
1.8 V ± 5%

VDD2DI
DAC2 Digital Power.
1.8 V ± 5%

Del R470, R478, R450, R472, R471, R469, R451 for TP on PV

Del L25 for TP on PV

Del R84, R85, R466, R467 for TP on PV

EDIDCLK 10,23 / EDIDDATA 10,23

DDCDATA 10,24 / DDCCLK 10,24

VTHM_DAT / VTHM_CLK

DDC 3V tolerance
--DDC1,DDC2,SDA/SCL
DDC 5V tolerance
--DDC3,DDC4

HDMI_SDA 23 / HDMI_SCL 23

VGATHRM+ / VGATHRM-

Memory ID

R495 *10K/F_4 MEM_ID0
R496 *10K/F_4 MEM_ID1
R493 *10K/F_4 MEM_ID2
R492 *10K/F_4 MEM_ID3

GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5

R93 0_4 — EXT_LVDS_BLON — 10,23 LVDS_BLON

GPIO8, GPIO9, GPIO10, GPIO11, GPIO12, GPIO13, HDMI_HP2

R526 0_4 — OSC_SPREAD, VGA_ALERT — 42 GFX_CORE_CNTRL0, 2 OSC_SPREAD

HPD3 — TEMP_FAIL, PWRCNTL_1, BBEN, ROMCS#, GPIO_23_CLKREQb, GPIO_24_JMODE — 5 TEMP_FAIL, 42 GFX_CORE_CNTRL1, 20 BBEN

R99 0_4, R91 10K/F_4 — +3V

T36, T34, T35, T38

R75 499/F_4, R76 249/F_4 — 1.8V+R6043(249R)=1.8V/3=0.6V — GENERICC — +0.6V_M72_VREFG

R69 715/F_4

+1.8V_DPLL_PVDD, DPLL_PVSS, +1.8V_VPCIE_PVDD, +VGACORE_MPVDD, MPVSS, +1.1V_DPLL_VDDC, EVGA-XTALI, EVGA-XTALO

R67 1K/F_4

DPLL_PVDD
Phase Lock Loop Power
Dedicated analog power pin for display PLLs.
1.8 V ± 3%

PCIE_PVDD
PCI-E PLL power.
1.8 V ± 5%

MPVDD
Memory Phase Lock Loop Power
Same as VDDC

DPLL_VDDC
Phase Lock Loop Power
Dedicated digital power pin for display PLLs.
1.1 V ± 5%

BLM18PG181SN1D(180,1.5A)_6 — L17 — 1.8V(40mA) — C114 10U/6.3V_8, C147 0.1U/10V_4

L71 — 1.8V(40mA) — C743 10U/6.3V_8, C747 1U/10V_4, C746 0.1U/10V_4

L79 — VDDC(345mA) — C822 10U/6.3V_8, C824 1U/10V_4, C823 0.1U/10V_4

L18 — 1.1V(100mA) — C106 10U/6.3V_8, C169 1U/10V_4, C161 0.1U/10V_4

C741 *22P/50V_4, Y7 *27MHZ, R468 *10M_6, C735 *22P/50V_4 — CL=20PF — EVGA-XTALI, EVGA-XTALO — For Int Clk 27Mhz

Thermal Sensor

5,35 MBCLK2 — R524 0_4 — MBCLK2
5,35 MBDATA2 — R525 0_4 — MBDATA2
VTHM_CLK — R518 *0_4
VTHM_DAT — R519 *0_4
+3V_DELAY — R516 10K/F_4 — VGA_ALERT

U30 — SMCLK, SMDATA, -ALT, GND, VCC, DXP, DXN, -OVT — G781-1P8@EV

761-1_3V — R509 200/F_6 — +3V_DELAY
C790 0.1U/10V_4
VGATHRM+
C793 2200P/50V_4
VGATHRM-
-VGATHRM — R513 10K/F_4 — +3V_DELAY

w/s 10 / 10

I2C ADDRESS: 9AH

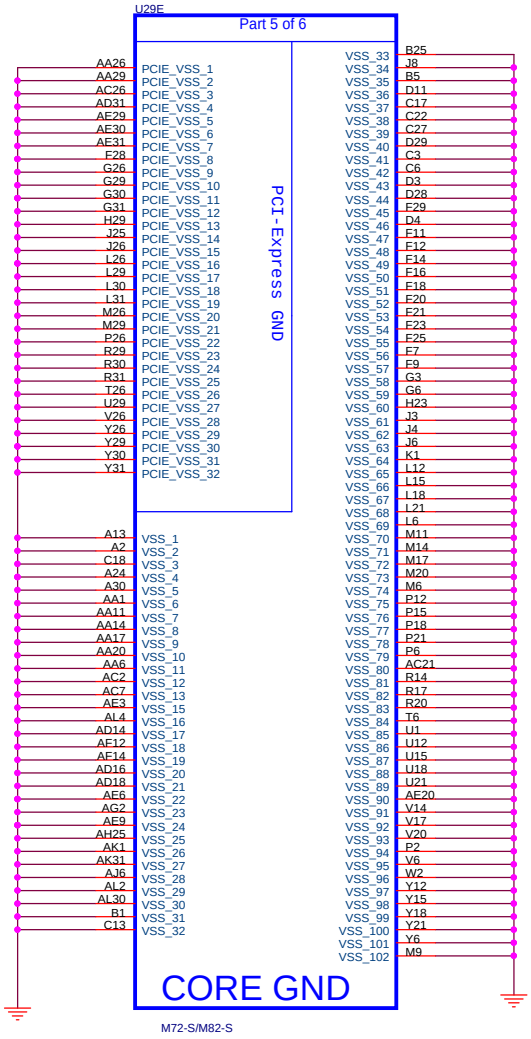
1.8V(65mA) — L16 — BLM18PG181SN1D(180,1.5A)_6 — C129 0.1U/10V_4, C168 1U/10V_4, C98 10U/6.3V_8

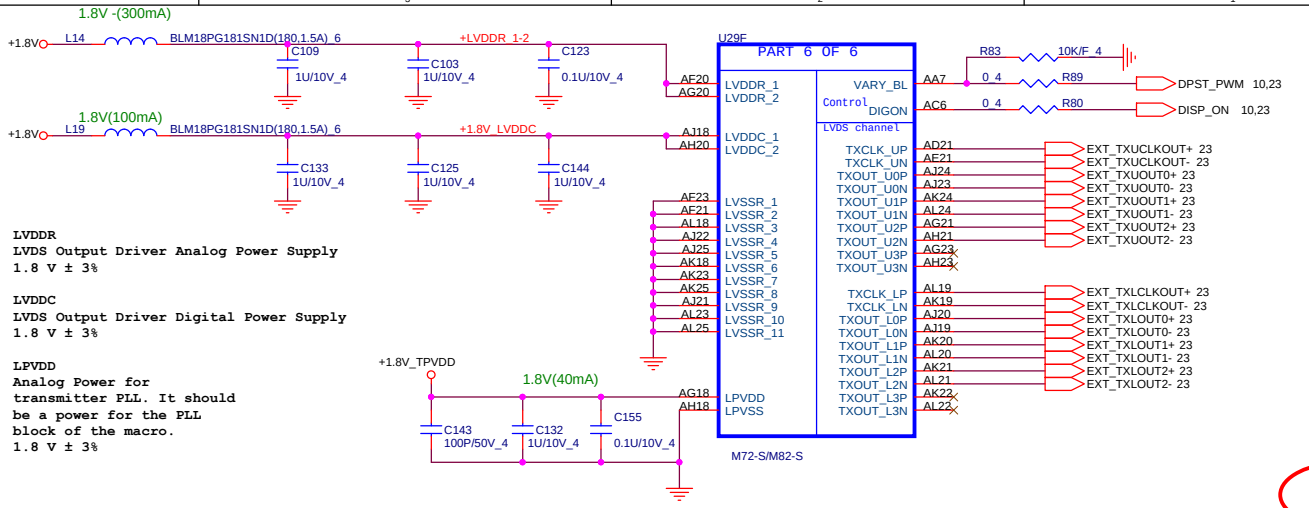
1.8V(20mA) — L24 — BLM18PG181SN1D(180,1.5A)_6 — C165 0.1U/10V_4, C182 1000P/50V_4, C145 10U/6.3V_8

1.8V(100mA) — L15 — BLM18PG181SN1D(180,1.5A)_6 — C110 0.1U/10V_4, C135 1U/10V_4, C97 10U/6.3V_8

1.8V(20mA) — L20 — BLM18PG181SN1D(180,1.5A)_6 — C113 0.1U/10V_4, C108 1000P/50V_4, C134 10U/6.3V_8

1.1V(S100,D200mA) — L70 — BLM18PG181SN1D(180,1.5A)_6 — C740 0.1U/10V_4, C742 1000P/50V_4, C737 10U/6.3V_8

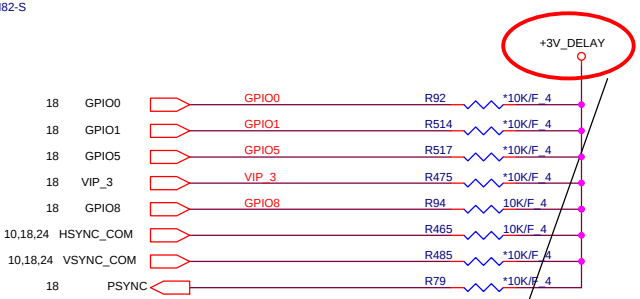




LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

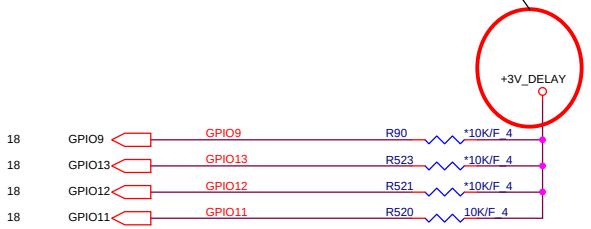
LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%



CONFIGURATION STRAPS

PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows eitherPCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1

SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_GND / LVDS/ Straps	1A

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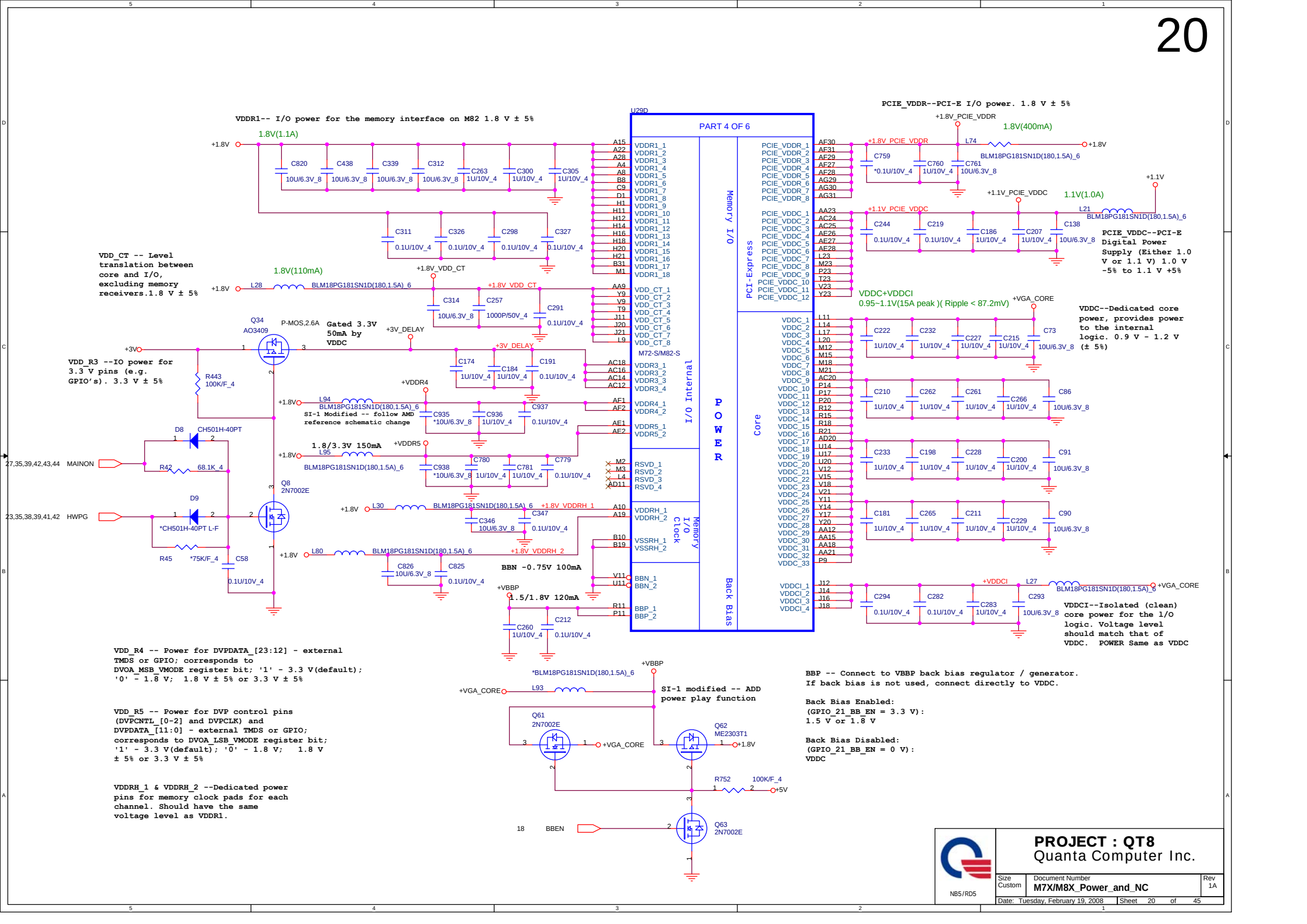
VDDR1-- I/O power for the memory interface on M82 1.8 V ± 5%
1.8V(1.1A)
+1.8V
C820 10U/6.3V_8
C438 10U/6.3V_8
C339 10U/6.3V_8
C312 10U/6.3V_8
C263 1U/10V_4
C300 1U/10V_4
C305 1U/10V_4
C311 0.1U/10V_4
C326 0.1U/10V_4
C298 0.1U/10V_4
C327 0.1U/10V_4
VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%
1.8V(110mA)
+1.8V
L28
BLM18PG181SN1D(180,1.5A)_6
+1.8V_VDD_CT
C314 10U/6.3V_8
C257 1000P/50V_4
C291 0.1U/10V_4
Q34
AO3409
P-MOS,2.6A
Gated 3.3V 50mA by VDDC
+3V_DELAY
+3V
VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%
R443 100K/F_4
C174 1U/10V_4
C184 1U/10V_4
C191 0.1U/10V_4
+VDDR4
L94
BLM18PG181SN1D(180,1.5A)_6
SI-1 Modified -- follow AMD reference schematic change
C935 *10U/6.3V_8
C936 1U/10V_4
C937 0.1U/10V_4
D8
CH501H-40PT
R42 68.1K_4
27,35,39,42,43,44 MAINON
1.8/3.3V 150mA
+VDDR5
L95
BLM18PG181SN1D(180,1.5A)_6
C938 *10U/6.3V_8
C780 1U/10V_4
C781 1U/10V_4
C779 0.1U/10V_4
D9
*CH501H-40PT L-F
R45 *75K/F_4
C58 0.1U/10V_4
Q8
2N7002E
23,35,38,39,41,42 HWPG
L30
BLM18PG181SN1D(180,1.5A)_6
+1.8V_VDDRH_1
C346 10U/6.3V_8
C347 0.1U/10V_4
L80
BLM18PG181SN1D(180,1.5A)_6
+1.8V_VDDRH_2
C826 10U/6.3V_8
C825 0.1U/10V_4
BBN -0.75V 100mA
+VBBP
1.5/1.8V 120mA
C260 1U/10V_4
C212 0.1U/10V_4
U29D
PART 4 OF 6
M72-S/M82-S
POWER
Memory I/O
PCI-Express
I/O Internal
Memory I/O Clock
Back Bias
Core
A15 VDDR1_1
A22 VDDR1_2
A28 VDDR1_3
A4 VDDR1_4
A8 VDDR1_5
B8 VDDR1_6
C9 VDDR1_7
D1 VDDR1_8
H1 VDDR1_9
H11 VDDR1_10
H12 VDDR1_11
H14 VDDR1_12
H16 VDDR1_13
H18 VDDR1_14
H20 VDDR1_15
H21 VDDR1_16
B31 VDDR1_17
M1 VDDR1_18
AA9 VDD_CT_1
Y9 VDD_CT_2
V9 VDD_CT_3
T9 VDD_CT_4
J11 VDD_CT_5
J20 VDD_CT_6
J21 VDD_CT_7
L9 VDD_CT_8
AC18 VDDR3_1
AC16 VDDR3_2
AC14 VDDR3_3
AC12 VDDR3_4
AF1 VDDR4_1
AF2 VDDR4_2
AE1 VDDR5_1
AE2 VDDR5_2
M2 RSVD_1
M3 RSVD_2
L4 RSVD_3
AD11 RSVD_4
A10 VDDRH_1
A19 VDDRH_2
B10 VSSRH_1
B19 VSSRH_2
V11 BBN_1
U11 BBN_2
R11 BBP_1
P11 BBP_2
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
PCIE_VDDR_8
PCIE_VDDC_1
PCIE_VDDC_2
PCIE_VDDC_3
PCIE_VDDC_4
PCIE_VDDC_5
PCIE_VDDC_6
PCIE_VDDC_7
PCIE_VDDC_8
PCIE_VDDC_9
PCIE_VDDC_10
PCIE_VDDC_11
PCIE_VDDC_12
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
VDDC_8
VDDC_9
VDDC_10
VDDC_11
VDDC_12
VDDC_13
VDDC_14
VDDC_15
VDDC_16
VDDC_17
VDDC_18
VDDC_19
VDDC_20
VDDC_21
VDDC_22
VDDC_23
VDDC_24
VDDC_25
VDDC_26
VDDC_27
VDDC_28
VDDC_29
VDDC_30
VDDC_31
VDDC_32
VDDC_33
VDDCI_1
VDDCI_2
VDDCI_3
VDDCI_4
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%
+1.8V_PCIE_VDDR
1.8V(400mA)
L74
BLM18PG181SN1D(180,1.5A)_6
C759 *0.1U/10V_4
C760 1U/10V_4
C761 10U/6.3V_8
+1.1V_PCIE_VDDC
1.1V(1.0A)
+1.1V
L21
BLM18PG181SN1D(180,1.5A)_6
C244 0.1U/10V_4
C219 0.1U/10V_4
C186 1U/10V_4
C207 1U/10V_4
C138 10U/6.3V_8
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%
VDDC+VDDCI
0.95~1.1V(15A peak)(Ripple < 87.2mV)
+VGA_CORE
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)
C222 1U/10V_4
C232 1U/10V_4
C227 1U/10V_4
C215 1U/10V_4
C73 10U/6.3V_8
C210 1U/10V_4
C262 1U/10V_4
C261 1U/10V_4
C266 1U/10V_4
C86 10U/6.3V_8
C233 1U/10V_4
C198 1U/10V_4
C228 1U/10V_4
C200 1U/10V_4
C91 10U/6.3V_8
C181 1U/10V_4
C265 1U/10V_4
C211 1U/10V_4
C229 1U/10V_4
C90 10U/6.3V_8
+VDDCI
L27
BLM18PG181SN1D(180,1.5A)_6
+VGA_CORE
C294 0.1U/10V_4
C282 0.1U/10V_4
C283 1U/10V_4
C293 10U/6.3V_8
VDDCI--Isolated (clean) core power for the 1/0 logic. Voltage level should match that of VDDC. POWER Same as VDDC
VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.
+VBBP
*BLM18PG181SN1D(180,1.5A)_6
+VGA_CORE
L93
SI-1 modified -- ADD power play function
Q61
2N7002E
Q62
ME2303T1
+VGA_CORE
+1.8V
R752 100K/F_4
+5V
18 BBEN
Q63
2N7002E
BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.
Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V
Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC
PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number M7X/M8X_Power_and_NC
Rev 1A
Date: Tuesday, February 19, 2008
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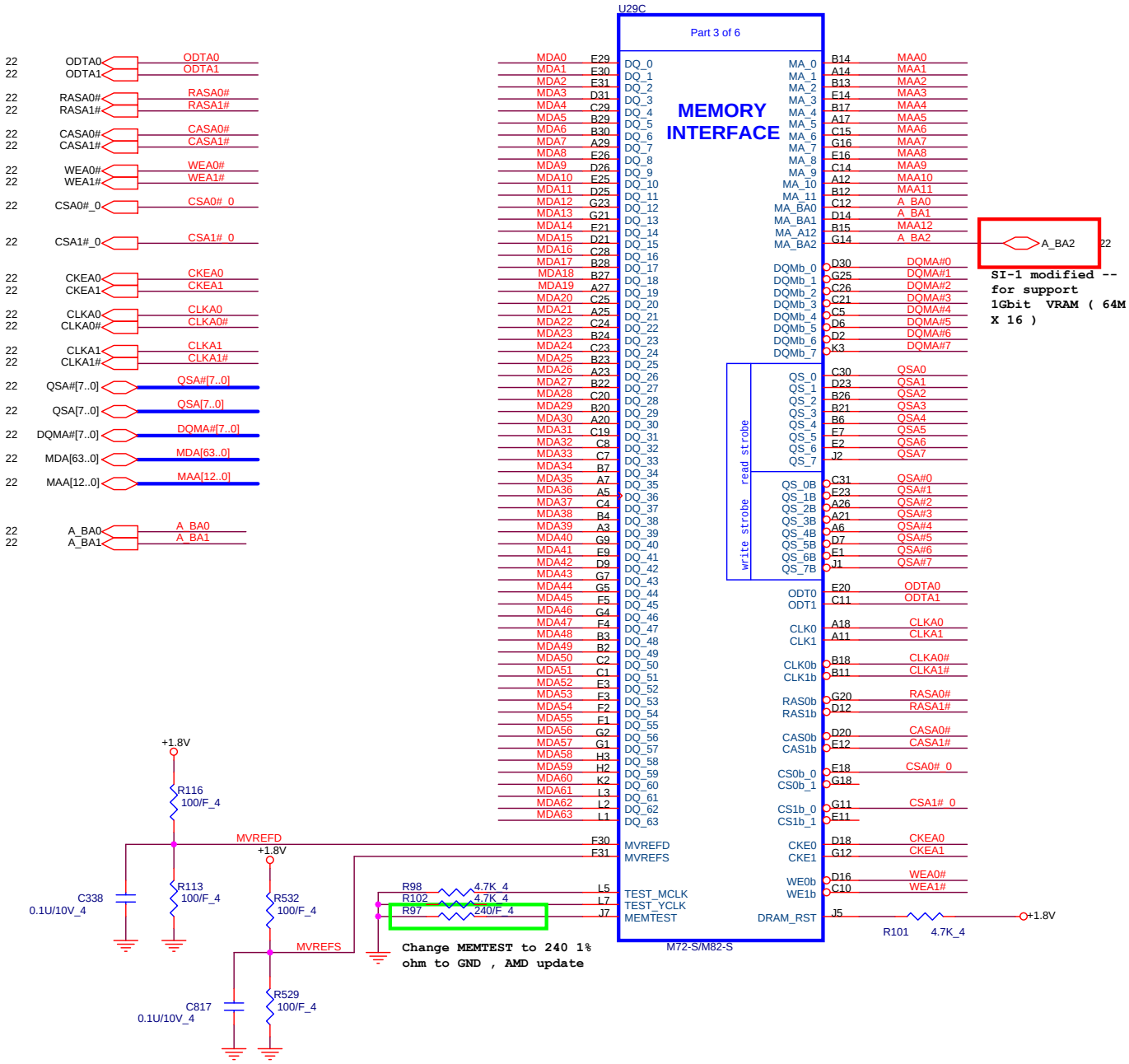
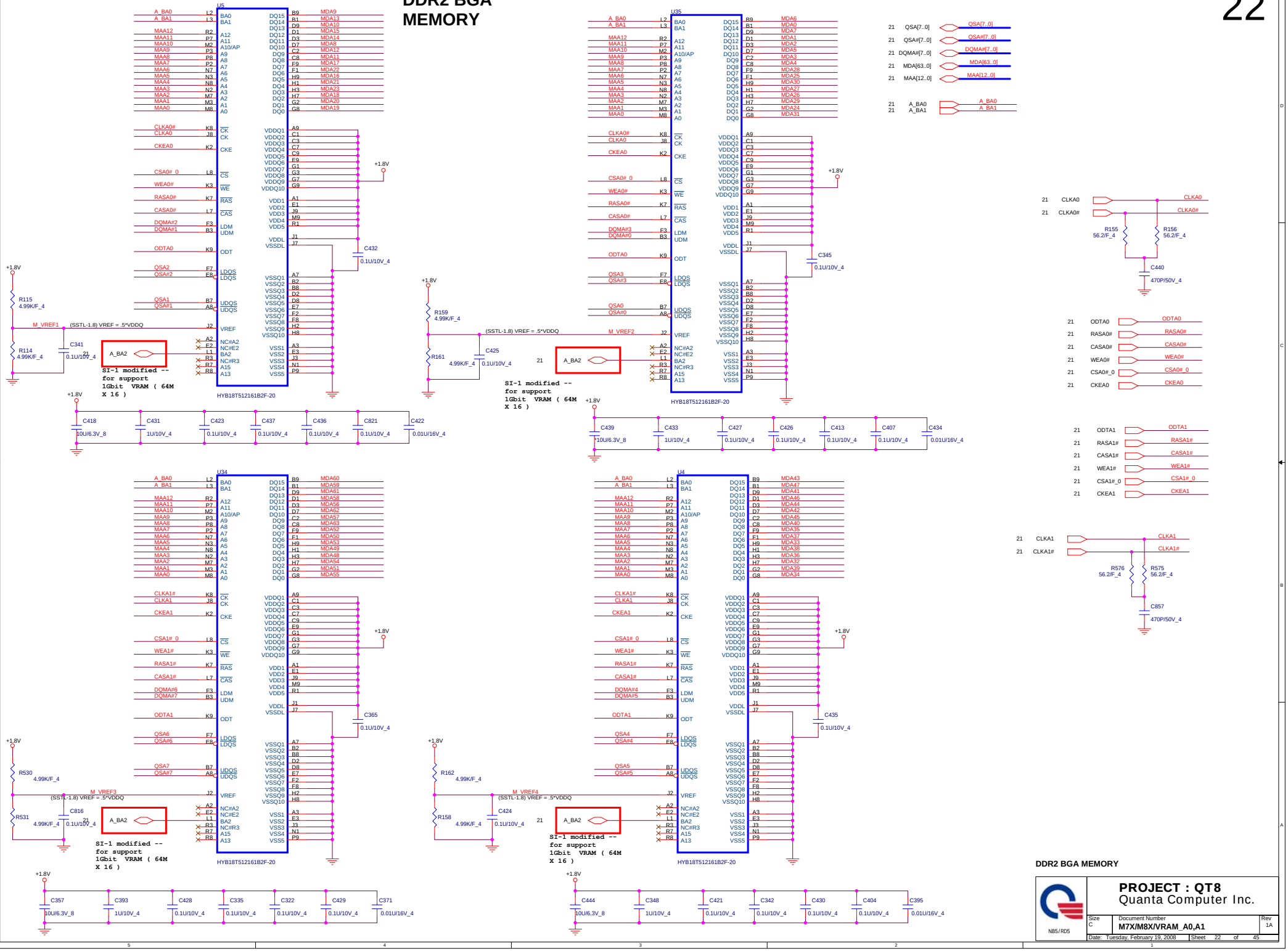


NB5/RD5	PROJECT : QT8 Quanta Computer Inc.		
	Size: B	Document Number: M7X/M8X/MEM_Interface	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 21 of 45	

DDR2 BGA MEMORY



DDR2 BGA MEMORY

NB5/RD5	**PROJECT : QT8** Quanta Computer Inc.	
	Size: C — Document Number: **M7X/M8X/VRAM_A0,A1**	Rev: 1A
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

10 LA_CLK — LA_CLK — RP3 — *0_4P2R_4 — TXLCLKOUT+
10 LA_CLK# — LA_CLK# — TXLCLKOUT-
10 LA_DATAP0 — LA_DATAP0 — RP1 — *0_4P2R_4 — TXLOUT0+
10 LA_DATAN0 — LA_DATAN0 — TXLOUT0-
10 LA_DATAP1 — LA_DATAP1 — RP4 — *0_4P2R_4 — TXLOUT1+
10 LA_DATAN1 — LA_DATAN1 — TXLOUT1-
10 LA_DATAP2 — LA_DATAP2 — RP5 — *0_4P2R_4 — TXLOUT2+
10 LA_DATAN2 — LA_DATAN2 — TXLOUT2-

10 LB_CLK — LB_CLK — RP2 — *0_4P2R_4 — TXUCLKOUT+
10 LB_CLK# — LB_CLK# — TXUCLKOUT-
10 LB_DATAP0 — LB_DATAP0 — RP6 — *0_4P2R_4 — TXUOUT0+
10 LB_DATAN0 — LB_DATAN0 — TXUOUT0-
10 LB_DATAP1 — LB_DATAP1 — RP8 — *0_4P2R_4 — TXUOUT1+
10 LB_DATAN1 — LB_DATAN1 — TXUOUT1-
10 LB_DATAN2 — LB_DATAN2 — RP7 — *0_4P2R_4 — TXUOUT2+
10 LB_DATAP2 — LB_DATAP2 — TXUOUT2+

OPTION SIGNAL FROM M8X to LVDS for discrete

19 EXT_TXLCLKOUT- — EXT_TXLCLKOUT- — RP59 — 0_4P2R_4 — TXLCLKOUT-
19 EXT_TXLCLKOUT+ — EXT_TXLCLKOUT+ — TXLCLKOUT+
19 EXT_TXLOUT0- — EXT_TXLOUT0- — RP57 — 0_4P2R_4 — TXLOUT0-
19 EXT_TXLOUT0+ — EXT_TXLOUT0+ — TXLOUT0+
19 EXT_TXLOUT1- — EXT_TXLOUT1- — RP60 — 0_4P2R_4 — TXLOUT1-
19 EXT_TXLOUT1+ — EXT_TXLOUT1+ — RP61 — 0_4P2R_4 — TXLOUT1+
19 EXT_TXLOUT2+ — EXT_TXLOUT2+ — TXLOUT2+
19 EXT_TXLOUT2- — EXT_TXLOUT2- — TXLOUT2-

19 EXT_TXUCLKOUT- — EXT_TXUCLKOUT- — RP58 — 0_4P2R_4 — TXUCLKOUT-
19 EXT_TXUCLKOUT+ — EXT_TXUCLKOUT+ — TXUCLKOUT+
19 EXT_TXUOUT0+ — EXT_TXUOUT0+ — RP62 — 0_4P2R_4 — TXUOUT0+
19 EXT_TXUOUT0- — EXT_TXUOUT0- — TXUOUT0-
19 EXT_TXUOUT1- — EXT_TXUOUT1- — RP64 — 0_4P2R_4 — TXUOUT1-
19 EXT_TXUOUT1+ — EXT_TXUOUT1+ — TXUOUT1+
19 EXT_TXUOUT2- — EXT_TXUOUT2- — RP63 — 0_4P2R_4 — TXUOUT2-
19 EXT_TXUOUT2+ — EXT_TXUOUT2+ — TXUOUT2+

UMA/DISCRETE select for HDMI

From RS780M

for Layout concern ,placement close north bridge

9 C_PEG_TX#15 — C_PEG_TX#15 — C386 — *0.1U/10V_4 — TX2_HDMI-L — TX2_HDMI+L — C387 — *0.1U/10V_4 — TX2_HDMI+
9 C_PEG_TX15
9 C_PEG_TX#14 — C_PEG_TX#14 — C388 — *0.1U/10V_4 — TX1_HDMI-L — TX1_HDMI+L — C389 — *0.1U/10V_4 — TX1_HDMI+
9 C_PEG_TX14
9 C_PEG_TX#13 — C_PEG_TX#13 — C355 — *0.1U/10V_4 — TX0_HDMI-L — TX0_HDMI+L — C344 — *0.1U/10V_4 — TX0_HDMI+
9 C_PEG_TX13
9 C_PEG_TX#12 — C_PEG_TX#12 — C827 — *0.1U/10V_4 — TXC_HDMI-L — TXC_HDMI+L — C828 — *0.1U/10V_4 — TXC_HDMI+
9 C_PEG_TX12

for Layout concern ,placement close HDMI conn

RP31: TX2_HDMI+L, TX2_HDMI-L → TX2_HDMI+, TX2_HDMI-
RP23: TX1_HDMI+L, TX1_HDMI-L → TX1_HDMI+, TX1_HDMI-
RP37: TX0_HDMI+L, TX0_HDMI-L → TX0_HDMI+, TX0_HDMI-
RP17: TXC_HDMI+L, TXC_HDMI-L → TXC_HDMI+, TXC_HDMI-

From M82-S

18 TX2_HDMI_L- — TX2_HDMI_L- — C794 — 0.1U/10V_4 — TX2_HDMI-
18 TX2_HDMI_L+ — TX2_HDMI_L+ — C789 — 0.1U/10V_4 — TX2_HDMI+
18 TX1_HDMI_L- — TX1_HDMI_L- — C782 — 0.1U/10V_4 — TX1_HDMI-
18 TX1_HDMI_L+ — TX1_HDMI_L+ — C786 — 0.1U/10V_4 — TX1_HDMI+
18 TX0_HDMI_L- — TX0_HDMI_L- — C799 — 0.1U/10V_4 — TX0_HDMI-
18 TX0_HDMI_L+ — TX0_HDMI_L+ — C797 — 0.1U/10V_4 — TX0_HDMI+
18 TXC_HDMI_L- — TXC_HDMI_L- — C768 — 0.1U/10V_4 — TXC_HDMI-
18 TXC_HDMI_L+ — TXC_HDMI_L+ — C776 — 0.1U/10V_4 — TXC_HDMI+

for Layout concern ,placement close HDMI conn

+5V — Q36 2N7002E — R528 100K/F_4

R507 499/F_4 TX2_HDMI+
R508 499/F_4 TX2_HDMI-
R506 499/F_4 TX1_HDMI+
R505 499/F_4 TX1_HDMI-
R512 499/F_4 TX0_HDMI+
R515 499/F_4 TX0_HDMI-
R504 499/F_4 TXC_HDMI+
R500 499/F_4 TXC_HDMI-

UMA RS780M ⊢ 750 ohm CS17502FB19

DIS M82-S ⊢ 499 ohm CS14992FB24

Close to HDMI Connector

+12VALW / +3V / +5VSUS / +3VLCD

+12VALW — R19 330K_6 — A03404 ID current 5.8A — N-MOS,5.8A Q1 AO3404 — +3VLCD
+3V — C16 0.1U/10V_4
+5VSUS — R14 100K/F_4 — Q3 PDTC144EU — Q4 2N7002E — C22 0.1U/10V_4 — R10 22_8 — LCDDISCHG
LCDON — LCDON# — Q2 2N7002E
10,19 DISP_ON — R17 2.2K_4

+5V — R401 75R/F_6 — +LOGO_PWR

SI-2 modified-delete R402 and R401 from 0ohm to 75ohm

+3V — R8 2.2K_4 EDIDCLK — R7 2.2K_4 EDIDDATA

+3VLCD — L1 PBY201209T-4A_8 — +3VLCD_CON — C12 10U/6.3V_8 — C10 0.1U/10V_4 — C13 0.01U/16V_4

+VIN_BLIGHT — +3VLCD_CON

C6 1000P/50V_4 — C678 1000P/50V_4

10,18 EDIDDATA — +3V — EDIDDATA — +LOGO_PWR — BLONCON

CN1 (41 / 42):
TXLCLKOUT+ / TXLCLKOUT-
TXLOUT0+ / TXLOUT0-
TXLOUT1+ / TXLOUT1-
TXLOUT2+ / TXLOUT2-
VADJ1 — EDIDCLK 10,18
Camera Pin
TXUCLKOUT+ / TXUCLKOUT-
TXUOUT0+ / TXUOUT0-
TXUOUT1+ / TXUOUT1-
TXUOUT2+ / TXUOUT2-

PN_BLON / LVDS_BLON / LCD_BK

PN_BLON — D5 CH501H-40PT — BLONCON — C28 22P/50V_4 — R22 100K/F_4
+3VPCU — R24 33K_6
D6 CH501H-40PT — LID_EC# — LID_EC# 34,35
10,18 LVDS_BLON — LVDS_BLON — R23 1K/F_4 — PN_BLON
D7 CH501H-40PT — HWPG — 20,35,38,39,41,42
12 LCD_BK — LCD_BK — Q5 PDTC144EU — R259 *10K/F_4 — +3VS5

Del R21 and Pull hi R259 to +3VS5, add D7 to HWPG on PV

PV del logo light

10,19 DPST_PWM — DPST_PWM — R88 — LCD CONN *0_4
35 PWM_VADJ — PWM_VADJ — R96 — 0_4 — VADJ1
C5 *4.7U/6.3V_6 — C7 0.1U/10V_4

+VIN / +VIN_BLIGHT

+VIN — L2 FBM2125 HM330-T(4A,0.015) 8 — +VIN_BLIGHT
C15 0.1U/50V_6 — C11 0.01U/50V_4 — C9 0.1U/50V_6 — C14 *10U/25V_12 — C8 0.1U/50V_6

HDMI HPD SENSE

10,18 TMDS_HPD — TMDS_HPD — R66 20K/F_4 — HDMI_DET
check 3v or 5v
D10 UDZS2.7BTE-17 — R64 100K/F_4

+5V_HDMVCC

+5V_HDMVCC — D31 CH501H-40PT — R494 4.7K_4 — HDMI_SCLK
+5V_HDMVCC — D32 CH501H-40PT — R503 4.7K_4 — HDMI_SDATA

Change R494, R503 to 4.7K for AMD on PV

HDMI PORT

CN29 HDMI CONN:
TX2_HDMI+ / TX2_HDMI- / TX1_HDMI+ / TX1_HDMI- / TX0_HDMI+ / TX0_HDMI- / TXC_HDMI+ / TXC_HDMI-
SHELL1 SHELL3 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL4 SHELL2

Del C748, C756 for HDMI on PV

HDMI_SCLK — L73 — HDMISCL
HDMI_SDATA — L75 — HDMISDA
+5V_HDMVCC
+5V — FUSE1A6V_POLY F1 — C128 *0.1U/10V_4
HDMI_DET

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

18 HDMI_SDA — HDMI_SDA — RP65 0_4P2R_4 — HDMI_SDATA
18 HDMI_SCL — HDMI_SCL — HDMI_SCLK

Discrete DDC4 is 5V tolerance , the MOSFET level shifter no need
UMA DDC is 3V tolerance,the MOSFET level shifter is need

DIS

+3V — R680 *2K/04 — 10 HDMI_DDC_CLK — Q59 *FDV301N — 3 HDMI_SCLK
+5V
Change 2N7002 to FDV301N for AMD on PV

HDMI_DDC_CLK — R753 *0_4 — HDMI_SCLK
HDMI_DDC_DATA — R755 *0_4 — HDMI_SDATA

UMA

+3V — R681 *2K/04 — 10 HDMI_DDC_DATA — Q60 *FDV301N — 3 HDMI_SDATA
+5V

NB5/RD5	**PROJECT : QT8** Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN,HDMI CONN	Rev: 1A
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CRT PORT

SI-2 modified --Change Layout footprint 12/27

+5VCRT — C670 0.1U/10V_4

+5V — F2 40 mils — +5VCRT

40 MIL

FUSE1A6V_POLY

CRT_R_1_L — L61 BLM18BA470SN1(47,300MA)_6 — CRT_R1

CRT_G_1_L — L60 BLM18BA470SN1(47,300MA)_6 — CRT_G1

CRT_B_1_L — L59 BLM18BA470SN1(47,300MA)_6 — CRT_B1

R400 150/F_4 · R399 150/F_4 · R398 150/F_4 · C677 5.6P/50V_6 · C675 5.6P/50V_6 · C672 5.6P/50V_6 · C671 5.6P/50V_6 · C674 5.6P/50V_6 · C676 5.6P/50V_6

EMI

CRT CONN CN20

close conn within 600mils

R400 for UAM use 140 ohm on PV(AMD)

+5V — C673 0.1U/10V_4

U21 AHCT1G125DCH

U22 AHCT1G125DCH

10,18,19 VSYNC_COM → PR_VSYNC 37

10,18,19 HSYNC_COM → PR_HSYNC 37

R1 0_4 CRTDDCCLK2

R3 33_4 CRTVSYNC

R4 33_4 CRTHSYNC

R5 0_4 CRTDDCDAT2

C1 *470P/50V_4 · C2 *47P/50V_4 · C3 *47P/50V_4 · C4 *47P/50V_4

follow AMD reference schematic change for reduce leakage to VDDR3 BUS

+3V_DELAY — R761 4.7K_4 — +3V — R25 *4.7K_4

10,18 DDCCLK — DDCCLK — Q6 2N7002E — DDCCLK2 — DDCCLK2 37

+3V_DELAY — R762 4.7K_4 — +3V — R26 *4.7K_4

10,18 DDCDATA — DDCDATA — Q7 2N7002E — DDCDAT2 — DDCDAT2 37

R2 6.81K_4 · R6 6.81K_4

+5VCRT — +5VCRT — CH501H-40PT — D25 — +5V_CRT2

+3V

D28 *BAV99W — CRT_R1

D27 *BAV99W — CRT_G1

D26 *BAV99W — CRT_B1

D1 *BAV99W — DDCCLK2

D2 *BAV99W — CRTVSYNC

D3 *BAV99W — CRTHSYNC

D4 *BAV99W — DDCDAT2

U23

37 PR_RED — PR_RED — CRT_R_1_L

37 PR_GEN — PR_GEN — CRT_G_1_L

37 PR_BLU — PR_BLU — CRT_B_1_L

35,37 PR_INSERT#

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E

YA YB YC YD

CRT_R CRT_G CRT_B → CRT_R 10,18 · CRT_G 10,18 · CRT_B 10,18

VCC GND

+5V_SW — R403 0_6 — +5V

C679 0.1U/10V_4

R404 10K/F_4

74CBT3257

EMI

CRT SWITCH

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	CRT	1A

Date: Tuesday, February 19, 2008 | Sheet 24 of 45

For 5158E

2 CLK_48M_CR — R397 *0_4 — XTLO

+3VSUS — R321 *100K/F_4

UMA BOM need to add

26,29 CARD_LED# — R320 *0_4 — CARD_LEDO

U19

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ

XD_CD# — SP2 — SD_CD# — SP4

SI-2 modified --Fix Y5 layout footprint to XTAL-5X3_2-3_8 (ME placement)

R362 *6.19K/F_4 — RREF

13 USBP6_CR- — DM
13 USBP6_CR+ — DP

C665 *5.6P/50V_4 — XTLO — *12MHz — Y5 — XTLI — C668 *5.6P/50V_4

R395 *270K_4

For 5158 BG6120000717

MODE_SEL — R394 *10K/F_4 — C667 *47P/50V_4

For 5158

+3VSUS — R667 *100K/F_4 — 5158_RST# — C925 *1U/10V_4

If SD_DAT1 connect to SP4 , MOD_SEL need to let it to N.C

XTLO XTLI MODE_SEL RST#

XD_CLE/CF_D3 XD_CE#/CF_D11 XD_ALE/CF_D4

SD_DAT2/XD_RE#/CF_D12 SD_DAT3/XD_WE#/CF_D5 XD_RDY/CF_D13 SD_DAT4/XD_WP#/CF_D6

SD_CMD SD_DAT5/XD_D0/CF_D14 SD_CLK/XD_D1/MS_CLK/CF_D7 SD_DAT6/XD_D7/MS_D3/CF_D15 CF_CS0# MS_INS#/CF_IORD# SD_DAT7/XD_D2/MS_D2/CF_IOWR# SD_DAT0/XD_D6/MS_D0/CF_RST# SD_DAT1/XD_D3/MS_D1/CF_IORDY XD_D5/MS_BS/CF_A2

AV_PLL_IN — C647 *0.1U/10V_4 — C918 *1U/10V_4

VREG_OUT 5V_IN A3V3_IN D3V3_IN — VREG

D3V3_OUT — C633 *0.1U/10V_4 — C634 *0.1U/10V_4 — C612 *0.1U/10V_4 — C589 *4.7U/6.3V_6 — +3VSUS

A3V3_OUT — +3VSUS

CARD_3V3_OUT — +3VCARD

AG33 AG_PLL DGND2 DGND1 — C629 *1U/10V_4 — C624 *0.1U/10V_4 — C917 *0.1U/10V_4

*RTS5158

SI-2 remove R673 not need -- UMA BOM remove

+3VSUS_RTS — C593 *0.1U/10V_4 — C598 *4.7U/6.3V_6 — R323 *0_6 — +3VSUS

+3VCARD — C628 *0.1U/10V_4 — C618 *0.1U/10V_4 — C617 *0.1U/10V_4

For 5158

SP6 — R339 *0_4 — SD_DAT1
SP4 — R333 *0_4

For 5158E

AL005158B10 -->RTS5158E

AL005158B00 -->RTS5158

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7	R315 *0_4	MS_DATA0_SD_DAT0	
	R316 *0_4	XD-D6	
SP6	R334 *0_4	MS_DATA1	
	R338 *0_4	XD-D3	
SP8	R345 *0_4	MS_DATA2_XD_D2	
SP16	R666 *0_4	SD_DAT2	
	R676 *0_4	XD-RE#	
SP5	R327 *0_4	MS_BS	
	R335 *0_4	XD-D5	
SP15	R675 *0_4	SD_DAT3	
	R390 *0_4	XD_WE	
SP11	R354 *0_4	SD_CLK_MS_CLK	
	R358 *0_4	XD-D1	
SP2	R319 *0_4	SD_WP	
SP13	R677 *0_4	XD-WP#	
SP19	R393 *0_4	XD-CLE	
SP4	R317 *0_4	XD-D4	
SP10	R351 *0_4	MS_DATA3	
	R348 *0_4	XD-D7	
SP14	R389 *0_4	XD-RB#	
SP12	R369 *0_4	XD-D0	
SP17	R391 *0_4	XD-ALE	
SP18	R392 *0_4	XD-CE#	
SD_CMD_R	R372 *0_4	SD_CMD	

CH501H-40PT — D23 — MS_CD# — XD_CD# — SD_CD# — CH501H-40PT — C873 270P/25V_4

RTS5158 need to remove D23/D24/C873

JMB 380 Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER

XD,MMC/SD,MS/MSP

+3VCARD — C905 *270P/25V_4

R678 *10K/F_4 — XD-WP#

Del R625 for TP on PV

CN36

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

GND GND GND GND GND SD-C/D SD-CD-SW SD-W/P SD-WP-SW XD-CD XD-VCC XD-DATA7 XD-DATA6 XD-DATA5 XD-DATA4 XD-DATA3 XD-DATA2 XD-DATA1 XD-DATA0 SD-CLK SD-VCC

MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

SD_CD# SD_CD# SD_WP SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

26 MS_CD#

5IN1 CARD READER SOCKET

+3VCARD — C872 2.2U/6.3V_6 — R607 150K/F_4

CLOSE CONN

+3VCARD — C887 0.1U/10V_4 — C894 0.1U/10V_4 — C874 0.1U/10V_4

+3V — Q25 *AO3409 — +3VCARD

+5V

26 MC_PWR_CTRL_0# — XD_PWON R387 *10K/F_4 — +3VCARD

R332 0_8

RESERVED for JMicron -- after programming can out-put +3.3V throught MC_PWR_CTRL_0# signal

SI-2 for 台端Conn

CN42

+3VCARD +3VCARD

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

xD-R/B xD-RE xD-CE xD-CLE xD-ALE xD-WE xD-WP xD-D0 xD-D1 SD-DAT2 SD-DAT3 SD-CMD GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

GND GND GND GND NC NC SD-CD SD-WP xD-CD xD-VCC xD-D7 xD-D6 xD-D5 SD-DAT1 xD-D4 xD-D3 SD-DAT0 xD-D2 SD-CLK SD-VCC

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

26 SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

*TAI TWUM 5IN1 CARD READER SOCKET

26 MDIO00 — R611 0_4 — MS_DATA0_SD_DAT0
26 MDIO01 — R623 0_4 — XD-D0
R608 0_4 — SD_DAT1
R610 0_4 — MS_DATA1
R622 0_4 — XD-D1
26 MDIO02 — R612 0_4 — MS_DATA2_XD_D2
R620 0_4 — SD_DAT2
26 MDIO03 — R614 0_4 — MS_DATA3
R619 0_4 — SD_DAT3
R606 0_4 — XD-D3
26 MDIO04 — R618 0_4 — SD_CMD
R609 0_4 — MS_BS
R627 0_4 — XD_WE
26 MDIO05 — R617 47/F_4 — SD_CLK_MS_CLK
R634 47/F_4 — XD-CE#
26 MDIO06 — R593 0_4 — SD_WP
R591 0_4 — XD-WP#
26 MDIO07 — R633 0_4 — XD-CLE
26 MDIO08 — R605 0_4 — XD-D4
26 MDIO09 — R603 0_4 — XD-D5
26 MDIO10 — R602 0_4 — XD-D6
26 MDIO11 — R601 0_4 — XD-D7
26 MDIO12 — R679 0_4 — XD-RE#
26 MDIO13 — R635 0_4 — XD-RB#
26 MDIO14 — R628 0_4 — XD-ALE

SI-2 modified - for Jmicron updae

PAD8 MDC_SPRING — PAD9 MDC_SPRING — PAD10 MDC_SPRING — PAD11 MDC_SPRING

H32 H31 *H-S315D110P2 — H2 *H-S315D110P2 — H13 *H-C173X118D173X118N — PAD7 — *MDC_SPRING

H22 *H-S315D110P2 — H23 *H-C244D186P2 — H6 *H-C217D157P2 — H9 *H-C217D157P2 — H8 *H-C217D157P2 — H3 *H-C256D157P2

K/B SCREW HOLE — VGA Hole

H12 — H7 *H-S315D110P2 — H25 *H-C315D118P2 — H18 *H-C256D217P2 — H17 *H-C256D217P2

PAD4 — Del PAD1 for TP on PV

MDC_SPRING — PAD5 — PAD2 — *MDC_SPRING

MDC_SPRING — PAD6 — PAD3

*MDC_SPRING *MDC_SPRING

for MDC cable routing

H5 *H-S315D110P2 — H11 *H-S315D110P2 — H4 *H-C217D181P2 — H10 *H-C217D181P2 — H1 *H-C315d118p2

Mini Card Hole

H20 *H-C256D217P2 — H14 *H-C256D217P2

SI-2 for CN37

H28 *H-C236D87P2 — H29 *H-C236D87P2 — H30 *H-C236D87P2

H26 *H-C256D217P2 — H27 *H-C256D217P2

PAD12 — MDC_SPRING

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

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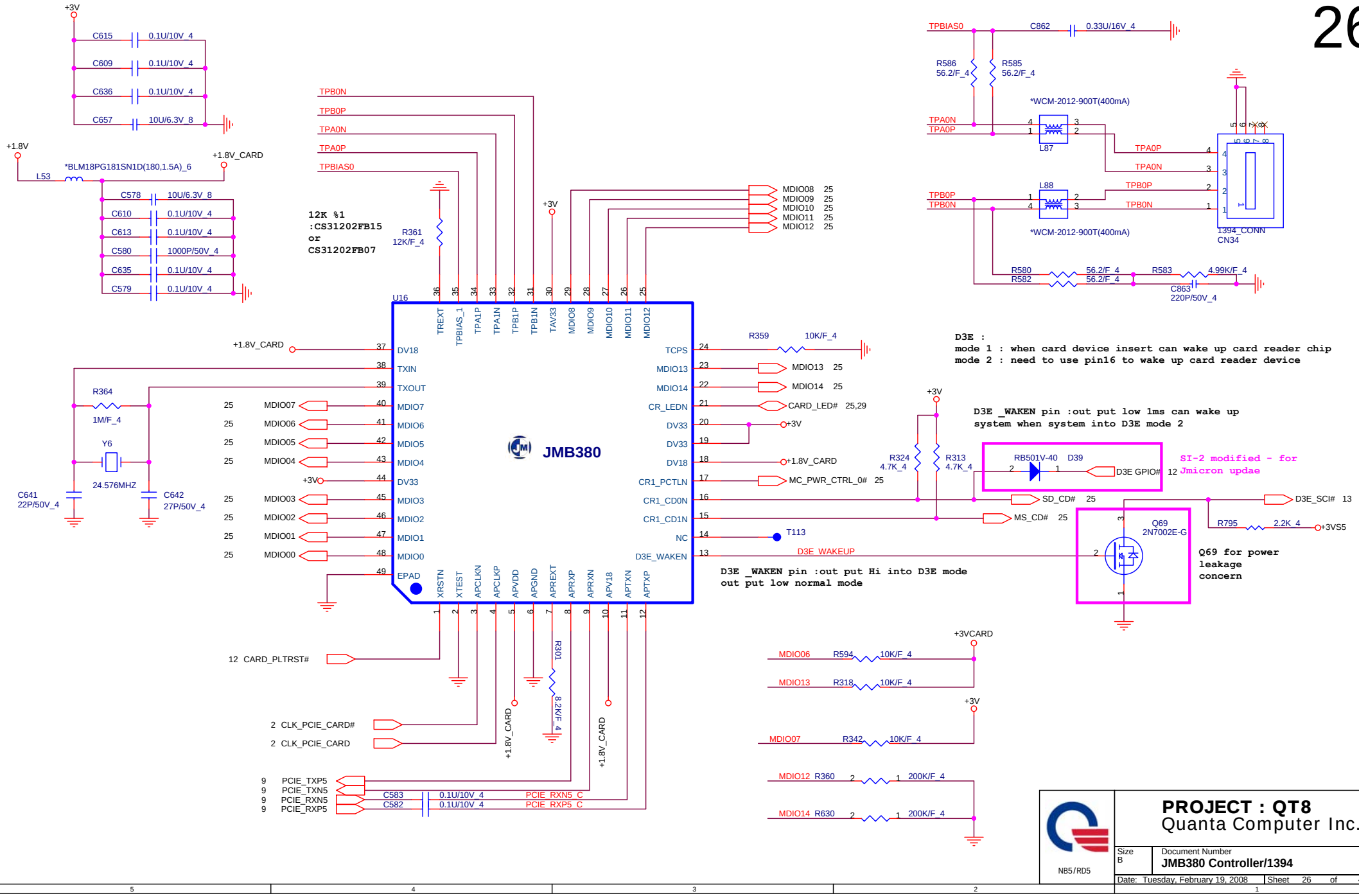

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	1A

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NB5/RD5

SI-2 Modified -- change footrint QFN48-7X7-5-49P-1H for datasheet update

SI-2 Modified

EAPD#--DEFAULT is Hi

Del R672 direct on PV

Del R686, R356, R349 direct on PV

Change C923, 924 footprint

TO Headphone jack

TO Internal Speakers

92HD71B7

recommand use X7R /10V

TO EXTERNAL MIC

TO DOCK MIC

Audio JACK: Normal Open
SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#-->DOCK MIC

Change to SHORT-1A for EMI on PV

SI-2 for EMI

TO AUDIO/B CON.

SI-2 modified -- Change footprint for ME request , pin 13,14 are 固定pin

TO Headphone jack

R807 change to 330K for HP on PV

Change C962, 963 footprint

Del R814, R815 on PV

TO DOCK Headphone

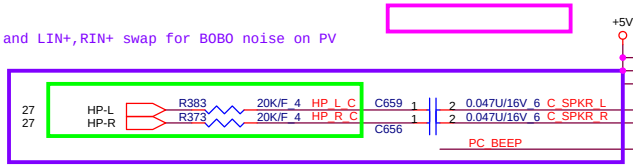
Add C141 for soft star on PV

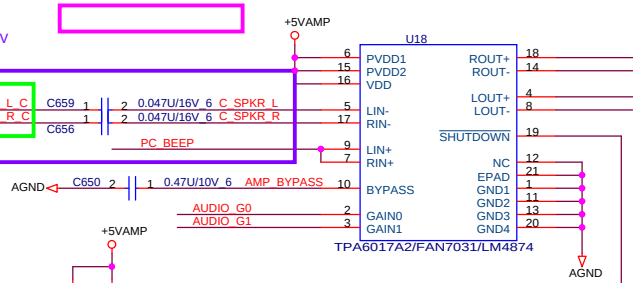
PROJECT : QT8 Quanta Computer Inc.		
Size: Custom	Document Number: Azalia AD1883	Rev: 1A
NB5/RD5	Date: Tuesday, February 19, 2008	Sheet 27 of 45

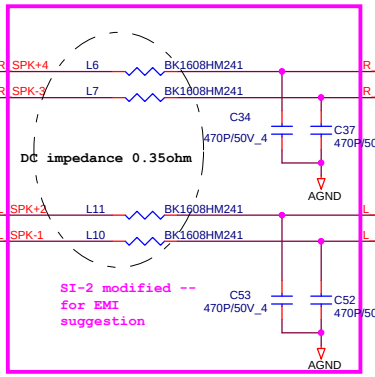
AUDIO AMPLIFIER

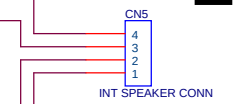
SI-2 Modified -- remove C621/C623

LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV









INT. SPEAKER

Vrms = Vpp / 2 √2

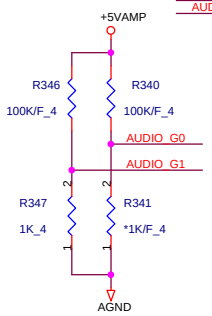
Power = (Vrms)²/ R

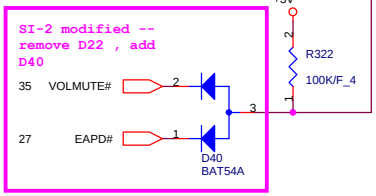
QT8 speaker -- 3.2ohm / 2W

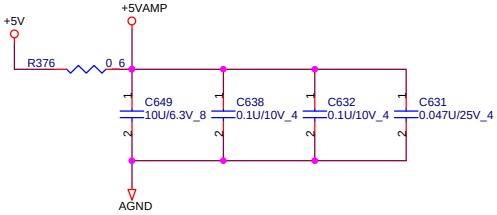
PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue

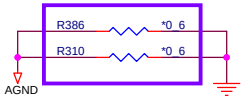
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K



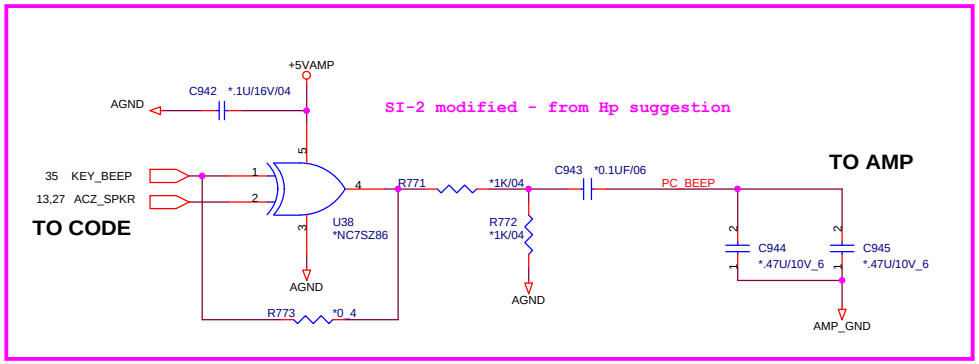






R386, R310 change to SHORT-1A on PV

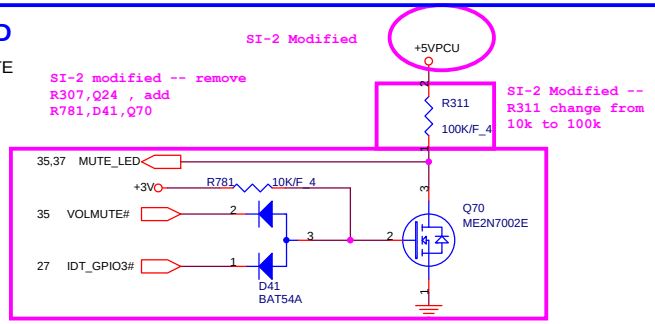
PC-BEEP



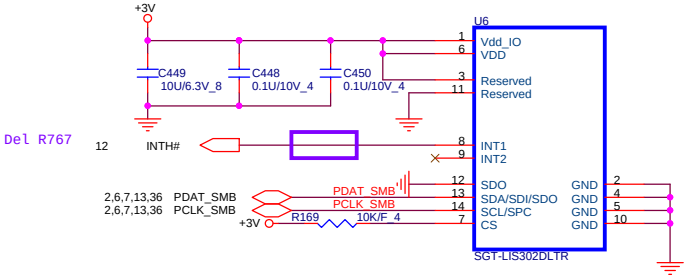
MUTE_LED

Low -->un-MUTE

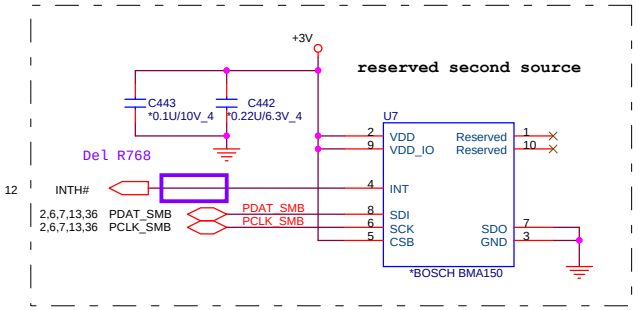
High-->Mute



Acceleration sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



NB5/RD5

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Quanta Computer Inc.

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Custom	AMP_TPA6017/INT SPK	1A

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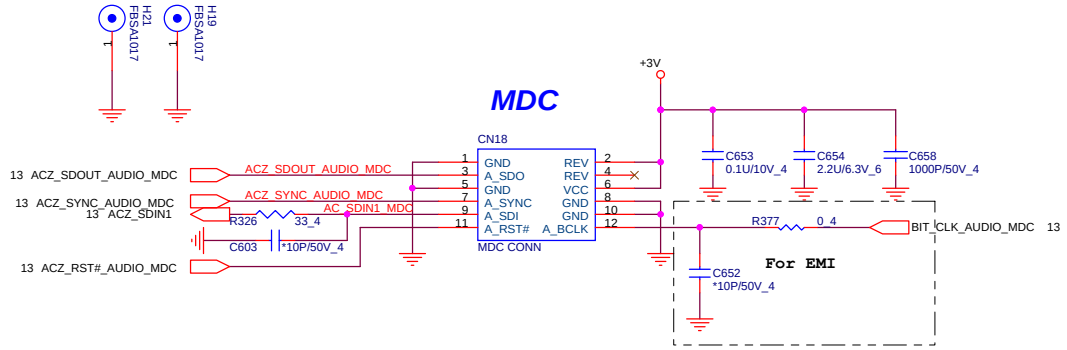
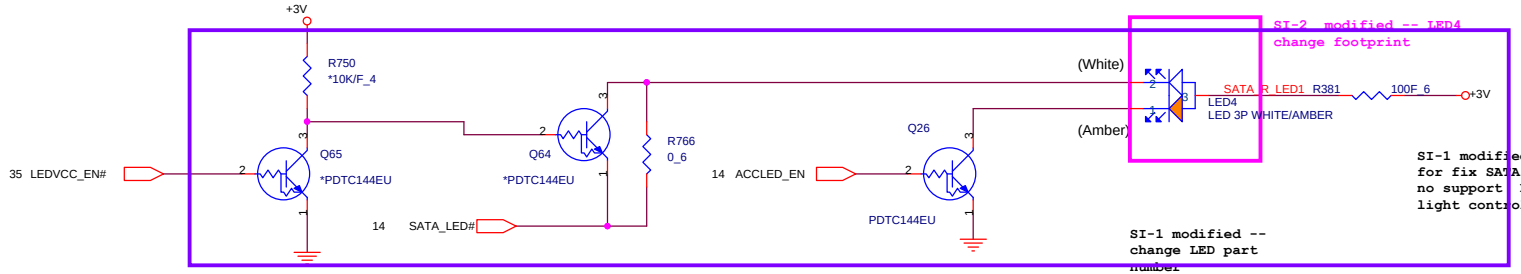
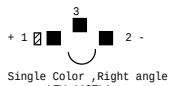
Modem CONN

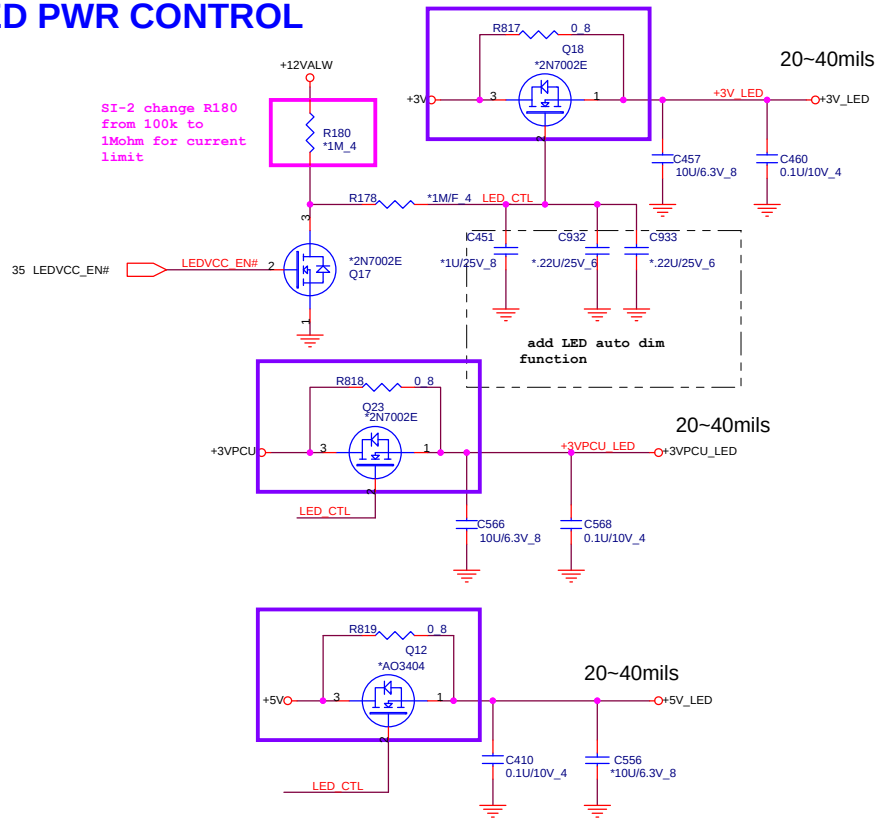




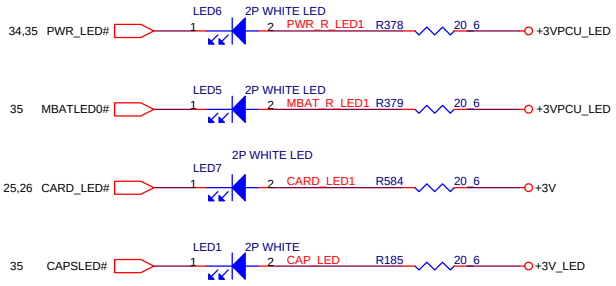
LED

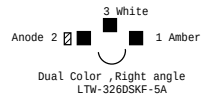


LED PWR CONTROL

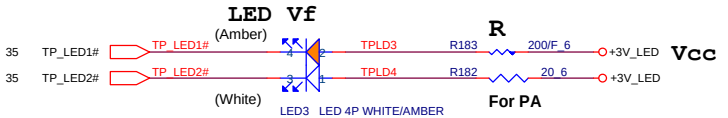


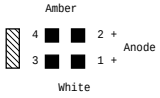
Del R380
Change R381 to 100
Add R766, R817, R818, R819
LED PWR control no-stuff on PV





I = Vcc -Vf / R





PROJECT : QT8
Quanta Computer Inc.

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Custom	MDC1.5 Con Accelerometer/ILED	1A

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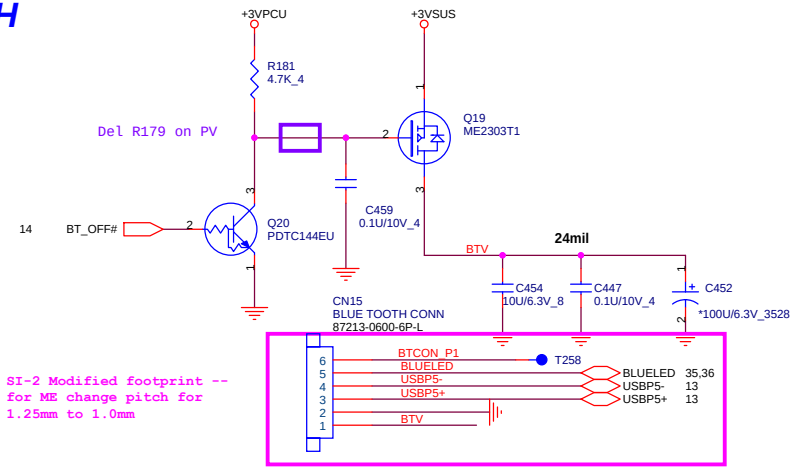
NB5/RD5

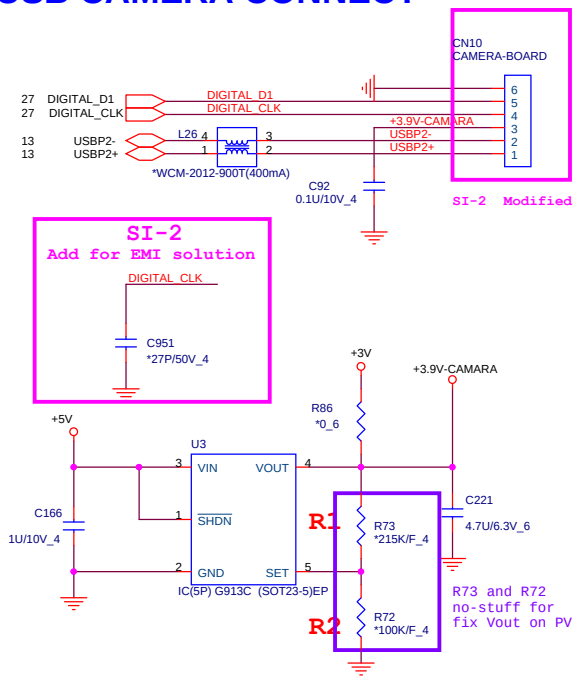
BLUETOOTH



For Discrete Touch-Screen

SI-2 Modified -- remove touch-screen function

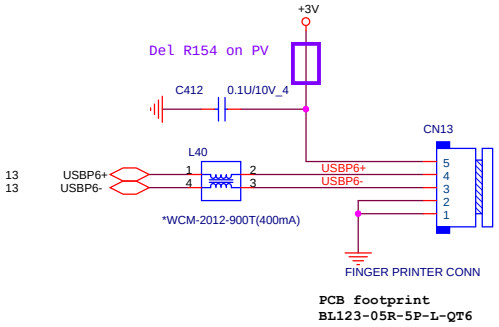
USB CAMERA CONNECT



Vout=1.25(1+R1/R2)

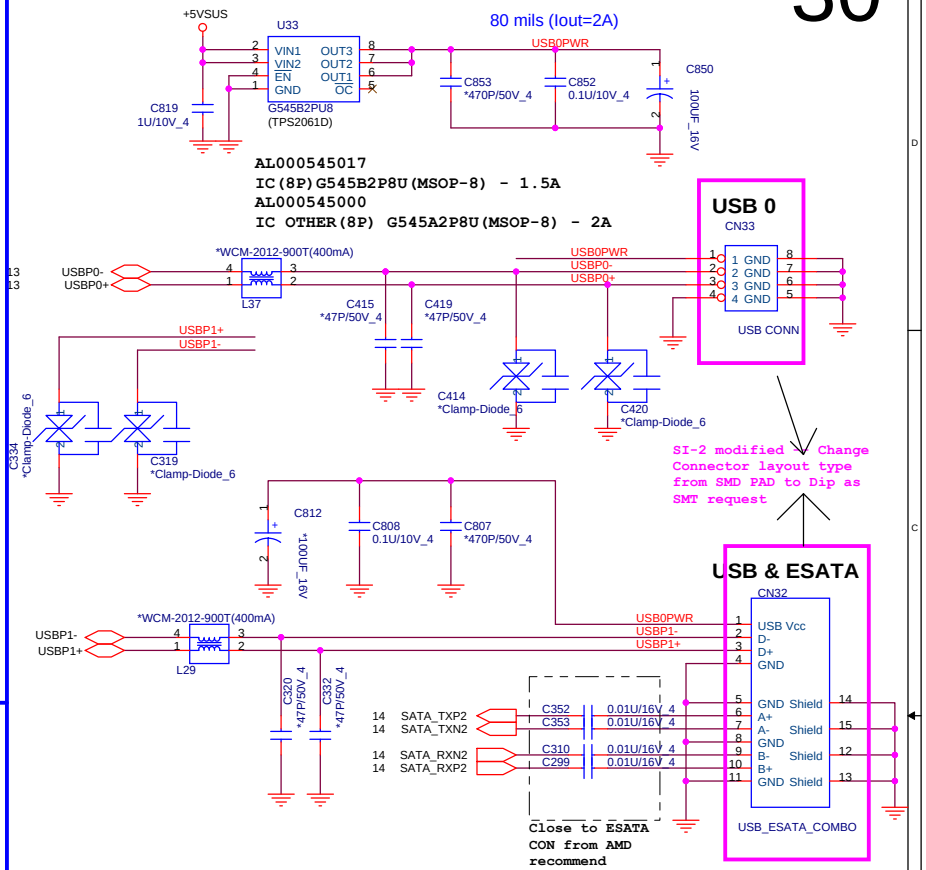
USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

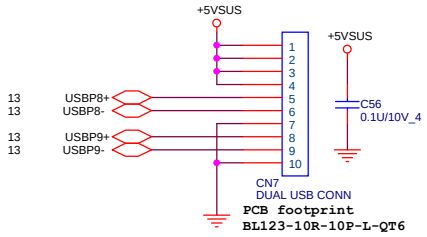


PCB footprint
BL123-05R-5P-L-QT6

LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



PCB footprint
BL123-10R-10P-L-QT6

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WEBCAM/FT/USBX4/ESATA	1A

Date: Tuesday, February 19, 2008 Sheet 30 of 45

NB5/RD5

Stuffed for 8101E/8102E/RTL8111C

Stuffed for RTL8111C(10/100/1000)

Stuffed for 8102E/RTL8101E

Del R50 on PV

Del R36, C712, C710 on PV

Del R766 for TP on PV

Del U1, R46 on PV

use BIOS to programming EEPROM , EEDI should be pull Hi

R46 only for 8111B, 8101E&8102E&8111C can remove

Remove R456 and Add D42 on PV

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R778 SI-2 modified -- RTL8111C remove , RTL8111B,8101E,8102E need to stuff

Del R429, R431, R433, R435, C718, C726 for 8111B on PV

Del R428 on PV

SI-2 modified -- LAN_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

Link

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

AL08101E005 IC(64P)RTL8101E-GR(QFN)

NS892402:GIGABIT DB0AT9LAN05

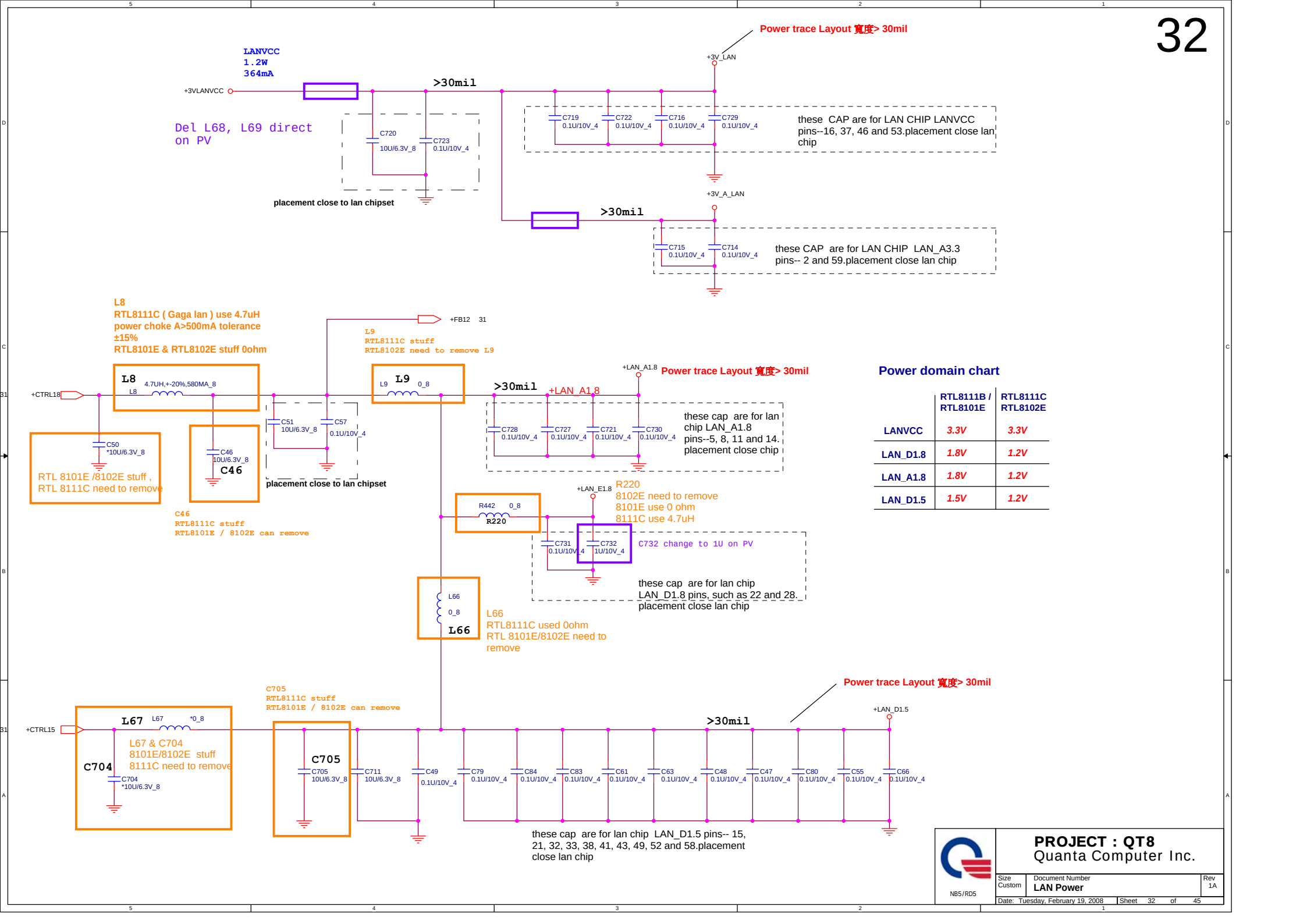
NS892405:10/100 DB0ZB1LAN04

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ11-RJ45 CN	1A

Date: Tuesday, February 19, 2008 Sheet 31 of 45

NB5/RD5



Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

NB5/RD5

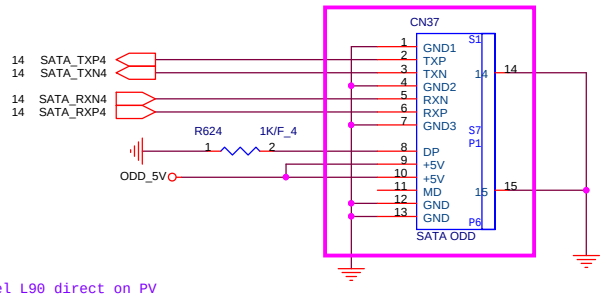
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A

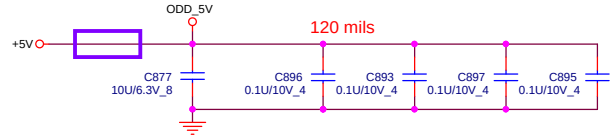
Date: Tuesday, February 19, 2008 | Sheet 32 of 45

SATA CD-ROM

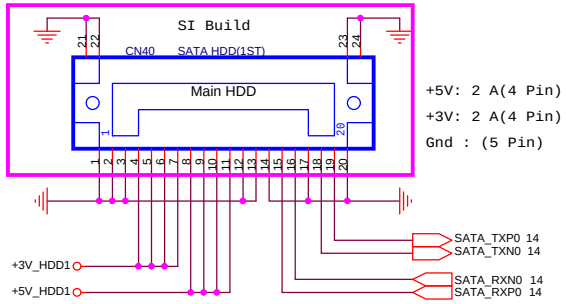
SI-2 Modified footprint -- Modify 12/27

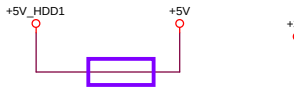


Del L90 direct on PV

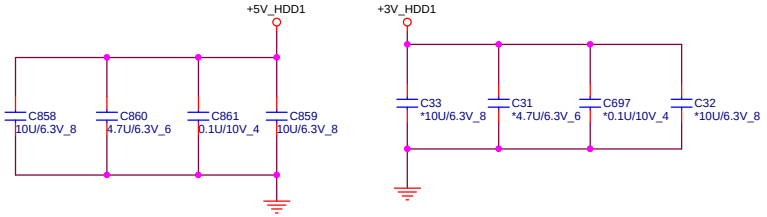


SI-2 Modified footprint -- Modify 固定孔 Size as SMT request





Del R578 direct on PV

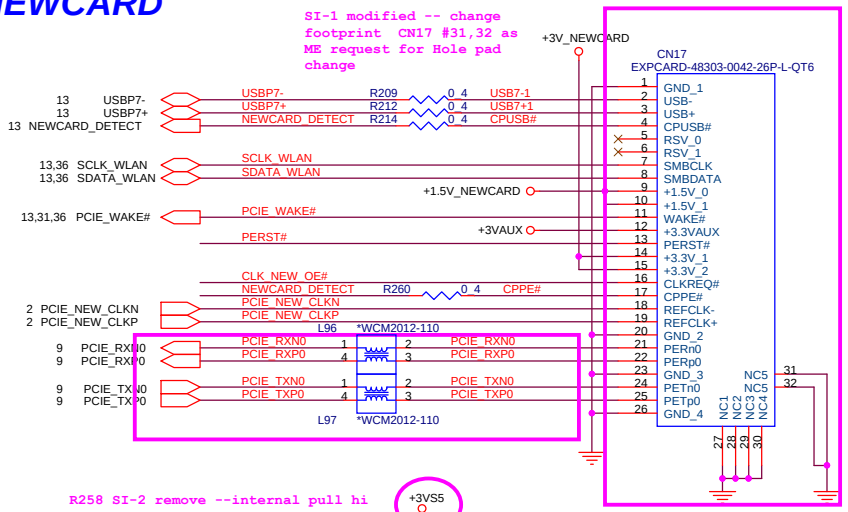


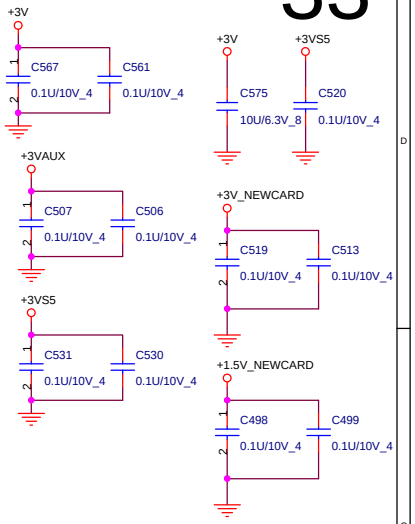
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

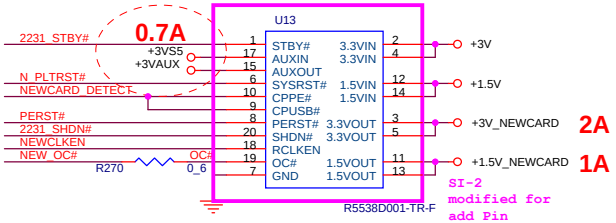
33

SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change





R258 SI-2 remove --internal pull hi



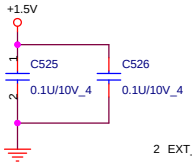
2A

1A

Del R790, R791, R792, R793 for RF on PV

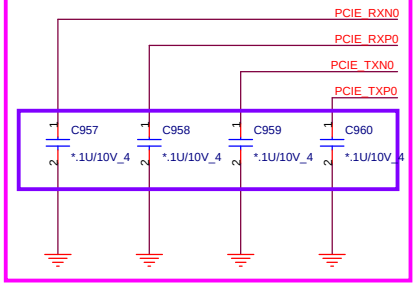
SI-2 modified for add Pin 21~25 as U25 Thermal pad tied to Gnd

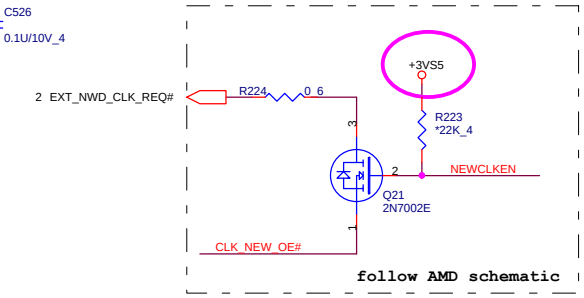
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

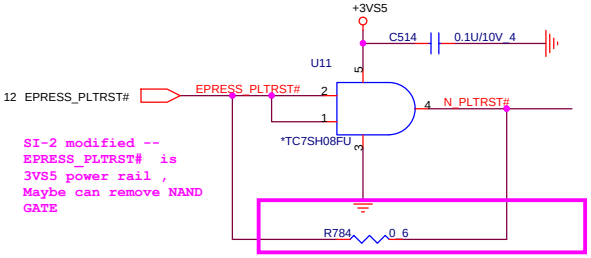


SI-2

For HP request to reserve







SI-2 modified -- EPRESS_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

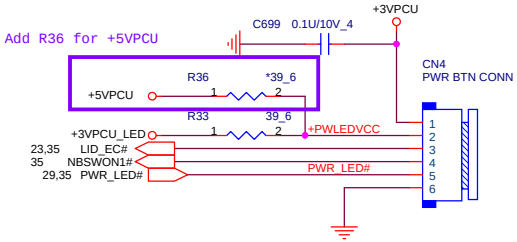
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/SATA ODD/SATA HDD	1A

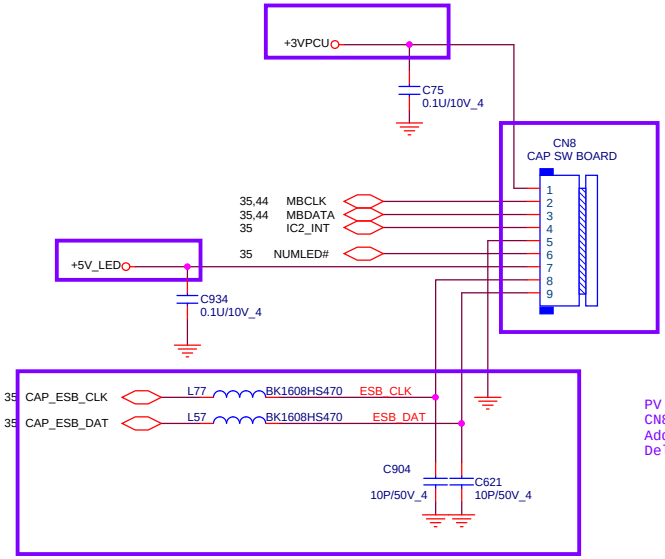
Date: Tuesday, February 19, 2008 Sheet 33 of 45

POWER BUTTON CONNECT



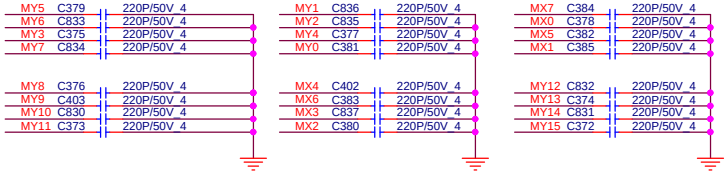
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

CAP SW CONNECT



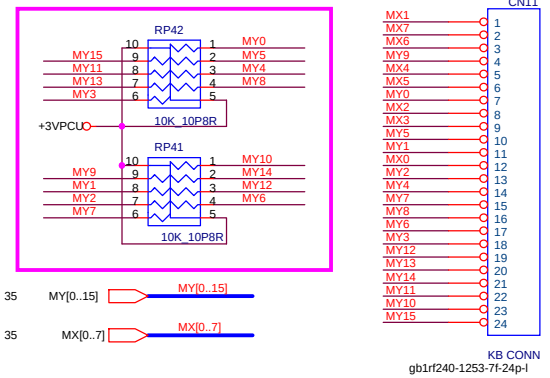
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103



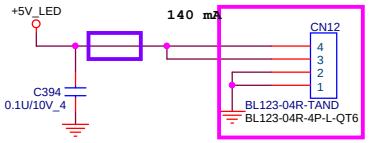
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



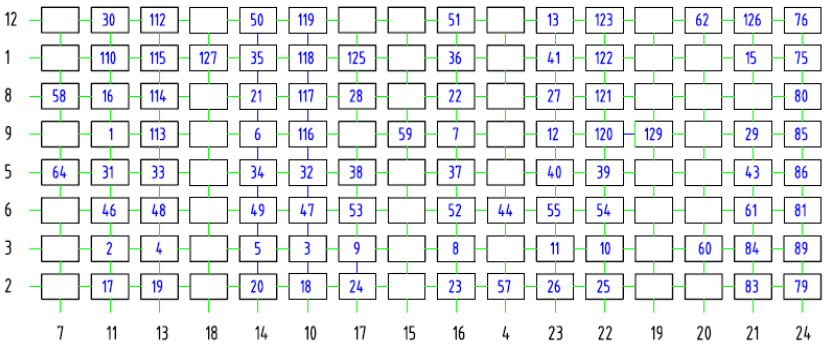
Del R770 on PV

SI-2 Modified 12/27



1.LEDVCC
2.LEDVCC
3. NC
4. GND

SI-2 Modified



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

Date: Tuesday, February 19, 2008 Sheet 34 of 45

Change U9 layout footprint
to LQFP128-16X16-4-AA1

U9

KB3926

For KB3926 C version

SI-2 for fix cpu vcore

SI-2 Modified for hp request

Del R249 on PV

Battery charge/discharge
Cap button

VGA thermal
system thermal

Pin 17 (GPIO0B) ==> assigned for ESB_CLK / Pull high 4.7K
Pin 18 (GPIO0C) ==> assigned for ESB_DAT / Pull high 4.7K

LAN_RESET# move to Pin 25
pin 18 (SWI#1) move to Pin 31

reserved for H/W CIR

Del R256 for TP on PV

SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

change D11 type for PV

UMA BOM missing

64.9K -->65W
33.7K -->90W

SI-2 Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

SI-2 modified for avoid AD-_ID noise

SB internal pull Hi 10k to 3v_s5

Change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

close conn

TOUCH PAD CONNECTOR

Del L86 on PV

25 mils

PCB footprint
BL121-12R-12P-L-QT6

PA

Update SW2, SW4, SW6 P/N on PV

TOUCH PAD ON/OFF

TOUCH PAD L/R

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

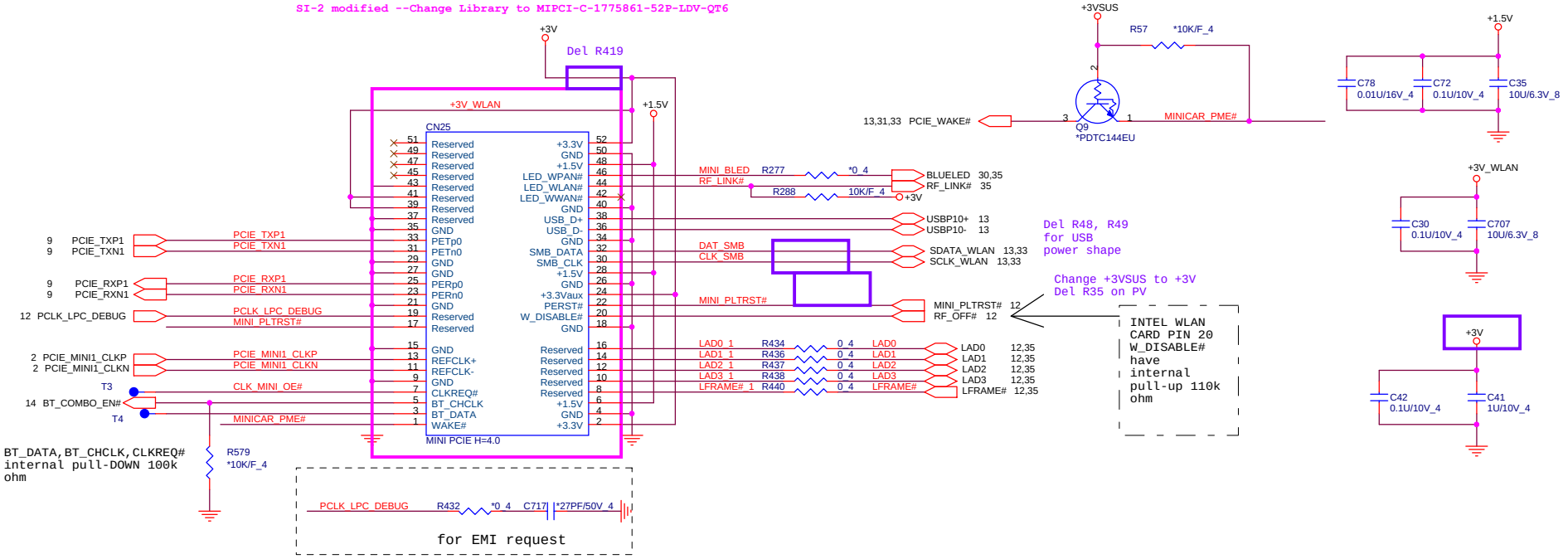
SST AKE5GFK0Z09 **1M byte SPI BIOS**
WINBOND AKE3GFP0N08
PME AKE3GZP0500
EON AKE3GZP0Q00

CS36492FB17 RES CHIP 64.9K 1/16W +-1%(0402)
CS33322FB13 RES CHIP 33.2K 1/16W +-1% (0402)

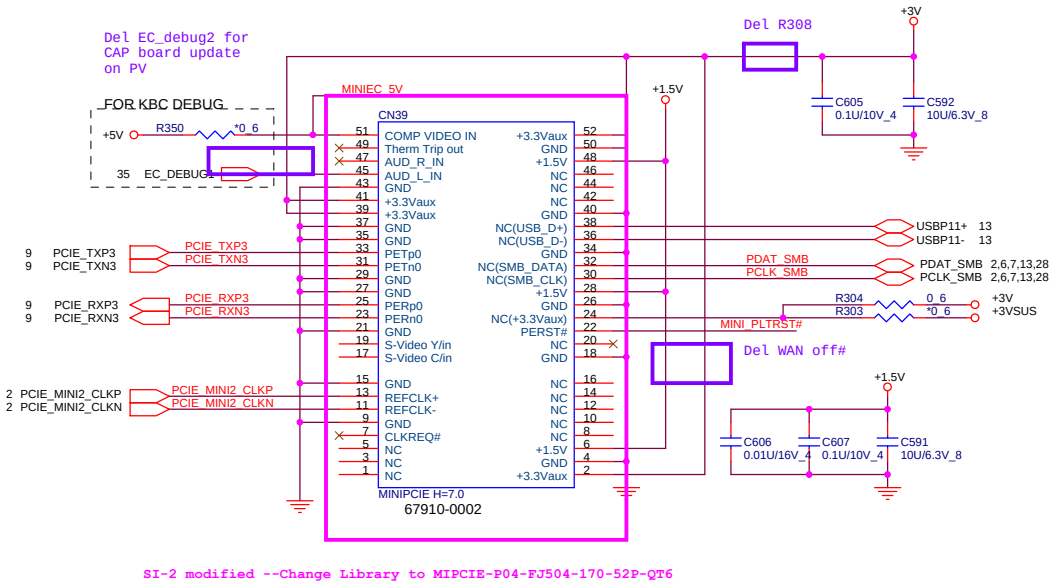
PROJECT :	QT8
Quanta Computer Inc.	
Size: Custom	Document Number: KB3926/ROM/TP
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 35 of 45

NB5/RD5

Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 TV tuner card

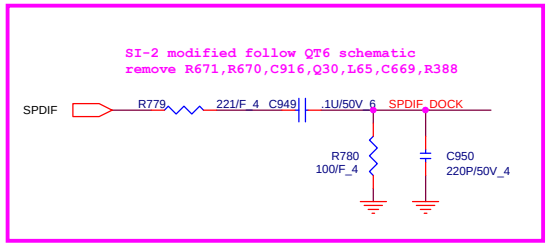


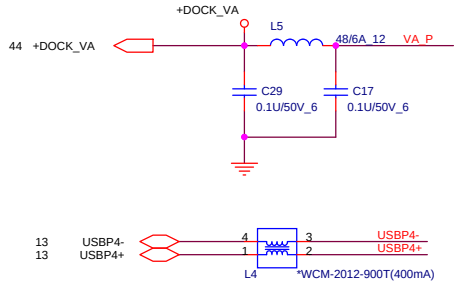
PROJECT :	QT8
	Quanta Computer Inc.
Size	Custom
Document Number	Mini CARD X 3
Rev	1A
Date:	Tuesday, February 19, 2008
Sheet	36 of 45

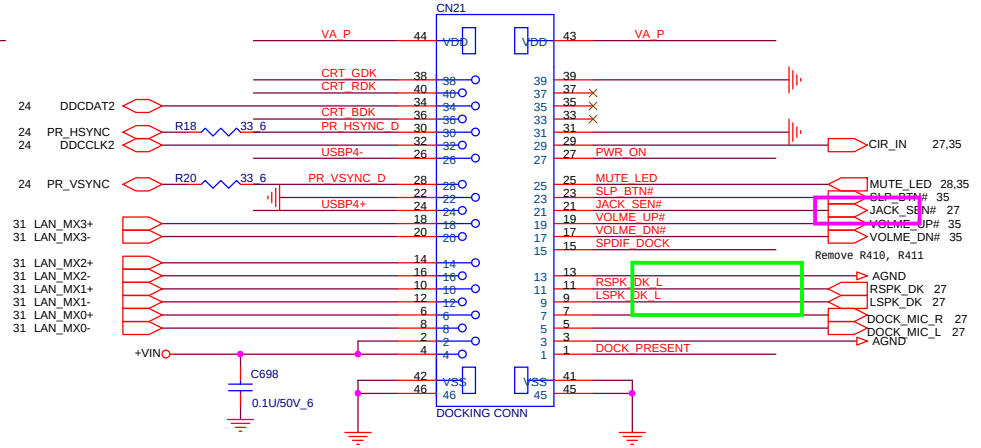
NB5/RD5

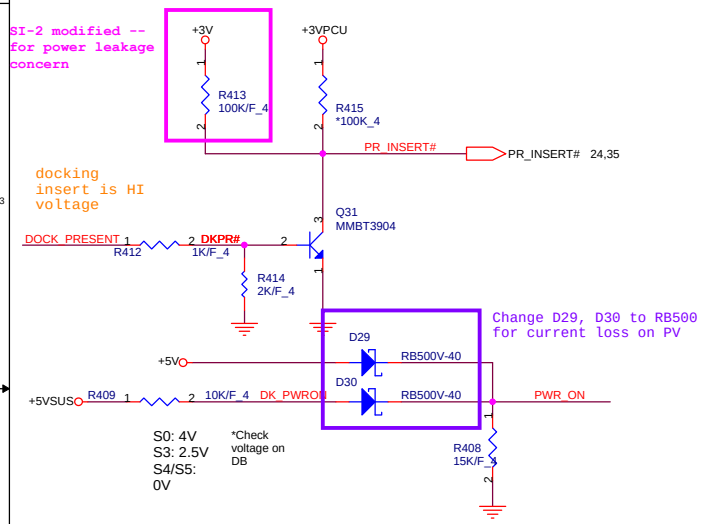
CABLE DOCK

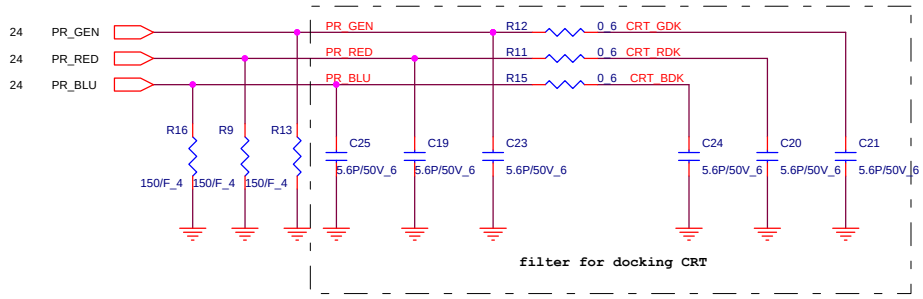
support 6A 200mils
CX000480005



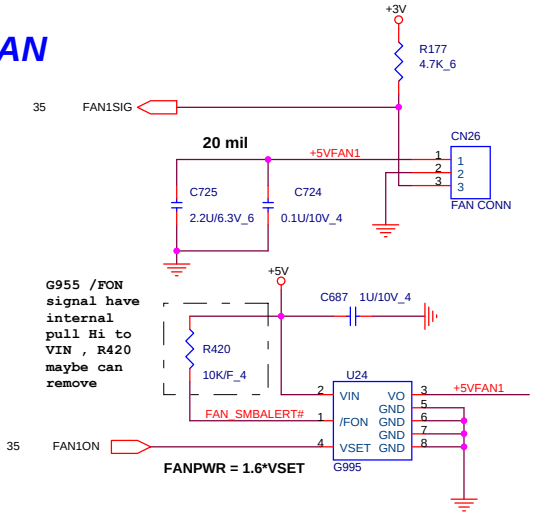


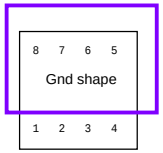




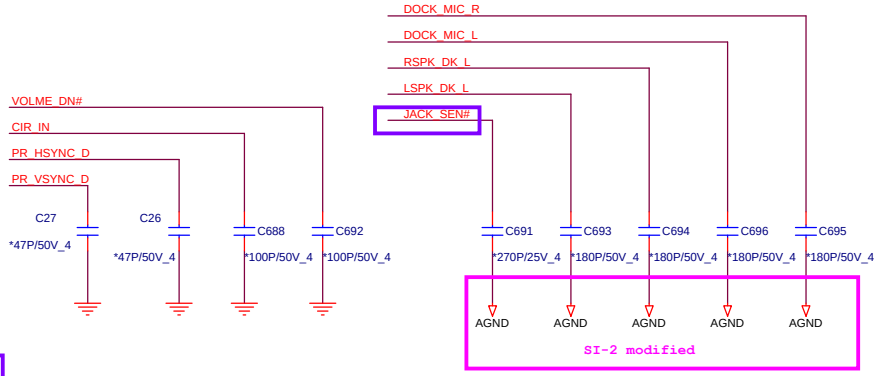


CPU FAN





G995 layout notice



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

Date: Tuesday, February 19, 2008 Sheet 37 of 45

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,18,20,23,24,25,26,27,28,29,30,31,33,35,36,37,39,43

+5VPCU 27,28,34,35,39,40,41,42,43
+3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
+3VSUS 13,25,30,36,39,41,43
+3VS5 5,7,12,13,14,15,16,23,26,33,43
+5VSUS 23,30,35,37,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

SI-1 Modified -ECAP6_3X6_1-7_2-QT8

Rds(on) 15m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Del PR159 for TP on PV

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

+3V
6.76A
S0-S1

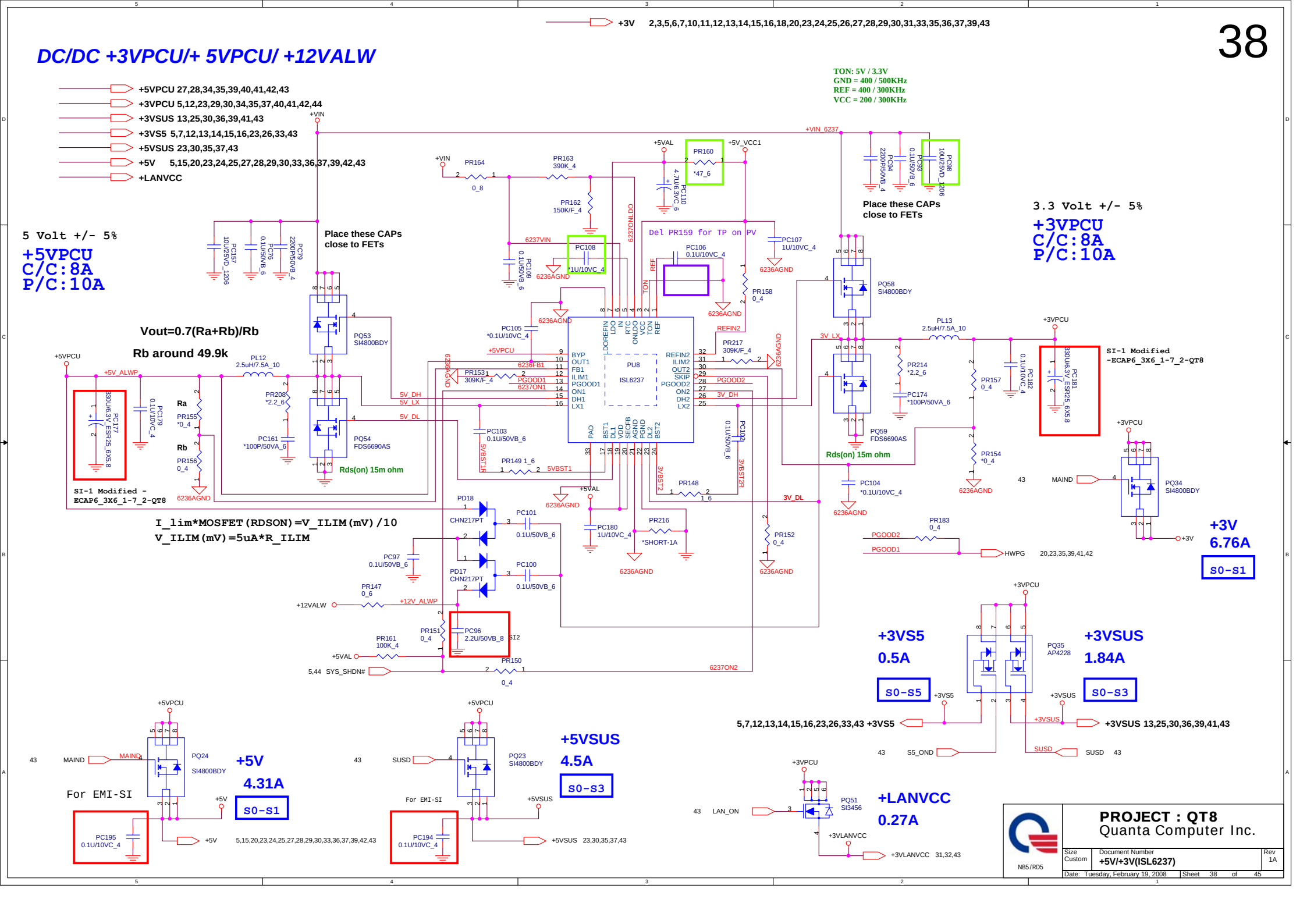
+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

+5VSUS
4.5A
S0-S3

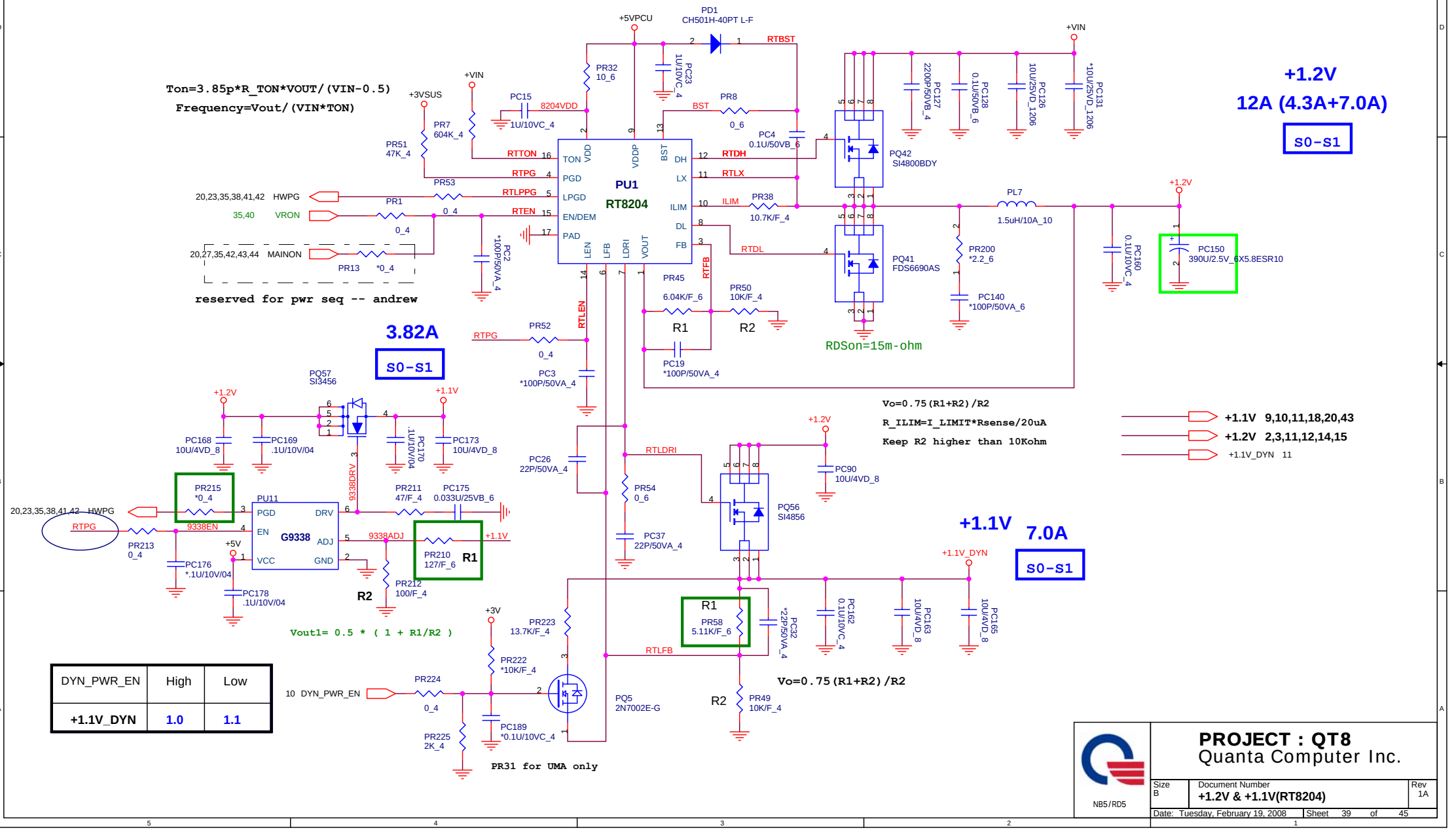
+LANVCC
0.27A



PROJECT : QT8		
Quanta Computer Inc.		
Size: Custom	Document Number: +5V/+3V(ISL6237)	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 38 of 45	

NB5/RD5

+1.1V & +1.2V

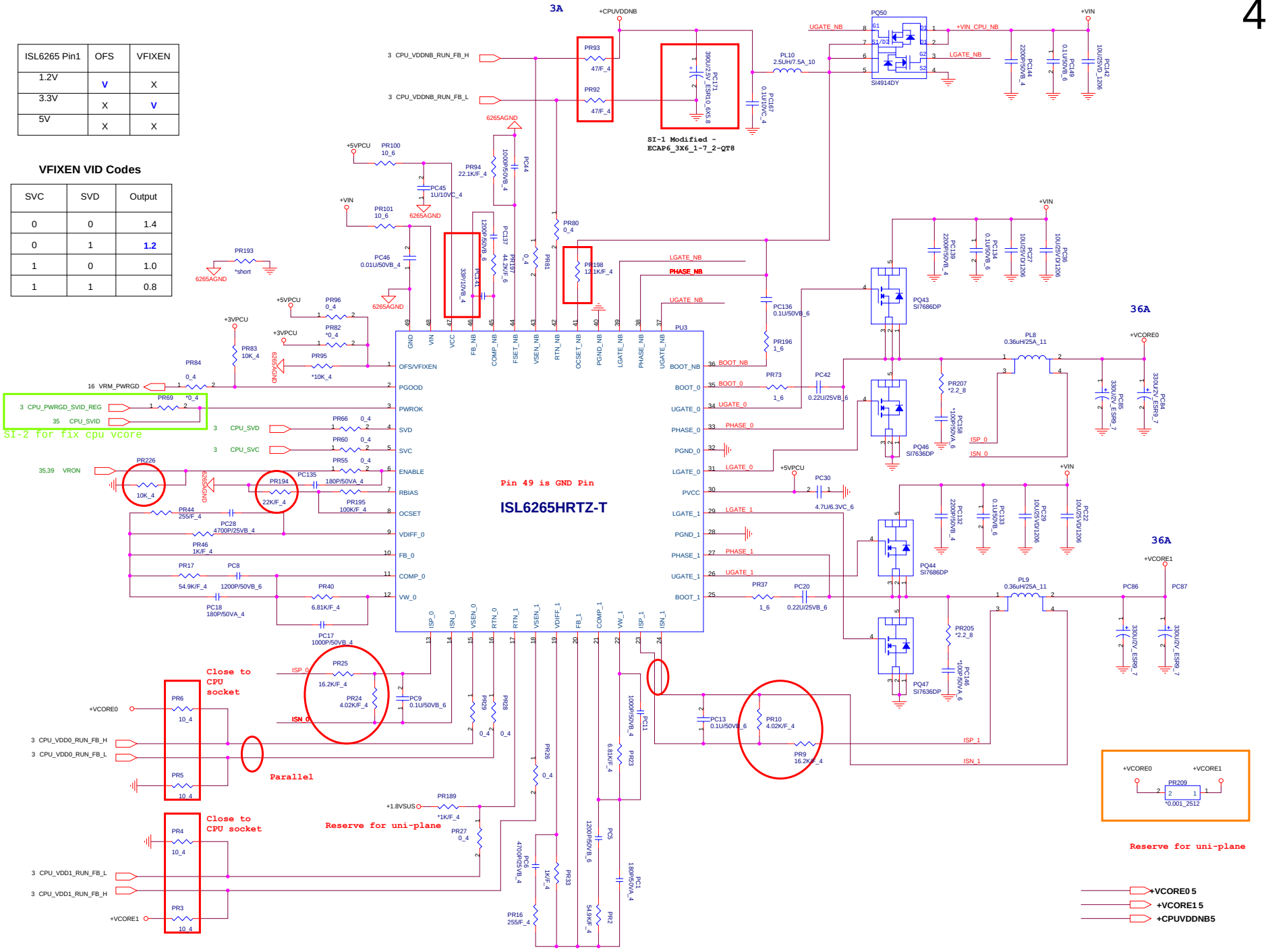


DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_CORE(ISL6265)	1A

NB5/RD5

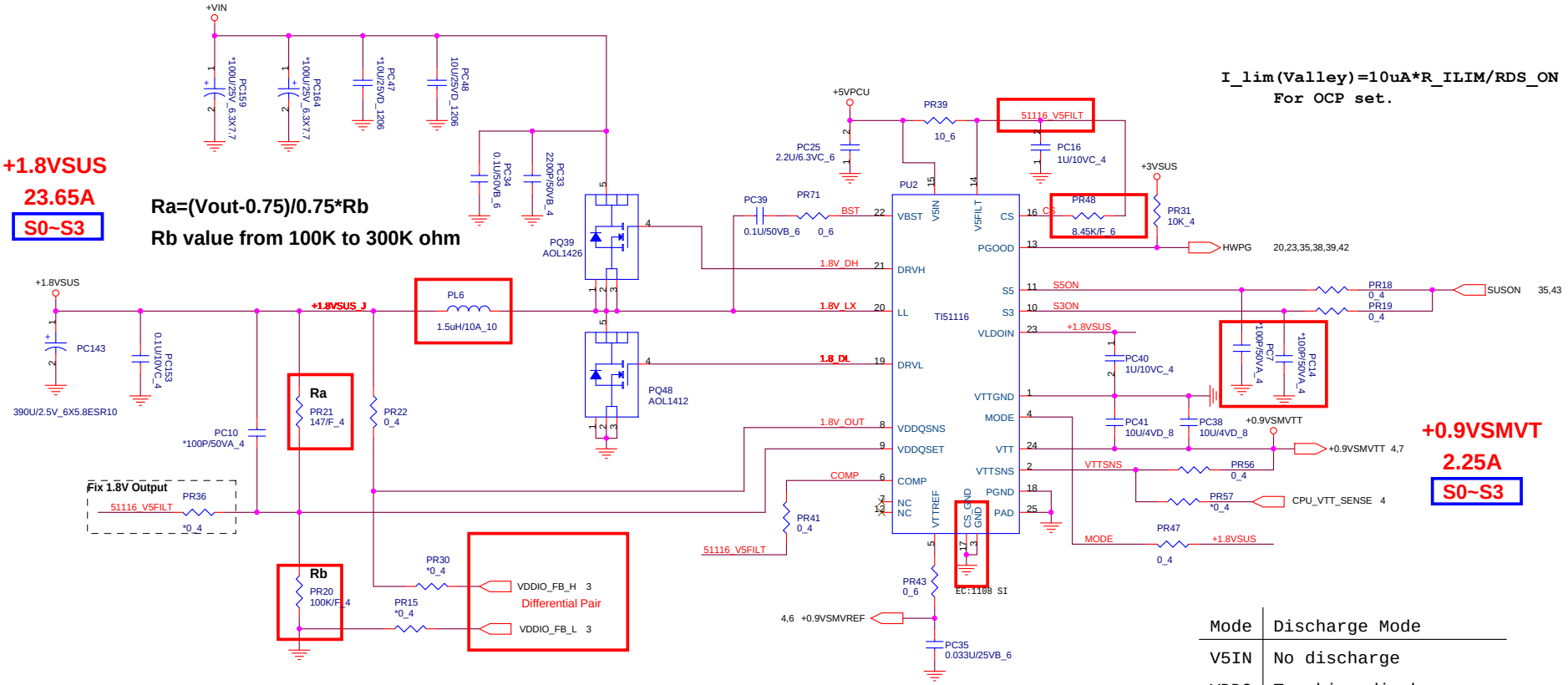
Date: Tuesday, February 19, 2008 Sheet 40 of 45

+2.5V 3
+1.8VSUS 3,4,5,6,7,40,42,43

+1.8VSUS
23.65A
S0~S3

Ra=(Vout-0.75)/0.75*Rb
Rb value from 100K to 300K ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

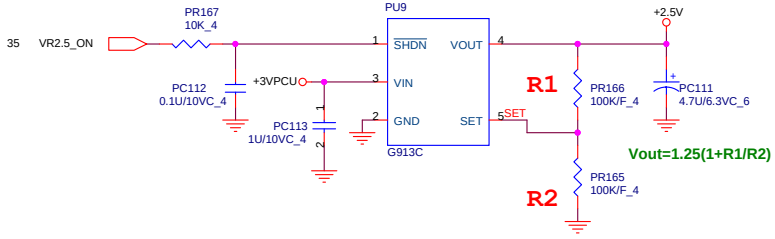


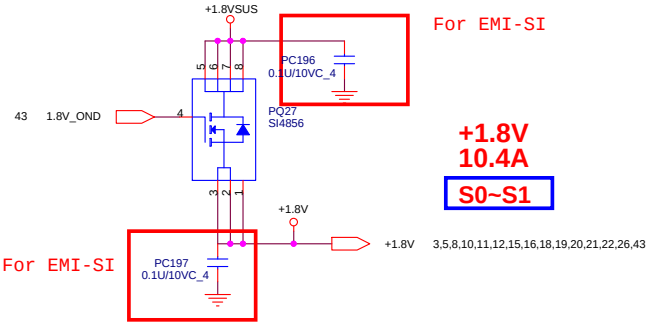
+0.9VSMVT
2.25A
S0~S3

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

+2.5V
0.25A
S0~S1

Close to CPU
SI power





+1.8V
10.4A
S0~S1

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)
I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

Discrete:SI4856
UMA:SI4800

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NB5/RD5

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A
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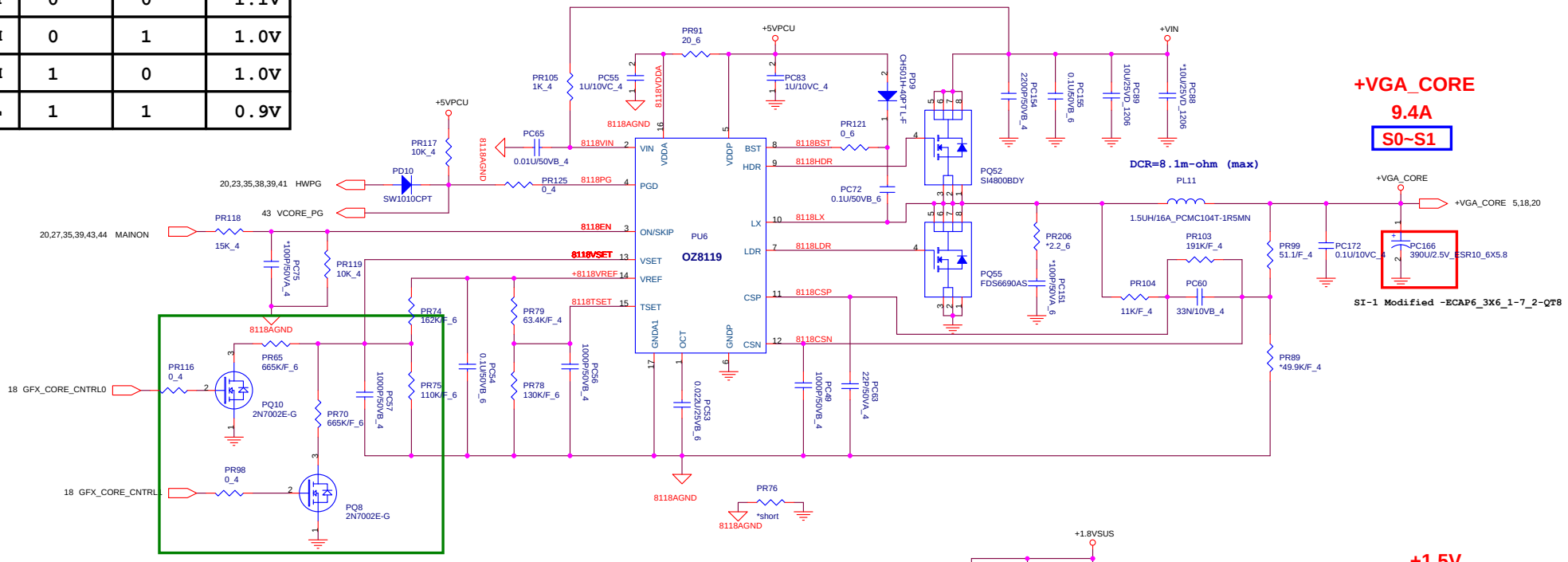
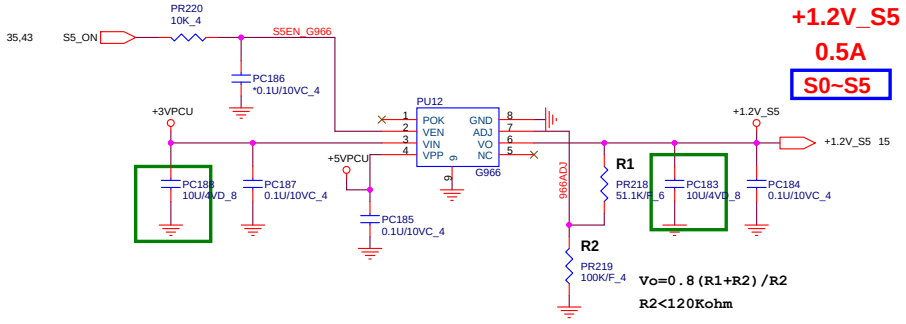
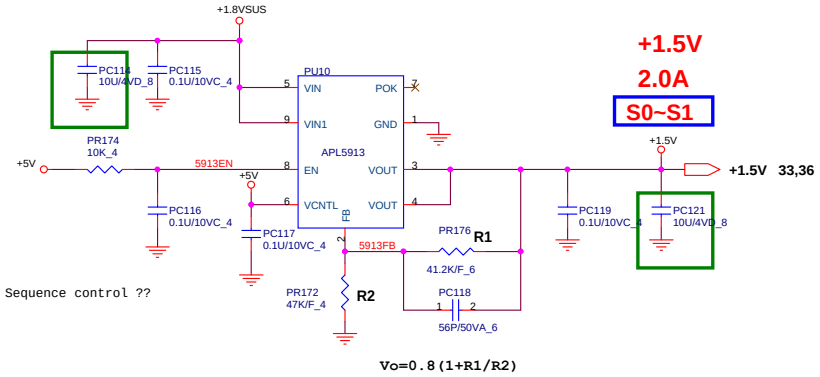
ATI M82-SE

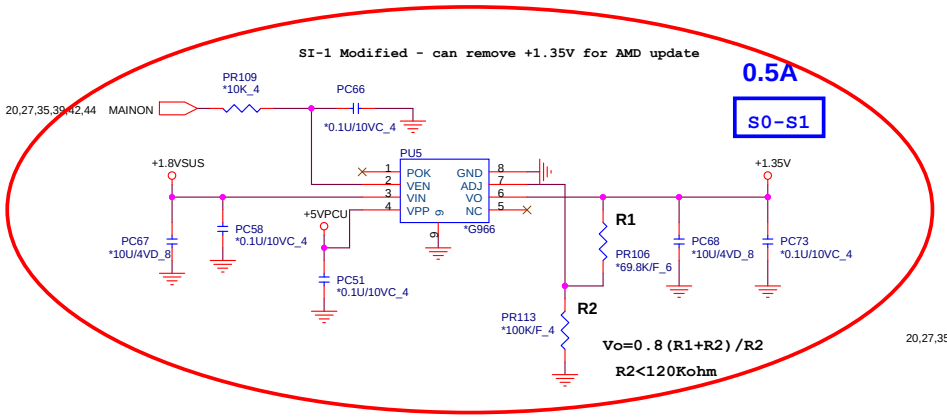
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

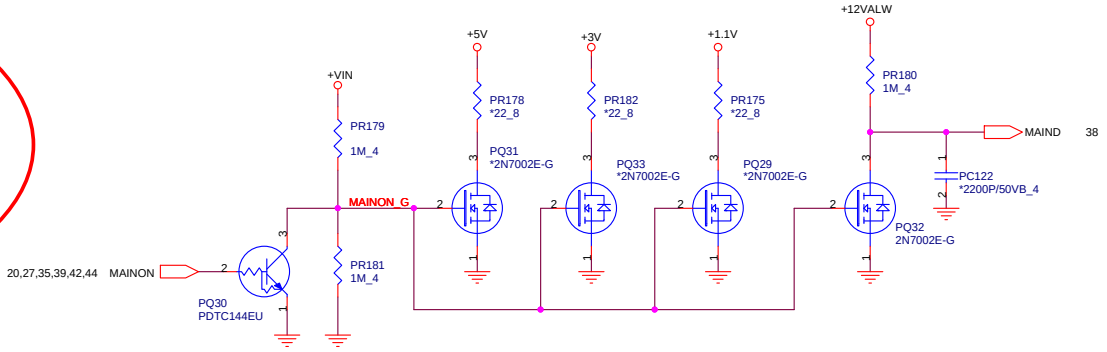
+VGA_CORE5,18,20
+1.2V_S5 15
+1.5V 33,36

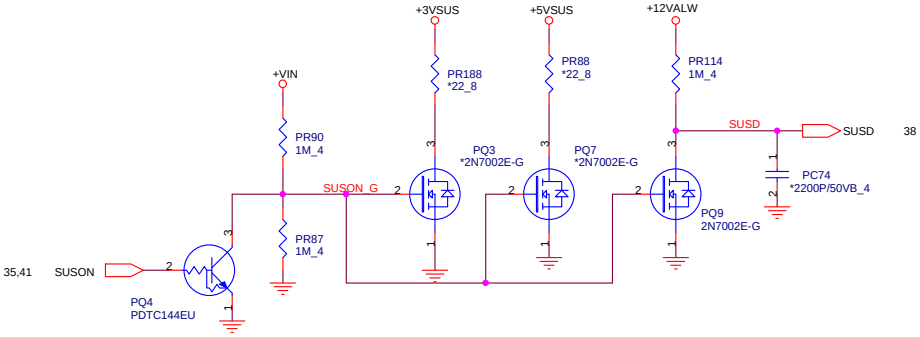


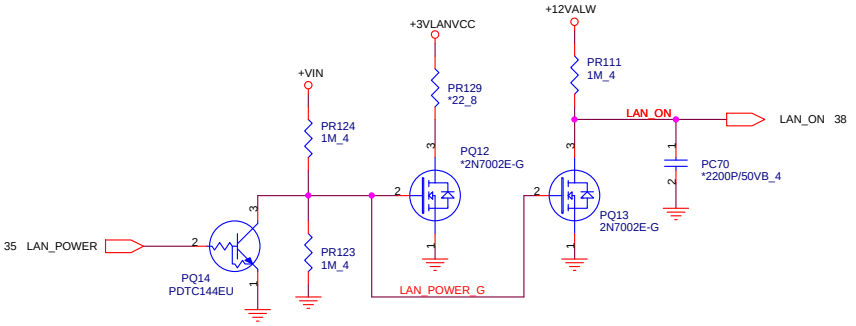




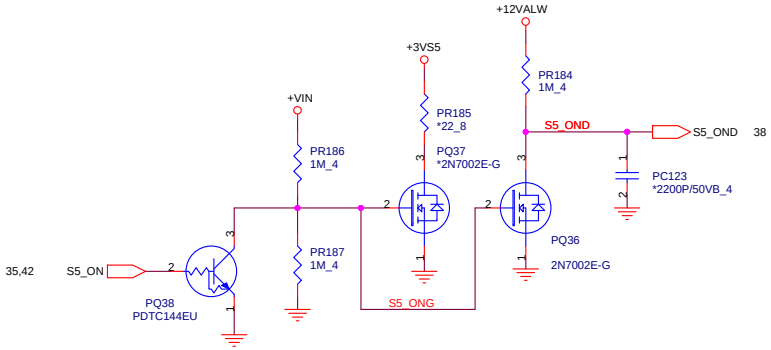


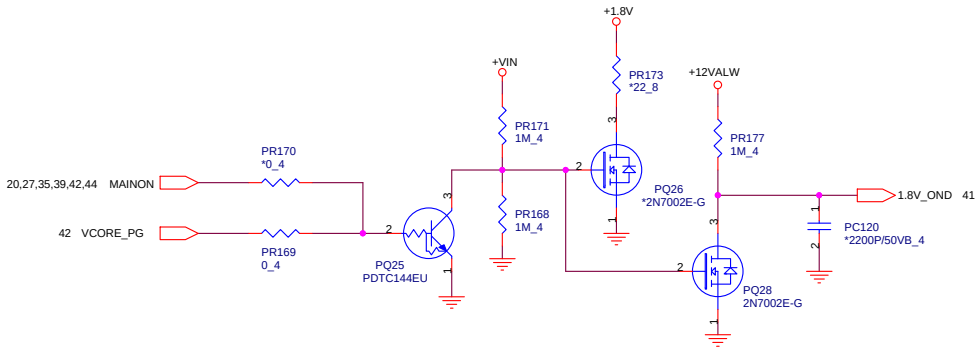






For Discrete Only





N85/RD5	PROJECT : QT8 Quanta Computer Inc.	
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TOP DC_JACK
65W/90W

ISL6251A

Close to AC soft start MOSFET

SI-2 modified -- EMI

ONLY for 3S battery pack

ADP TYPE	PR72 Value	P/N
65W	102K/F	CS41022FB19
90W	7.5K/F	CS27502FB11

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Quanta Computer Inc.

Size: Custom | Document Number: CHARGER (ISL6251) | Rev: 1A
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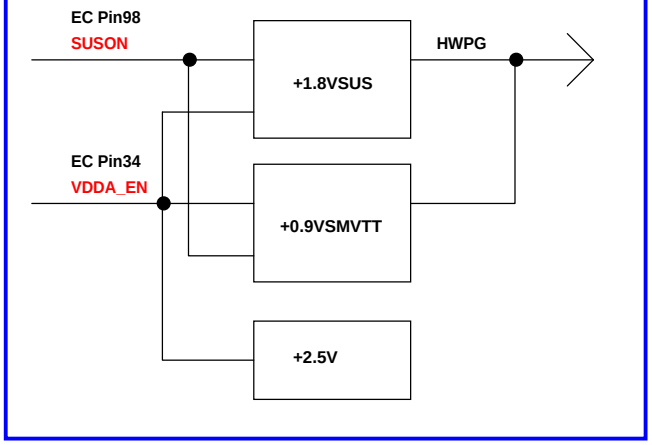
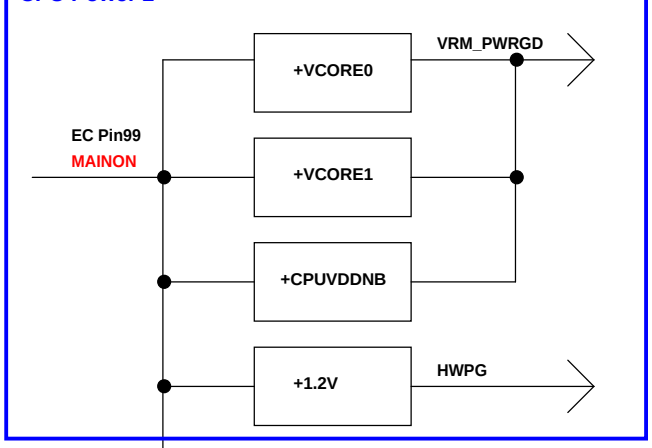
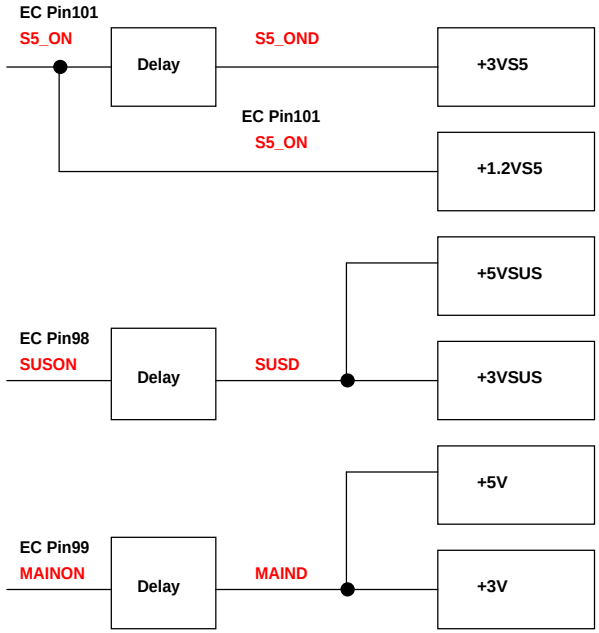
NB5/RD5

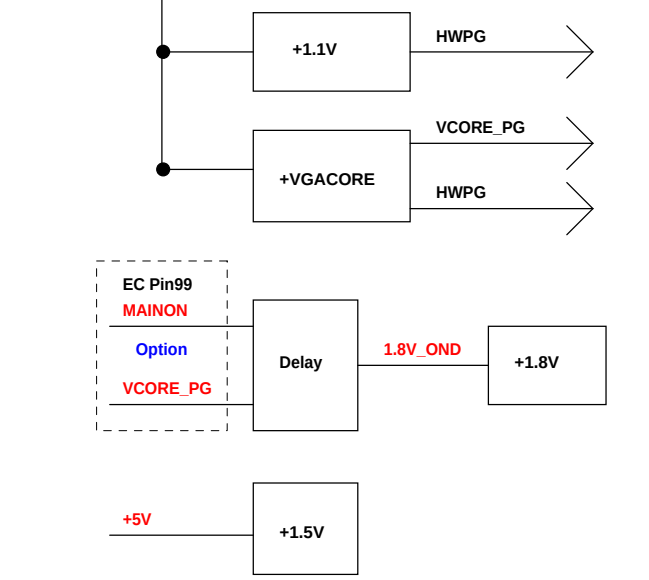
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD5

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Size	Document Number	Rev
Custom	Power control	1A

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