

# Wistron Confidential

## MV-3

2008/08/20

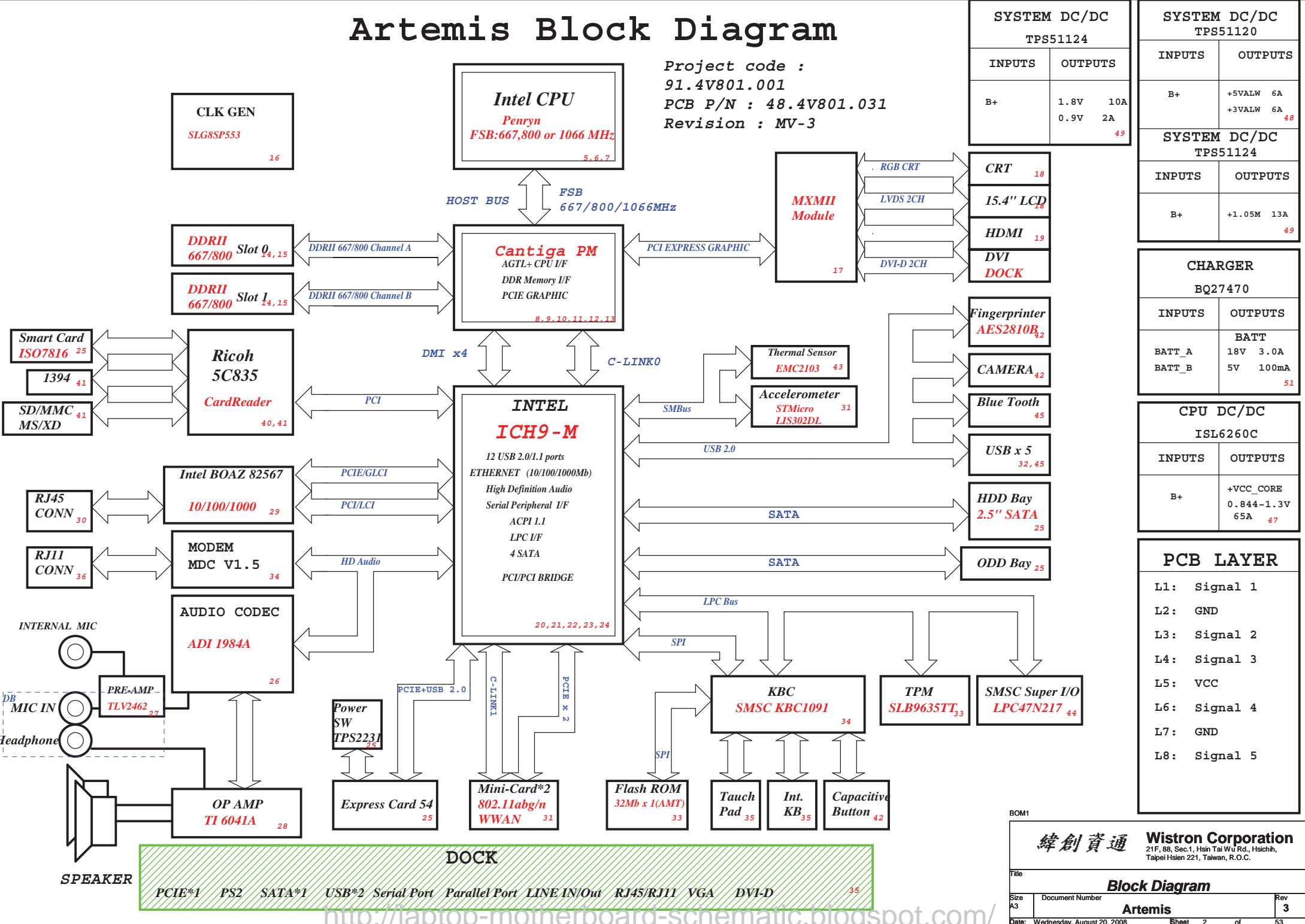
REV :MV-03

BOM1

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Title			
<b>VOX</b>			
Size A3	Document Number	<b>Artemis</b>	Rev <b>3</b>
Date: Wednesday, August 20, 2008		Sheet 1	of 53

# Artemis Block Diagram

Project code :  
91.4V801.001  
PCB P/N : 48.4V801.031  
Revision : MV-3



SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	1.8V 10A 0.9V 2A

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 6A +3VALW 6A

SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	+1.05M 13A

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA

CPU DC/DC ISL6260C	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 65A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

BOM1

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Title: **Block Diagram**

Size A3 Document Number: **Artemis** Rev: **3**

Date: Wednesday, August 20, 2008 Sheet 2 of 53

5

4

3

2

1

D

D

C

C

B

B

A

A

VOX

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<b>Change Notes List</b>		
Size A3	Document Number <b>Artemis</b>	Rev <b>3</b>
Date: Wednesday, August 20, 2008	Sheet 1	of 3

### Voltage Rails

○ MEANS ON    × MEANS OFF

power plane State	+B +3VL LD05	+5VALW +3VALW	+1.5V +5V +0.75V	+5VS +3VS +1.5VS +CPU CORE +VCCP	+3VM +1.05VM	CLOCK
S0	○	○	○	○	○	○
S3/M1	○	○	○	×	○	○
S3	○	○	○	×	○	○
S5 S4/AC	○	○	×	×	○	○
S5 S4/Battery only	○	×	×	×	×	×
S5 S4/AC & Battery don't exist	×	×	×	×	×	×

### PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	<del>Floppy Disk</del>
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	USB1
1	USB4
2	EXPRESS SLOT
3	USB5
4	USB2
5	USB3
6	Bluetooth
7	WWAN
8	Fingerprint
9	Dock 1
10	Camera
11	Dock 2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

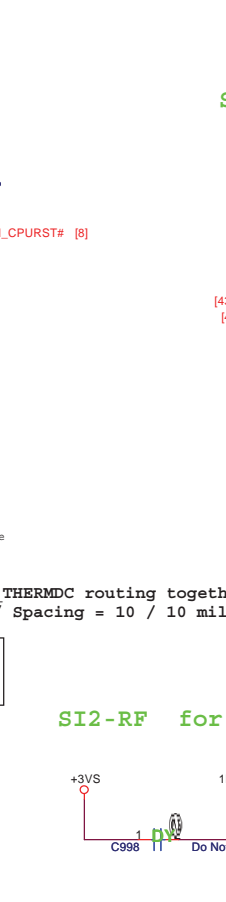
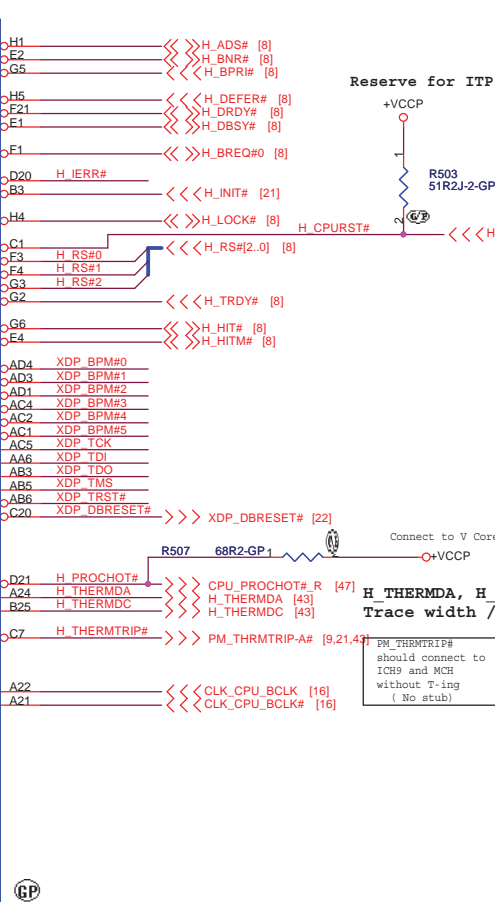
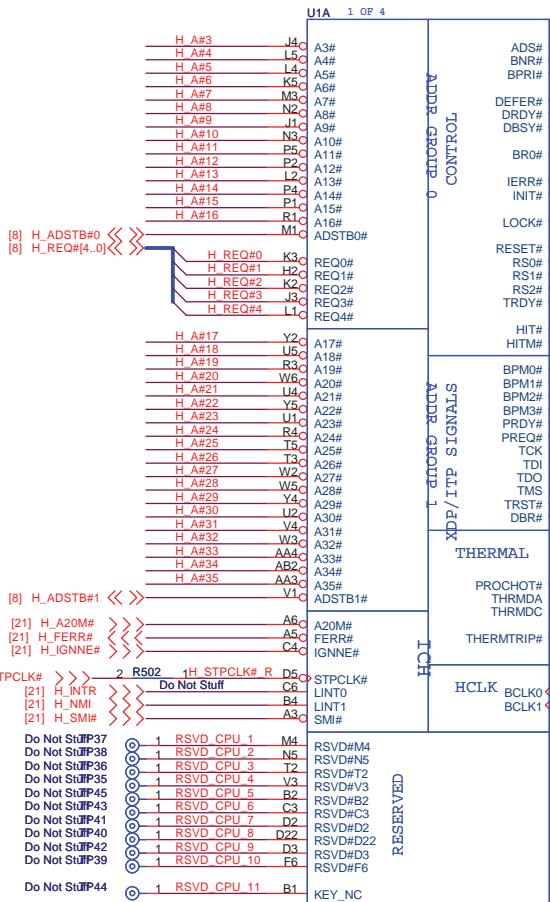
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	<del>Floppy</del>
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0
17	Intel 82801I (ICH9 Family) PCI Express Root Port -27D2 Intel 82801I (ICH9 Family) USB Universal Host Control
18	Intel 82801I (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801I (ICH9 Family) PCI Express Root Port -27D6 Intel 82801I (ICH9 Family) USB Universal Host Control
20	Intel 82801I (ICH9 Family) USB Universal Host Control Intel 82801I (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801I (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control Accelerometer LIS302DL
23	HP Mobile Data Protection Sensor

VOX

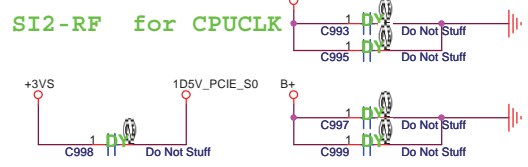
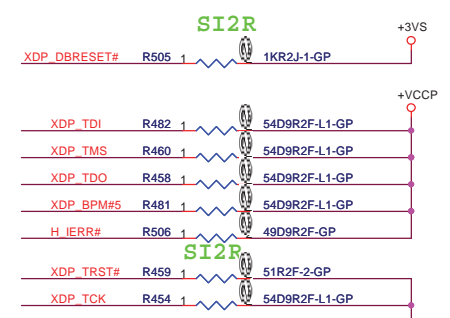
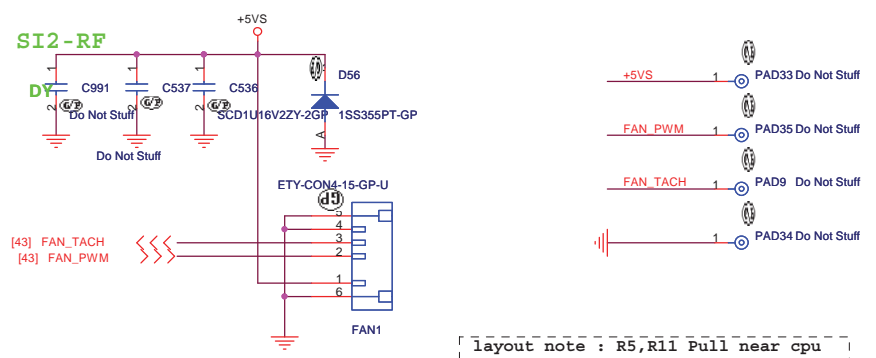
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<b>Artemis List</b>	
Title	
Size A3	Document Number
Date: Wednesday, August 20, 2008	Sheet 4 of 53
Rev	<b>3</b>

# CPU ( 1 of 3 )

5 H\_A#[35..3] <<< H\_A#[35..3]

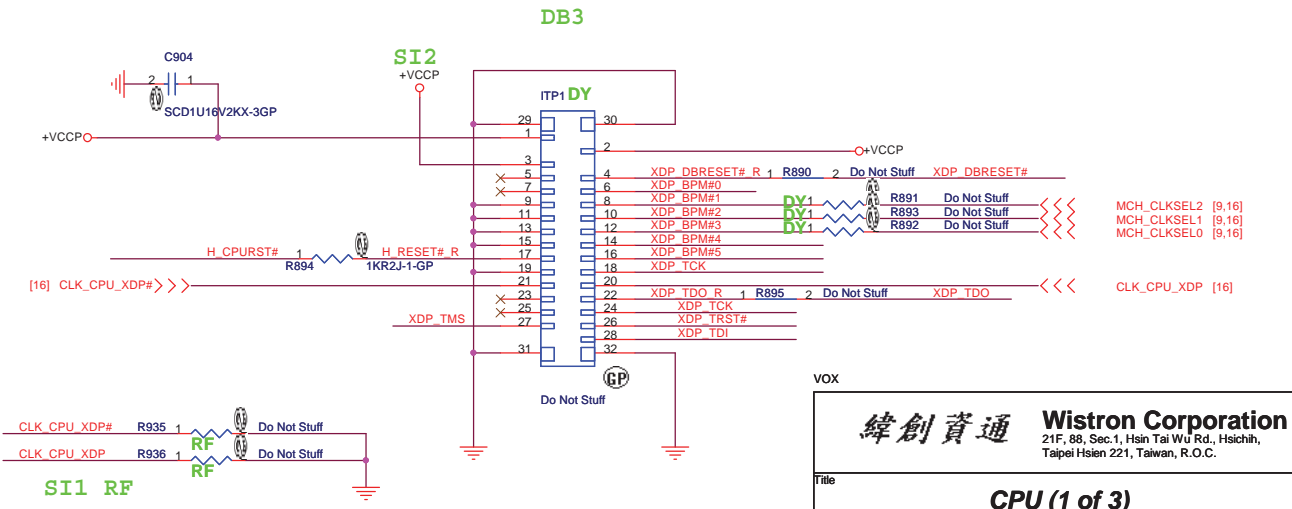
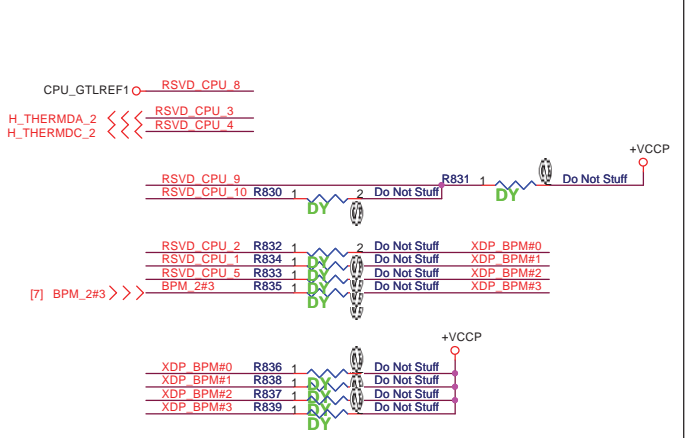


## 4 WIRE PWM Fan Control circuit



BGA479-SKT-8-GP-U3  
62.10053.401

## DB2 Quad Core support

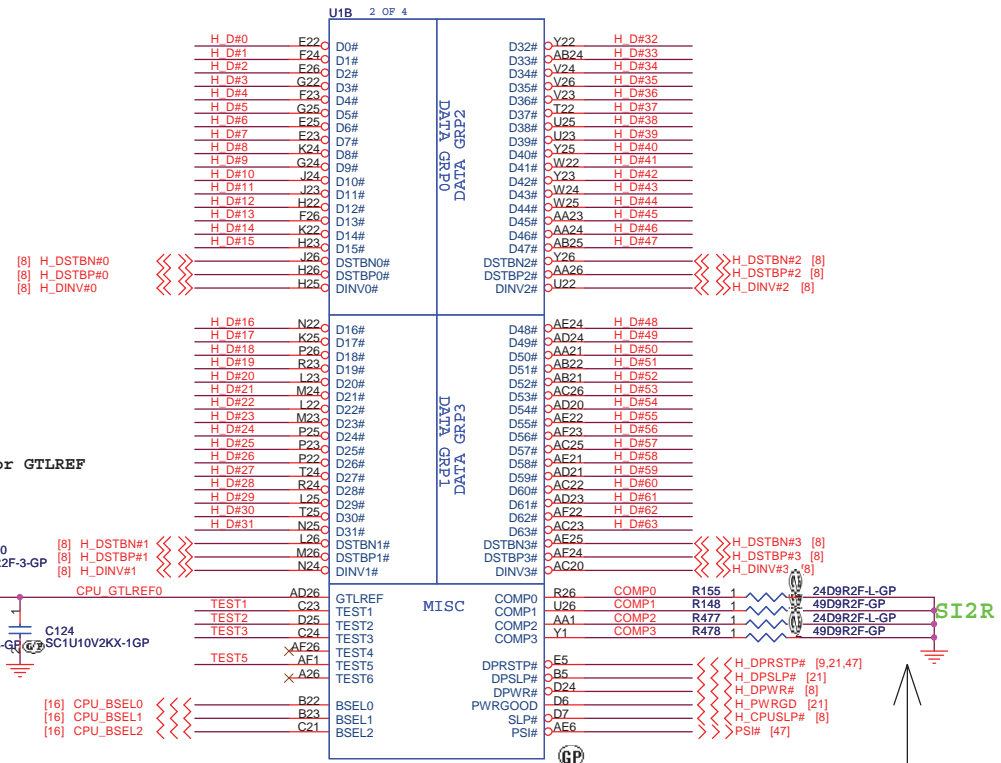


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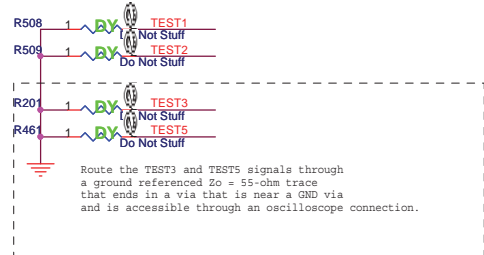
File CPU (1 of 3)  
Size Document Number Rev 3  
Date: Wednesday, August 20, 2008 Sheet 5 of 53

# CPU ( 2 of 3 )

H\_DINV#3..0 << >> H\_DINV#3..0 [8]  
 H\_DSTBN#3..0 << >> H\_DSTBN#3..0 [8]  
 H\_DSTBP#3..0 << >> H\_DSTBP#3..0 [8]  
 H\_D#63..0 << >> H\_D#63..0 [8]

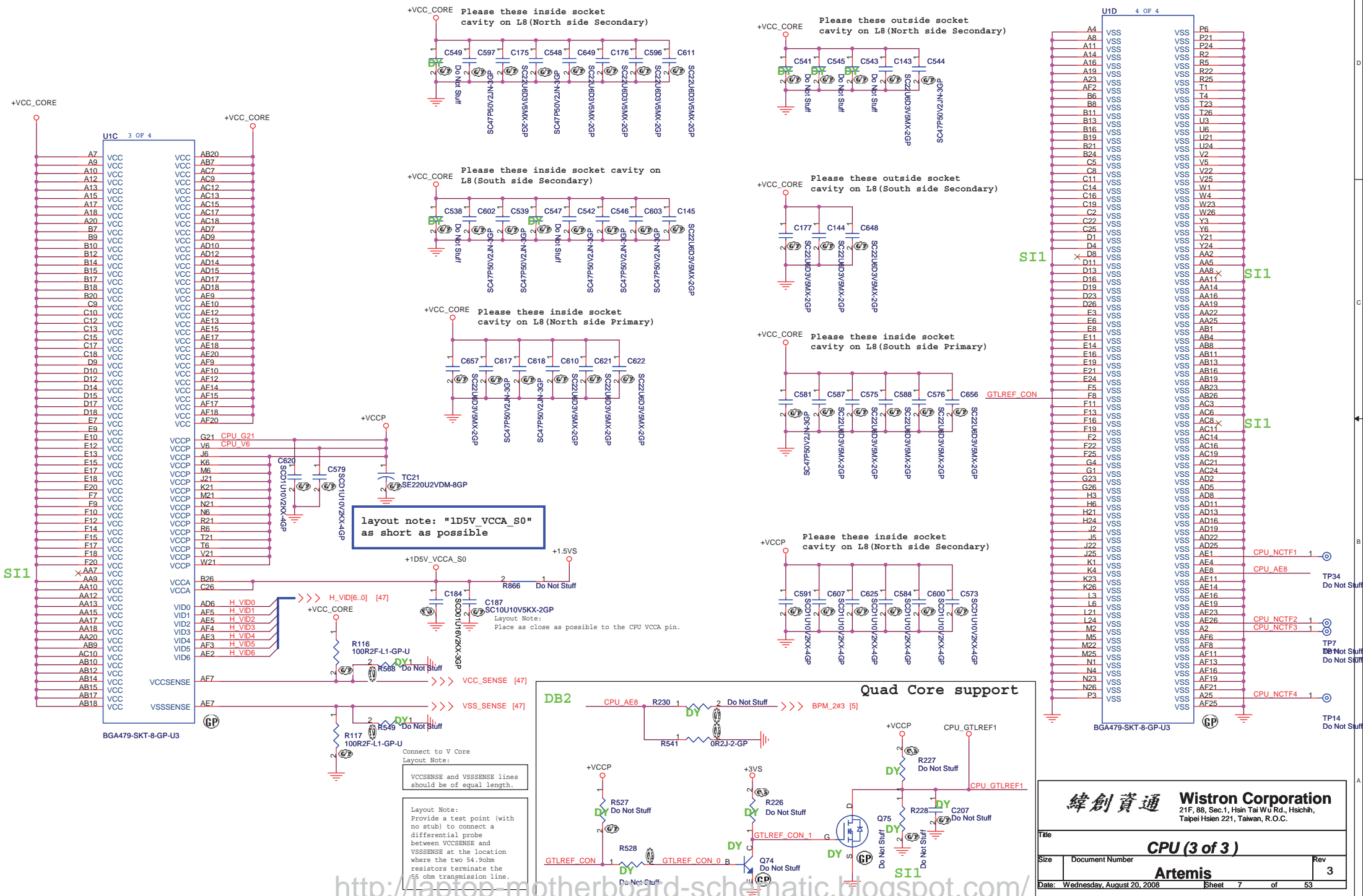


Layout notes  
 Z = 55 Ohm 0.5" MAX for GTLREF



Layout Note:  
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

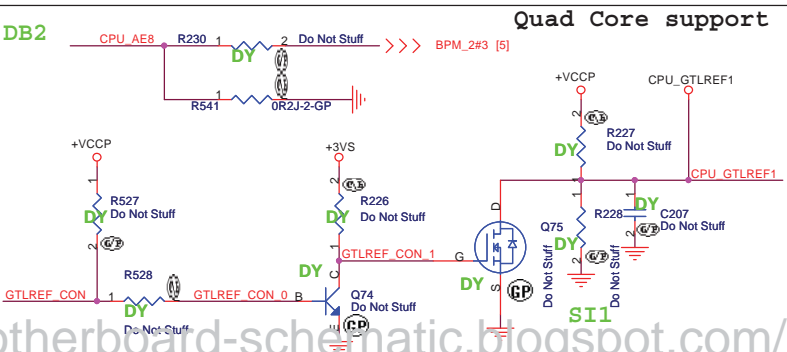
# CPU ( 3 of 3 )



layout note: "1D5V\_VCCA\_S0" as short as possible

Connect to V Core  
Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.  
Layout Note:  
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

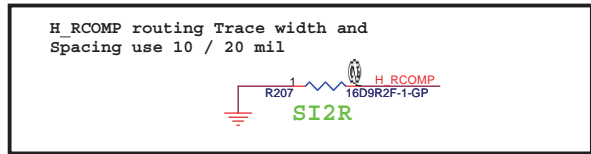
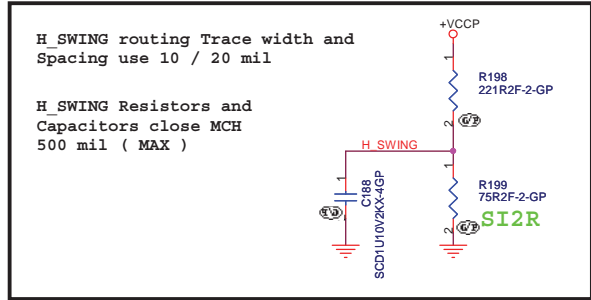


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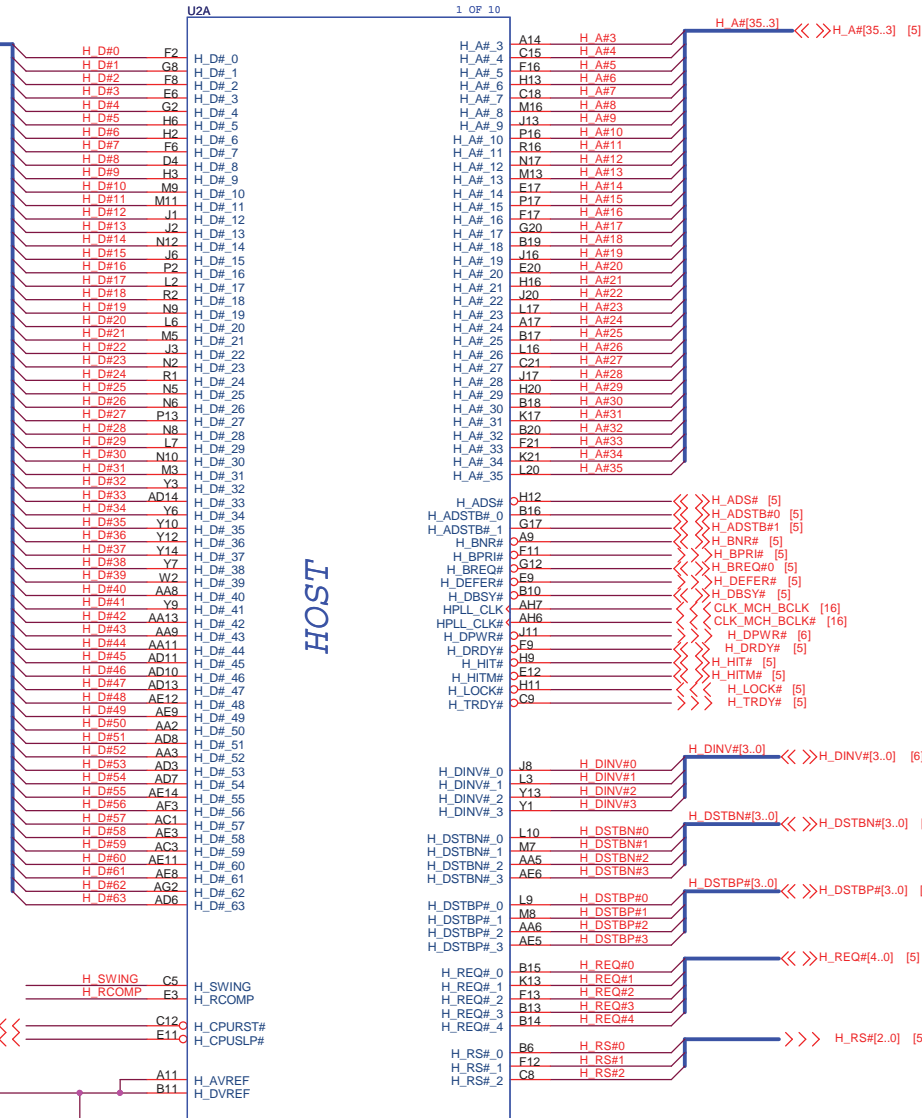
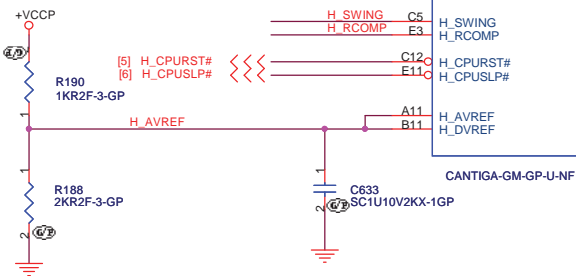
**CPU (3 of 3)**

File	Document Number	Rev
	<b>Artemis</b>	<b>3</b>
Date: Wednesday, August 20, 2008	Sheet 7 of 53	

# NB ( 1 of 6 ) HOST



Place them near to the chip ( < 0.5" )

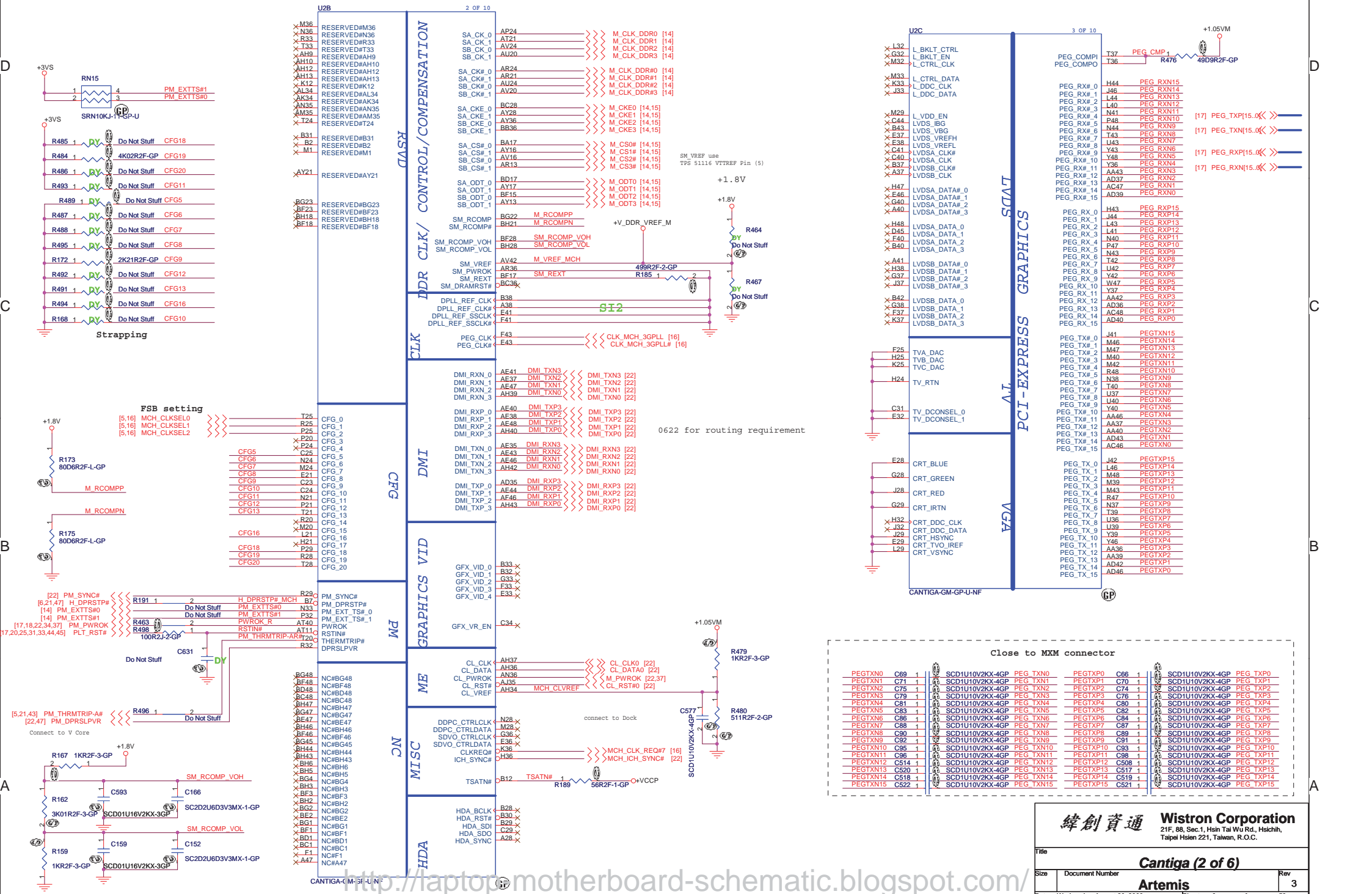


HOST



# NB ( 2 of 6 ) 3 PEG/DMI

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

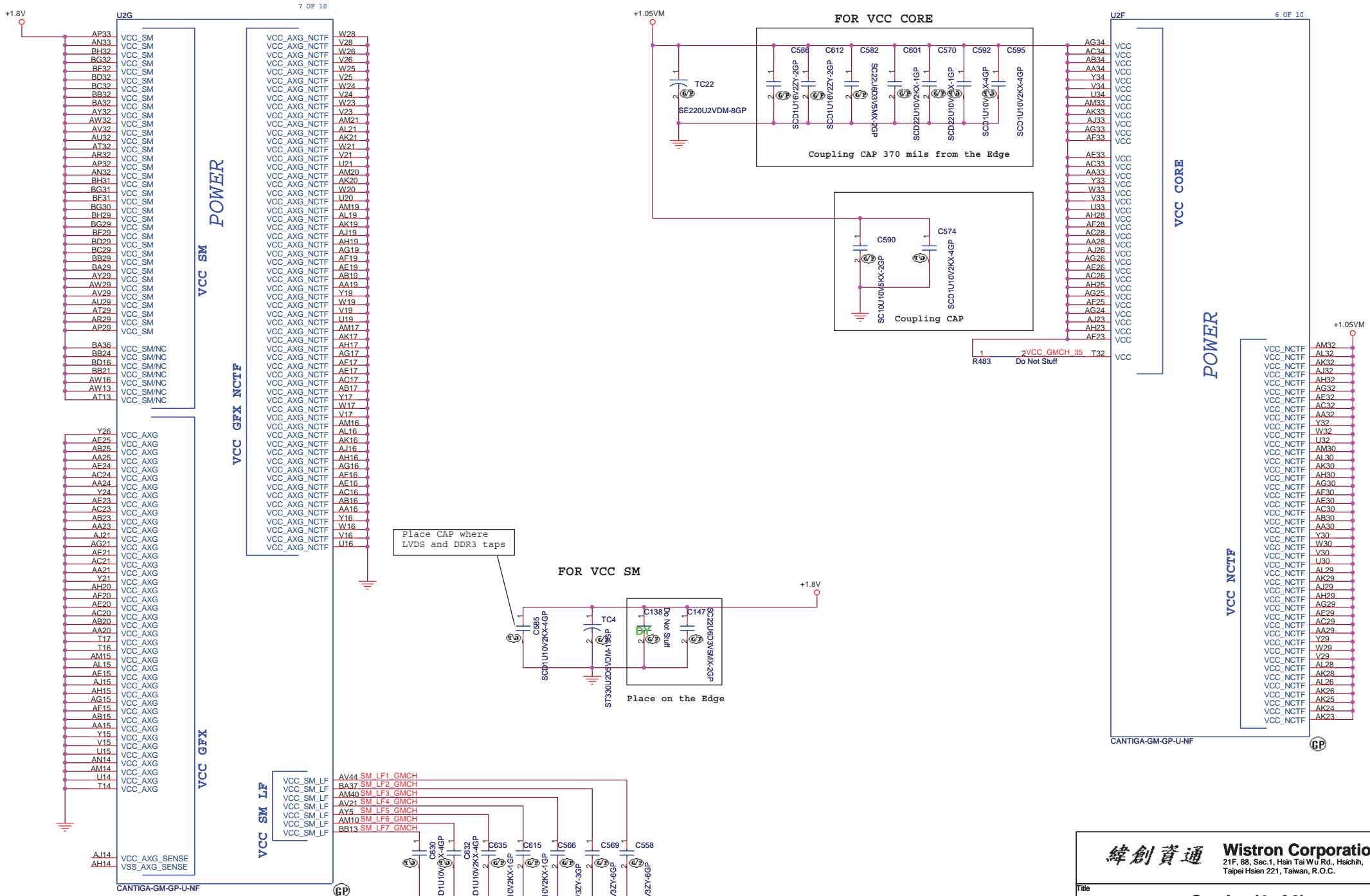


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Title		Cantiga (2 of 6)	
Size	Document Number	Rev	3
Date:	Wednesday, August 20, 2008	Sheet	9 of 53



# NB ( 4 of 6 ) PWR

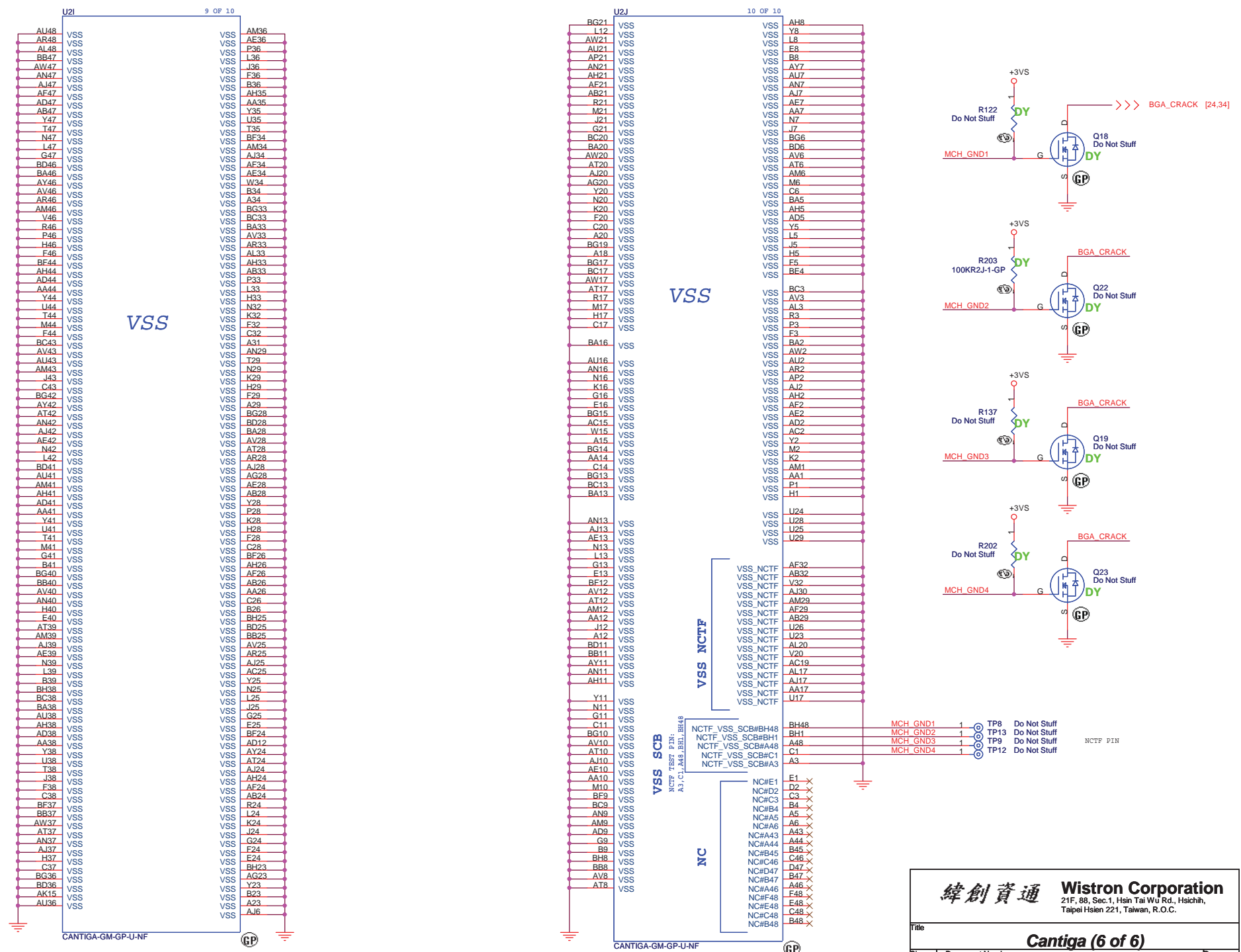


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Title: <b>Cantiga (4 of 6)</b>		
Size	Document Number	Rev
<b>Artemis</b>		<b>3</b>
Date: Wednesday, August 20, 2008	Sheet 11 of	53



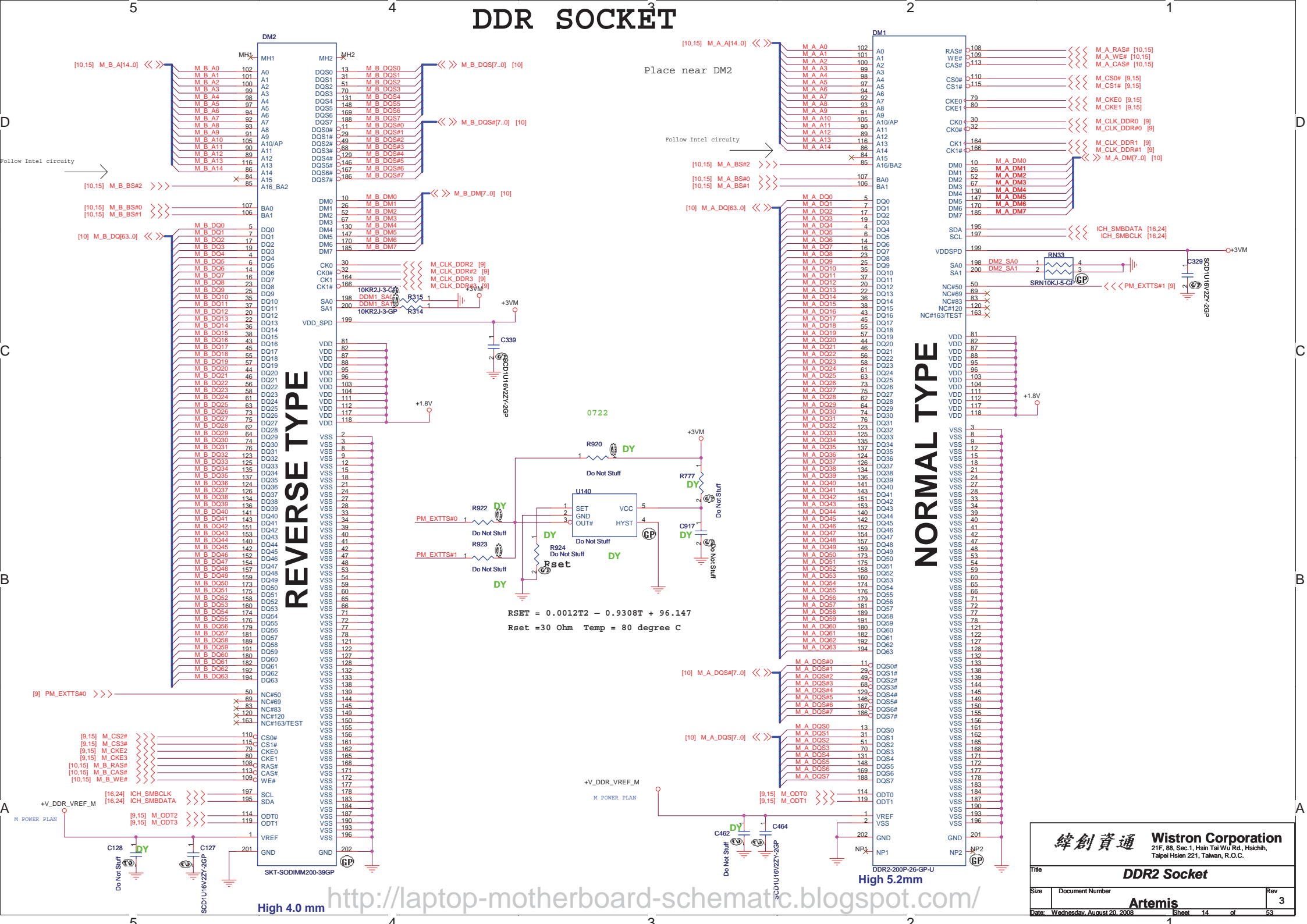
# NB ( 6 of 6 ) GND

07/20 BGA CRACK CIRCUIT



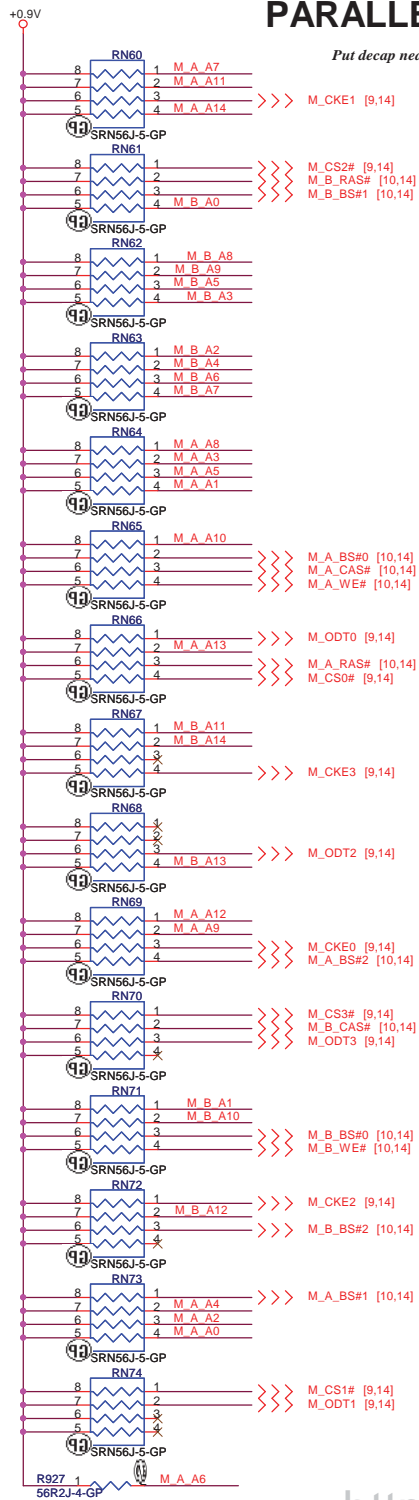
<b>緯創資通 Wistron Corporation</b>	
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Title: <b>Cantiga (6 of 6)</b>	
Size: Document Number	Rev: <b>3</b>
Date: Wednesday, August 20, 2008 Sheet 13 of 53	

# DDR SOCKET



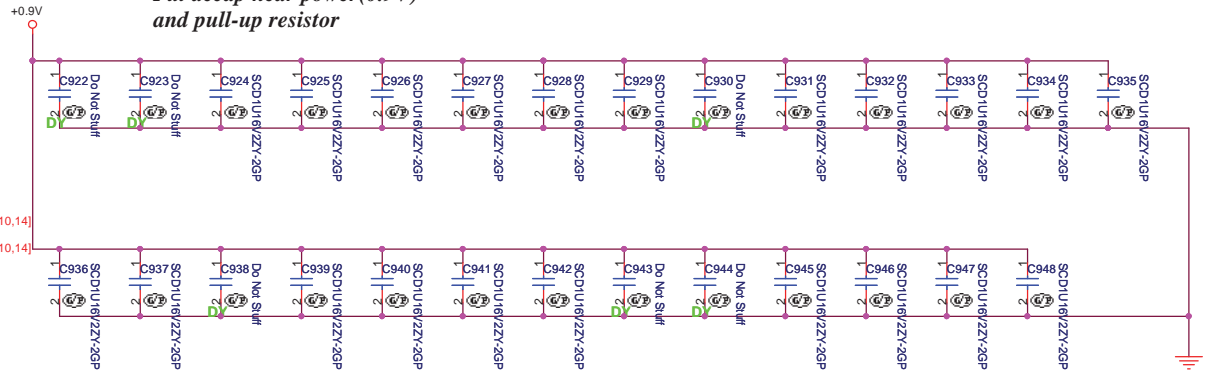
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

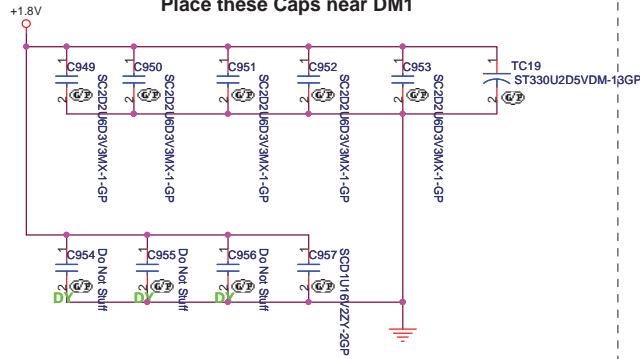


# Decoupling Capacitor

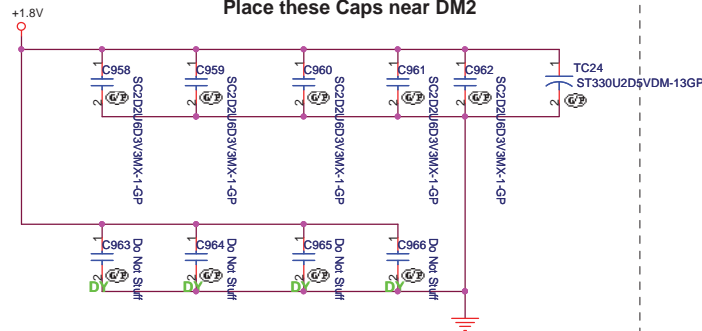
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



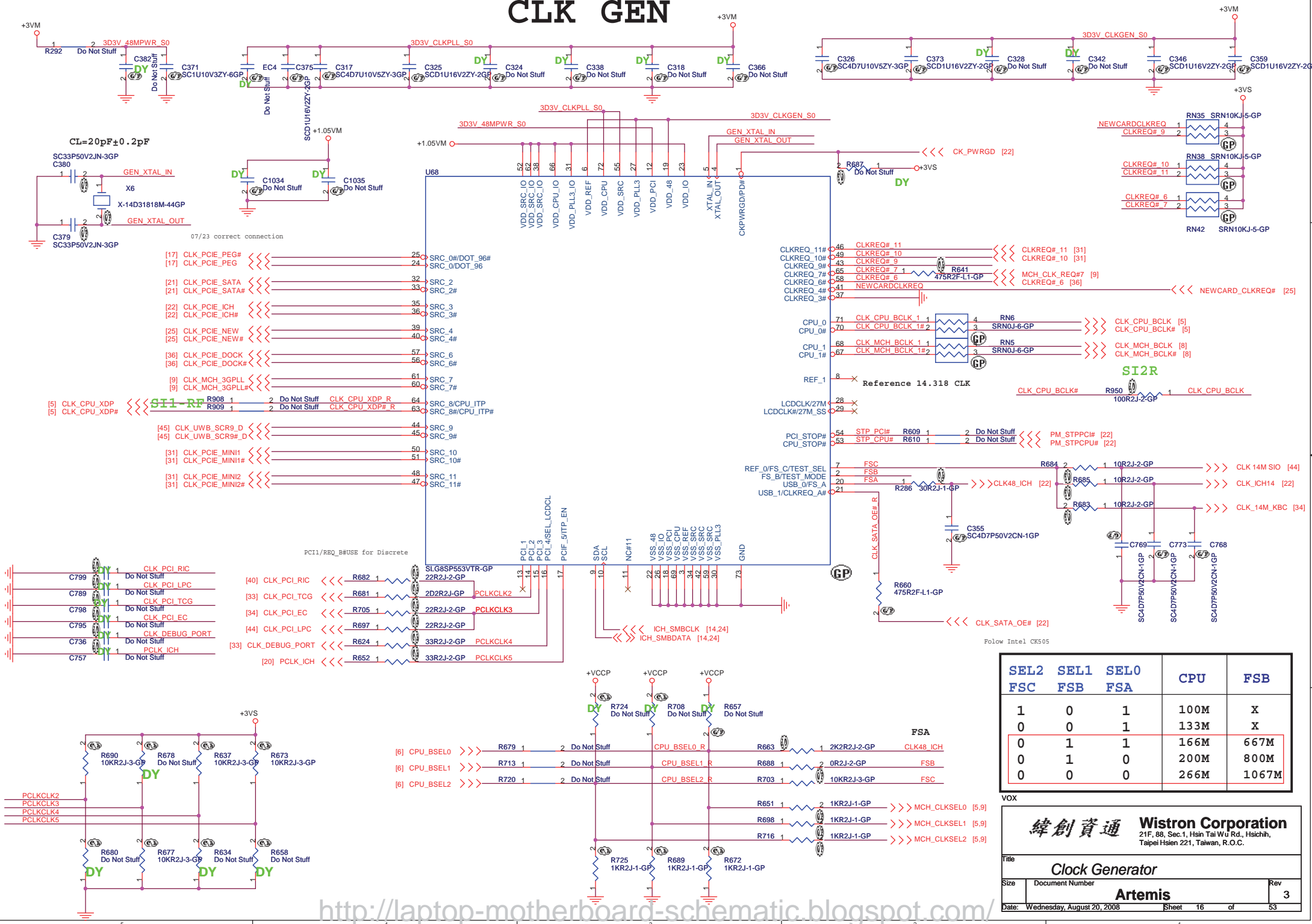
Place these Caps near DM2



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Title <b>DDR2 Termination Resistor</b>		
Size	Document Number	Rev
	<b>ARTEMIS</b>	<b>3</b>
Date: Wednesday, August 20, 2008	Sheet 15	of 53

# CLK GEN



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

VOX

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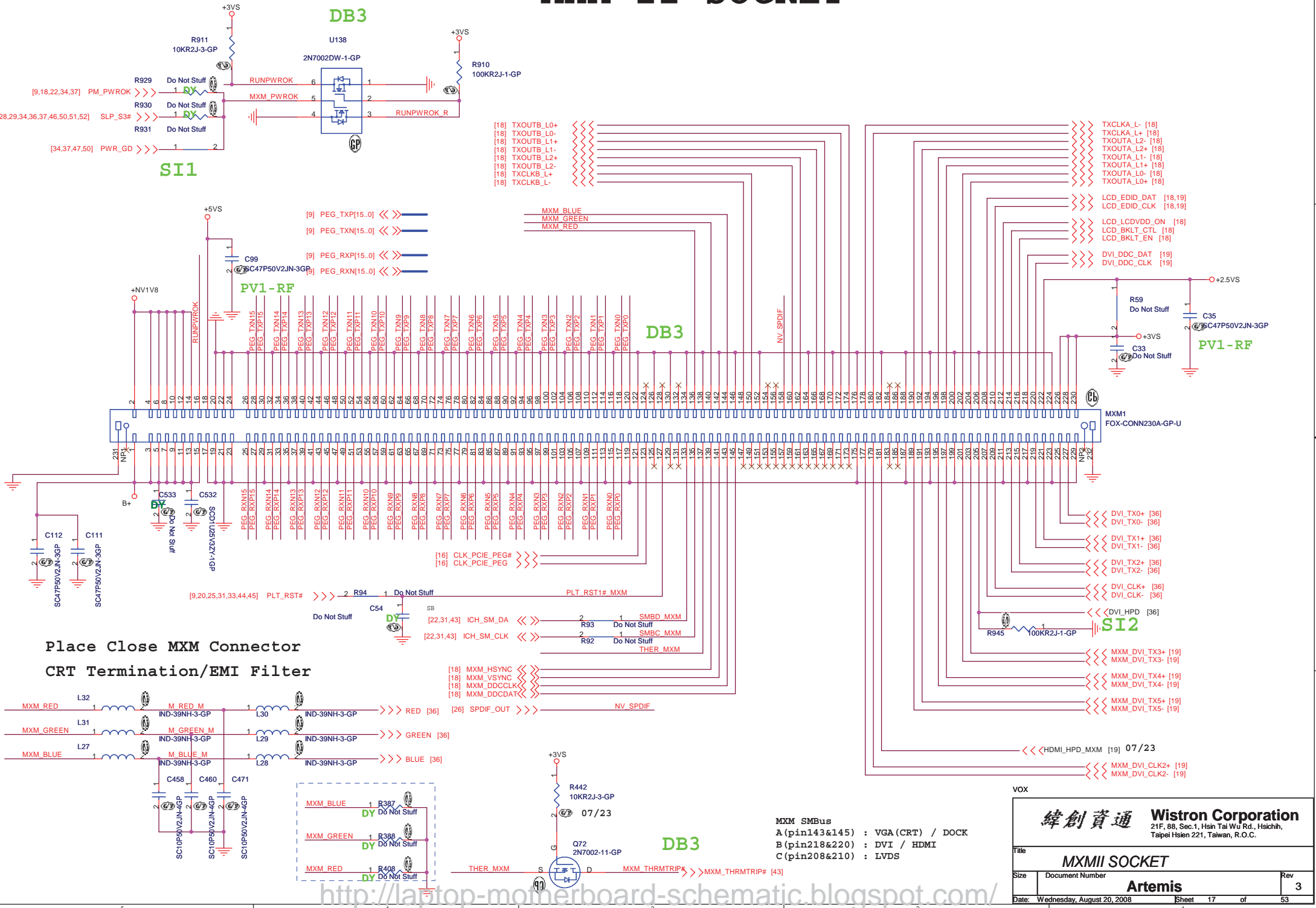
Title: **Clock Generator**

Size: Document Number **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 16 of 53



# MXM II SOCKET



Place Close MXM Connector  
CRT Termination/EMI Filter

MXM SMBus  
 A (pin143&145) : VGA(CRT) / DOCK  
 B (pin218&220) : DVI / HDMI  
 C (pin208&210) : LVDS

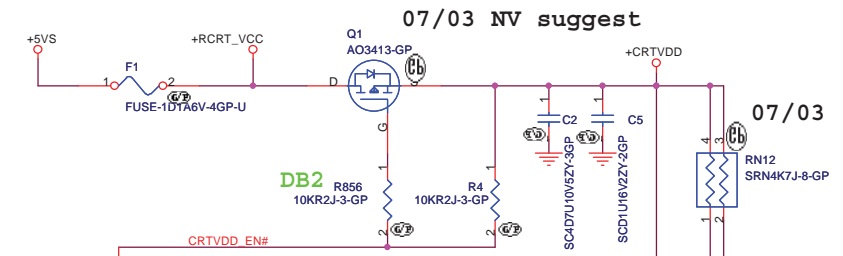
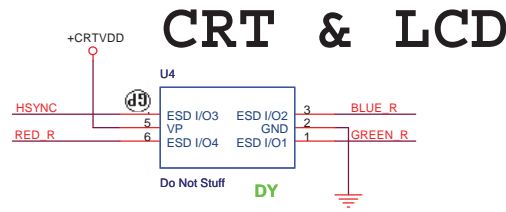
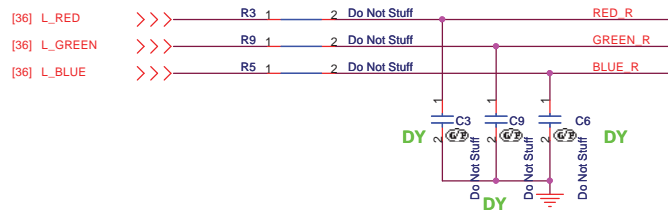
VOX

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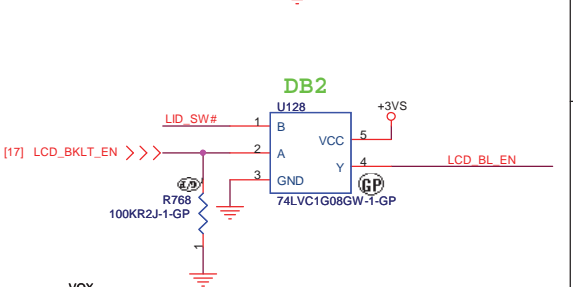
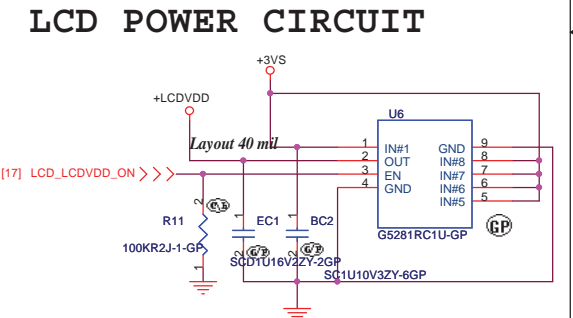
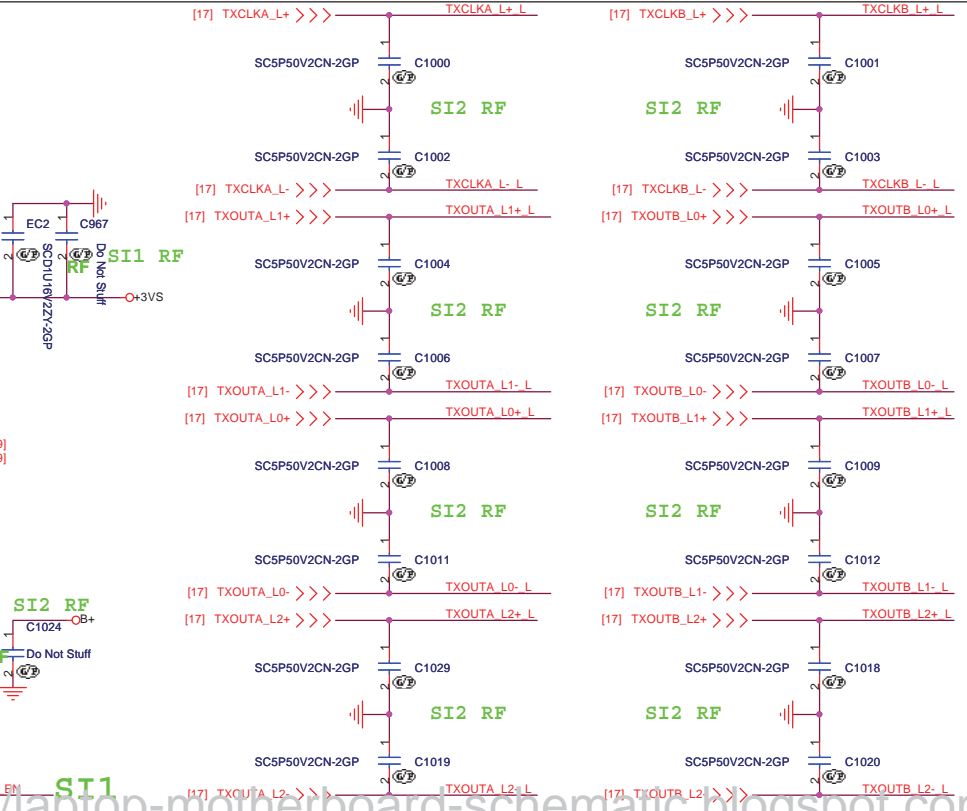
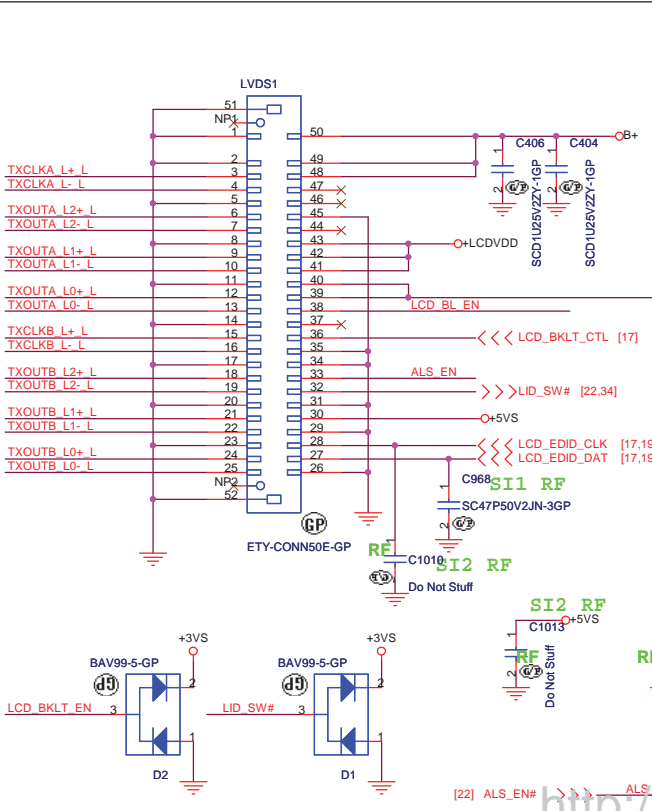
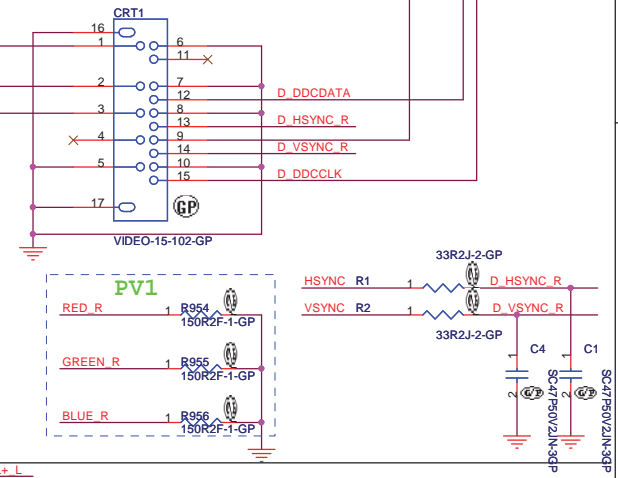
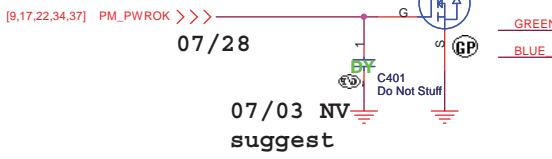
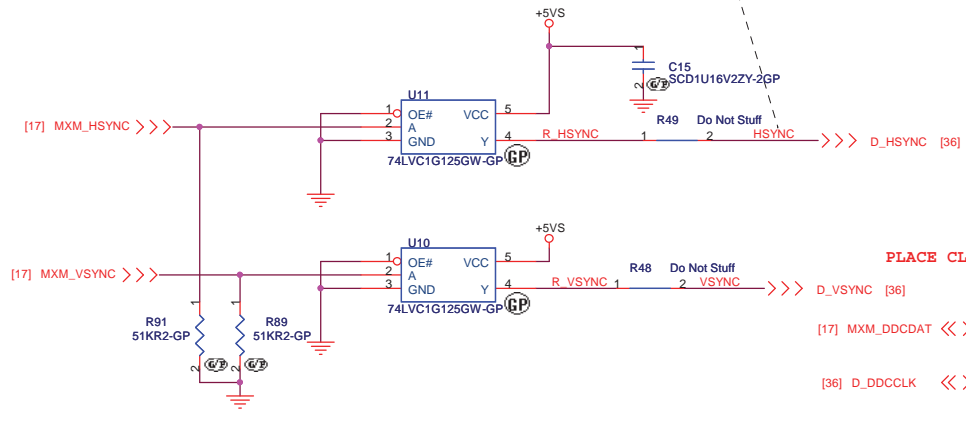
Title: **MXMII SOCKET**

Size	Document Number	Rev
	<b>Artemis</b>	<b>3</b>

Date: Wednesday, August 20, 2008 Sheet 17 of 53



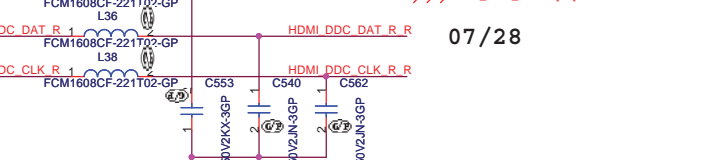
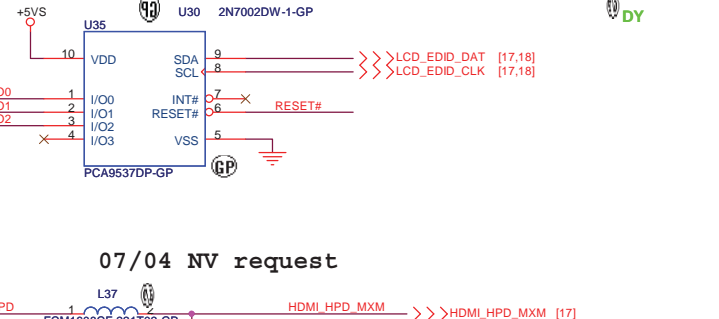
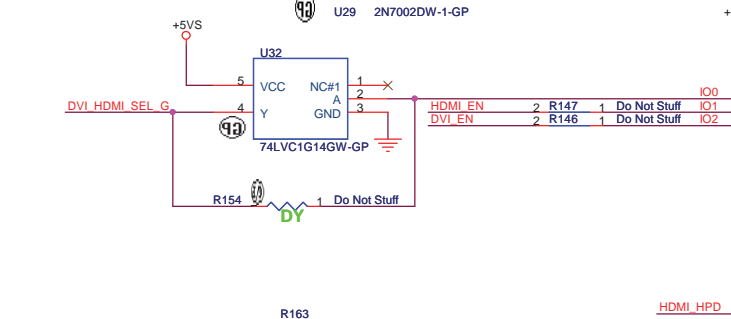
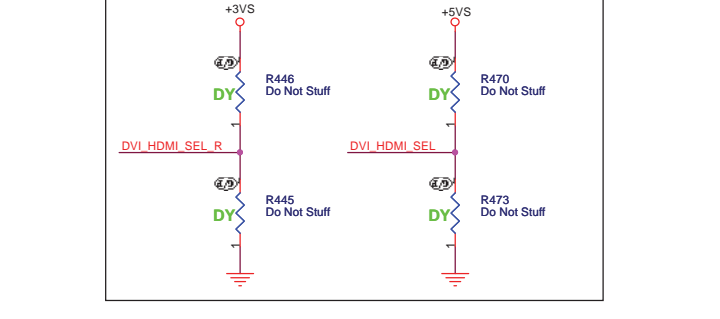
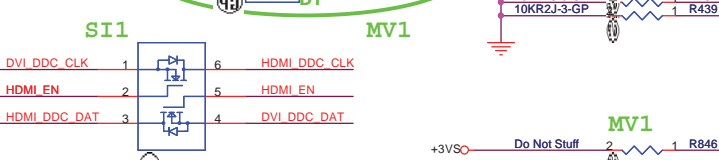
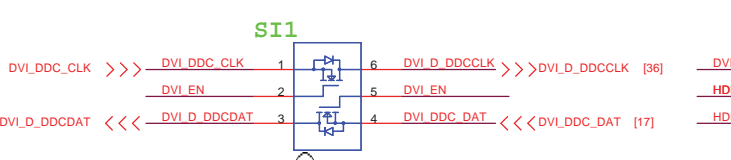
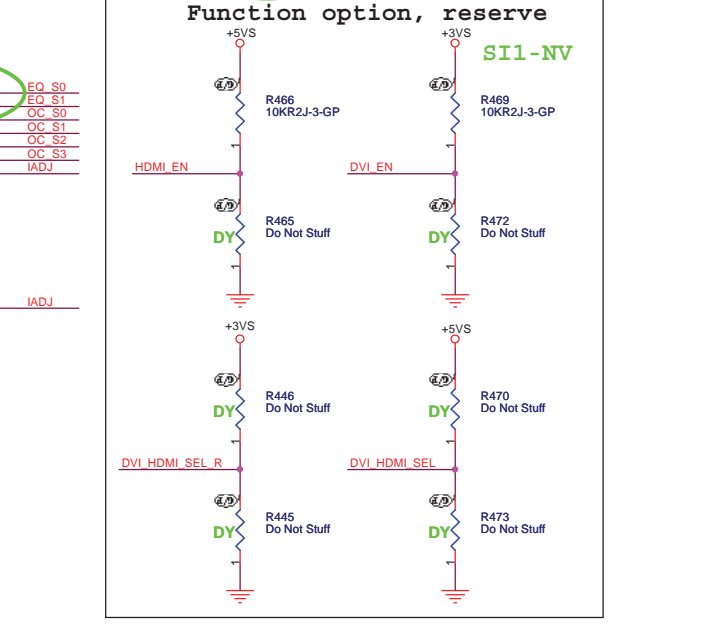
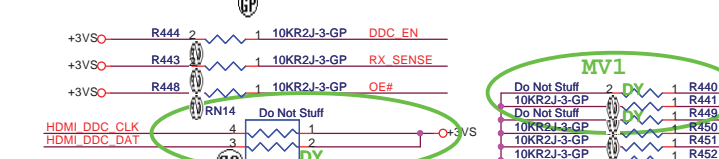
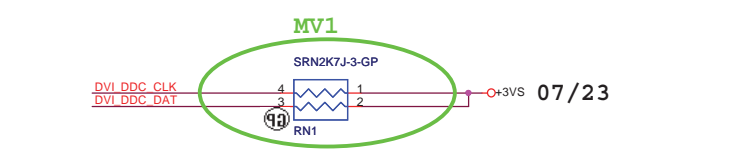
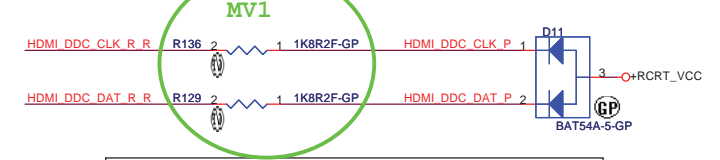
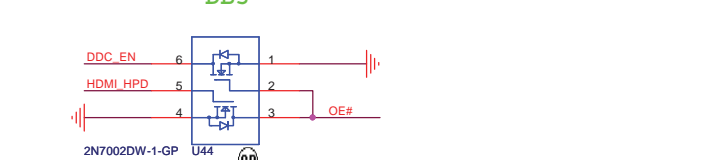
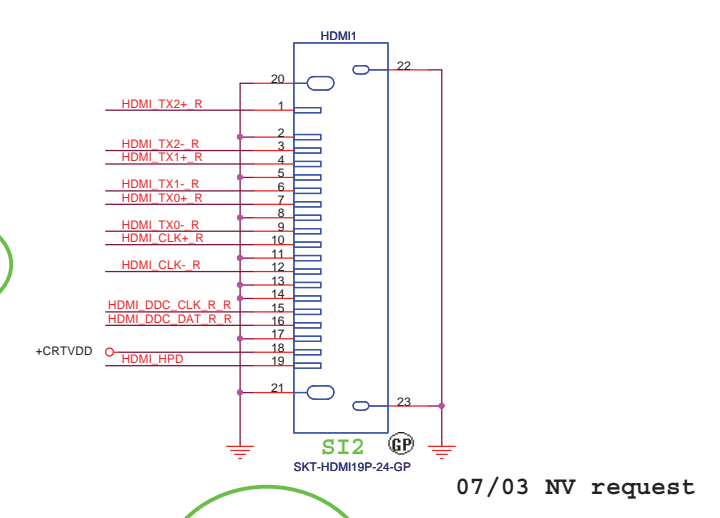
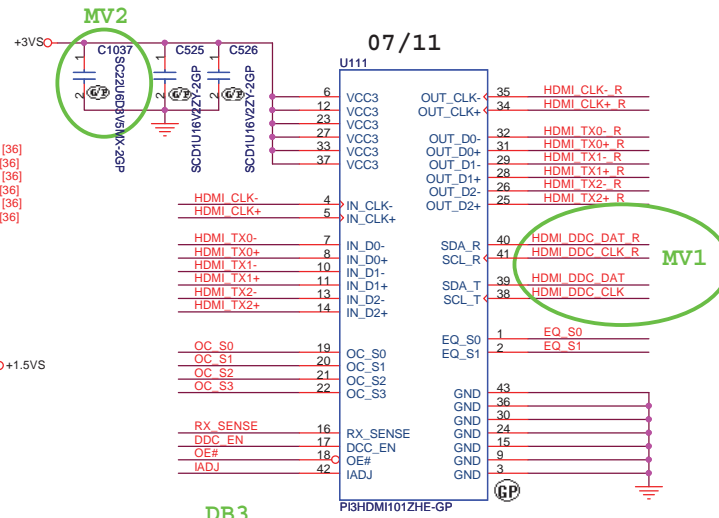
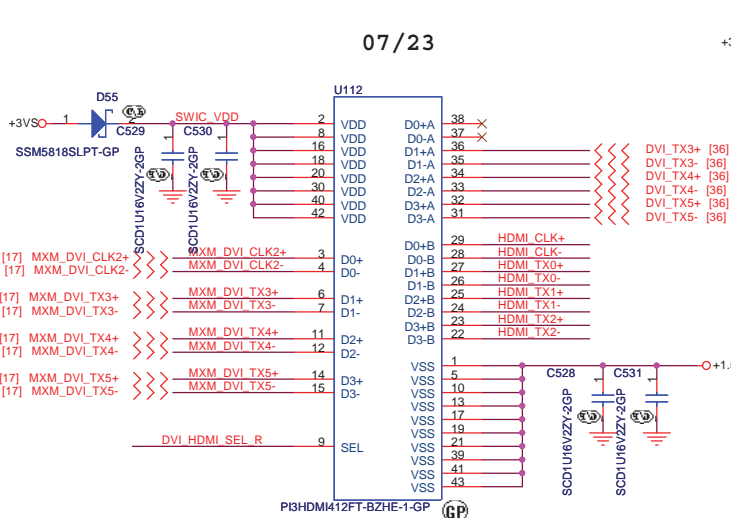
Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. , THEN TO SYSTEM CRT CONN.



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**CRT/LCD CONNECTOR**

Title	Document Number		
Size	Artemis		
A3	Rev	3	
Date: Wednesday, August 20, 2008	Sheet	18	of 53



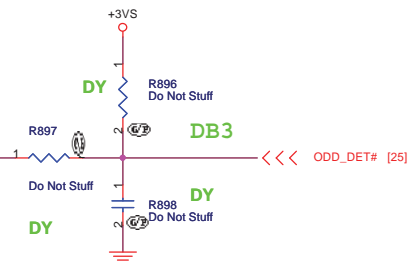
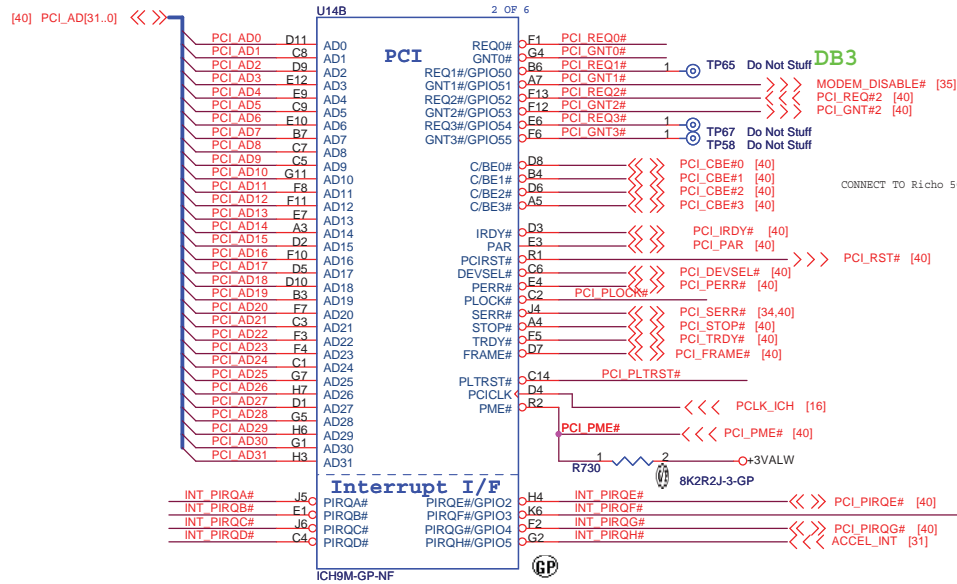
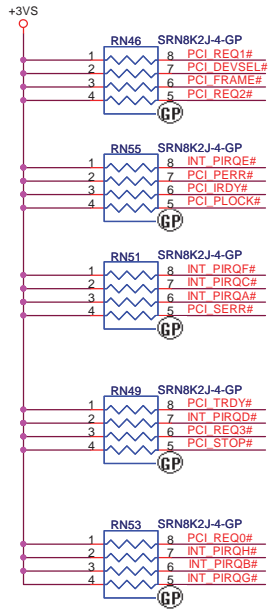
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**HDMI CONN.**

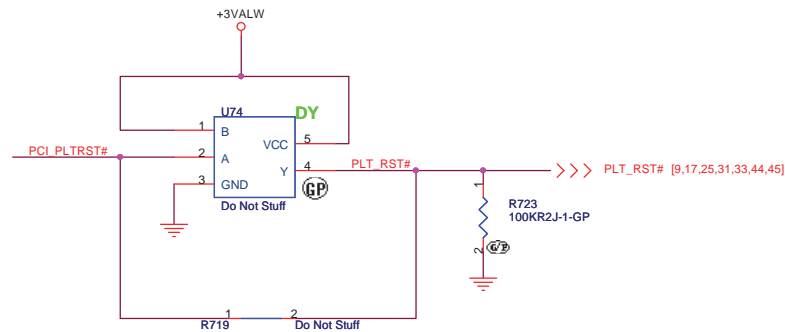
Document Number: **Artemis**

Date: Wednesday, August 20, 2008 Sheet 19 of 53

# ICH9-M (1 of 5) PCI



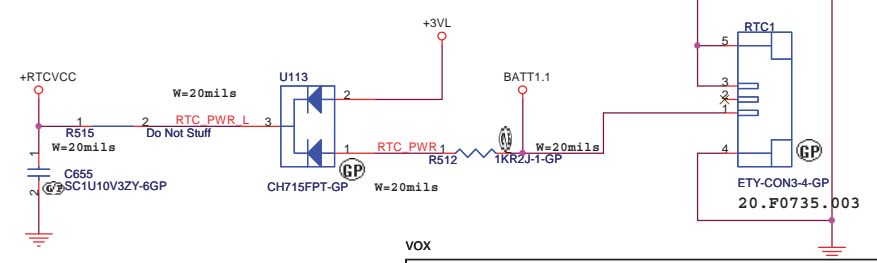
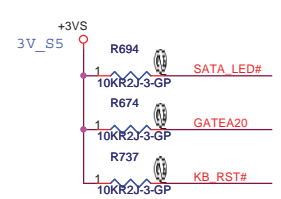
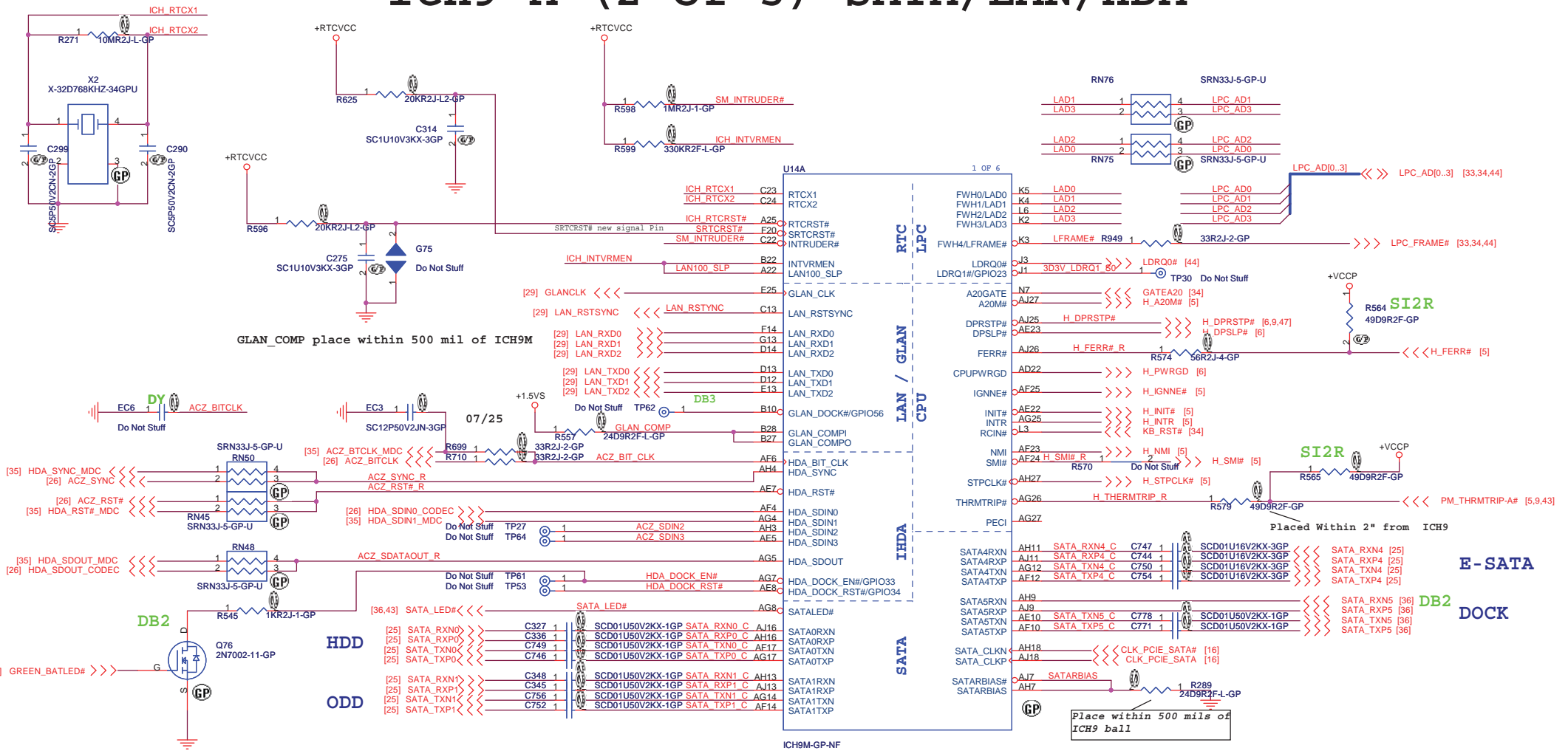
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default



VOX

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<b>ICH9-M (1 of 5)</b>			
File	Document Number	Rev	3
<b>Artemis</b>		Date: Wednesday, August 20, 2008	Sheet 20 of 53

# ICH9-M (2 of 5) SATA/LAN/HDA



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

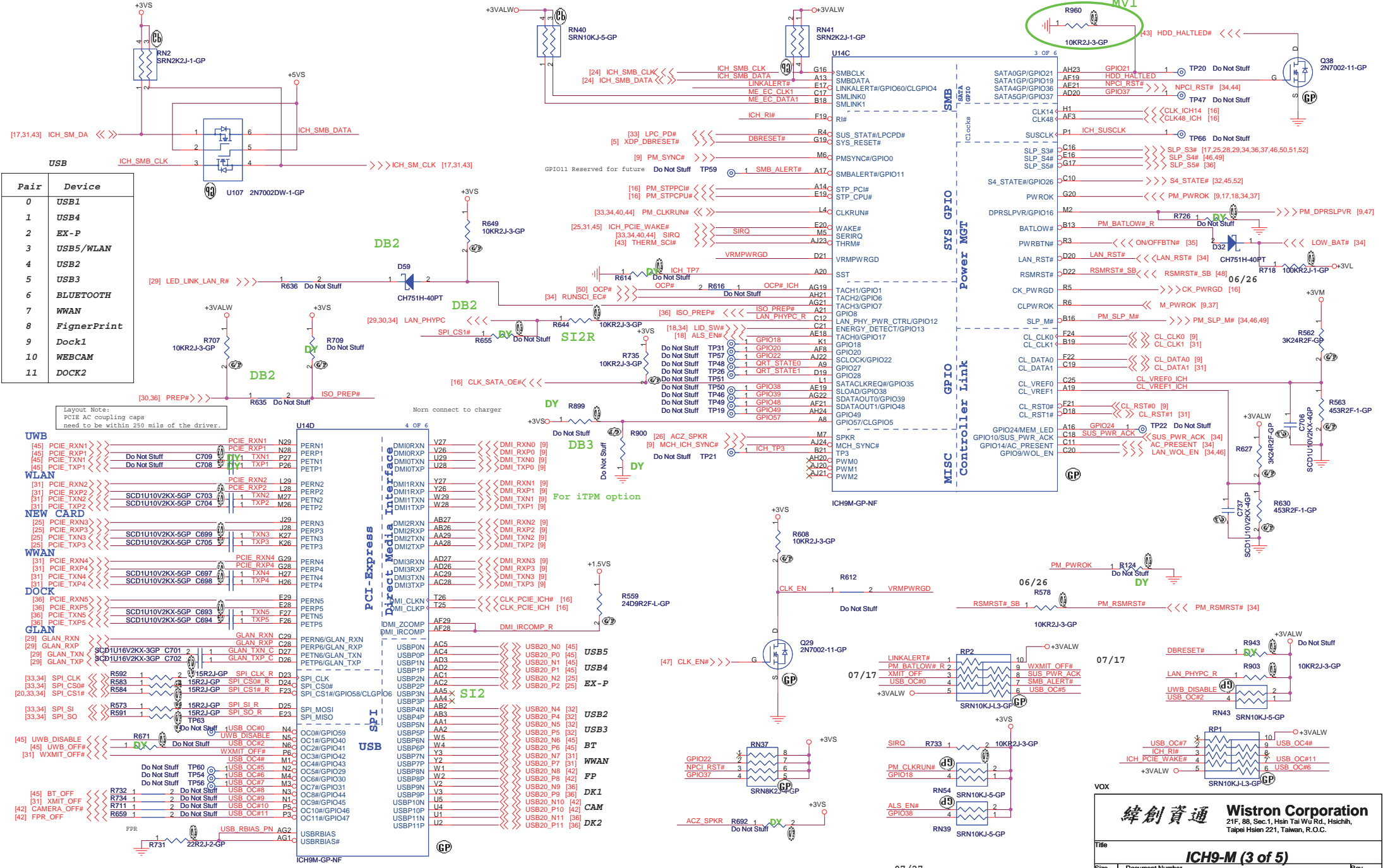
緯創資通 **Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 5)**

Size	Document Number	Rev
		3

Date: Wednesday, August 20, 2008 Sheet 21 of 53

# ICH9-M (3 of 5) USB/PCIE/DMI



Pair	Device
0	USB1
1	USB4
2	EX-P
3	USB5/WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FingerPrint
9	Dock1
10	WEBCAM
11	DOCK2

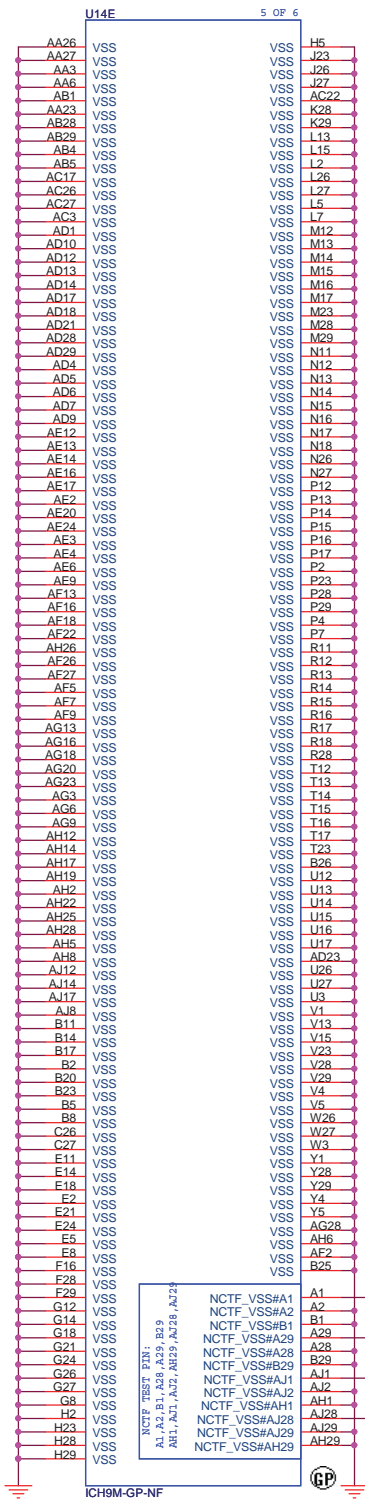
Pair	Device
[45]	PCI_E_RXN1
[45]	PCI_E_RXP1
[45]	PCI_E_TXN1
[45]	PCI_E_TXP1
[31]	PCI_E_RXN2
[31]	PCI_E_RXP2
[31]	PCI_E_TXN2
[31]	PCI_E_TXP2
[25]	PCI_E_RXN3
[25]	PCI_E_RXP3
[25]	PCI_E_TXN3
[25]	PCI_E_TXP3
[31]	PCI_E_RXN4
[31]	PCI_E_RXP4
[31]	PCI_E_TXN4
[31]	PCI_E_TXP4
[36]	PCI_E_RXN5
[36]	PCI_E_RXP5
[36]	PCI_E_TXN5
[36]	PCI_E_TXP5
[29]	GLAN_RXN
[29]	GLAN_RXP
[29]	GLAN_TXN
[29]	GLAN_TXP
[33,34]	SPI_CLK
[33,34]	SPI_CS0#
[20,33,34]	SPI_CS1#
[33,34]	SPI_SI
[33,34]	SPI_SO
[45]	UWB_DISABLE
[45]	UWB_OFF#
[31]	WXMIT_OFF#
[45]	BT_OFF
[31]	XMIT_OFF
[42]	CAMERA_OFF#
[42]	FPR_OFF

Pair	Device
[45]	PCI_E_RXN1
[45]	PCI_E_RXP1
[45]	PCI_E_TXN1
[45]	PCI_E_TXP1
[31]	PCI_E_RXN2
[31]	PCI_E_RXP2
[31]	PCI_E_TXN2
[31]	PCI_E_TXP2
[25]	PCI_E_RXN3
[25]	PCI_E_RXP3
[25]	PCI_E_TXN3
[25]	PCI_E_TXP3
[31]	PCI_E_RXN4
[31]	PCI_E_RXP4
[31]	PCI_E_TXN4
[31]	PCI_E_TXP4
[36]	PCI_E_RXN5
[36]	PCI_E_RXP5
[36]	PCI_E_TXN5
[36]	PCI_E_TXP5
[29]	GLAN_RXN
[29]	GLAN_RXP
[29]	GLAN_TXN
[29]	GLAN_TXP
[33,34]	SPI_CLK
[33,34]	SPI_CS0#
[20,33,34]	SPI_CS1#
[33,34]	SPI_SI
[33,34]	SPI_SO
[45]	UWB_DISABLE
[45]	UWB_OFF#
[31]	WXMIT_OFF#
[45]	BT_OFF
[31]	XMIT_OFF
[42]	CAMERA_OFF#
[42]	FPR_OFF

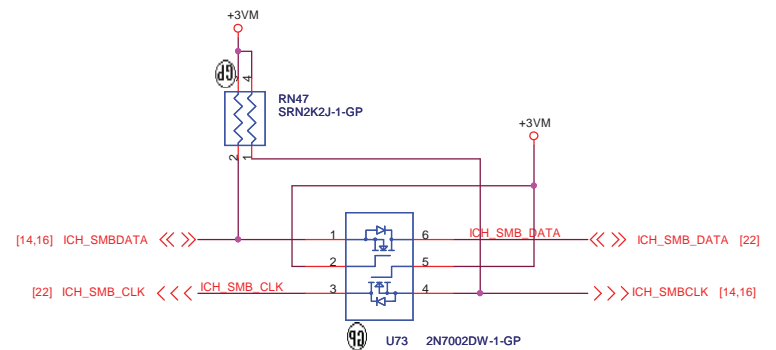
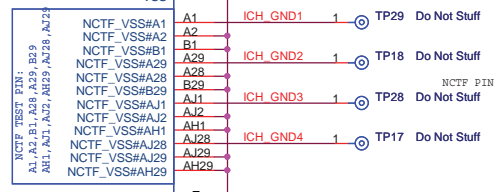
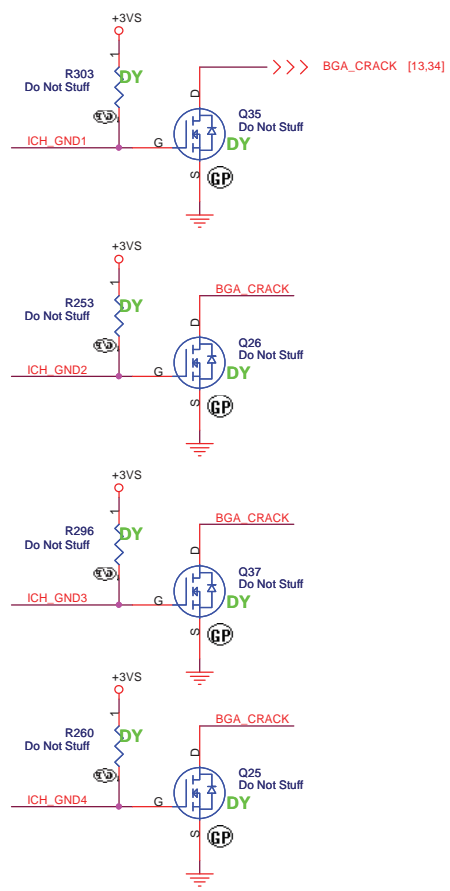
**緯創資通 Wistron Corporation**  
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<b>ICH9-M (3 of 5)</b>		
Title	Document Number	Rev
		3
<b>Artemis</b>		
Date: Wednesday, August 20, 2008	Sheet 22	of 53





07/20 BGA CRACK CIRCUIT



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

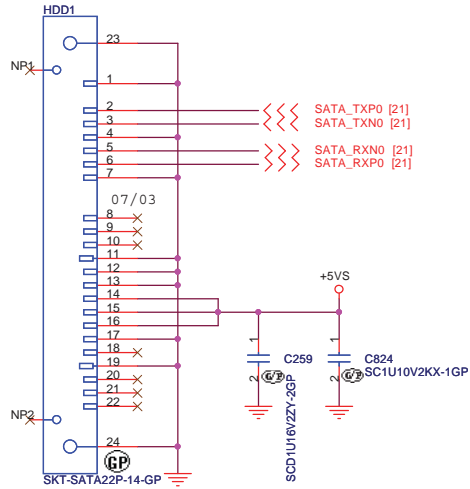
SMBUS

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

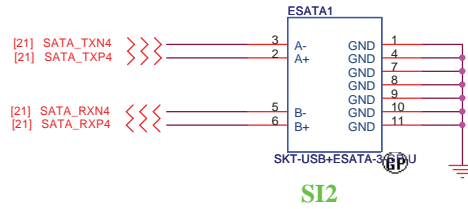
Title		
ICH9-M (5 of 5)		
Size	Document Number	Rev
	Artemis	3
Date: Wednesday, August 20, 2008	Sheet 24 of 53	



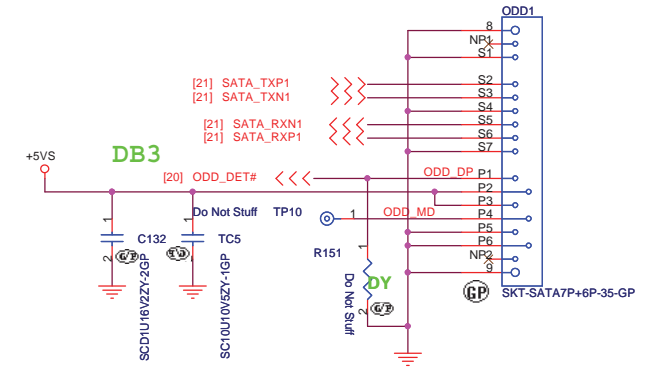
# SATA HDD Connector



# ESATA Connector

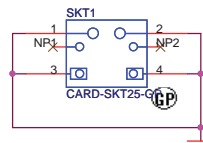


# ODD Connector

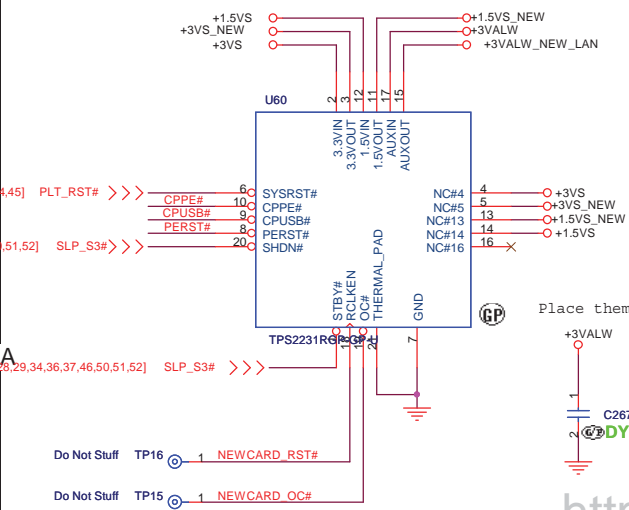
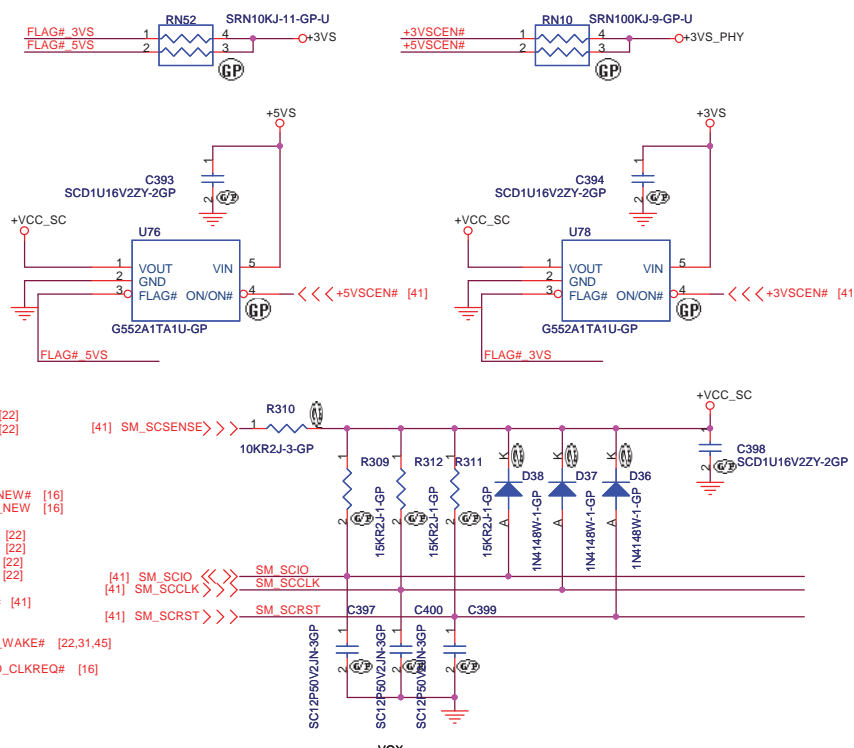
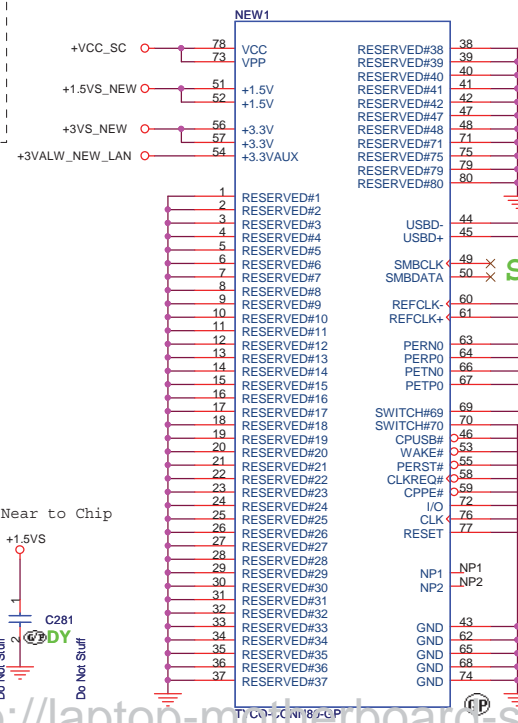
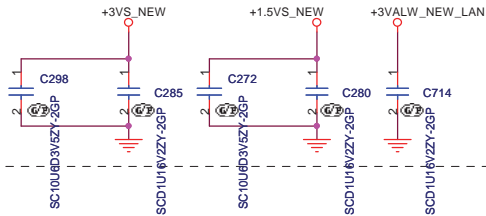


# NEWCARD/SMART CARD Connector

For Newcard socket



Place them Near to Connector

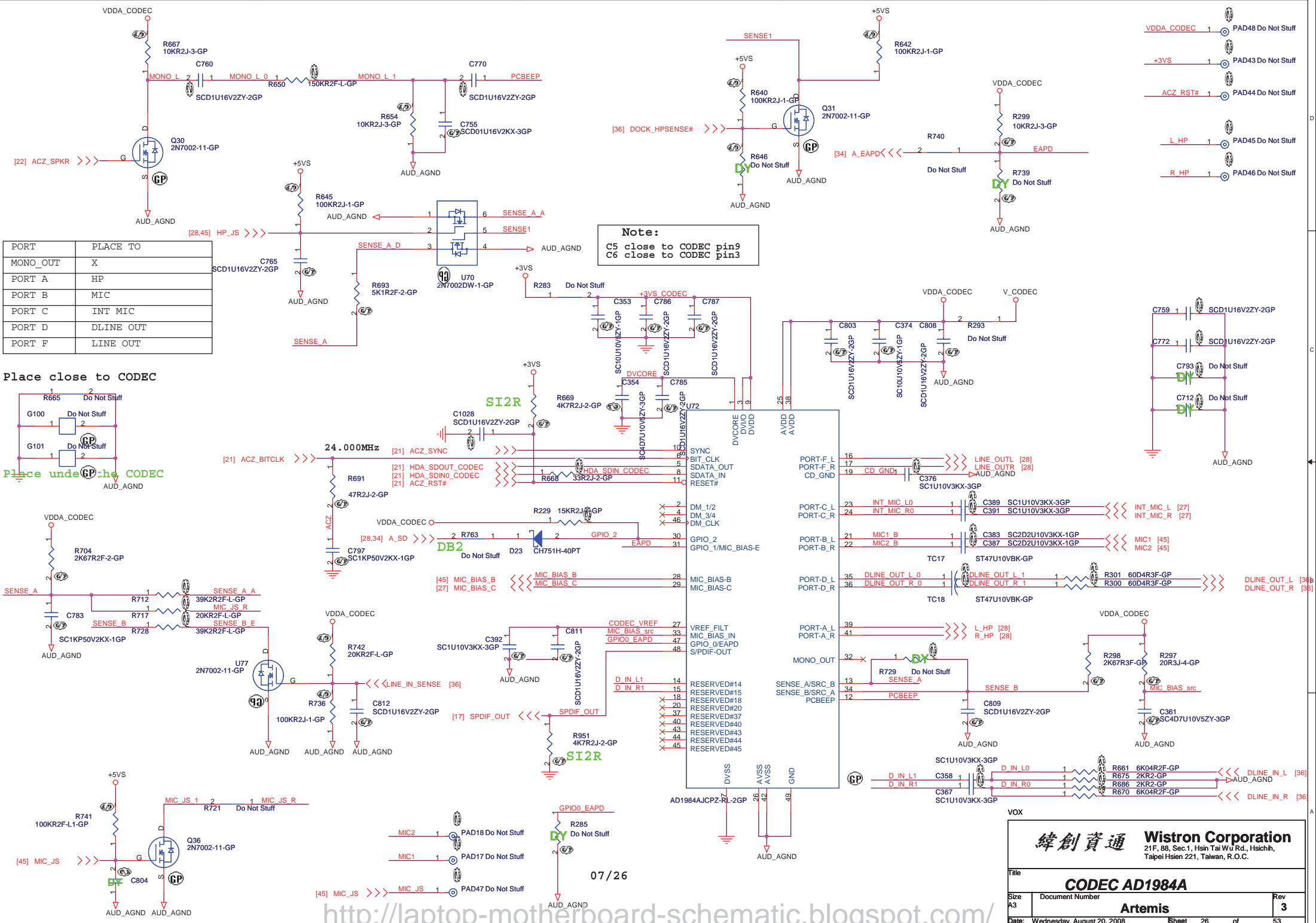


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**HDD/NEW CARD CONN.**

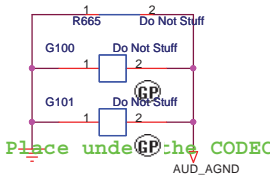
Artemis

Date: Wednesday, August 20, 2008 Sheet 25 of 53



PORT	PLACE TO
MONO_OUT	X
PORT A	HP
PORT B	MIC
PORT C	INT MIC
PORT D	DLINE OUT
PORT F	LINE OUT

**Place close to CODEC**



**Note:**  
 C5 close to CODEC pin9  
 C6 close to CODEC pin3

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File: **CODEC AD1984A**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008		Sheet 26 of 53

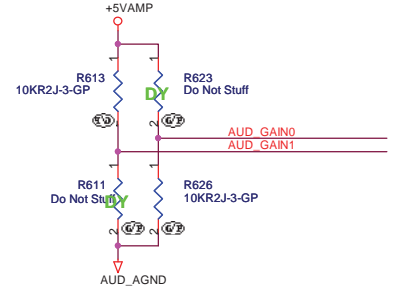
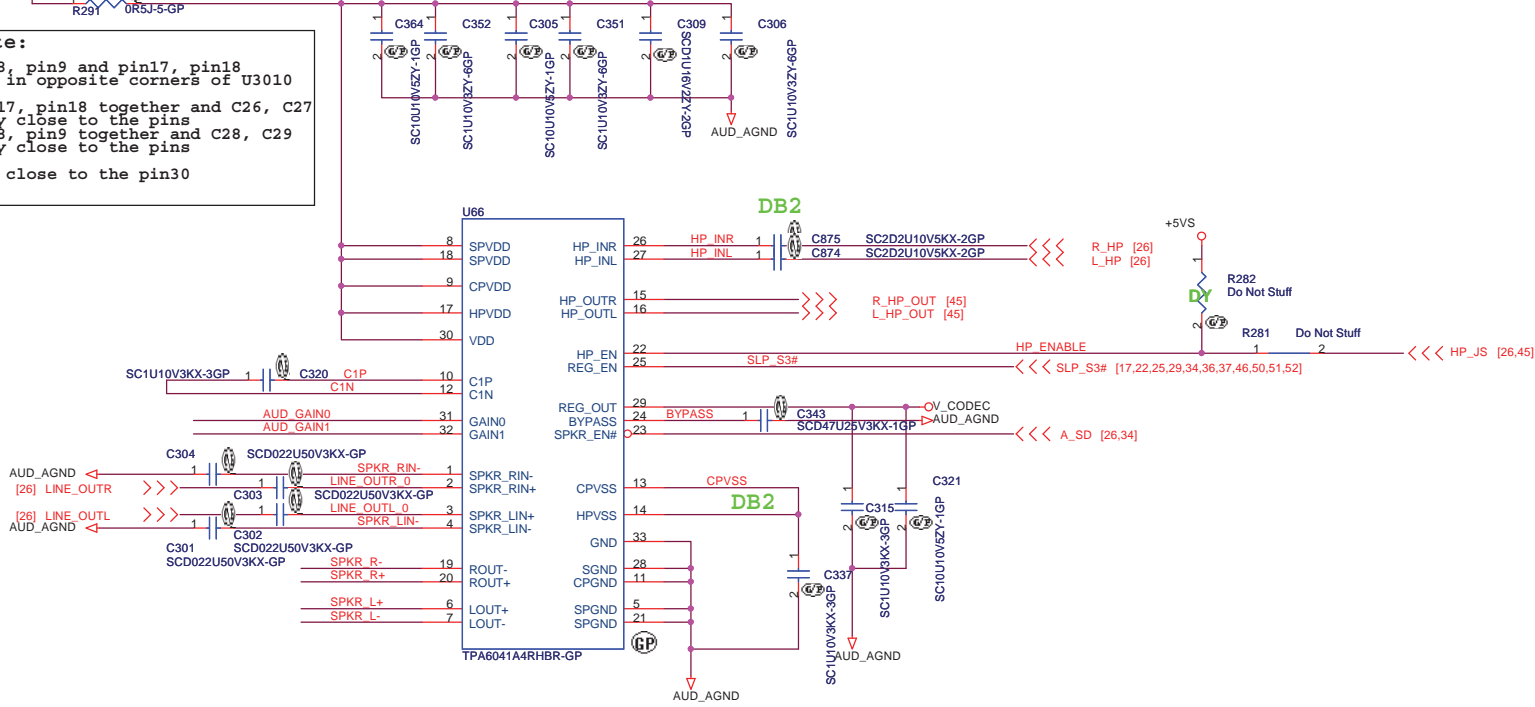
07/26



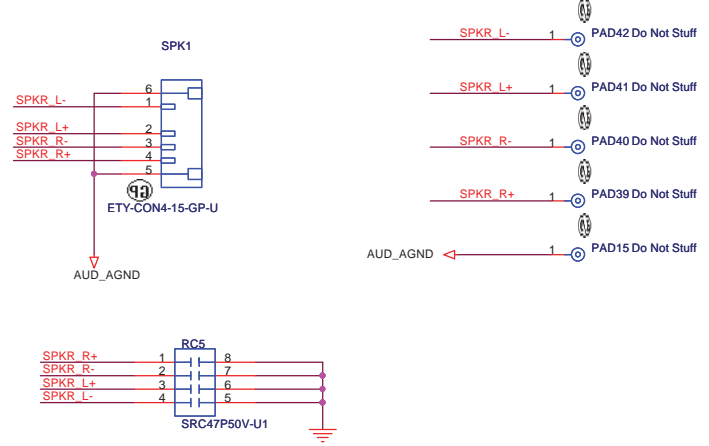
SI2R  
+5VS

+5VAMP

**Note:**  
 pin8, pin9 and pin17, pin18  
 are in opposite corners of U3010  
 pin17, pin18 together and C26, C27  
 very close to the pins  
 pin8, pin9 together and C28, C29  
 very close to the pins  
 C32 close to the pin30



### Speaker CONN.

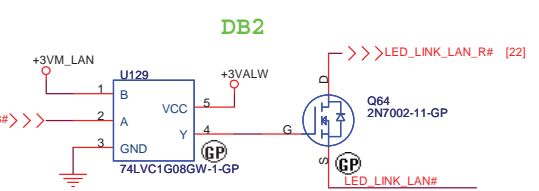
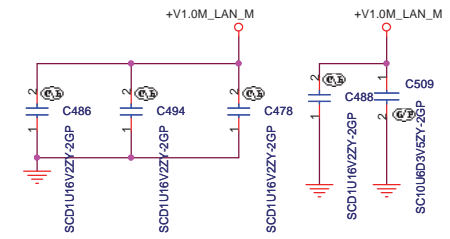
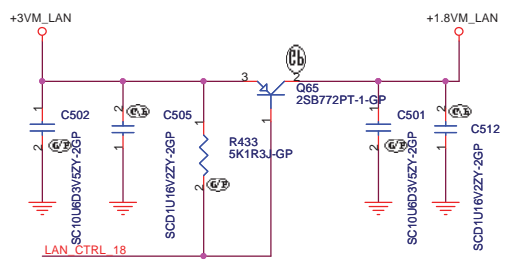
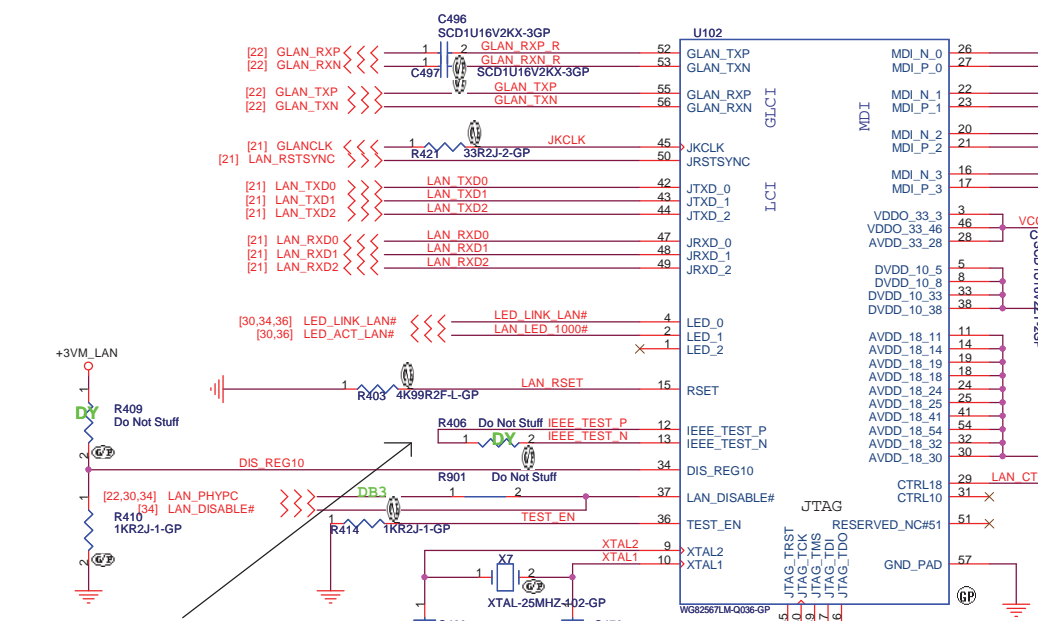
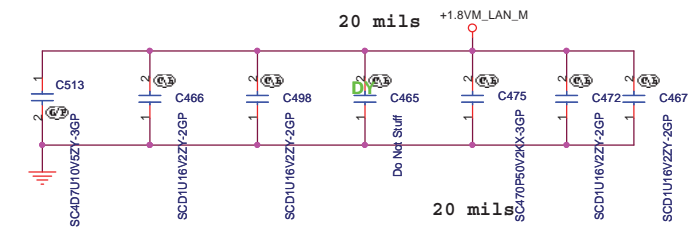
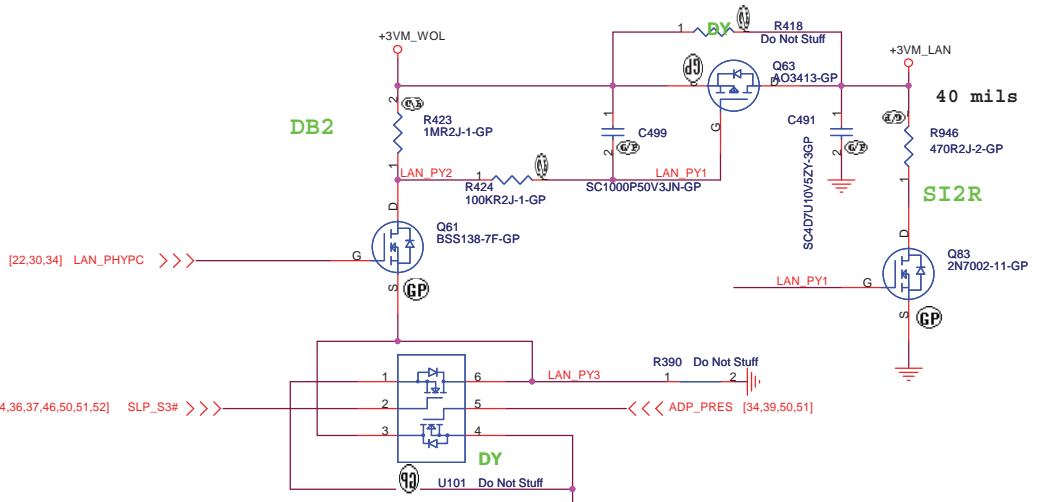


VOX

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Title: **AMP & SPEAKER**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008	Sheet 28	of 53



Layout Note  
Keep this R406 on top side  
and route differentially

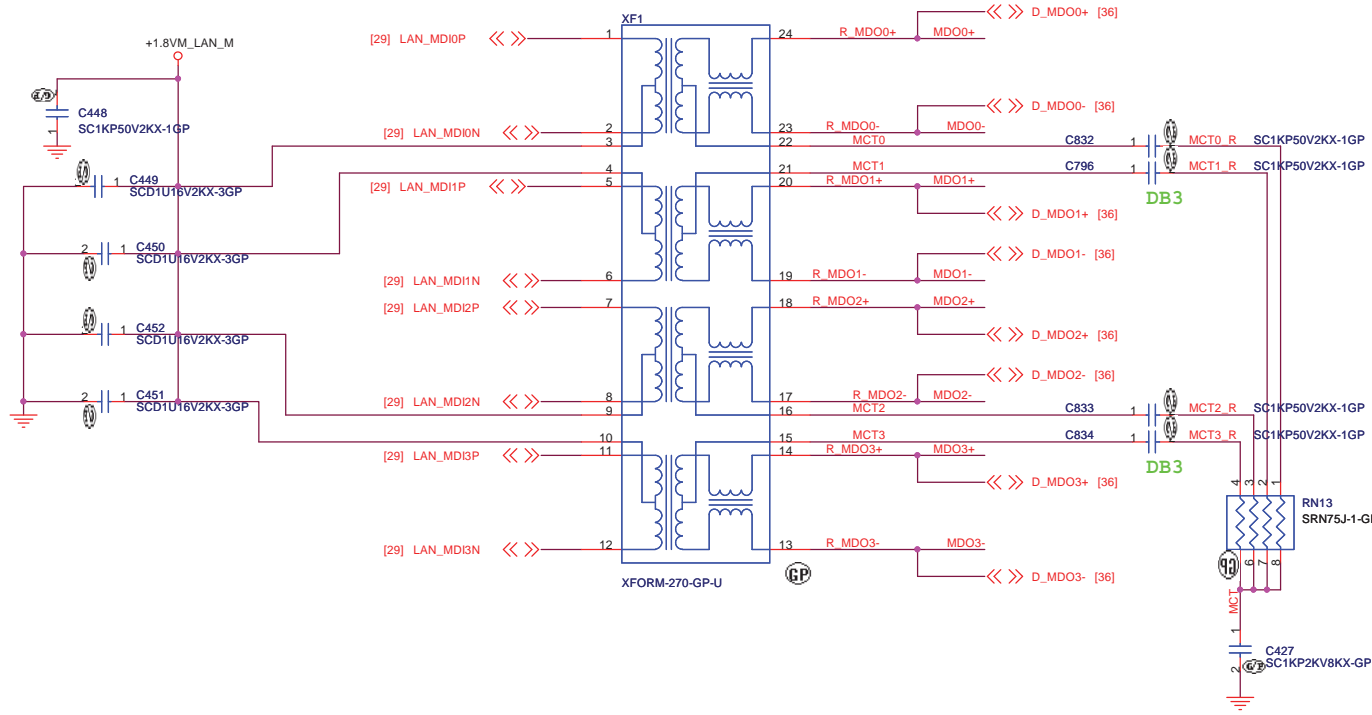
VOX

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

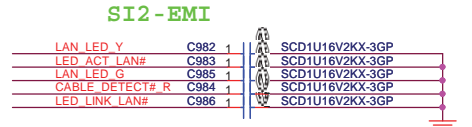
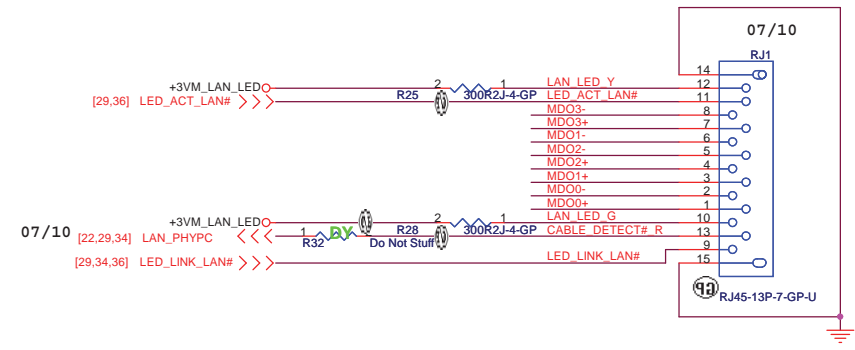
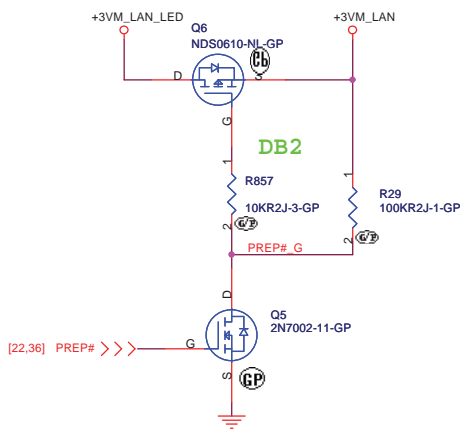
Title: **Intel 82567 Boaz**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008	Sheet 29	of 53

Note : MDO[3..0]+ signals should route to RJ45 first then to DOCK CONN .



### LAN ENERGY DET



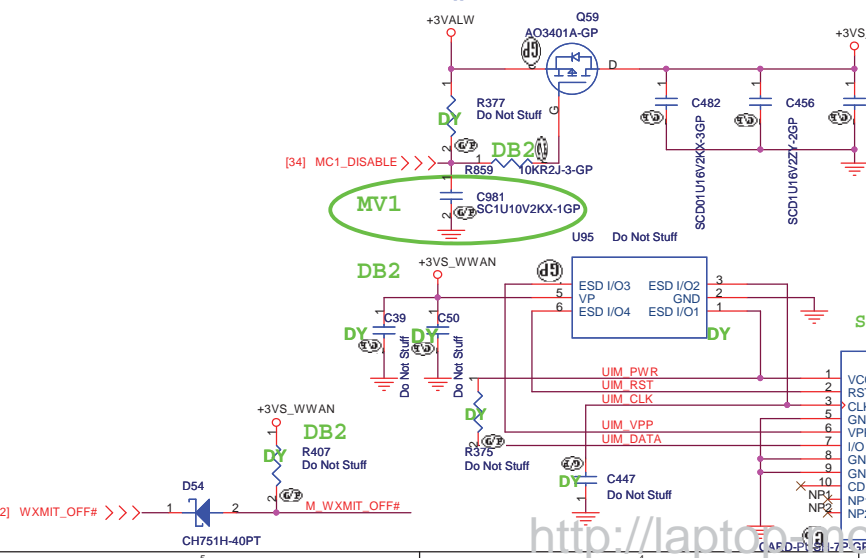
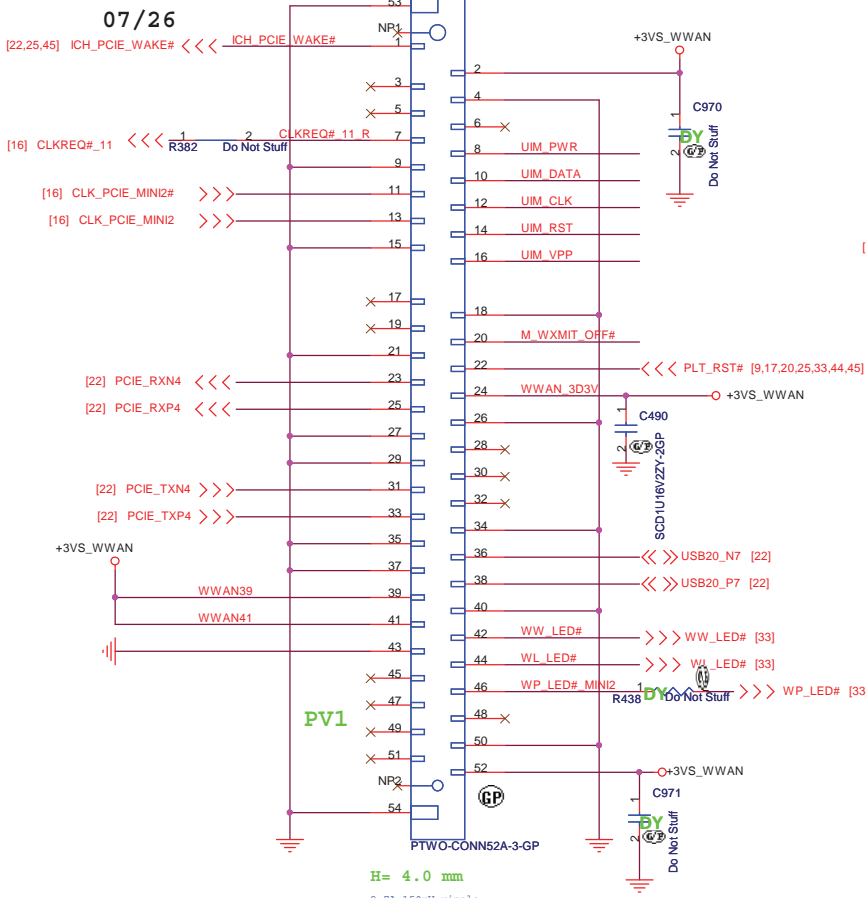
VOX

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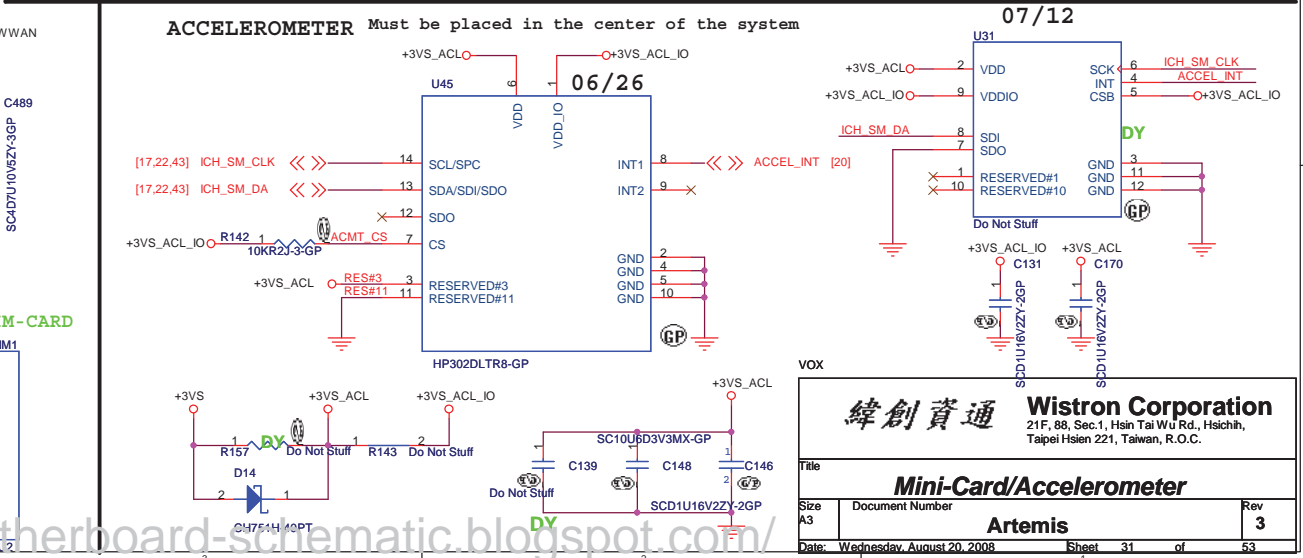
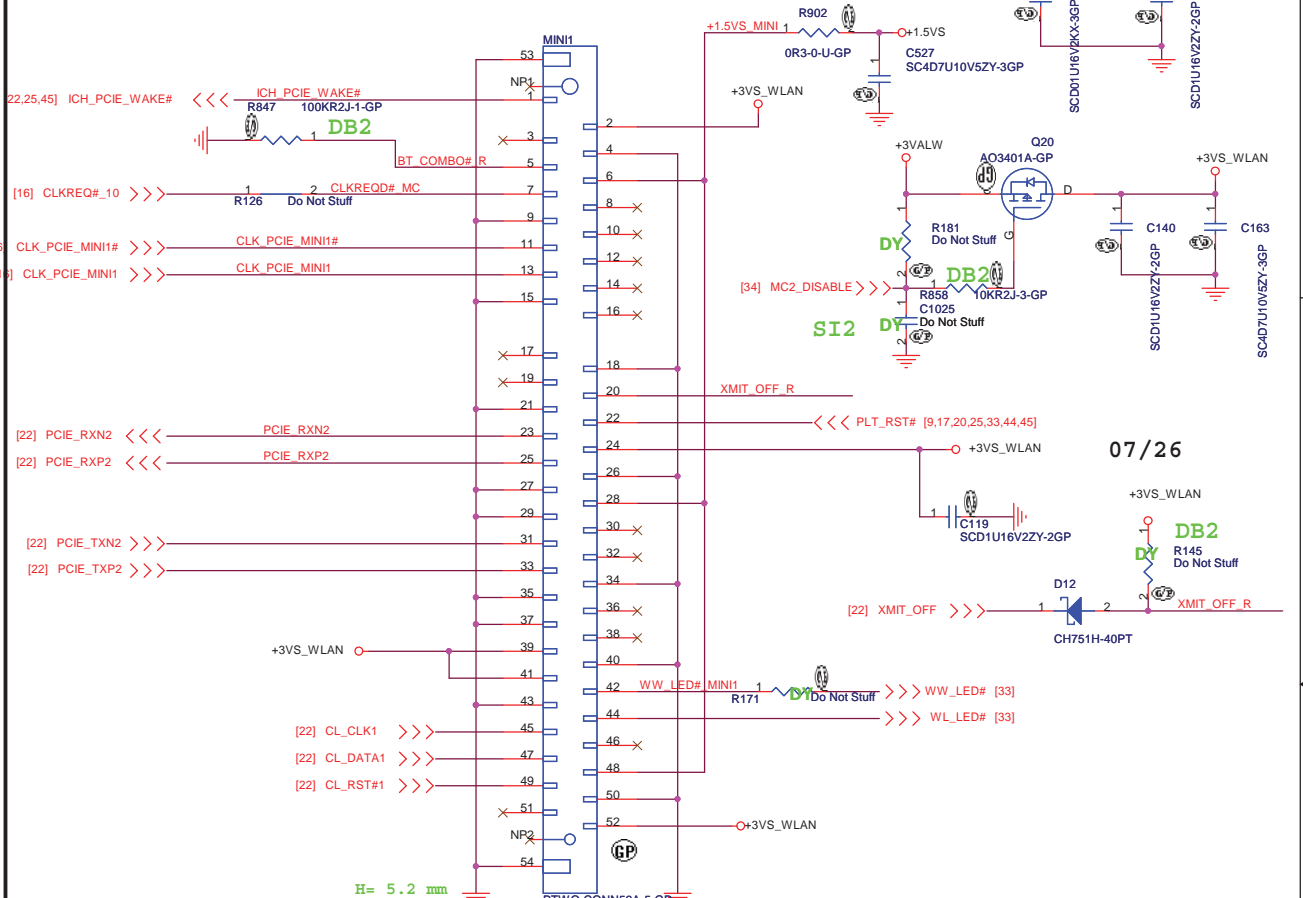
Title: **Magnetic & RJ45**

Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008	Sheet 30	of 53

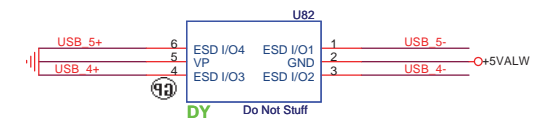
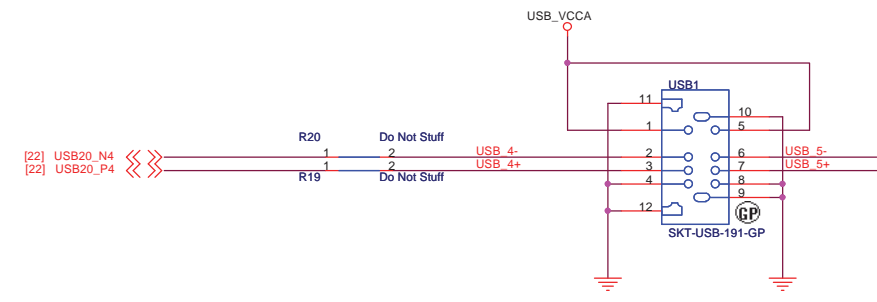
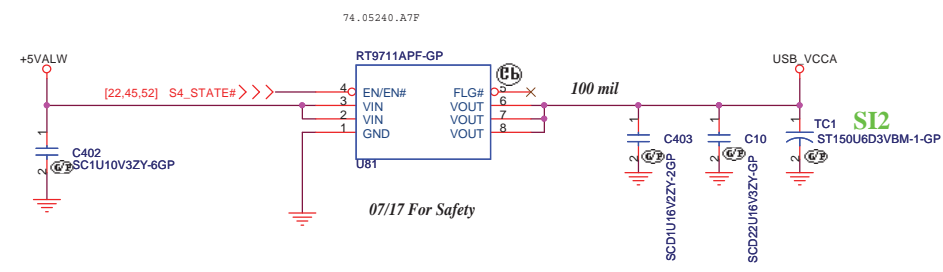
# Mini-Card--WWAN BOTTOM



# Mini-Card--WLAN TOP



74.02231.073-->74.00577.A73,74.05538.073  
2462--G1224



VOX

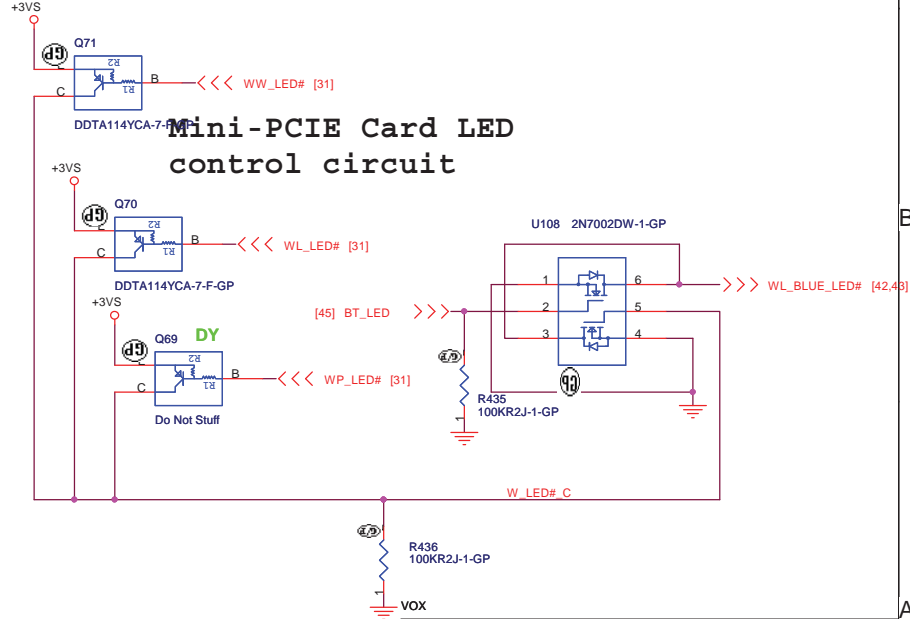
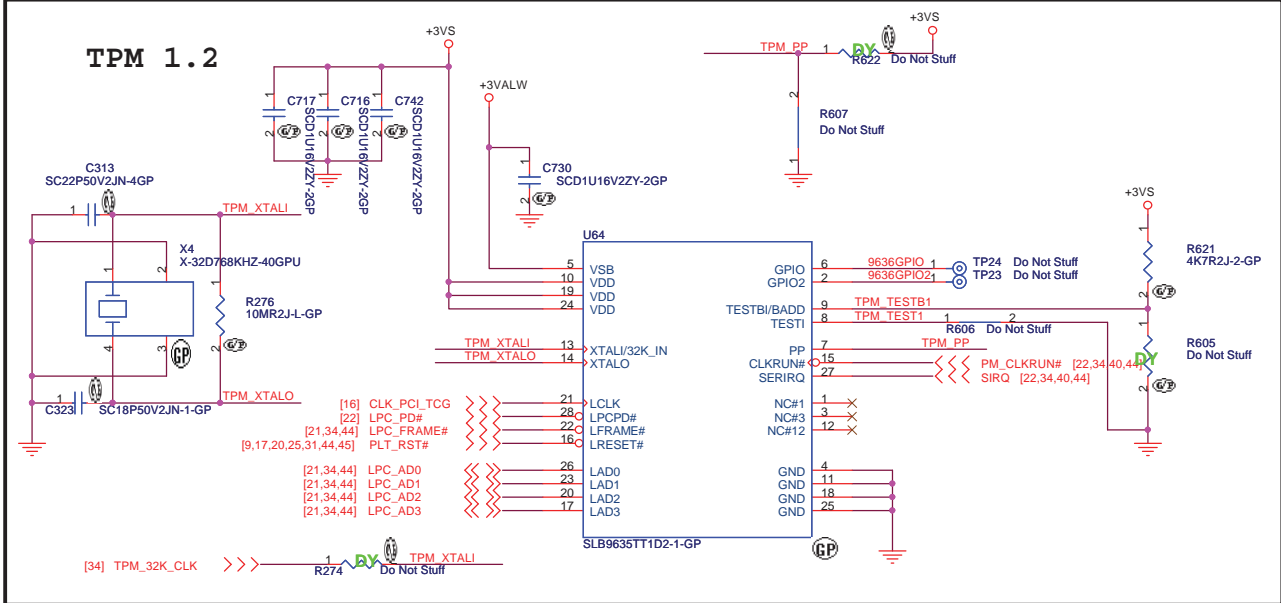
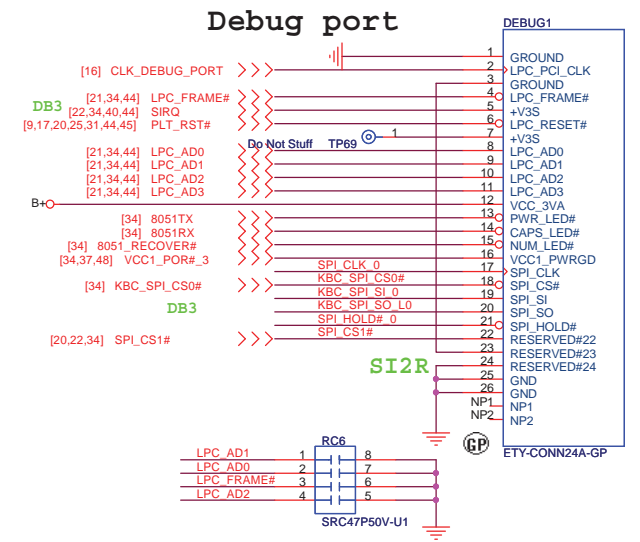
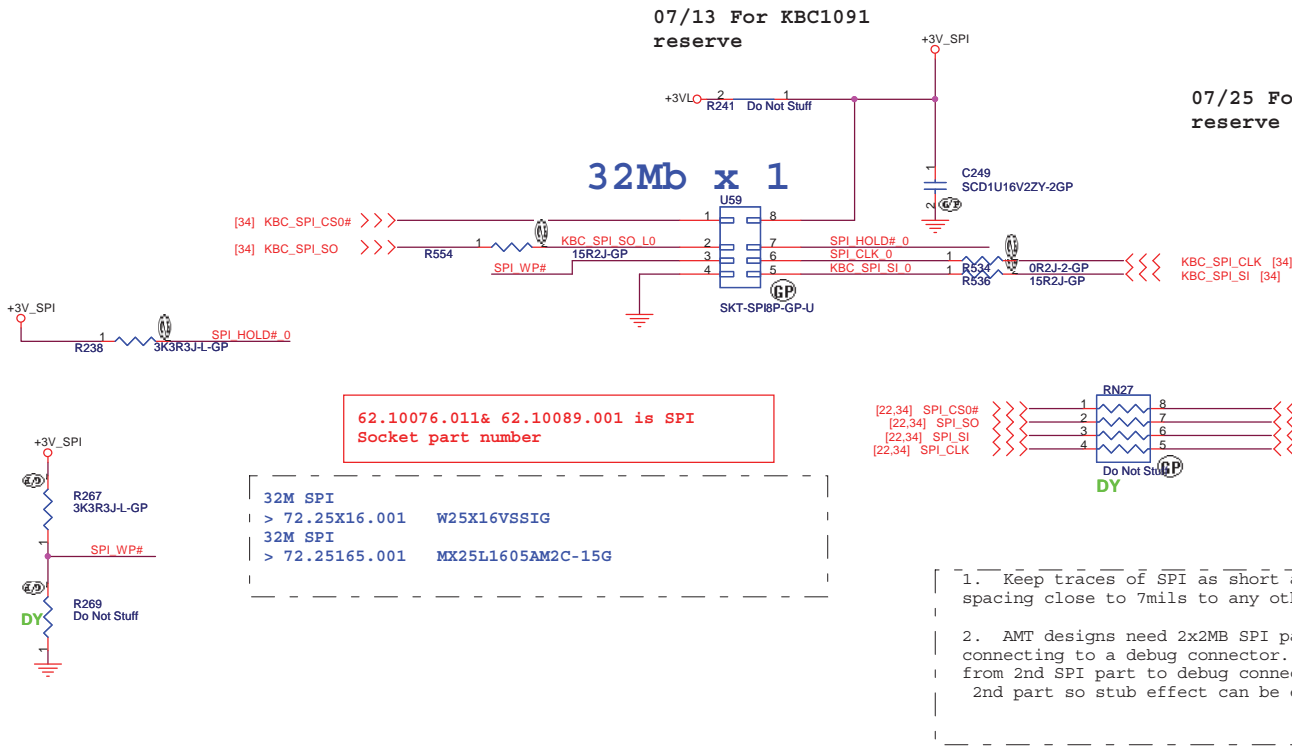
**緯創資通 Wistron Corporation**  
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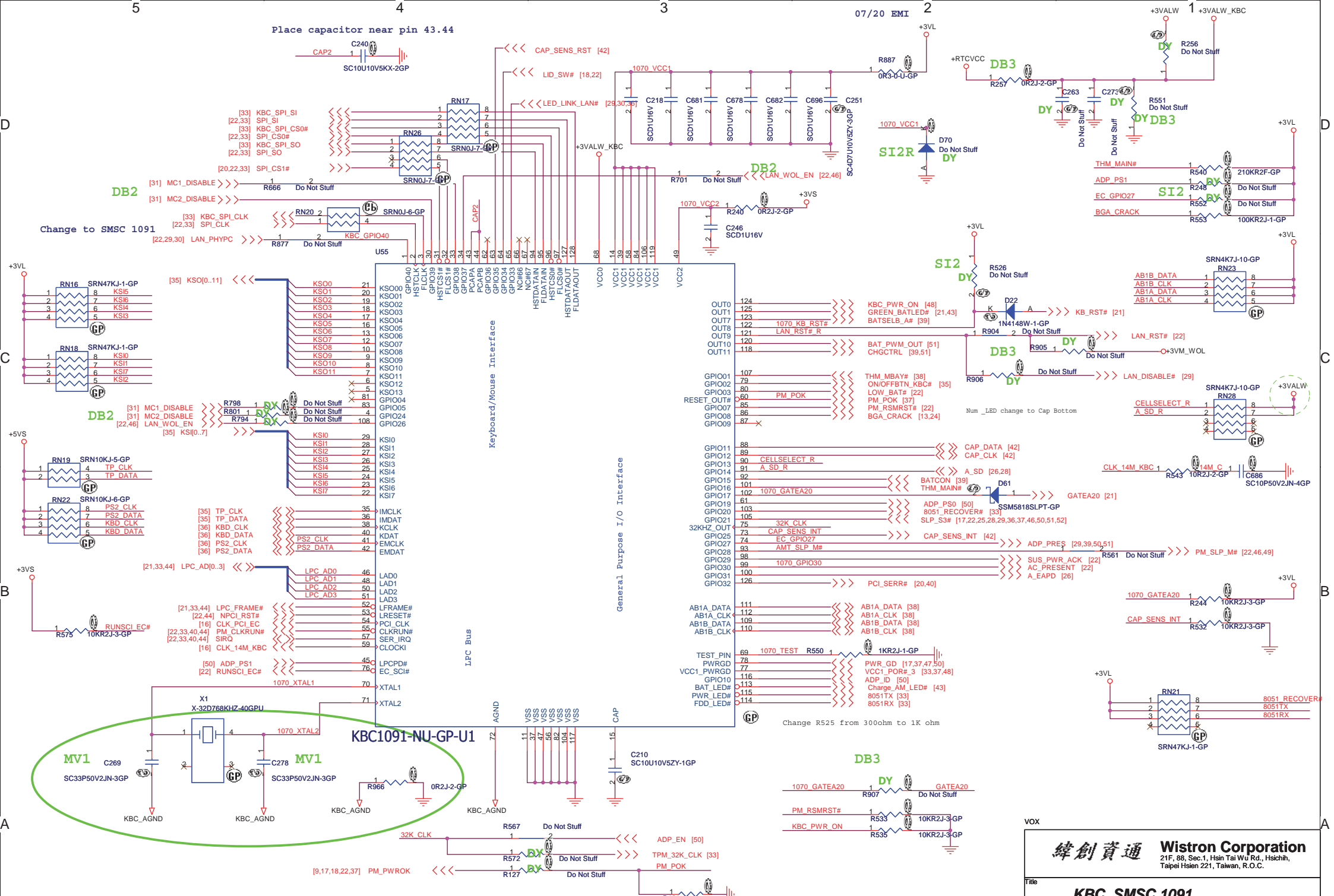
Title: **USB Connector**

Size A3 Document Number **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 32 of 53







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VOX

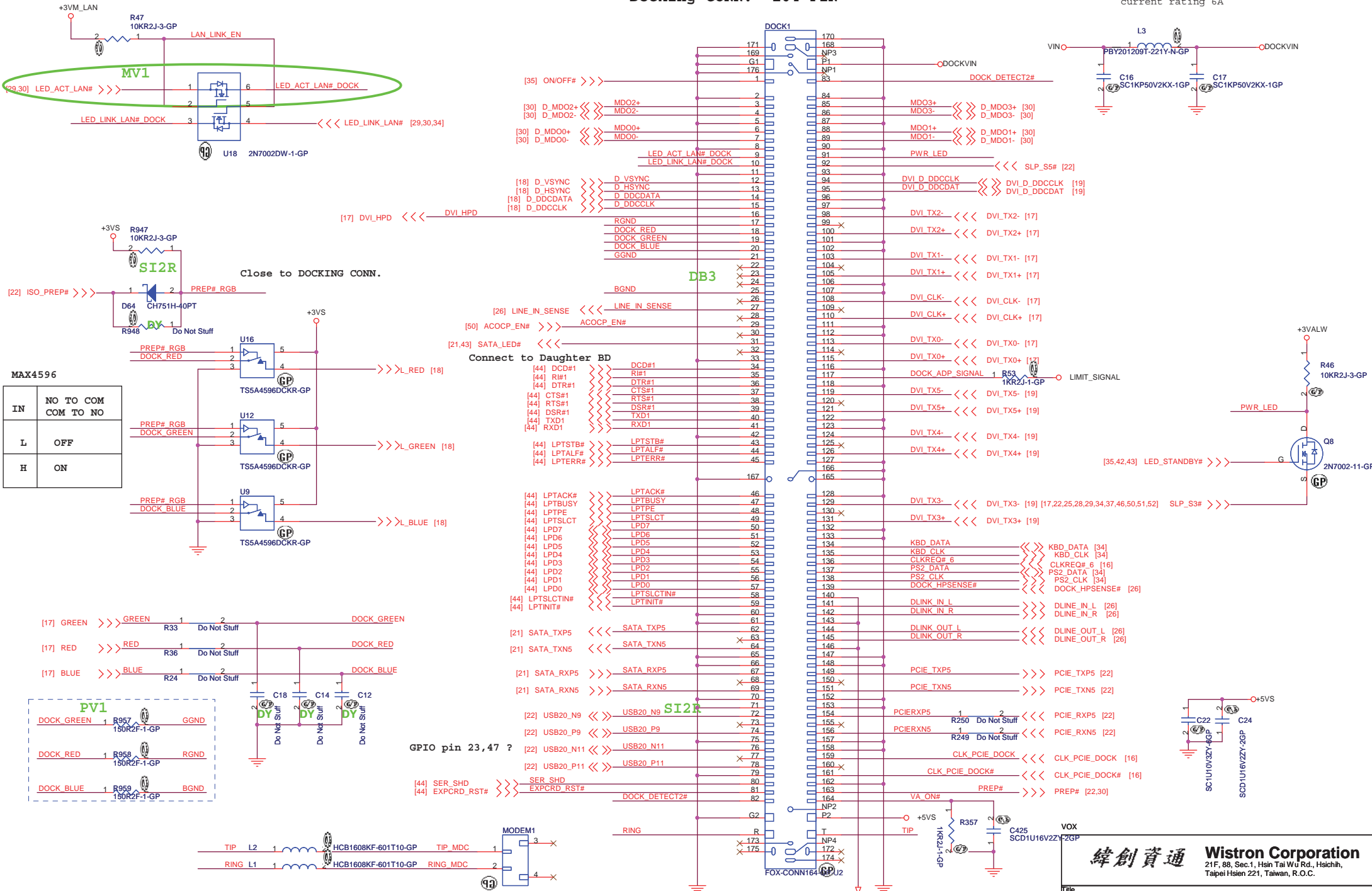
**緯創資通** **Wistron Corporation**  
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Title		KBC SMSC 1091	
Size	A3	Document Number	Artemis
Date:	Wednesday, August 20, 2008	Sheet	34 of 53
Rev	3		



# Docking CONN. 164 PIN

current rating 6A



Layout Notes :  
Place MODEM1 & BEAD near Docking connector

For TII and Ring cut all layers

<http://laptop-motherboard-schematic.blogspot.com/>

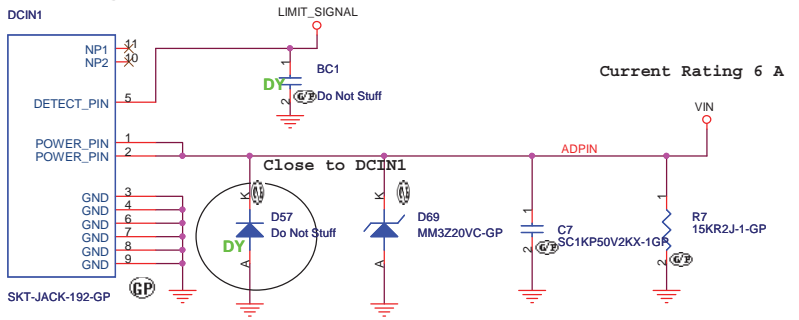
緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**Docking CONN**

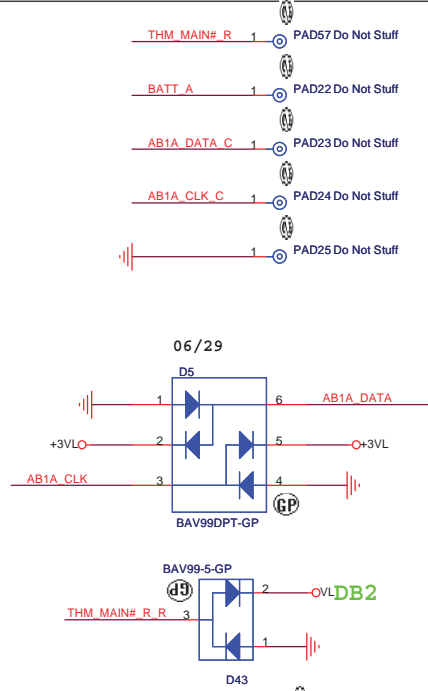
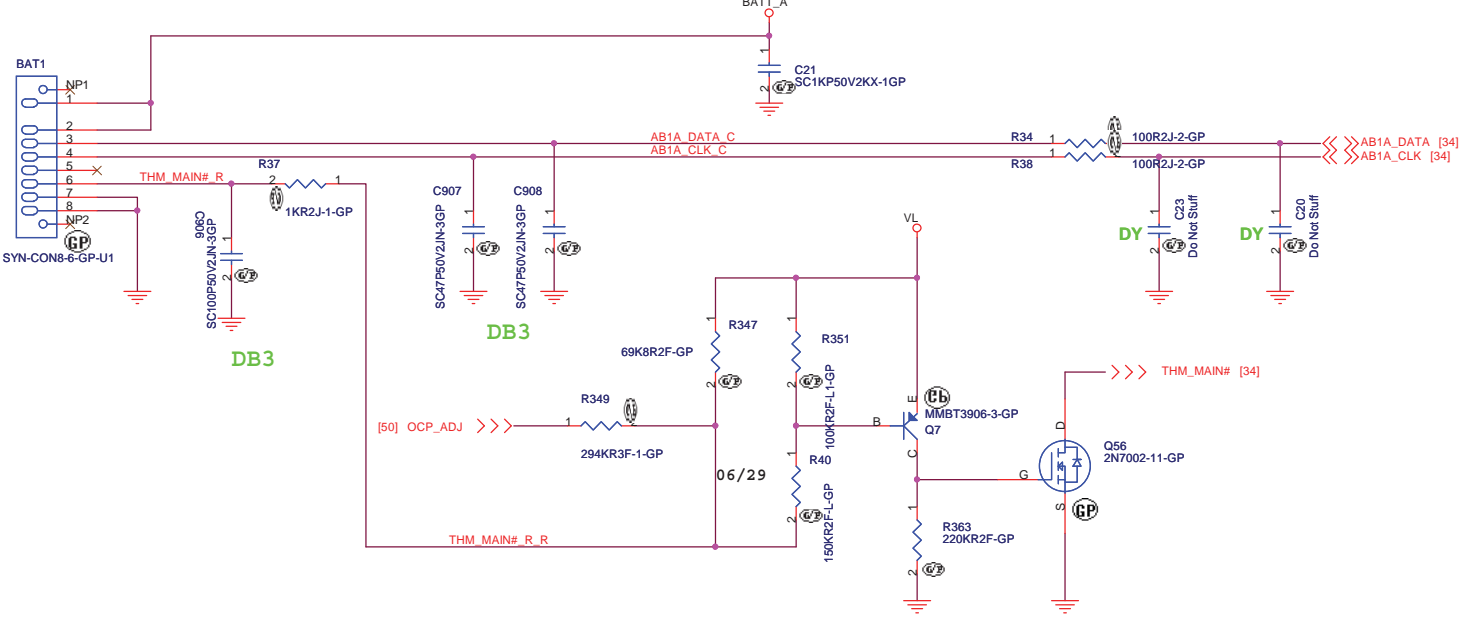
Size A3	Document Number	Artemis	Rev 3
Date: Wednesday, August 20, 2008	Sheet 36	of	53



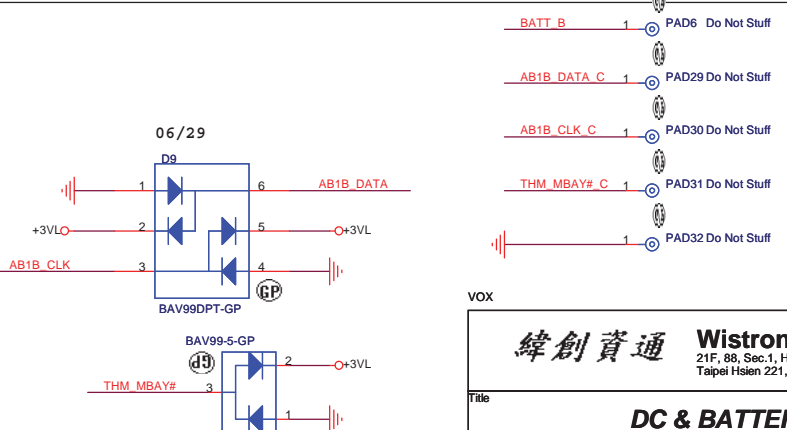
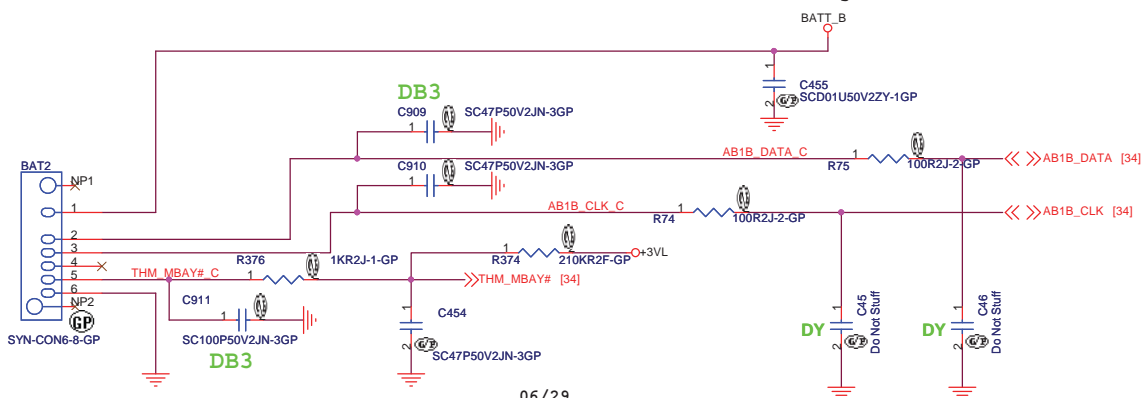
# Adaptor in to generate DCBATTOUT



# MAIN BATTERY CONNECTOR



# BAY BATTERY CONNECTOR



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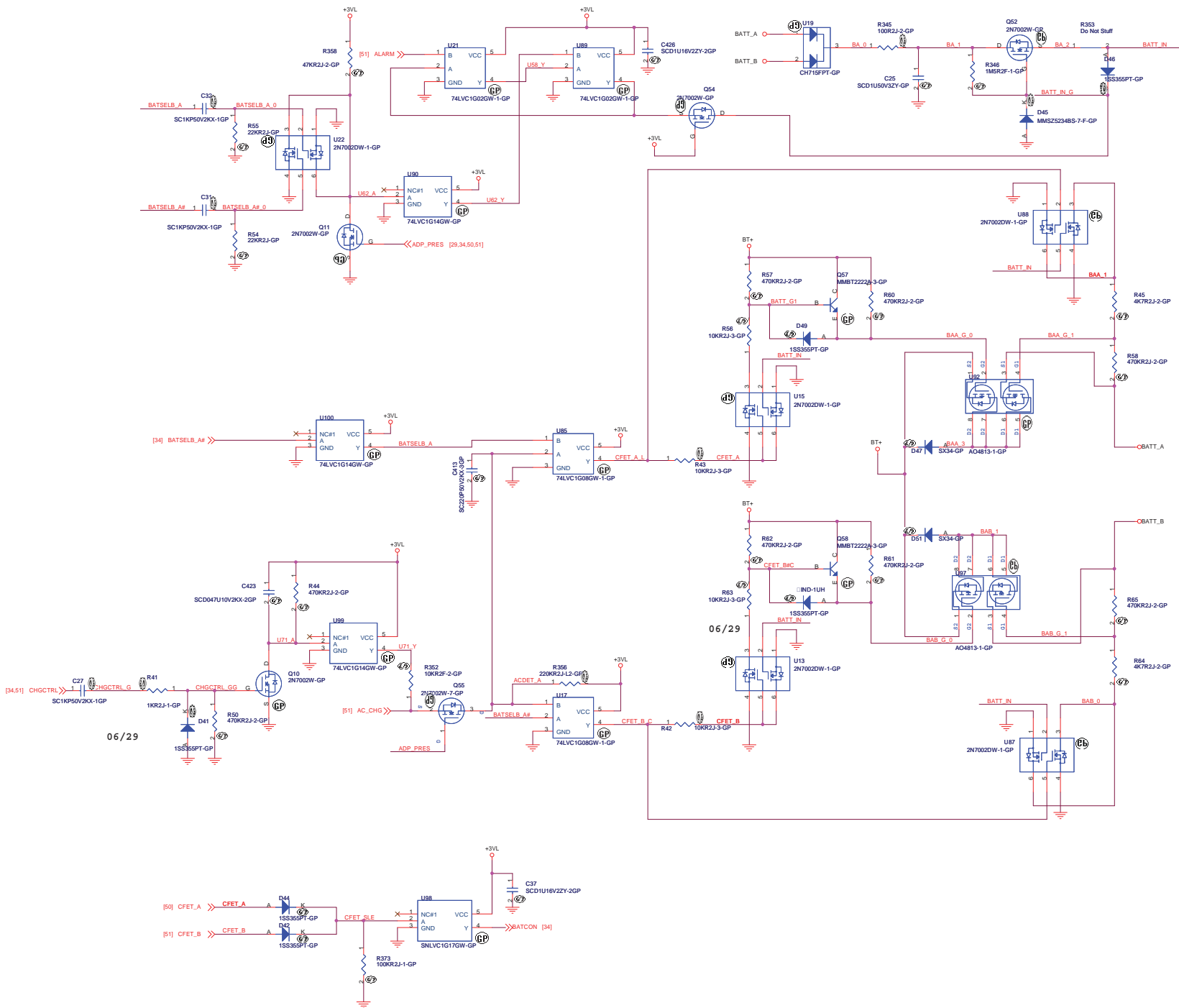
VOX

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Title: **DC & BATTERY CONN.**

Size A3 Document Number **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 38 of 53



<http://laptop-motherboard-schematic.blogspot.com/>

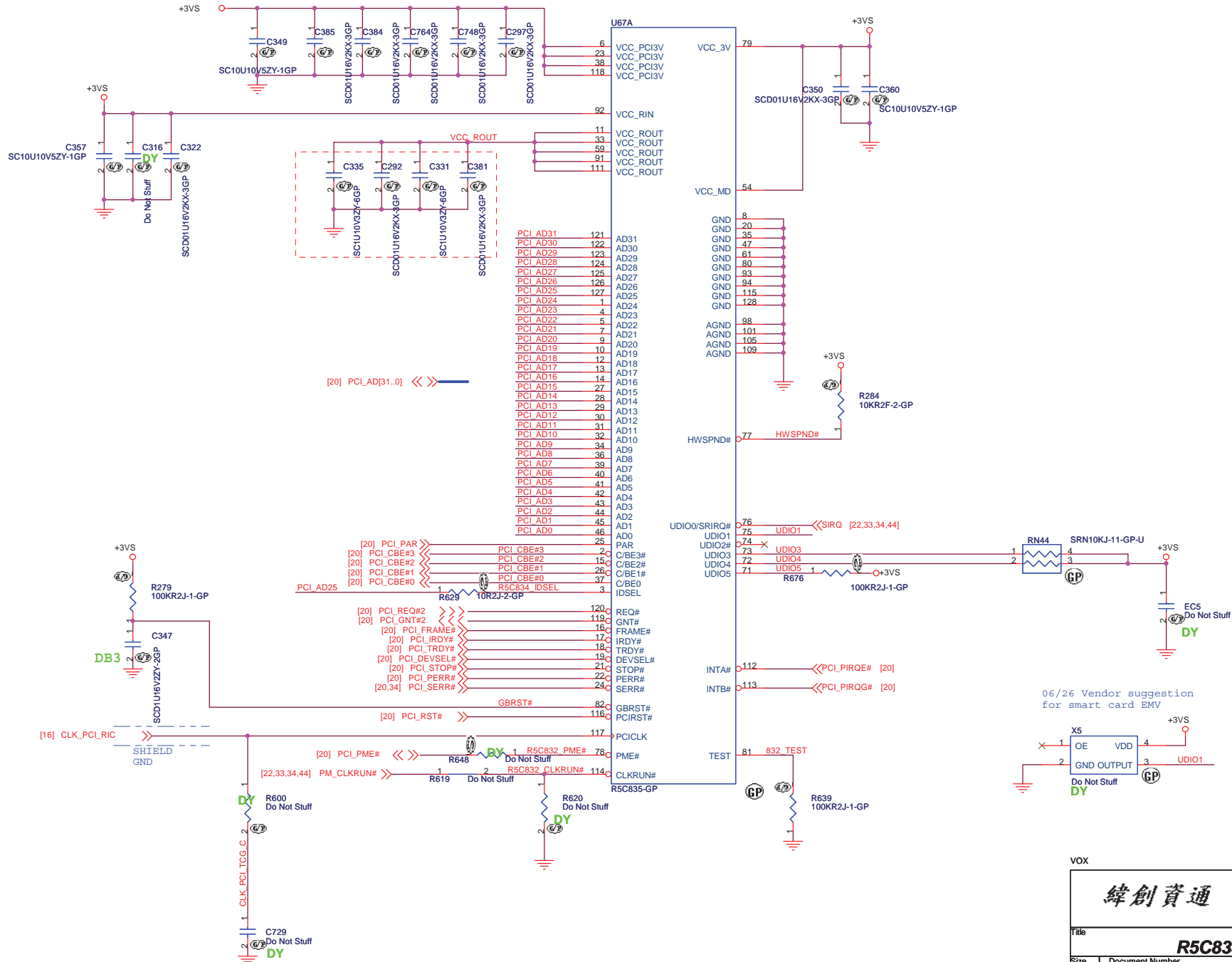
File		Rev	
Size		Date	
K2		2008	
Document Number		Sheet 39 of 53	
Artemis		3	
Date: Wednesday, August 20, 2008			

緯創資通 Wistron Corporation  
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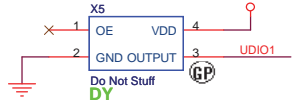
**Battery Selector**

Artemis

# RICOH R5C835 (1 OF 2) PCI



06/26 Vendor suggestion for smart card EMV



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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C835/PCI**

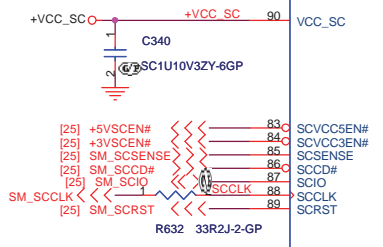
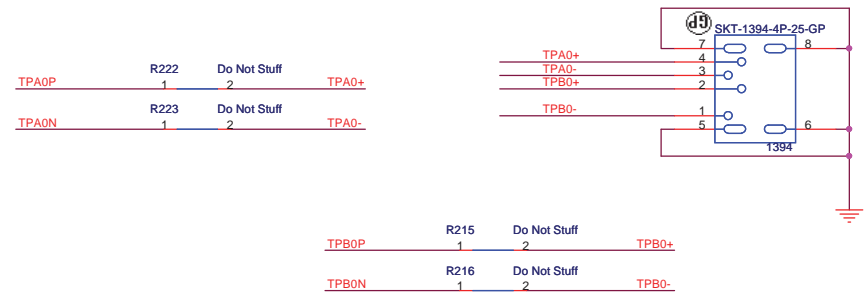
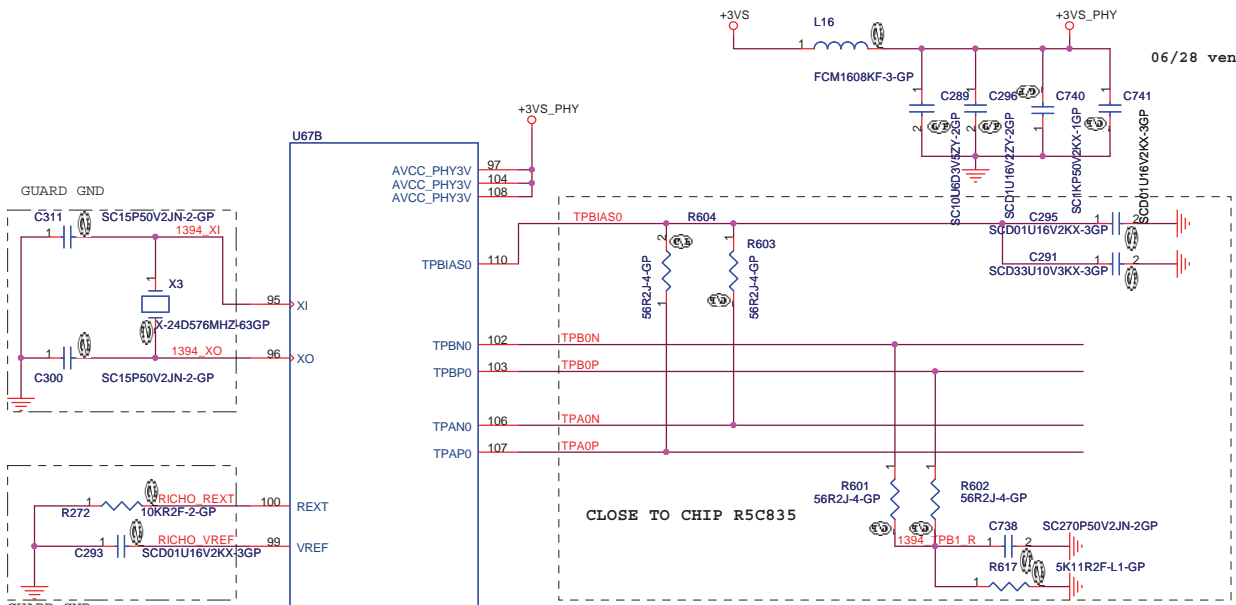
Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008		Sheet 40 of 53



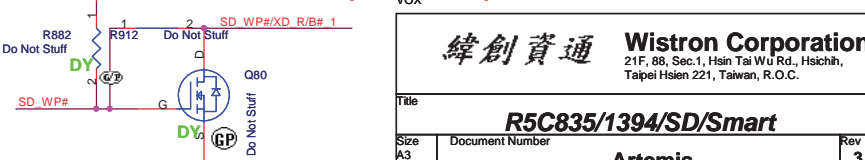
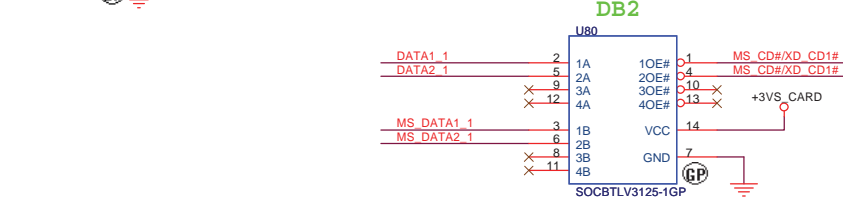
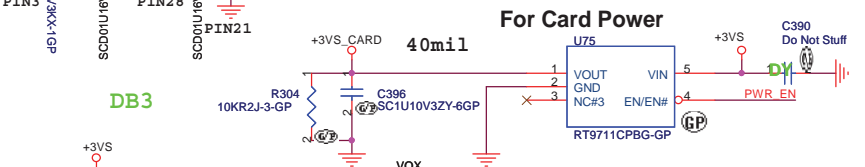
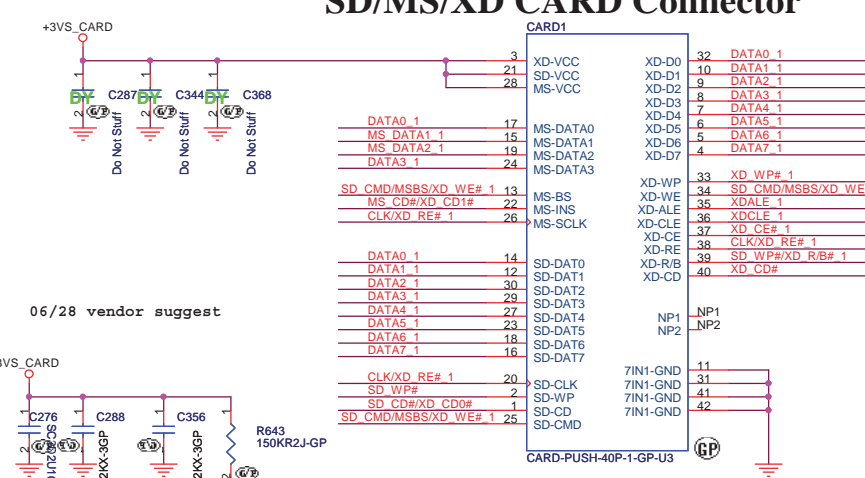
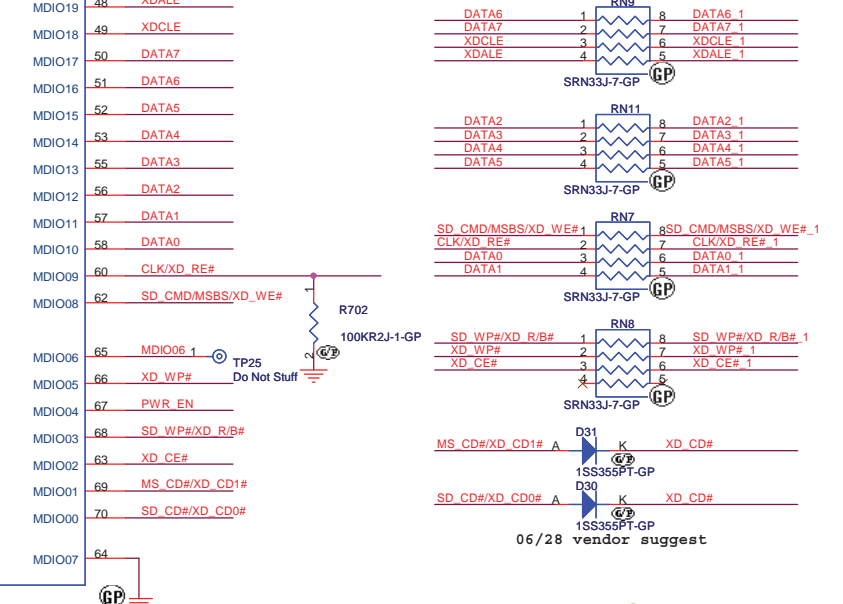
# RICOH R5C835 (2 OF 2)

Layout notes :  
1394

-----GND  
-----TPB0-  
-----TPB0+  
-----GND  
-----TPA0-  
-----TPA0+  
-----GND



Layout notes :  
external parts for  
VREF, REXT and FIL0 as  
close as possible to R5C835.

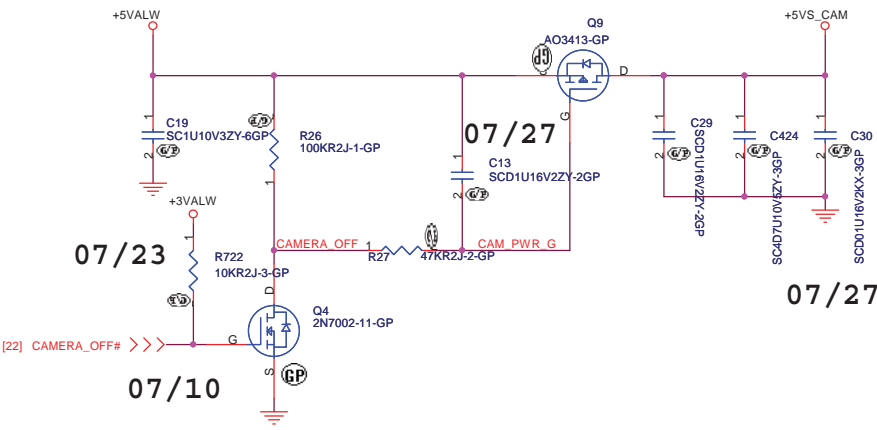


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

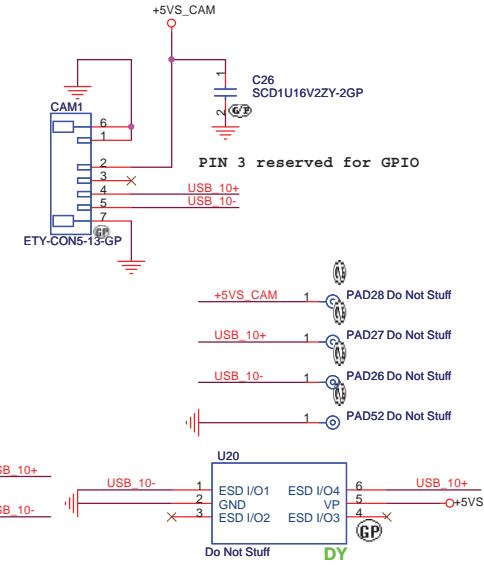
**R5C835/1394/SD/Smart**

File	Document Number	Rev
		<b>3</b>
Size	<b>Artemis</b>	
A3	Date: Wednesday, August 20, 2008	Sheet 41 of 53

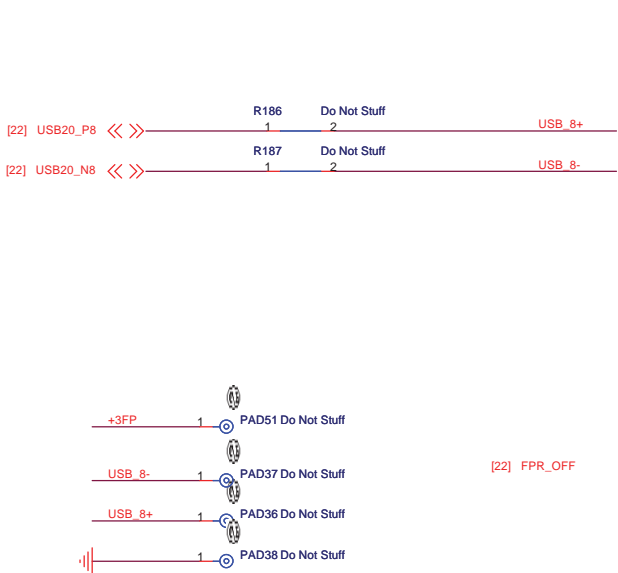
# CAMERA



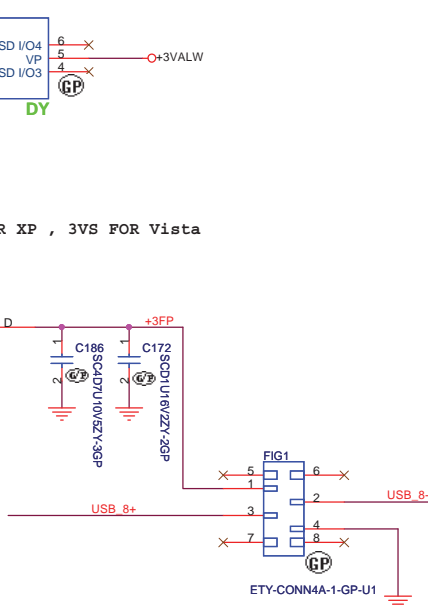
# CAMERA Conn.



# FingerPrint



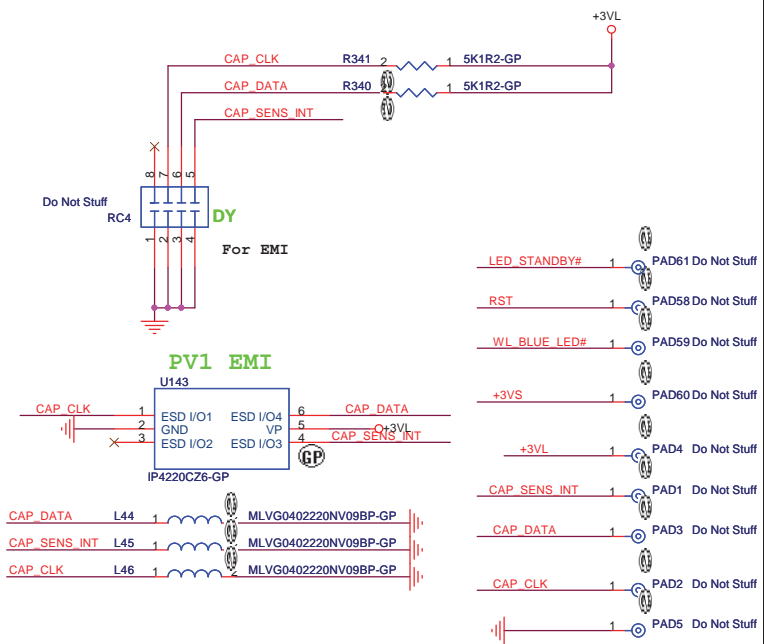
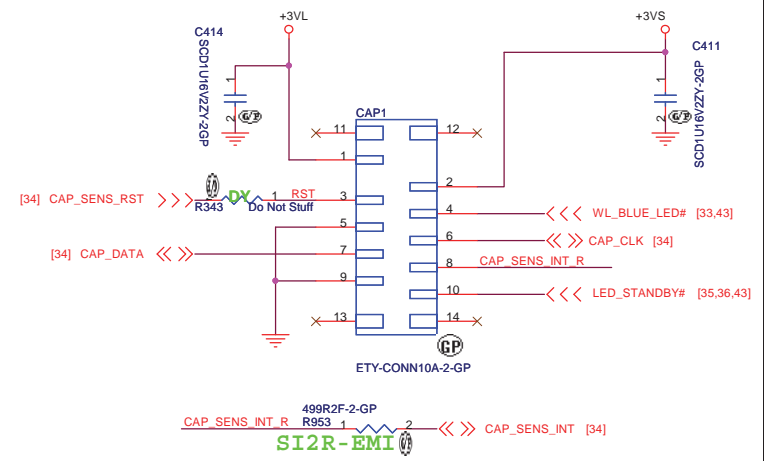
# FingerPrint Conn.



# SYSTEM CAPACITY BOARD

Vol up , Vol down , Mute , Presentation

PIN 3 reserved for GPIO



VOX

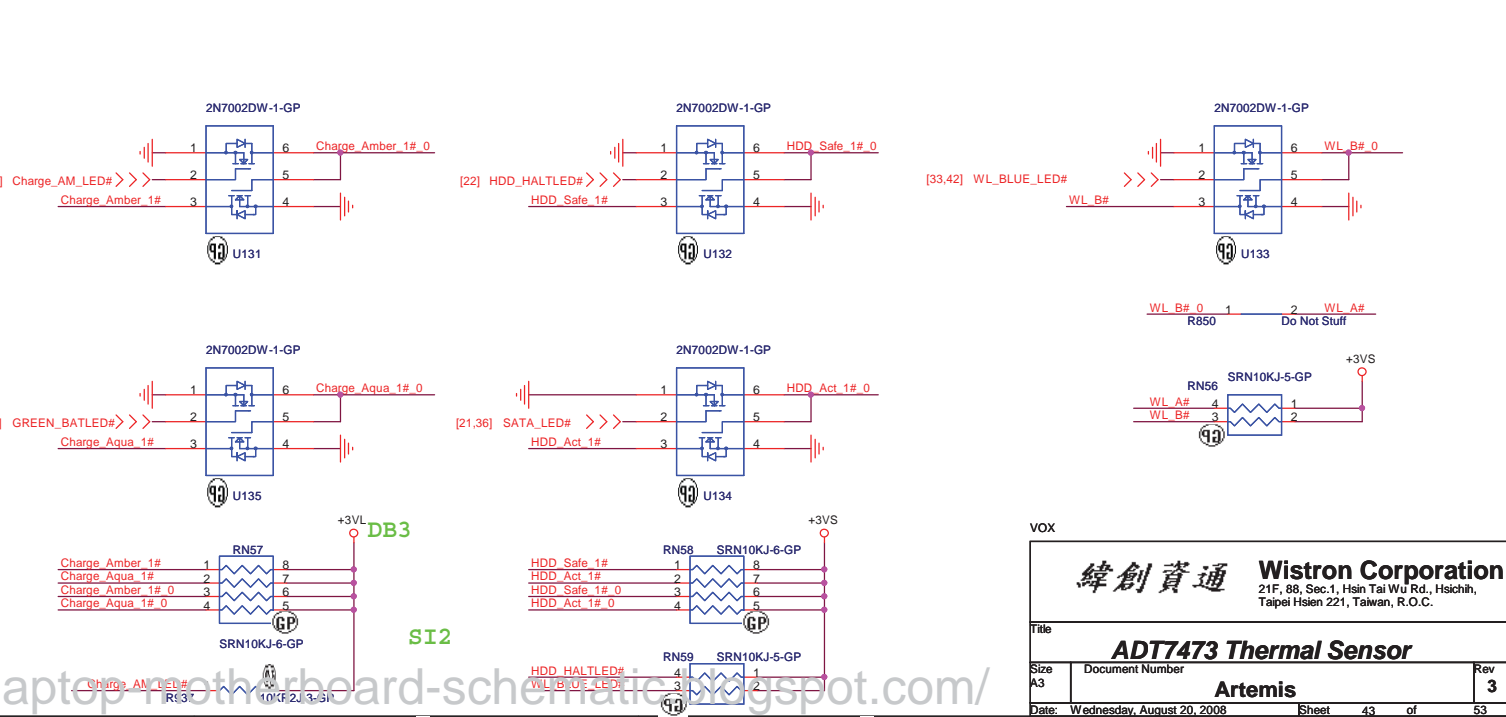
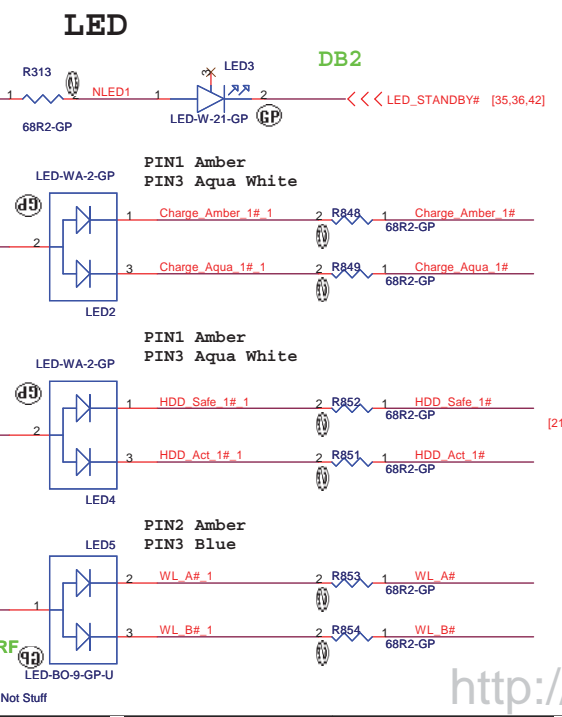
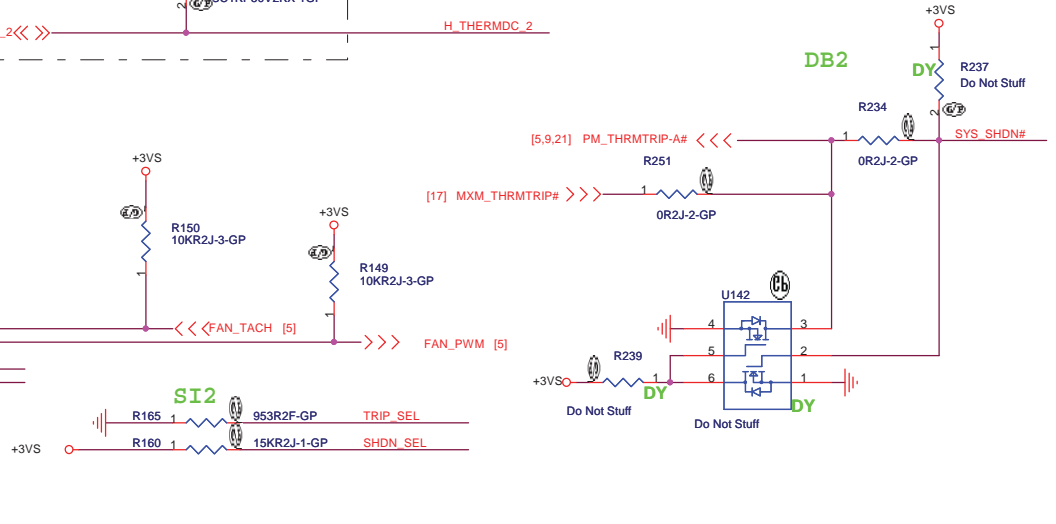
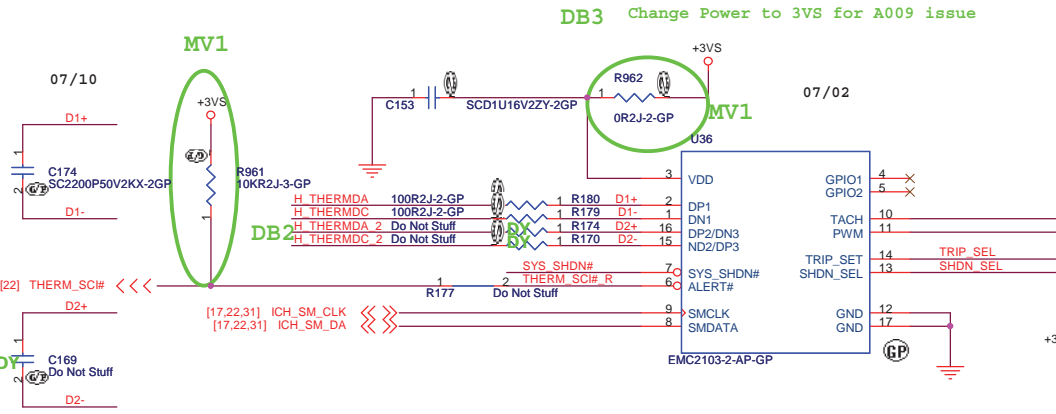
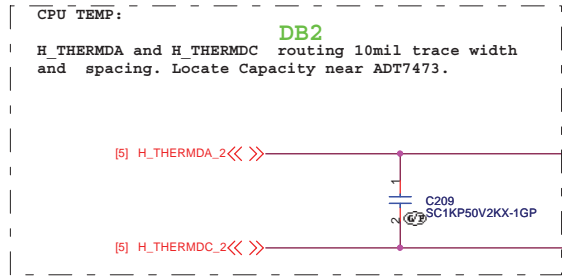
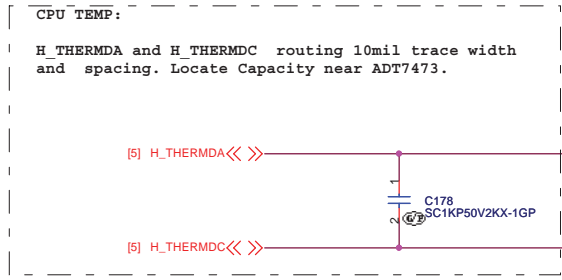
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Title: **Camera/W-COM**

Size: A3 Document Number: **Artemis** Rev: **3**

Date: Wednesday, August 20, 2008 Sheet: 42 of 53

# Thermal Sensor



VOX

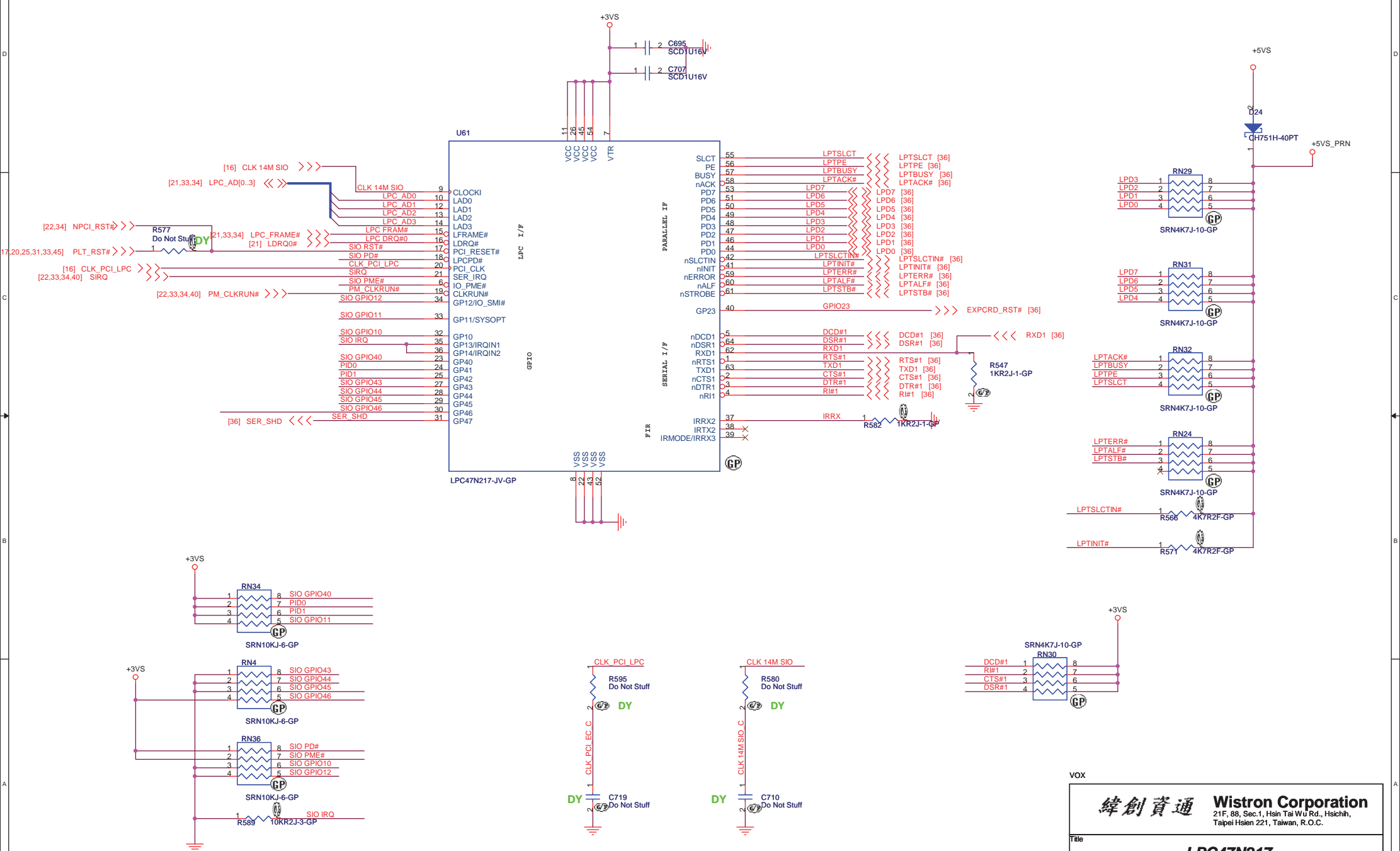
**緯創資通 Wistron Corporation**  
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Title: **ADT7473 Thermal Sensor**

Size A3 Document Number **Artemis** Rev **3**

Date: Wednesday, August 20, 2008 Sheet 43 of 53

# SIO



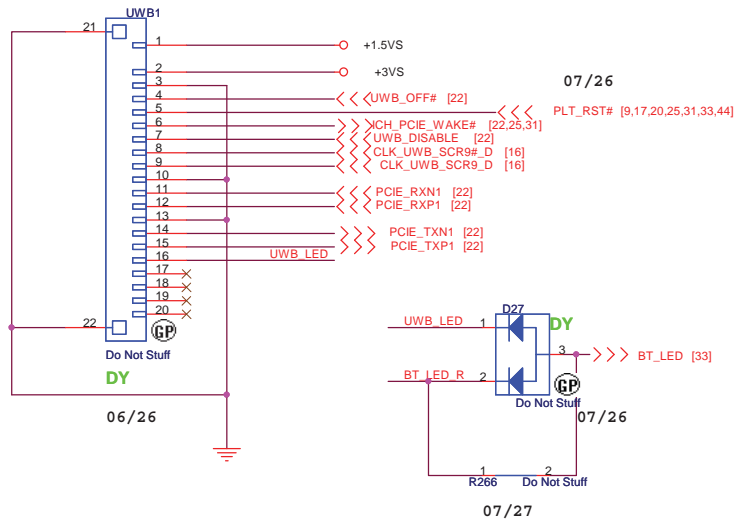
VOX

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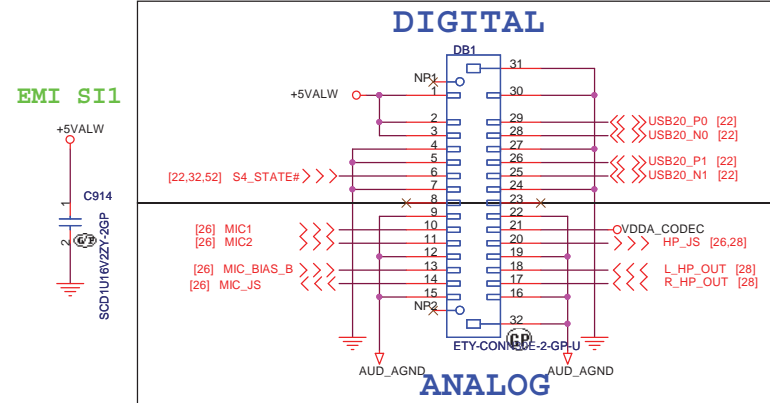
Title: **LPC47N217**

Size A3	Document Number	Rev <b>3</b>
Date: Wednesday, August 20, 2008		Sheet 44 of 53

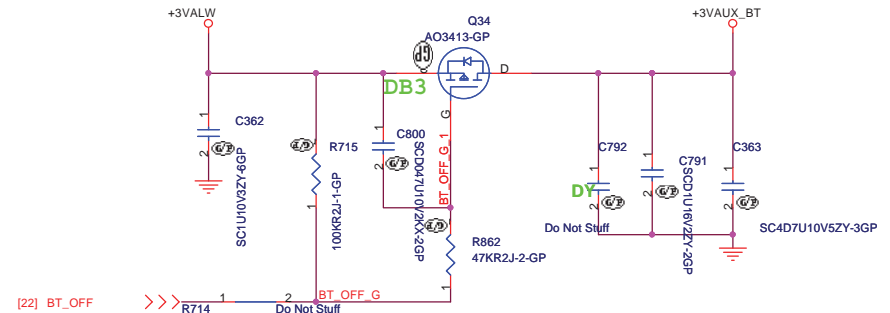
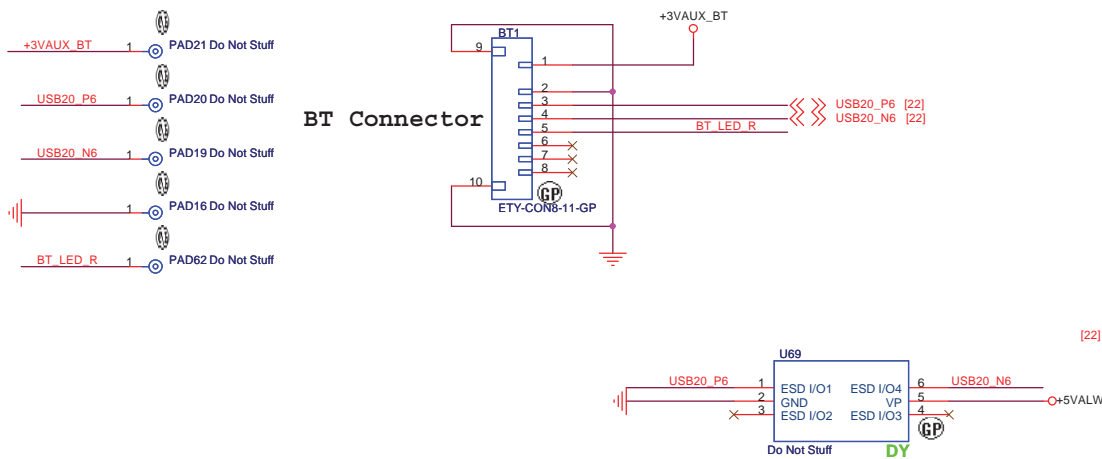
### UWB Connector



### AUDIO Daughter Board Connector



### Bluetooth Connector

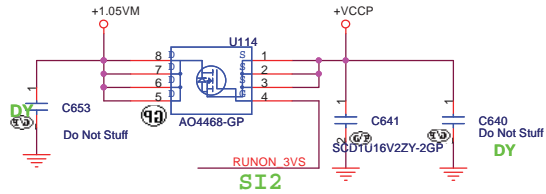


VOX

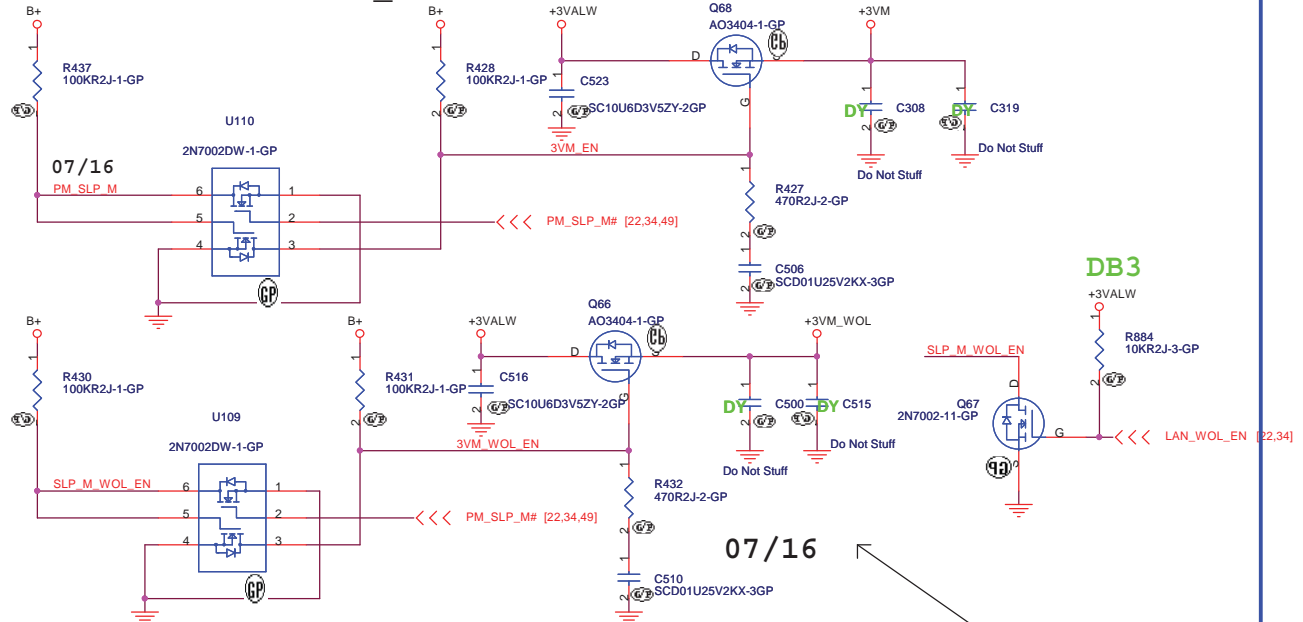
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>BT/UWB/Audio board Connector</b>		
Size A3	Document Number <b>Artemis</b>	Rev <b>3</b>
Date: Wednesday, August 20, 2008		Sheet 45 of 53

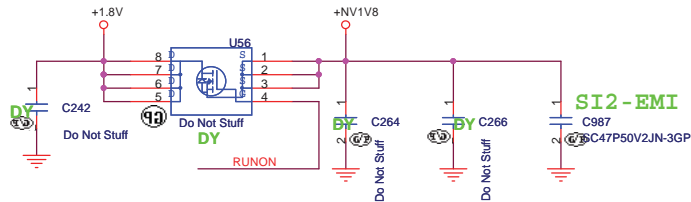
### +1.05VM to +VCCP Transfer



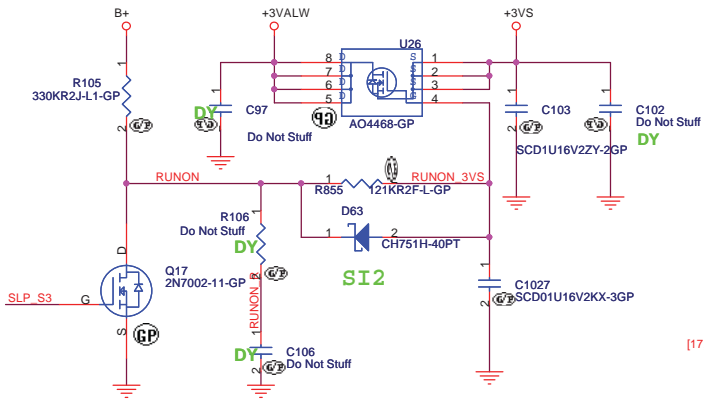
### +3VALW to +3VM / +3VM\_WOL Transfer



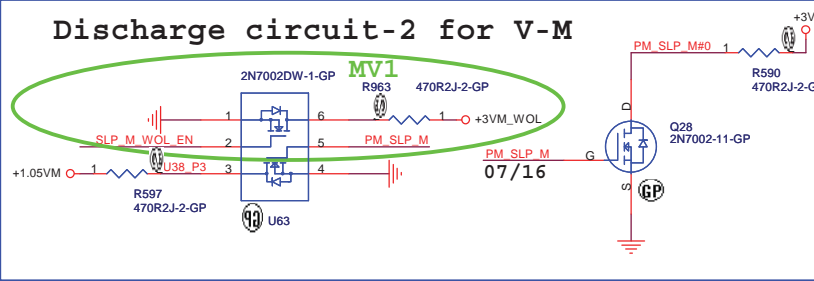
### +1.8V to +1.8VS Transfer



### +3VALW to +3VS Transfer

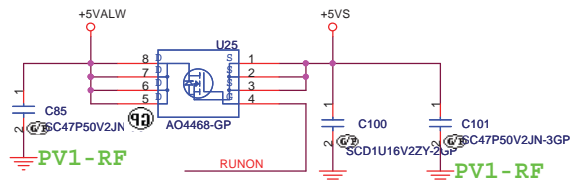


### Discharge circuit-2 for V-M

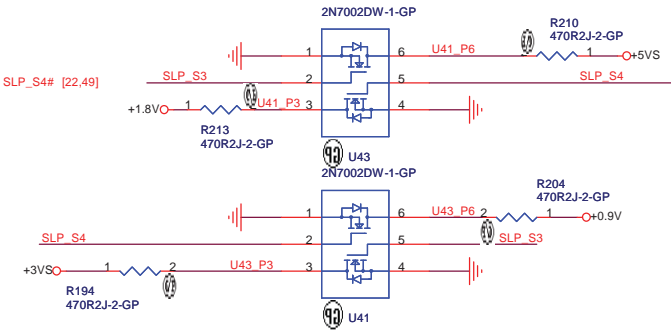
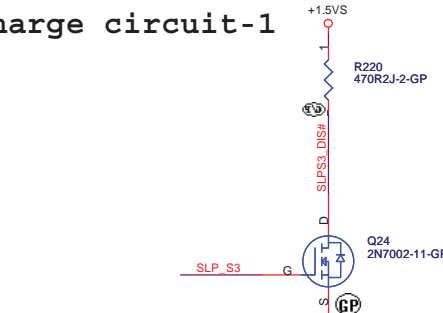


PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	MoIff / No WOL
0	1	3.3V	0V	Legacy WOL/ MoEff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

### +5VALW to +5VS Transfer



### Discharge circuit-1

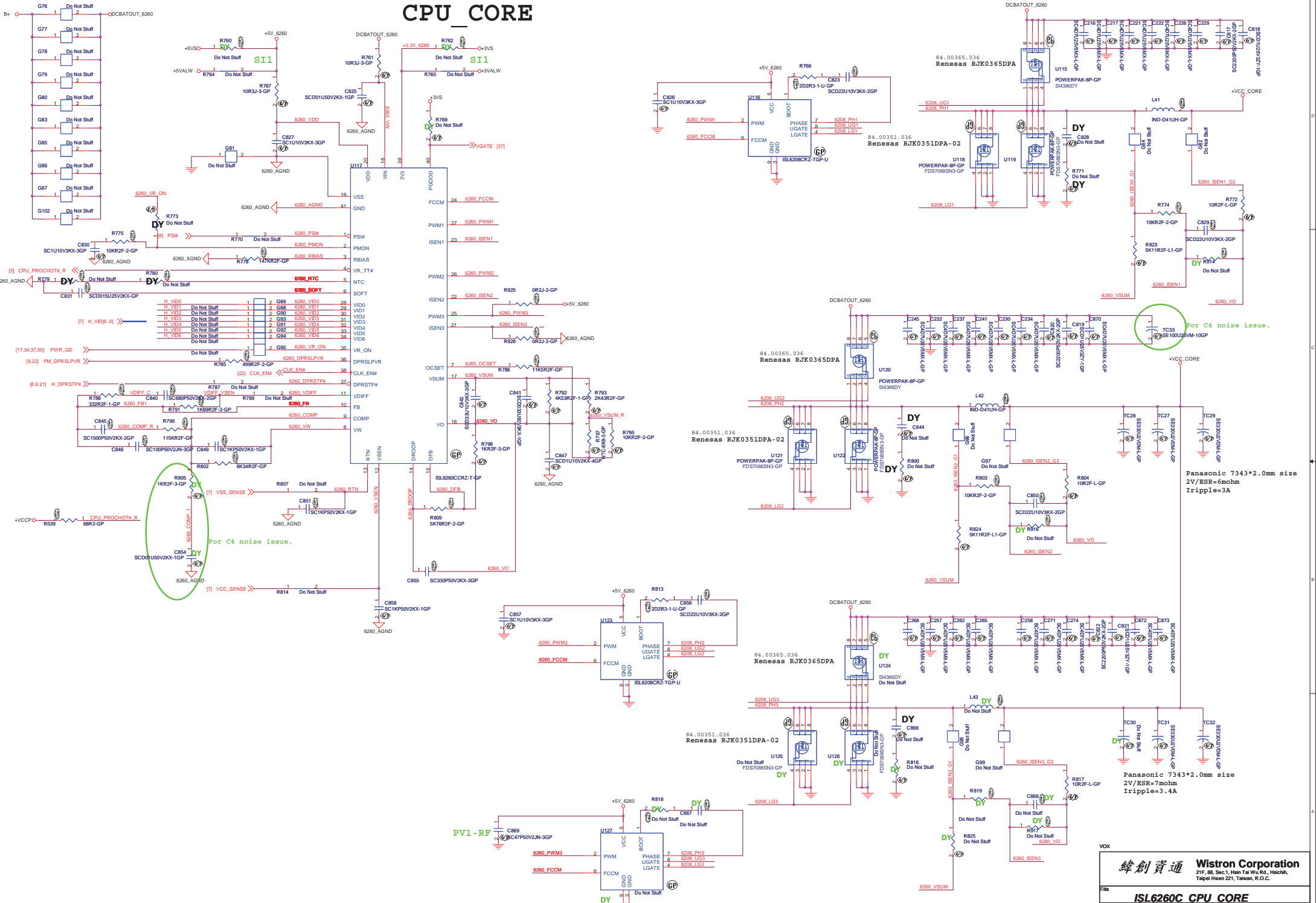


VOX

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Title		
DC/DC Circuit		
Size A3	Document Number	Rev 3
Date: Wednesday, August 20, 2008		Sheet 46 of 53

# CPU\_CORE



<http://laptop-motherboard-schematic.blogspot.com/>

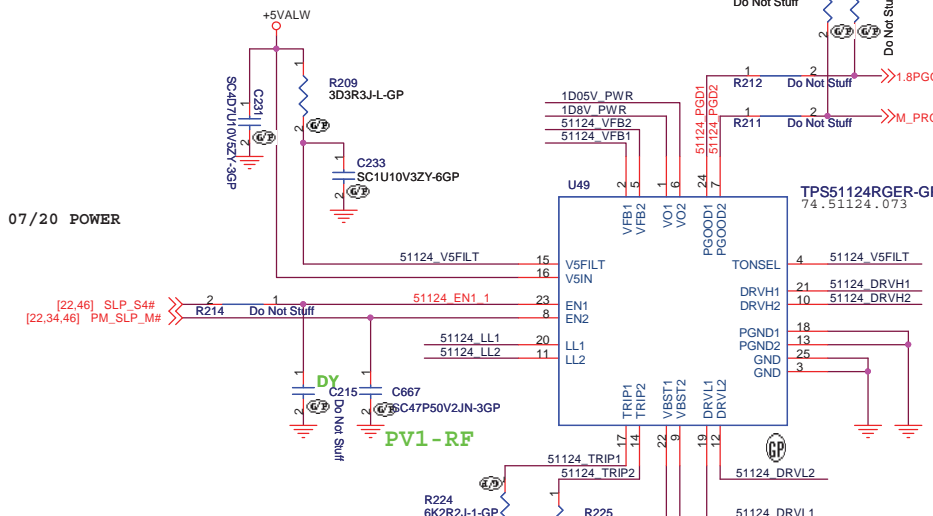
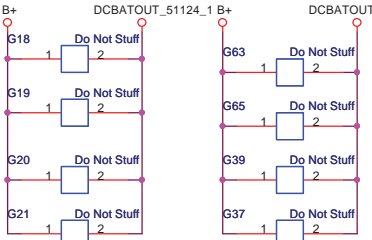
<b>緯創資通</b> Wistron Corporation 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.	
<b>ISL6260C CPU CORE</b>	
File	Rev <b>3</b>
Size	Document Number
Date: Wednesday, August 20, 2008	Sheet 47 of 53



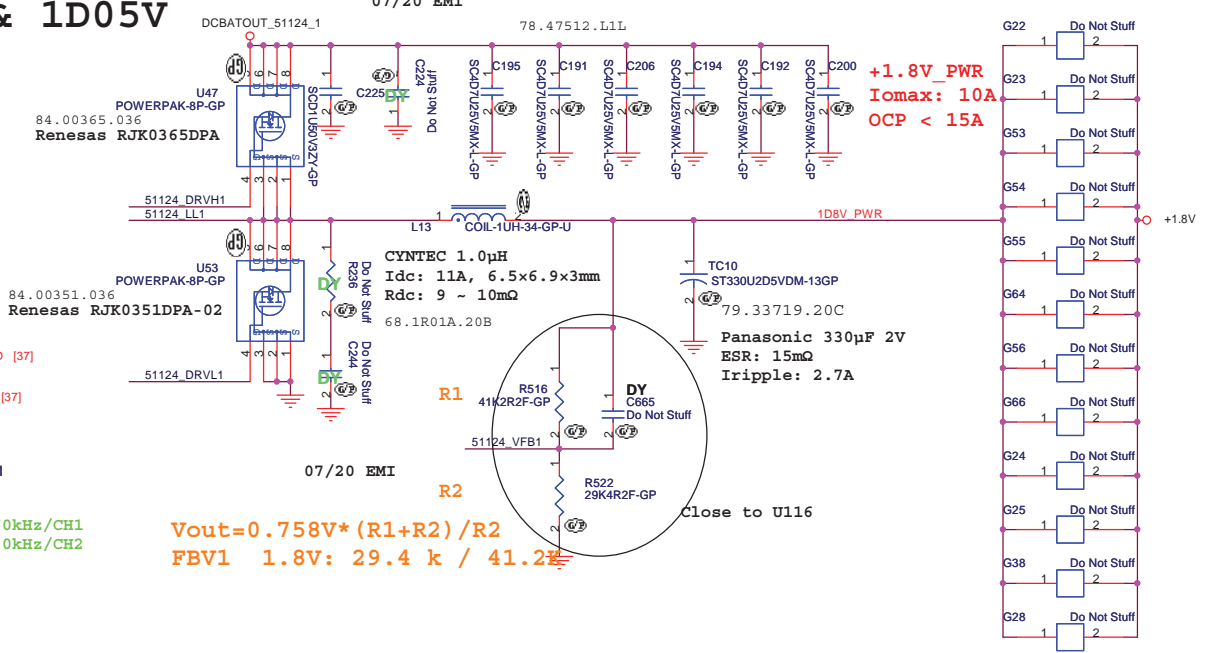
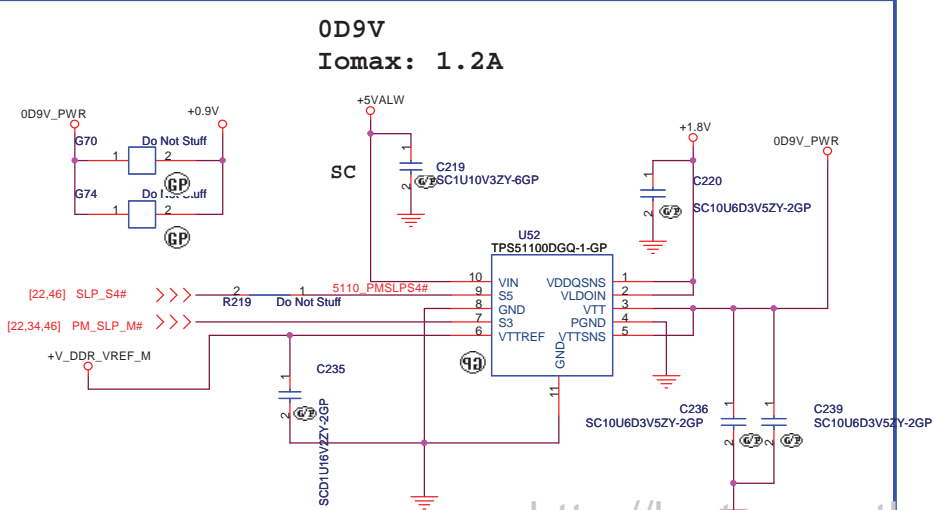


# 1D8V & 1D05V

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360kHz/CH1 420kHz/CH2

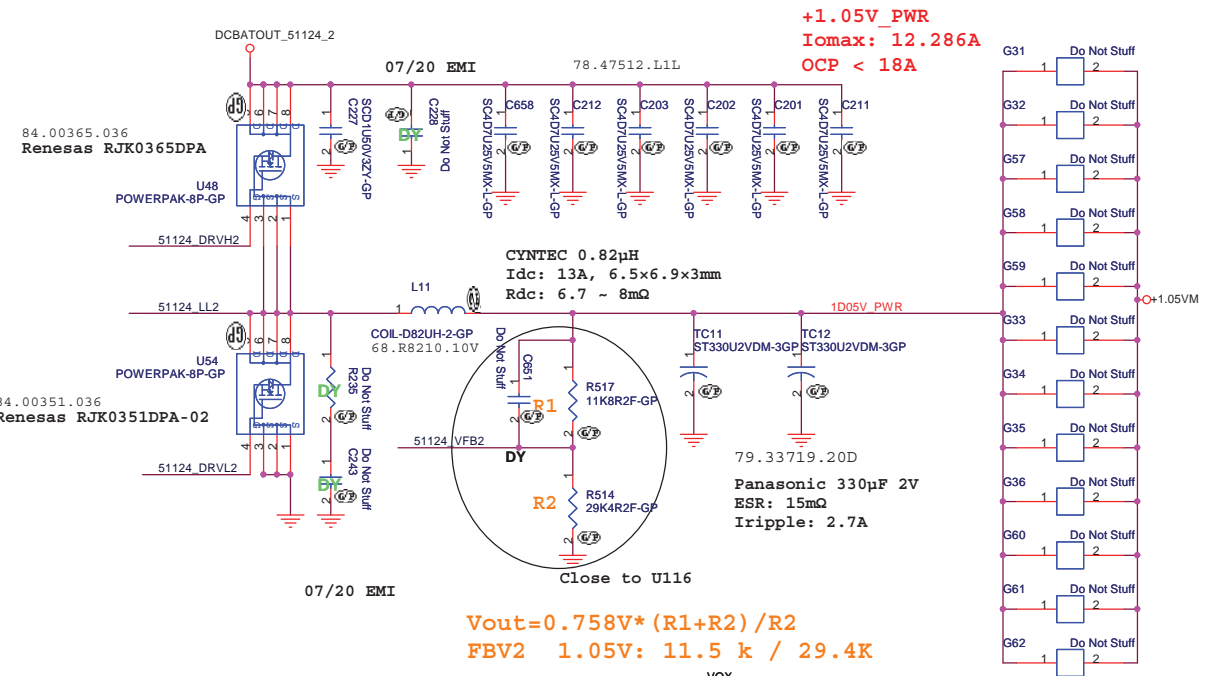


1.5V OCP: 12A, Trip1: 12K7  
1.05V OCP: 15A, Trip2: 7k5



$$V_{out} = 0.758V * (R1 + R2) / R2$$

$$FBV1 \ 1.8V: 29.4 \text{ k} / 41.2 \text{ k}$$



$$V_{out} = 0.758V * (R1 + R2) / R2$$

$$FBV2 \ 1.05V: 11.5 \text{ k} / 29.4 \text{ k}$$

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Title: **TPS51124 1D5V/1D05V**

Size A3	Document Number	Rev
	<b>Artemis</b>	<b>3</b>

Date: Wednesday, August 20, 2008 Sheet 49 of 53







