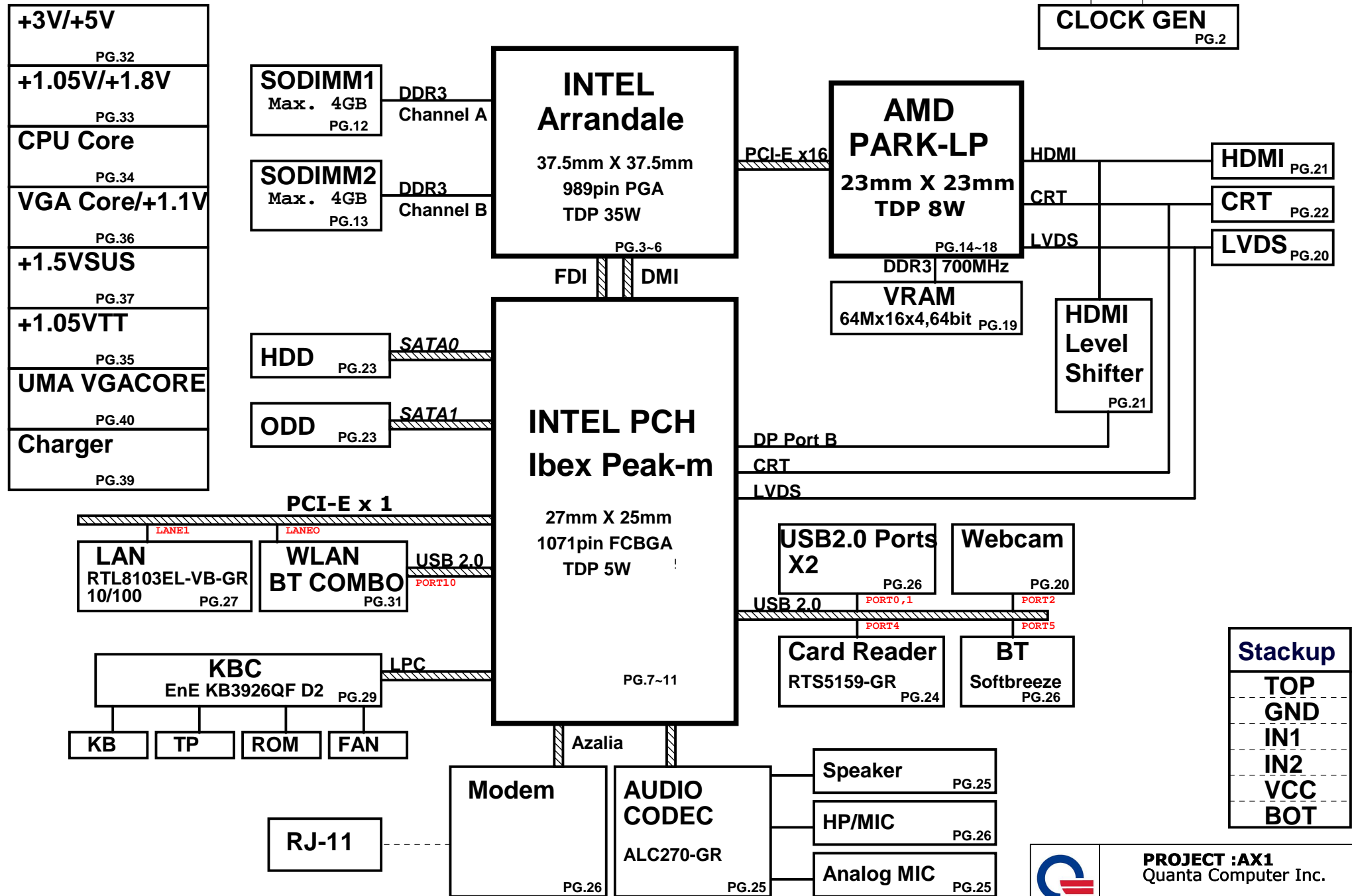
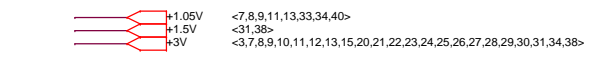
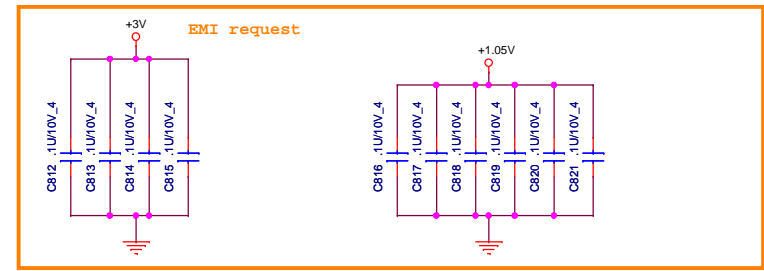
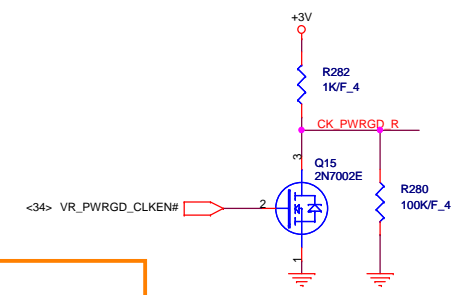
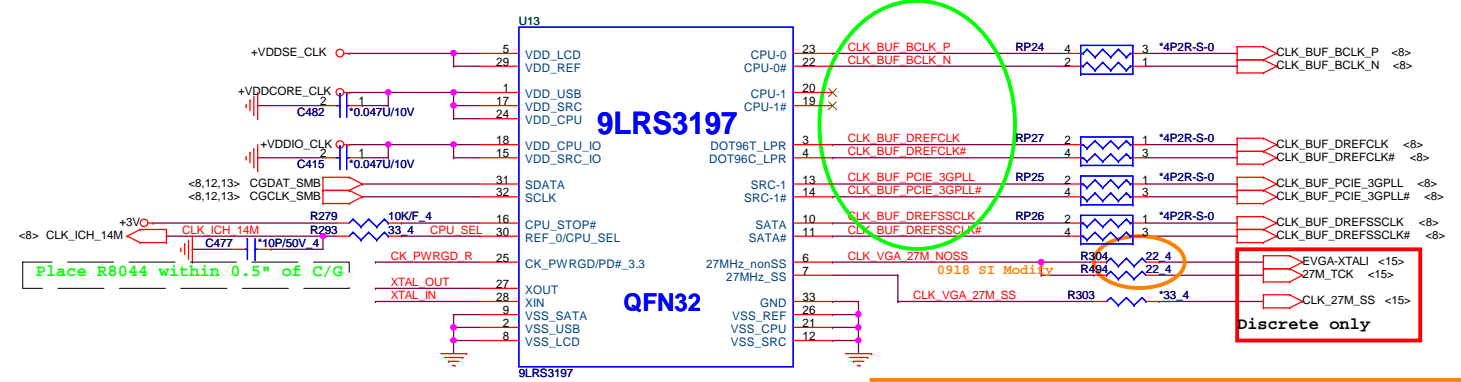
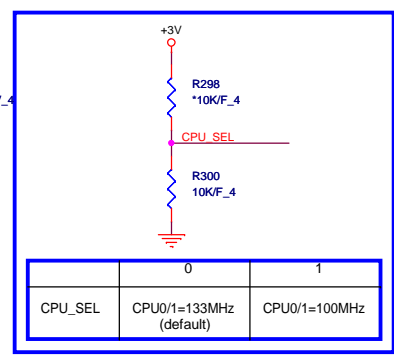
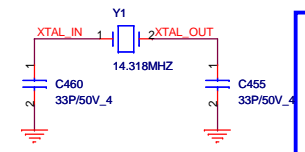
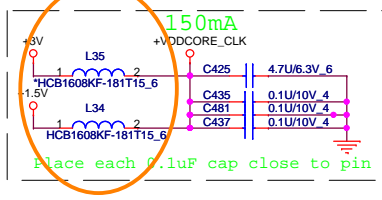
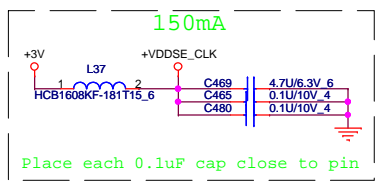
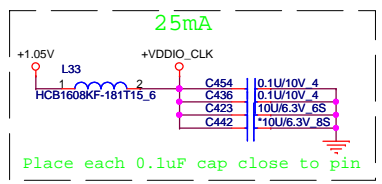


AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM

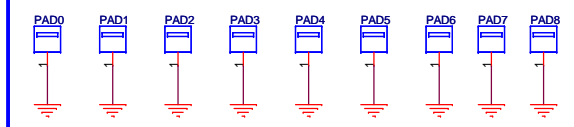
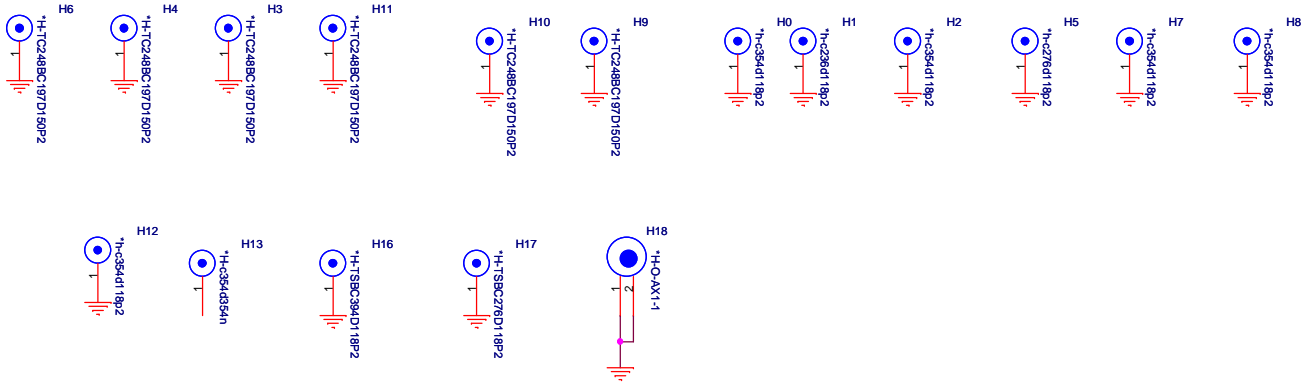


exaint@hotmail.com



CPU

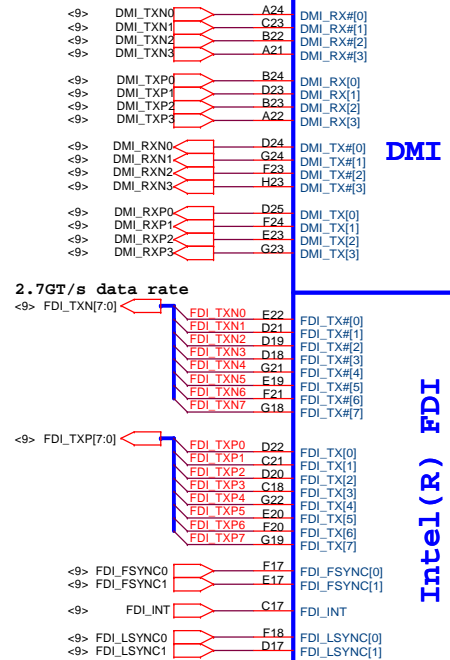
GPU



PROJECT :AX1
Quanta Computer Inc.

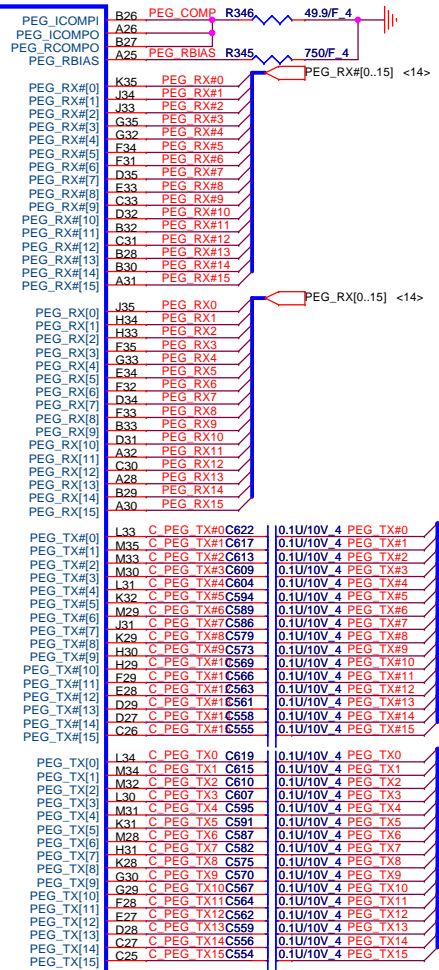
Ra	DIS	UMA
Rb	NA	0 ohm
Rc	0 ohm	NA

U16A

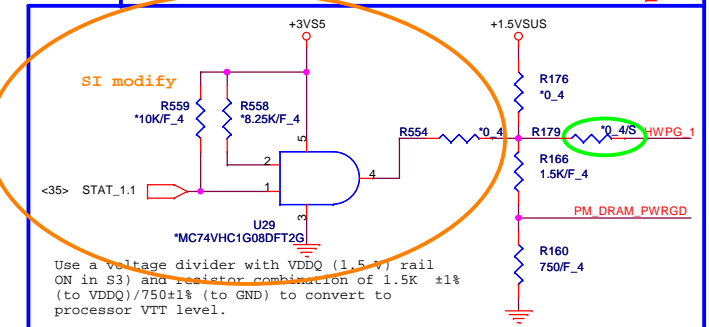
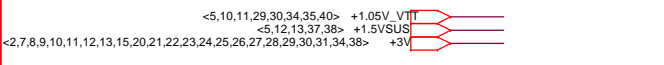
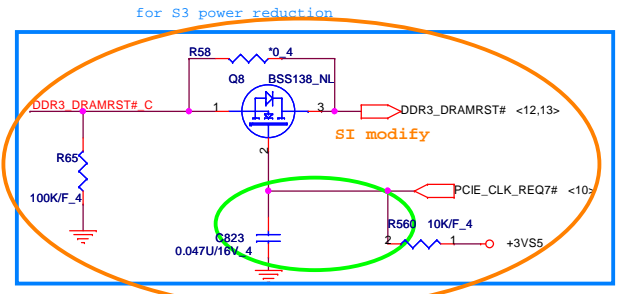
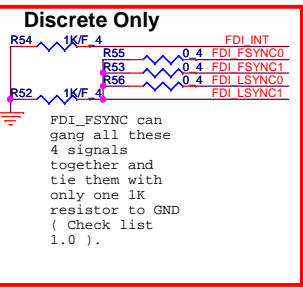


DMI

Intel(R) FDI
PCI EXPRESS -- GRAPHICS



IC_AUB_CFD_rPGA_R1P0



MISC

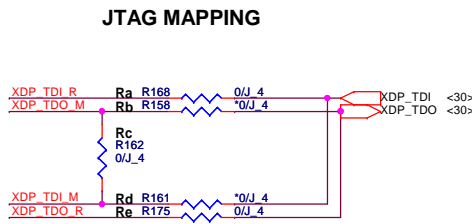
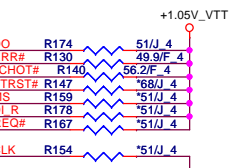
THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC_AUB_CFD_rPGA_R1P0

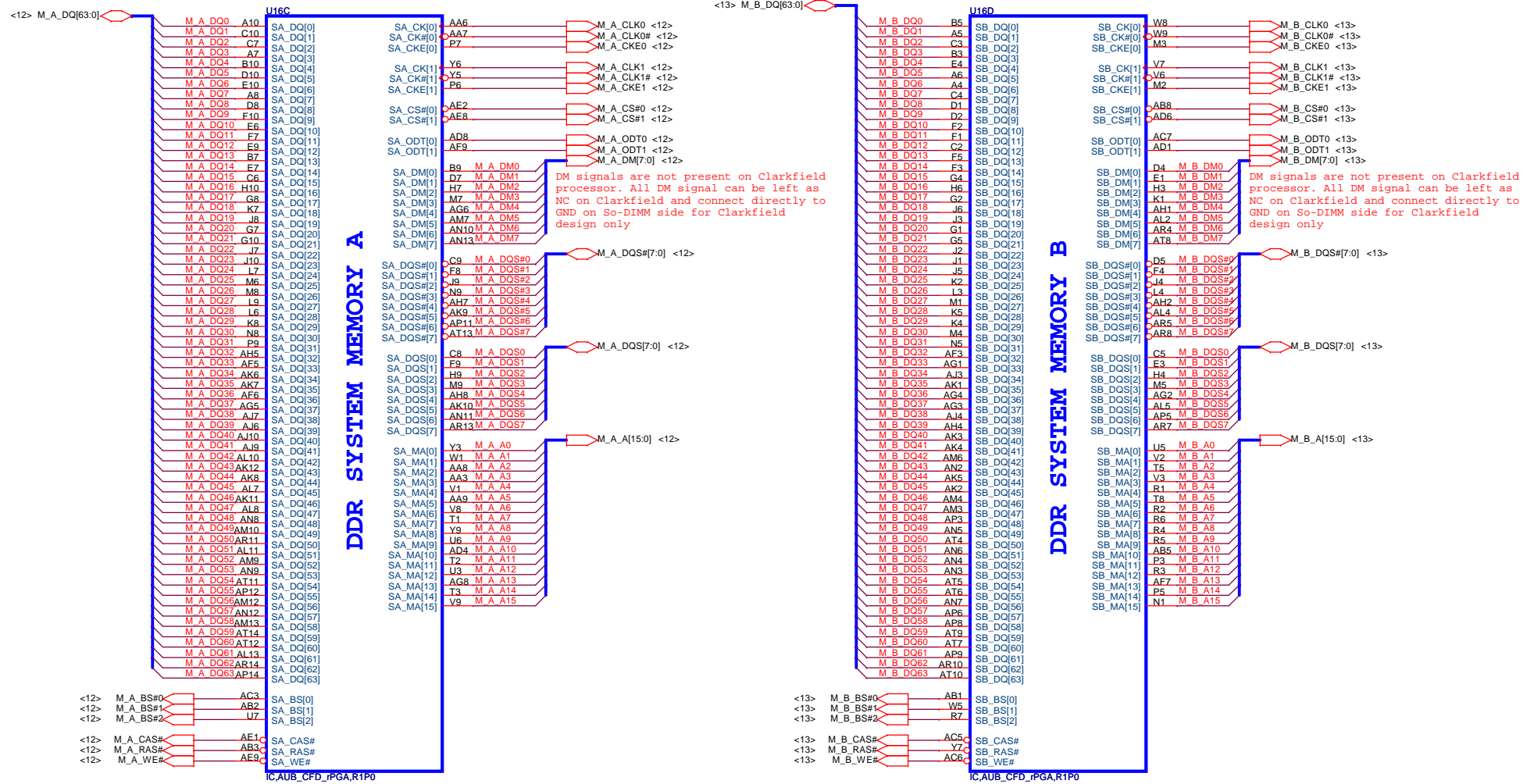


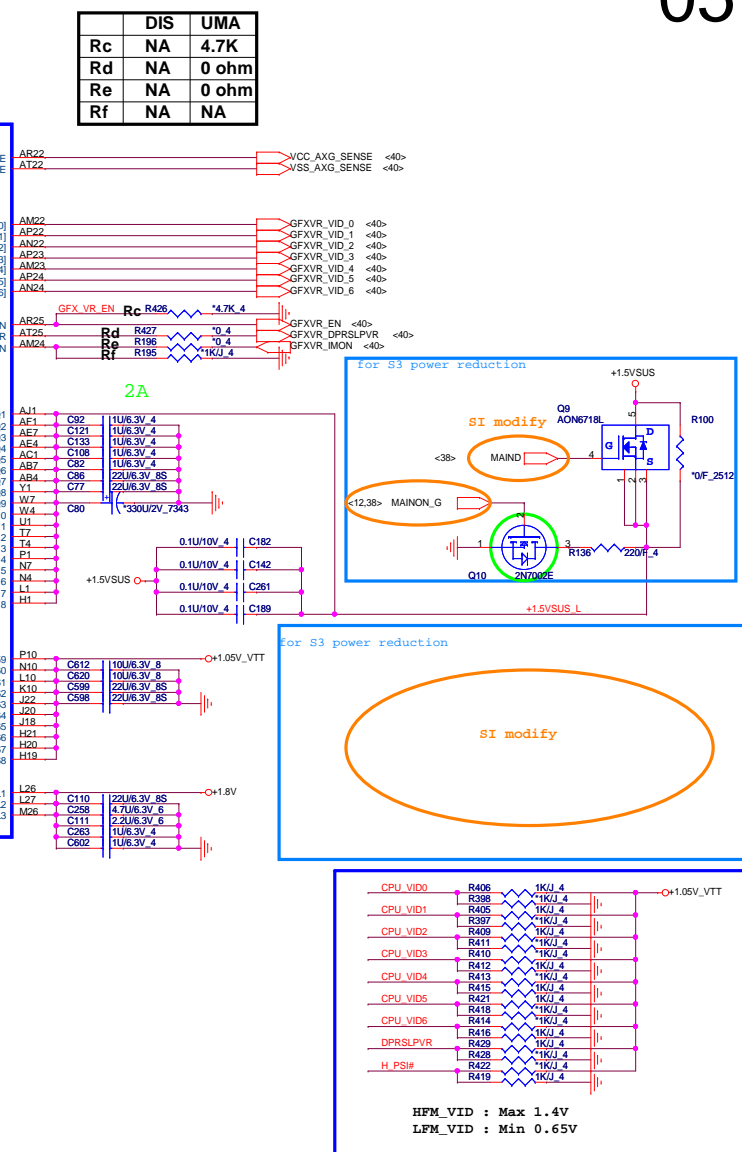
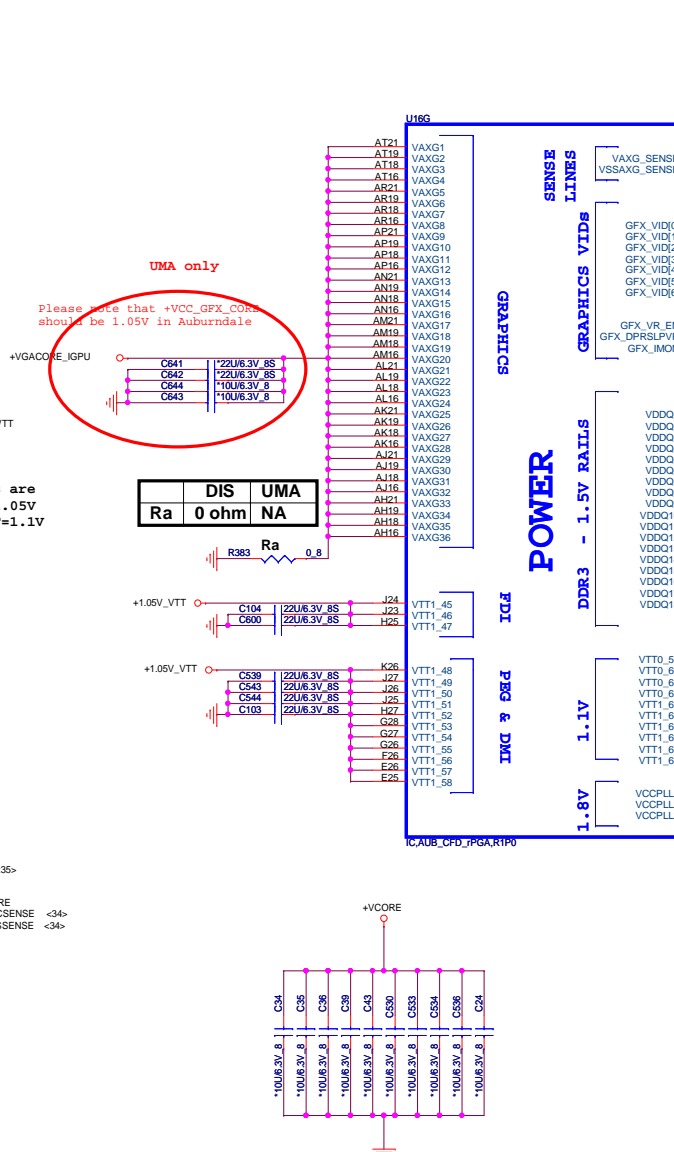
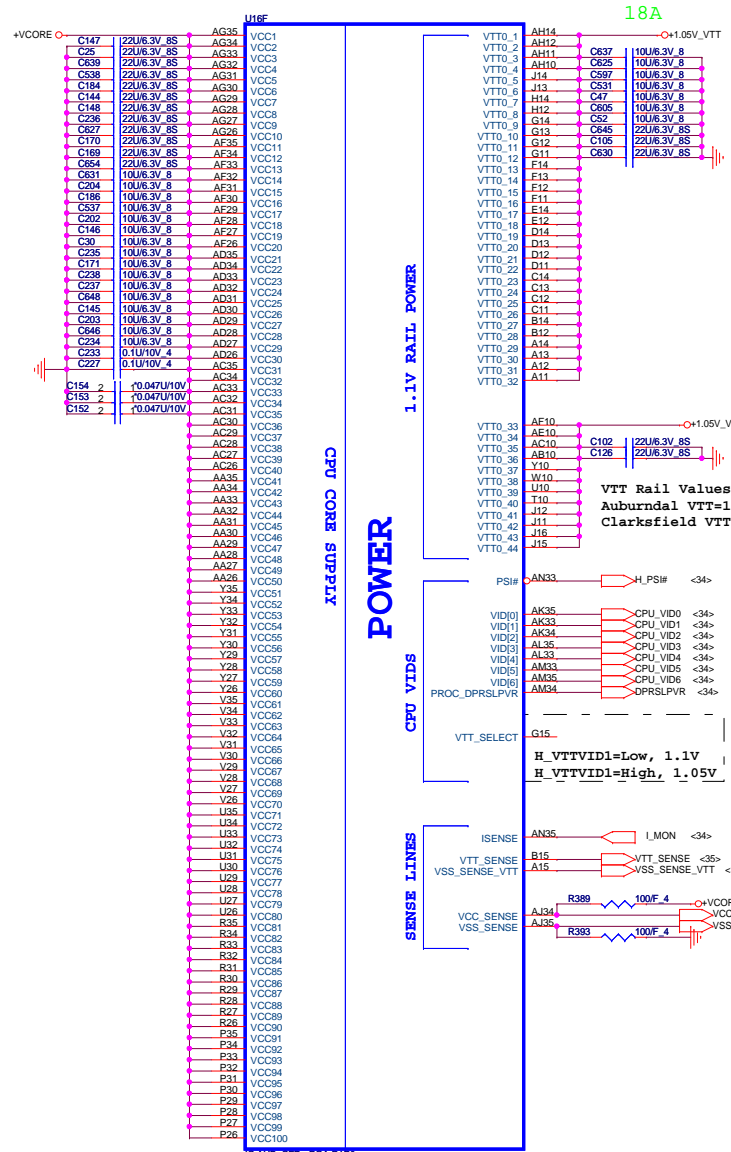
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number
PROCESSOR 1/4(HOST&PEX)	
Date: Monday, November 30, 2009	Sheet 3 of 40

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





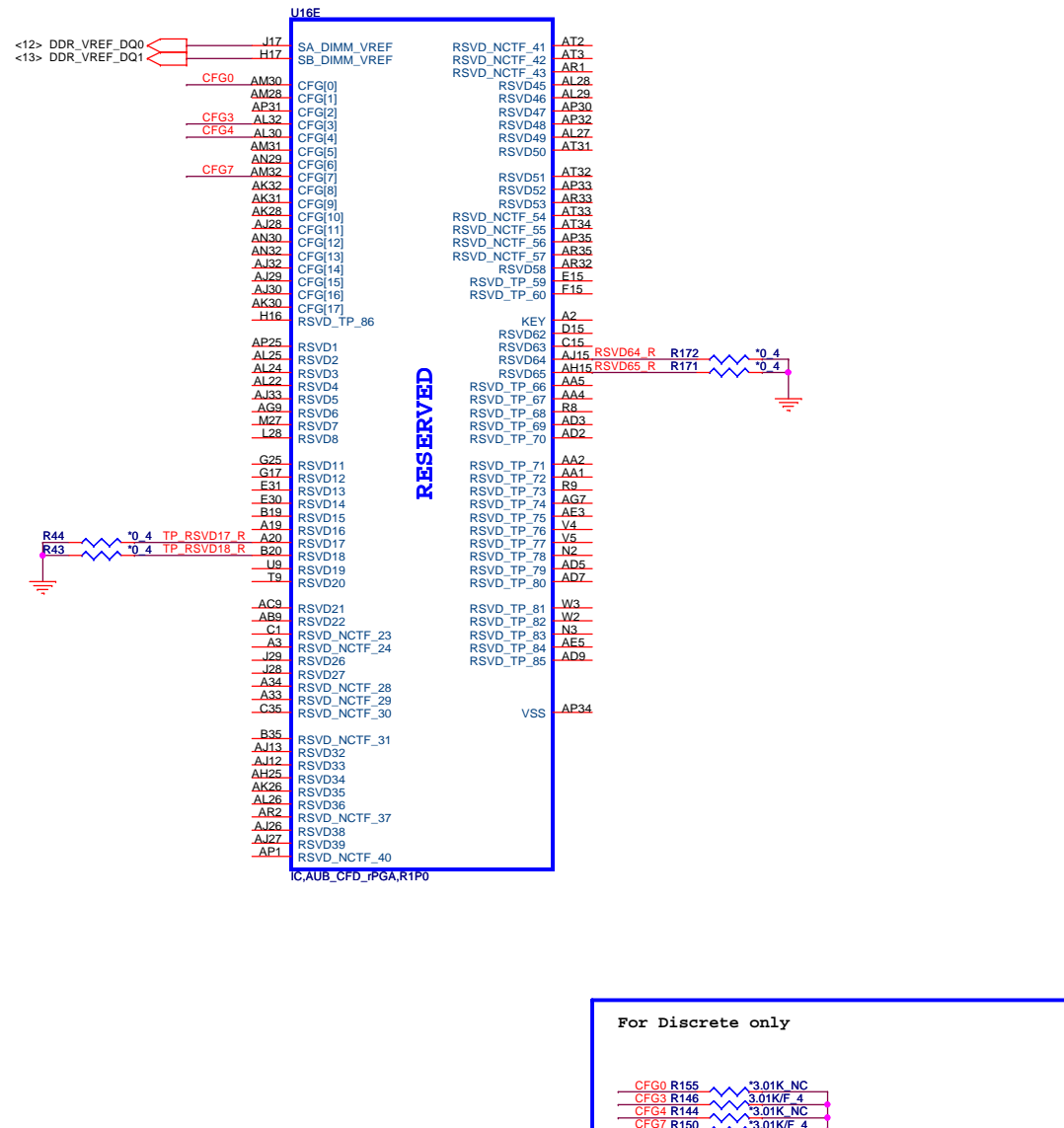
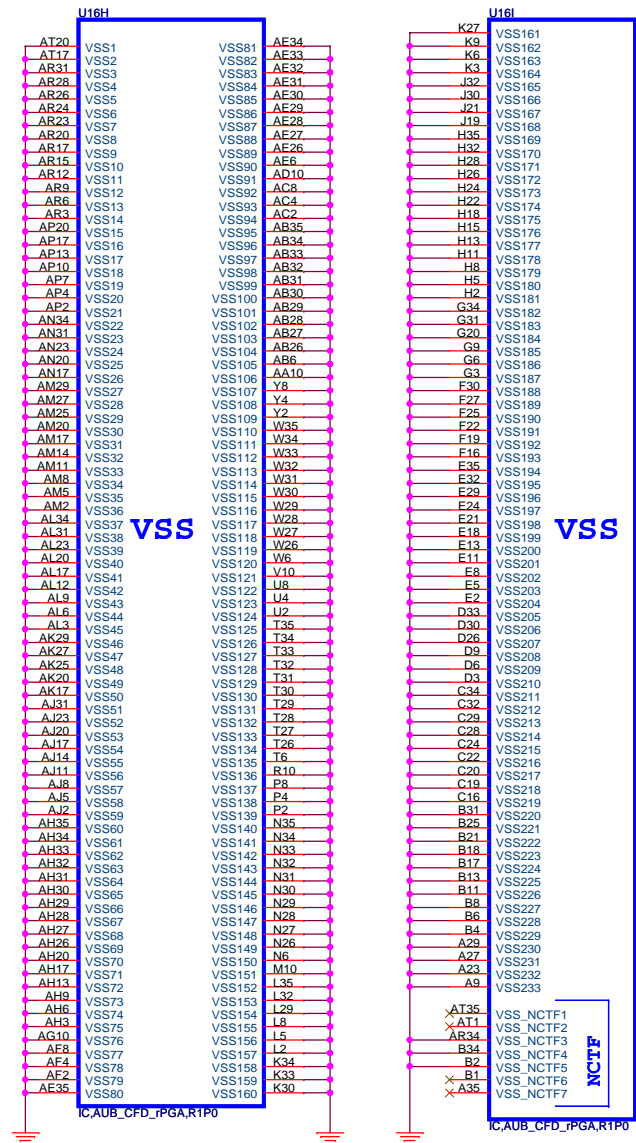
PROJECT : AX1
Quanta Computer Inc.

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Size Custom Document Number PROCESSOR 3/4(POWER) Rev 1A
Date: Thursday, December 03, 2009 Sheet 5 of 40

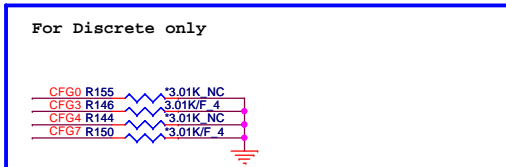
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



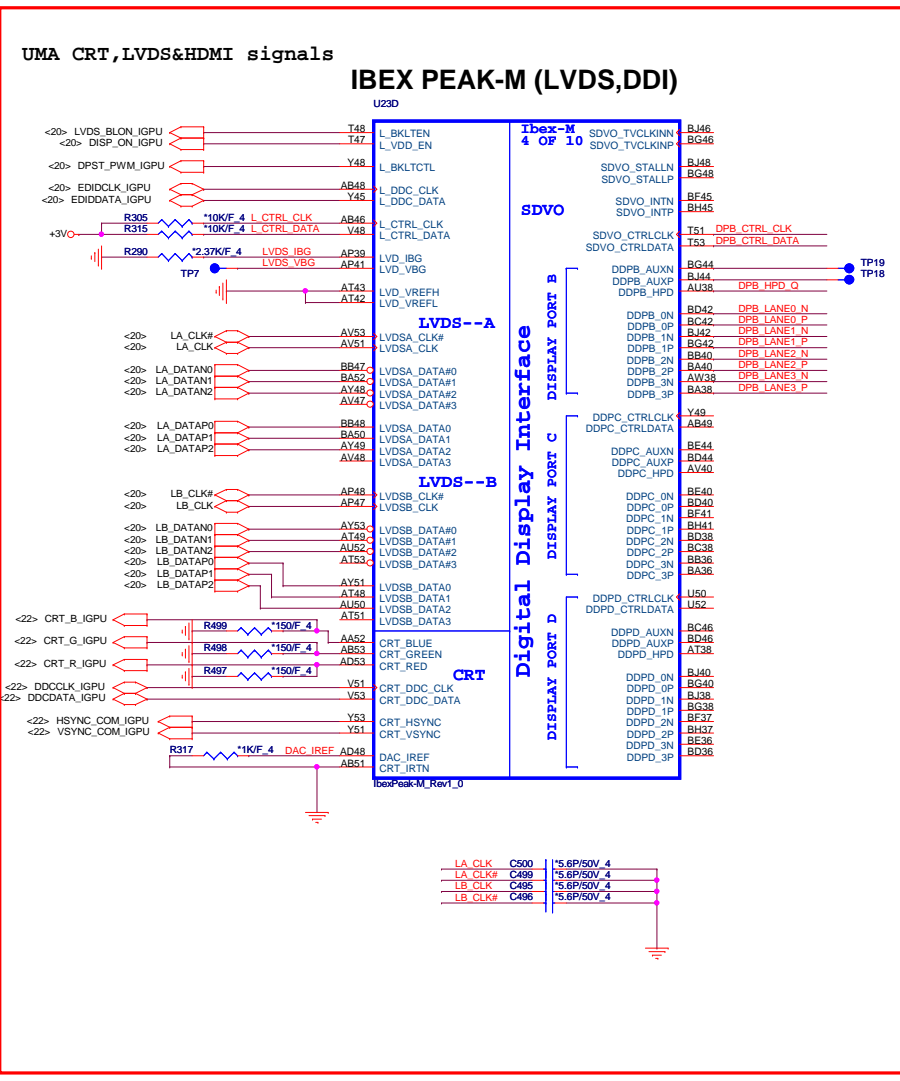
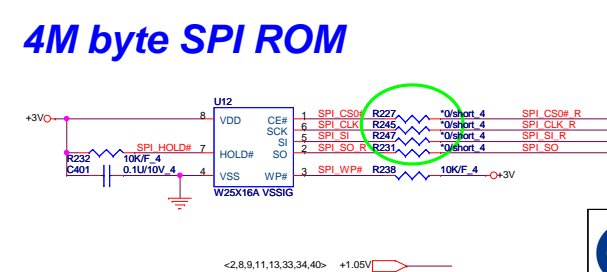
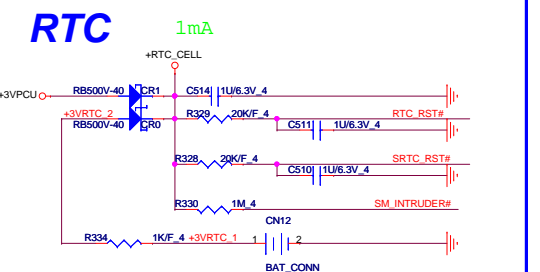
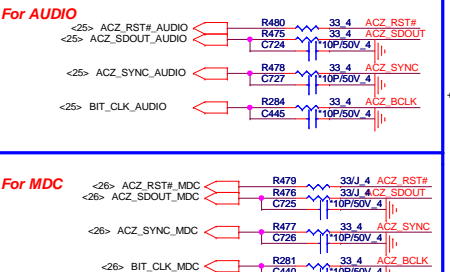
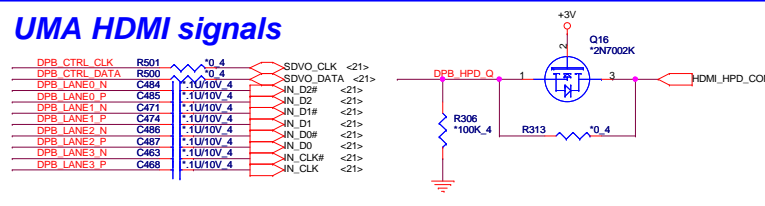
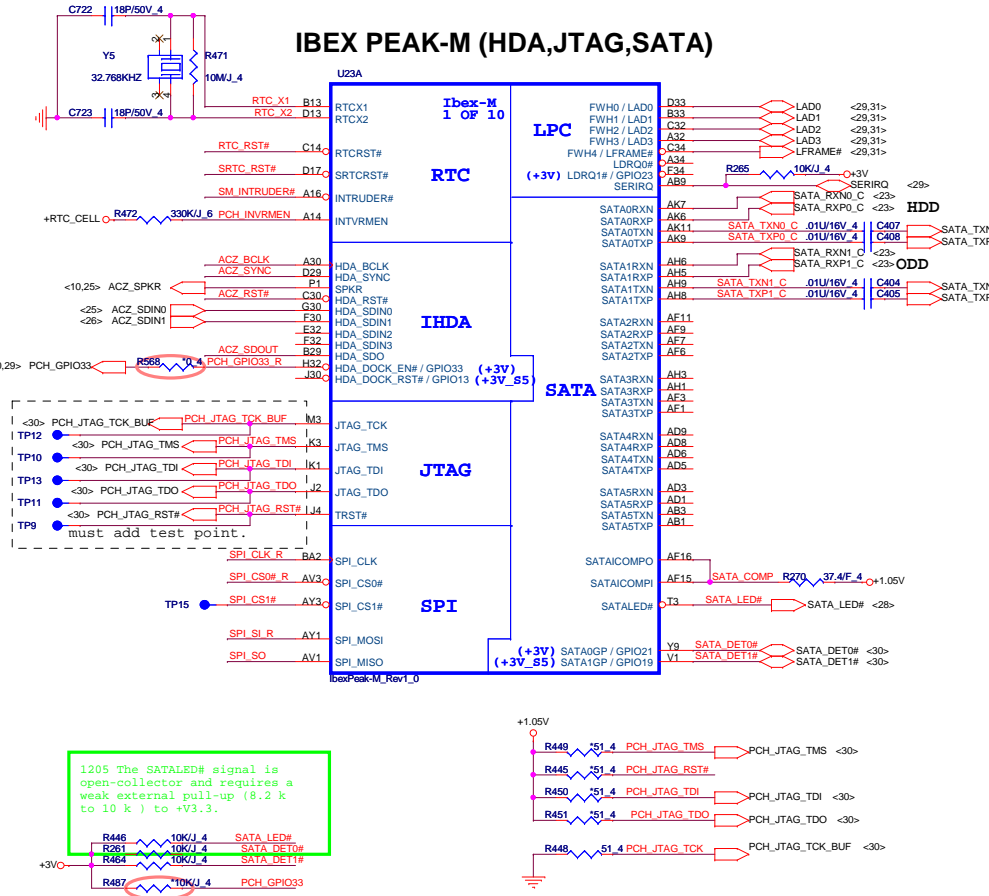
CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

PROJECT :AX1
Quanta Computer Inc.

Size Custom Document Number PROCESSOR 4/4 (GND) Rev 1A
Date: Thursday, November 12, 2009 | Sheet 6 of 40

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

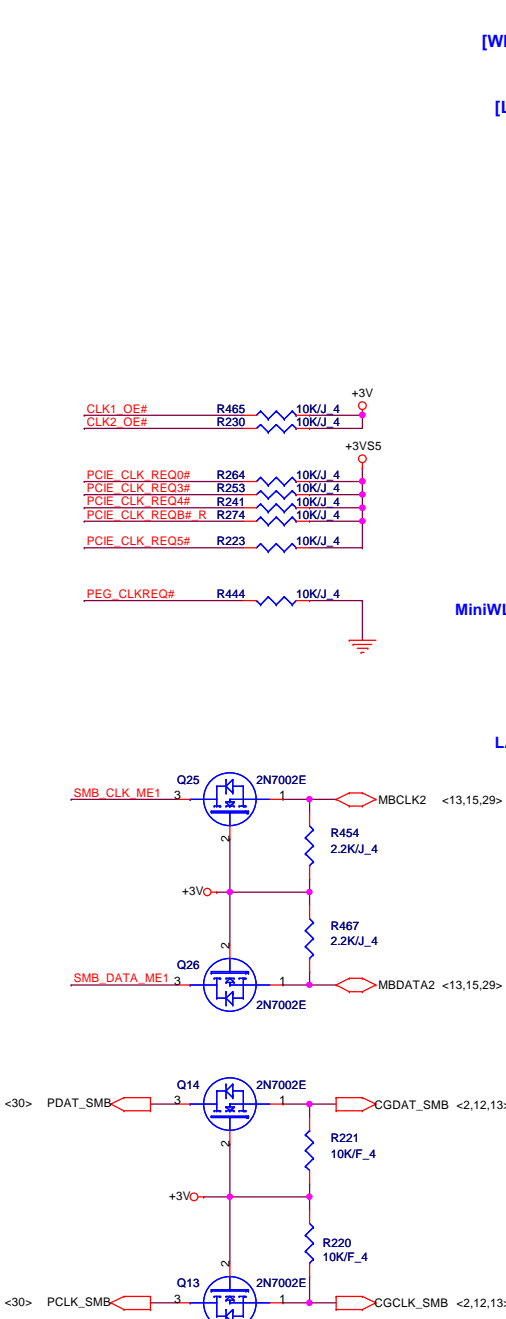
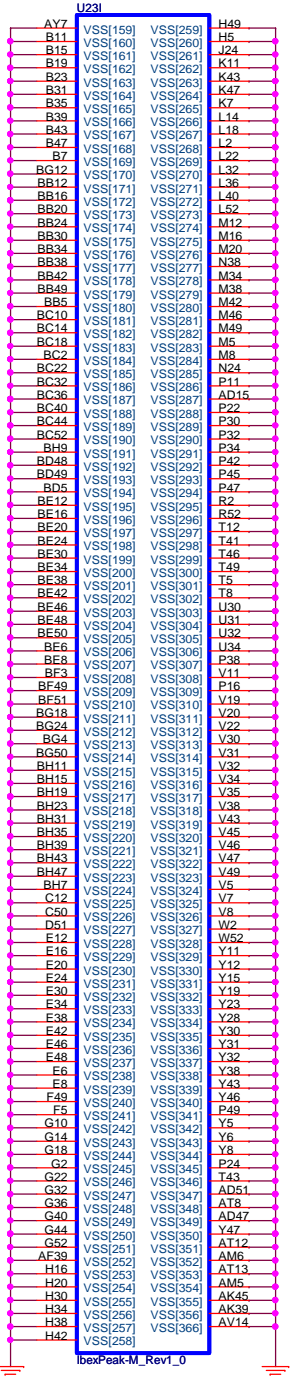


Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZPN00
MAX	AKE39FPN00

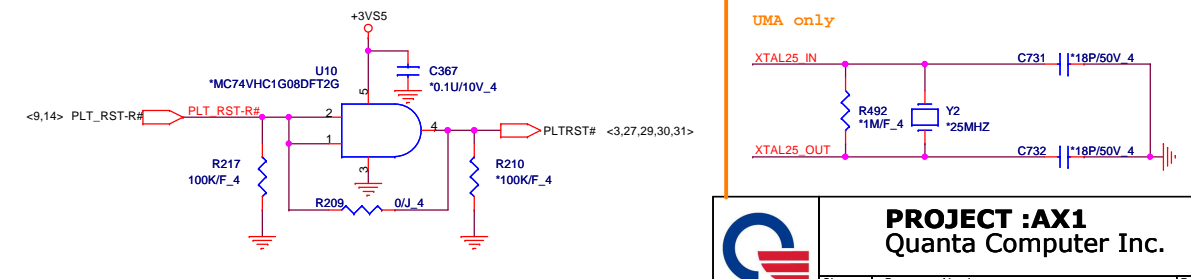
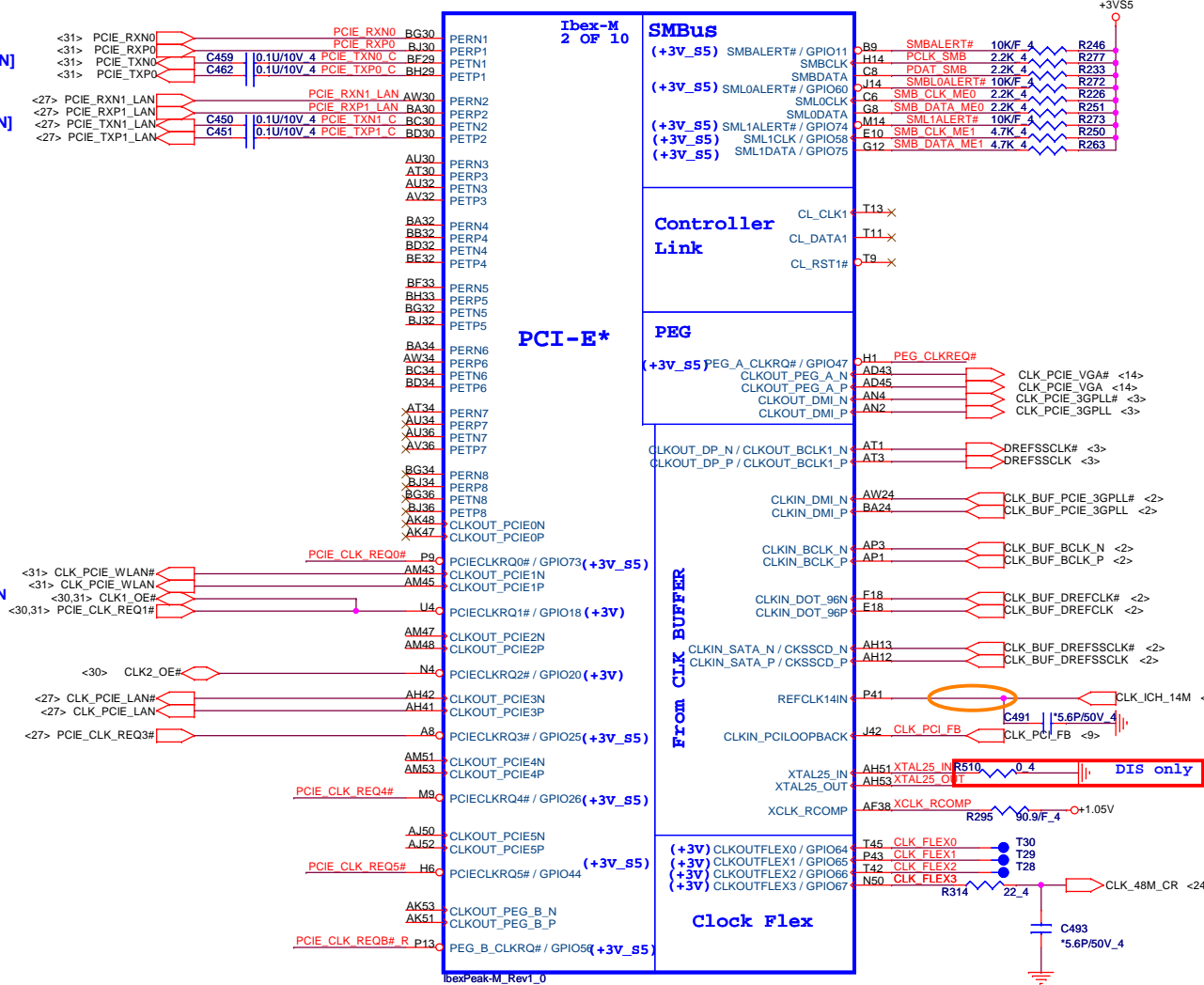
PROJECT : AX1
Quanta Computer Inc.

Size Custom Document Number **PCH 1/5 (SATA,HDA,LPC)** Rev 1A

Date: Monday, November 30, 2009 Sheet 7 of 40



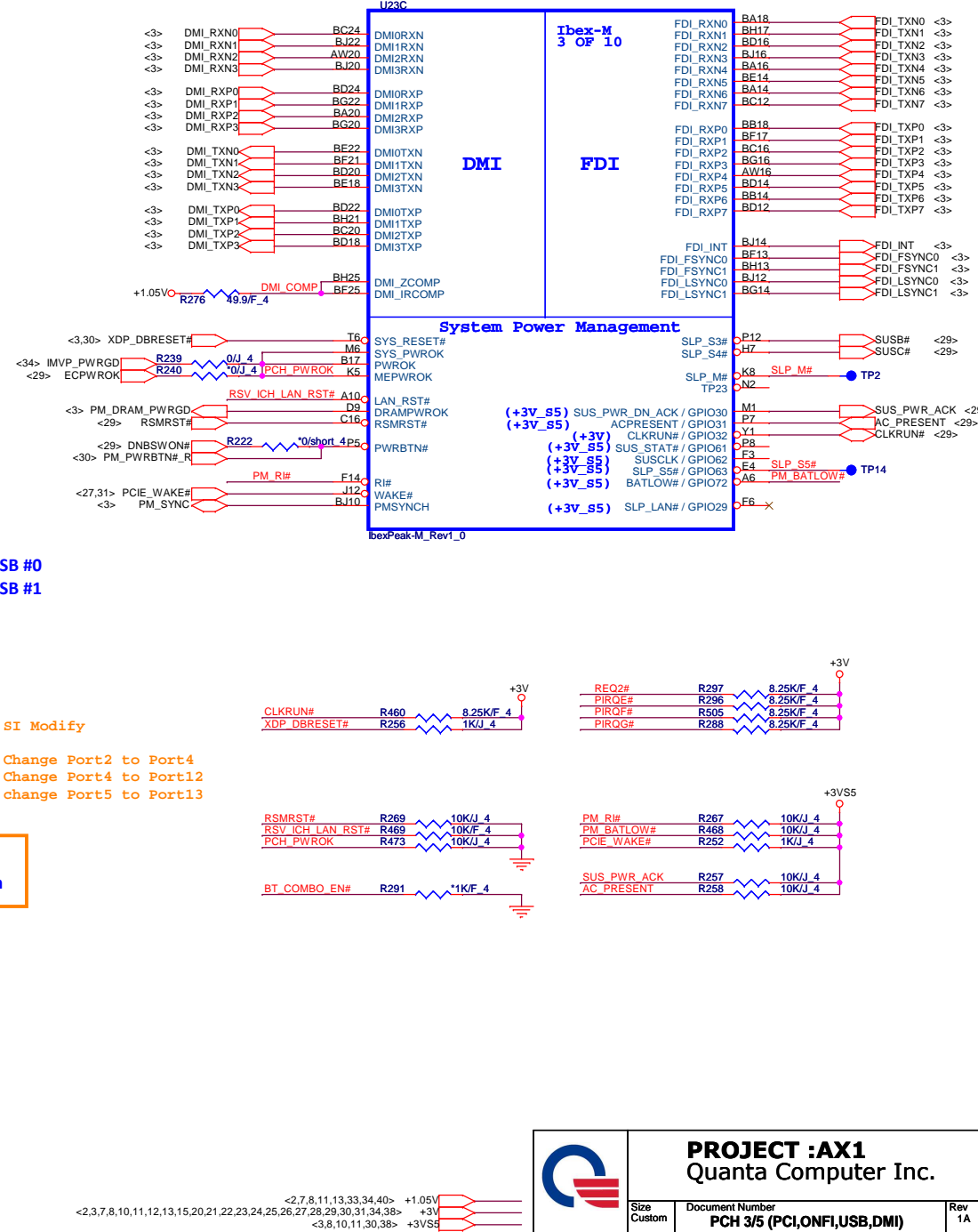
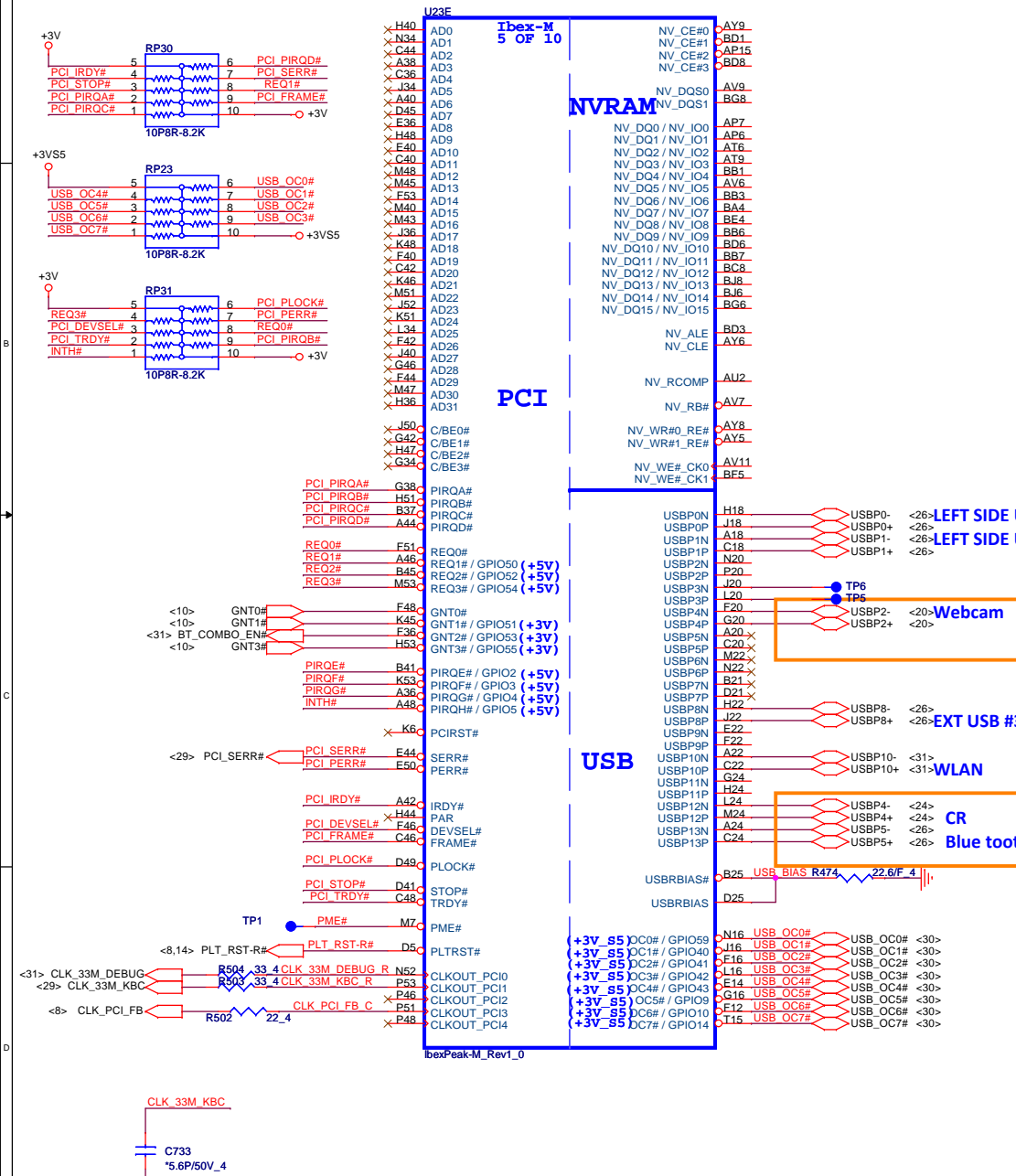
IBEX PEAK-M (PCI-E, SMBUS, CLK)



PROJECT :AX1
 Quanta Computer Inc.

Size Custom	Document Number PCH 2/5 (PCI-E, SMBUS, CK)	Rev 1A
Date: Monday, November 30, 2009 Sheet 8 of 40		

IBEX PEAK-M (PCI,USB,NVRAM)



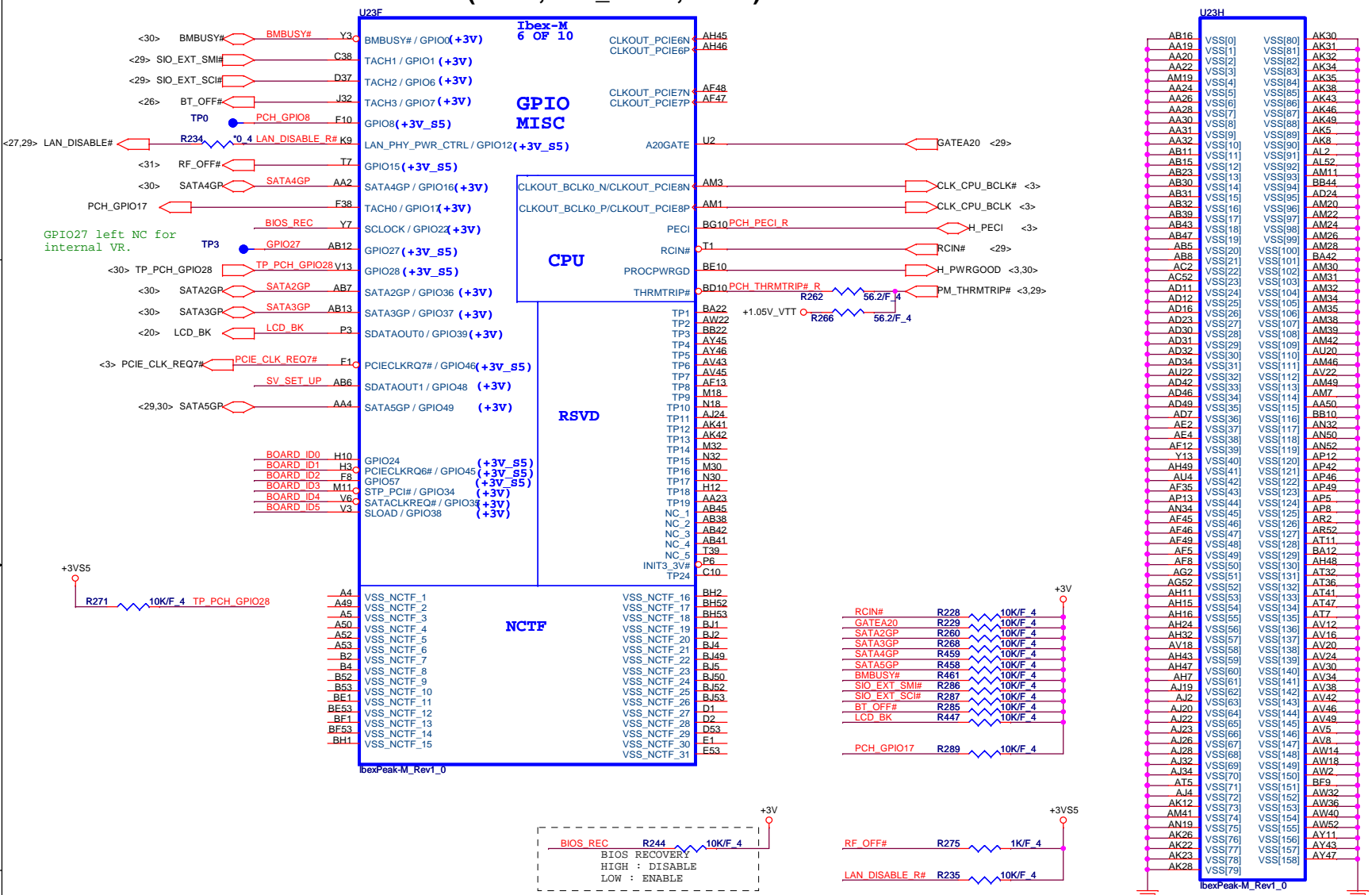
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number PCH 3/5 (PCI,ONFI,USB,DMI)	Rev 1A
Date: Monday, November 30, 2009 Sheet 9 of 40		

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

10



A16 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

SV SET UP R259 10K/F 4

SV_SET_UP

1-X High = Strong (Default)

GNT0# R302 *1K/F 4

GNT1# R506 *1K/F 4

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

NV_ALE

High = Enable
Low = Disable

DMI Termination Voltage

NV_CLE

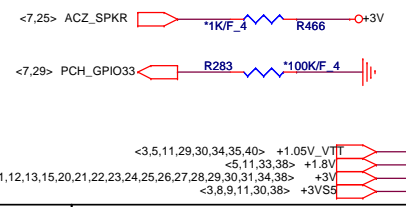
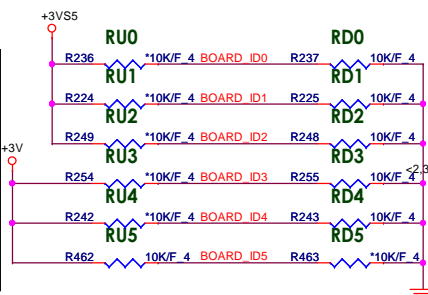
Set to Vcc when LOW
Set to Vcc/2 when HIGH

No Reboot Strap

BOARD ID SETTING

Board ID5: For identify UMA and DIS
Board ID4: For identify FF and DF
Board ID3: Reserve
Board ID2: Reserve
Board ID1: Reserve

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA FF	0	0	0	0	0	0
UMA DF	0	0	0	0	1	0
DIS	0	0	0	0	0	1



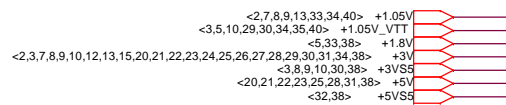
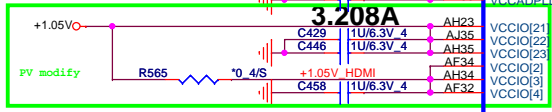
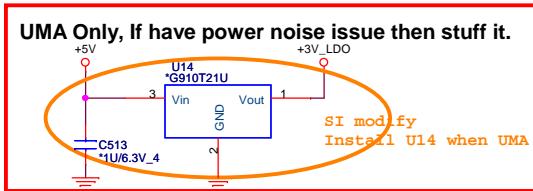
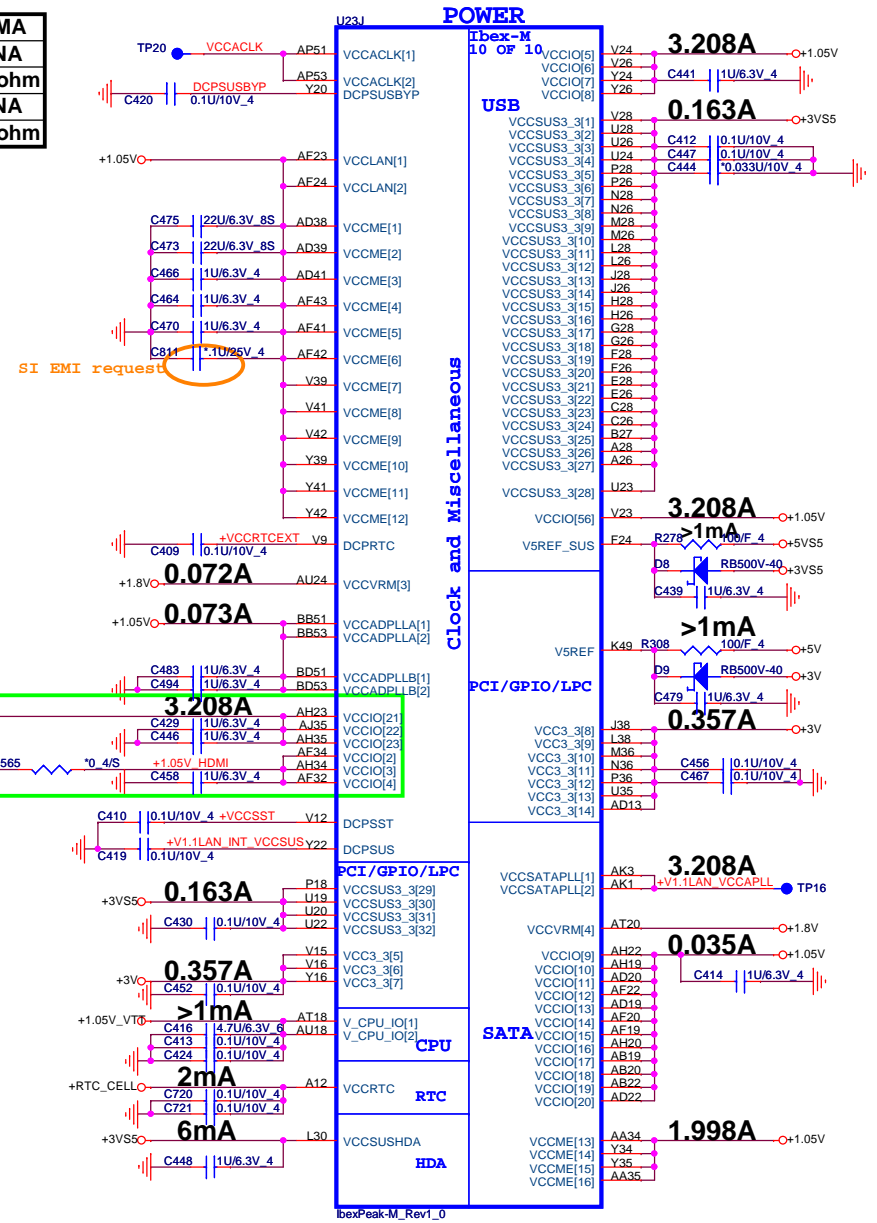
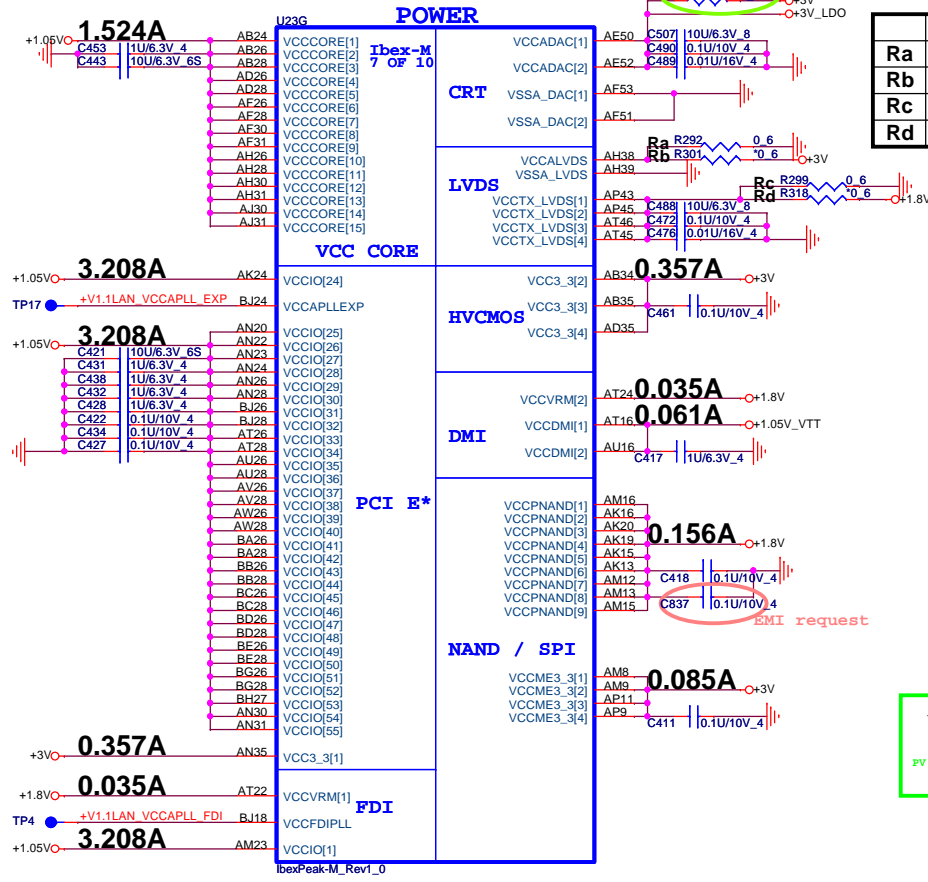
PROJECT :AX1
Quanta Computer Inc.

Size Custom Document Number PCH 4/5 (GPIO & Strap) Rev 1A

Date: Thursday, November 12, 2009 Sheet 10 of 40

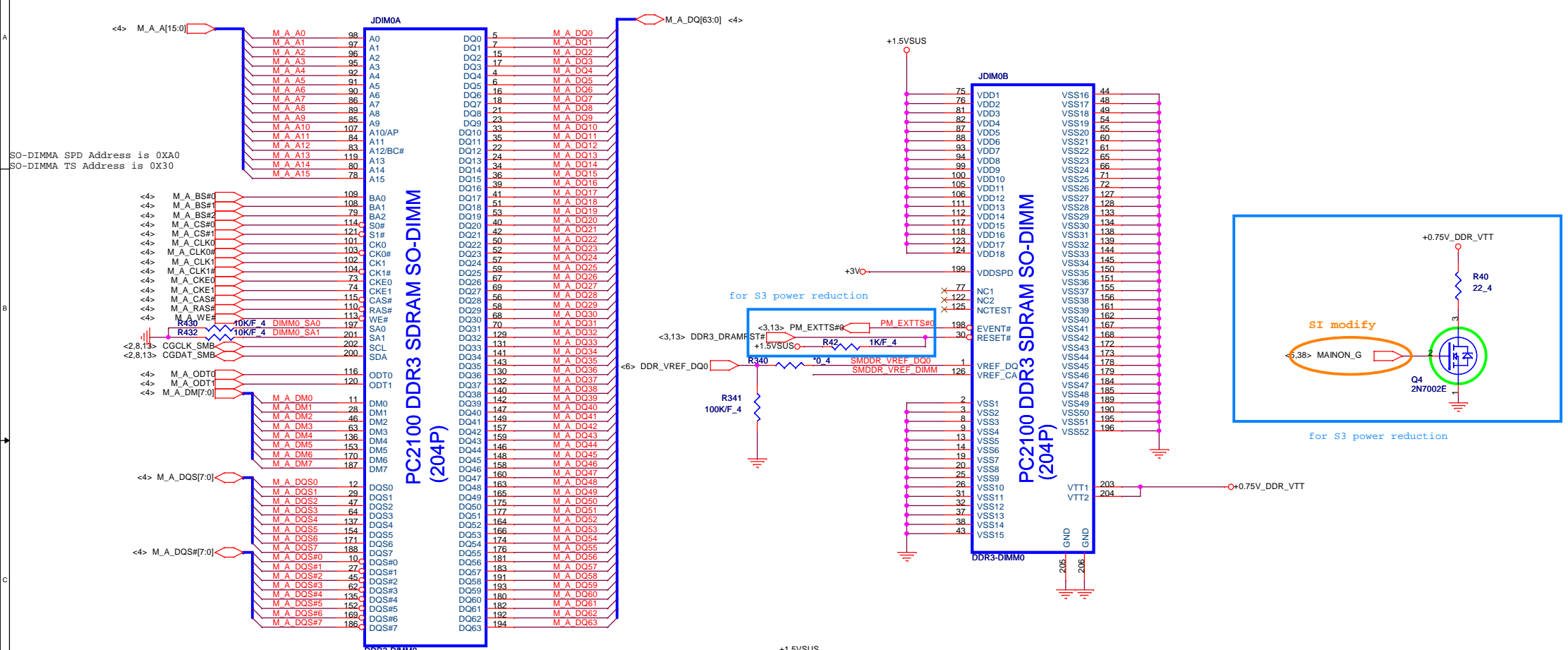
SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

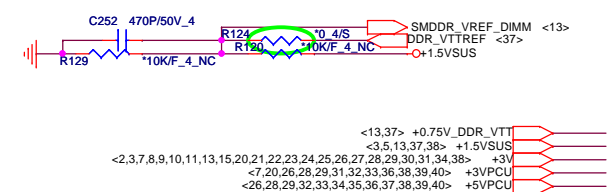
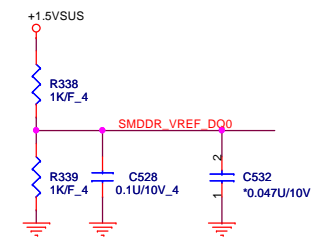
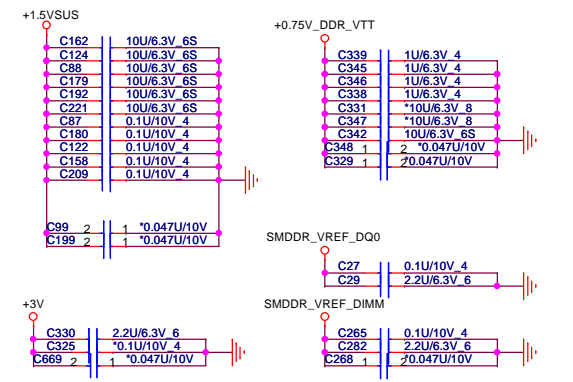


PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
Date: Thursday, November 12, 2009 Sheet 11 of 40		

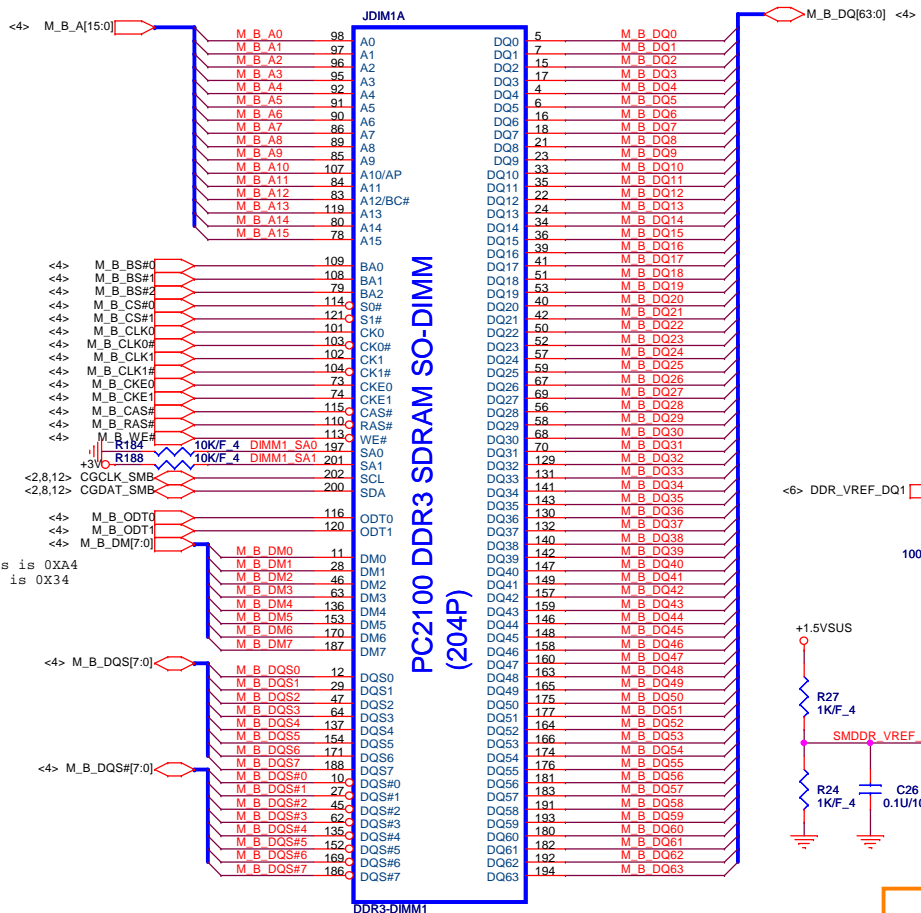


Place these Caps near So-Dimm0.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-0	Rev 1A
Date: Thursday, November 12, 2009 Sheet 12 of 40		

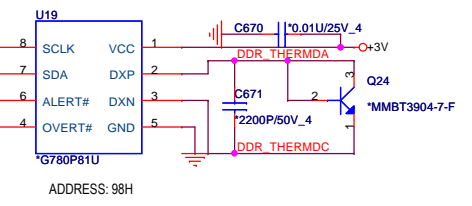
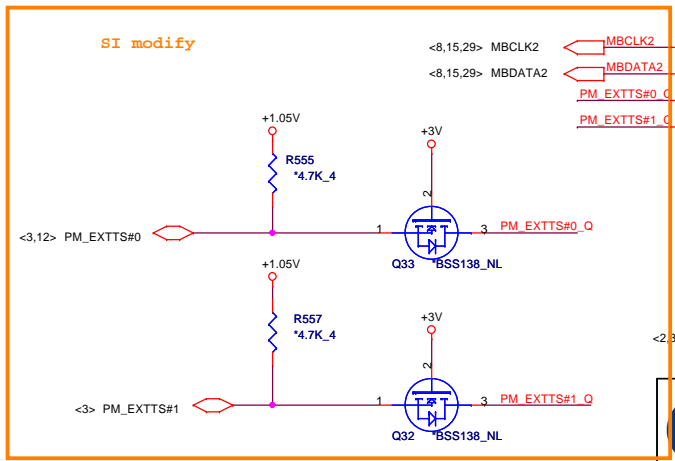
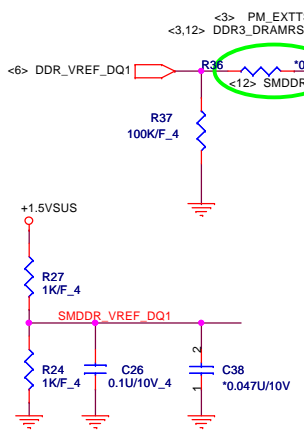
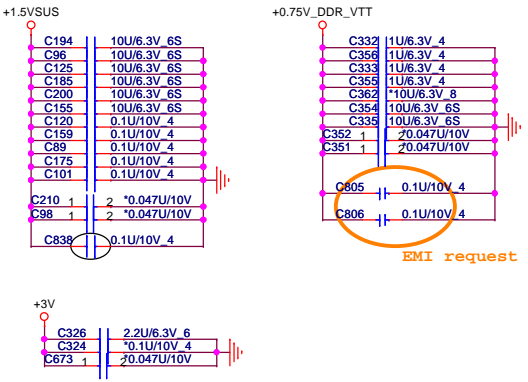


SO-DIMM SPD Address is 0XA4
SO-DIMM TS Address is 0X34

PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

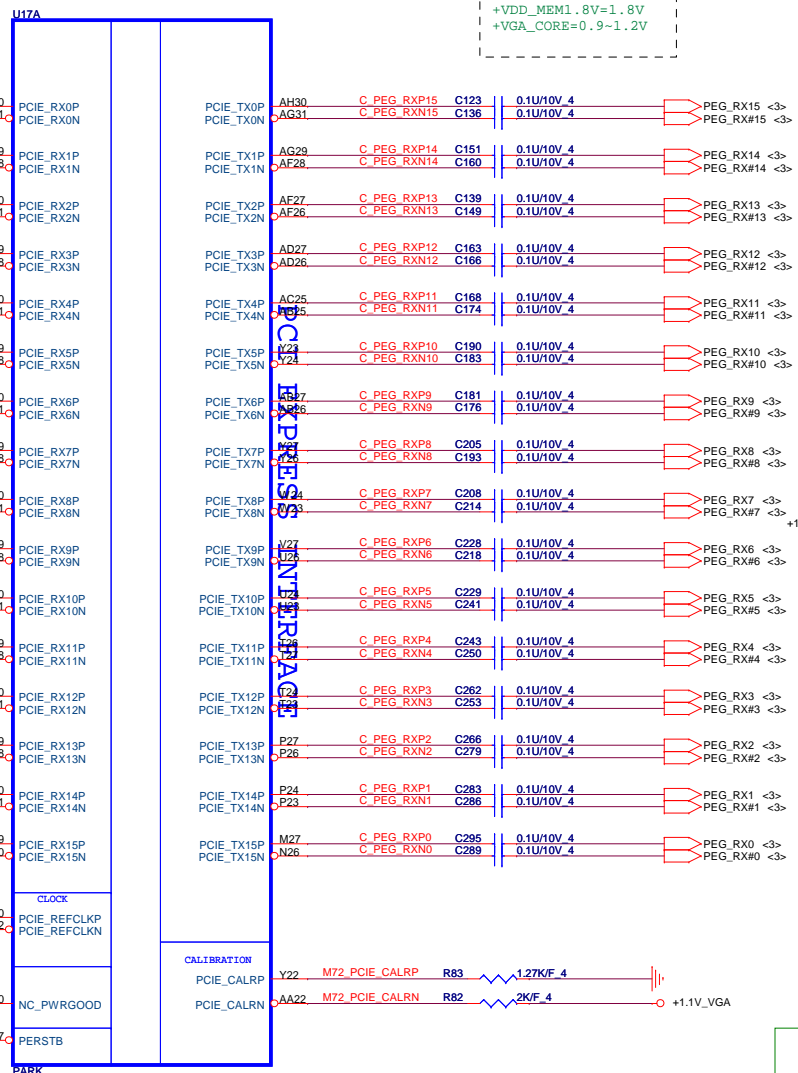


PROJECT :AX1
Quanta Computer Inc.

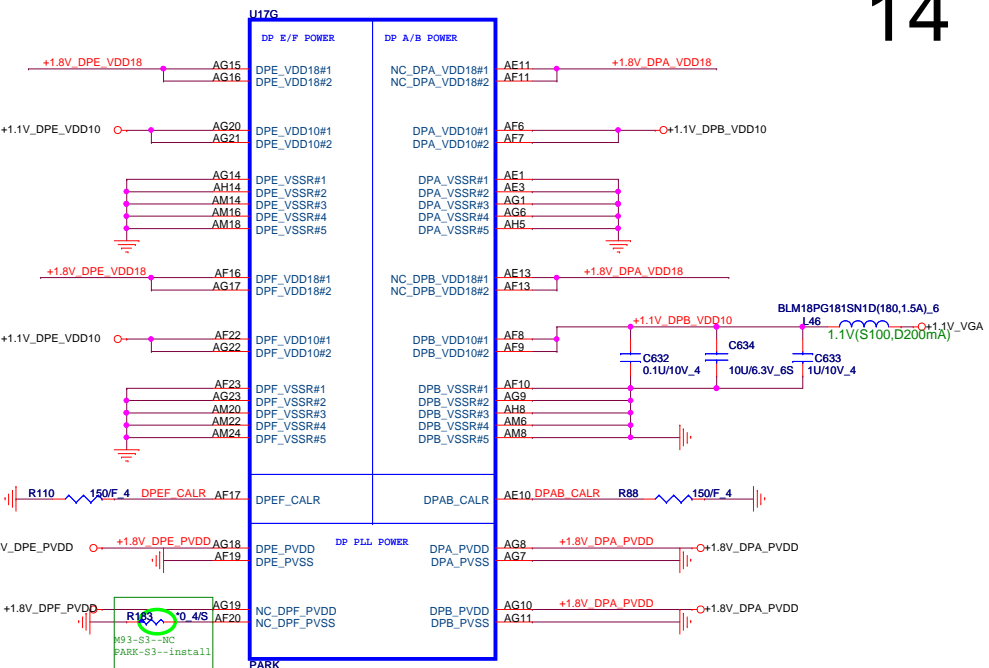
Size Custom Document Number **DDR3 DIMM-1** Rev 1A

Date: Thursday, December 03, 2009 | Sheet 13 of 40

2.5GT/s bit rate



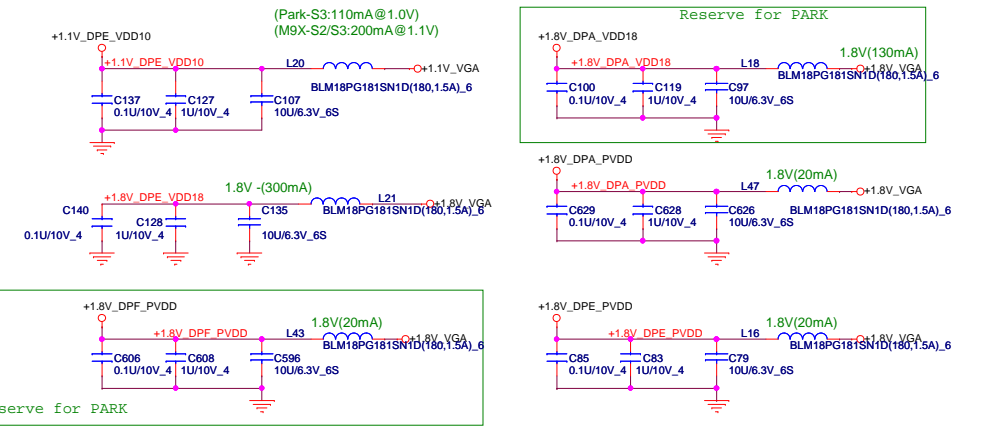
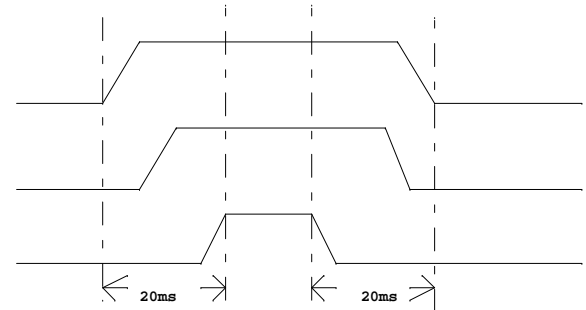
POWER
 +PCIE_VDDR=1.2V
 +VDD_MEM1.8V=1.8V
 +VGA_CORE=0.9-1.2V



M93-S3--NC
 PARK-S3--install
 10K 4 1 2 R149

100MHz (+/-300ppm) input frequency,
 0-0.7V single-ended swing

- VGA Core BPP
- VGA Core VDDR
- +1.8V PCIE_VDDR
- +1.8V PCIE_PVDD
- +1.8V VDDR1
- +3V_VGA VDDR3

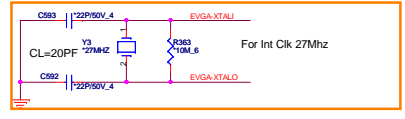
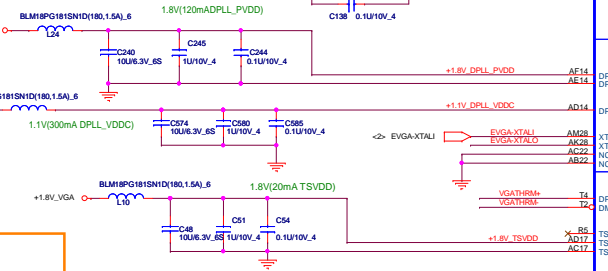
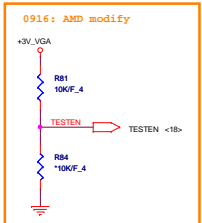
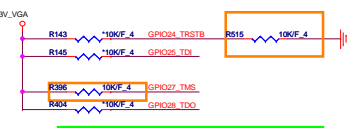
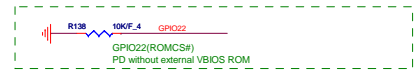
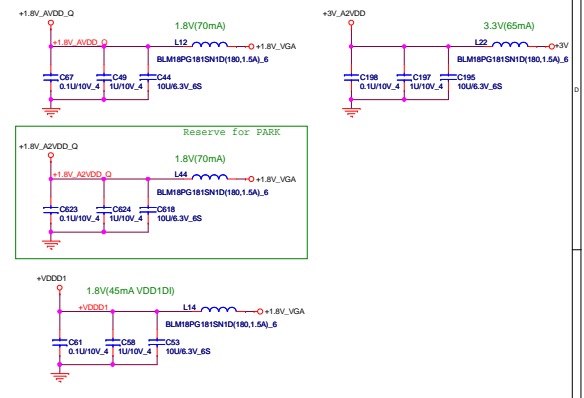
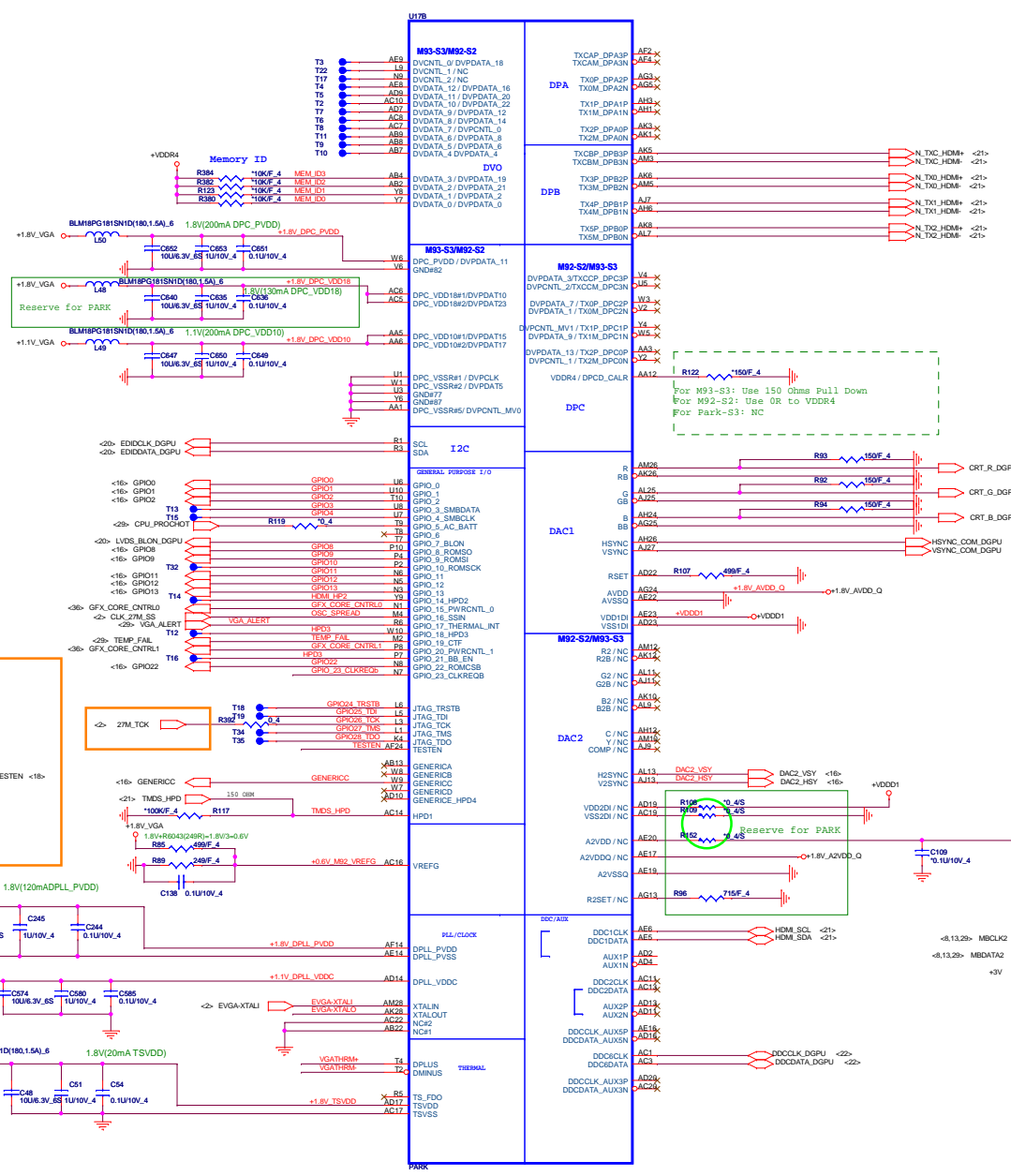


PROJECT :AX1
Quanta Computer Inc.

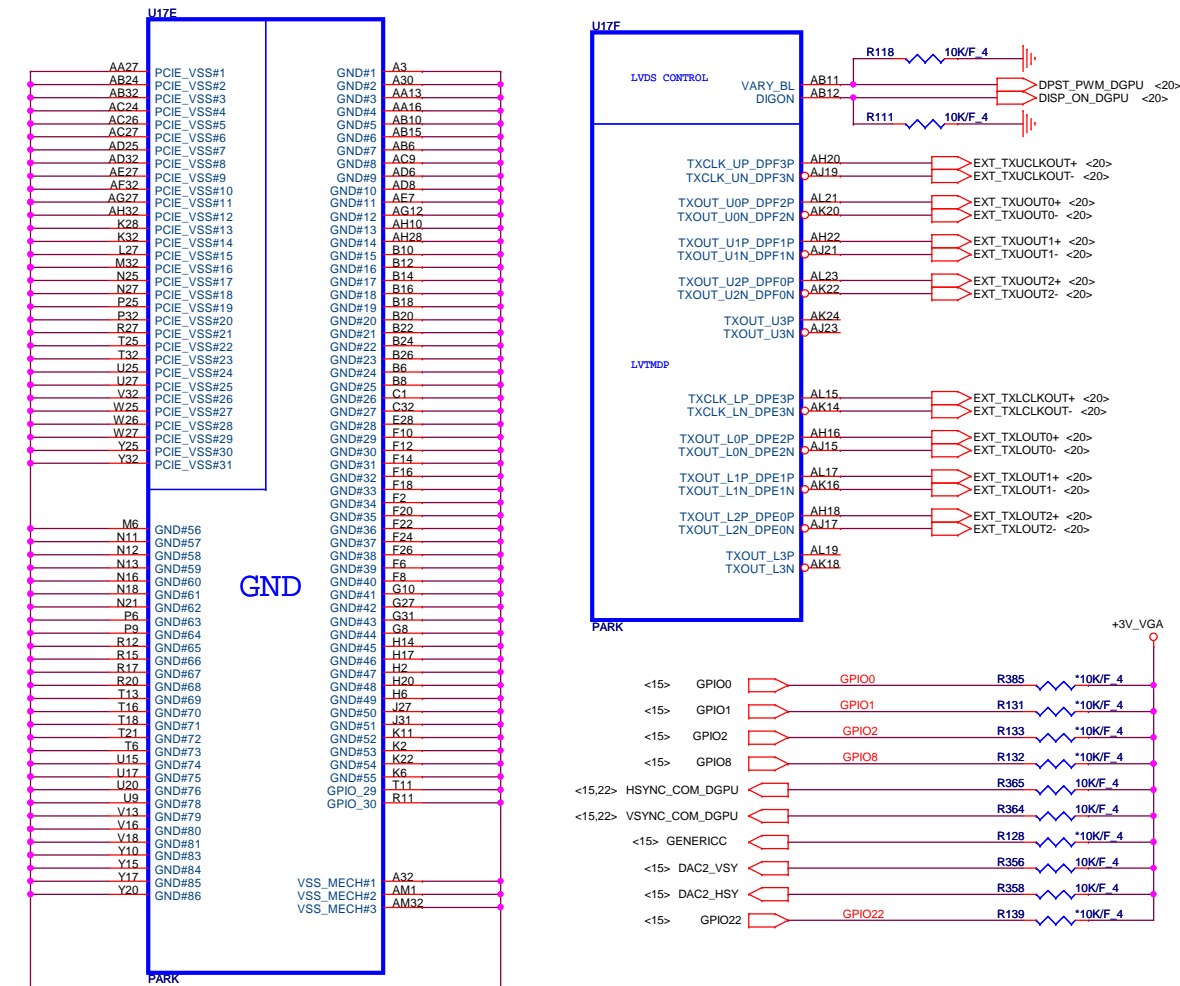
Size Custom	Document Number M93_PCIE_Interface	Rev 1A
Date: Thursday, November 12, 2009 Sheet 14 of 40		

NEM_ID[3:0]	Vendor	Type	Vendor P/N
0000 0001	Samsung (E die) Hynix	64*16-800MHZ 64*16-800MHZ	K4M1G1646E-HC12 H5TQ1G63BFR-12C

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



PROJECT :AX1		
Quanta Computer Inc.		
Size Custom	Document Number M93_MAIN	Rev 1A
Date Thursday, November 12, 2009	Sheet 15	of 40

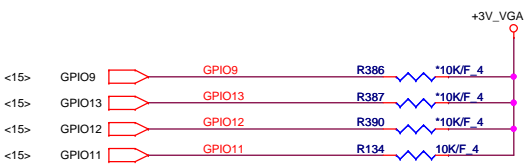


CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2,0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 0 11

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1



It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

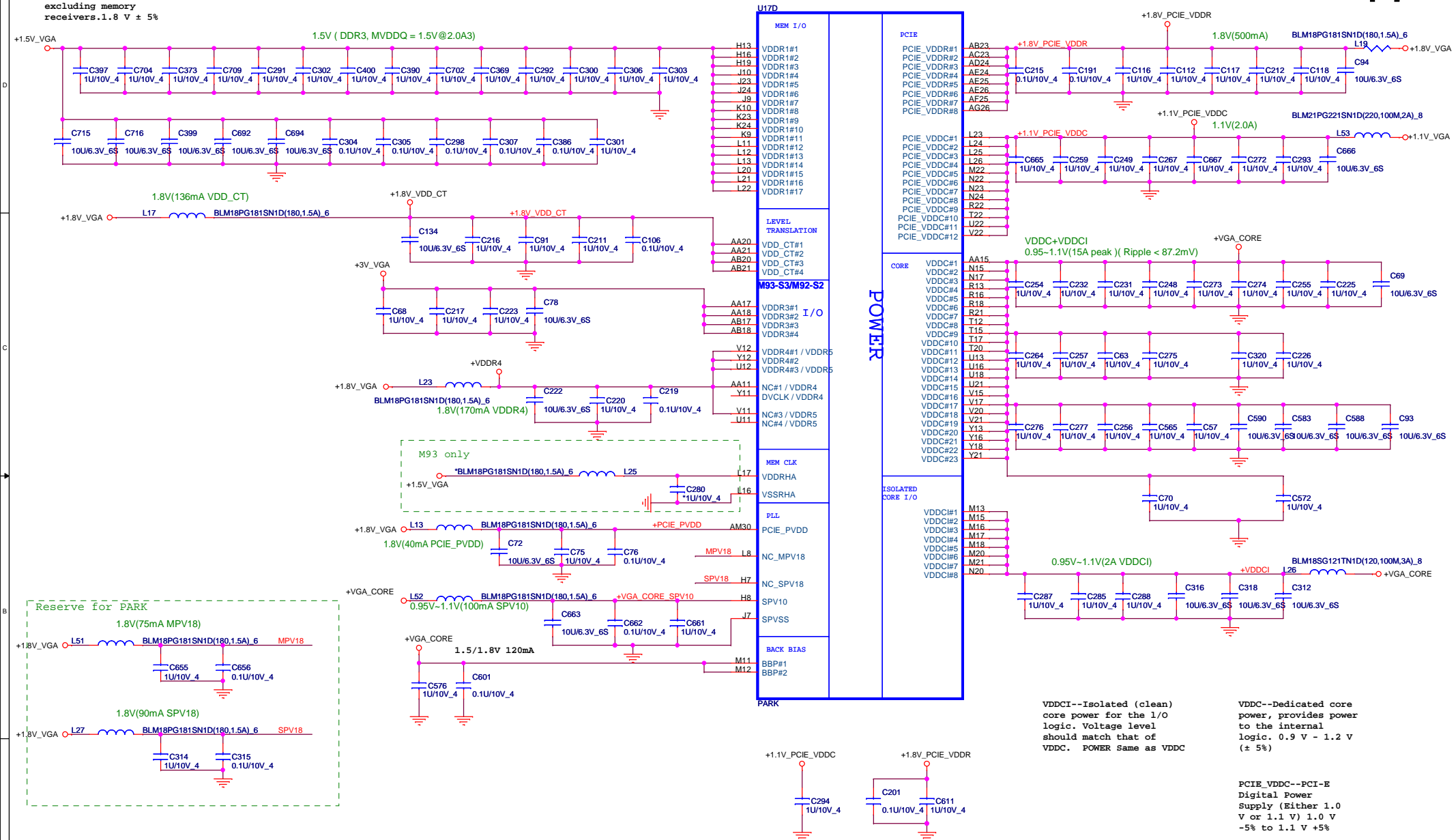


PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number M93_GND / LVDS / Straps	Rev 1A
Date: Thursday, November 12, 2009	Sheet 16 of 40	

VDD_CT -- Level translation between core and I/O, excluding memory receivers. 1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

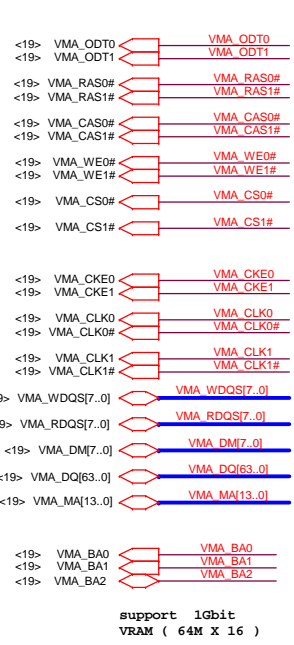
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

PROJECT :AX1
Quanta Computer Inc.

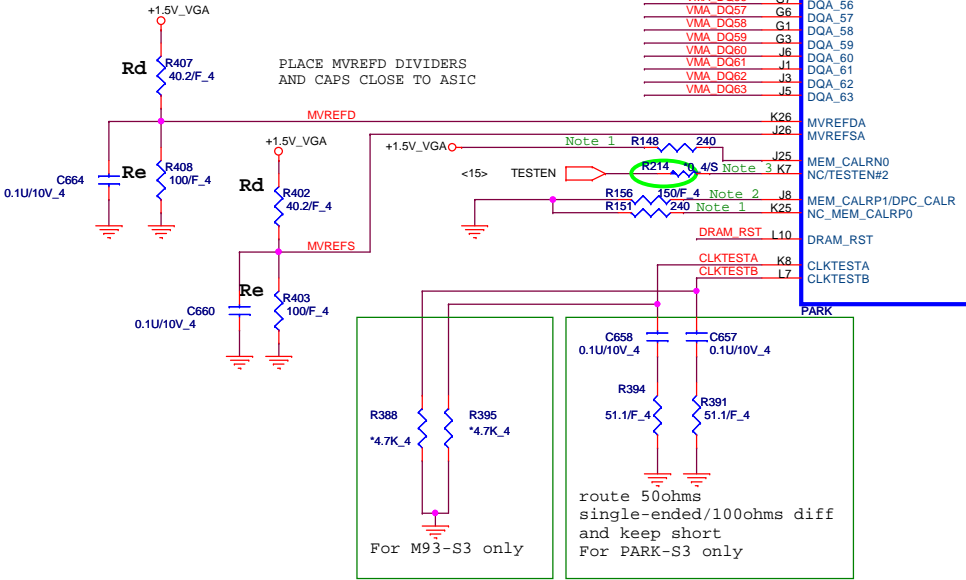
Size Custom	Document Number M93_Power_and_NC	Rev 1A
Date: Tuesday, November 10, 2009		Sheet 17 of 40

exaint@hotmail.com

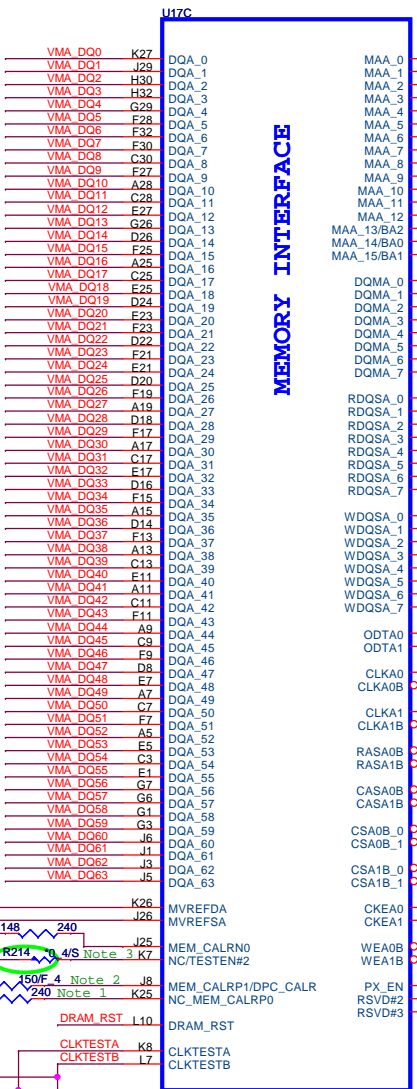


support 1gbit
VRAM (64M X 16)

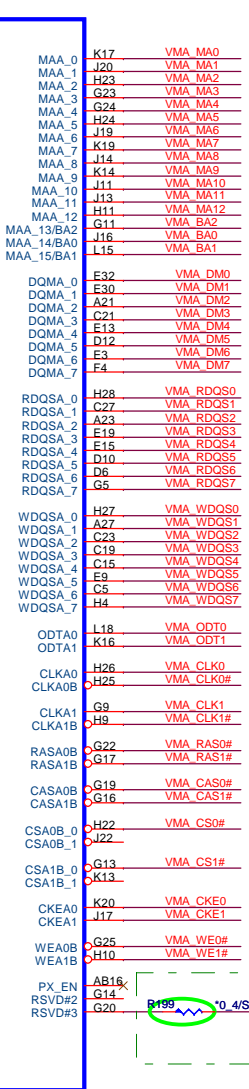
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Rd)	40.2R	40.2R
MVREF TO GND (Re)	100R	100R



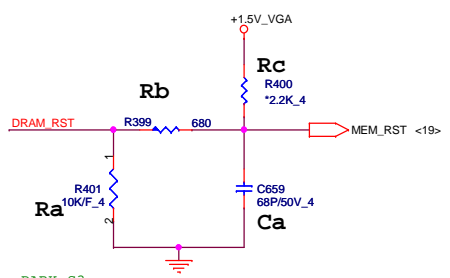
Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
 Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
 For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
 Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
 For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



MEMORY INTERFACE



For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.



Designator	M9X-S2 and M93-S3	Park-S3
Ra	NC	10K
Rb	0R/Short	680R
Rc	2.2K	NC
Ca	2.2nF	68pF

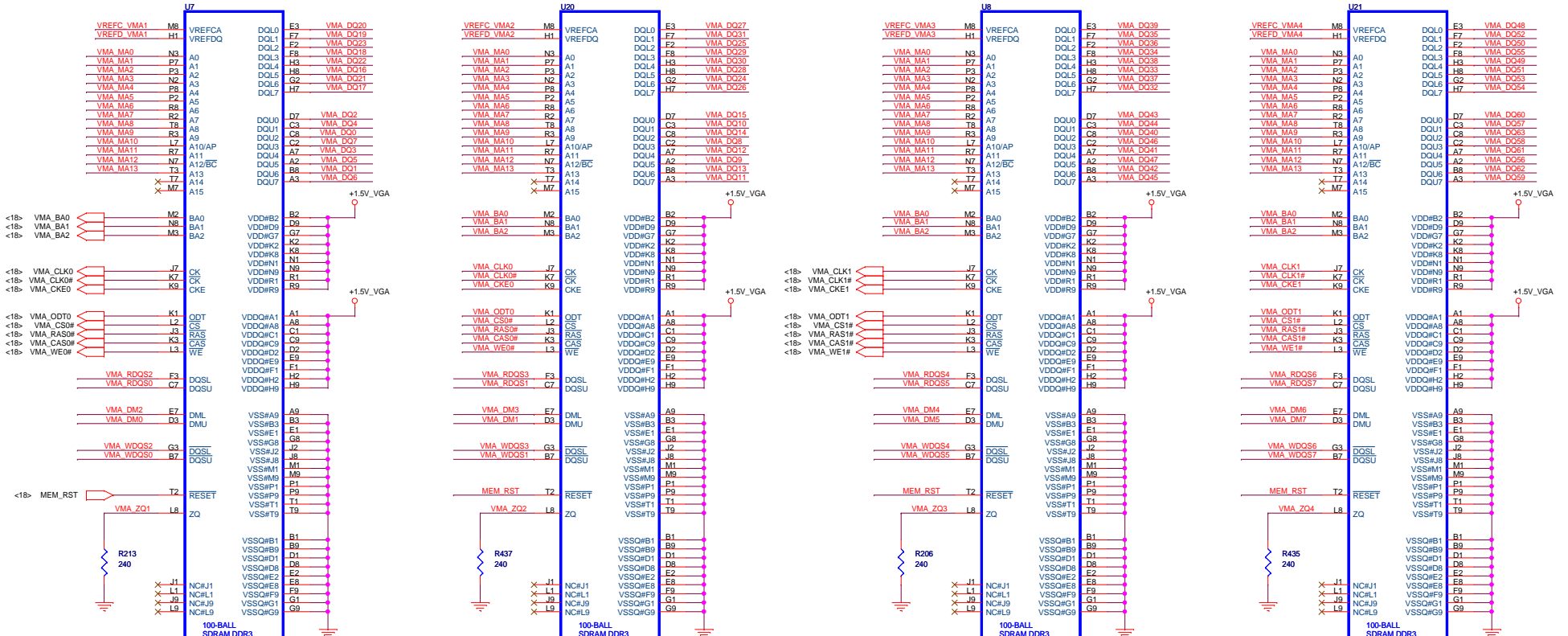


PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number M93_MEM_Interface	Rev 1A
Date: Thursday, November 12, 2009 Sheet 18 of 40		

512MB DDR3

<18> VMA_MA[13..0] VMA_MA[13..0] <18> VMA_DQ[63..0] <18> VMA_DQ[63..0]
 <18> VMA_DM[7..0] <18> VMA_DM[7..0] <18> VMA_RDQS[7..0] <18> VMA_RDQS[7..0]



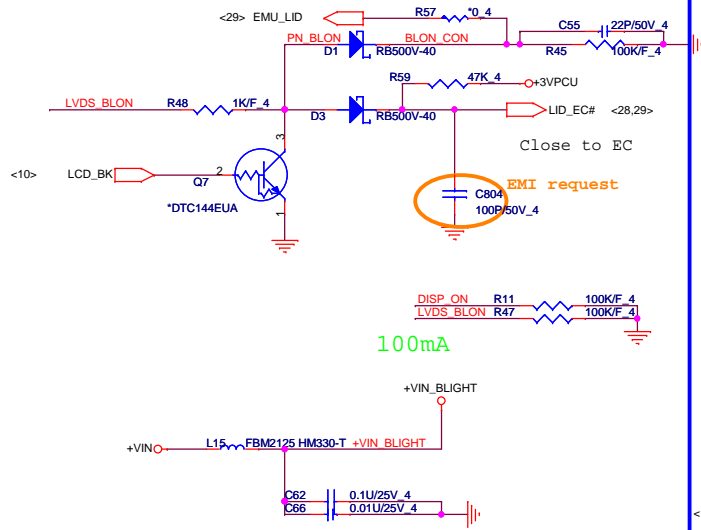
	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

PROJECT :AX1
Quanta Computer Inc.

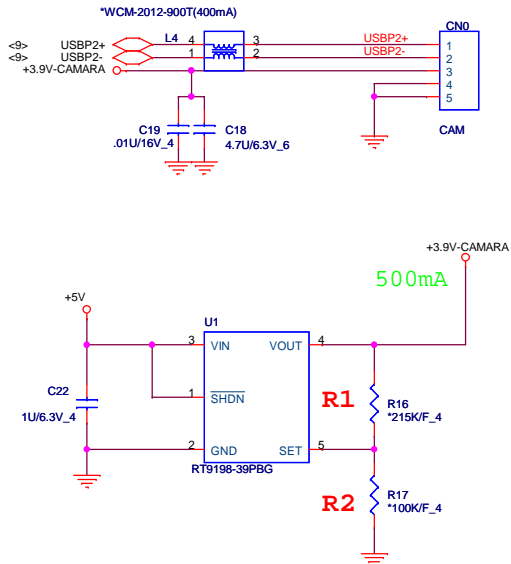
Size Custom	Document Number M93/VRAM_A0,A1	Rev 1A
Date: Thursday, November 12, 2009		Sheet 19 of 40

examint@hotmail.com

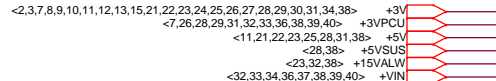
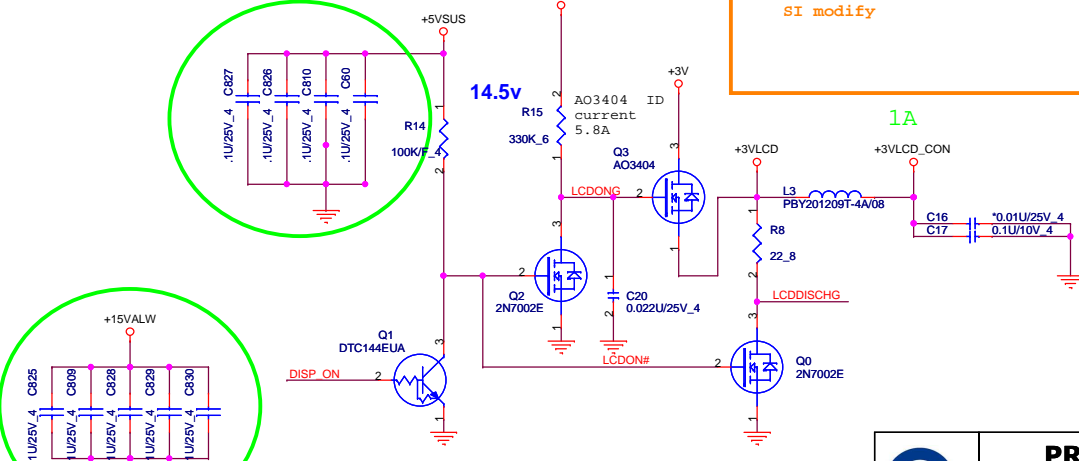
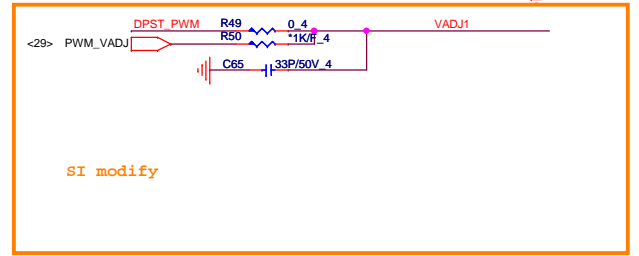
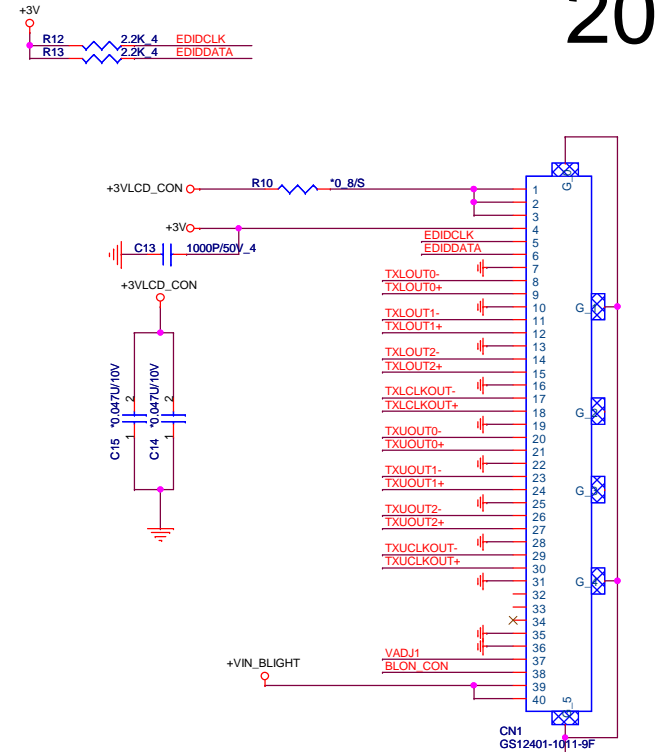
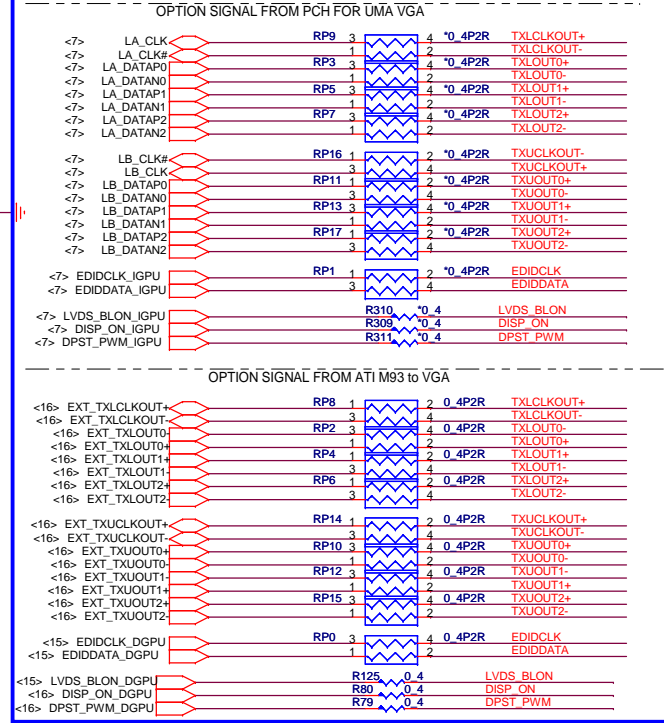
LID Switch




CAMERA



- 1. If LCD connector near GPU, then place these series Resistors near GPU
- 2. If LCD connector near PCH, then place these series Resistors near PCH





PROJECT :AX1

Quanta Computer Inc.

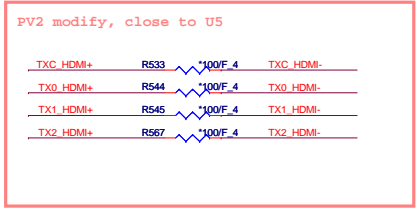
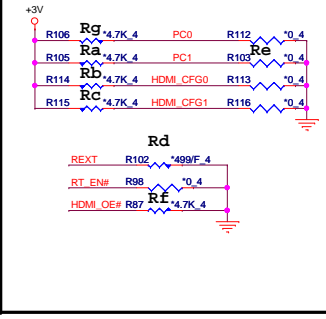
Rev 1A

Size Custom	Document Number LCD CONN/LID/CAM	Date: Thursday, November 12, 2009
Sheet 20 of 40		

Signals		PDT	CHR	PIM
PC1	Ra	NC	NC	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	4.7K	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella
 CHR : need Na R1182, add R1027 for capella

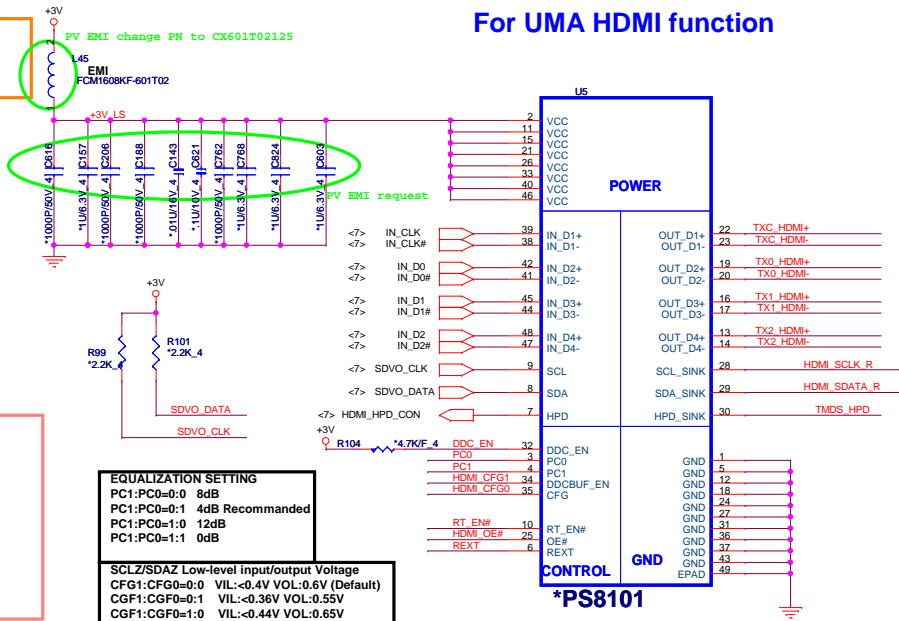
Vendor:PDT P/N:AL008101000
 Vendor:CHR P/N:AL007318002
 Vendor:PIM P/N:ALP411LS004



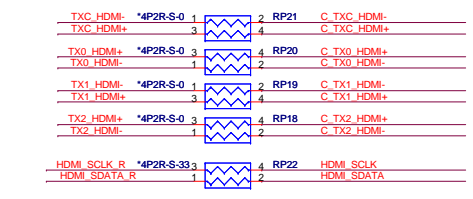
EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
 CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
 CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

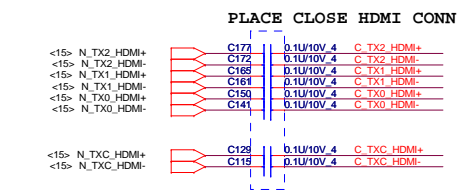
For UMA HDMI function



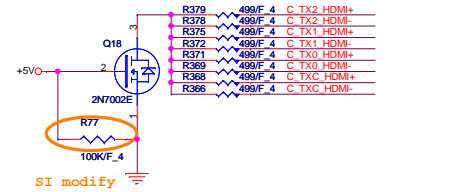
FOR UMA ONLY FROM LEVEL SHIFTER



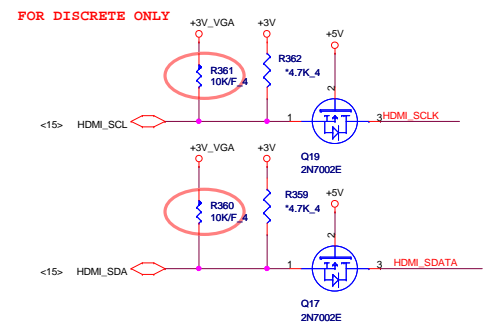
FOR DISCRETE ONLY FROM M93/PARK



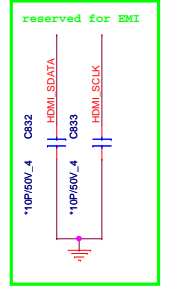
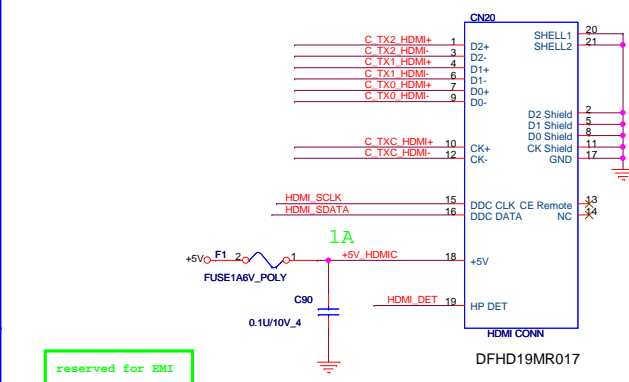
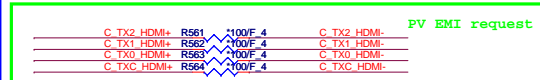
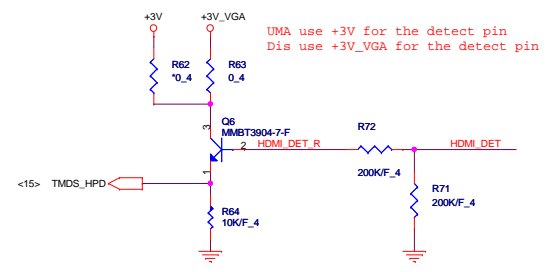
FOR DISCRETE ONLY



DISCRETE HDMI I2C SELECT
Close to HDMI Connector



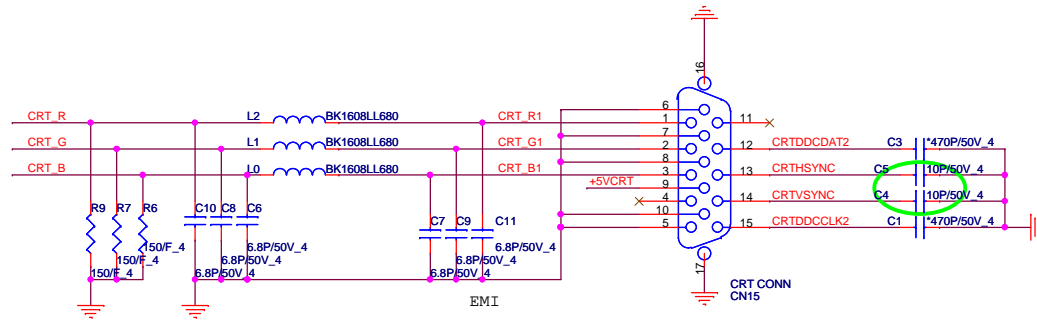
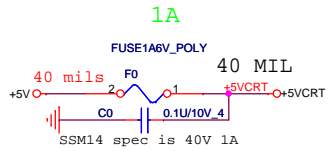
UMA & DISCRETE HDMI HPD SENSE



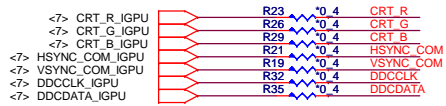
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	HDMI CONN	
Date: Monday, November 16, 2009	Sheet 21 of 40	

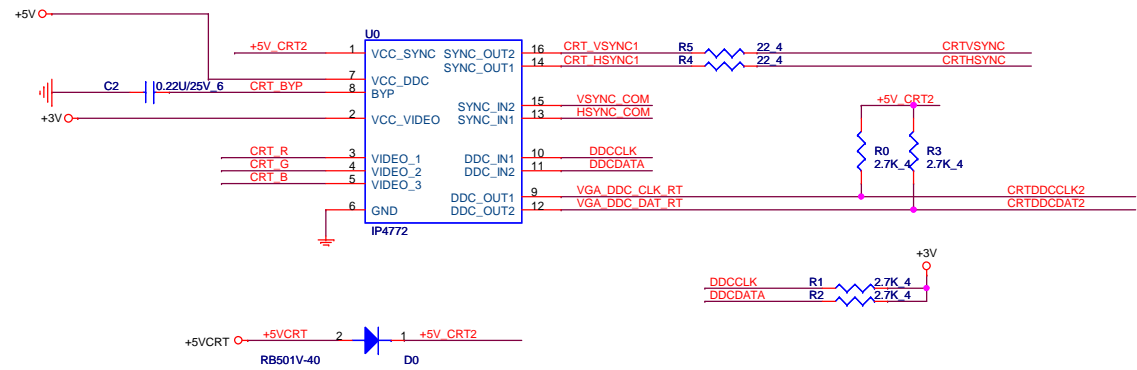
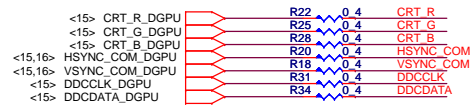
CRT PORT



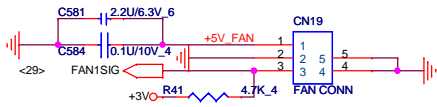
FOR UMA



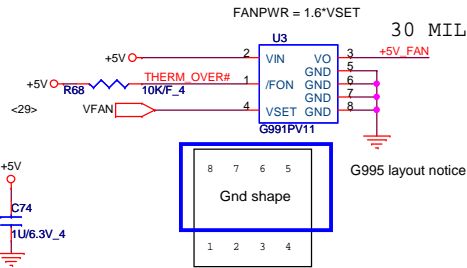
FOR DISCRETE



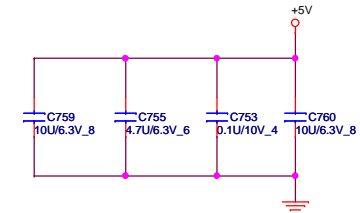
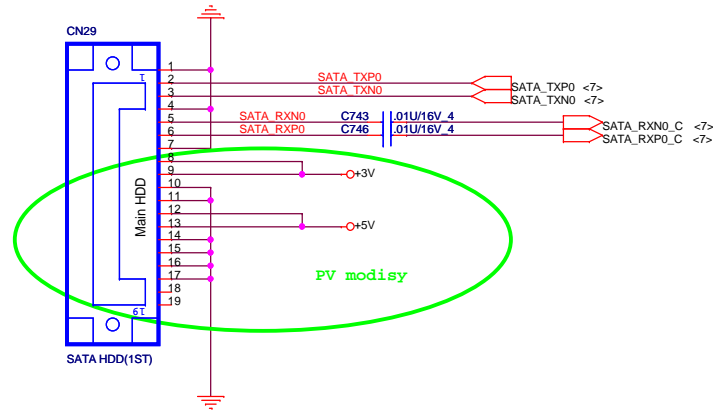
CPU FAN



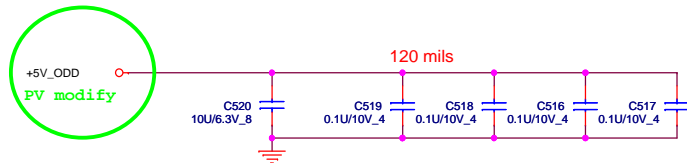
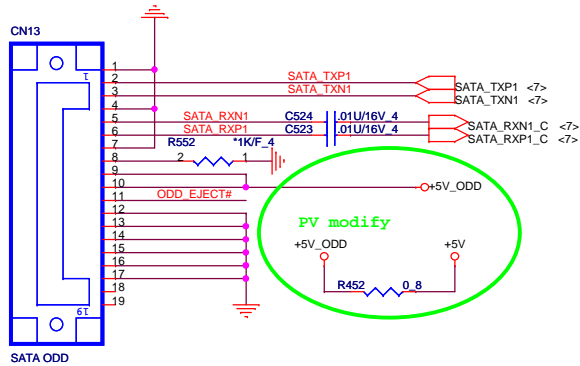
DFHD03MR008



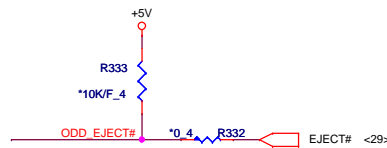
SATA HDD CONNECTOR



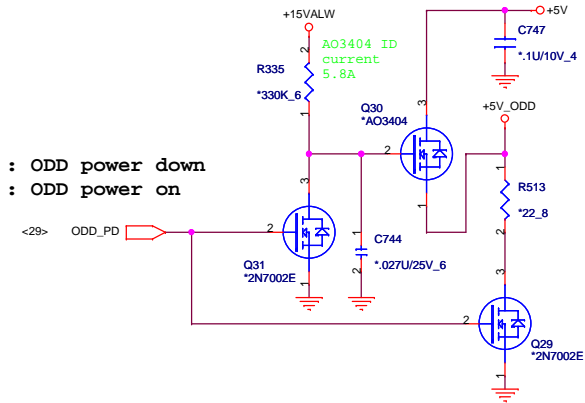
SATA ODD CONNECTOR



SI Add

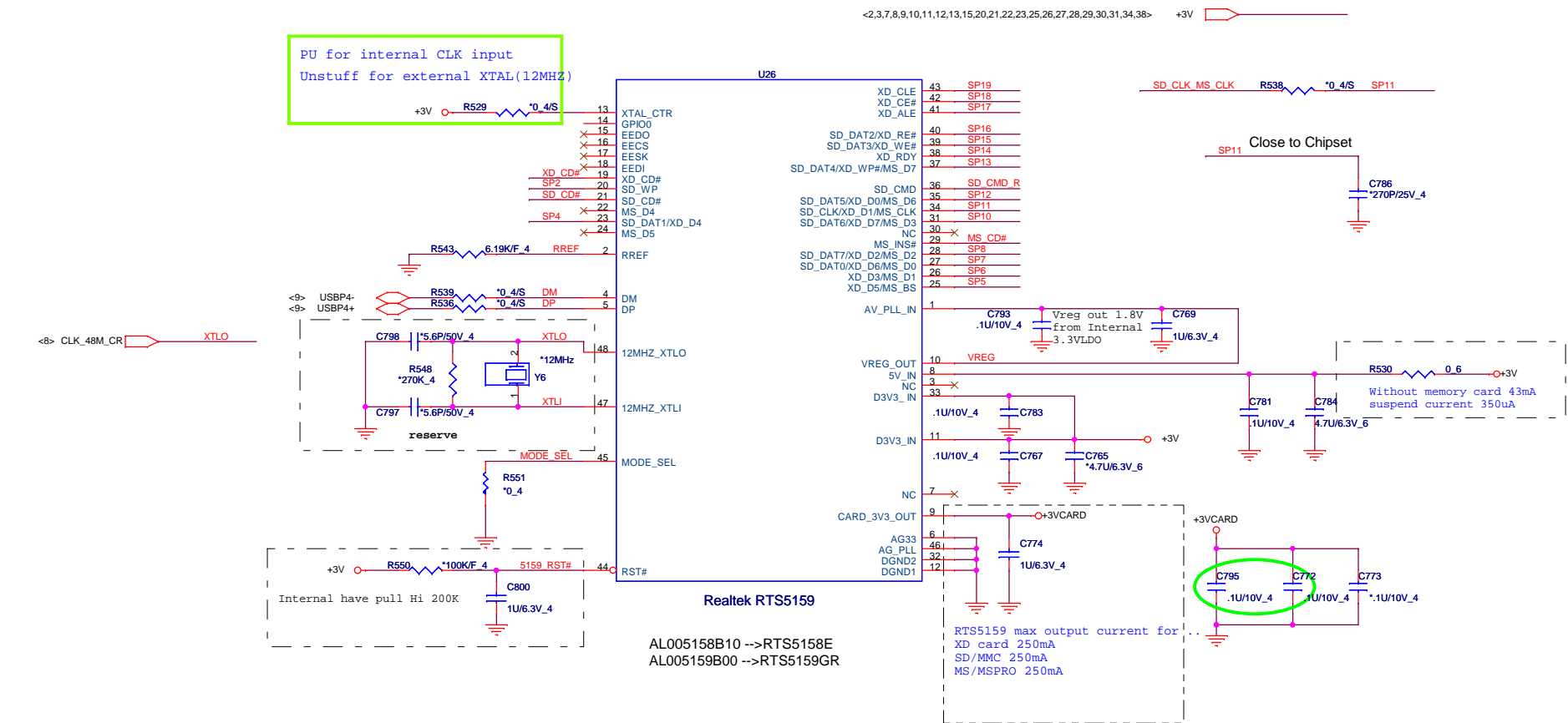


High : ODD power down
Low : ODD power on



PROJECT :AX1
Quanta Computer Inc.

PU for internal CLK input
Unstuff for external XTAL(12MHZ)

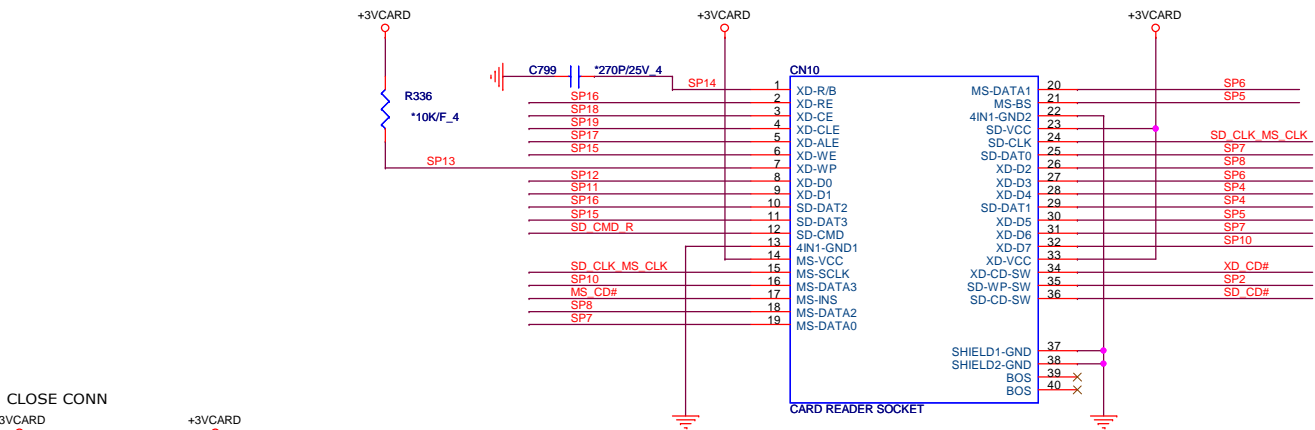


Realtek RTS5159
AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR

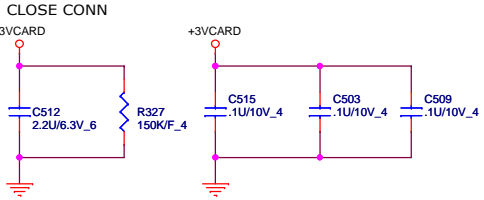
RTS5159 max output current for...
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

Note:

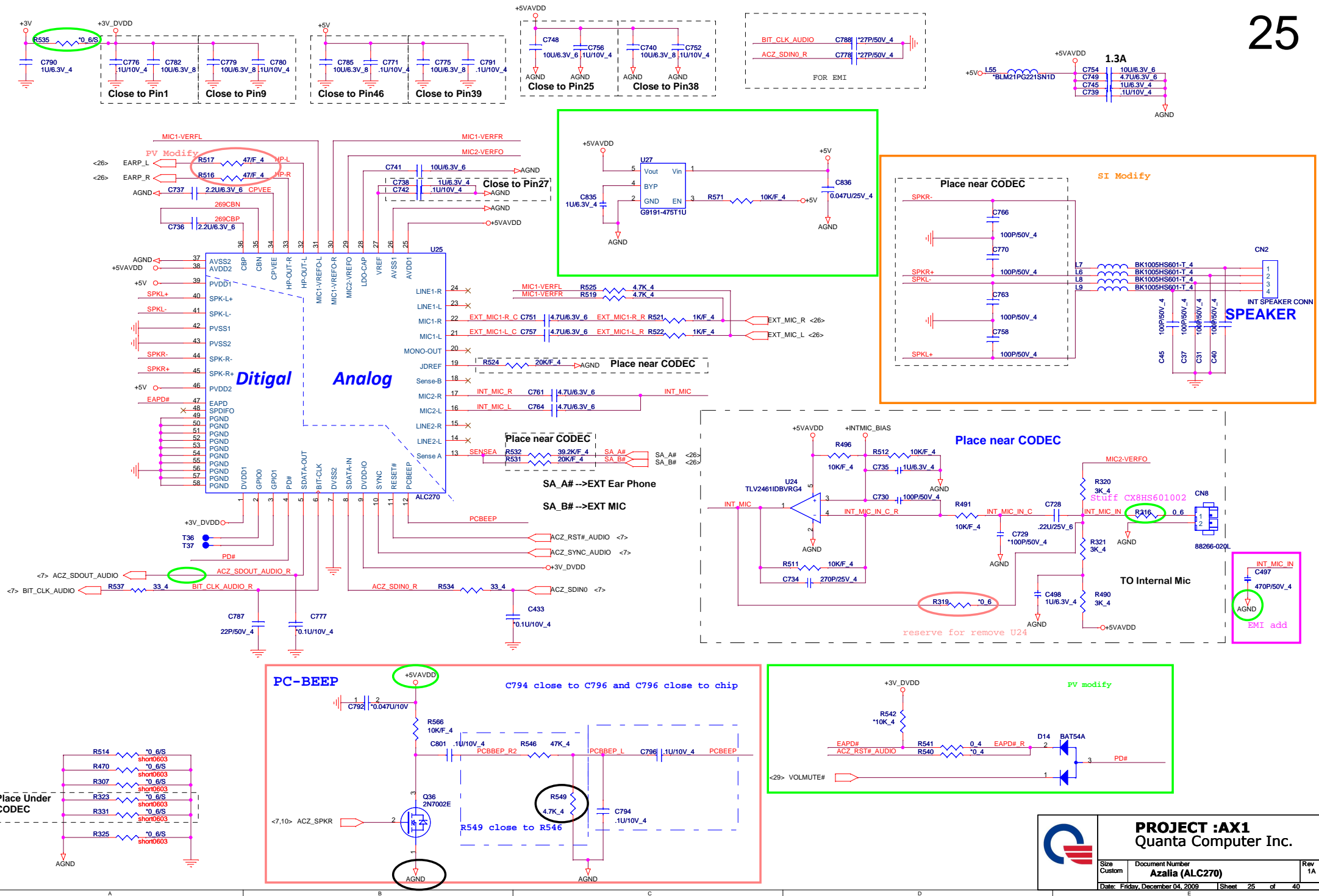
SP0	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5		MS BS XD D5
SP6	MS INS#	MS D1 XD D3
SP7	SD_DAT0	MS D0 XD D6
SP8	SD_DAT7	MS D2 XD D2
SP9		MS INS#
SP10	SD_DAT6	MS D3 XD D7
SP11	SD_CLK	MS_SCLK XD D1
SP12	SD_DAT5	XD D0
SP13	SD_DAT4	XD_WP#
SP14		XD R/B#
SP15	SD_DAT3	XD WE#
SP16	SD_DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE



5 IN1 CARD-READER (PUSH-PUSH)
Support SD/SD PRO/MMC/MS/MS PRO/XD Cards



PROJECT :AX1
Quanta Computer Inc.



Close to Pin1

Close to Pin9

Close to Pin46

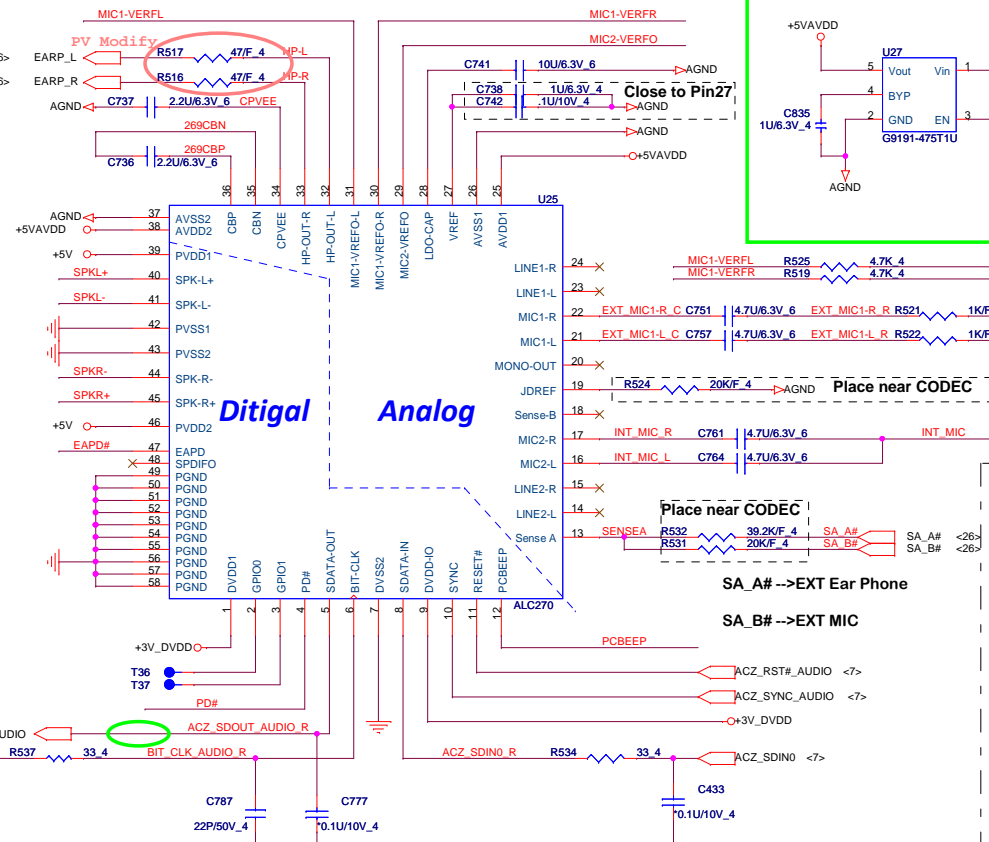
Close to Pin39

Close to Pin25

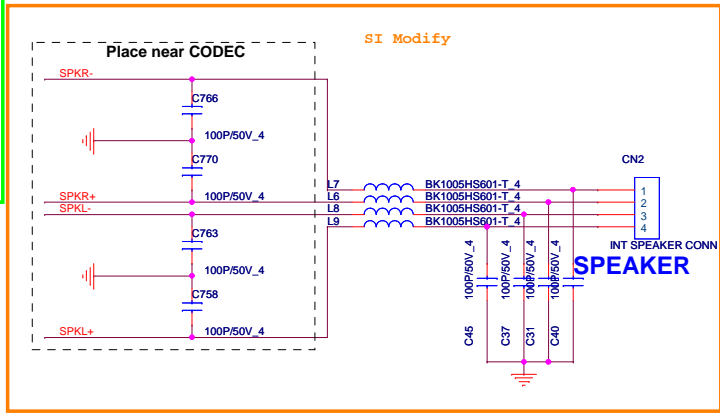
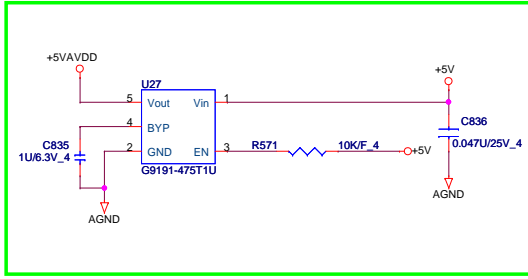
Close to Pin38

BIT_CLK_AUDIO C788 *27P/50V_4
ACZ_SDIN0_R C778 *27P/50V_4
FOR EMI

+5VAVDD 1.3A
C754 10U/6.3V_6
C749 4.7U/6.3V_6
C745 1U/6.3V_4
C739 .1U/10V_4



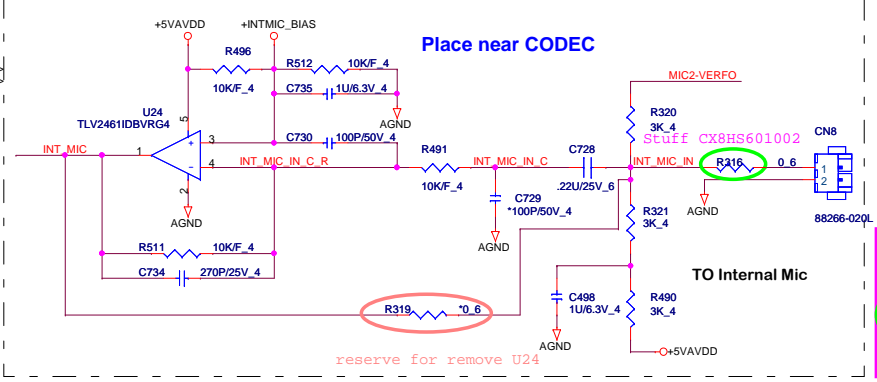
Digital Analog



Place near CODEC

SI Modify

INT SPEAKER CONN
SPEAKER

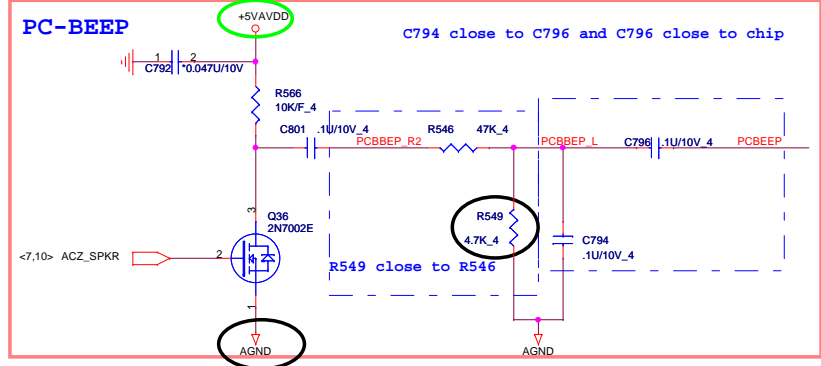


Place near CODEC

TO Internal Mic

reserve for remove U24

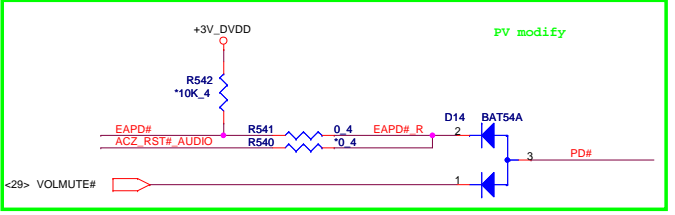
INT MIC IN
C497 470P/50V_4
EMI add



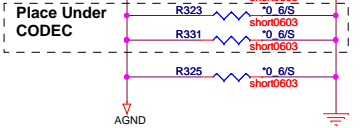
PC-BEEP

C794 close to C796 and C796 close to chip

R549 close to R546



PV modify



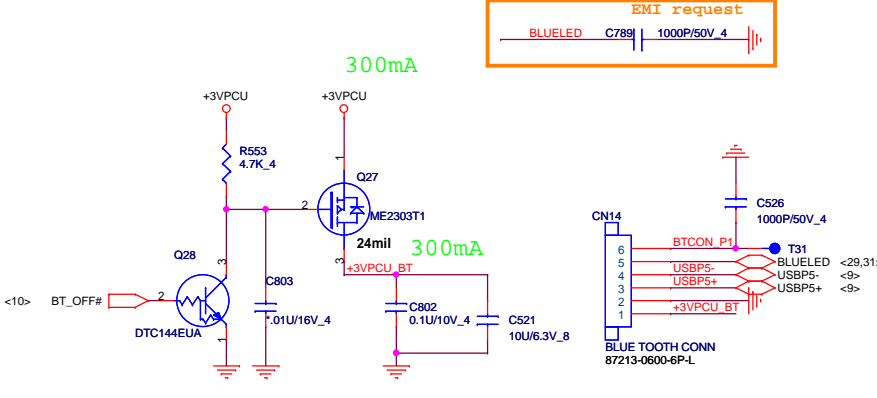
Place Under CODEC



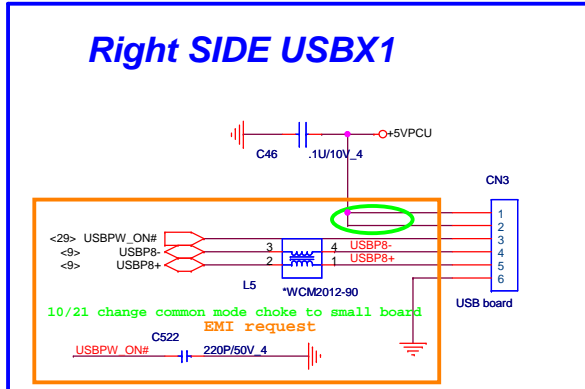
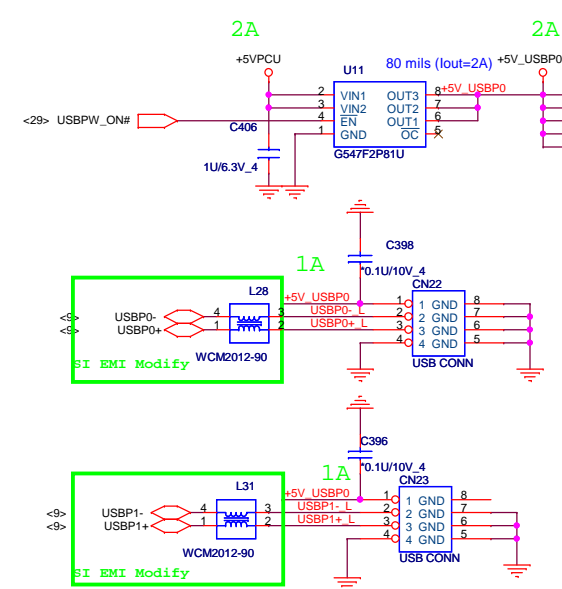
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number Azalia (ALC270)	Rev 1A
Date: Friday, December 04, 2009 Sheet 25 of 40		

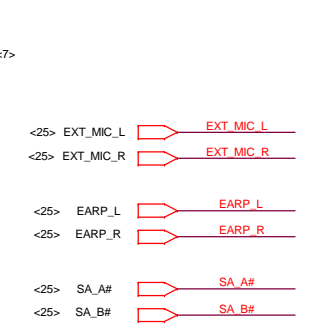
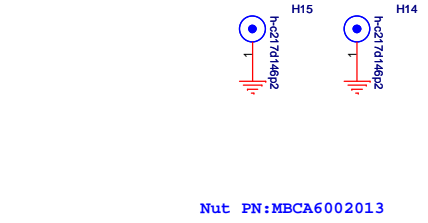
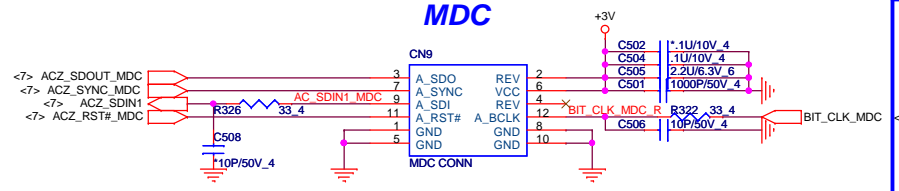
BLUETOOTH



LEFT SIDE USBX1

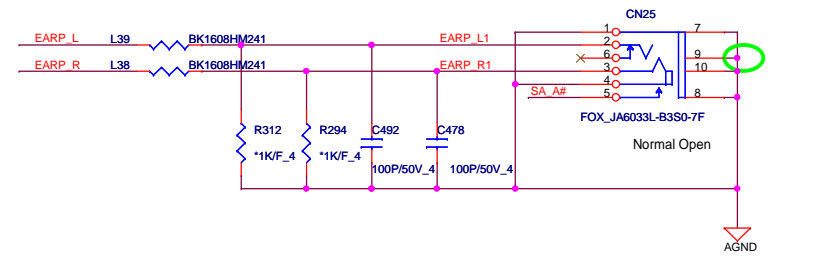


Modem CONN

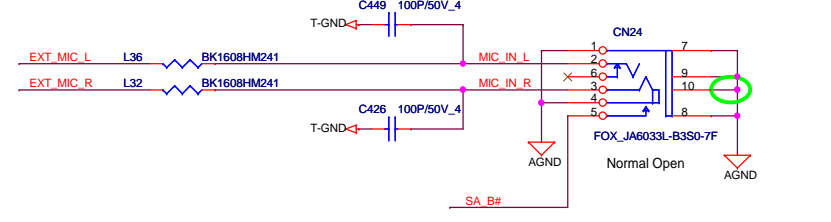


SA_A# --> EXT Ear Phone
SA_B# --> EXT MIC

Line out

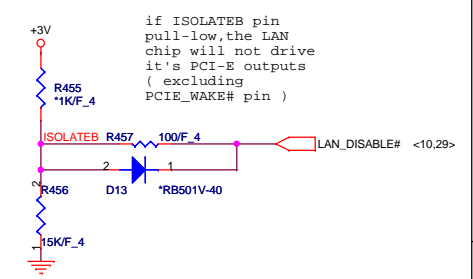
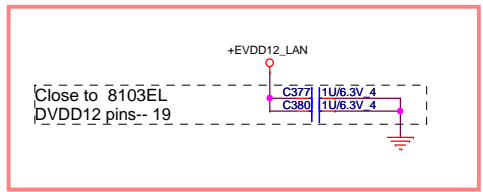
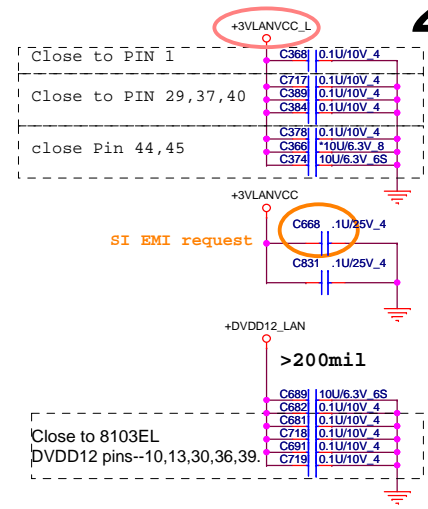
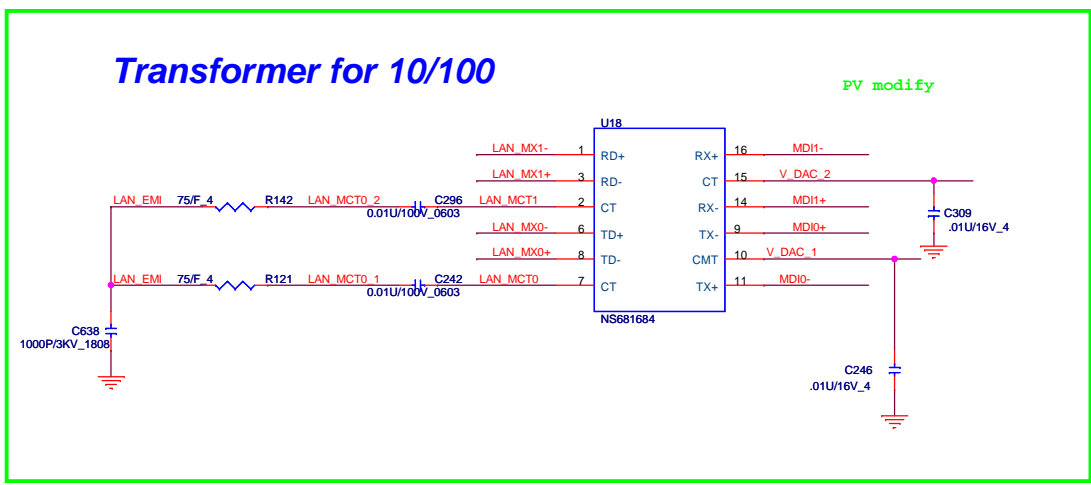
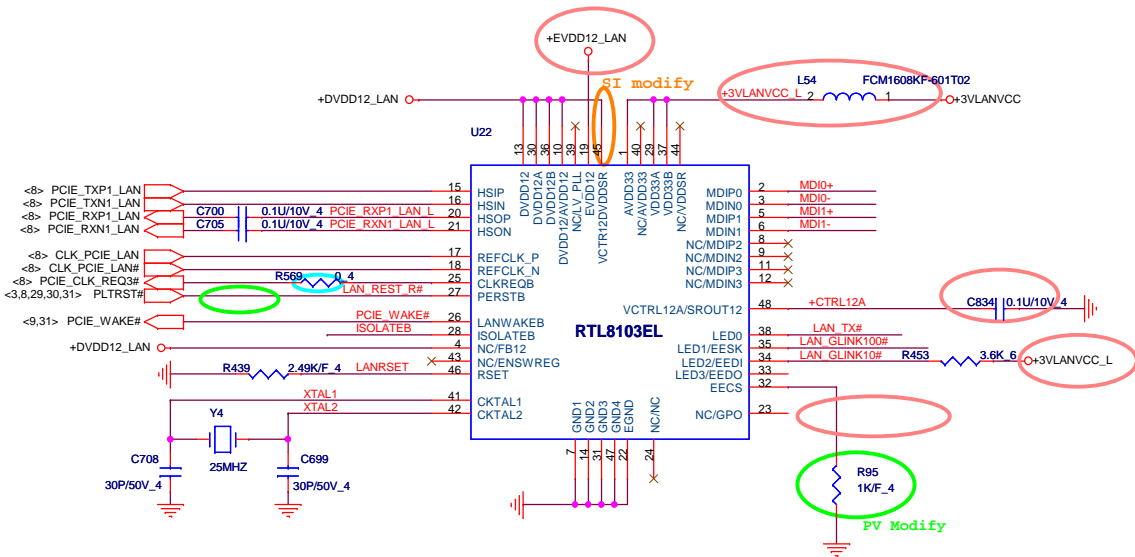


MIC

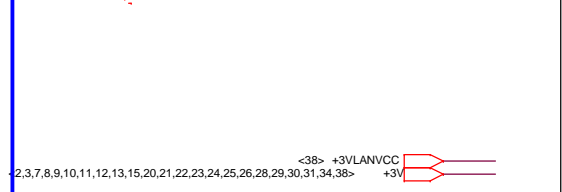
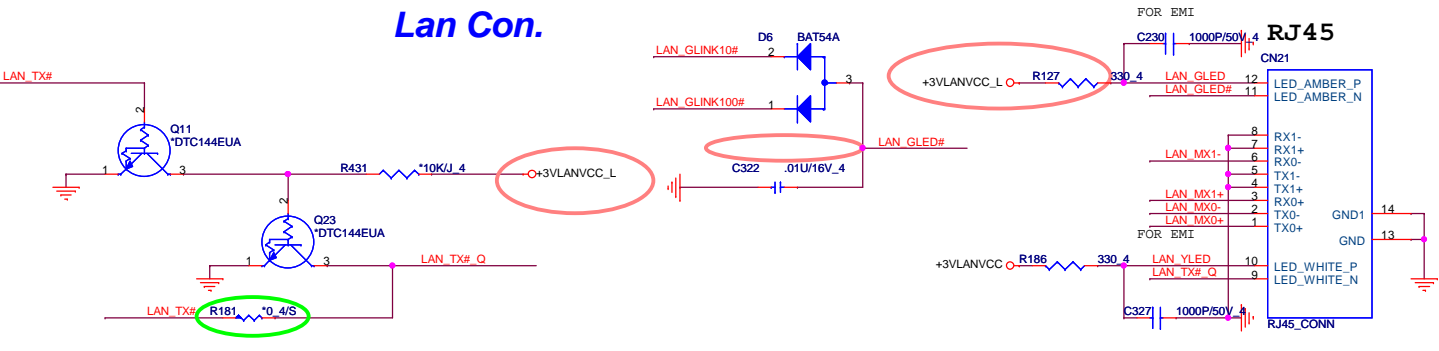


PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number USB/BT/Modem/Audio Jack	Rev 1A
Date: Monday, November 30, 2009 Sheet 26 of 40		



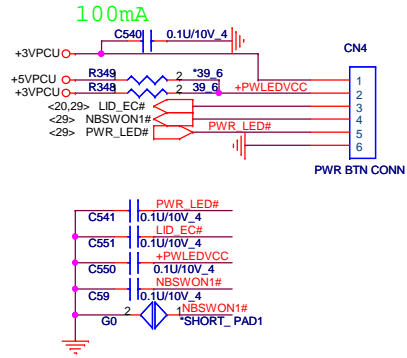
Lan Con.



PROJECT :AX1
Quanta Computer Inc.

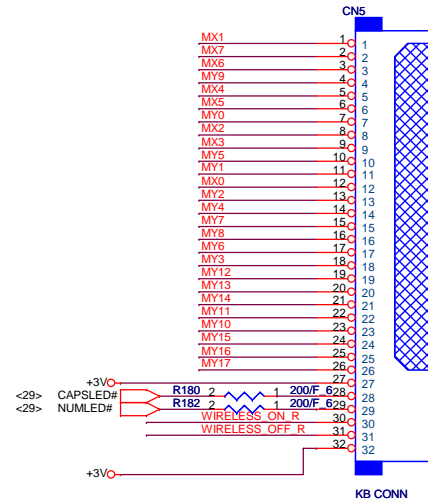
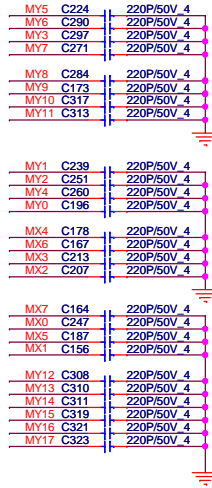
Size Custom	Document Number RTL811DL/8103EL	Rev 1A
Date: Monday, November 30, 2009 Sheet 27 of 40		

POWER BOTTON CONNECT

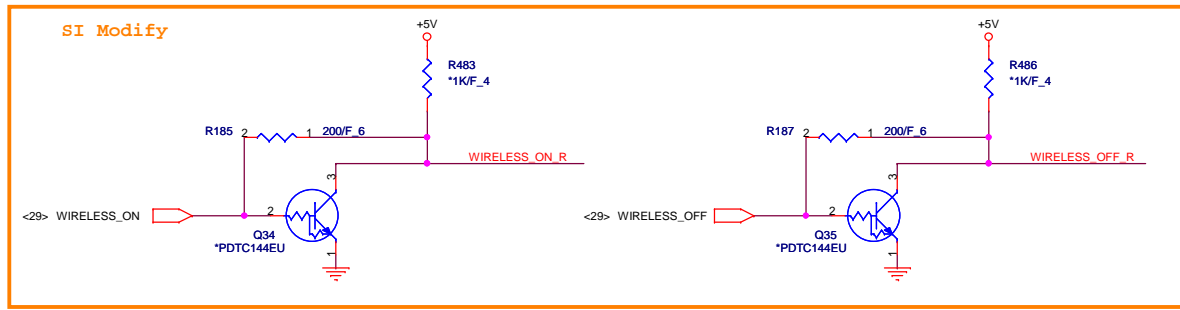
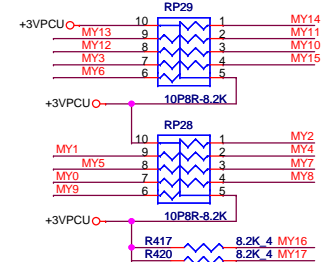


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

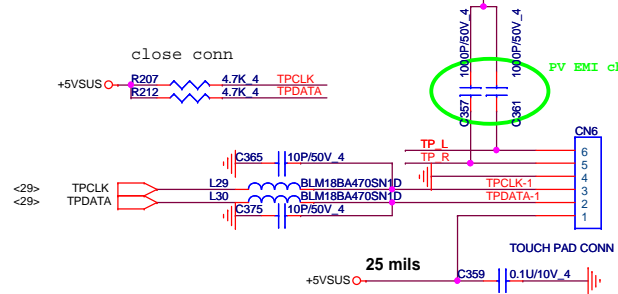
KEYBOARD Con.



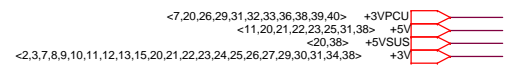
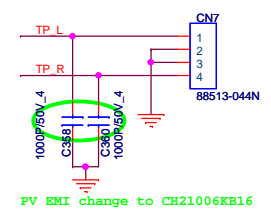
KEYBOARD PULL-UP

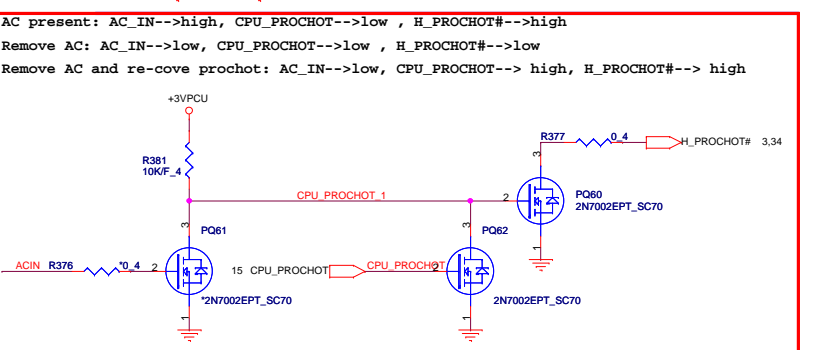
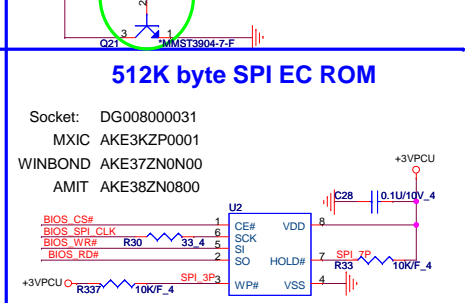
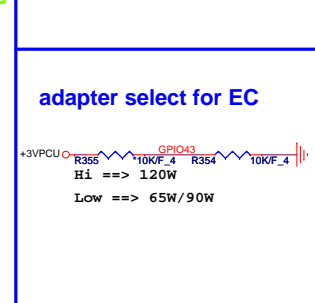
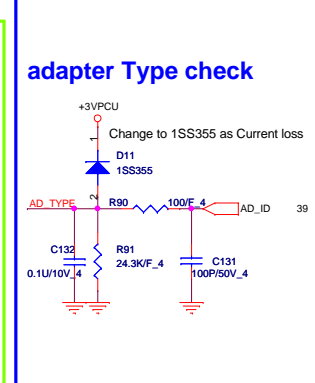
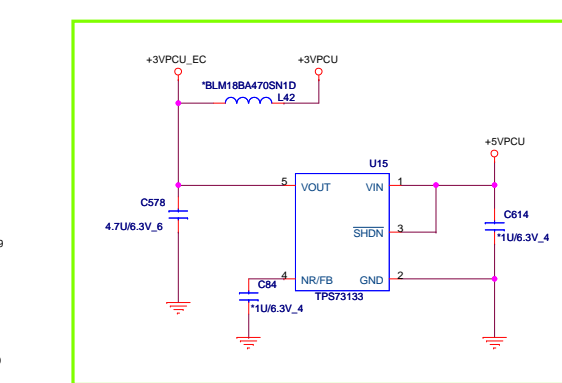
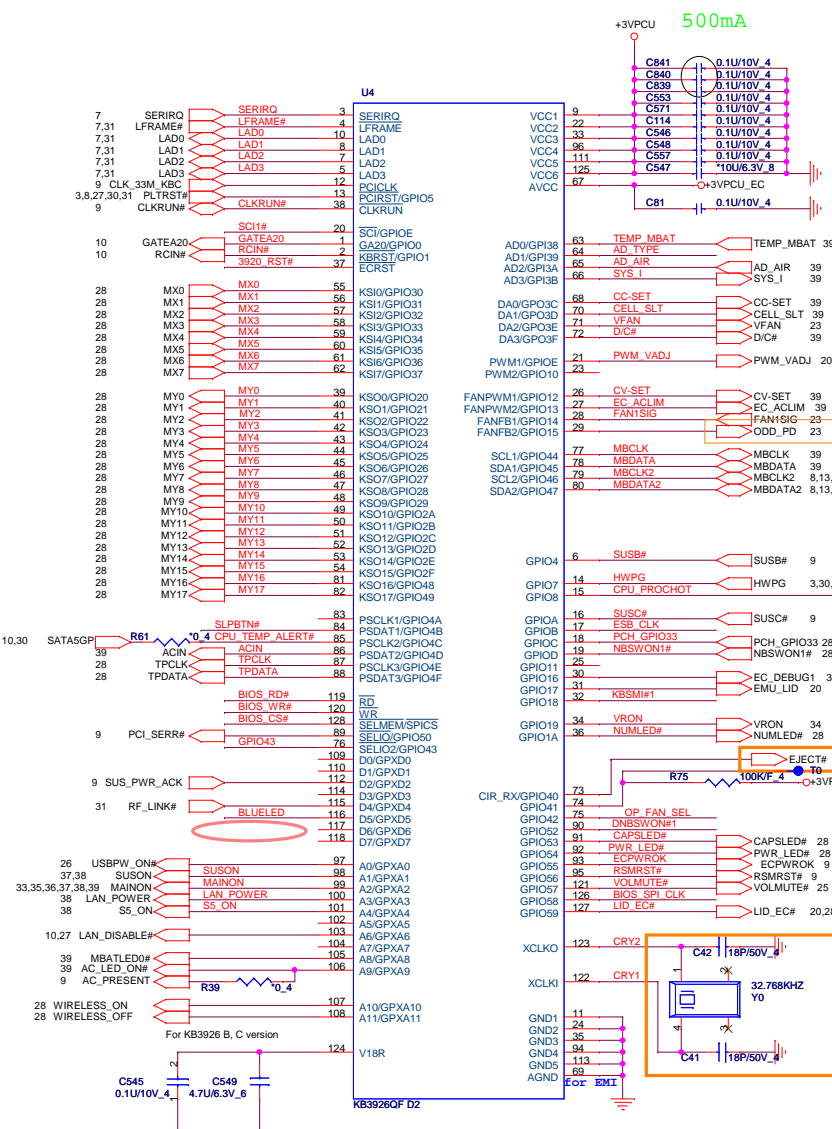


TOUCH PAD Con.



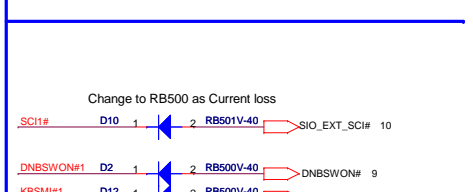
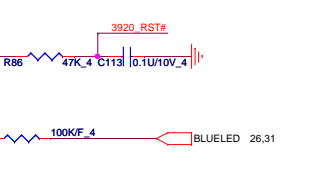
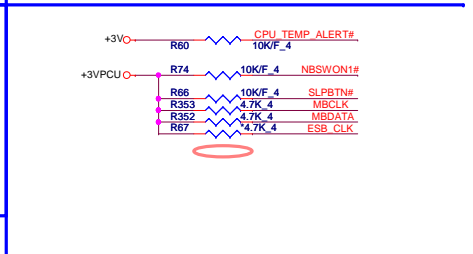
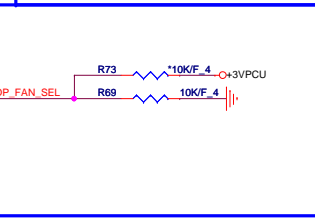
To TOUCH PAD SW board



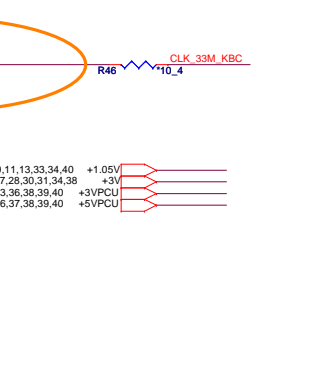
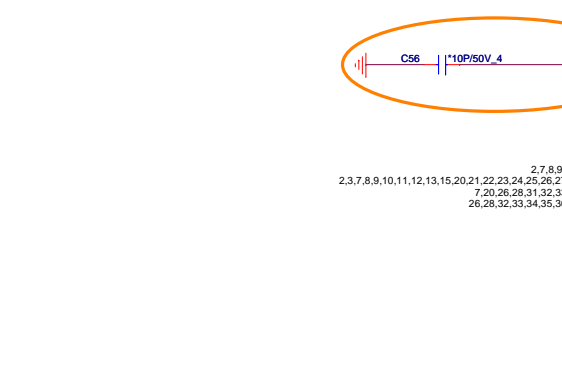


Project Model	GPIO42
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)

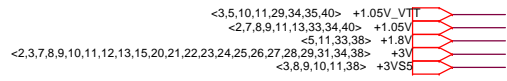
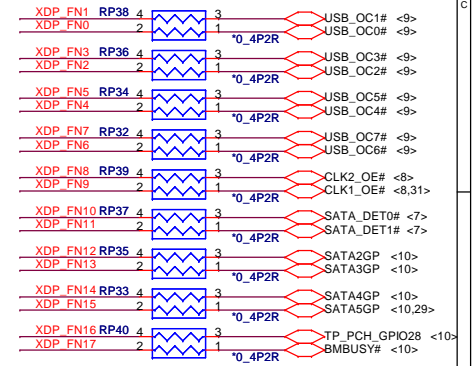
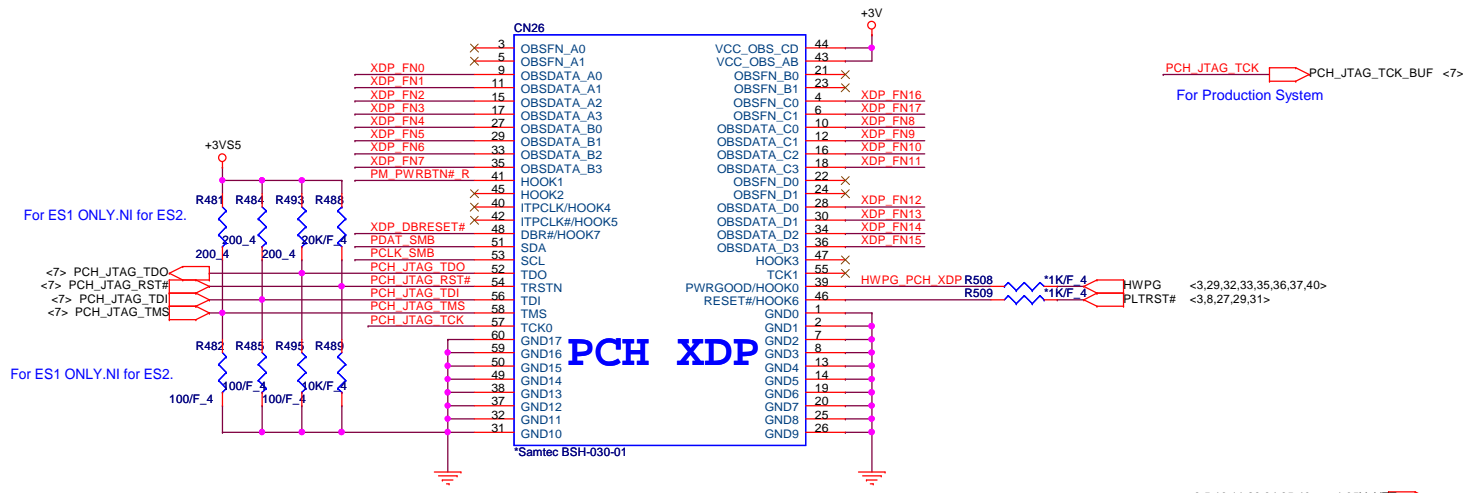
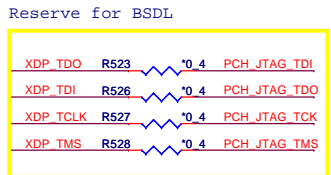
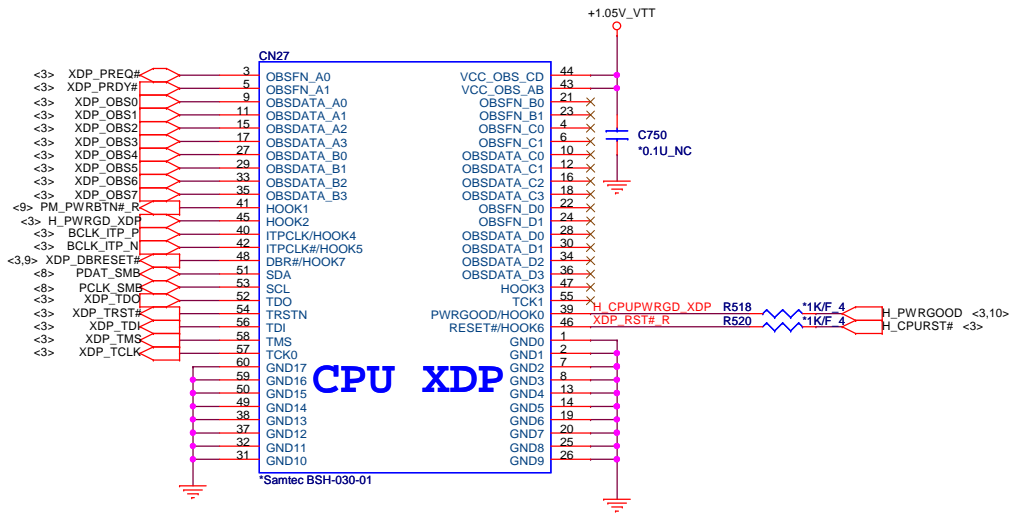
GPIO42 control fan table



AC present: AC_IN-->high, CPU_PROCHOT-->low, H_PROCHOT#-->high
 Remove AC: AC_IN-->low, CPU_PROCHOT-->low, H_PROCHOT#-->low
 Remove AC and re-cove prohot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high



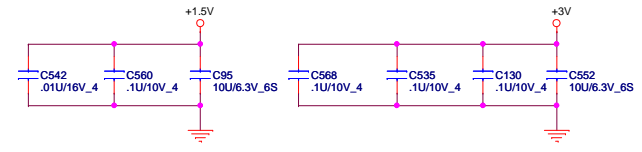
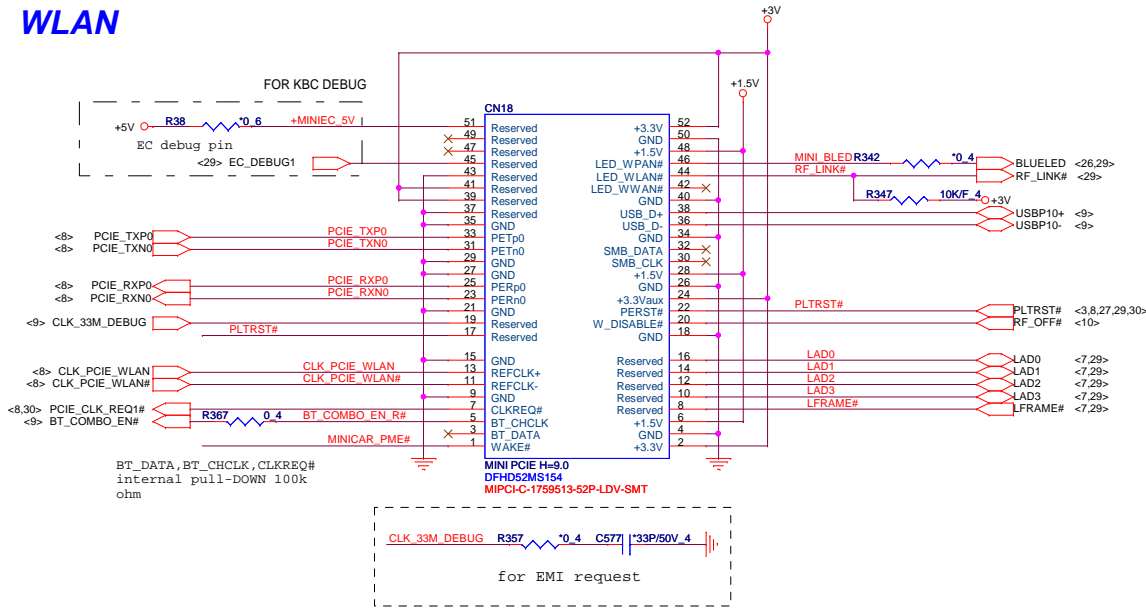
Change to RB500 as Current loss
 SIO_EXT_SCI# 10
 DNBSWON#1 9
 SIO_EXT_SMI# 10
 Add Pin 117,103 for DSM,116 for Bluetooth
 Delete T10 and tie pin 117 from Lan for DSM



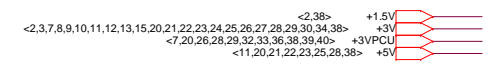
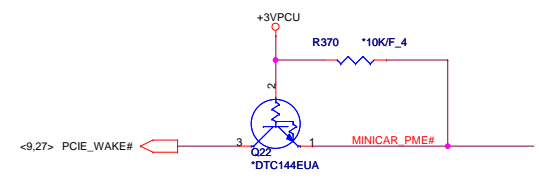
PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number XDP/BRAIDWOOD	Rev 1A
Date: Thursday, November 12, 2009 Sheet 30 of 40		

Mini PCI-E Card 1 WLAN



INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm



	PROJECT :AX1 Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X1	Rev 1A
	Date: Thursday, November 12, 2009 Sheet 31 of 40		

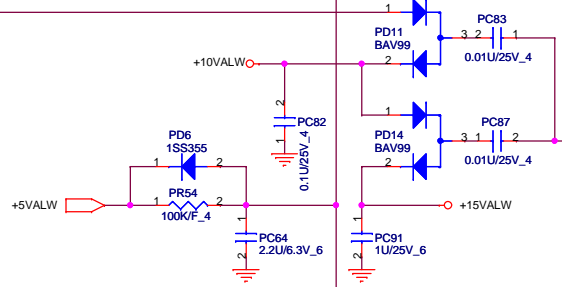
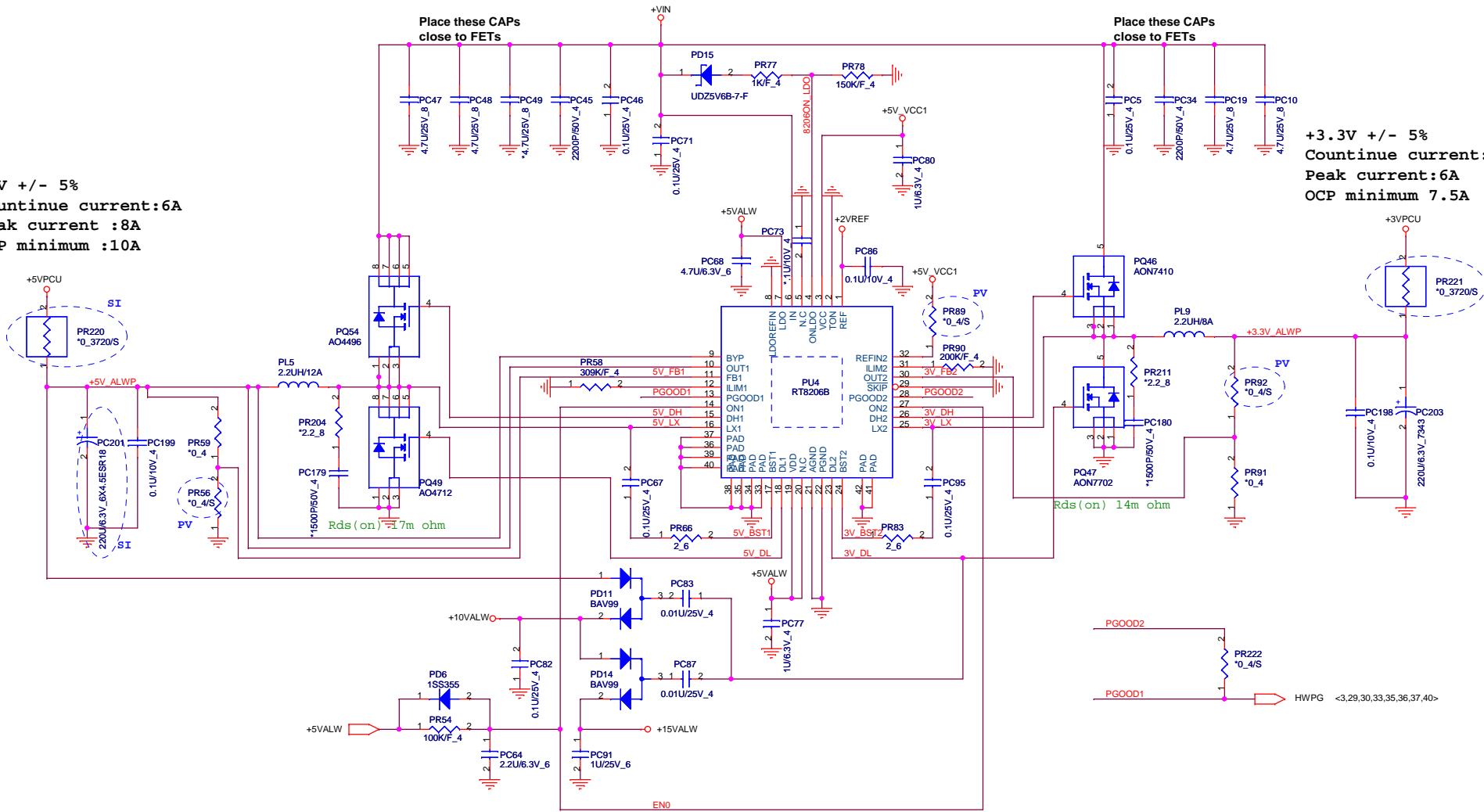
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
 Countinue current:6A
 Peak current :8A
 OCP minimum :10A

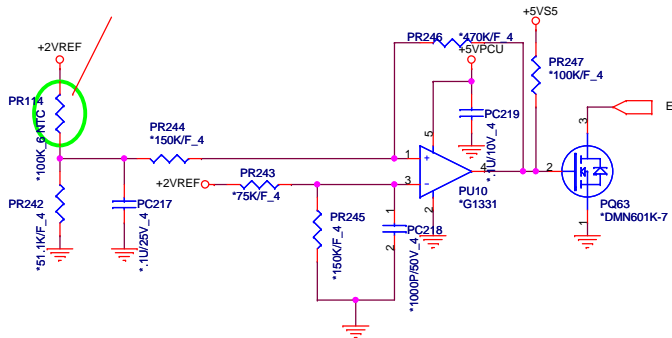
+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A

Place these CAPS
 close to FETs

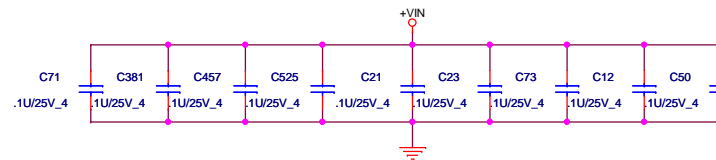
Place these CAPS
 close to FETs




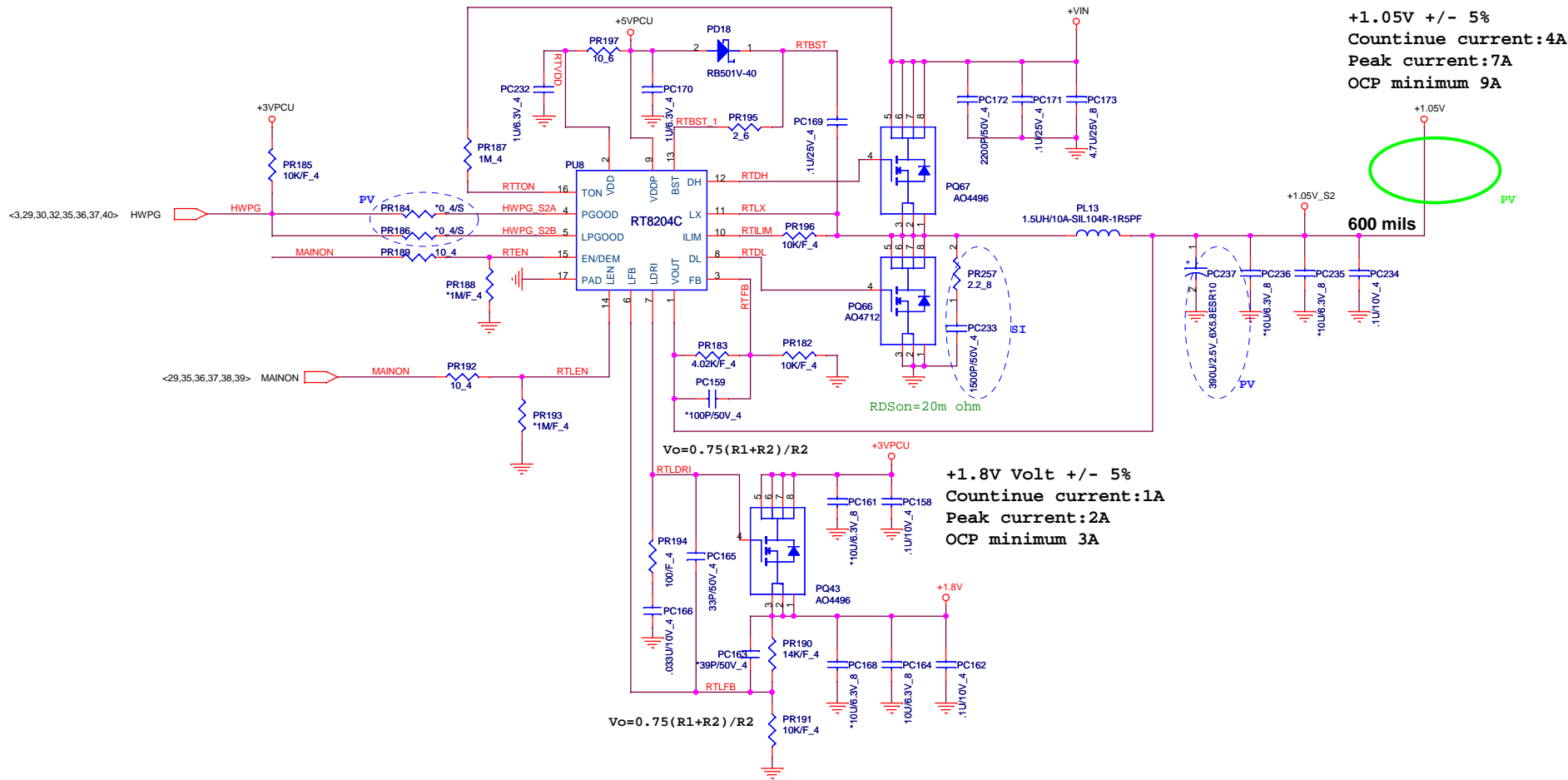
NTC need place under CPU Socket
 CPU Thermal protection at 90 +/-3 degrec




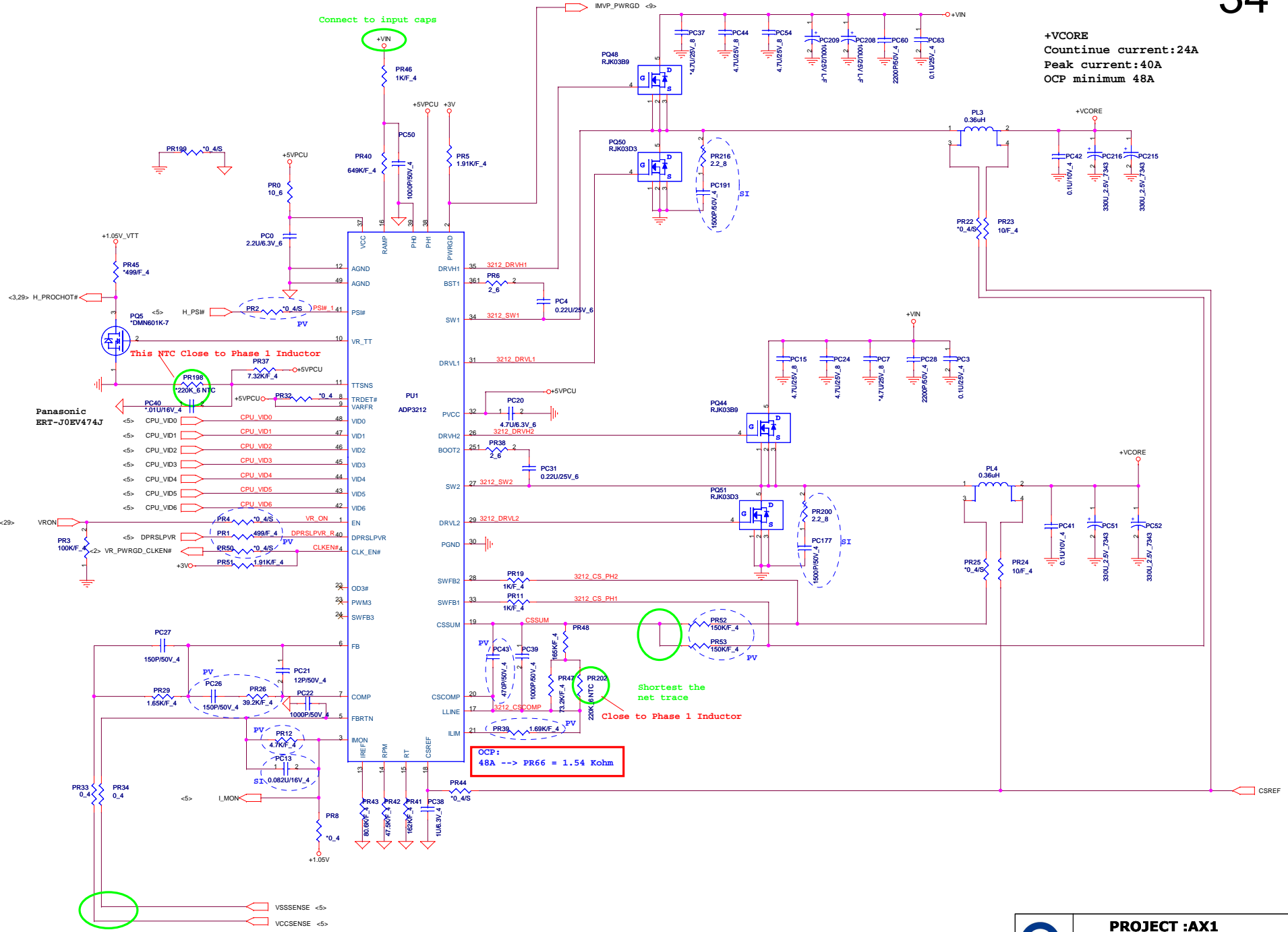
EMI request

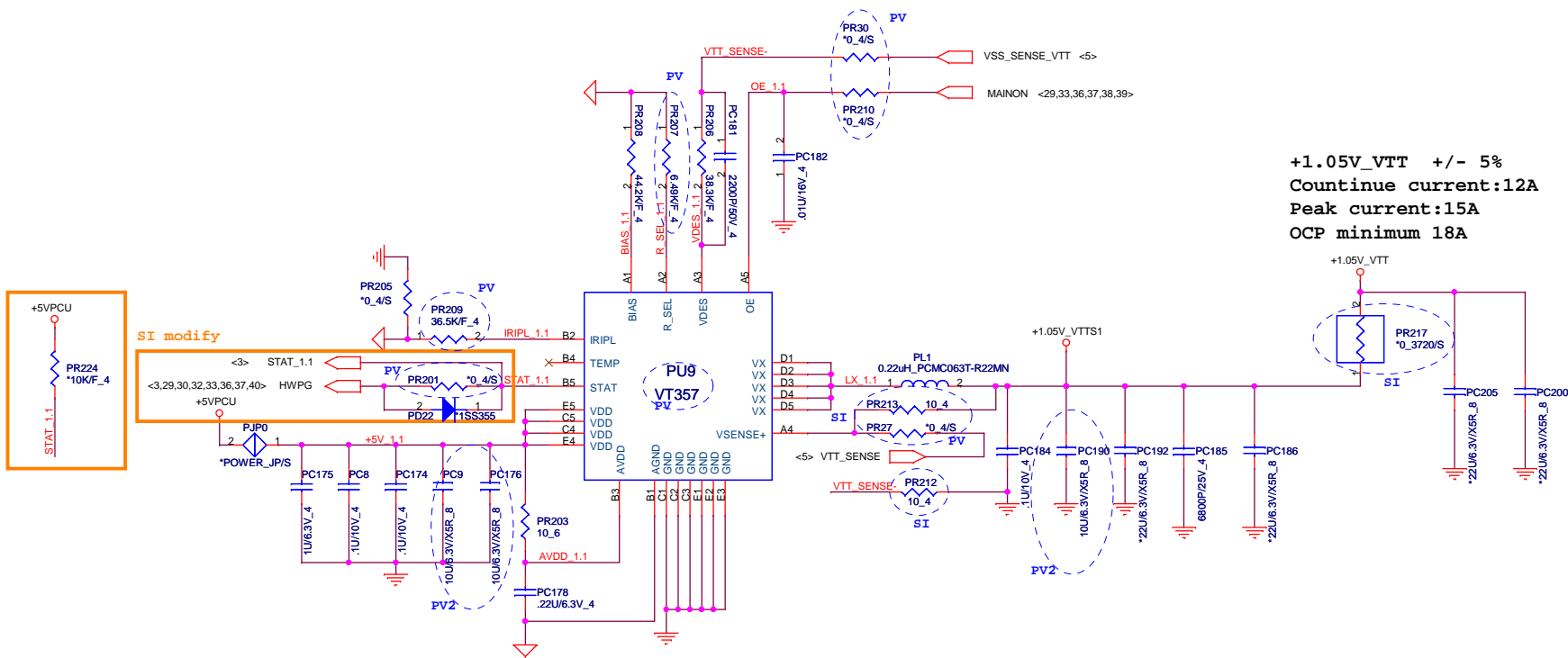


	PROJECT :AX1	
	Quanta Computer Inc.	
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Thursday, November 12, 2009 Sheet 32 of 40		



	PROJECT :AX1 Quanta Computer Inc.	
	Size Custom	Document Number +1.05V/+1.8V (RT8204C)
Date: Thursday, November 12, 2009 Sheet 33 of 40		





+1.05V_VTT +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



PROJECT :AX1
Quanta Computer Inc.

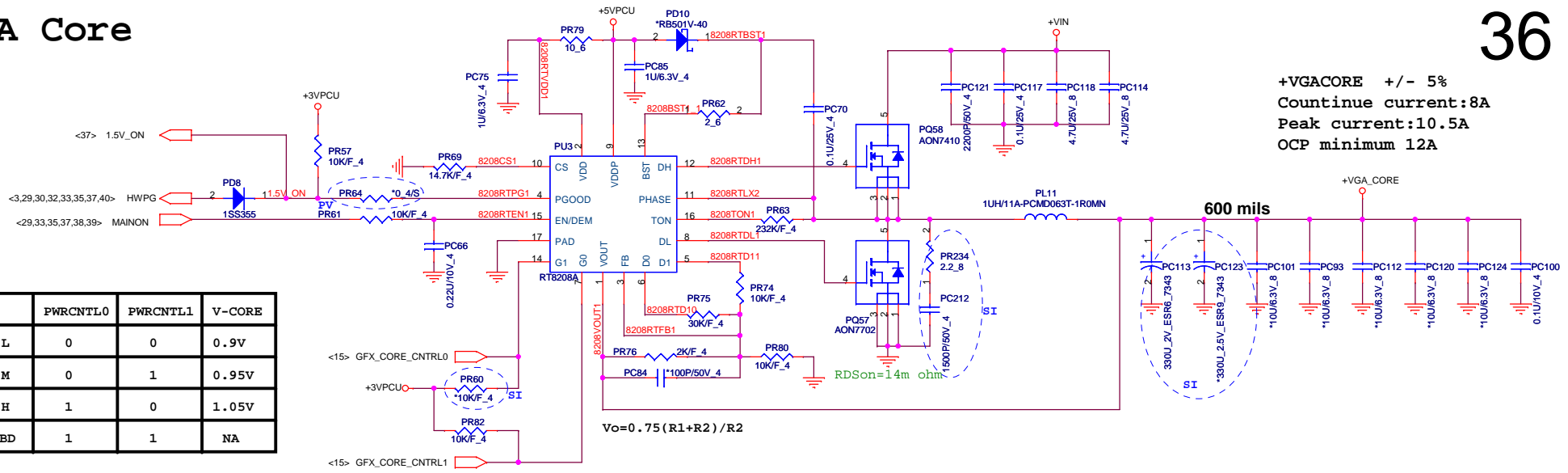
Size Custom	Document Number +1.05V_VTT (VT358)	Rev 1A
Date: Thursday, November 12, 2009		Sheet 35 of 40

VGA Core

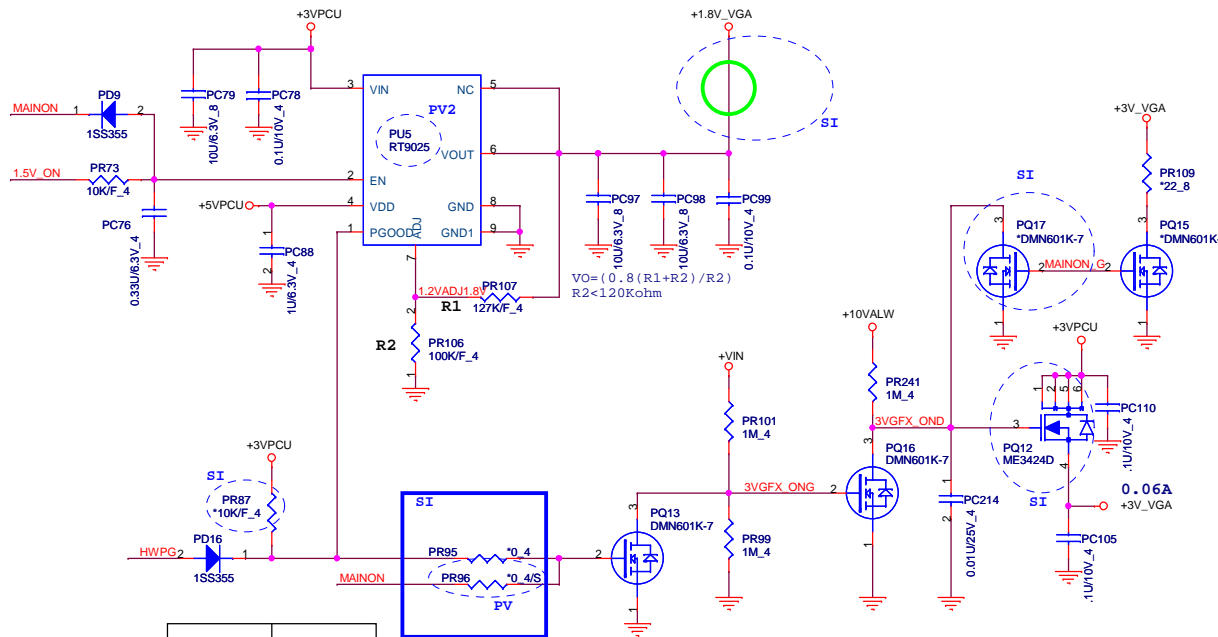
36

+VGCORE +/- 5%
Countinue current:8A
Peak current:10.5A
OCP minimum 12A

	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A

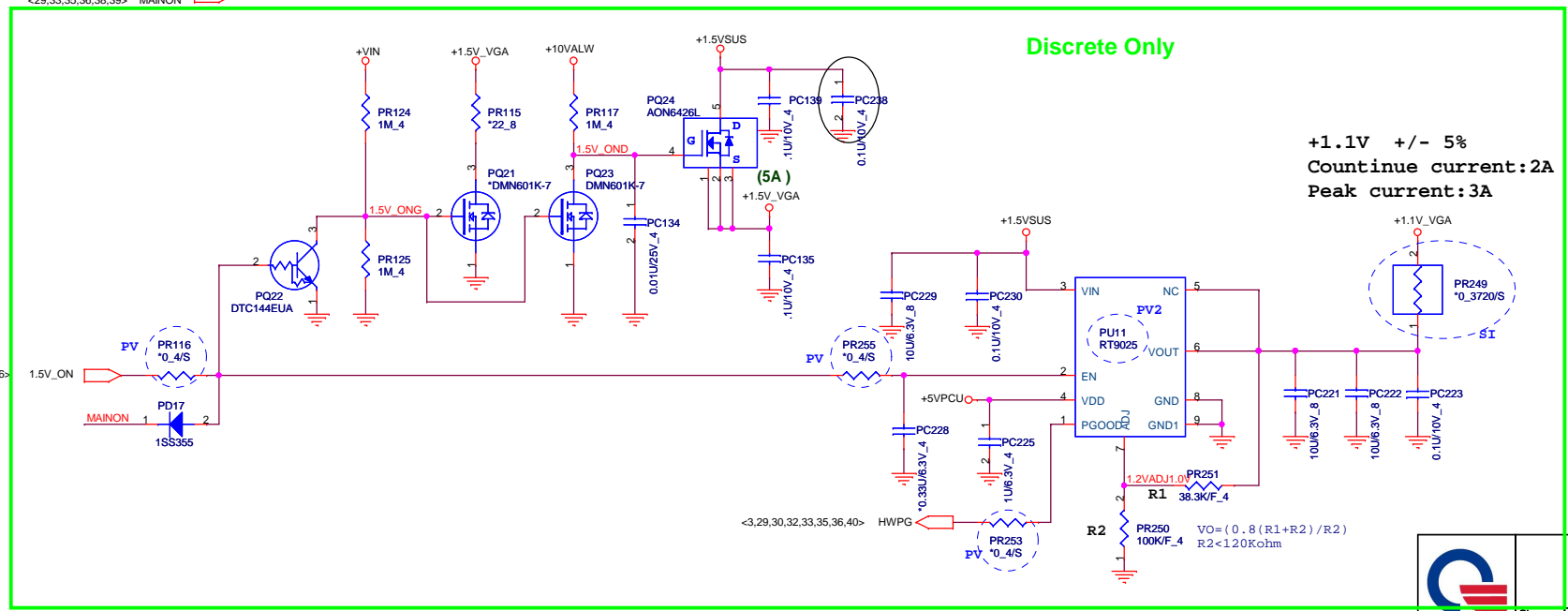
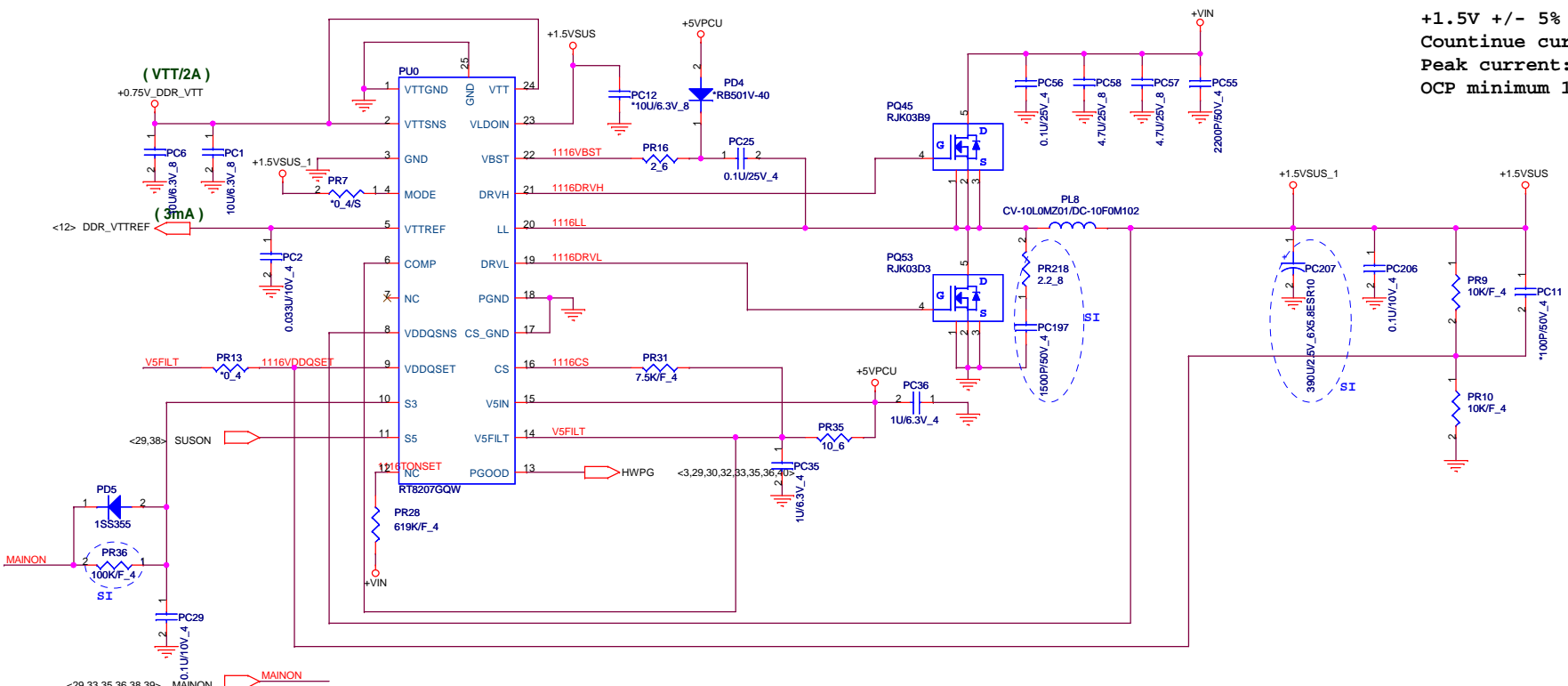


PR95	For M93
PR96	For PARK



PROJECT :AX1
Quanta Computer Inc.

+1.5V +/- 5%
 Countinue current:6A
 Peak current:12A
 OCP minimum 15A




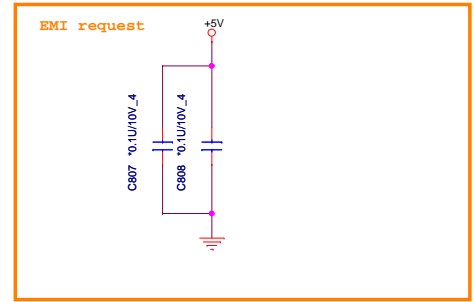
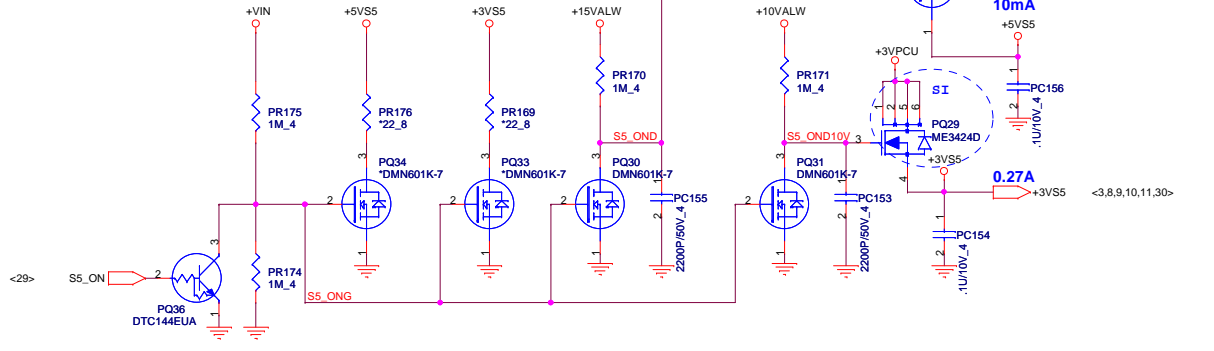
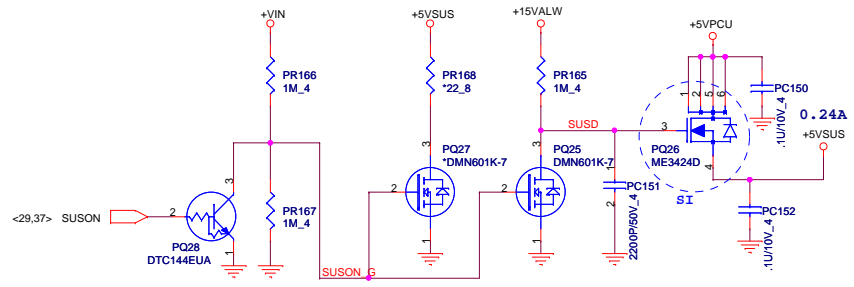
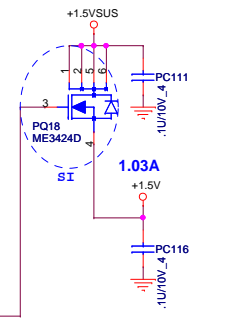
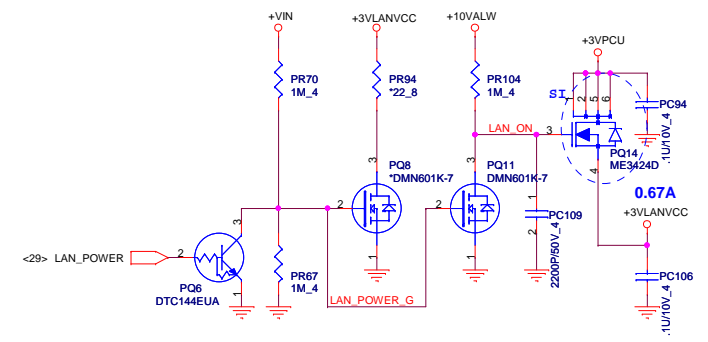
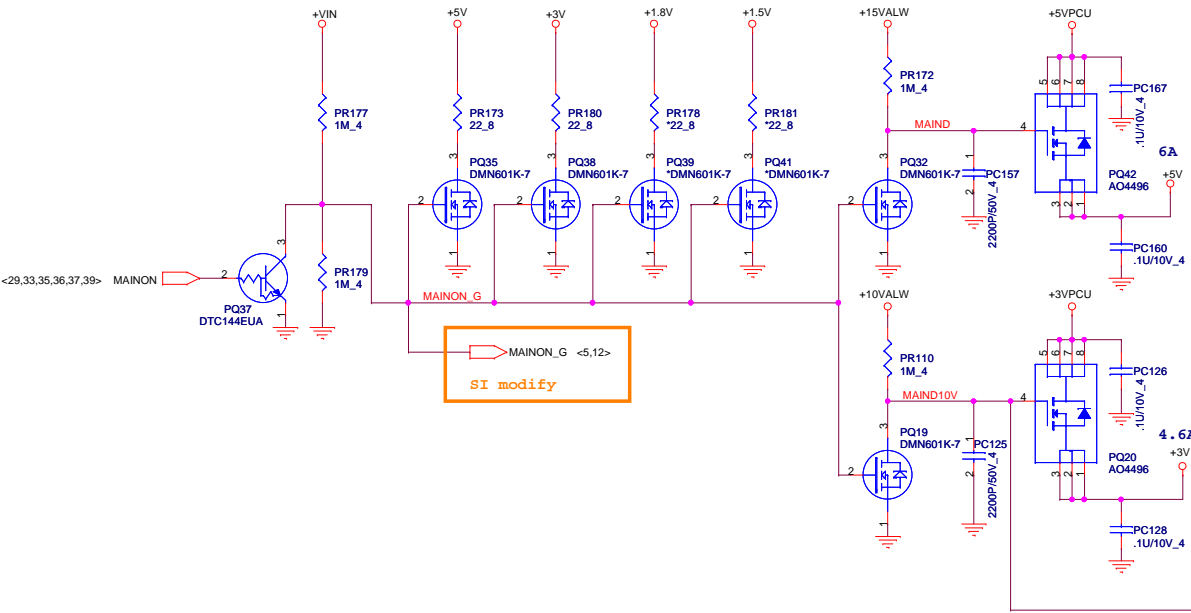
+1.1V +/- 5%
 Countinue current:2A
 Peak current:3A

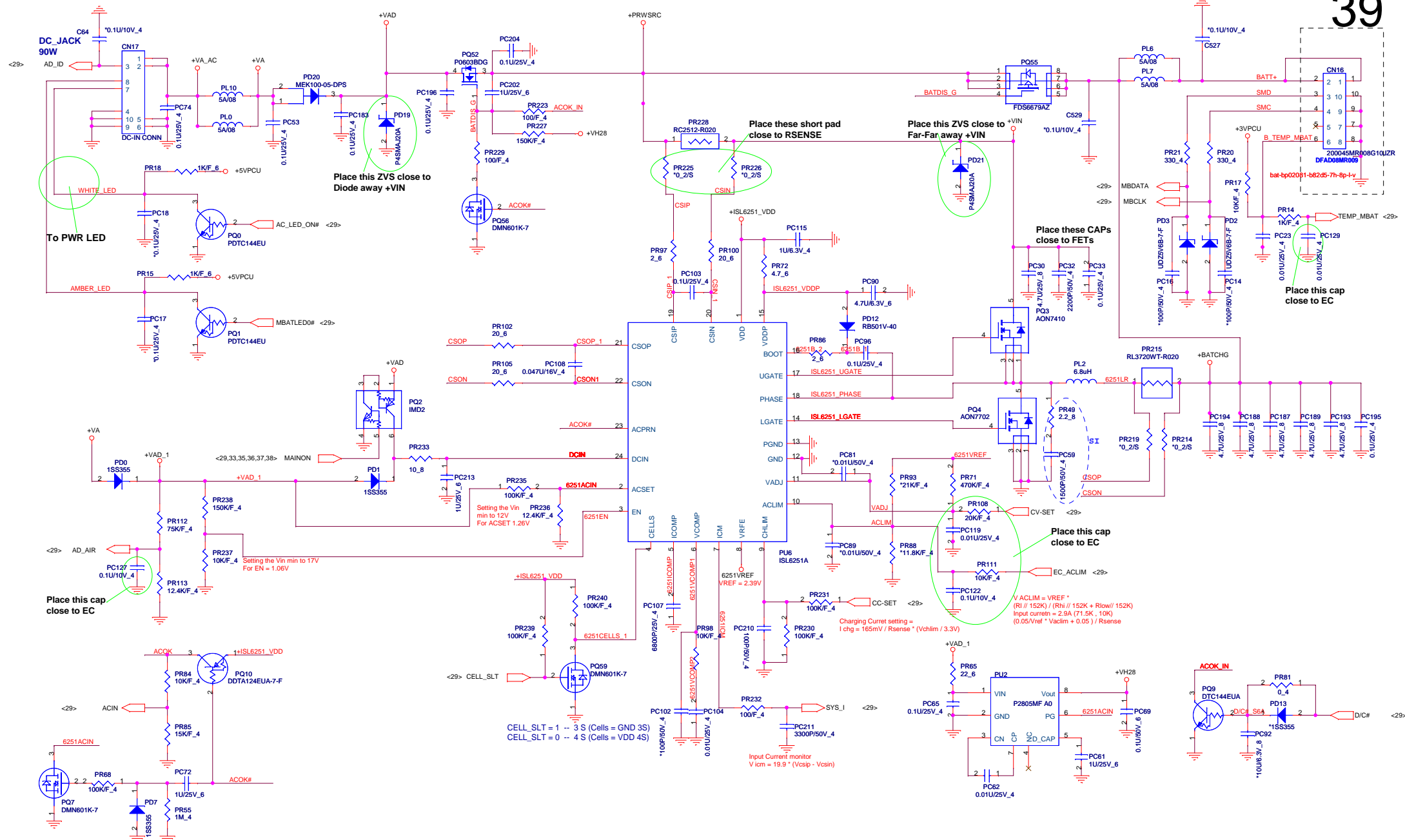


PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number DDR3 (RT8207)	Rev 1A
Date: Thursday, December 03, 2009 Sheet 37 of 40		

SI modify
 MAIND <5>





Place this ZVS close to Diode away +VIN

Place these short pad close to RSENSE

Place this ZVS close to Far-Far away +VIN

Place these CAPs close to FETs

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
 CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Input Current monitor
 $V_{icm} = 19.9 \cdot (V_{csp1} - V_{csm})$

$V_{AC LIM} = V_{REF} \cdot \frac{(R1 // 152K)}{(R_{hi} // 152K + R_{low} // 152K)}$
 Input current = 2.9A (71.5K, 10K)
 $(0.05 \cdot V_{ref} \cdot V_{aclim} + 0.05) / R_{sense}$

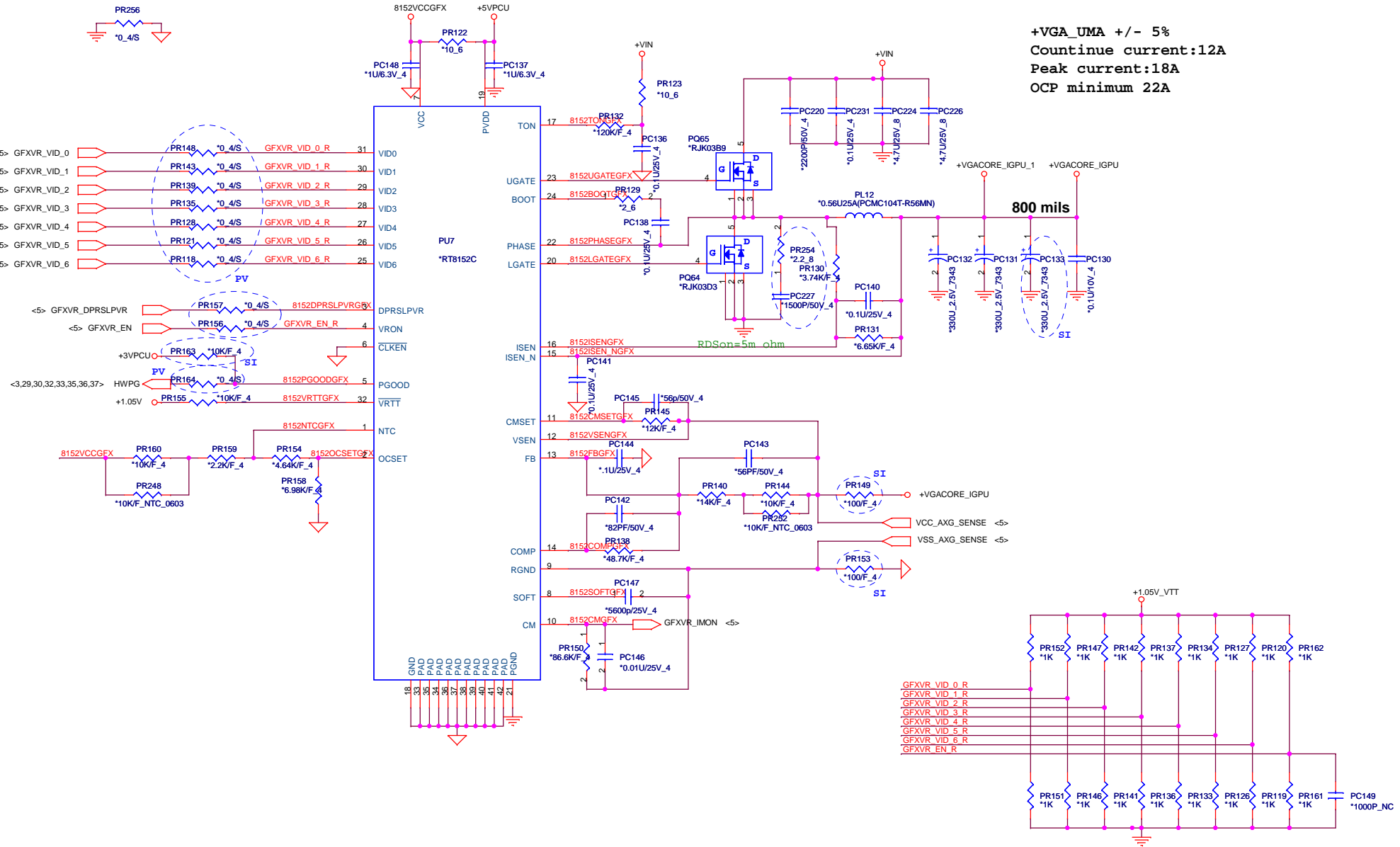
Charging Current setting =
 $I_{chg} = 165mV / R_{sense} \cdot (V_{chlim} / 3.3V)$



PROJECT :AX1
Quanta Computer Inc.

Size	Custom	Document Number	CHARGER (ISL6251)	Rev	1A
Date:	Thursday, November 12, 2009	Sheet	39	of	40

+VGA_UMA +/- 5%
Continue current:12A
Peak current:18A
OCp minimum 22A



PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number UMA GPU CORE (RT8152C)	Rev 1A
Date: Thursday, November 12, 2009 Sheet 40 of 40		