

1	2	3	4	5	6	7	8
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# Zenith UMA DDR3

## Cycle 1

### PV BUILD

2009.05.25

A  
B  
C  
D  
E  
F

A  
B  
C  
D  
E  
F

DATE	CHANGE NO.	REV
1	2	

DRAWER	EE	DATE	POWER	DATE	<b>INVENTEC</b>
DESIGN					
CHECK					TITLE
RESPONSIBLE					<i>Zenith UMA DDR3</i>
SIZE =	3	VER :			SIZE CODE
FILE NAME :	XXXX-XXXXXX-XX				A3 CS
P/N	XXXXXXXXXXXX				DOC. NUMBER
					Model No
					SHEET
					1 OF 52
					REV
					AXI

1	2	3	4	5	6	7	8
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	26- DDR3-DIMM0	47- BT & MDC & TCM
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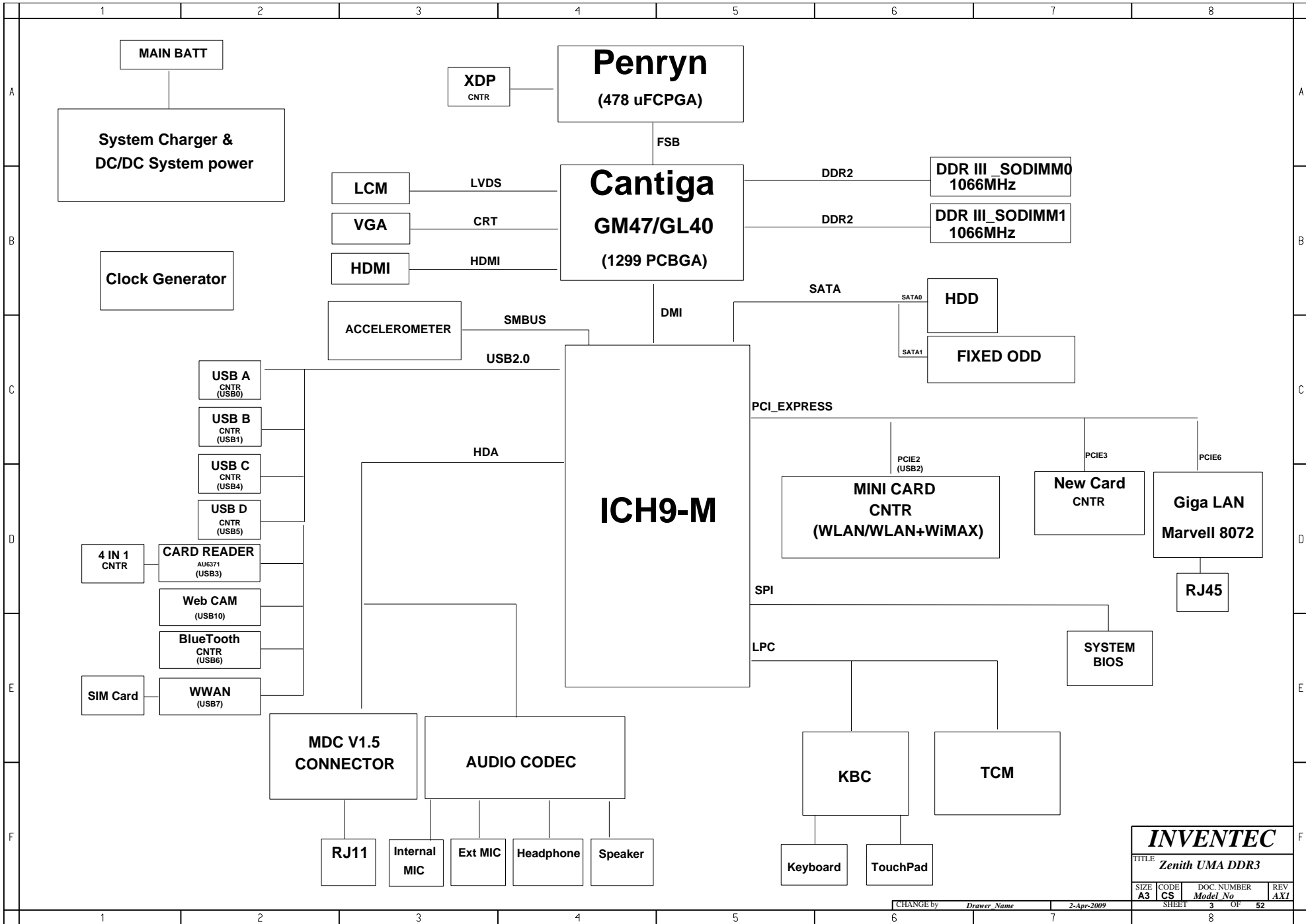
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TITLE *Zenith UMA DDR3*

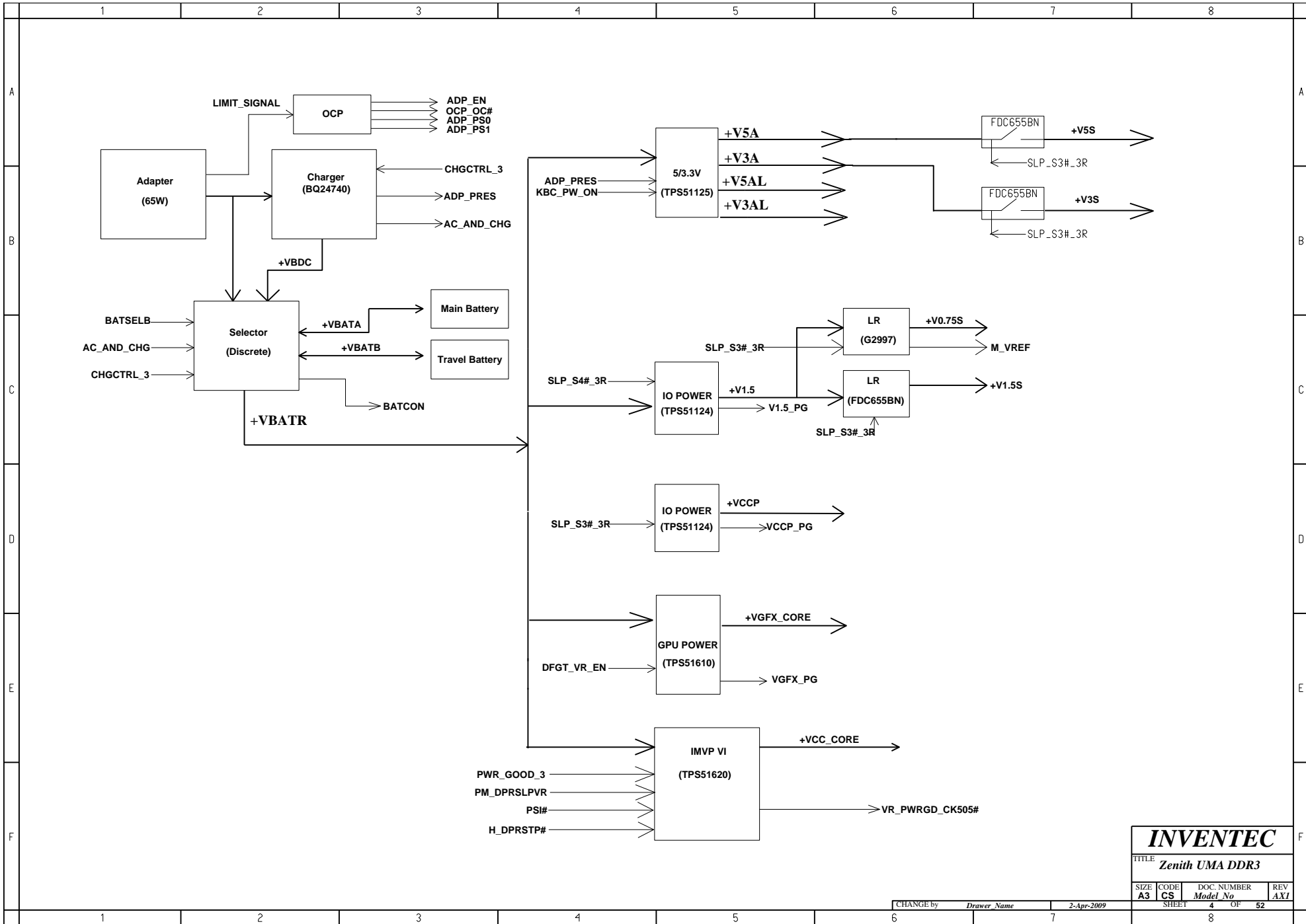
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Drawer Name* 2-Apr-2009

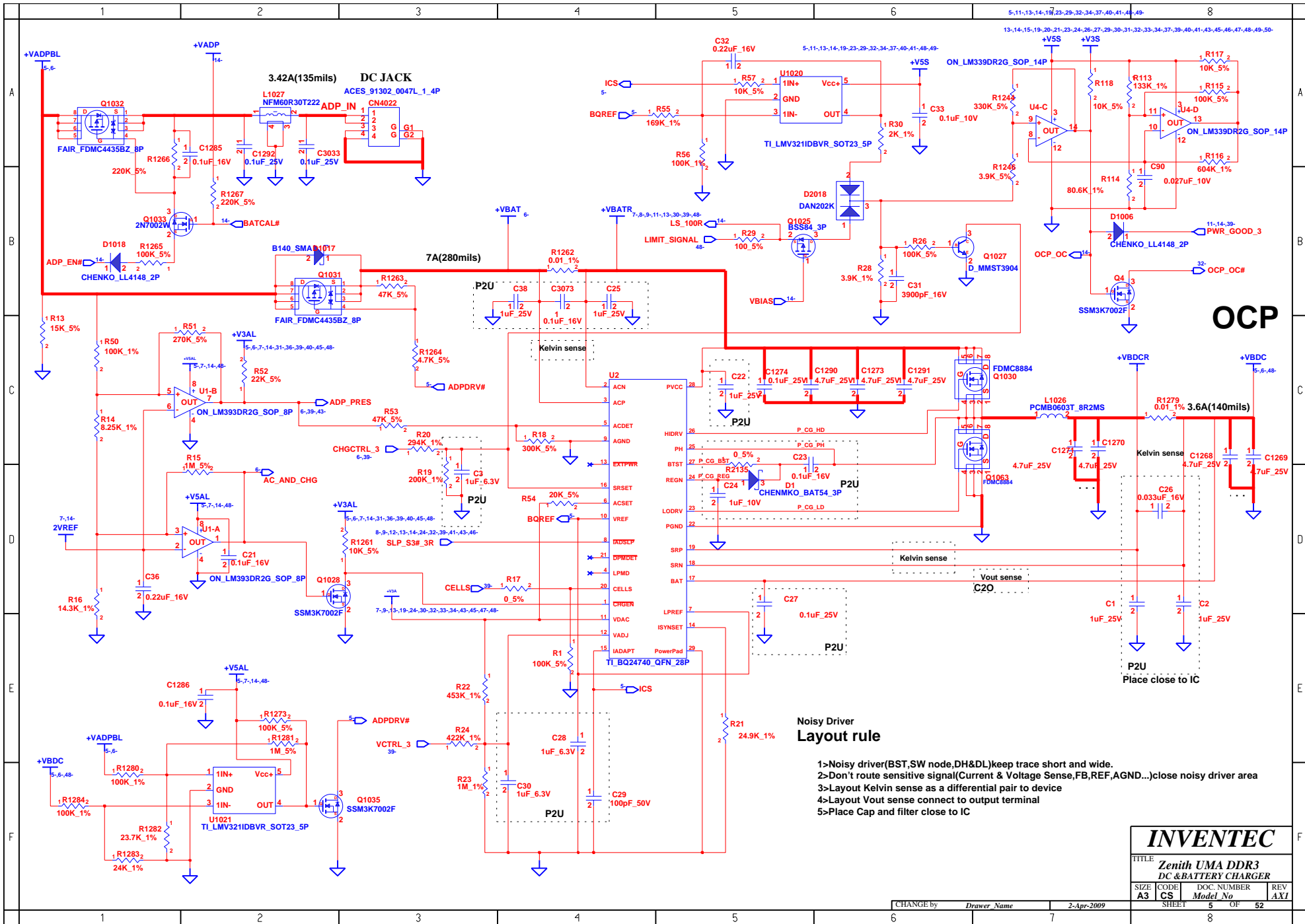
SHEET 2 OF 52



<b>INVENTEC</b>			
TITLE Zenith UMA DDR3			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Drawer Name		2-Apr-2009	SHEET 3 OF 52



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	SHEET 4 OF 52

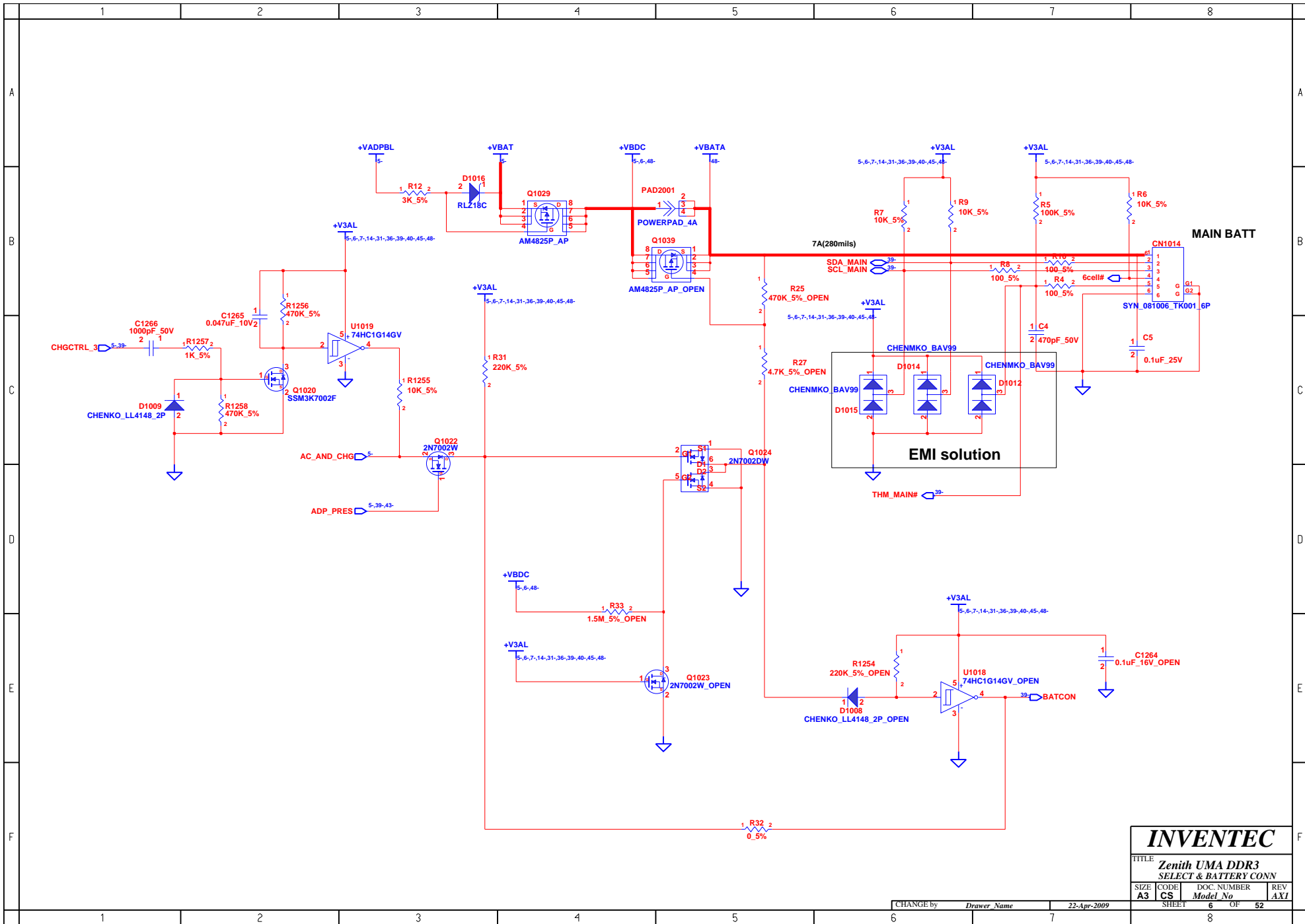


**OCP**

**Noisy Driver  
Layout rule**

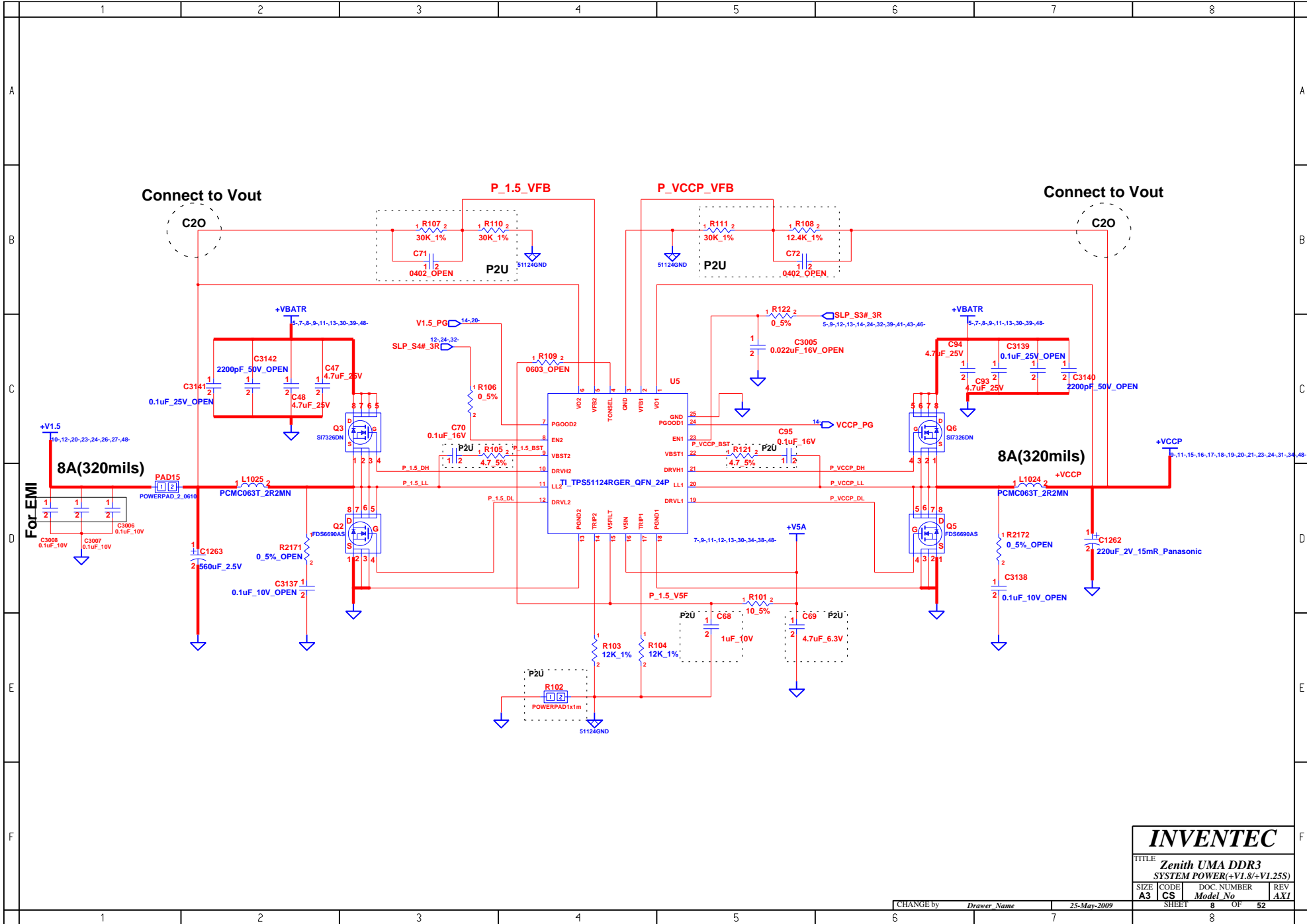
- 1>Noisy driver(BST,SW node,DH&DL)keep trace short and wide.
- 2>Don't route sensitive signal(Current & Voltage Sense,FB,REF,AGND...)close noisy driver area
- 3>Layout Kelvin sense as a differential pair to device
- 4>Layout Vout sense connect to output terminal
- 5>Place Cap and filter close to IC

<b>INVENTEC</b>				
TITLE <b>Zenith UMA DDR3 DC &amp; BATTERY CHARGER</b>				
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>AX1</b>	
CHANGE by <i>Drawer Name</i>		2-Apr-2009		SHEET <b>5</b> OF <b>52</b>



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 SELECT &amp; BATTERY CONN</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		22-Apr-2009	
SHEET 6		OF 52	





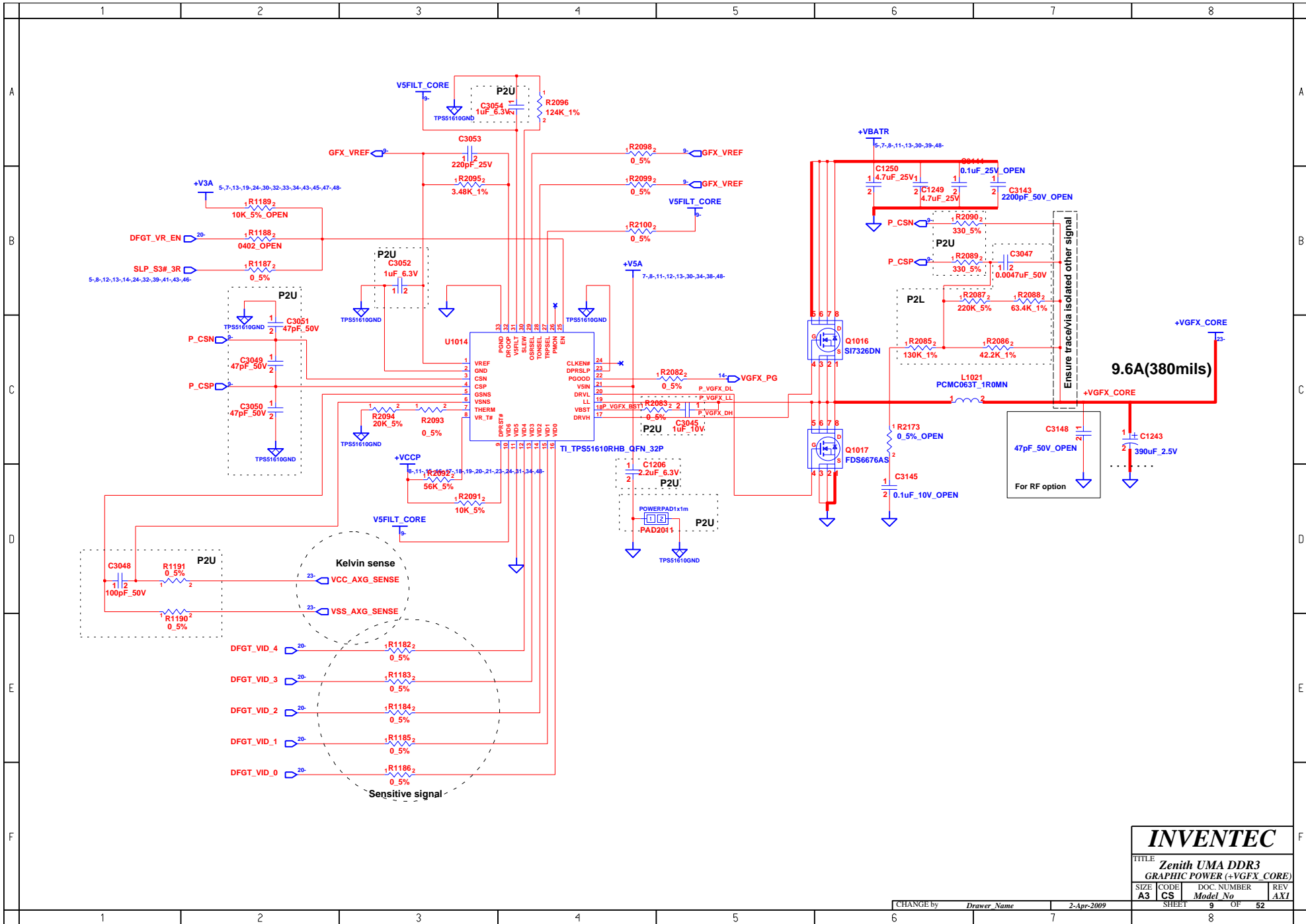
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TITLE  
**Zenith UMA DDR3**  
 SYSTEM POWER(+V1.8/+V1.25S)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by	Drawer Name	25-May-2009	SHEET	8	OF	52
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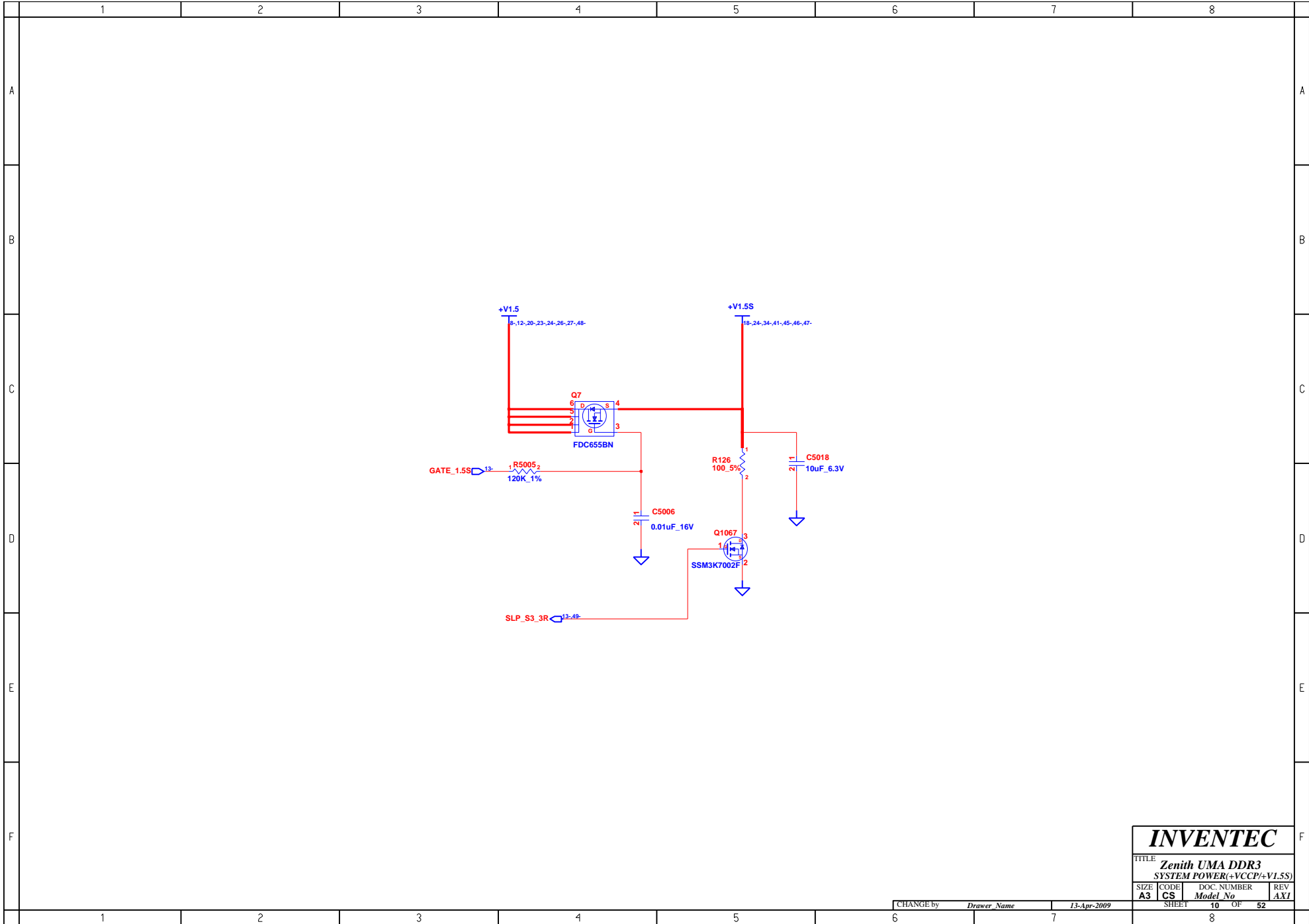


# INVENTEC

TITLE  
**Zenith UMA DDR3  
 GRAPHIC POWER (+VGFX\_CORE)**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AXI</b>
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CHANGE by *Drawer Name* 2-Apr-2009 SHEET 9 OF 52



**INVENTEC**

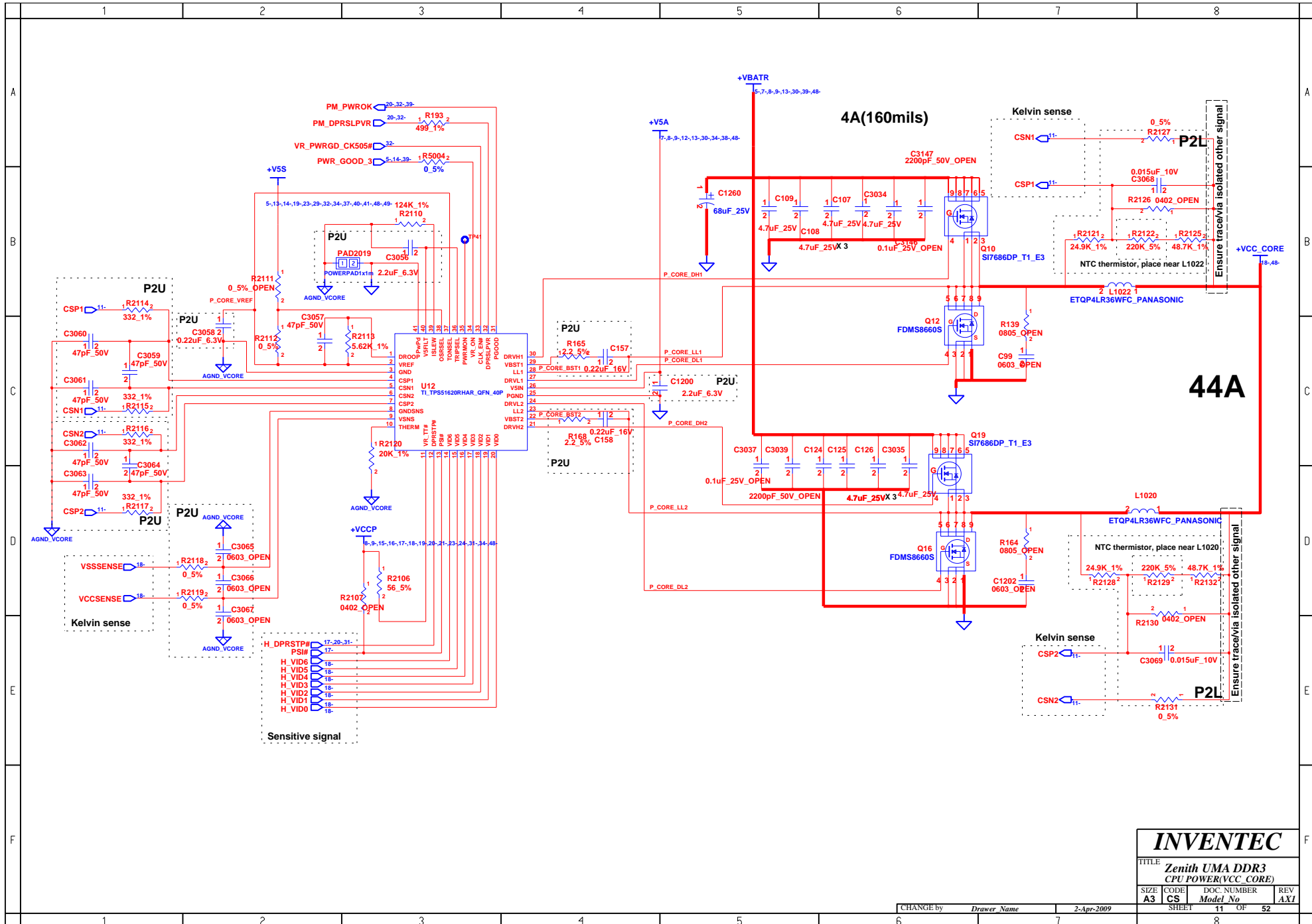
TITLE **Zenith UMA DDR3  
SYSTEM POWER(+VCCP/+V1.5S)**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No.</i>	REV <b>AXI</b>
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CHANGE by *Drawer Name* 13-Apr-2009

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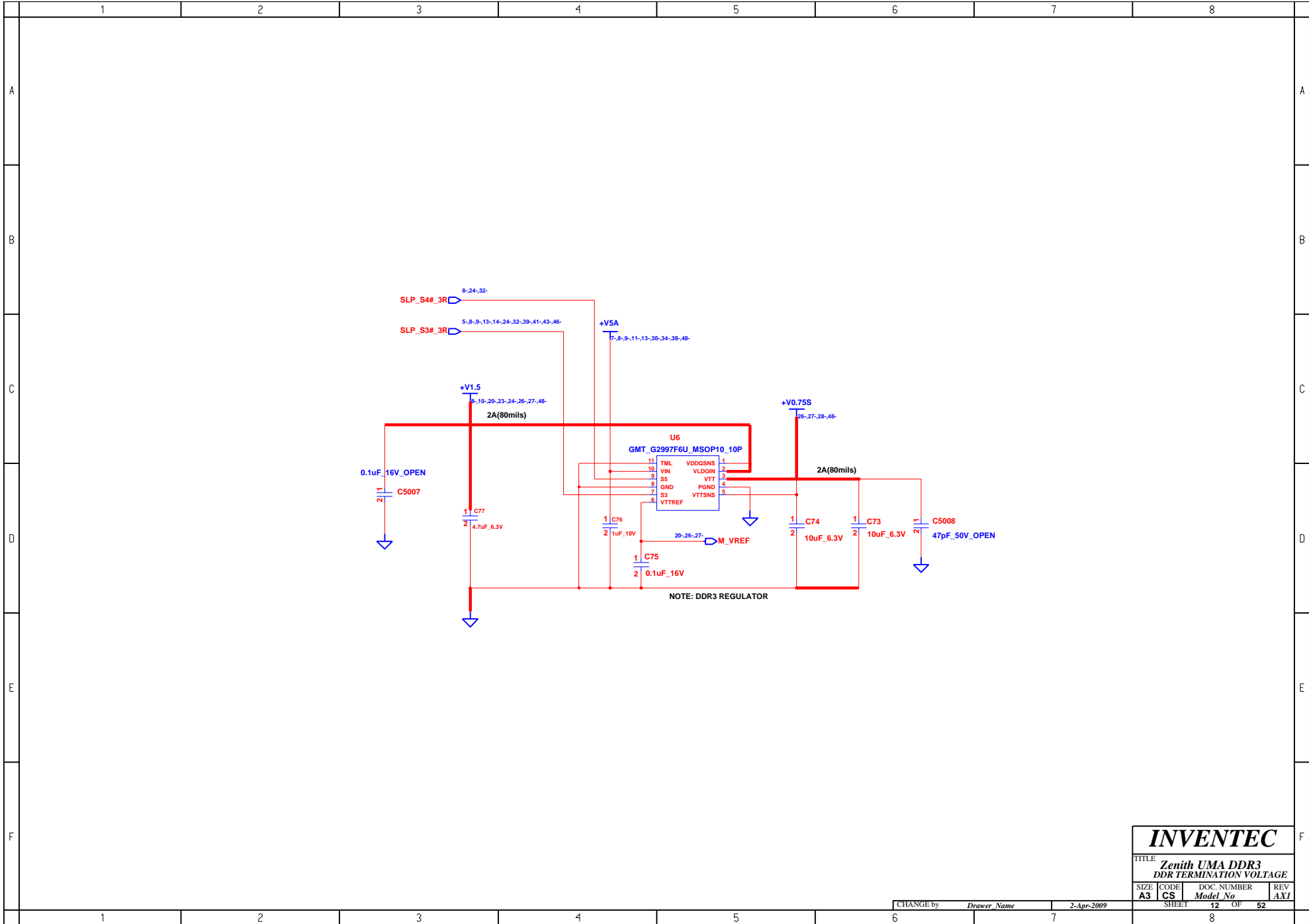
	1	2	3	4	5	6	7	8	
A									
B									
C									
D									
E									
F									
	1	2	3	4	5	6	7	8	



**INVENTEC**

TITLE  
Zenith UMA DDR3  
CPU POWER(VCC\_CORE)

SIZE A3	CODE CS	DOC NUMBER Doc No	REV AX1
CHANGE by Drawer Name		2-Apr-2009	
SHEET 11		OF 52	



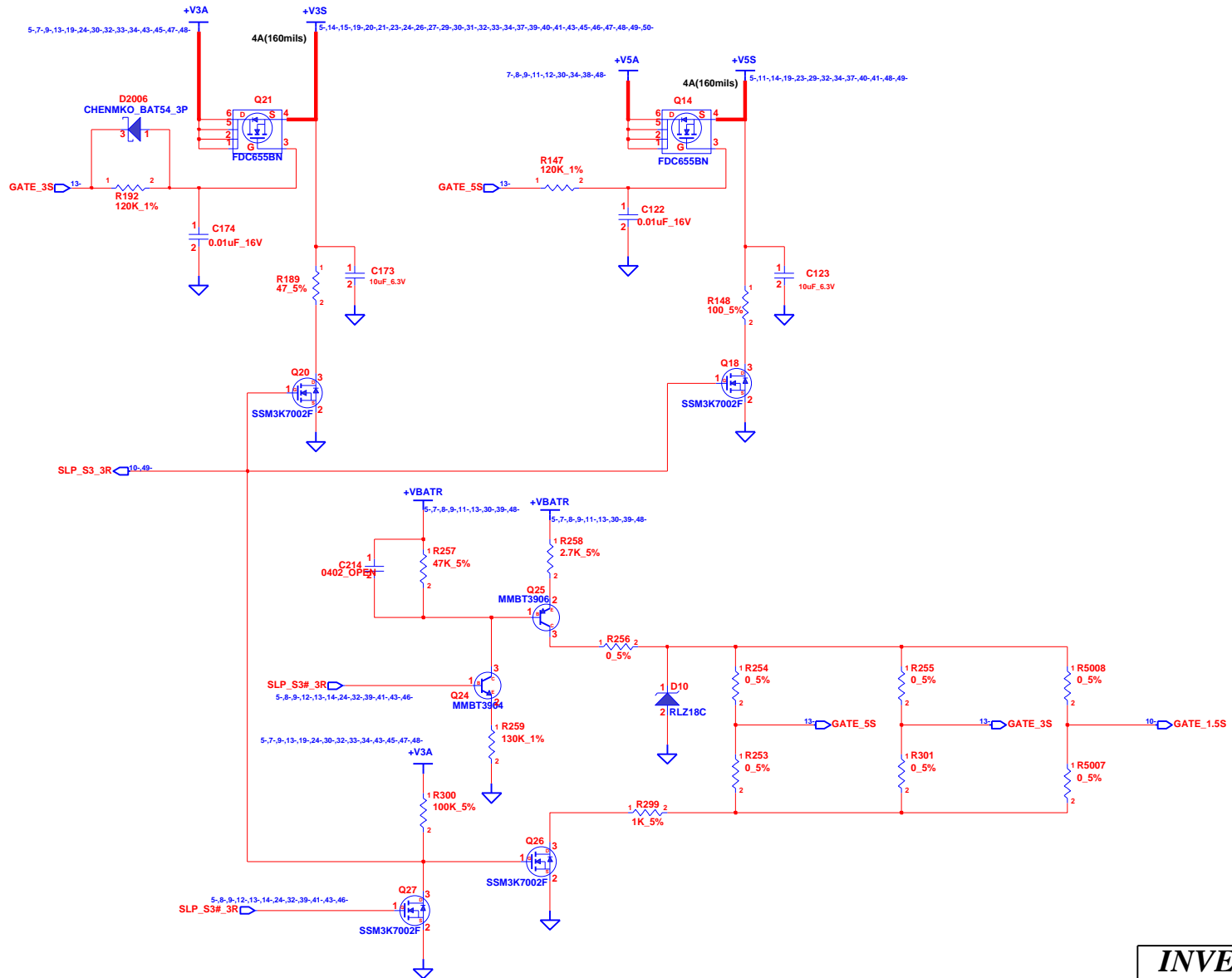
**INVENTEC**

TITLE **Zenith UMA DDR3  
DDR TERMINATION VOLTAGE**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
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CHANGE by *Drawer Name* 2-Apr-2009

SHEET 12 OF 52

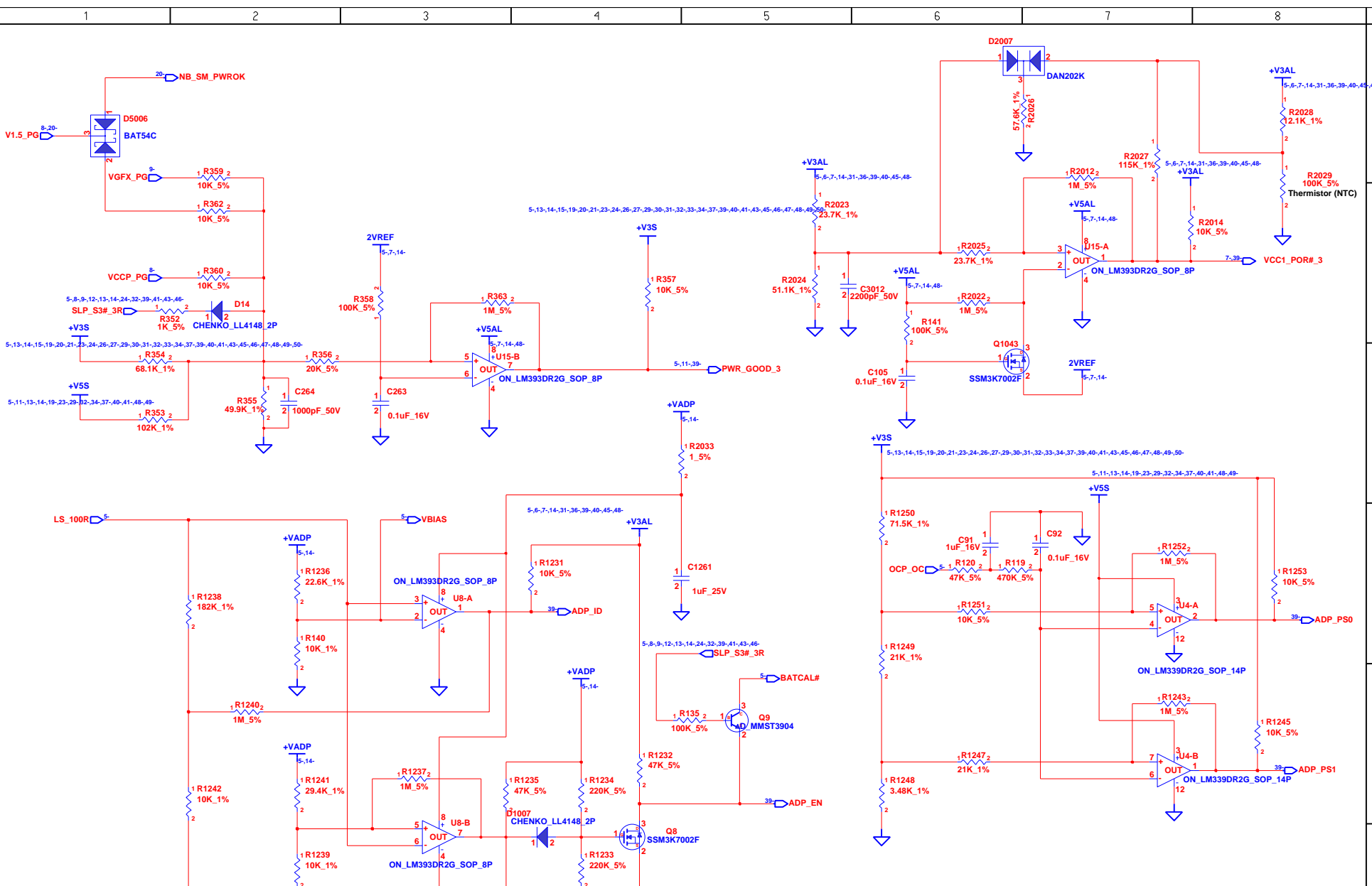


# INVENTEC

TITLE			
Zenith UMA DDR3 POWER(SLEEP)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI
CHANGE by		2-Apr-2009	SHEET 13 OF 52
Drawer Name			

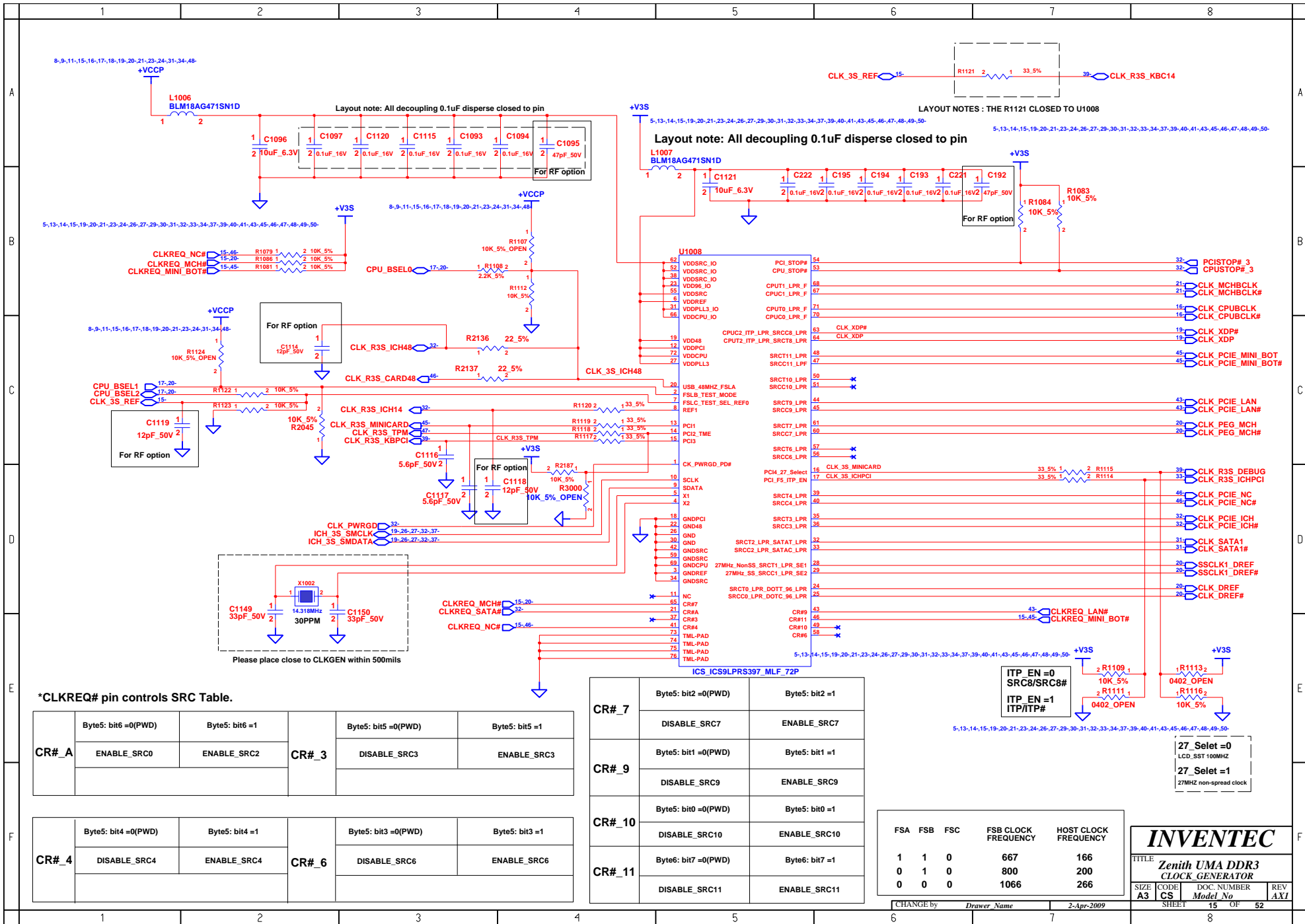
CHANGE by *Drawer Name* 2-Apr-2009

SHEET 13 OF 52



**INVENTEC**

TITLE			
Zenith UMA DDR3 POWER(SEQUENCE)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	Model No	AXI



\*CLKREQ# pin controls SRC Table.

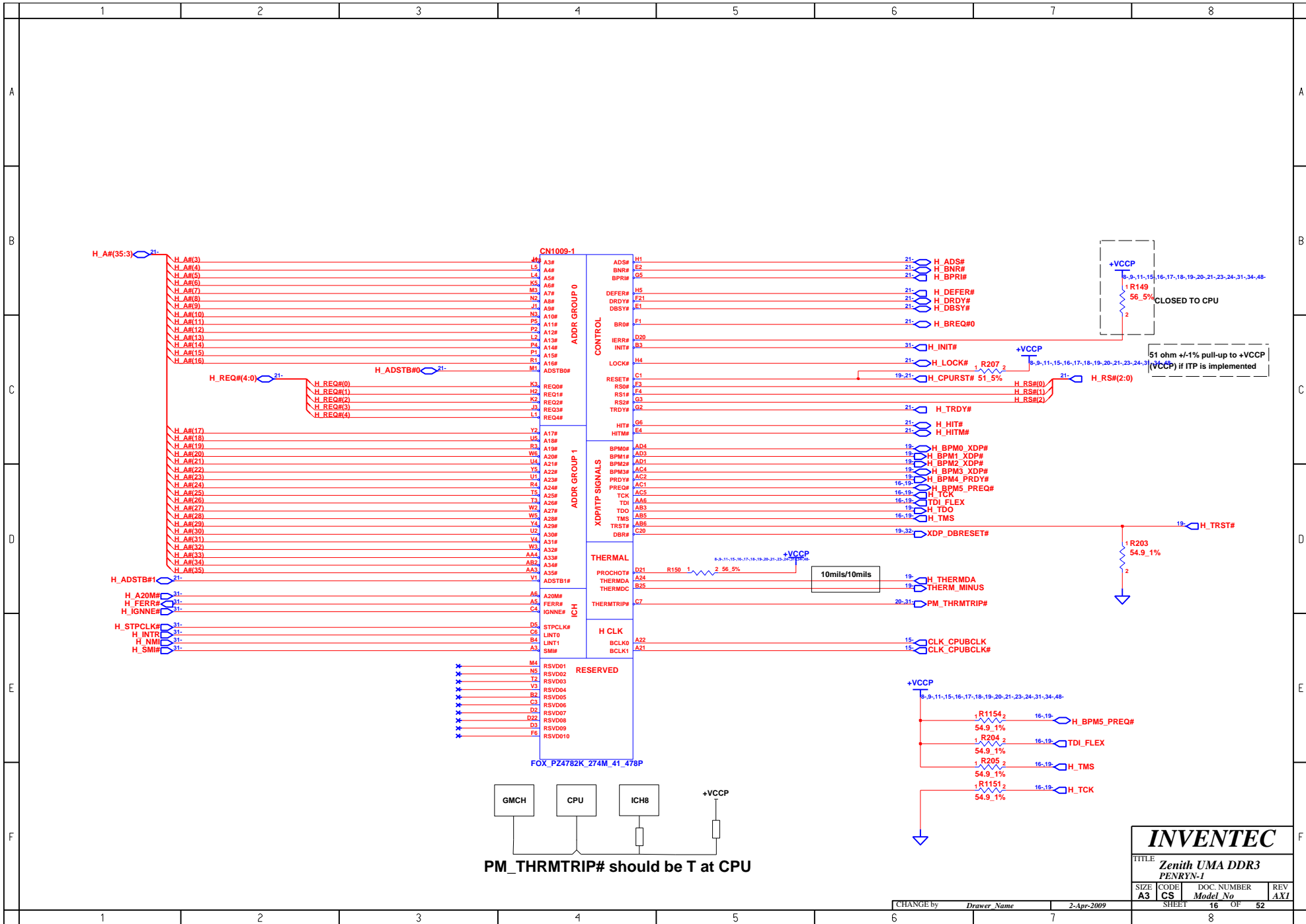
CR#_A	Byte5: bit6 =0(PWD)	Byte5: bit6 =1	CR#_3	Byte5: bit5 =0(PWD)	Byte5: bit5 =1
	ENABLE_SRC0	ENABLE_SRC2		DISABLE_SRC3	ENABLE_SRC3

CR#_4	Byte5: bit4 =0(PWD)	Byte5: bit4 =1	CR#_6	Byte5: bit3 =0(PWD)	Byte5: bit3 =1
	DISABLE_SRC4	ENABLE_SRC4		DISABLE_SRC6	ENABLE_SRC6

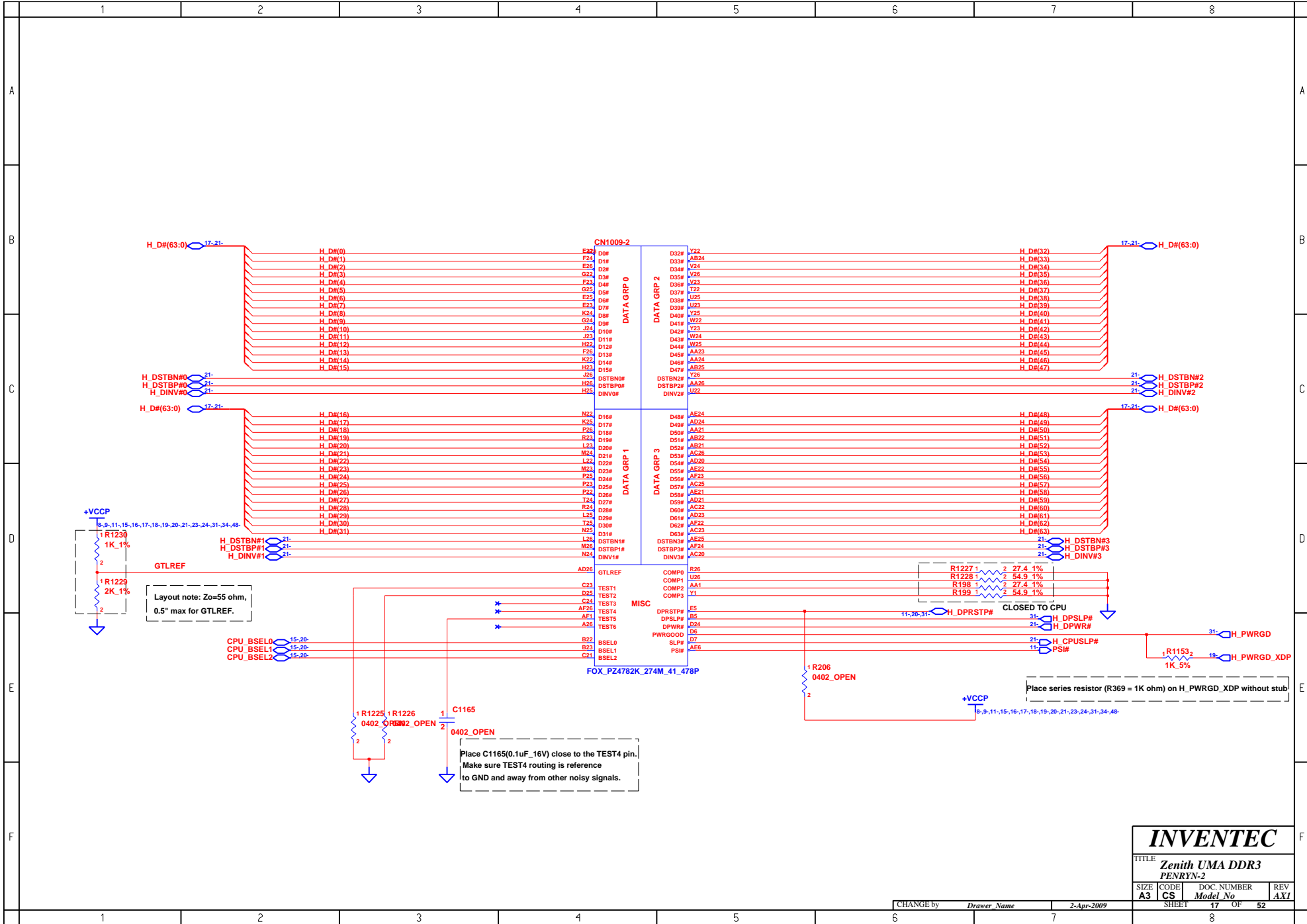
CR#_7	Byte5: bit2 =0(PWD)	Byte5: bit2 =1
	DISABLE_SRC7	ENABLE_SRC7
CR#_9	Byte5: bit1 =0(PWD)	Byte5: bit1 =1
	DISABLE_SRC9	ENABLE_SRC9
CR#_10	Byte5: bit0 =0(PWD)	Byte5: bit0 =1
	DISABLE_SRC10	ENABLE_SRC10
CR#_11	Byte6: bit7 =0(PWD)	Byte6: bit7 =1
	DISABLE_SRC11	ENABLE_SRC11

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1066	266

<b>INVENTEC</b>			
TITLE Zenith UMA DDR3 CLOCK GENERATOR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	Doc No	AXI

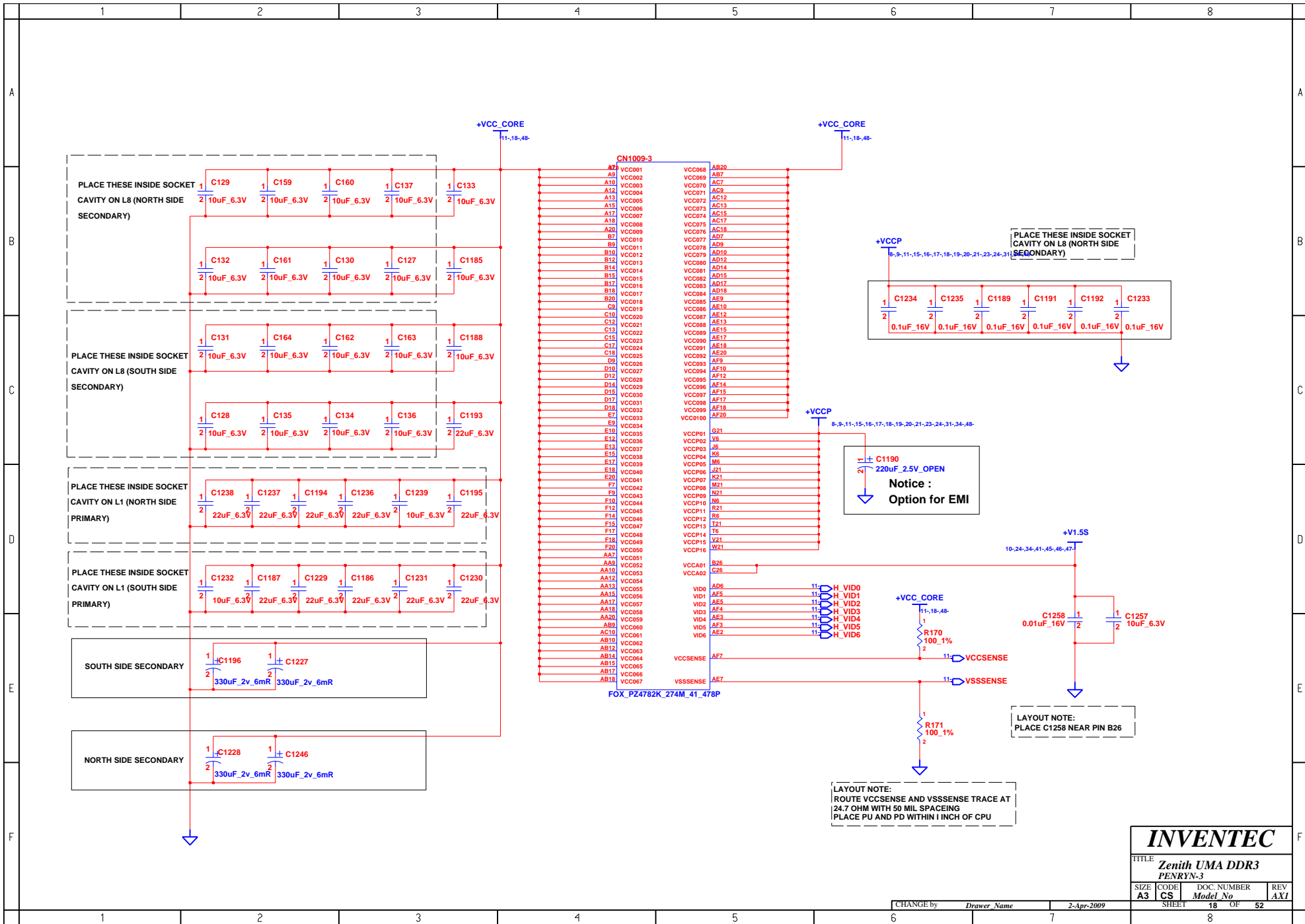






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 TITLE  
 Zenith UMA DDR3  
 PENRYN-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

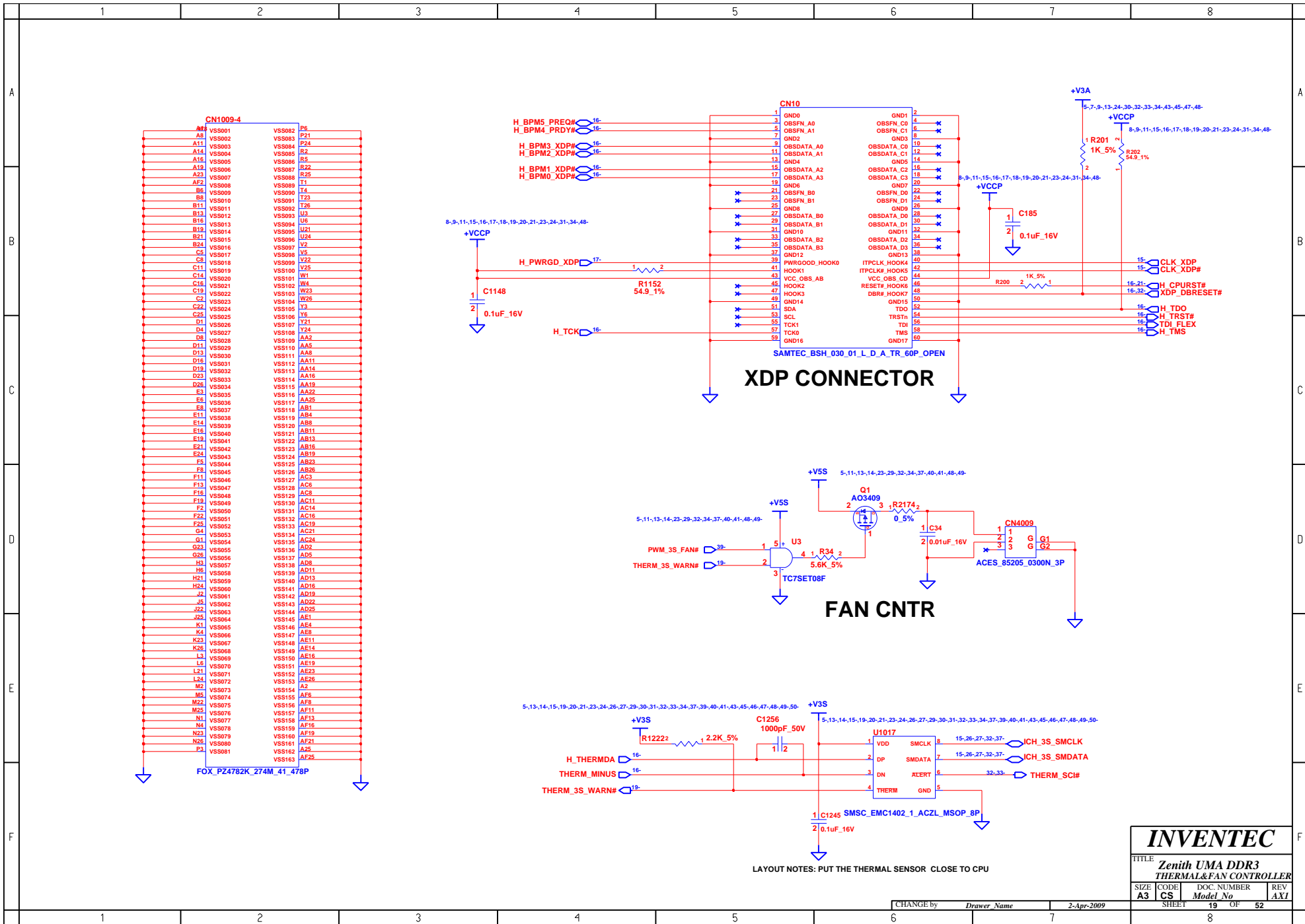


# INVENTEC

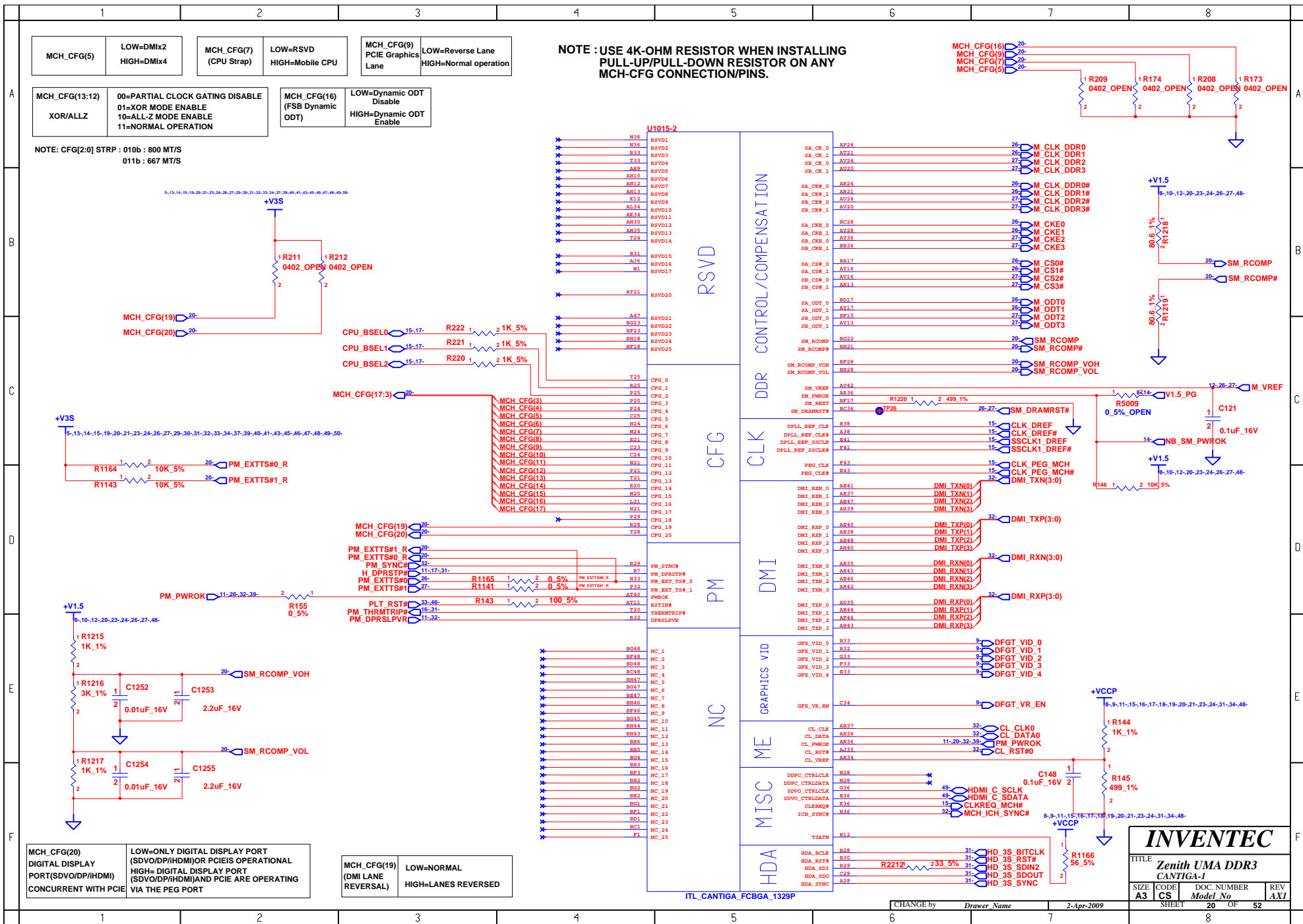
TITLE  
**Zenith UMA DDR3  
 PENRYN-3**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Drawer Name* 2-Apr-2009 SHEET 18 OF 52



<b>INVENTEC</b>			
TITLE: <b>Zenith UMA DDR3 THERMAL&amp;FAN CONTROLLER</b>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI
CHANGE by: <i>Drawer Name</i>			2-Apr-2009
SHEET 19			OF 52



**NOTE : USE 4K-OHM RESISTOR WHEN INSTALLING PULL-UP/PULL-DOWN RESISTOR ON ANY MCH-CFG CONNECTION/PINS.**

MCH_CFG(5)	LOW=DMiX2 HIGH=DMiX4	MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU	MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation
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MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION	MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable
----------------------------	--	----------------------------------	--

NOTE: CFG[2:0] STRP : 010b : 800 MT/S  
011b : 667 MT/S

MCH_CFG(19)	LOW=ONLY DIGITAL DISPLAY PORT (SDVO/DP/HDMI) OR PCIE IS OPERATIONAL HIGH= DIGITAL DISPLAY PORT (SDVO/DP/HDMI) AND PCIE ARE OPERATING CONCURRENT WITH PCIE VIA THE PEG PORT
-------------	---

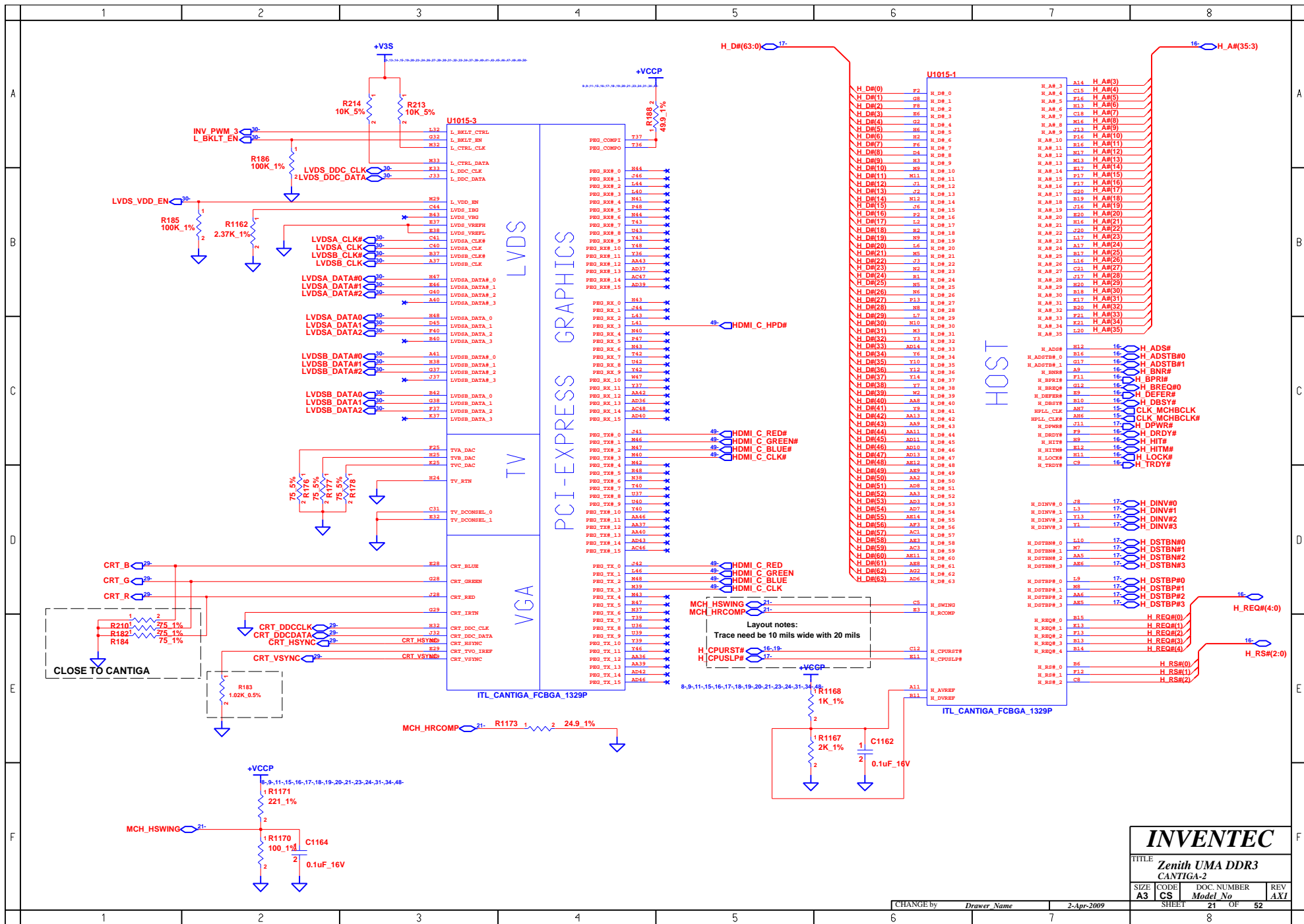
MCH_CFG(19) REVERSAL	LOW=NORMAL HIGH=LANES REVERSED
-------------------------	-----------------------------------

**INVENTEC**

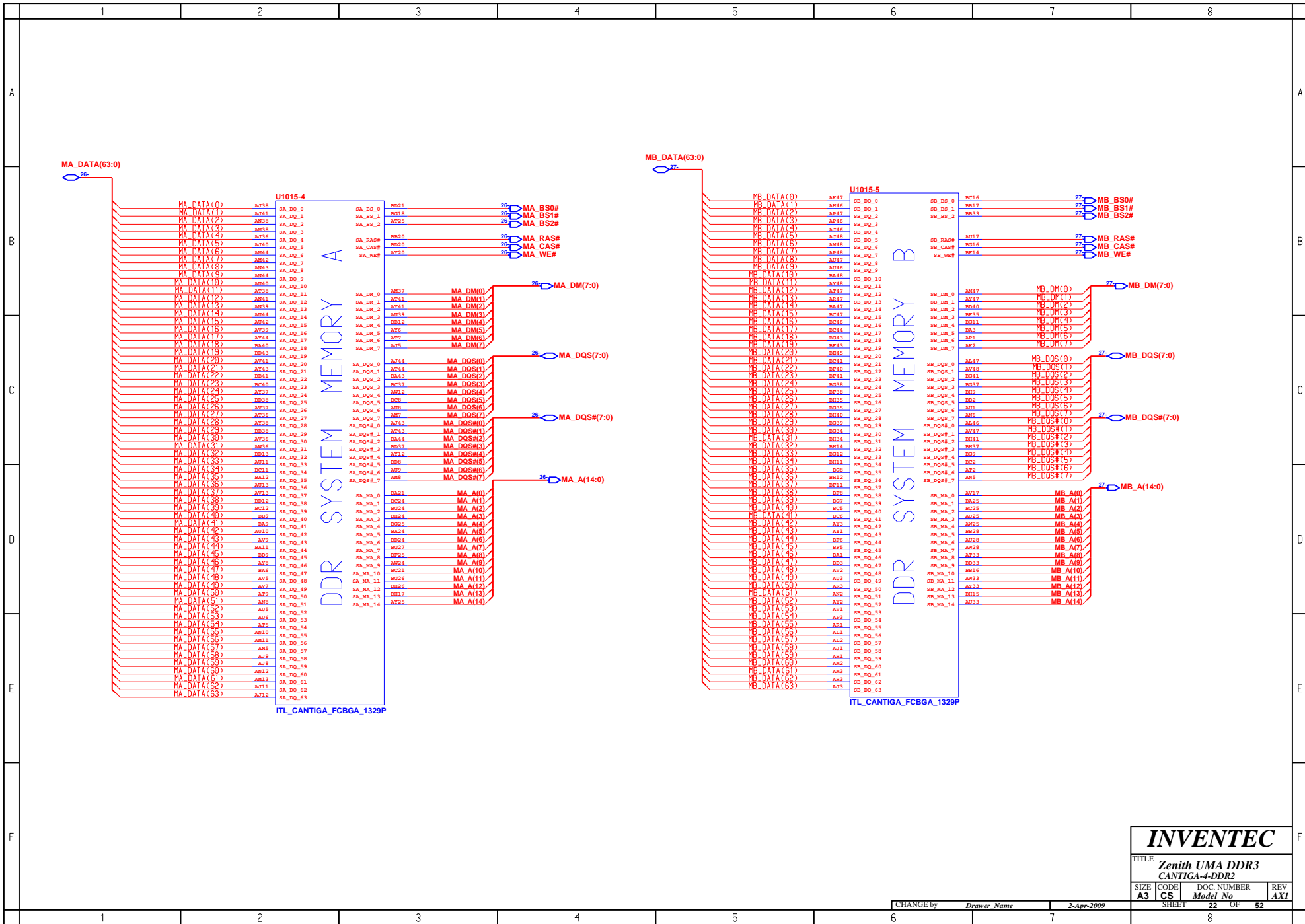
TITLE: **Zenith UMA DDR3 CANTIGA-1**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1

SHEET 20 OF 52



<b>INVENTEC</b>			
TITLE Zenith UMA DDR3 CANTIGA-2			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Drawer Name		2-Apr-2009	
SHEET 21		OF 52	

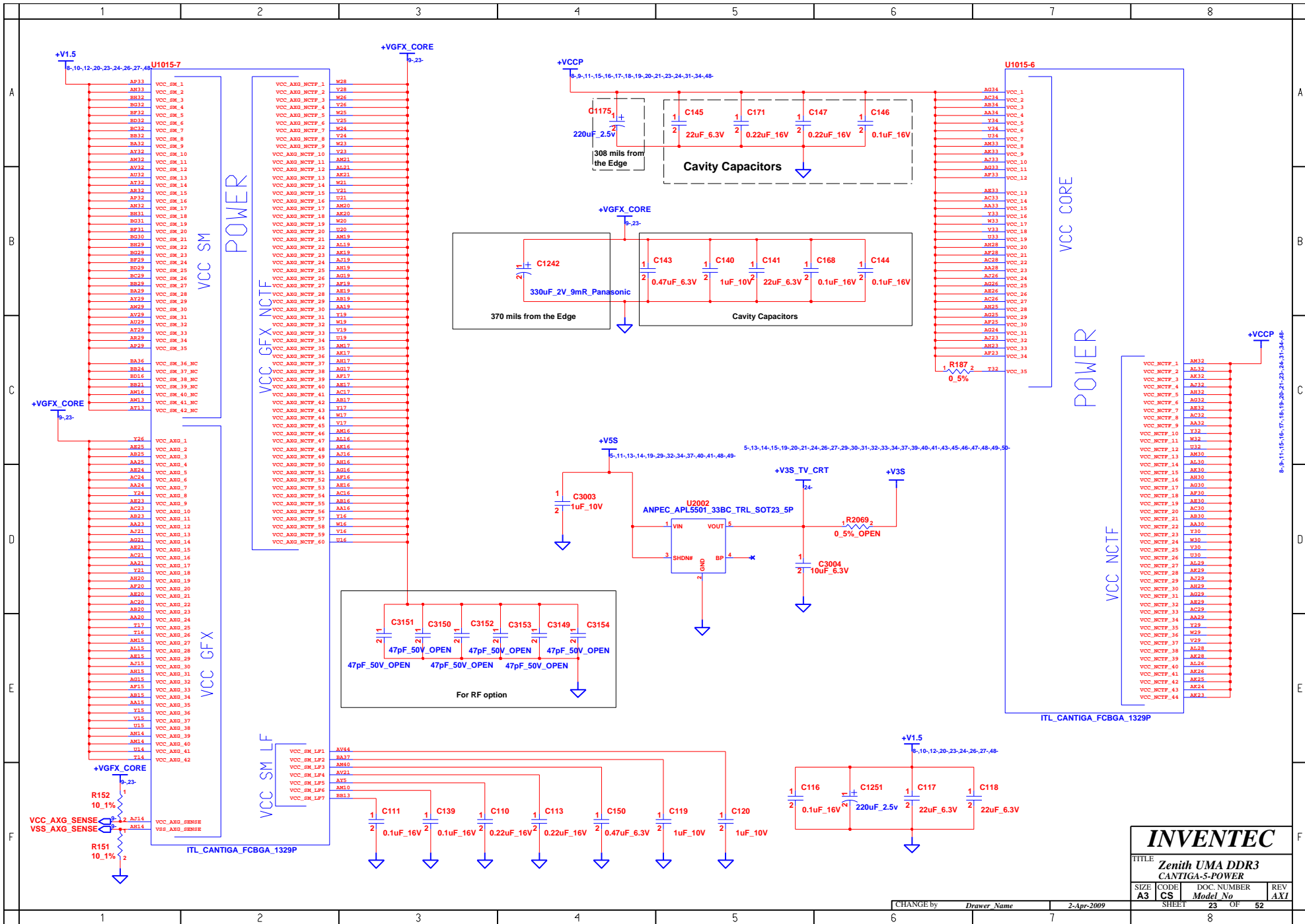


**INVENTEC**

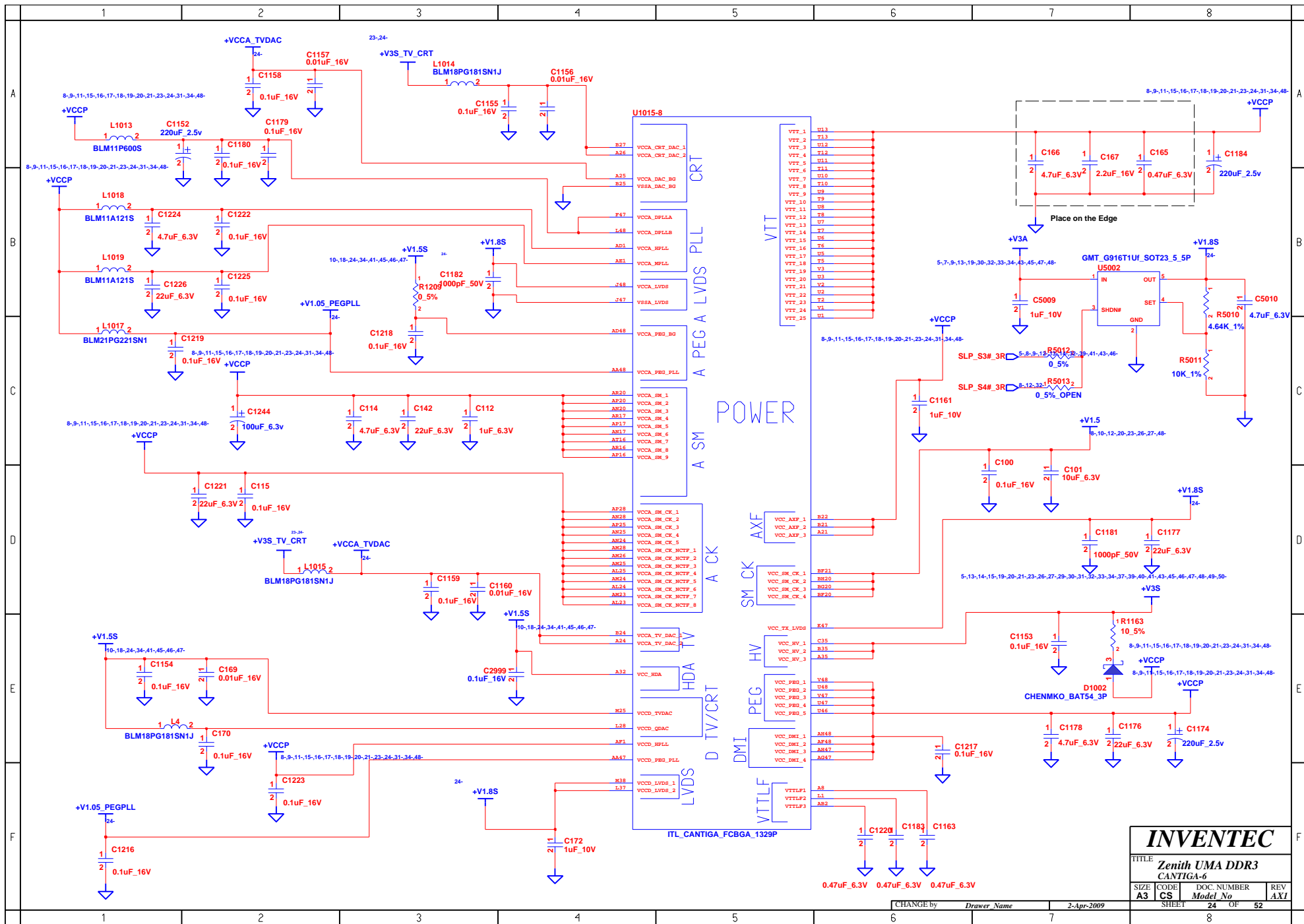
TITLE  
Zenith UMA DDR3  
CANTIGA-4-DDR2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1

CHANGE by *Drawer Name* 2-Apr-2009 SHEET 22 OF 52



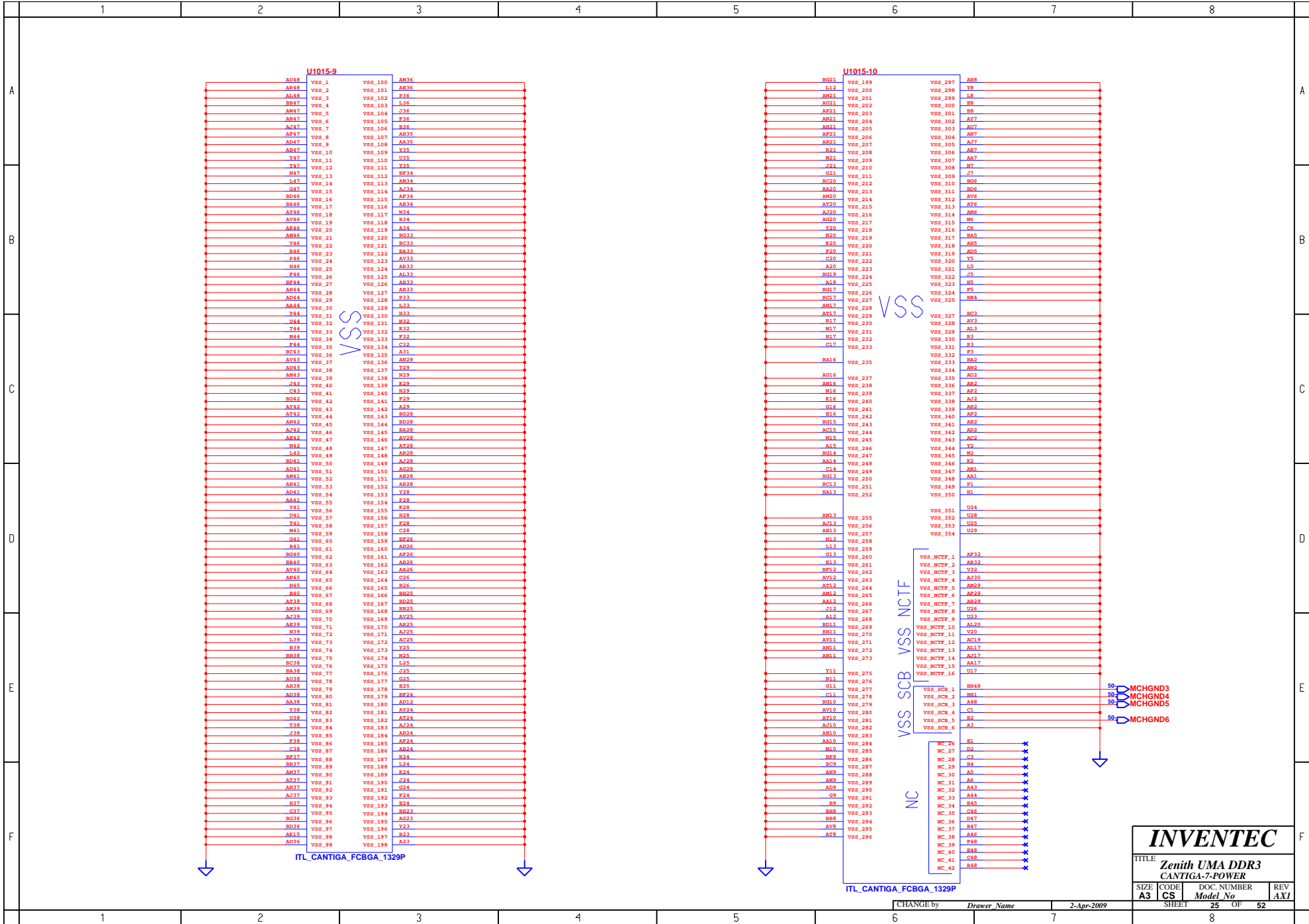
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TITLE <b>Zenith UMA DDR3 CANTIGA-5-POWER</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	
SHEET <b>23</b>		OF <b>52</b>	



POWER

<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 CANTIGA-6</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	
SHEET <b>24</b>		OF <b>52</b>	



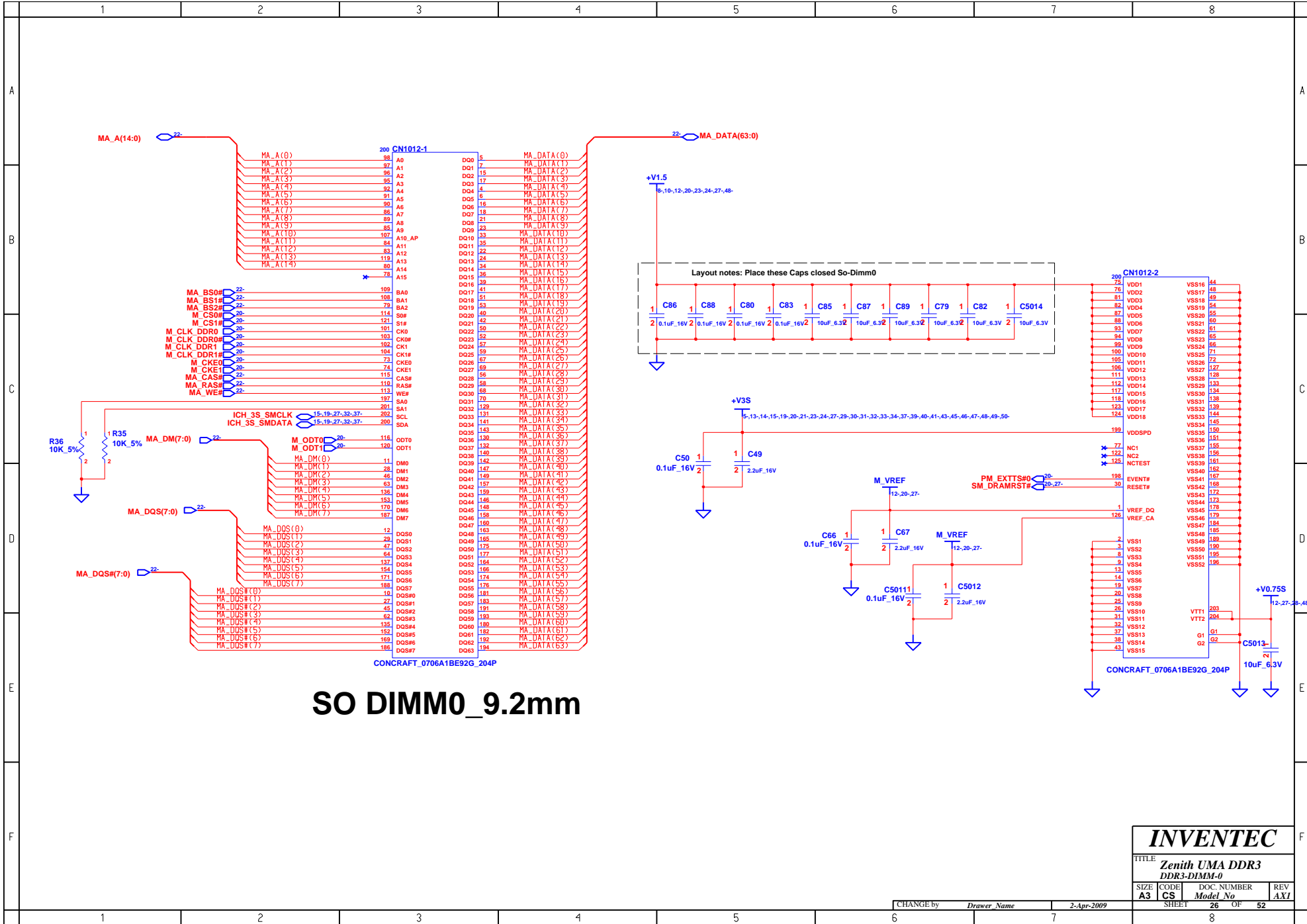


**INVENTEC**

TITLE  
Zenith UMA DDR3  
CANTIGA-7-POWER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1

SHEET 25 OF 52



# SO DIMM\_9.2mm

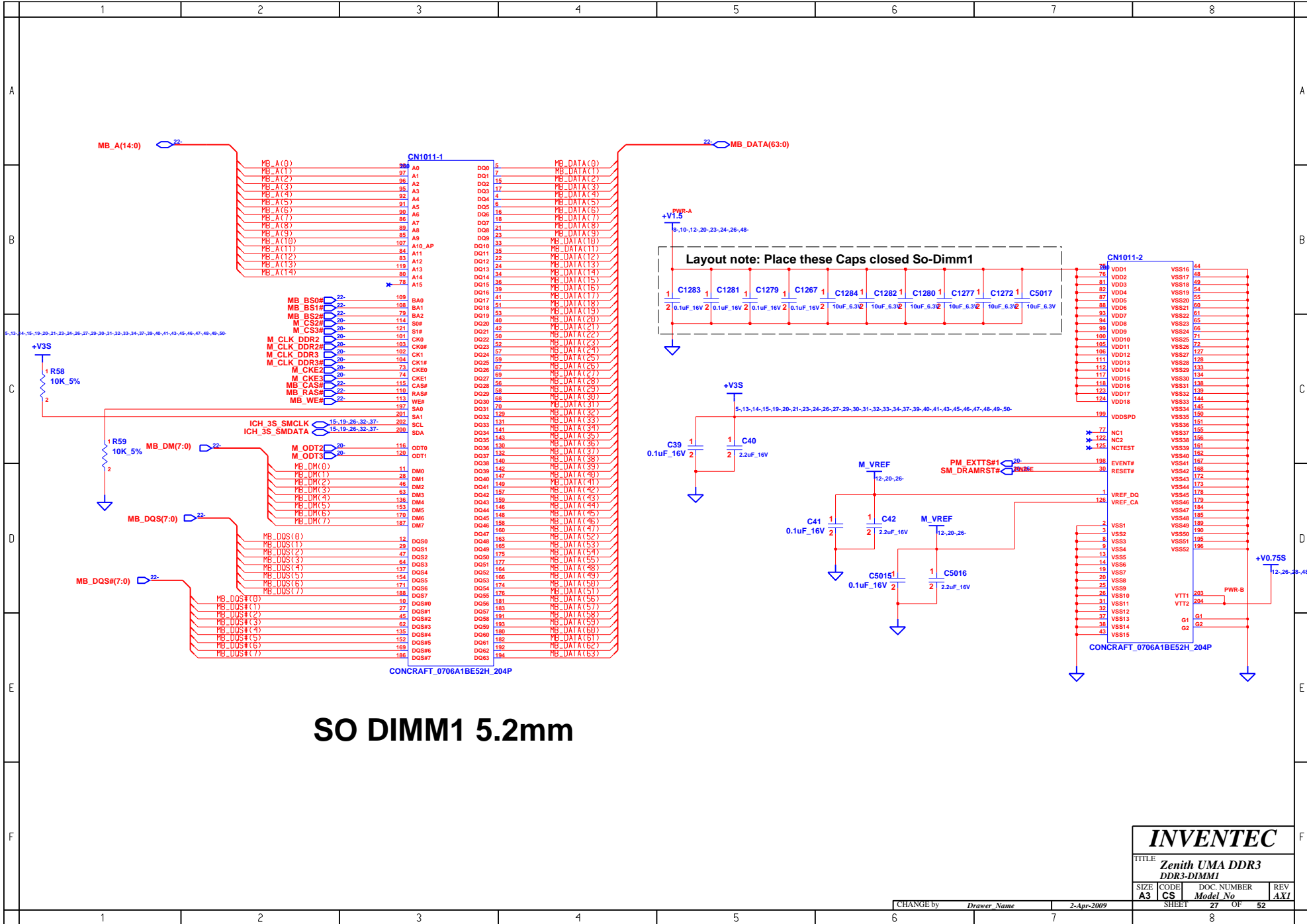
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TITLE  
**Zenith UMA DDR3  
 DDR3-DIMM-0**

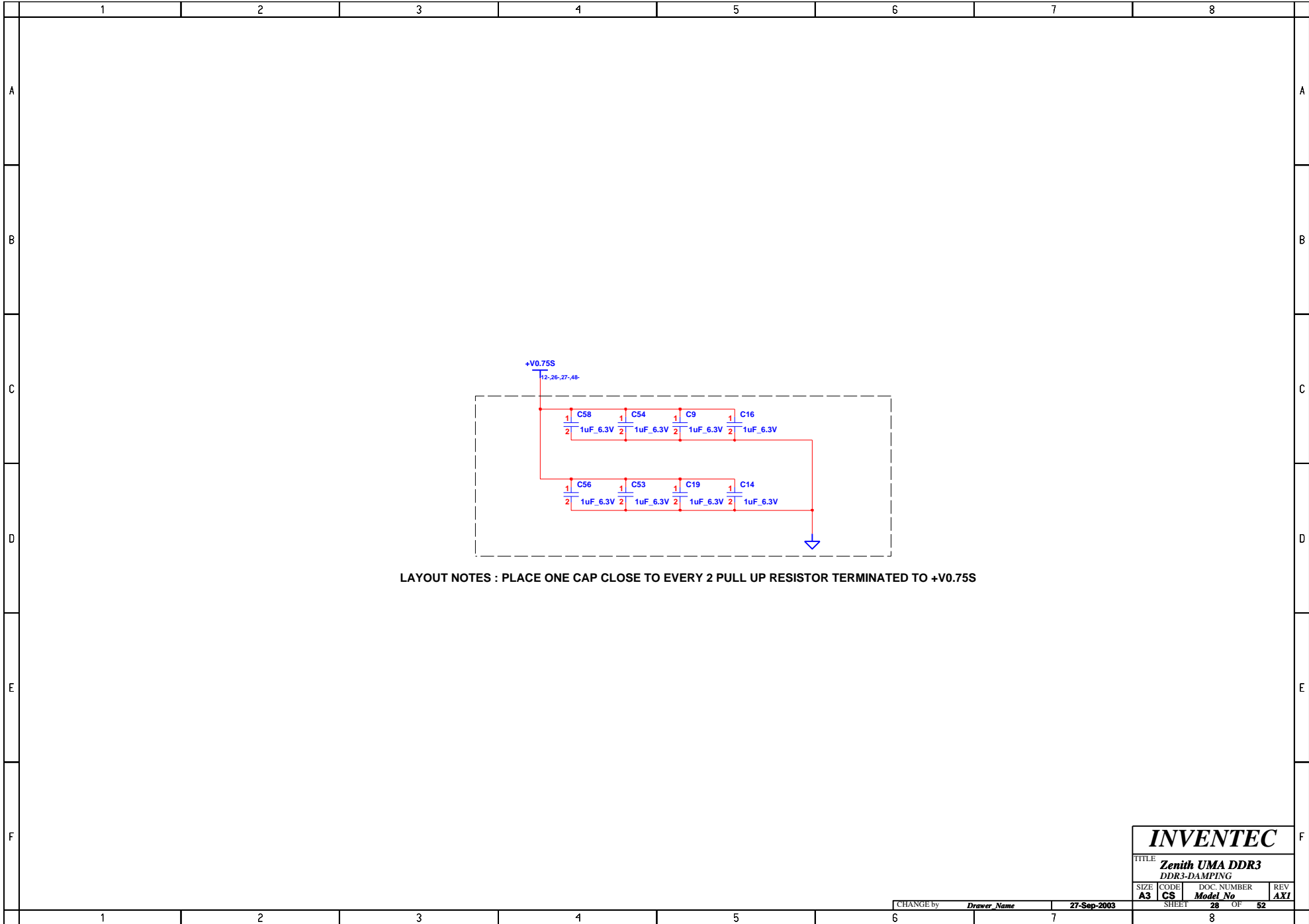
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A3	CS	26	AX1

CHANGE by *Drawer Name* 2-Apr-2009

SHEET 26 OF 52



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 DDR3-DIMM1</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <i>AXI</i>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	
SHEET 27		OF 52	



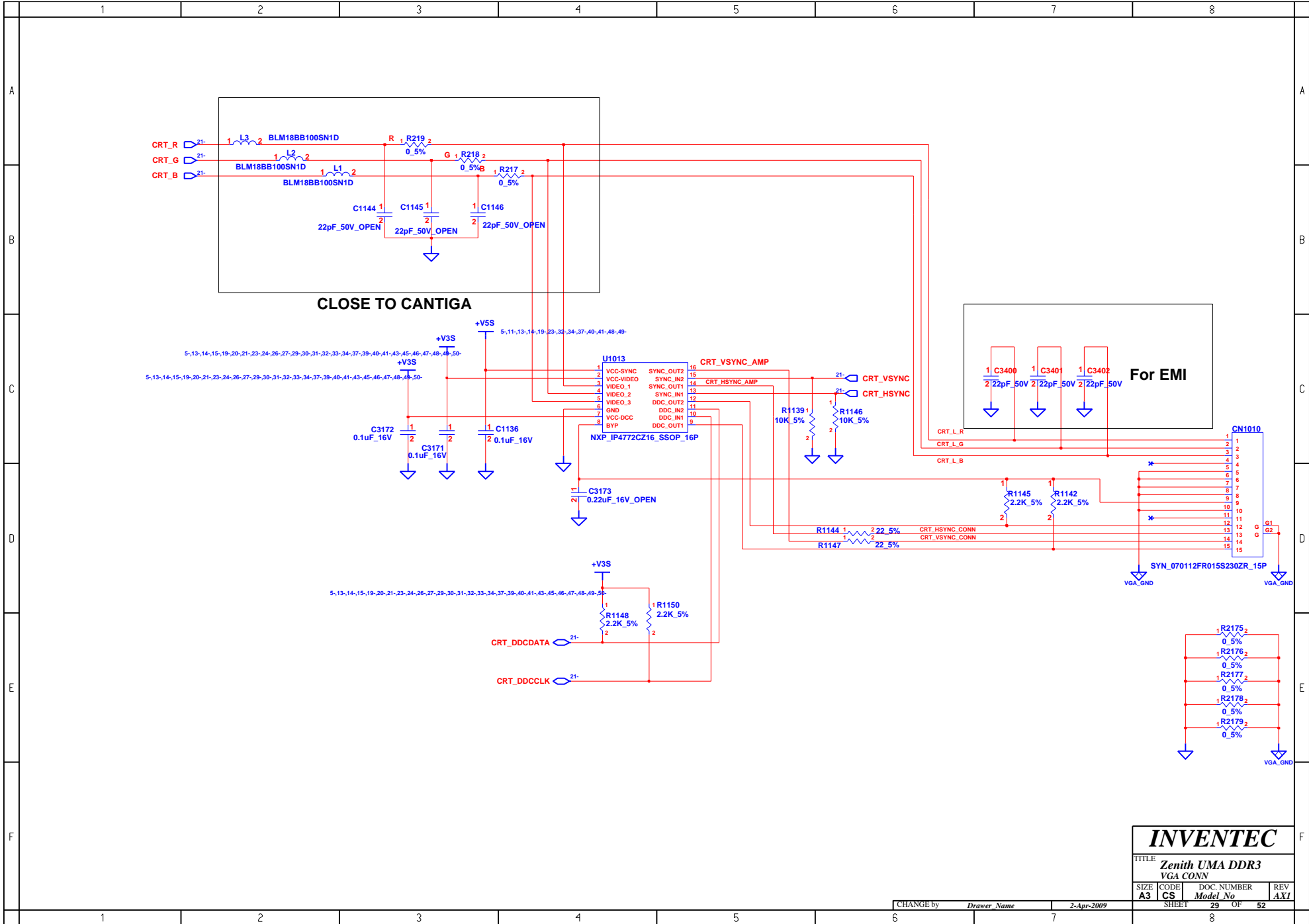
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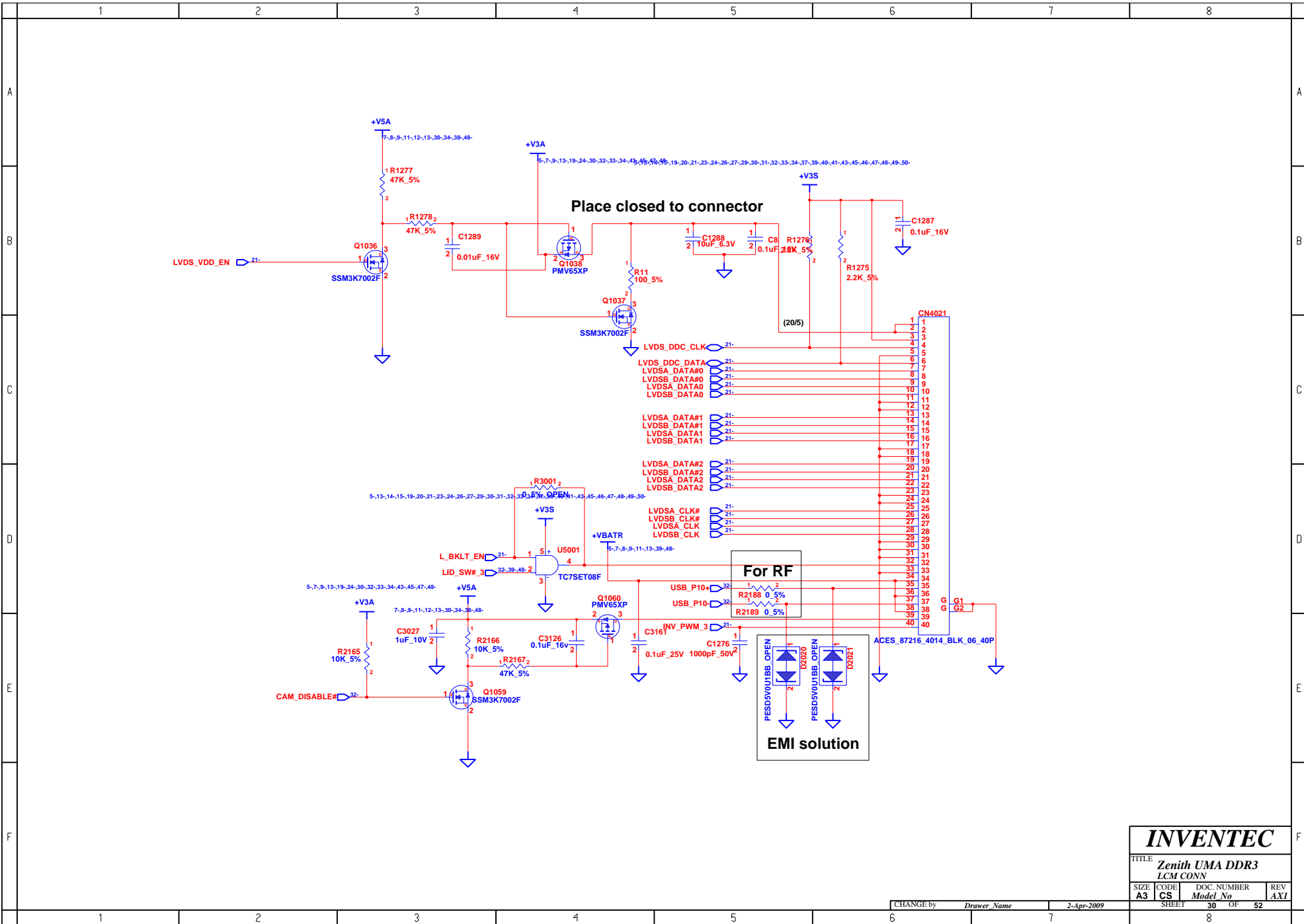
TITLE  
**Zenith UMA DDR3**  
DDR3-DAMPING

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>AXI</b>
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CHANGE by *Drawer Name* 27-Sep-2003

SHEET 28 OF 52



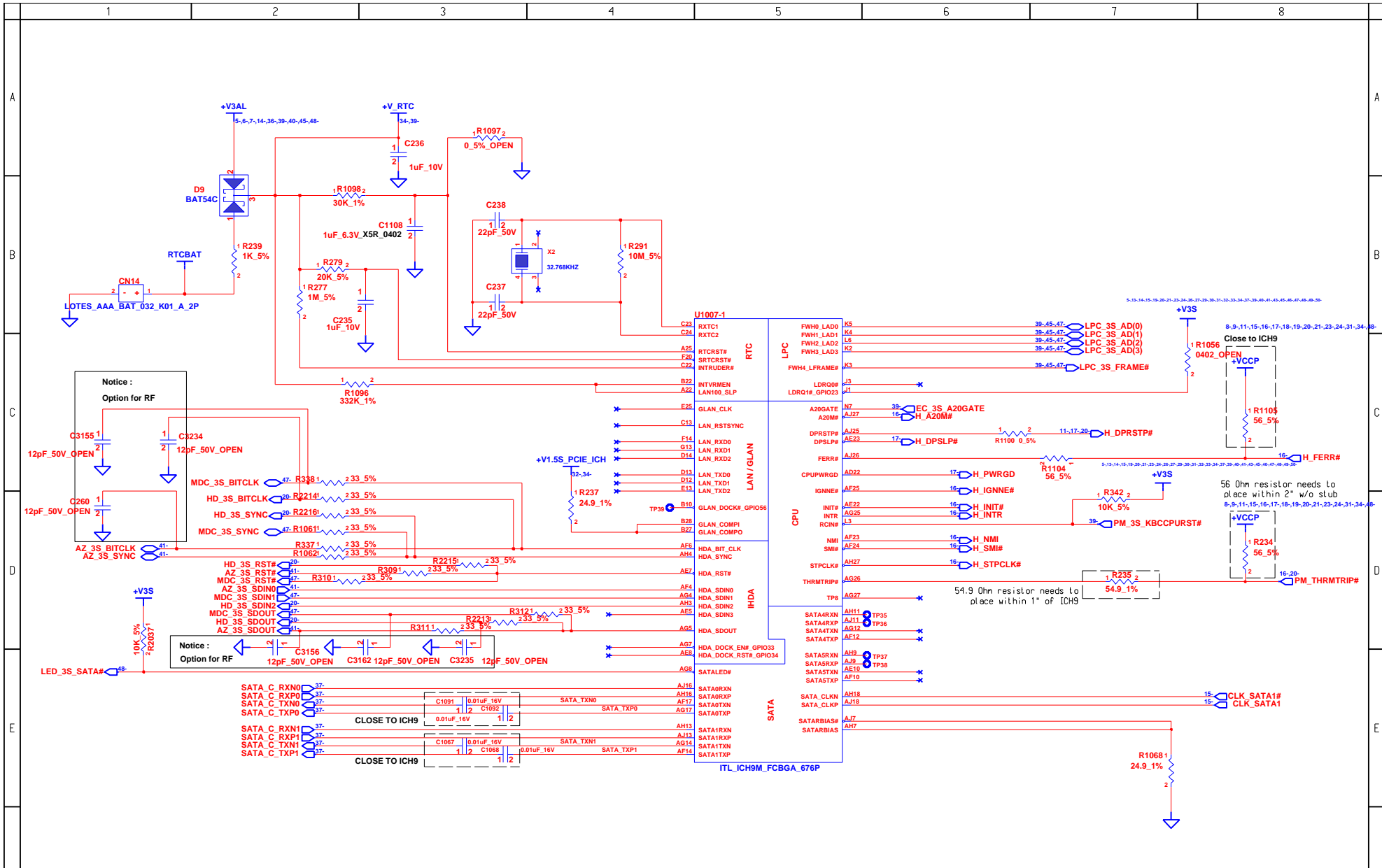


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TITLE  
**Zenith UMA DDR3**  
**LCM CONN**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

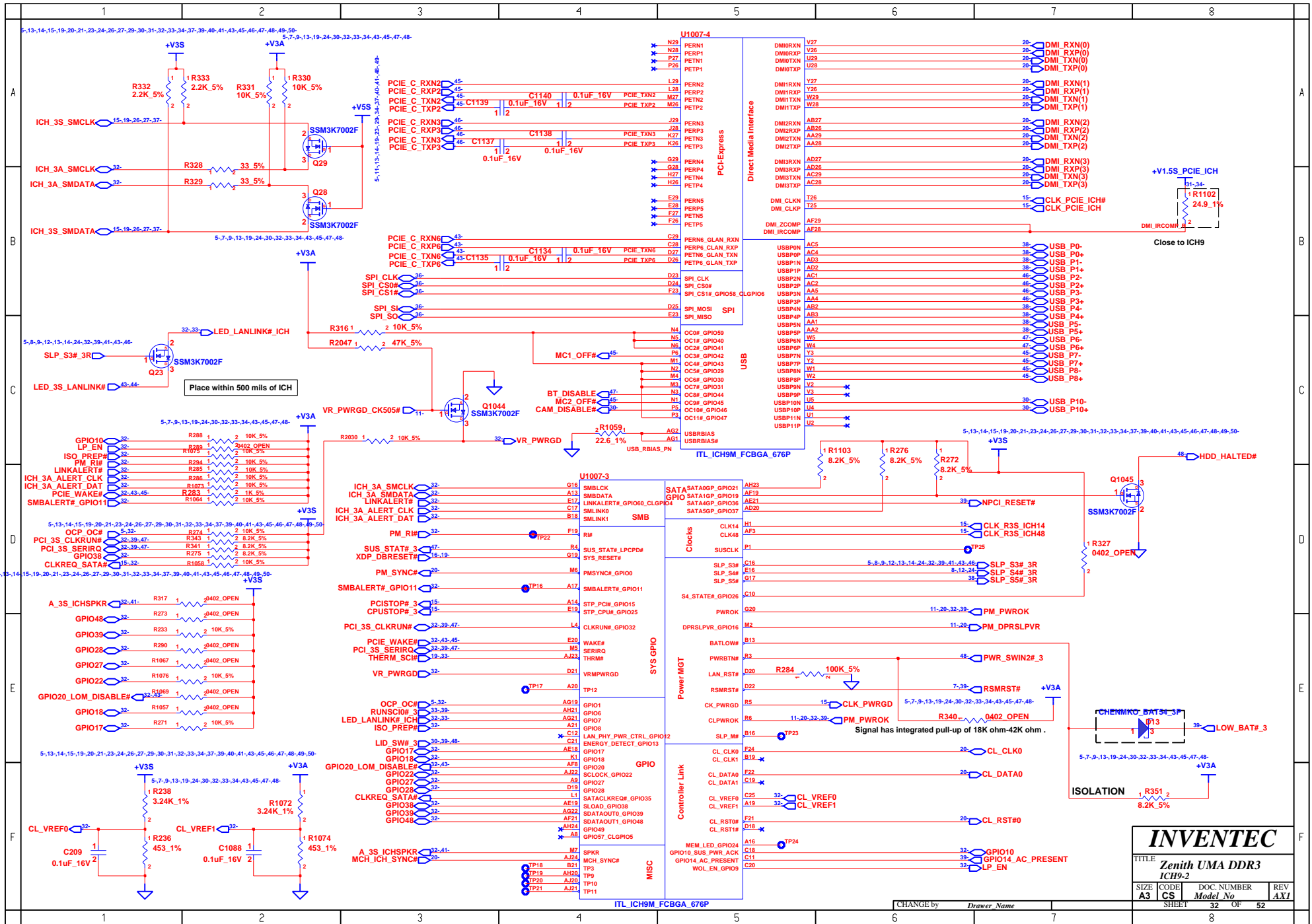
CHANGE by *Drawer Name* 2-Apr-2009  
 SHEET 30 OF 52



**INVENTEC**

TITLE  
Zenith UMA DDR3  
ICH9-1

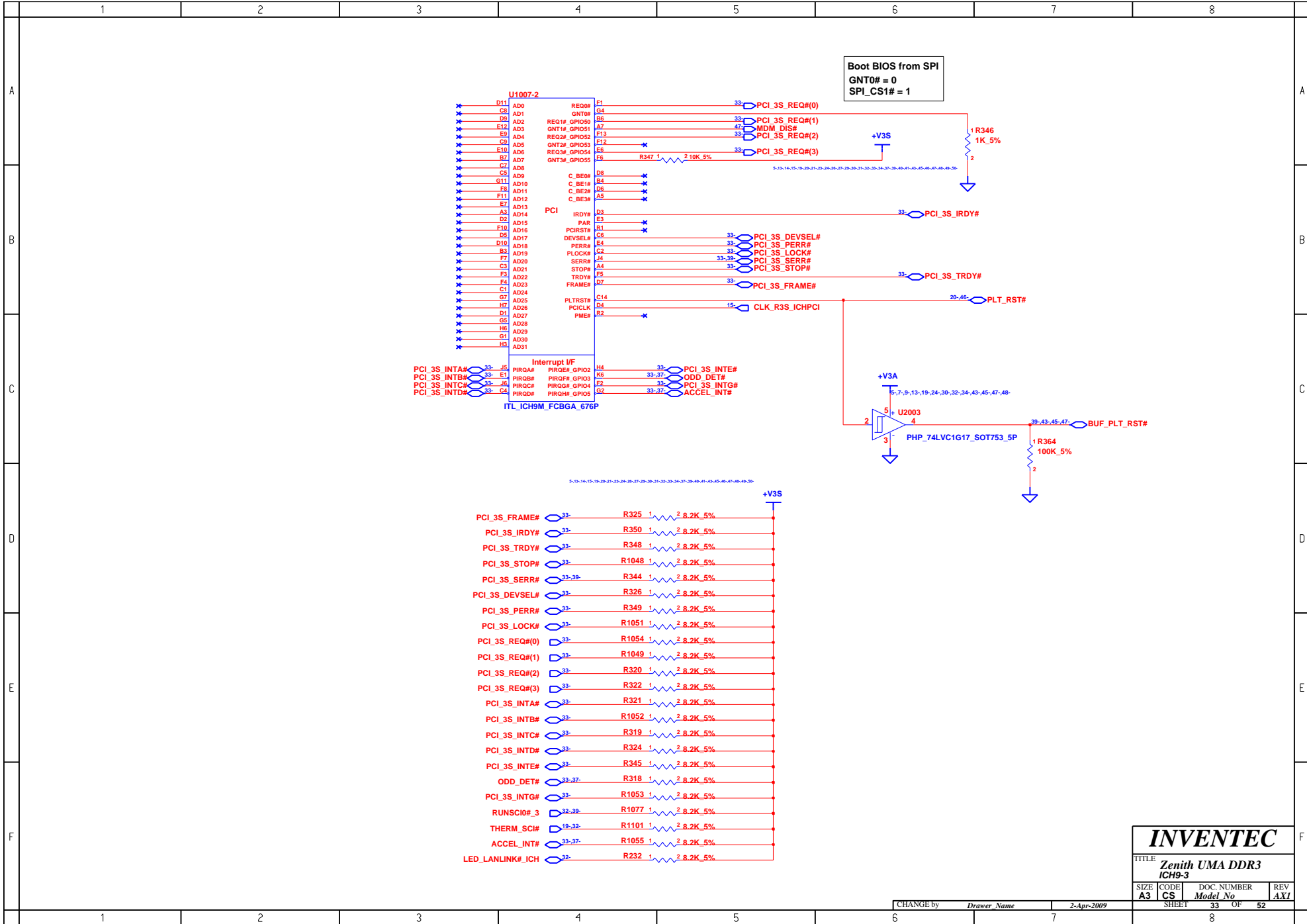
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1



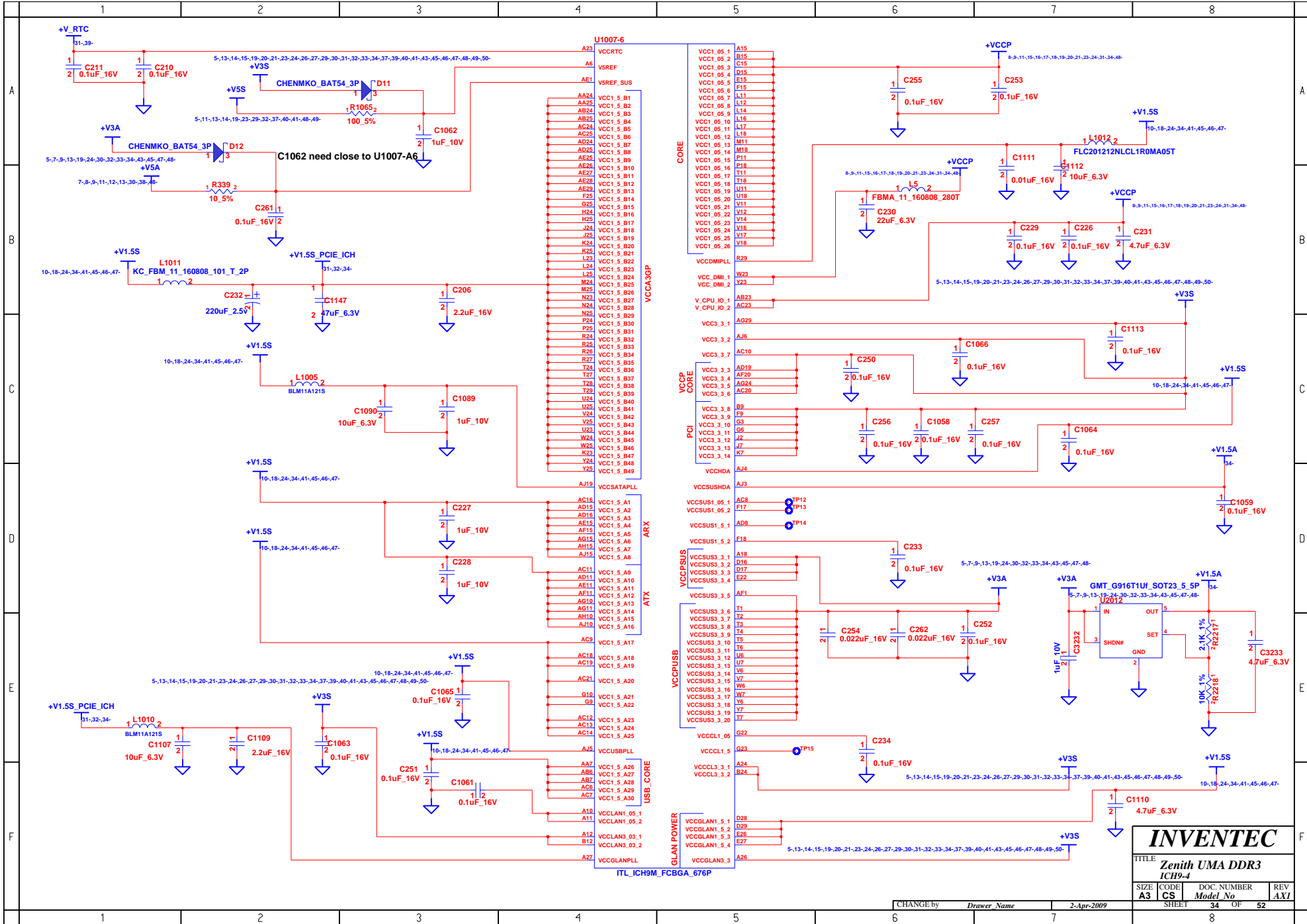
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TITLE <b>Zenith UMA DDR3 ICH9-2</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <i>Model No</i>	REV <b>AX1</b>
SHEET <b>32</b>		OF <b>52</b>	

CHANGE by *Drawer Name*

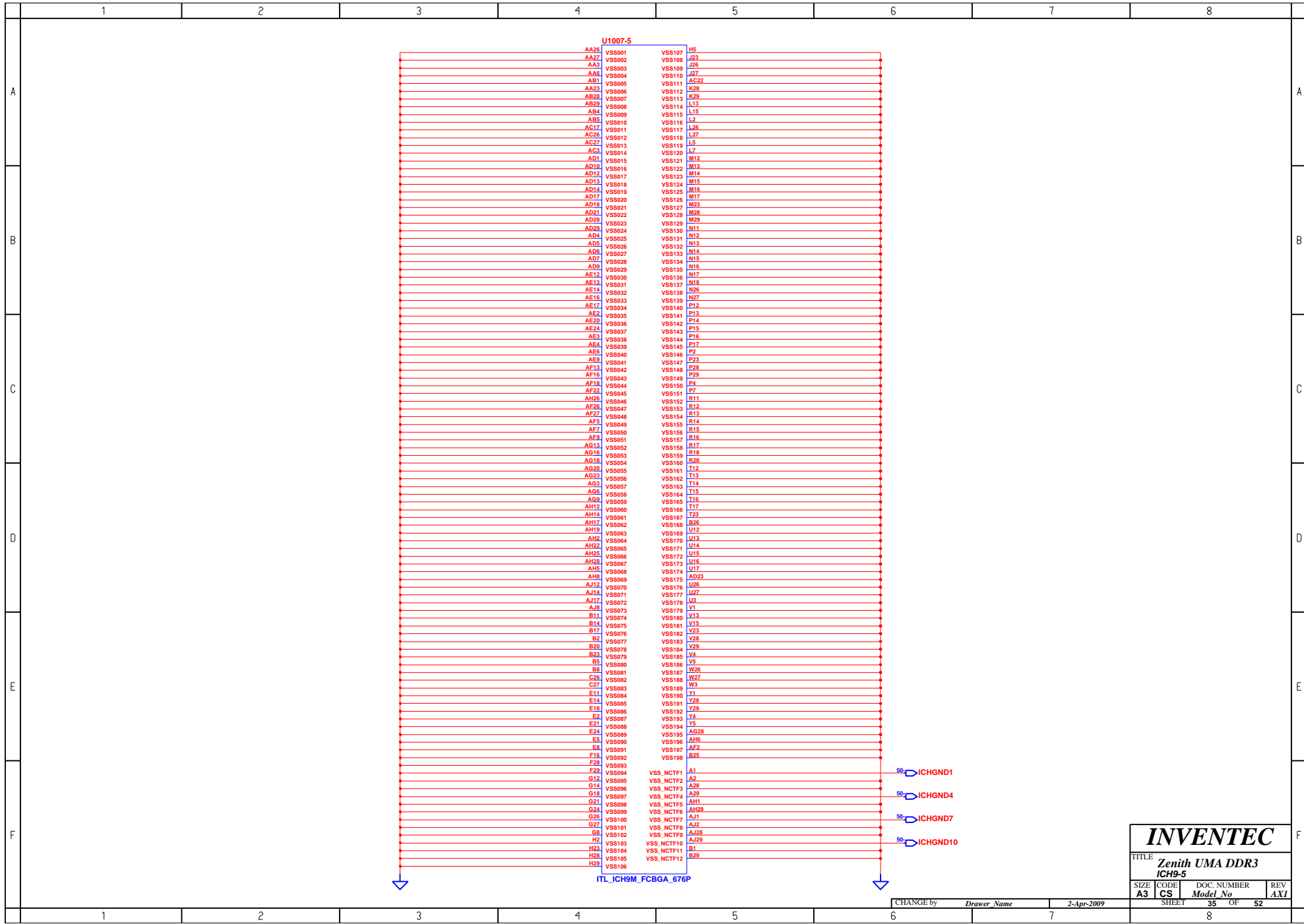




<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3</b> <b>ICH9-3</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	
SHEET <b>33</b>		OF <b>52</b>	



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3</b>			
IC19-4			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1
CHANGE by		Drawer Name	2-Apr-2009
SHEET		34	OF 52



U1007-5

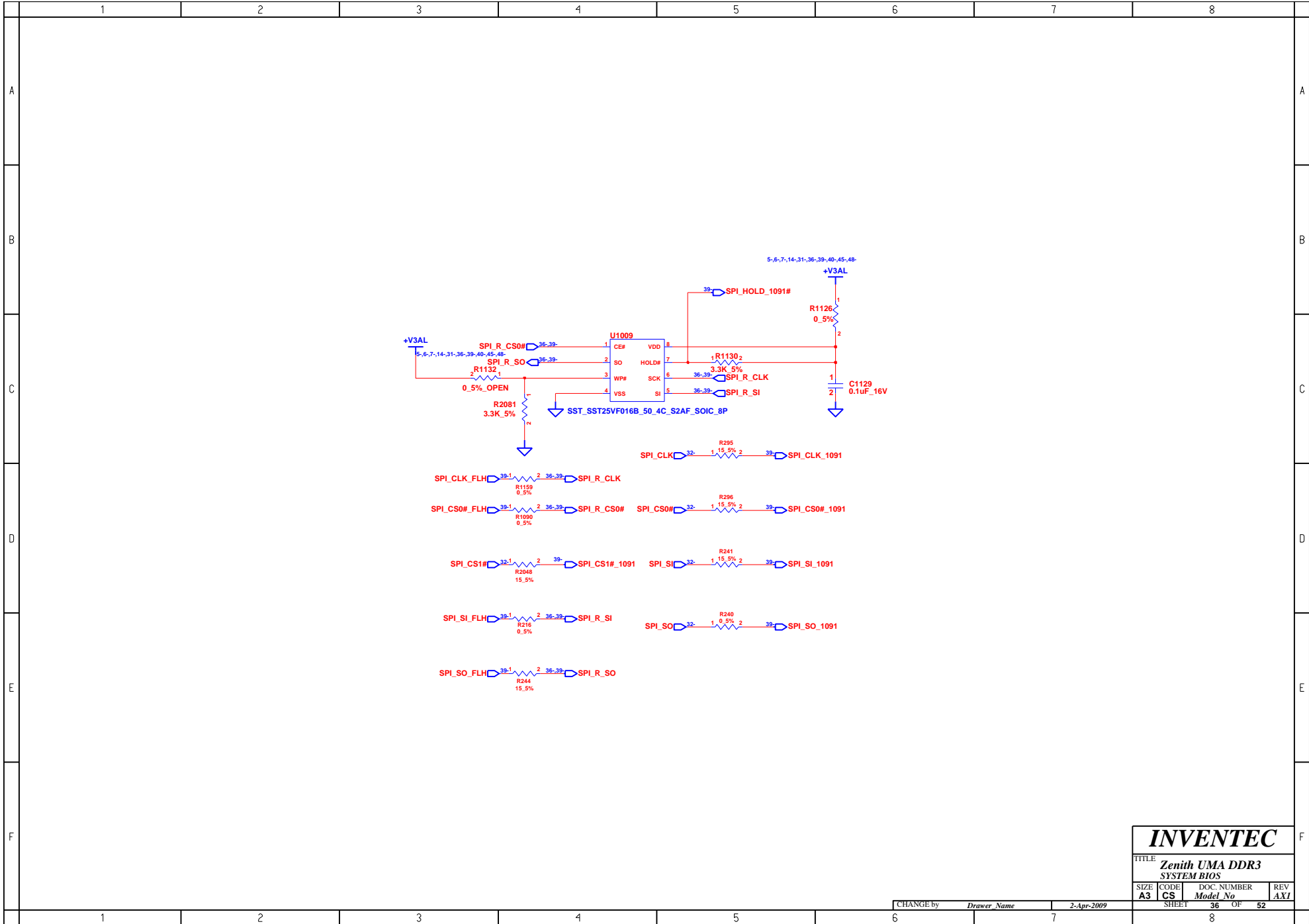
ITL\_ICH9M\_FCBGA 676P

# INVENTEC

TITLE  
Zenith UMA DDR3  
ICH9-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1
SHEET		35 OF	52

CHANGE by *Drawer Name* 2-Apr-2009



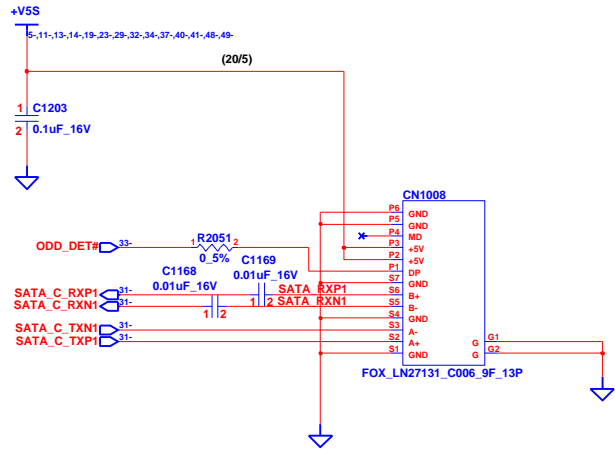
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TITLE  
**Zenith UMA DDR3  
 SYSTEM BIOS**

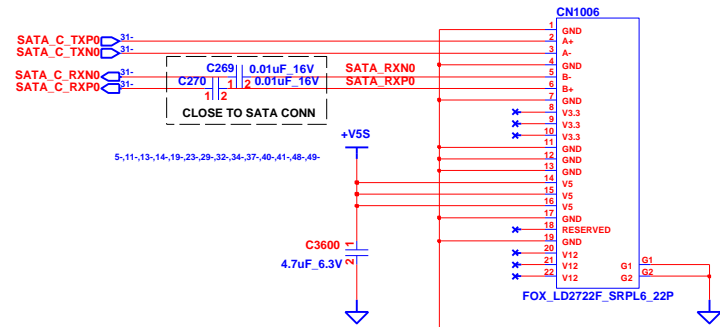
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CHANGE by *Drawer Name* 2-Apr-2009

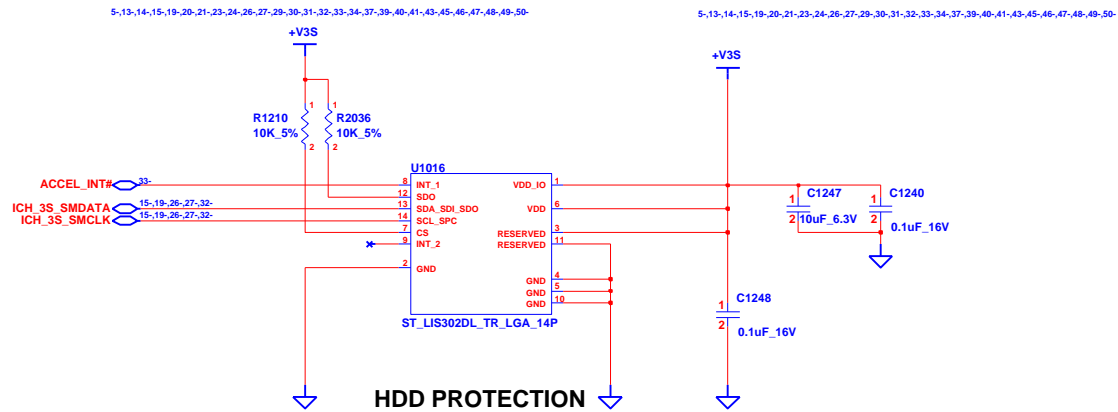
SHEET **36** OF **52**



### SATA ODD CNTR

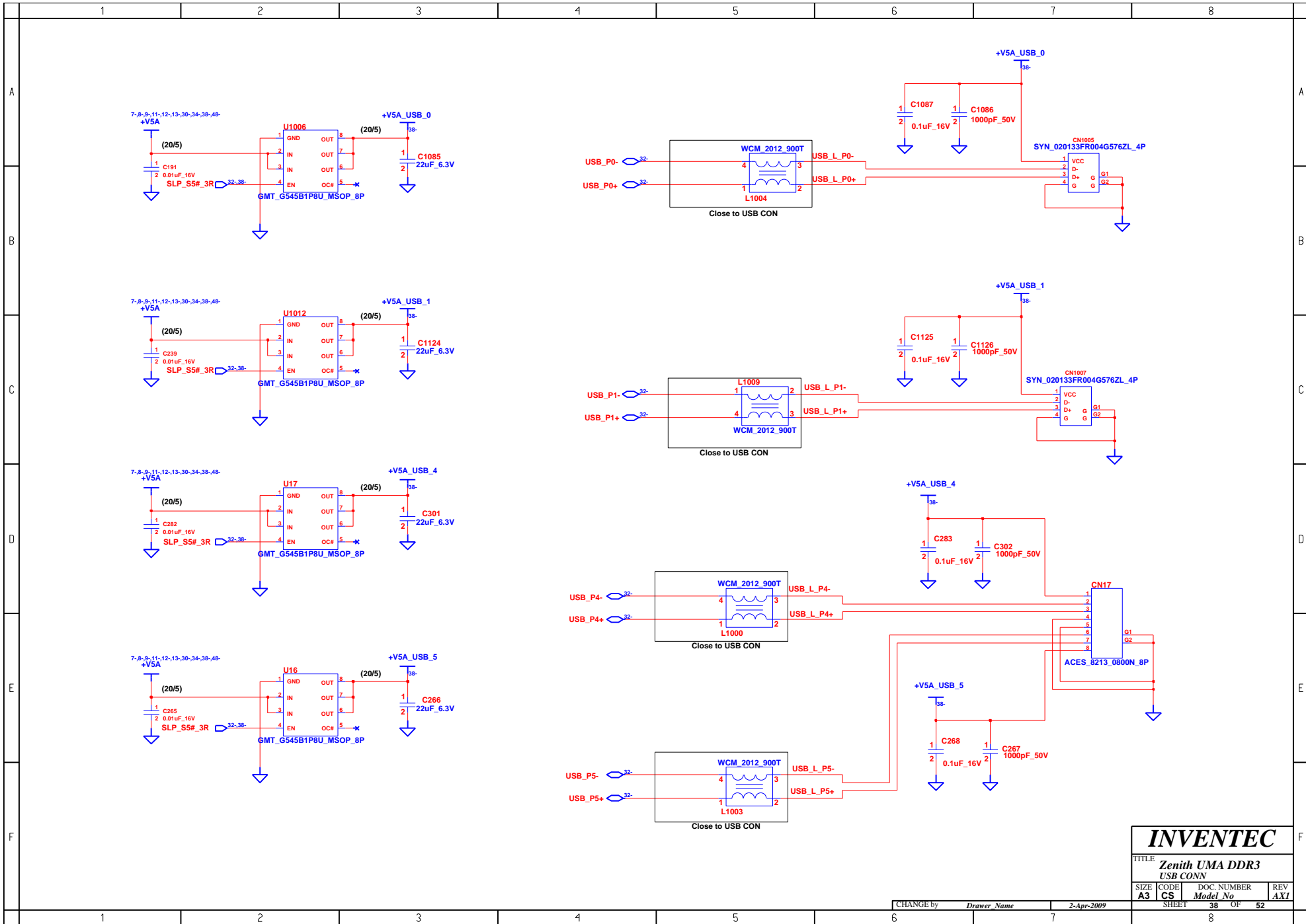


### SATA HDD CNTR



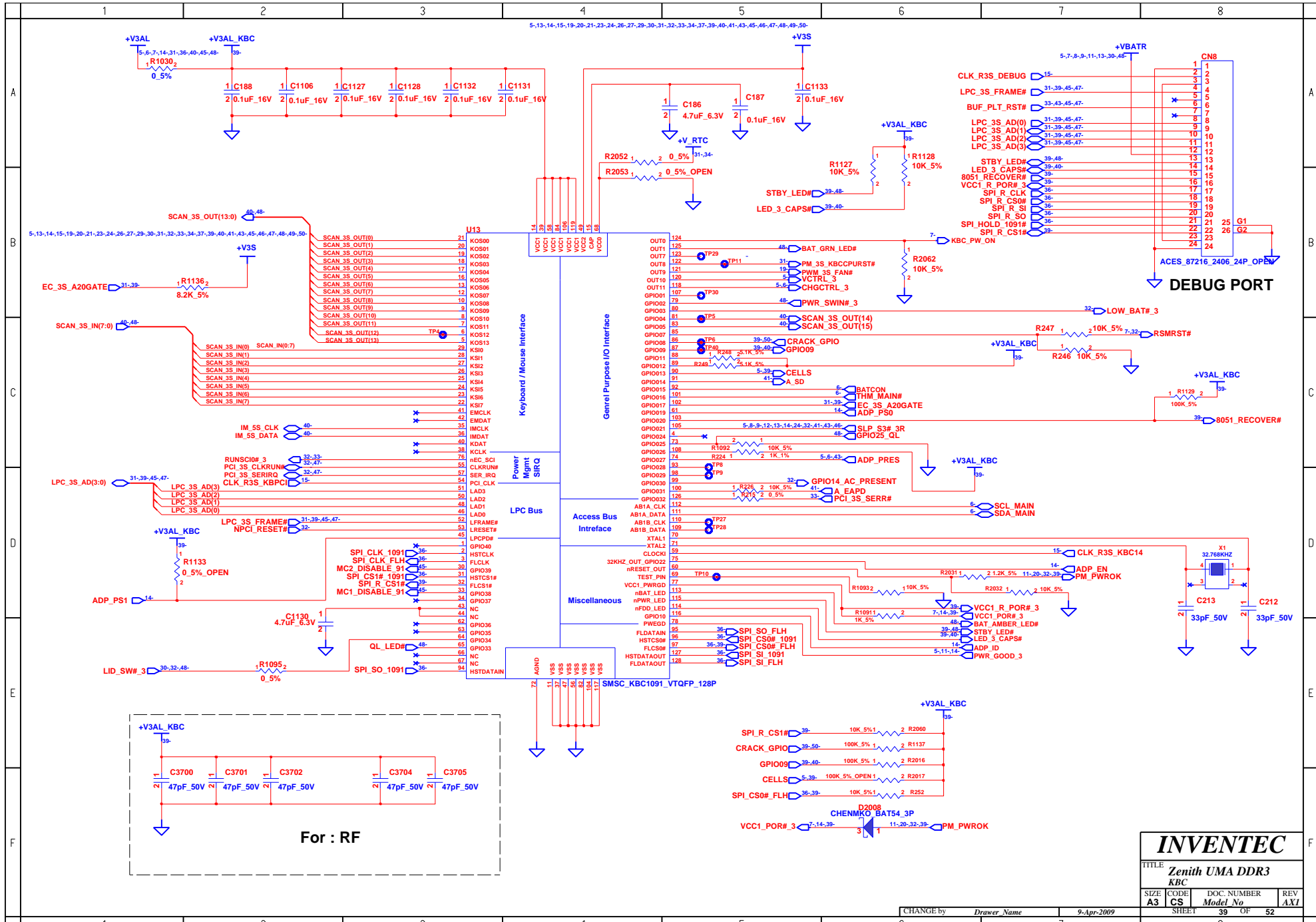
### HDD PROTECTION

<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 HDD &amp; ODD CONN &amp; HD Protec</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	SHEET 37 OF 52



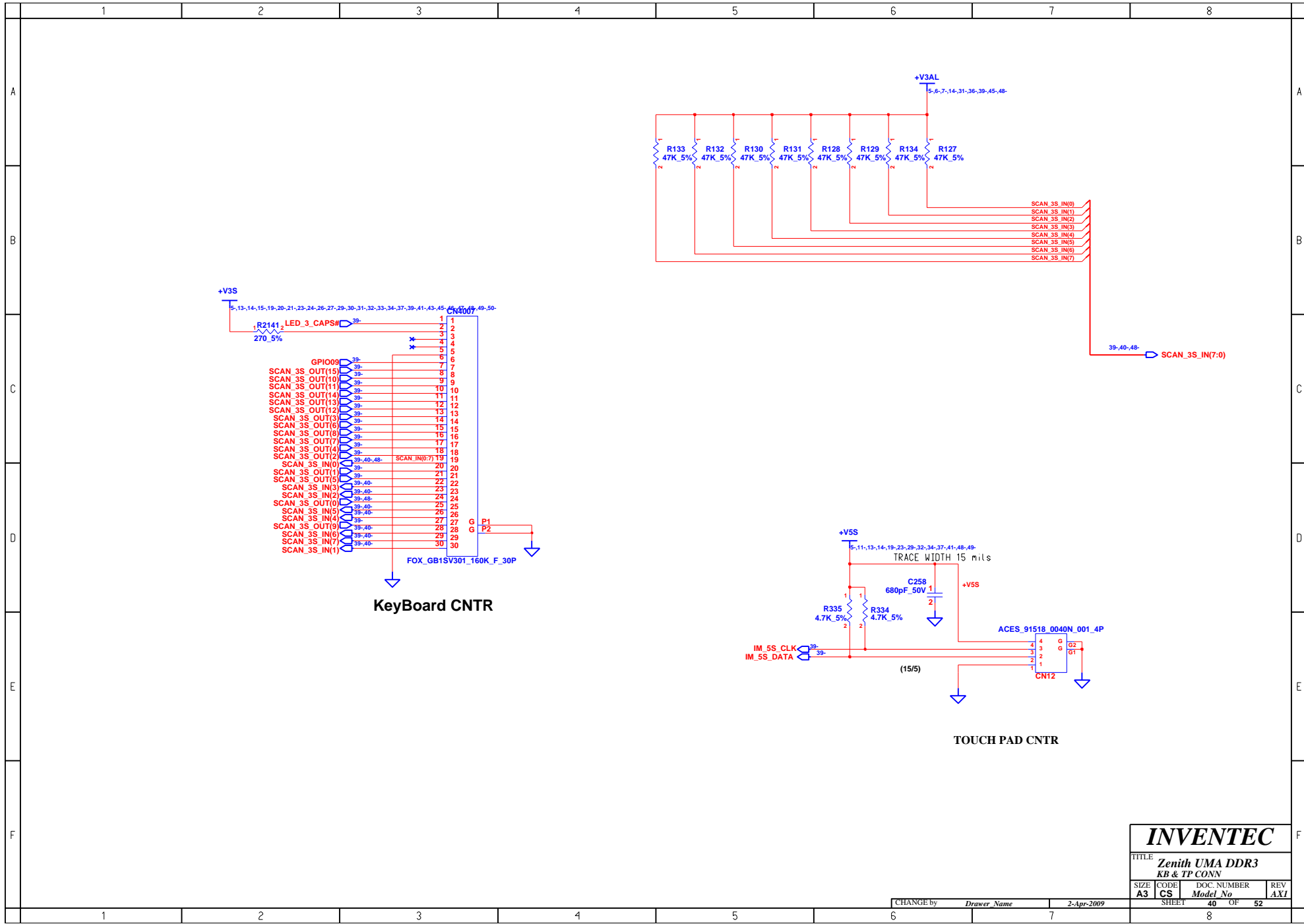
# INVENTEC

TITLE			
Zenith UMA DDR3			
USB CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 KBC</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>Model No</b>	REV <b>AX1</b>
SHEET <b>39</b>		OF <b>52</b>	

CHANGE by *Drawer Name* 9-Apr-2009

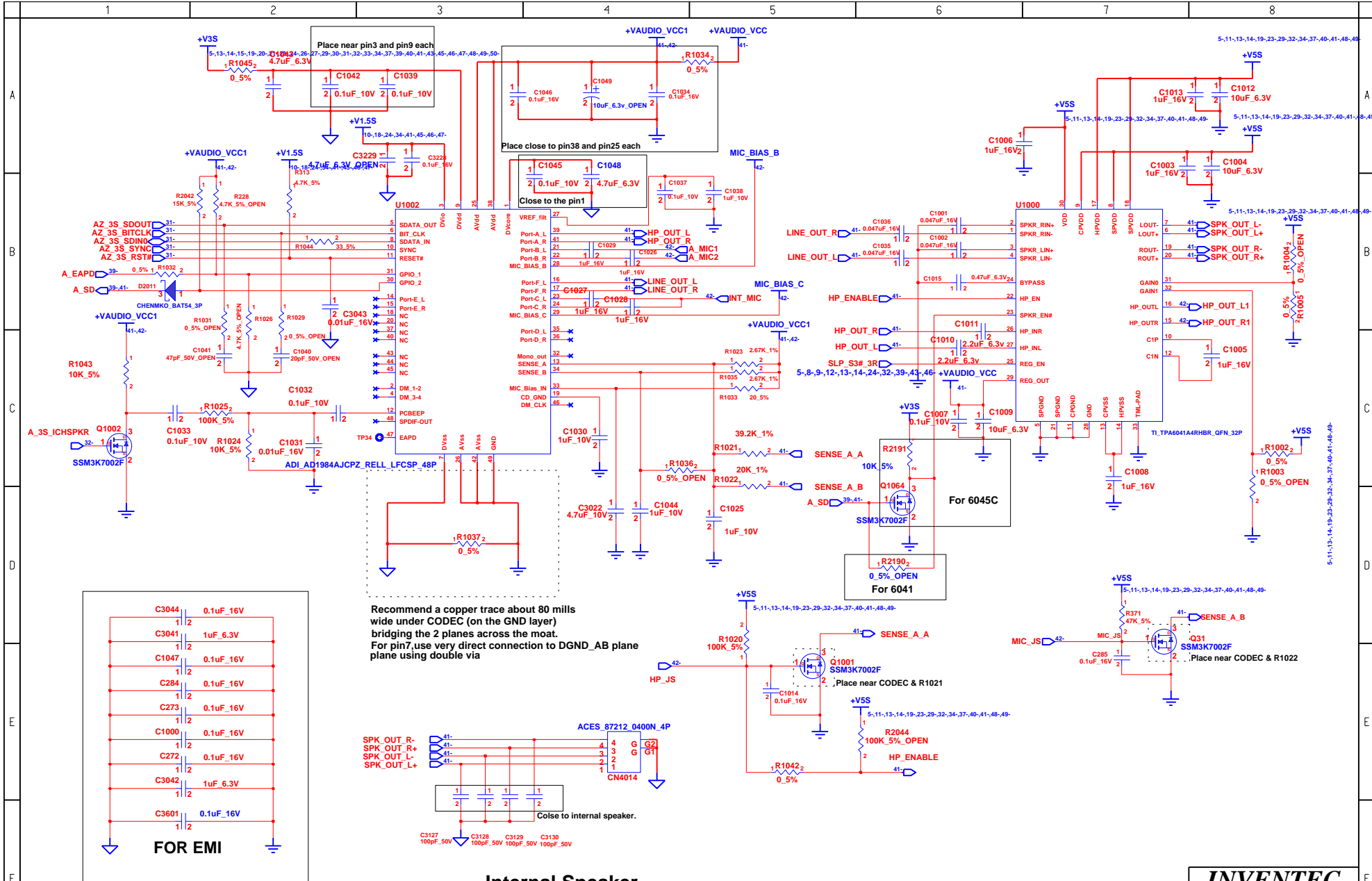


**Keyboard CNTR**

**TOUCH PAD CNTR**

<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 KB &amp; TP CONN</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	SHEET 40 OF 52

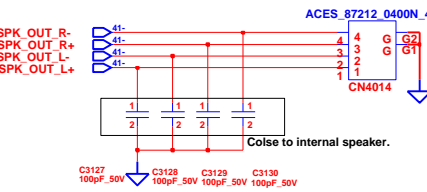




Recommend a copper trace about 80 mils wide under CODEC (on the GND layer) bridging the 2 planes across the moat. For pin7, use very direct connection to DGND\_AB plane using double via

C3044	0.1uF_16V
C3041	1uF_6.3V
C1047	0.1uF_16V
C284	0.1uF_16V
C273	0.1uF_16V
C1000	0.1uF_16V
C272	0.1uF_16V
C3042	1uF_6.3V
C3601	0.1uF_16V

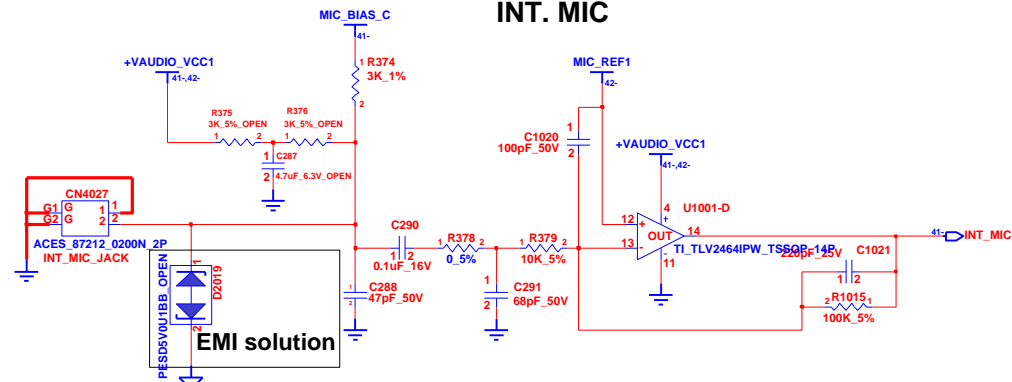
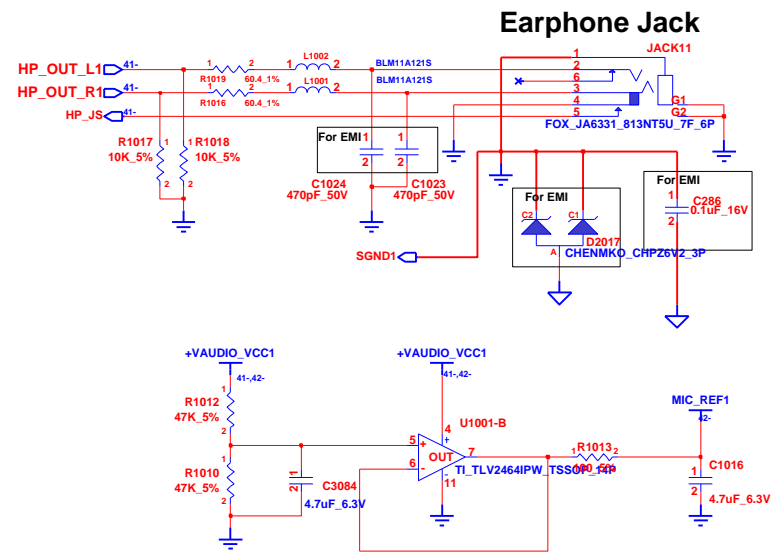
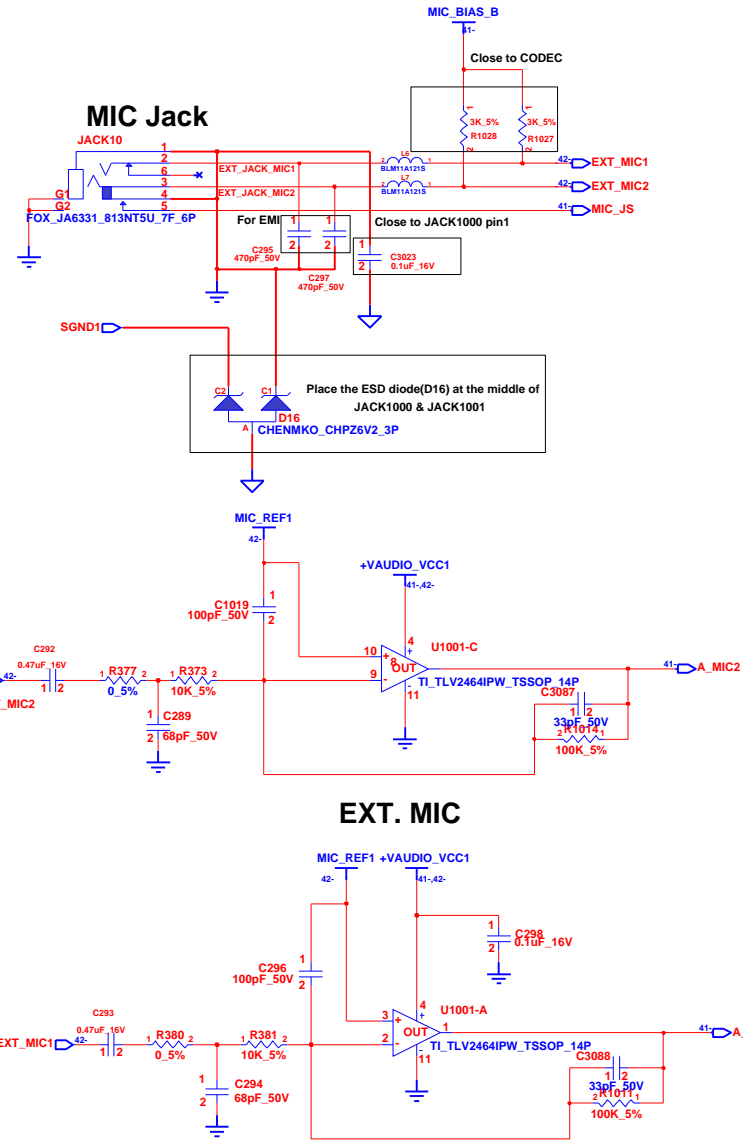
**FOR EMI**



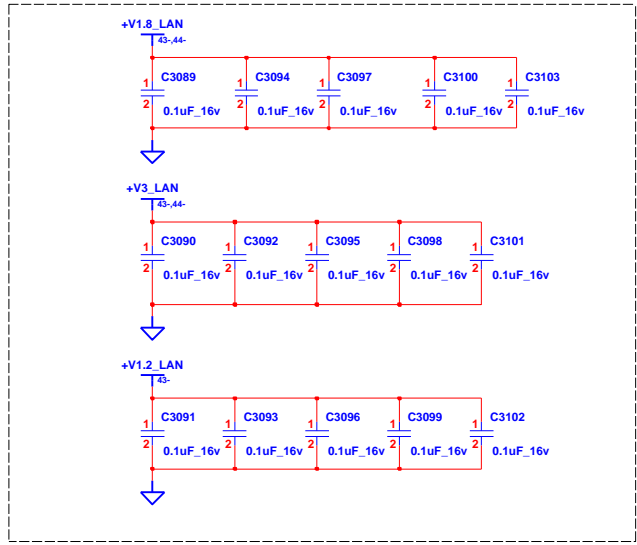
**Internal Speaker**

**INVENTEC**

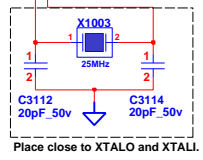
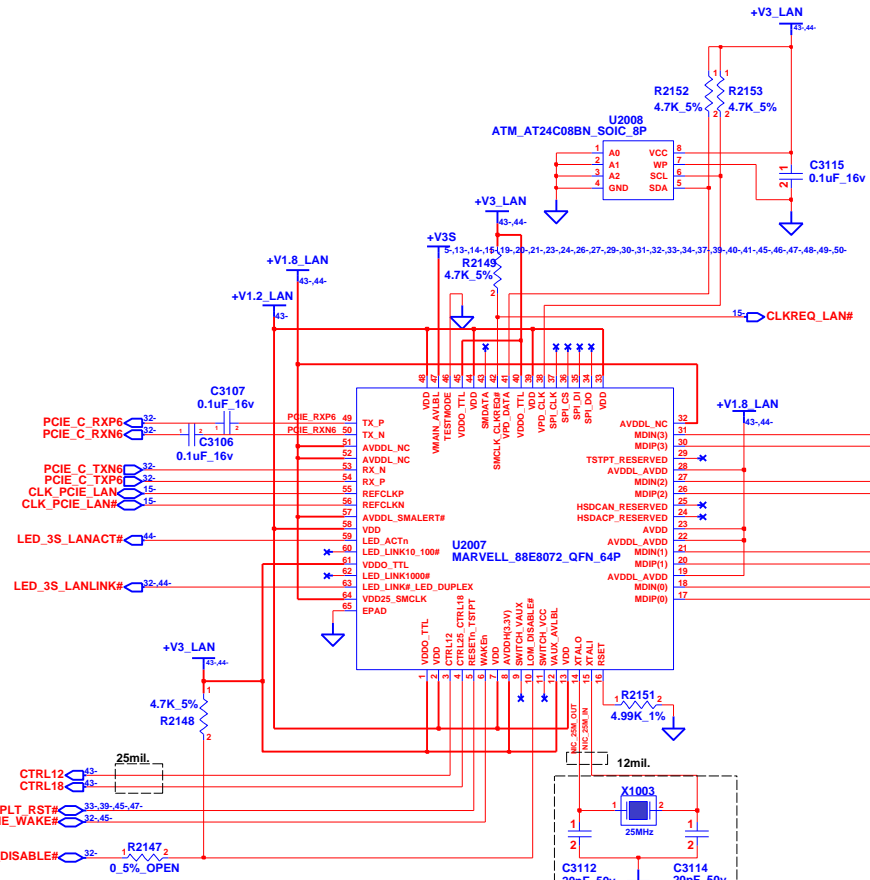
TITLE			
Zenith UMA DDR3 AUDIO CODEC			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1



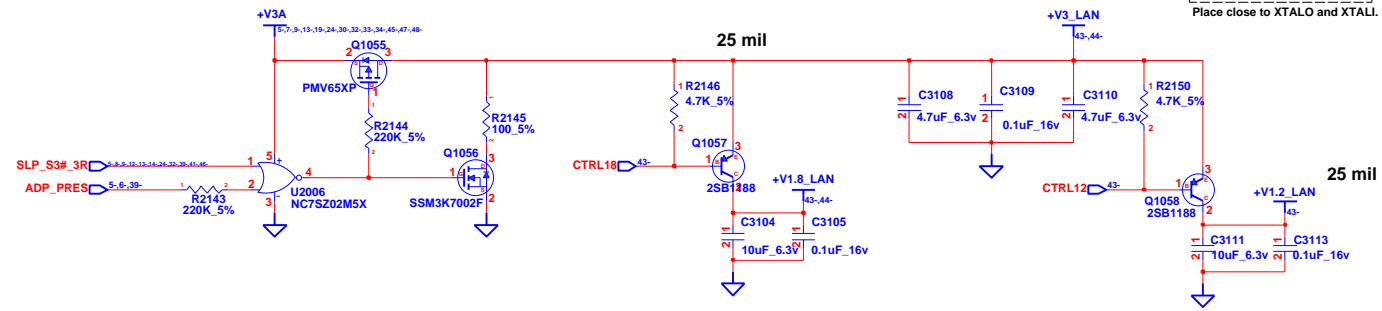
<b>INVENTEC</b>			
TITLE Zenith UMA DDR3 AUDIO JACK			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Drawer Name		2-Apr-2009	
SHEET 42		OF 52	



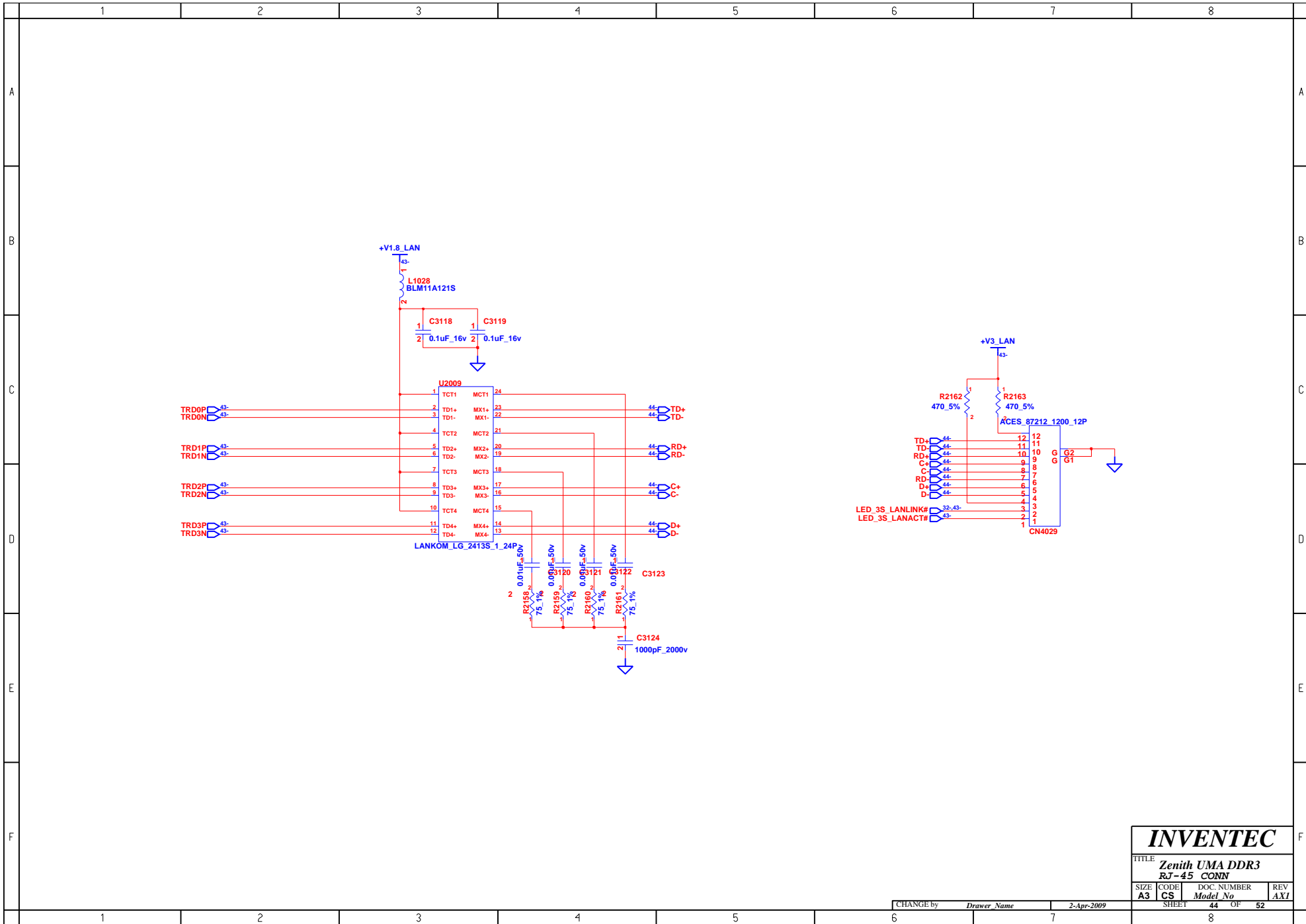
Place bypass cap as close as possible with every power pin.



Place close to XTALO and XTALI.



<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 Giga LAN</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	
SHEET 43		OF 52	



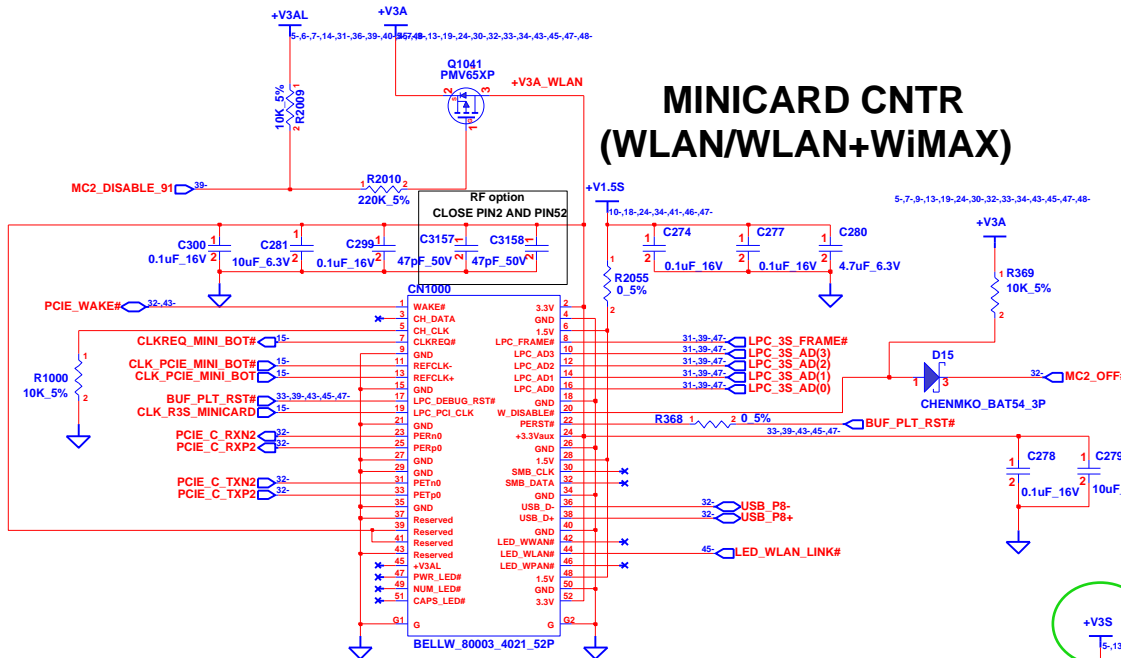
# INVENTEC

TITLE  
**Zenith UMA DDR3**  
**RJ-45 CONN**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
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CHANGE by *Drawer Name* 2-Apr-2009 SHEET 44 OF 52

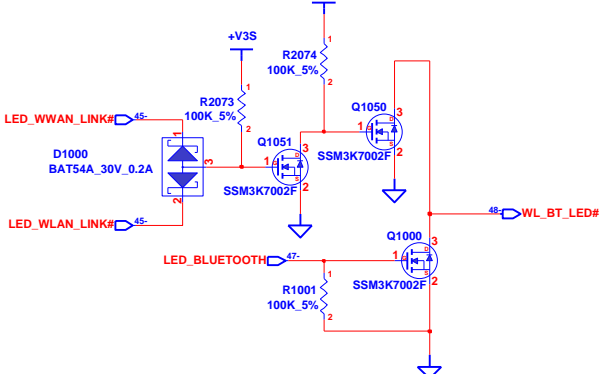
# MINICARD CNTR (WLAN/WLAN+WiMAX)



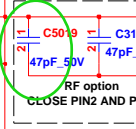
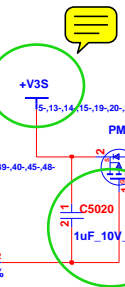
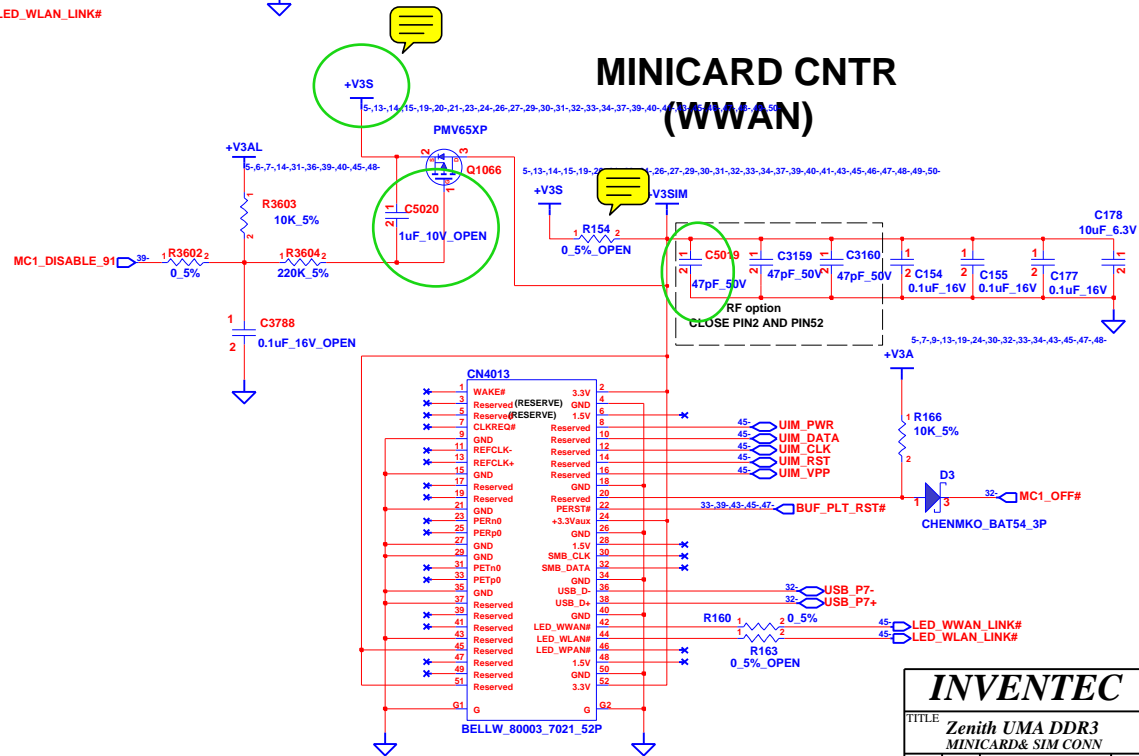
5,13,14,15,19,20,21,23,24,26,27,29,30,31,32,33,34,37,39,40,41,43,45,46,47,48,49,50

5,13,14,15,19,20,21,23,24,26,27,29,30,31,32,33,34,37,39,40,41,43,45,46,47,48,49,50

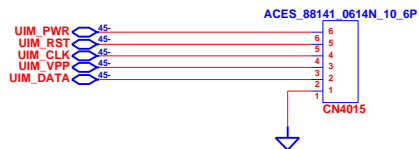
# WLAN\_Bluetooth LED



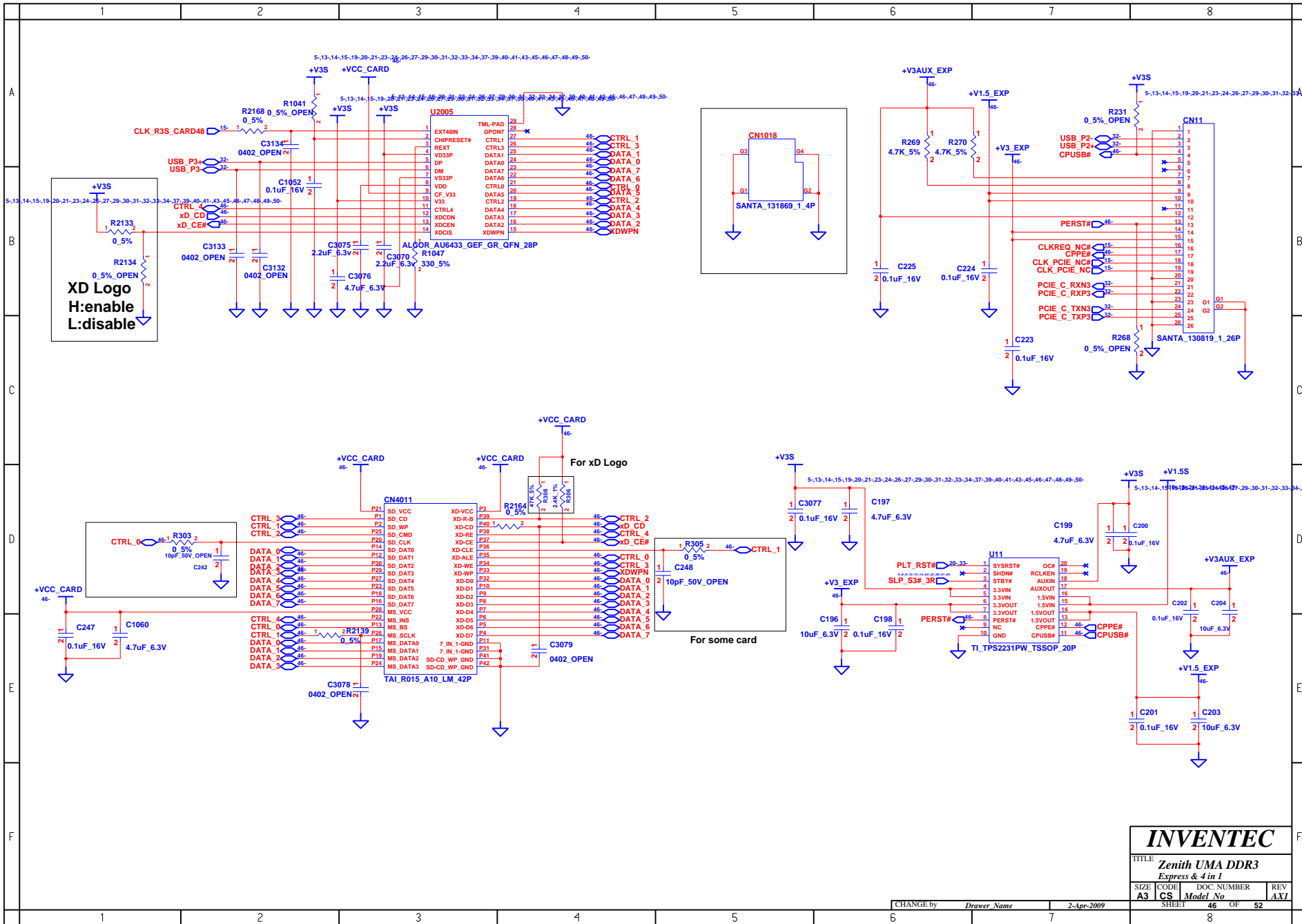
# MINICARD CNTR (WWAN)



# SIMCARD CNTR



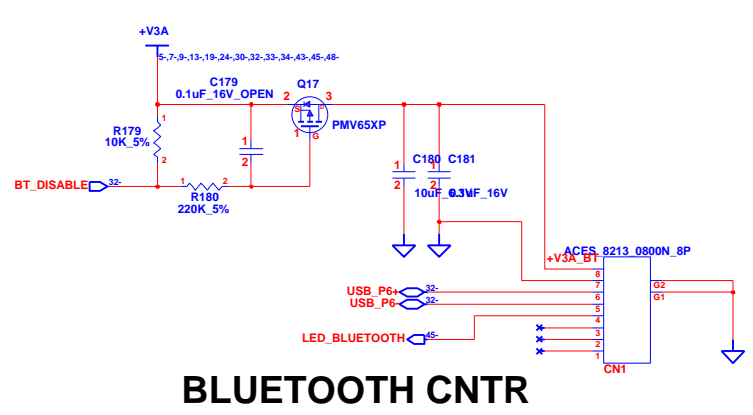
<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 MINICARD&amp; SIM CONN</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		25-May-2009	SHEET 45 OF 52



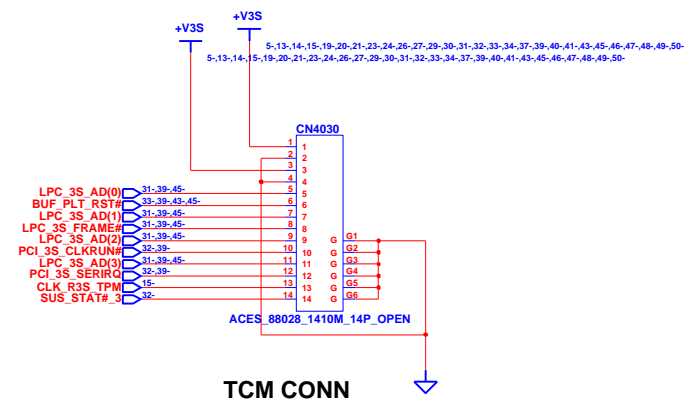
# INVENTEC

TITLE  
**Zenith UMA DDR3**  
 Express & 4 in 1  
 SIZE CODE DOC. NUMBER REV  
 A3 CS Model No AX1  
 SHEET 46 OF 52

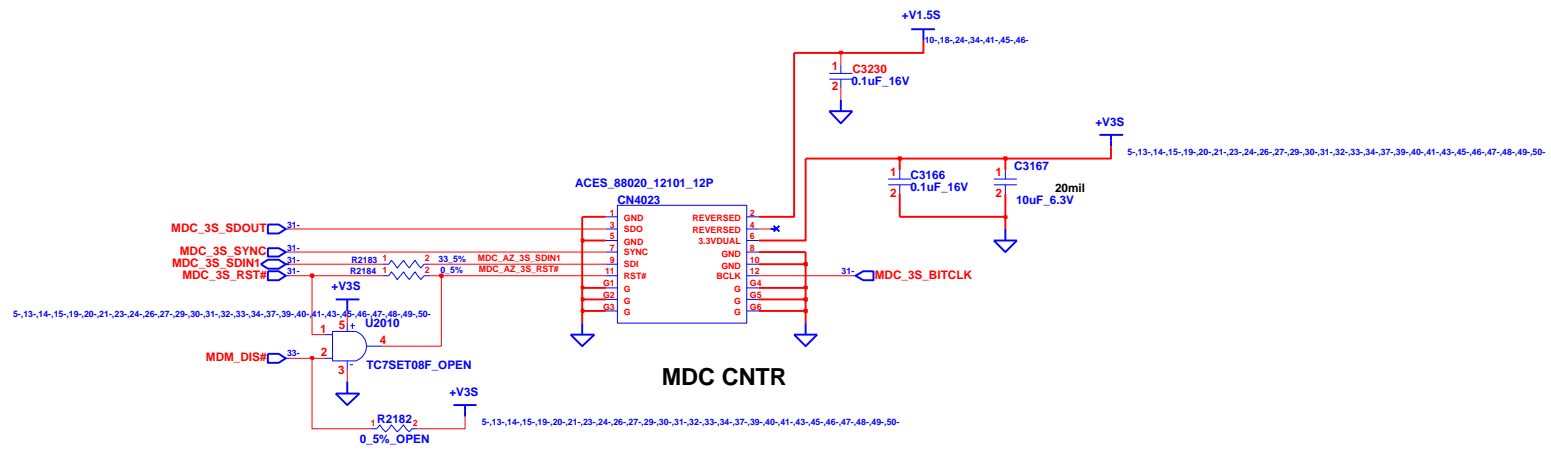
CHANGE by *Drawer Name* 2-Apr-2009



**BLUETOOTH CNTR**

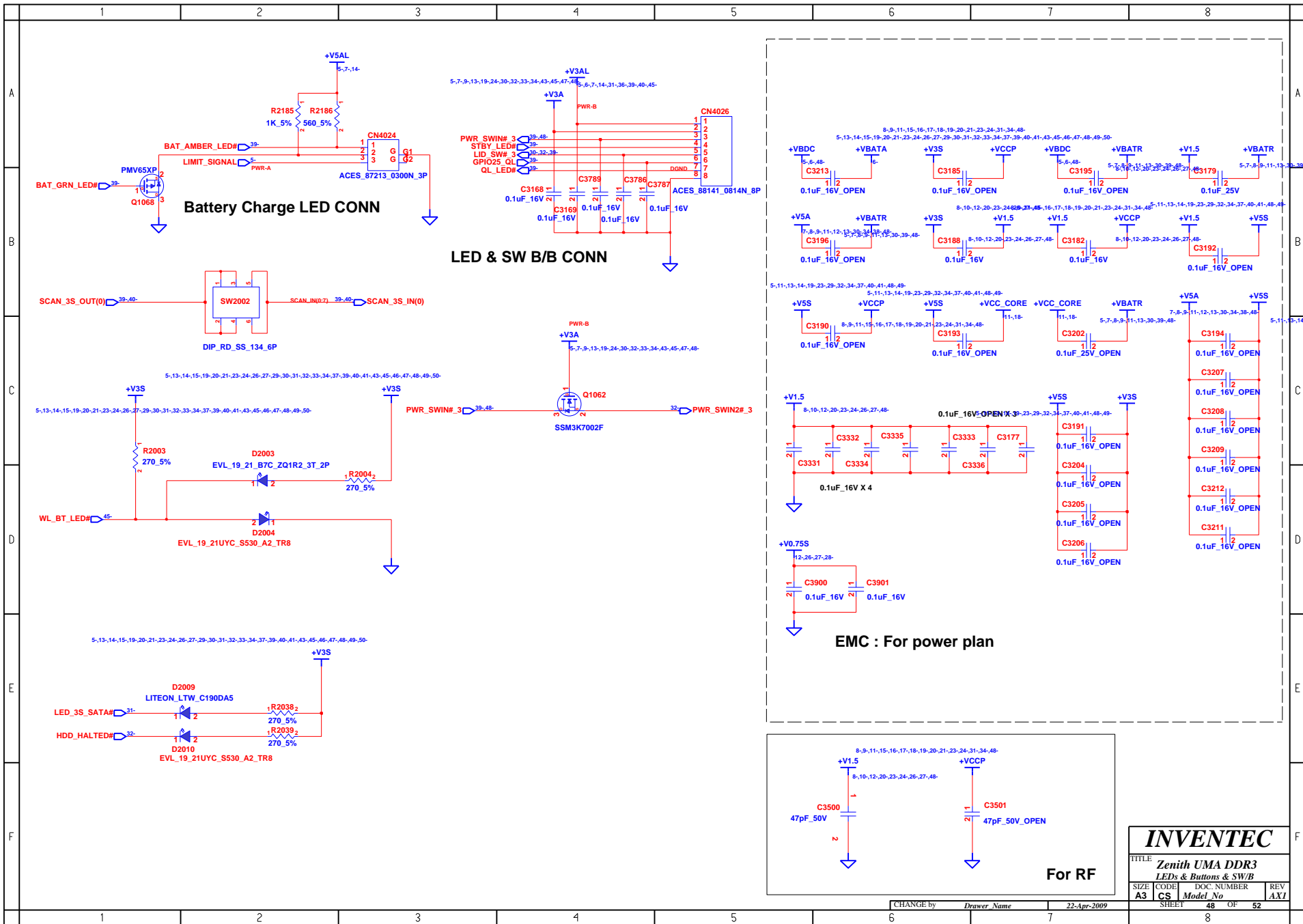


**TCM CONN**



**MDC CNTR**

<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3 BT &amp; MDC &amp; TCM</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	SHEET 47 OF 52



**Battery Charge LED CONN**

**LED & SW B/B CONN**

**EMC : For power plan**

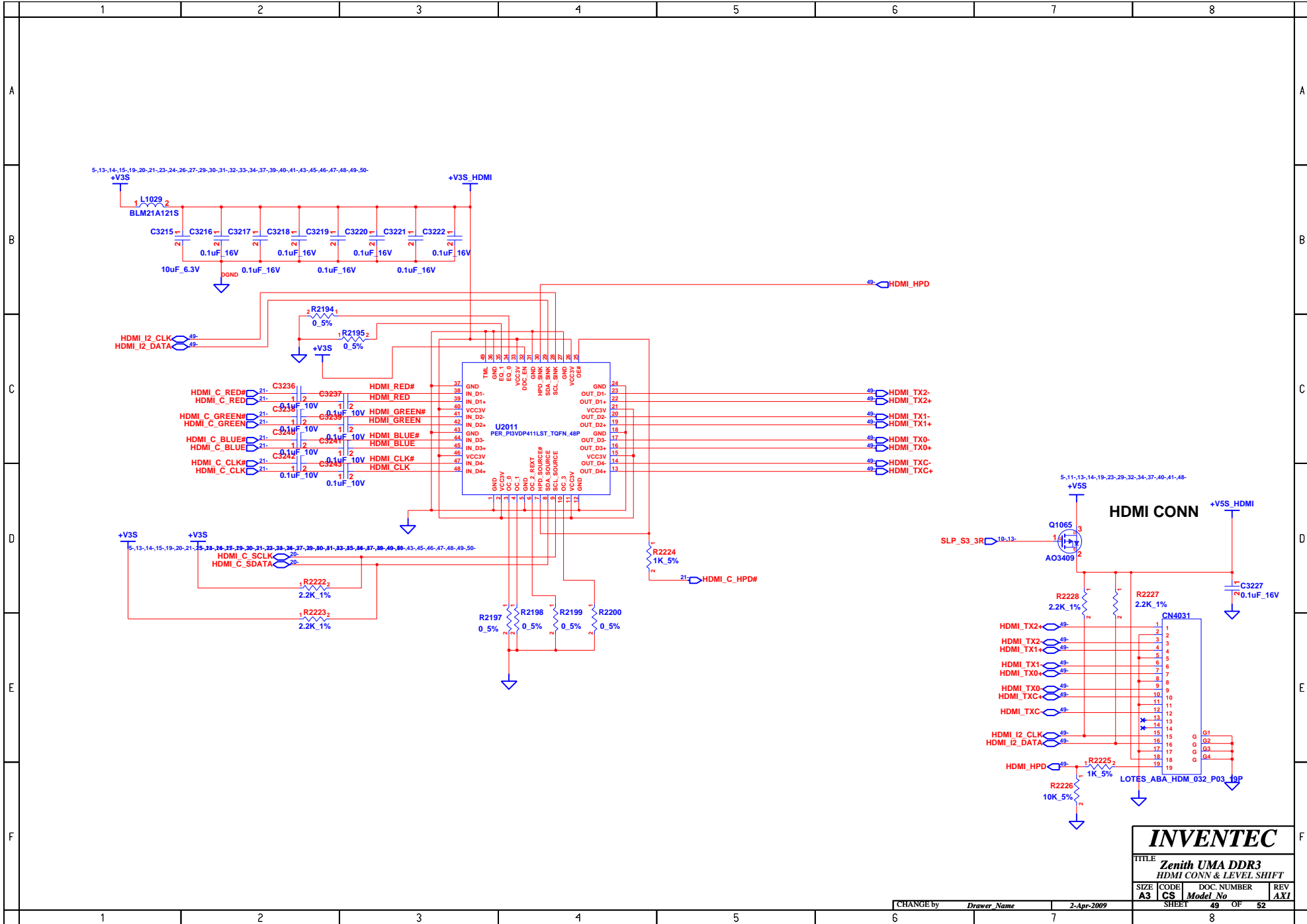
**For RF**

**INVENTEC**

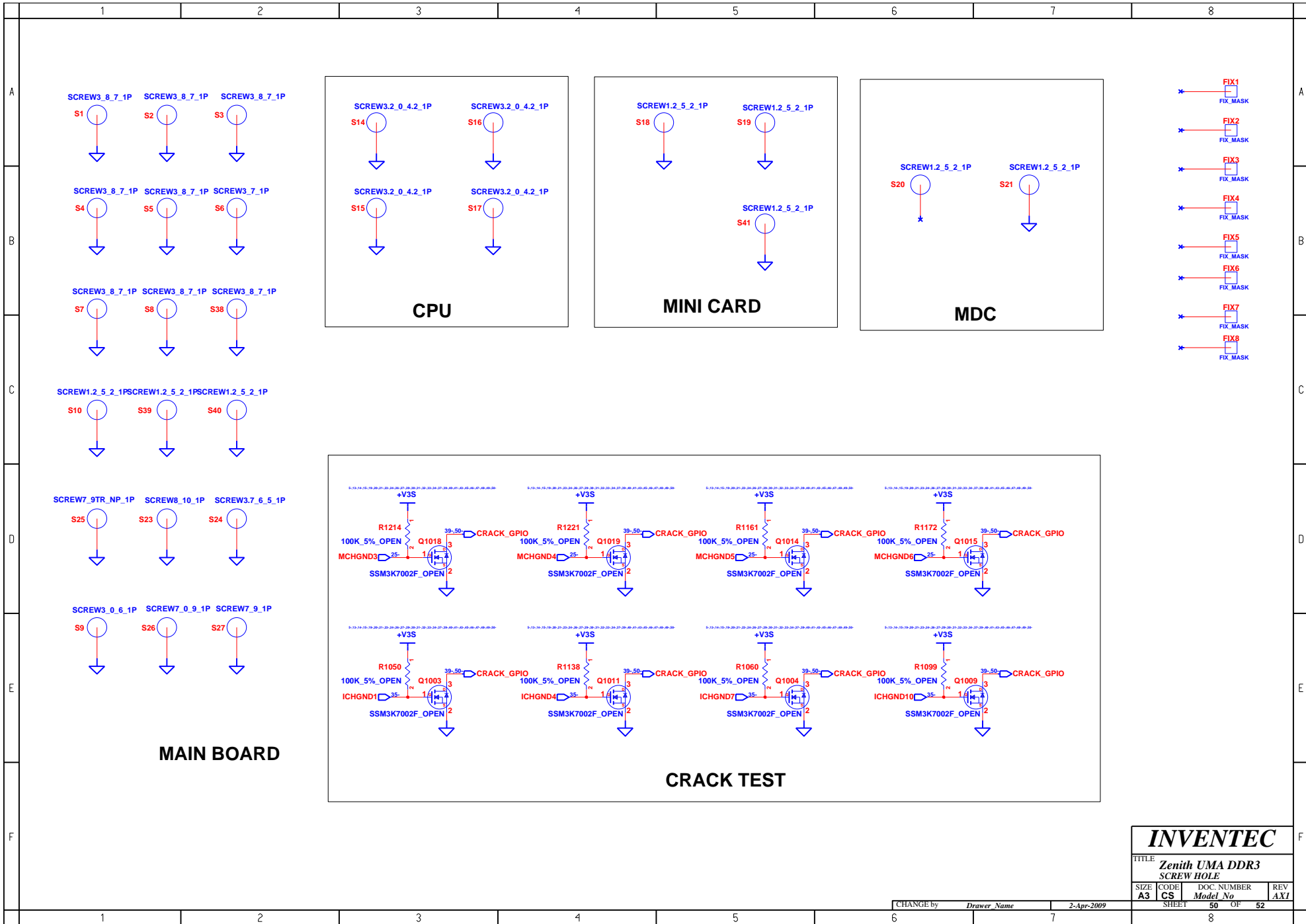
TITLE **Zenith UMA DDR3**  
**LEDs & Buttons & SW/B**

SIZE	CODE	DOC. NUMBER	REV.
A3	CS	Model No	AXT

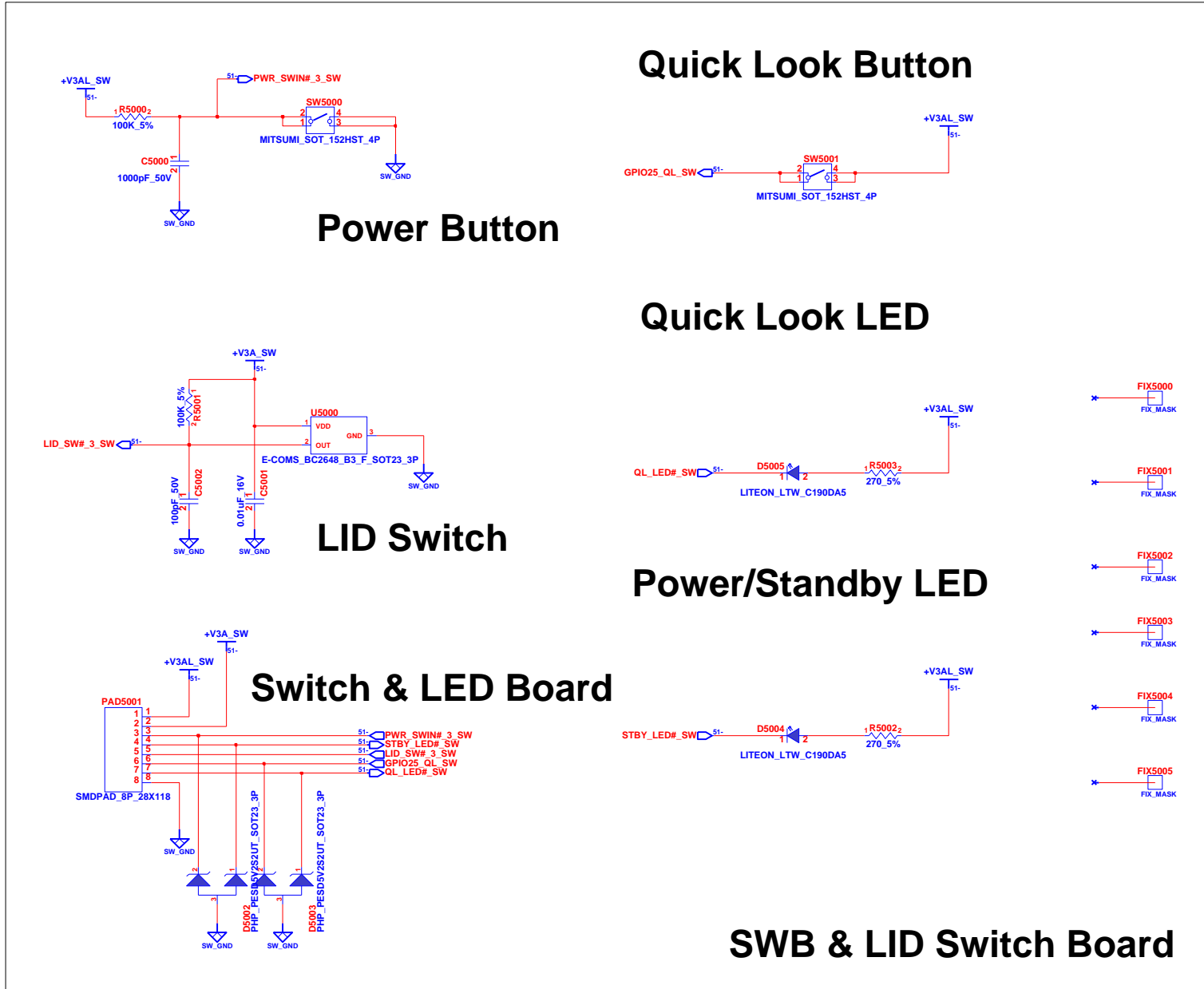




<b>INVENTEC</b>			
TITLE <b>Zenith UMA DDR3</b> HDMI CONN & LEVEL SHIFT			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <i>Model No</i>	REV <b>AX1</b>
CHANGE by <i>Drawer Name</i>		2-Apr-2009	SHEET 49 OF 52



<b>INVENTEC</b>			
TITLE Zenith UMA DDR3 SCREW HOLE			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Drawer Name		2-Apr-2009	SHEET 50 OF 52
1	2	3	8



### Quick Look Button

### Power Button

### Quick Look LED

### LID Switch

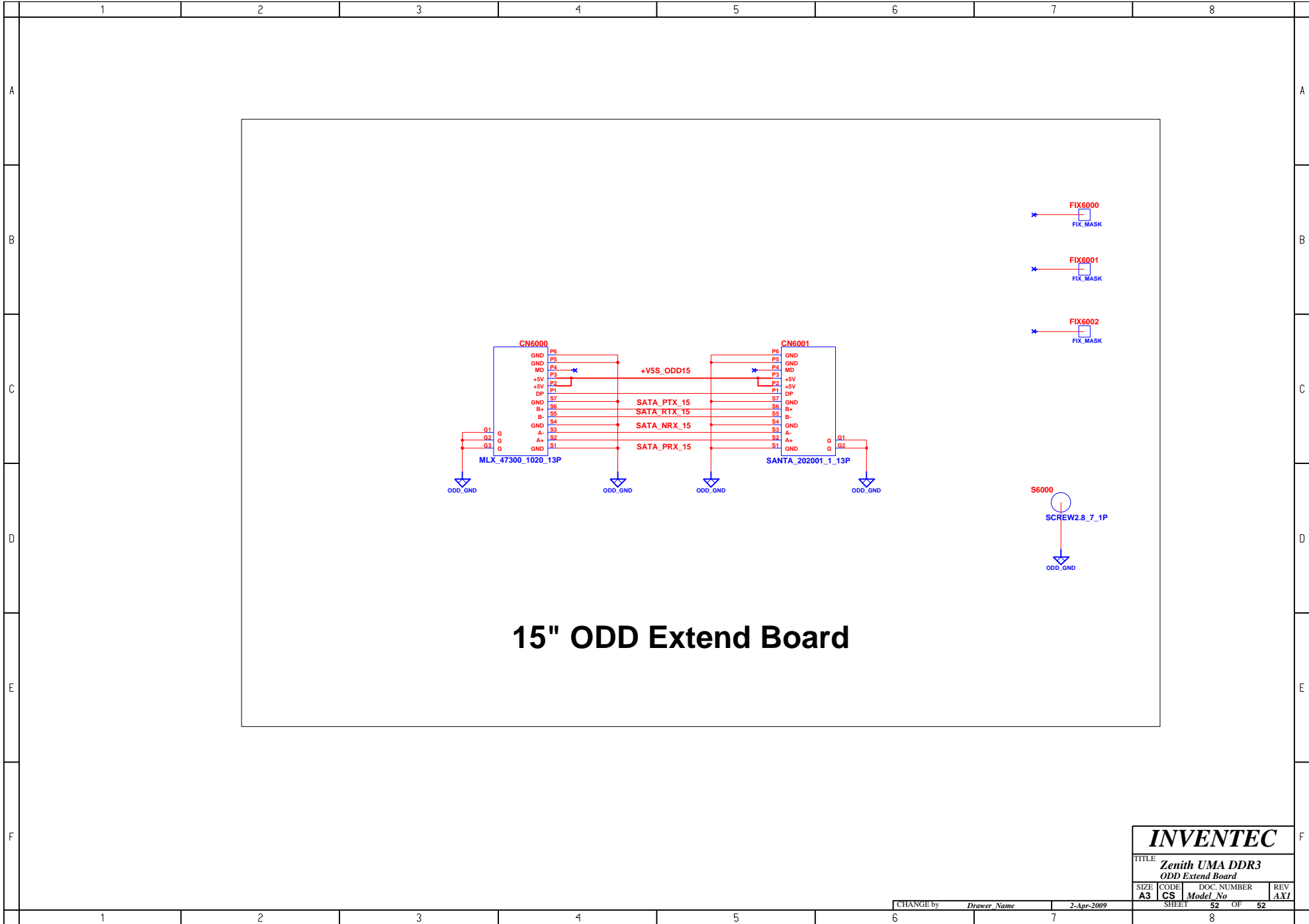
### Power/Standby LED

### Switch & LED Board

### SWB & LID Switch Board

- ★ FIX5000  
FIX\_MASK
- ★ FIX5001  
FIX\_MASK
- ★ FIX5002  
FIX\_MASK
- ★ FIX5003  
FIX\_MASK
- ★ FIX5004  
FIX\_MASK
- ★ FIX5005  
FIX\_MASK

<b>INVENTEC</b>			
TITLE Zenith UMA DDR3 SWB & LID Switch			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
CHANGE by Drawer Name		2-Apr-2009	
SHEET 51		OF 52	



# 15" ODD Extend Board

**INVENTEC**

TITLE: **Zenith UMA DDR3  
ODD Extend Board**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Drawer Name* 2-Apr-2009

SHEET 52 OF 52