MODEL	REV	CHANGE LIST
CT3/5 MB 31CT3MB0015 31CT3MB0031	1A	PAGE 2 --- Enable CLK48M from clokc generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL. PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032. PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor. PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality. PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting. 2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue. 3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage. PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402). PAGE 15 --- Add a level-shift cicuit for EDID interface. PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M. 2. Remove the reserve resistors (R693~R695) of parallel interface for PCI1510. PAGE 18 --- Remove R696, connect controller and power switch directly . PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test. PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality. 2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment. PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection. 2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue. PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application. PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging. PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms. 2. Add a LPC debug port for software team to debug convenient. PAGE 30 --- Add GMT fan controller for B-test to costdown. PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking. 2. Add R713 to enable the mux in the Tampa-2 cable PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue. PAGE 35 --- 1. Move 5V_S5 circuit to Page 36. 2. De-popuplate PQ129 and PR182. 3. Change PR178 value from 22 ohm to 47 ohm. PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.

Model / Page	CT3/5 MB BOARD FROM	CT3/5 MB BOARD TO
1	1A	
2	1A	2A
3	1A	2A
4	1A	2A
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	2A
11	1A	2A
12	1A	2A
13	1A	
14	1A	
15	1A	2A
16	1A	
17	1A	2A
18	1A	2A
19	1A	2A
20	1A	
21	1A	
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	
26	1A	2A
27	1A	2A
28	1A	
29	1A	
30	1A	2A
31	1A	2A
32	1A	
33	1A	2A
34	1A	
35	1A	2A
36	1A	2A
37	1A	
38	1A	
39	1A	

MODEL	REV	CHANGE LIST
CT3/5 MB 31CT3MB0015 31CT3MB0031	2A	

```
PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance.

PAGE 3 --- 1. Add R733 as pull-up resistor for PREQ#.
PAGE 11 --- 1. Add RF_OFF# and BT_OFF#
PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance.
            2. Remove R701 & R702 for unused PCI1510RVGF circuit.
PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side.
            2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM.
            3. Add a discharge circuit for media card power.
            4. Add R718 to solve cross-talk issue of MS-Pro card.
            5. Add R717 to solve SM card can't write protect issue.
            6. Add R719~R736 as terminal on all multi-function pins.
            7. Add pull-up circuit.

PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit.
            2. Modify LPC pin name.

PAGE 28 --- 1. Change HDD and ODD select definition.

PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue.
            1. Change L66, L67, L68 from BK1608HM470 to 0R.
            2. Remove C931, C932, C933.
            3. Change C934, C935, C936 from 22P to 5.6P.
            4. Change C6, C14, C350 from 10P to 5.6P.
            5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T.

PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.
            2. Reserve S-video impedance match circuit.
```

Model / Page	CT3/5 MB BOARD FROM	CT3/5 MB BOARD TO
1	1A	
2	2A	3A
3	2A	3A
4	2A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	2A	
11	2A	
12	1A	
13	1A	
14	1A	
15	2A	
16	1A	
17	2A	3A
18	2A	3A
19	2A	
20	1A	
21	1A	
22	2A	
23	2A	
24	2A	
25	1A	
26	2A	2A
27	2A	
28	1A	2A
29	1A	
30	2A	
31	2A	
32	1A	
33	2A	
34	2A	
35	2A	
36	2A	
37	2A	
38	2A	
39	2A	

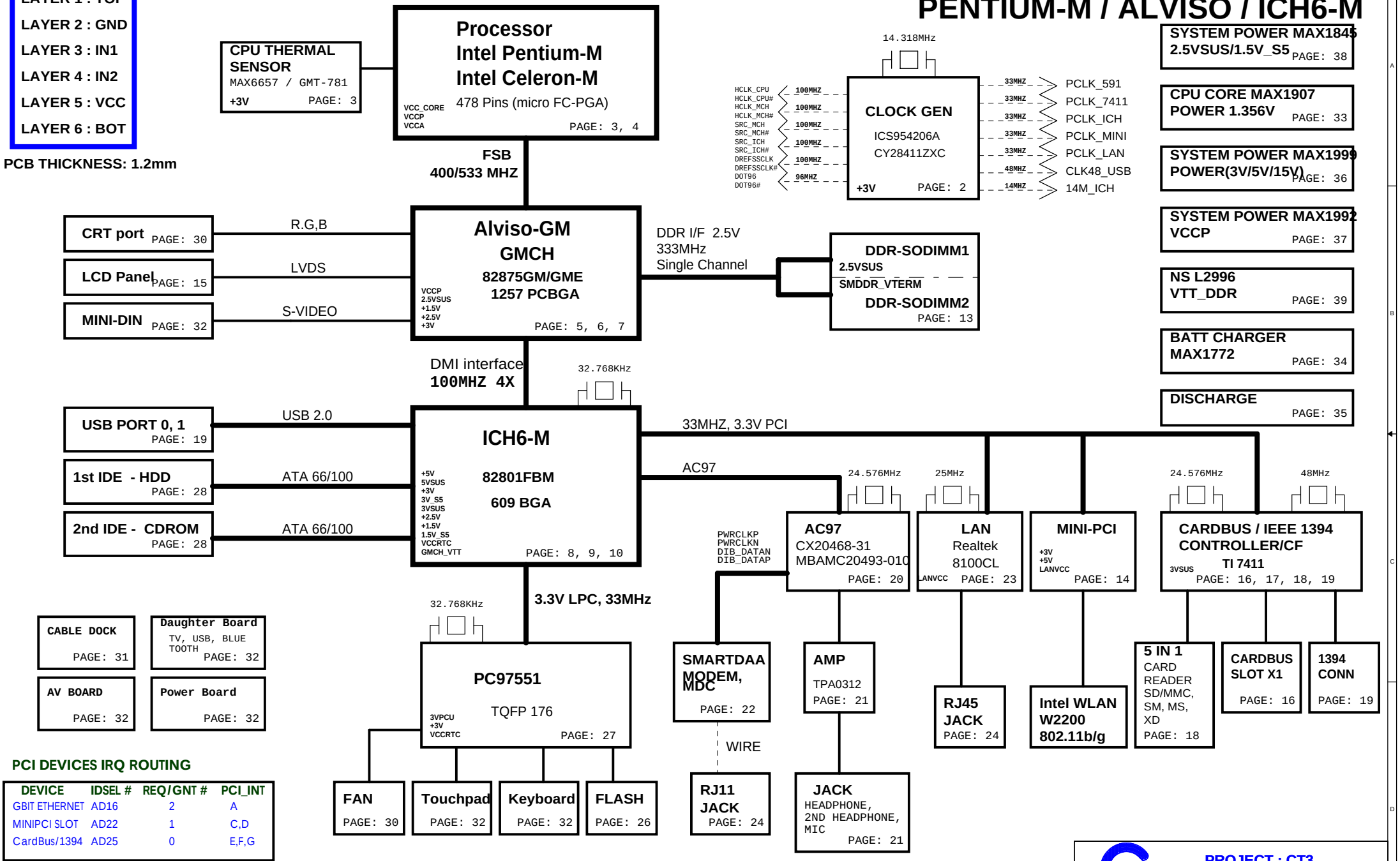
CT3 BLOCK DIAGRAM

PENTIUM-M / ALVISO / ICH6-M

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

PCB THICKNESS: 1.2mm



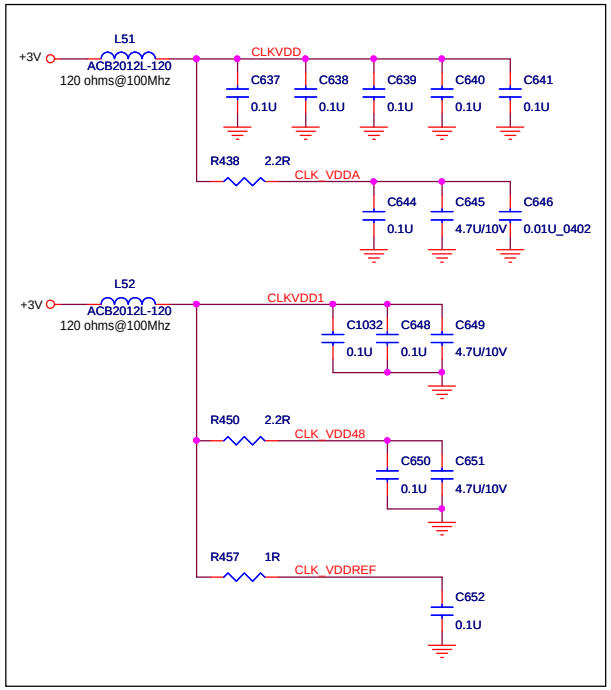
PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	2	A
MINIPCI SLOT	AD22	1	C,D
CardBus/1394	AD25	0	E,F,G

PROJECT : CT3
Quanta Computer Inc.

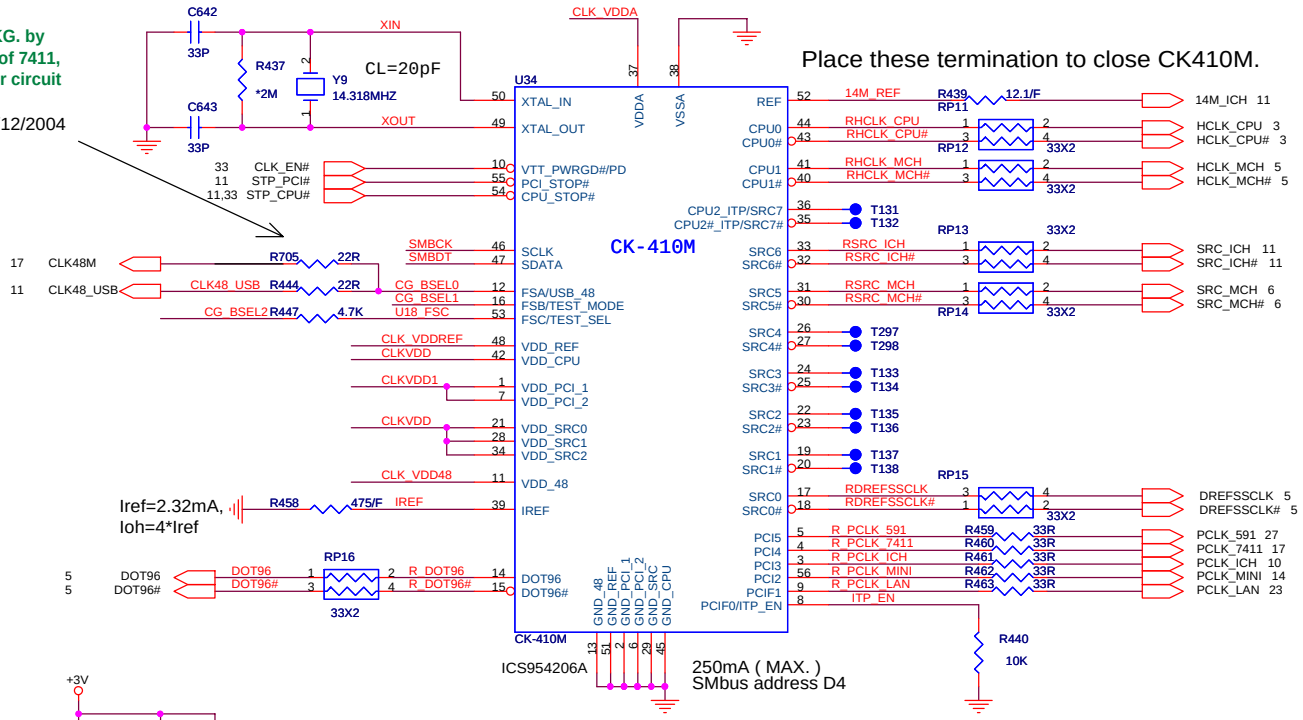
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, December 27, 2004 Sheet 1 of 39



SI stage:
Enable CLK48M from CKG. by R705 for the PLL circuit of 7411, and disable the ocsillator circuit at PCI7411 side.

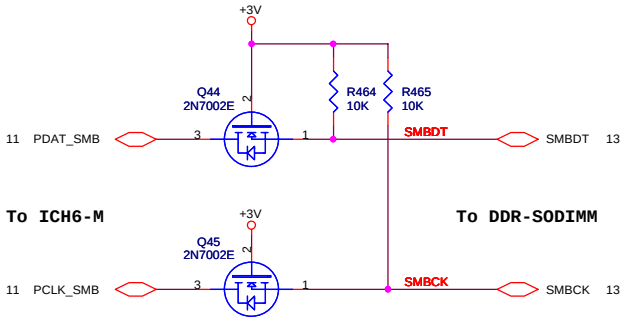
Sting 10/12/2004



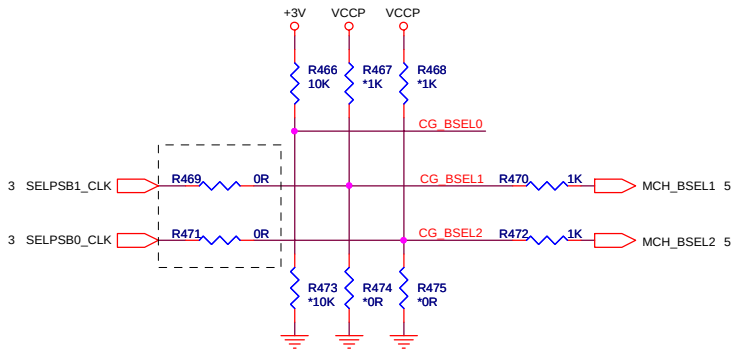
Place these termination to close CK410M.

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DOTHAN FSB 400
0	0	1	133	100	33	DOTHAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

**** Frequence select by CPU auto sense.***



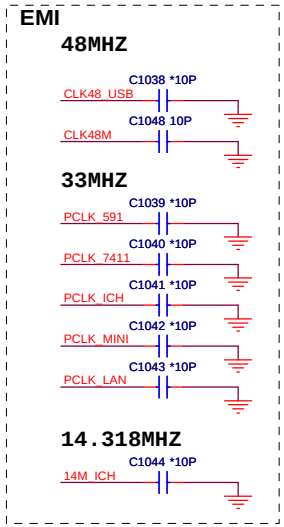
R_PCLK_LAN	ITP_EN
0: SRCCLK=96MHZ	0: SRC_7 Pair
1: SRCCLK=100MHZ	1: CPU_2 ITP Pair

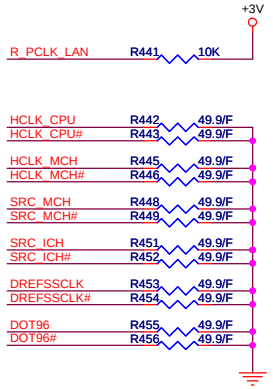


R469,R471
Dothan-A can remove so that the FSB frequency will be selected by hardware setting(R474,R475,R467,R468).
Dothan-B should be populated.

PV stage:
Add C1048 for CLK48M to get better EMI performance.

Sting 11/29/2004

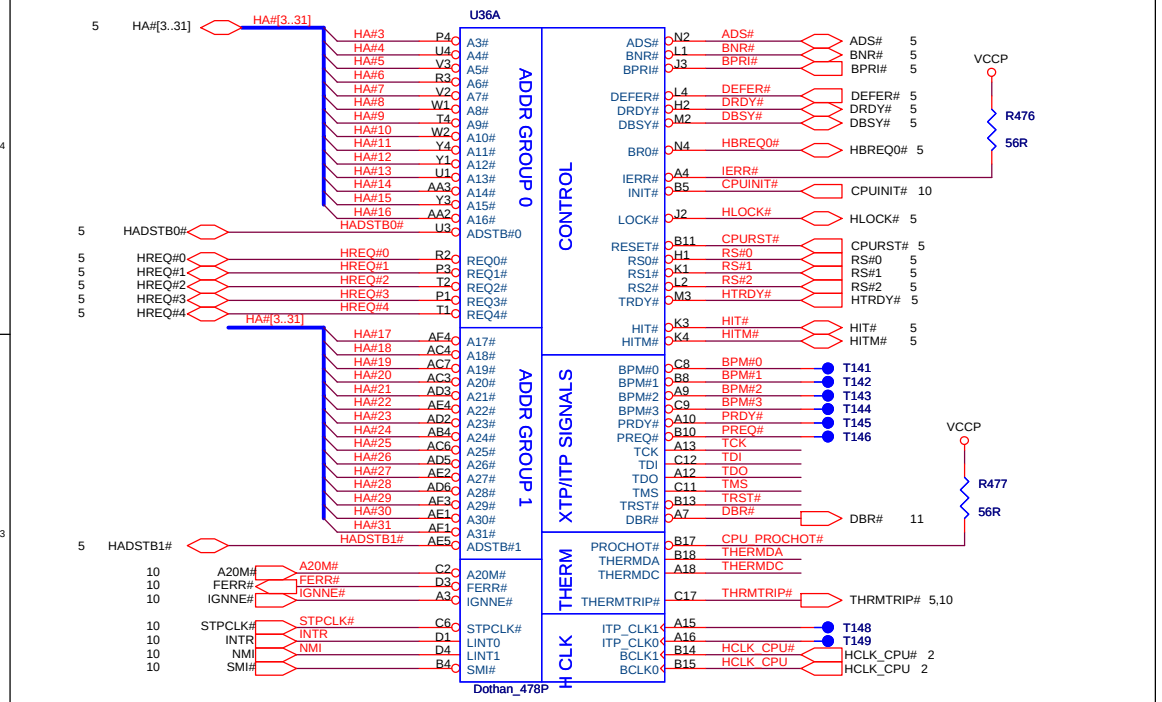


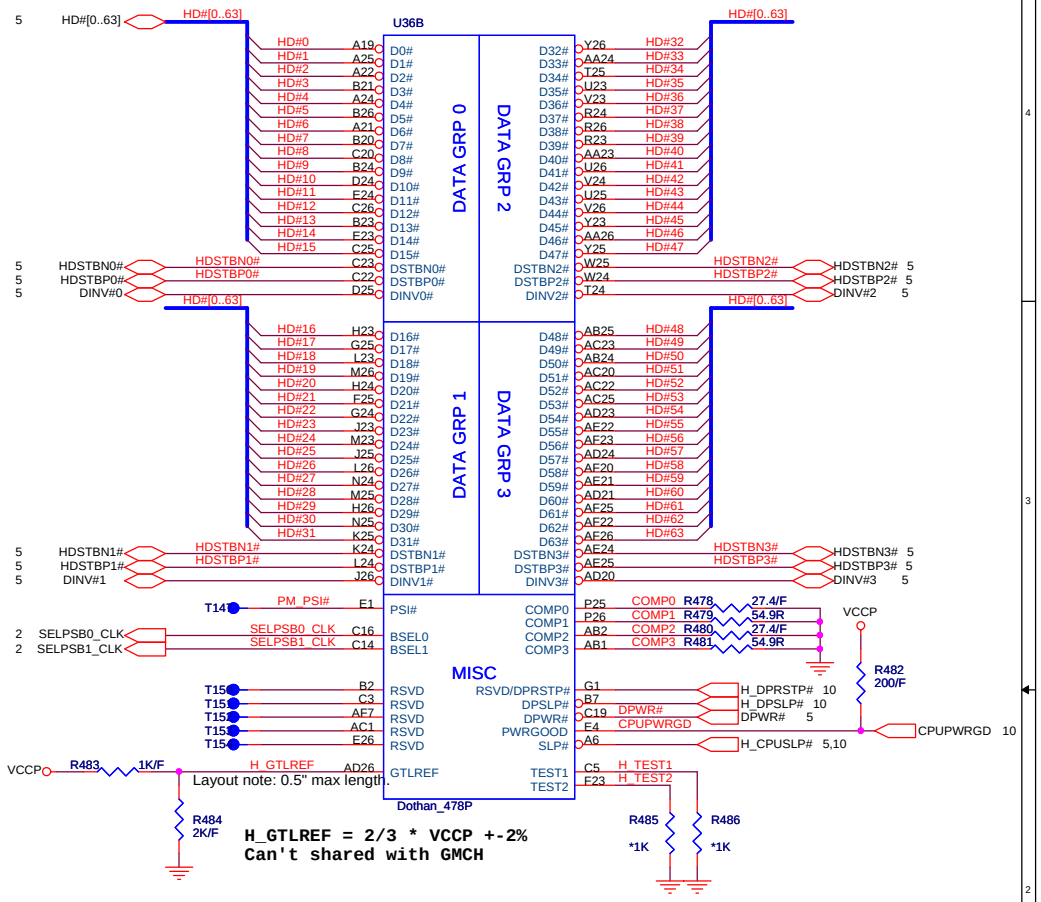


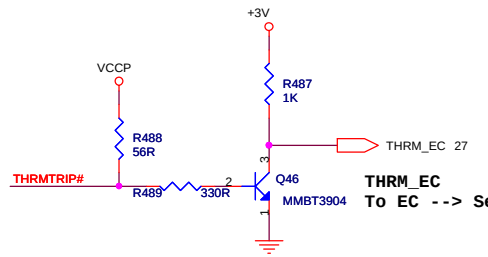
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A

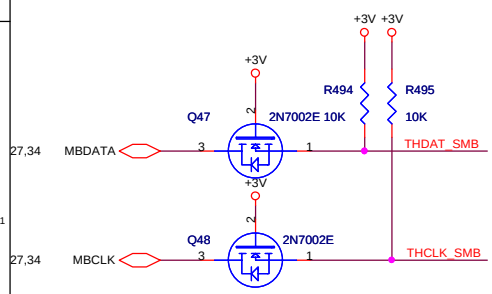
Date: Monday, December 27, 2004 Sheet 2 of 39

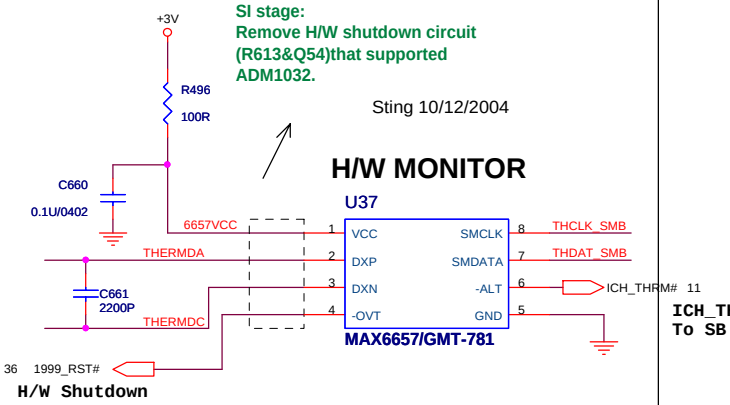






THRM_EC
To EC --> Send FANSIG to control fan.





SI stage:
Remove H/W shutdown circuit (R613&Q54)that supported ADM1032.

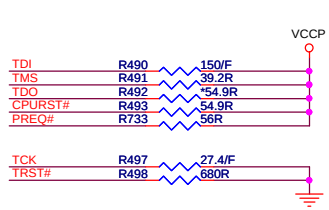
Sting 10/12/2004

H/W MONITOR

U37

H/W Shutdown

ICH_THRM#
To SB --> System throttling

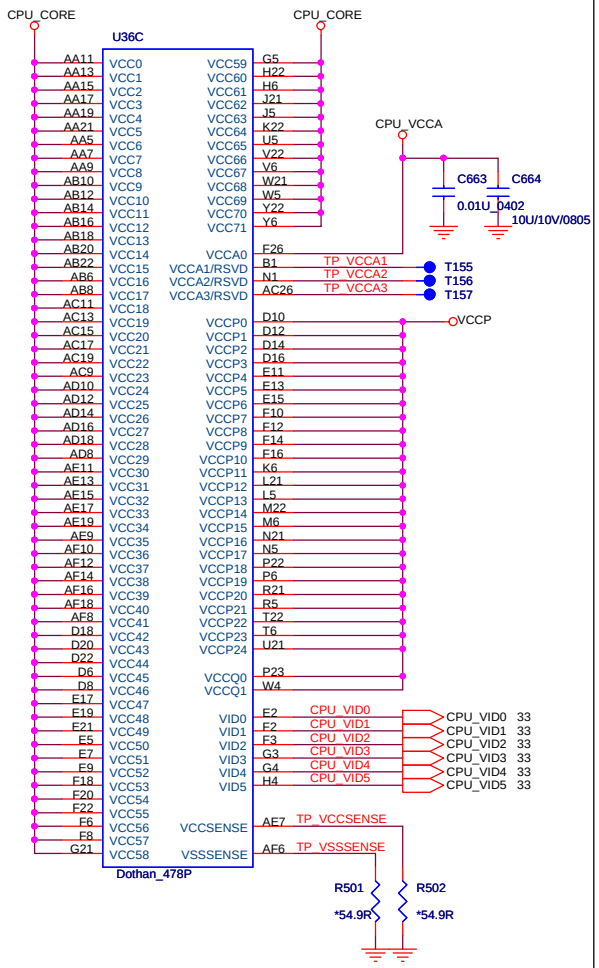


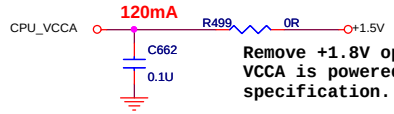
PV stage:
Add R733 as pull-up resistor for PREQ#.
Sting 11/29/2004

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dothan CPU (Host Bus)	3A

Date: Monday, December 27, 2004 Sheet 3 of 39



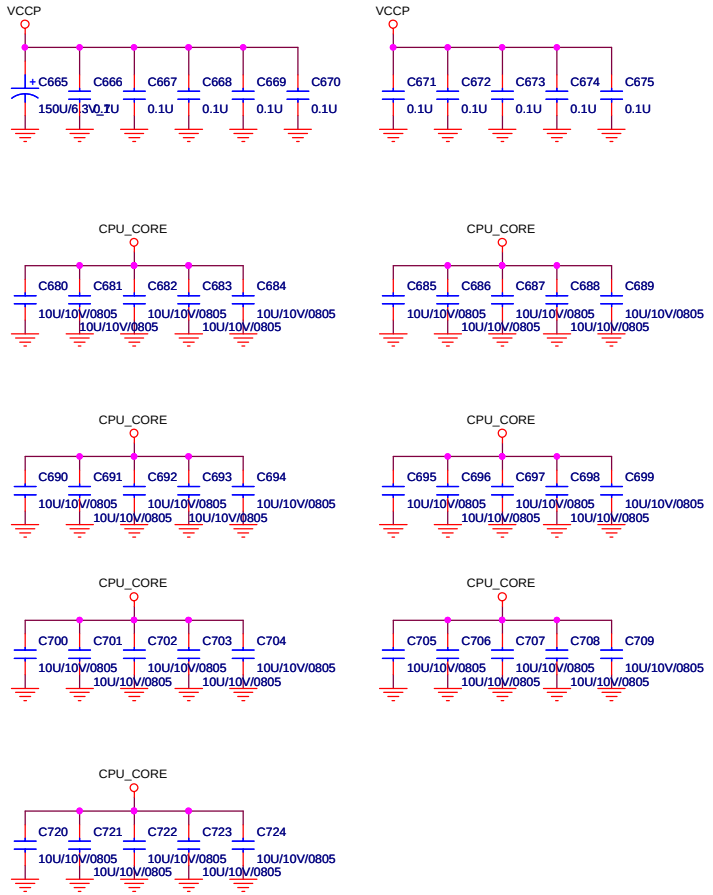


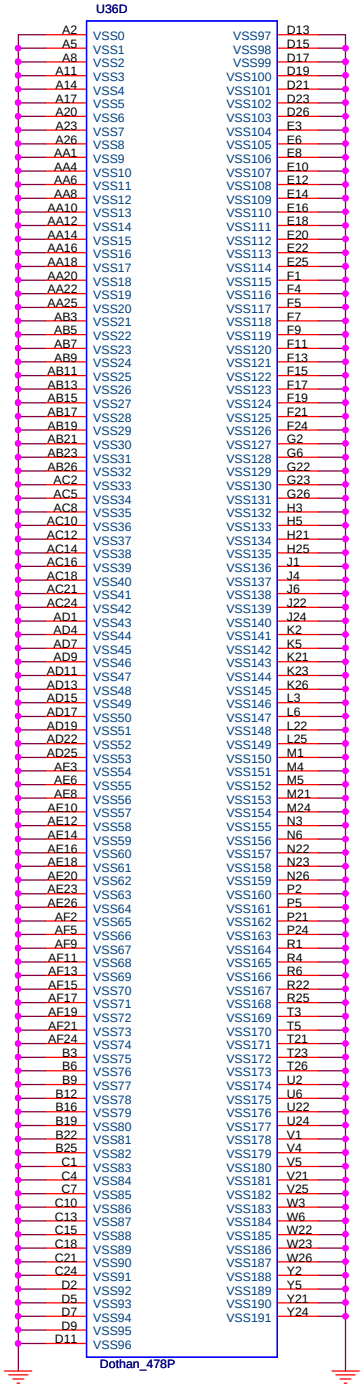
Remove +1.8V optional cause of the VCCA is powered by +1.5V in Intel specification.

Sting 08/05/2004

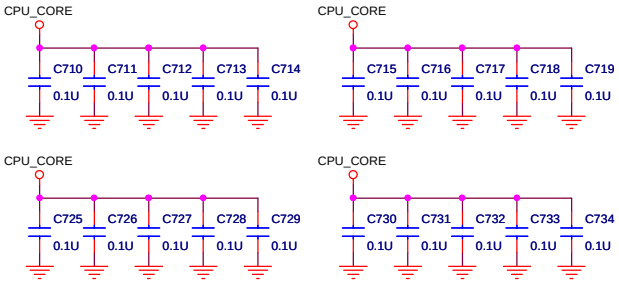
SI stage:
Use X7R type to replace Y5V type for Decoupling/Bypass capacitor.

Sting 10/12/2004





CPU de-coupling capacitor

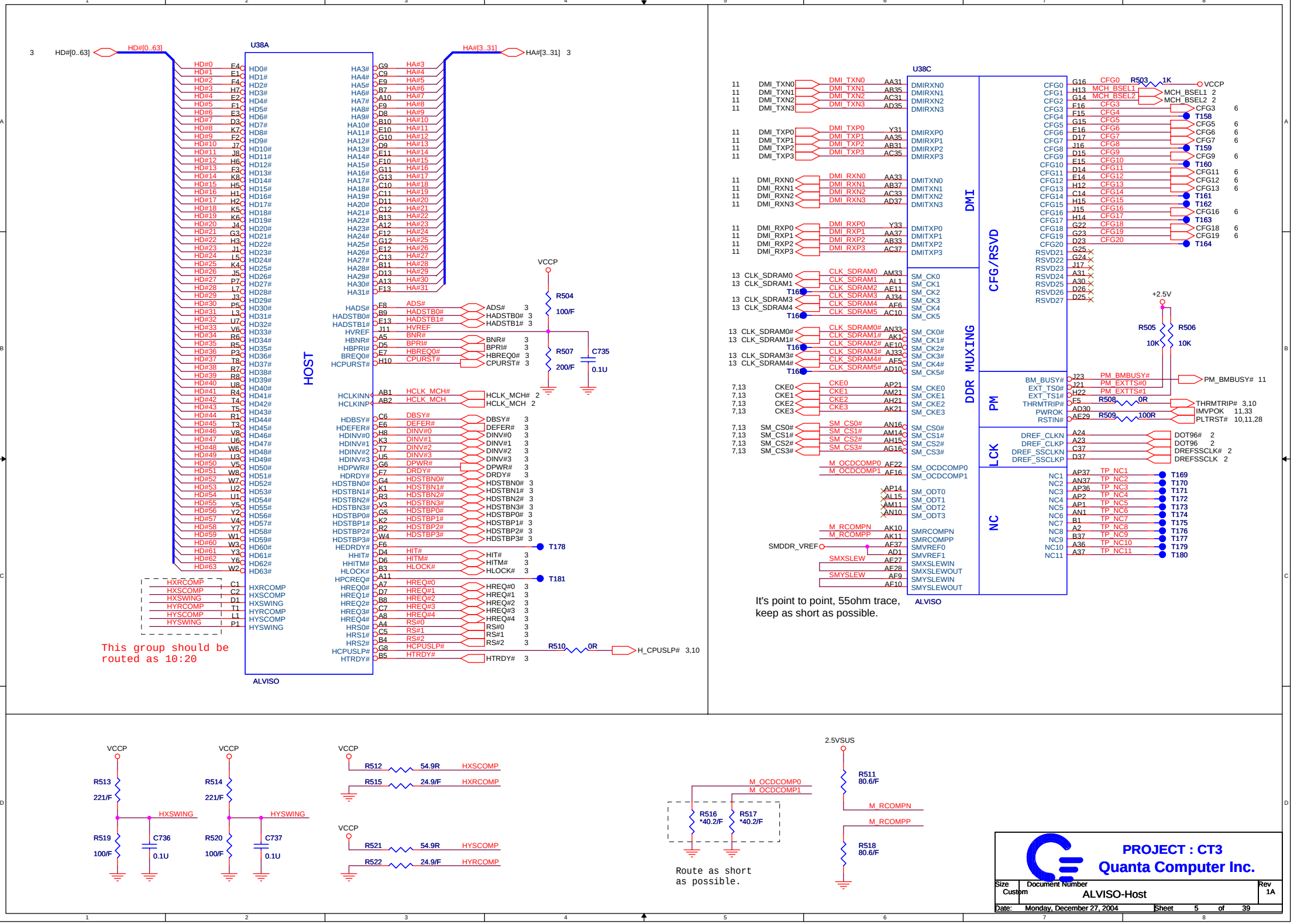


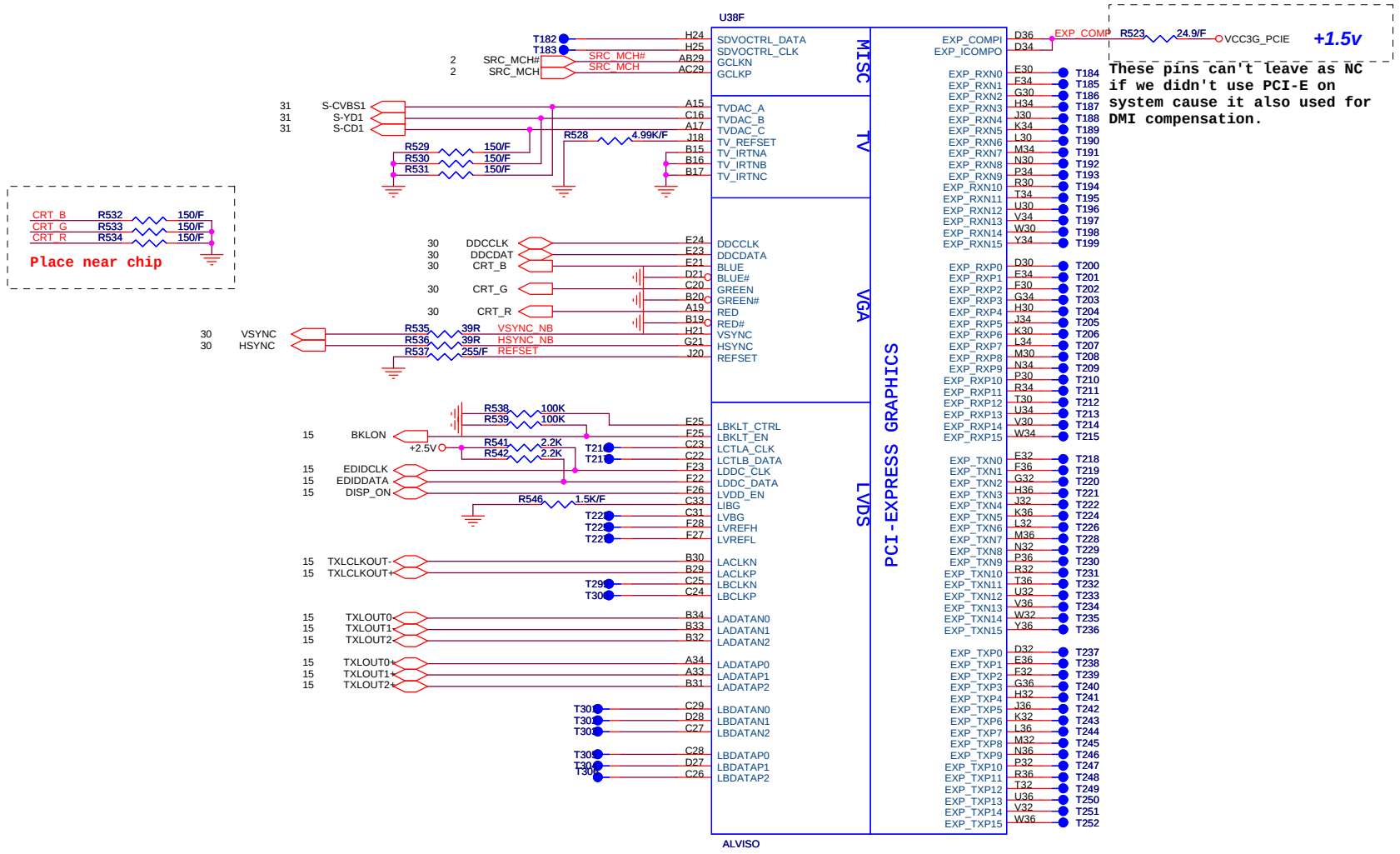
CPU Bypass capacitor

PROJECT : CT3
Quanta Computer Inc.

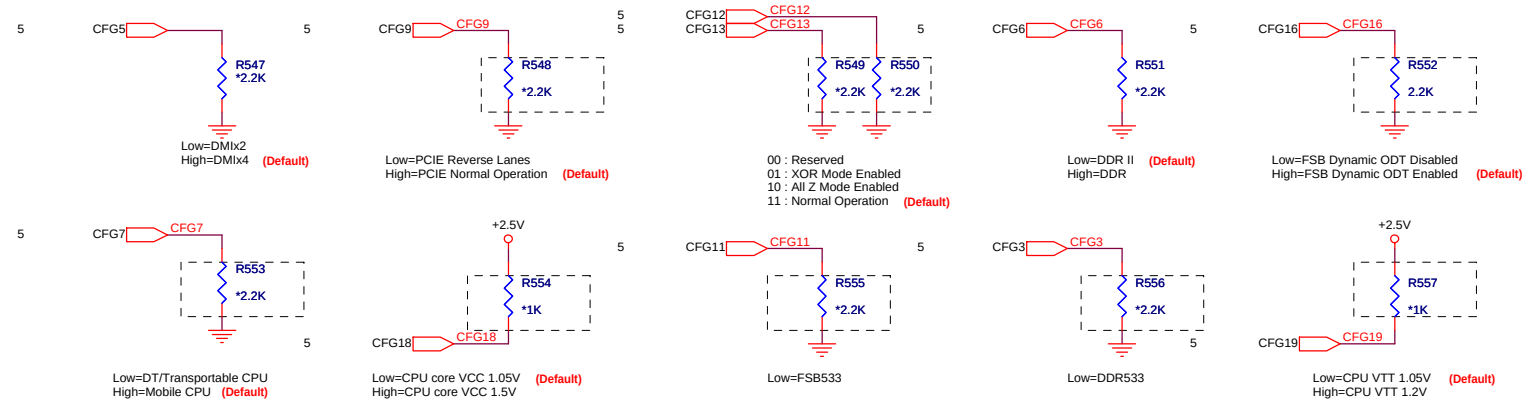
Size	Document Number	Rev
Custom	CPU POWER / GND	2A

Date: Monday, December 27, 2004 Sheet 4 of 39


U38A
HOST
ALVISO
HD#[0..63]
HA#[3..31]
HXRCOMP
HXSCOMP
HXSWING
HYRCOMP
HYSCOMP
HYSWING
This group should be routed as 10:20
VCCP
R504
100/F
R507
200/F
C735
0.1U
T178
T181
R510
0R
H_CPUSLP# 3,10
U38C
DMI
DDR MUXING
CFG/RSVD
PM
LCK
NC
R503
1K
MCH_BSEL1
MCH_BSEL2
R505
10K
R506
10K
+2.5V
PM_BMBUSY# 11
R508
0R
R509
100R
THRMTRIP# 3,10
IMVPOK 11,33
PLTRST# 10,11,28
DOT96# 2
DREFSSCLK# 2
SMDDR_VREF
It's point to point, 55ohm trace, keep as short as possible.
R513
221/F
R519
100/F
C736
0.1U
HXSWING
R514
221/F
R520
100/F
C737
0.1U
HYSWING
R512
54.9R
HXSCOMP
R515
24.9/F
HXRCOMP
R521
54.9R
HYSCOMP
R522
24.9/F
HYRCOMP
M_OCDCOMP0
M_OCDCOMP1
R516
*40.2/F
R517
*40.2/F
Route as short as possible.
2.5VSUS
R511
80.6/F
M_RCOMPN
M_RCOMPP
R518
80.6/F
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number
ALVISO-Host
Rev 1A
Date: Monday, December 27, 2004
Sheet 5 of 39



Strapping



CFG[2:0]
001=533MT/S FSB
101=400MT/S FSB

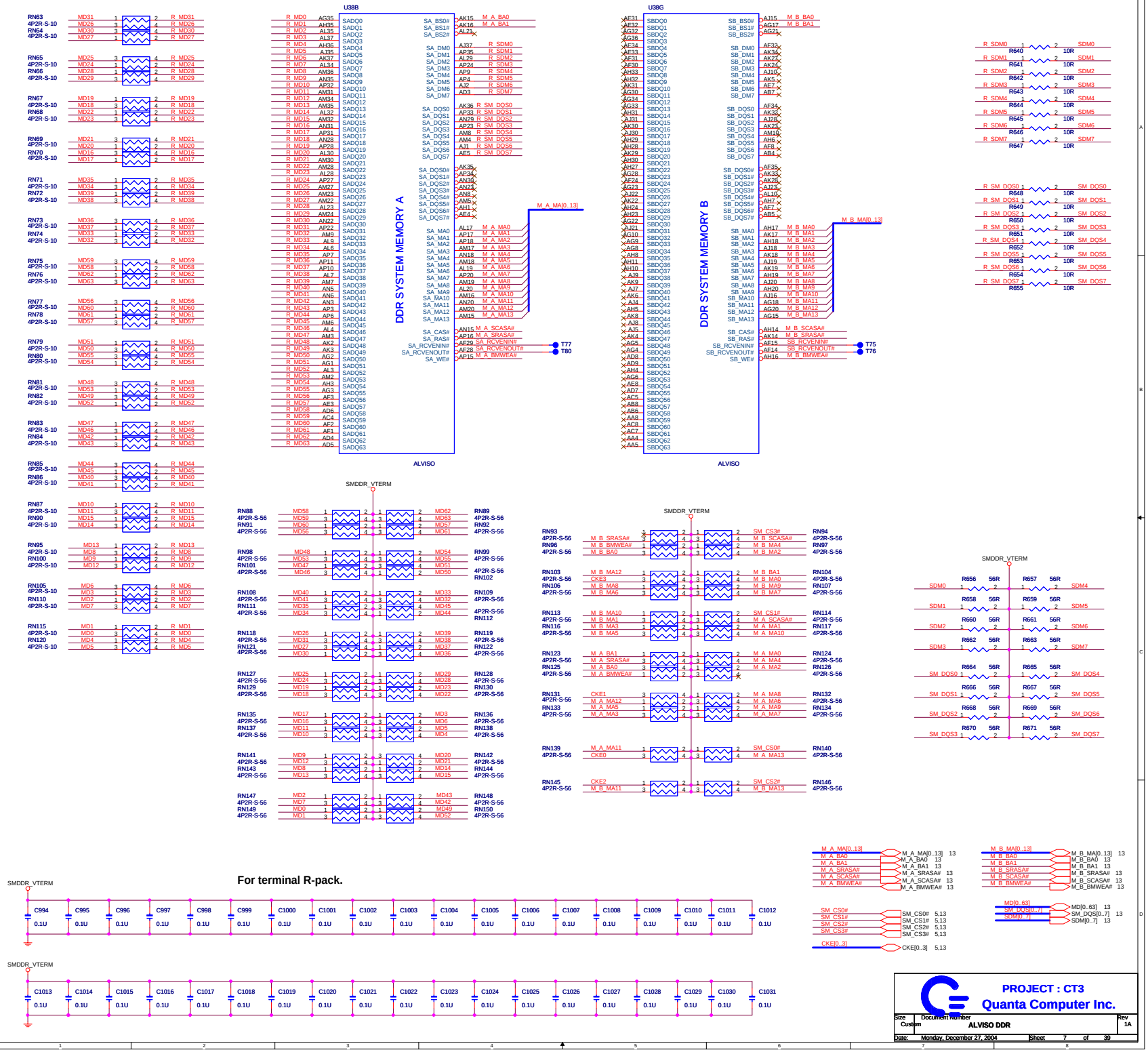
CFG[3:17] have internal pullup.

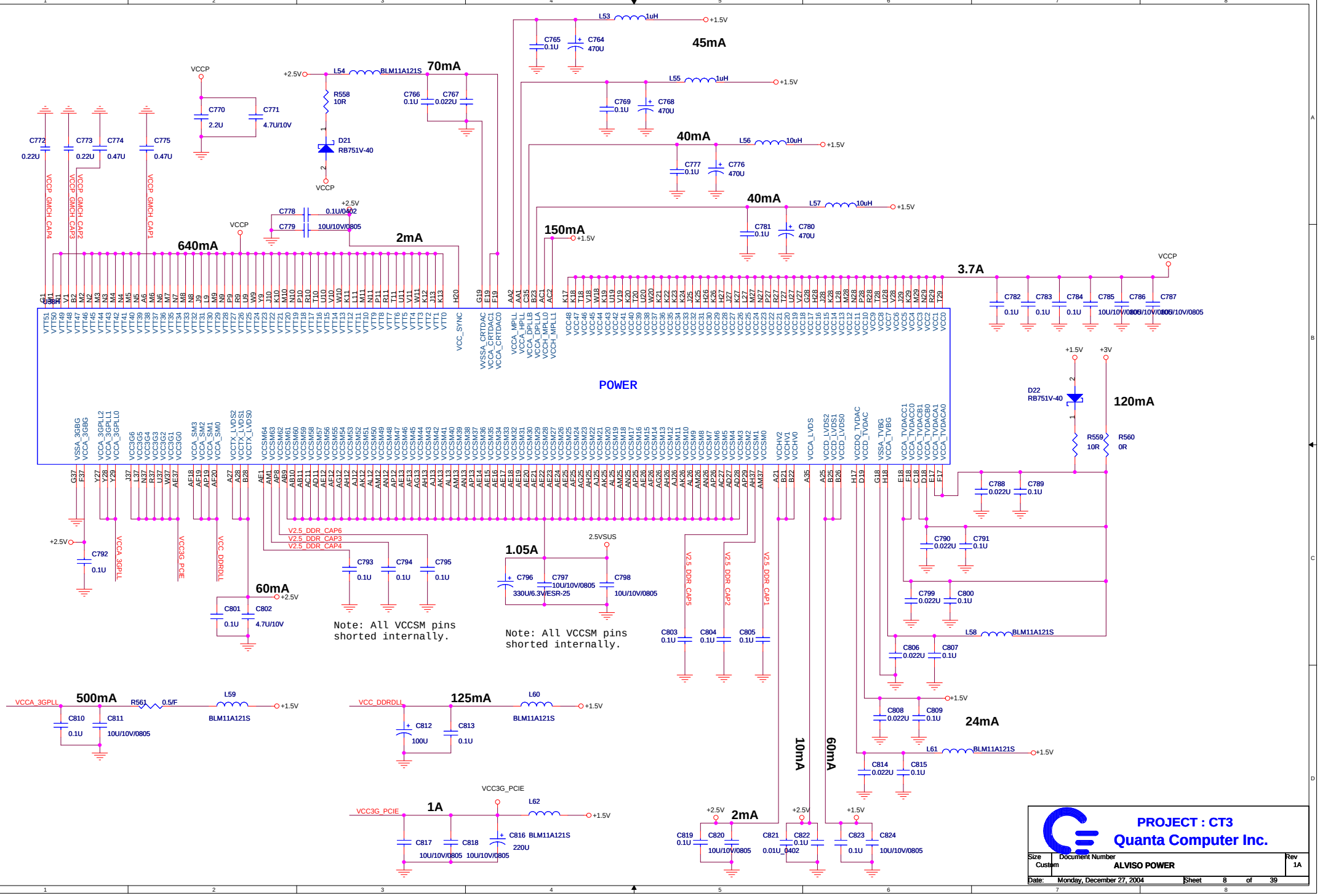
CFG[18:19] have internal pulldown.

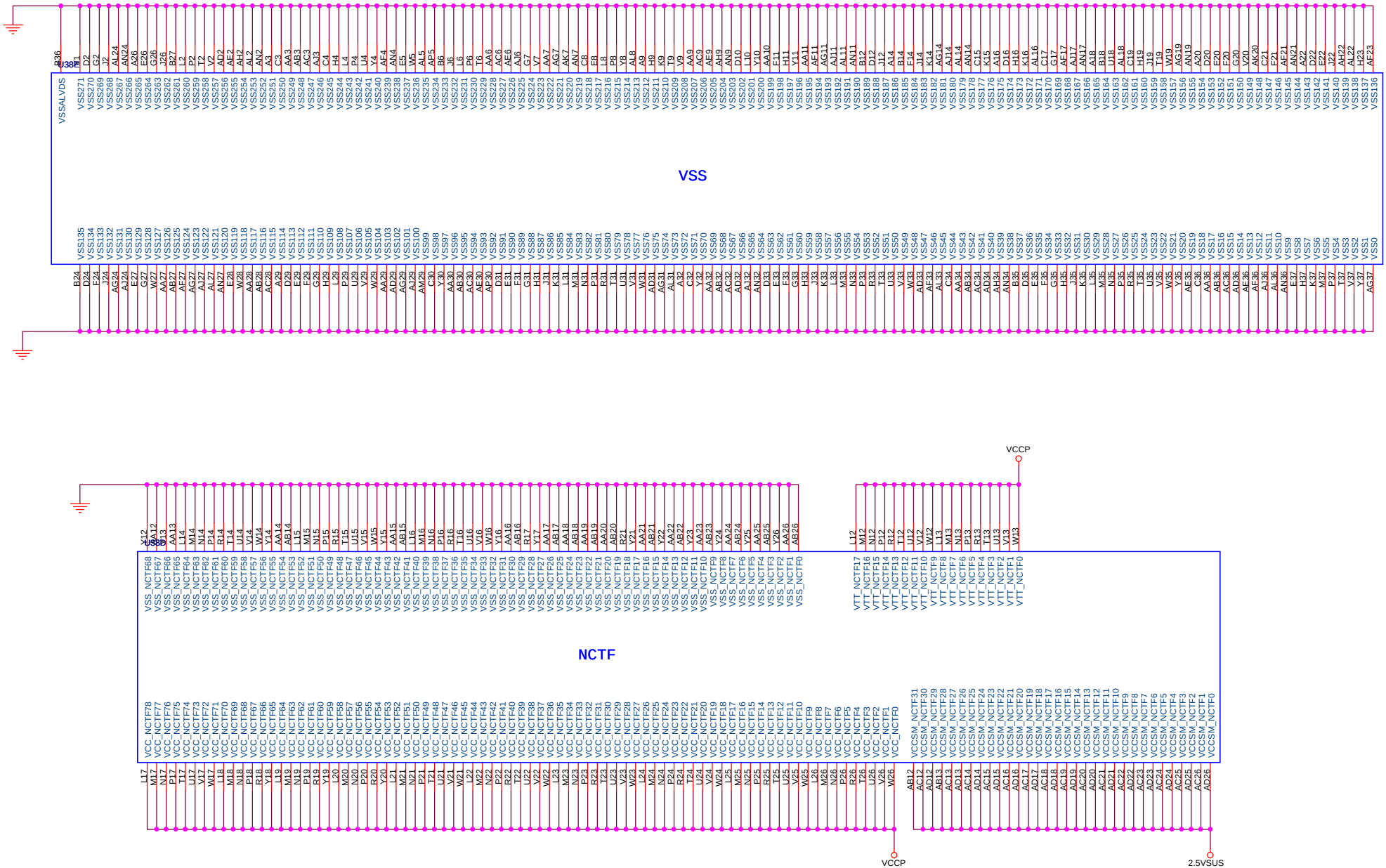
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALVISO DMI	1A

Date: Monday, December 27, 2004 Sheet 6 of 39


U38B
DDR SYSTEM MEMORY A
ALVISO
U38G
DDR SYSTEM MEMORY B
ALVISO
M_A_MA[0..13]
M_B_MA[0..13]
T77
T80
T75
T76
SMDDR_VTERM
For terminal R-pack.
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number ALVISO DDR
Rev 1A
Date: Monday, December 27, 2004
Sheet 7 of 39


POWER
45mA
40mA
40mA
150mA
3.7A
120mA
70mA
640mA
2mA
60mA
1.05A
500mA
125mA
1A
10mA
60mA
24mA
2mA
L53 1uH
L55 1uH
L56 10uH
L57 10uH
L54 BLM11A121S
L58 BLM11A121S
L59 BLM11A121S
L60 BLM11A121S
L61 BLM11A121S
L62 BLM11A121S
D21 RB751V-40
D22 RB751V-40
R558 10R
R559 10R
R560 0R
R561 0.5/F
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number ALVISO POWER
Rev 1A
Date: Monday, December 27, 2004
Sheet 8 of 39

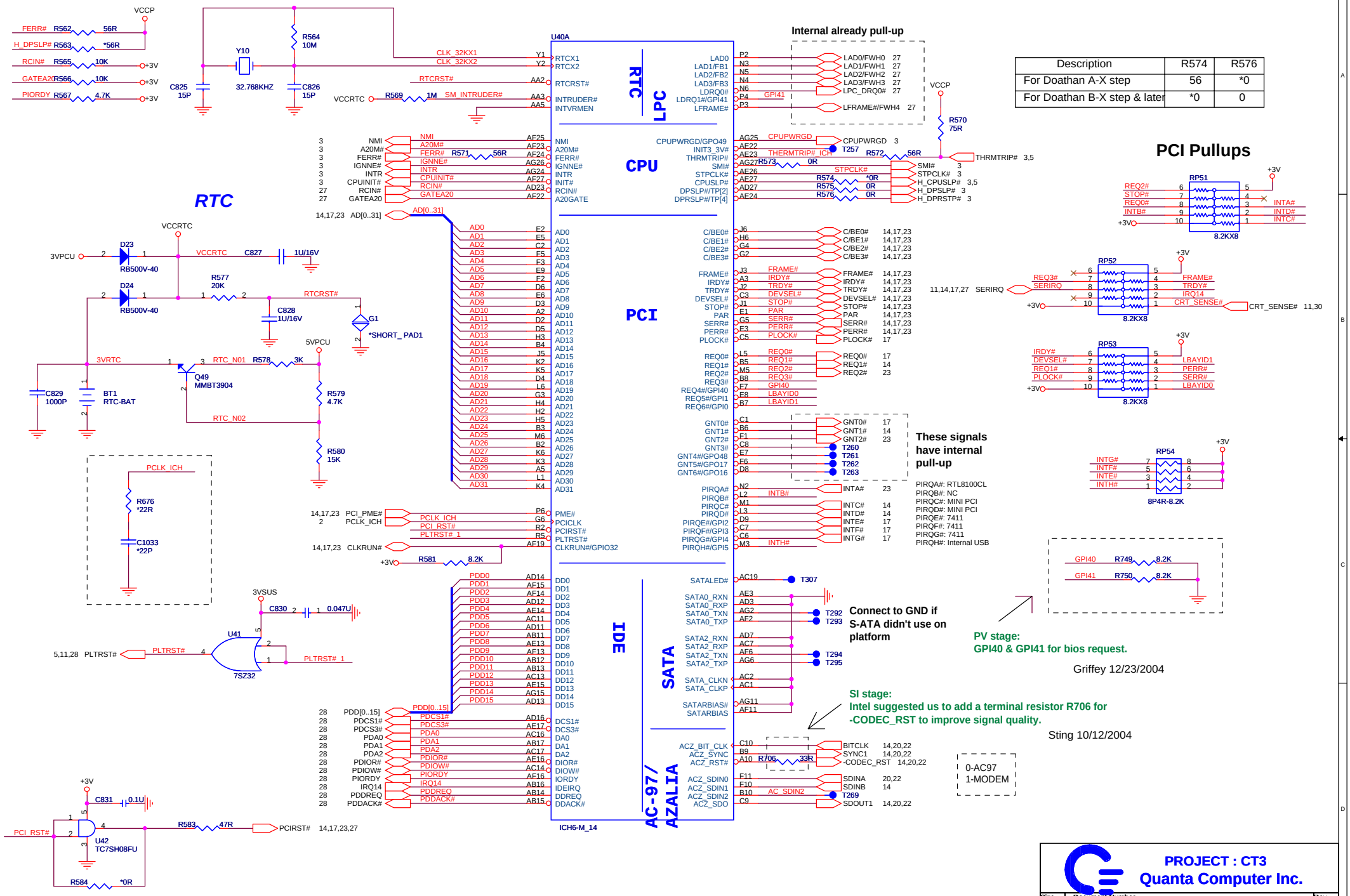


PROJECT : CT3

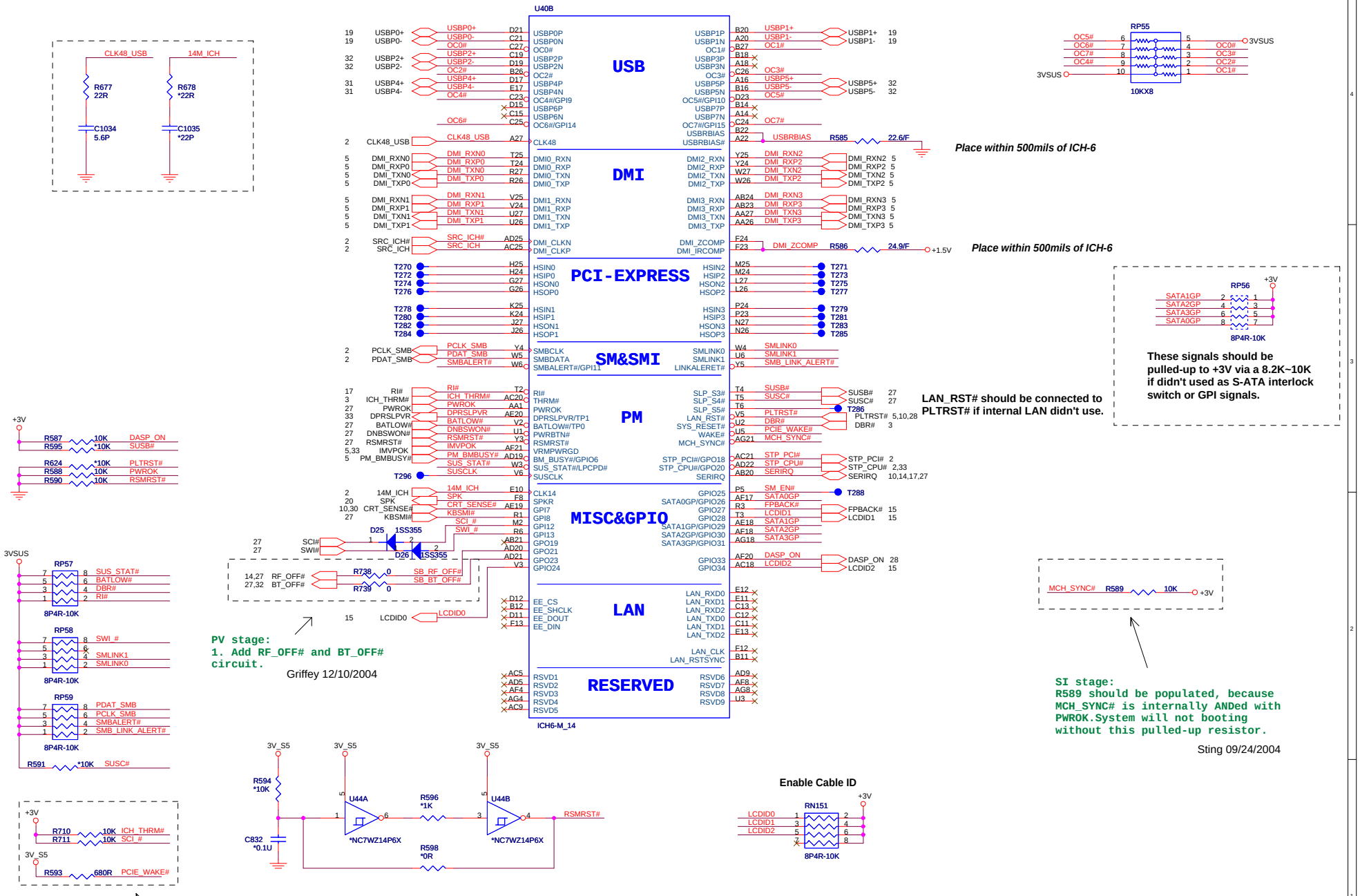
Quanta Computer Inc.

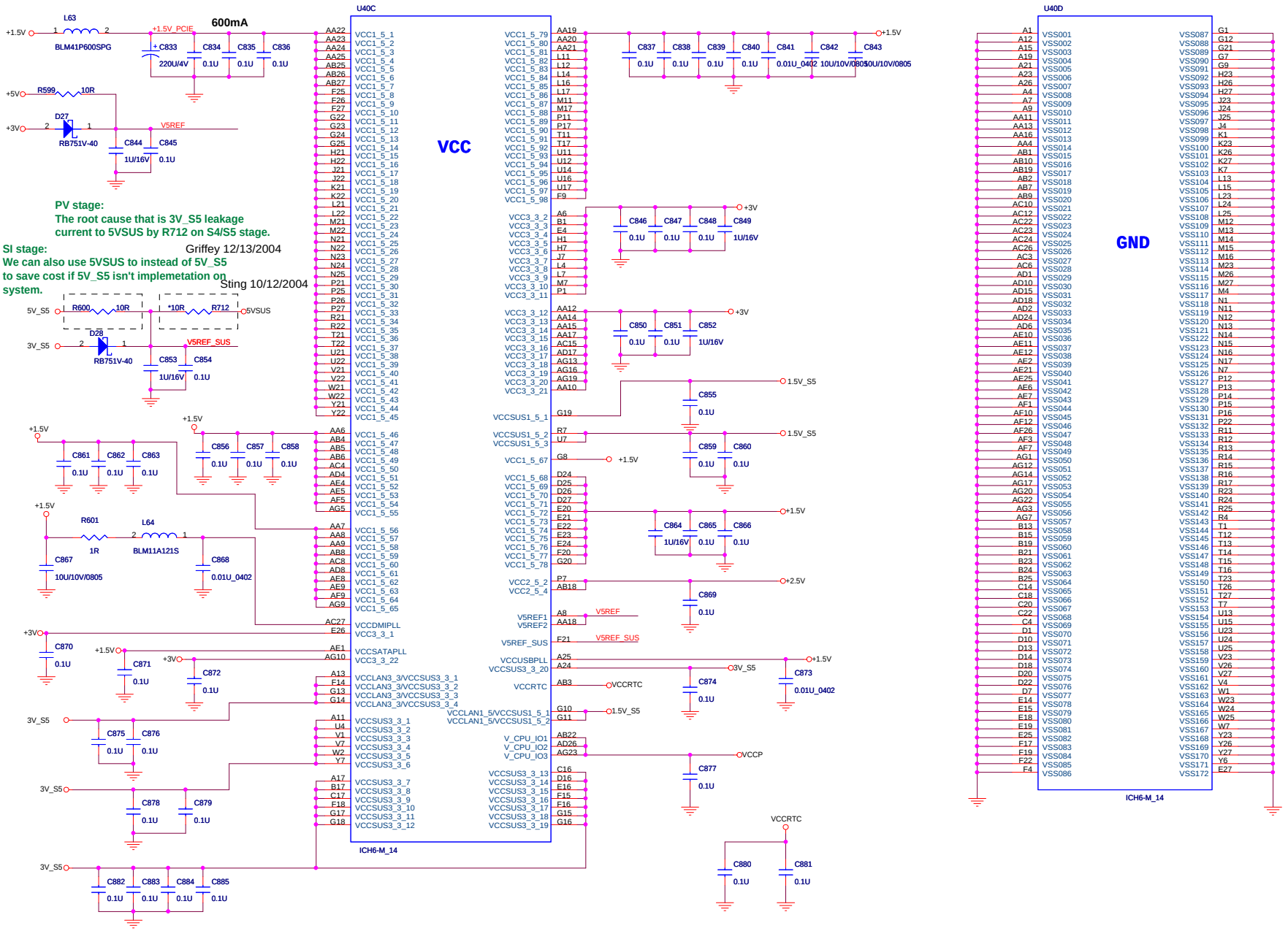
Size	Document Number	Rev
Custom	ALVISO VSS/NCTF	1A

Date: Monday, December 27, 2004 Sheet 9 of 39



Description	R574	R576
For Doathan A-X step	56	*0
For Doathan B-X step & later	*0	0


U40B
USB
DMI
PCI-EXPRESS
SM&SMI
PM
MISC&GPIO
LAN
RESERVED
ICH6-M_14
CLK48_USB
14M_ICH
R677 22R
R678 *22R
C1034 5.6P
C1035 *22P
R585 22.6/F
Place within 500mils of ICH-6
R586 24.9/F
+1.5V
RP55
10KX8
3VSUS
RP56
8P4R-10K
These signals should be pulled-up to +3V via a 8.2K~10K if didn't used as S-ATA interlock switch or GPI signals.
LAN_RST# should be connected to PLTRST# if internal LAN didn't use.
R587 10K DASP_ON
R595 *10K SUSB#
R624 *10K PLTRST#
R588 10K PWROK
R590 10K RSMRST#
RP57
RP58
RP59
R591 *10K SUSC#
D25 1SS355
D26 1SS355
R738 0
R739 0
SB_RF_OFF#
SB_BT_OFF#
LCDID0
R589 10K
MCH_SYNC#
PV stage:
1. Add RF_OFF# and BT_OFF# circuit.
Griffey 12/10/2004
SI stage:
R589 should be populated, because MCH_SYNC# is internally ANDed with PWROK.System will not booting without this pulled-up resistor.
Sting 09/24/2004
R594 *10K
C832 *0.1U
U44A
U44B
R596 *1K
R598 *0R
*NC7WZ14P6X
RSMRST#
Enable Cable ID
RN151
R710 10K ICH_THRM#
R711 10K SCI_#
R593 680R PCIE_WAKE#
1. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue.
2. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to solve leakage issue.
Sting 10/06/2004
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number ICH6-M (USB/HUB/LPC)
Rev 2A
Date: Monday, December 27, 2004
Sheet 11 of 39



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6-M (POWER)	2A

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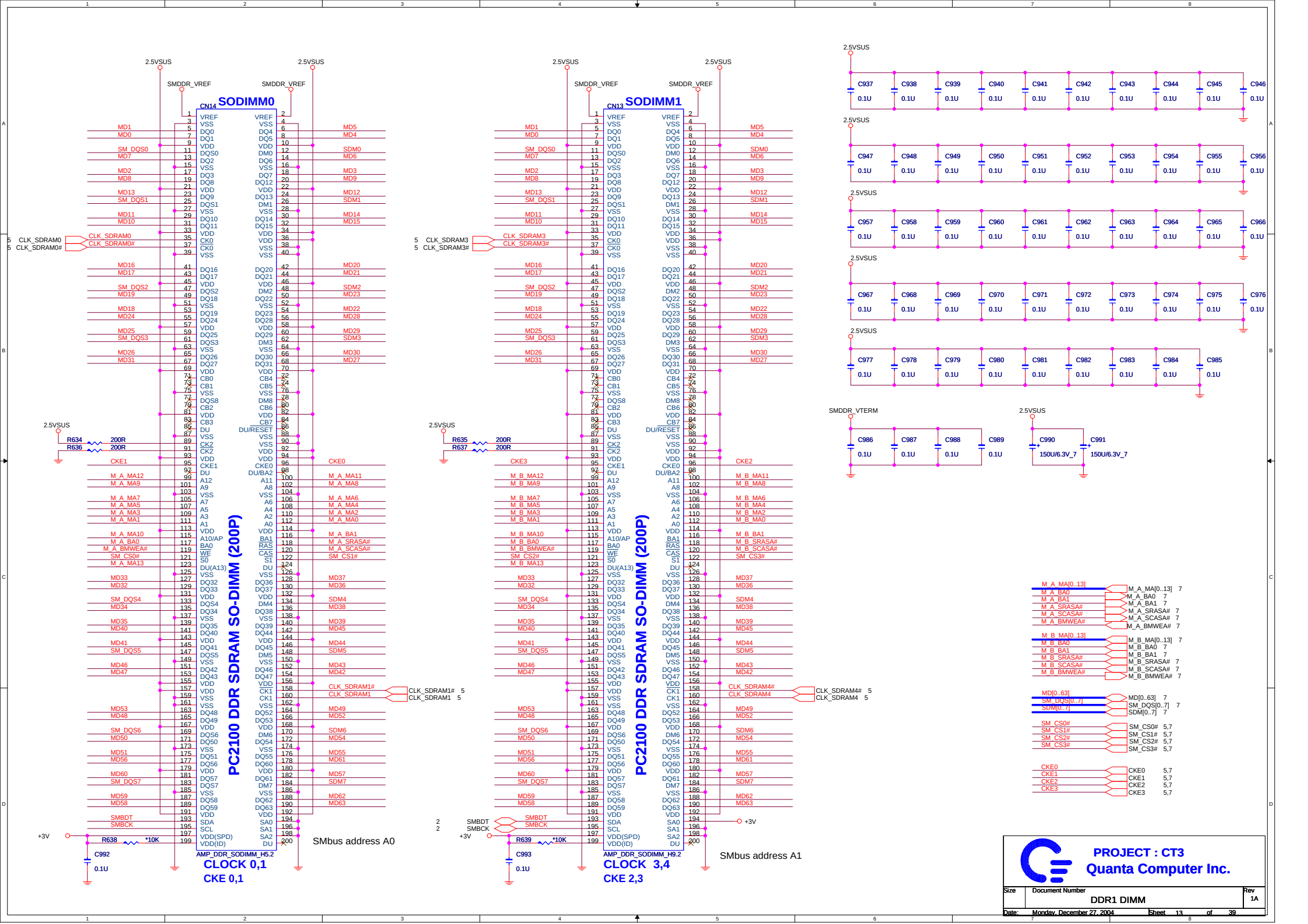
SODIMM0
CN14
PC2100 DDR SDRAM SO-DIMM (200P)
AMP_DDR_SODIMM_H5.2
CLOCK 0,1
CKE 0,1
SMbus address A0
SODIMM1
CN13
PC2100 DDR SDRAM SO-DIMM (200P)
AMP_DDR_SODIMM_H9.2
CLOCK 3,4
CKE 2,3
SMbus address A1
2.5VSUS
SMDDR_VREF
SMDDR_VTERM
+3V
R634 200R
R636 200R
R635 200R
R637 200R
R638 *10K
R639 *10K
C992 0.1U
C993 0.1U
C937 C938 C939 C940 C941 C942 C943 C944 C945 C946 0.1U
C947 C948 C949 C950 C951 C952 C953 C954 C955 C956 0.1U
C957 C958 C959 C960 C961 C962 C963 C964 C965 C966 0.1U
C967 C968 C969 C970 C971 C972 C973 C974 C975 C976 0.1U
C977 C978 C979 C980 C981 C982 C983 C984 C985 0.1U
C986 C987 C988 C989 0.1U
C990 150U/6.3V_7
C991 150U/6.3V_7
M_A_MA[0..13]
M_B_MA[0..13]
MD[0..63]
SM_DQS[0..7]
SDM[0..7]
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
CKE0
CKE1
CKE2
CKE3
PROJECT : CT3
Quanta Computer Inc.
Size
Document Number
DDR1 DIMM
Rev
1A
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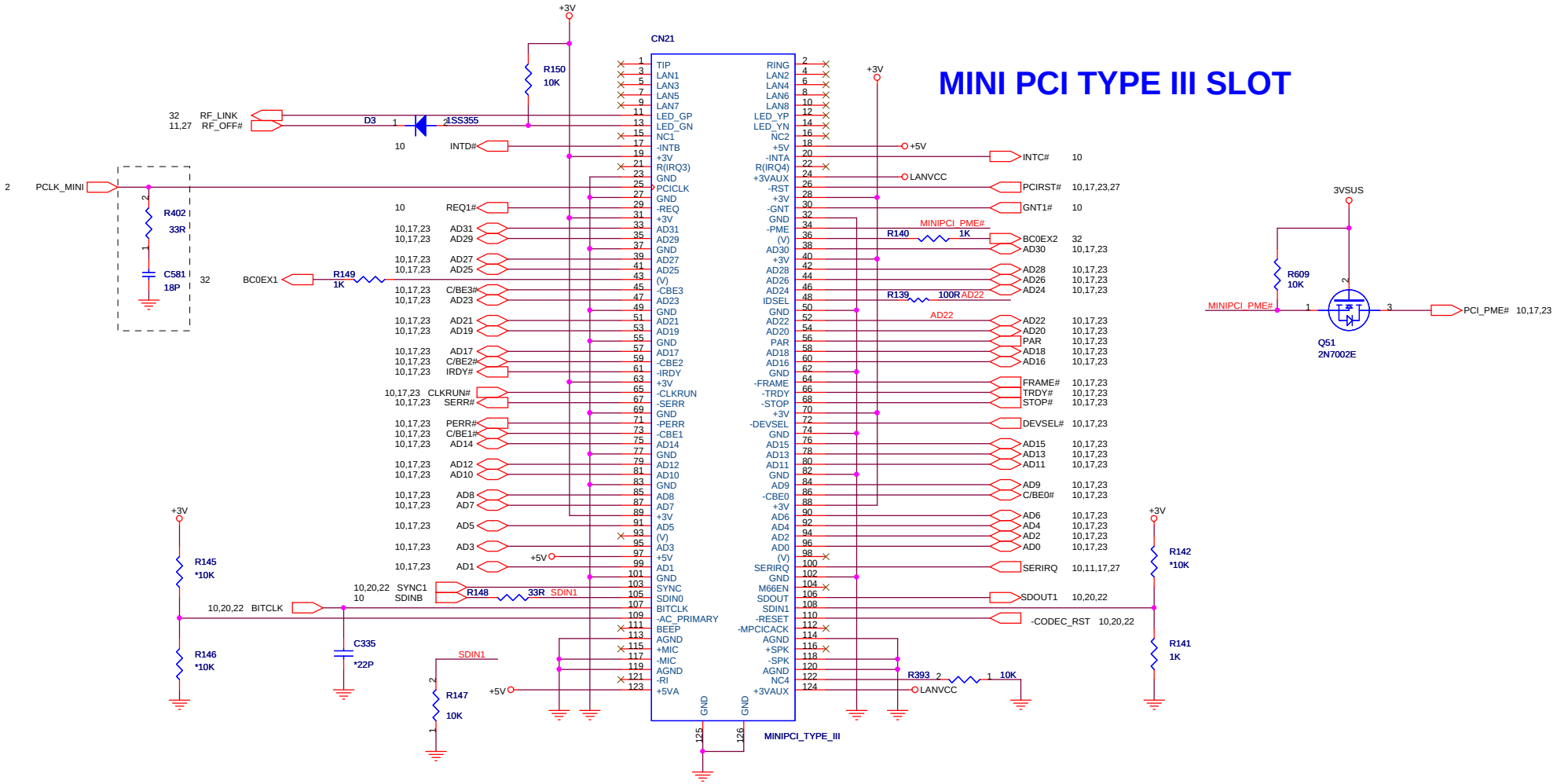
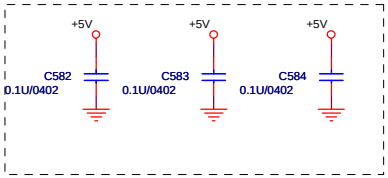
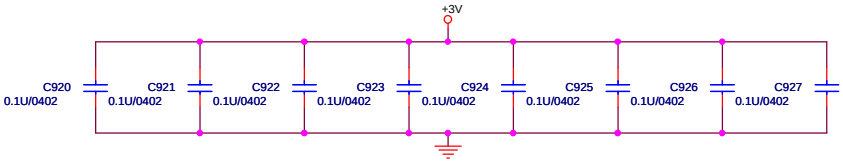
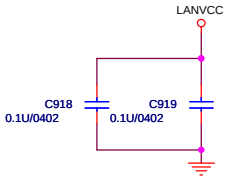
MINI PCI TYPE III SLOT









PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINIPCI_TYPE_III	1A

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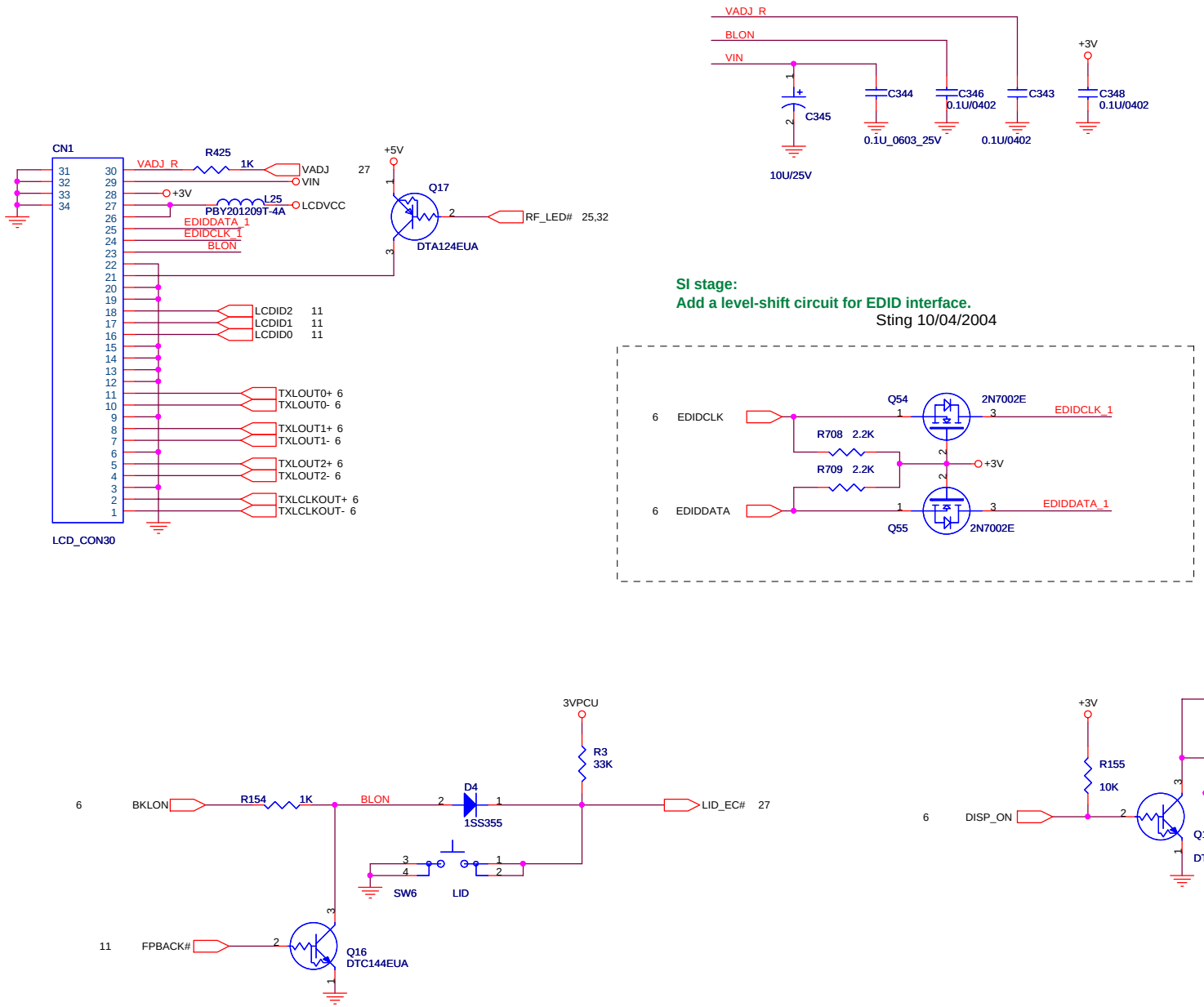

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	2A
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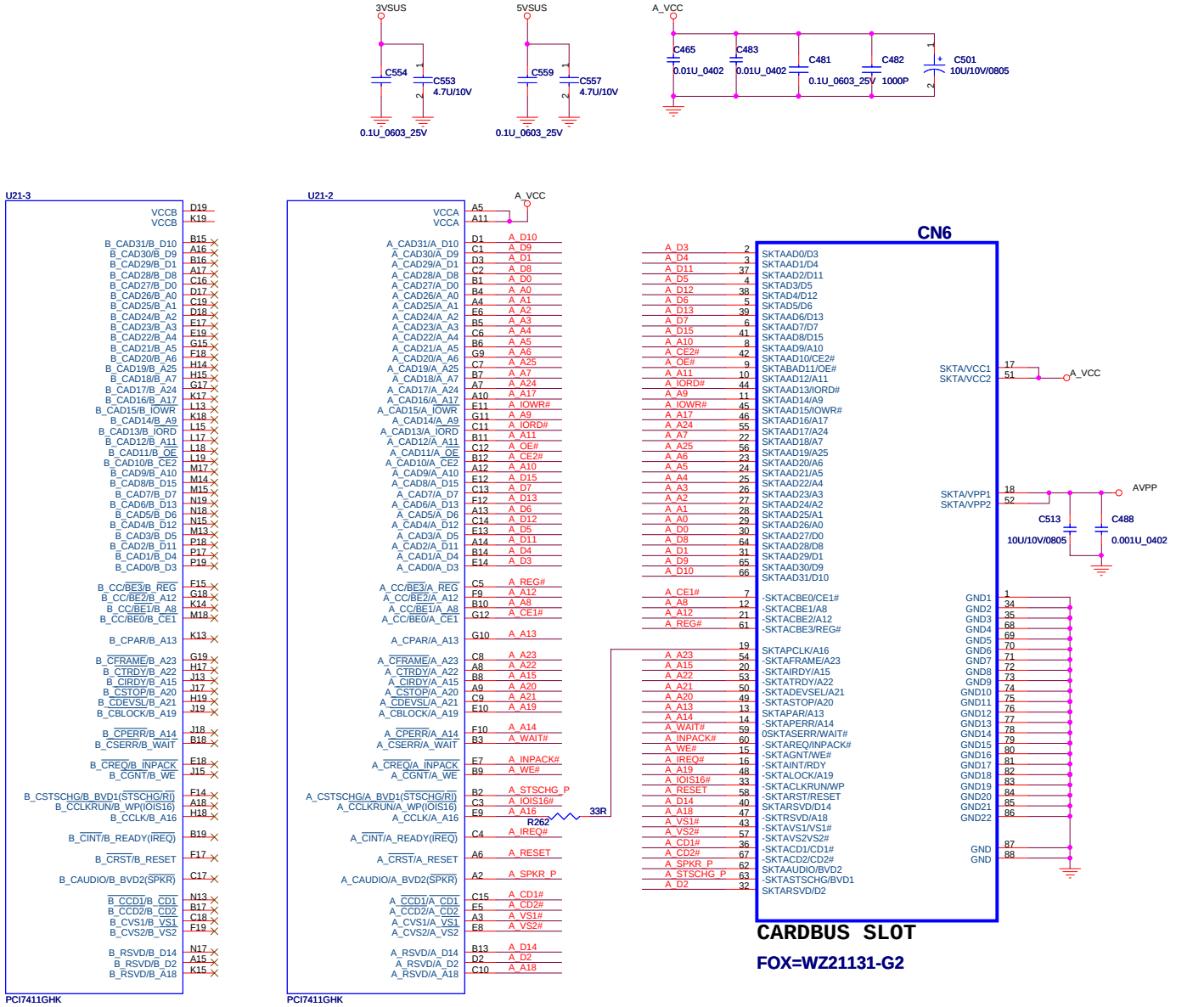
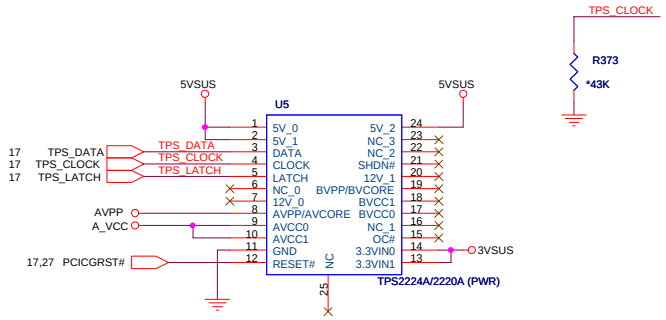
CardBus Connector



CARDBUS POWER SWITCH

For PCI7411



For PCI1510

PV stage:
Remove unused PCI1510RVGF circuit.

Griffey 12/08/2004

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	CardBus Connector	1A

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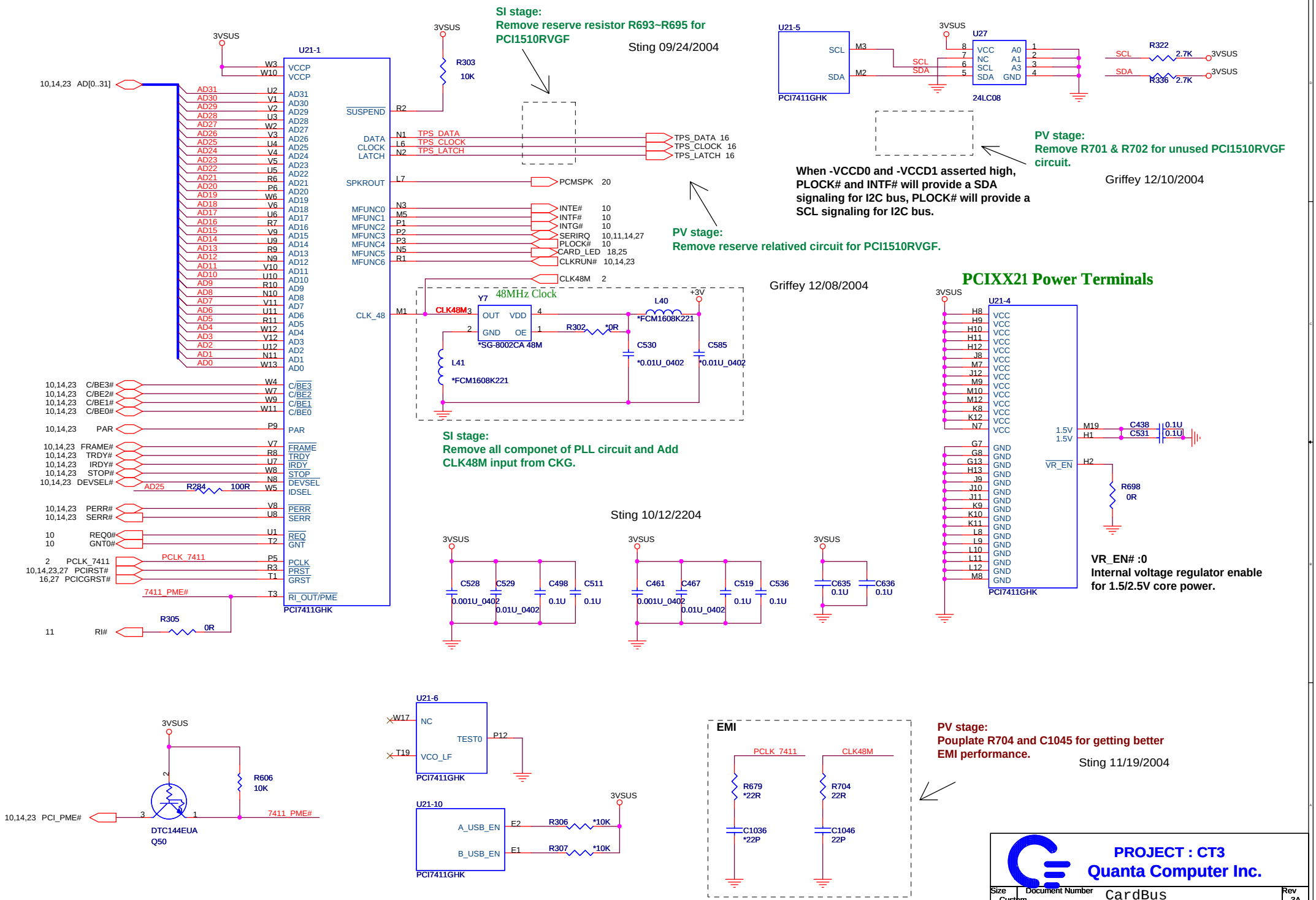
CardBus


SI stage:
Remove reserve resistor R693~R695 for PCI1510RVGF
Sting 09/24/2004
U21-1
PCI7411GHK
3VSUS
R303 10K
10,14,23 AD[0..31]
SUSPEND
DATA
CLOCK
LATCH
TPS_DATA 16
TPS_CLOCK 16
TPS_LATCH 16
SPKROUT
PCMSPK 20
MFUNC0
MFUNC1
MFUNC2
MFUNC3
MFUNC4
MFUNC5
MFUNC6
INTE# 10
INTF# 10
INTG# 10
SERIRQ 10,11,14,27
PLOCK# 10
CARD_LED 18,25
CLKRUN# 10,14,23
CLK48M 2
CLK_48
Y7 48MHz Clock
OUT VDD
GND OE
*SG-8002CA 48M
L40 *FCM1608K221
L41 *FCM1608K221
R302 *0R
C530 *0.01U_0402
C585 *0.01U_0402
+3V
Griffey 12/08/2004
SI stage:
Remove all componet of PLL circuit and Add CLK48M input from CKG.
10,14,23 C/BE3#
10,14,23 C/BE2#
10,14,23 C/BE1#
10,14,23 C/BE0#
10,14,23 PAR
10,14,23 FRAME#
10,14,23 TRDY#
10,14,23 IRDY#
10,14,23 STOP#
10,14,23 DEVSEL#
AD25 R284 100R
10,14,23 PERR#
10,14,23 SERR#
10 REQ0#
10 GNT0#
2 PCLK_7411
10,14,23,27 PCIRST#
16,27 PCICGRST#
PCLK_7411
7411_PME#
R305 0R
11 RI#
Sting 10/12/2204
C528 0.001U_0402
C529 0.01U_0402
C498 0.1U
C511 0.1U
C461 0.001U_0402
C467 0.01U_0402
C519 0.1U
C536 0.1U
C635 0.1U
C636 0.1U
U21-5
PCI7411GHK
SCL
SDA
M3
M2
U27
24LC08
VCC
NC
SCL
SDA
A0
A1
A3
GND
R322 2.7K
R336 2.7K
PV stage:
Remove R701 & R702 for unused PCI1510RVGF circuit.
Griffey 12/10/2004
When -VCCD0 and -VCCD1 asserted high, PLOCK# and INTF# will provide a SDA signaling for I2C bus, PLOCK# will provide a SCL signaling for I2C bus.
PV stage:
Remove reserve relatived circuit for PCI1510RVGF.
PCIXX21 Power Terminals
U21-4
PCI7411GHK
VCC
GND
1.5V
VR_EN
M19
H1
H2
C438 0.1U
C531 0.1U
R698 0R
VR_EN# :0
Internal voltage regulator enable for 1.5/2.5V core power.
DTC144EUA
Q50
R606 10K
10,14,23 PCI_PME#
7411_PME#
U21-6
W17
T19
NC
TEST0
VCO_LF
P12
U21-10
A_USB_EN
B_USB_EN
E2
E1
R306 *10K
R307 *10K
EMI
PCLK_7411
CLK48M
R679 *22R
R704 22R
C1036 *22P
C1046 22P
PV stage:
Pouplate R704 and C1045 for getting better EMI performance.
Sting 11/19/2004
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number CardBus
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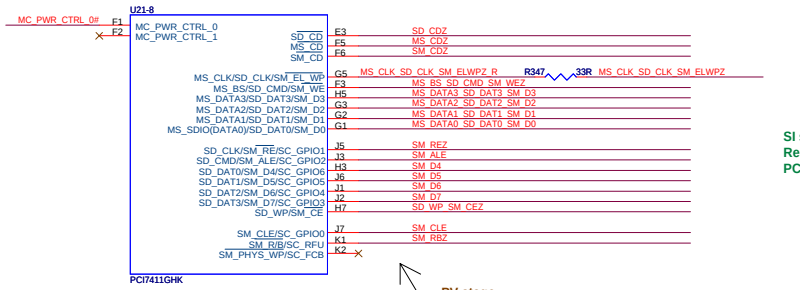
CARD POWER CONTROL



PV stage:
1. Disconnect SM_PHYS_WP.
2. Tie SM_EL_WP with SM_PHYS_WP of SM card to allow for normal operation of SD and SM.

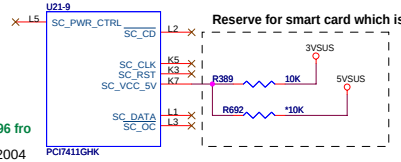
Sting 11/19/2004

PV stage:
Remove reserve relatived circuit for PCI1510RVGF.

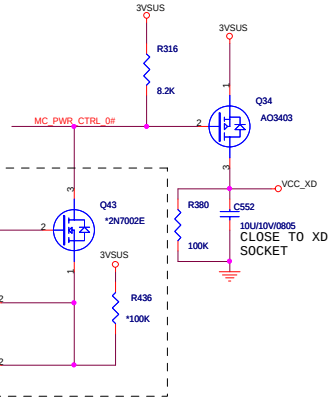
Griffey 12/08/2004

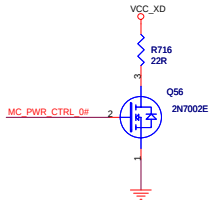
SI stage:
Remove reserve resistor R696 fro PCI1510RVGF.

Sting 10/12/2004



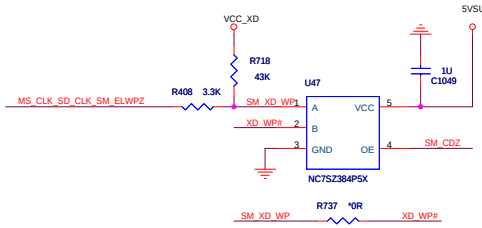
Reserve for smart card which is powered by 5V.





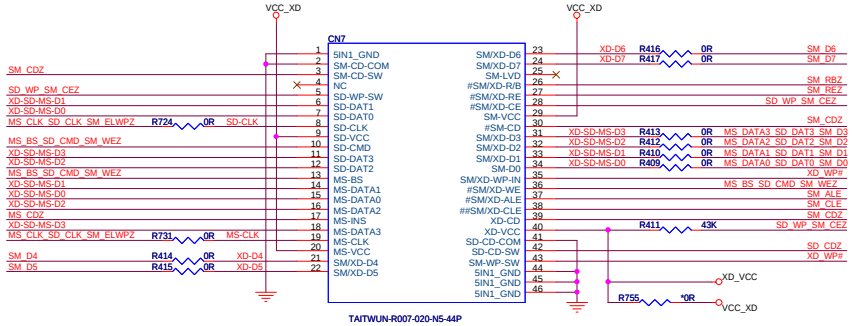
PV stage:
Add a discharge circuit for media card power.

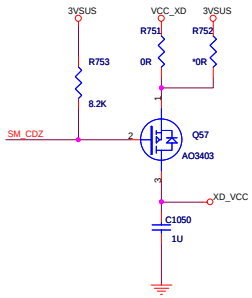
Sting 11/19/2004



PV stage:
1. Add quick switch circuit.

Griffey 12/10/2004

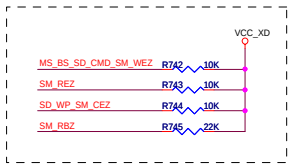




5 IN1 CARD READER

PV stage:
1. Add pull-up circuit.

Griffey 12/20/2004



PV stage:
1. Add R717 to solve SM card can't write protect issue.
2. Add R718 to solve cross-talk issue of MS-PRO card.
3. Add R719~R736 as terminal on all multi-funtion pin.

Sting 11/19/2004

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Quanta Computer Inc.

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C	CARD READER CONN	3A

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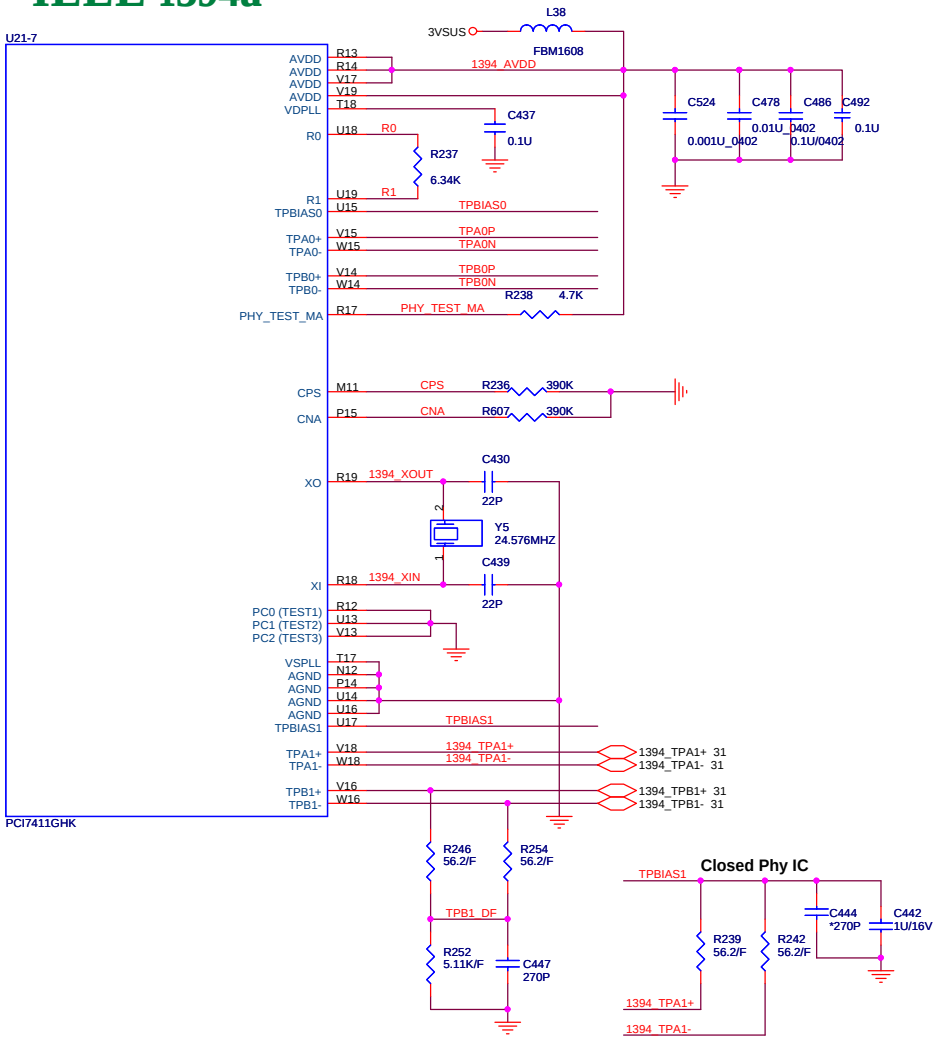
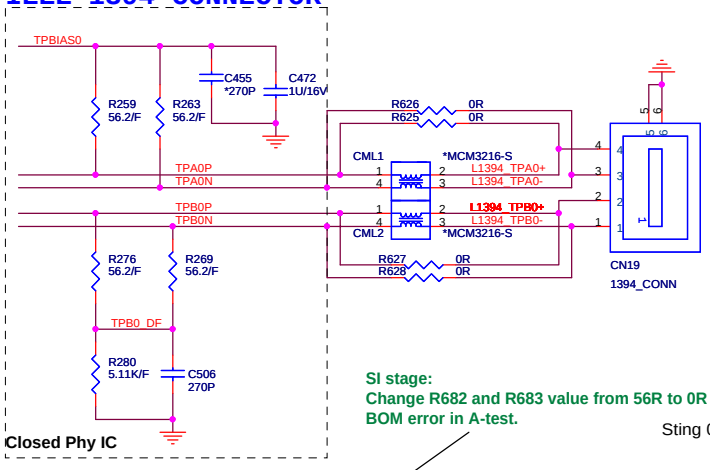
IEEE 1394a

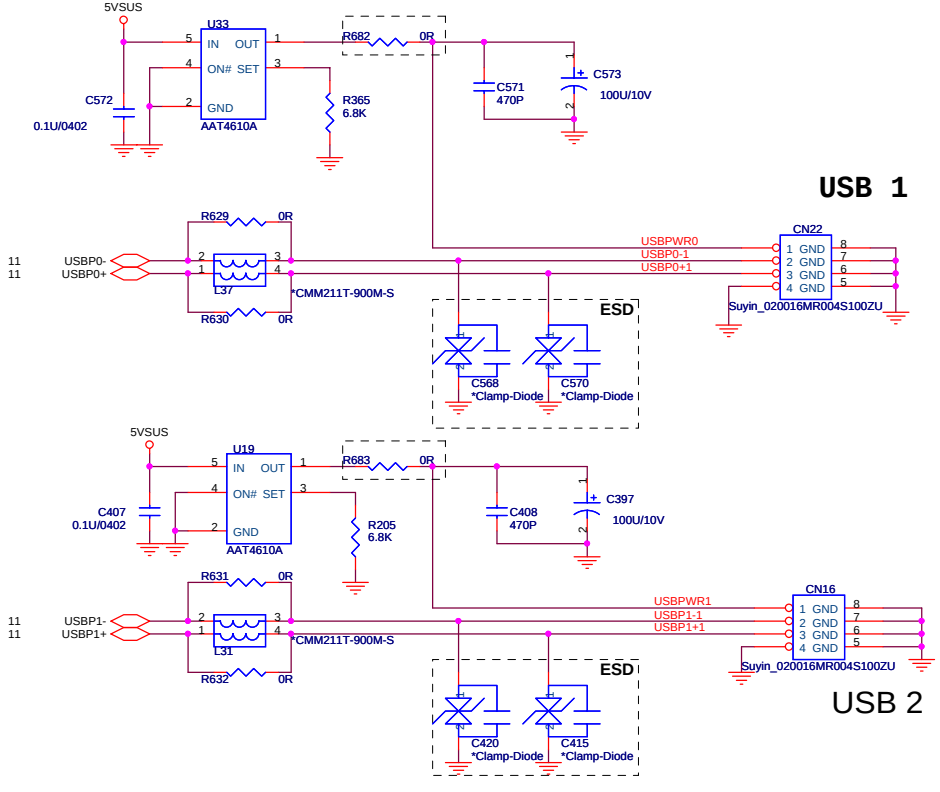


IEEE 1394 CONNECTOR



SI stage:
Change R682 and R683 value from 56R to 0R cause of BOM error in A-test.

Sting 09/24/2004



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Quanta Computer Inc.

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Custom	IEEE 1394A, USBX2	2A

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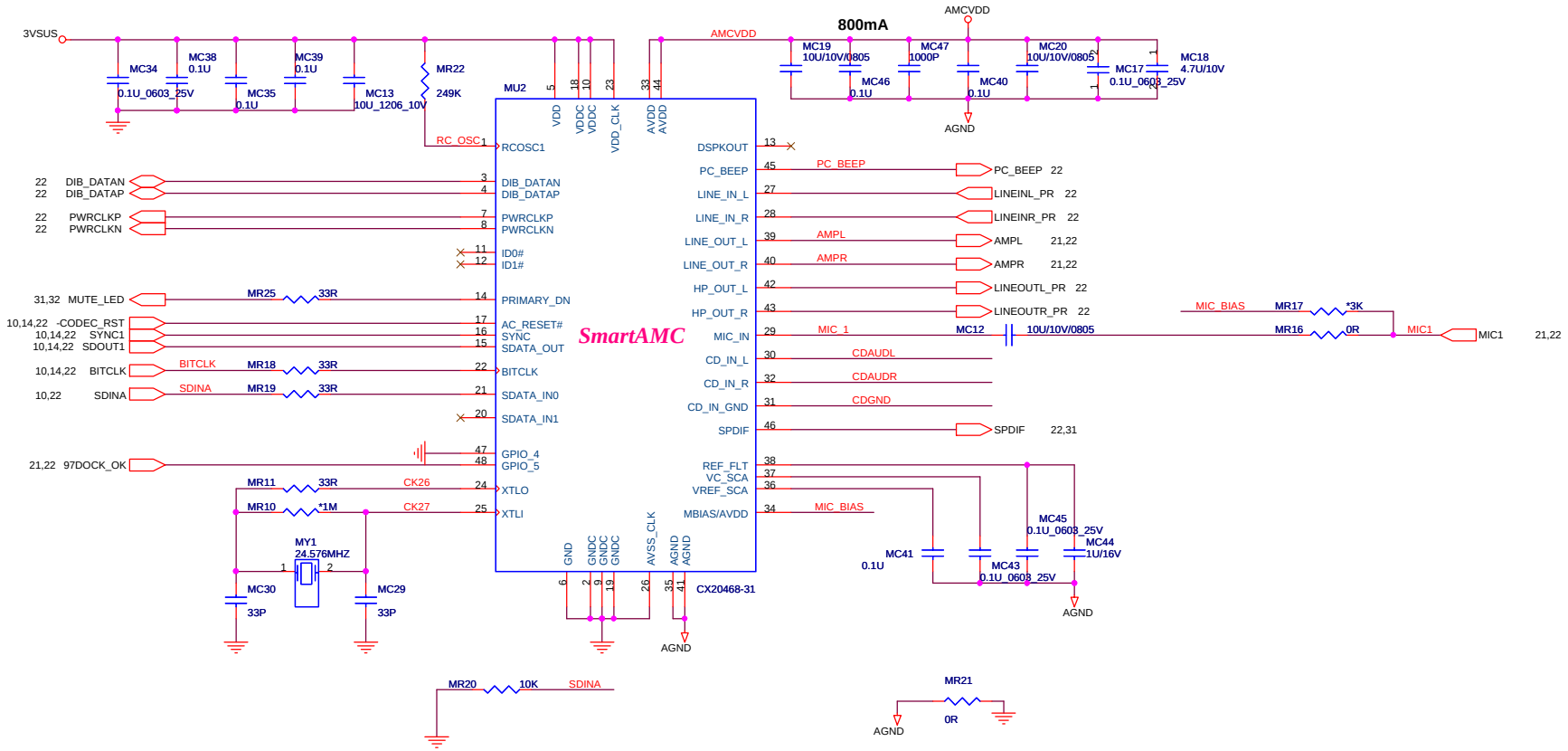
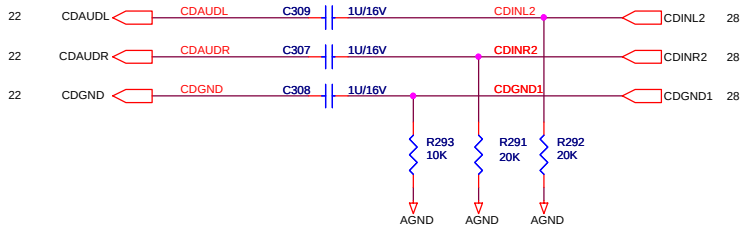
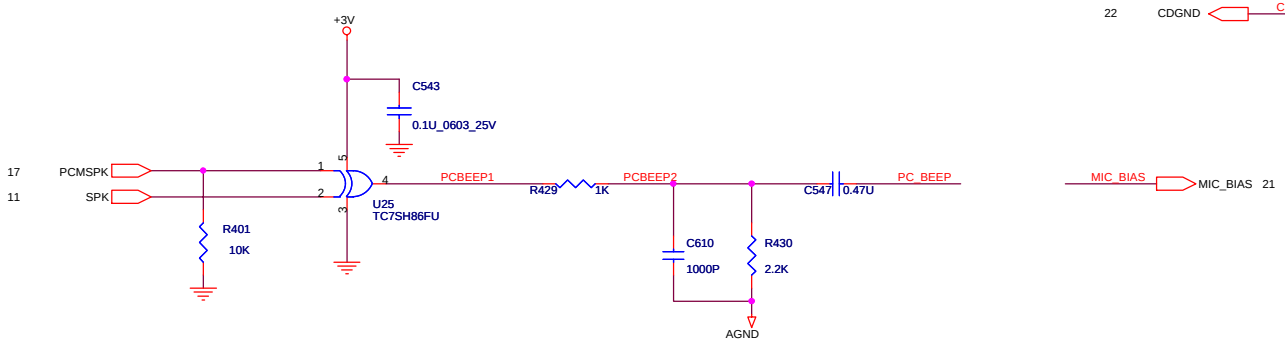
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



FROM CD-ROM



PC SPEAKER



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	AMC97 CODEC	1A

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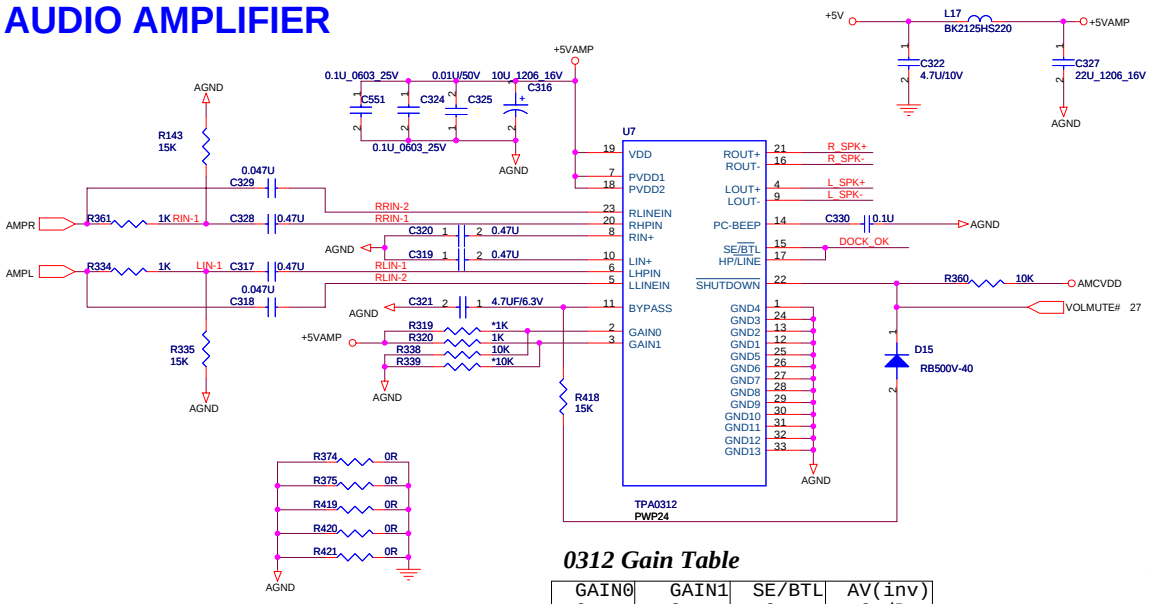
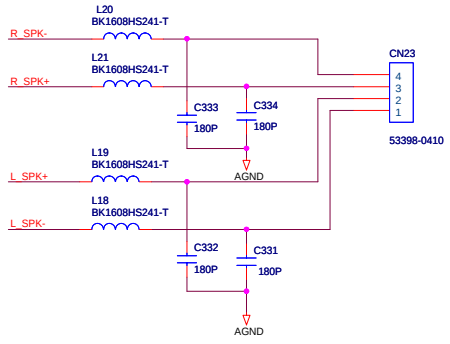
AUDIO AMPLIFIER

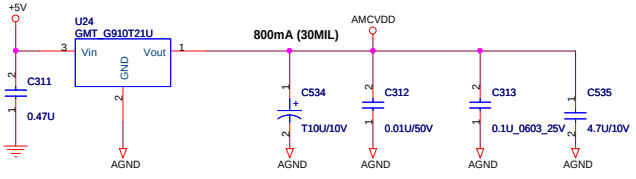


0312 Gain Table

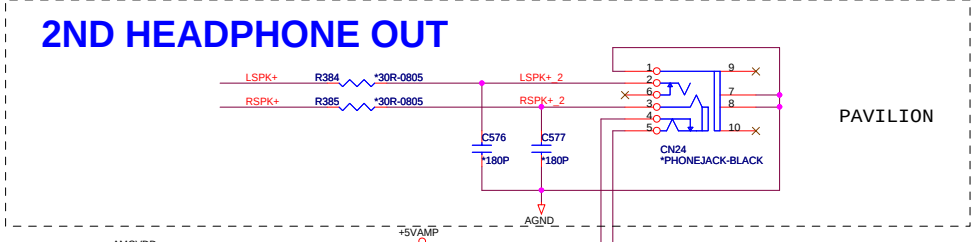
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

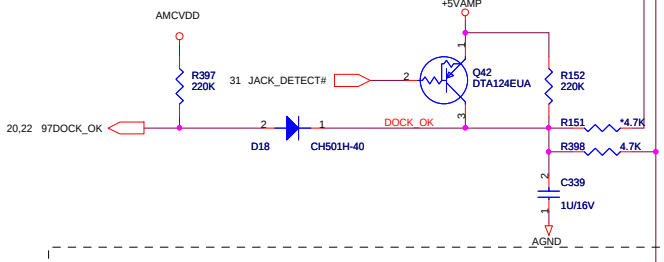
SPEAKER OUT





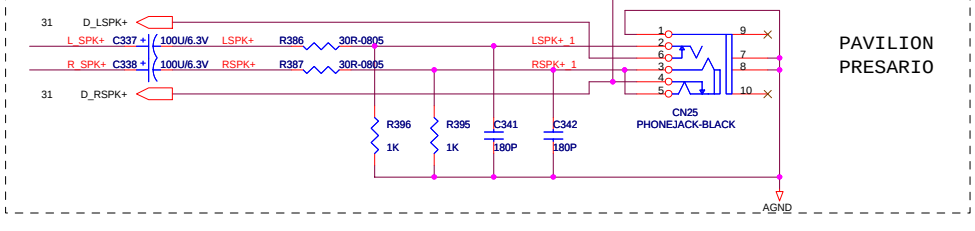
2ND HEADPHONE OUT



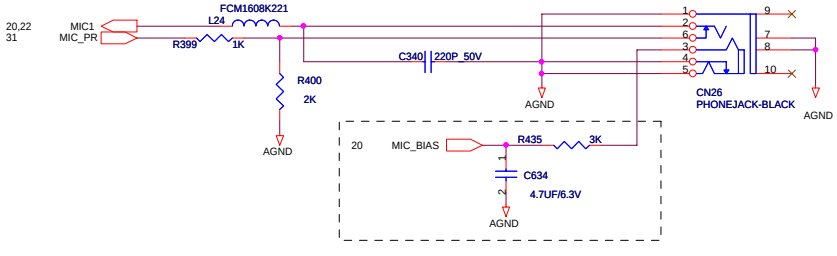


	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

HEADPHONE OUT



MICROPHONE



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP_ TI-TPA0312	1A

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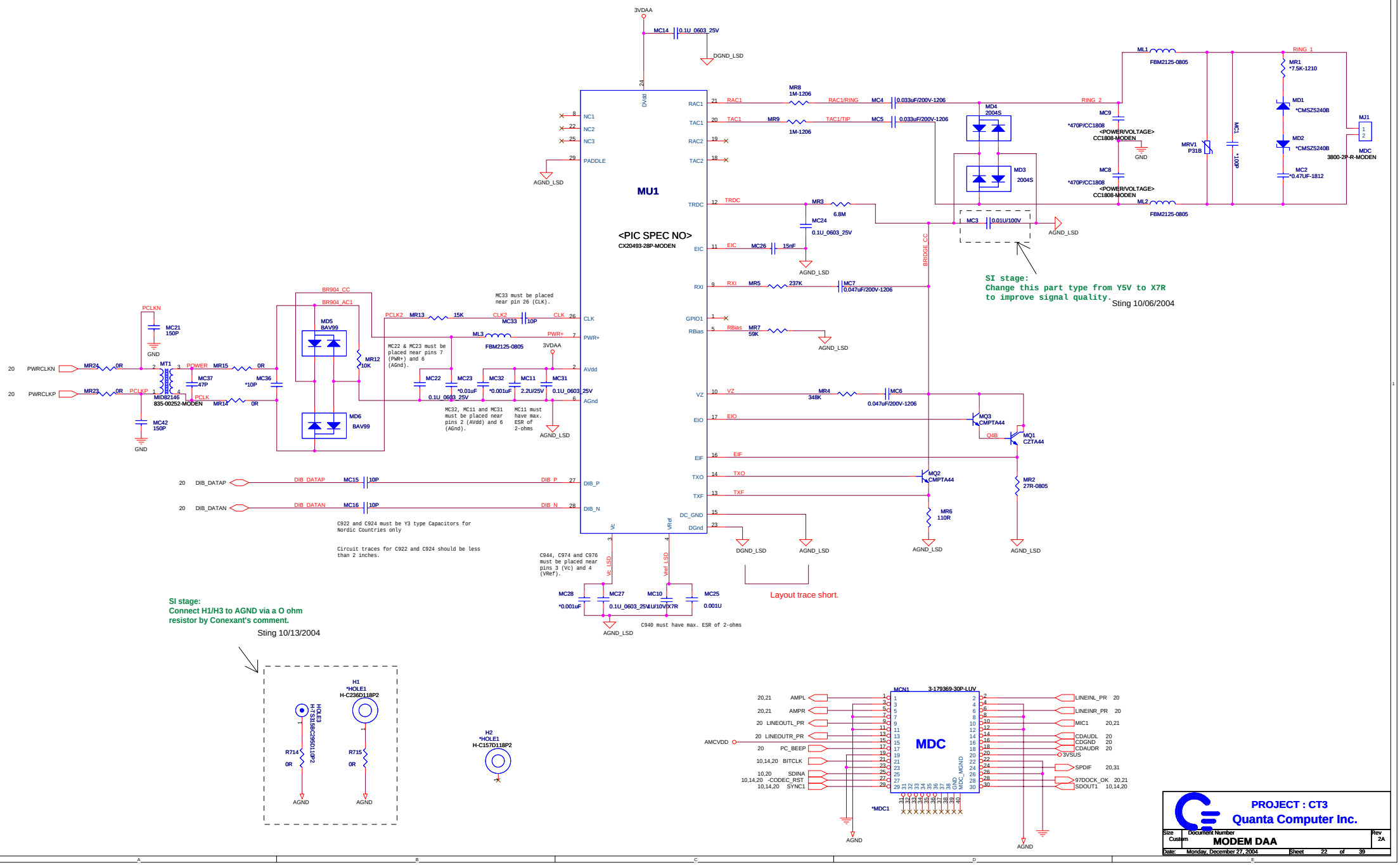
MU1
<PIC SPEC NO>
CX20493-28P-MODEN
3VDAA
MC14 0.1U_0603_25V
DGND_LSD
AGND_LSD
RAC1
TAC1
RAC2
TAC2
TRDC
EIC
RXI
GPIO1
RBias
VZ
EIO
EIF
TXO
TXF
DC_GND
DGnd
DIB_P
DIB_N
CLK
PWR+
AVdd
AGnd
Vc
VRef
DVdd
PADDLE
NC1
NC2
NC3
MR8 1M-1206
MR9 1M-1206
RAC1/RING
TAC1/TIP
MC4 0.033uF/200V-1206
MC5 0.033uF/200V-1206
MD4 2004S
MD3 2004S
MC9 *470P/CC1808 <POWER/VOLTAGE> CC1808-MODEN
MC8 *470P/CC1808 <POWER/VOLTAGE> CC1808-MODEN
GND
ML1 FBM2125-0805
ML2 FBM2125-0805
RING_1
RING_2
MR1 *7.5K-1210
MD1 *CMSZ5240B
MD2 *CMSZ5240B
MC2 *0.47UF-1812
MJ1
MDC 3800-2P-R-MODEN
MRV1 P31B
MC1 *100P
MR3 6.8M
MC24 0.1U_0603_25V
MC26 15nF
MR5 237K
MC7 0.047uF/200V-1206
MR7 59K
MC3 0.01U/100V
BRIDGE CC
MR4 348K
MC6 0.047uF/200V-1206
MQ3 CMPTA44
MQ1 CZTA44
Q4B
MQ2 CMPTA44
MR2 27R-0805
MR6 110R
MC33 must be placed near pin 26 (CLK).
MC22 & MC23 must be placed near pins 7 (PWR+) and 6 (AGnd).
MC32, MC11 and MC31 must be placed near pins 2 (AVdd) and 6 (AGnd).
MC11 must have max. ESR of 2-ohms
PCLK2 MR13 15K
CLK2 MC33 10P
ML3 FBM2125-0805
MC22 0.1U_0603_25V
MC23 *0.01uF
MC32 *0.001uF
MC11 2.2U/25V
MC31 0.1U_0603_25V
PCLKN
PCLKP
MC21 150P
MC42 150P
MR24 0R
MR23 0R
MR15 0R
MR14 0R
MT1 MID82146 835-00252-MODEN
MC37 47P
MC36 *10P
MD5 BAV99
MD6 BAV99
MR12 10K
BR904_CC
BR904_AC1
PWRCLKN
PWRCLKP
PCLKN
PCLKP
PCLK
PPOWER
DIB_DATAP
DIB_DATAN
MC15 10P
MC16 10P
C922 and C924 must be Y3 type Capacitors for Nordic Countries only
Circuit traces for C922 and C924 should be less than 2 inches.
C944, C974 and C976 must be placed near pins 3 (Vc) and 4 (VRef).
Vc_LSD
Vref_LSD
MC28 *0.001uF
MC27 0.1U_0603_25V
MC10 1U/10V/X7R
MC25 0.001U
C940 must have max. ESR of 2-ohms
Layout trace short.
SI stage:
Change this part type from Y5V to X7R
to improve signal quality.
Sting 10/06/2004
SI stage:
Connect H1/H3 to AGND via a O ohm
resistor by Conexant's comment.
Sting 10/13/2004
H1 *HOLE1 H-C236D118P2
H3 *HOLE3 H-C236D118P2
R714 0R
R715 0R
AGND
H2 *HOLE1 H-C157D118P2
MCN1 3-179369-30P-LUV
MDC
*MDC1
AMPL
AMPR
LINEOUTL_PR
LINEOUTR_PR
PC_BEEP
BITCLK
SDINA
CODEC_RST
SYNC1
AMCVDD
LINEINL_PR
LINEINR_PR
MIC1
CDAUDL
CDGND
CDAUDR
3VSUS
SPDIF
97DOCK_OK
SDOUT1
MDC_MGND
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number MODEM DAA
Rev 2A
Date: Monday, December 27, 2004
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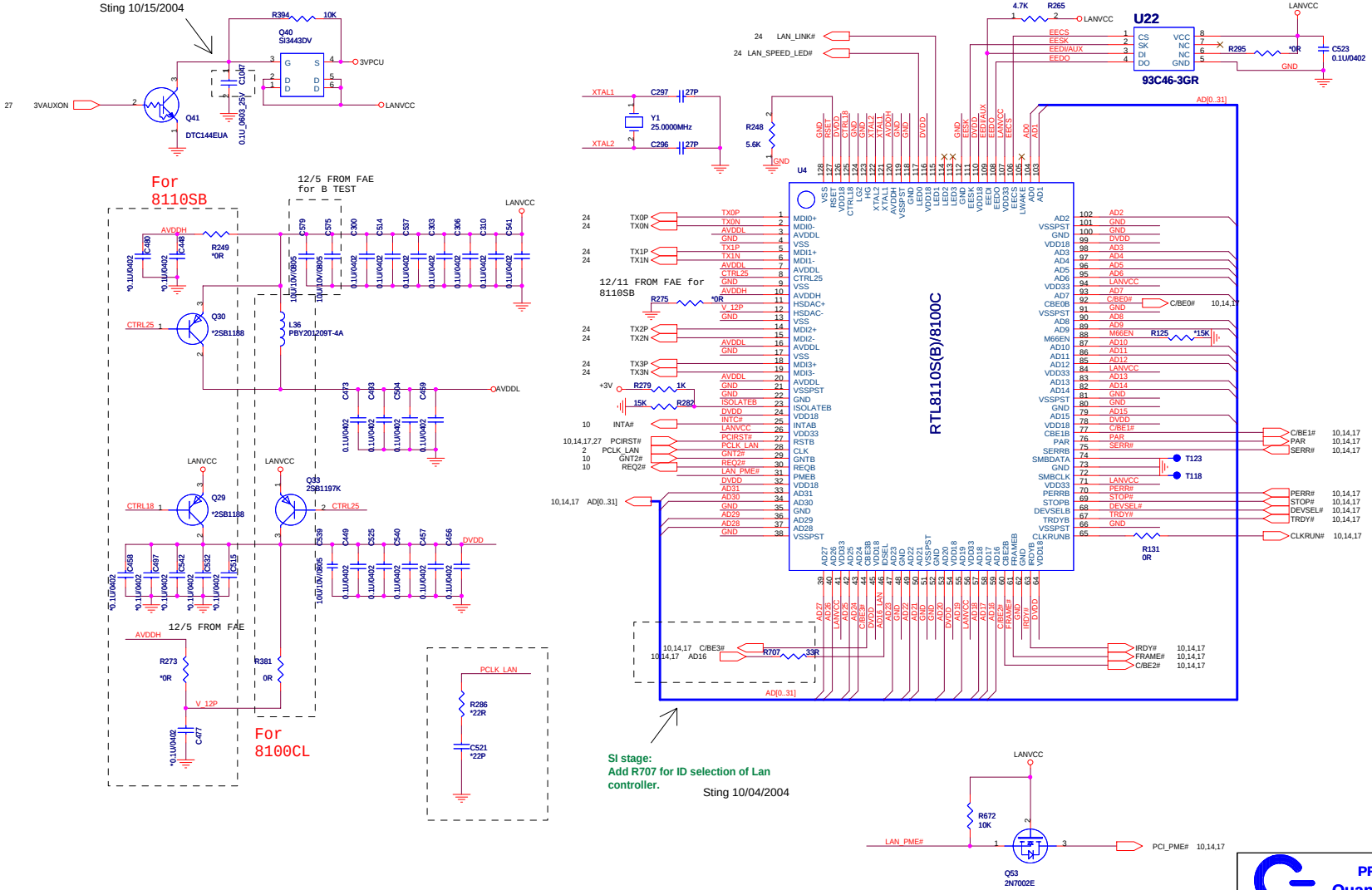
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120

SI stage:
Add a 0.1uF to make Q40 turn on slowly, because 3VPCU will drop when LANVCC turned on quickly. it will make EC state machine crazy.

Sting 10/15/2004



SI stage:
Add R707 for ID selection of Lan controller.

Sting 10/04/2004

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	RTL8100CL / RTL8110SB	2A

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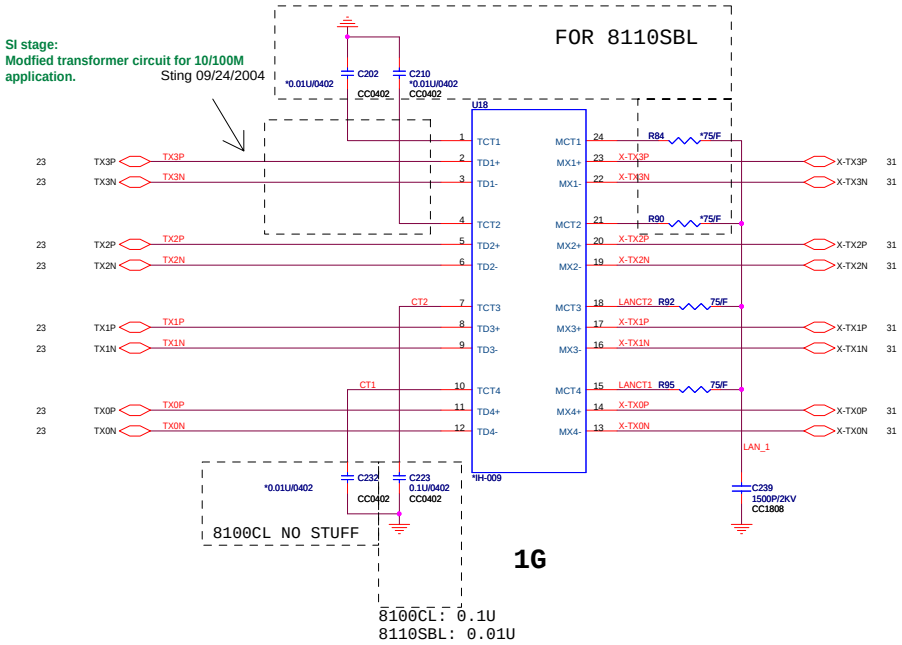

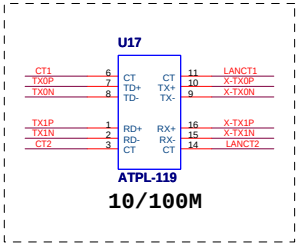

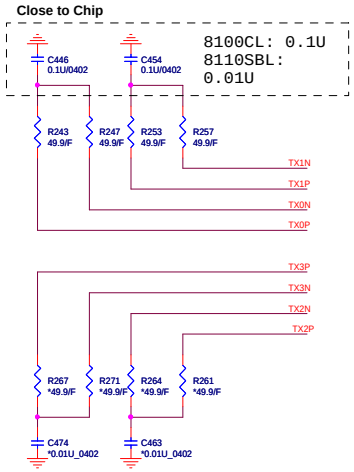

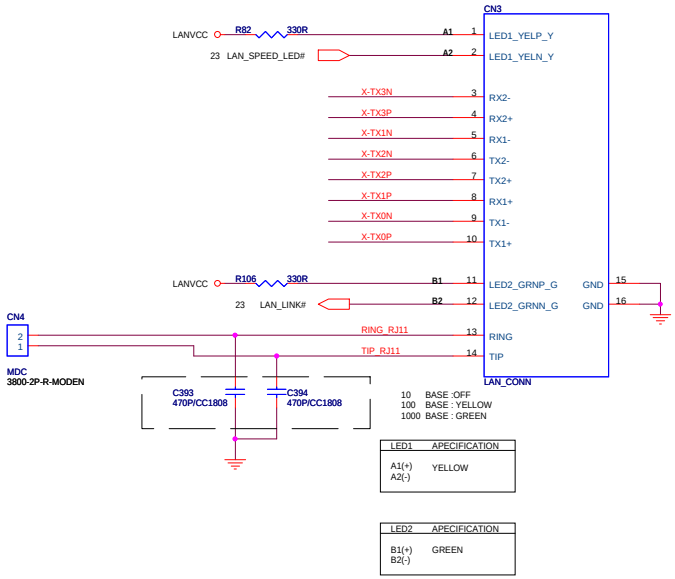

LED1	APECIFICATION
A1(+) A2(-)	YELLOW

LED2	APECIFICATION
B1(+) B2(-)	GREEN

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	LAN, RJ11, RJ45	2A

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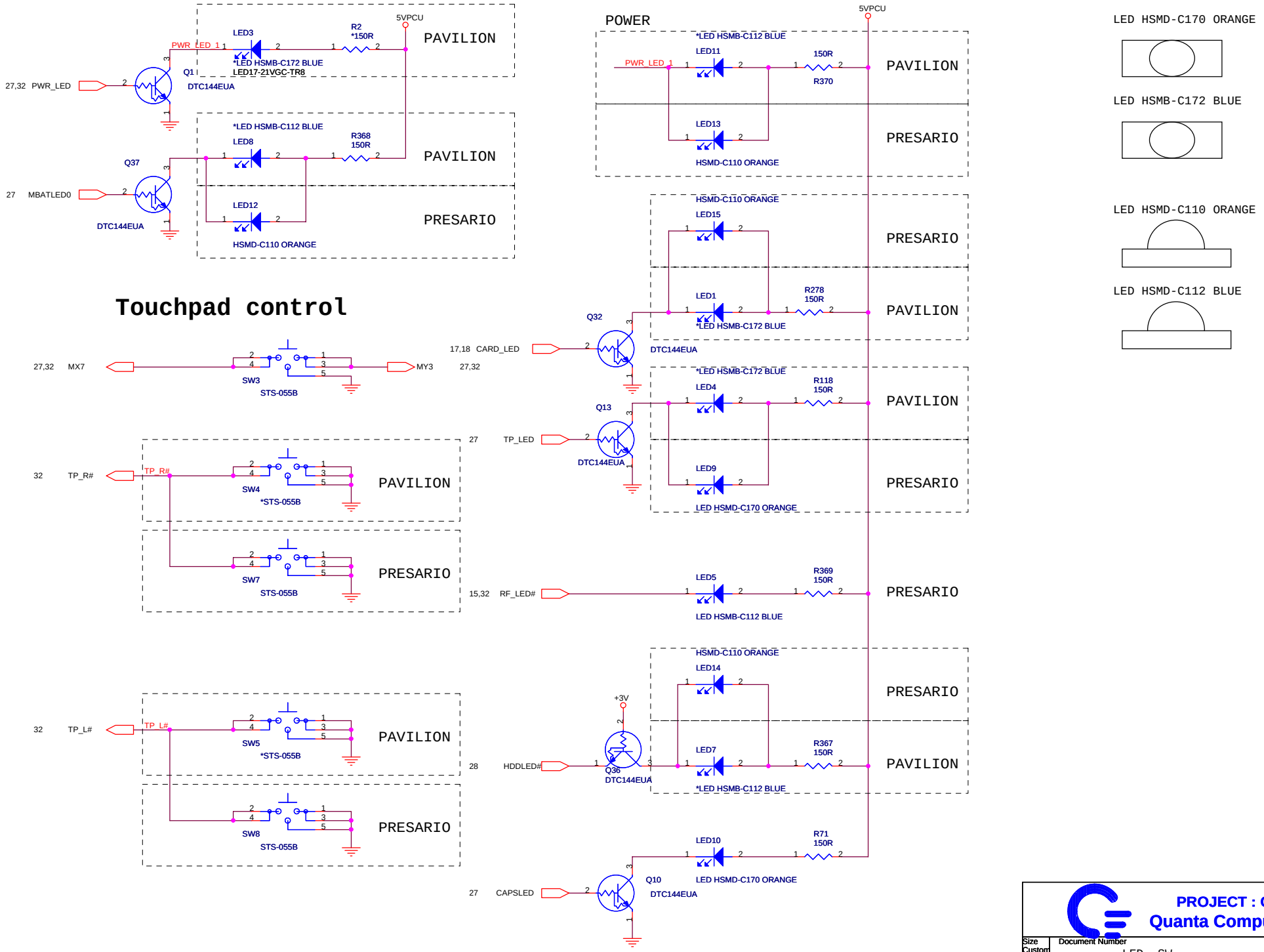

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED, SW	1A

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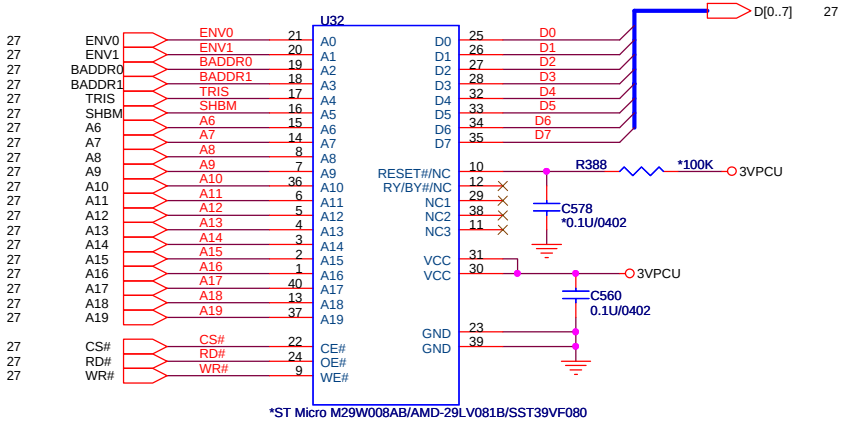
8Mbit (1M Byte), TSSOP40

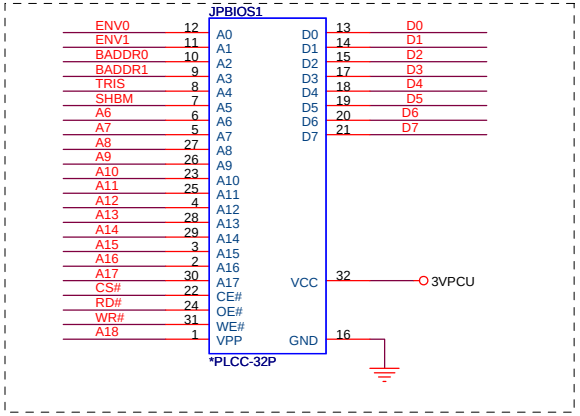


1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

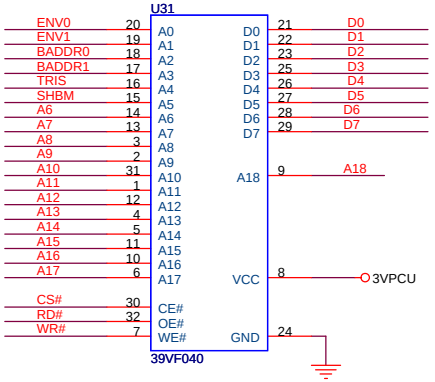
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

SI stage:
Add PLCC32 cause of it is convenient for Bios debugging.

Sting 10/01/2004



4Mbit (512k Byte), TSSOP32



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
B	BIOS ROM	2A

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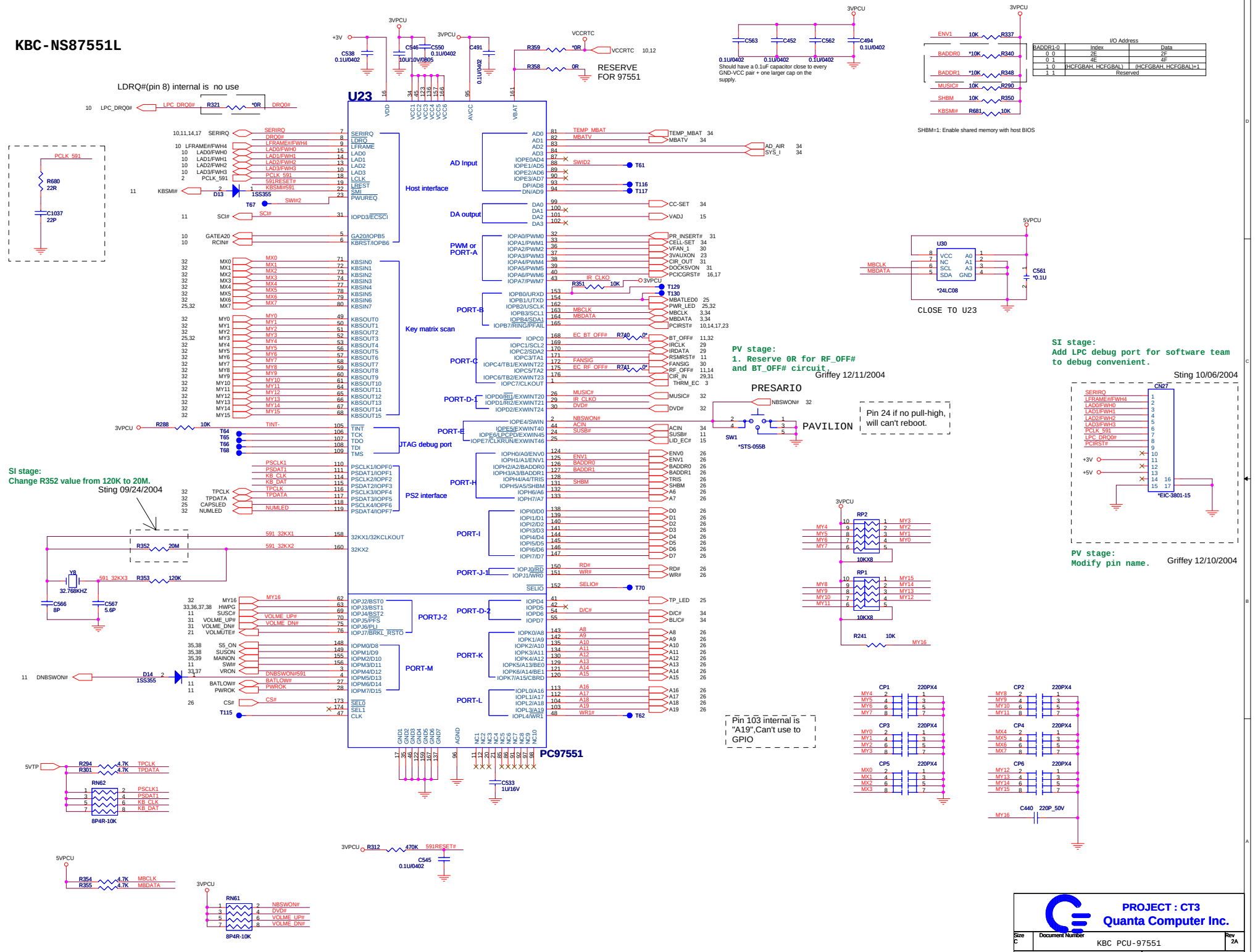
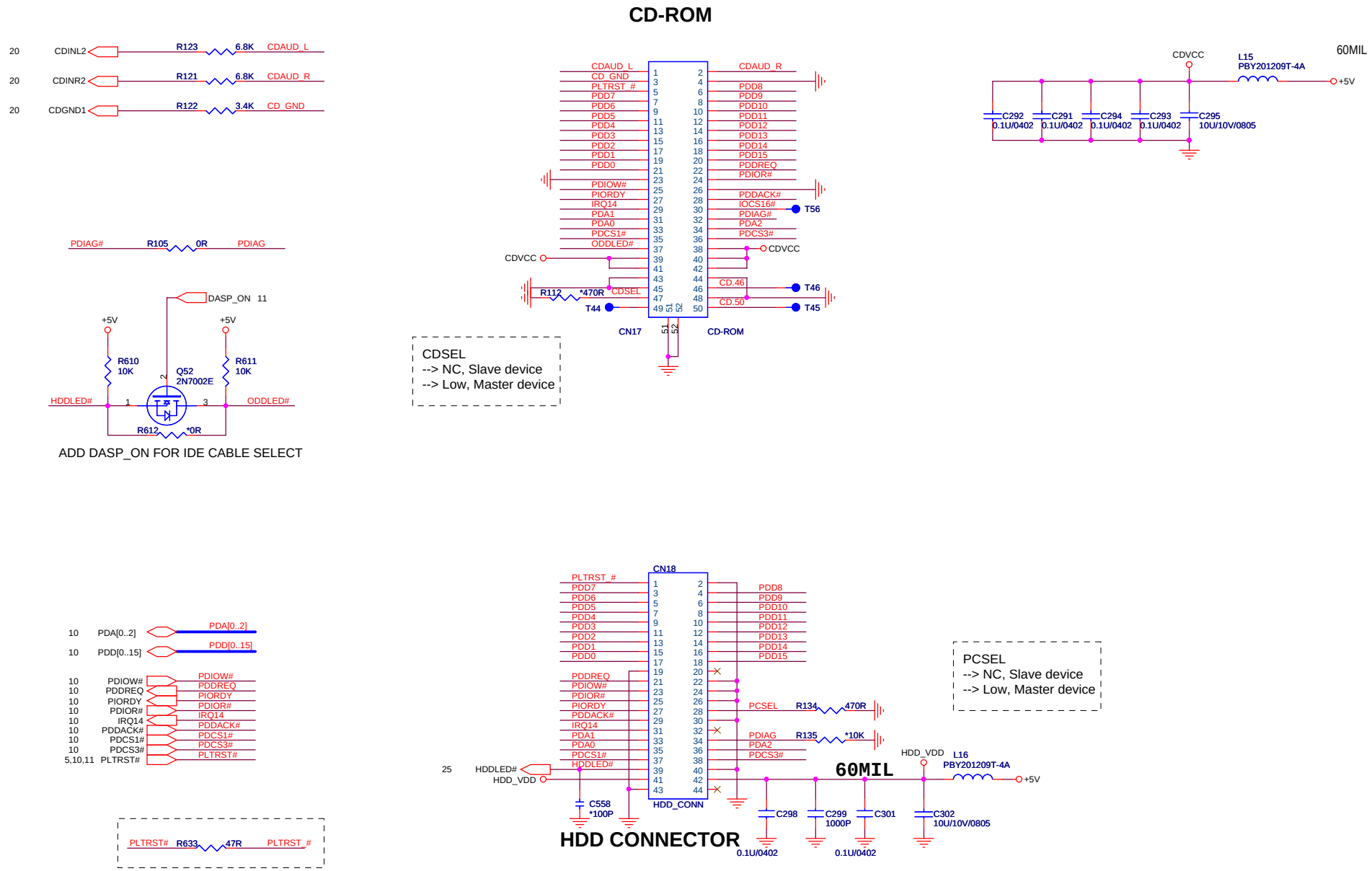
KBC-NS87551L



HDD, CD-ROM



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD&ODD CONN.	2A

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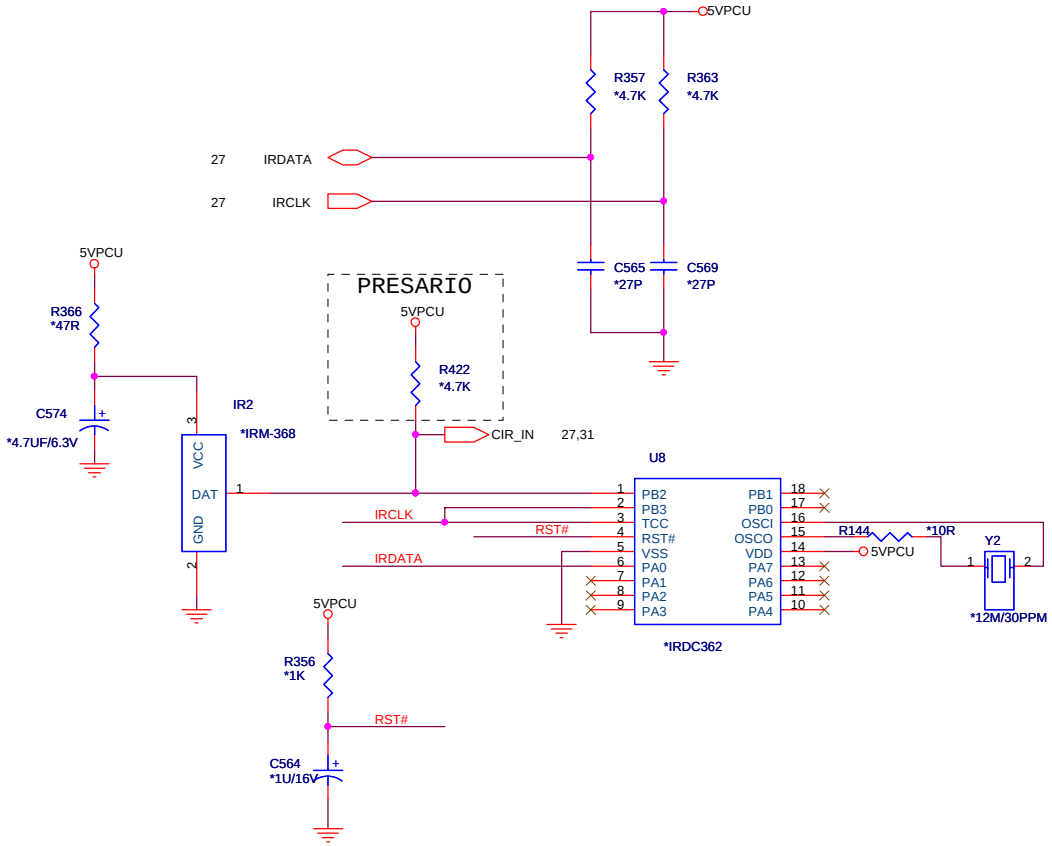

PROJECT : CT3

Quanta Computer Inc.

Size	Document Number	Rev
B	REMOTE IRDC362	1A

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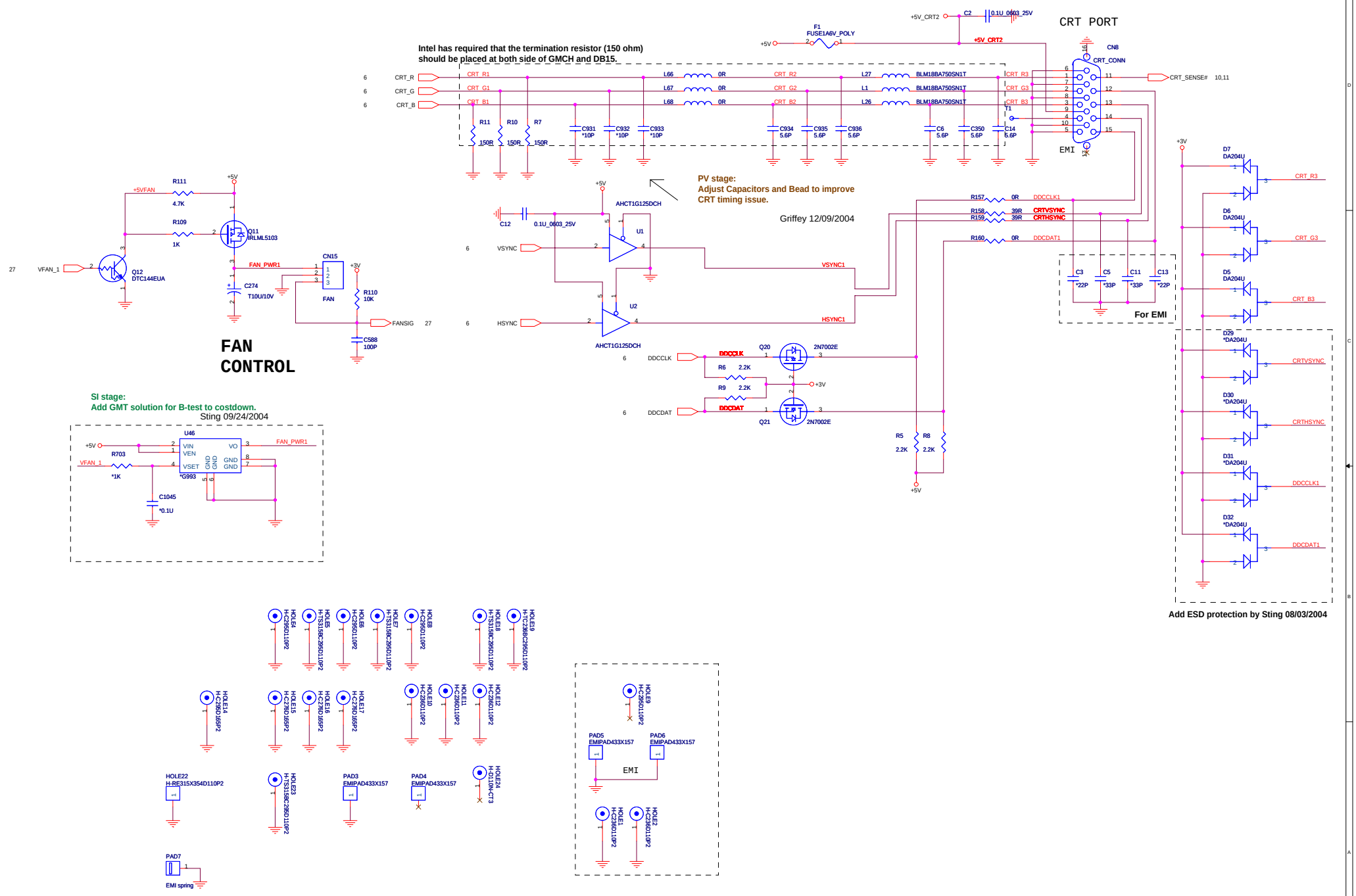

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	FAN, CRT, EMI PAD	2A

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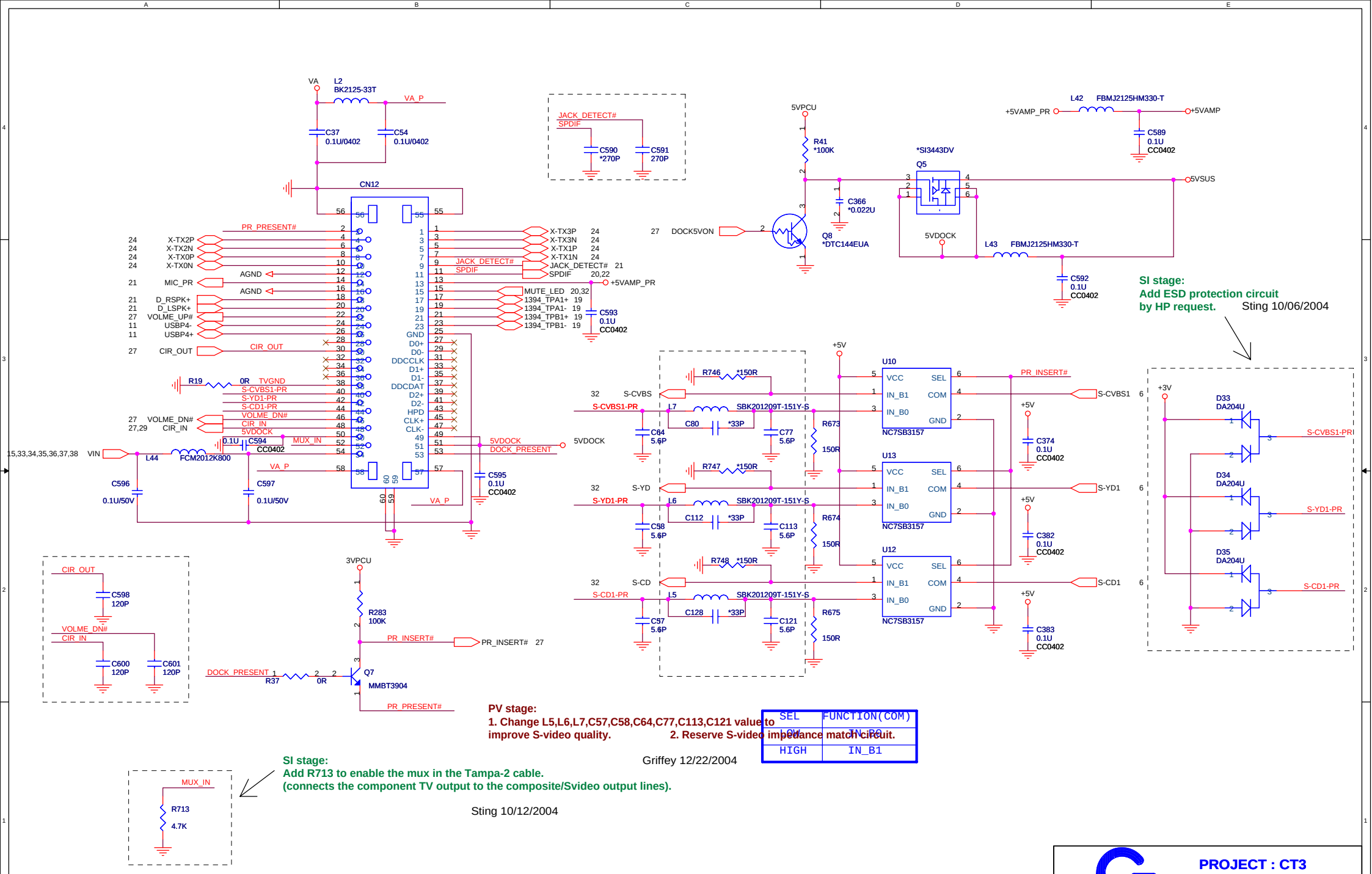

SI stage:
Add ESD protection circuit
by HP request.

Sting 10/06/2004

PV stage:
1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.
2. Reserve S-video impedance match circuit.

SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

Griffey 12/22/2004

SI stage:
Add R713 to enable the mux in the Tampa-2 cable.
(connects the component TV output to the composite/Svideo output lines).

Sting 10/12/2004

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING	2A

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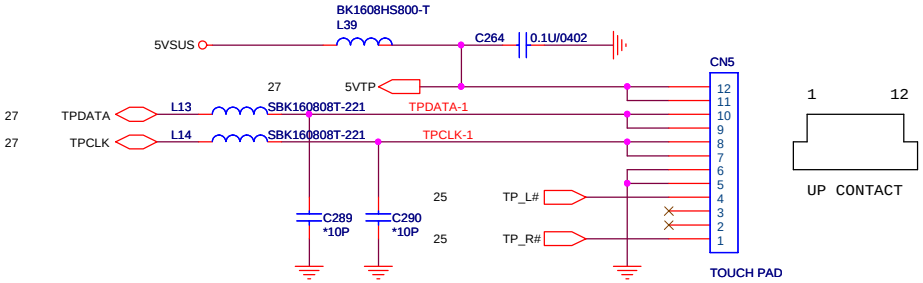
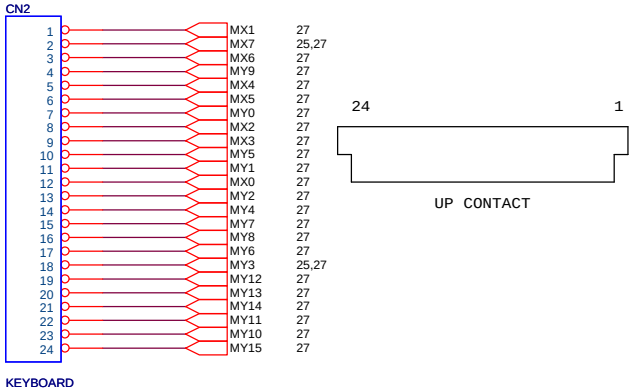
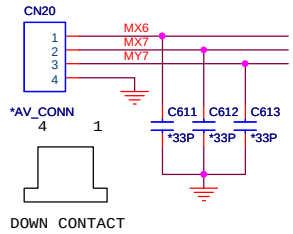
TOUCH PAD CONNECTOR



KEYBOARD CONNECTOR

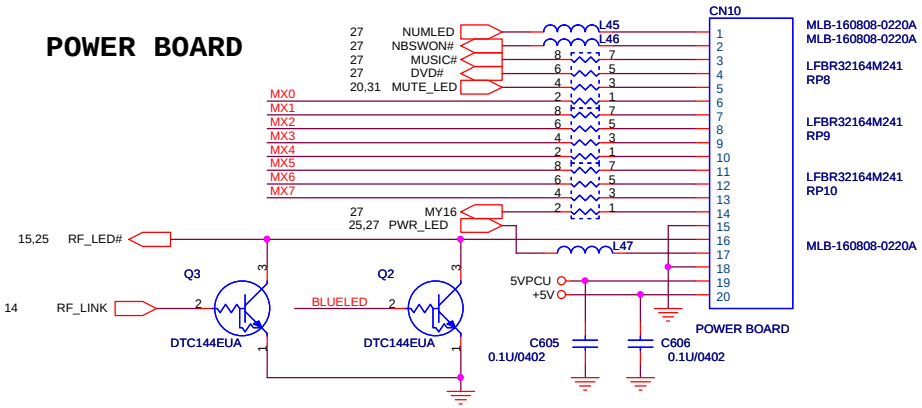


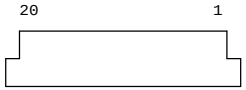
AV BOARD



MX6	MX7
ENTER	MENU

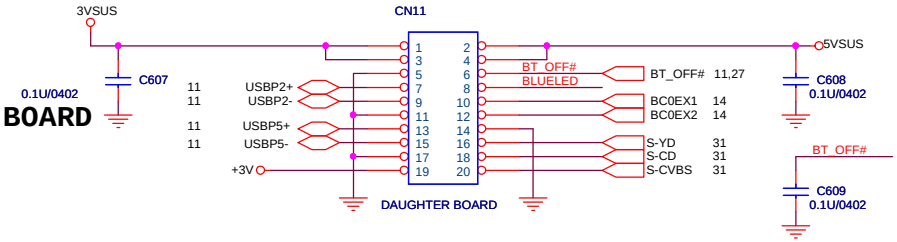
POWER BOARD

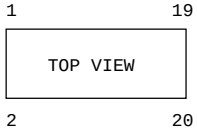




MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD





PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH/TP/BTB	1A

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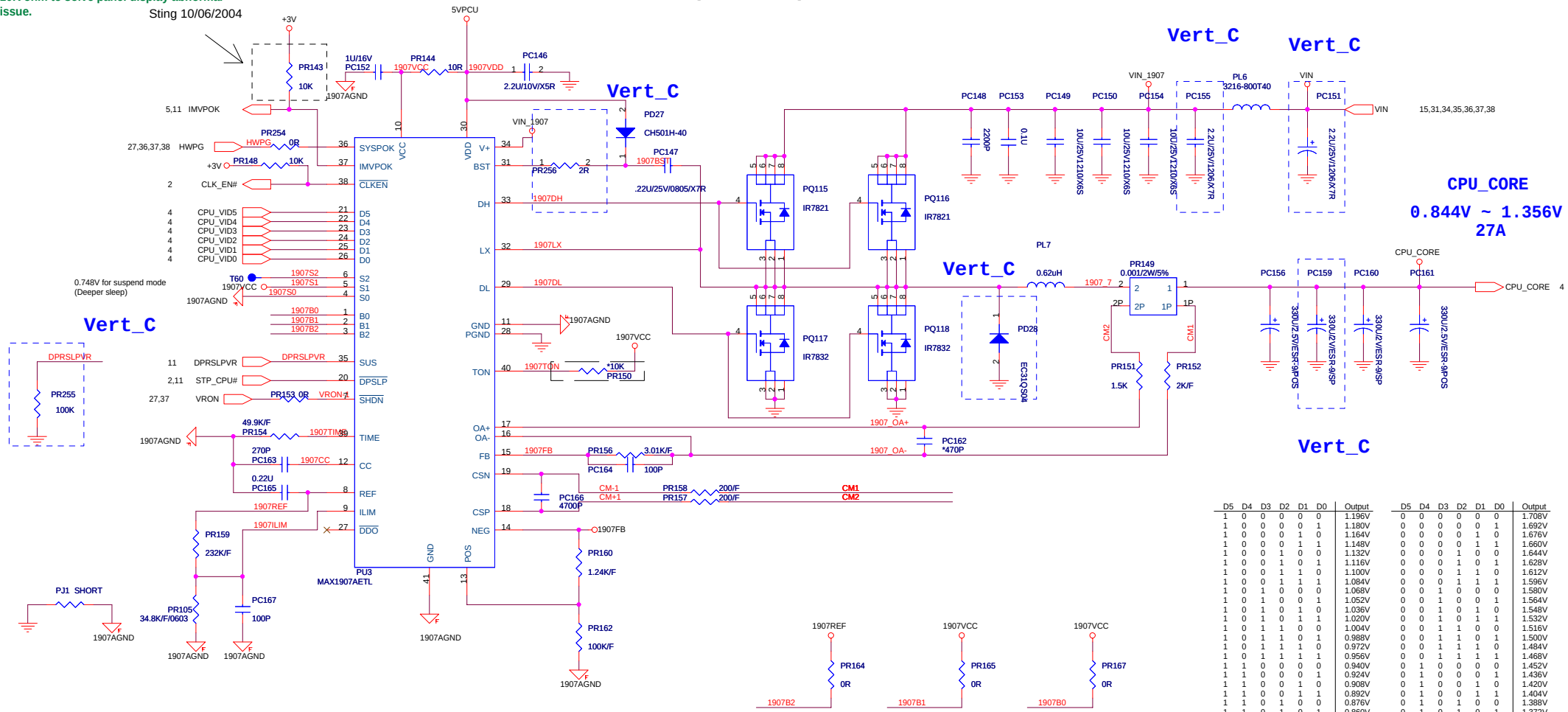
CPU VCC_CORE (MAX1907)

SI stage:
Change PR143 value from 100K ohms to 10K ohm to solve panel display abnormal issue.

Sting 10/06/2004



SUSPEND MODE (SUS=HIGH)			
S2	S1	S0	Output
OPEN	VCC	GND	0.748V

VCC_BOOT			
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU CORE POWER	2A

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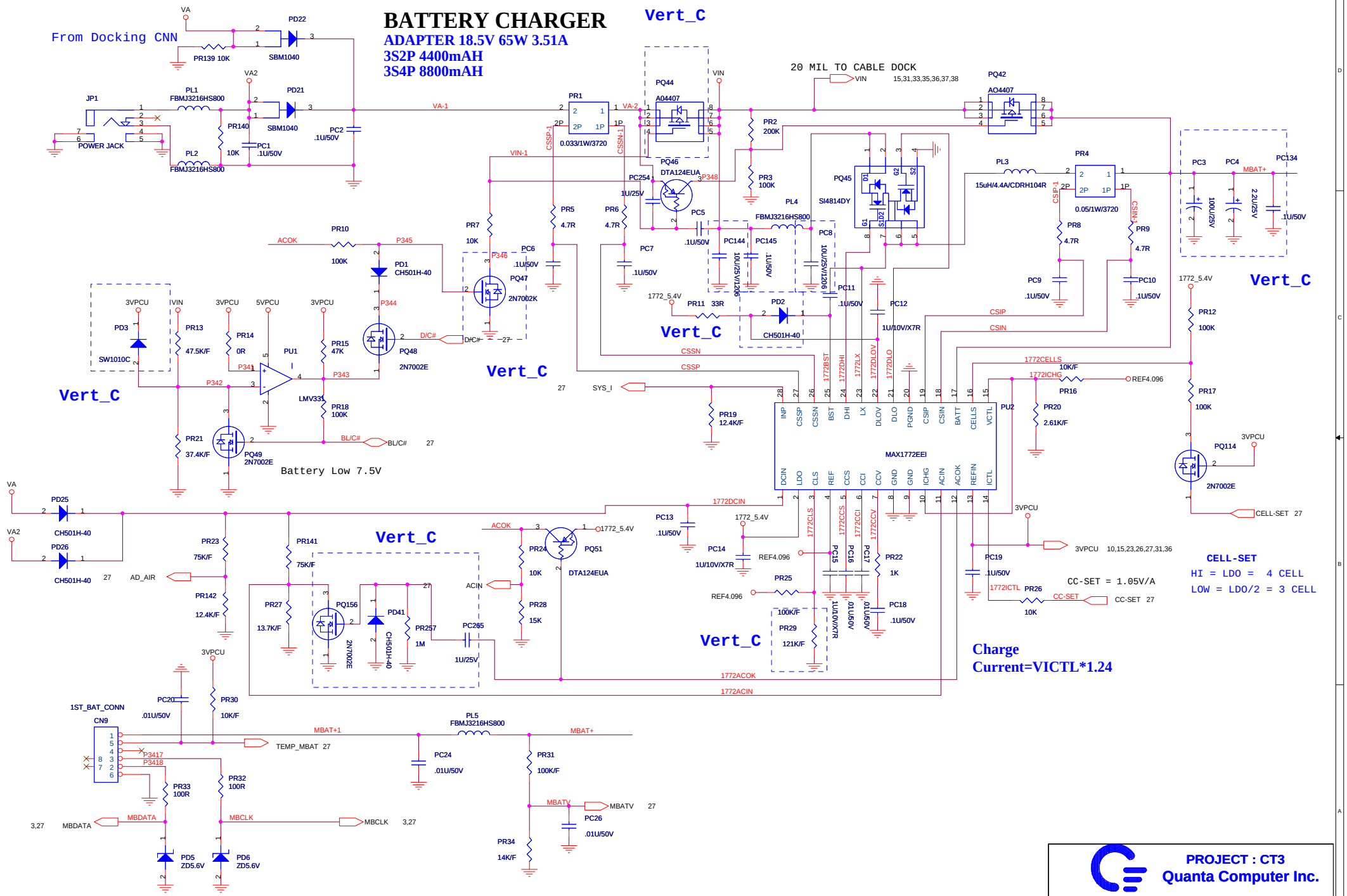
BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A
3S2P 4400mAH
3S4P 8800mAH



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1772/CHARGING	2A

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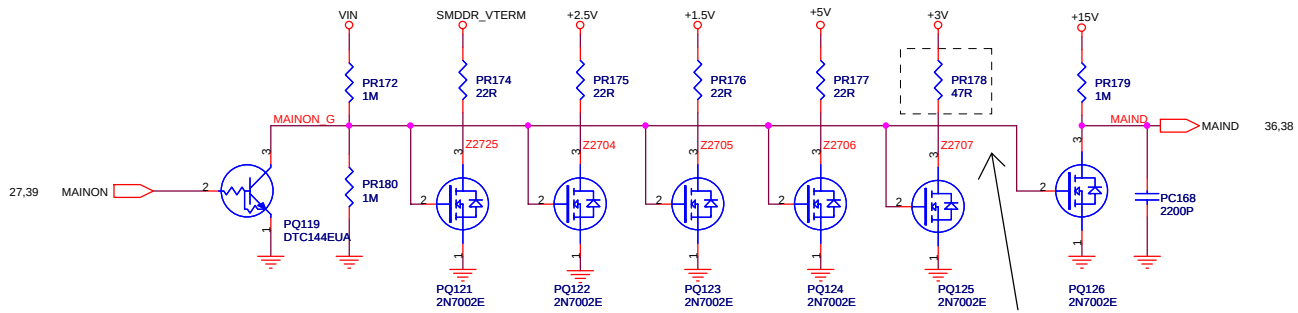
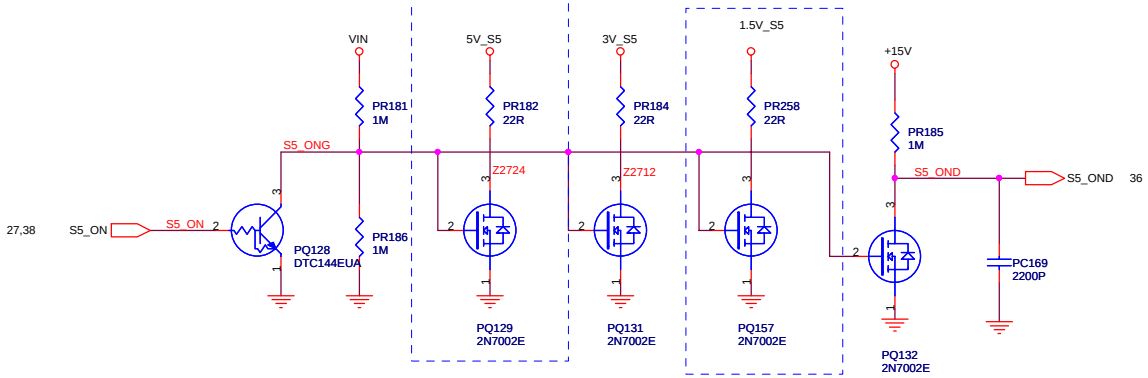


Vert_C

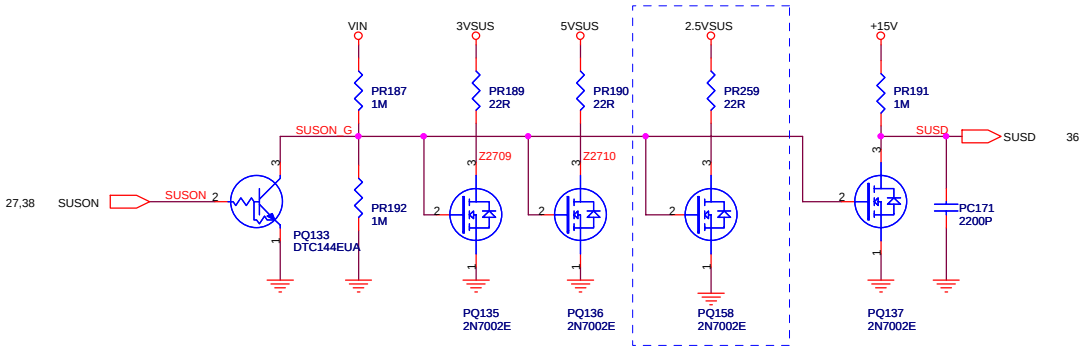
Vert_C

SI stage:
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

Sting 10/19/2004



Vert_C



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**DISCHARGE**	2A

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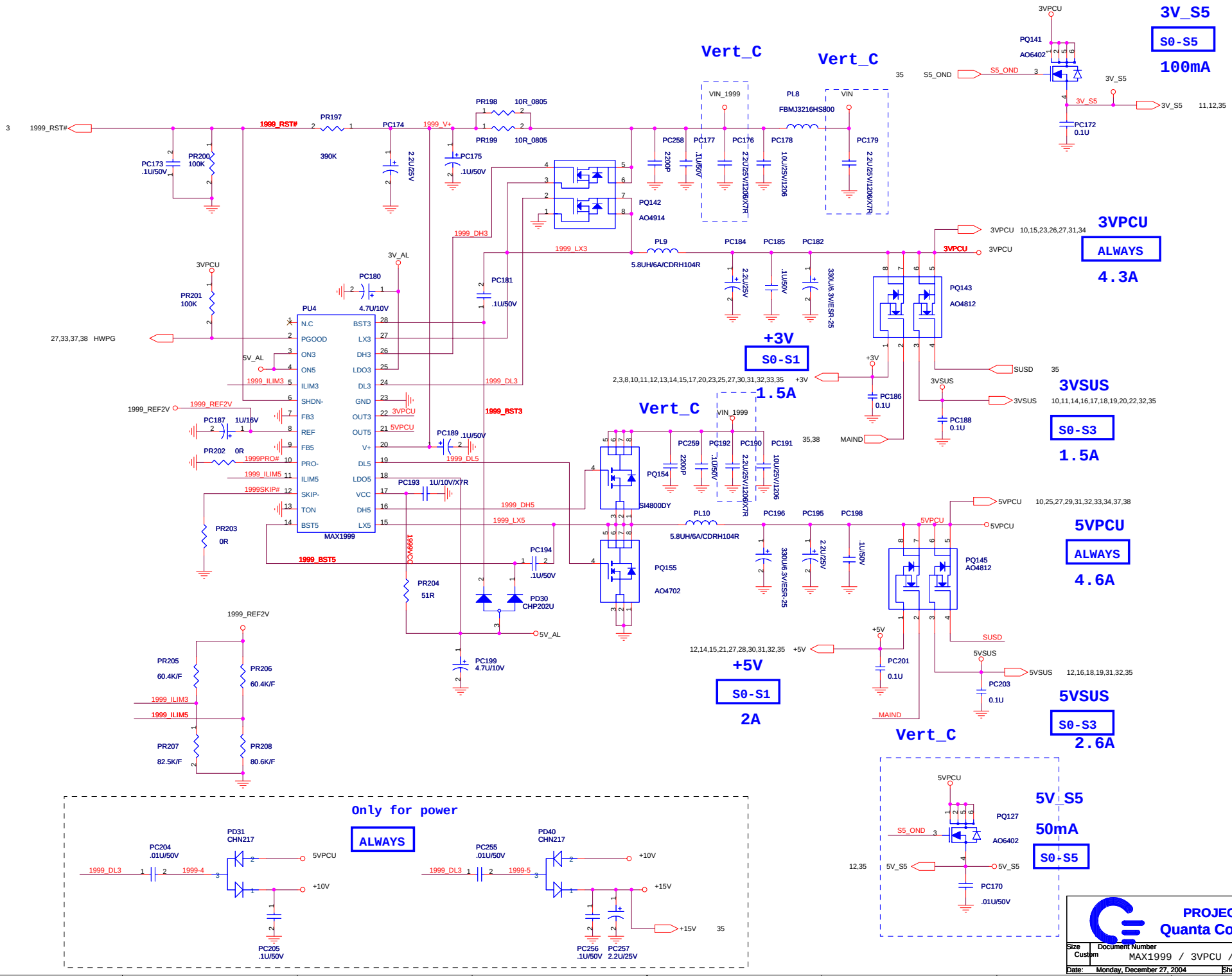
3V_S5
S0-S5
100mA
3VPCU
ALWAYS
4.3A
+3V
S0-S1
1.5A
3VSUS
S0-S3
1.5A
5VPCU
ALWAYS
4.6A
+5V
S0-S1
2A
5VSUS
S0-S3
2.6A
5V_S5
50mA
S0+S5
Vert_C
MAX1999
PU4
PQ141
AO6402
PQ142
AO4914
PQ143
AO4812
PQ145
AO4812
PQ154
SI4800DY
PQ155
AO702
PQ127
AO6402
PL8
FBMJ3216HS800
PL9
5.8UH/6A/CDRH104R
PL10
5.8UH/6A/CDRH104R
PD30
CHP202U
Only for power
ALWAYS
PD31
CHN217
PD40
CHN217
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number
MAX1999 / 3VPCU / 5VPCU / 15V
Rev 2A
Date: Monday, December 27, 2004
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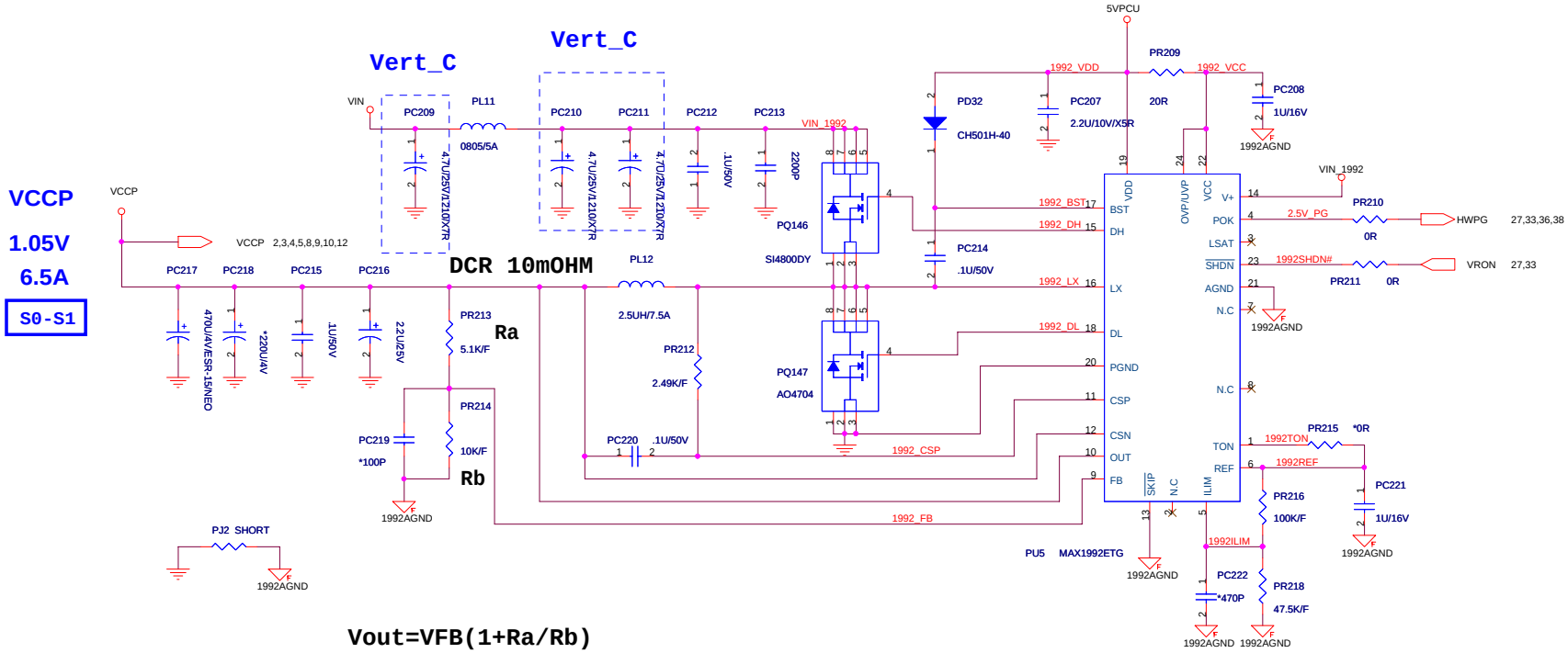

Vout=VFB(1+Ra/Rb)

#VFB=0.7V

PROJECT : CT3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCCP	2A

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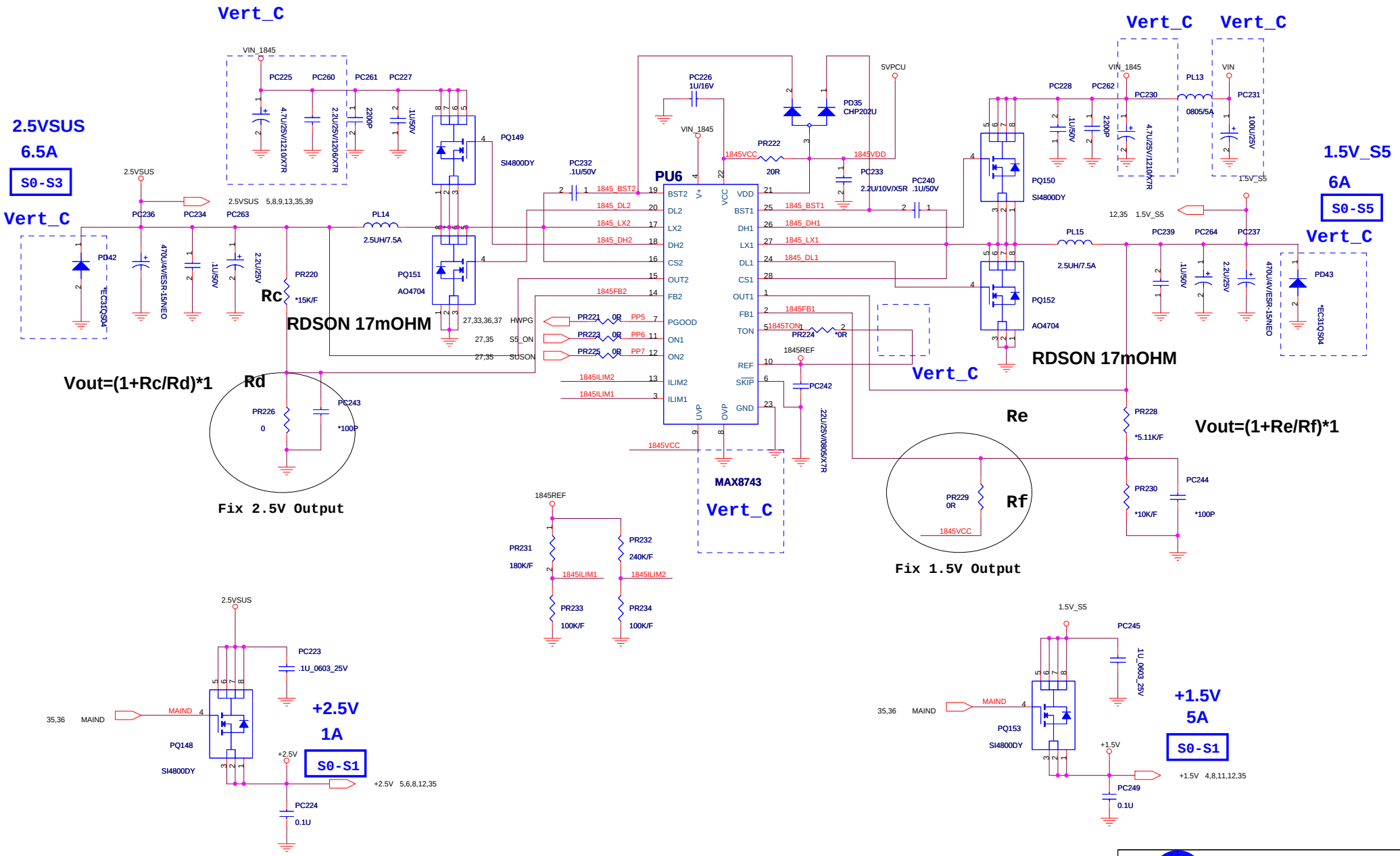
Vert_C
2.5VSUS
6.5A
S0-S3
Vert_C
VIN_1845
PC225
PC260
PC261
PC227
4.7U/25V/1210/X7R
2.2U/25V/1206/X7R
2200P
.1U/50V
PQ149
SI4800DY
PC232
.1U/50V
PU6
PC226
1U/16V
VIN_1845
PR222
20R
1845VCC
1845VDD
PD35
CHP202U
5VPCU
PC233
2.2U/10V/X5R
PC240
.1U/50V
1845_BST2
1845_DL2
1845_LX2
1845_DH2
1845_BST1
1845_DH1
1845_LX1
1845_DL1
1845FB2
1845FB1
1845TON
1845REF
1845ILIM2
1845ILIM1
PR221 0R PP5
PR223 0R PP6
PR224 *0R
PR225 0R PP7
27,33,36,37 HWPG
27,35 S5_ON
27,35 SUSON
BST2
DL2
LX2
DH2
CS2
OUT2
FB2
PGOOD
ON1
ON2
ILIM2
ILIM1
VDD
BST1
DH1
LX1
DL1
CS1
OUT1
FB1
TON
REF
SKIP
GND
UVP
OVP
V+
VCC
MAX8743
Vert_C
PC242
.22U/25V/0805/X7R
2.5VSUS
PC236
PC234
PC263
2.5VSUS 5,8,9,13,35,39
PL14
2.5UH/7.5A
PD42
*EC3Q/S04
470U/4V/ESR-15/NEO
.1U/50V
2.2U/25V
PR220
*15K/F
Rc
PQ151
AO4704
RDSON 17mOHM
Vout=(1+Rc/Rd)*1
Rd
PR226
0
PC243
*100P
Fix 2.5V Output
1845REF
PR231
180K/F
PR232
240K/F
1845ILIM1
1845ILIM2
PR233
100K/F
PR234
100K/F
Vert_C
Vert_C
Vert_C
VIN_1845
PC228
PC262
PC230
PL13
0805/5A
VIN
PC231
100U/25V
1.5V_S5
6A
S0-S5
PQ150
SI4800DY
12,35 1.5V_S5
PL15
2.5UH/7.5A
PC239
PC264
PC237
Vert_C
PD43
*EC3Q/S04
PQ152
AO4704
RDSON 17mOHM
Vert_C
Re
PR228
*5.11K/F
Vout=(1+Re/Rf)*1
PR229
0R
Rf
1845VCC
PR230
*10K/F
PC244
*100P
Fix 1.5V Output
2.5VSUS
PC223
.1U_0603_25V
35,36 MAIND
MAIND
PQ148
SI4800DY
+2.5V
1A
S0-S1
+2.5V
+2.5V 5,6,8,12,35
PC224
0.1U
1.5V_S5
PC245
.1U_0603_25V
35,36 MAIND
MAIND
PQ153
SI4800DY
+1.5V
5A
S0-S1
+1.5V
+1.5V 4,8,11,12,35
PC249
0.1U
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number 2.5VSUS / 1.5V_S5
Rev 2A
Date: Monday, December 27, 2004
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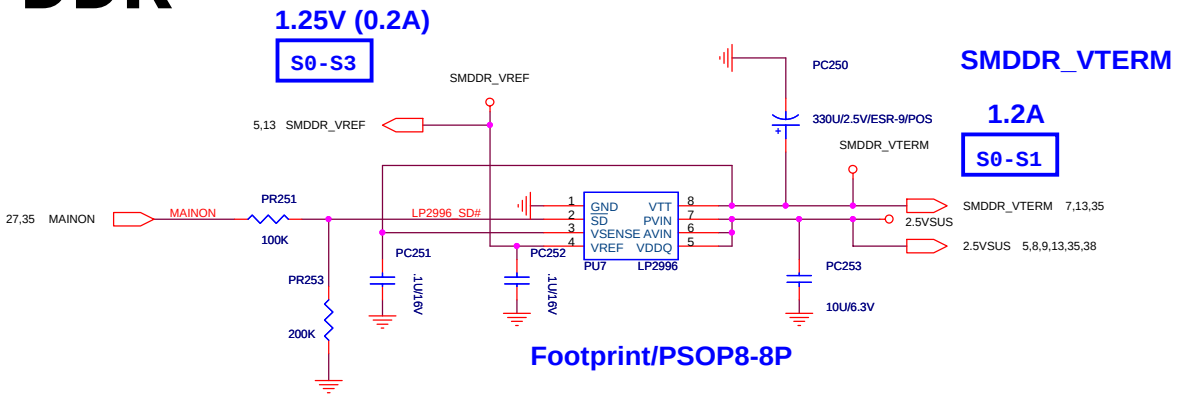
DDR



PROJECT : CT3

Quanta Computer Inc.

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