

Compal confidential

Schematics Document

Mobile AMD S1G2 CPU with ATI
RX781(NB) & SB700(SB) core logic

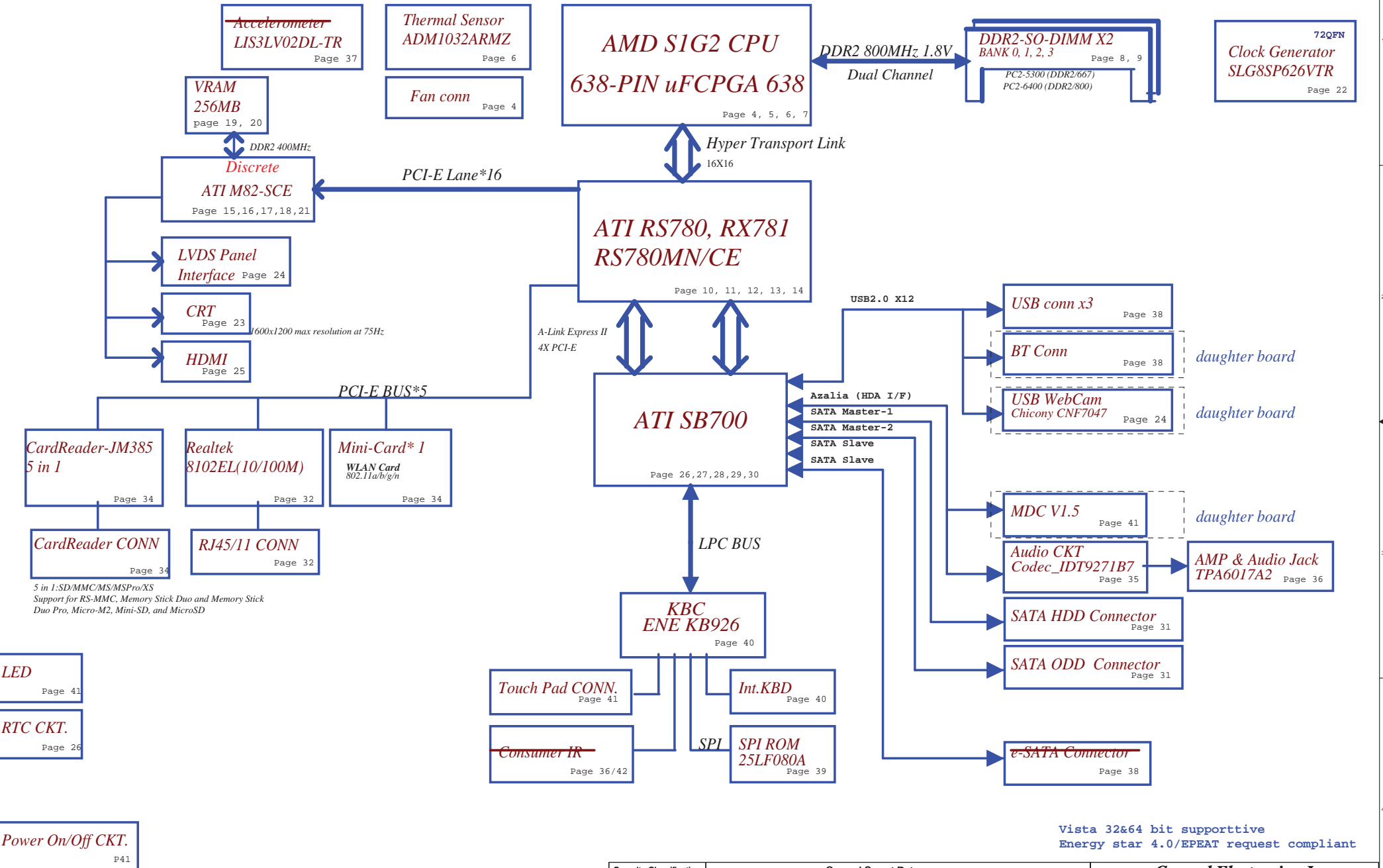
2008-05-14

REV:1.0



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OPP Rachman AMD 14" Discrete - LA-4112P



Vista 32&64 bit supporttive
Energy star 4.0/EPEAT request compliant

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Voltage Rails ○ MEANS ON X MEANS OFF

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

power plane / State	+B +3VL +5VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_0 +CPU_CORE_1 +CPU_CORE_NB
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

EC SM Bus1 address

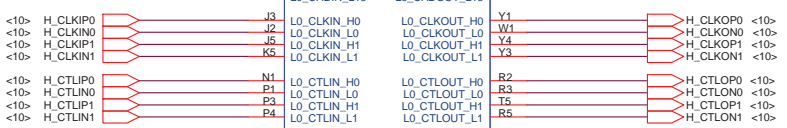
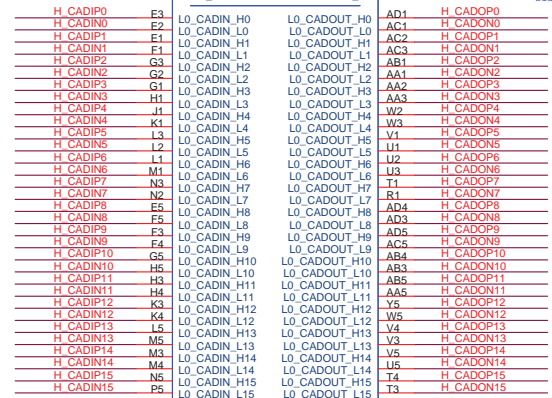
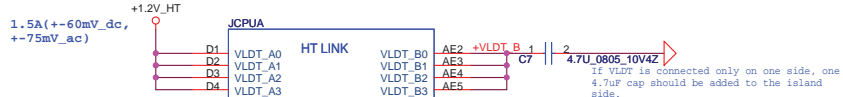
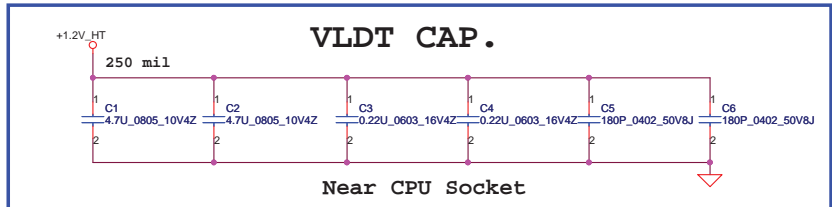
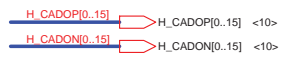
EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	ADI1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b	ADI1032-1 VGA	98H	1001 100X b
CPU SIC interface	98H	1001 100X b			

SMBUS Control Table

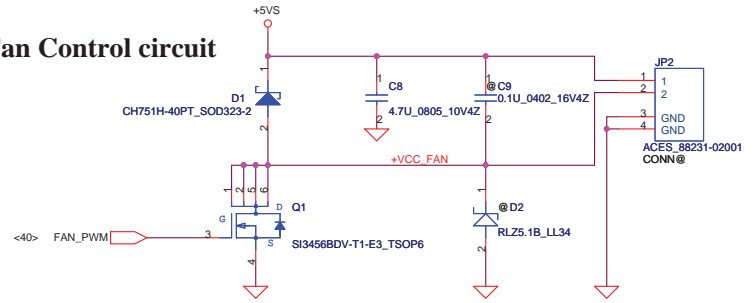
	SOURCE	THERMAL SENSOR VGA M82-SE ADM1032	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	WL MINI CARD Slot 1	LCD	HDMI	CRT	Q-Sensor
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_CK2	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_DA2	KB926	V	X	X	V	X	X	X	X	X	X	X
SCL	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
SDA	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
DDC4CLK	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC4DATA	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC3CLK	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
DDC3DATA	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
SCL0	SB700	X	X	X	X	V	V	X	X	X	X	V
SDA0	SB700	X	X	X	X	V	V	X	X	X	X	V
SCL1	SB700	X	X	X	X	X	X	V	X	X	X	X
SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

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FOX_P26382A-284S-41F_GRIFFIN
 CONN@
 Athlon 64 S1
 Processor Socket

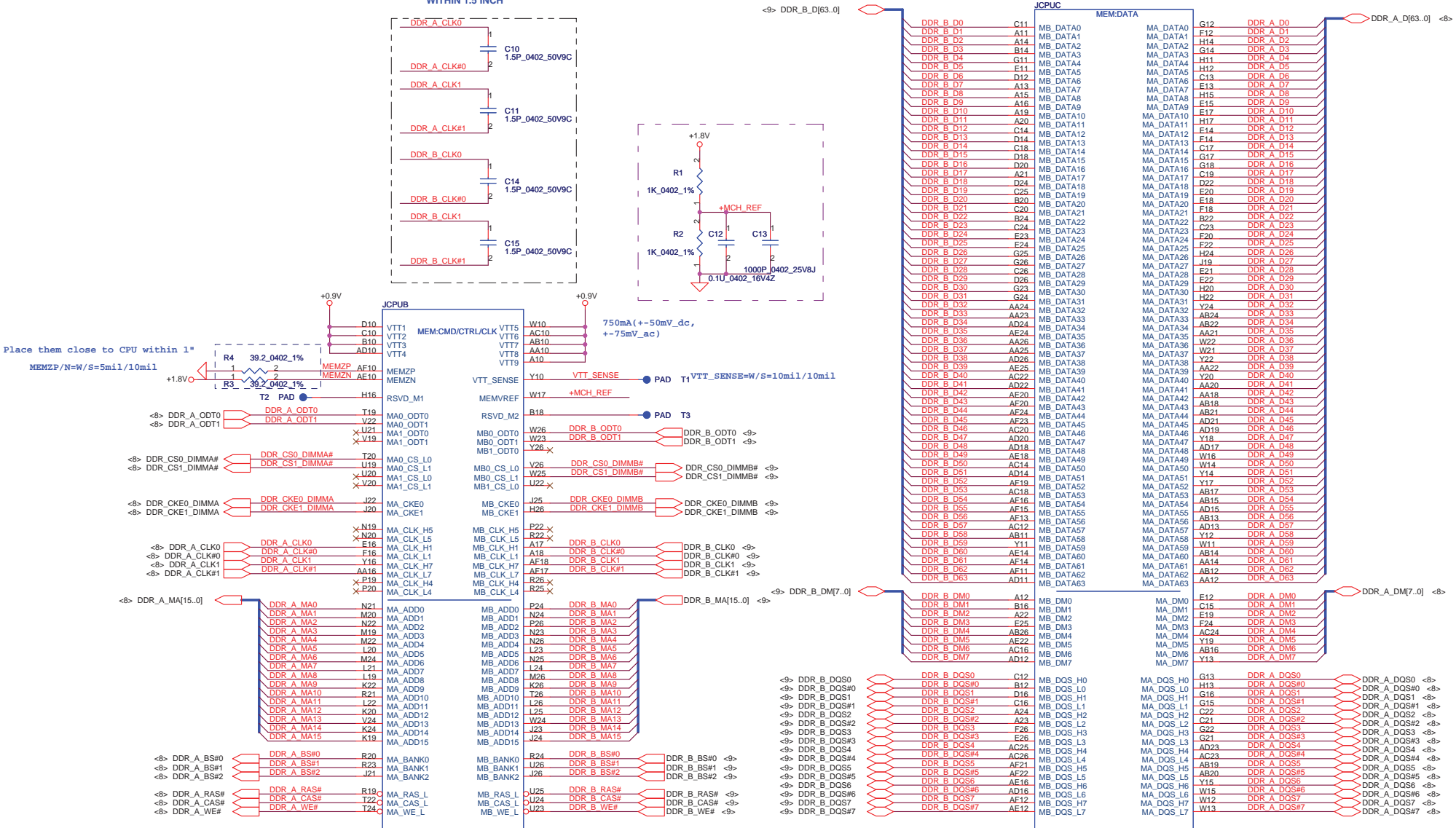
PWM Fan Control circuit



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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

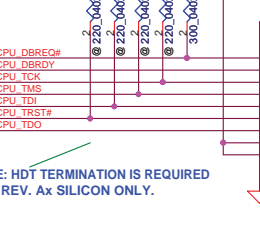
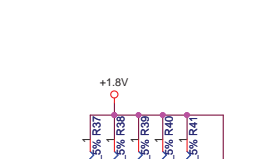
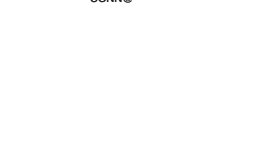
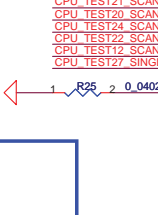
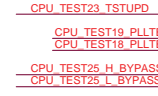
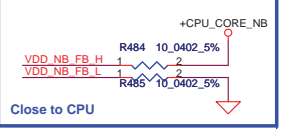
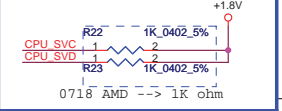
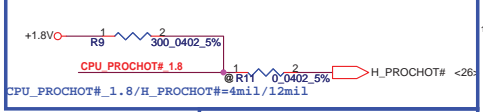
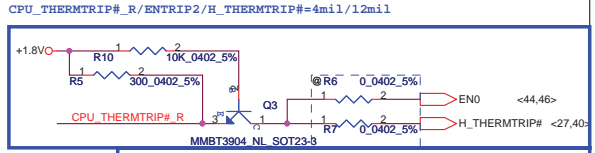
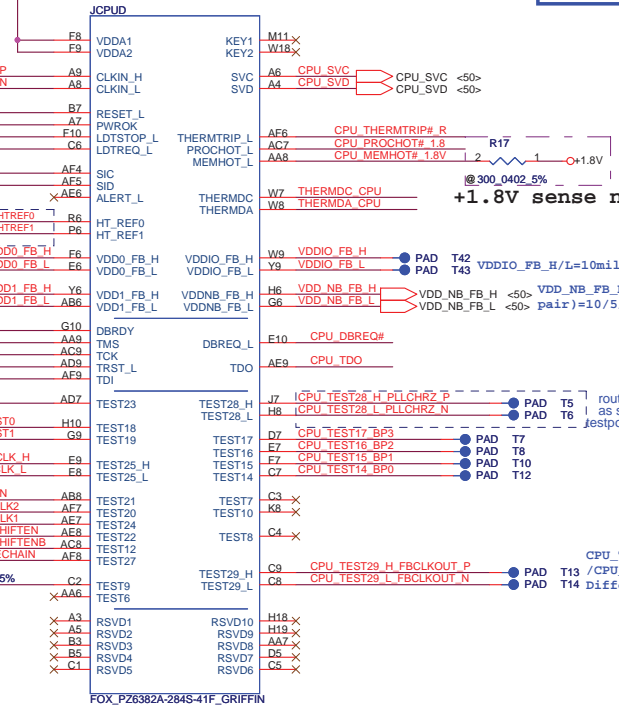
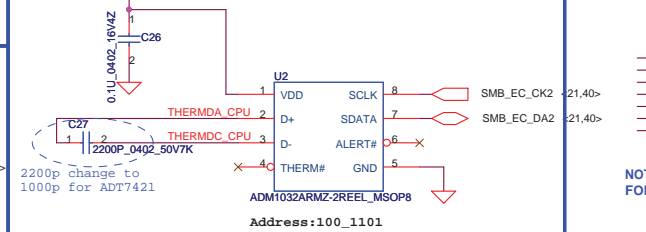
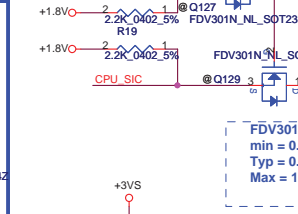
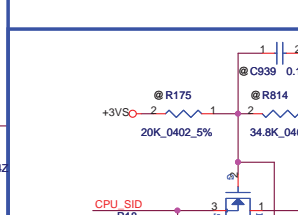
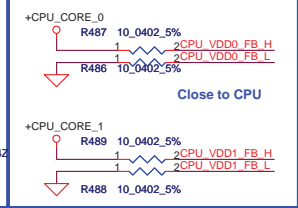
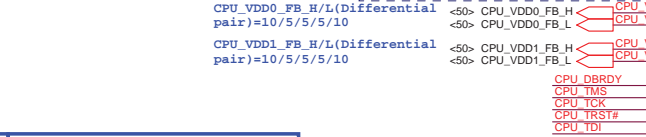
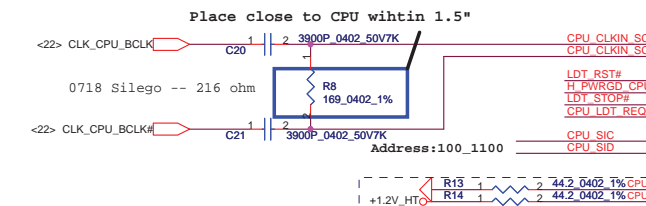
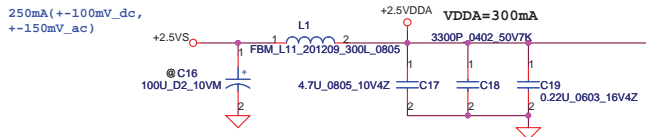


Place them close to CPU within 1"

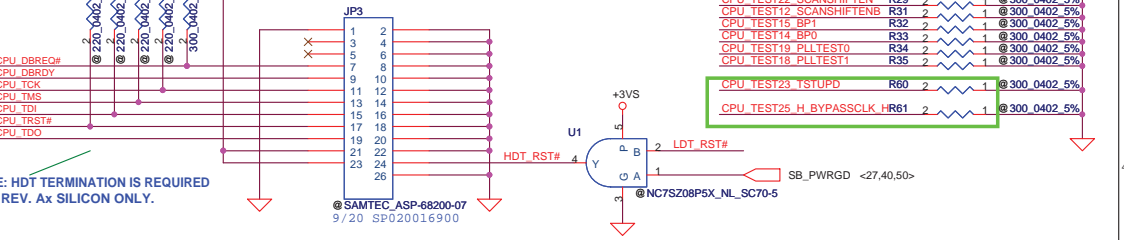
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Athlon 64 S1
Processor
Socket
CONN@

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HDT Connector

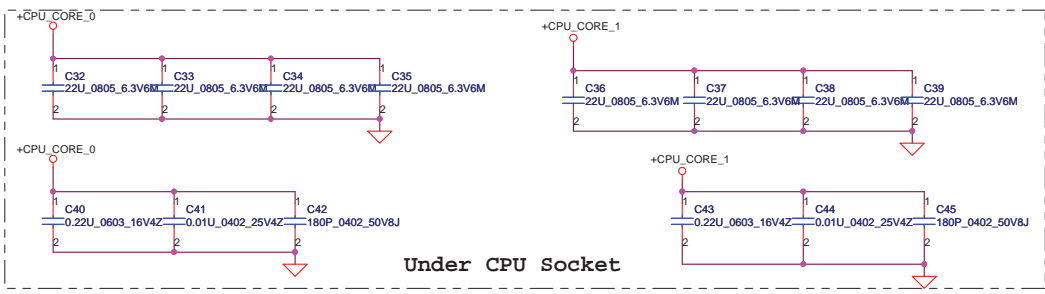
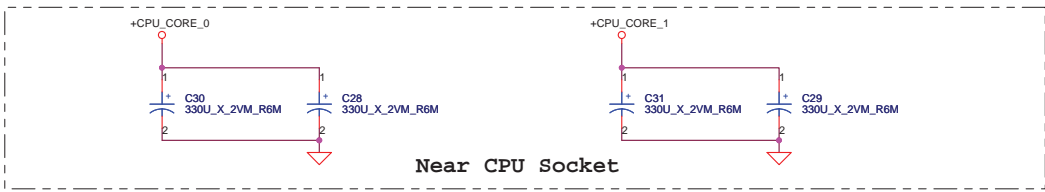


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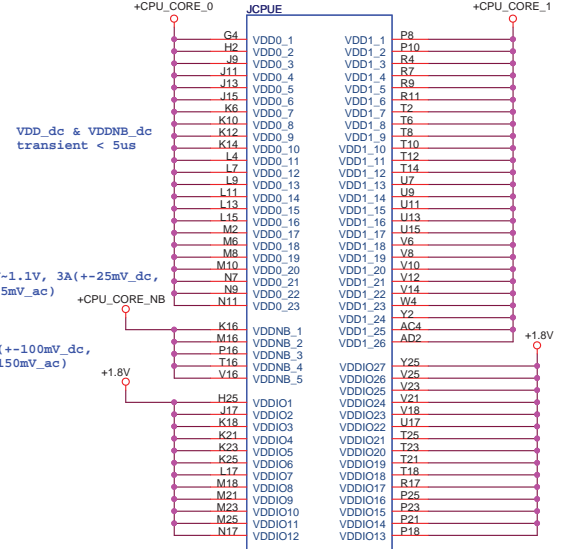
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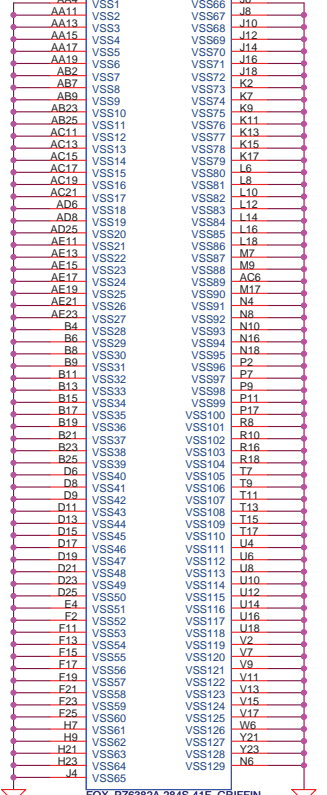
VDD(+CPU_CORE) decoupling.



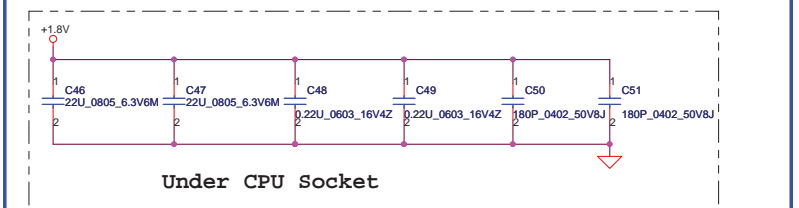
18A/7200mil/36vias
+CPU_CORE_0



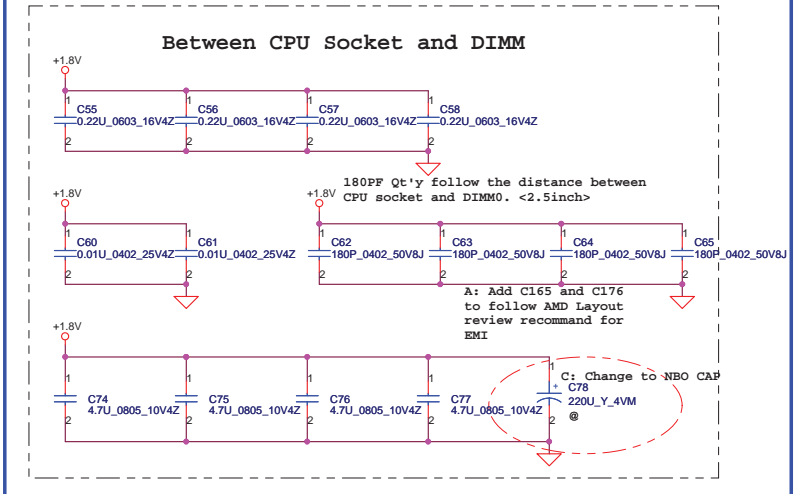
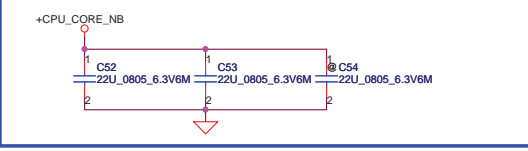
18A/7200mil/36vias
+CPU_CORE_1



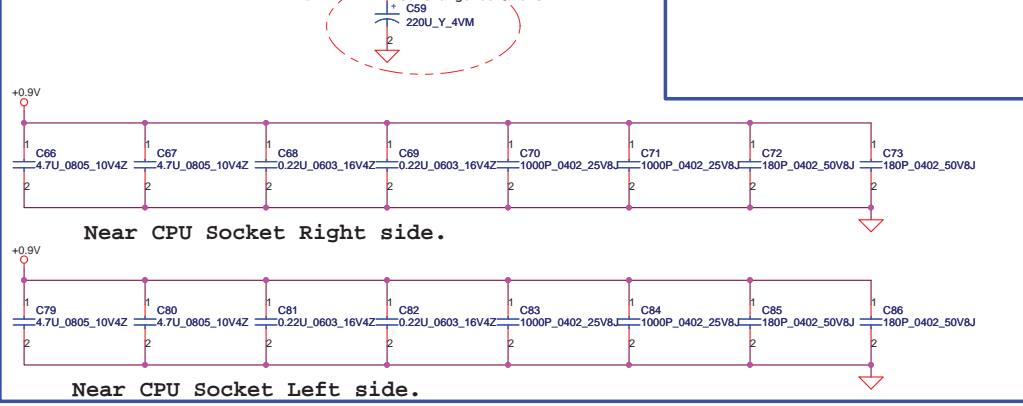
VDDIO decoupling.



+CPU_CORE_NB decoupling.



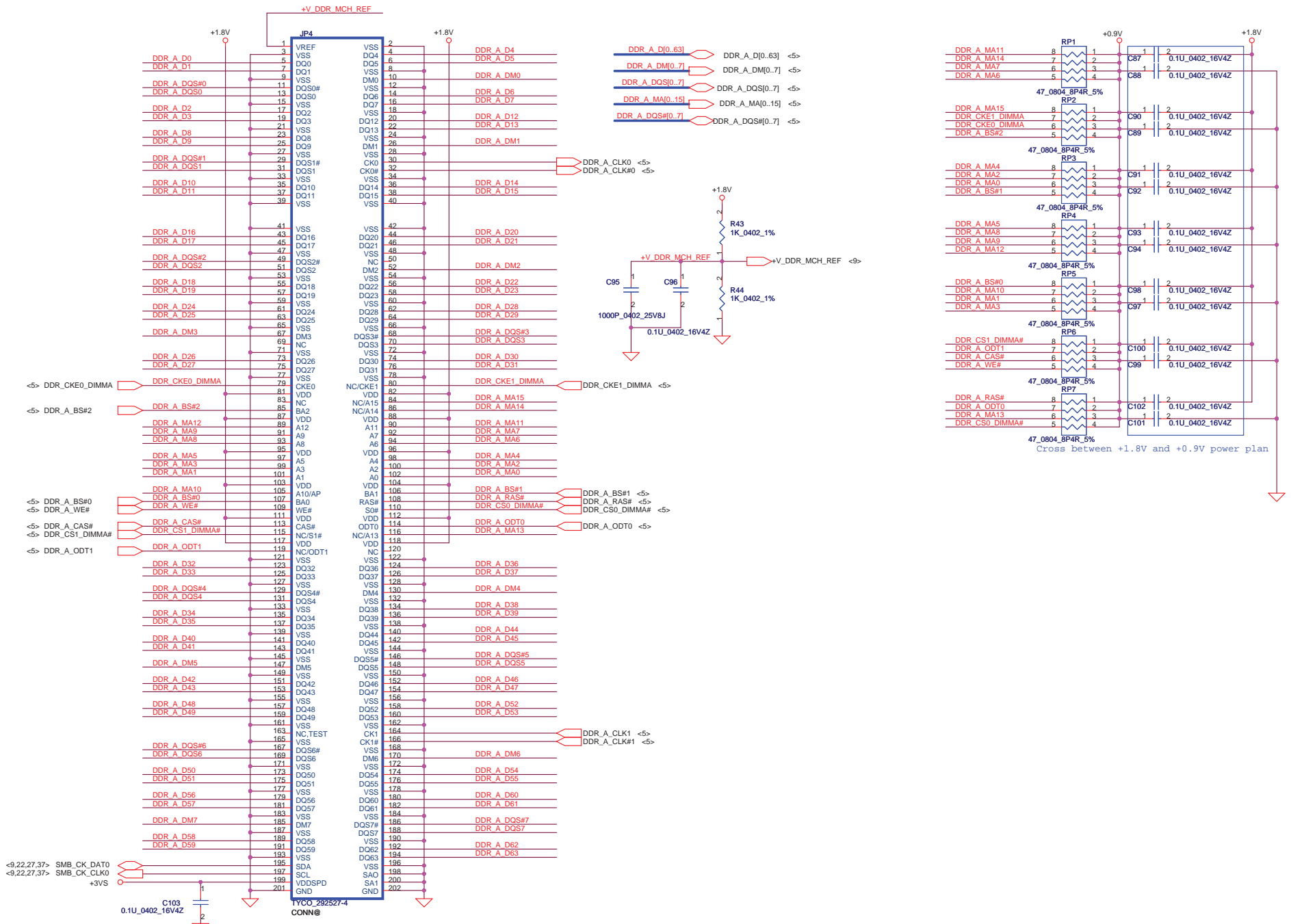
VTT decoupling.



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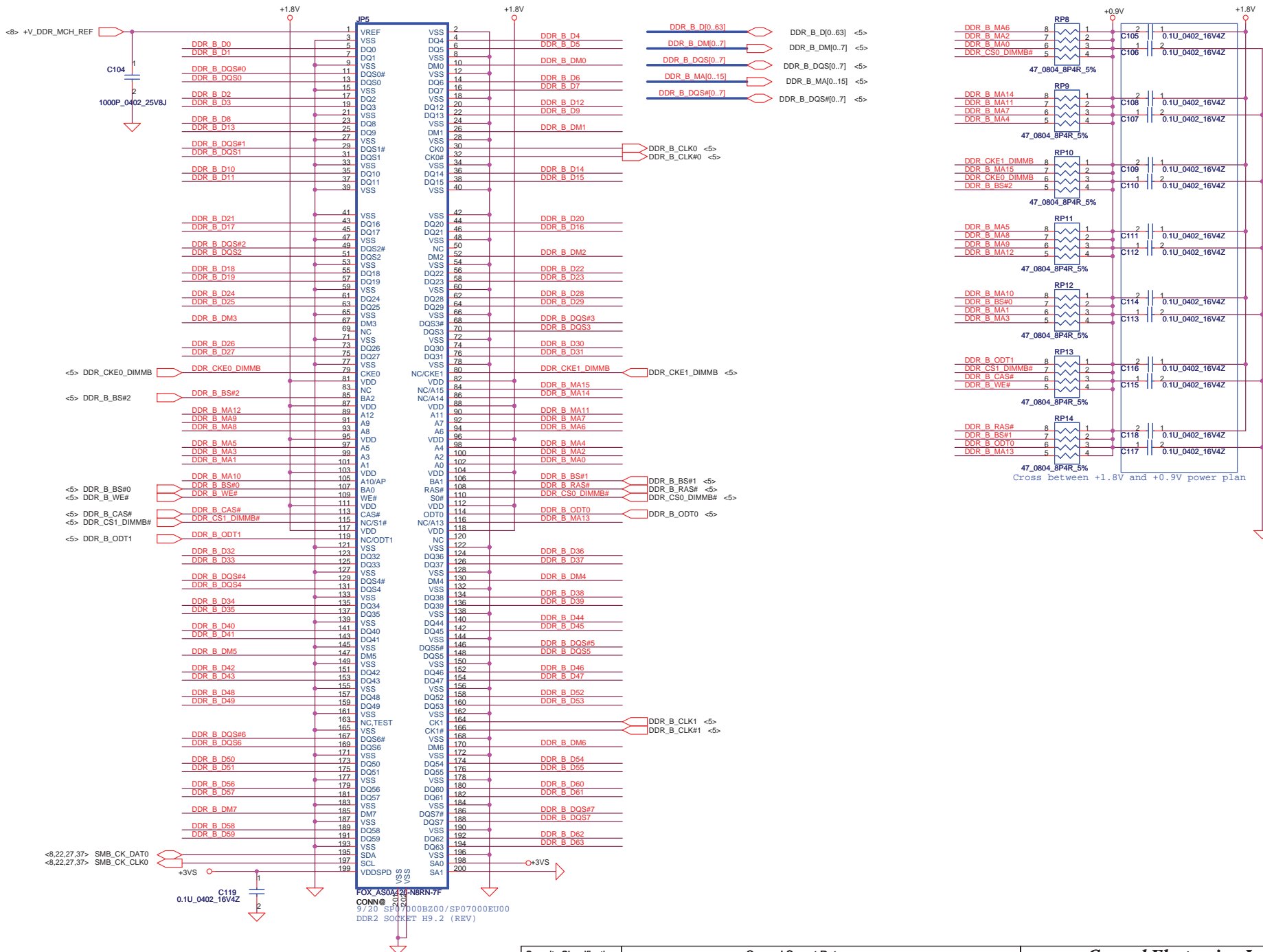
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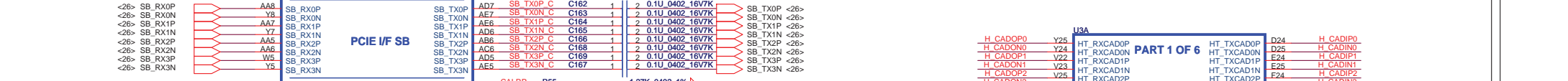
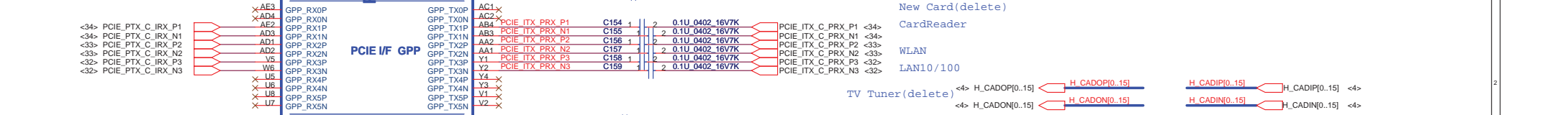
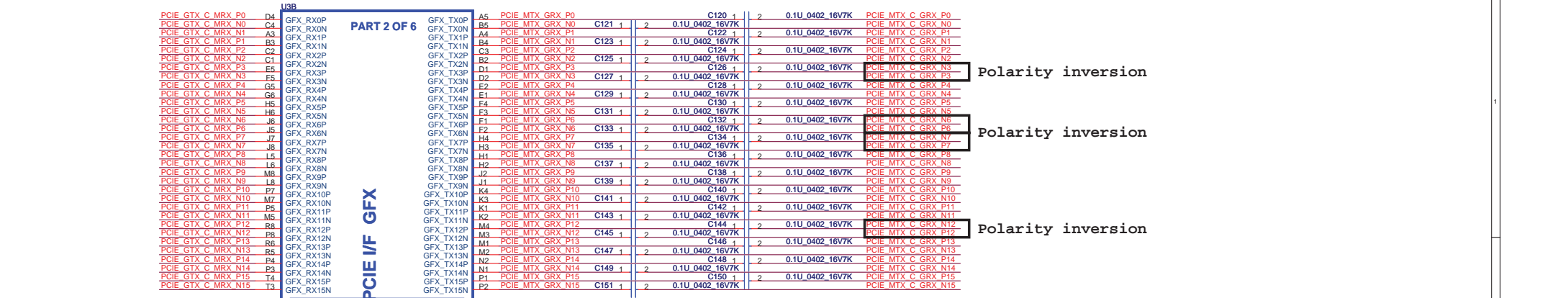
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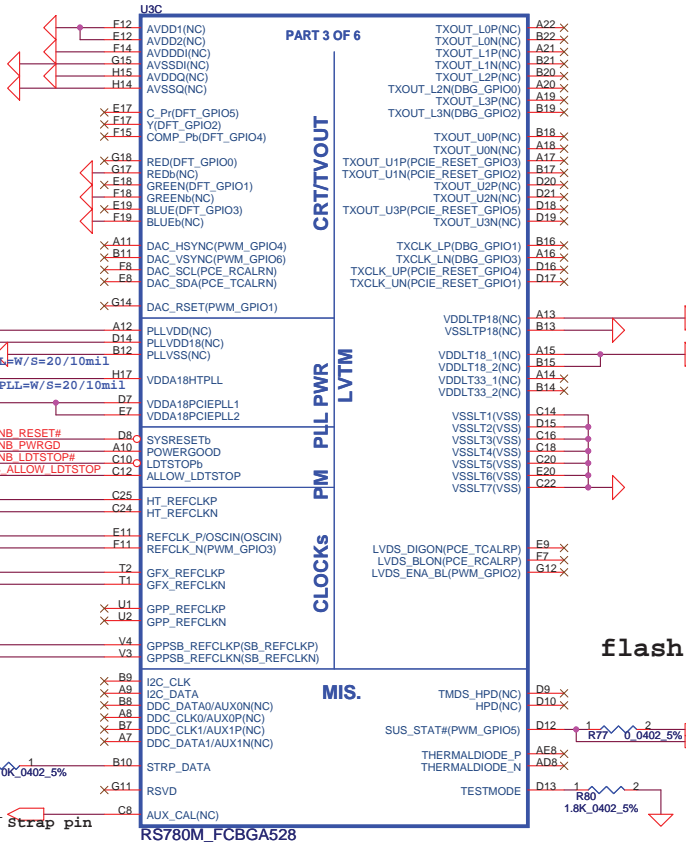
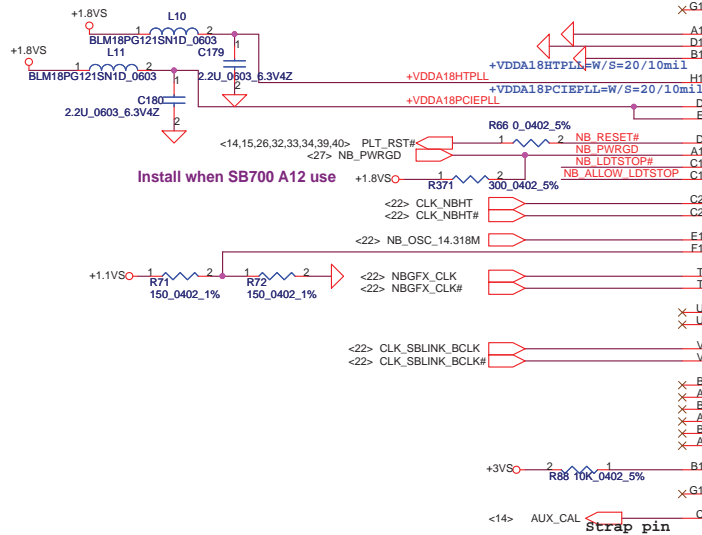
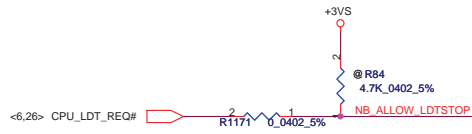
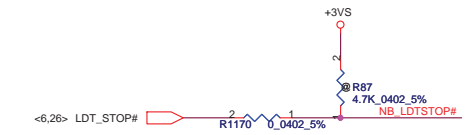


RS780M Display Port Support (muxed on GFX)

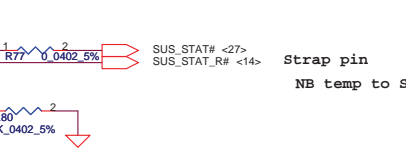


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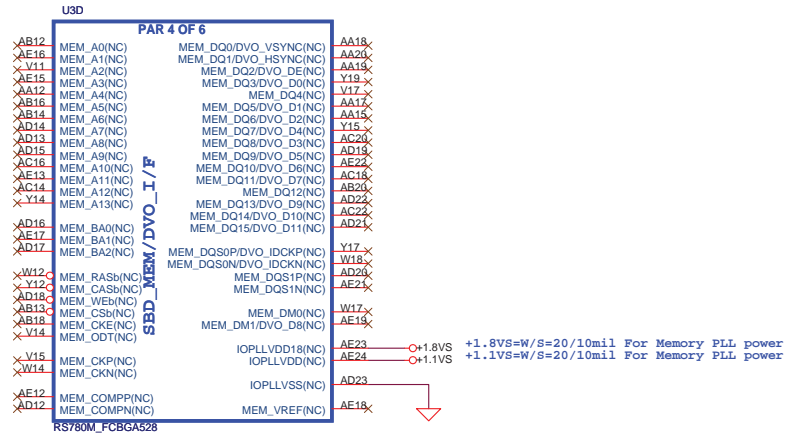




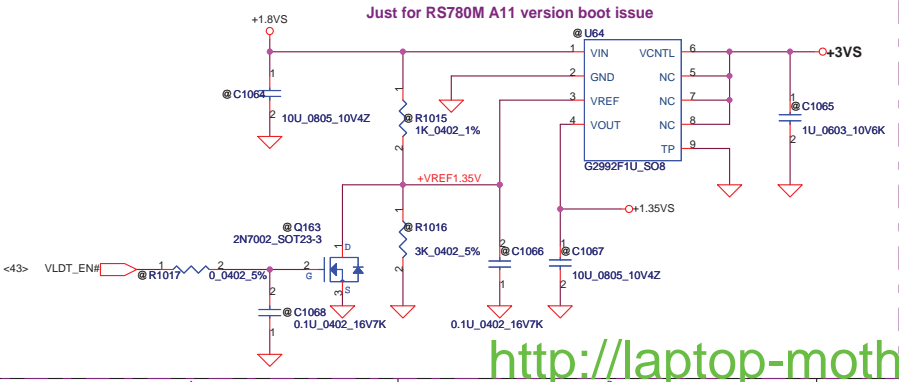
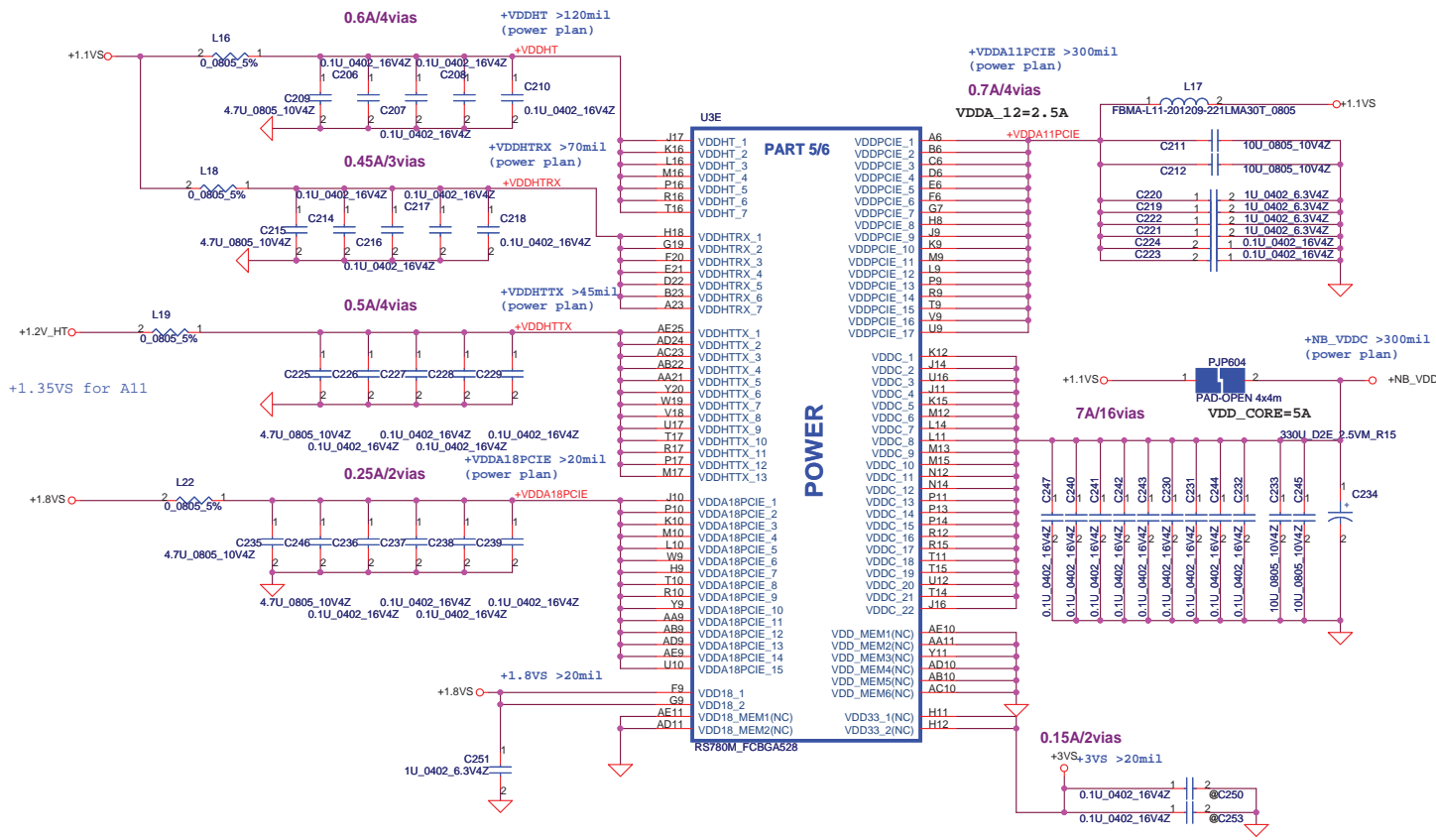
flash issue check IALAA



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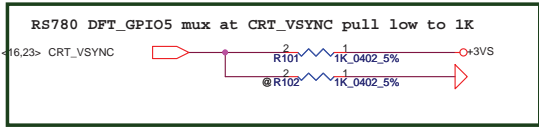
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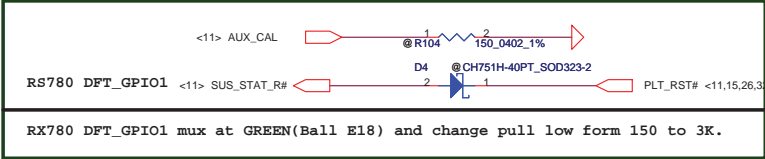
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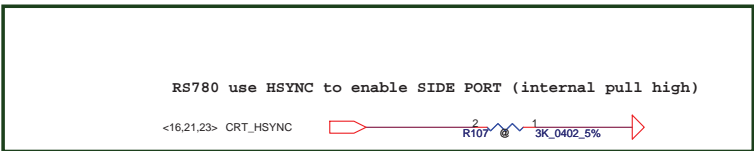
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
 1 : Disable (RS740) Enable (RX780, RS780)
 0 : Enable (Rs740) Disable (RX780, RS780)
 PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#



DFT_GPIO1:LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use Default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

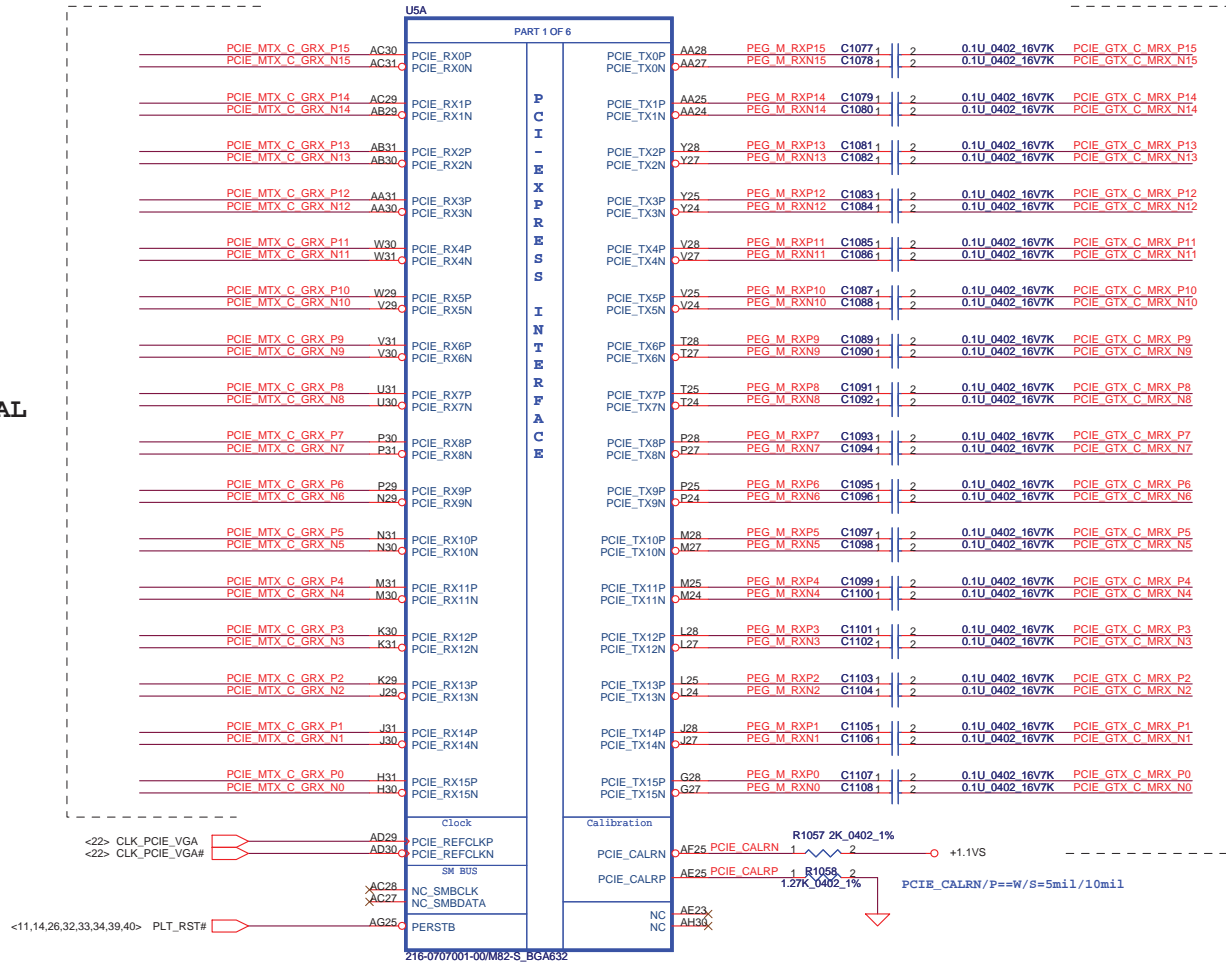
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 1. Disable (RS740/RS780)
 0 : Enable (RS740/RS780)

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<10> PCIE_GTX_C_MRX_P[0..15] ← PCIE GTX C MRX P[0..15]
 <10> PCIE_GTX_C_MRX_N[0..15] ← PCIE GTX C MRX N[0..15]
 <10> PCIE_MTX_C_GRX_P[0..15] ← PCIE MTX C GRX P[0..15]
 <10> PCIE_MTX_C_GRX_N[0..15] ← PCIE MTX C GRX N[0..15]

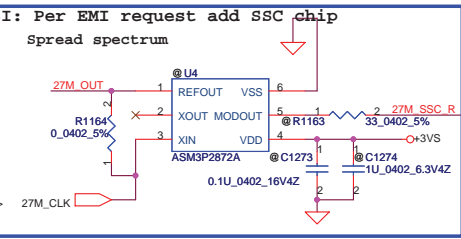
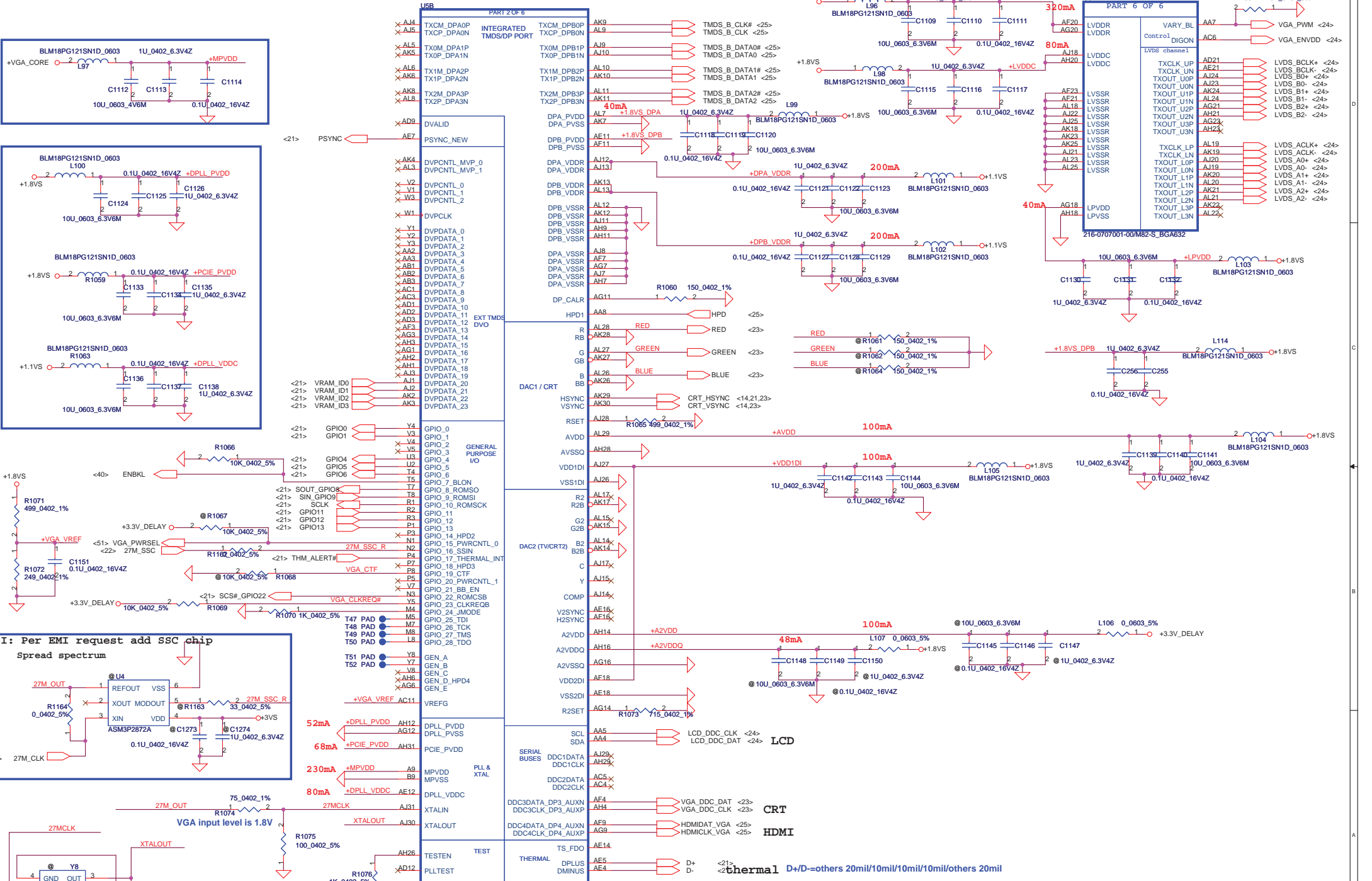
PCIE LANE REVERSAL

PCIE LANE REVERSAL



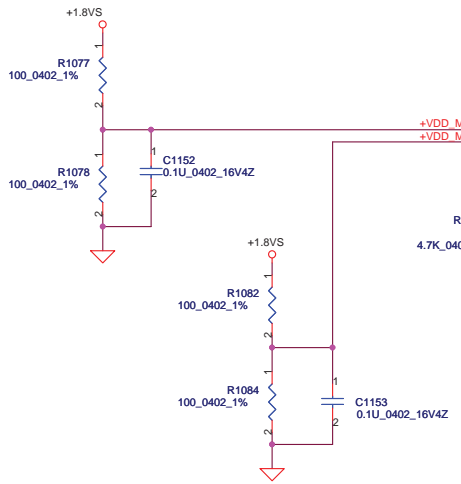
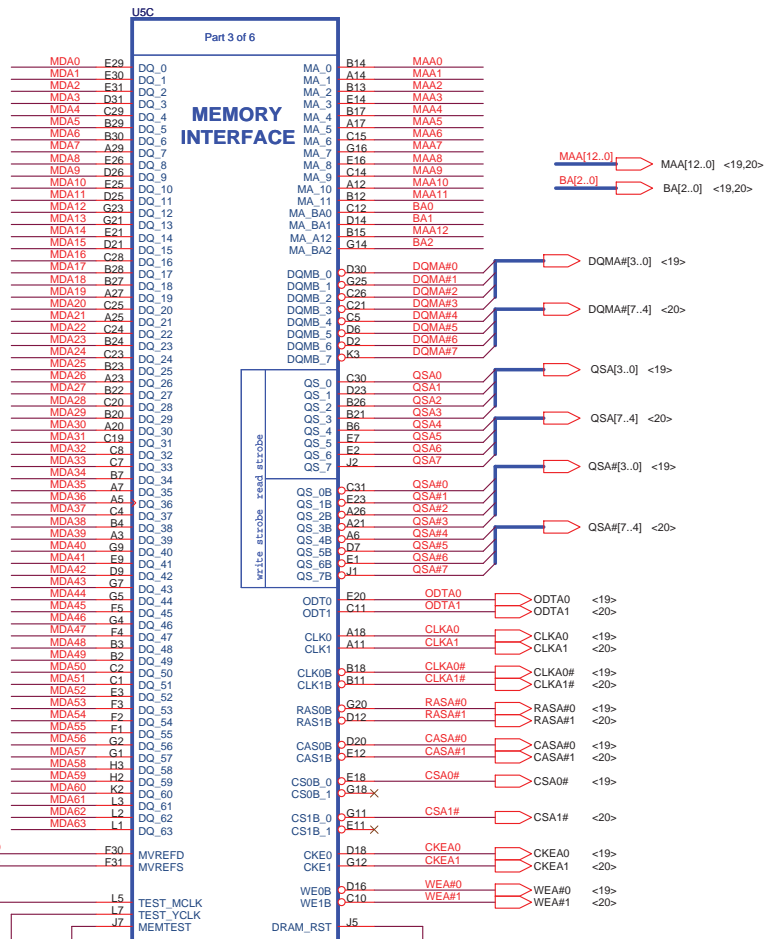
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polarity swap for ATI commond



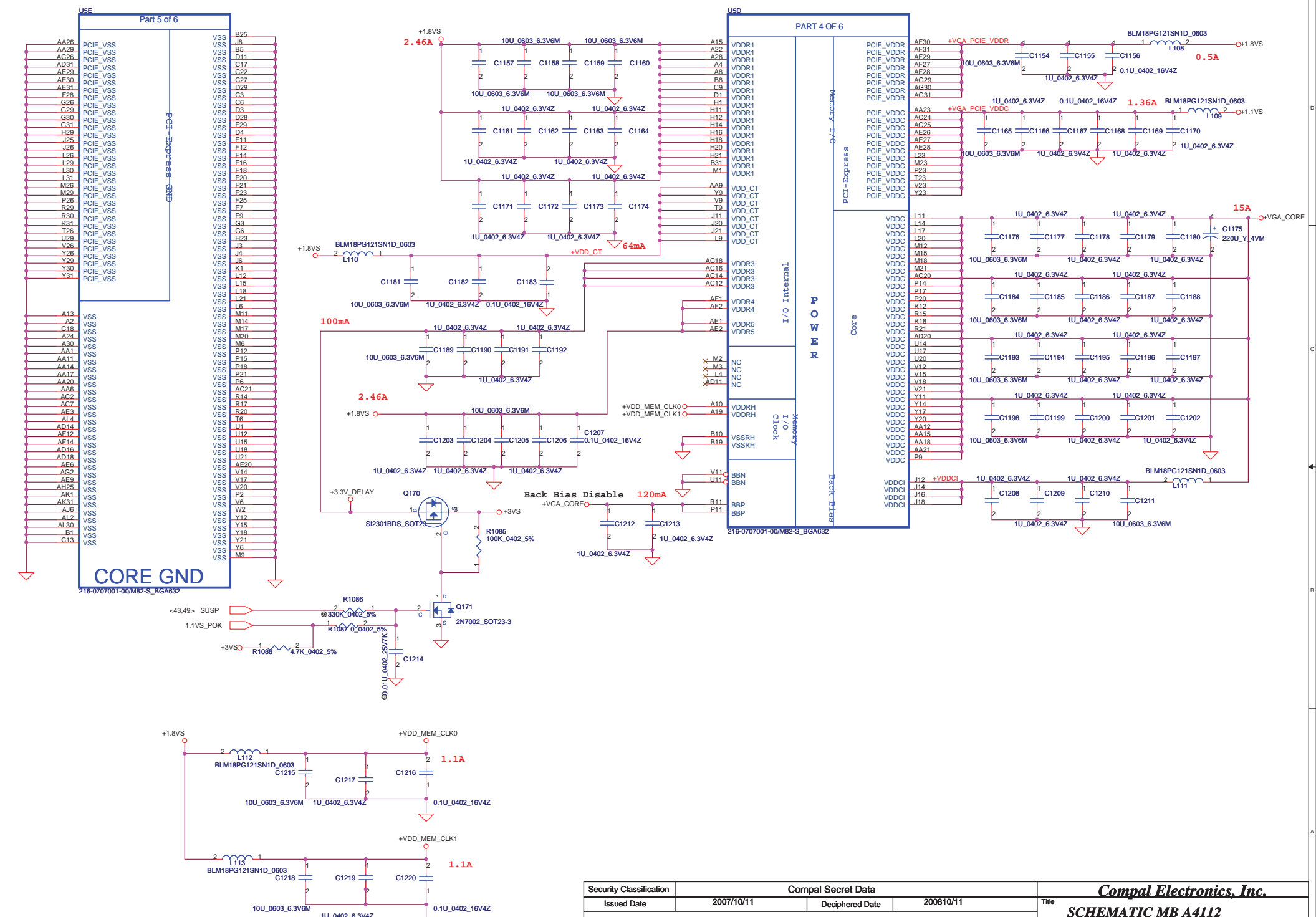
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<20> MDA[63..32] ← MDA[63..32]
 <19> MDA[31..0] ← MDA[31..0]



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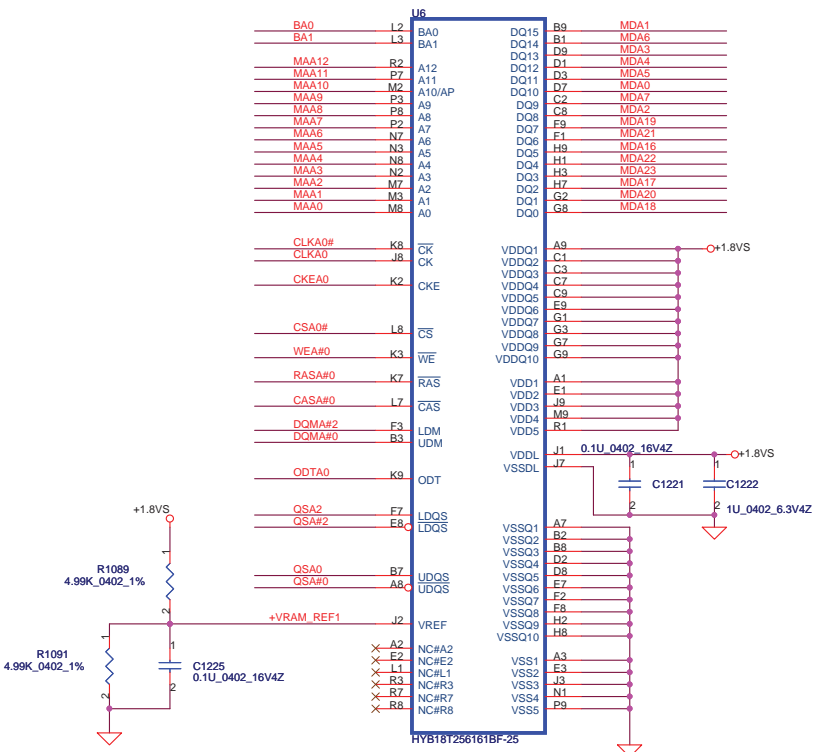


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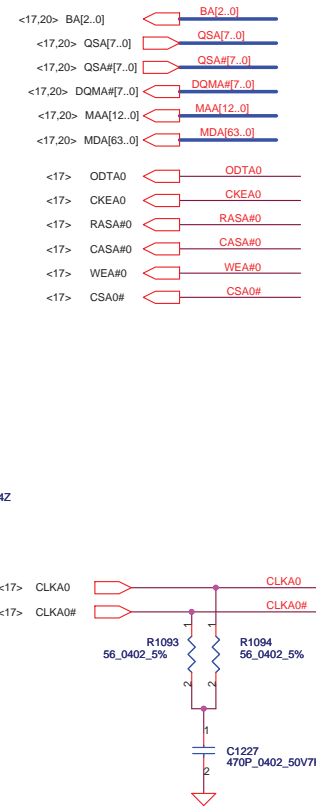
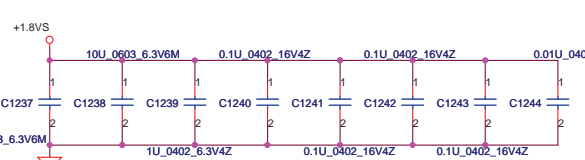
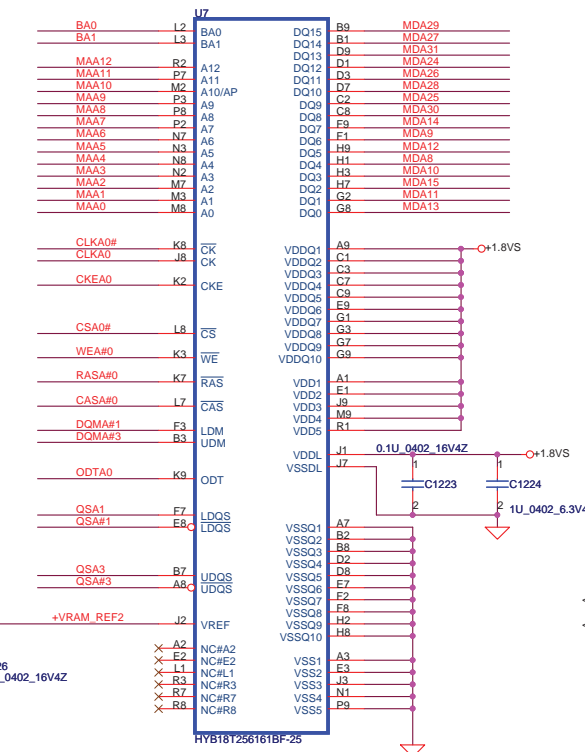
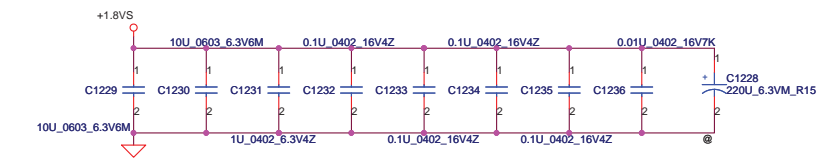
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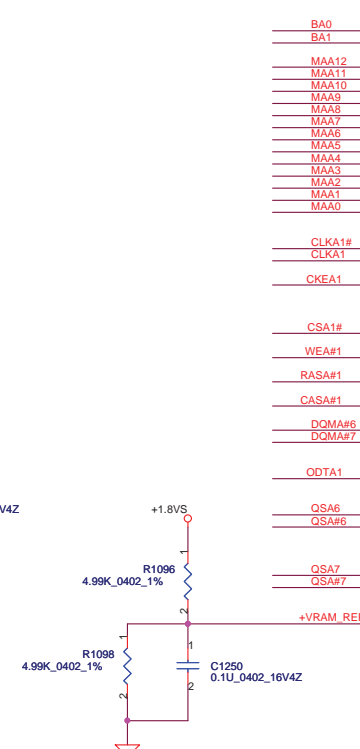
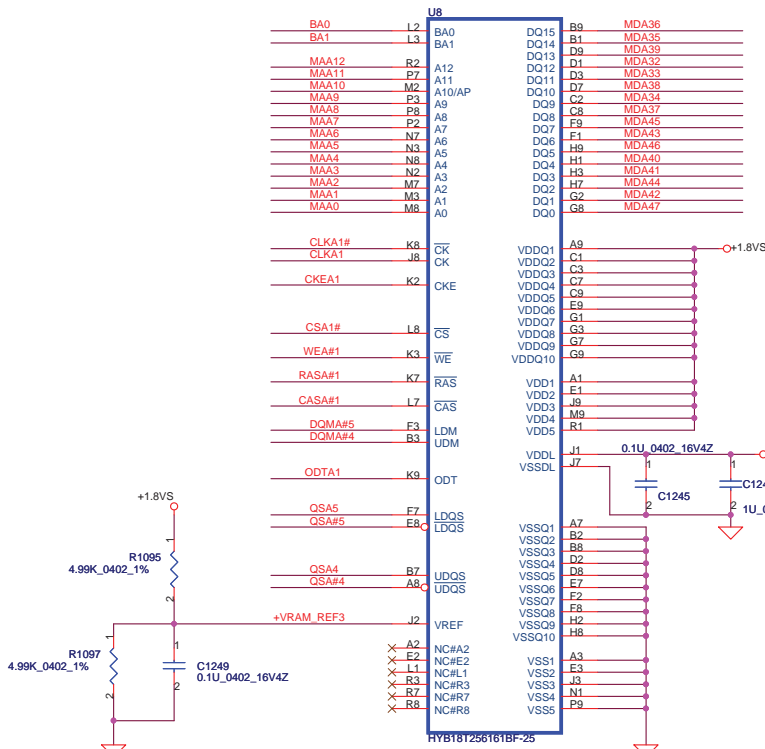
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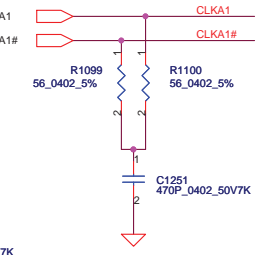
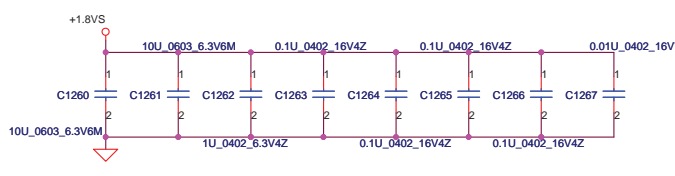
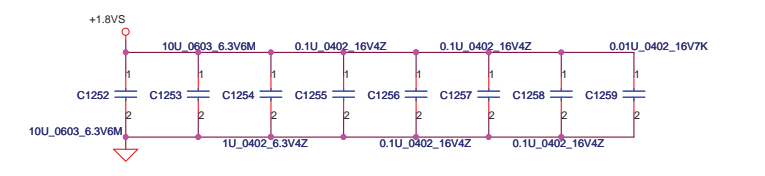


SA00002A600(QIMONDA) S IC D2 32M16/500 HYB18T512161B2F-20 84P
 SA00002AJ10(SAMSTUNG) IC D2 32M16/500 K4N51163QG-HC20 FBGA84



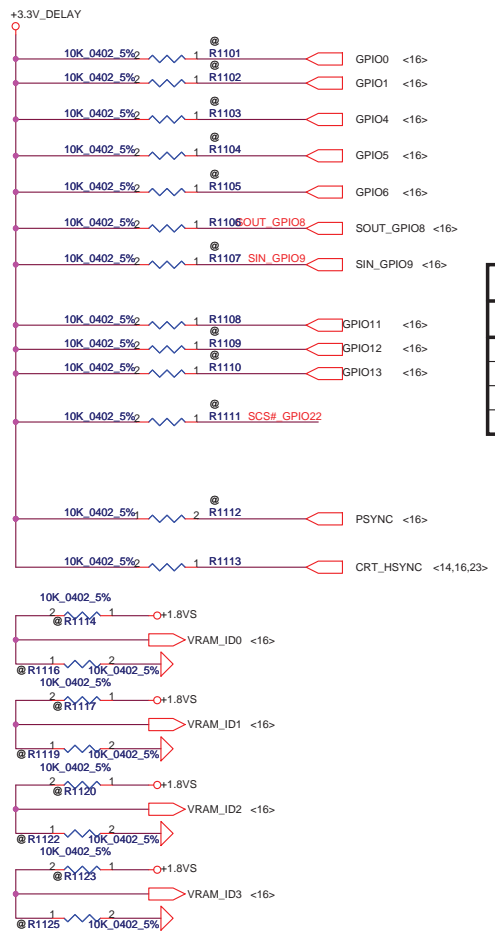


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- <17,19> DQMA#[7..0] DQMA#[7..0]
- <17,19> MAA[12..0] MAA[12..0]
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- <17,19> QSA[7..0] QSA[7..0]
- <17,19> MDA[63..0] MDA[63..0]
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- <17> CKEA1 CKEA1
- <17> RASA#1 RASA#1
- <17> CASA#1 CASA#1
- <17> WEA#1 WEA#1
- <17> CSA1# CSA1#



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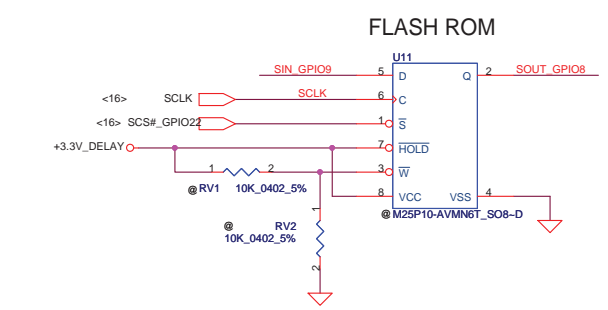
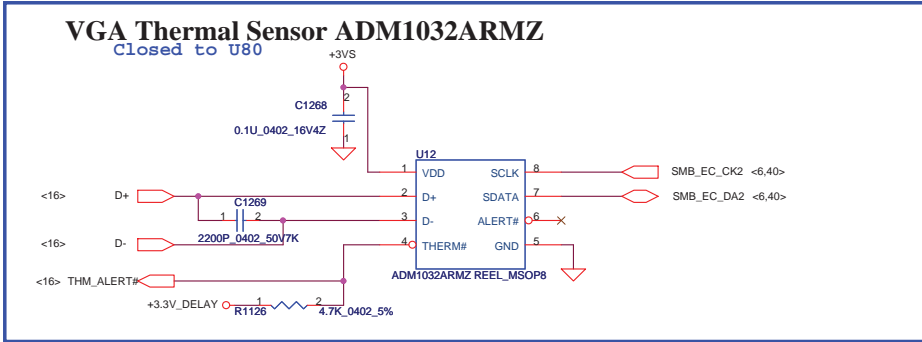
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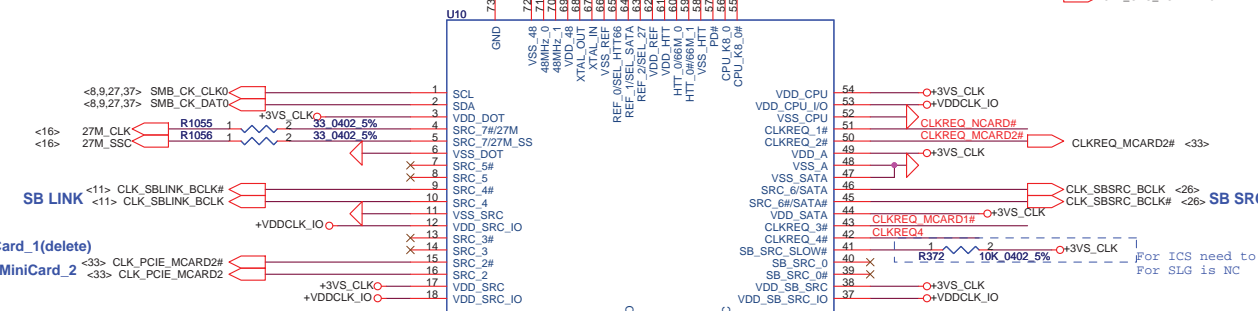
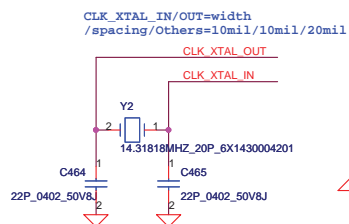
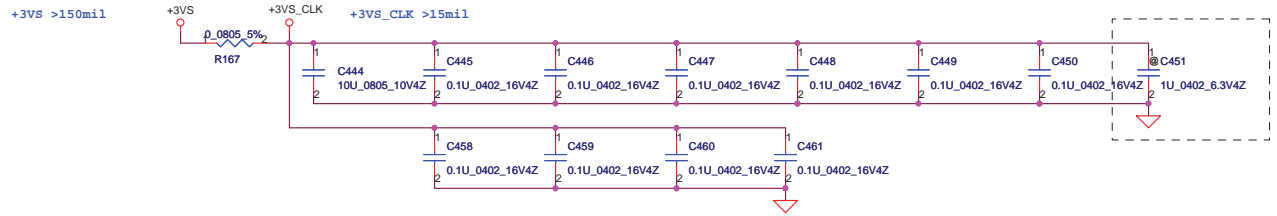
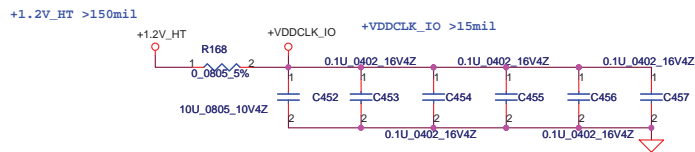
GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	MEMORY SIZE
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
			VRAM_ID 3,2,1,0
			Samsung 64Mx16 1.8V
			Samsung 32Mx16 1.8V
			Hynix 64Mx16 1.8V
			Hynix 32Mx16 1.8V
			Qimonda 32Mx16 1.8V
			Qimonda 64Mx16 1.8V
BIF_VGA_DIS	PSYNC	VGA ENABLED==0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1
			500MHz DVPDATA (23,22,21,20)

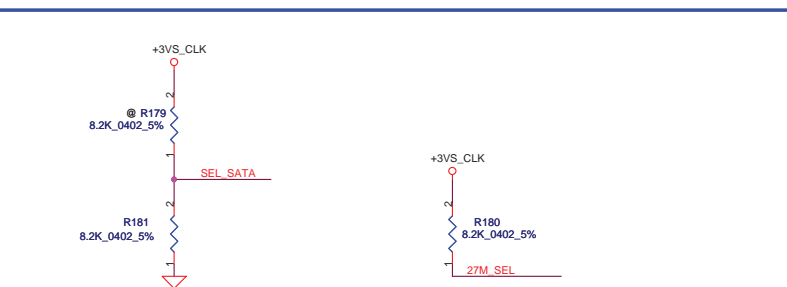
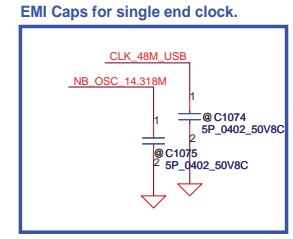
ATI RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESE	
GPIO2	GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GENERICC	GPIO21_BB_EN GPIO_28_TDO



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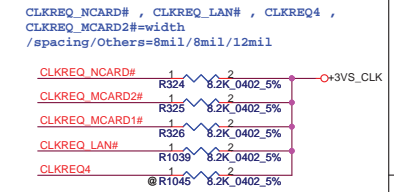
OSC_14M_NB	
RS780	1.1V 158R/90.0R



SEL_SATA	1	configure as SATA output
	0	configure as normal SRC(SRC 6) output
* default		
27M_SEL	1	configure as 27M and 27M SS output
	0	configure as SRC 7 output
* default		

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0	configure as differential 100MHz output
* default		



NB CLOCK INPUT TABLE

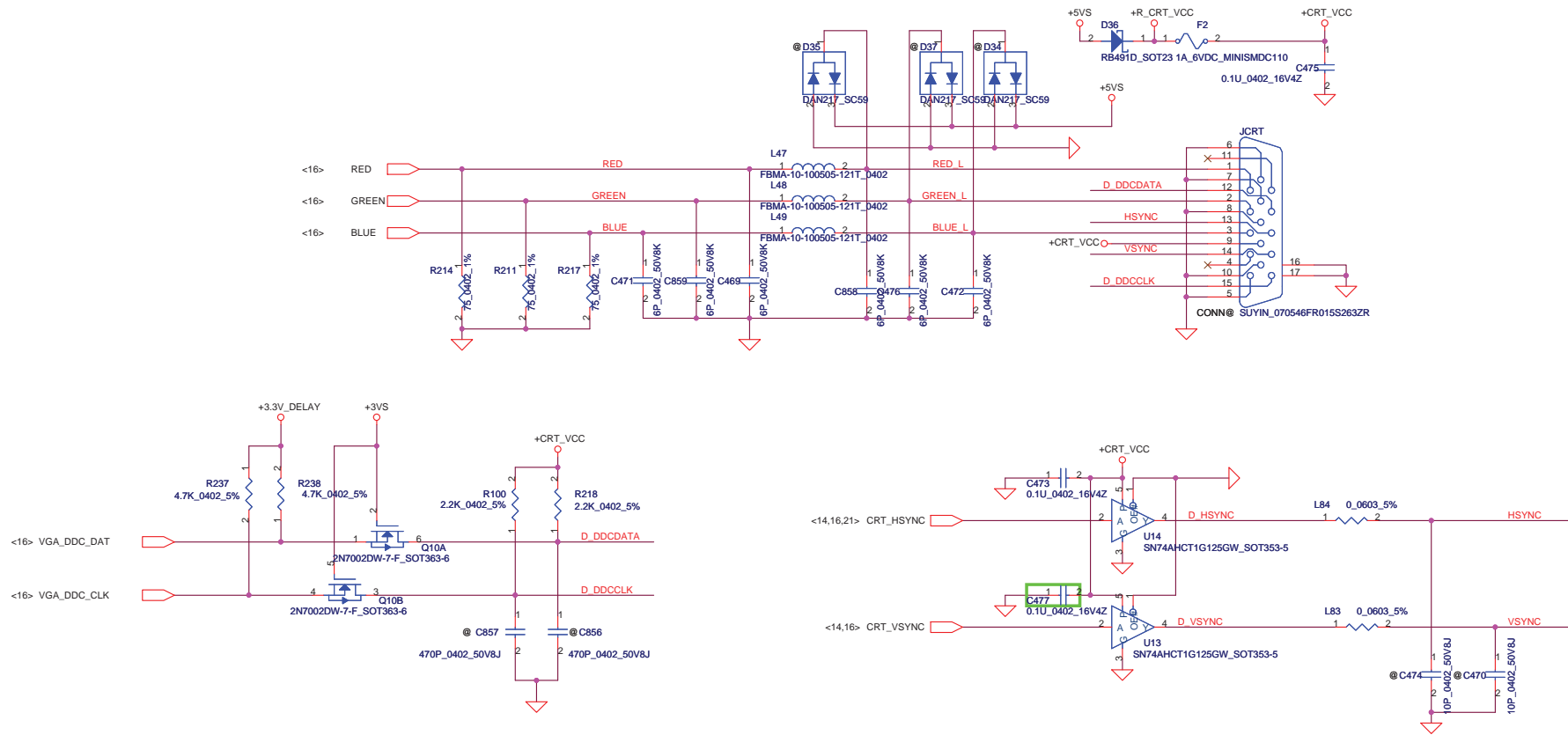
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P		
REFCLK_N	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF(N/OUT)*

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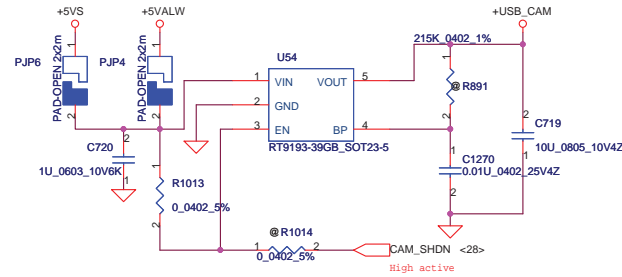
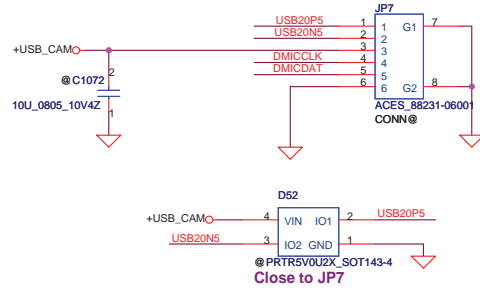
CRT CONNECTOR



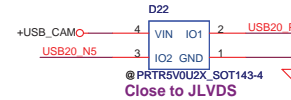
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WebCam+Digital Mic



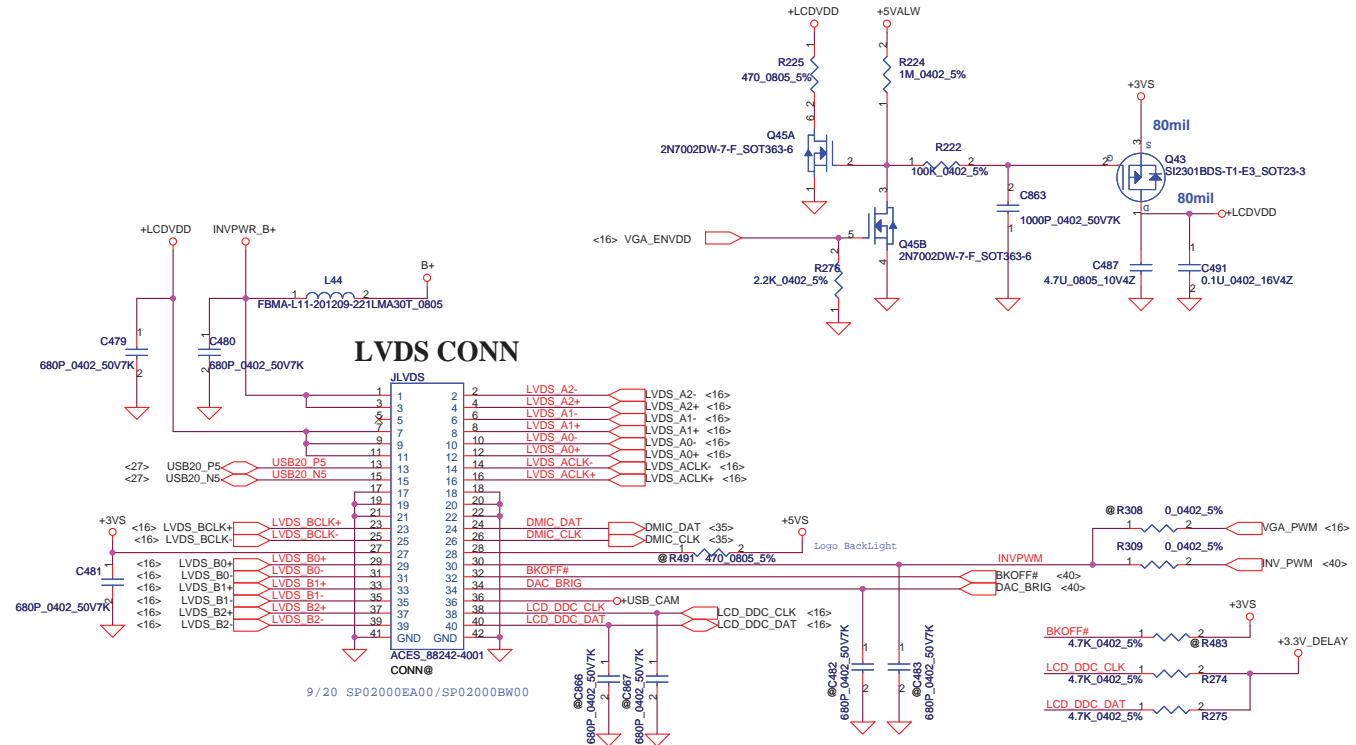
USB_VCCA is +3.9V, R892:100K; R891:215KKohm
G916 Vref=1.25V



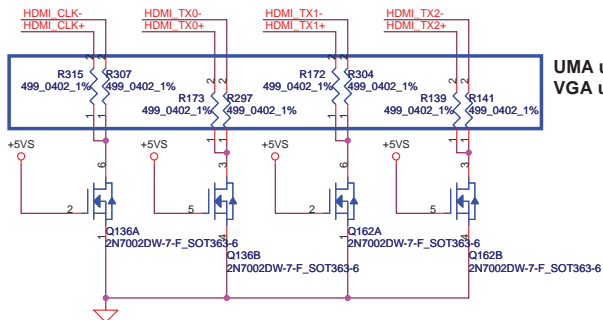
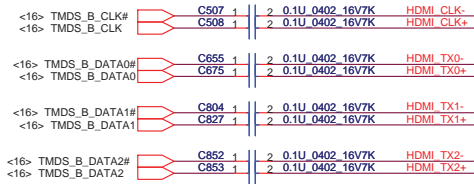
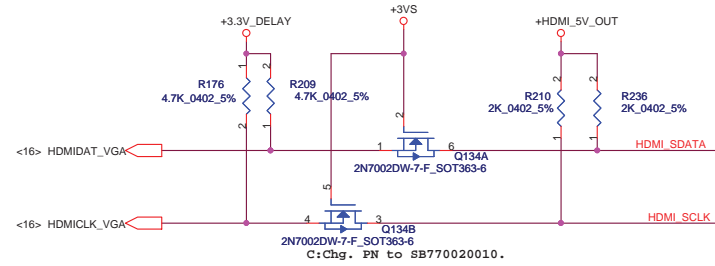
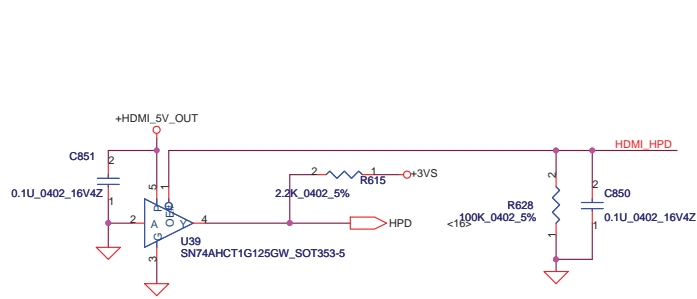
@R1027 0.0402_5%
USB20_P5 1
USB20N5 2
@R1028 0.0402_5%
USB20P5
USB20N5

@R1029 0.0402_5%
DMIC_CLK1 1
DMIC_CLK2 2
@R1030 0.0402_5%
DMICDAT
DMICCLK

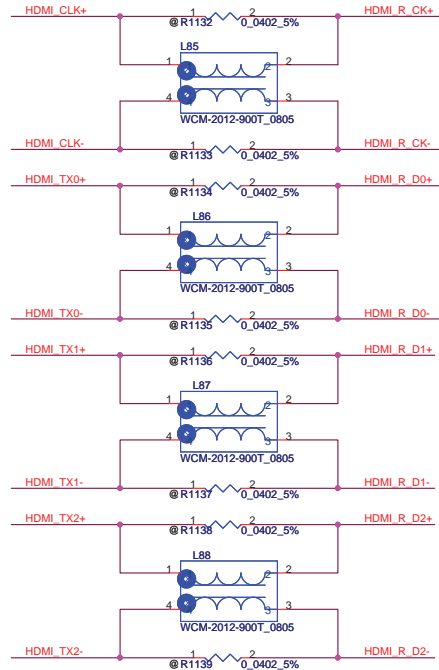
Close to JLVDS



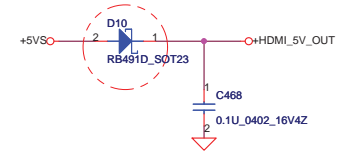
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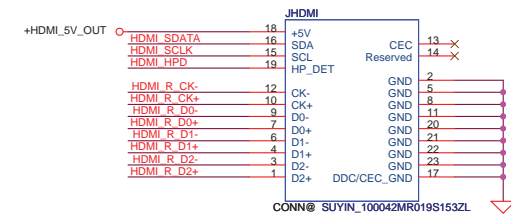
COMMON MODE CHECK is SM070000K00 KING_WCM-2012-900T_4P



MP:Update D10 to meet HDMI.



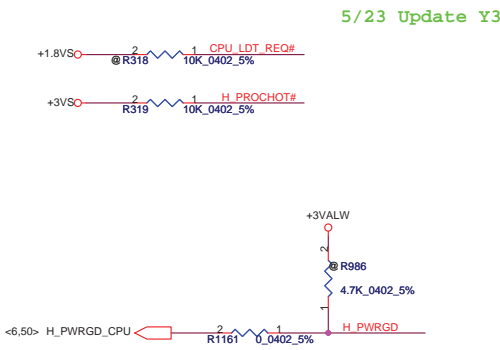
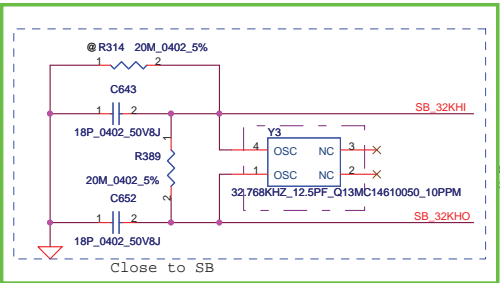
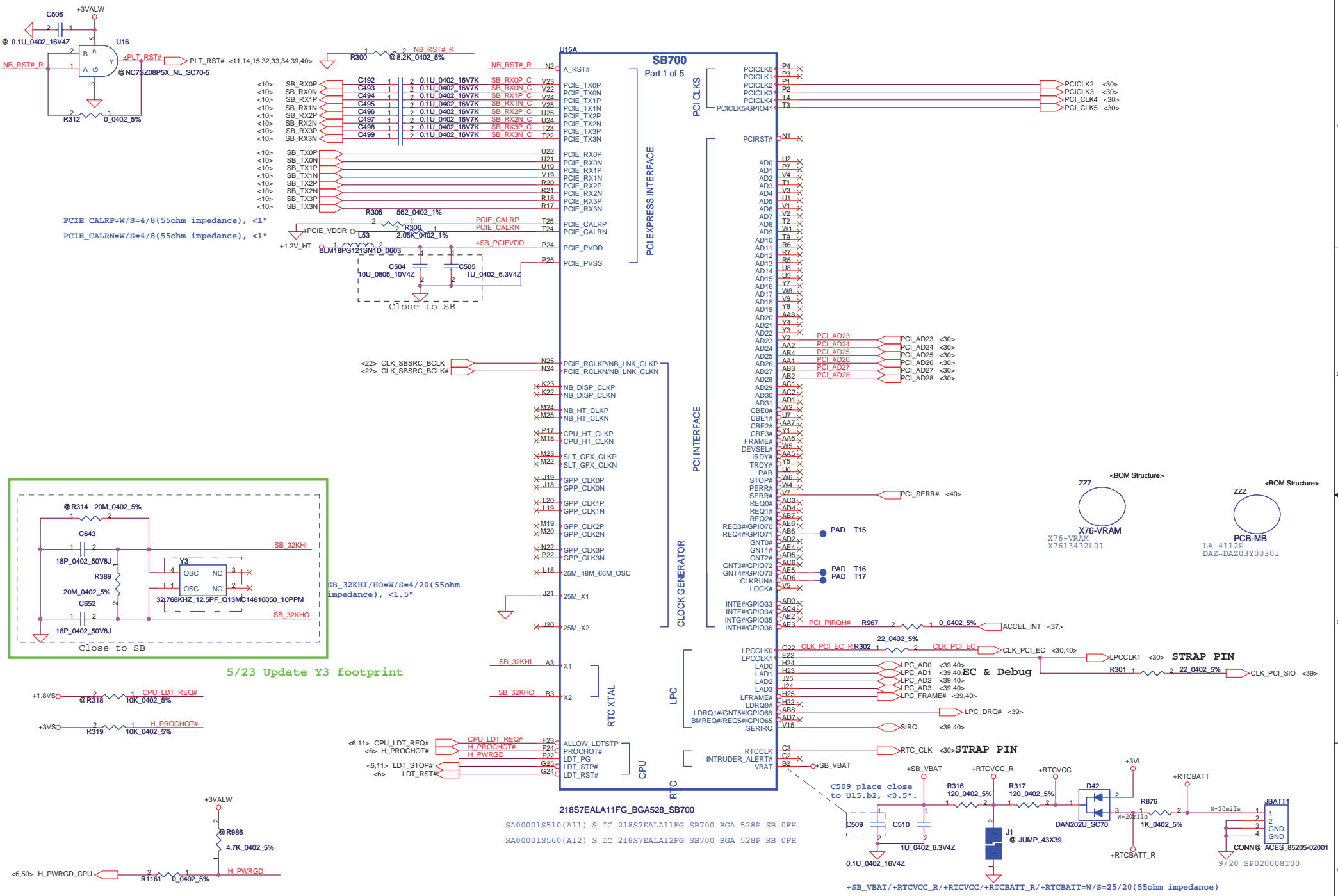
HDMI Connector



CONN@ SUYIN_100042MR019S1532L

9/20 DC020709040

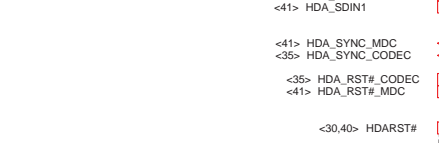
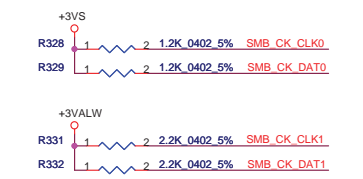
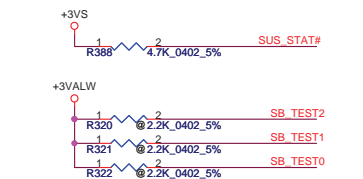
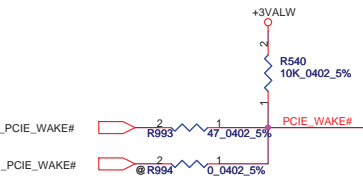
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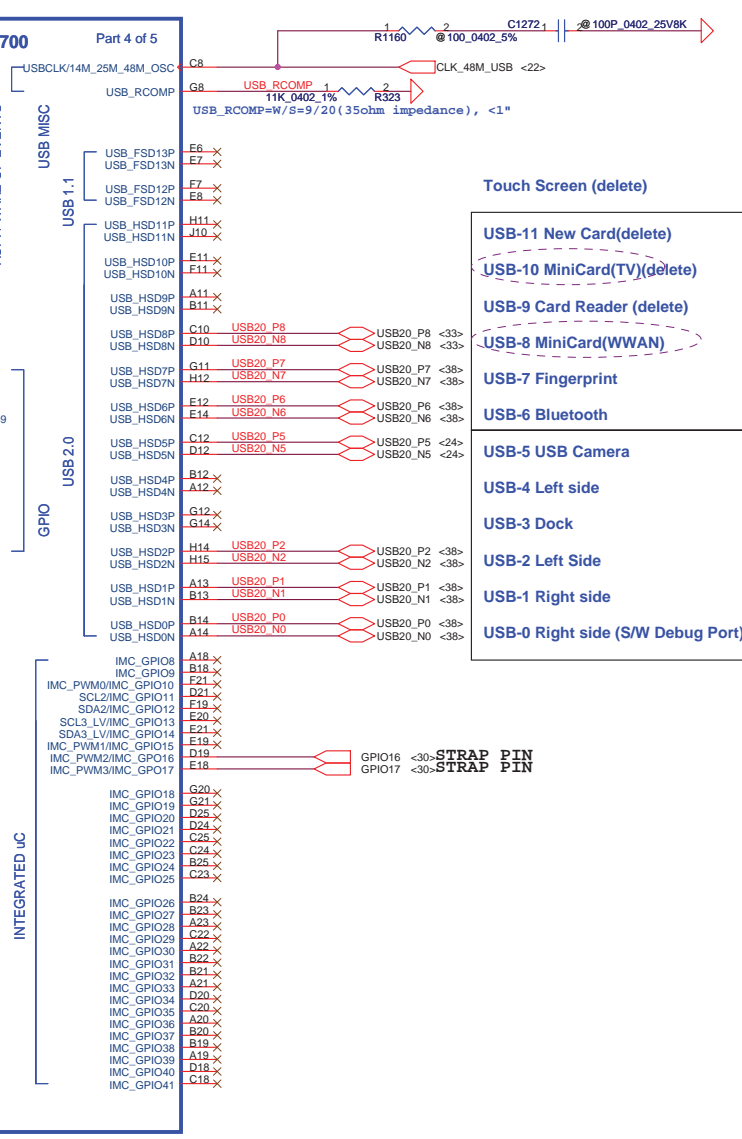
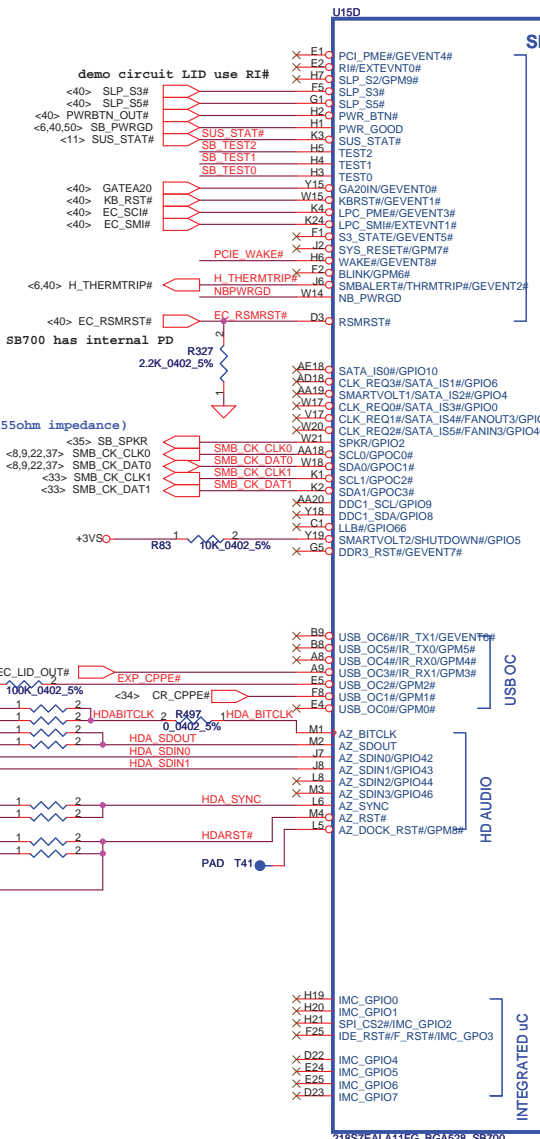
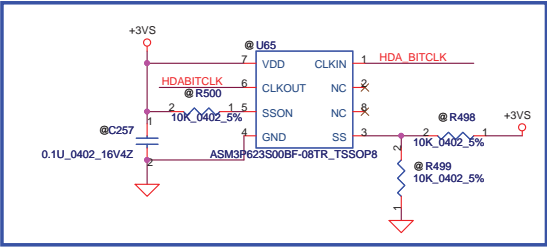
5/23 Update Y3 footprint

218S7EALA11FG_BGA528_SB700
 SA00001S510(A11) S IC 218S7EALA11FG SB700 BGA 528P SB 0FH
 SA00001S560(A12) S IC 218S7EALA12FG SB700 BGA 528P SB 0FH

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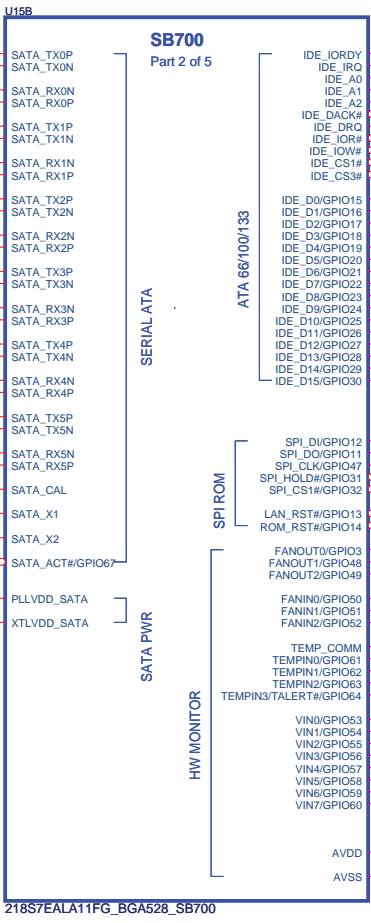
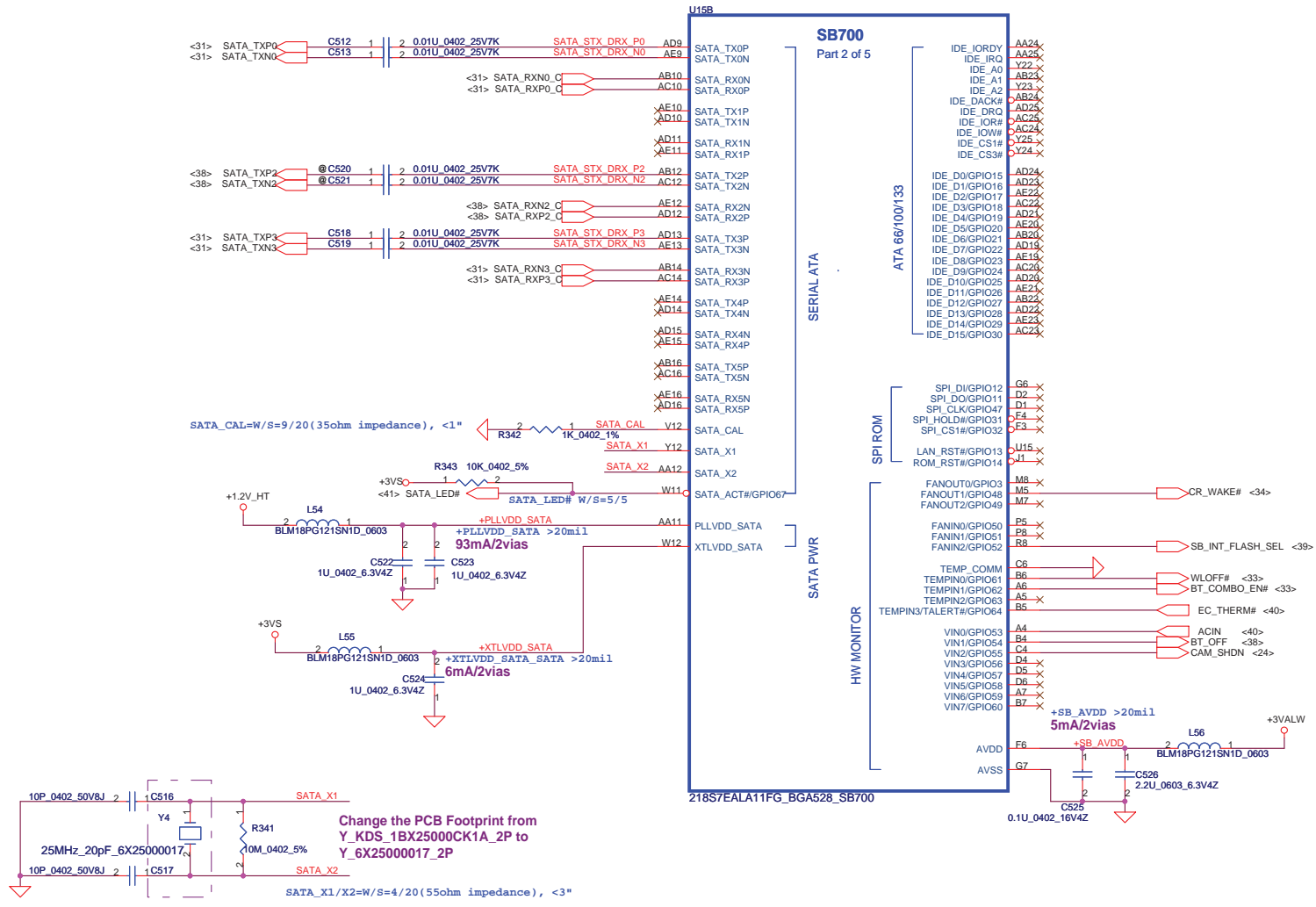


For EMI request.



- Touch Screen (delete)
- USB-11 New Card(delete)
- USB-10 MiniCard(TV)(delete)
- USB-9 Card Reader (delete)
- USB-8 MiniCard(WWAN)
- USB-7 Fingerprint
- USB-6 Bluetooth
- USB-5 USB Camera
- USB-4 Left side
- USB-3 Dock
- USB-2 Left Side
- USB-1 Right side
- USB-0 Right side (S/W Debug Port)

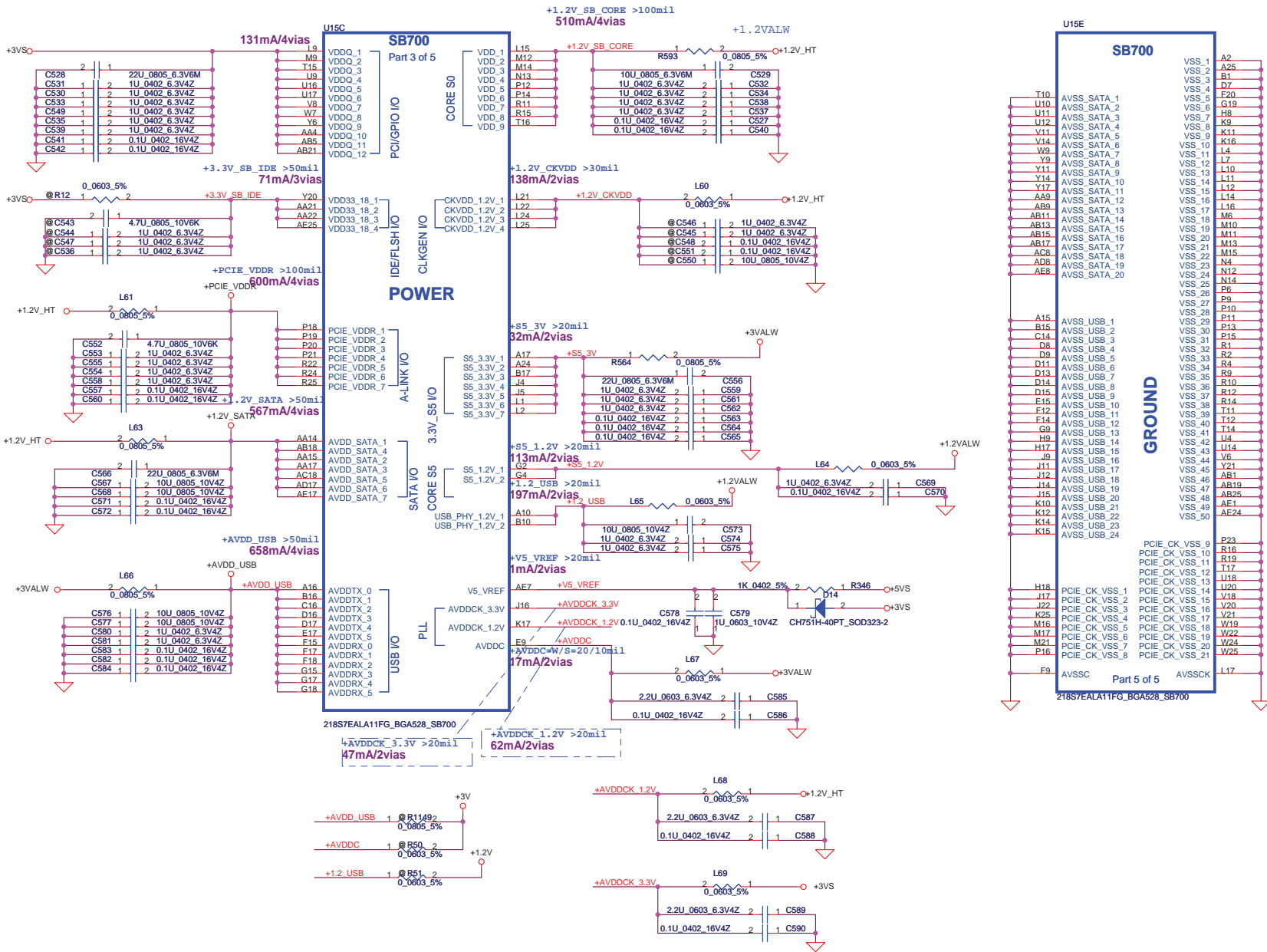
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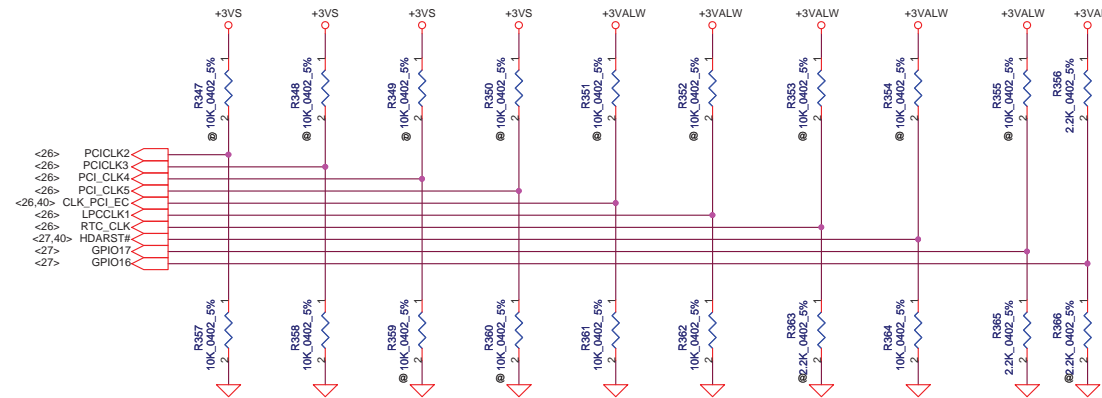
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

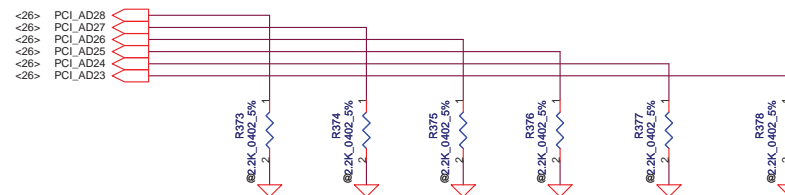
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



DEBUG STRAPS

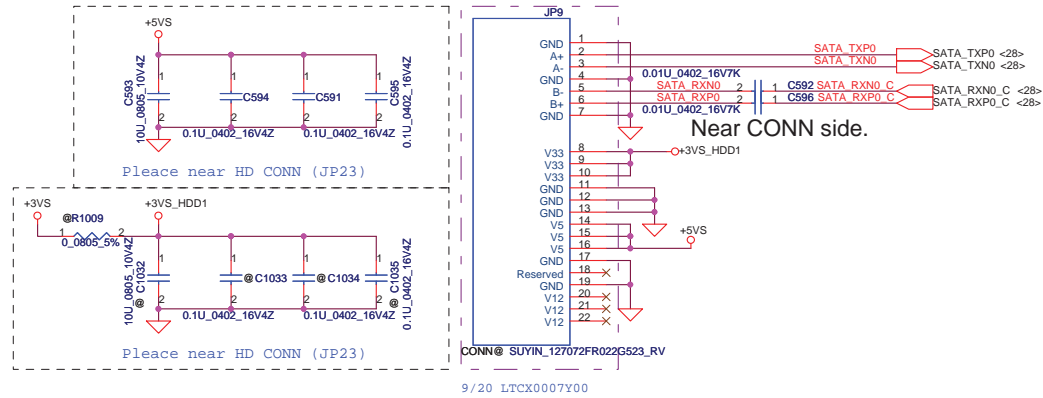
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



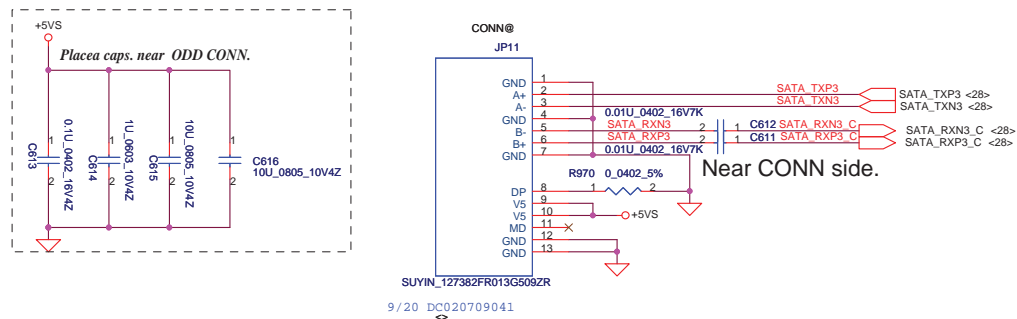
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HDD Connector

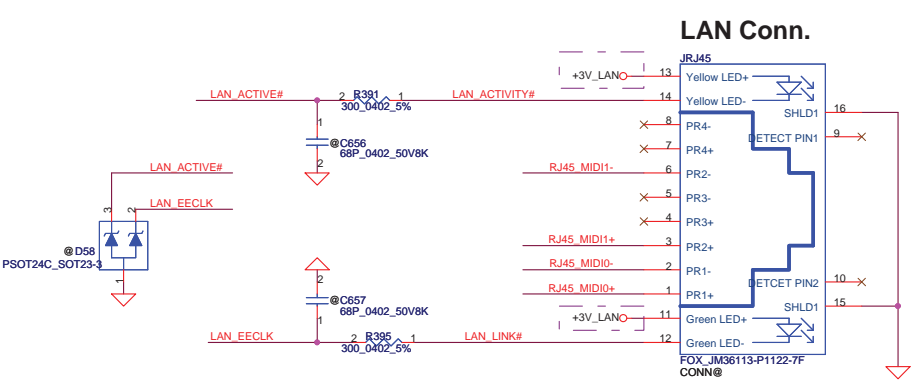
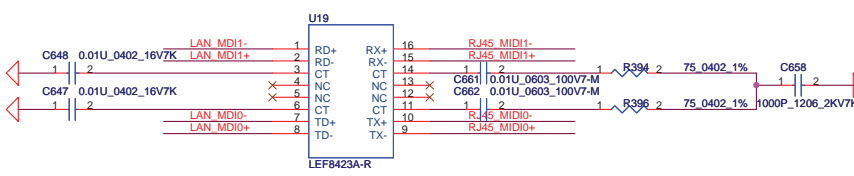
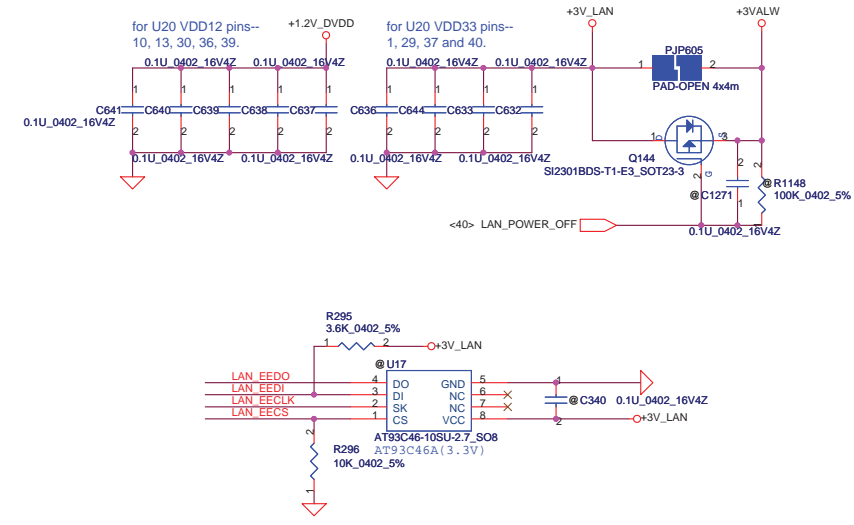
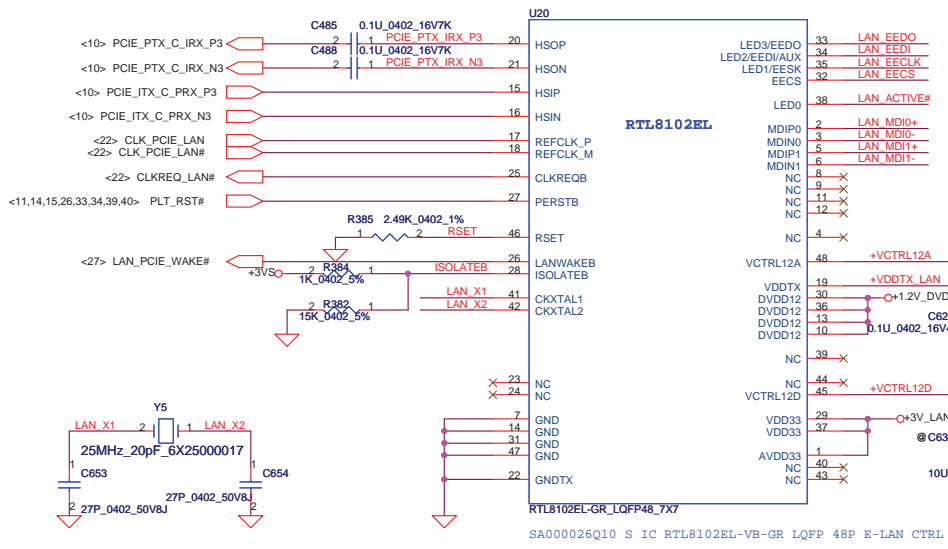


Multi-Bay Connector-option(deltet)

CD-ROM Connector



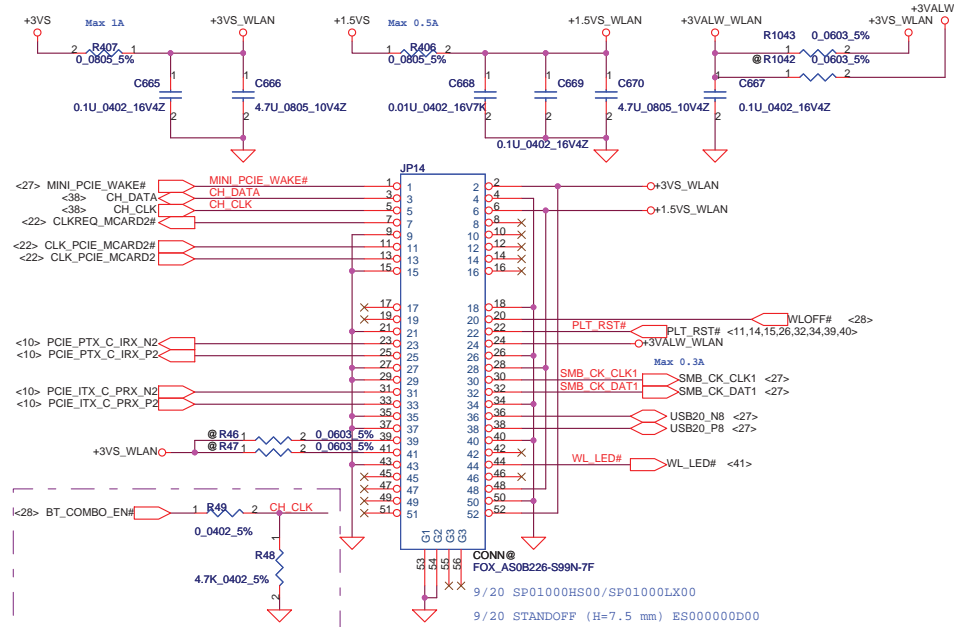
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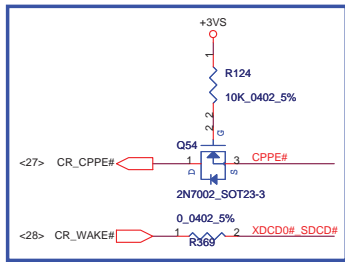
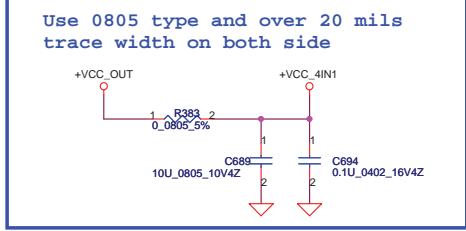
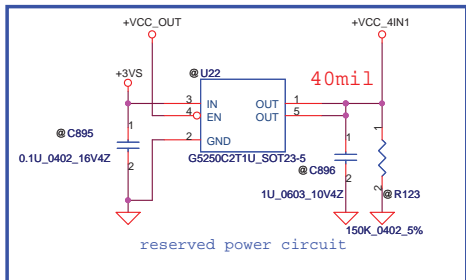
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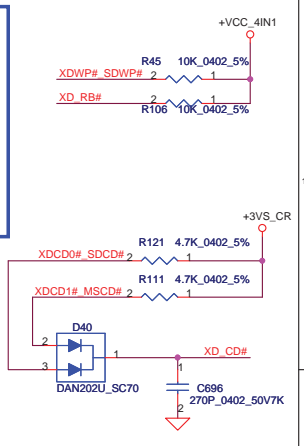
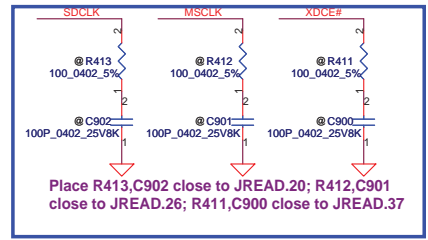
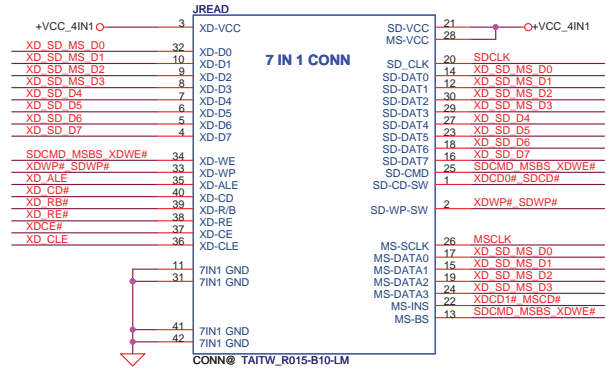
Mini Card Slot 1---WLAN



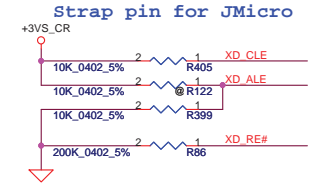
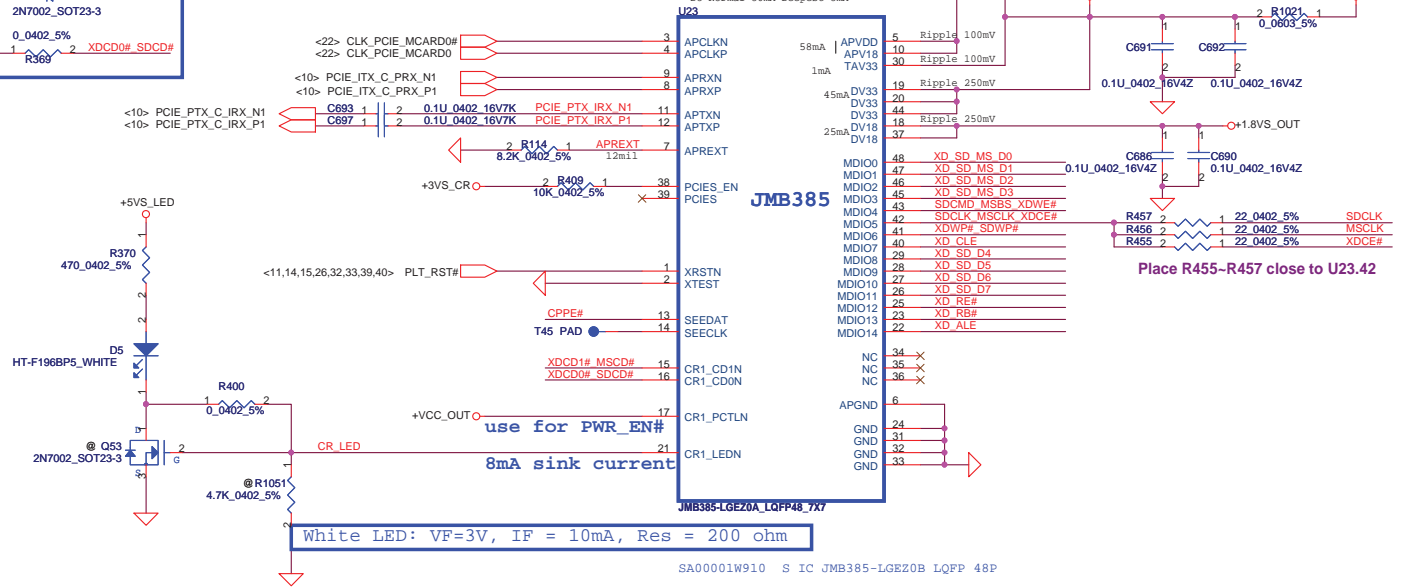
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Card Reader Connector



Power Circuit

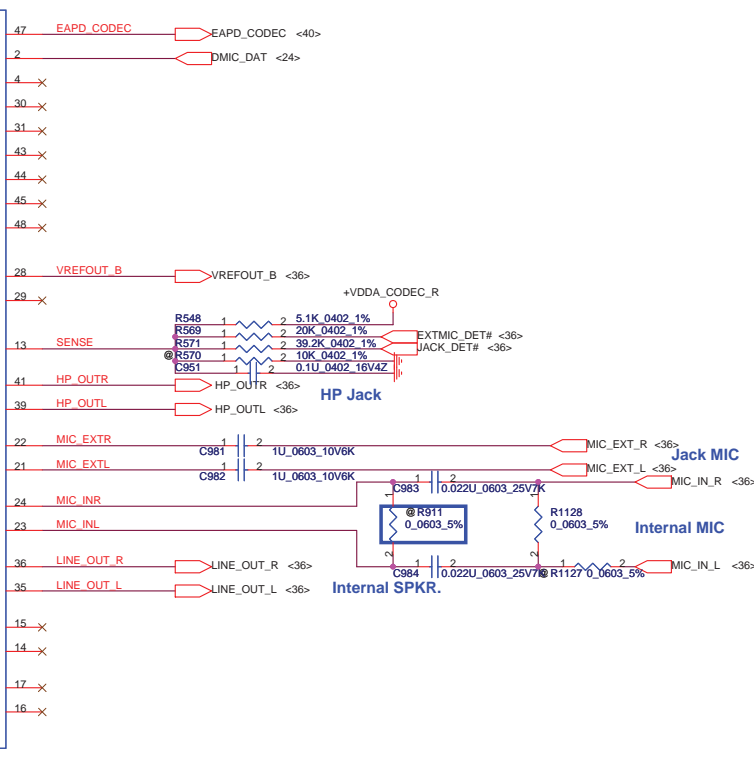
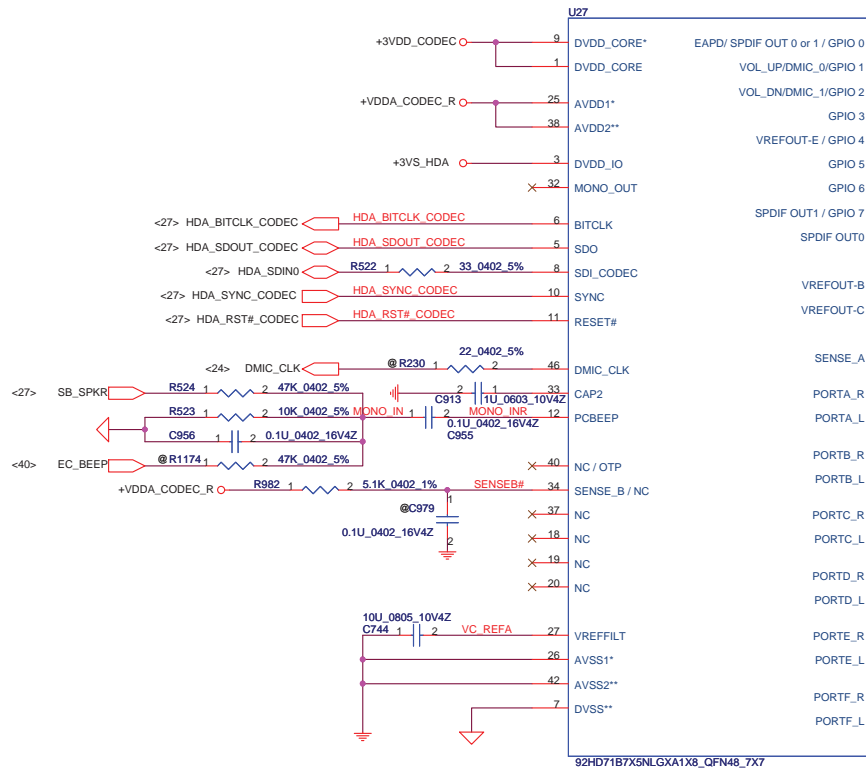
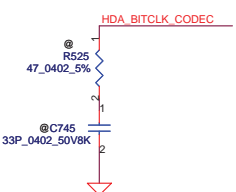
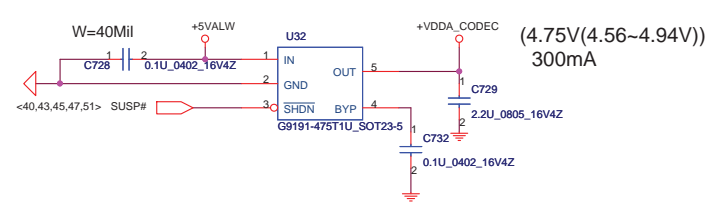
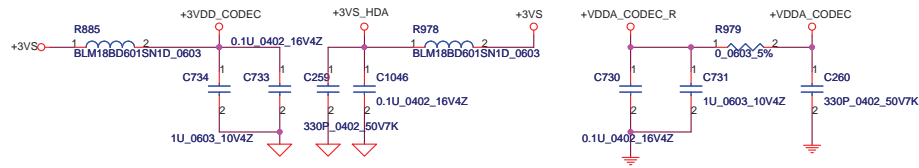


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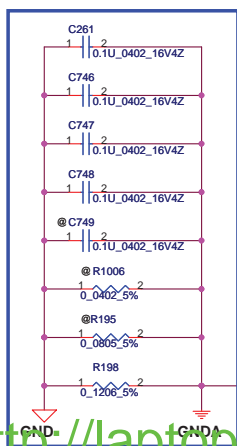
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CODEC POWER

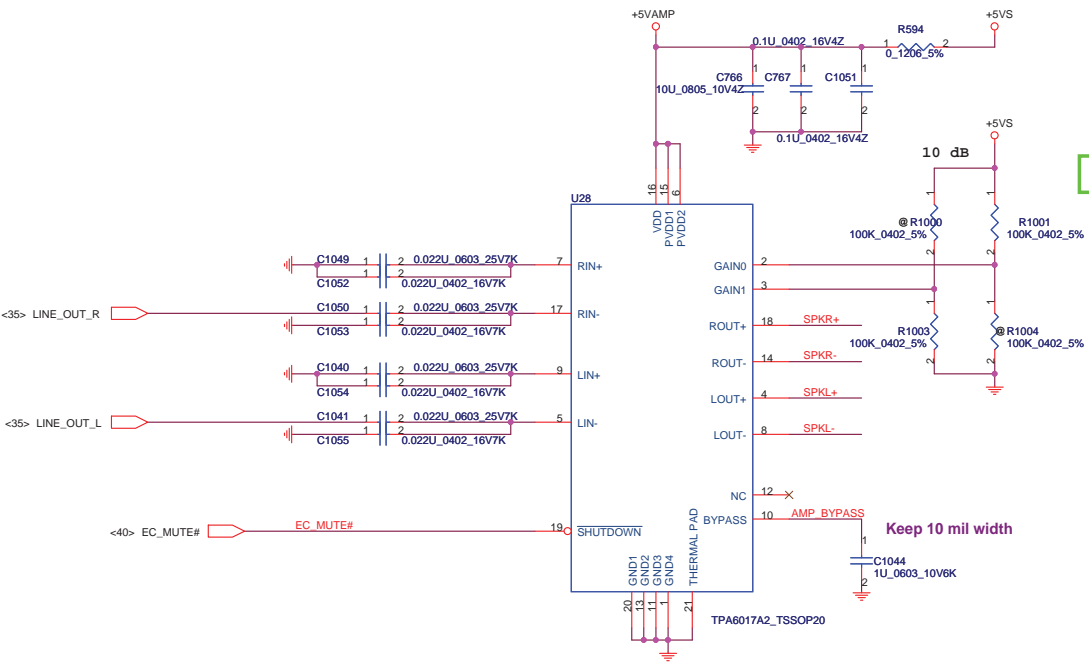


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

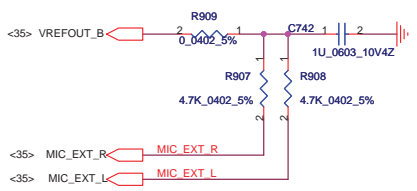
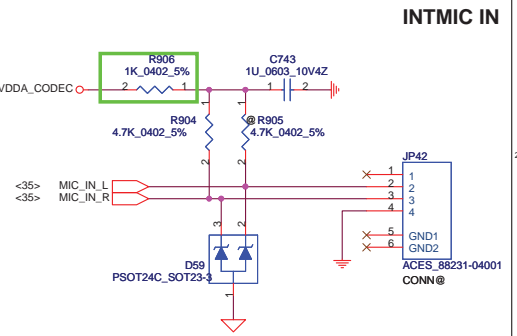
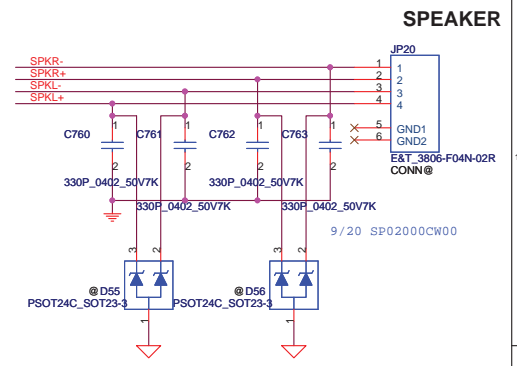


Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

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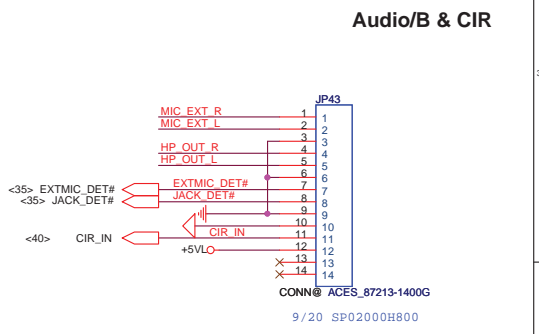
GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



EXTMIC IN



HP OUT For M/B

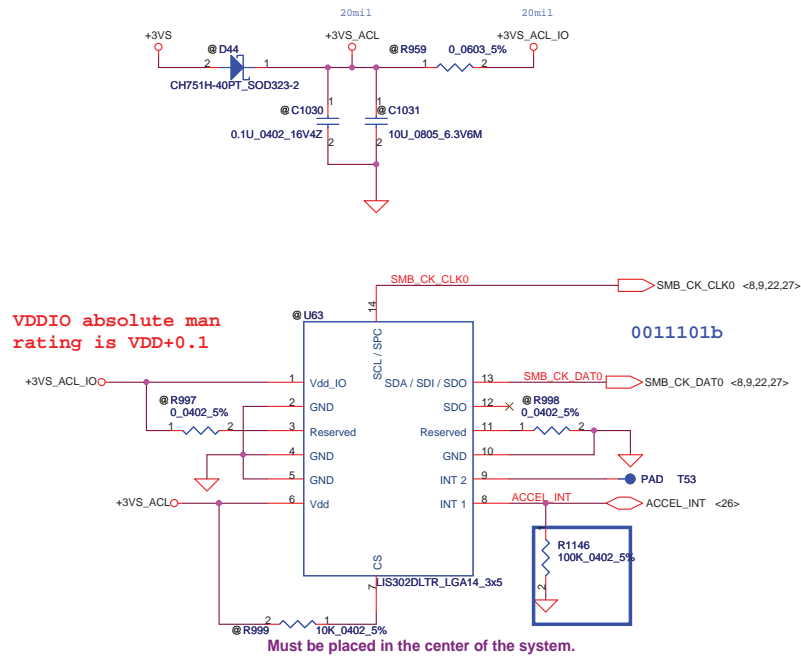


Audio/B & CIR

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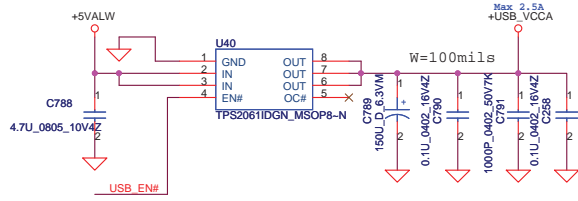
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ACCELEROMETER

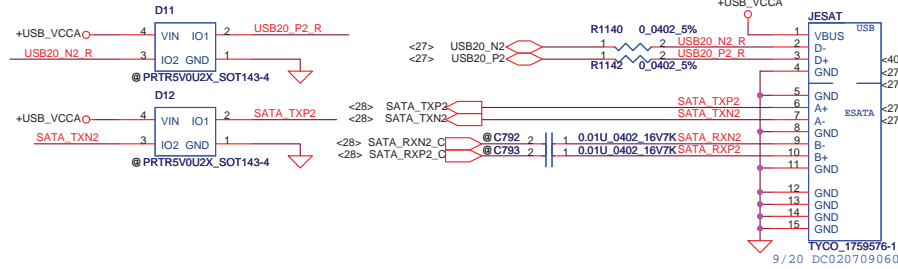


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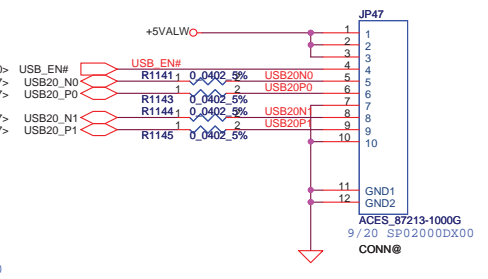
Left side USB CONNECTOR



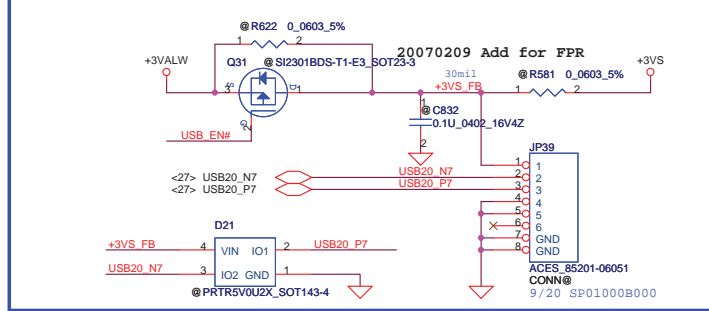
Left side ESATA5/USB2 combination Connector



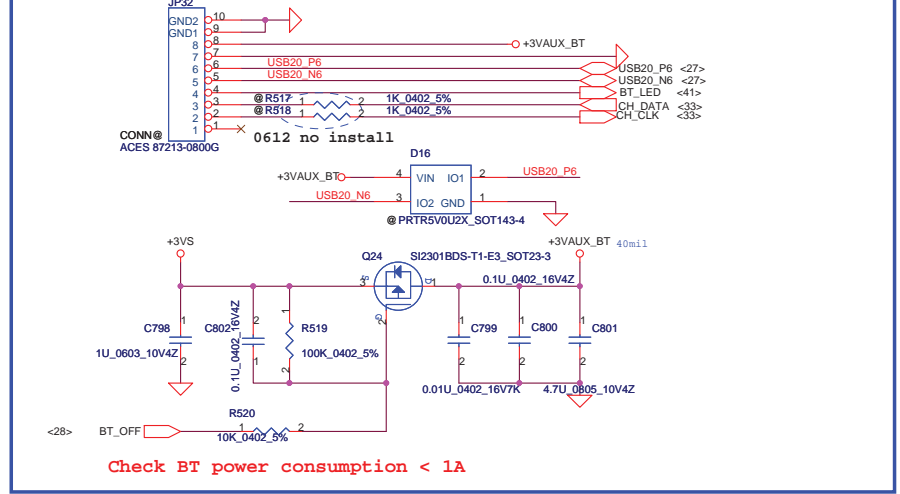
Right side USB 0&1 Board Conn



Finger printer

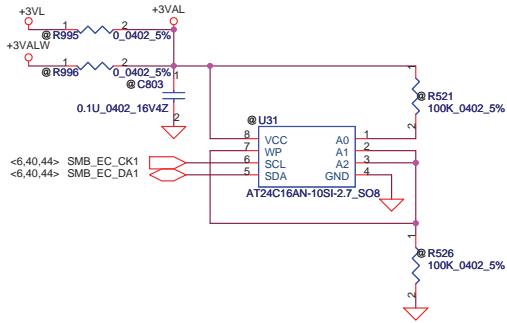


BT Connector

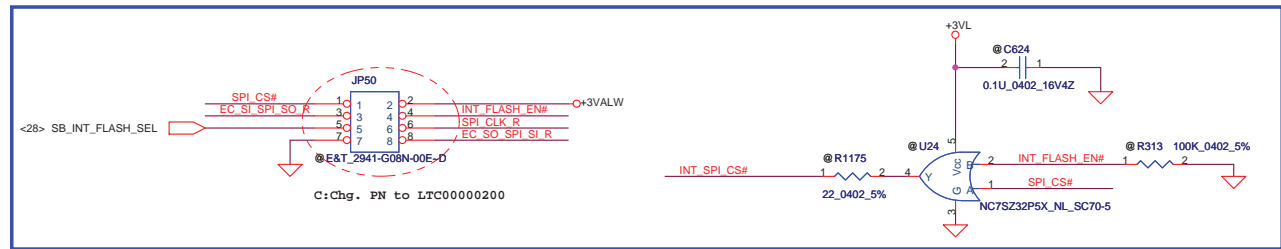
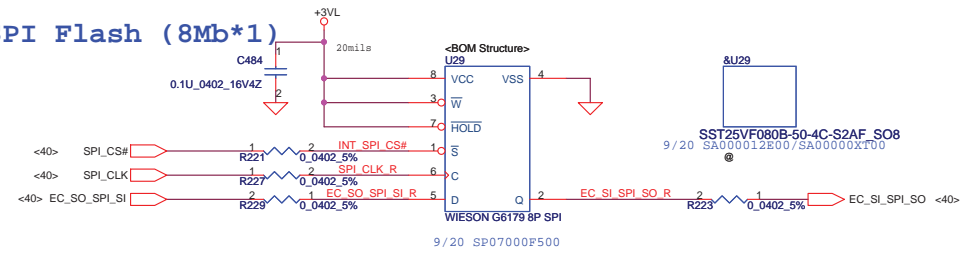


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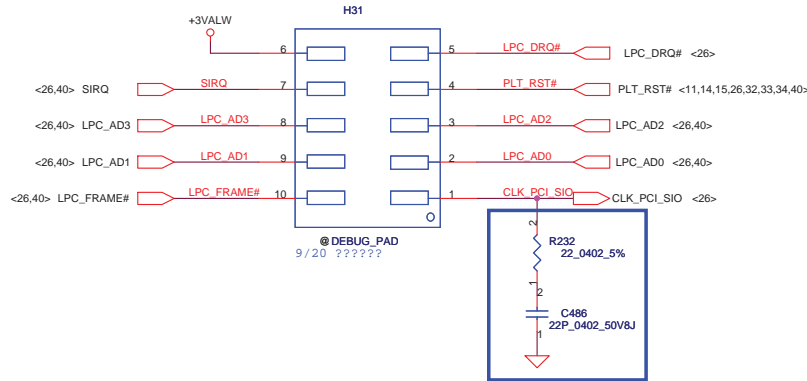
<http://laptop-motherboard-schematic.blogspot.com/>



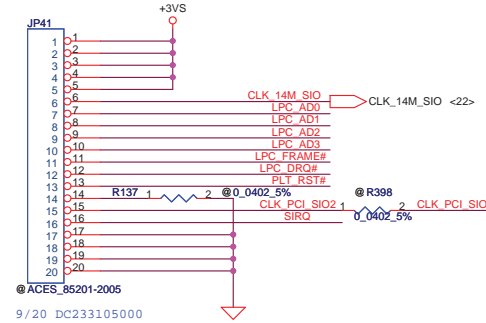
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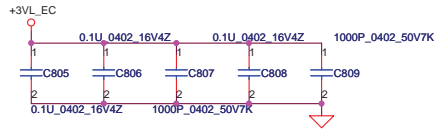
LPC Debug Port



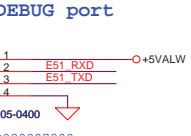
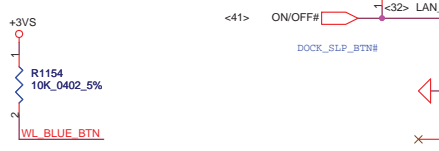
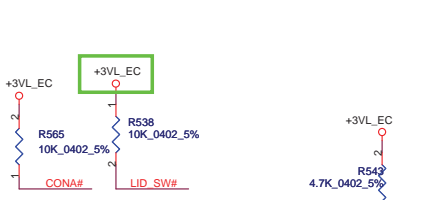
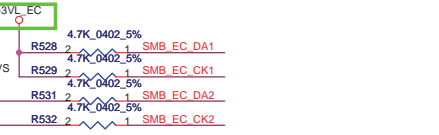
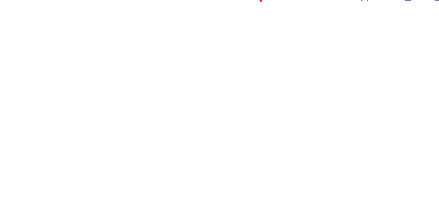
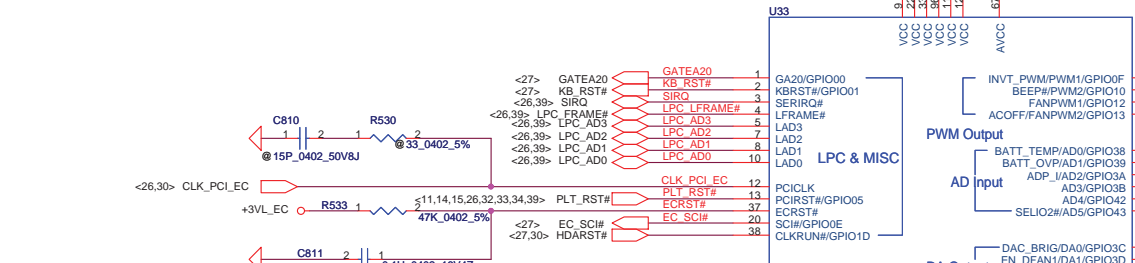
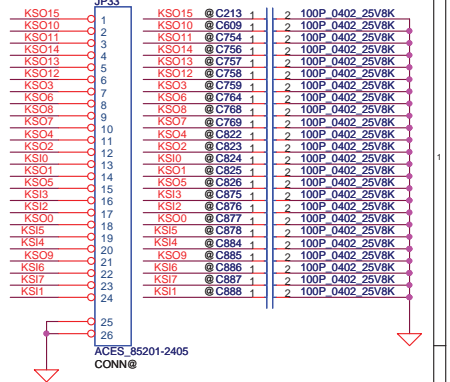
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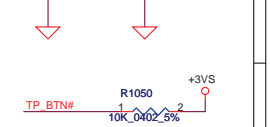
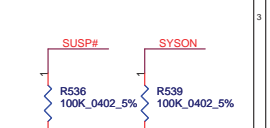
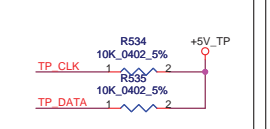
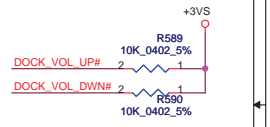
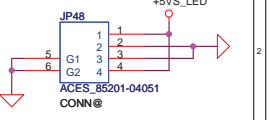
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Keyboard Connector For EMI



KB Back Light Conn



select SPI ROM or LPC ROM

DOCK VOL UP#

DOCK VOL DWN#

TP_CLK

TP_DATA

SUSP#

SYSON

TP_BTN#

VR_ON

AC_IN

VR_ON

AC_IN

TP_LED#

TP_LED#

VR_ON

AC_IN

TP_LED#

TP_LED#

Need luf for 926 C version

KB926FC0_LQFP128_14X14
SA00001J540(CO) S IC KB926FC0 LQFP 128P

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Issued Date	2007/10/11
Deciphered Date	2008/10/11

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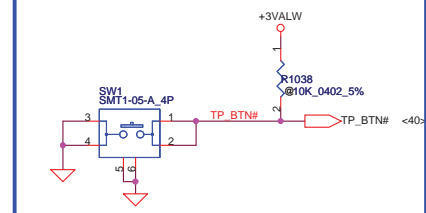
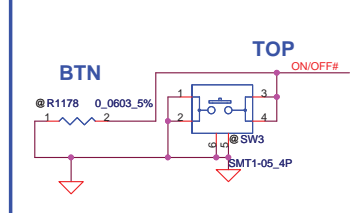
Schematic MB A4112

Size: 401568, Document Number: 401568, Date: Friday, February 13, 2009, Sheet: 40 of 54

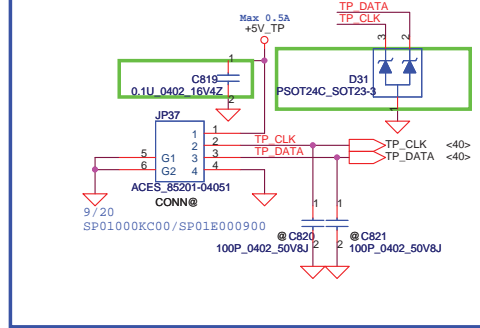
for debug only

ON/OFF Button Connector(delete)

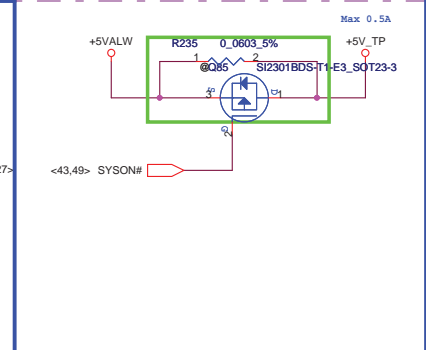
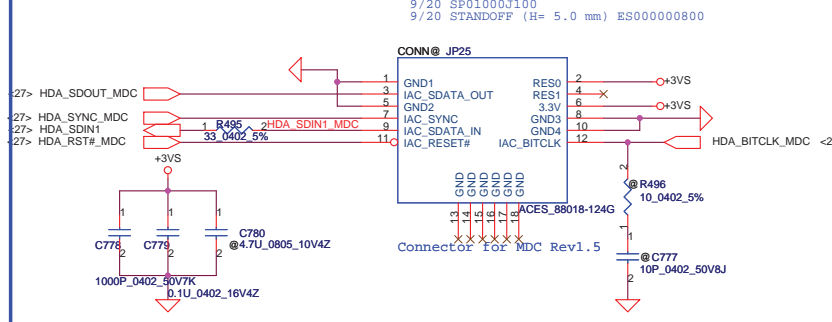
TP ON/OFF



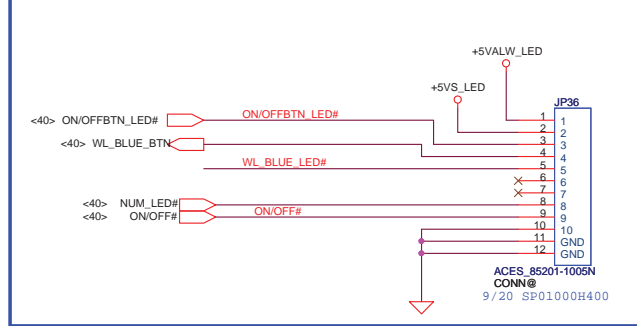
M/B TO TP/B



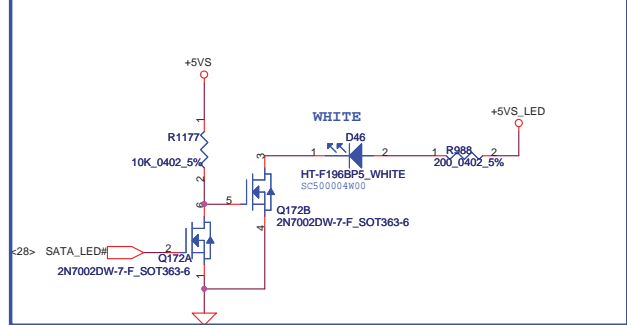
MDC 1.5 Conn.



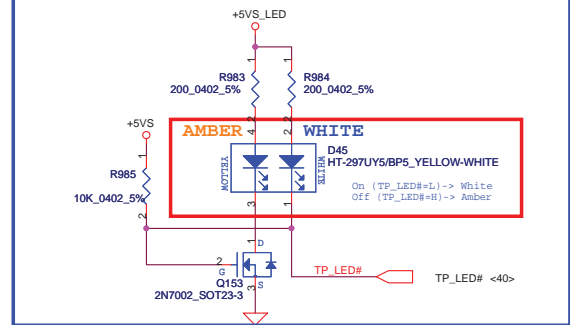
SWITCH BOARD.



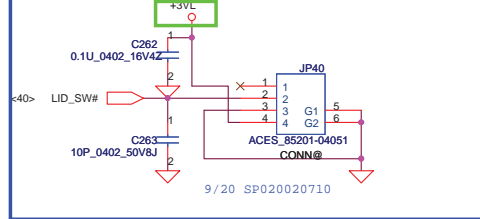
HDD LED



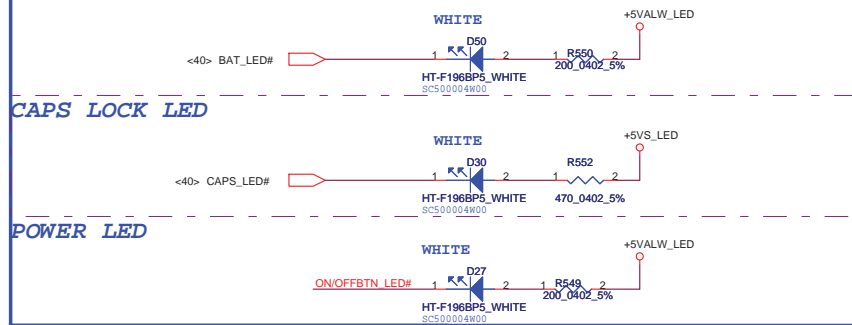
TouchPAD ON/OFF LED



Reed switch BOARD.



Battery Charge LED



White LED: VF=3V, IF = 10mA, Res = 200 ohm
Amber LED: VF=1.8V, IF = 8mA, Res = 390 ohm

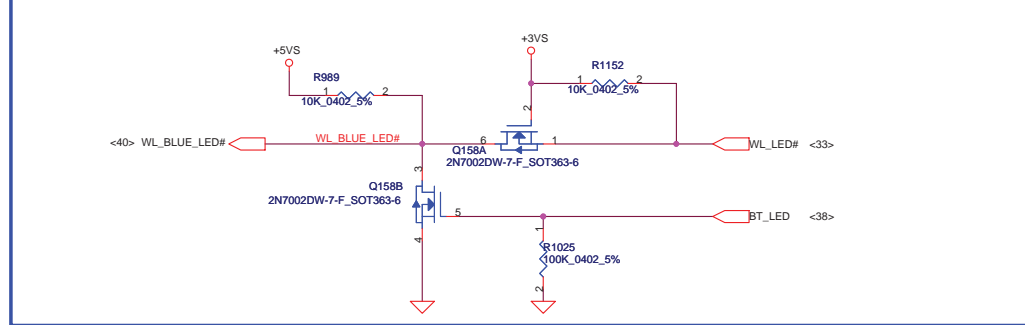
CAPS LOCK LED



POWER LED



WLAN and BT LED inform pin to KBC



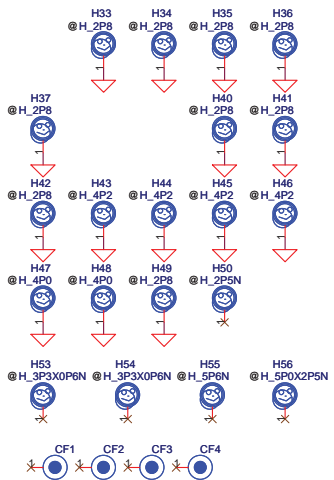
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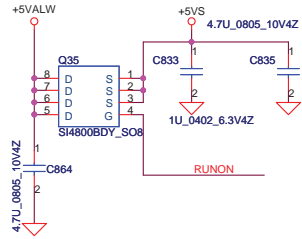
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H47, H48 -Stand off of MODEM on BOT Side

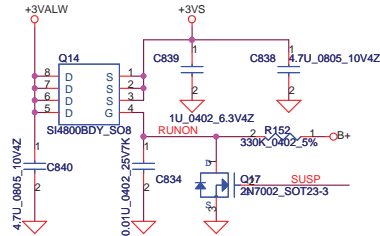


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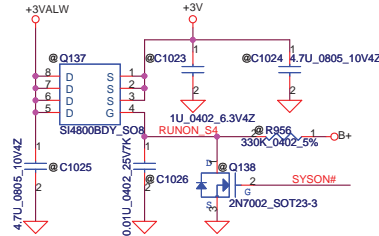
+5VALW TO +5VS



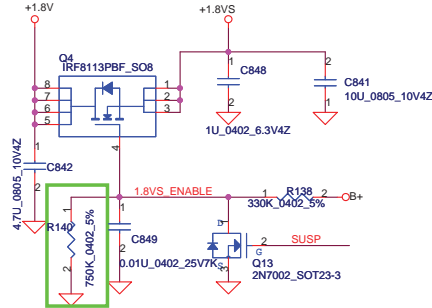
+3VALW TO +3VS



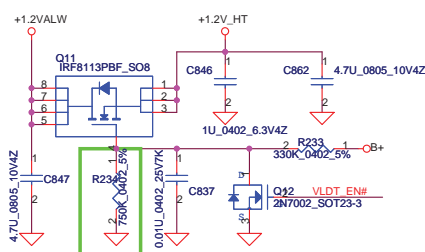
+3VALW TO +3V



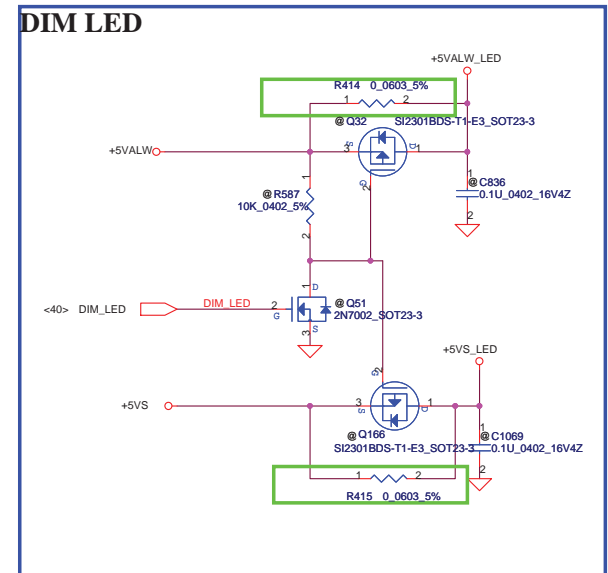
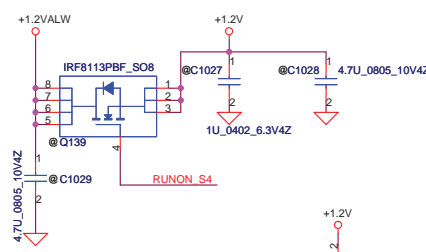
+1.8V TO +1.8VS



+1.2VALW TO +1.2V HT

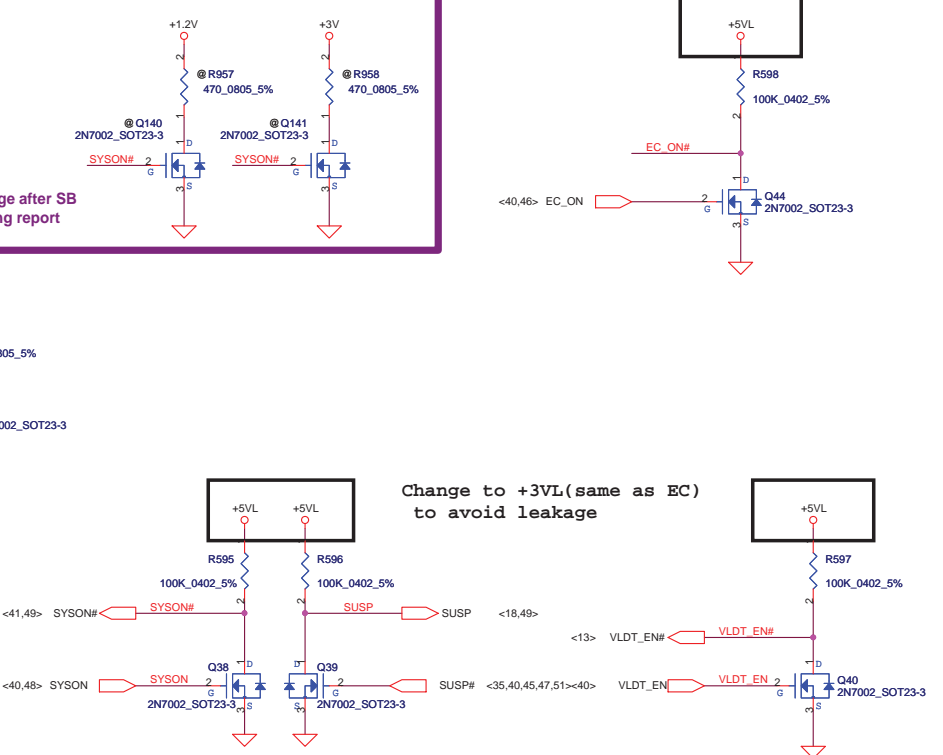
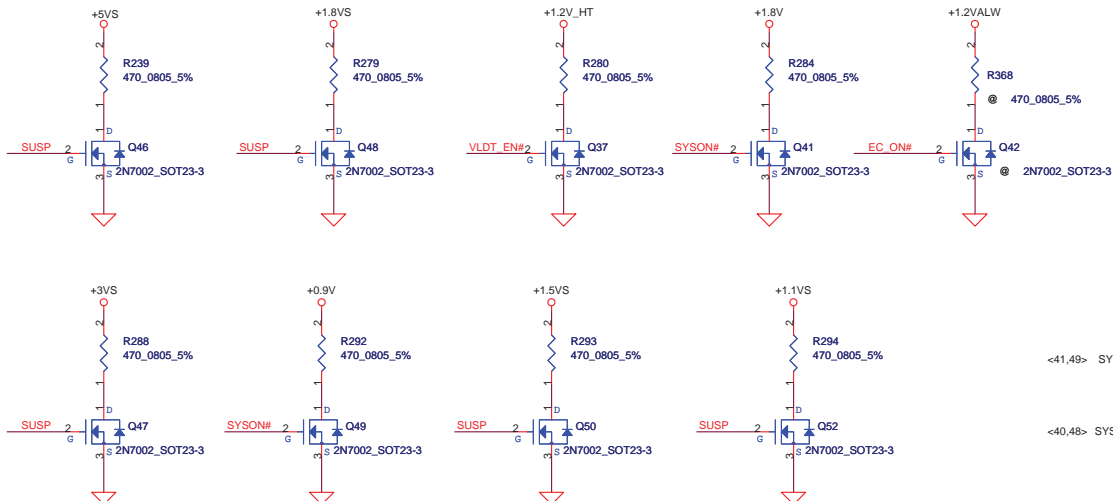


+1.2VALW TO +1.2V



Reserve until SI-1 stage after SB
USB PHY power saving report

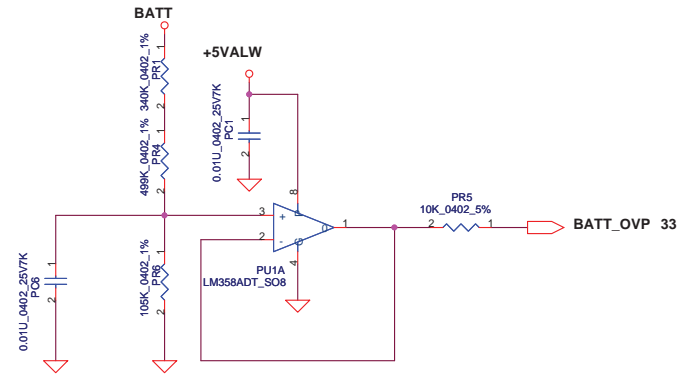
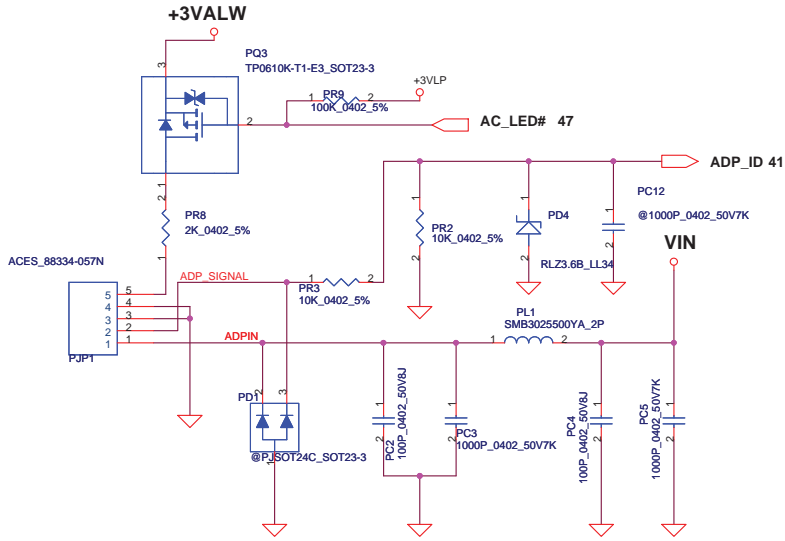
Discharge circuit



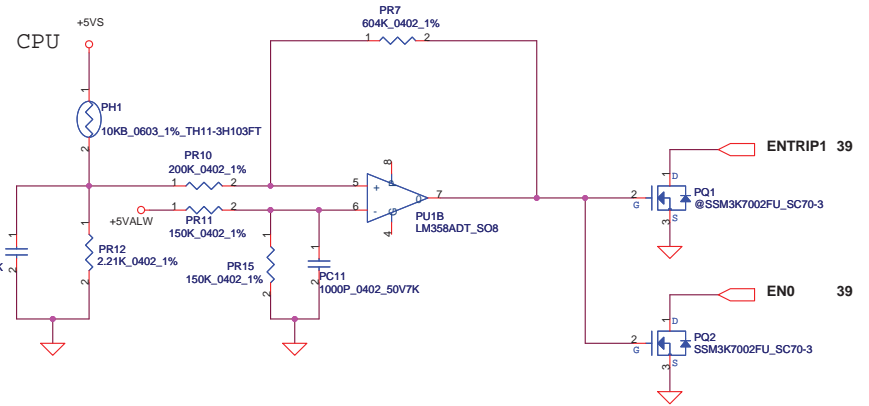
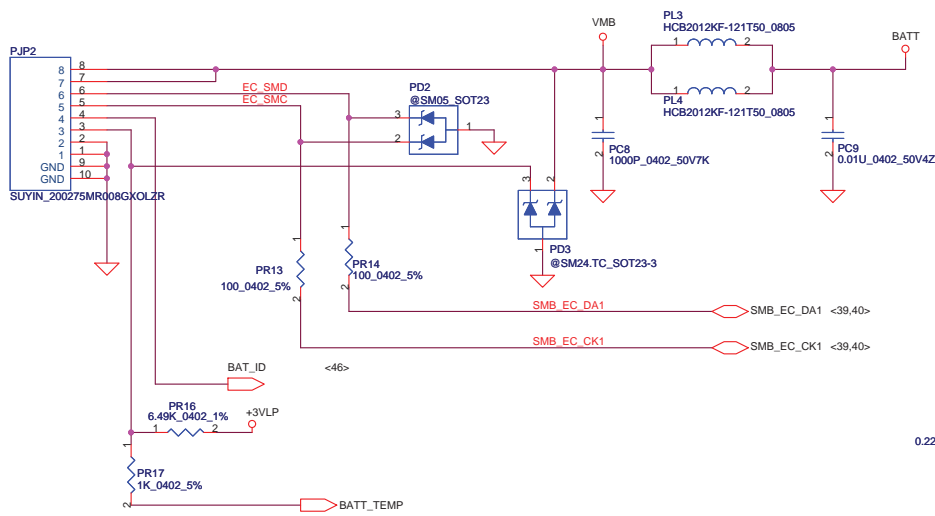
Change to +3VL (same as EC)
to avoid leakage

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BATT1
45@CR2032 RTC BATTERY

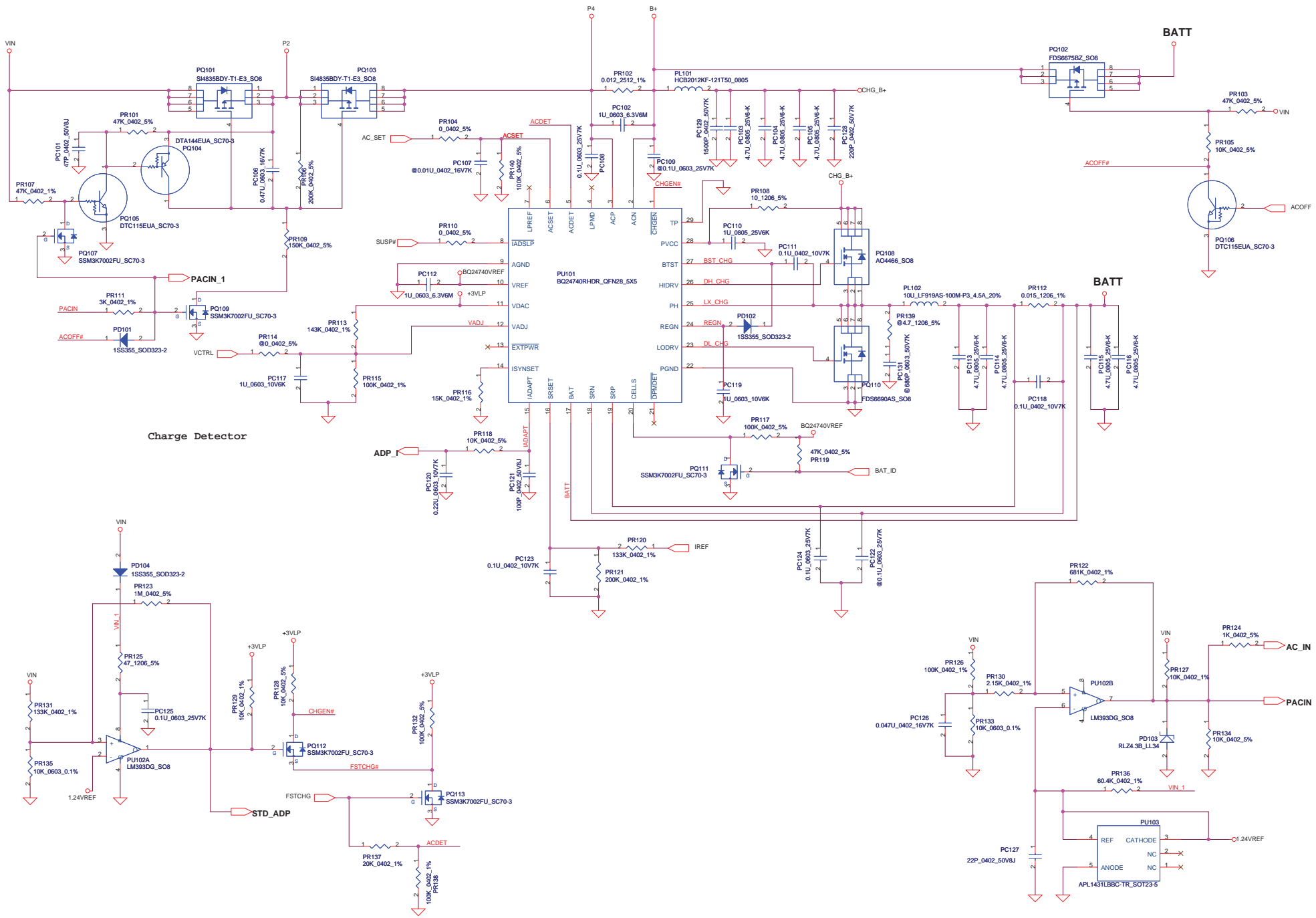


PH1 under CPU bottom side :
CPU thermal protection at 95 +-3 degree C



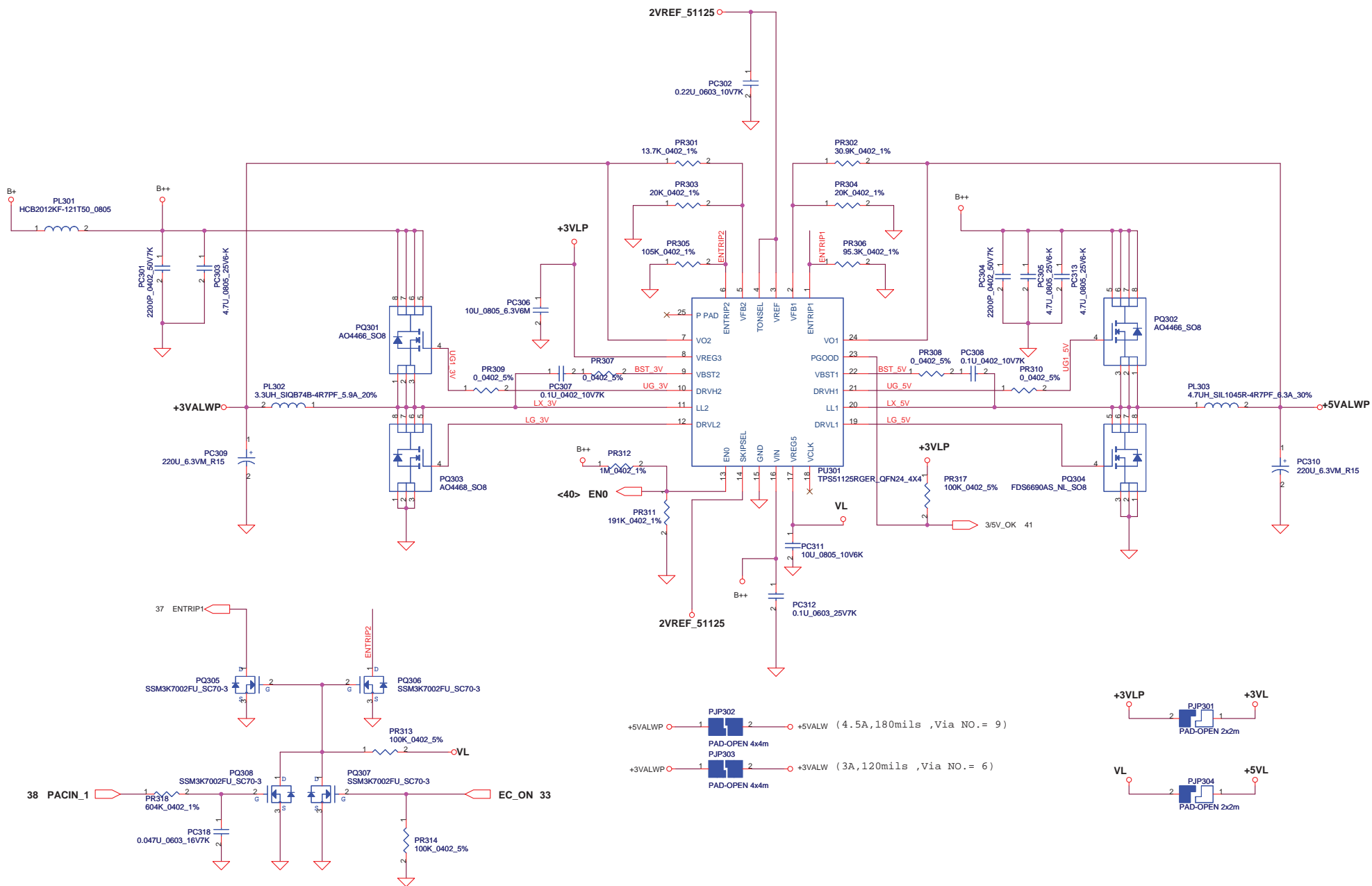
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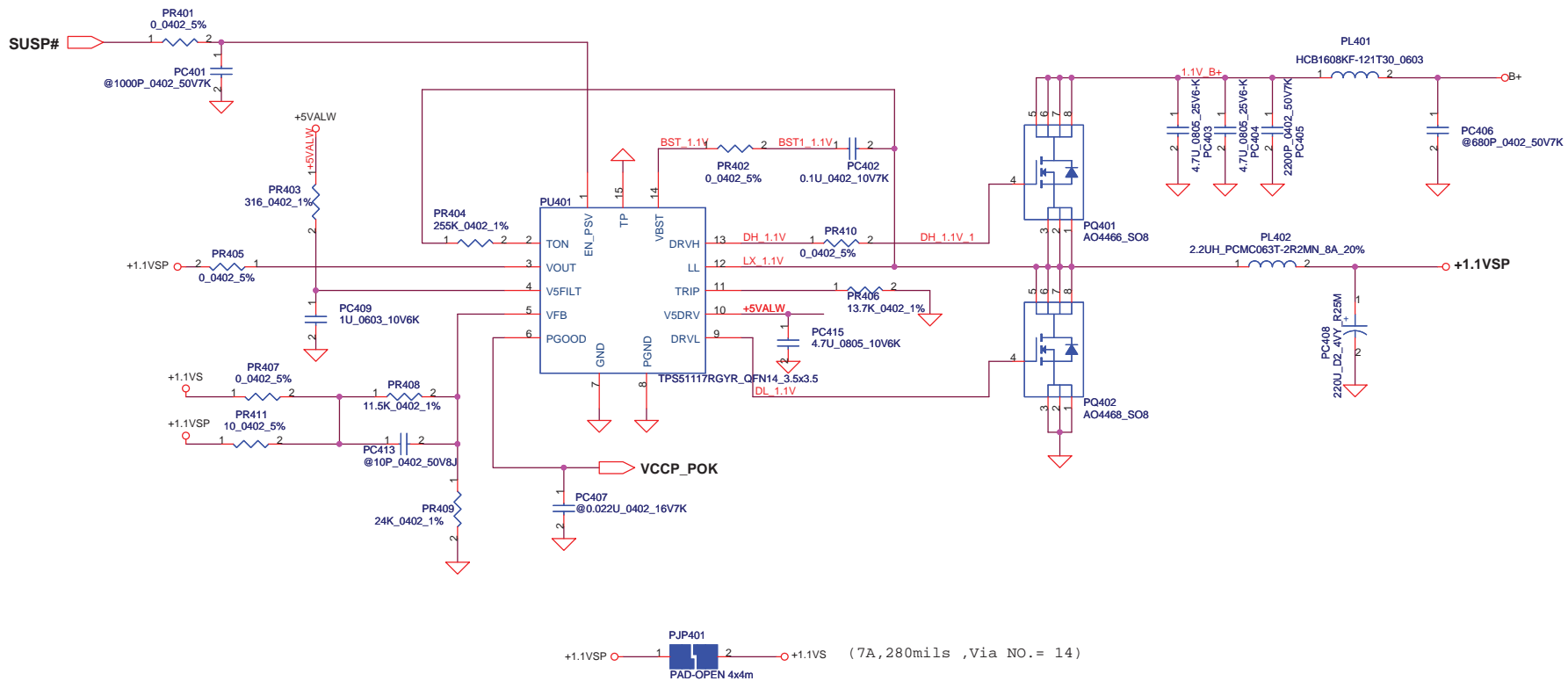
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http://laptop-motherboard.com



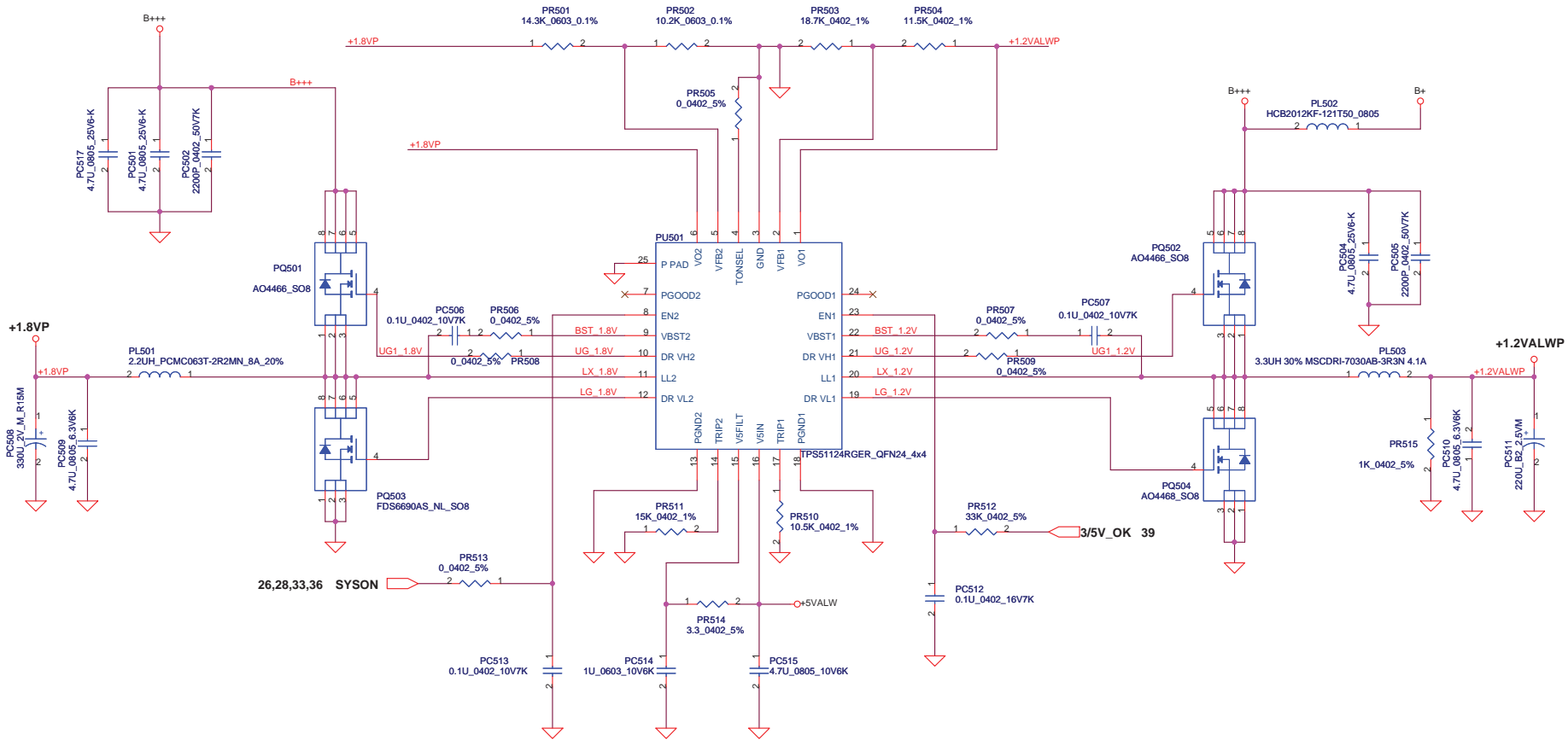
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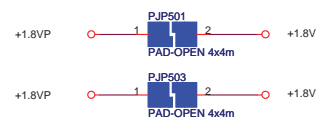


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(8A,320mils ,Via NO.=16)

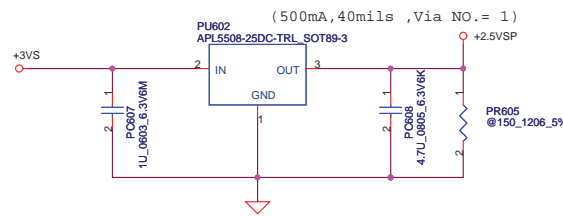
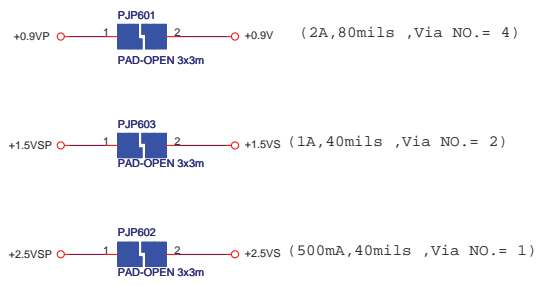
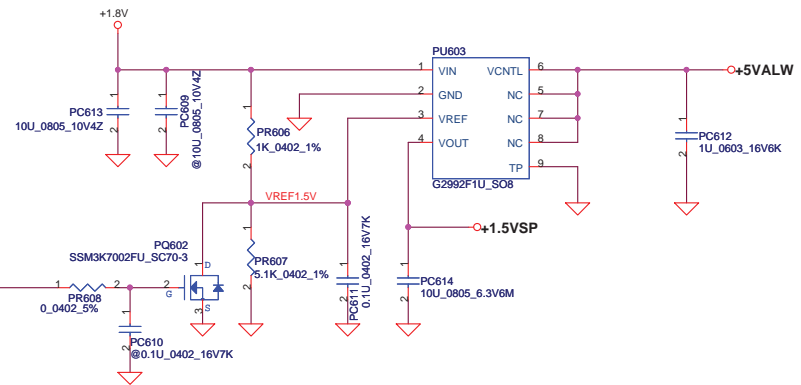
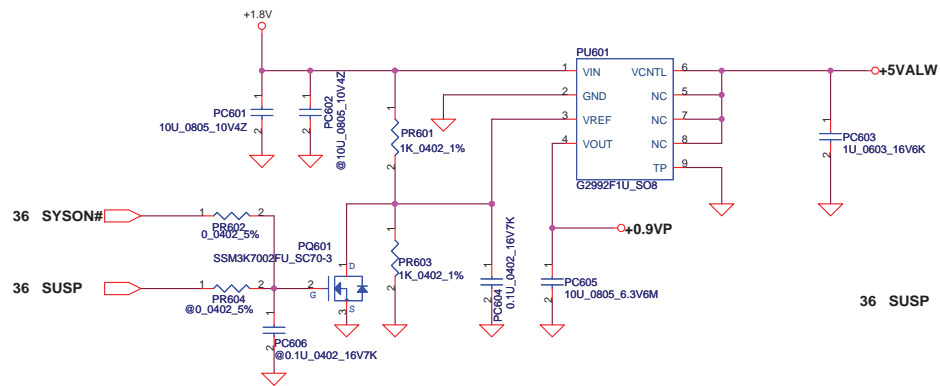


(4A,160mils ,Via NO.=8)



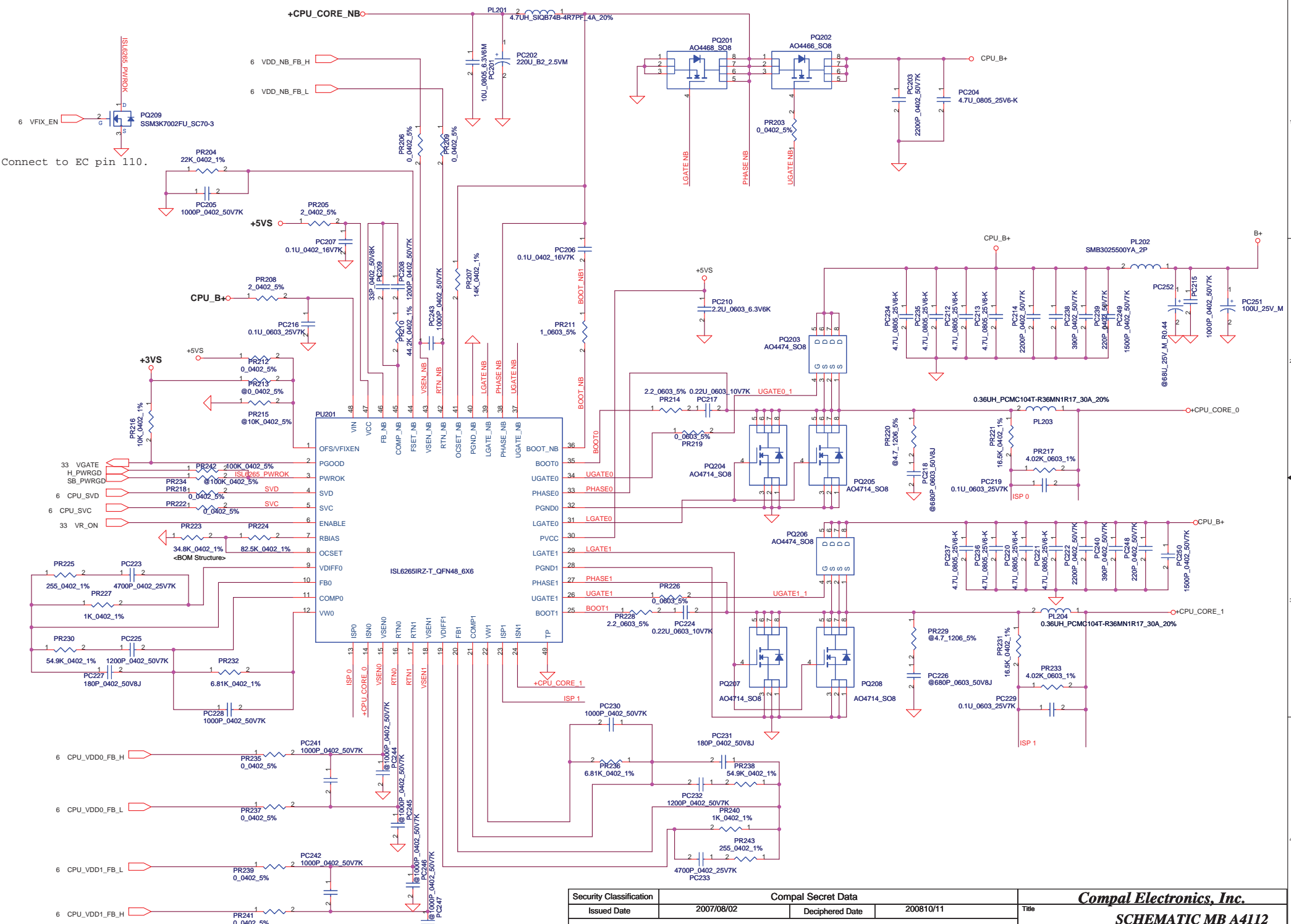
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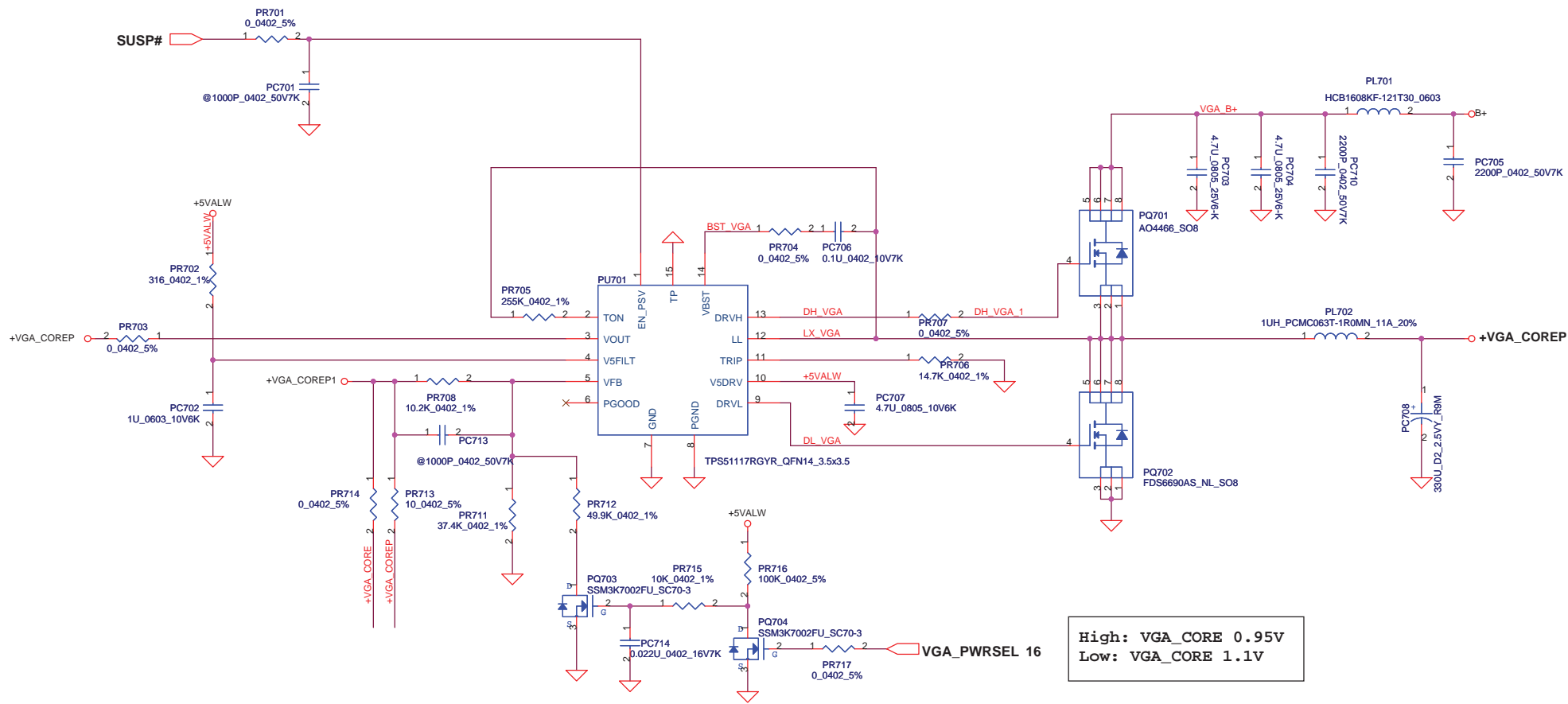
Connect to EC pin 110.

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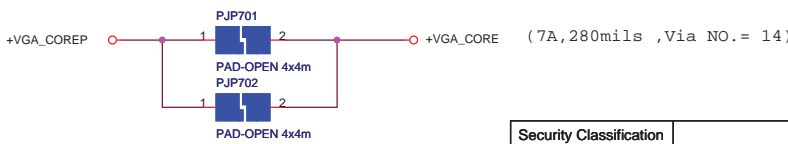
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High: VGA_CORE 0.95V
Low: VGA_CORE 1.1V



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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
2	51	VGA_COREP	12/31	Compal	PWR request	Connect the PR715 and PC714 to PQ703 pin1	
3	51	VGA_COREP	12/31	Compal	EMI request	Change PC705 to 2220pF	
4	50	CPU_CORE	12/31	Compal	EMI request	Add PC238, PC239, PC240, PC248	
5	50	CPU_CORE	12/31	Compal	Vendor request	Change PR221 and PR231 to 16.6K_ohm Change PR217 and PR233 to 4.02K_ohm Change PR223 to 17.8K_ohm Change PR224 to 100K_ohm	
6	45	Charger	12/31	Compal	EMI request	add PC128	
7	45	Charger	01/04	Compal	PWR request	Change PQ102 to FDS6675BZ	
8	50	CPU_CORE	01/04	Compal	PWR request	Change PQ204, PQ205, PQ207, PQ208 to FDS6676AS Add PQ209 and PQ234 to fix CPU core voltage.	
9	44	DC Connector /CPU_OTP	01/09	Compal	AC LED change to KBC control	AC_LED connect to KBC pin 97	
10	51	VGA_COREP	02/27	Compal	Change VGA low voltage to 0.95V	Change PR712 to 49.9K_ohm and PR711 to 37.4K_ohm	
11	46	3.3VALWP/5VALWP	02/27	Compal	Change OTC shun down pin.	Change OTC shun down pin to PU301 pin13.	
12	50	CPU_CORE	03/03	Compal	EMI request	Add PC249, PC250	
13	45	Charger	03/03	Compal	EMI request	Add PC129	
14	50	CPU_CORE	03/03	Compal	HW request	Add H_PWRGD	
15	44	DC Connector /CPU_OTP	04/02	Compal	AC LED issue	Change AC_LED# pull high to +3VLP	
16	50	CPU_CORE	04/24	Compal	acoustic noise	Add PC251	
17	44	DC Connector /CPU_OTP	04/24	Compal	HW CPU thermal protection change to 95 +-3 degree C	Change PR12 to 2.21K_ohm	

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LA-4112P Rev0.2 -> 0.3 Product Improvement Record (P.I.R.)

Circuit change list:

1. Un-Stuff C18, Q127, Q129, R175, R814, C939 and change SMBus 2 -> SMBus 1. (Page 6)-* Follow 17" AMD circuit change.
2. Add signal H_PWRGD_CPU to option CPU core chip`s PWR OK. (Page 6)-* Follow AMD recommand power up sequence change.
3. Change signal name ENTRIP2 to EN0. (Page 6)-* For power team chagne request.
4. Un-Stuff C54. (Page 7)-* Follow 17" AMD circuit change.
5. AVDD1, AVDD2, AVDDI, AVDDQ, .PLVDD, PLVDD18, VDDLTP18, VDDLTP18_1, VDDLTP18_2 directly conecct to GND. (Page11)-* For RX781 change recommand.
6. VDD18_MEM1, VDD18_MEM_2 directly conecct to GND. (Page 13)-* For RX781 change recommand.
7. Change Bead L16, L22 to 0 ohm and Delete L20, L21 than use jumper to link the power. (Page 13)-* Follow 17" AMD circuit change.
8. Change R101, R102 3K -> 1K ohm. (Page 14)-* ATI recommand.
9. Add VGA_PWN to Panel. (Page 16/24)-* For panel power saving request.
10. Un-stuff R1101. (Page 21)-* For PCI-E EA request.
11. Add signal CLK_14M_SIO. (Page 22)-* For debug port request.
12. Stuff C447. (Page 23)-* EMI/ESD recommand.
13. Add +5VS power for webcam`s LDO power option. (Page 24)-* Follow 17" AMD circuit change.
14. Change C863 0.047U -> 1000p. (Page 24)-* Fix panel power down waveform bounce.
15. Change Bead L61, L61 to 0 ohm. (Page 29)-* Follow 17" AMD circuit change.
16. Un-stuff R1148, C1271. (Page 32)-* Follow 17" AMD circuit change.
17. Modify JRJ45 layout footprint. (Page 32)-* For DFX request.
18. Add D58 ESD diode. (Page 32)-* EMI/ESD recommand.
19. Stuff R1043, Un-stuff R1042 (Page 33)-* Follow 17" AMD circuit change.
20. Add R399, R400 and un-stuff R122, R1051, Q53. (Page 34)-* Follow project common design.
21. Add C259, C260, C261 and stuff C746, C747, C748 and change C760, C761, C762, C763 100p -> 330p. (Page 35/36)-* EMI/ESD recommand.
22. Signal INTMIC_DET directly connect to AGND and Delete Q160, Q151, R951. (Page 35/36)-* OPP dont need the detect circuit.
23. Add C258. (Page 38)-* EMI/ESD recommand.
24. ME change JP32 and change Q24`s power +3VALW -> +3VS. (Page 38)-* Follow 17" AMD circuit change.
25. Add LPC debug port. (Page 39)-* For debug request.
26. Add D57, R397. (Page 40)-* Fix AC-IN chip power rail different issue.
27. Delete Q34, R645. (Page 41)-* Follow 17" AMD circuit change.
28. Add C262, C263. (Page 41)-* For Small/B design change.
29. Chagne C1175 type B2 ->Y. (Page 18)-* For fixed ME issue.
30. Add C264. (Page 22)-* For IDT request.
31. Add L85, L86, L87, L88. (Page 22)-* For EMI/ESD recommand.

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LA-4112P Rev0.3 -> 1.0 Product Improvement Record (P.I.R.)

Circuit change list:

1. Reserve R59, R60, R61. (Page 6)-* AMD suggest to reserve the pull high/down resistor of these test pin.
2. Add C477 0.1UF. (Page 23)-* For EMI recommand.
3. Change R906 from 0 ohm to 1k ohm. (Page 36)-* For reduce MIC background noise issue.
4. Change SMB DA1/CK1 pull high power rail from +3VALW to +3VL. (Page 40)-* EC recommand & follow Riply change list.
5. Add C819 0.1UF & D31 ESD diode. (Page 41)-* For EMI recommand.
6. Add R414 & R415 0 ohm. (Page 43)-* no support DIM function.
8. Add R140 & R234 750k ohm. (Page 43)-* Solve Rds on issue.

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