

# Compal confidential

## Schematics Document

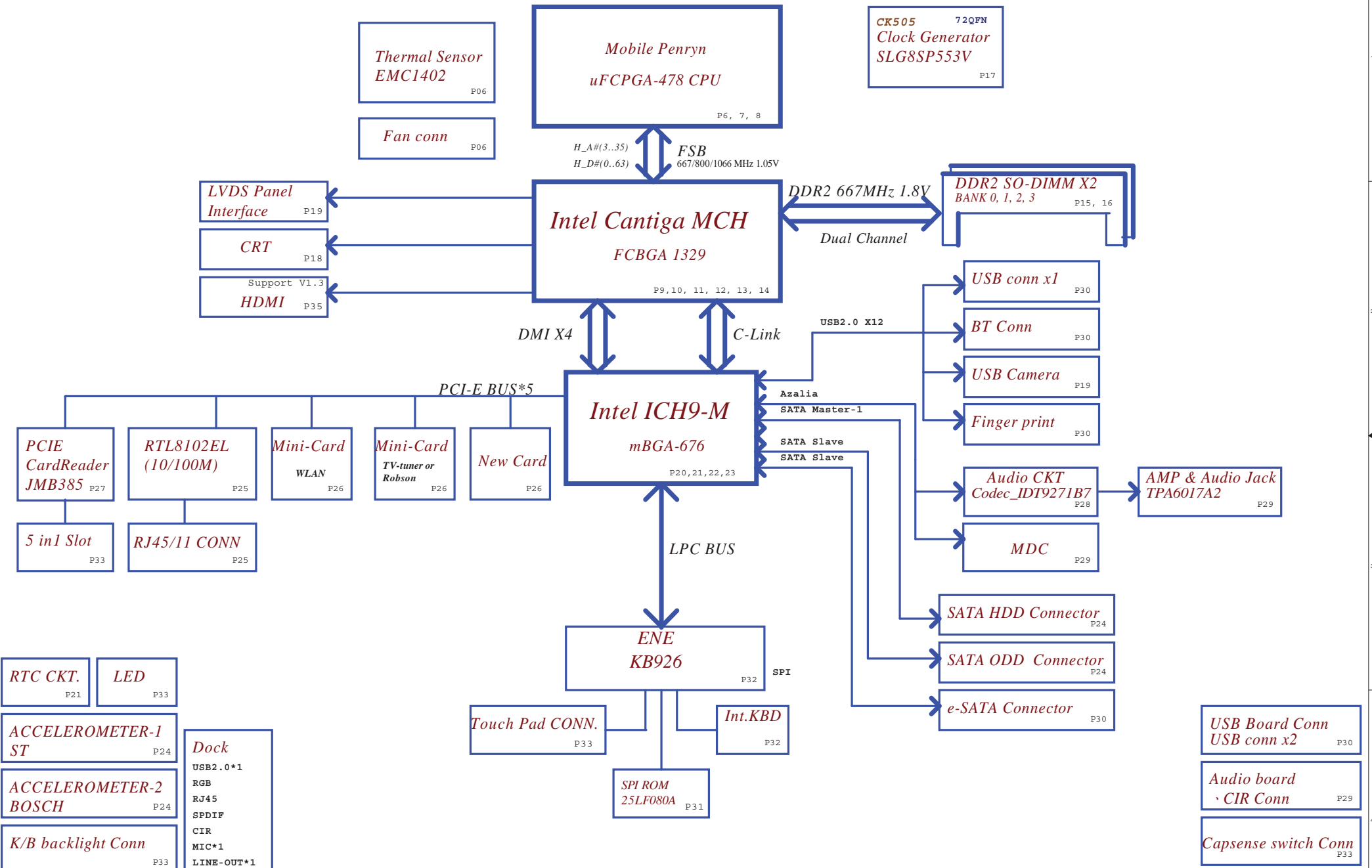
Mobile Penryn uFCPGA with Intel  
Cantiga\_GM+ICH9-M core logic

2008-01-01

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	產出人員	
	產出日期	
	解密日期	

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# Montevina Consumer 14" UMA



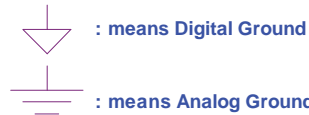
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### Voltage Rails

O MEANS ON X MEANS OFF

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### Symbol Note :



@ :	means just reserve , no build
45 @ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

### USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

### PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

### SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@  
 43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@  
 43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@  
 43154432L04 : OPP@/DEBUG@  
 43154432L05 : OPP@/DEBUG@

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

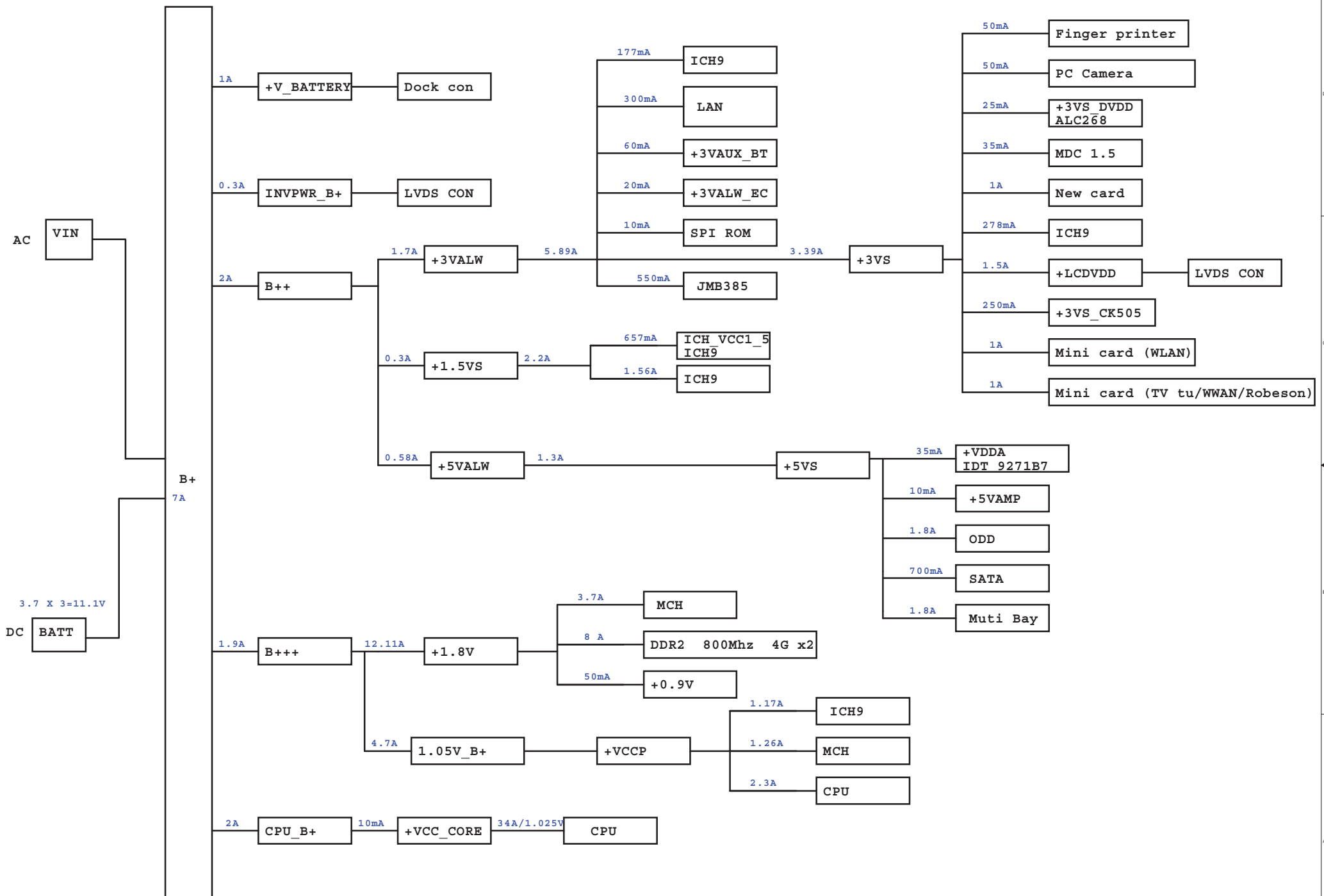
43154432L01 : UMA GM PA FF (SI-1)  
 43154432L02 : UMA GM PR FF (SI-1)  
 43154432L03 : UMA GL PR FF-  
 43154432L04 : UMA GM OPP (SI-1)  
 43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930  
 ICH9M A2 ES2 Base : SA00002AN10

DA600007100 --->Main  
 DAZ03V00100 --->OPP

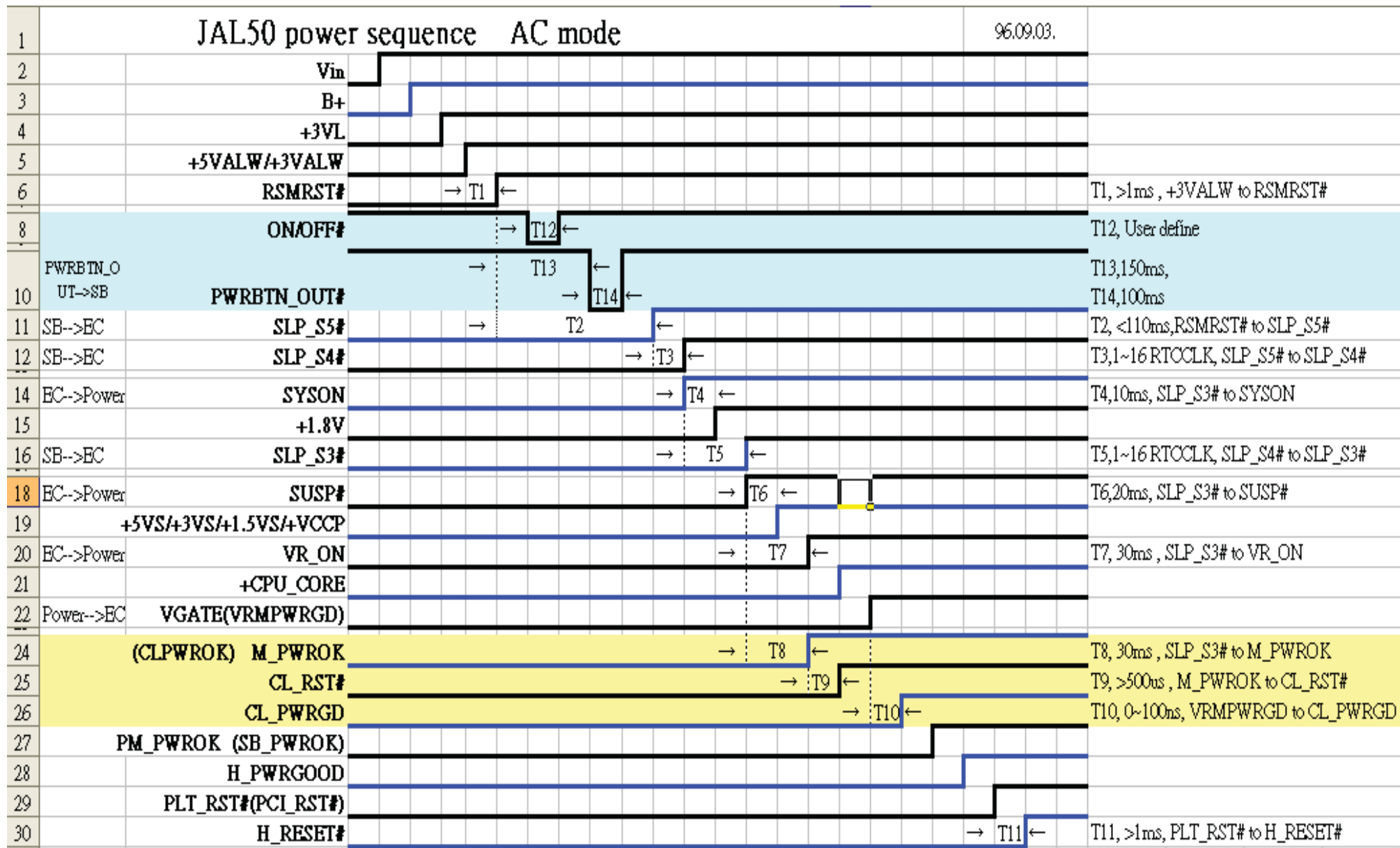
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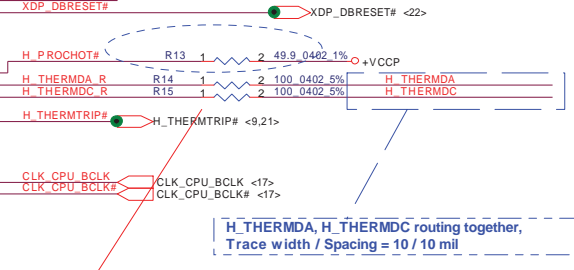
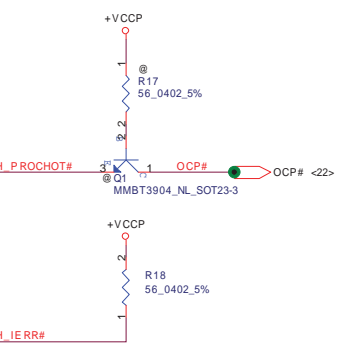
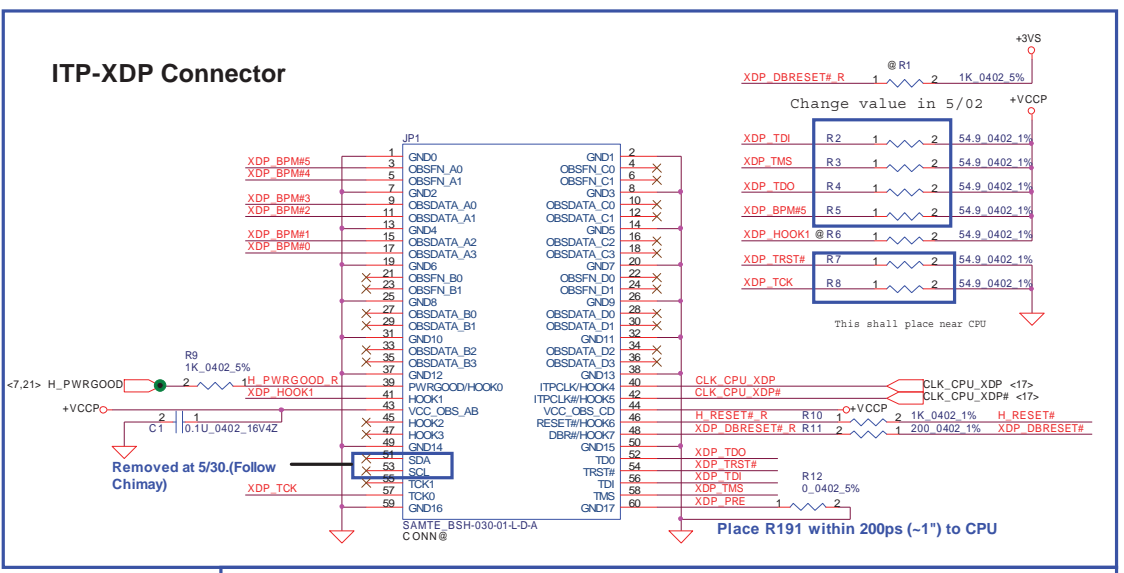
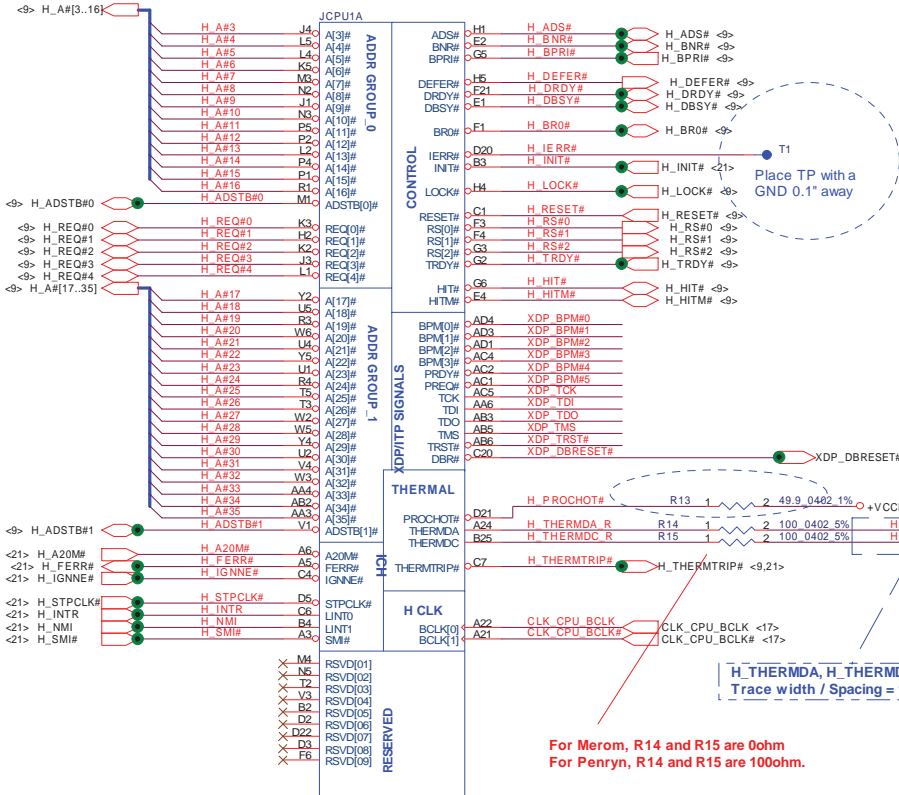
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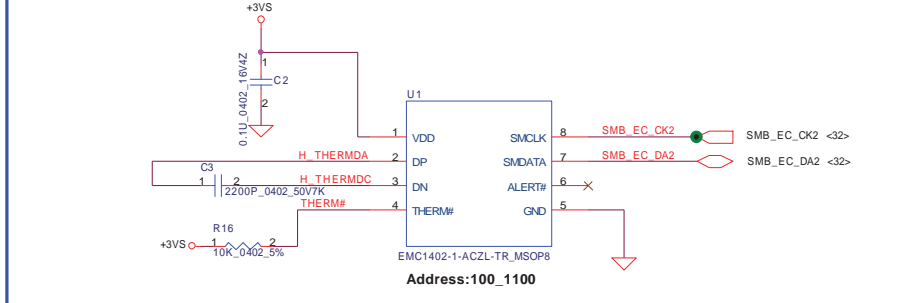
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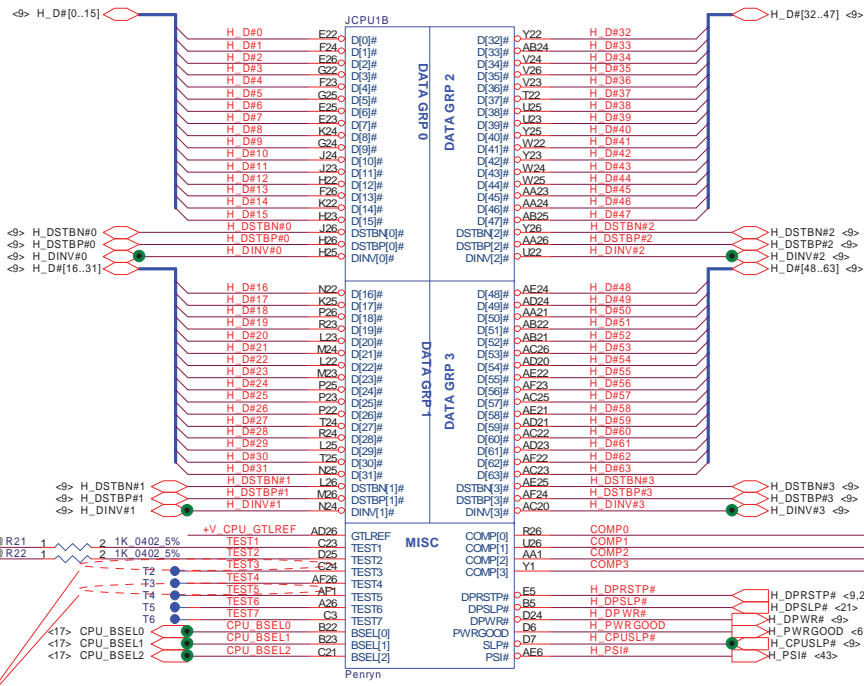


For Merom, R14 and R15 are 0ohm  
For Penryn, R14 and R15 are 100ohm.



### PWM Fan Control circuit

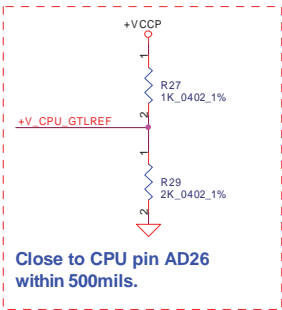
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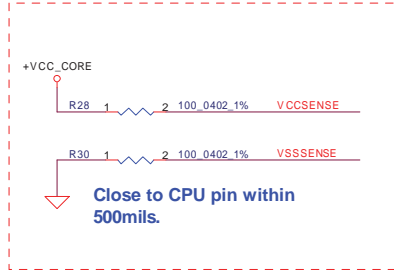
\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

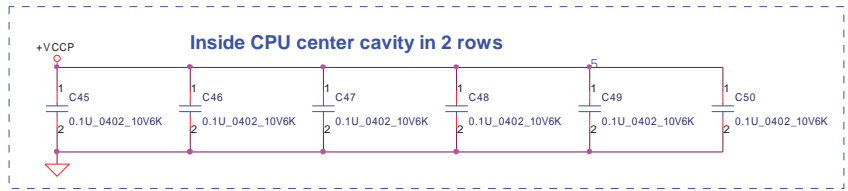
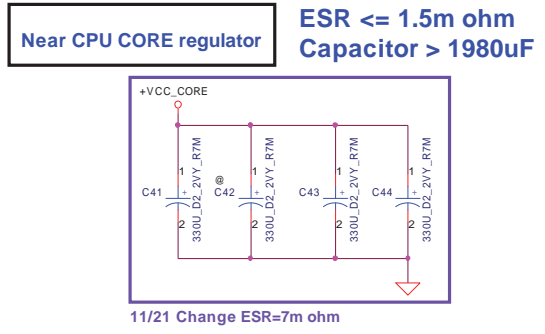
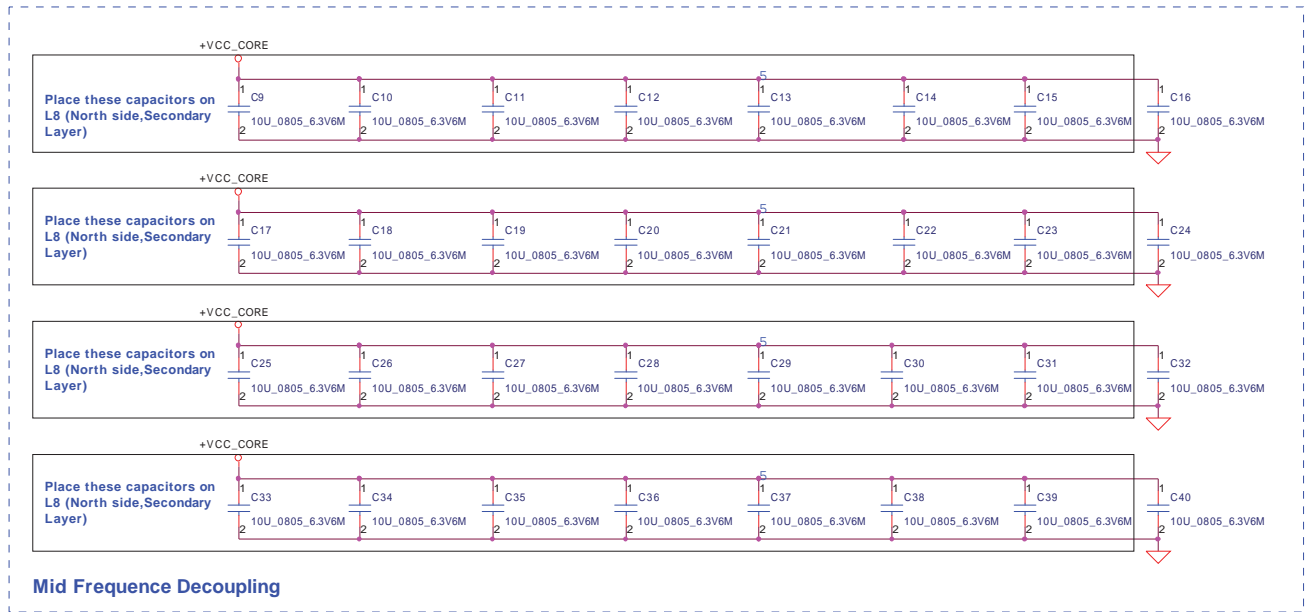
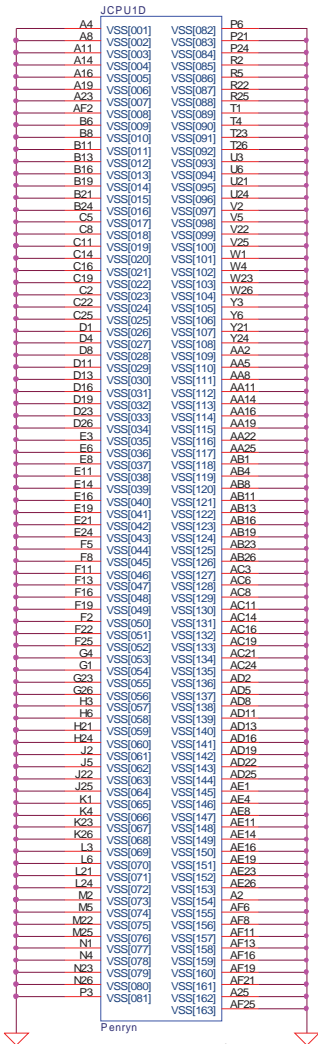
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



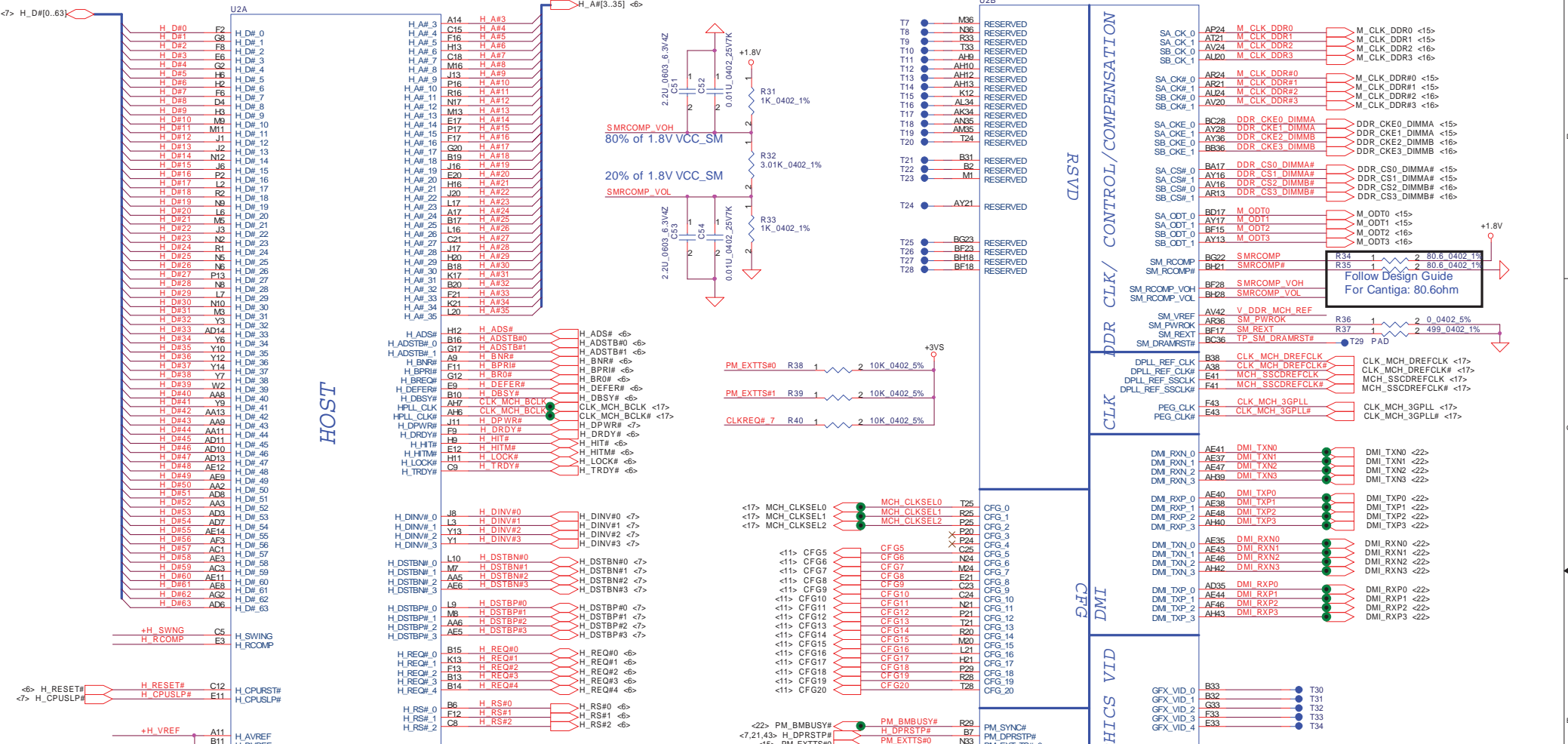
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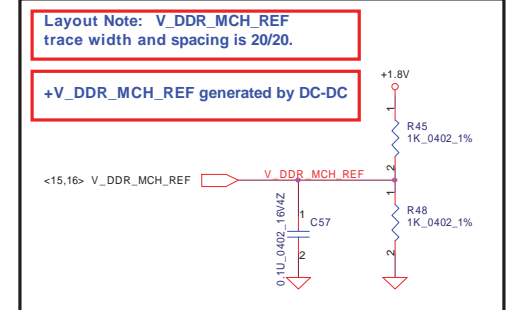
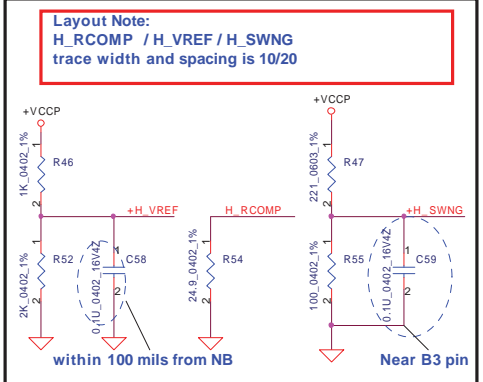
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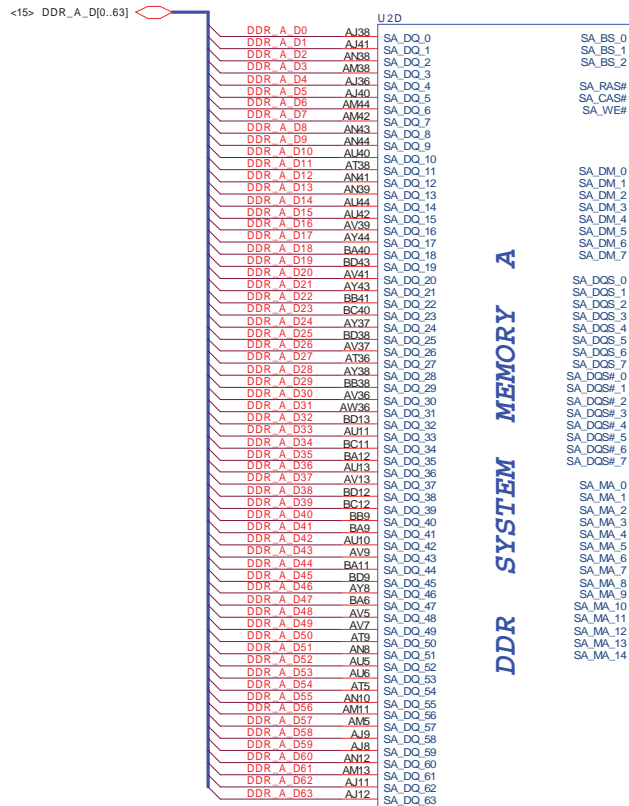


**Layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



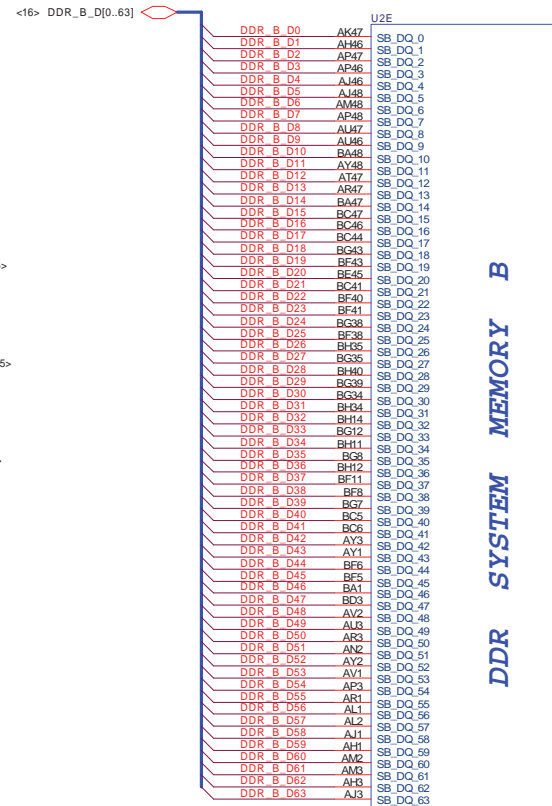
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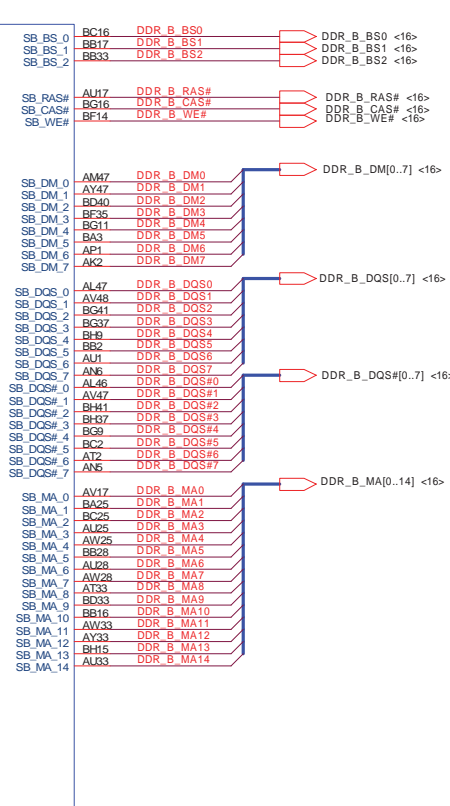
CANTIGA ES\_FCBGA1329

DDR SYSTEM MEMORY A



CANTIGA ES\_FCBGA1329

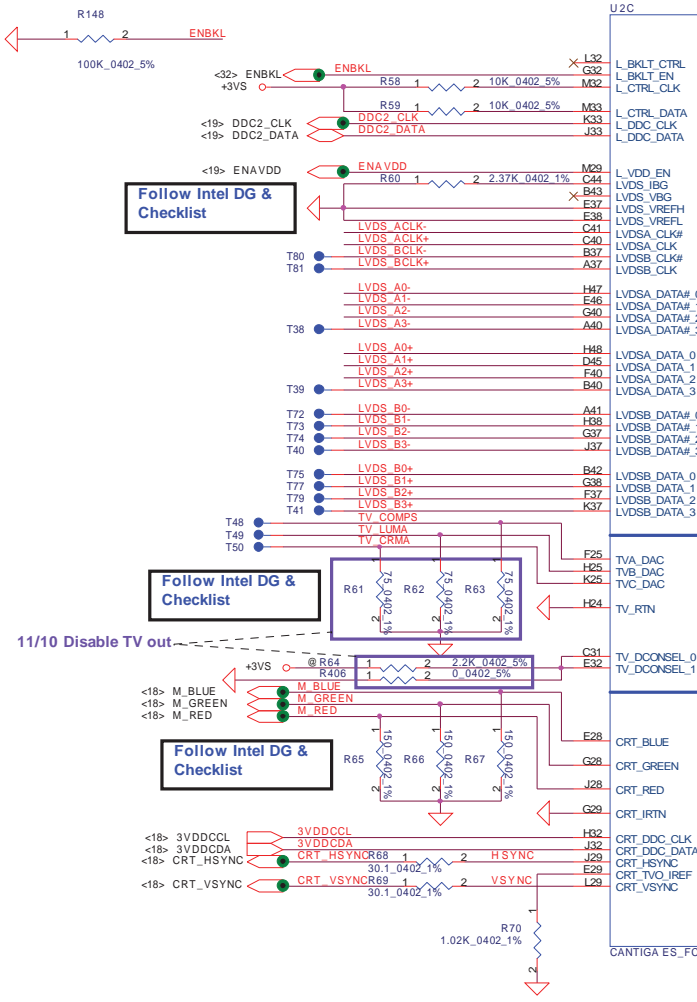
DDR SYSTEM MEMORY B



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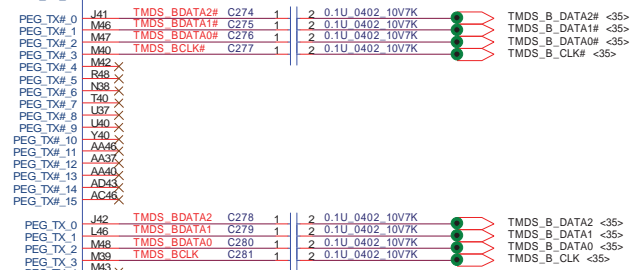
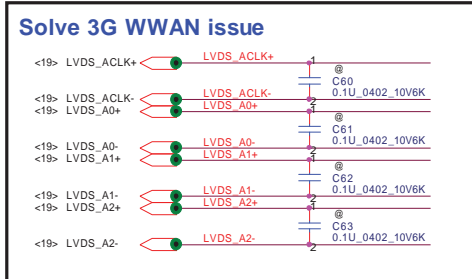


Follow Intel DG & Checklist

Follow Intel DG & Checklist

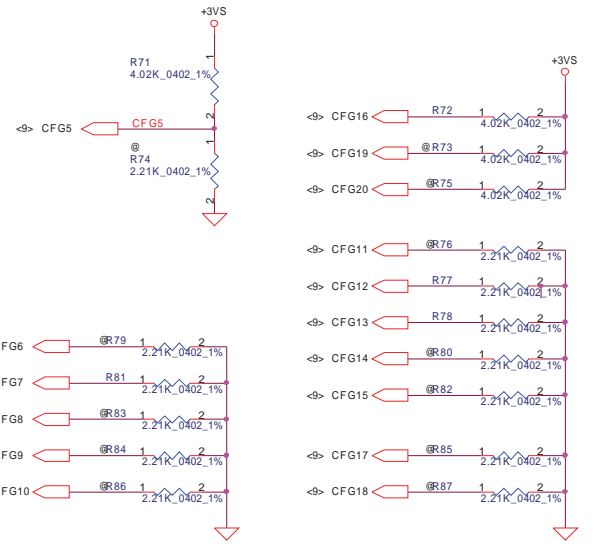
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11/10 Disable TV out



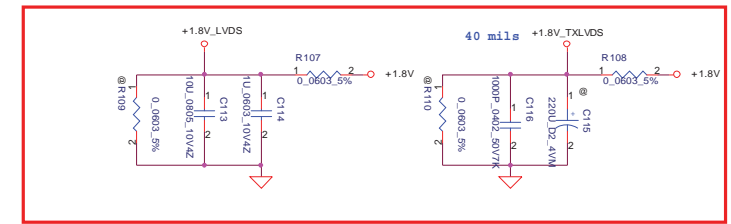
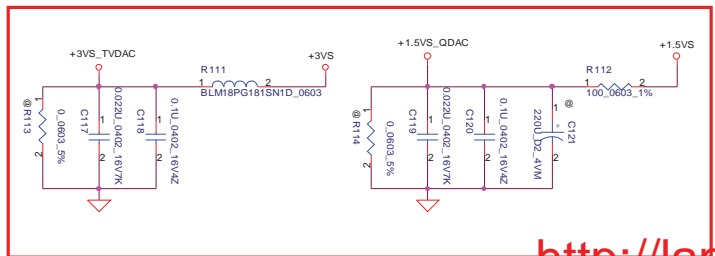
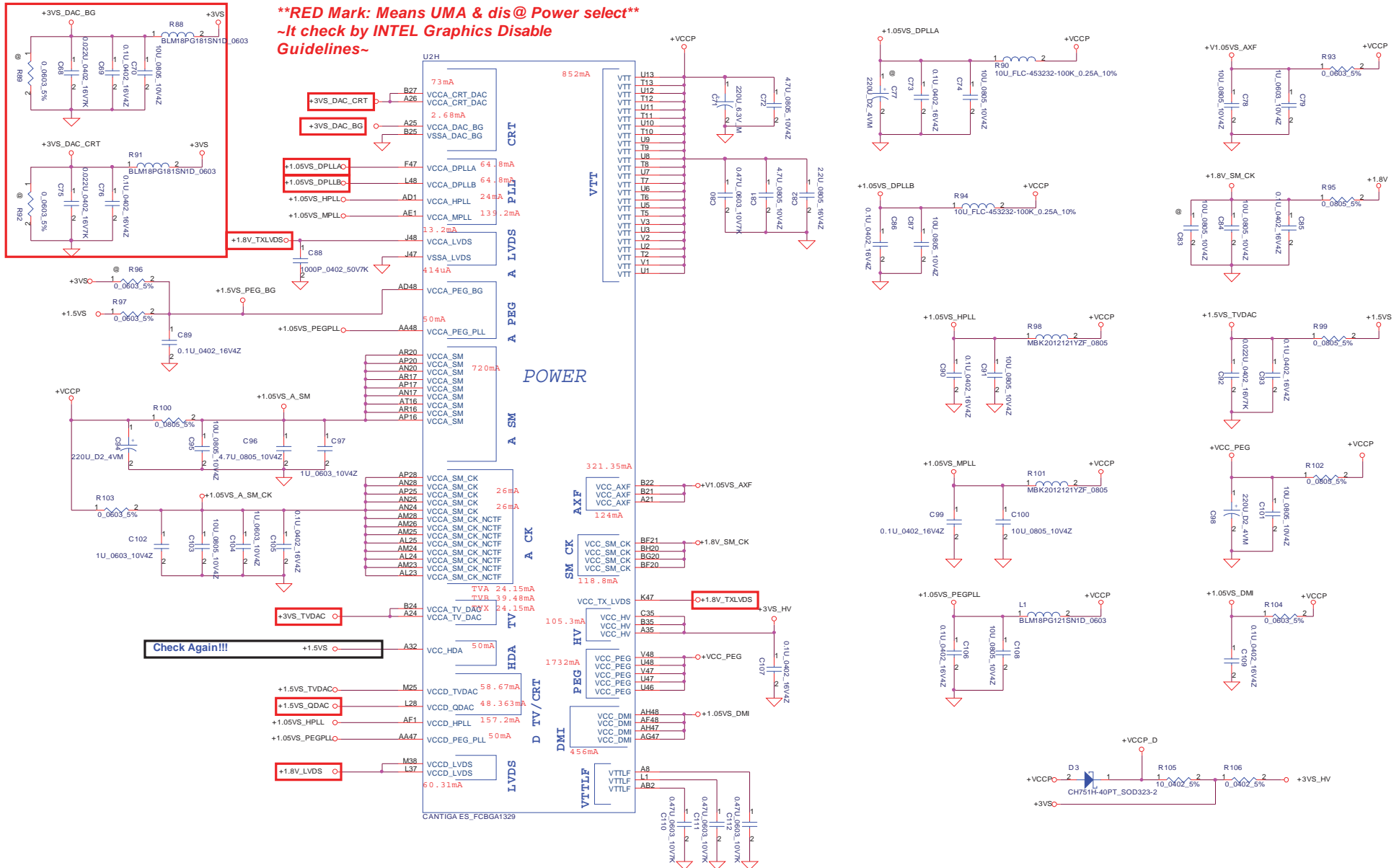
## Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



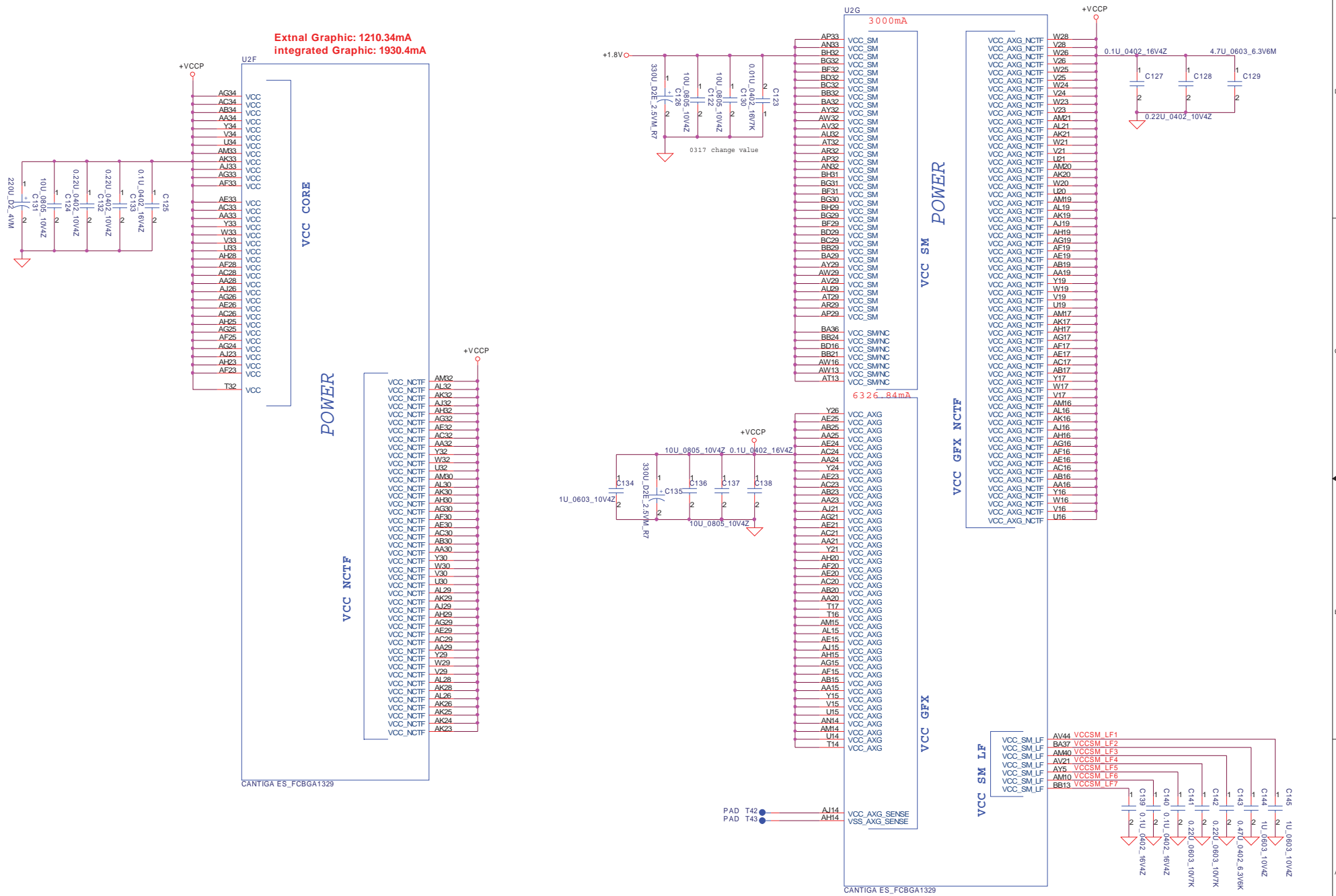
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**\*\*RED Mark: Means UMA & dis@ Power select\*\***  
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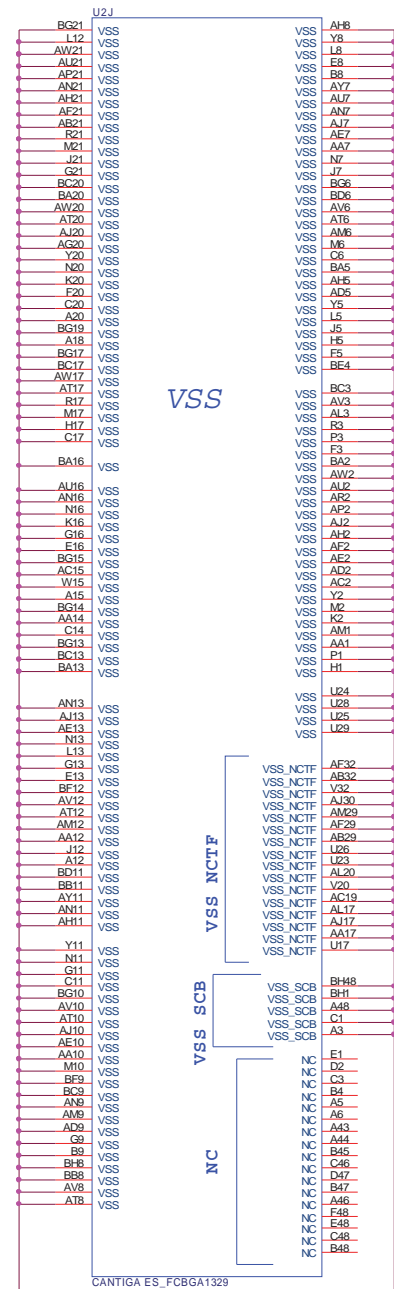
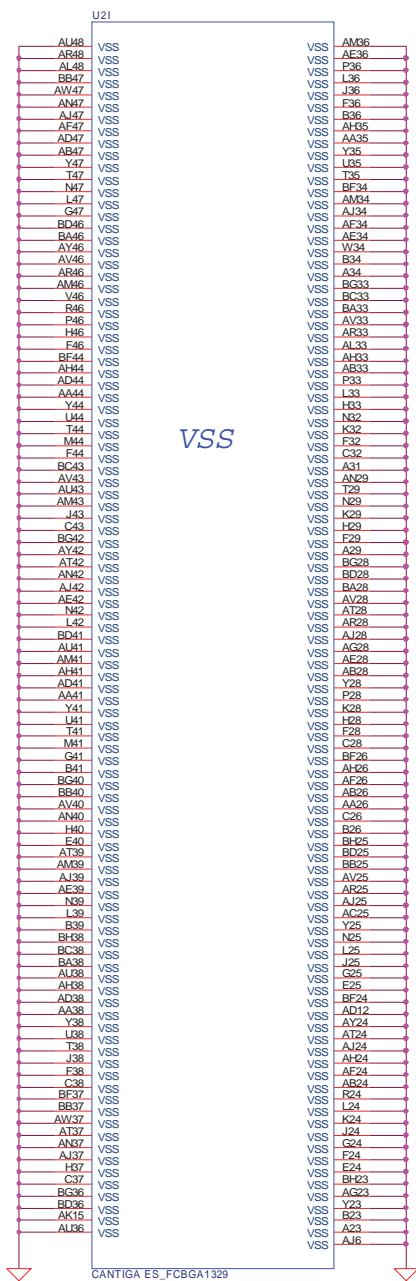
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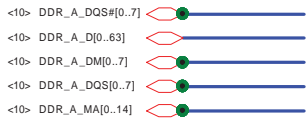
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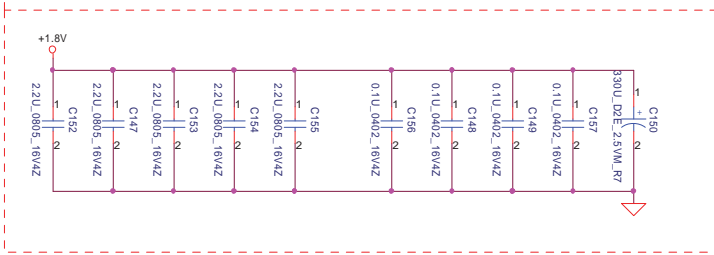


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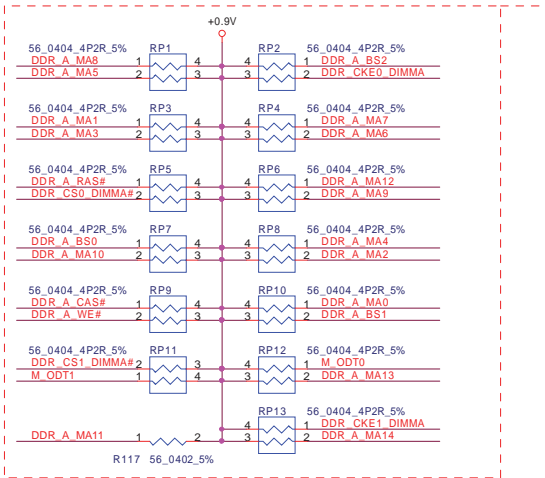
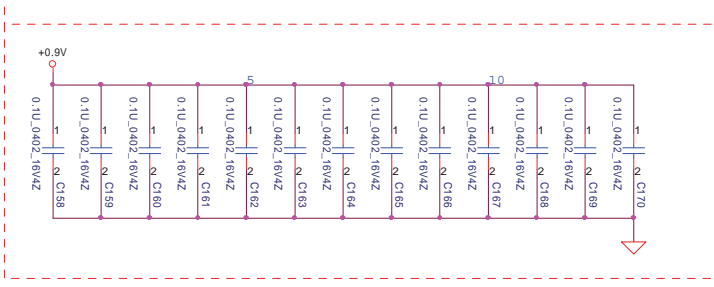
<http://laptop-motherboard-schematic.blogspot.com>



**Layout Note:**  
Place near JP3



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V5



**Layout Note:**  
Place these resistor closely JP3, all trace length Max=1.5"



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				<b>DDRII-SODIMM SLOT1</b>
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http://laptop-motherboard-schematic.blogspot.com				Montevina Blade UMA LA4101P
Date: Saturday, January 05, 2008				Rev 0.3
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<10> DDR\_B\_DQS[0..7]

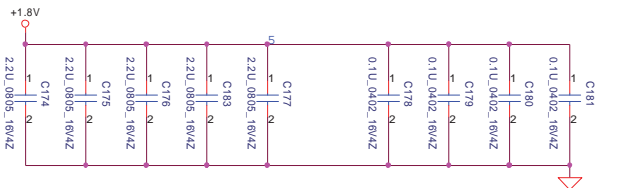
<10> DDR\_B\_D[0..63]

<10> DDR\_B\_DM[0..7]

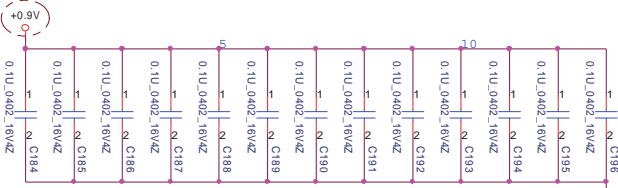
<10> DDR\_B\_DQS[0..7]

<10> DDR\_B\_MA[0..14]

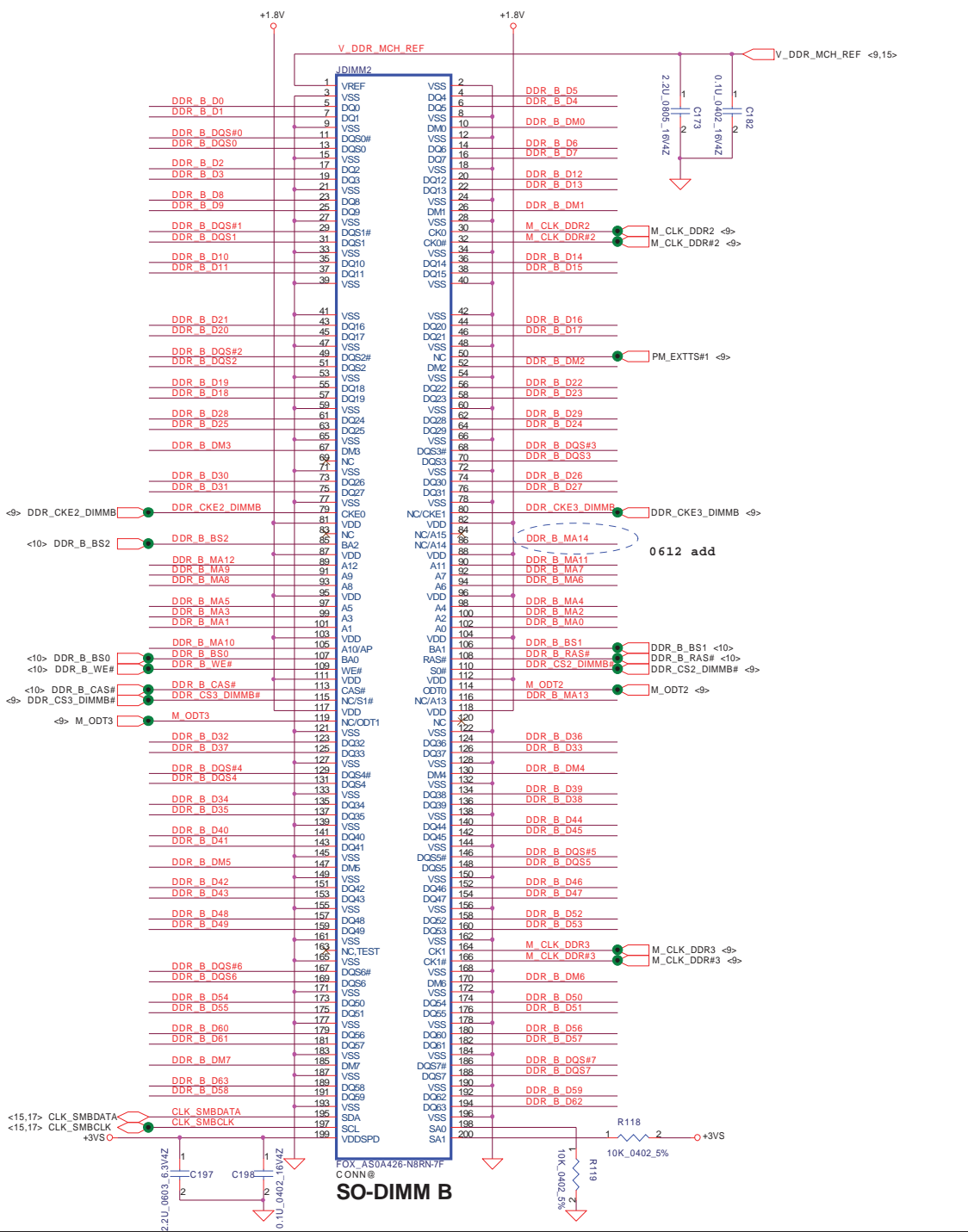
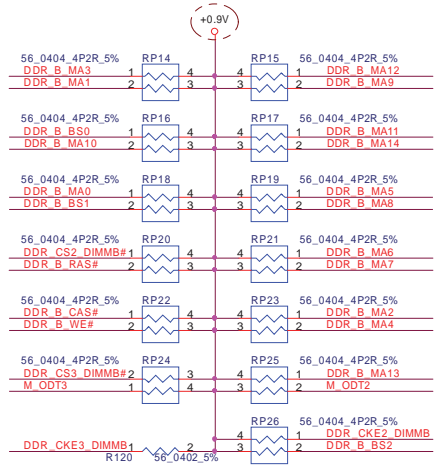
**Layout Note:**  
Place near JP10



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP3, all trace length Max=1.5"

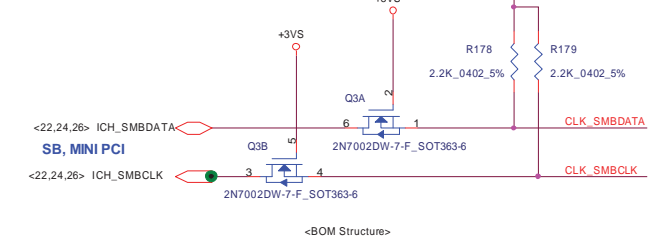
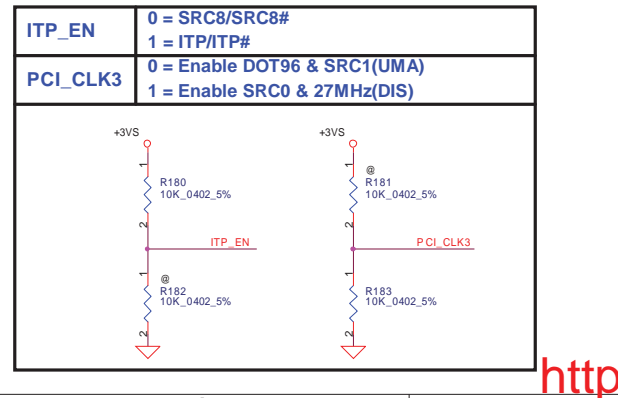
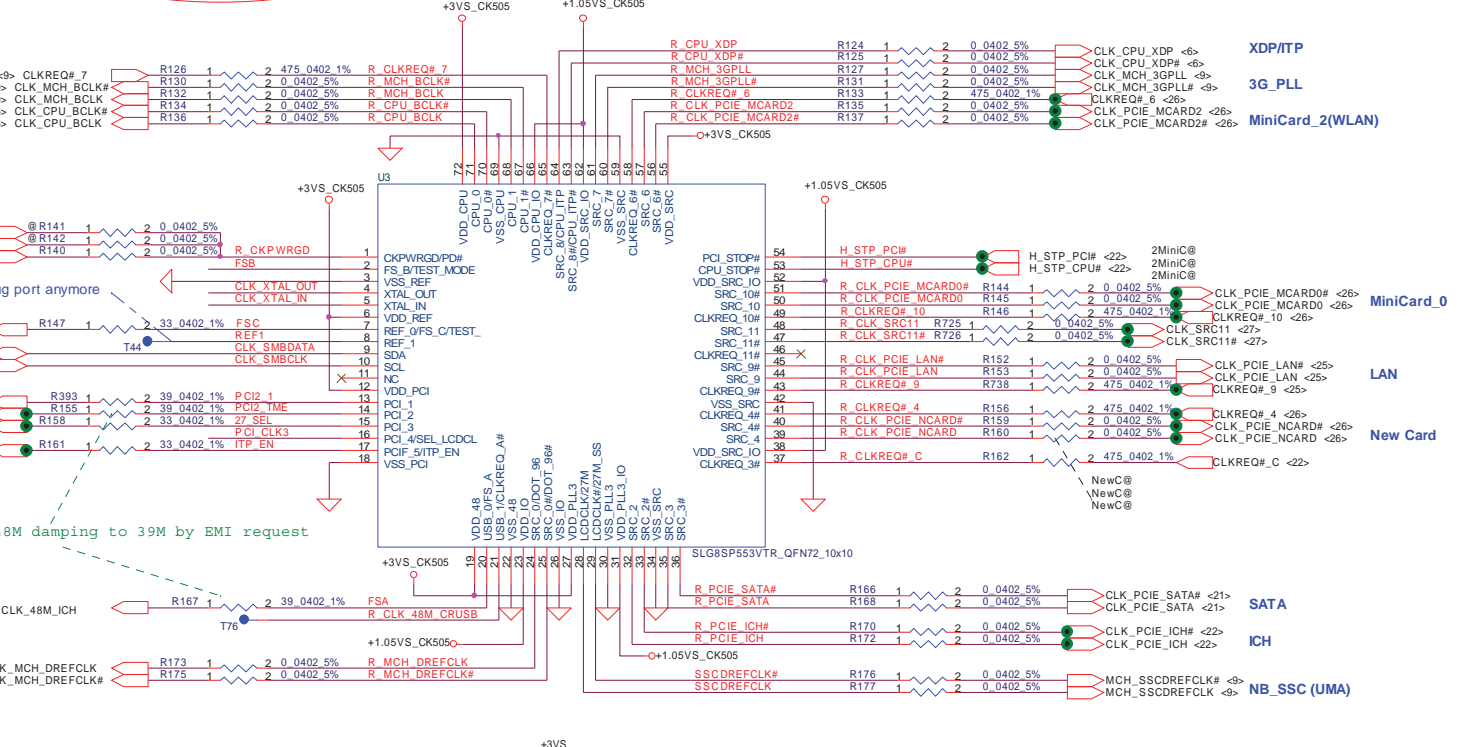
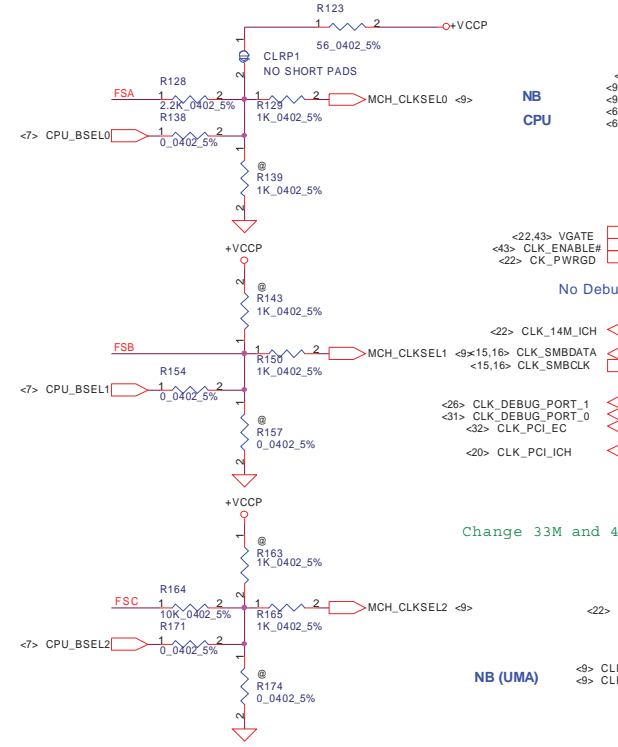
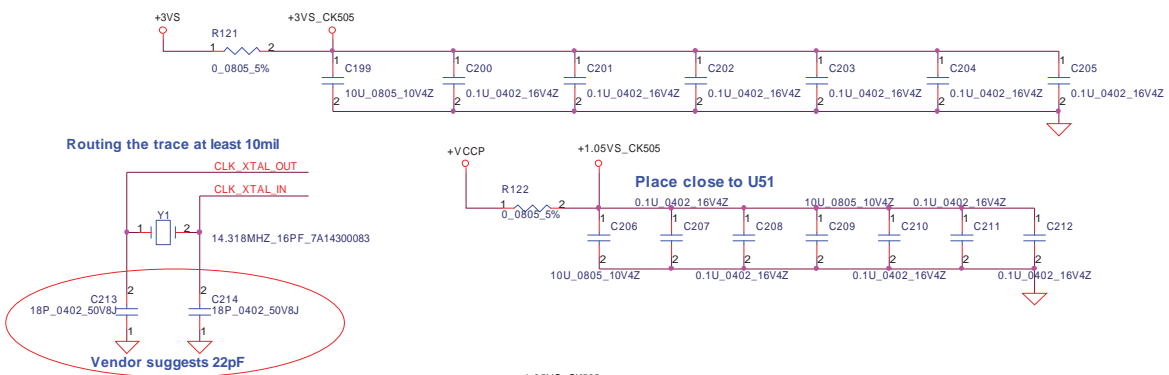


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				Compal Electronics, Inc.	
				DDRII-SODIMM SLOT2	
				Montevina Blade UMA LA4101P	
				Size	Document Number
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

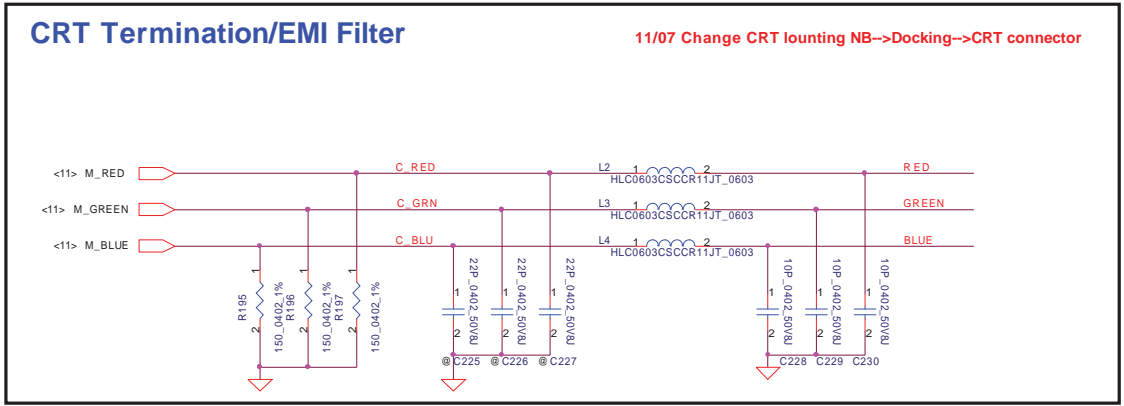
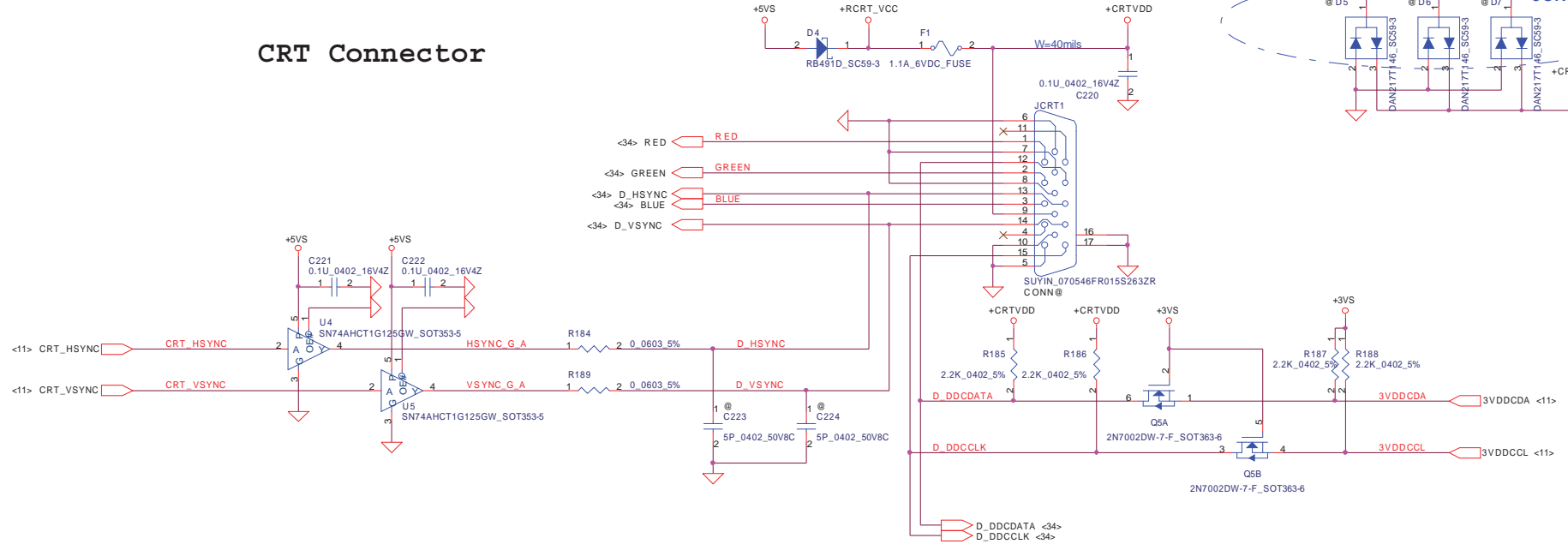


@C215	5P_0402_50V8C	2	1	CLK_48M_ICH
@C216	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@C217	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@C218	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@C219	5P_0402_50V8C	2	1	CLK_DEBUG_PORT_0

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Size	Document Number	Rev	
	Montevina Blade UMA LA4101P	0.3	
Date:	Saturday, January 05, 2008	Sheet	17 of 46

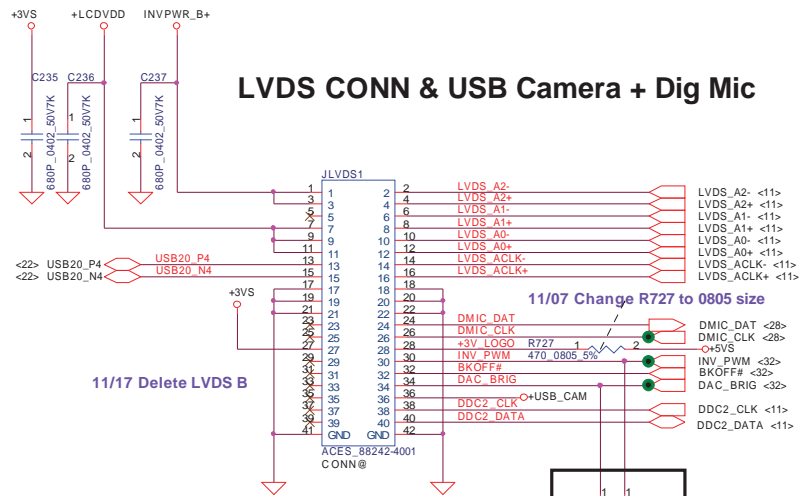
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# CRT Connector



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				Montevina Blade UMA LA4101P	
				Rev	0.3
				Date:	Saturday, January 05, 2008
				Sheet	18 of 46

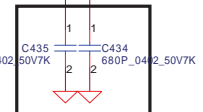
<http://laptop-motherboard-schematic.blogspot.com/>



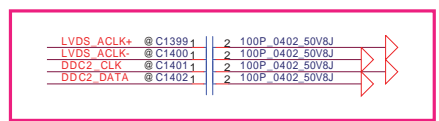
### LVDS CONN & USB Camera + Dig Mic

11/17 Delete LVDS B

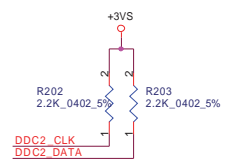
11/07 Change R727 to 0805 size



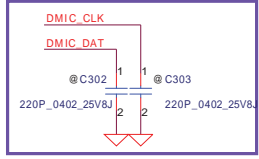
0308 Install all cap for EMI request.



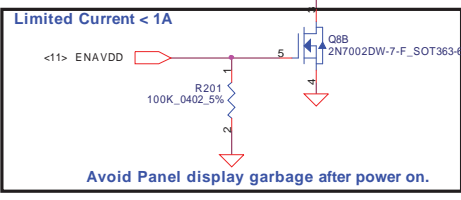
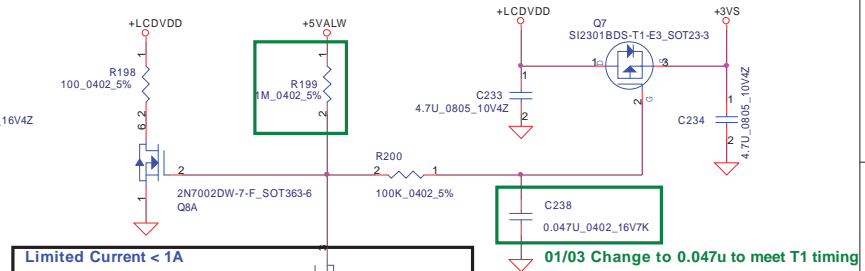
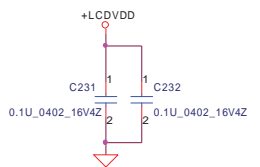
0831 EMI request



Must close JLVD51pin 24 - 26

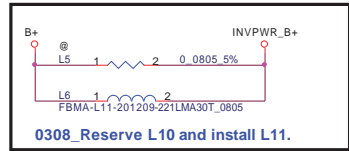


11/09 EMI reserver

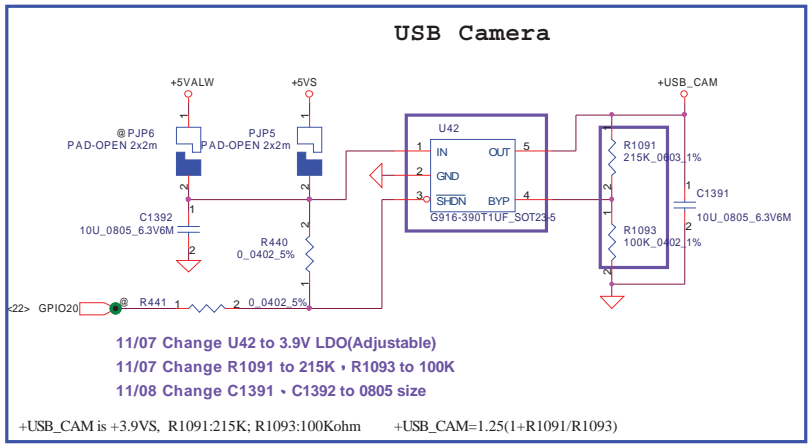


Avoid Panel display garbage after power on.

01/03 Change to 0.047u to meet T1 timing



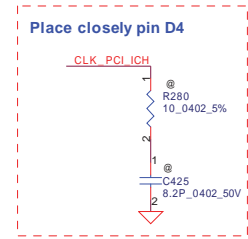
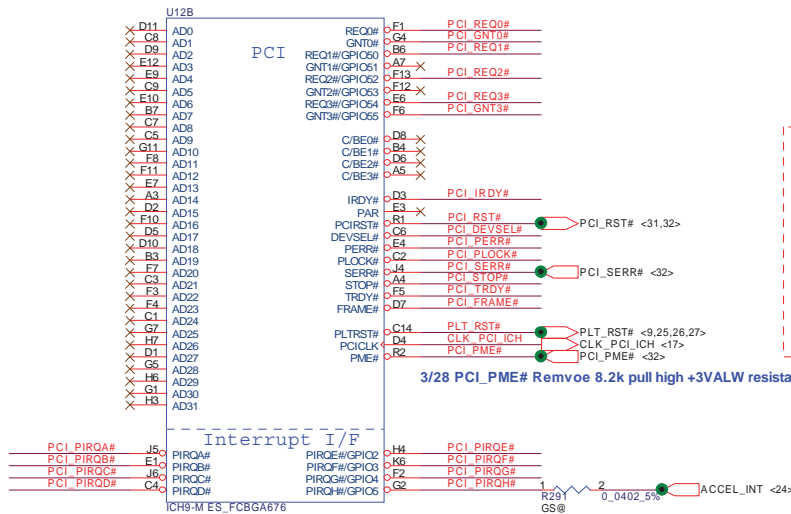
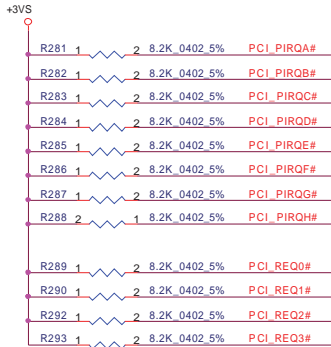
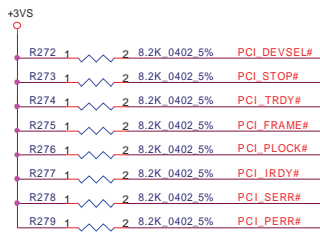
0308 Reserve L10 and install L11.



11/07 Change U42 to 3.9V LDO(Adjustable)  
 11/07 Change R1091 to 215K + R1093 to 100K  
 11/08 Change C1391 + C1392 to 0805 size

+USB\_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB\_CAM=1.25(1+R1091/R1093)

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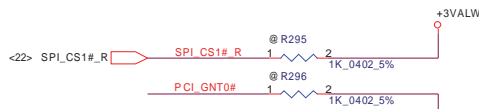
### A16 swap override Strap

PCI\_GNT3# Low= A16 swap override Enable  
High= Default \*

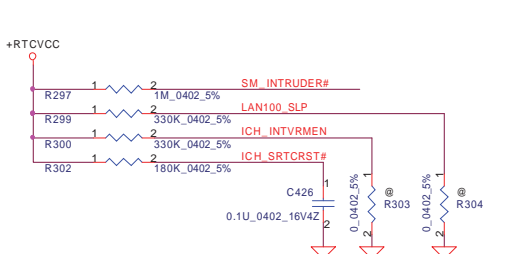


### Boot BIOS Strap

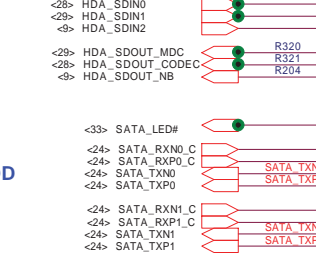
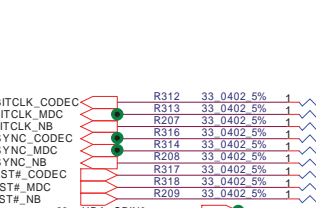
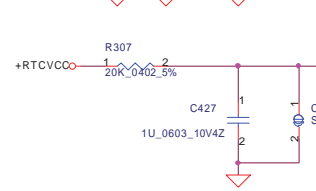
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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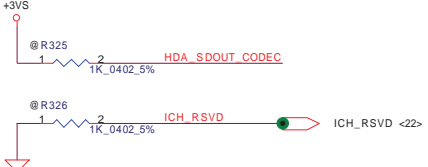


<b>ICH8M Internal VR Enable Strap</b> (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
<b>ICH8M LAN100 SLP Strap</b> (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



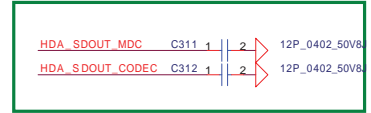
P-HDD

**XOR CHAIN ENTRANCE STRAP:RSVD**

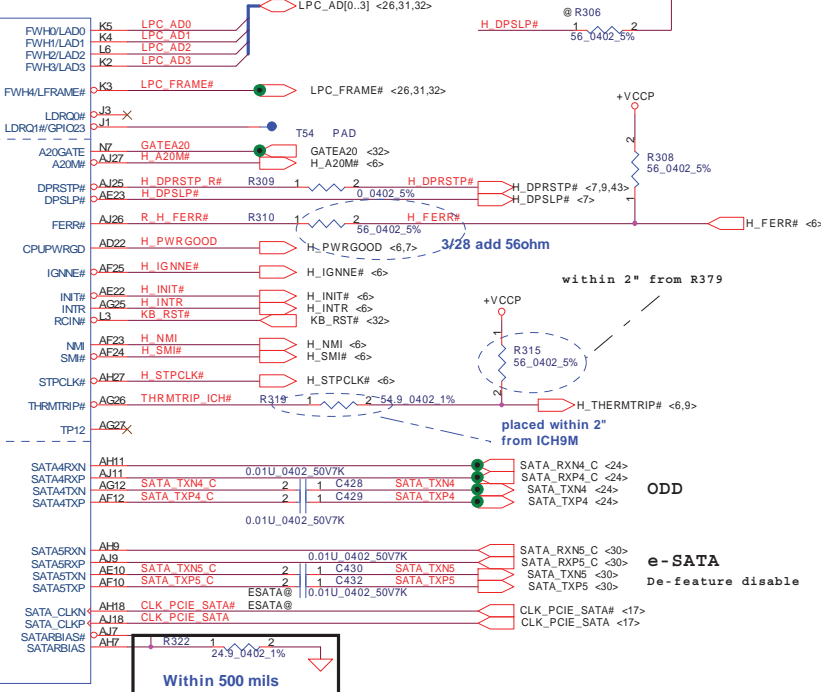
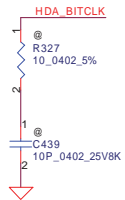
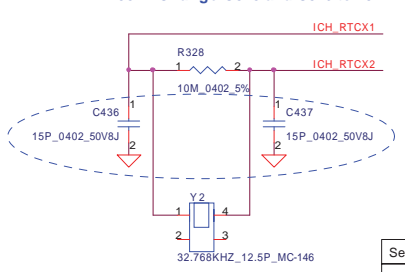


ICH_RSVD	HDA_SDOUT_CODEC
0	0
0	1
1	0
1	1

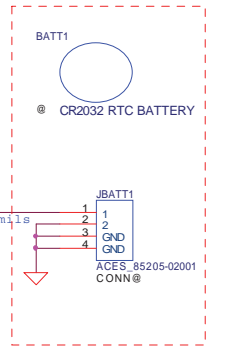
**Add 12p on HDA\_SDOUT and HDA\_SDOUT**



**0821 Change C528 and C516 to 15PF**

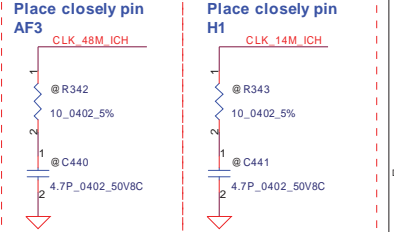
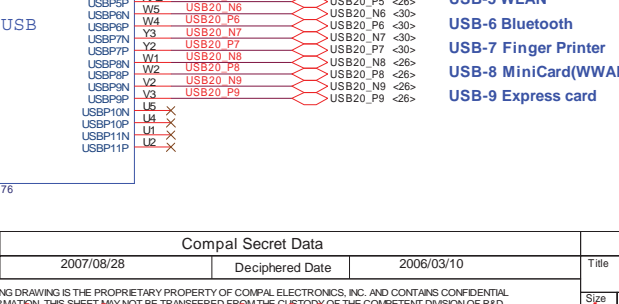
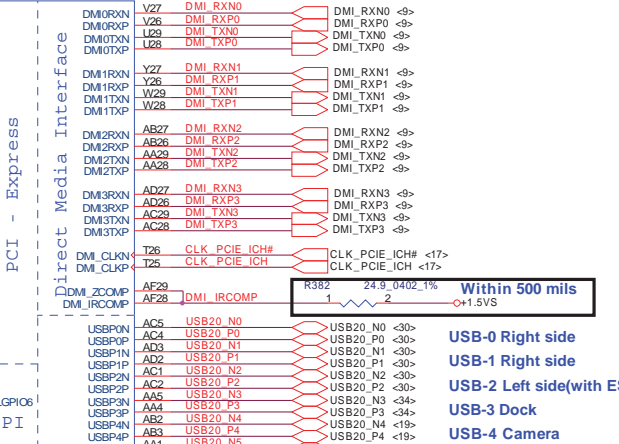
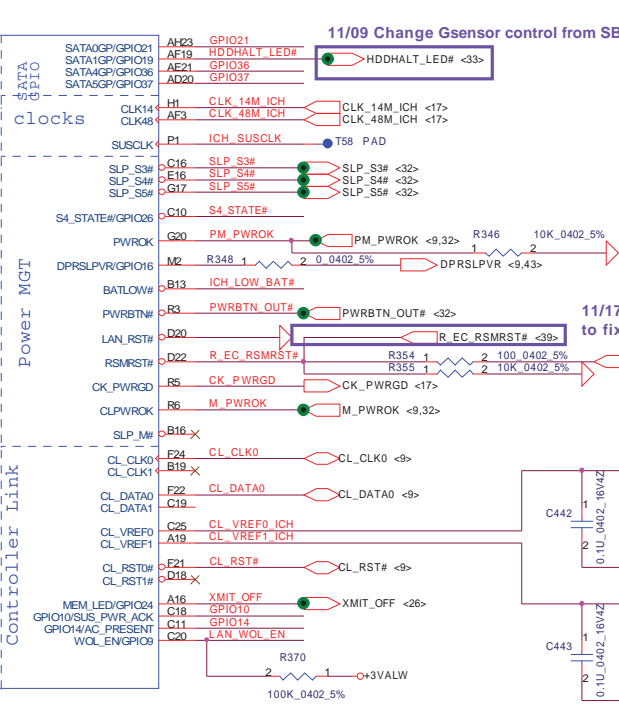
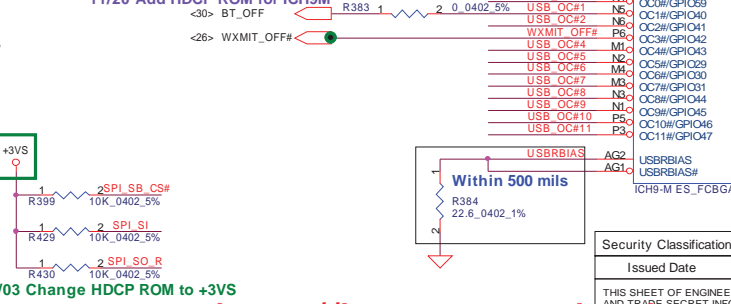
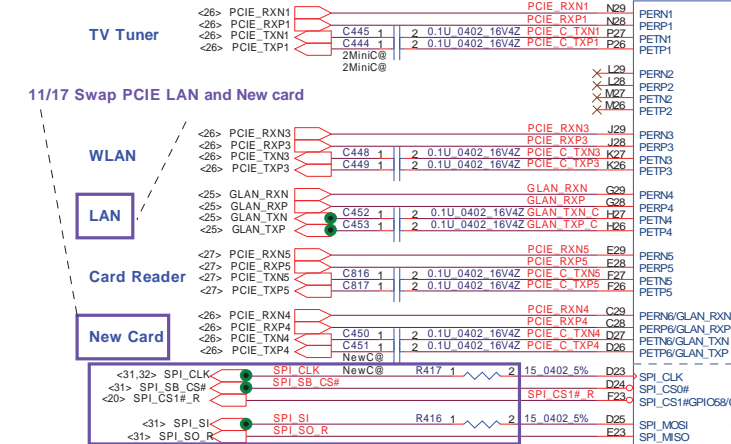
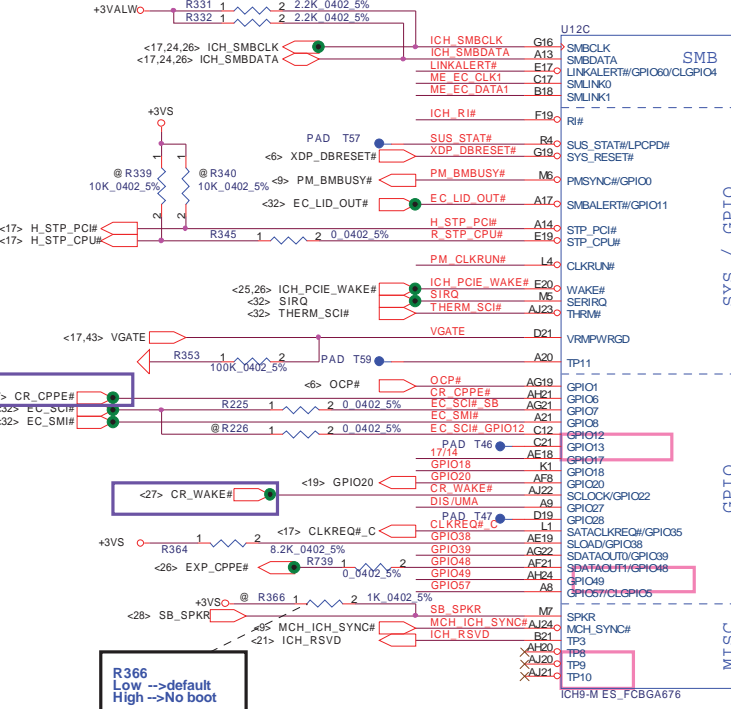
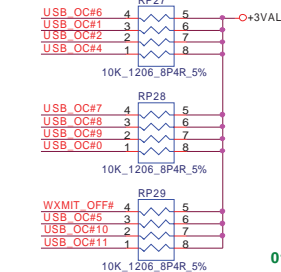
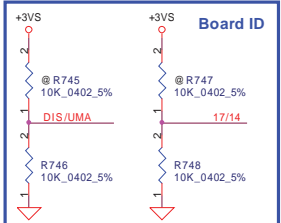
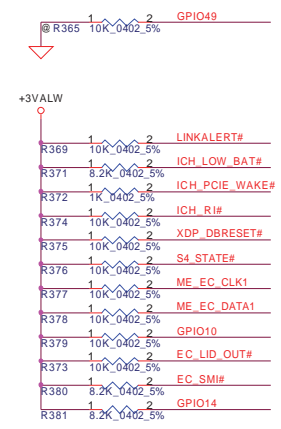
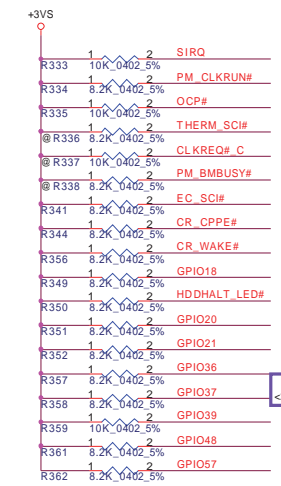


e-SATA  
De-feature disable

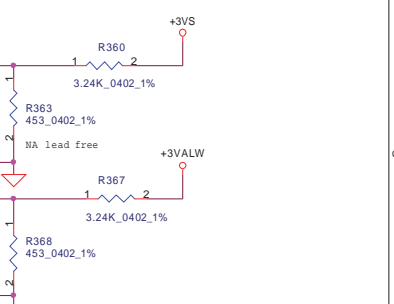


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<b>ICH9(2/4) LAN,HD,IDE,LPC</b>	
Size	Document Number
Custom	Montevina Blade UMA LA410P
Date:	Rev
Saturday, January 05, 2008	0.3



11/17 Add +3VALW GD to EC\_RSMRST# to fix Battery mode can't boot issue



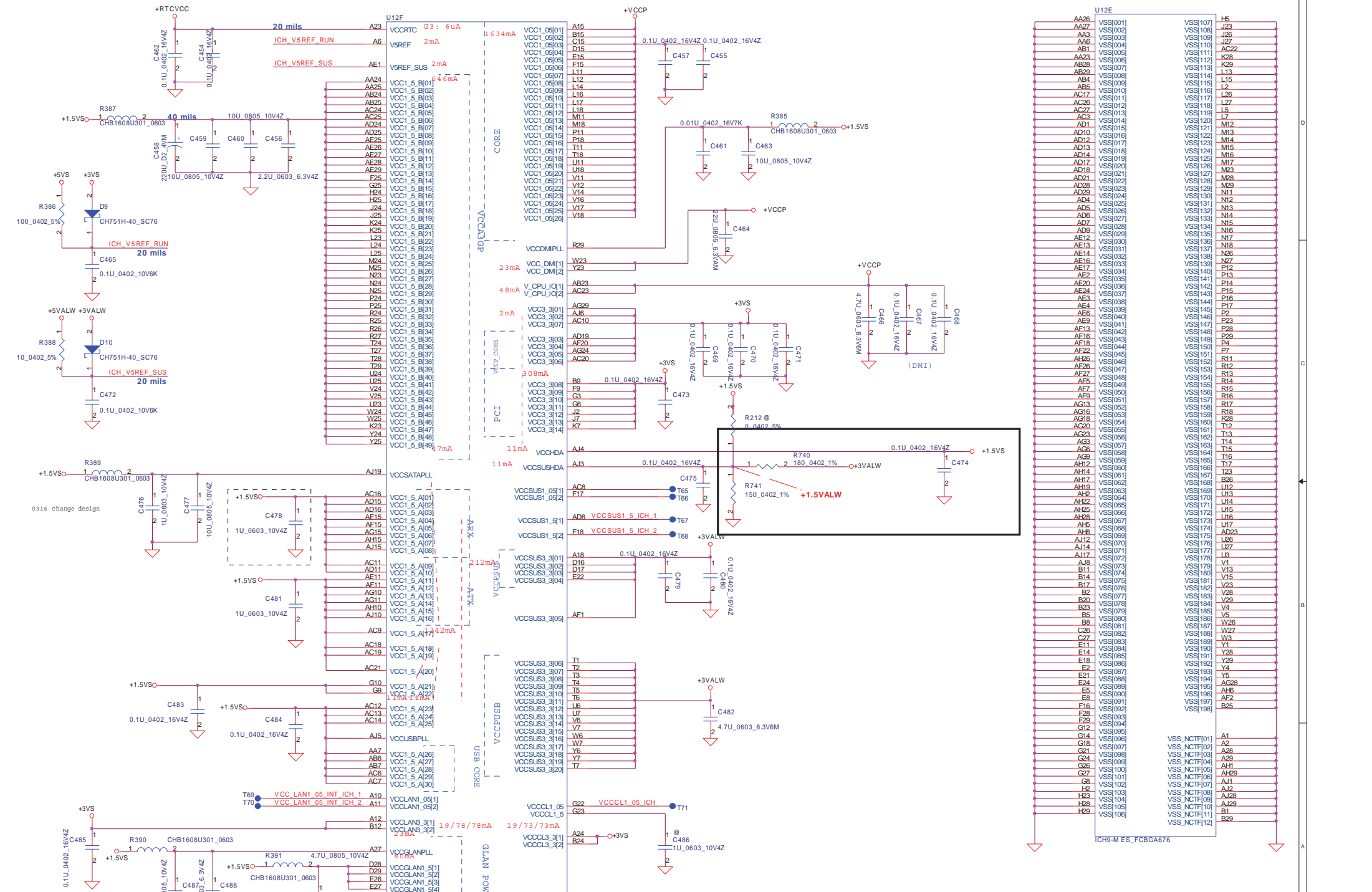
Security Classification	Compal Secret Data
Issued Date	2007/08/28
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ICH9(3/4) DMI,USB,GPIO,PCIE

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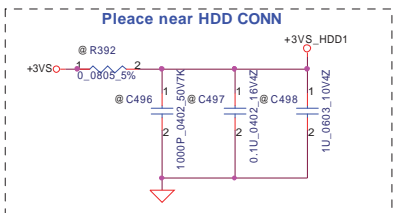
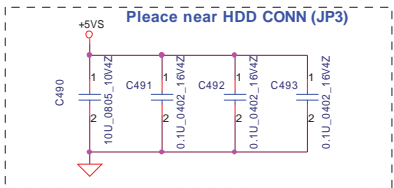
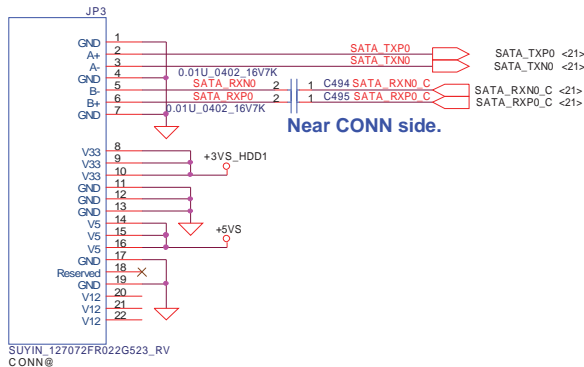
Security Classification	Compal Secret Data		Title
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.		
ICH9/4/4 POWER&GND		
Size	Document Number	Rev
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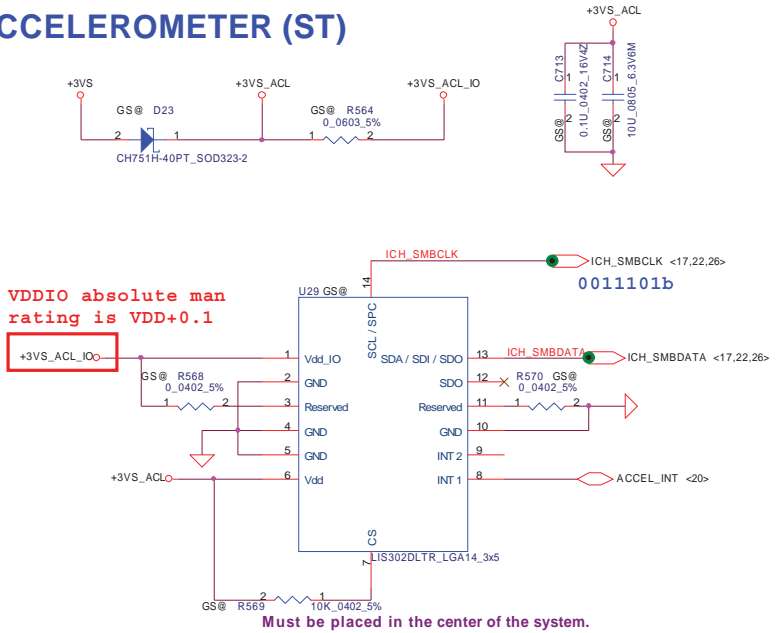
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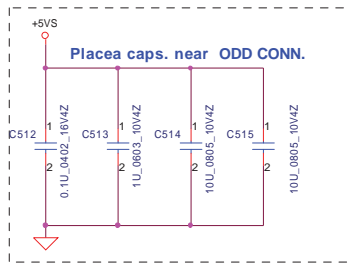
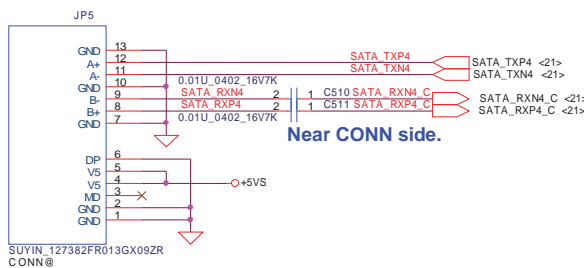
## HDD Connector



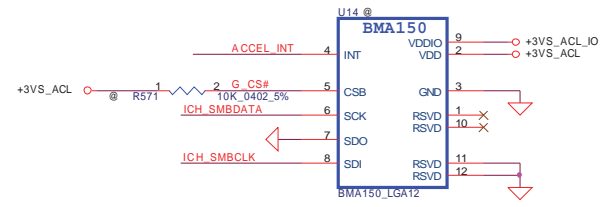
## ACCELEROMETER (ST)



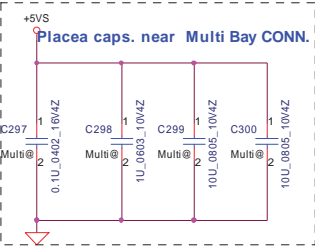
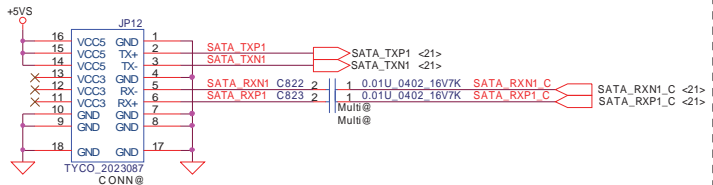
## CD-ROM Connector



## ACCELEROMETER (Bosch)



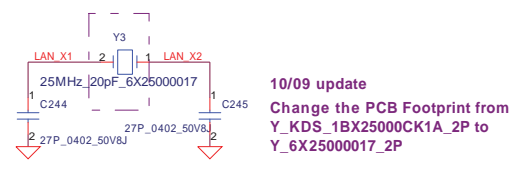
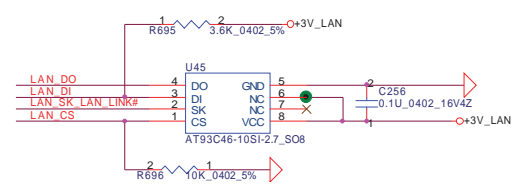
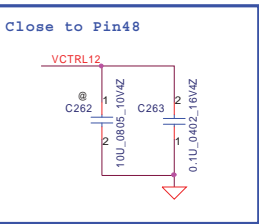
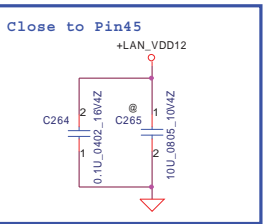
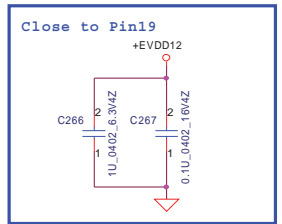
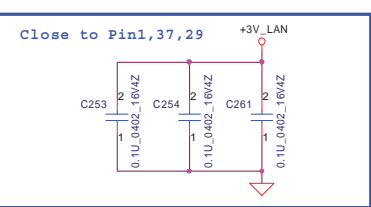
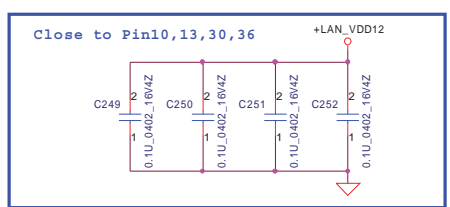
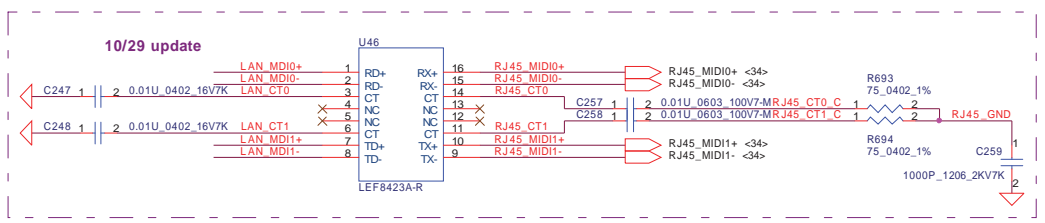
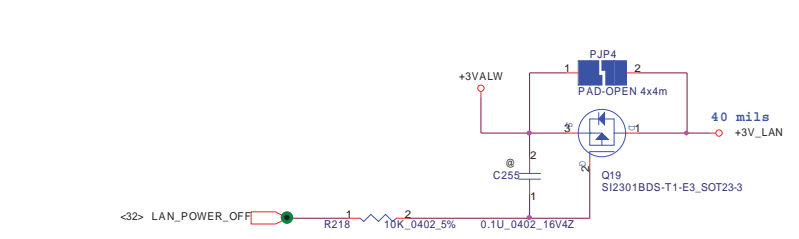
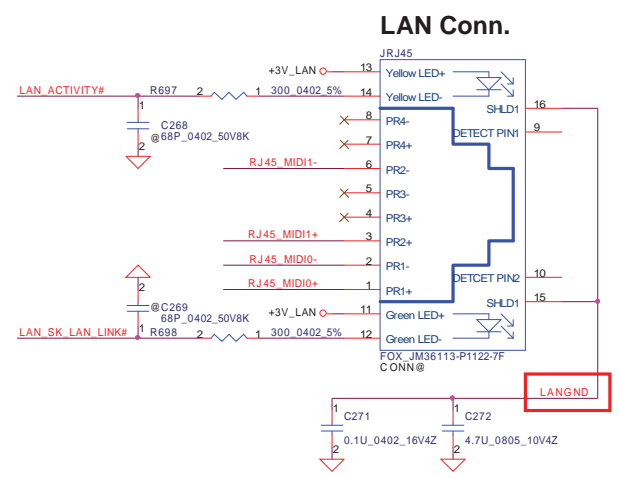
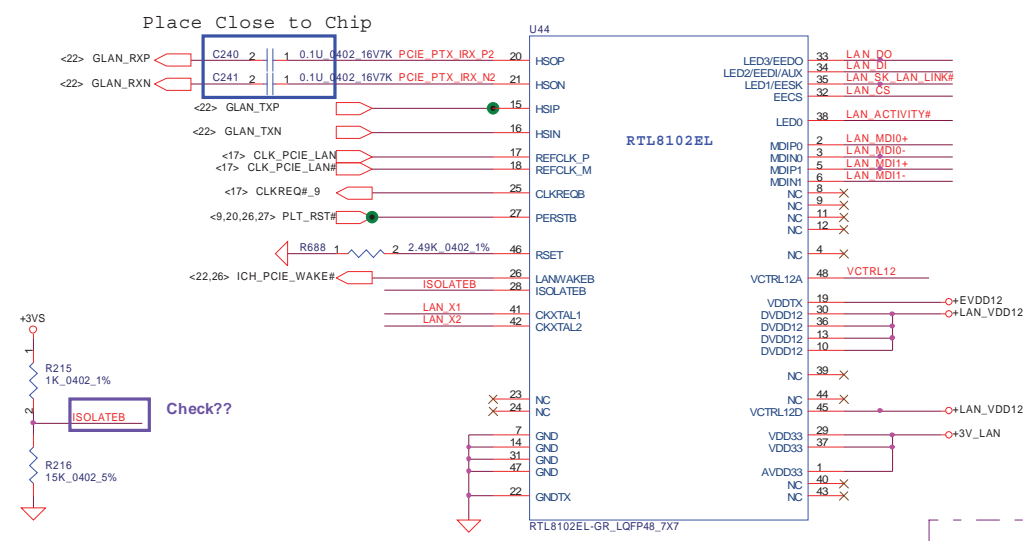
## Multi Bay



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		2006/03/10
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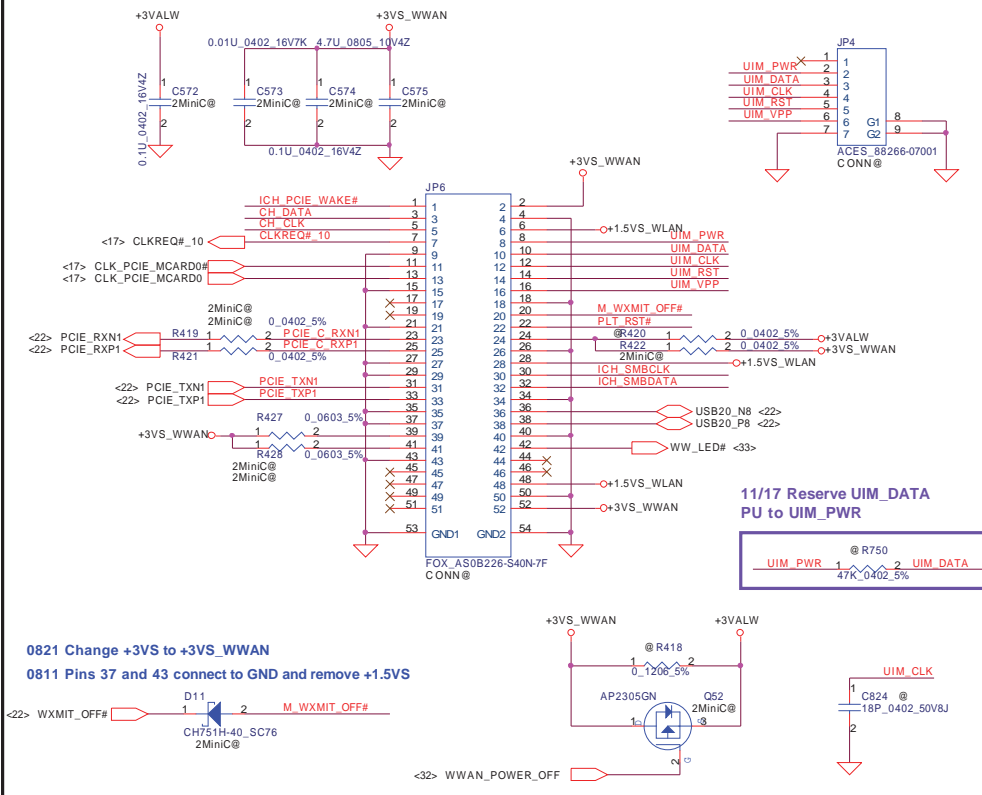
Compal Electronics, Inc.	
Title	HDD & CDROM
Size	Document Number
Custom	Montevina Blade UMA LA410IP
Date:	Saturday, January 05, 2008
Sheet	24 of 46



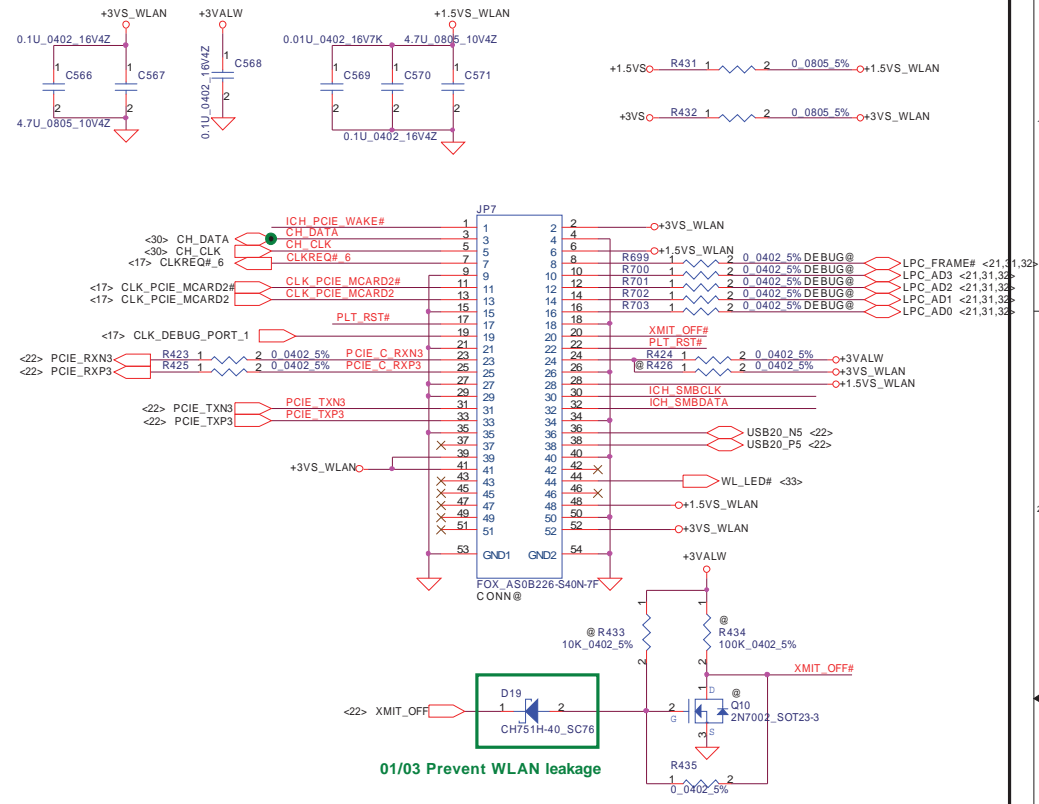


Security Classification	Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2007/06/30	RTL8102EL LAN
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				Document Number Montevina Blade UMA LA4101P
				Rev 0.3
Date: Sunday, January 05, 2008				Sheet 25 of 46

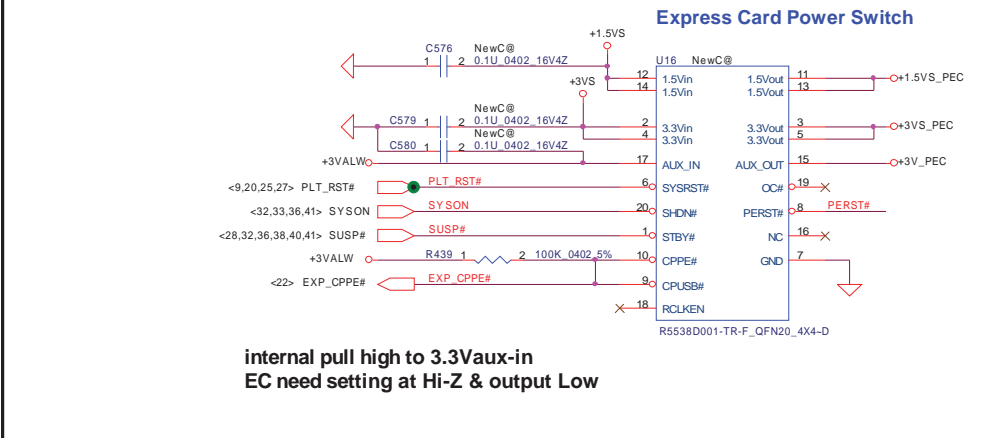
# Mini Card 0--TV tuner/WWAN/Robson SIM card Connector



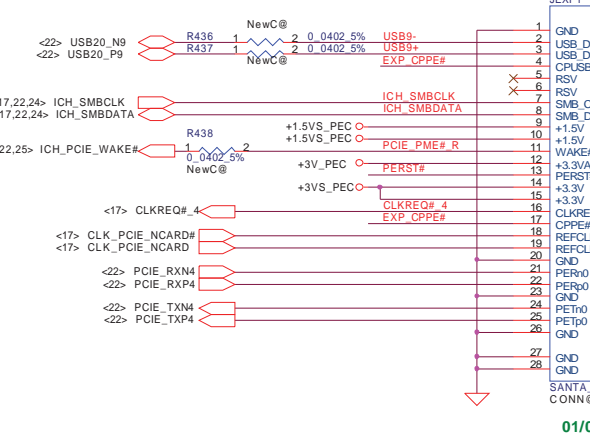
# Mini Card 2---WLAN



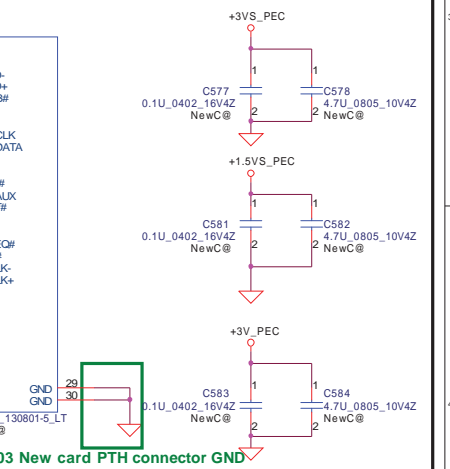
# New Card



# Close to JEXP



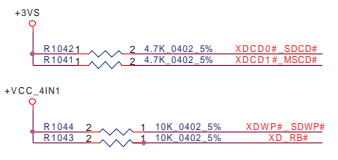
# Near to Express Card slot.



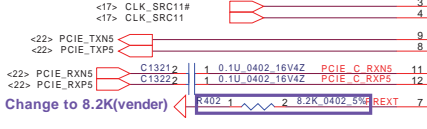
Security Classification	Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date
		2006/07/26

Title		<b>Compal Electronics, Inc.</b>	
		<b>WLAN, WWAN, New Card</b>	
Size	Document Number	Rev	
	Montevina Blade UMA LA4101P	0.3	

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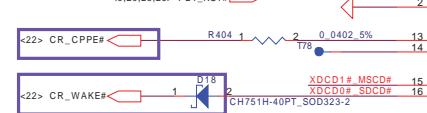


09/26 (JMicron) recommend width/length: 12mil / <250mil for PREXT signal (pin 7)



11/07 Change to 8.2K(vender)

09/26 (JMicron) recommend add a test point for pin 13 + 14

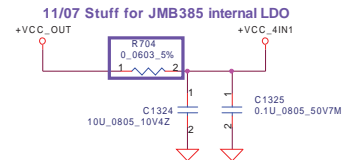
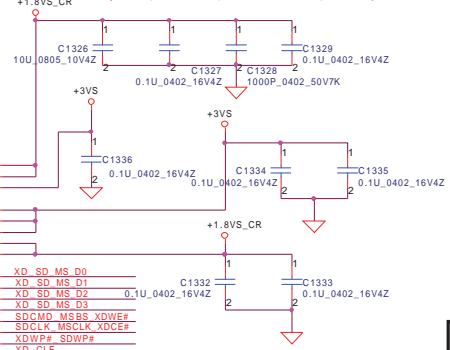


11/09 Add D18 for cardreader wake up

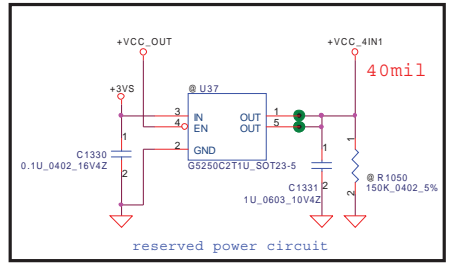
+vcc\_out use for PWR\_EN# 8mA sink current



09/26 (JMicron) recommend C1328/1000pF close to U36 pin5  
 09/26 (JMicron) recommend place C1329/0.1uF near by C1328  
 09/26 (JMicron) recommend (APVDD, 20 mil width, less than 120mil long)

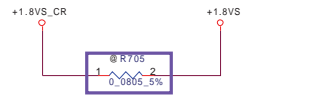


Use 0603 type and over 20 mils trace width on both side  
 09/26 (JMicron) recommend change to 0805 Size  
 09/26 (JMicron) recommend +VCC\_OUT >30mil



11/07 Change U37 correct PCBFootprint SOT23  
 11/07 BOM delete for JMB385 internal LDO

09/26 Must change P mos FET

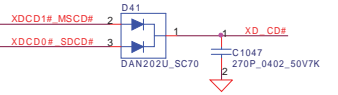
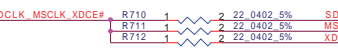
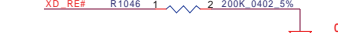


11/07 Don't stuff for JMB385 internal LDO

11/07 Change to 10K(vender)

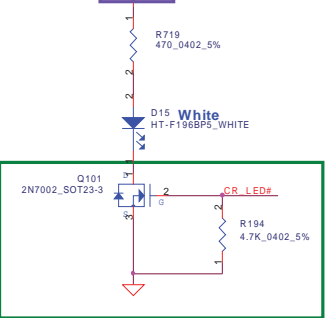


01/03 Change Cardreader LED control



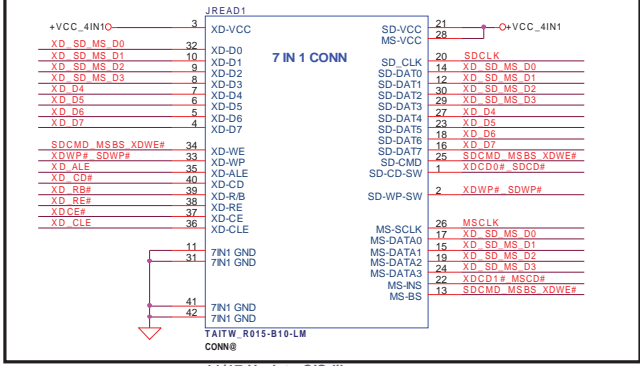
White LED: VF=3V, IF = 5mA, Res = 56ohm

11/09 don't support DIM function



01/03 Change Cardreader LED control

### Card Reader Connector

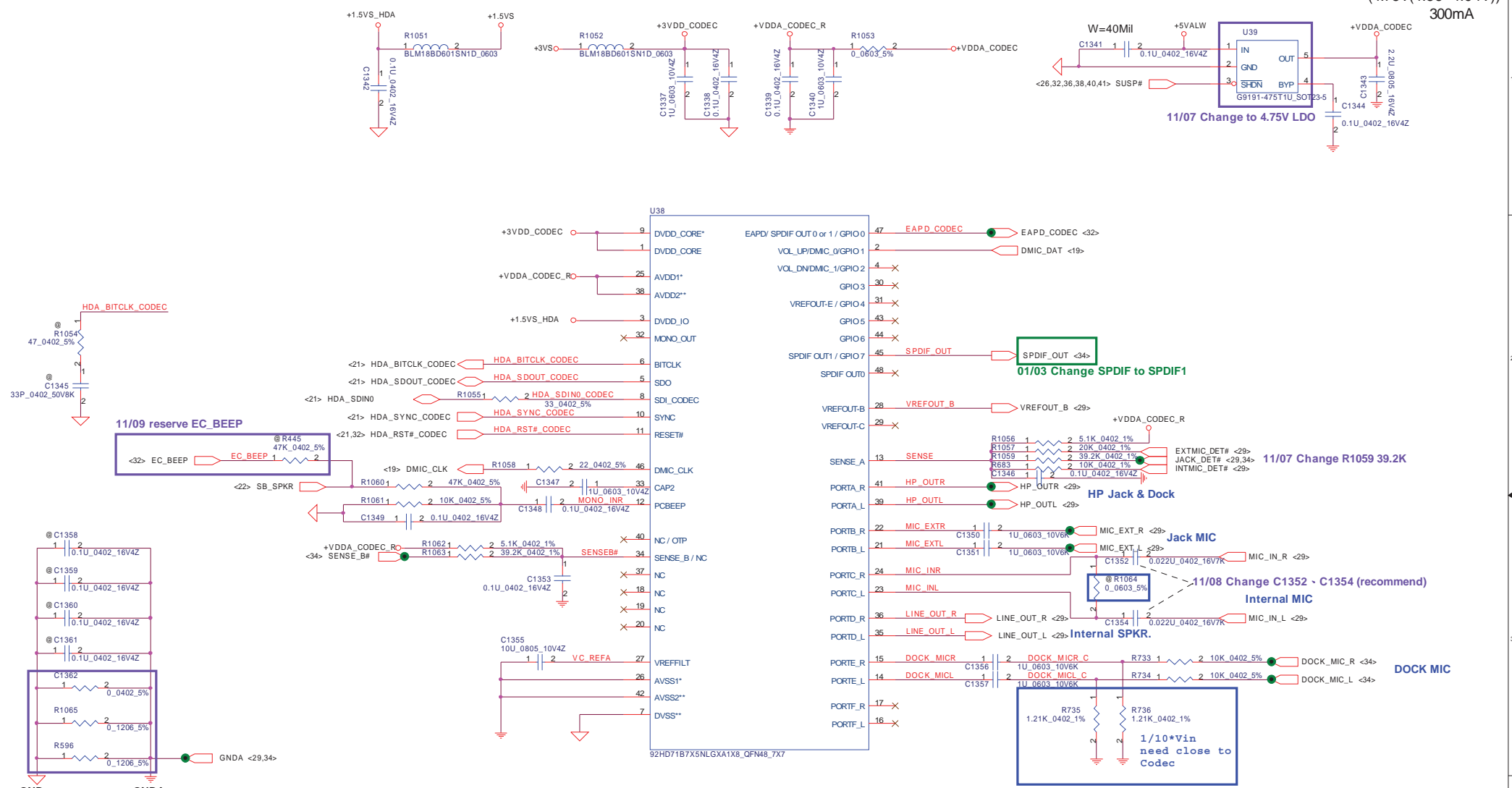


11/17 Update CIS library

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Issued Date	2007/08/28	Deciphered Date	2006/10/06	USB CardReader&CONN	
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Date	Saturday, January 05, 2008	Sheet	27	of 48	

# CODEC POWER

(4.75V(4.56~4.94V))  
300mA

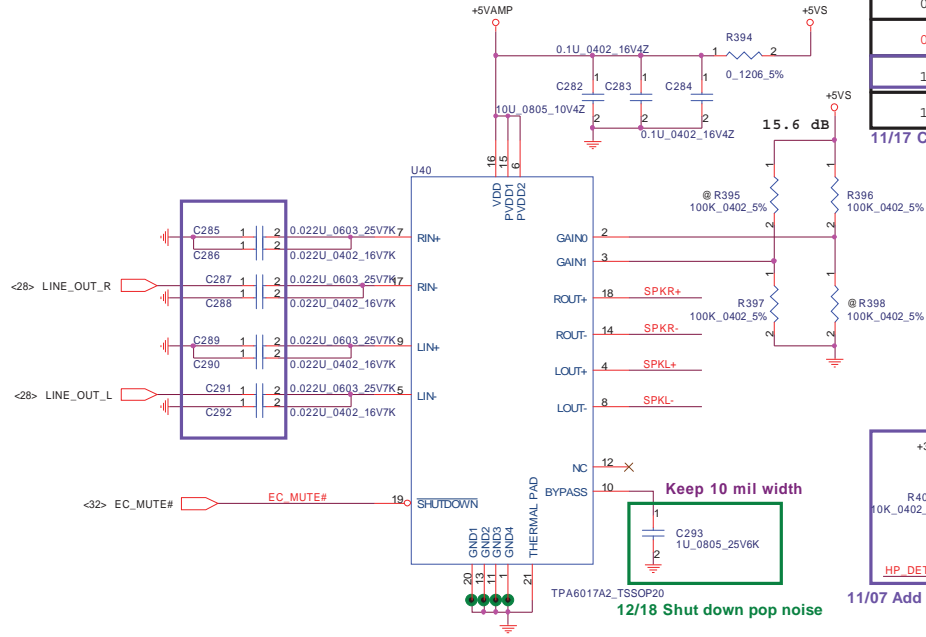


11/07 Stuff 0 Ohm for AGND and GND

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

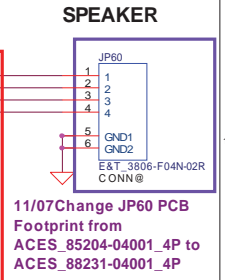
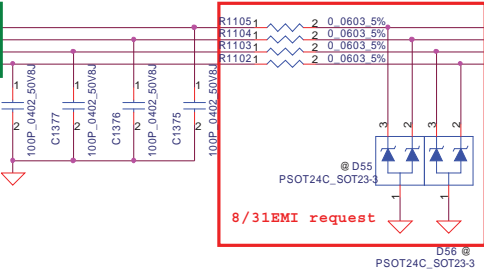
Security Classification	Compal Secret Data			Title	Codec_IDT9271B7		
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Size	Document Number	Rev	
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				Date:	Saturday, January 05, 2008	Sheet	28 of 46

<http://laptop-motherboard-schematic.blogspot.com/>



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

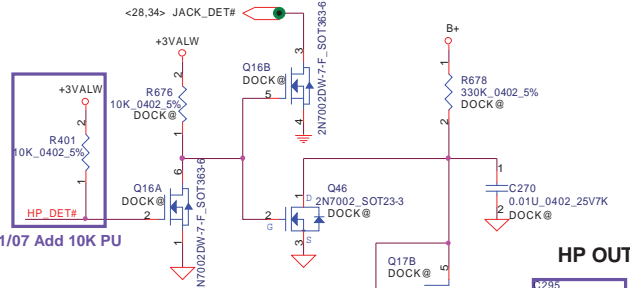
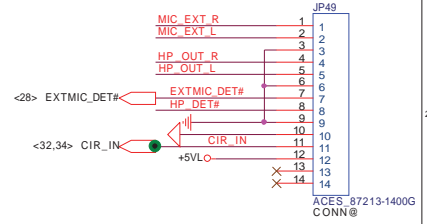
SPKR+  
SPKR-  
SPKL+  
SPKL-



11/07 Change JP60 PCB Footprint from ACES\_85204-04001\_4P to ACES\_88231-04001\_4P

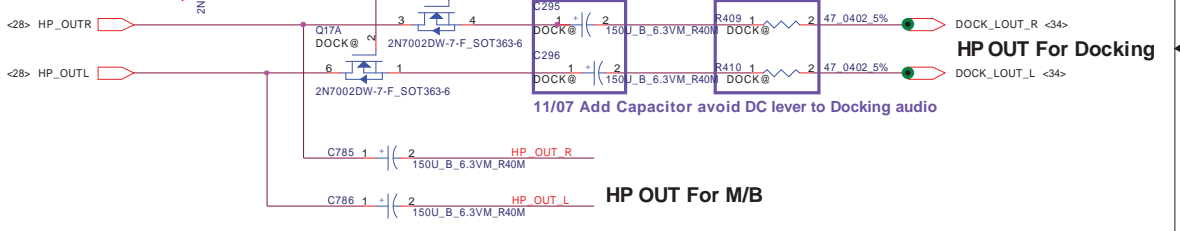
8/31EMI request

Audio/B & CIR



11/07 Add 10K PU

HP OUT

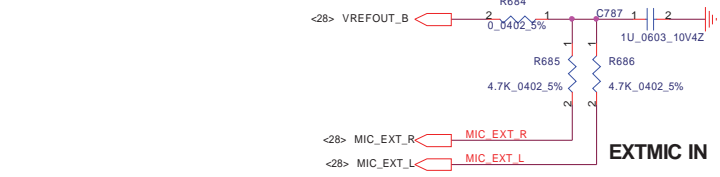
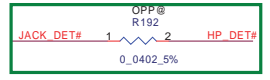


11/07 Add Capacitor avoid DC lever to Docking audio

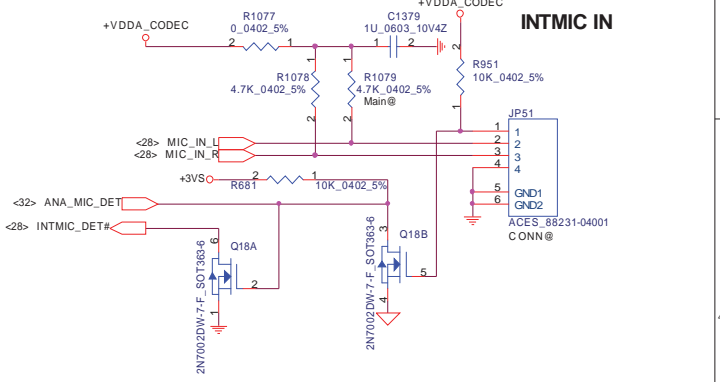
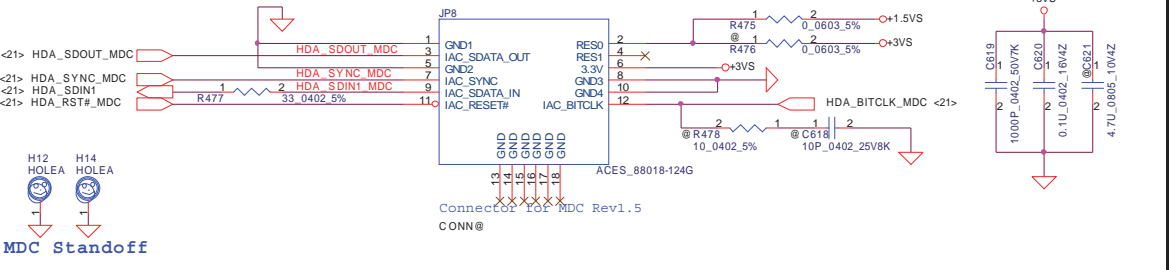
HP OUT For Docking

DOCK\_LOUT\_R <34>  
DOCK\_LOUT\_L <34>

HP OUT For M/B

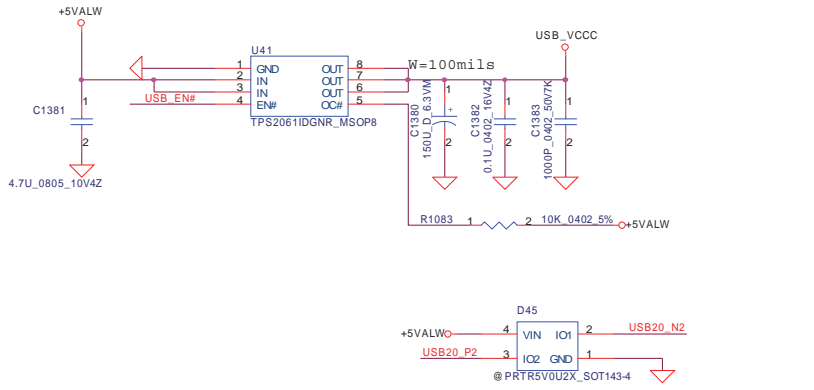


MDC 1.5 Conn.

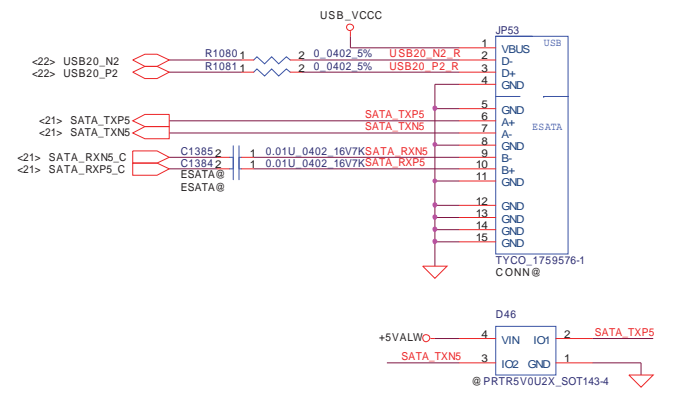


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			Custom
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			Rev 0.3
			Date: Saturday, January 05, 2008
			Sheet 29 of 46

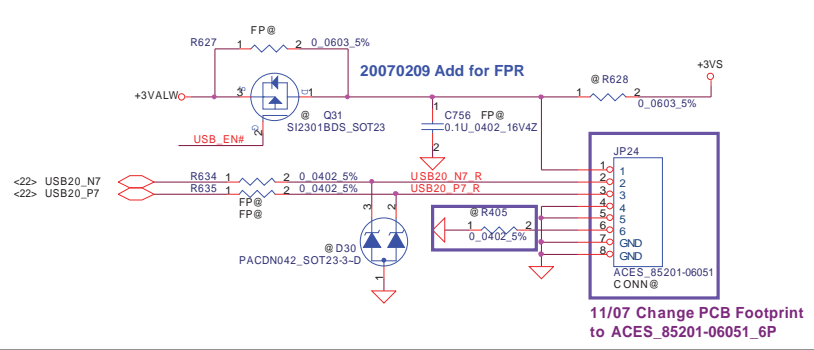
### Left side USB Connector



### Left side ESATA/USB combination Connector

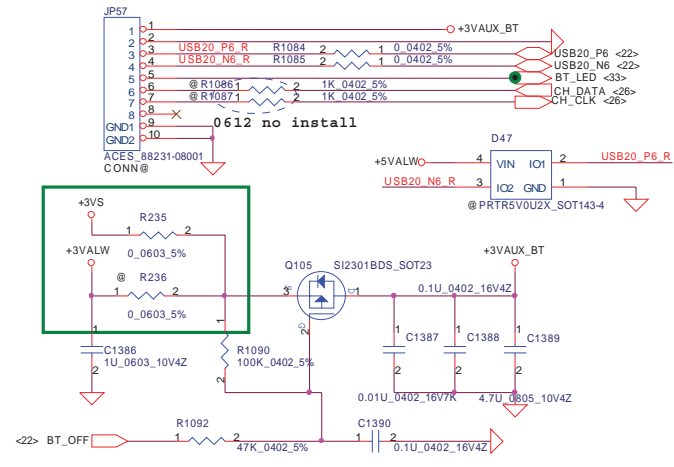


### Finger printer

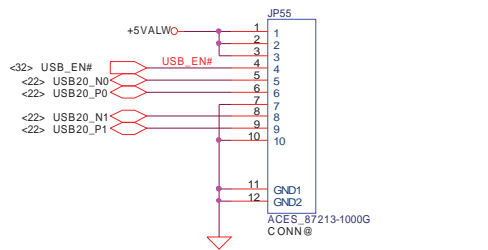


### BT Connector

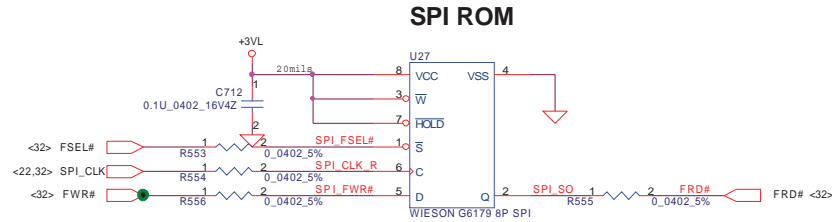
Need change to New version



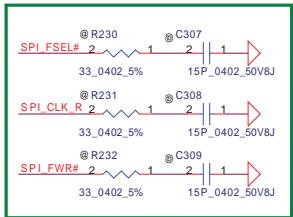
### USB cable connector for Right side



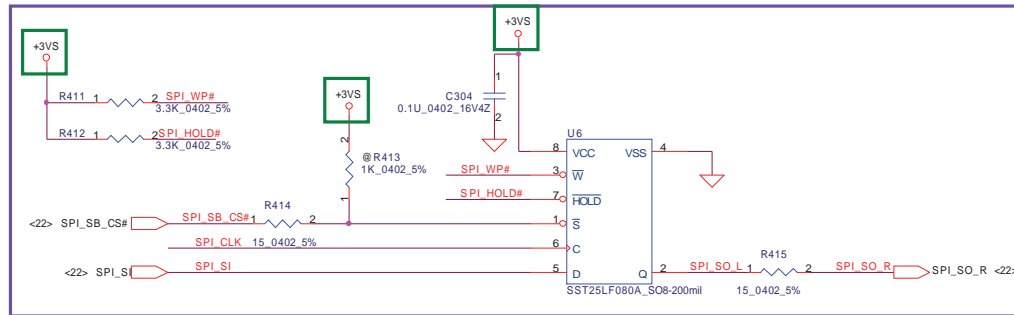
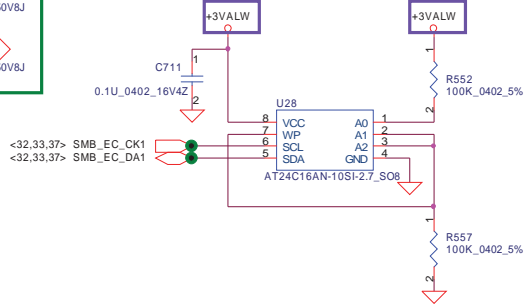
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Size	Document Number	Rev		
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Date:	Saturday, January 05, 2008	Sheet	30	of 46



SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH  
WIESO\_G6179-100000\_8P



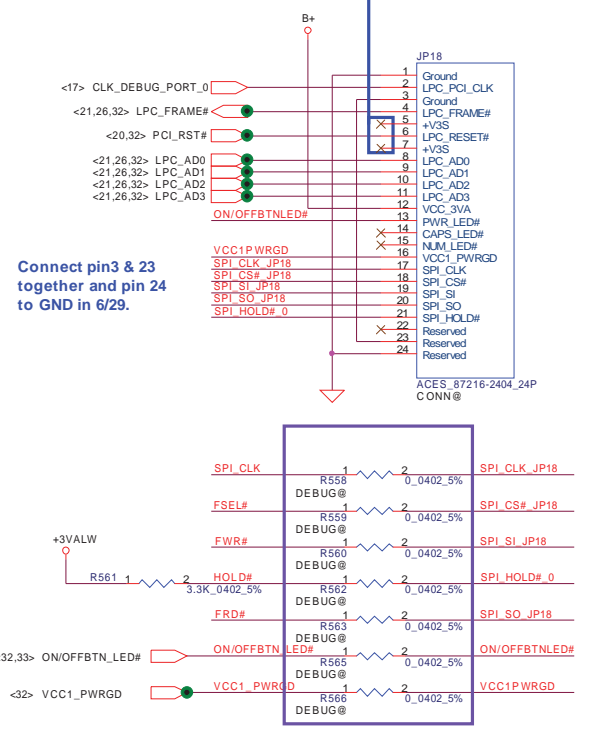
11/16 Change TO +3VALW



11/17 Add SB HDPC ROM  
01/03 Change HDPC ROM to +3VS

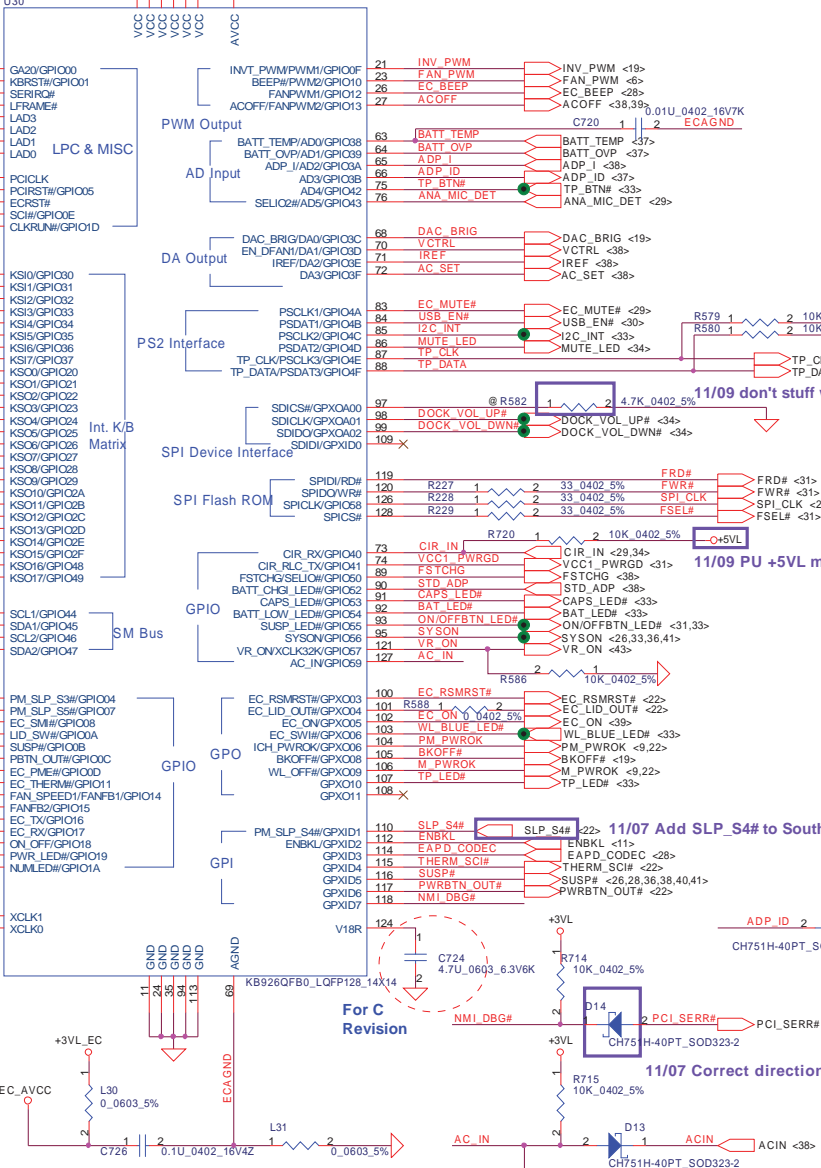
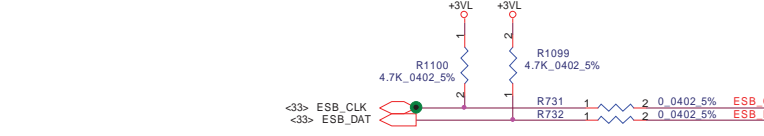
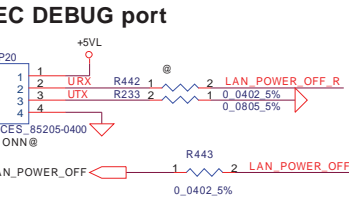
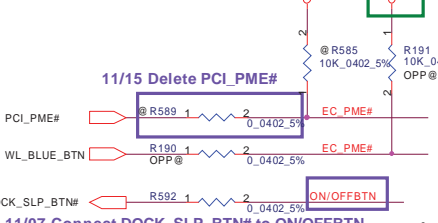
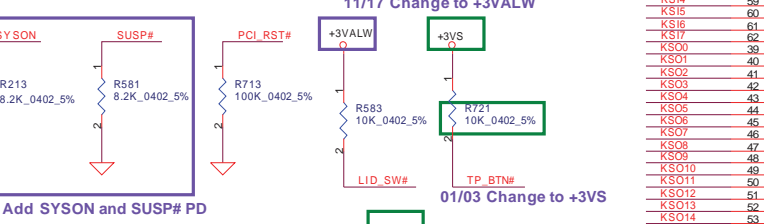
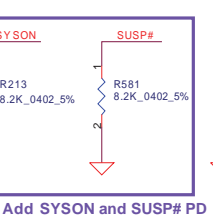
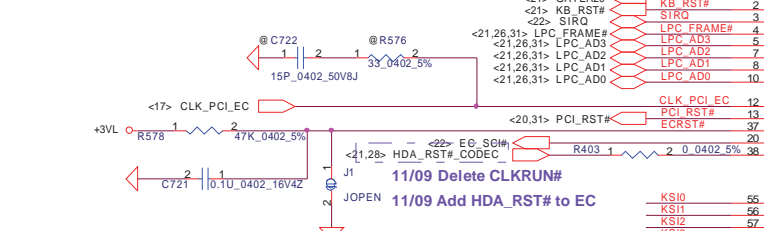
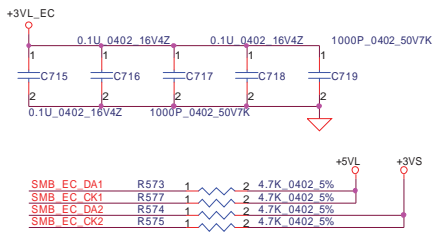
**LPC Debug Port**

Change from +3VL to +3VS. 6/9  
Removed +3VS. 6/13



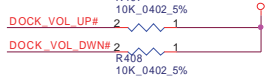
Connect pin3 & 23  
together and pin 24  
to GND in 6/29.

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Size	Document Number	Date		Rev		
	Montevina Blade UMA LA4101P	Saturday, January 05, 2008		Sheet 31 of 46		0.3



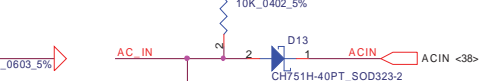
**For EMI**

KSO15 @ C792	1	2	100P_0402_50V8J
KSO10 @ C793	1	2	100P_0402_50V8J
KSO11 @ C794	1	2	100P_0402_50V8J
KSO14 @ C795	1	2	100P_0402_50V8J
KSO13 @ C796	1	2	100P_0402_50V8J
KSO12 @ C797	1	2	100P_0402_50V8J
KSO3 @ C798	1	2	100P_0402_50V8J
KSO6 @ C799	1	2	100P_0402_50V8J
KSO8 @ C800	1	2	100P_0402_50V8J
KSO7 @ C801	1	2	100P_0402_50V8J
KSO4 @ C802	1	2	100P_0402_50V8J
KSO2 @ C803	1	2	100P_0402_50V8J
KS10 @ C804	1	2	100P_0402_50V8J
KSO1 @ C805	1	2	100P_0402_50V8J
KSO5 @ C806	1	2	100P_0402_50V8J
KS13 @ C807	1	2	100P_0402_50V8J
KS12 @ C808	1	2	100P_0402_50V8J
KSO0 @ C809	1	2	100P_0402_50V8J
KS15 @ C810	1	2	100P_0402_50V8J
KS14 @ C811	1	2	100P_0402_50V8J
KSO9 @ C812	1	2	100P_0402_50V8J
KS16 @ C813	1	2	100P_0402_50V8J
KS17 @ C814	1	2	100P_0402_50V8J
KS11 @ C815	1	2	100P_0402_50V8J



**14" INT\_KBD CONN.( TYPE "D" KB)**

KS015	1
KS010	2
KS011	3
KS014	4
KS013	5
KS03	6
KS06	7
KS08	8
KS07	9
KS04	10
KS02	11
KS10	12
KS012	13
KS05	14
KS15	15
KS12	16
KS00	17
KS15	18
KS14	19
KS09	20
KS16	21
KS17	22
KS11	23
KS11	24

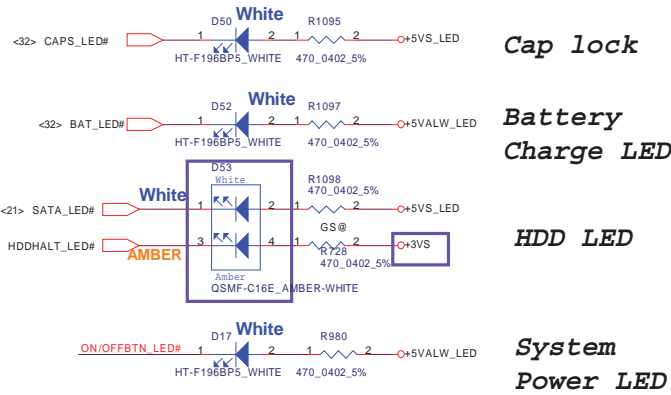


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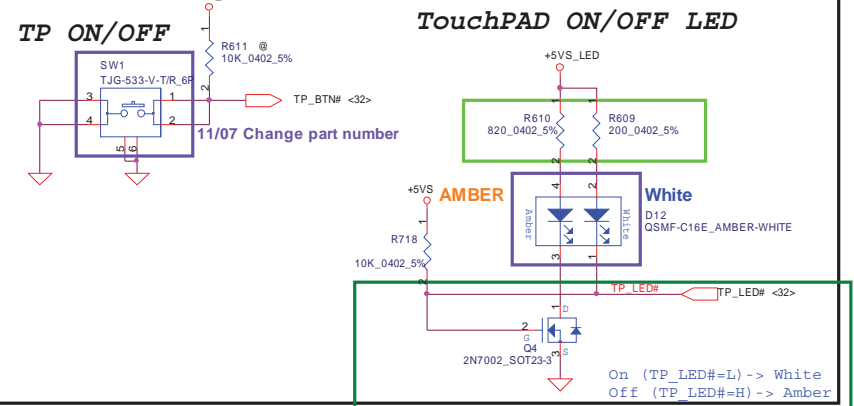
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EC KB926/KB Conn.	
Title	Montevina Blade UMA LA4101P
Size	Document Number
Rev	0.3



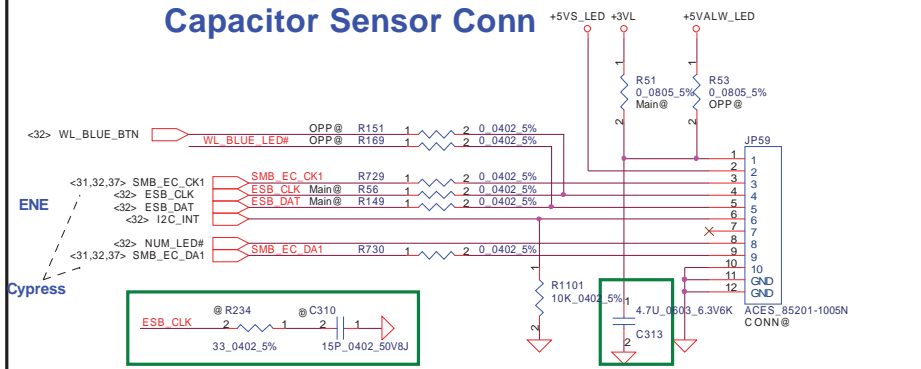
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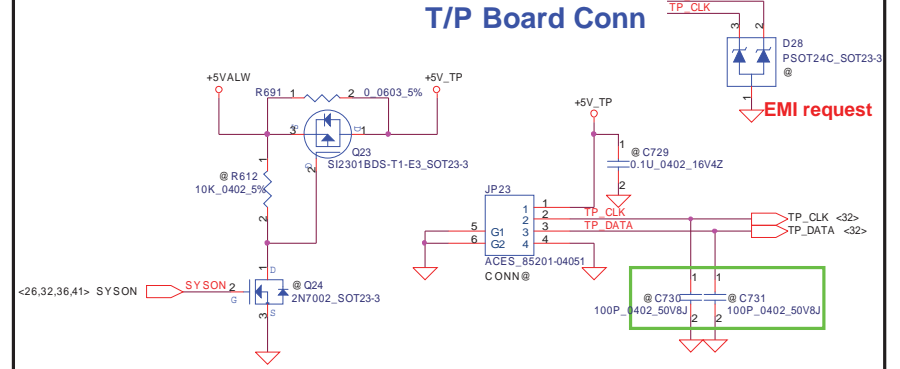
### T/P Board (Include T/P\_ON/OFF)



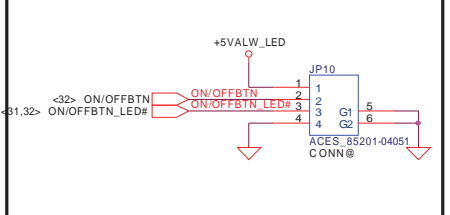
### Capacitor Sensor Conn



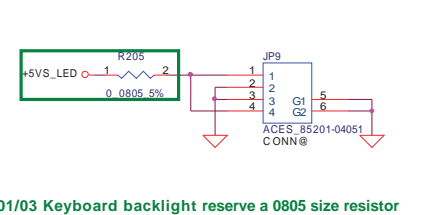
### T/P Board Conn



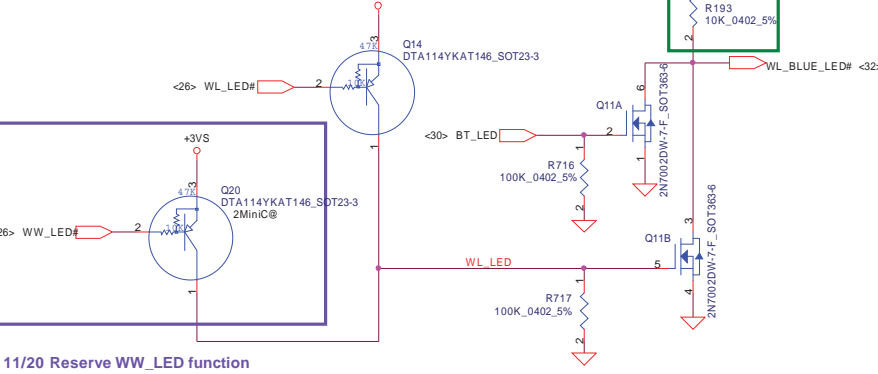
### ON/OFF Button Connector



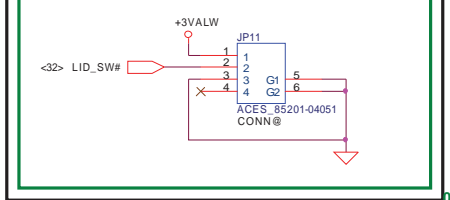
### Keyboard backlight Conn



### Mini card LED



### Lid Switch Connector

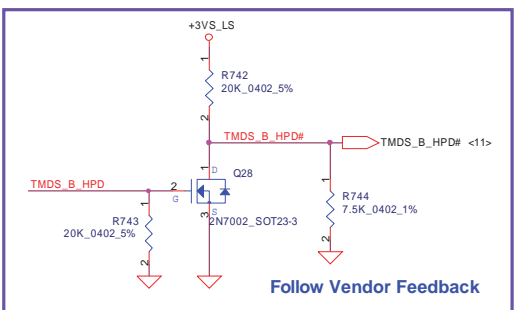


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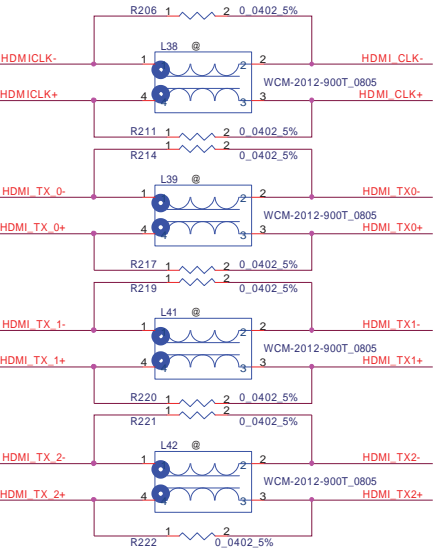
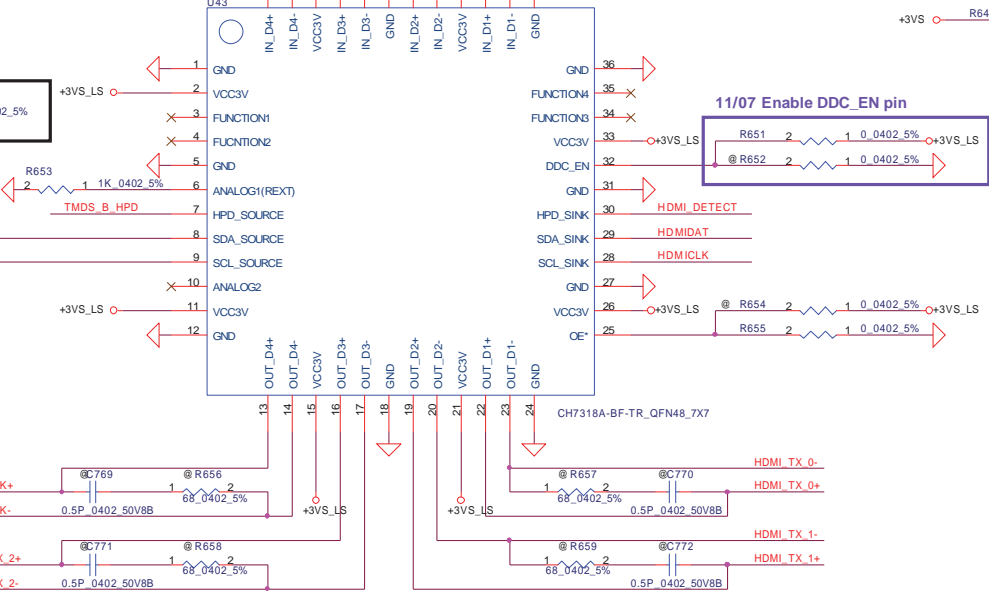
**Follow Intel Feedback putting 2.2K ohm**



11/07 correct TMDS\_B\_HPD# connection to North bridge

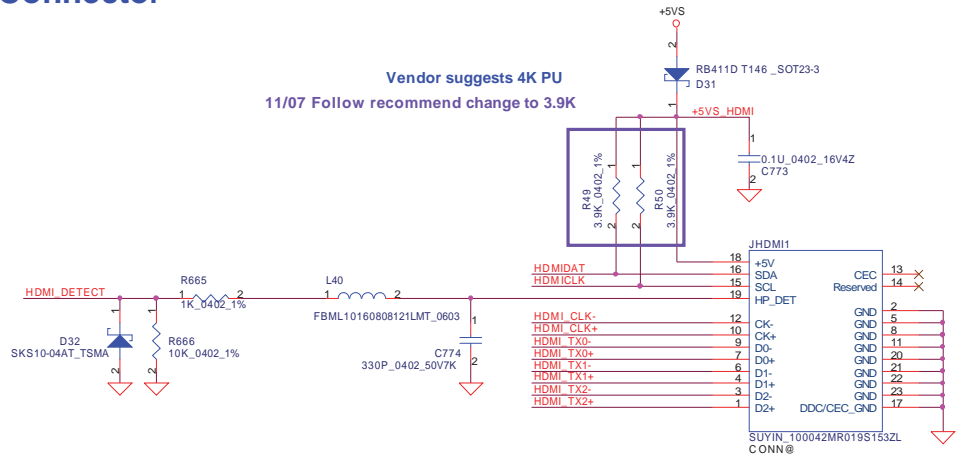
**Follow Vendor Feedback**

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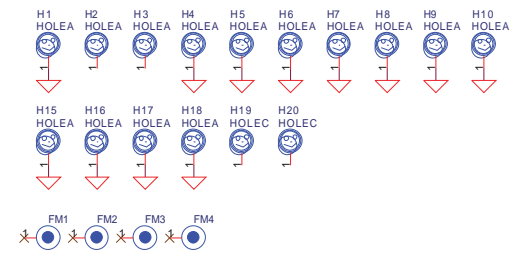
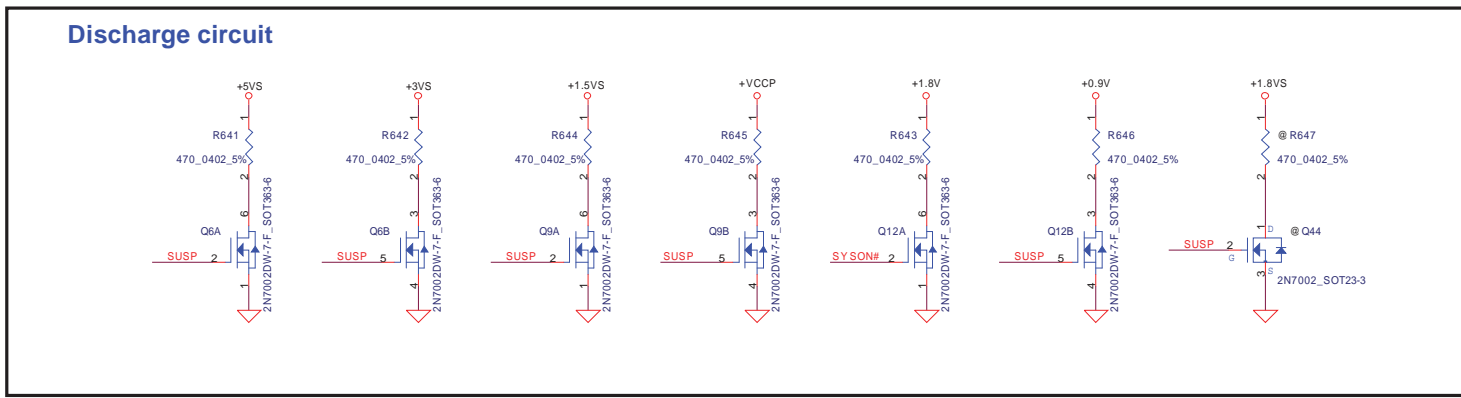
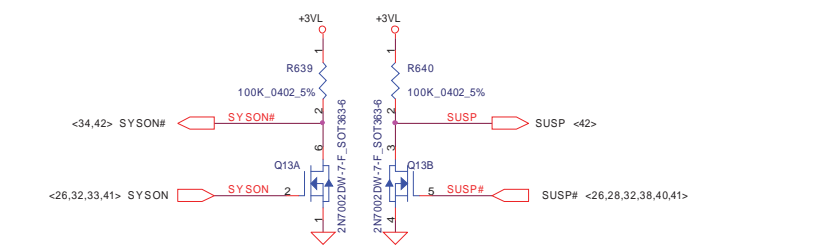
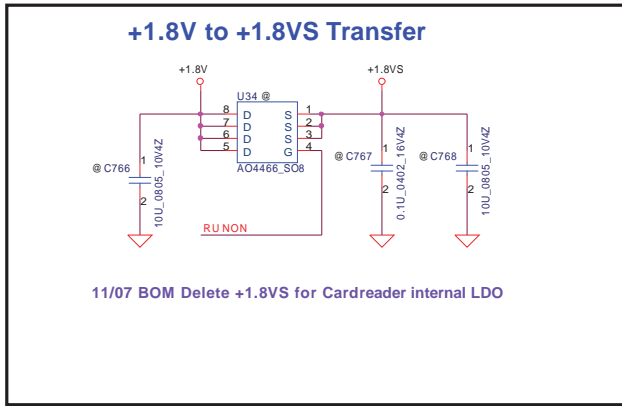
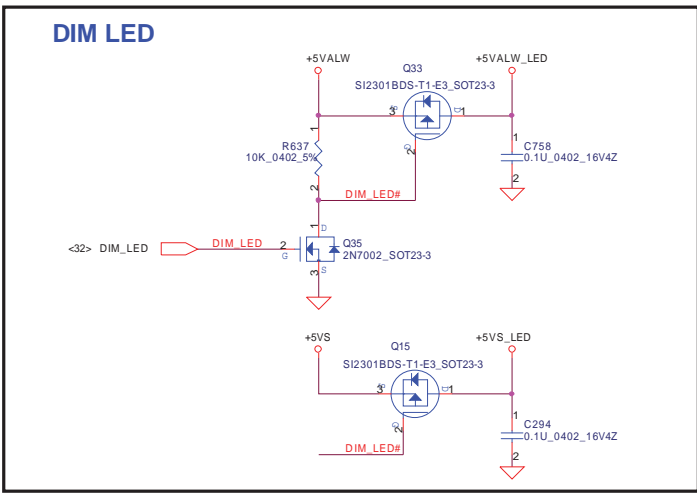
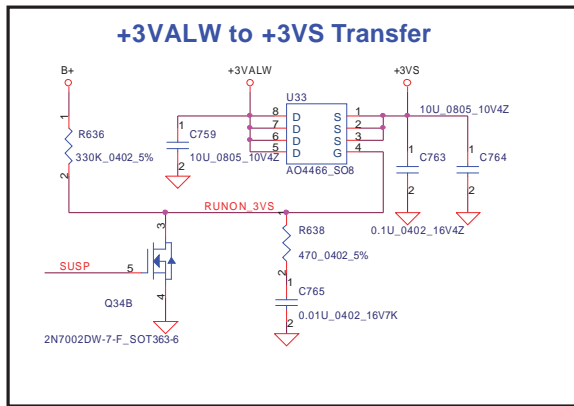
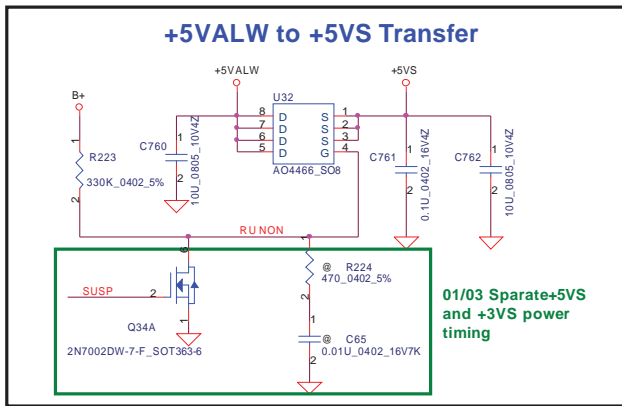


01/03 Reserver 0 ohm co lay with common choke

### HDMI Connector

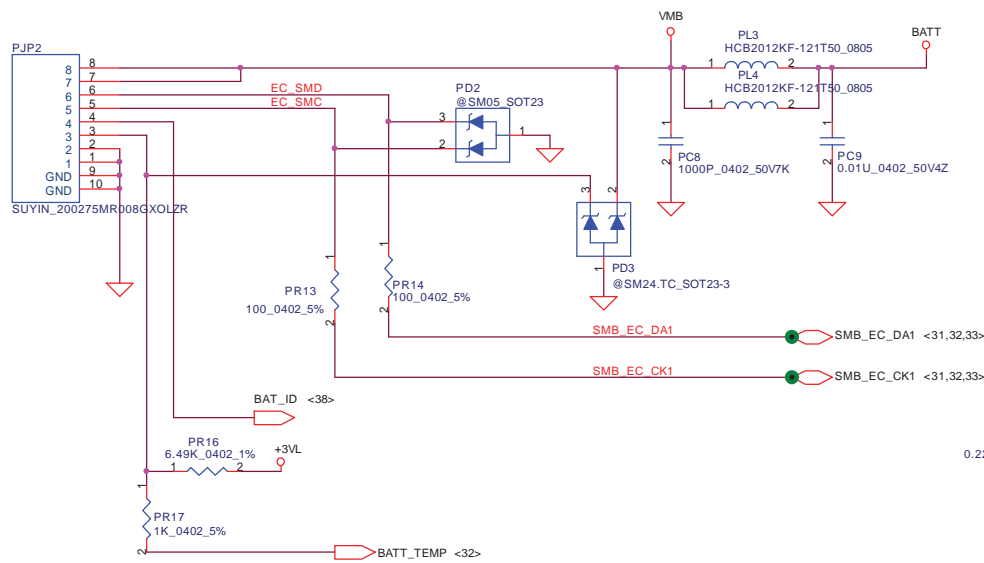
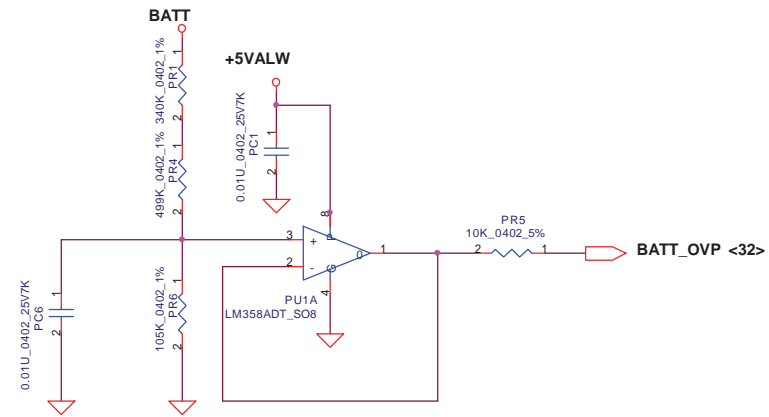
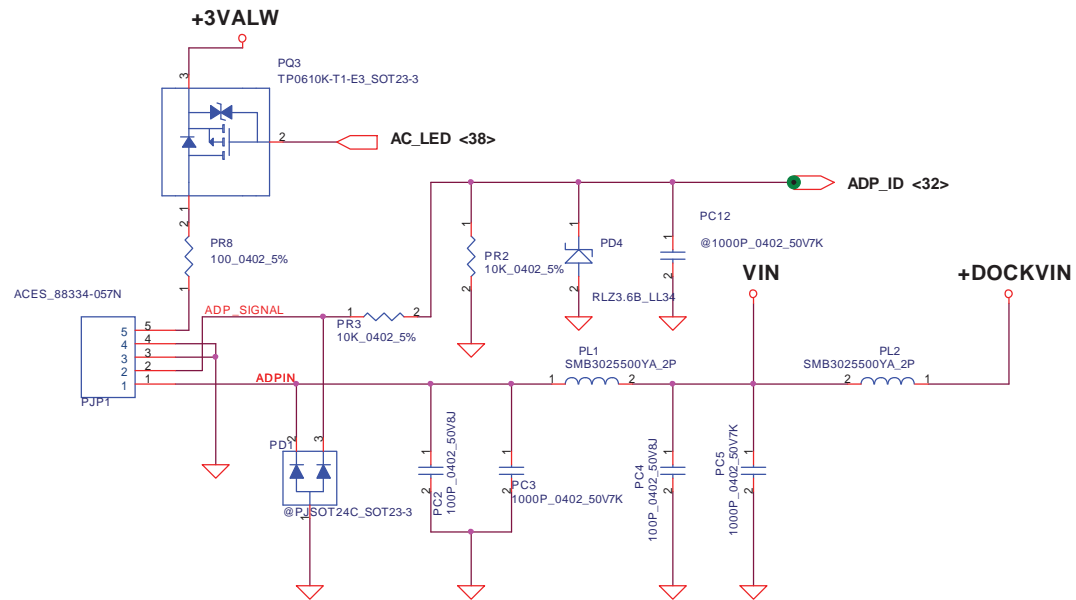


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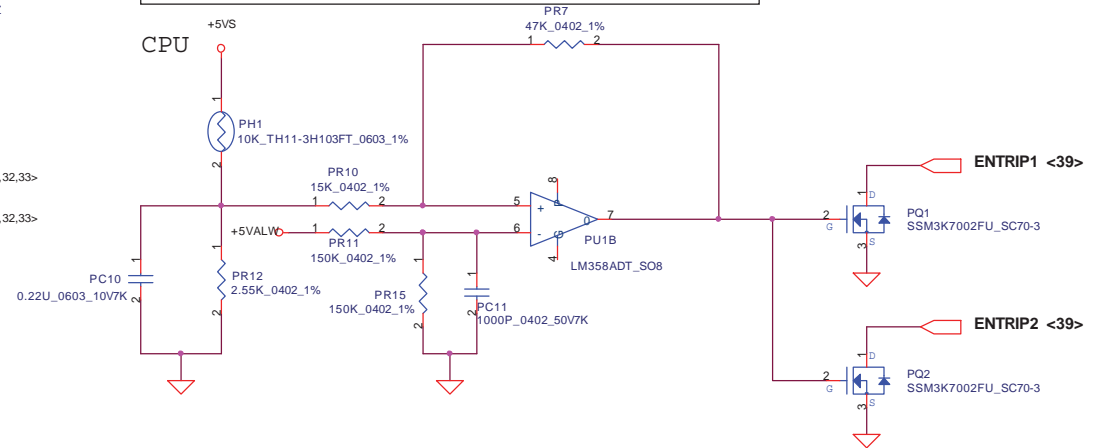


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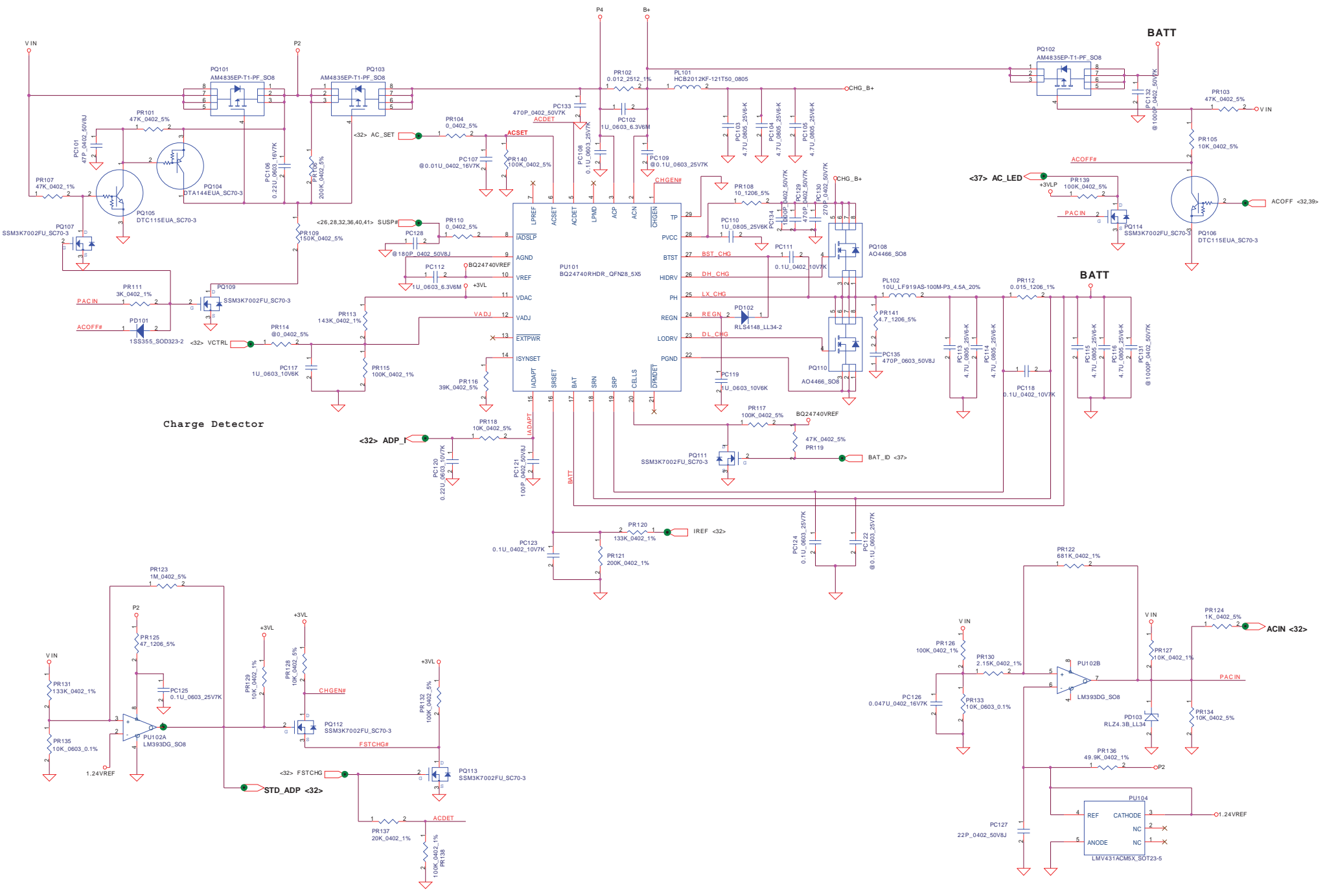


PH1 under CPU bottom side :  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 47 +-3 degree C



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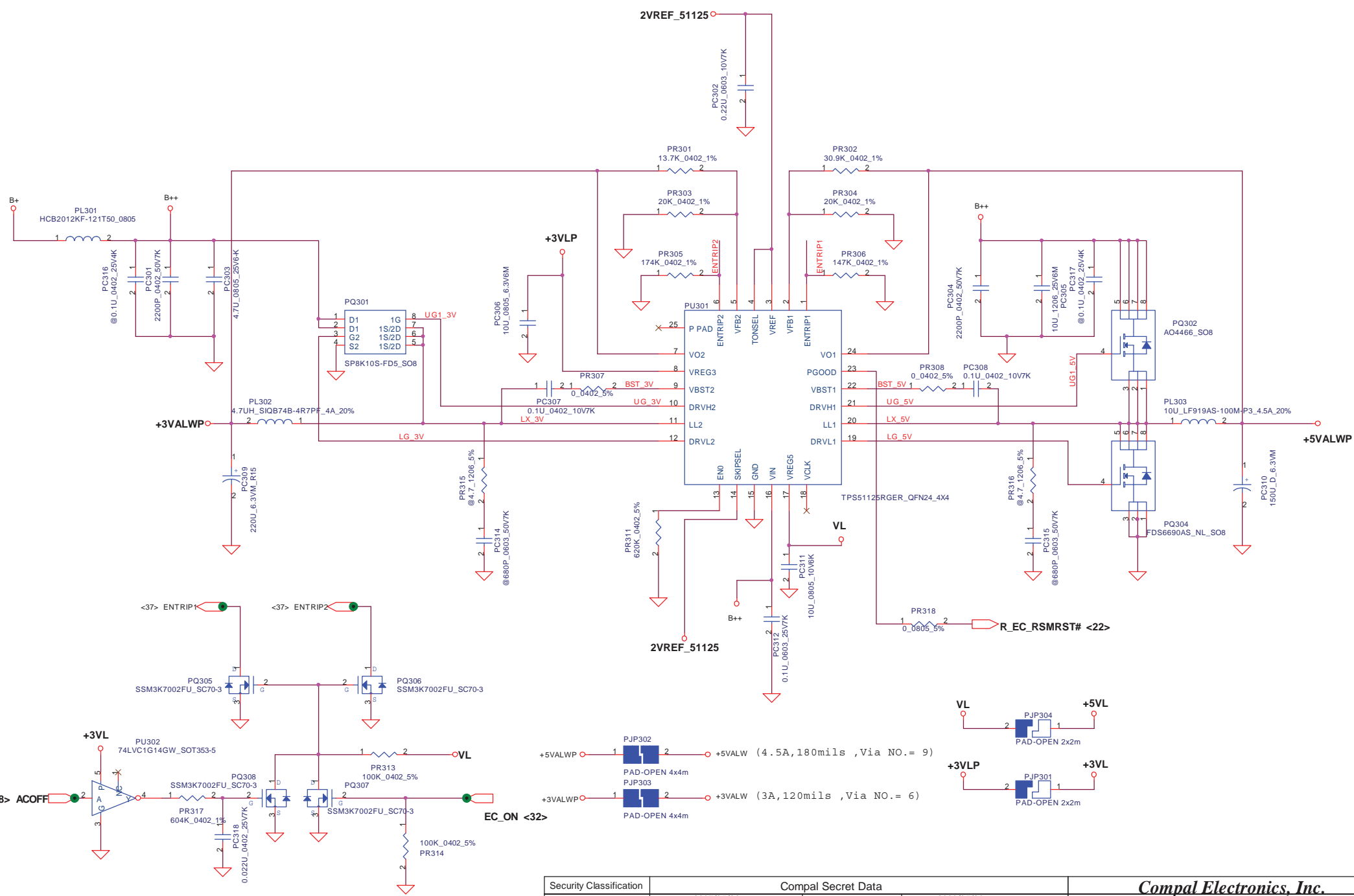
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Charge Detector

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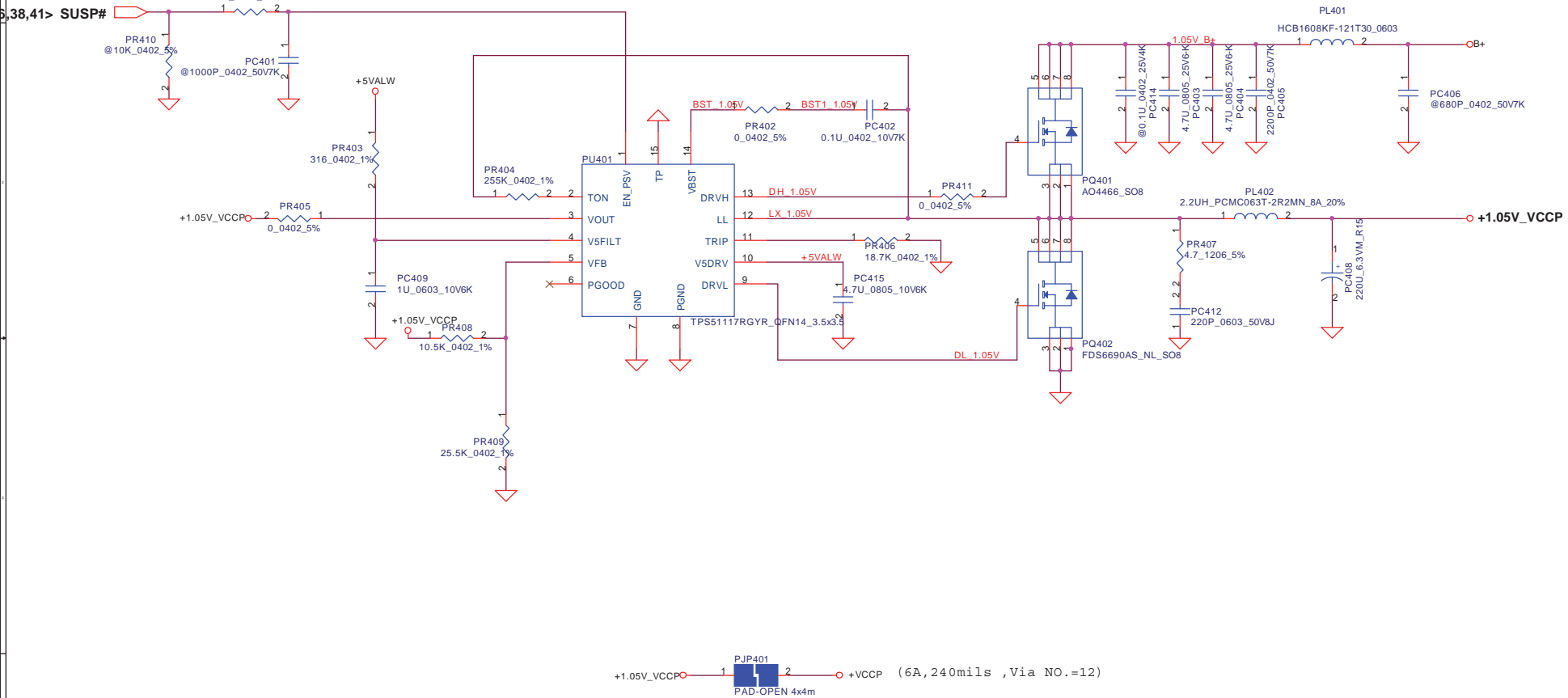
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<b>3.3VALWP/5VALWP</b>		
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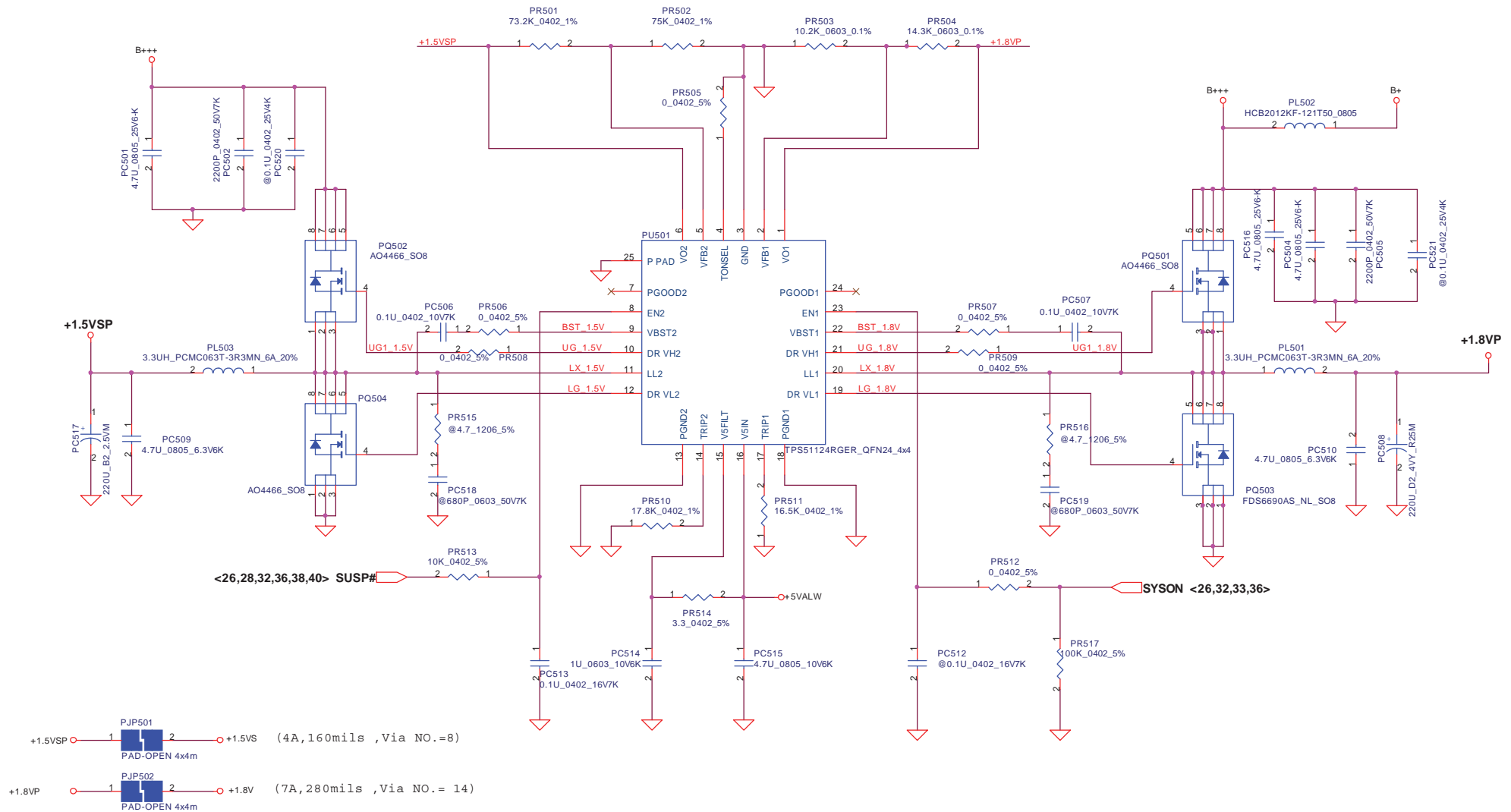
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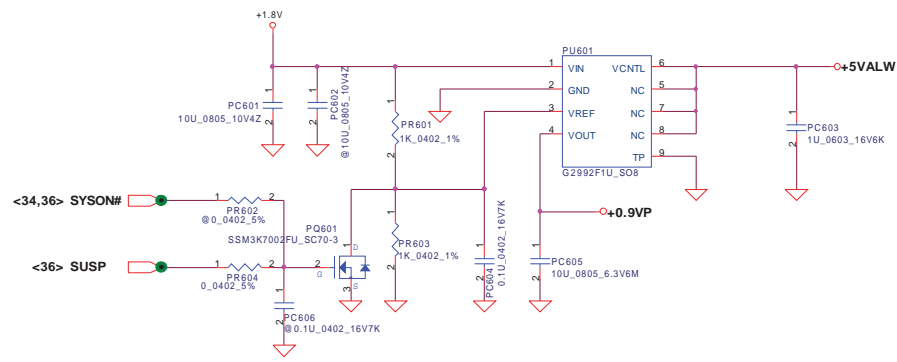




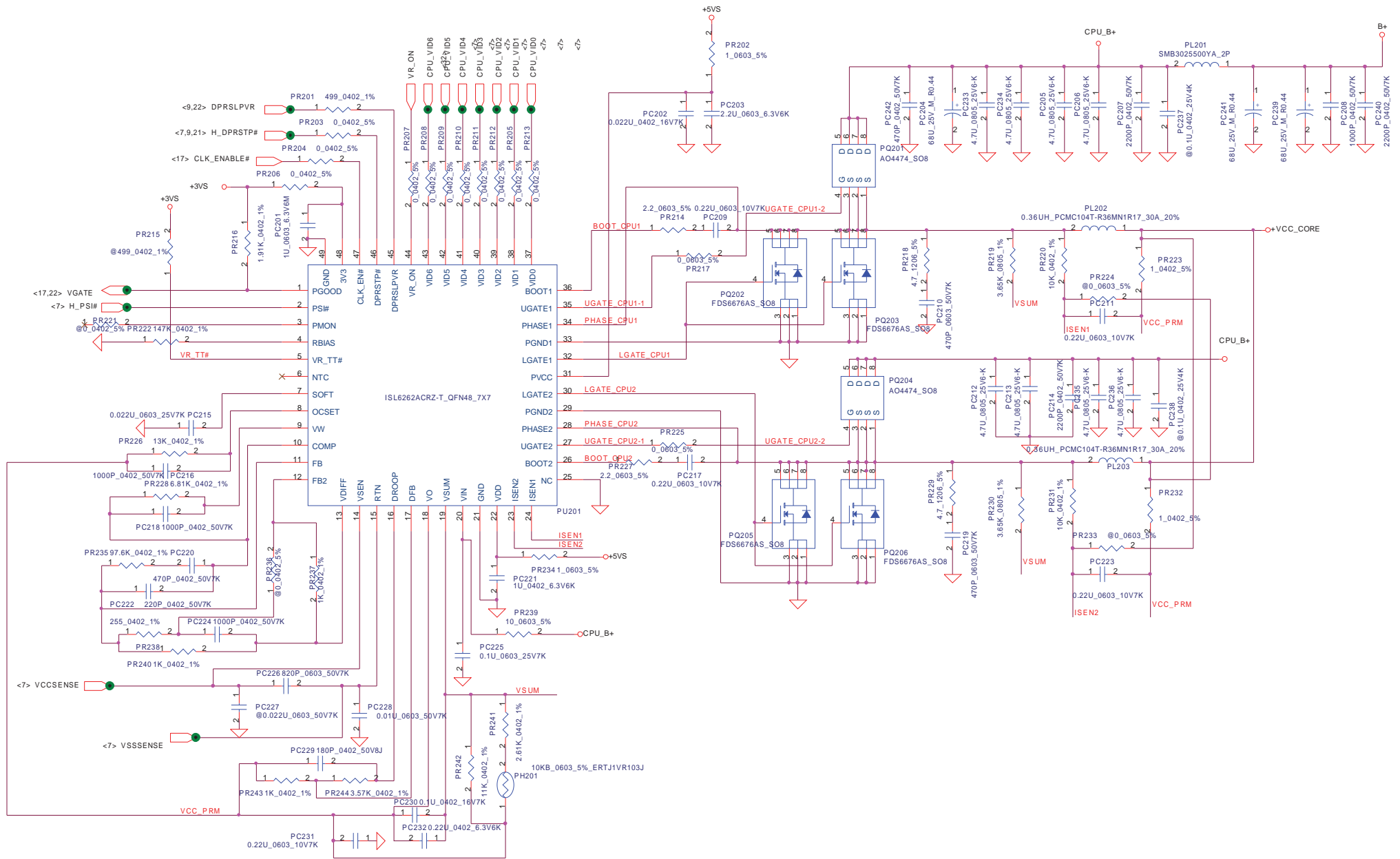
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Title		
1.5VSP/1.8VP		
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<b>+CPU_CORE</b>			
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K、R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#、GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285-C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295、BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction prectect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC_EN must enable、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOOUT and HDA_SDOOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
39					
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# Version Change List ( P. I. R. List ) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
10							
11							
12							
13							
14							

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