

AT3 BLOCK DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

04-- 0402 footprint
 06-- 0603 footprint
 08-- 0805 footprint
 12-- 1206 footprint
 F-- 1% tolerance

CPU Merom
 478P (uPGA)/35W
 PAG 3, 4

CPU THERMAL SENSOR
 PAG 5

CLOCK GEN
 ICS9LPRS355AGLFT
 64pinsTSSOP
 PAG 2

NORTH BRIDGE
 Crestline
 PAG 7, 8, 9, 10, 11, 12

NVIDIA G3-64 for 15.4"
NVIDIA G3-128 for 17"
 820p FCBGA
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HDMI CON
 Option for 17" only
 PAG 26

DDRII-SODIMM1
 DDRII 533,667 MHz
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DDRII-SODIMM2
 DDRII 533,667 MHz
 PAG 13, 14

Cable Docking
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 VGA
 RJ-45
 CIR/Pwr btn
 SPDIF Out
 Stereo MIC
 Headphone Jack
 USB Port
 VOL Cntr
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SYSTEM CHARGER(MAX8724)
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SYSTEM POWER MAX8778
 PAG 42

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CPU CORE MAX8771
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 ICH-8M
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 Mini PCI-E Card x1
 Express Card x1
 Cable Docking x1

PCI BUS / 33MHz
 PCI-E
 Azalia

Keyboard
 Touch Pad
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CIR
 PAG 36

Capacitive Sense SW
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FAN
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Flash
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SPI
 PAG 37

Two-element microphone
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Audio Jacks (Phone/ MIC)
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LAN
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 PCIE-LAN
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 RICOH 832
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IEEE1394
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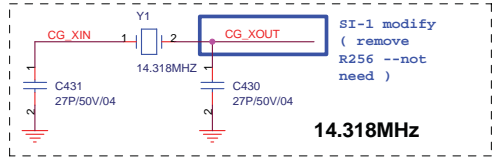
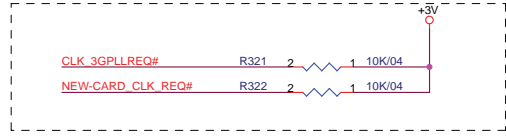
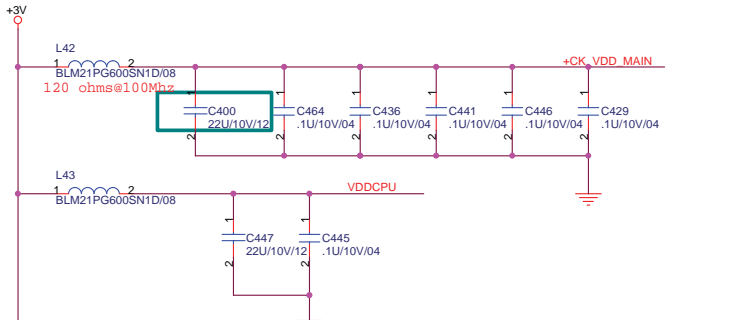
Memory
 CardReader
 PAG 27

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#, INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#, INTD#	MINI PCI for debug

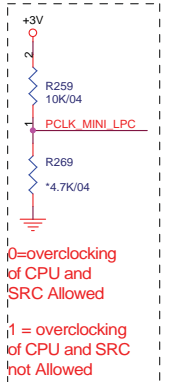
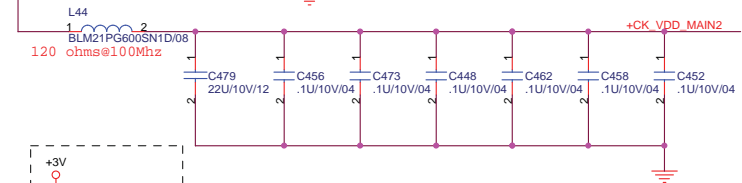


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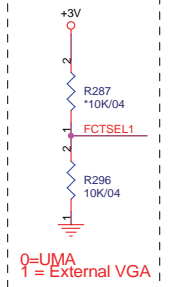
Size Custom	Document Number BLOCK DIAGRAM	Rev 1A
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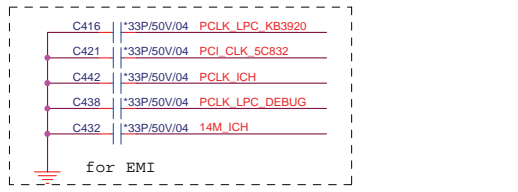
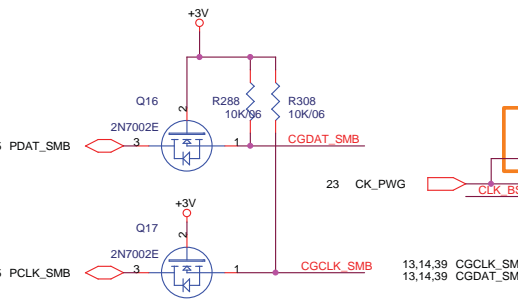
internal have already build-in 33ohm damping resistor



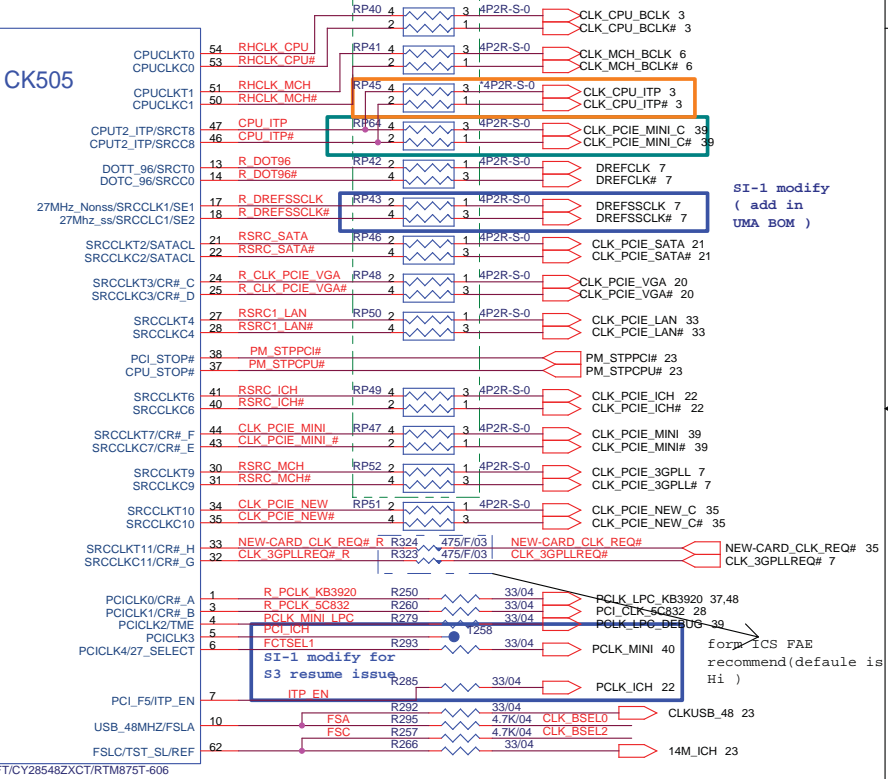
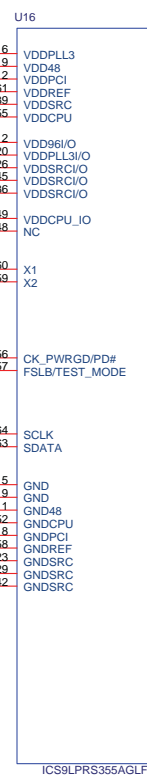
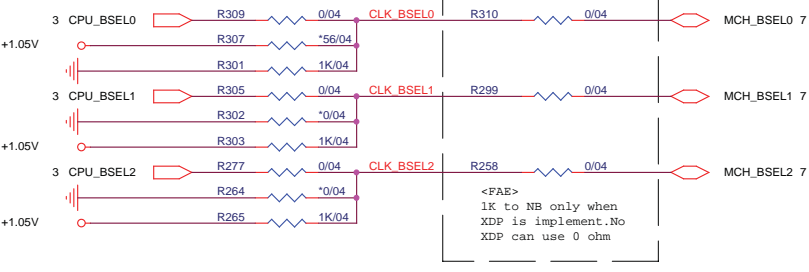
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



0=UMA
1 = External VGA



CPU Clock select



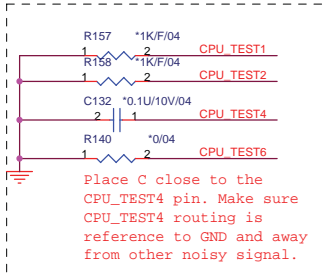
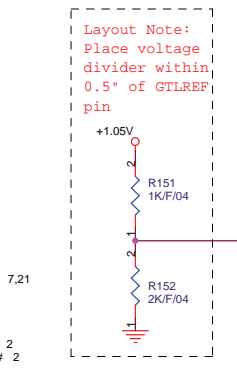
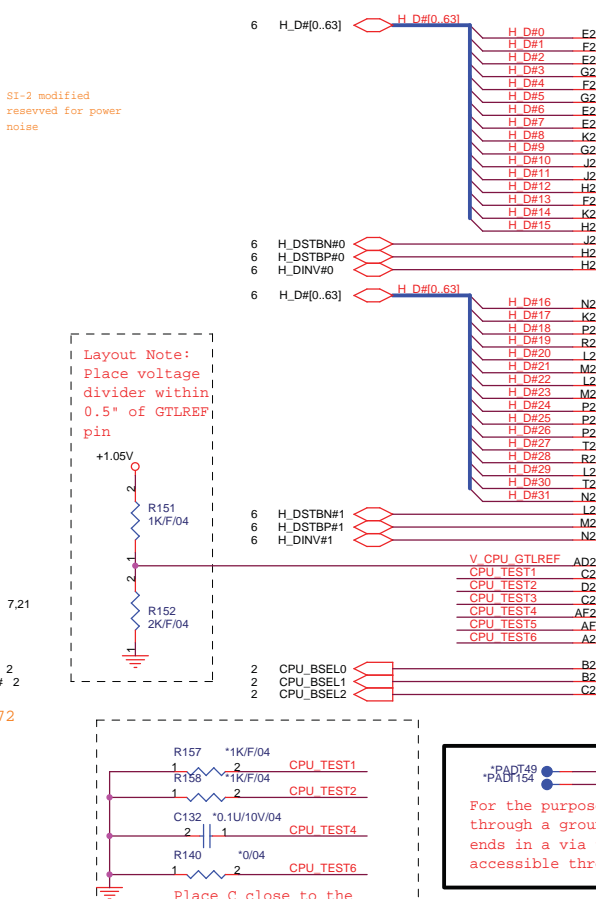
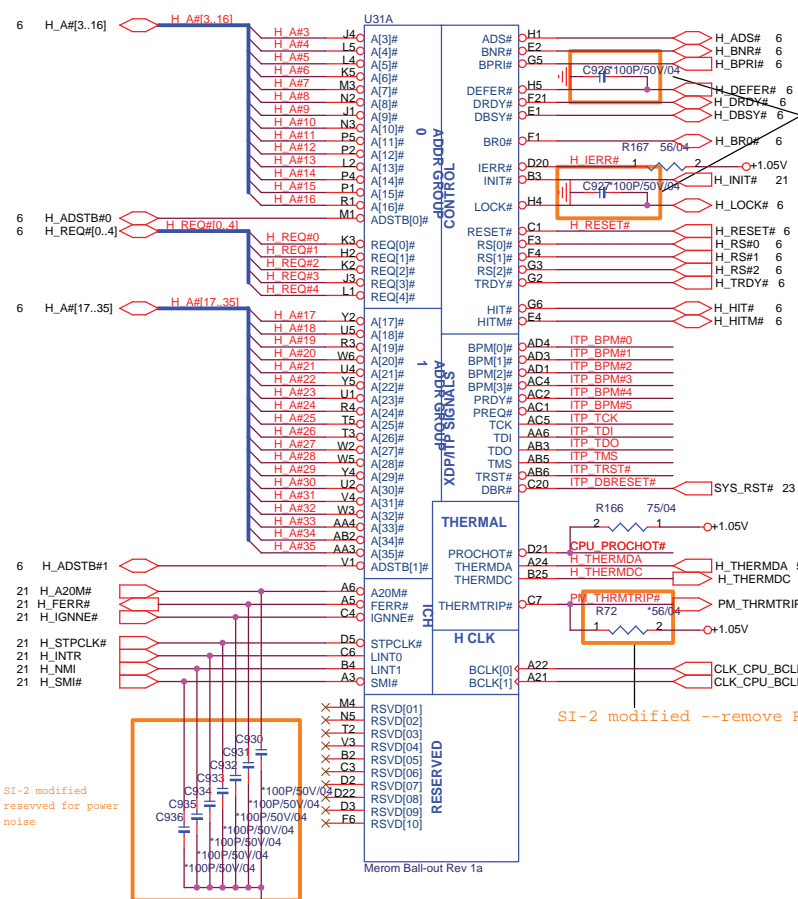
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GLCK_SEL = FCTSEL1

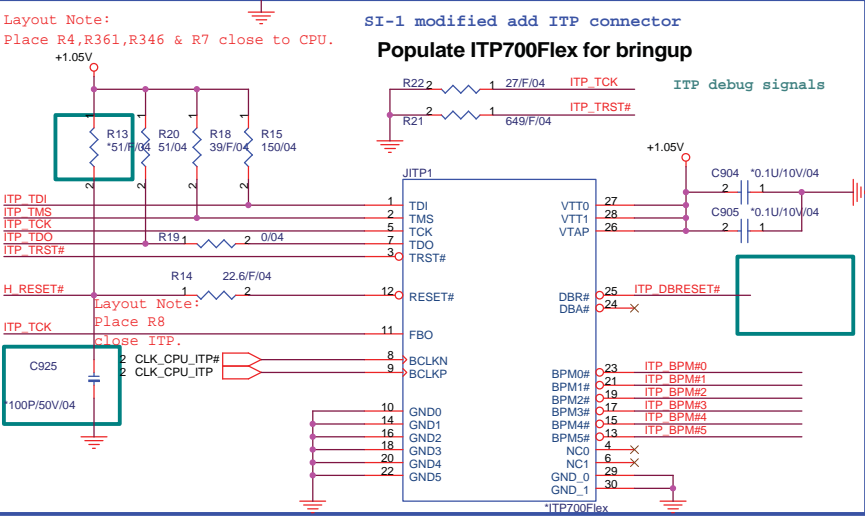
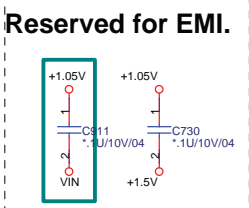
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



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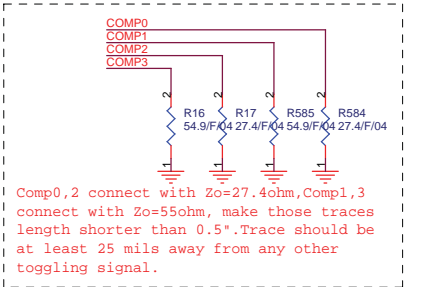
For the purpose of testability, route these signals through a ground referenced Z0 = 50ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

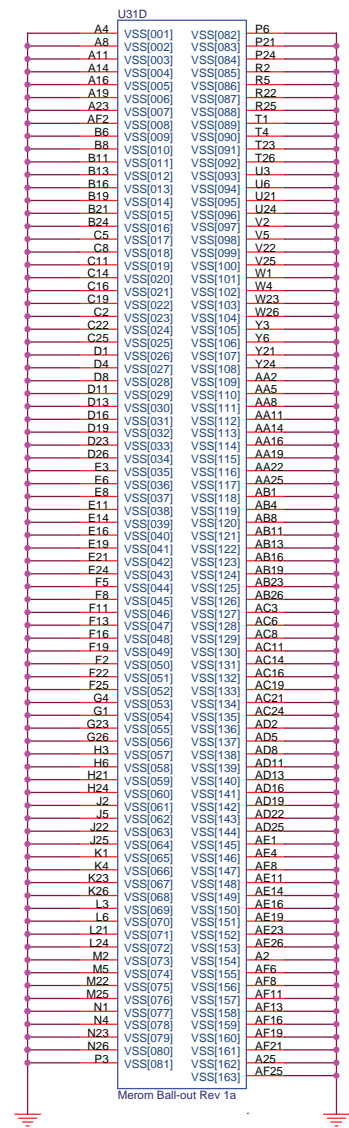
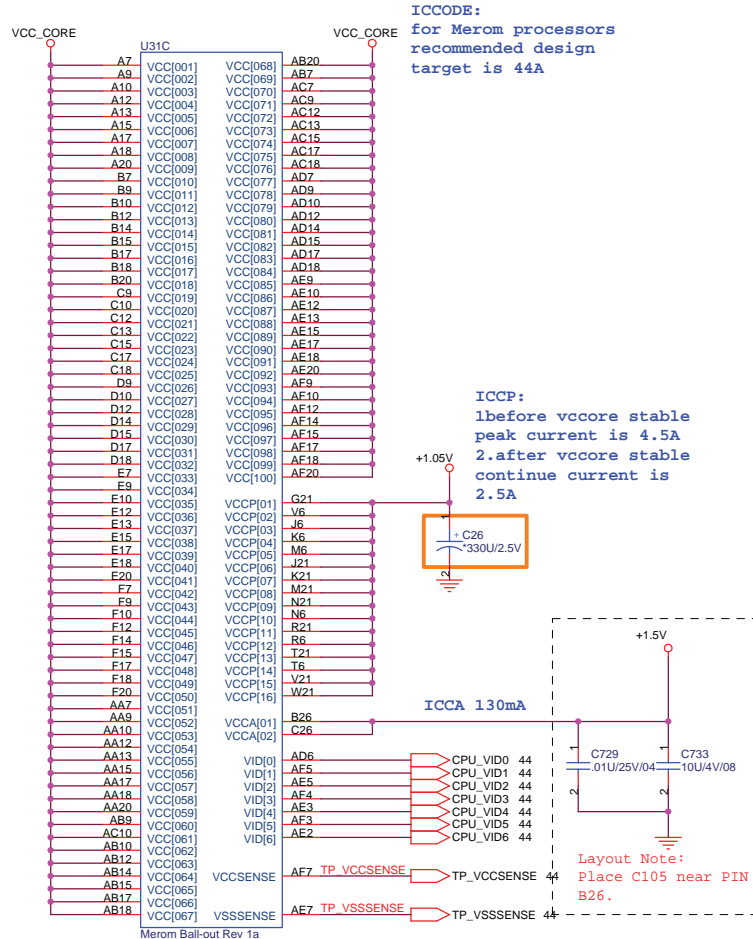
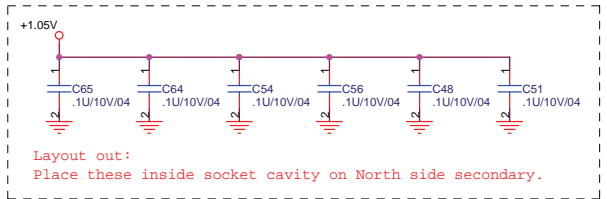
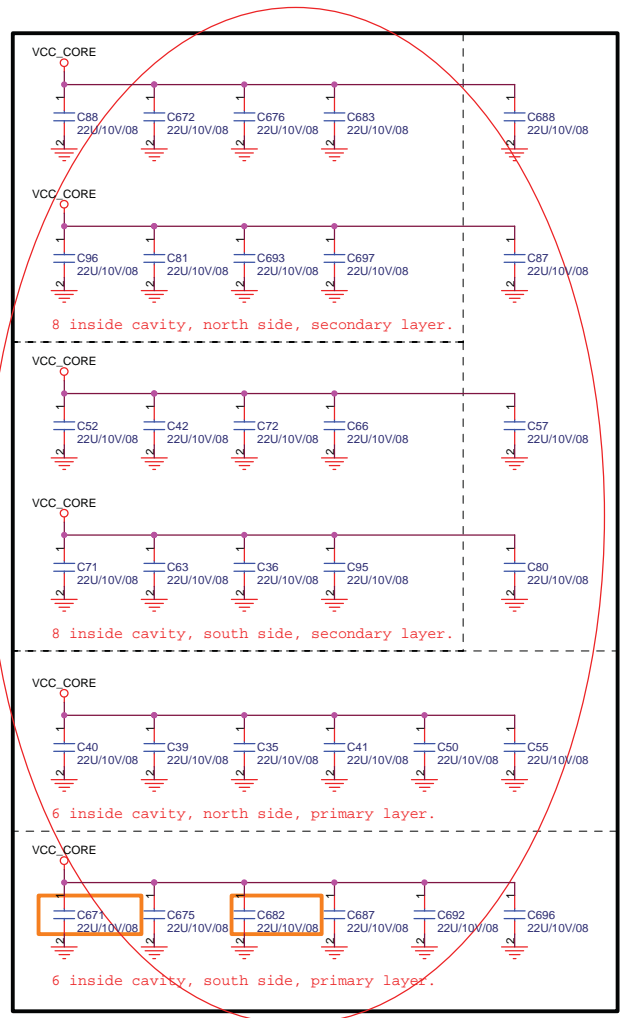


Note: Populate R5, R8, C372 & R430 when ITP connector is populated.
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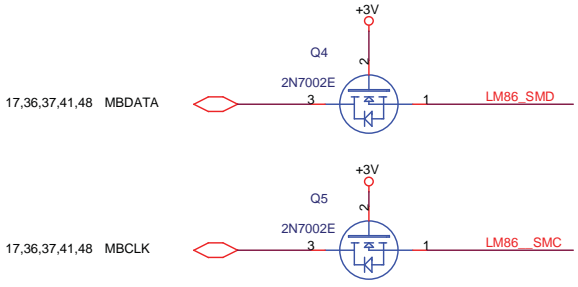
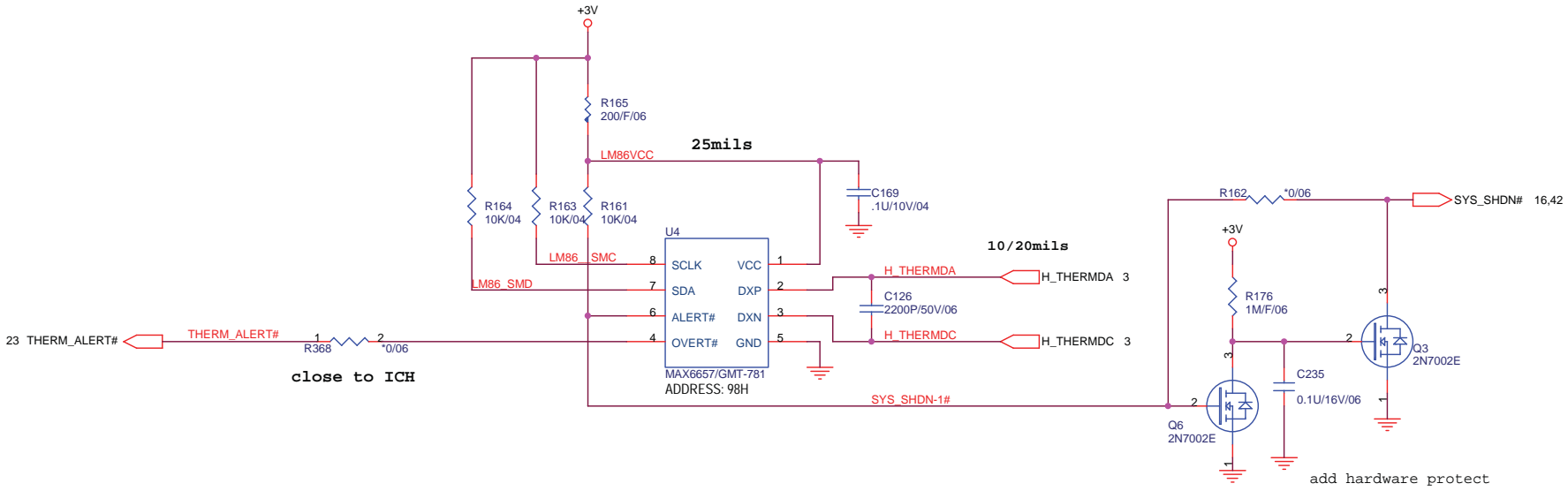
Size Custom | Document Number **CLOCK GENERATOR** | Rev 1A

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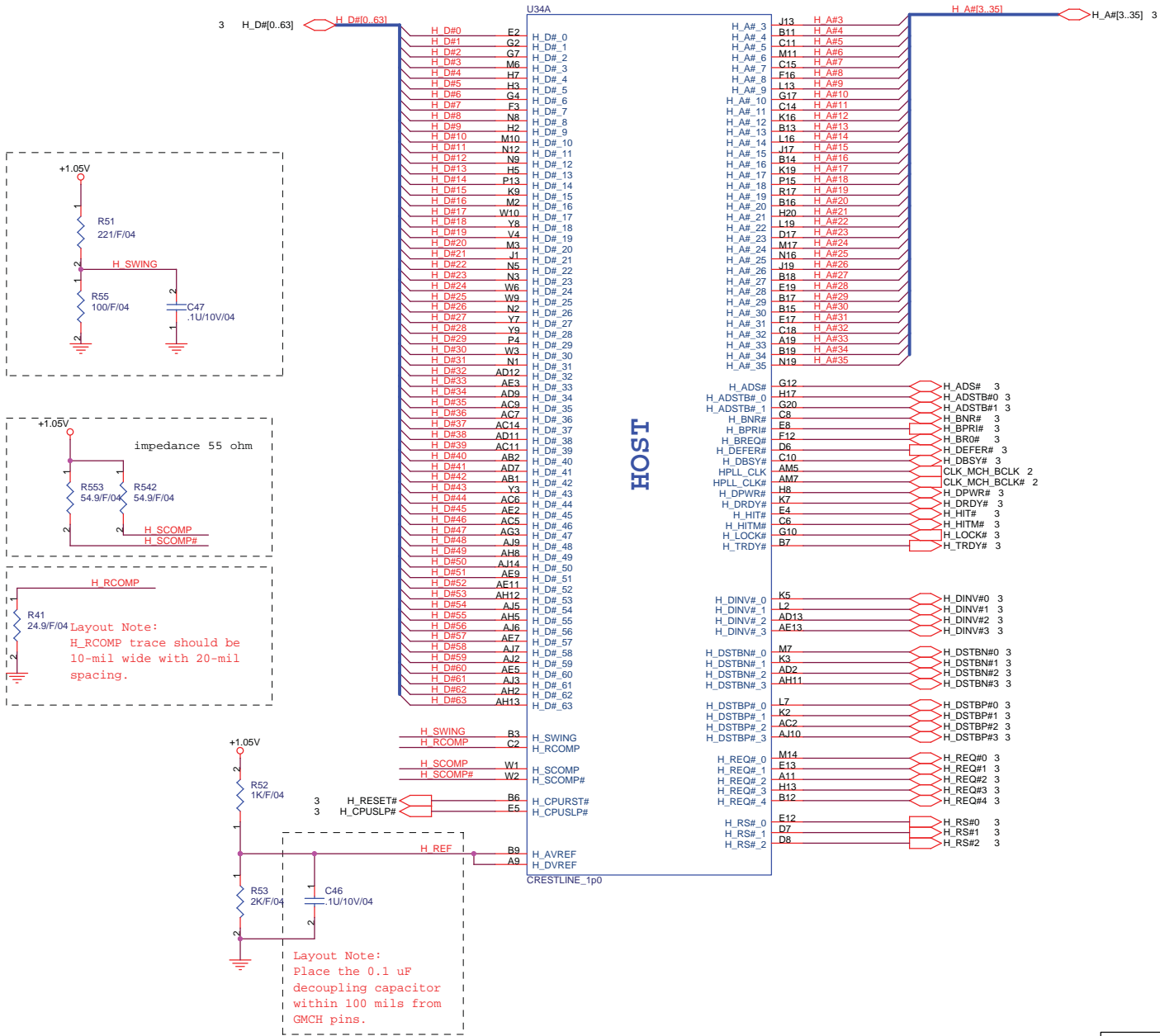
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Size Custom	Document Number Merom Processor (POWER)	Rev 1A
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Size B	Document Number THERMAL LM86	Rev 1A
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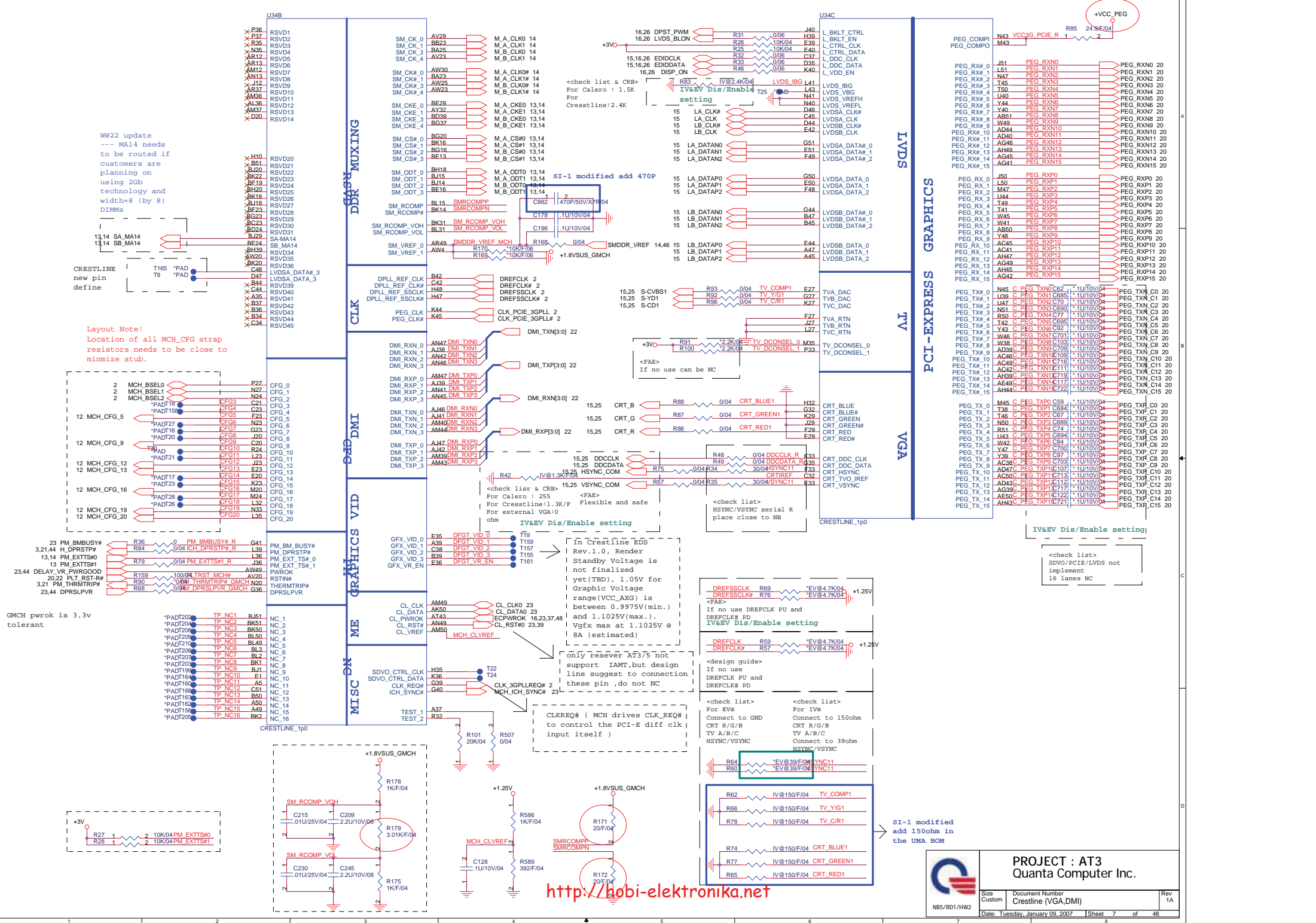


HOST

Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.

Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.

	PROJECT : AT3 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number Crestline (HOST)	
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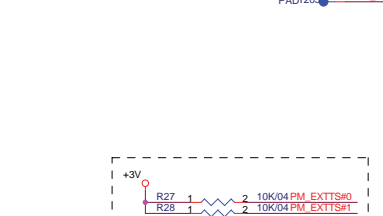
Ww22 update
 --- MA14 needs
 to be routed if
 customers are
 planning on
 using 2Gb
 technology and
 widths (by 8)
 DIMMs

CRESTLINE
 new pin
 define

Layout Note:
 Location of all MCH_CFG strap
 resistors needs to be close to
 minimize stub.

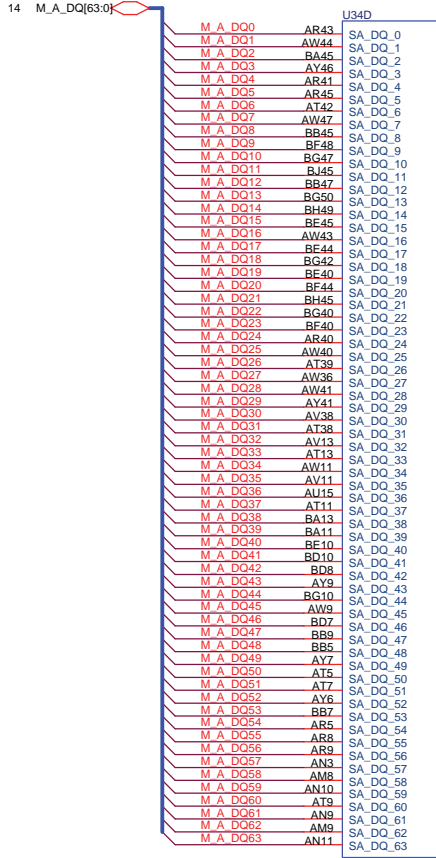
23 PM_BMBUSY#
 3.2144 H_DPRSTP#
 13.14 PM_EXTTS#0
 13 PM_EXTTS#1
 23.44 DELAY_VR_PWRGOOD
 20.22 FLT_RST#R
 3.21 PM_THRRTRIP#
 23.44 DPRSLPVR

GMCH pwrok is 3.3v
 tolerant

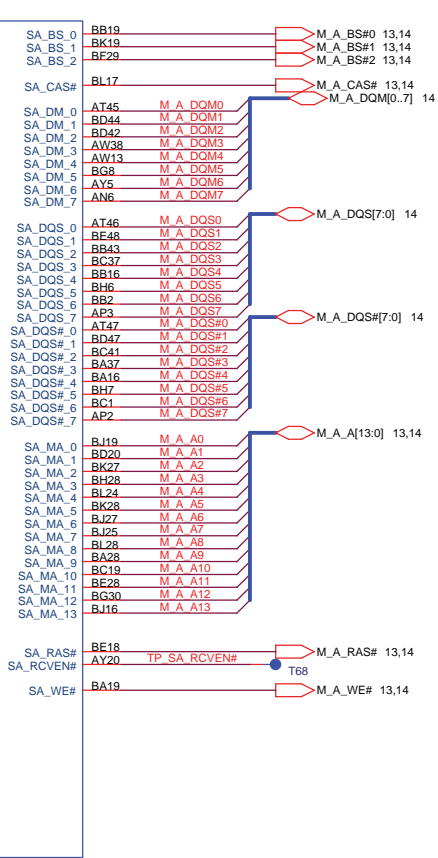


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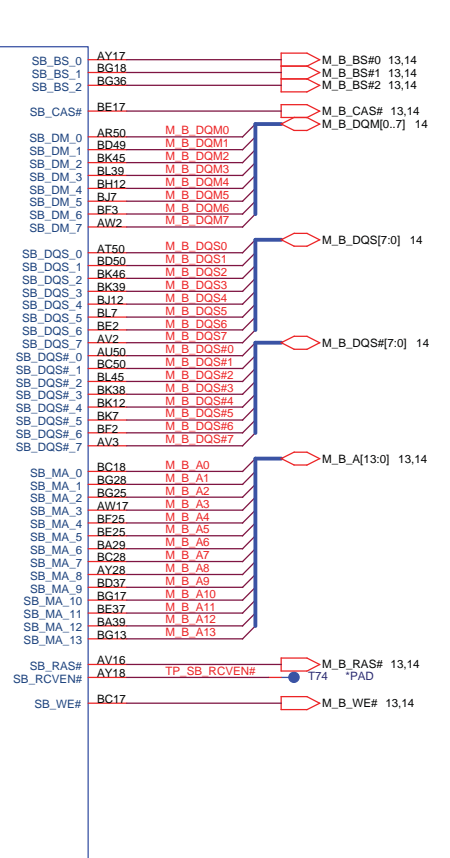
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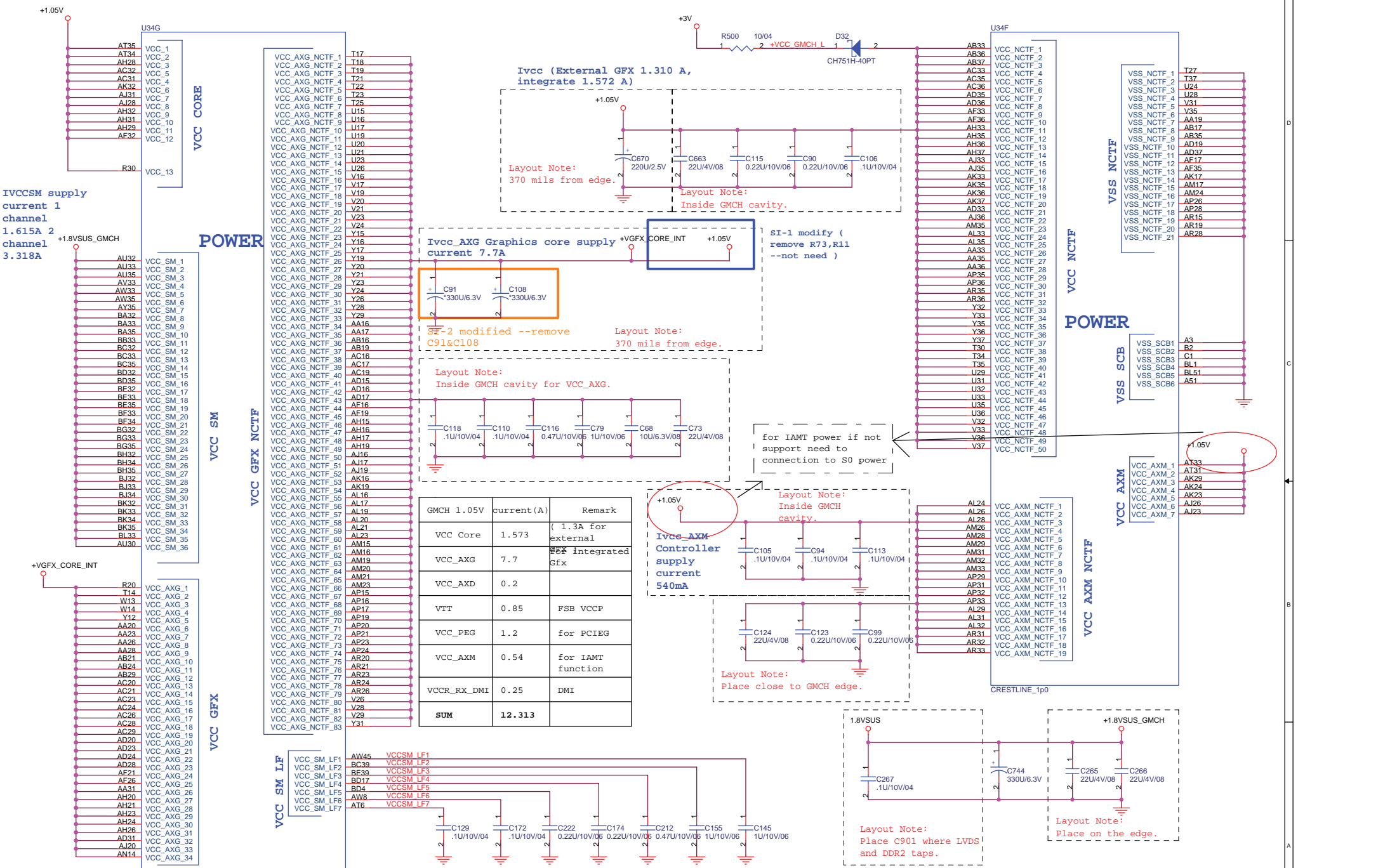
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



 NBS/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number Crestline (DDR)	Date: Tuesday, January 09, 2007



Ivcv (External GFX 1.310 A, integrate 1.572 A)

Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity.

Ivcv AXG Graphics core supply
current 7.7A

C91 & C108
C91 & C108
C91 & C108

Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity for VCC_AXG.

for IAMT power if not support need to connection to S0 power

Ivcv AXM Controller supply current 540mA

Layout Note:
Inside GMCH cavity.

Layout Note:
Place close to GMCH edge.

Layout Note:
Place C901 where LVDS and DDR2 taps.

Layout Note:
Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VIT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

POWER

POWER

VCC AXM

VCC AXM NCTF

VCC AXM

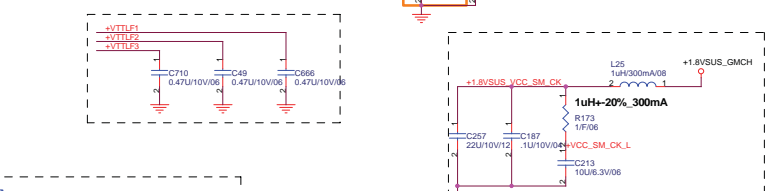
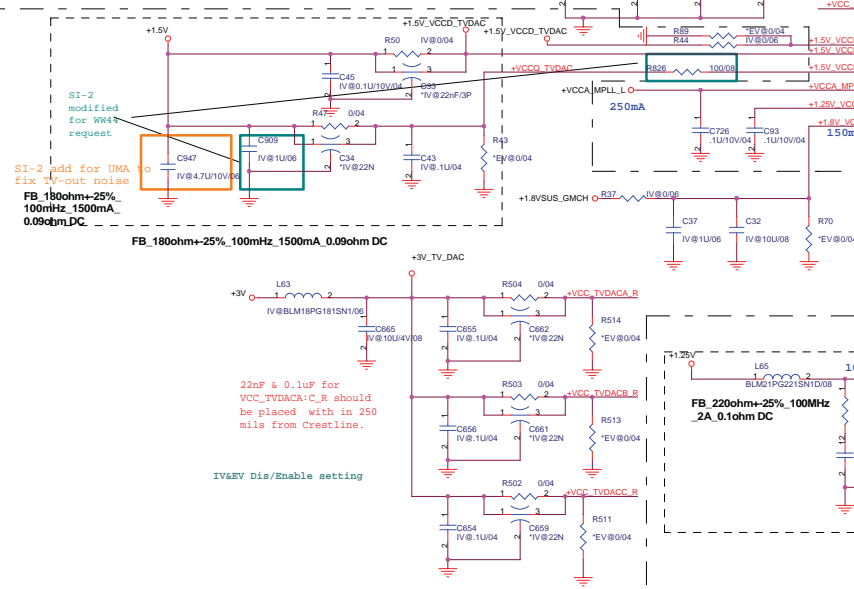
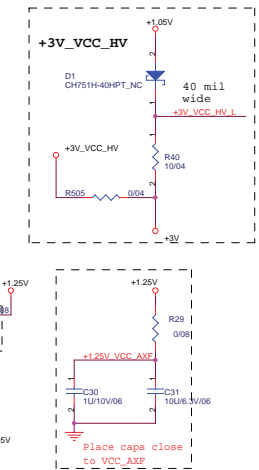
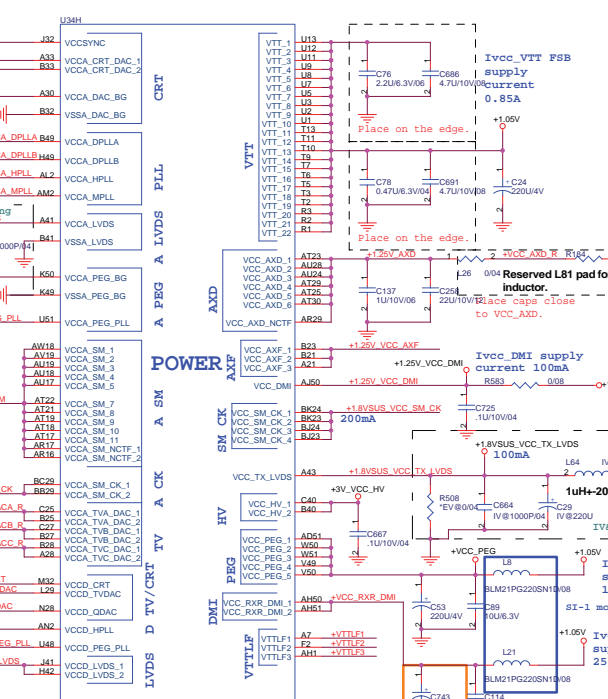
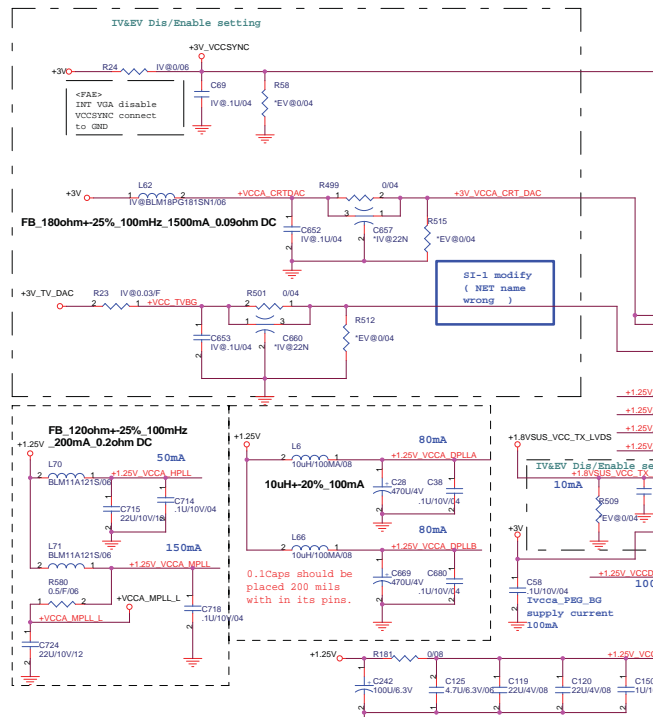
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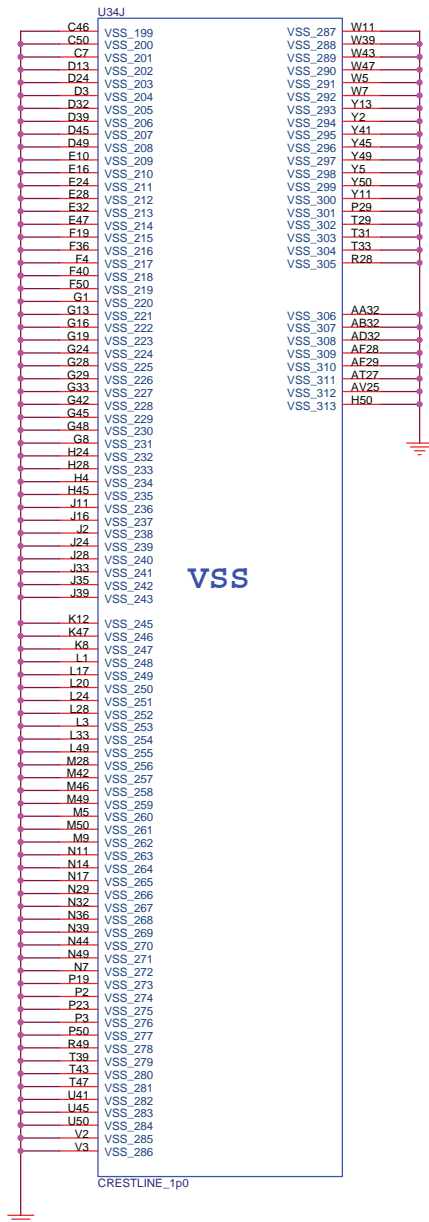
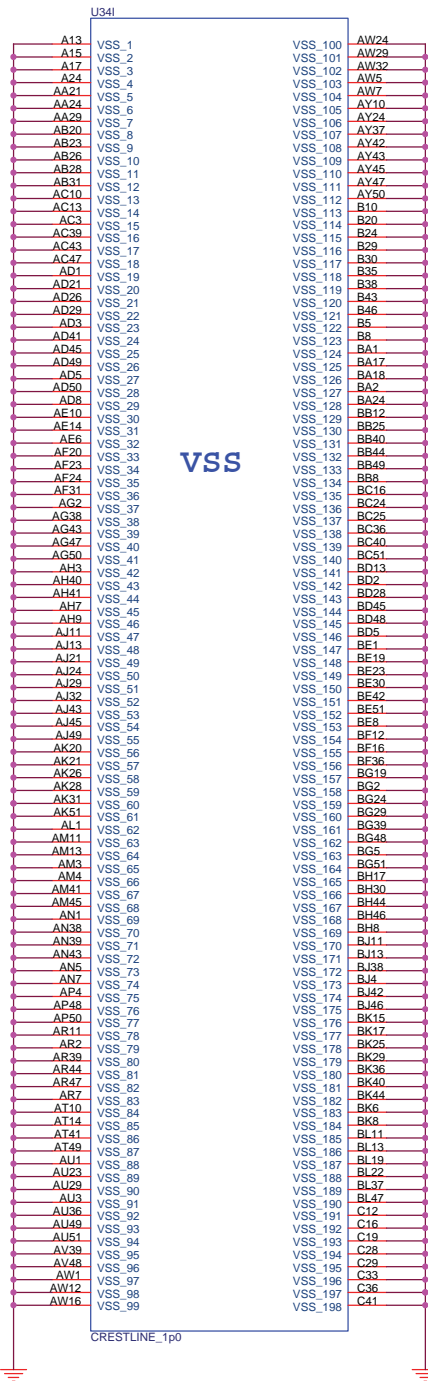

LVDS Disable/Enable guideline
External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline
External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TV_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TV_DAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TV_DAC	3.3V	GND	VCCSYNC	3.3V	GND



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Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

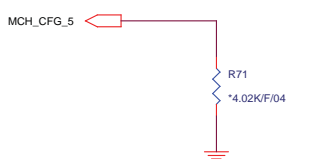
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

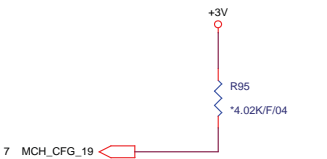
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)
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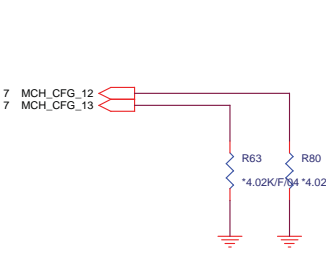
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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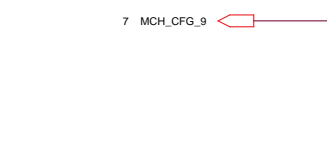
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

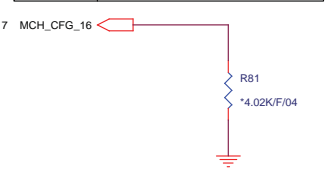
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--



SDVO Present
Strap define at External DVI control page

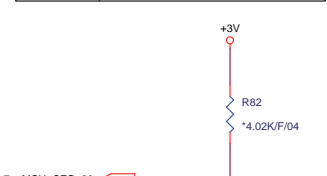
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIe Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
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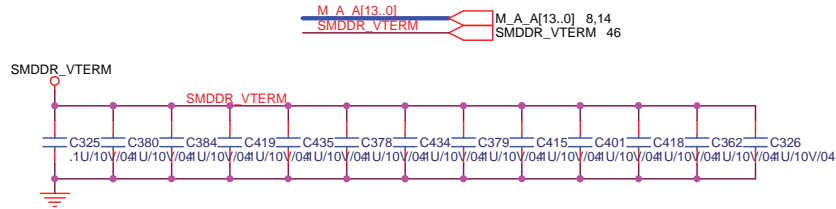


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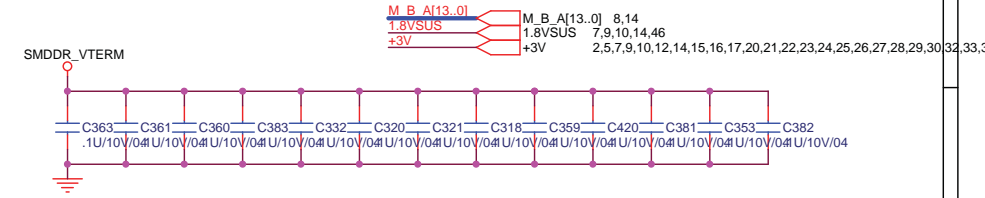
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DDRII DUAL CHANNEL A,B.

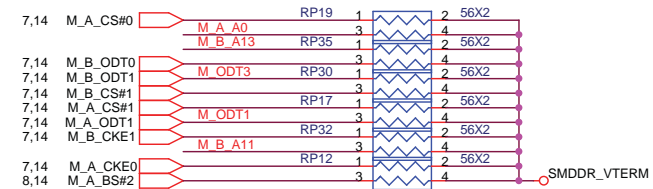
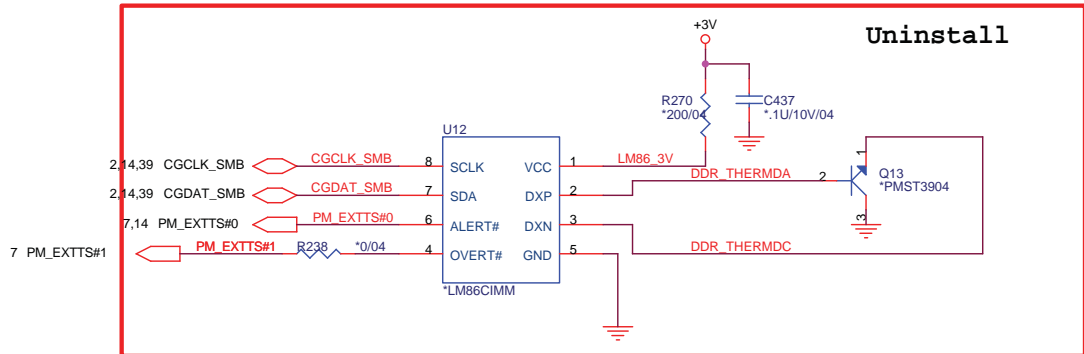
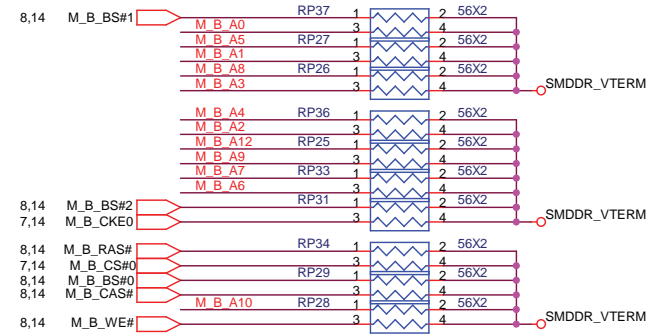
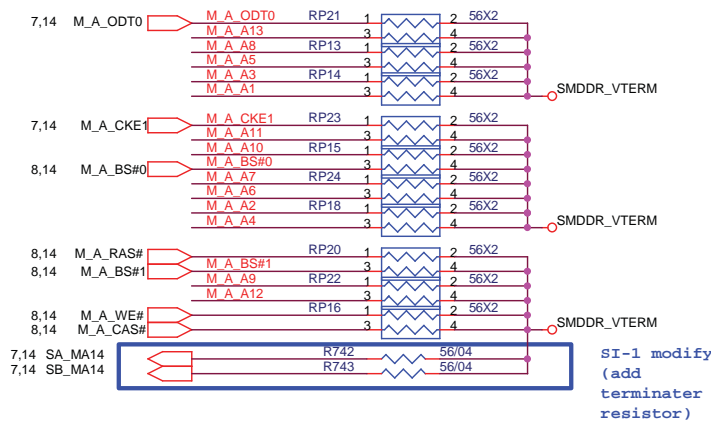
DDRII A CHANNEL



DDRII B CHANNEL

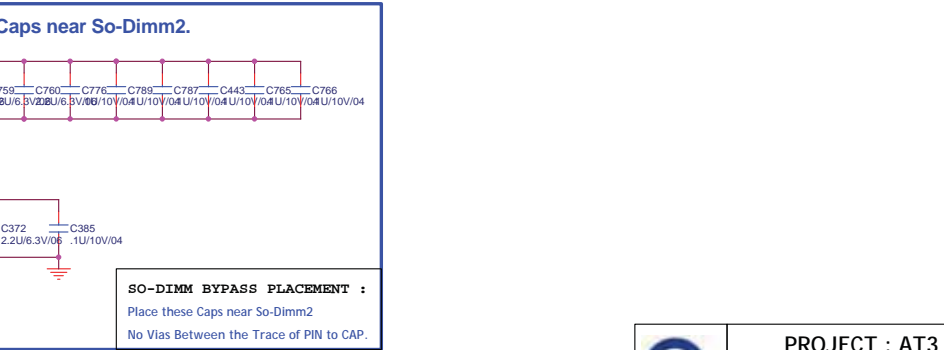
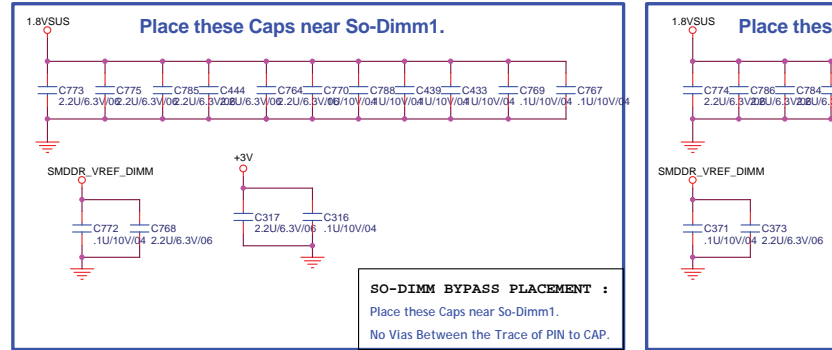
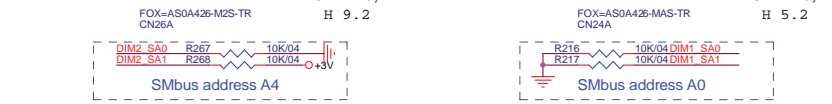
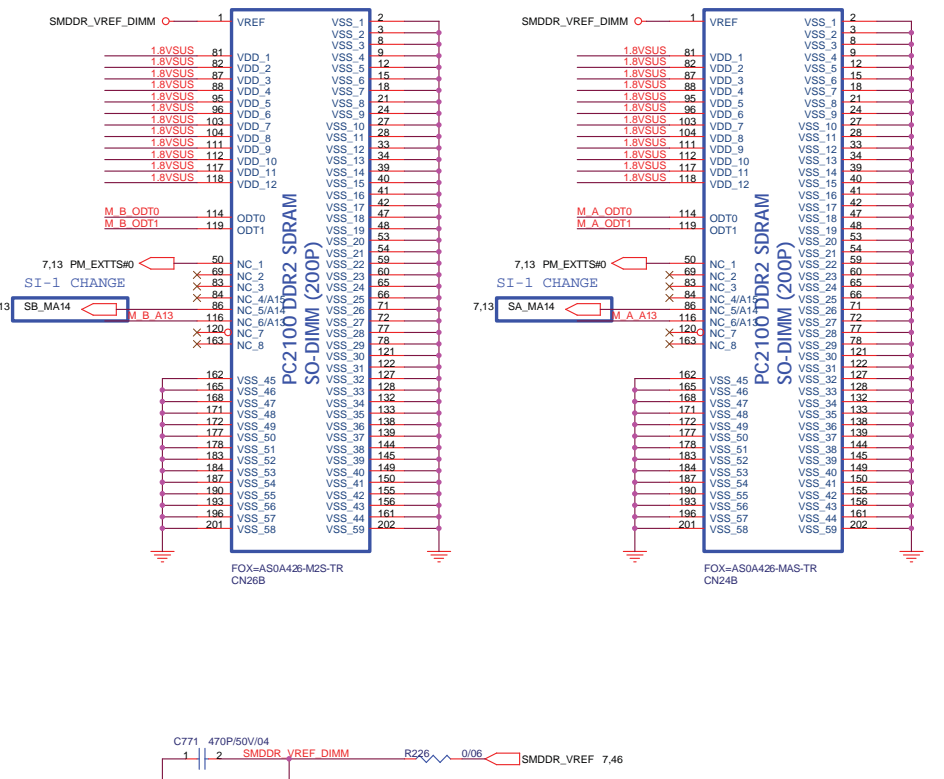
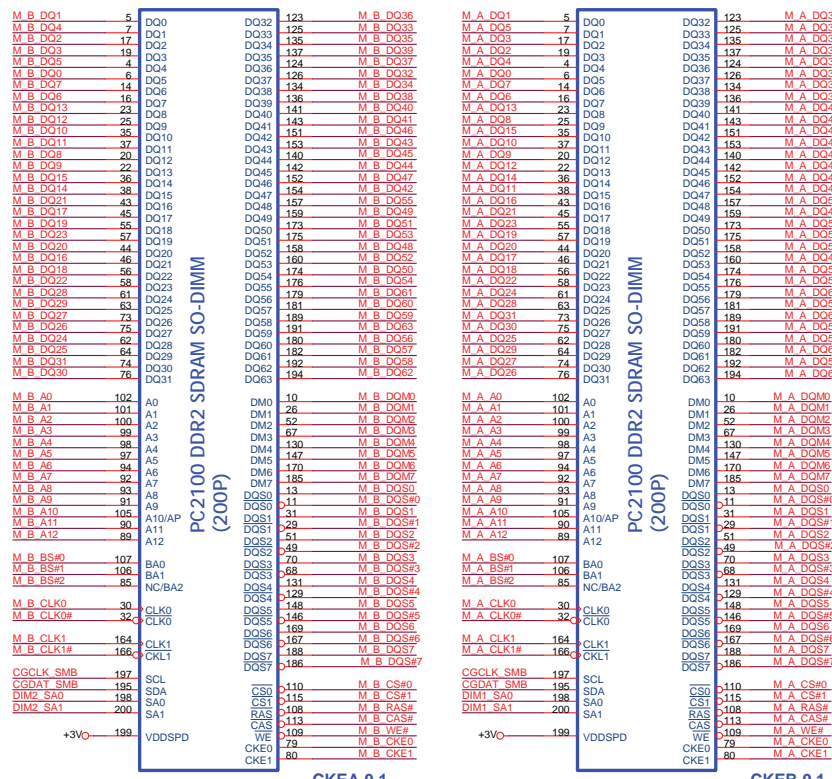
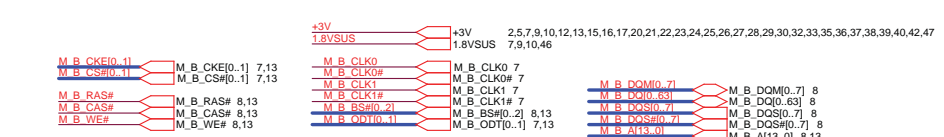
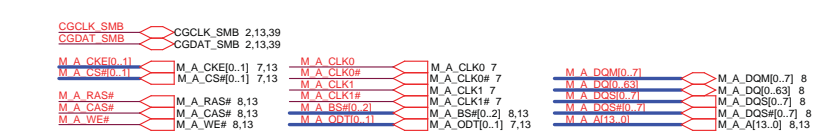


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDRR_VTERM



PROJECT : AT3
Quanta Computer Inc.

Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 13 of 48



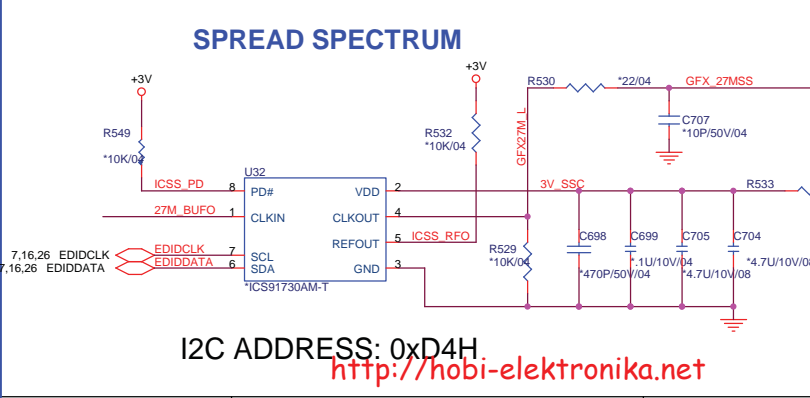
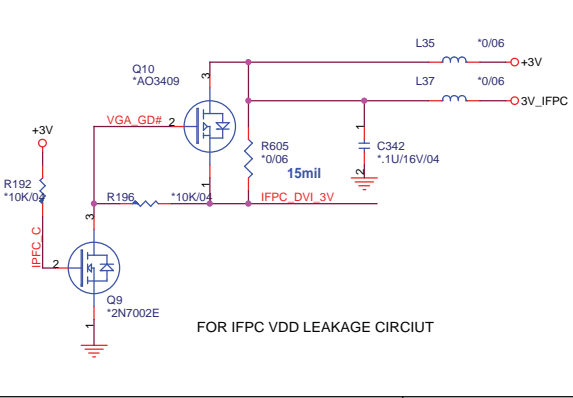
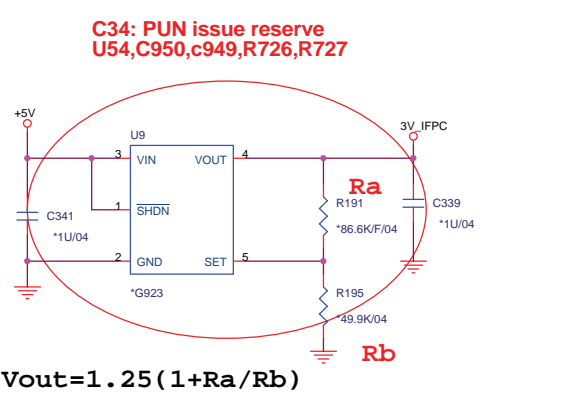
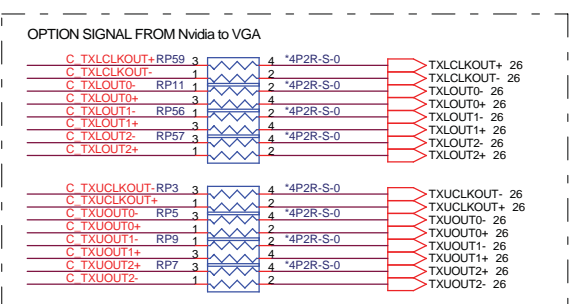
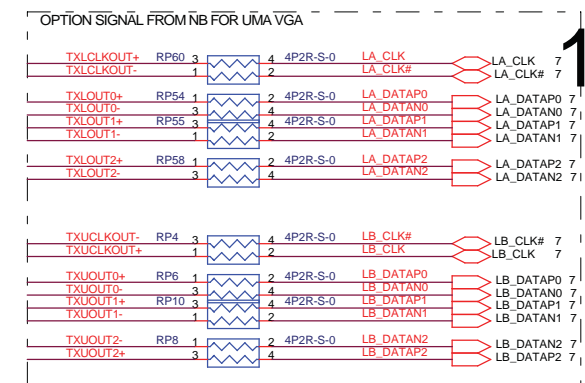
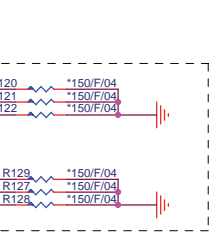
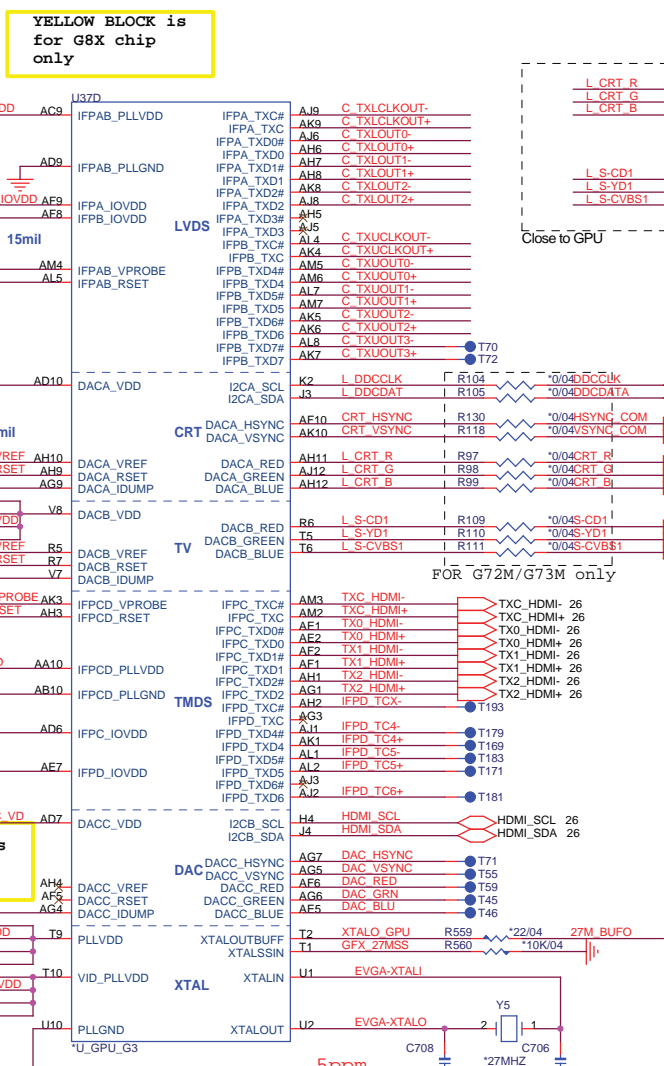
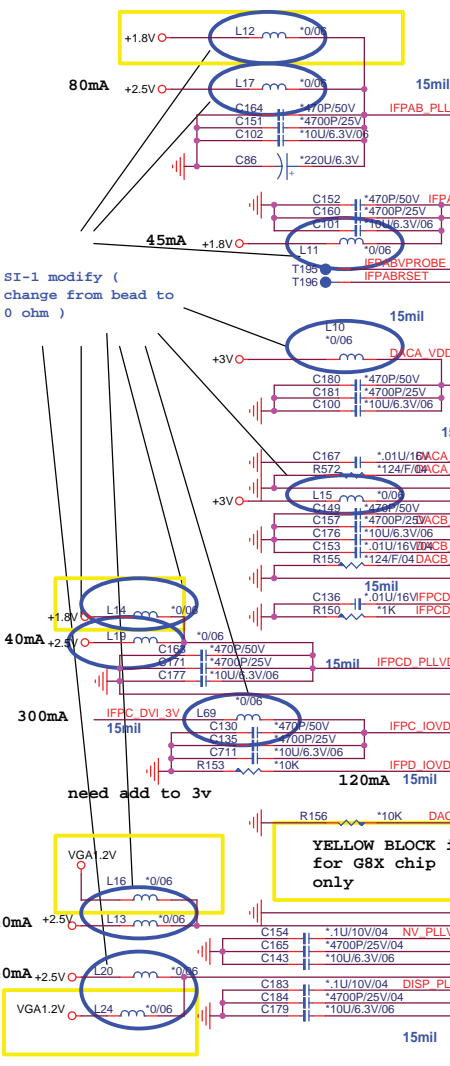
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.

PROJECT : AT3
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Size Custom Document Number
NBS/RD1/HW2 DDRII SO-DIMM(200P) Rev 1A

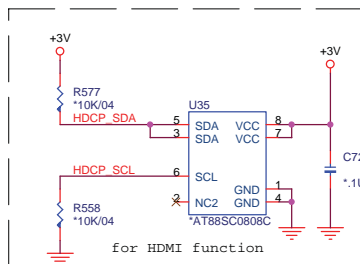
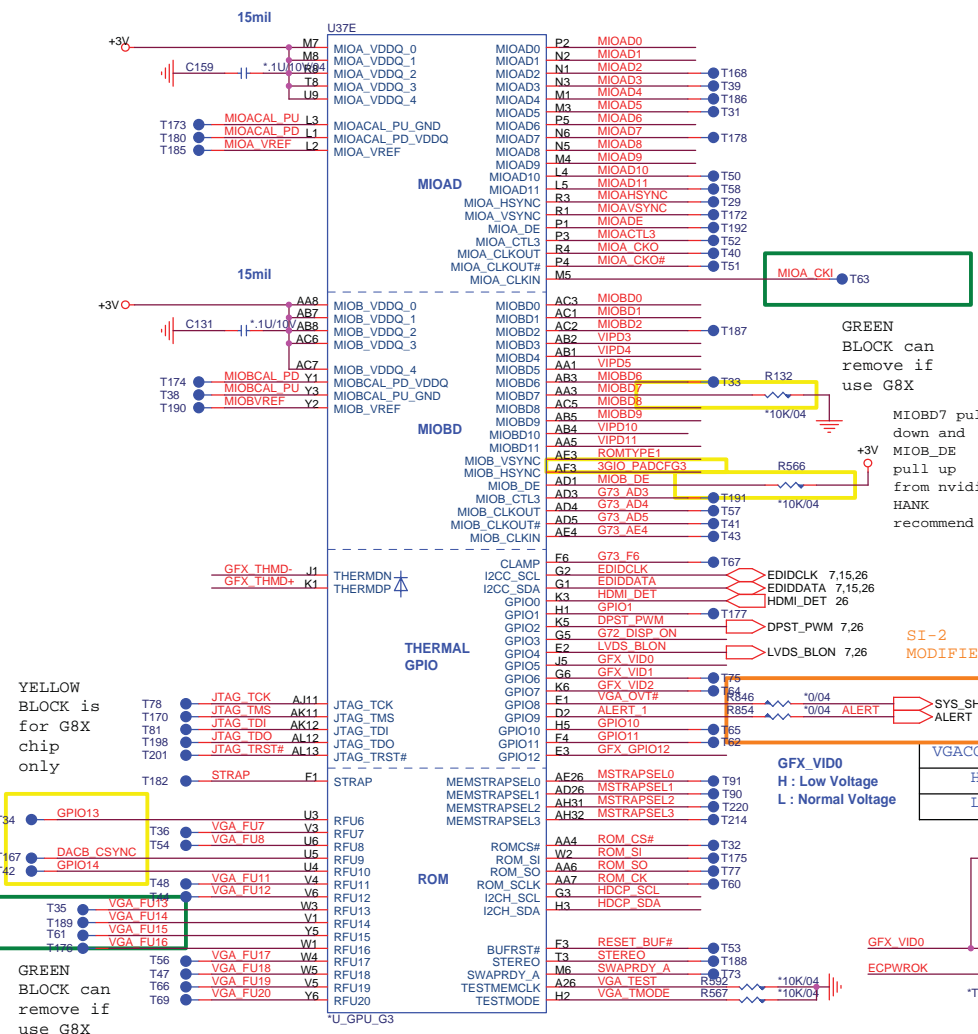
Date: Tuesday, January 09, 2007 Sheet 14 of 48



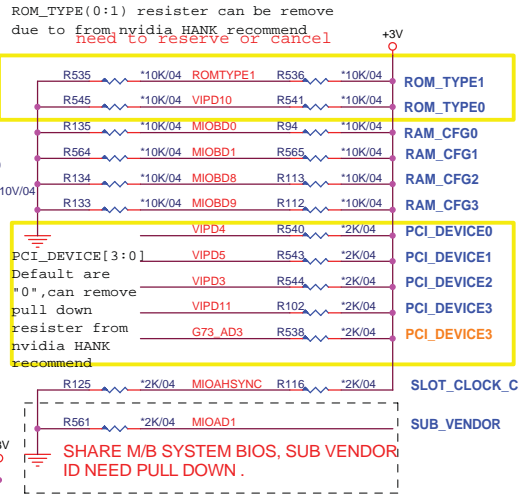
PROJECT : AT3
Quanta Computer Inc.

Size Custom | Document Number NVG73M (LVDS/DVI/CRT/TV) | Rev 1A
 Date: Tuesday, January 09, 2007 | Sheet 15 of 48

I2C ADDRESS: 0xD4H
<http://hobi-elektronika.net>



PCI_DEVICE	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

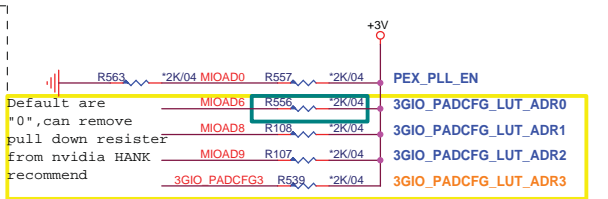
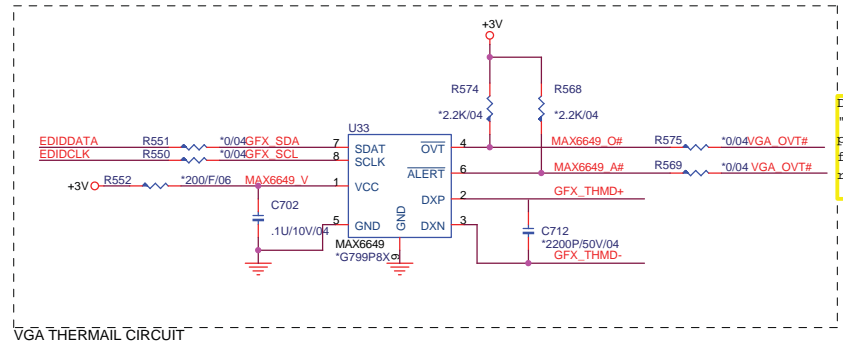
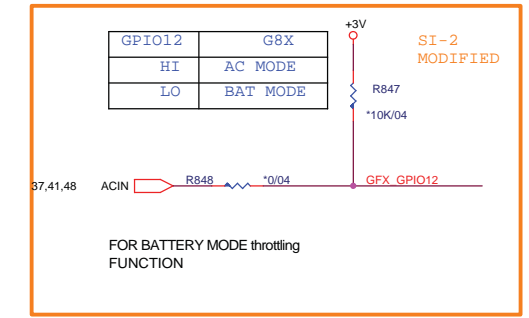


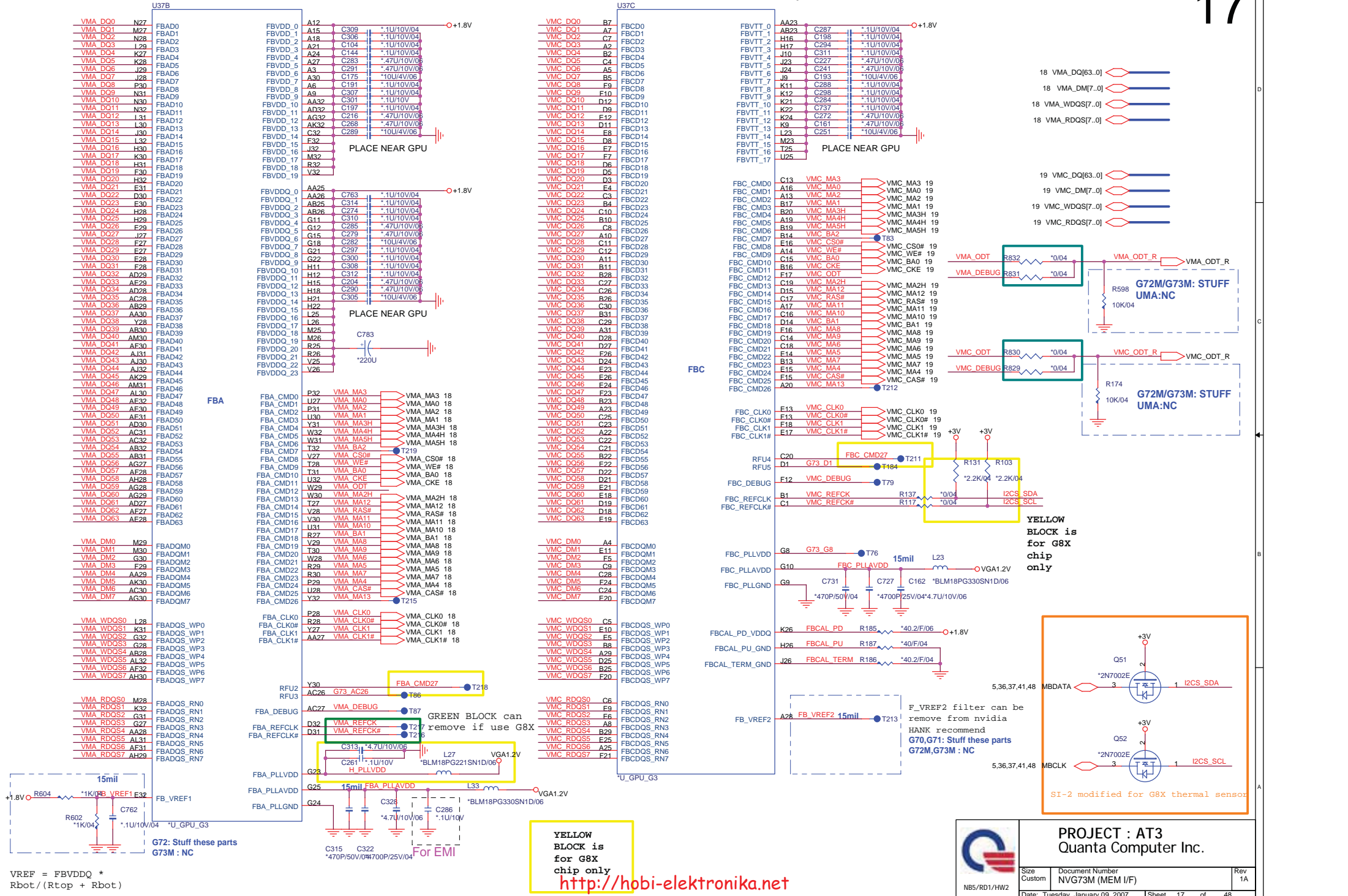
G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infinion
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infinion
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infinion
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infinion
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infinion
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



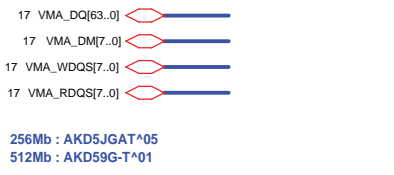
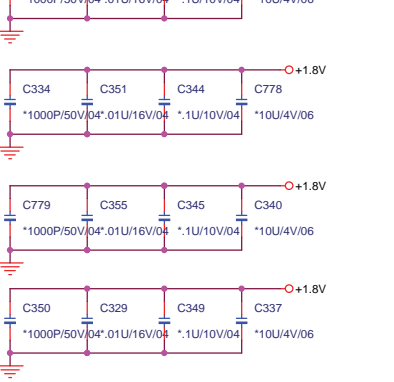
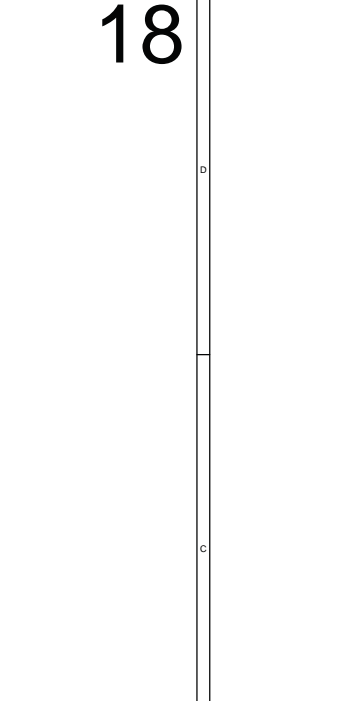
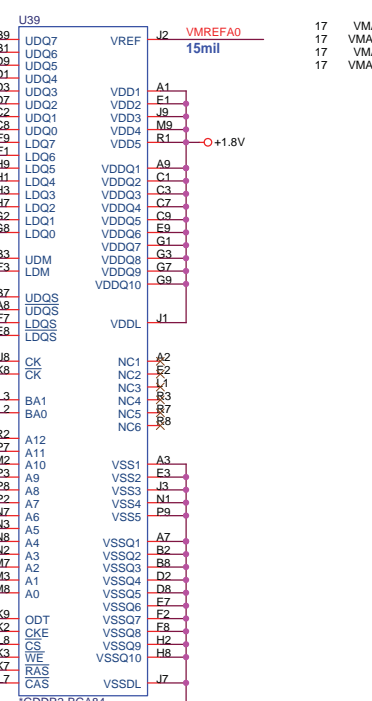
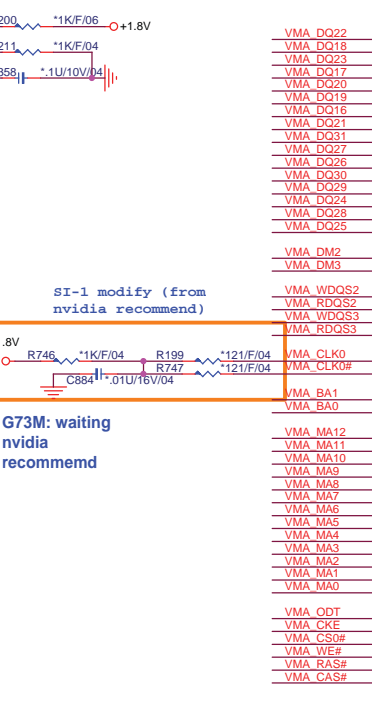


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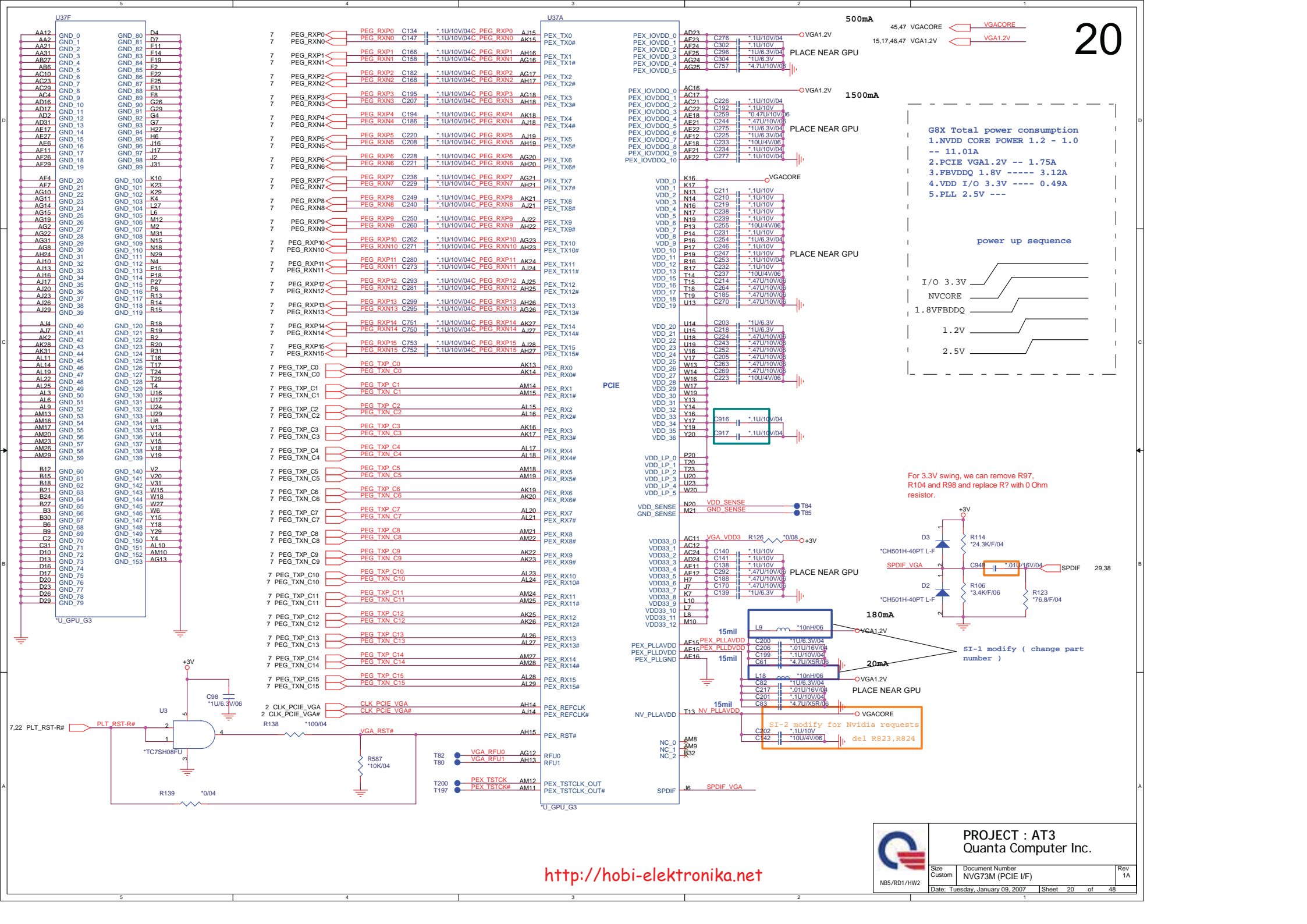
Size Custom | Document Number NVG73M (MEM I/F) | Rev 1A
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YELLOW BLOCK is for G8X chip only
<http://hobi-elektronika.net>

VREF = FBVDDQ * Rbot / (Rtop + Rbot)

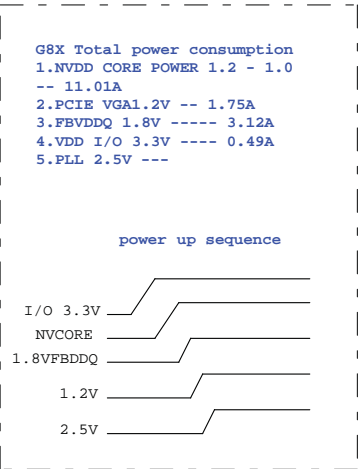


256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01



500mA 45.47 VGACORE 15.17,46,47 VGA1.2V

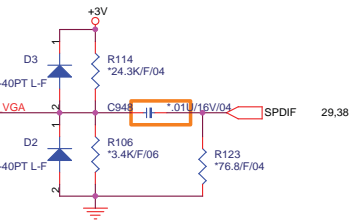
1500mA



- 1. NVDD CORE POWER 1.2 - 1.0
- 11.01A
- 2. PCIE VGA1.2V -- 1.75A
- 3. FBVDDQ 1.8V ----- 3.12A
- 4. VDD I/O 3.3V ----- 0.49A
- 5. PLL 2.5V ---

power up sequence

For 3.3V swing, we can remove R97, R104 and R98 and replace R7 with 0 Ohm resistor.



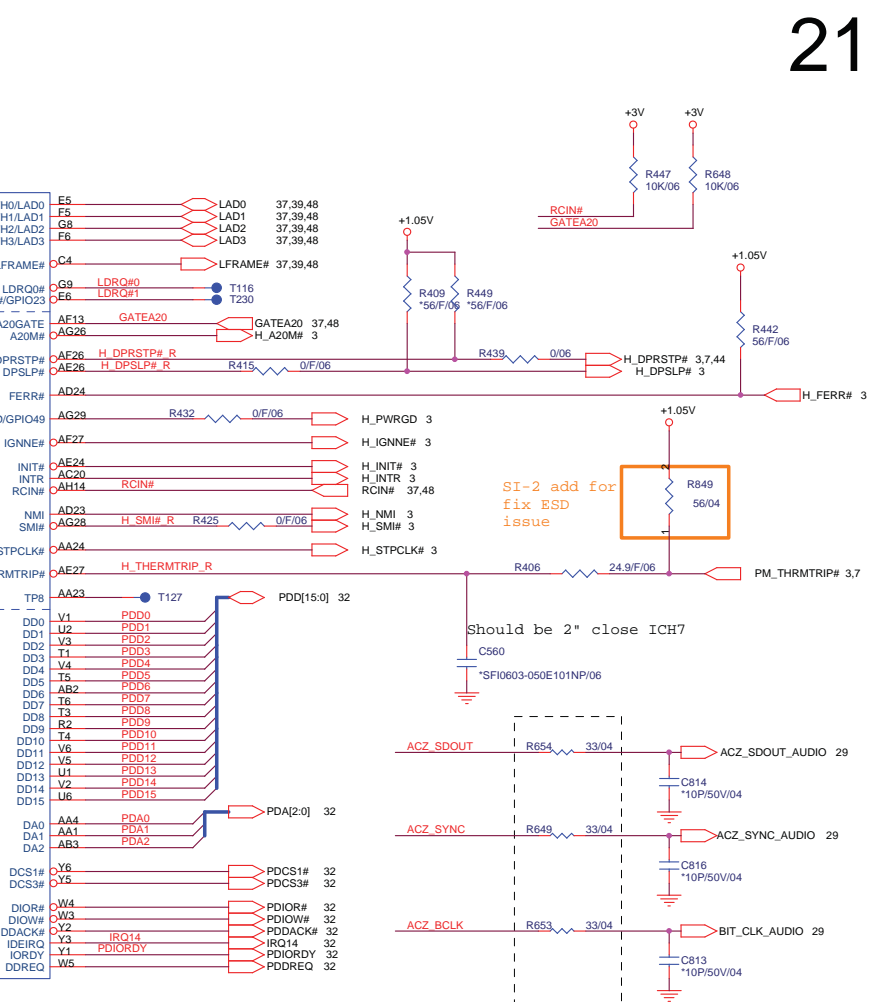
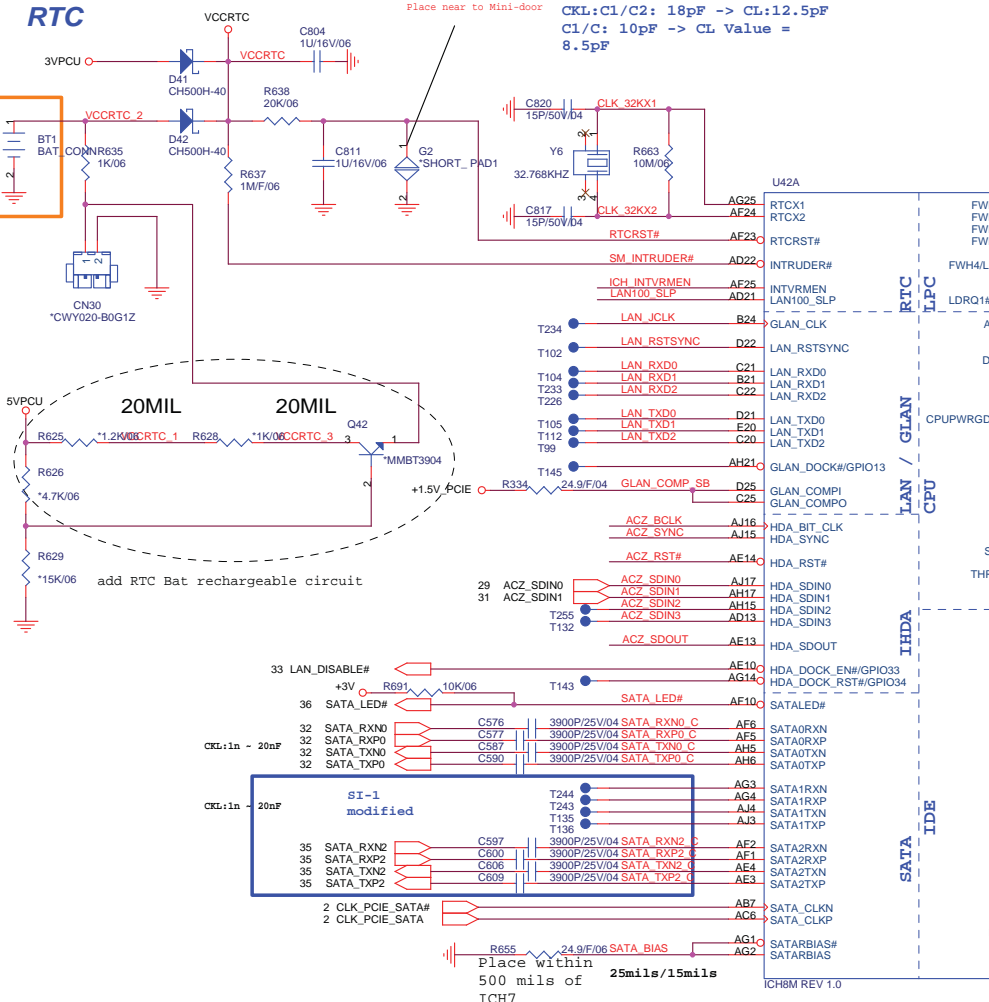
SI-1 modify (change part number)

SI-2 modify for Nvidia requests del R823, R824

PROJECT : AT3
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Size Custom	Document Number NVG73M (PCIE I/F)	Rev 1A
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RTC



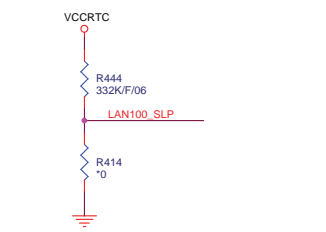
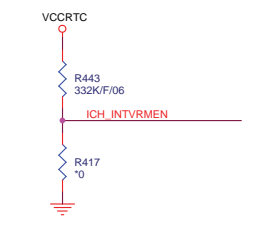
SB Strap

ICH8-M Internal VR Enable strap
 (Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

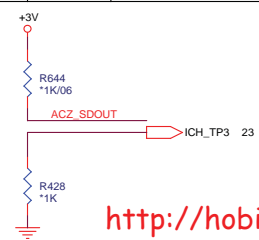
ICH8-M LAN100_SLP Strap
 (Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

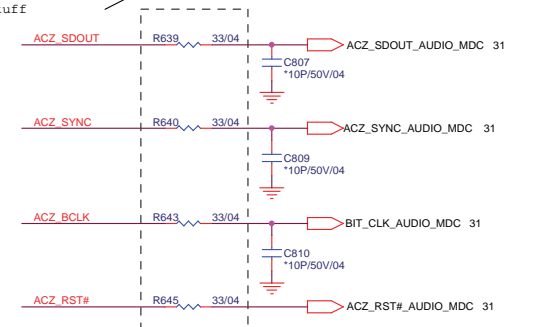


XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1



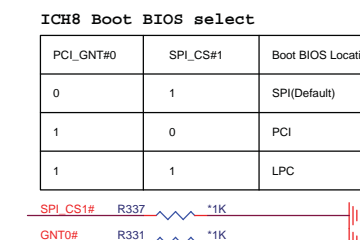
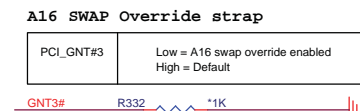
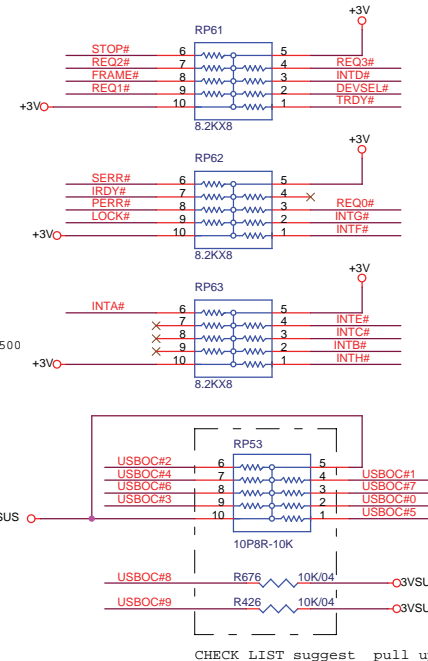
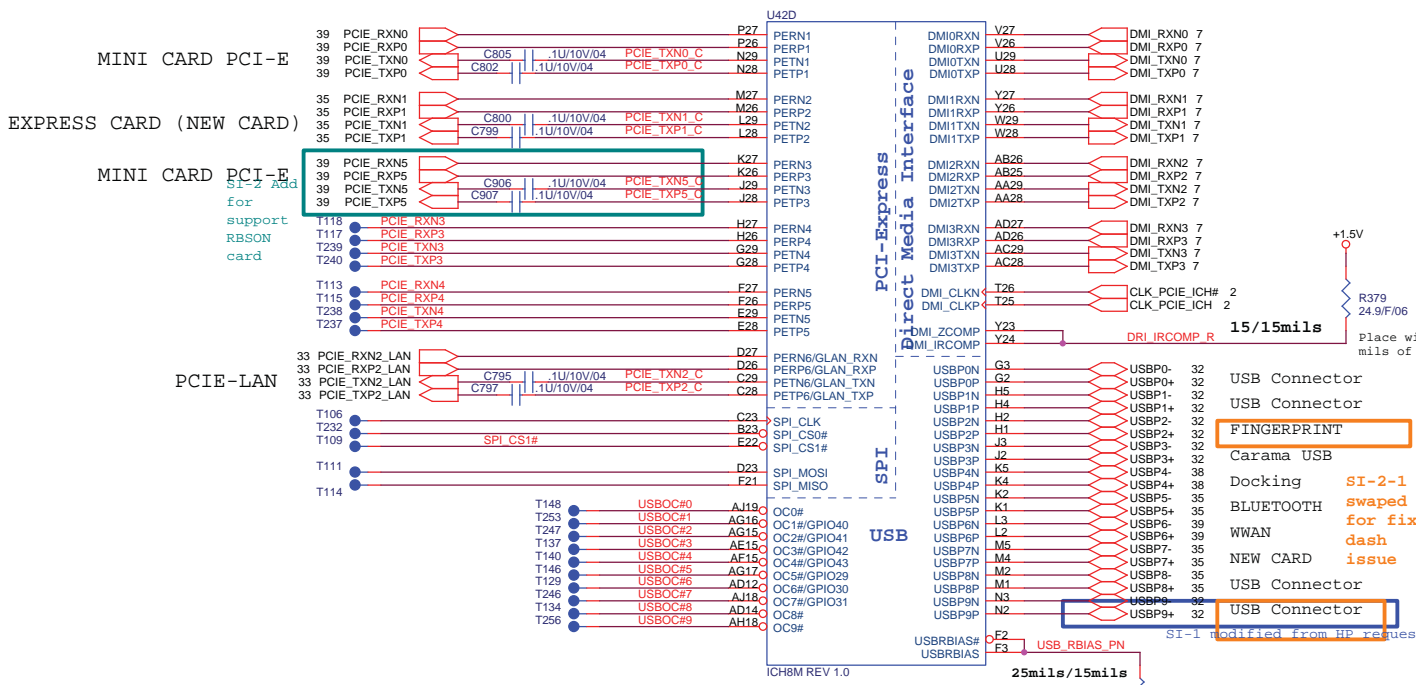
intel check list
 define to stuff
 33ohm



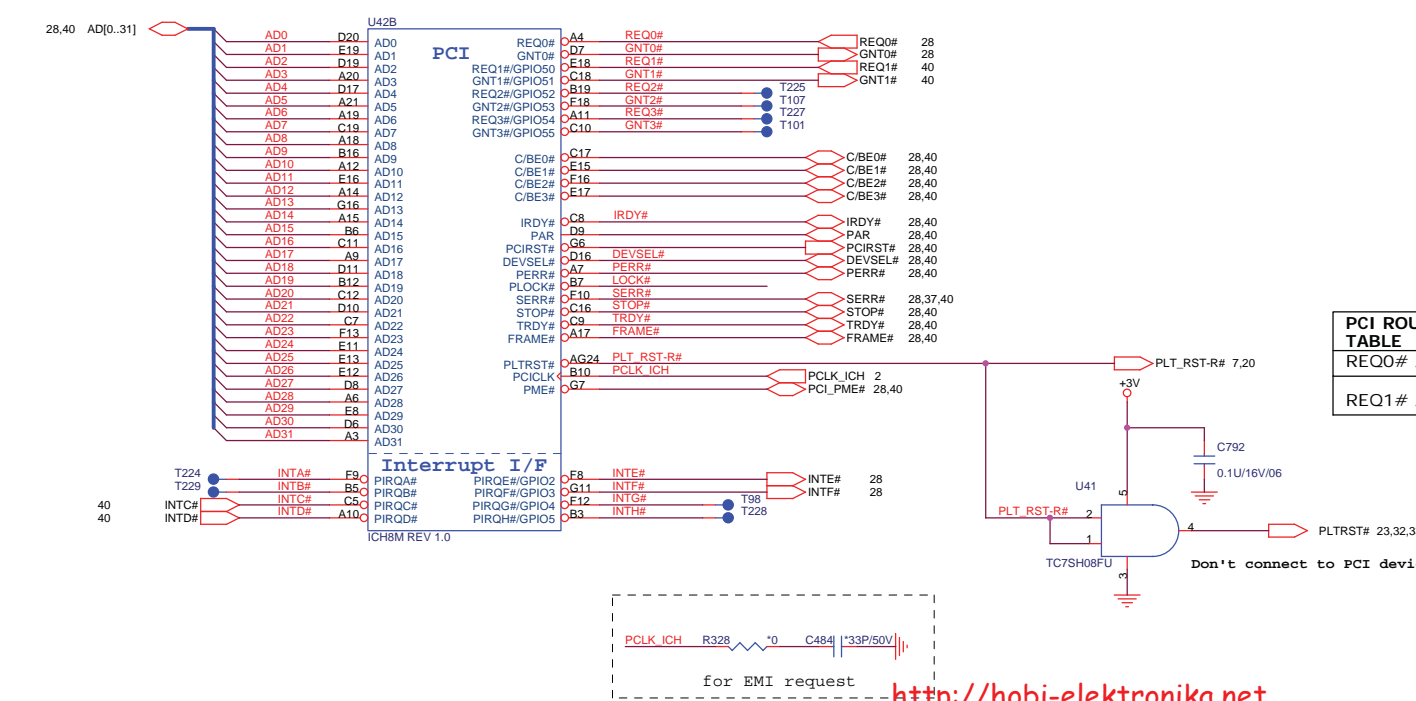
<http://hobi-elektronika.net>

PROJECT : AT3
 Quanta Computer Inc.

Size Custom	Document Number ICH7-M HOST(1/4)	Rev 1A
Date: Tuesday, January 09, 2007 Sheet 21 of 48		



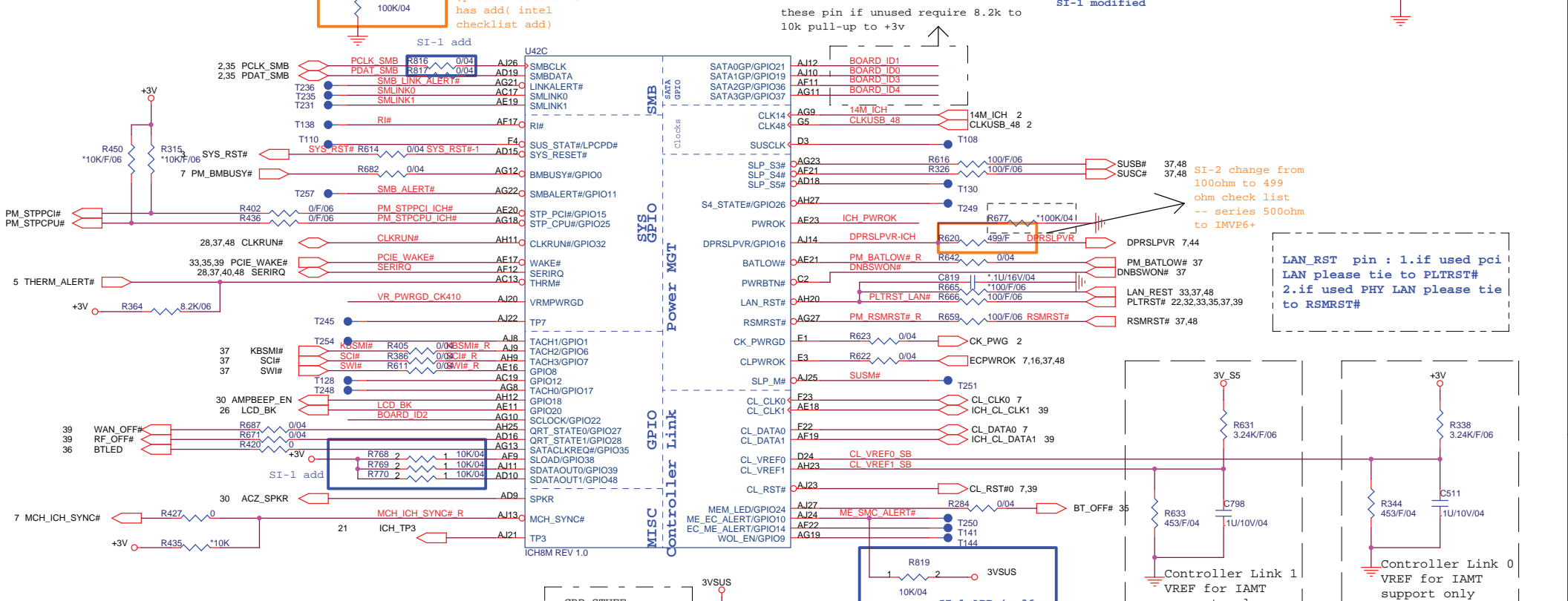
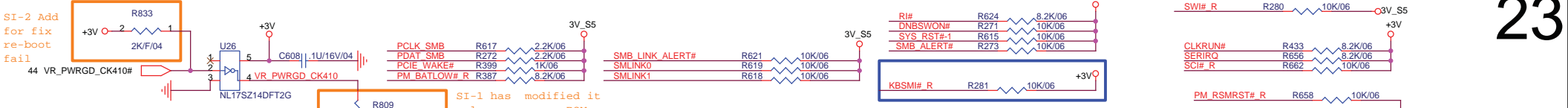
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug



PROJECT : AT3
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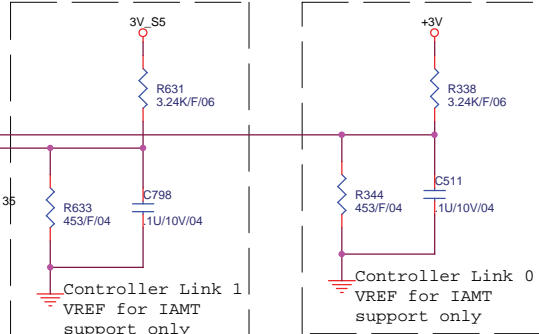
Size Custom Document Number ICH7-M M PCI E(2/4) Rev 1A

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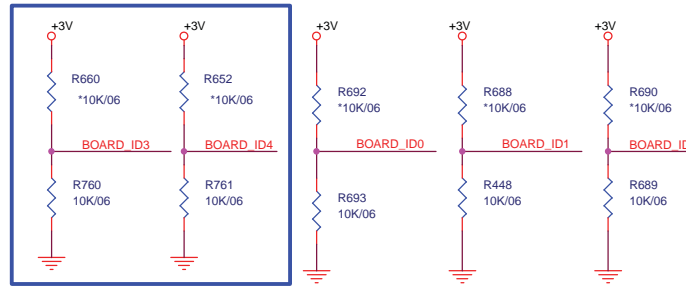
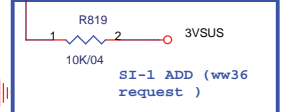
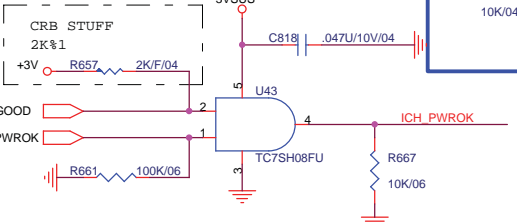
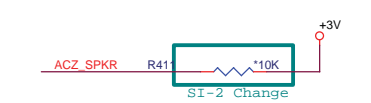


SI-2 change from 100ohm to 499 ohm check list -- series 500ohm to IMVP6+

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#



No Reboot strap
 HDA_SPKR Low = Default High = No Reboot



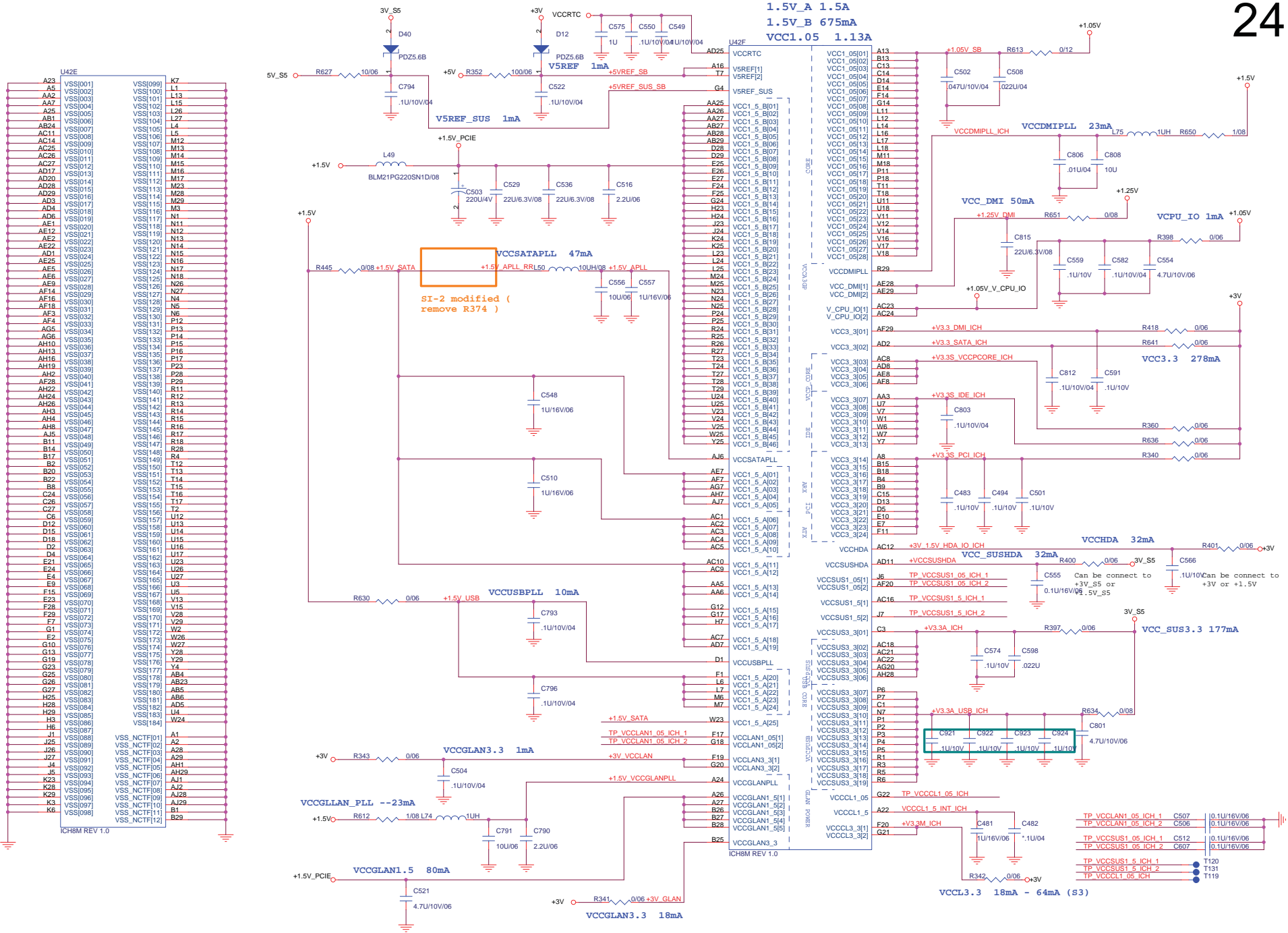
Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15"PAV Discrete 965PM+G86MV+128M (0:1:0)	17" PAV Discrete 965PM+G86MV+128M (0:1:1)	17" PAV Discrete 965PM+G84MV+256M (1:0:0)	17" PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff

<http://mobi-elektronika.net>

PROJECT : AT3
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Size Custom	Document Number ICH7-M GPIO(3/4)	Rev 1A
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1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A



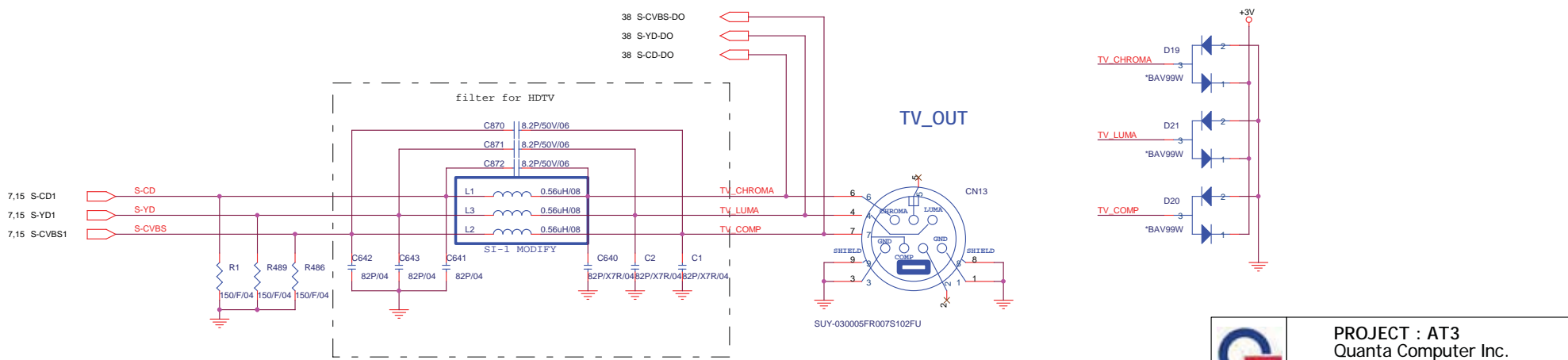
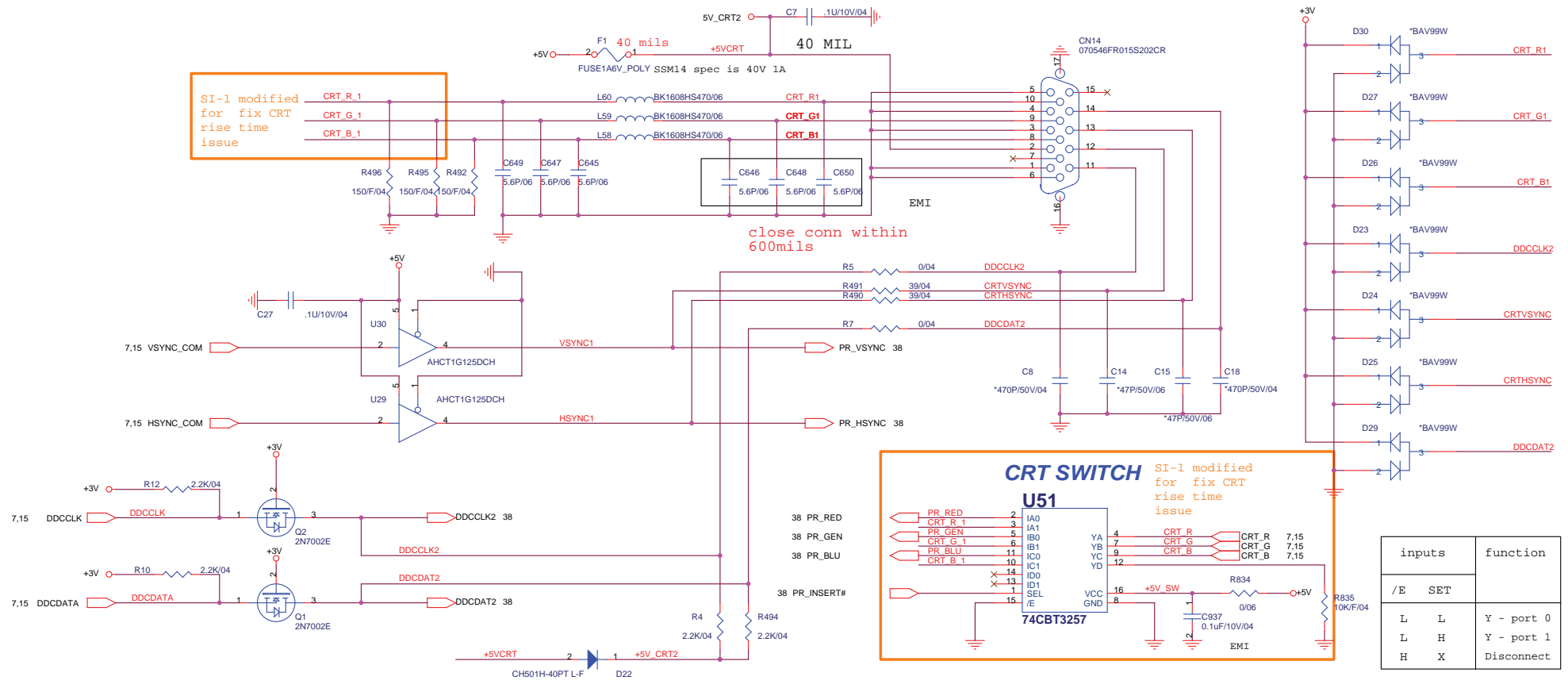
U42E

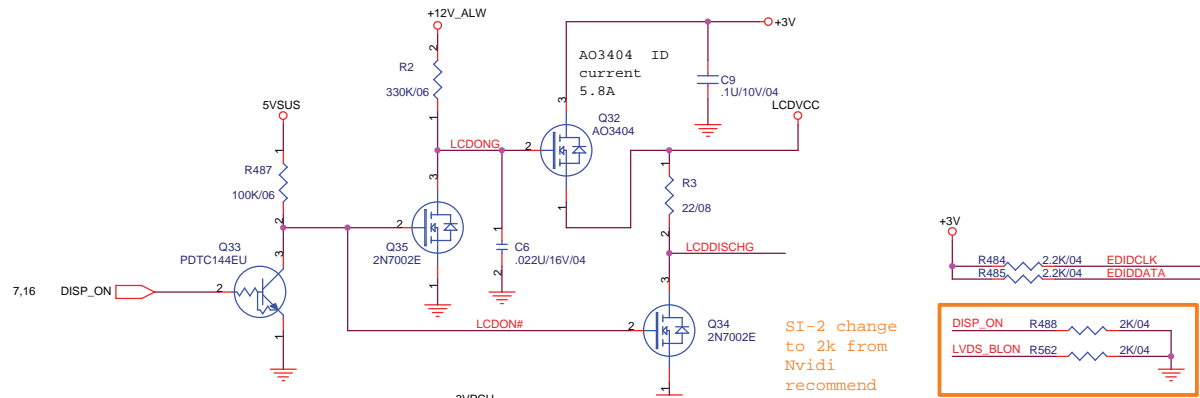
A23	VSS[001]	VSS[099]	K7
A5	VSS[002]	VSS[100]	L1
AA2	VSS[003]	VSS[101]	L13
AA7	VSS[004]	VSS[102]	L26
A25	VSS[005]	VSS[103]	L26
AB1	VSS[006]	VSS[104]	L27
AB24	VSS[007]	VSS[105]	L4
AC11	VSS[008]	VSS[106]	L5
AC14	VSS[009]	VSS[107]	M12
AC25	VSS[010]	VSS[108]	M13
AC26	VSS[011]	VSS[109]	M14
AC27	VSS[012]	VSS[110]	M15
AD20	VSS[013]	VSS[111]	M16
AD28	VSS[014]	VSS[112]	M17
AD29	VSS[015]	VSS[113]	M23
AD3	VSS[016]	VSS[114]	M28
AD4	VSS[017]	VSS[115]	M29
AD6	VSS[018]	VSS[116]	N1
AE12	VSS[019]	VSS[117]	N11
AE1	VSS[020]	VSS[118]	N13
AE2	VSS[021]	VSS[119]	N13
AE22	VSS[022]	VSS[120]	N21
AD1	VSS[023]	VSS[121]	N15
AE25	VSS[024]	VSS[122]	N16
AE5	VSS[025]	VSS[123]	N17
AE6	VSS[026]	VSS[124]	N17
AE9	VSS[027]	VSS[125]	N18
AE14	VSS[028]	VSS[126]	N27
AE16	VSS[029]	VSS[127]	N27
AF3	VSS[030]	VSS[128]	N4
AF4	VSS[031]	VSS[129]	N6
AG5	VSS[032]	VSS[130]	P12
AG6	VSS[033]	VSS[131]	P13
AH10	VSS[034]	VSS[132]	P14
AH13	VSS[035]	VSS[133]	P14
AH16	VSS[036]	VSS[134]	P16
AH19	VSS[037]	VSS[135]	P17
AH2	VSS[038]	VSS[136]	P23
AH22	VSS[039]	VSS[137]	P28
AH24	VSS[040]	VSS[138]	P28
AH26	VSS[041]	VSS[139]	R11
AH3	VSS[042]	VSS[140]	R12
AH4	VSS[043]	VSS[141]	R12
AH8	VSS[044]	VSS[142]	R13
AH11	VSS[045]	VSS[143]	R14
AH12	VSS[046]	VSS[144]	R15
AH18	VSS[047]	VSS[145]	R16
AH19	VSS[048]	VSS[146]	R18
B11	VSS[049]	VSS[147]	R28
B14	VSS[050]	VSS[148]	R4
B17	VSS[051]	VSS[149]	T12
B2	VSS[052]	VSS[150]	T13
B20	VSS[053]	VSS[151]	T13
B22	VSS[054]	VSS[152]	T14
BB	VSS[055]	VSS[153]	T15
C24	VSS[056]	VSS[154]	T16
C26	VSS[057]	VSS[155]	T17
C27	VSS[058]	VSS[156]	U12
C6	VSS[059]	VSS[157]	U13
D12	VSS[060]	VSS[158]	U13
D15	VSS[061]	VSS[159]	U14
D18	VSS[062]	VSS[160]	U15
D2	VSS[063]	VSS[161]	U16
D4	VSS[064]	VSS[162]	U17
E21	VSS[065]	VSS[163]	U27
E24	VSS[066]	VSS[164]	U27
E4	VSS[067]	VSS[165]	U3
E9	VSS[068]	VSS[166]	U3
F15	VSS[069]	VSS[167]	V15
F28	VSS[070]	VSS[168]	V15
F29	VSS[071]	VSS[169]	V28
F7	VSS[072]	VSS[170]	V29
G1	VSS[073]	VSS[171]	V2
G1	VSS[074]	VSS[172]	V2
G10	VSS[075]	VSS[173]	W26
G13	VSS[076]	VSS[174]	W27
G19	VSS[077]	VSS[175]	Y28
G23	VSS[078]	VSS[176]	Y29
G25	VSS[079]	VSS[177]	Y4
G26	VSS[080]	VSS[178]	AB4
G27	VSS[081]	VSS[179]	AB23
H25	VSS[082]	VSS[180]	AB5
H28	VSS[083]	VSS[181]	AB6
H29	VSS[084]	VSS[182]	AD6
H3	VSS[085]	VSS[183]	LA
H6	VSS[086]	VSS[184]	W24
J1	VSS[087]	VSS[185]	
J25	VSS[088]	VSS_NCTF[01]	A1
J26	VSS[089]	VSS_NCTF[02]	A2
J26	VSS[090]	VSS_NCTF[03]	A28
J27	VSS[091]	VSS_NCTF[04]	AH1
J4	VSS[092]	VSS_NCTF[05]	AH29
J5	VSS[093]	VSS_NCTF[06]	AJ1
K23	VSS[094]	VSS_NCTF[07]	AJ28
K29	VSS[095]	VSS_NCTF[08]	AJ29
K3	VSS[096]	VSS_NCTF[09]	B29
K6	VSS[097]	VSS_NCTF[10]	
	VSS[098]	VSS_NCTF[11]	
		VSS_NCTF[12]	

PROJECT : AT3
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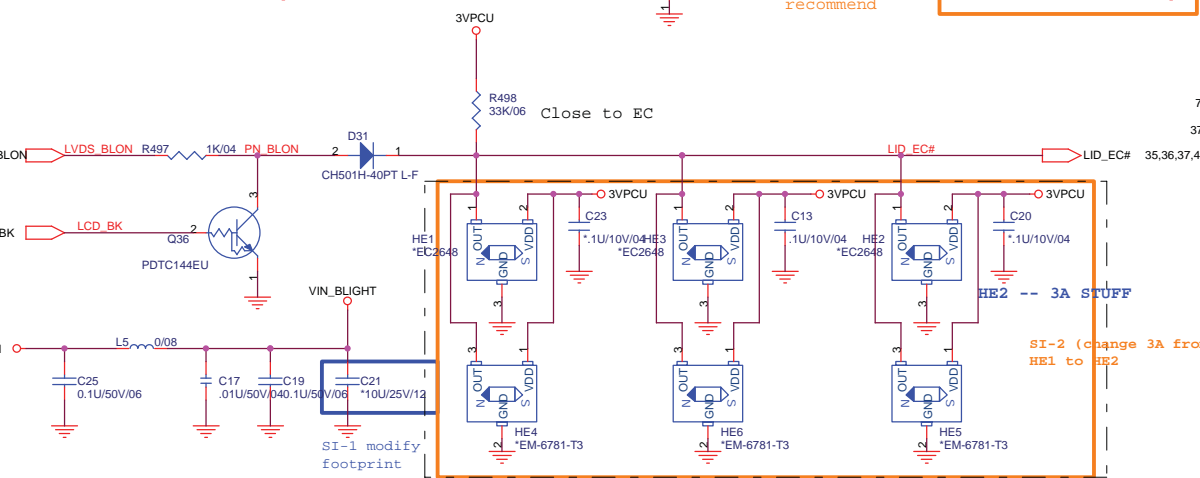
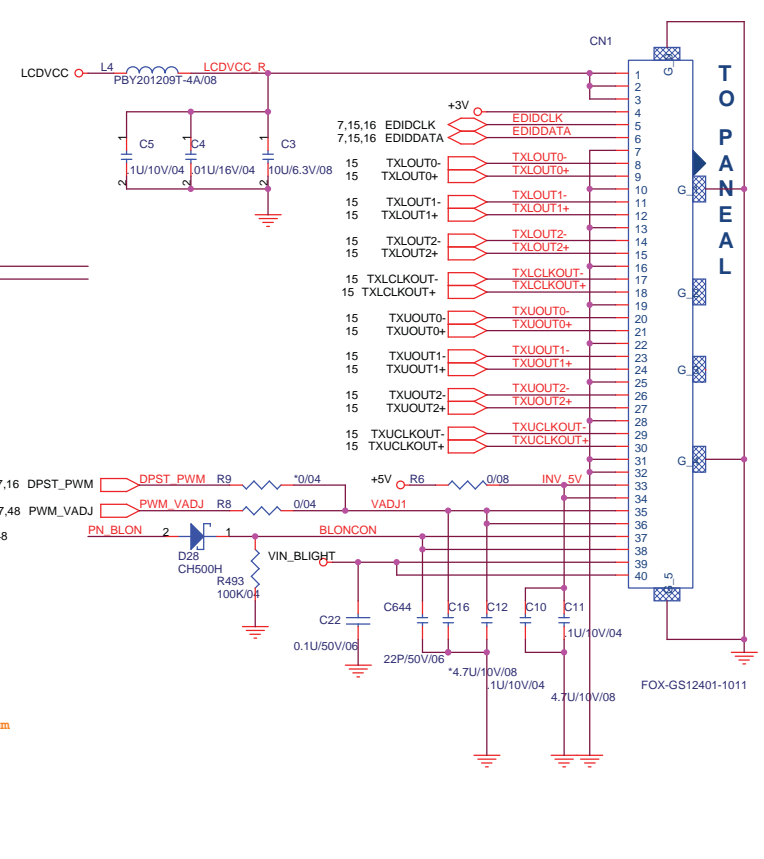
Size Custom	Document Number ICH7-M POWER(4/4)	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 24 of 48

CRT PORT

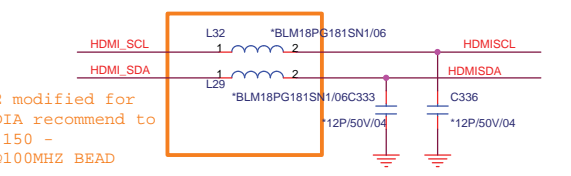




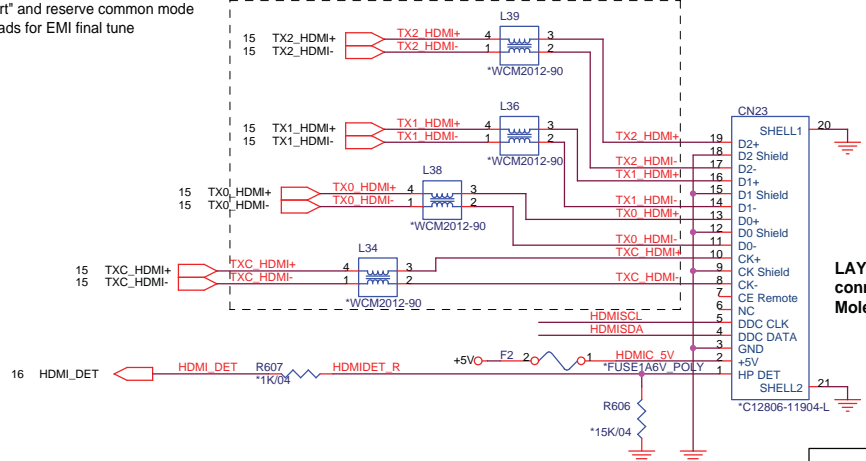
SI-2 change to 2k from Nvidia recommend



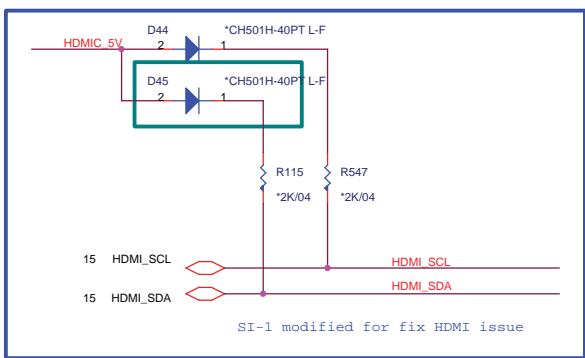
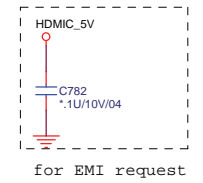
SI-1 modify footprint



DB "short" and reserve common mode choke pads for EMI final tune



HDMI PORT

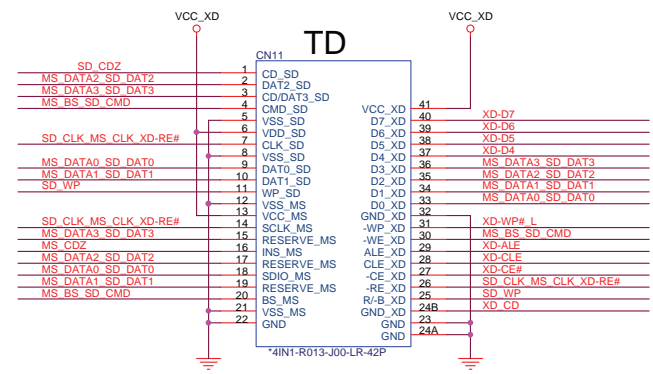
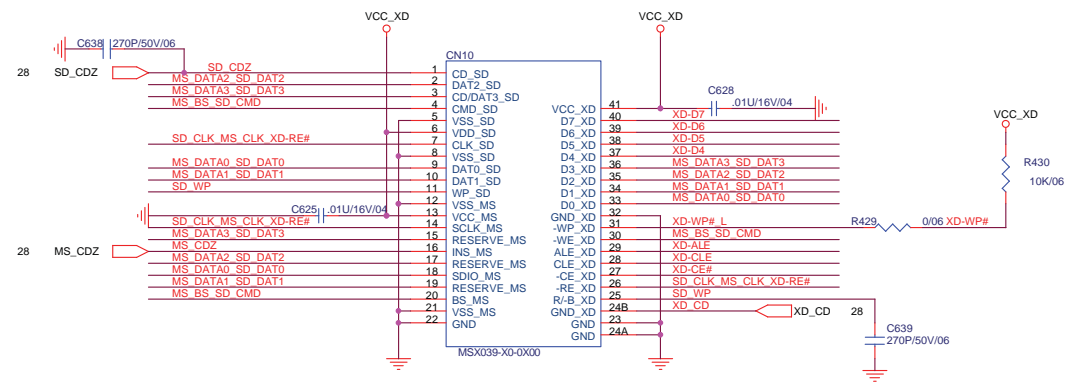


SI-1 modified for fix HDMI issue

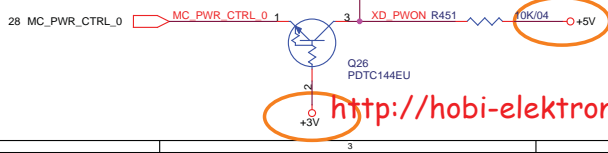
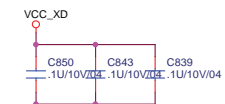
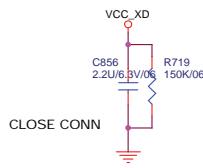
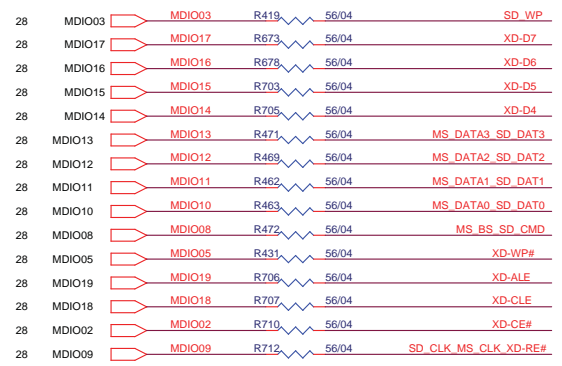
PROJECT : AT3
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/HDMI CONN	Rev 1A
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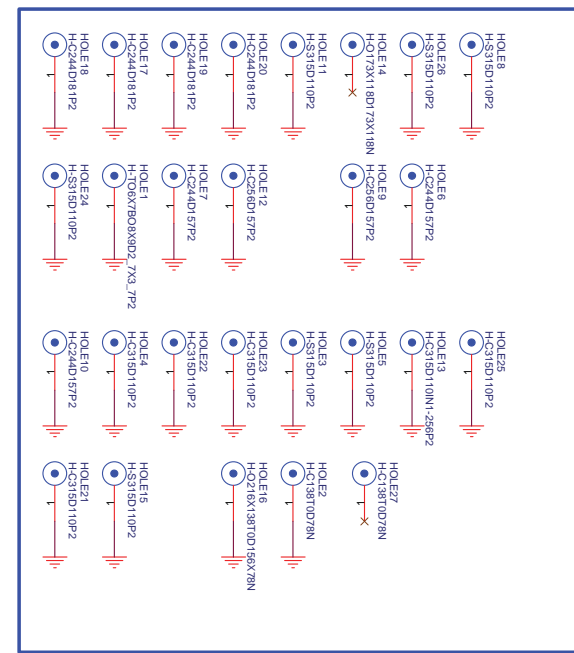
5 IN1 CARD READER XD, MMC/SD, MS/MSP



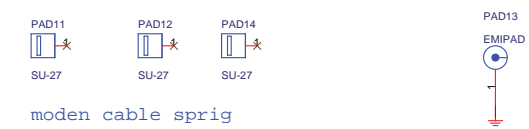
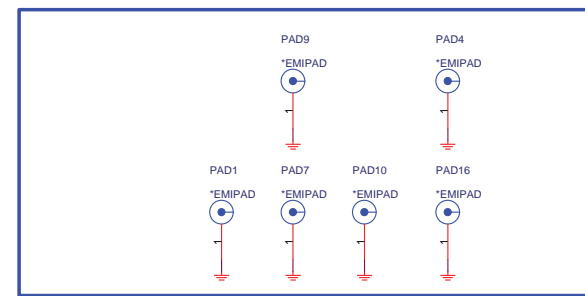
bom create 2'nd source



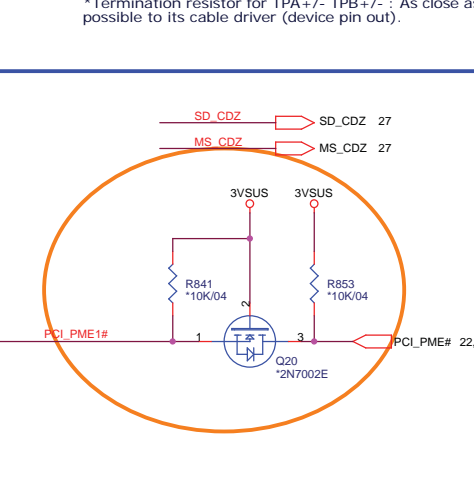
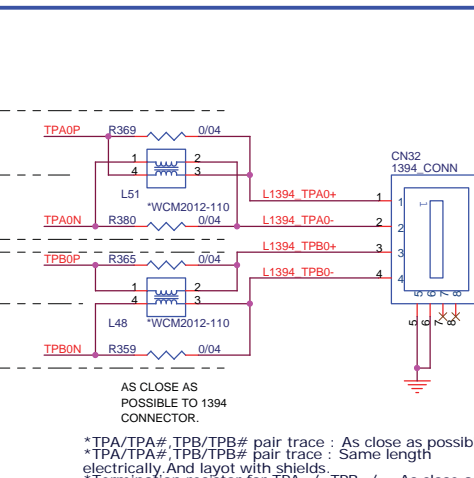
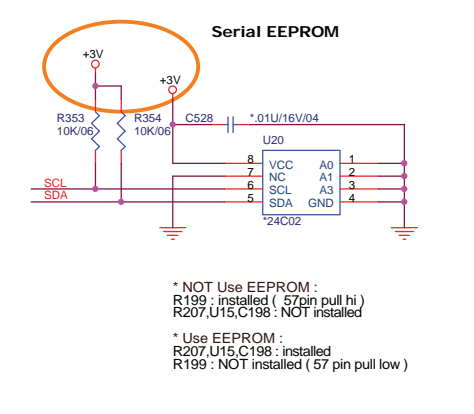
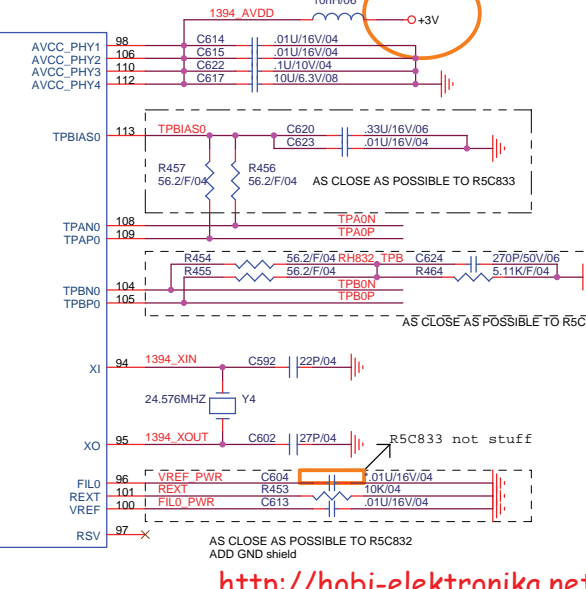
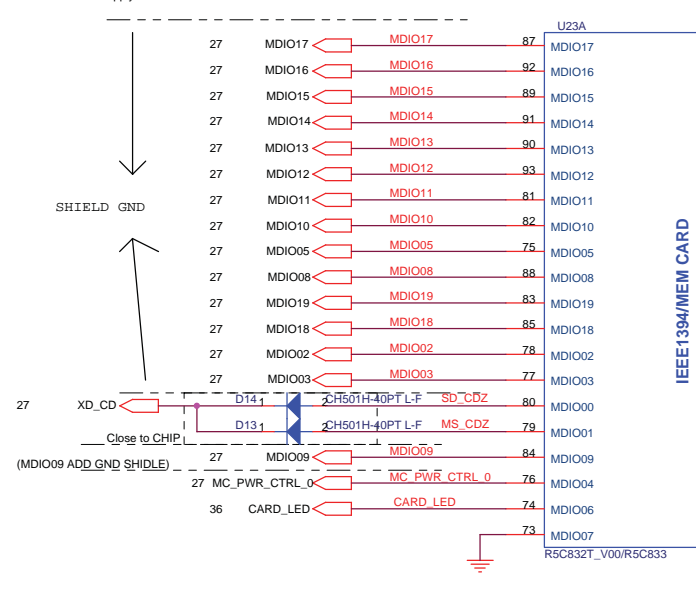
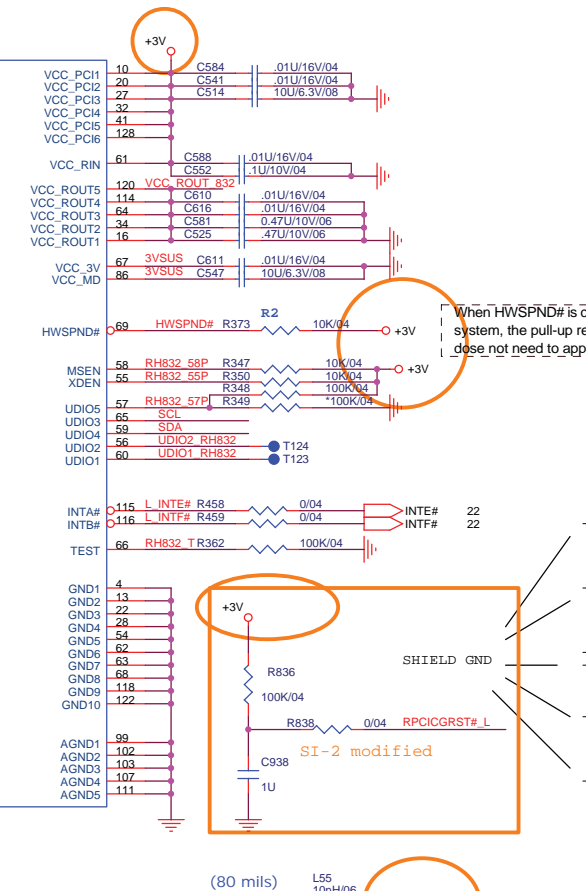
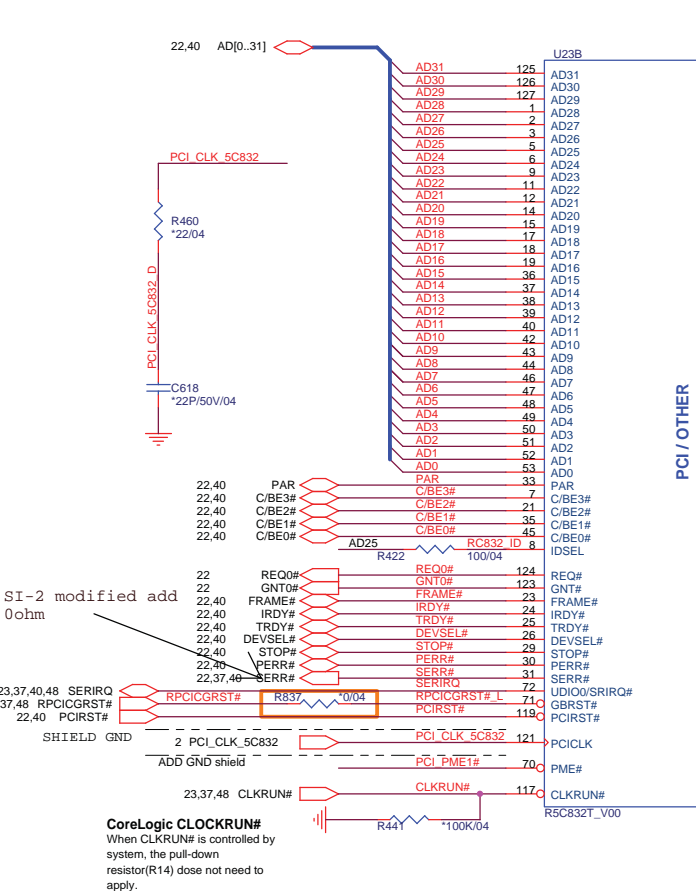
SCREW HOLE



EMI PAD



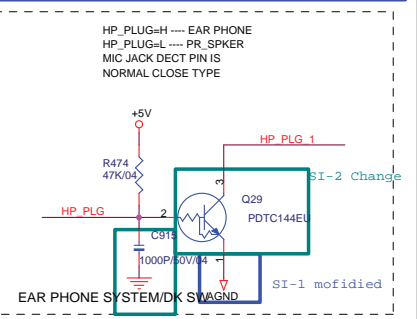
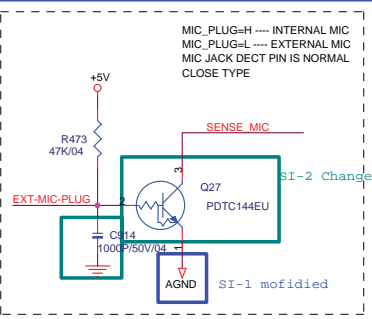
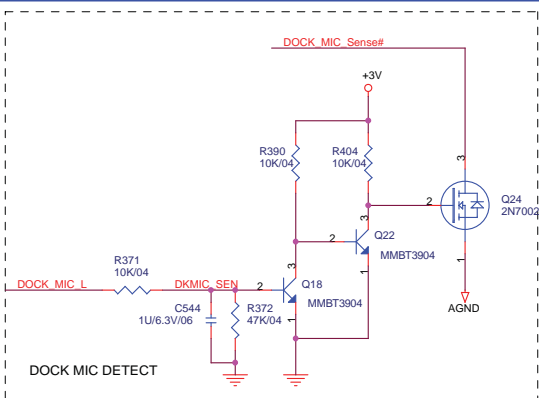
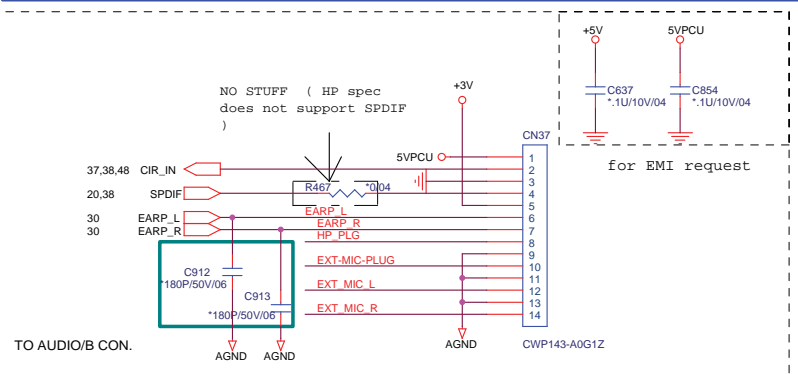
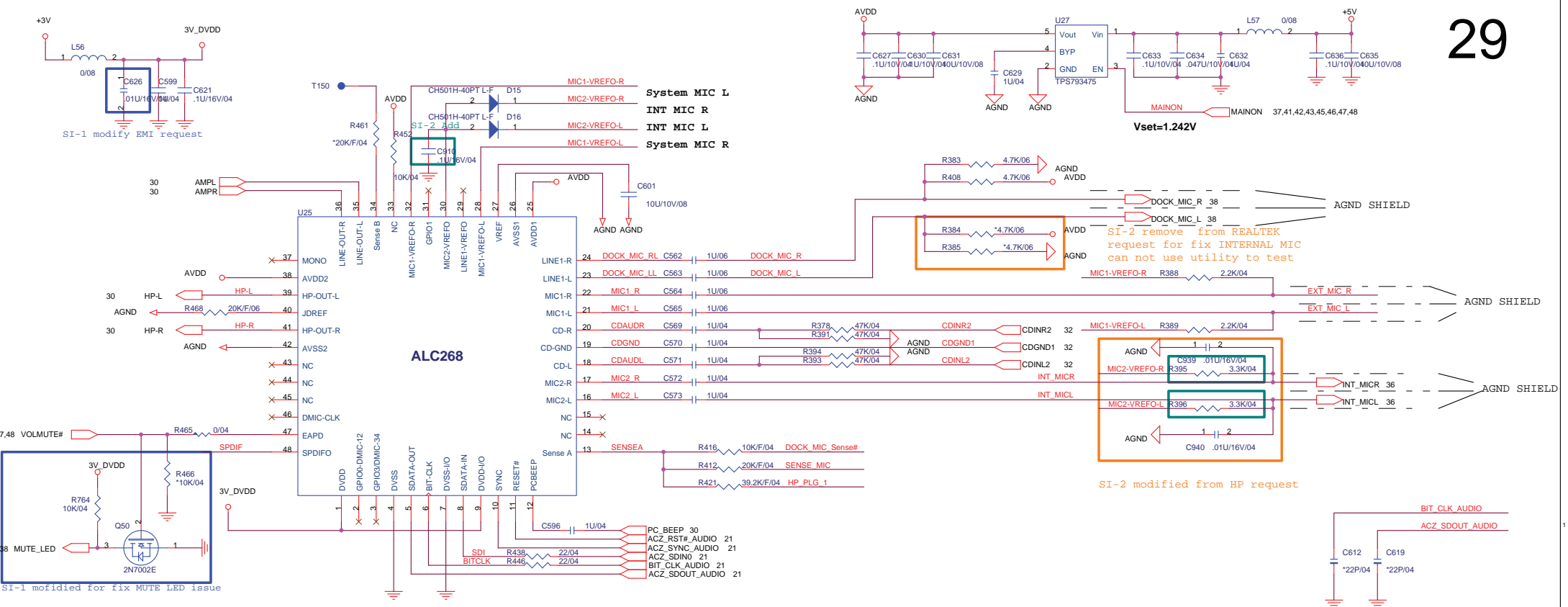
	PROJECT : AT3 Quanta Computer Inc.	
	Size Custom	Document Number CARD READER/HOLE
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NBS/RD1/HW2		Sheet 27 of 48




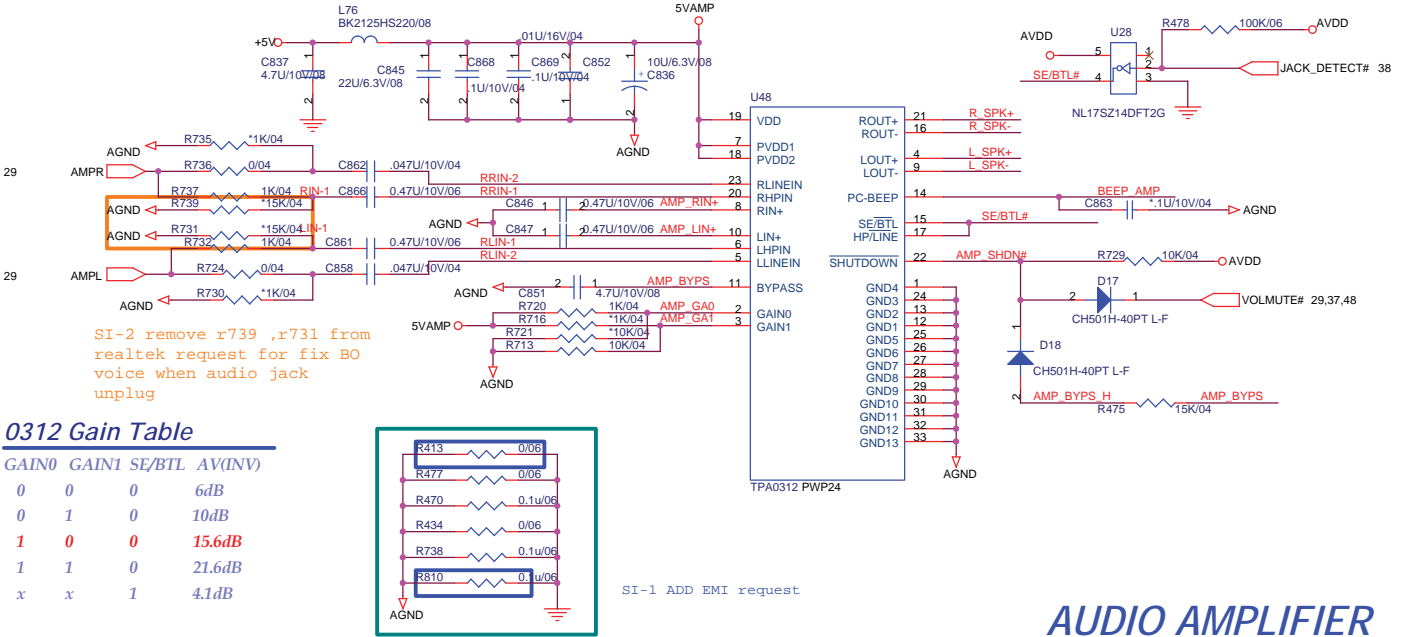
PROJECT : AT3
Quanta Computer Inc.

Size Custom	Document Number RICOH832 Controller	Rev 1A
Date: Tuesday, January 09, 2007		Sheet 28 of 48

NBS/RD1/HW2

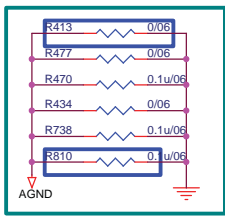


 NBS/RD1/HW2	PROJECT : AT3		Rev 1A
	Azalia CONEXANT20549-12		1A
	Date: Tuesday, January 09, 2007	Sheet 29 of 48	

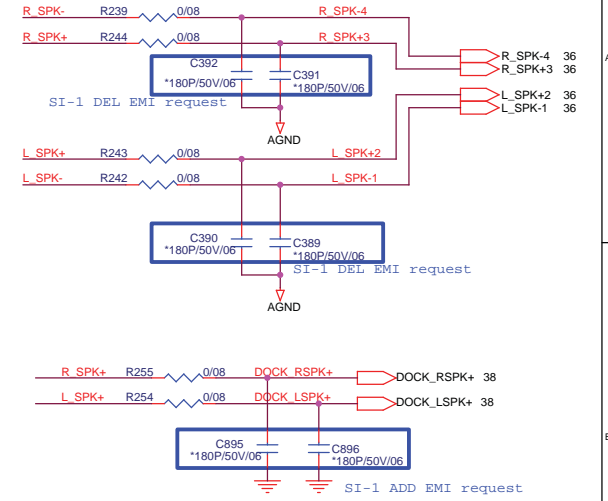


0312 Gain Table

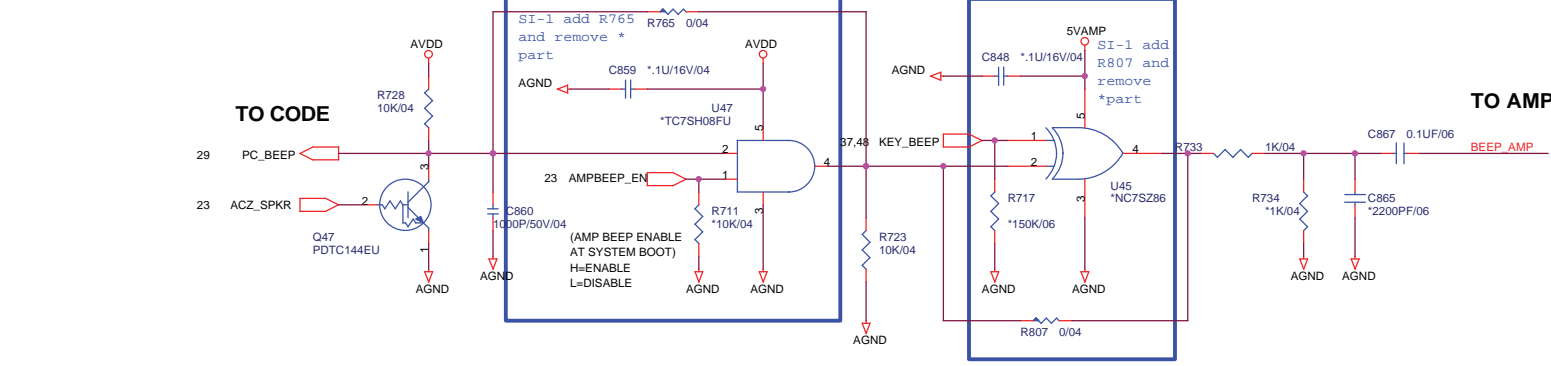
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



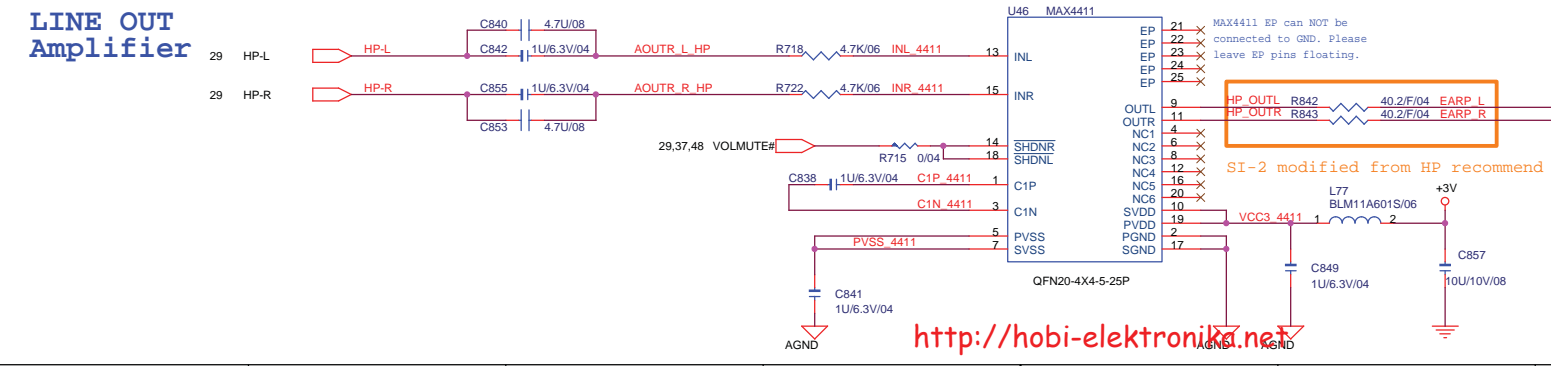
AUDIO AMPLIFIER



PCSPK BEEP



LINE OUT Amplifier

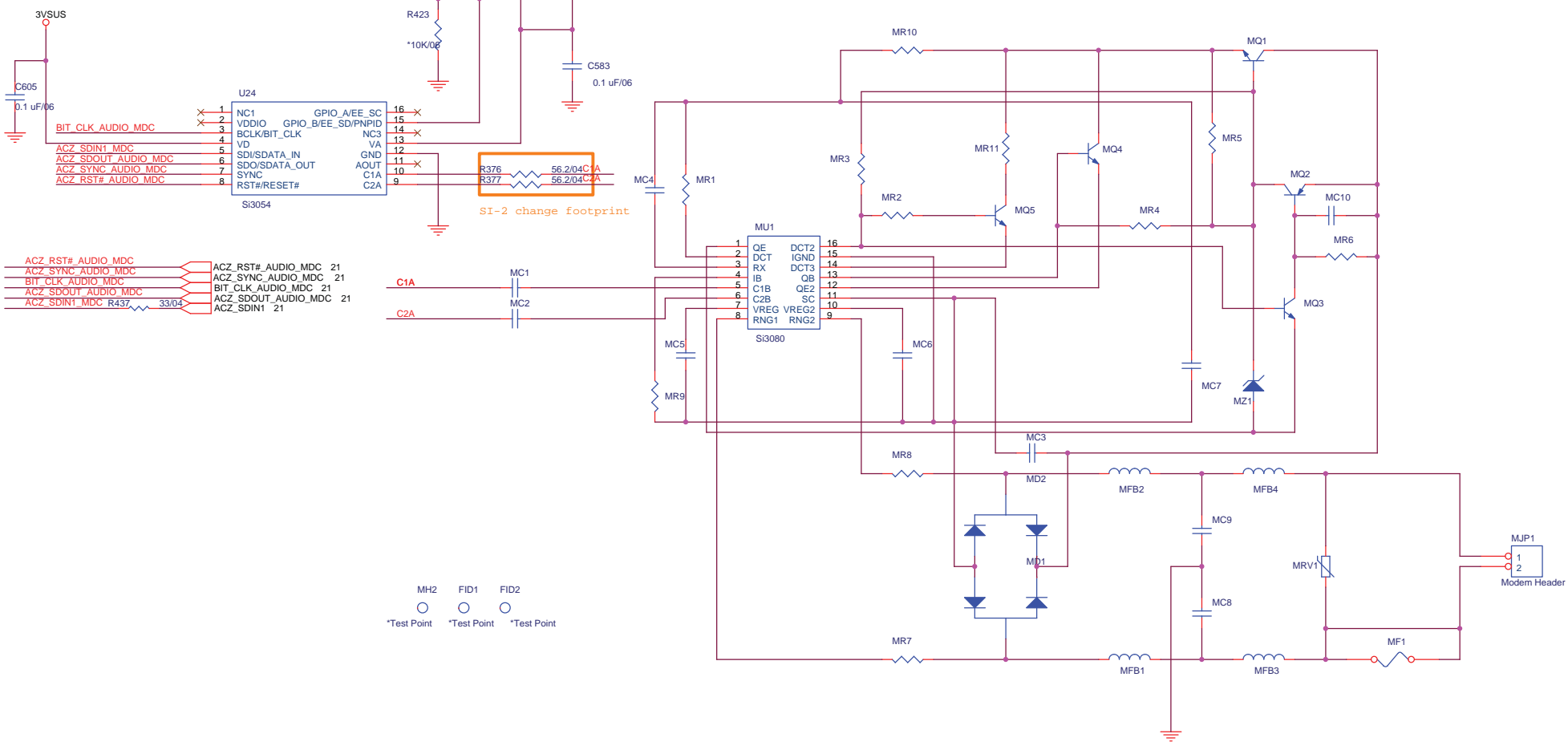


<http://hobi-elektronika.net>

PROJECT : AT3
Quanta Computer Inc.

Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
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No Ground Plane In DAA Section
Homologation Area



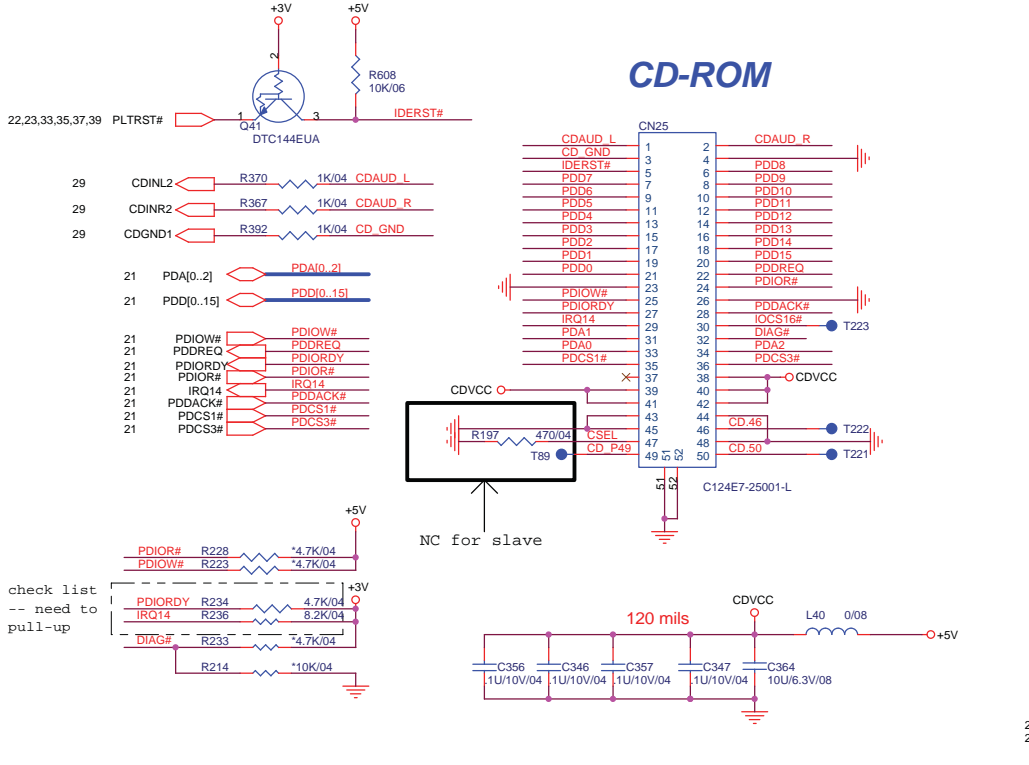
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

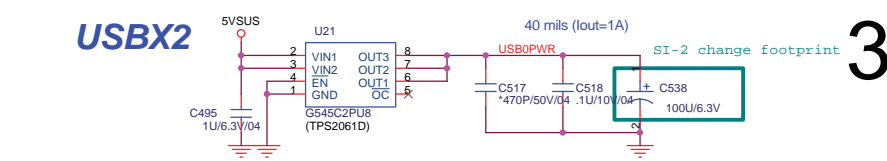
<http://hobi-elektronika.net>

	PROJECT : AT3 Quanta Computer Inc.	
	Size Custom NBS/RD1/HW2	Document Number MODEM(DAA)
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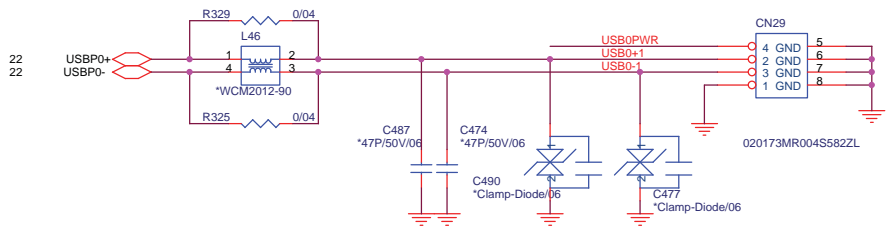
CD-ROM



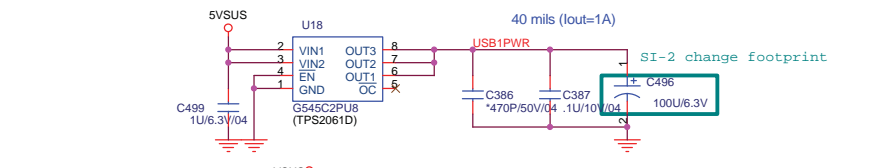
USBX2



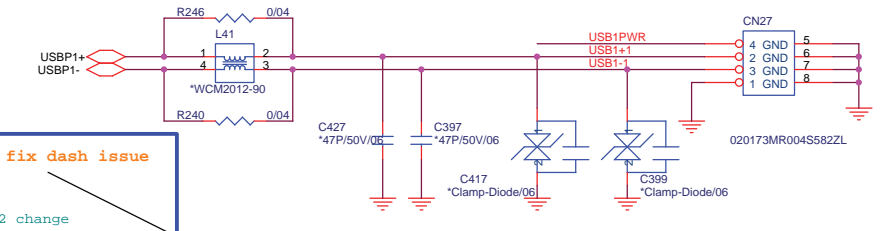
USB 0



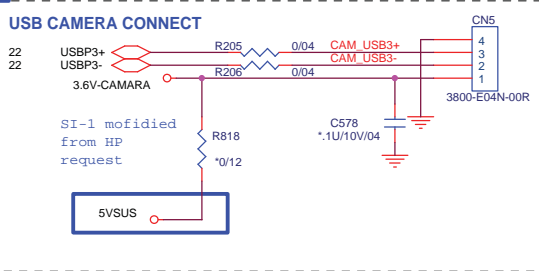
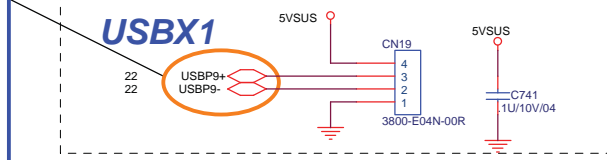
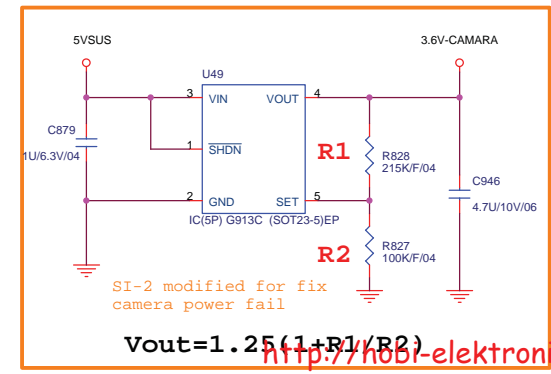
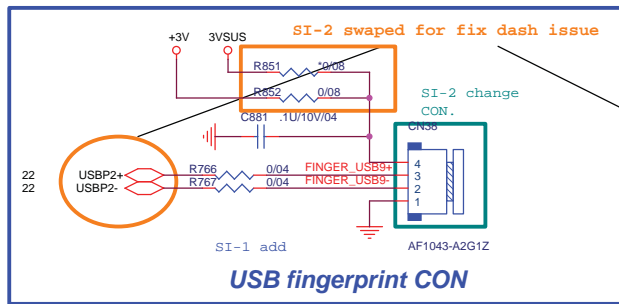
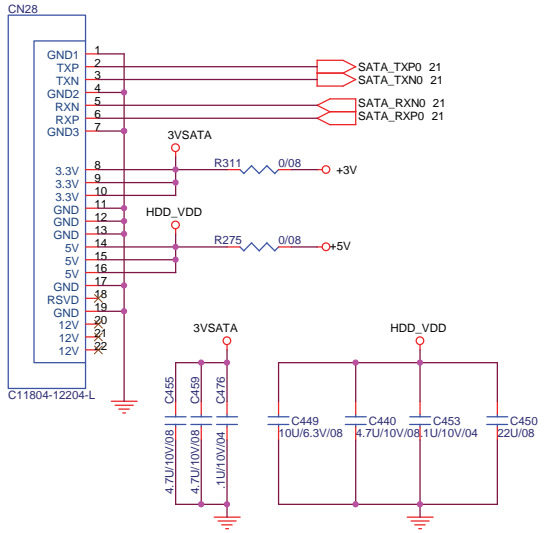
USBX1



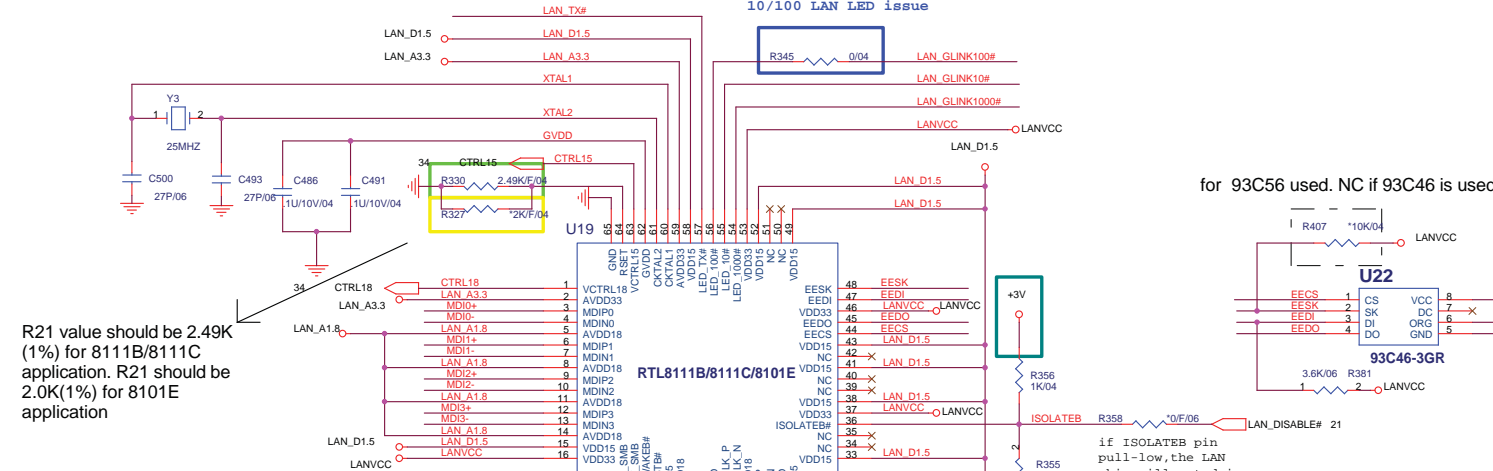
USB 1



SATA_1 CONNECTOR

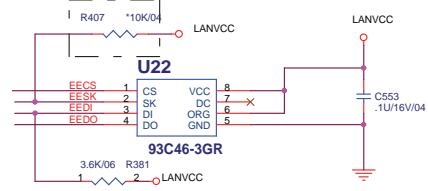


SI-1 BOM add to fix 10/100 LAN LED issue

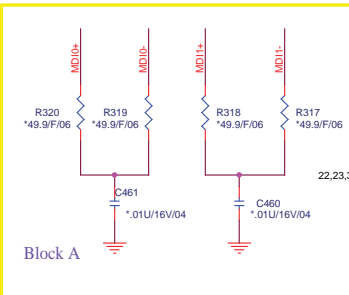


R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

for 93C56 used. NC if 93C46 is used.

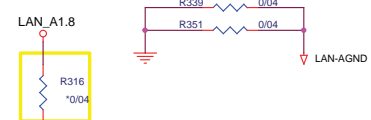


BLOCK A is only for RTL8101E application.

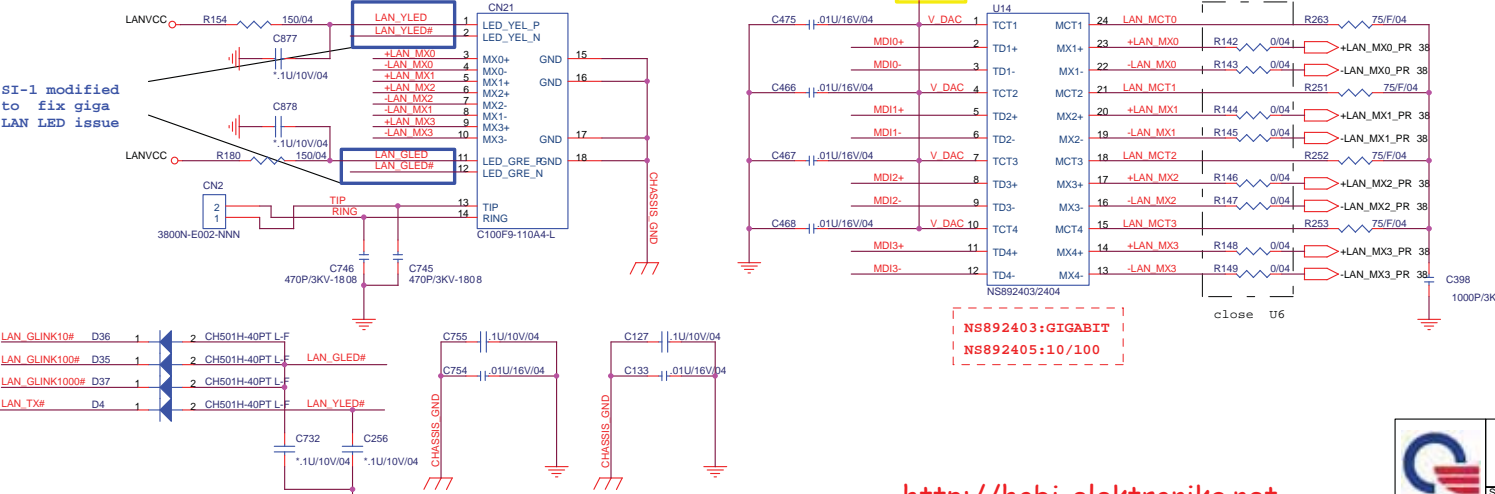


Block A

Remove R70 for 8111B and 8111C



RJ45



NS892403:GIGABIT
NS892405:10/100

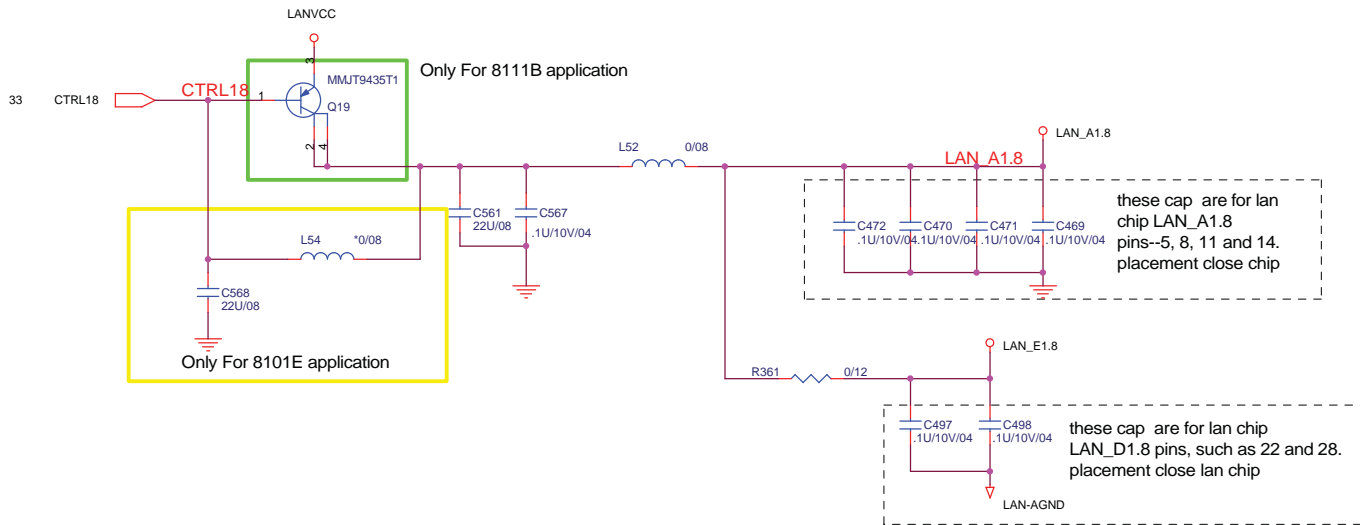
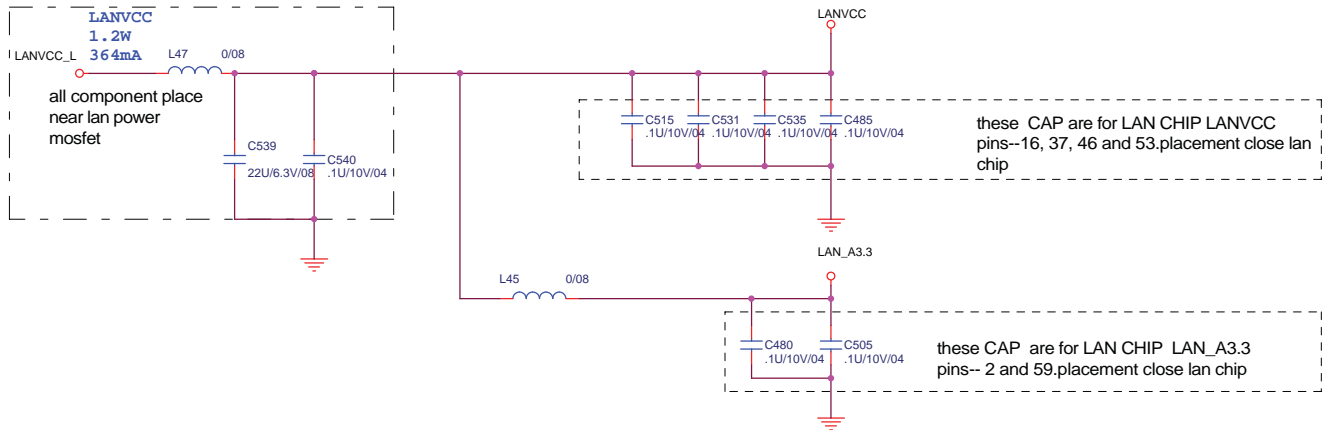
PROJECT : AT3
Quanta Computer Inc.

Size Custom	Document Number RTL8111B/8111C/8101E	Rev 1A
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NBS/RD1/HWZ

T : Stuffed for RTL8111B(10/100/1000)

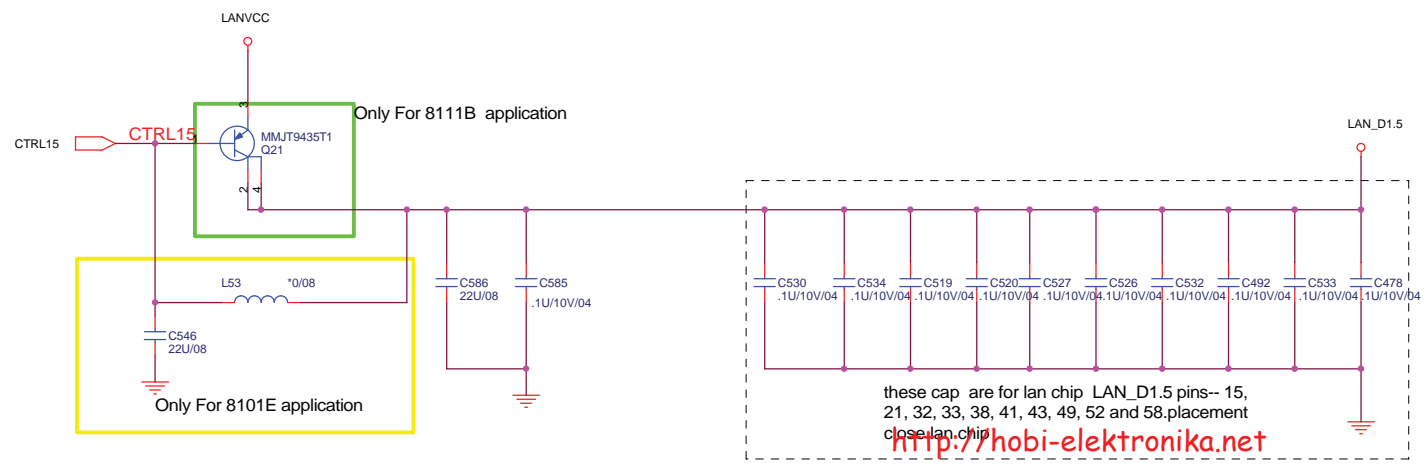
E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B/ RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A



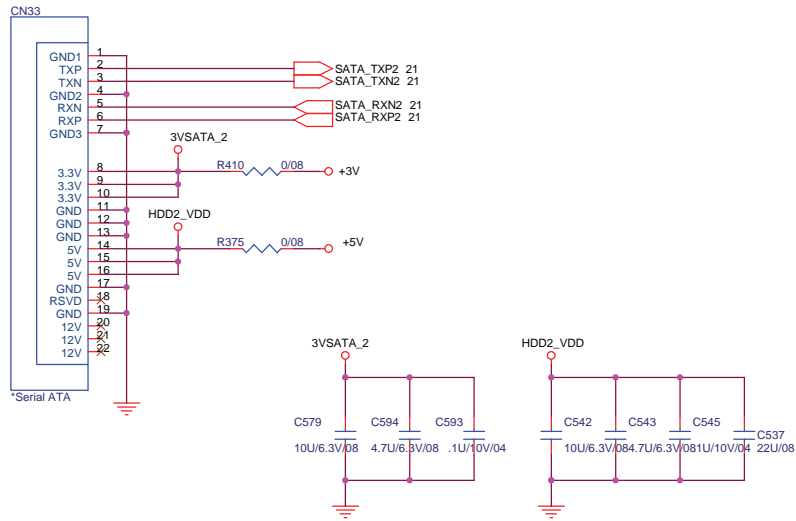
<http://hobi-elektronika.net>

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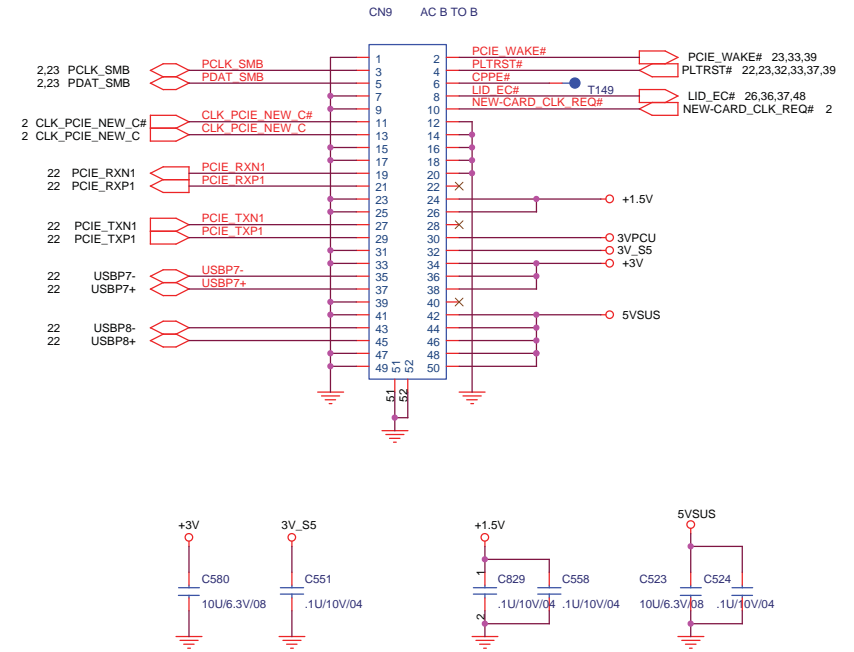
Size A3	Document Number LAN POWER	Rev 1A
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SATA_2 CONNECTOR

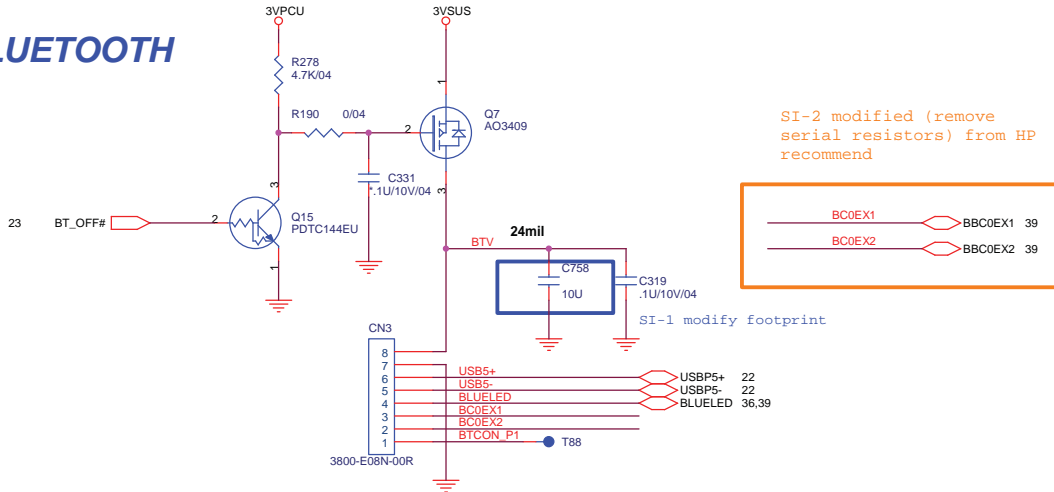
For 17"W Second HDD



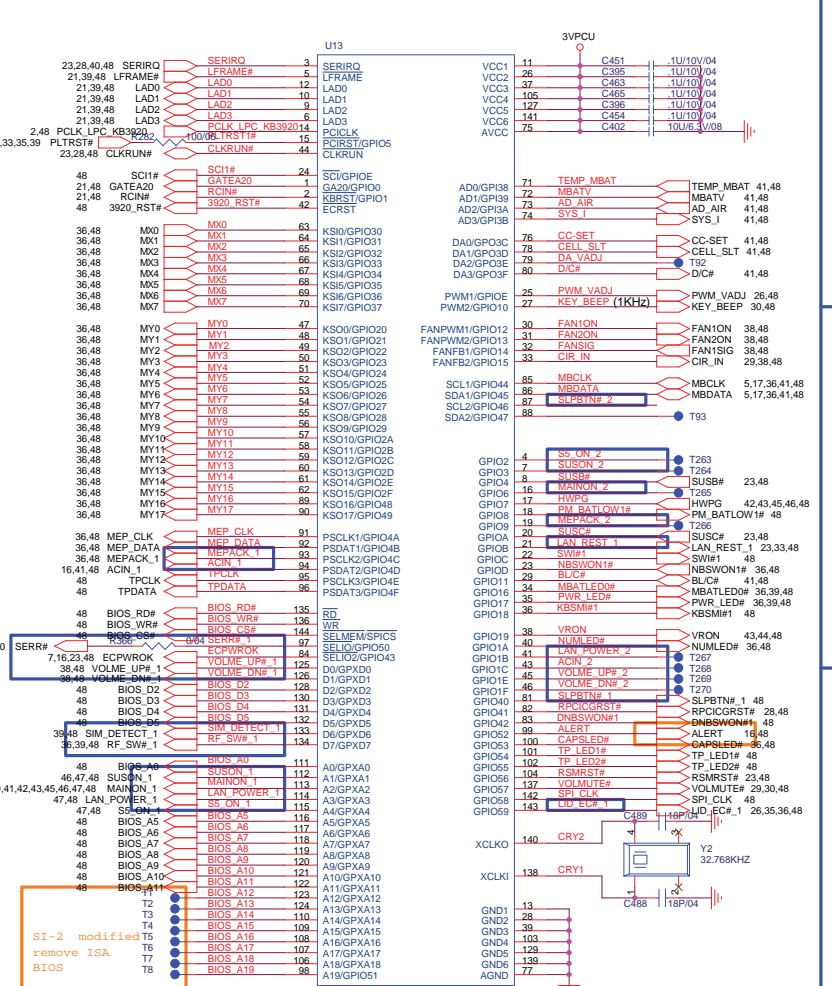
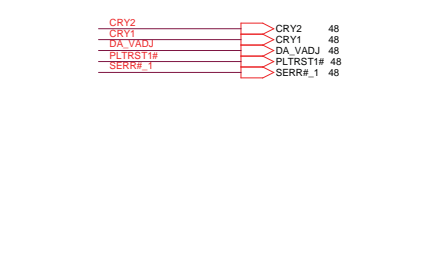
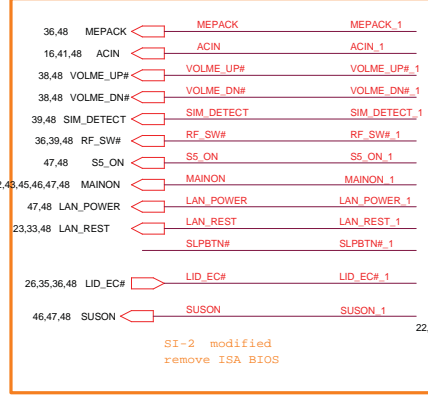
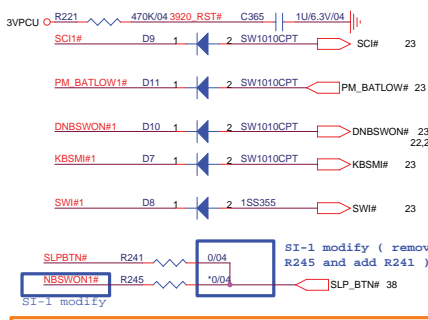
NEWCARD



BLUETOOTH

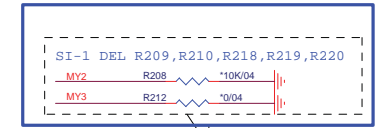


PROJECT : AT3 Quanta Computer Inc.		
Size Custom NBS/RD1/HW2	Document Number NEW CARD/BT	Rev 1A
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STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



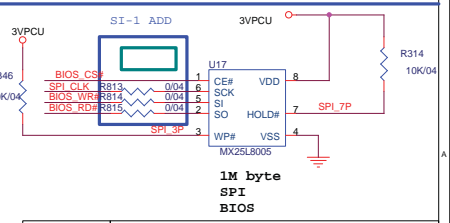
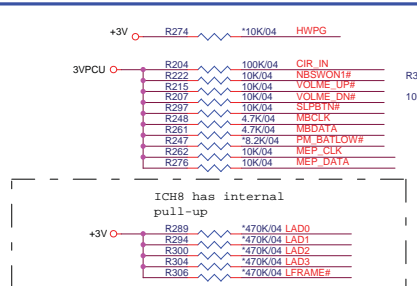
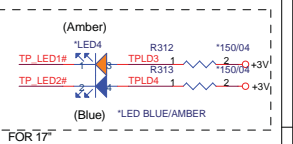
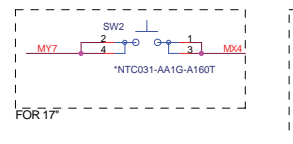
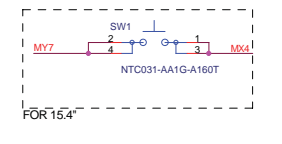
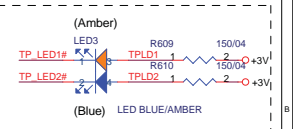
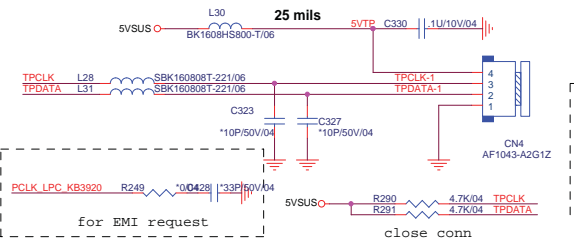
All hardware straps default internal pull-up, so don't need pull-up outside. A TEST need try --andrew ????

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified
remove ISA
BIOS

TOUCH PAD CONNECTOR



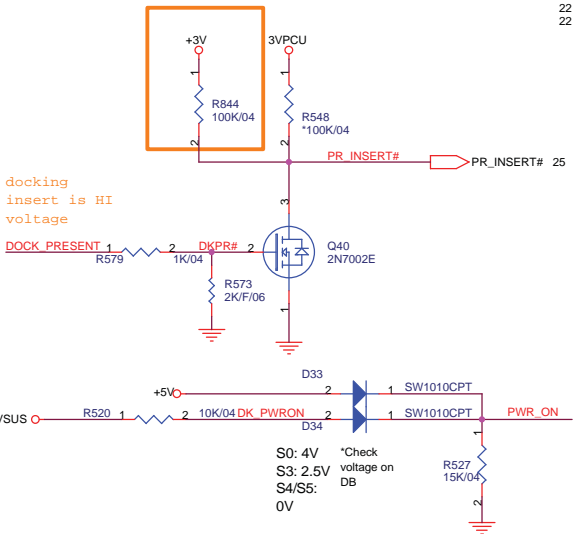
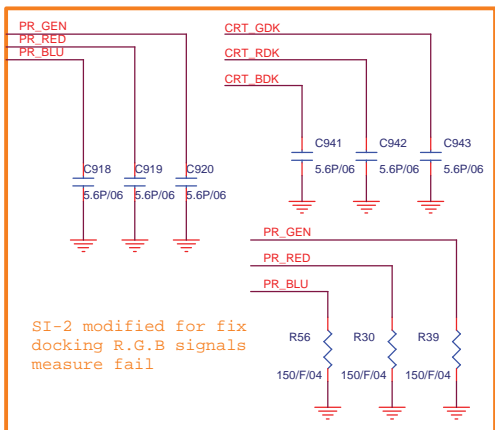
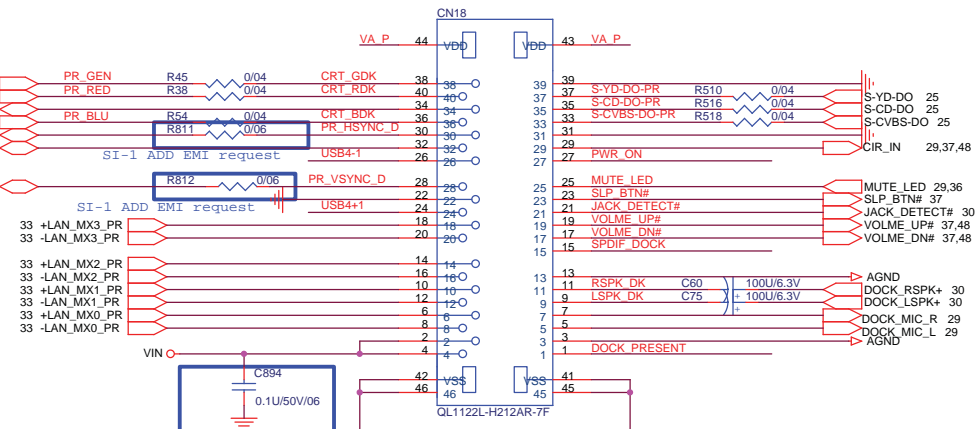
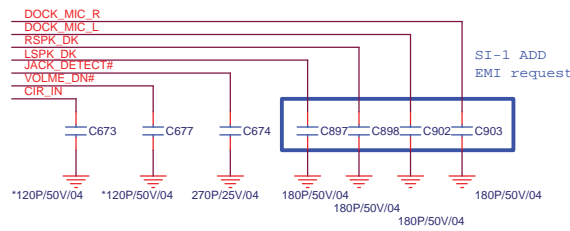
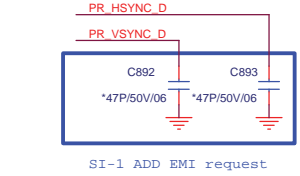
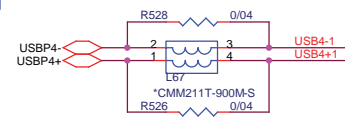
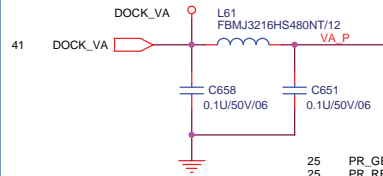
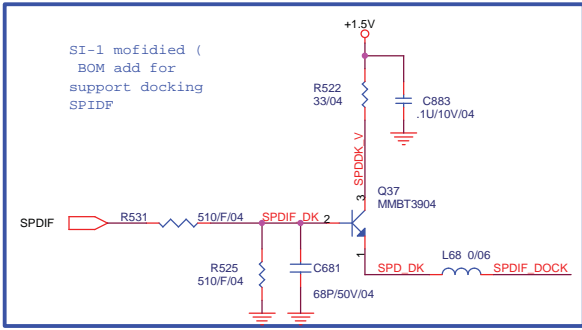
1M byte
SPI
BIOS

PROJECT : AT3
Quanta Computer Inc.

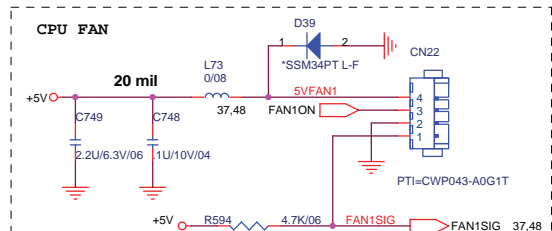
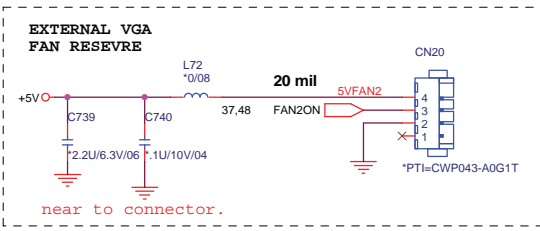
Size Custom	Document Number KB3920/ROM/TP	Rev 1A
Date: Tuesday, January 09, 2007	Sheet	37 of 48

CABLE DOCK

support 6A 200mils
CX000480005



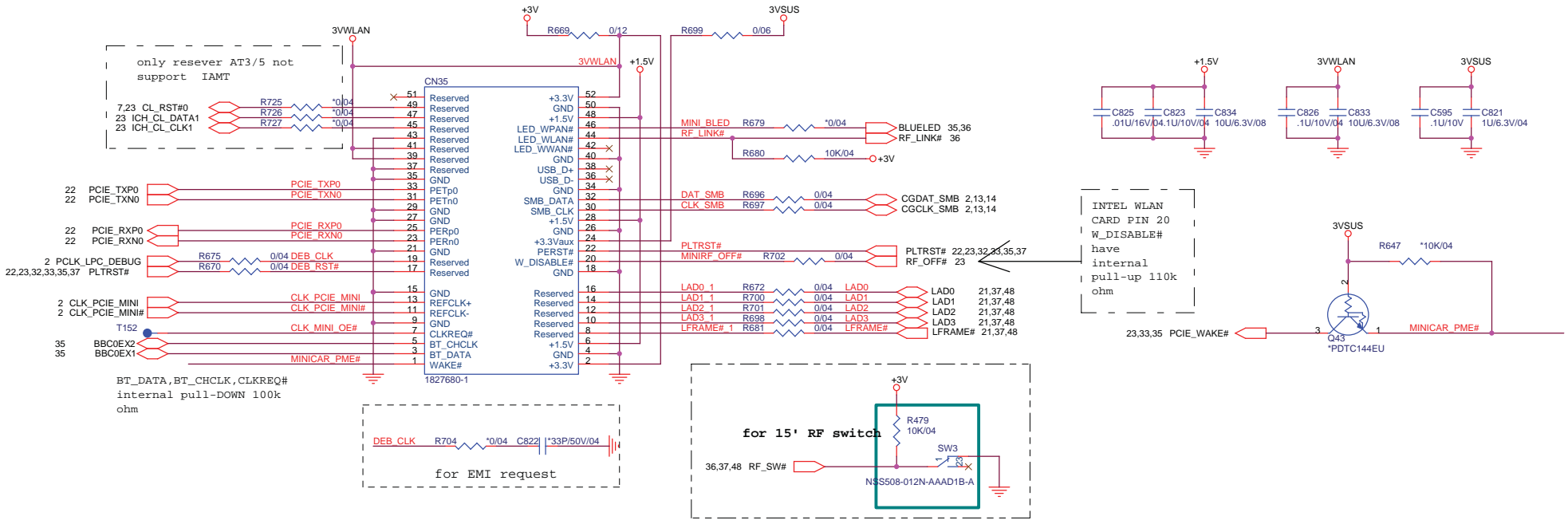
FAN



PROJECT : AT3
Quanta Computer Inc.

Size Custom	Document Number CABLE DOCKING/FAN	Rev 1A
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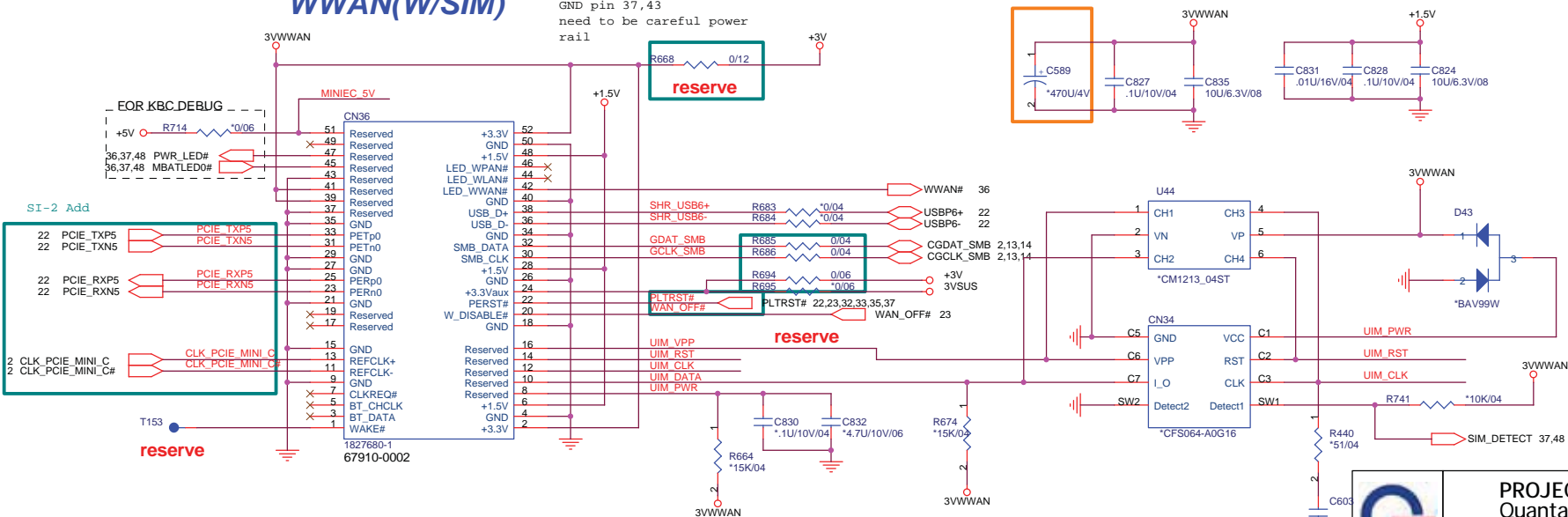
Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 WWAN(W/SIM)

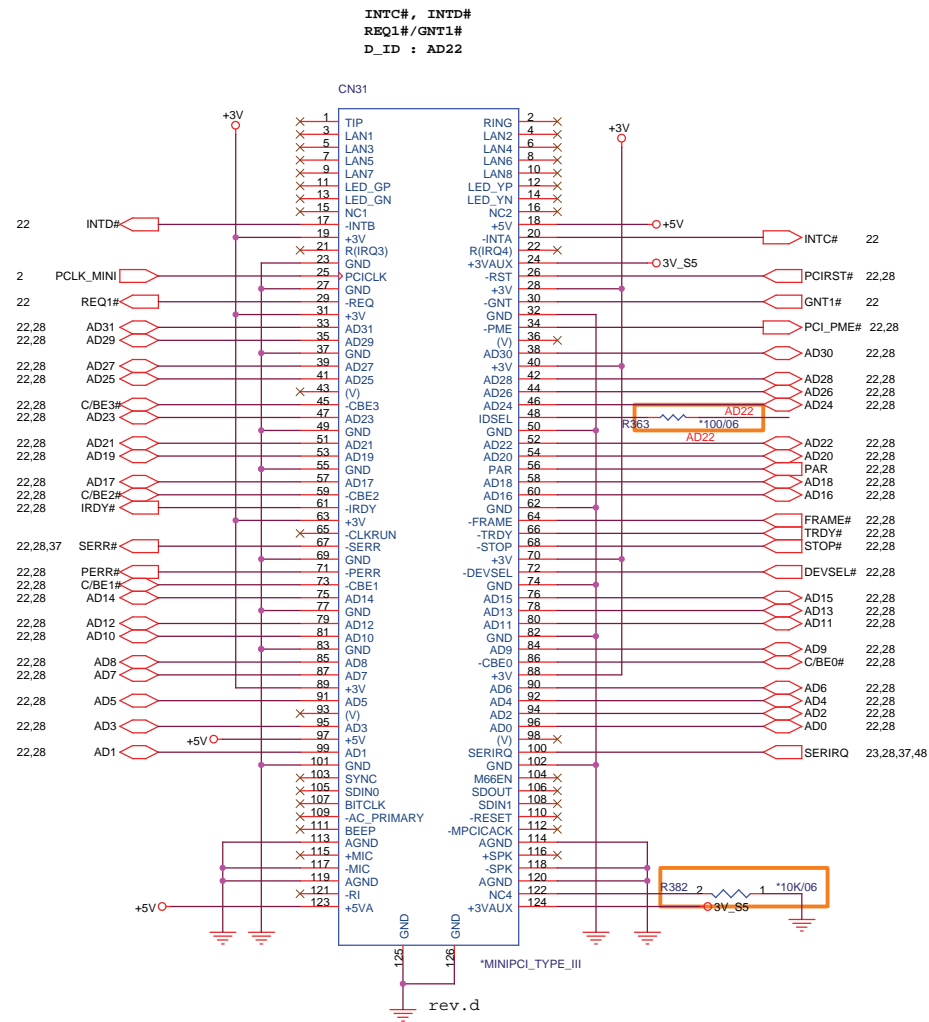
WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

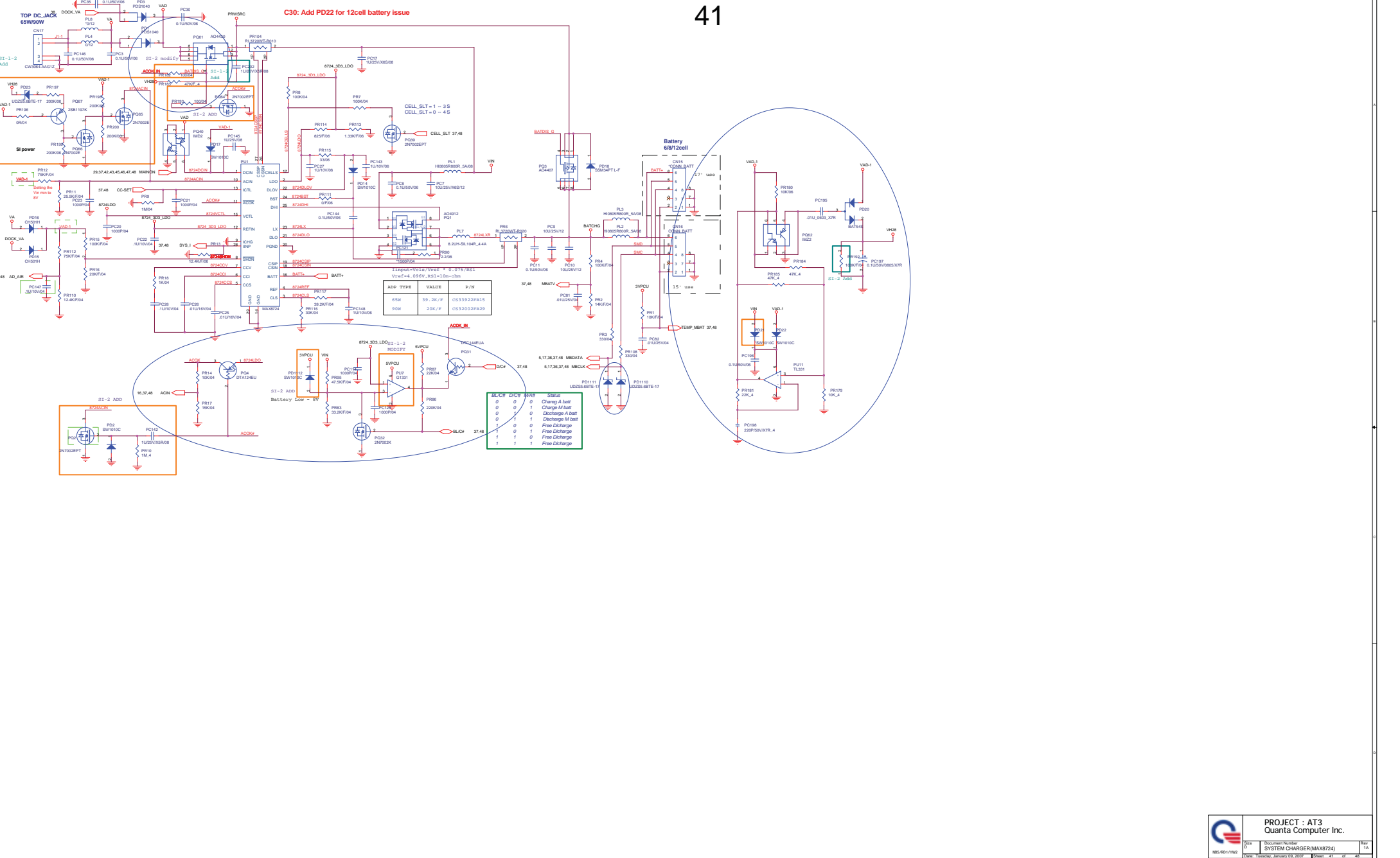
SI-2 modified
(BOM remove C589)



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MINI PCI TYPE III SLOT



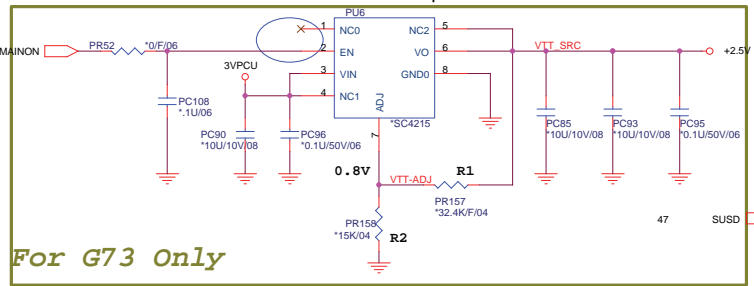


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

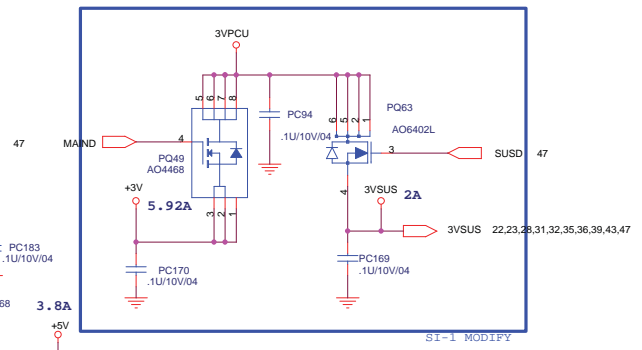
5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Max Power Consumption 1.6W



<http://hobi-elektronika.net>

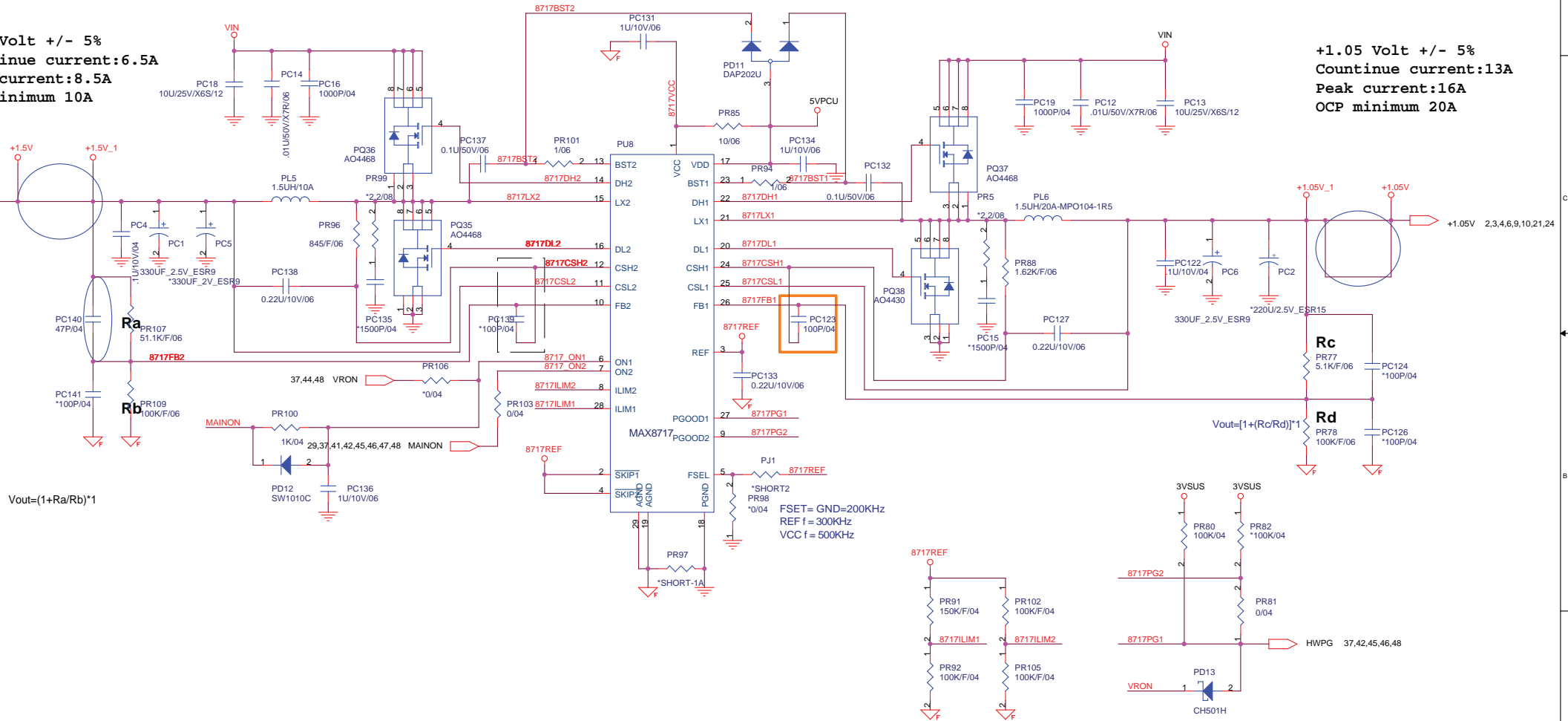


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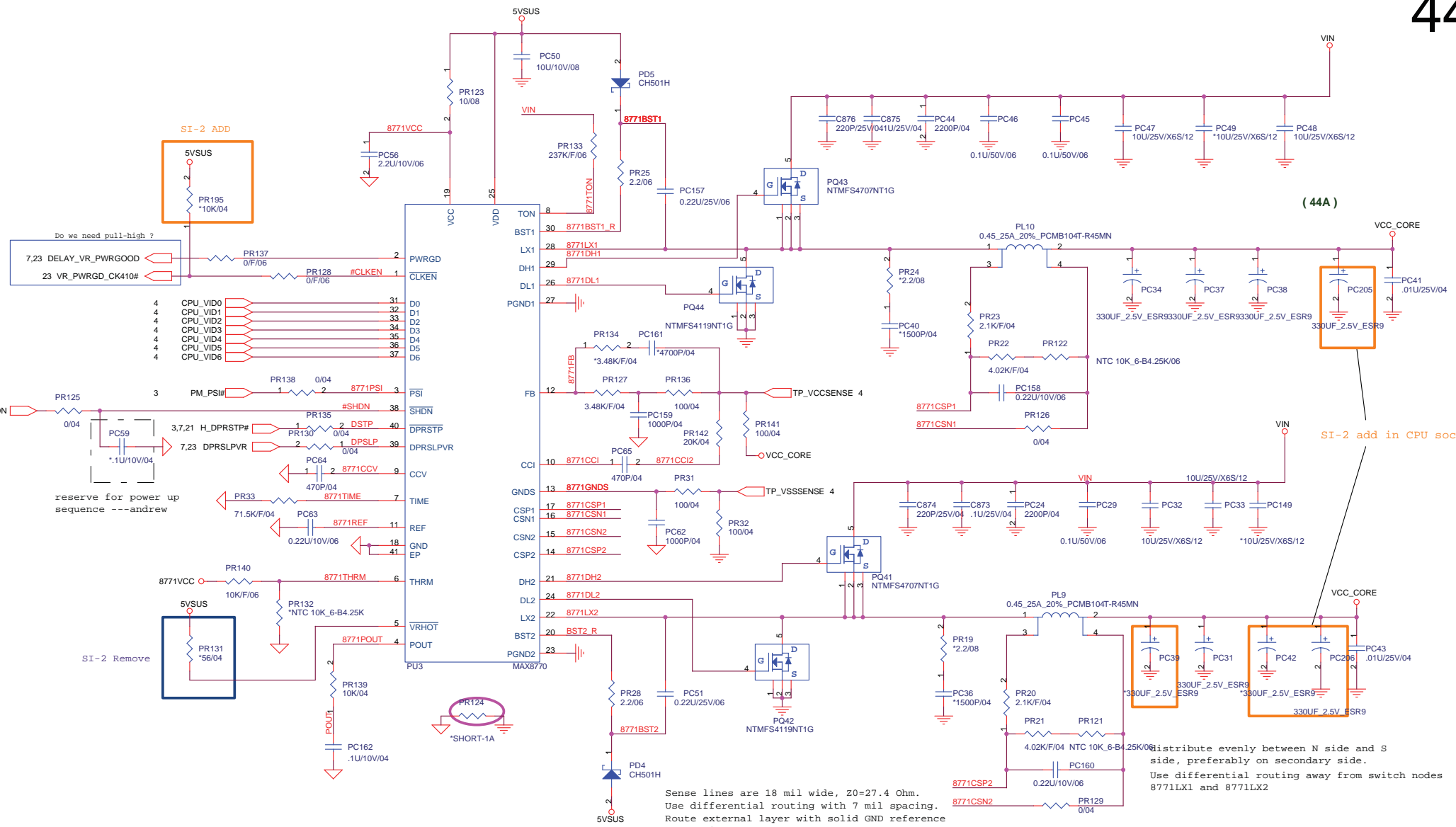
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



$V_{out} = (1 + R_a/R_b) * 1$

 NBS/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.		
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Sense lines are 18 mil wide, Z0=27.4 Ohm.
 Use differential routing with 7 mil spacing.
 Route external layer with solid GND reference
 (no split planes).
 Use 25 mil separation from any other signal.

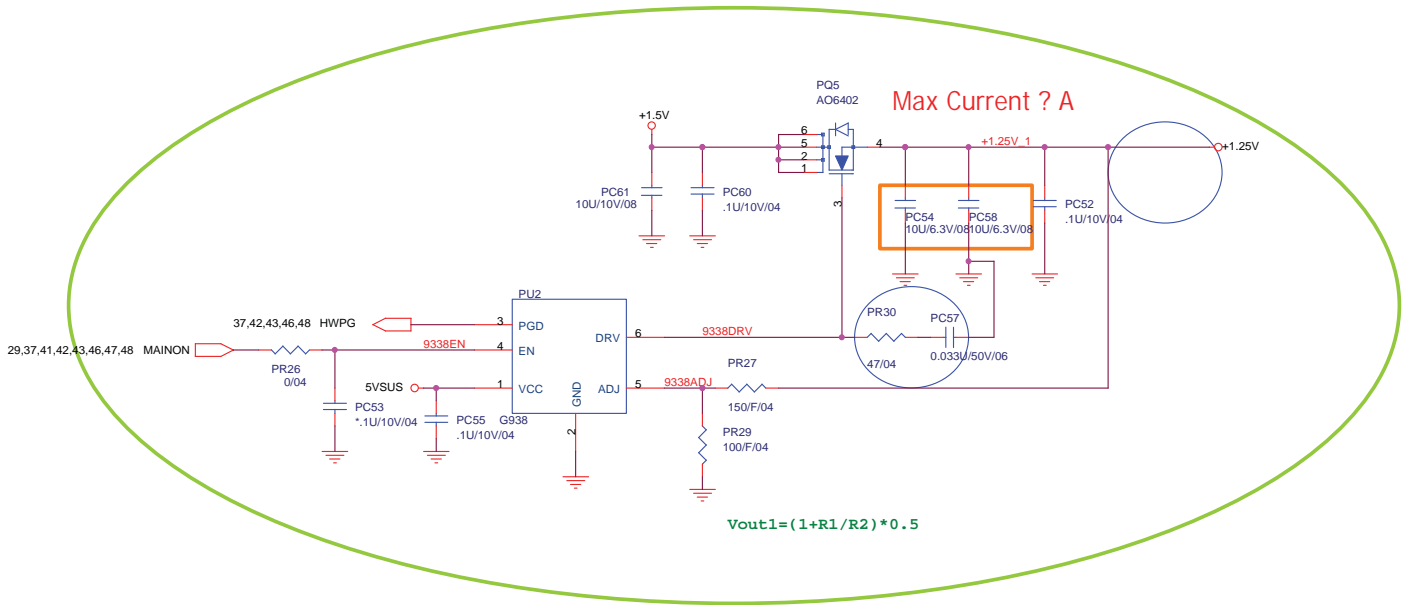
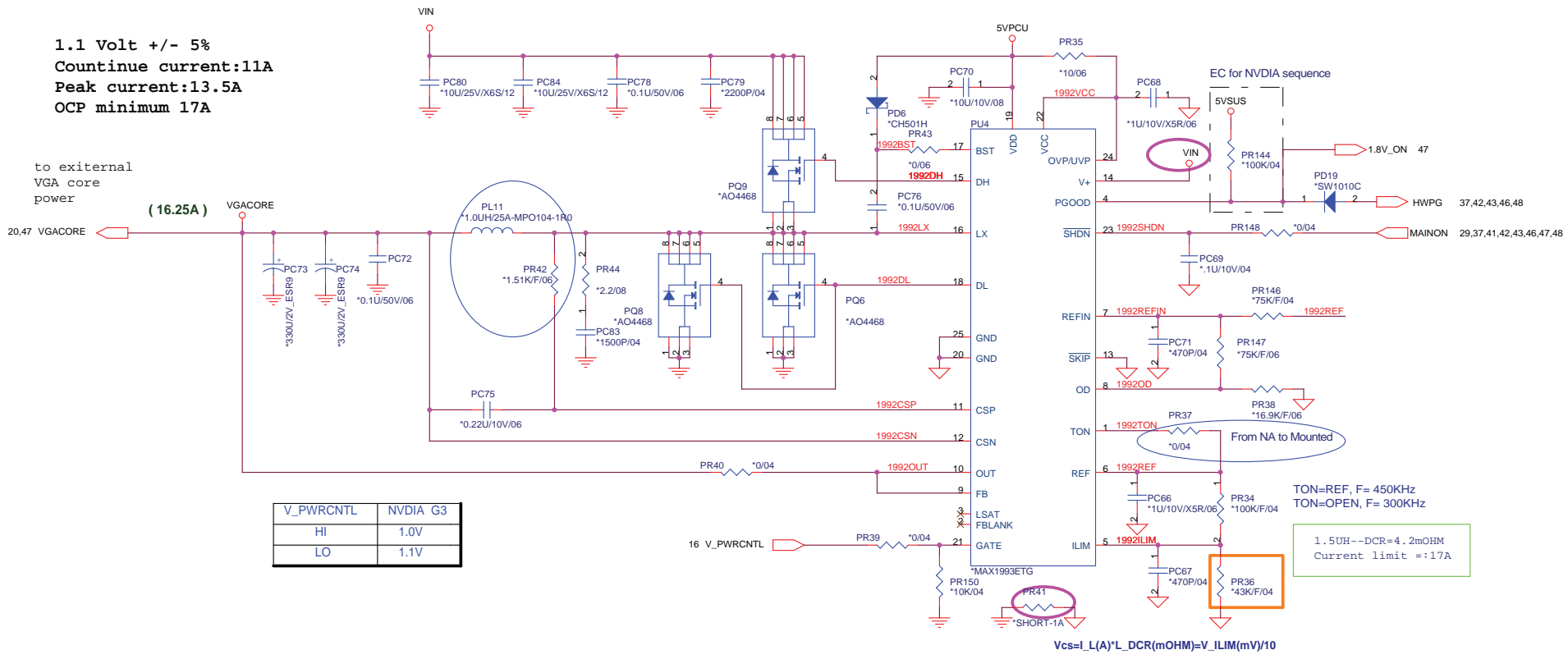
Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

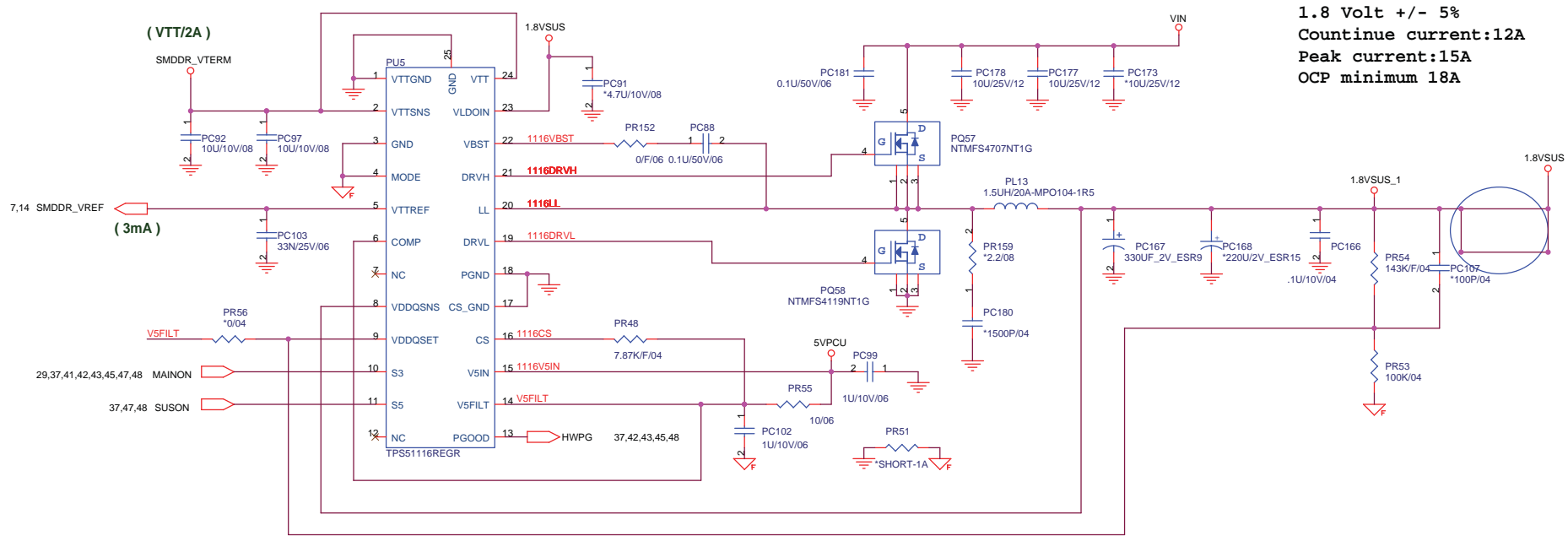
(44A)

SI-2 add in CPU socket

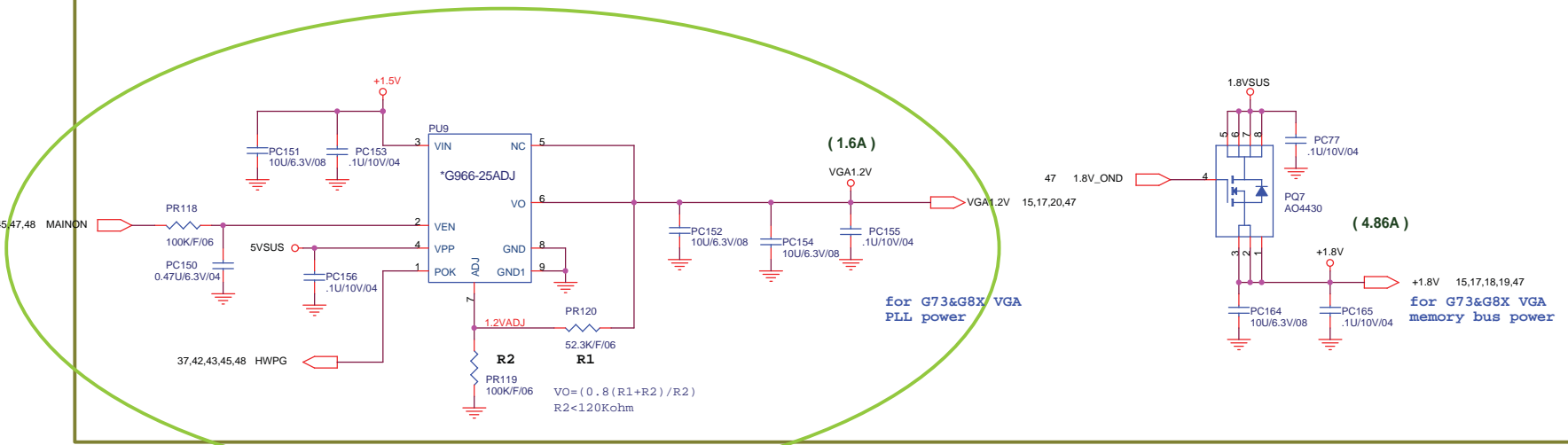
	PROJECT : AT3 Quanta Computer Inc.		
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1.1 Volt +/- 5%
 Countinue current:11A
 Peak current:13.5A
 OCP minimum 17A



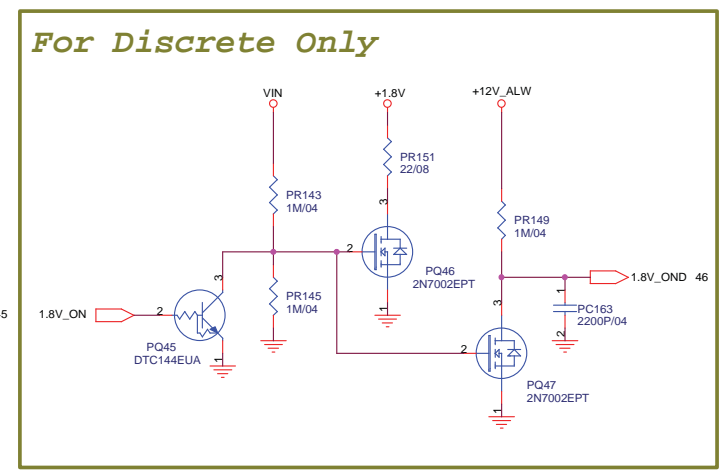
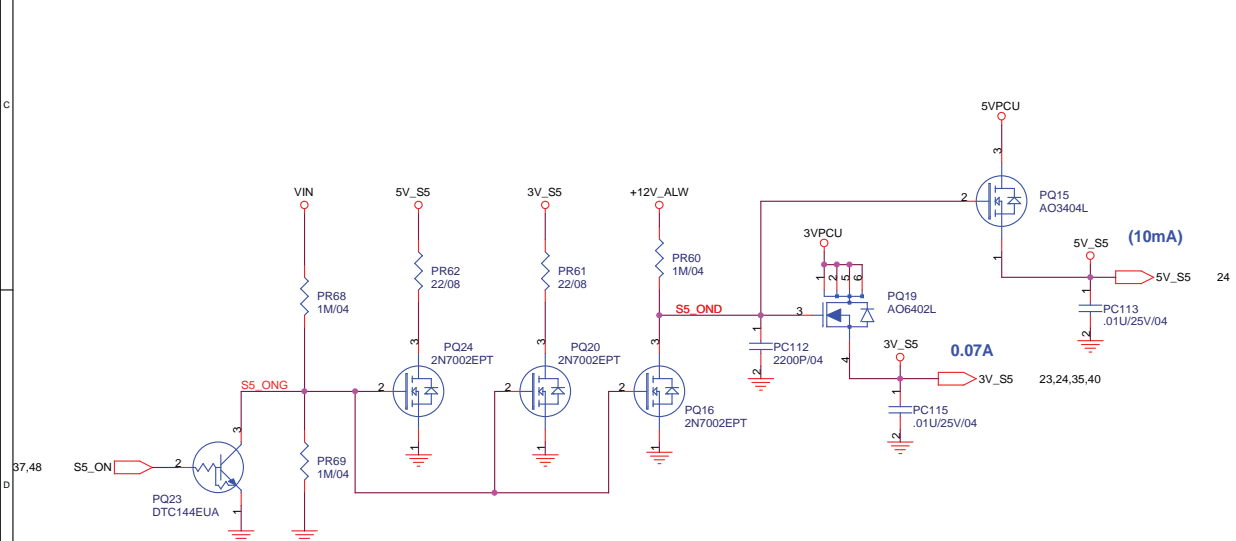
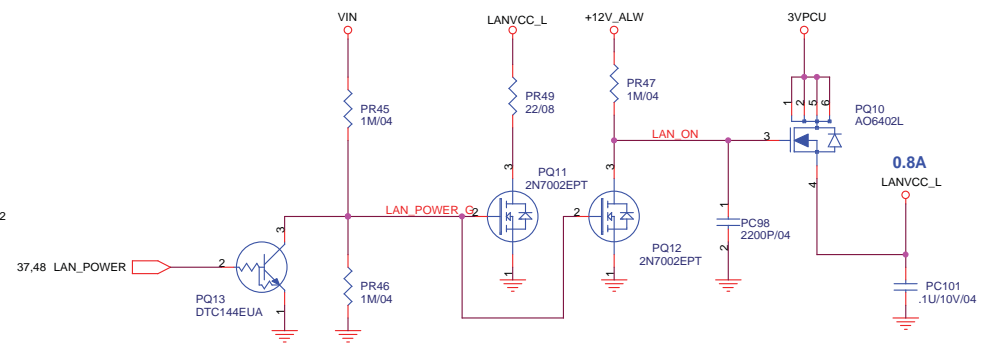
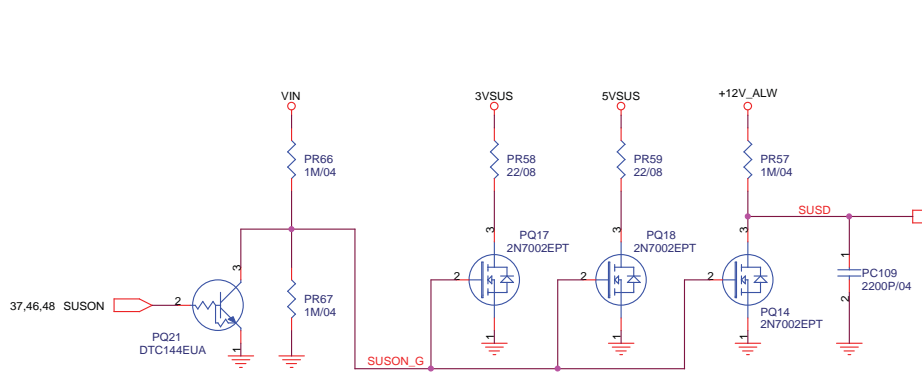
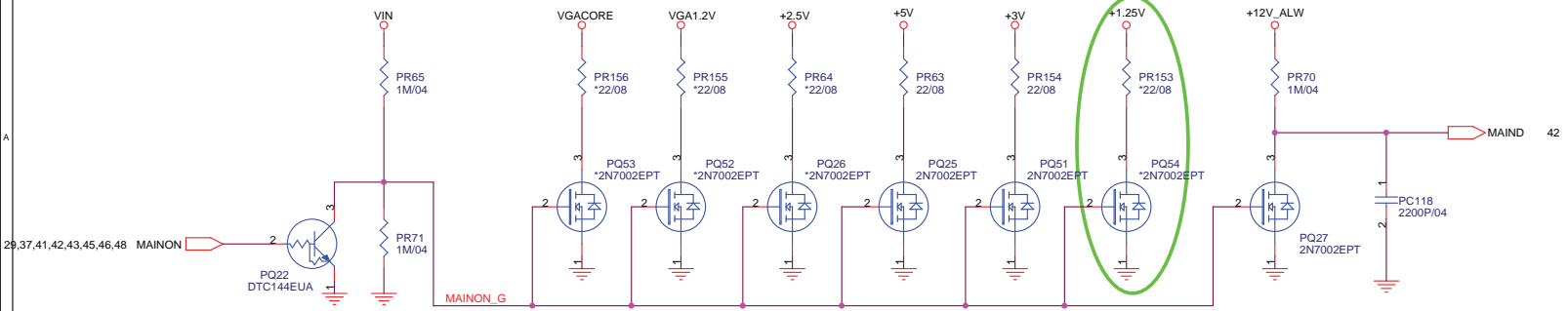



For Discrete Only

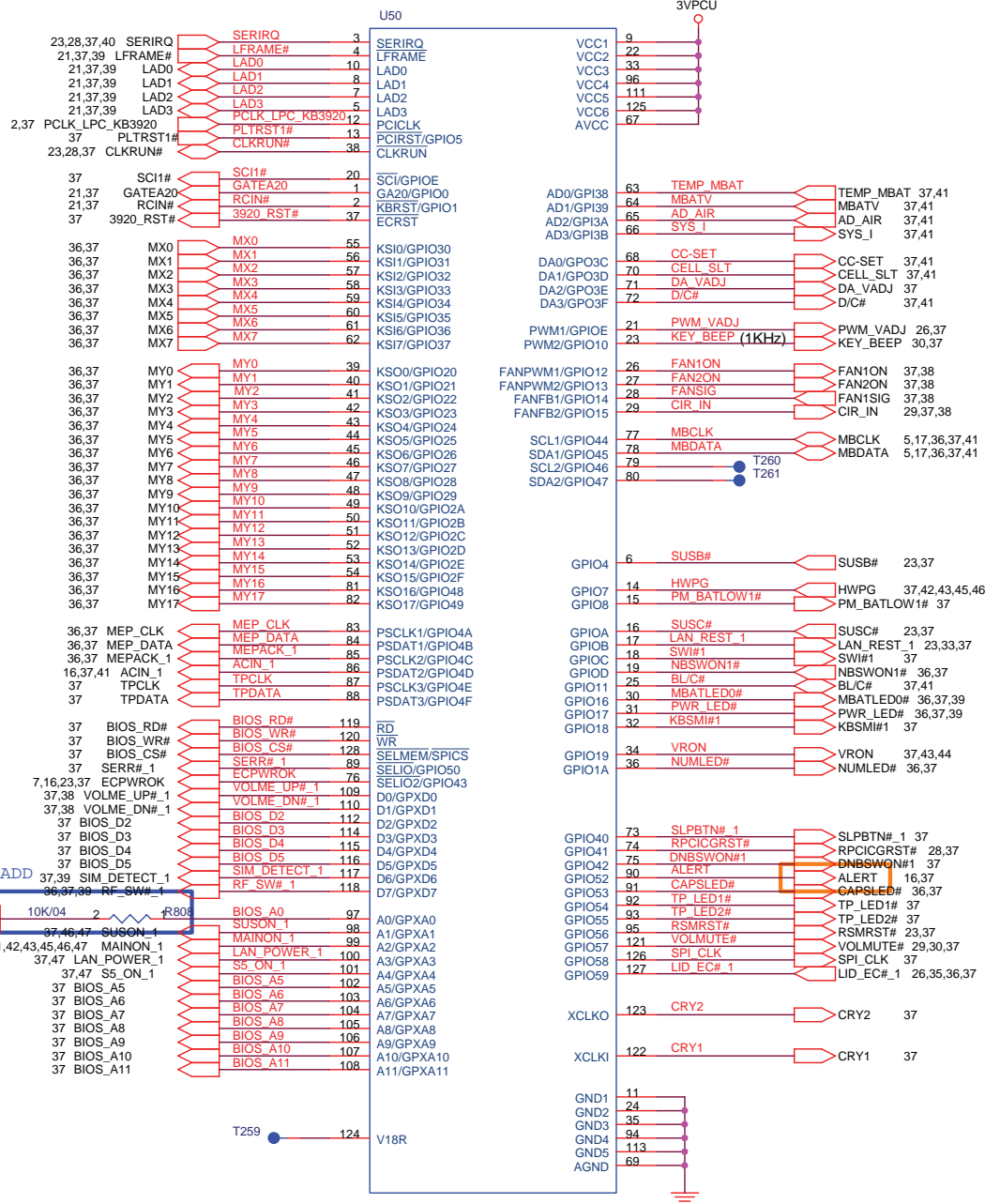


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KB3926

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