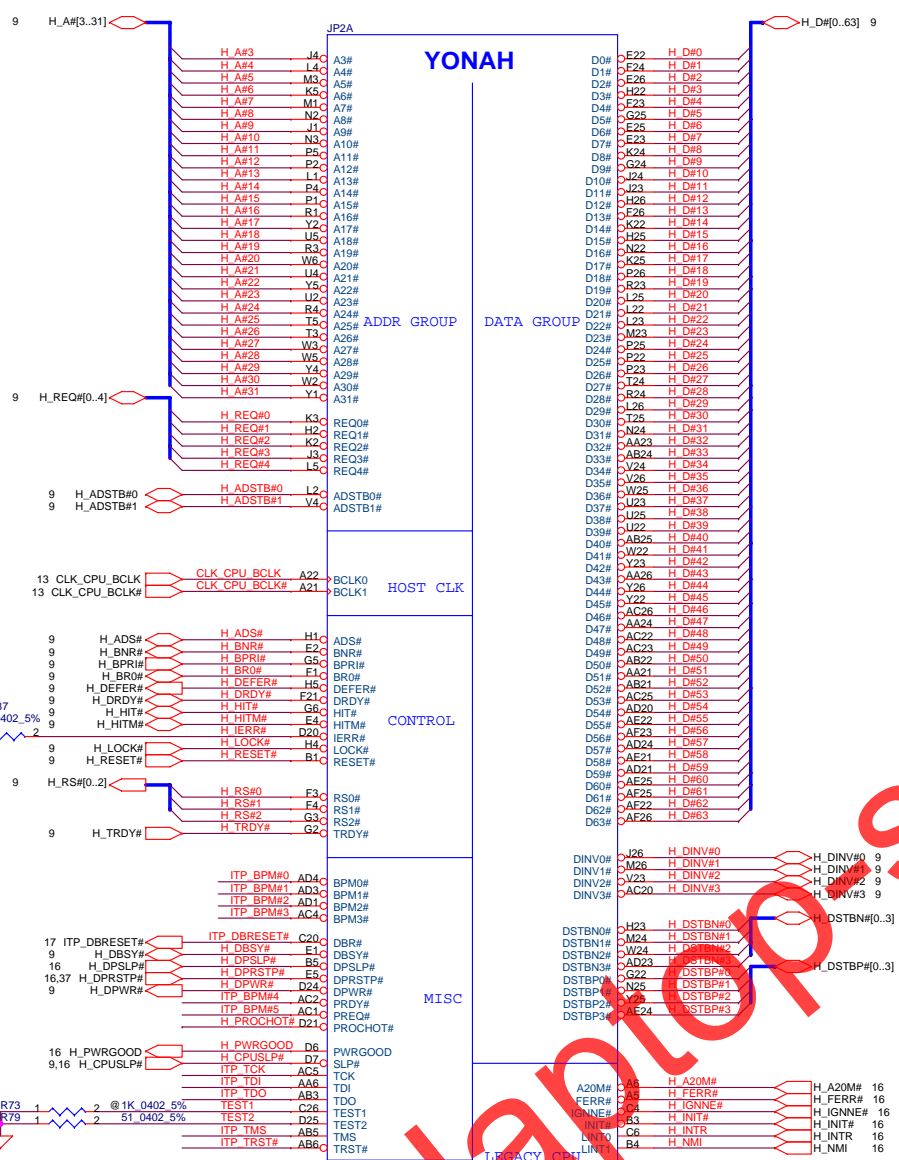
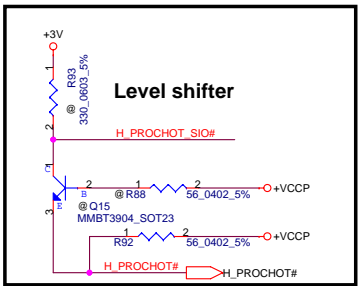
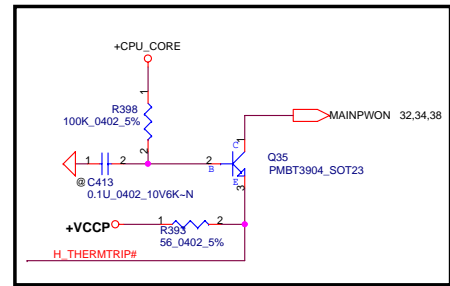
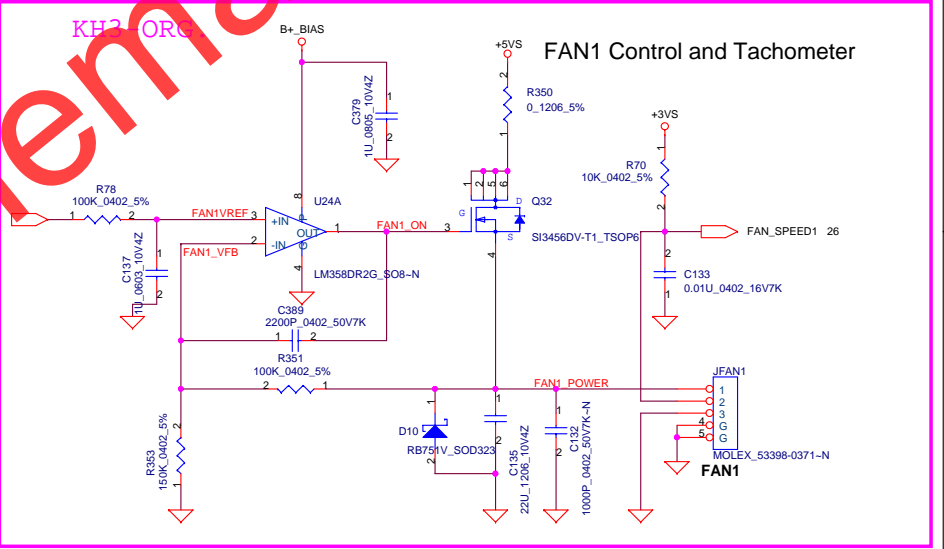
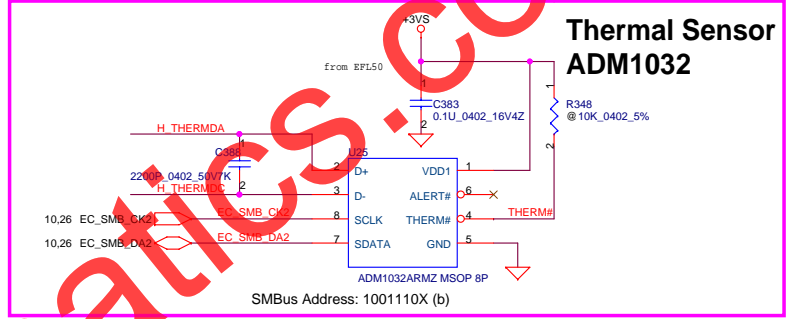
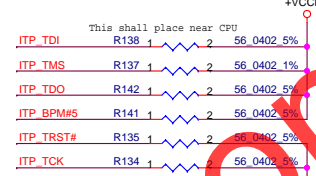
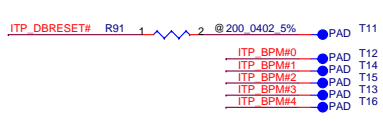


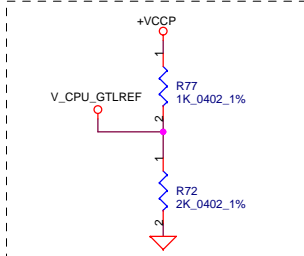
www.laptop-schematics.com



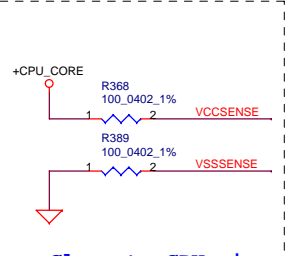
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



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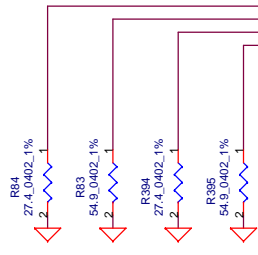
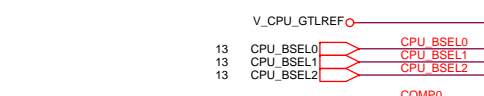
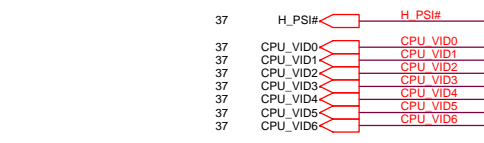
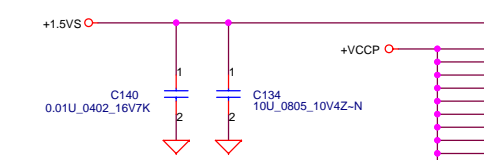
Close to CPU pin AD26 within 0.5 inch



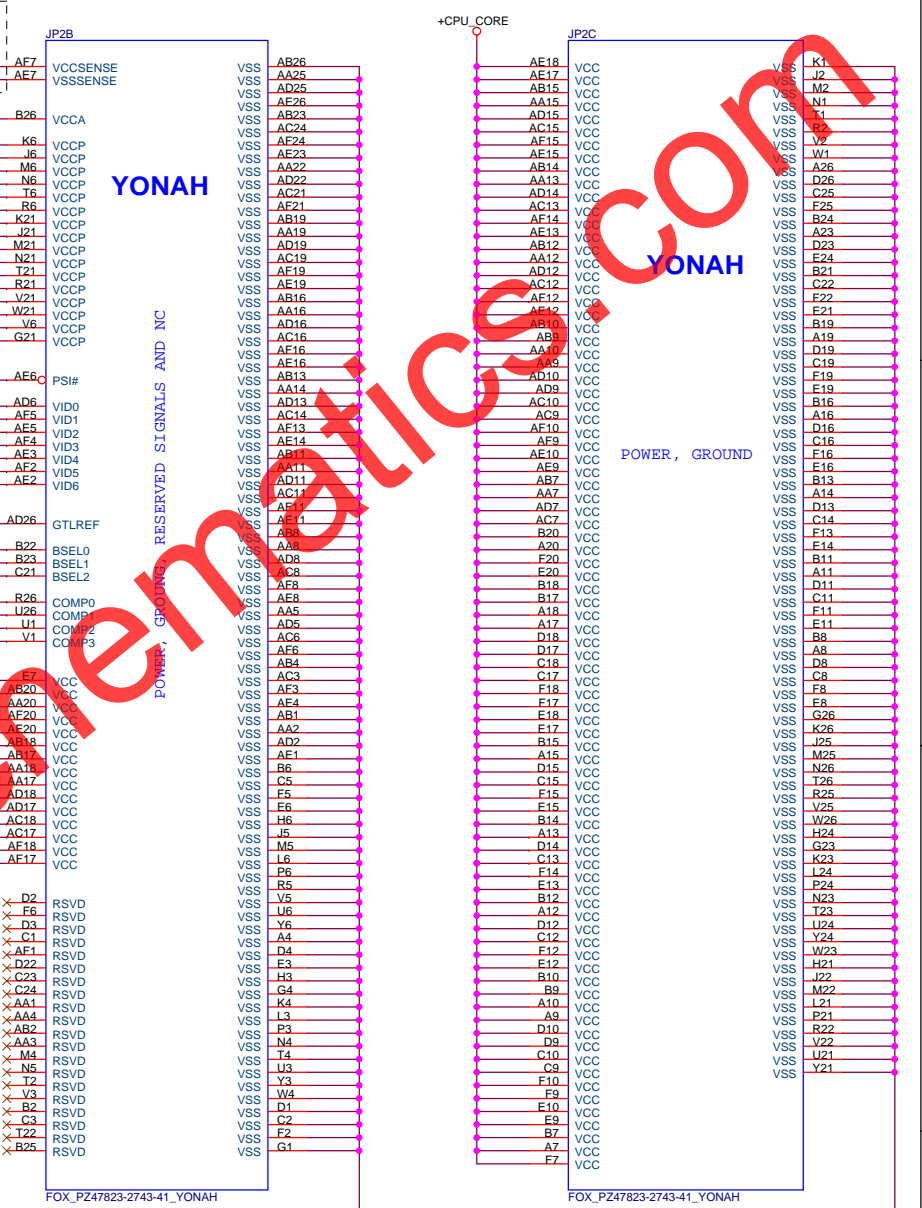
Close to CPU pin within 500mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Length match within 25 mils  
The trace width 18 mils space  
7 mils



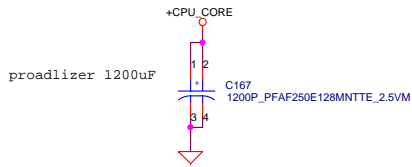
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



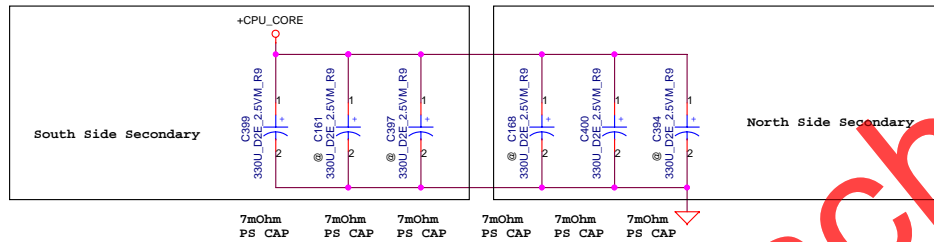
FOX\_PZ47823-2743-41\_YONAH

FOX\_PZ47823-2743-41\_YONAH

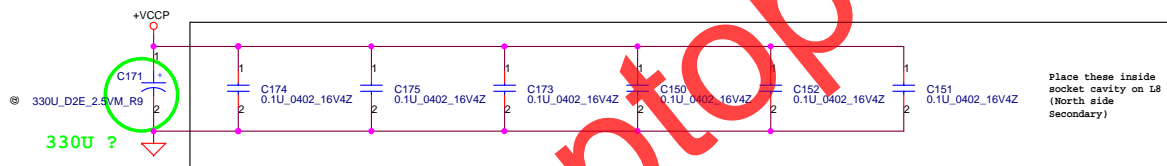
www.laptop-schematics.com



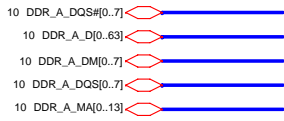
Mid Frequency Decoupling



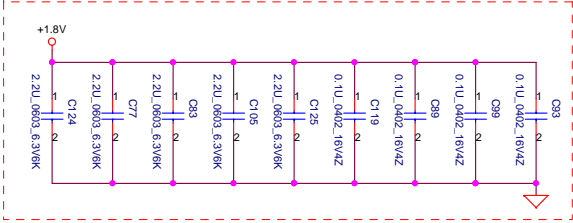
ESR <= 1.5m ohm  
Capacitor > 1980uF



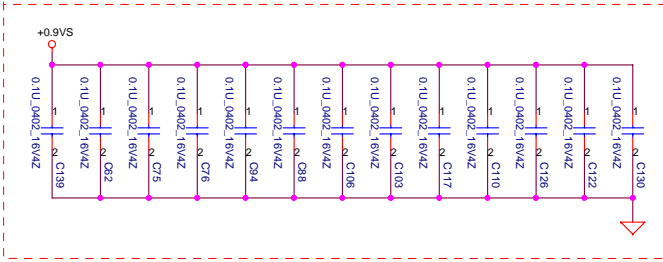
www.laptop-schematics.com



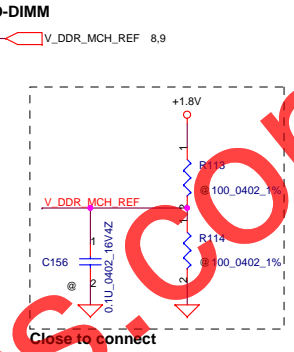
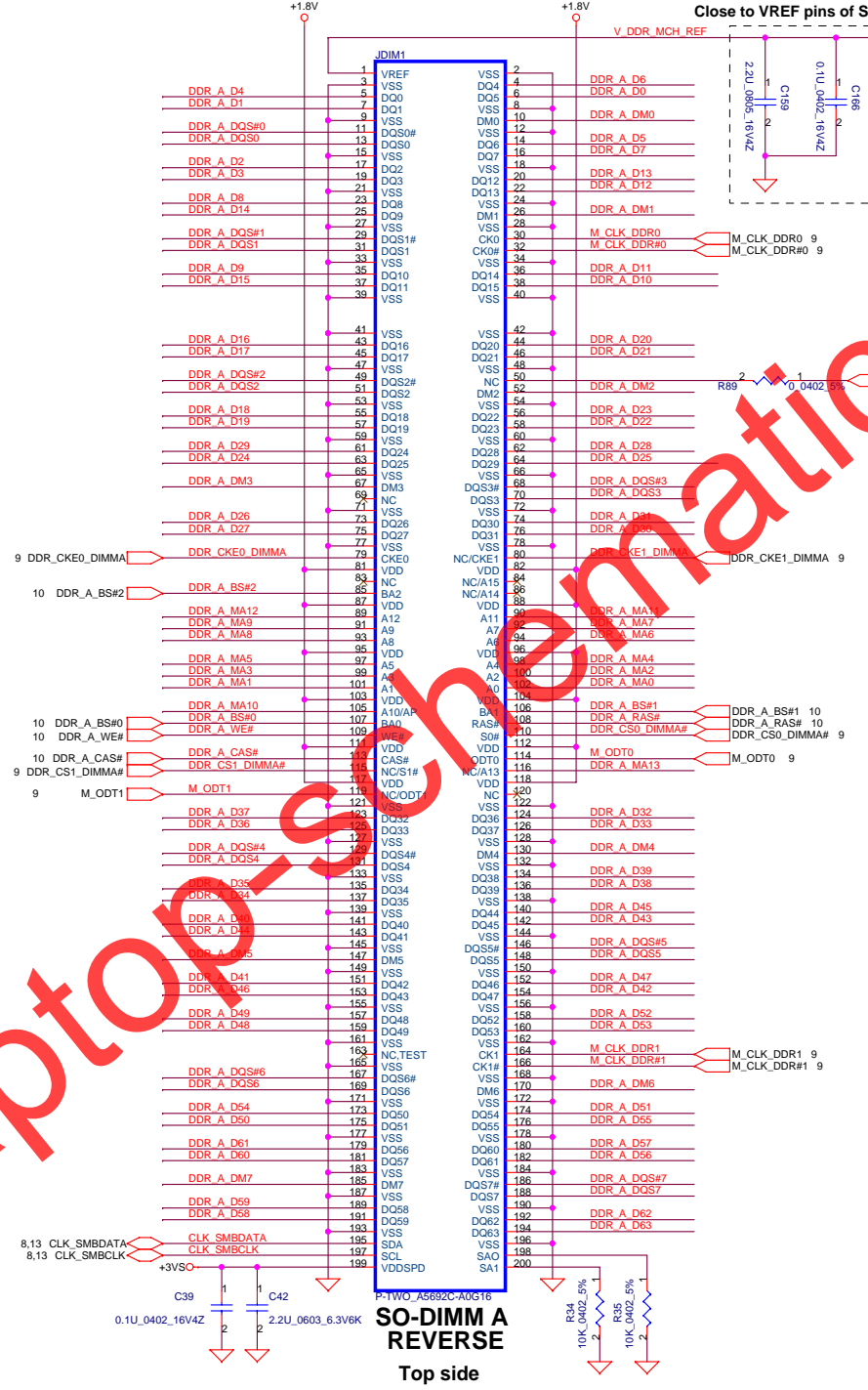
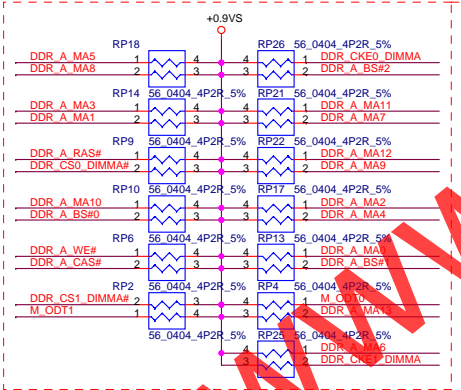
**Layout Note:**  
Place near JP41



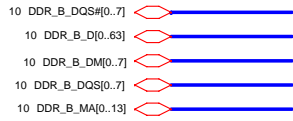
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



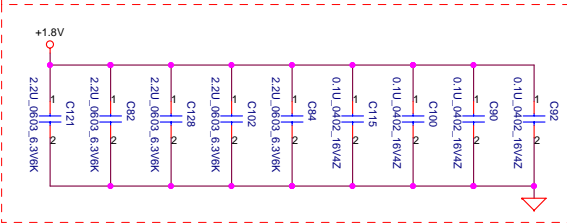
**Layout Note:**  
Place these resistor closely JP41, all trace length Max=1.5"



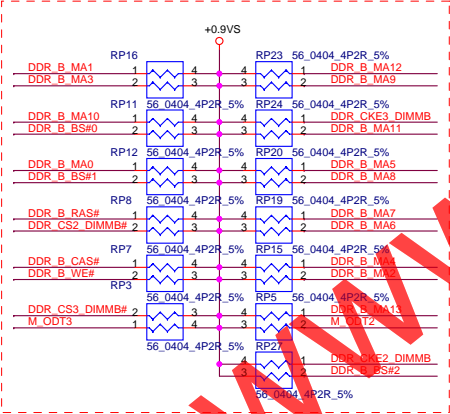
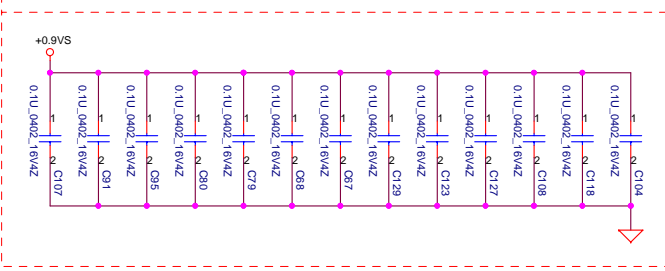
SO-DIMM A REVERSE Top side



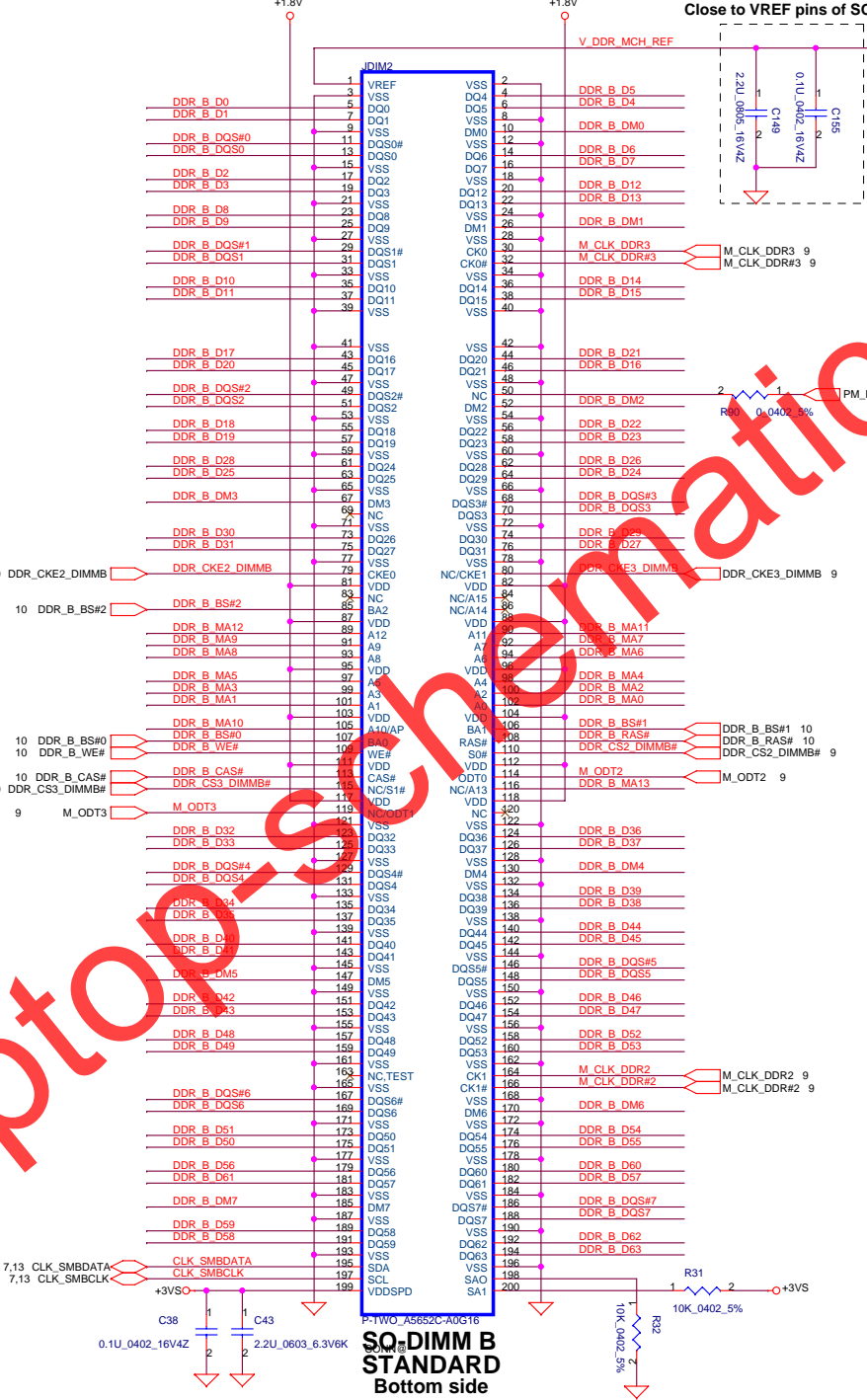
**Layout Note:**  
Place near JP42



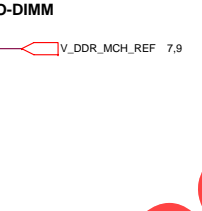
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP42, all trace length Max=1.5"

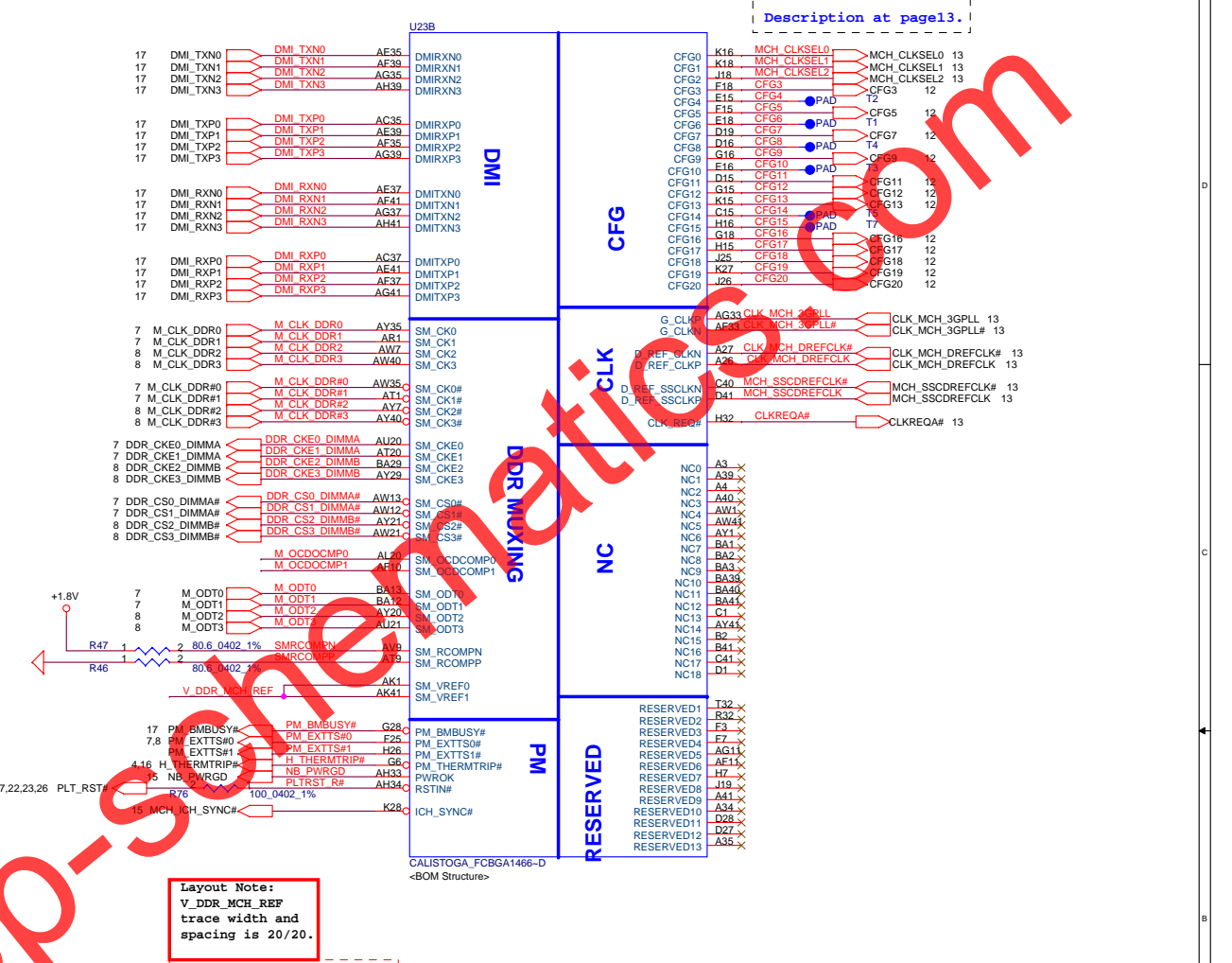
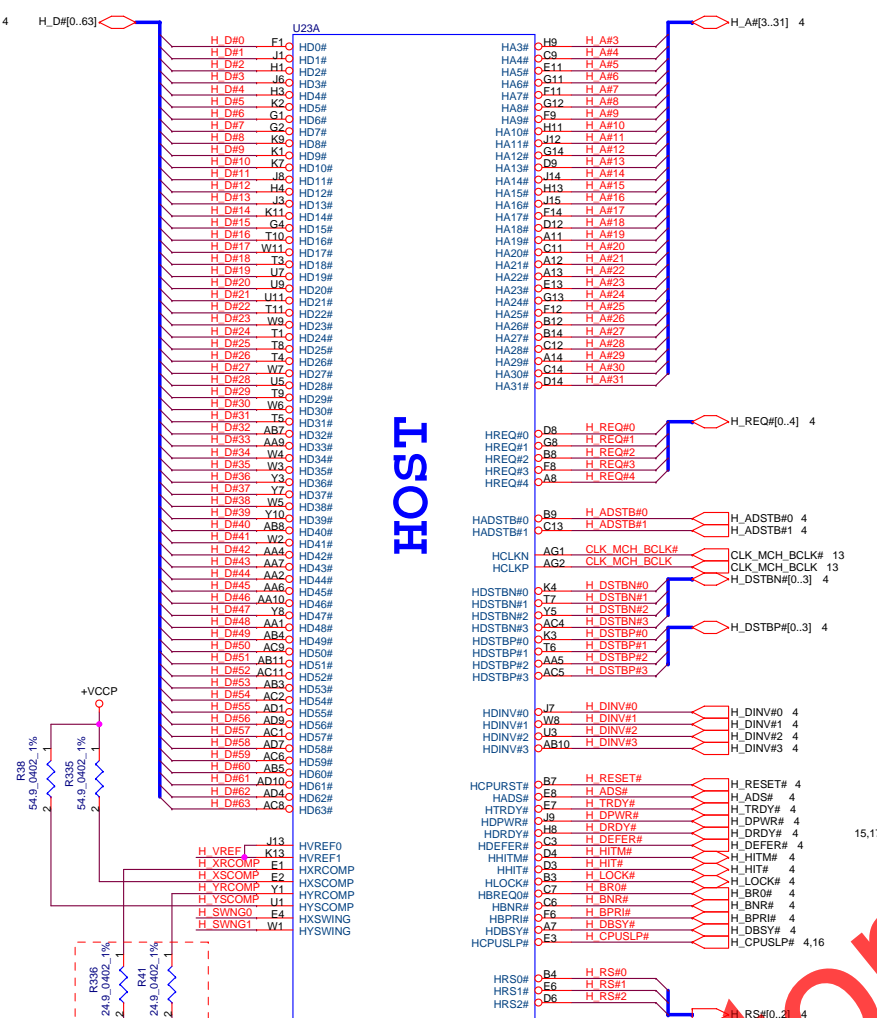


**SO-DIMM B  
STANDARD  
Bottom side**

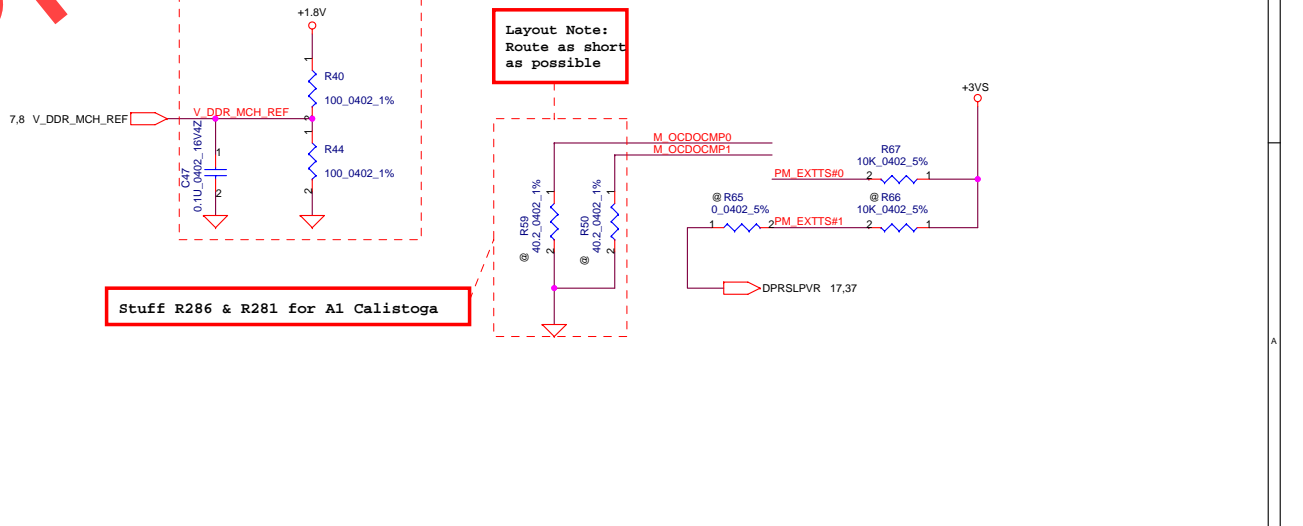
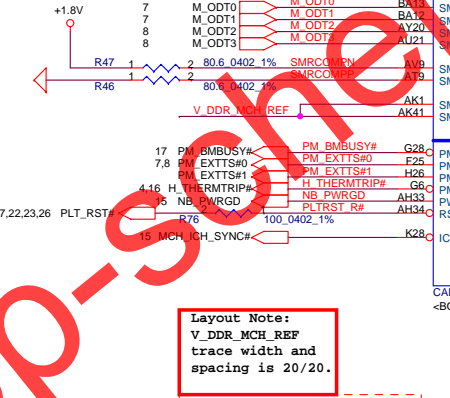
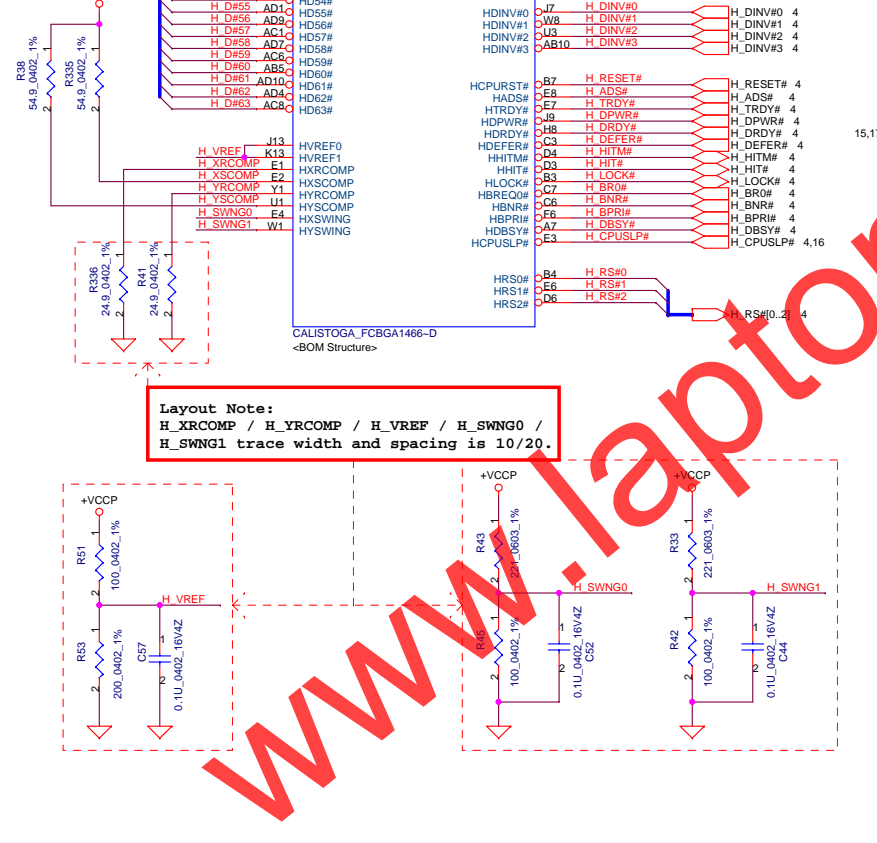


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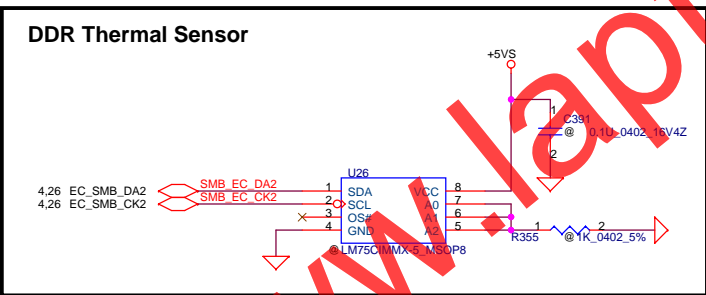
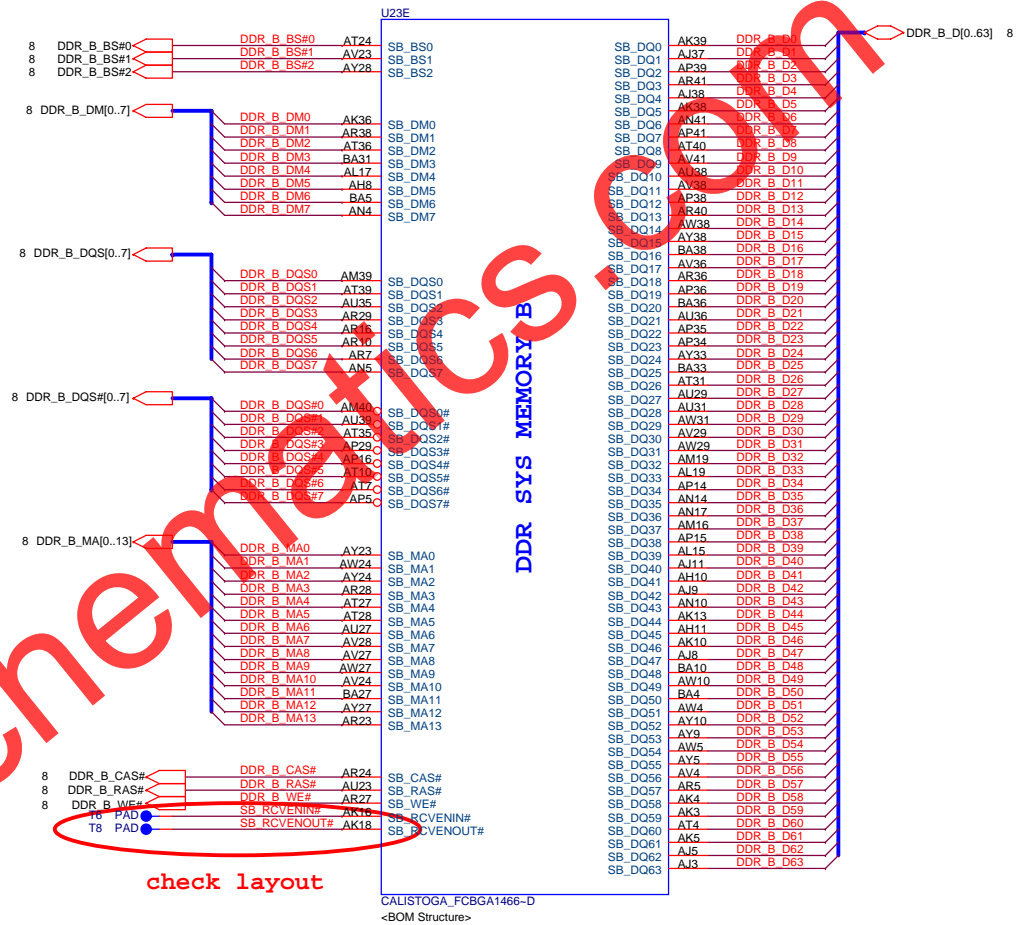
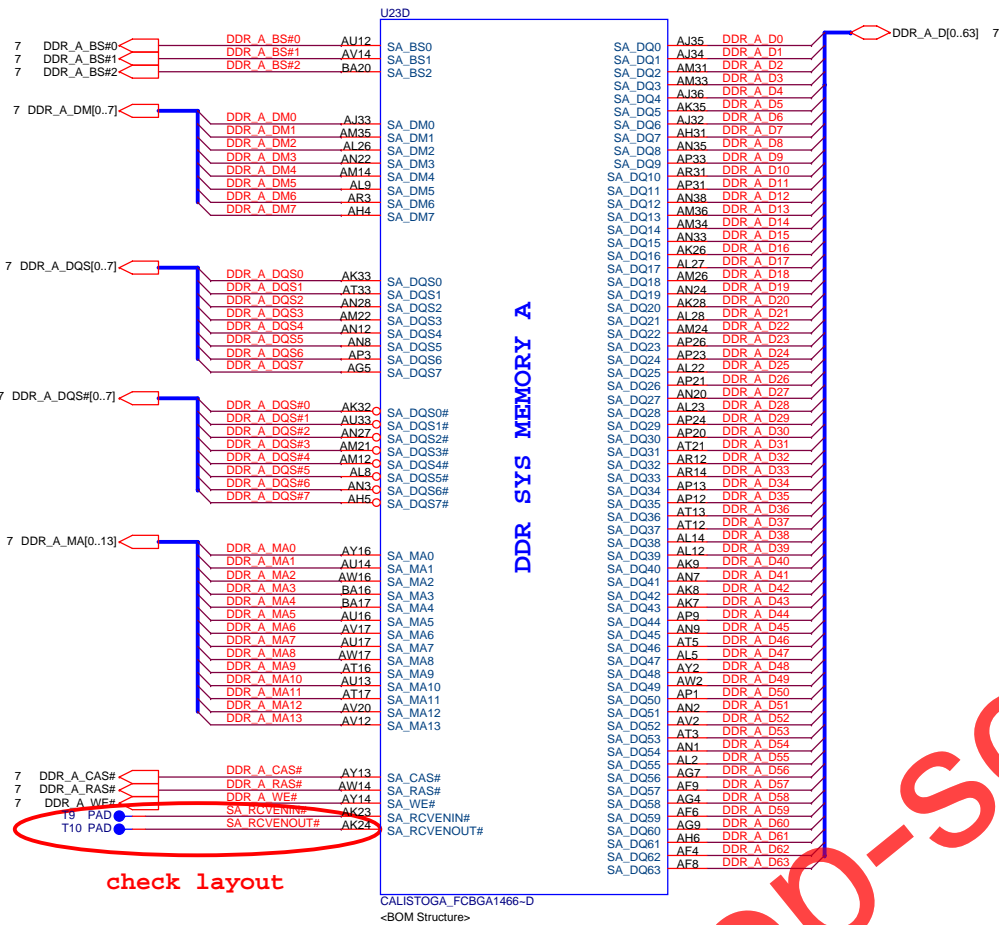




Description at pagel3.



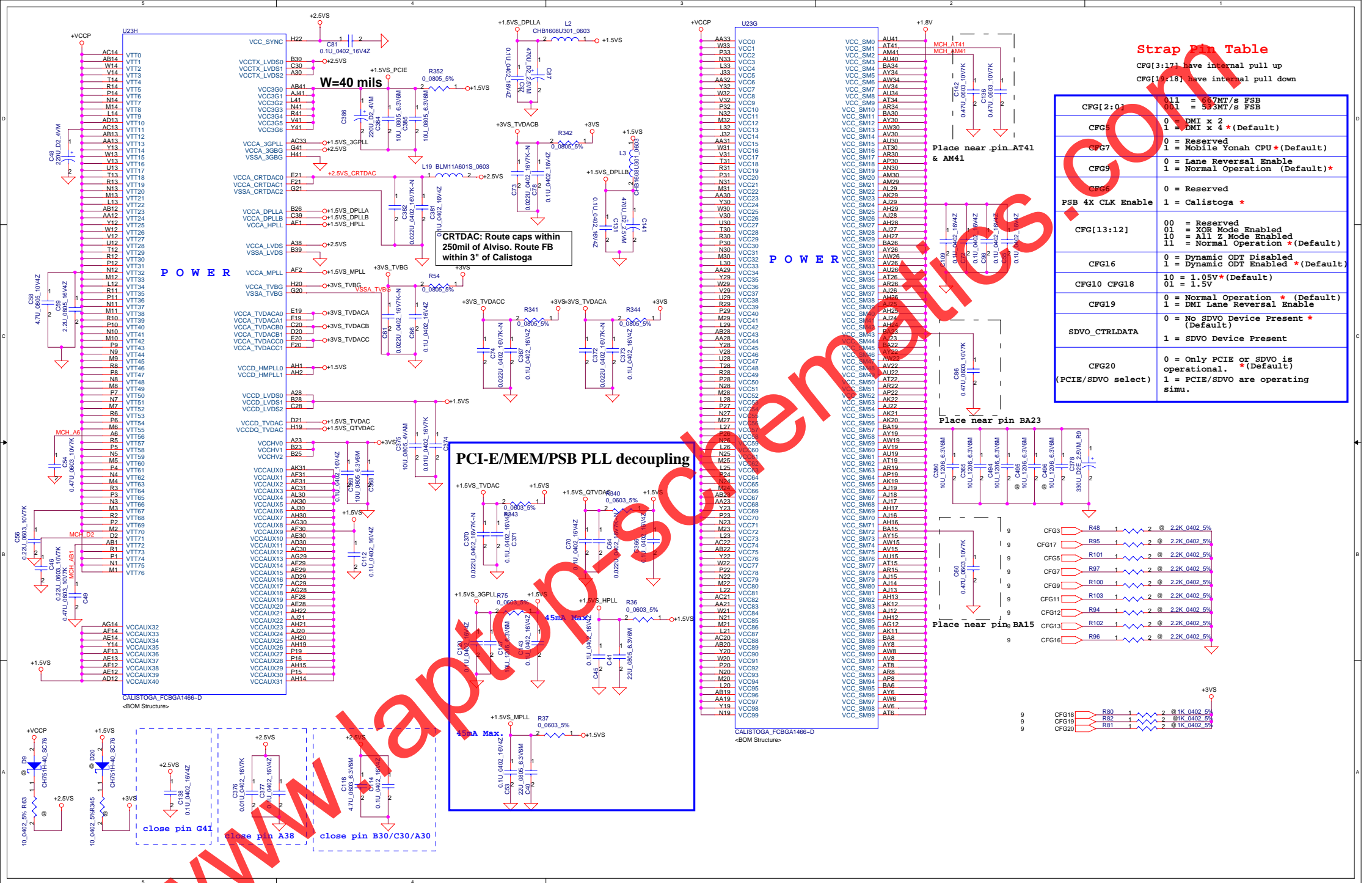
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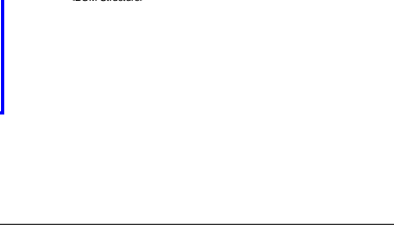
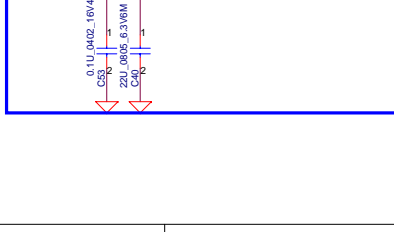
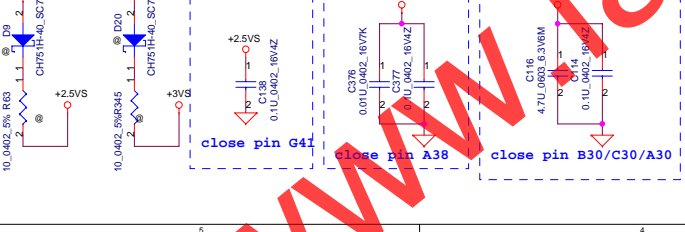
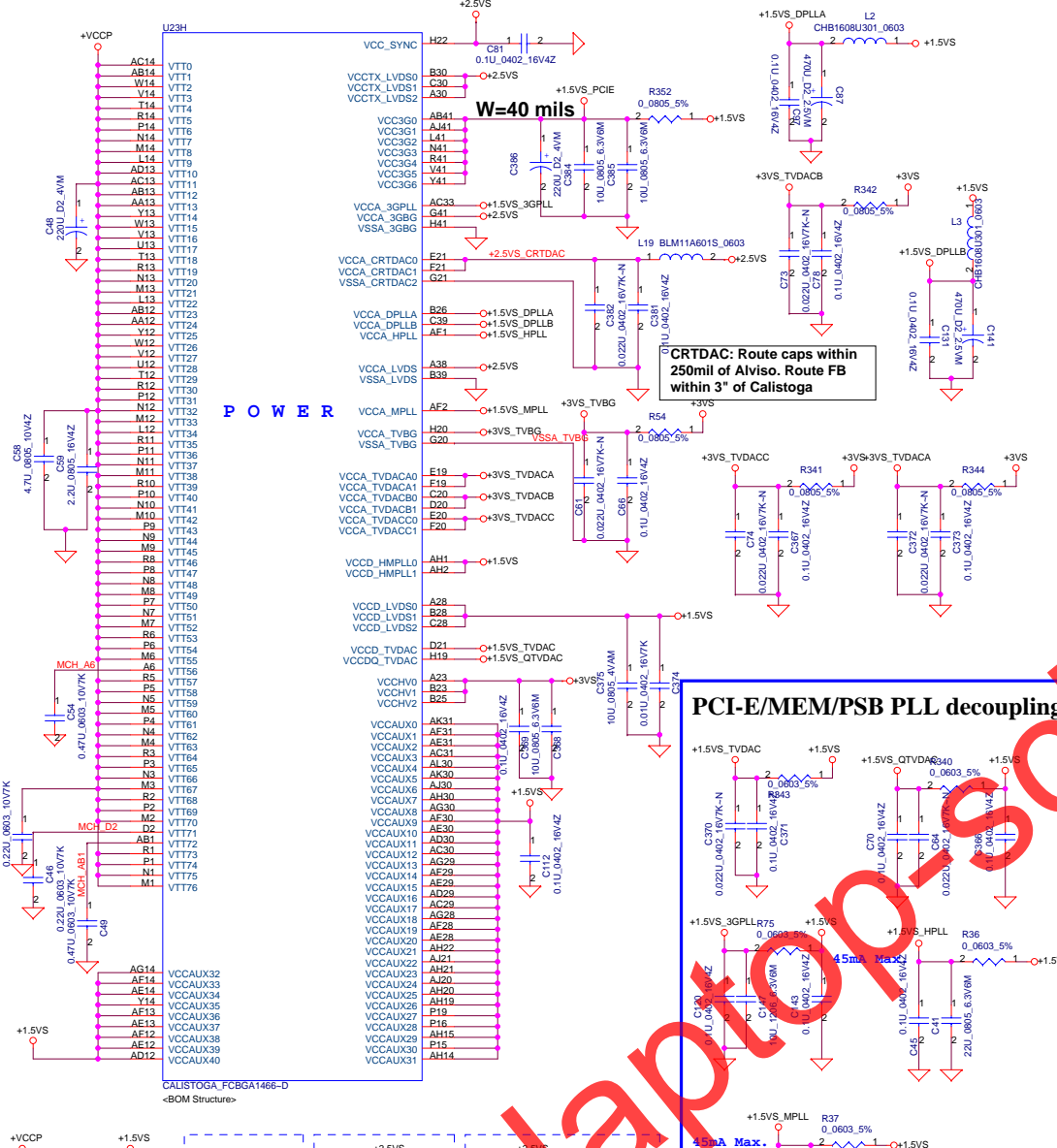
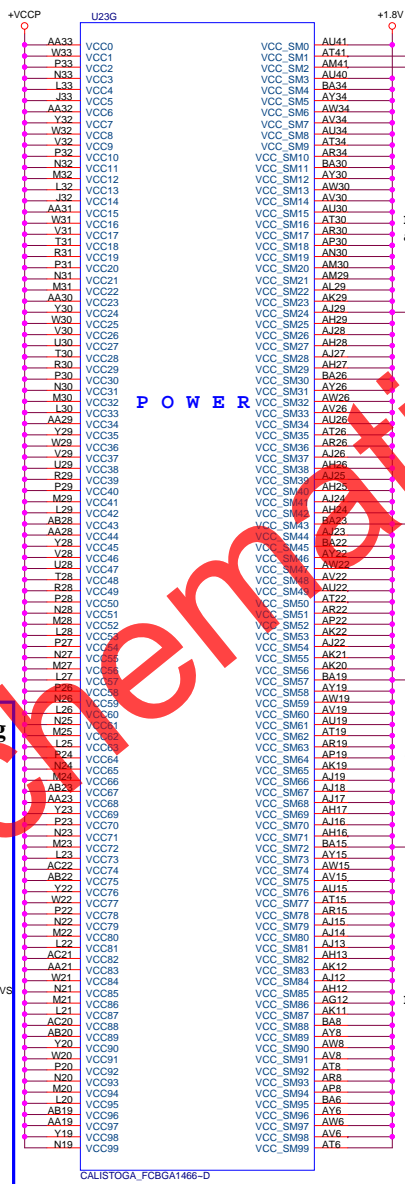
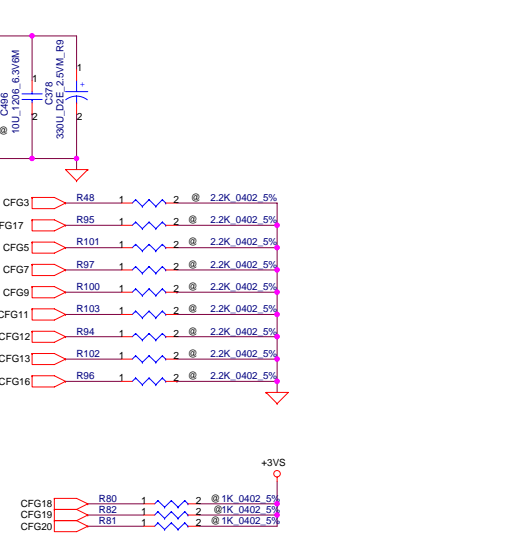




### Strap Pin Table

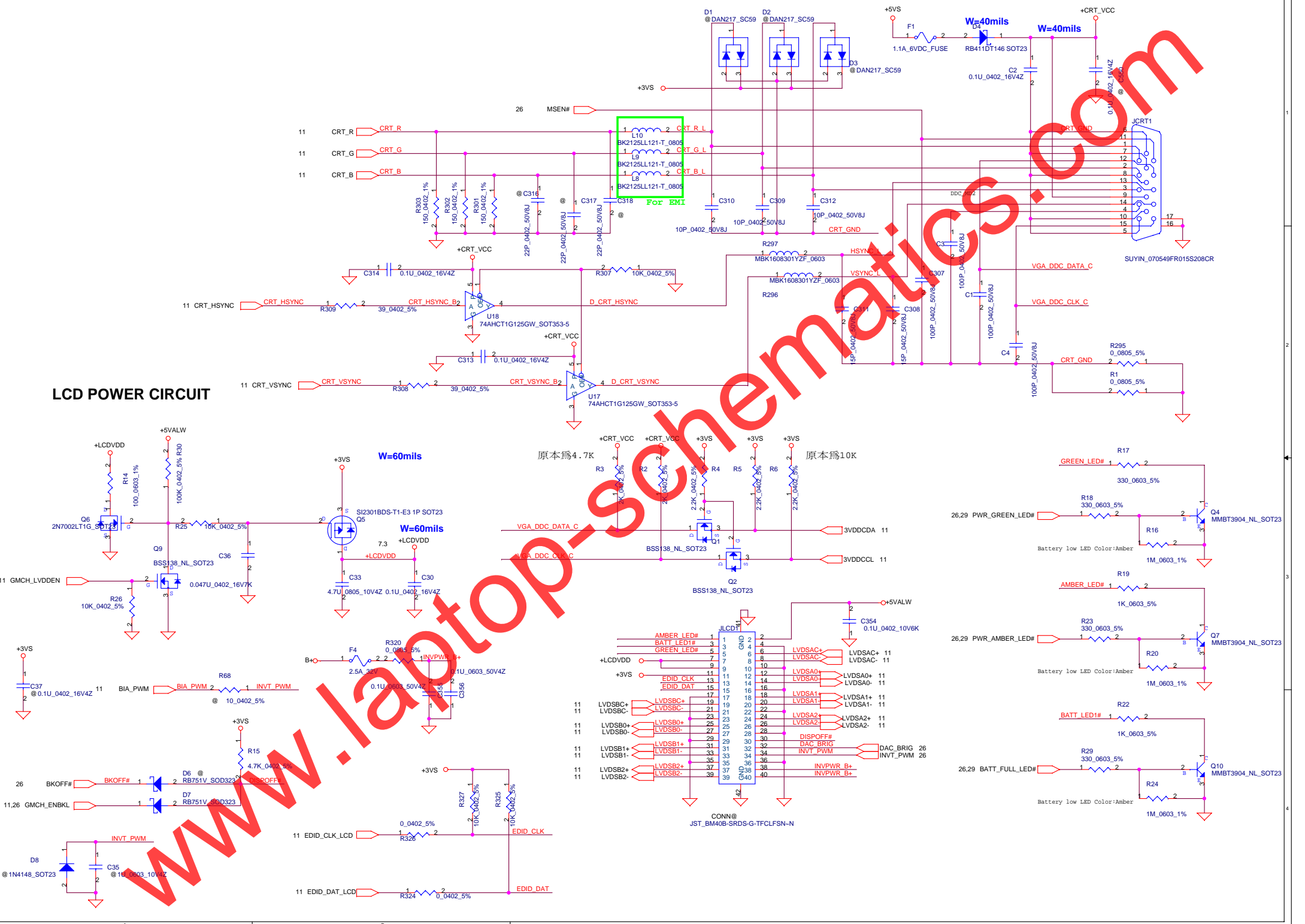
CFG[3:17] have internal pull up  
 CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 553MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable (Default)
SDVO_CTRLDATA	1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.



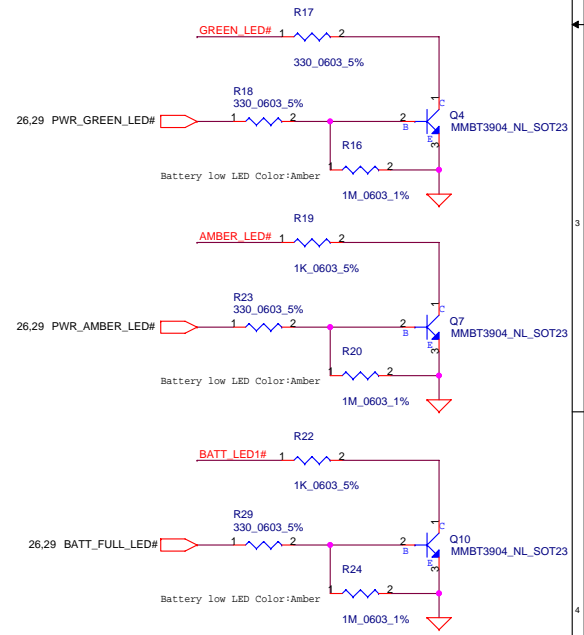


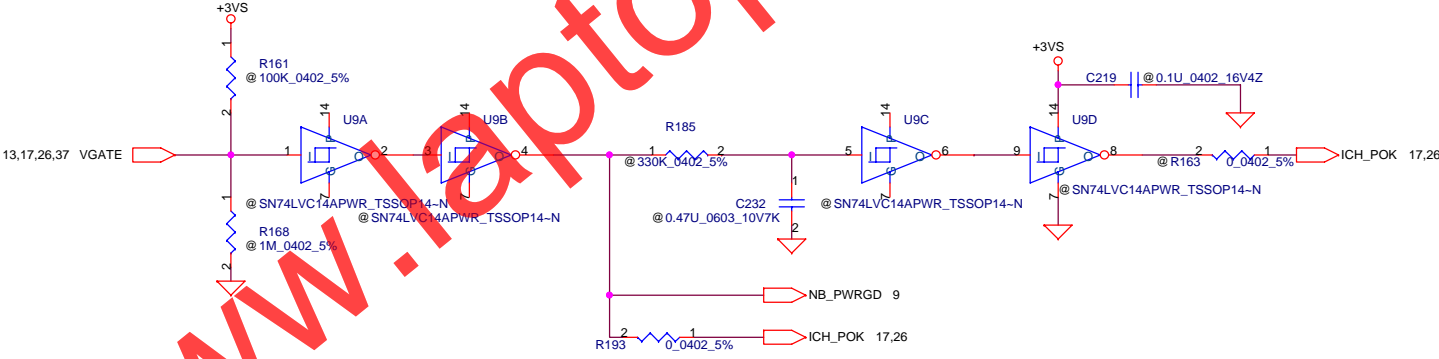
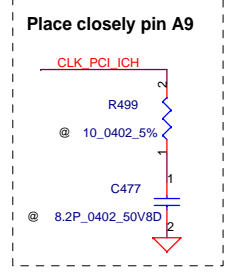
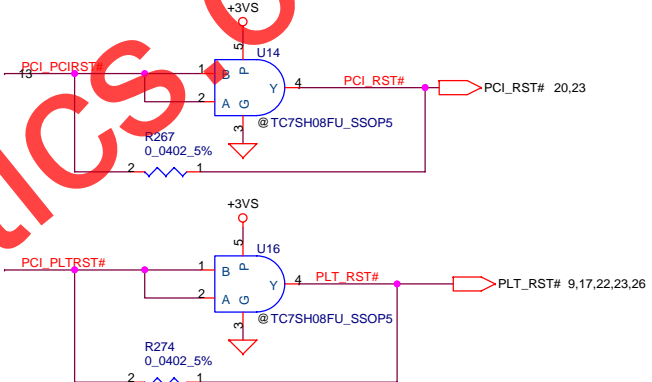
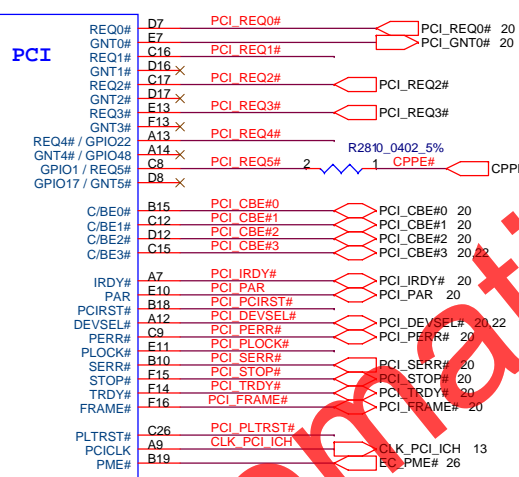
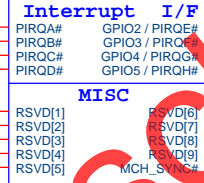
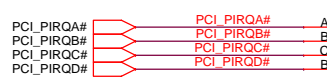
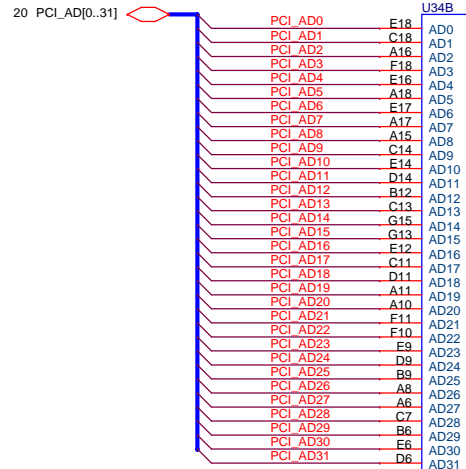
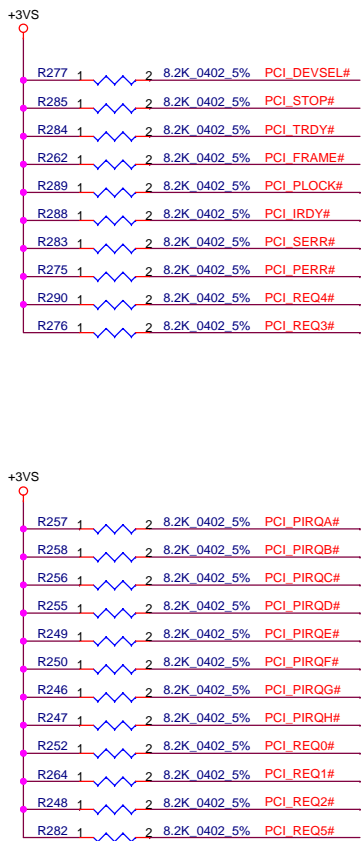
# LCD POWER CIRCUIT



原本為4.7K  
原本為10K

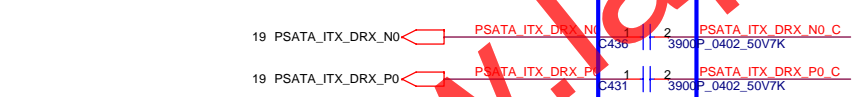
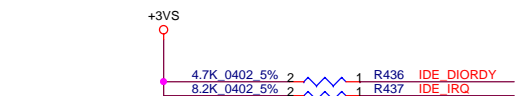
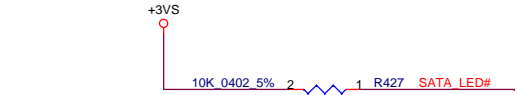
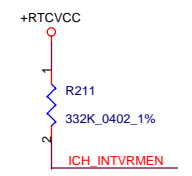
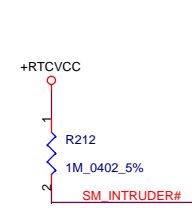
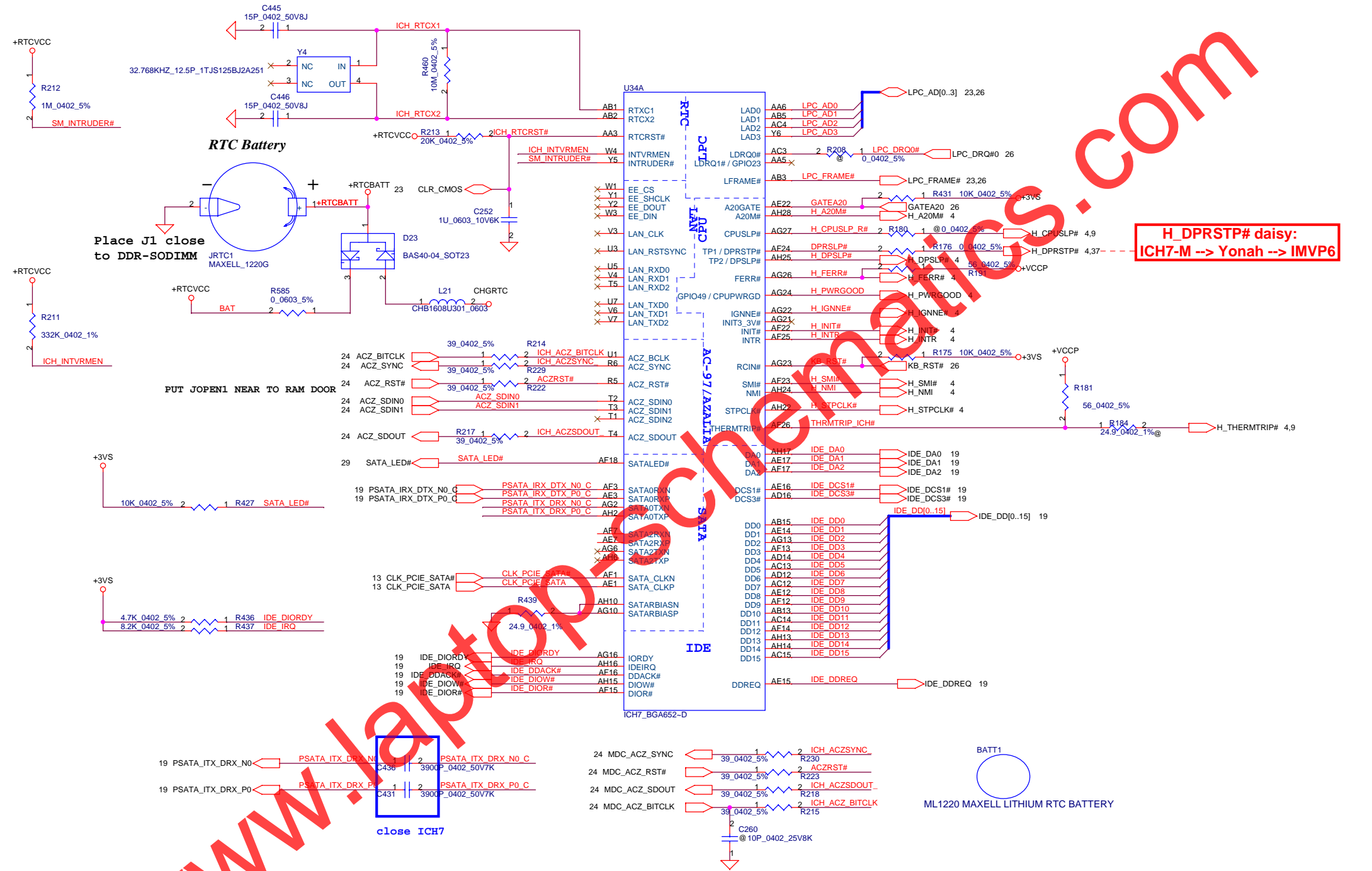
CONN@ JST\_BM40B-SRDS-G-TFCLFSN-N





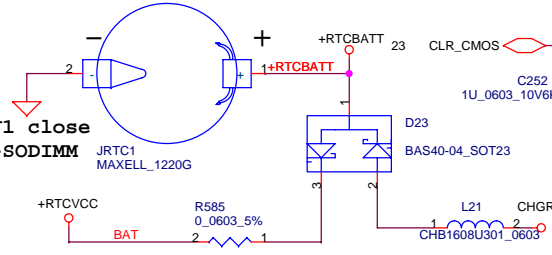
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close ICH7

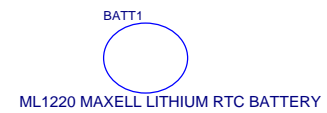
RTC Battery



Place J1 close to DDR-SODIMM

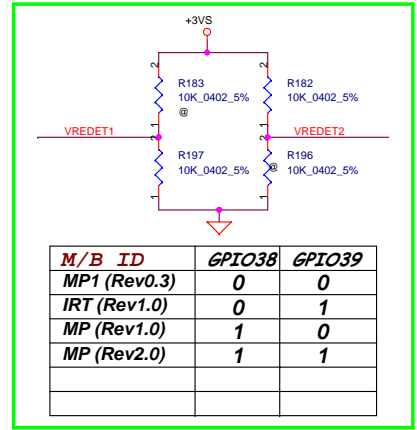
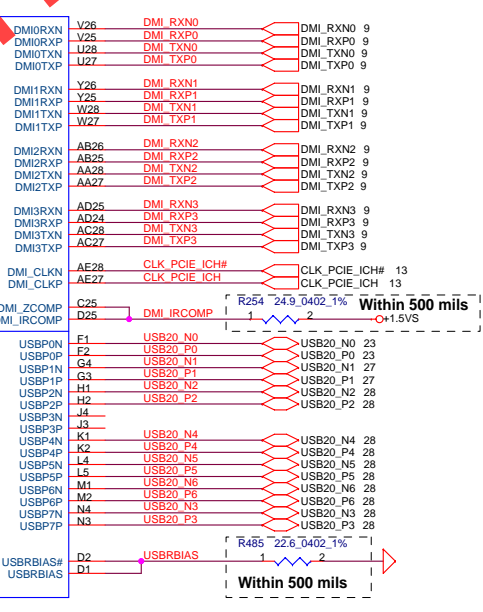
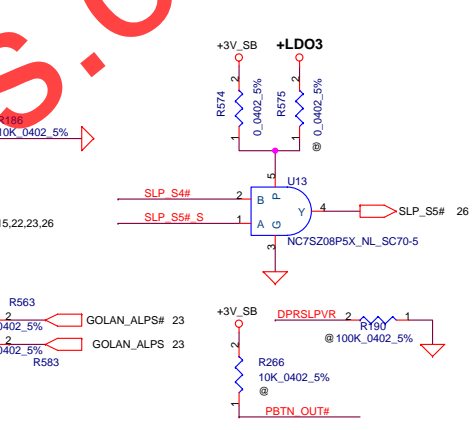
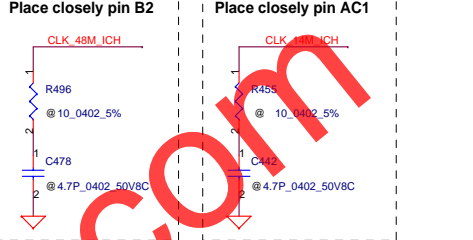
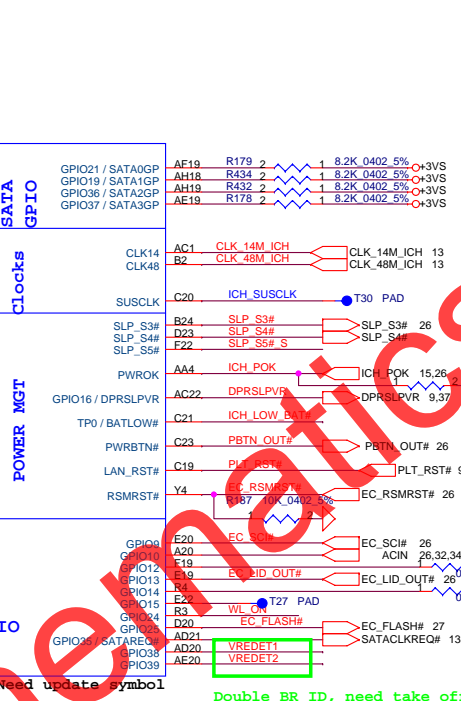
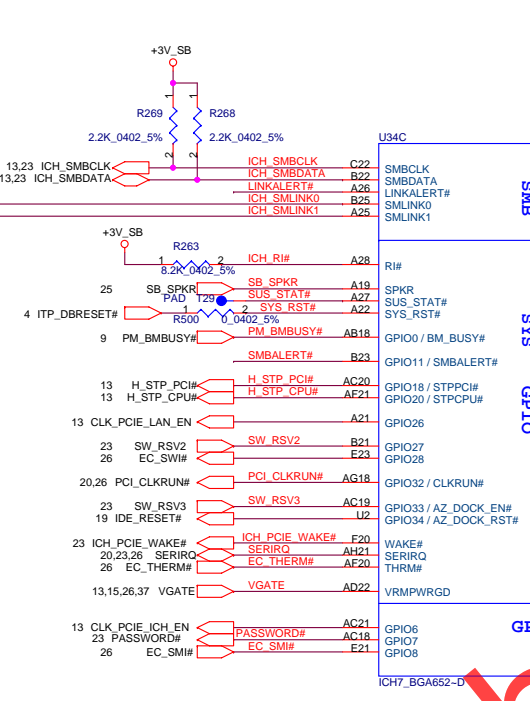
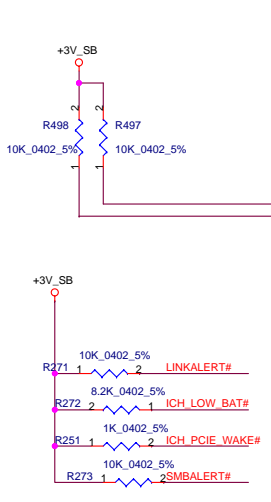
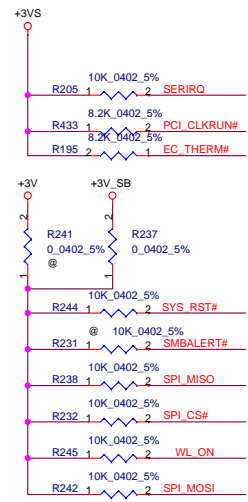
PUT JOPEN1 NEAR TO RAM DOOR

H\_DPRSTP# daisy:  
ICH7-M --> Yonah --> IMVP6

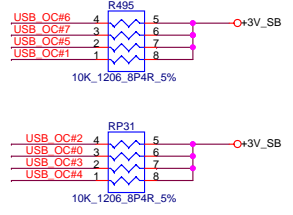


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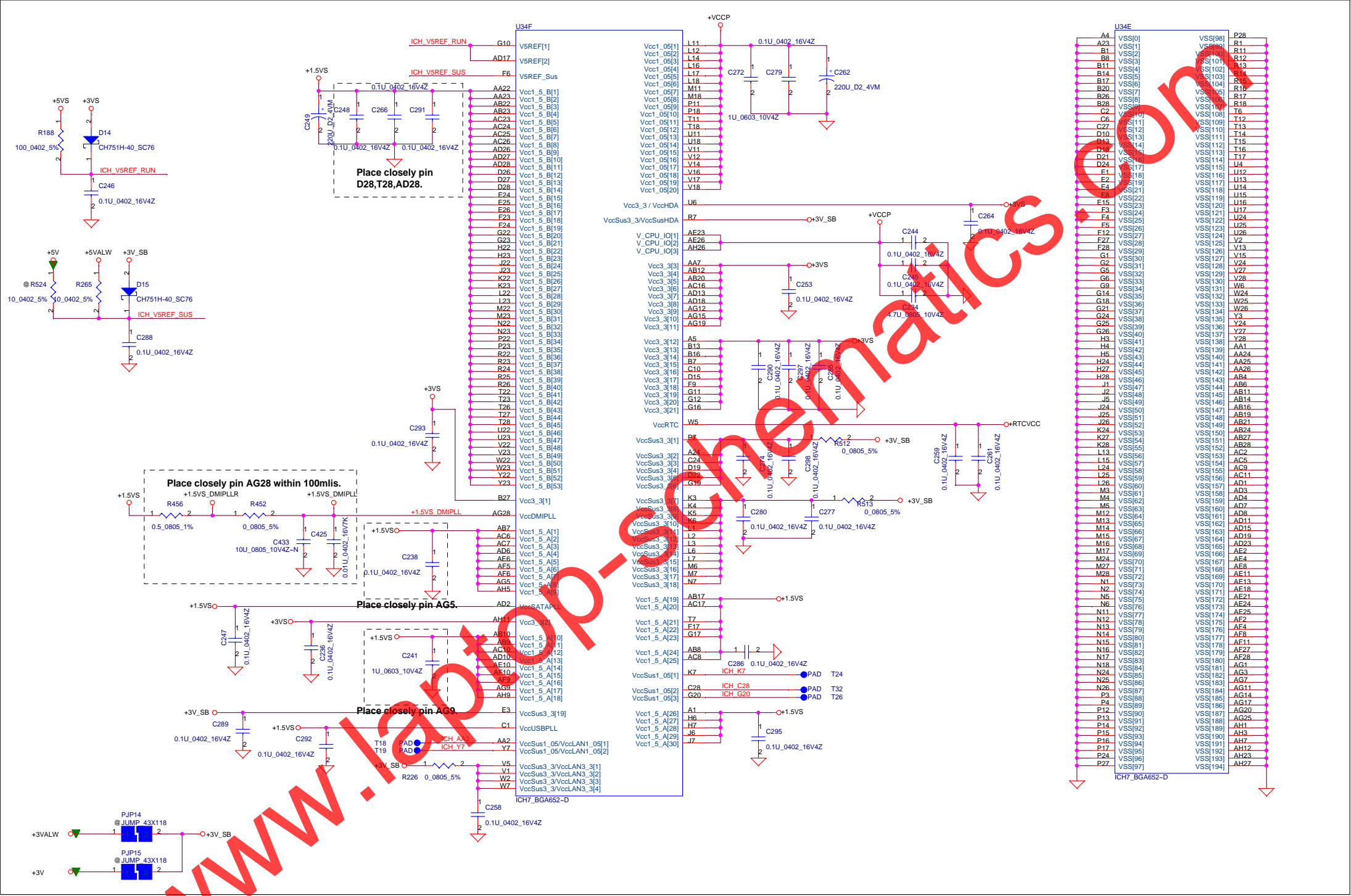


M/B ID	GPIO38	GPIO39
MP1 (Rev.0.3)	0	0
IRT (Rev1.0)	0	1
MP (Rev1.0)	1	0
MP (Rev2.0)	1	1

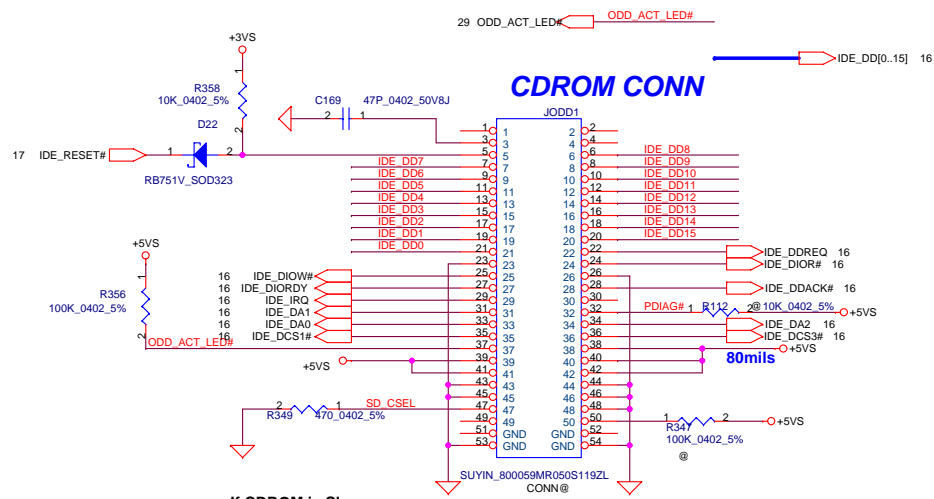


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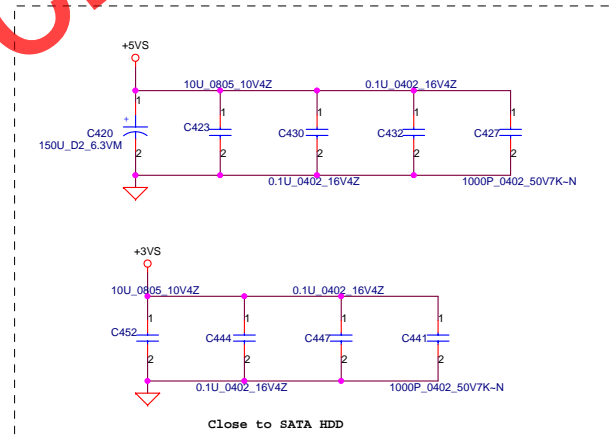
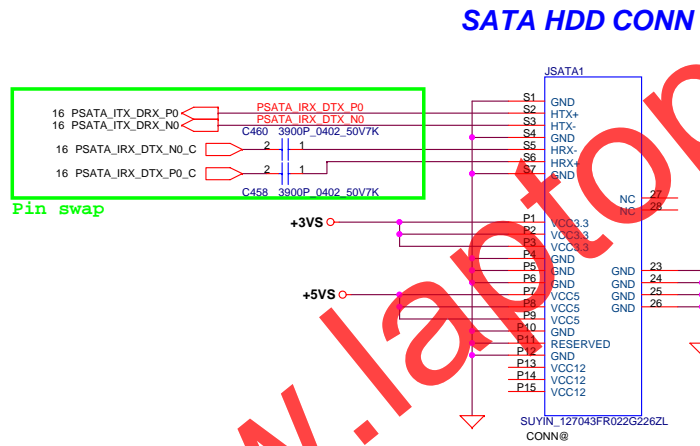
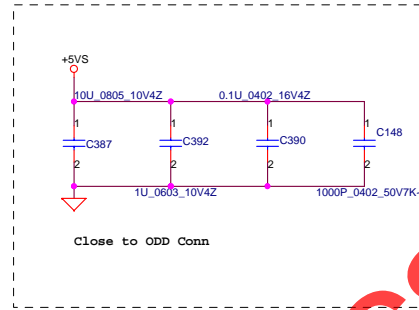
Need update symbol  
Double BR ID, need take off

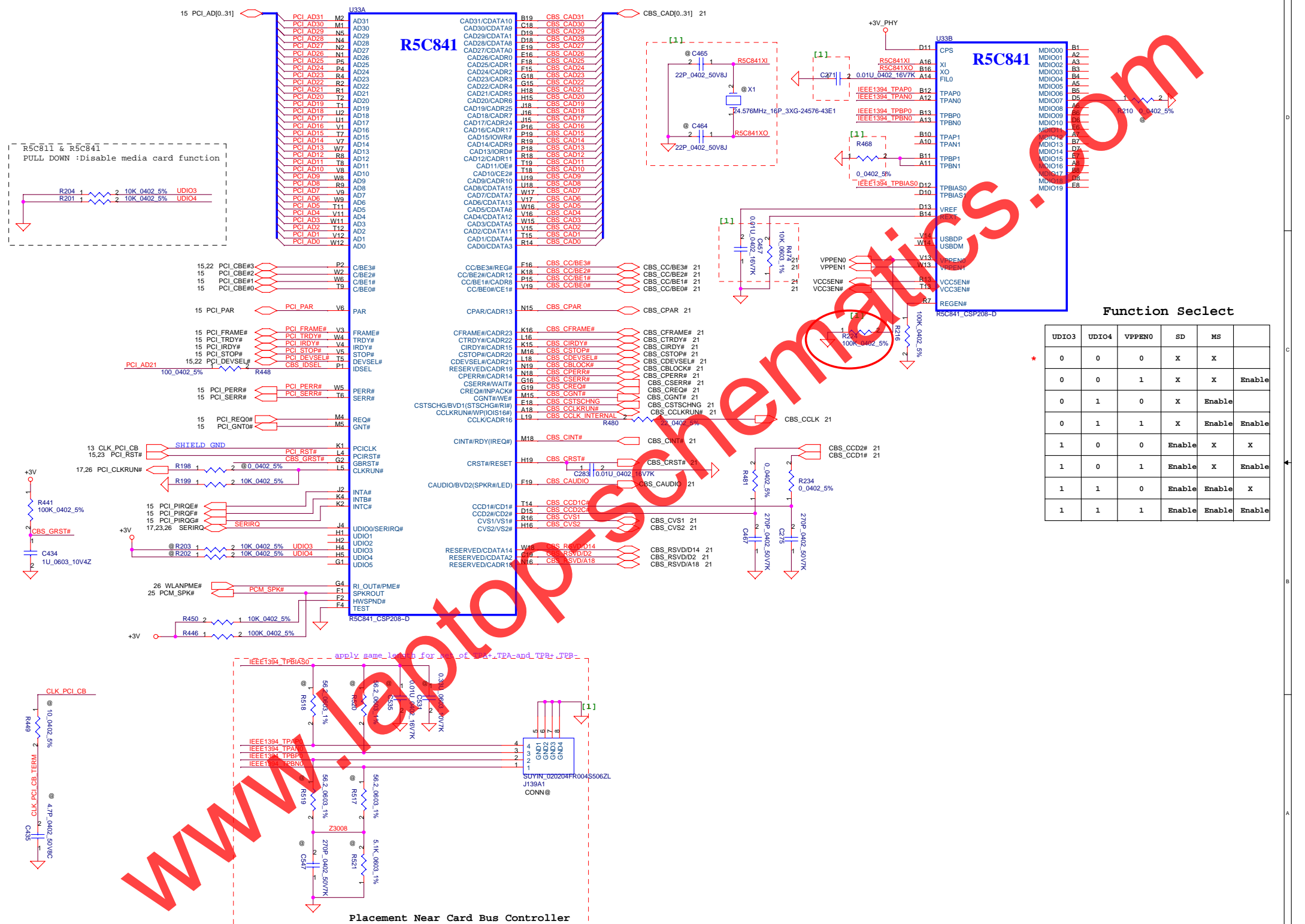


www.geminaelectronics.com



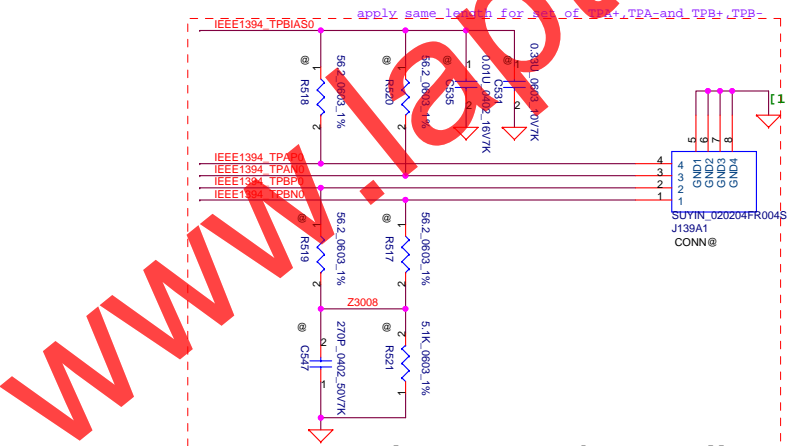
If CDROM is Slave  
then SD\_CSEL= Floating  
else SD\_CSEL= Low

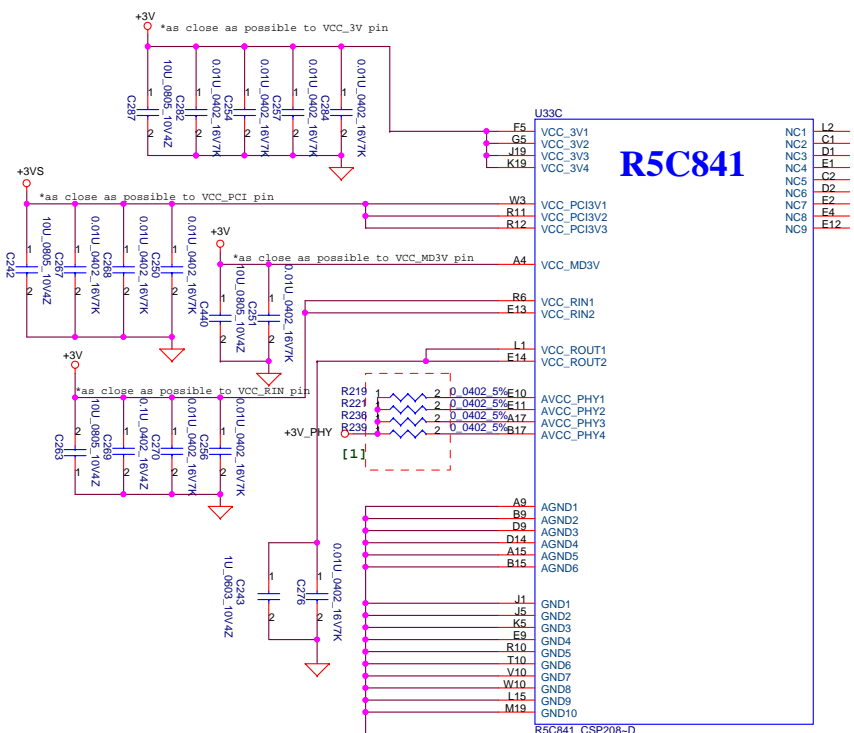




R5C811 & R5C841  
PULL DOWN :Disable media card function

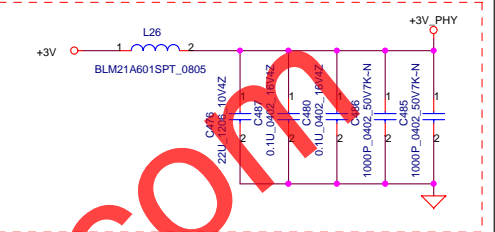
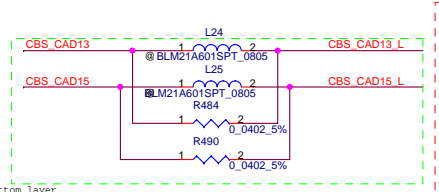
R204 1 2 10K 0402 5% UDIO3  
R201 1 2 10K 0402 5% UDIO4



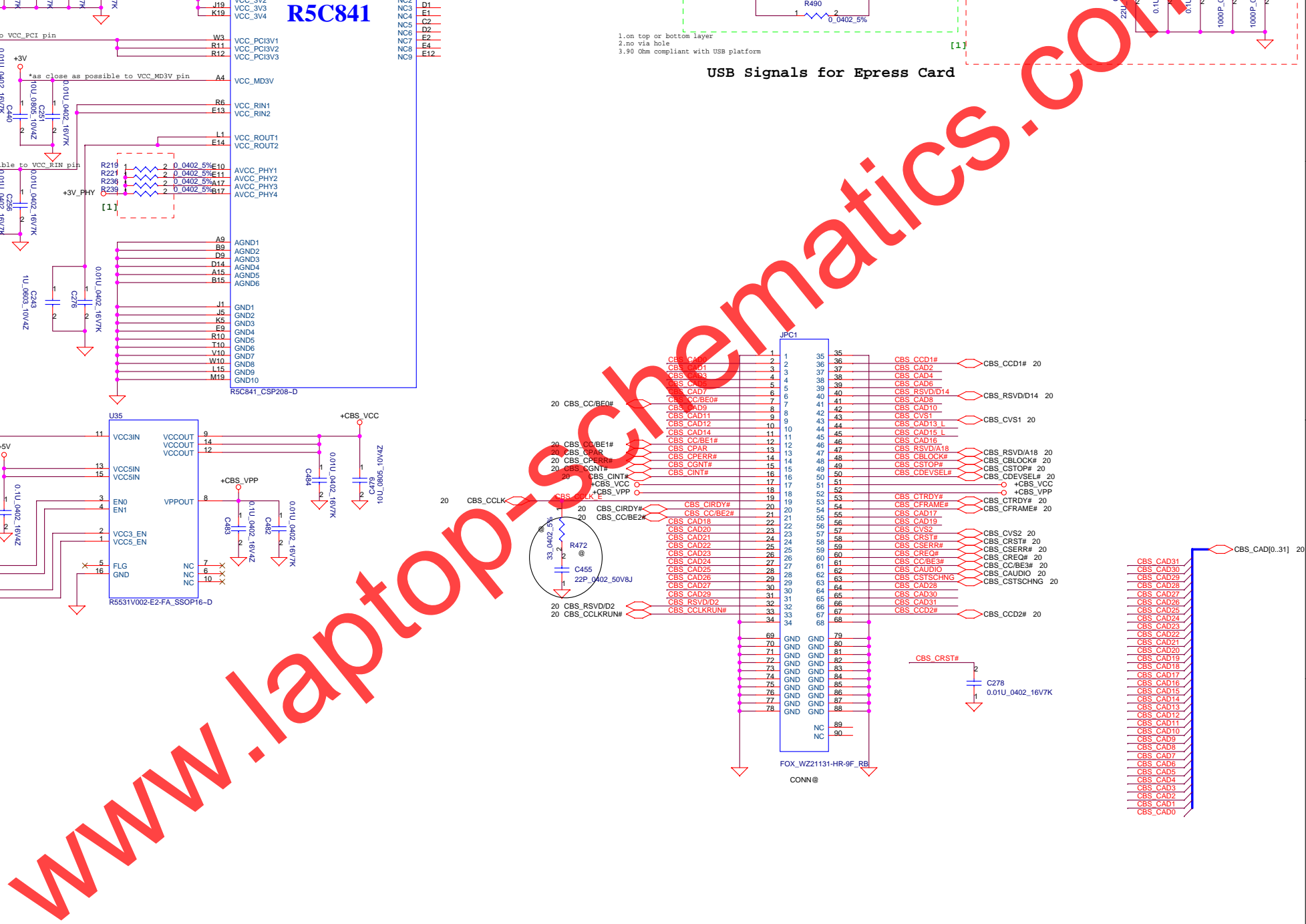
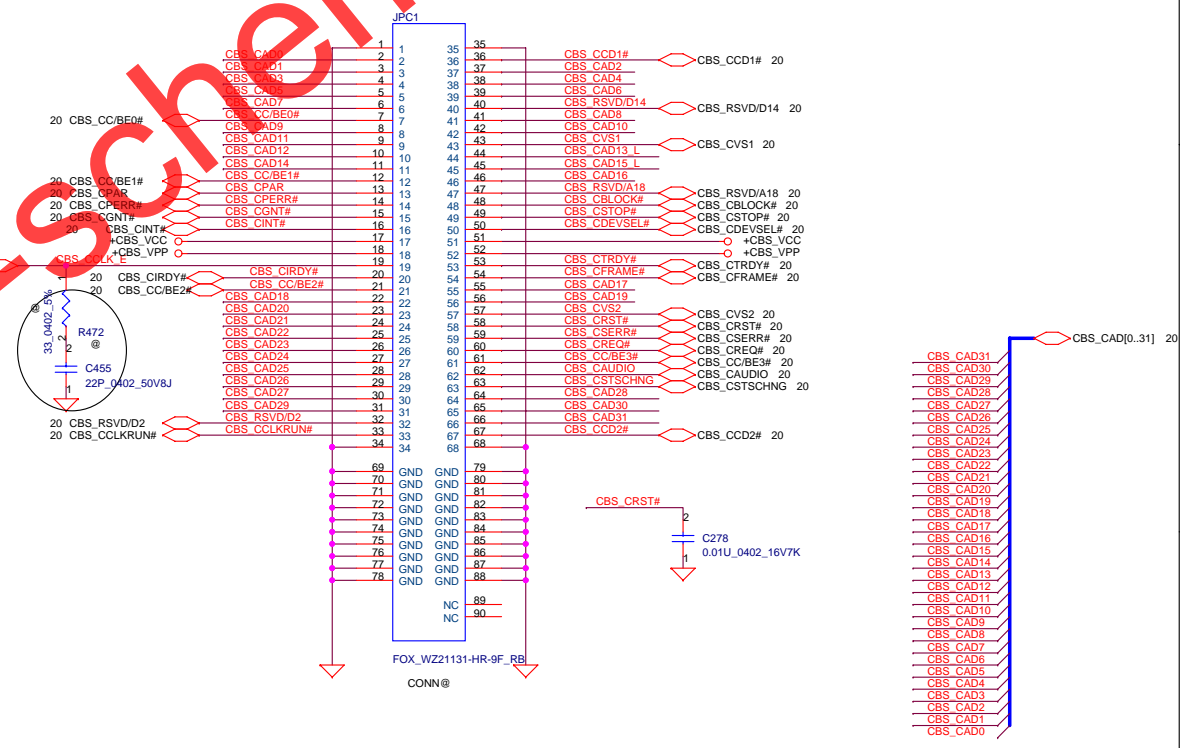
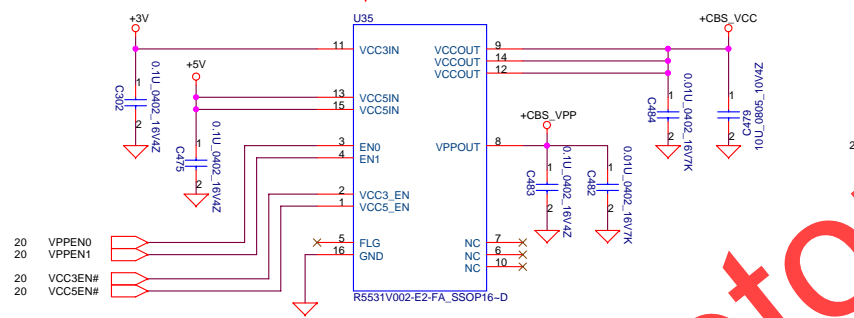


**R5C841**

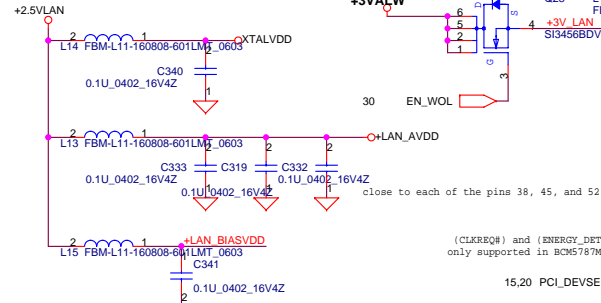
1. on top or bottom layer  
 2. no via hole  
 3.90 ohm compliant with USB platform



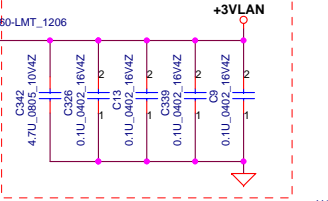
**USB Signals for Epress Card**



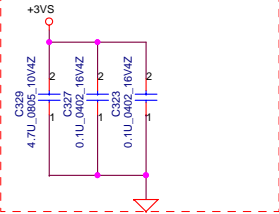
**Layout Notice : Filter place as close chip as possible.**



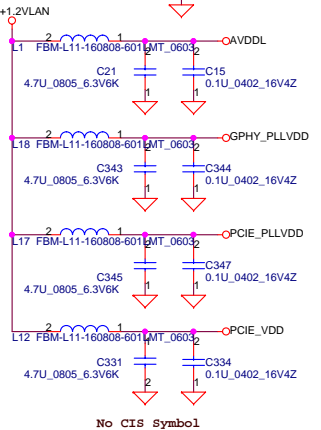
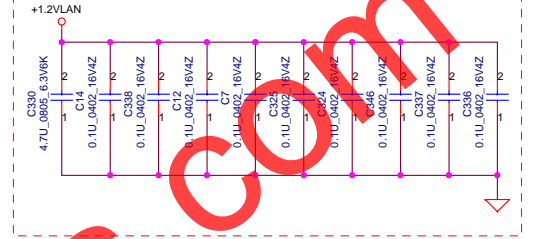
**Layout Notice : Place as close chip as possible.**



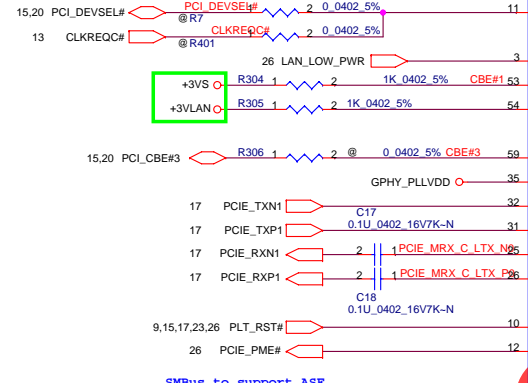
**Layout Notice : 3.3V filter. Place as close chip as possible.**



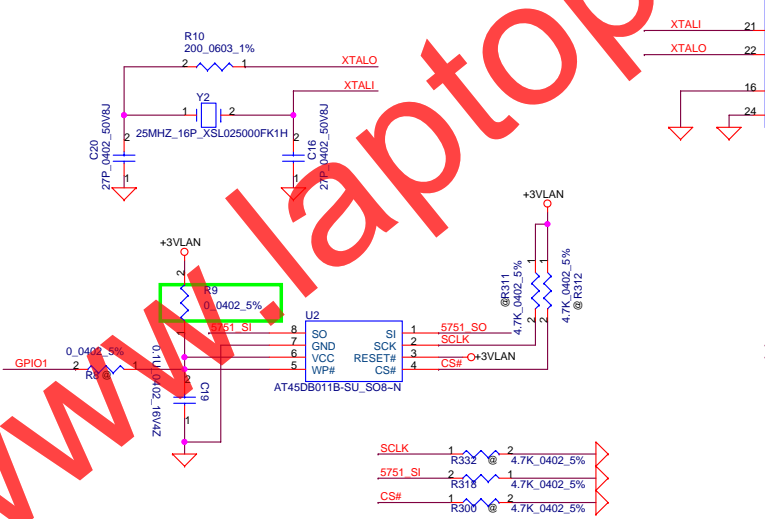
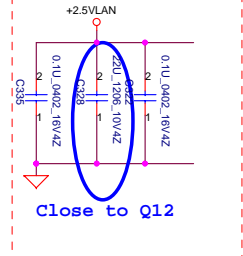
**Layout Notice : 1.2V filter. Place as close chip as possible.**



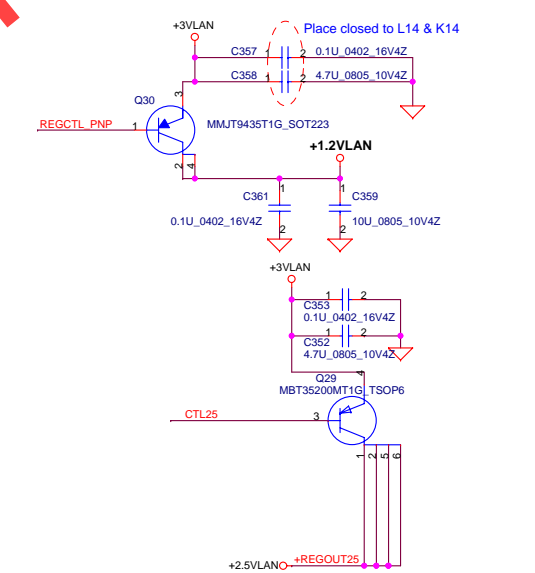
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



**Layout Notice : Place as close chip as possible.**

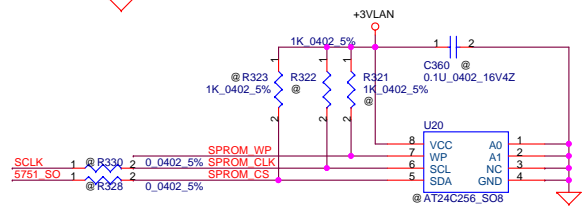


R884, R864 stuff if U61 is installed



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

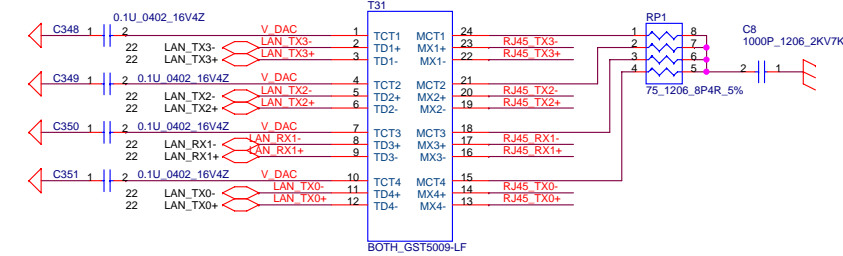
**Layout Notice : Filter place as close chip as possible.**



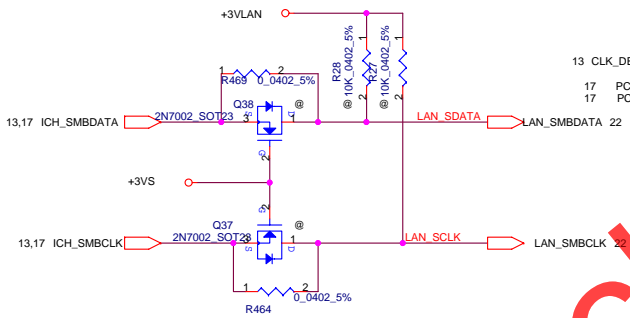
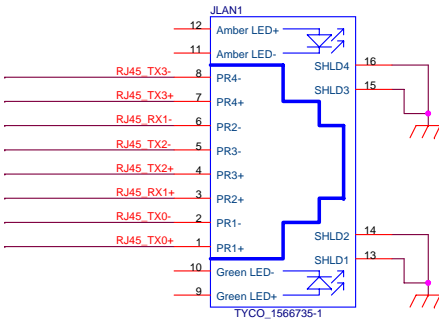




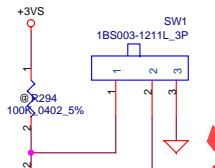
1. ES2 by rework form 0805 to 0603
2. Part name will modify in next phase



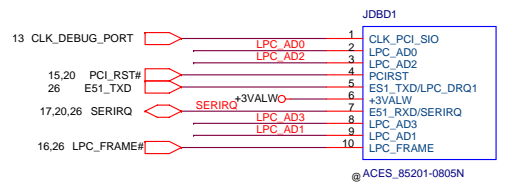
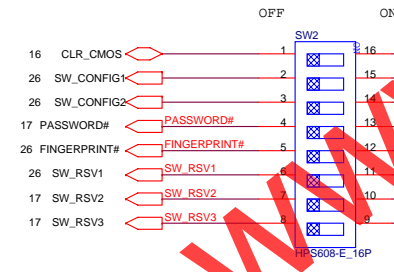
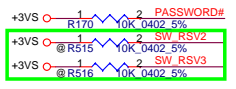
**Layout Note**  
24HST1041A-3 pls close to conn.



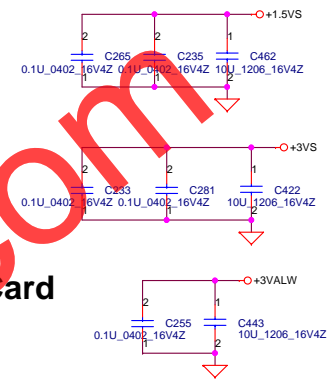
**Wireless\_BTN**  
Killer switch



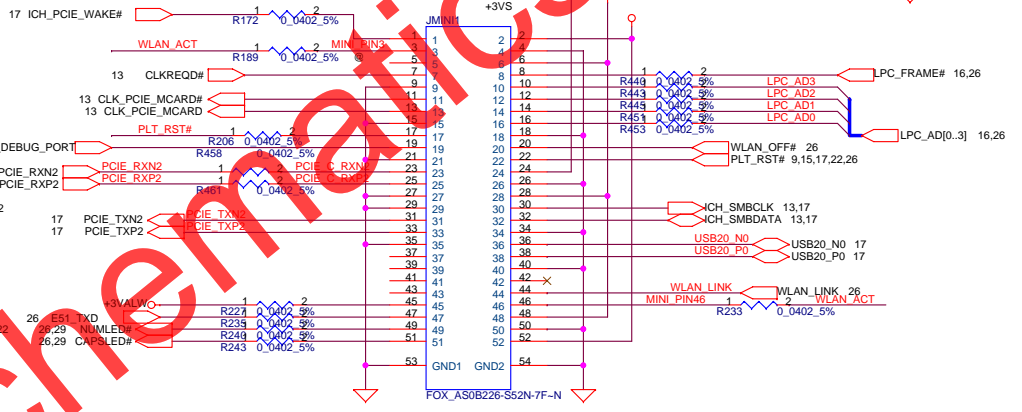
All 49.9 ohm + 0.1 uF termination components close to BCM5751M



For DEBUG

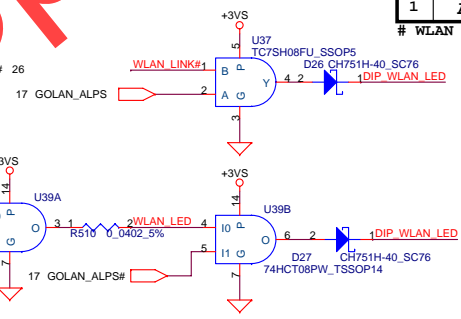


**Mini-Express Card**

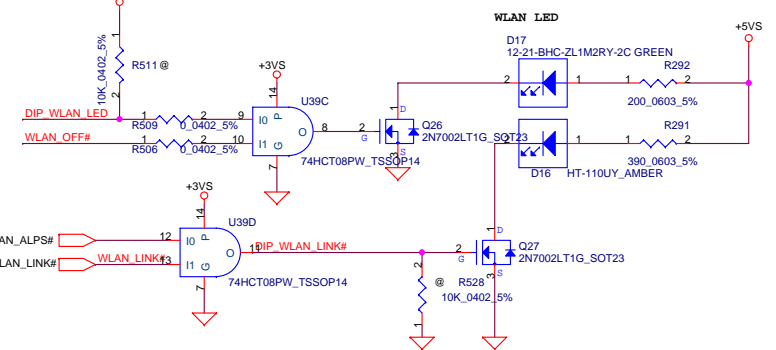


GOLAN_ALPS#	
0	GOLAN
1	ALPS

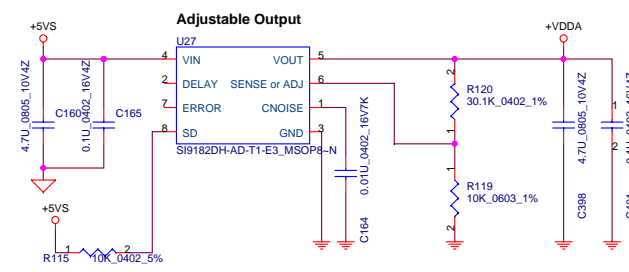
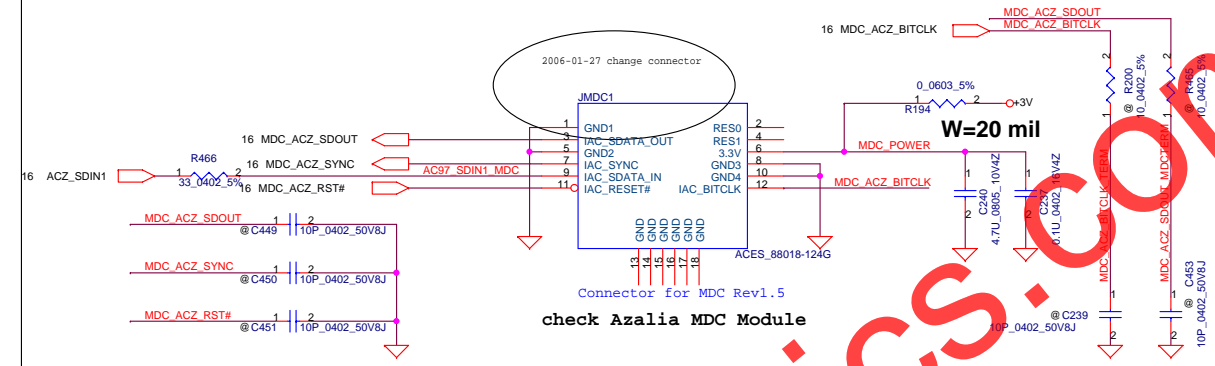
# WLAN detect by BIOS and program GOLAN\_ALPS# to control WLAN LED



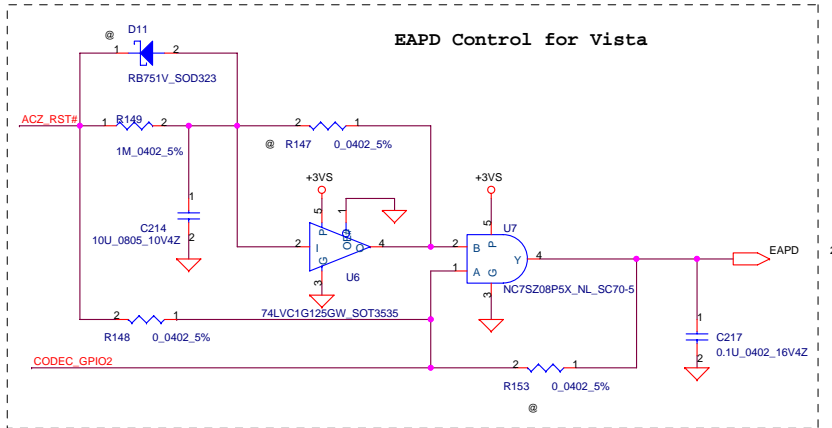
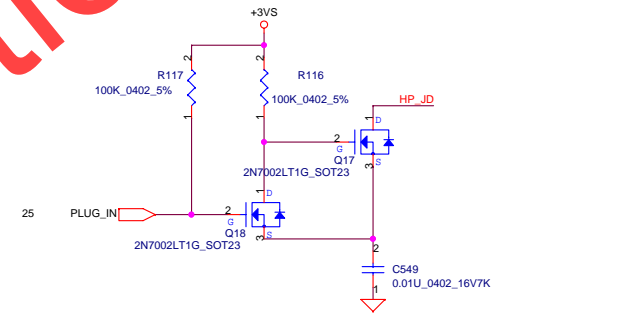
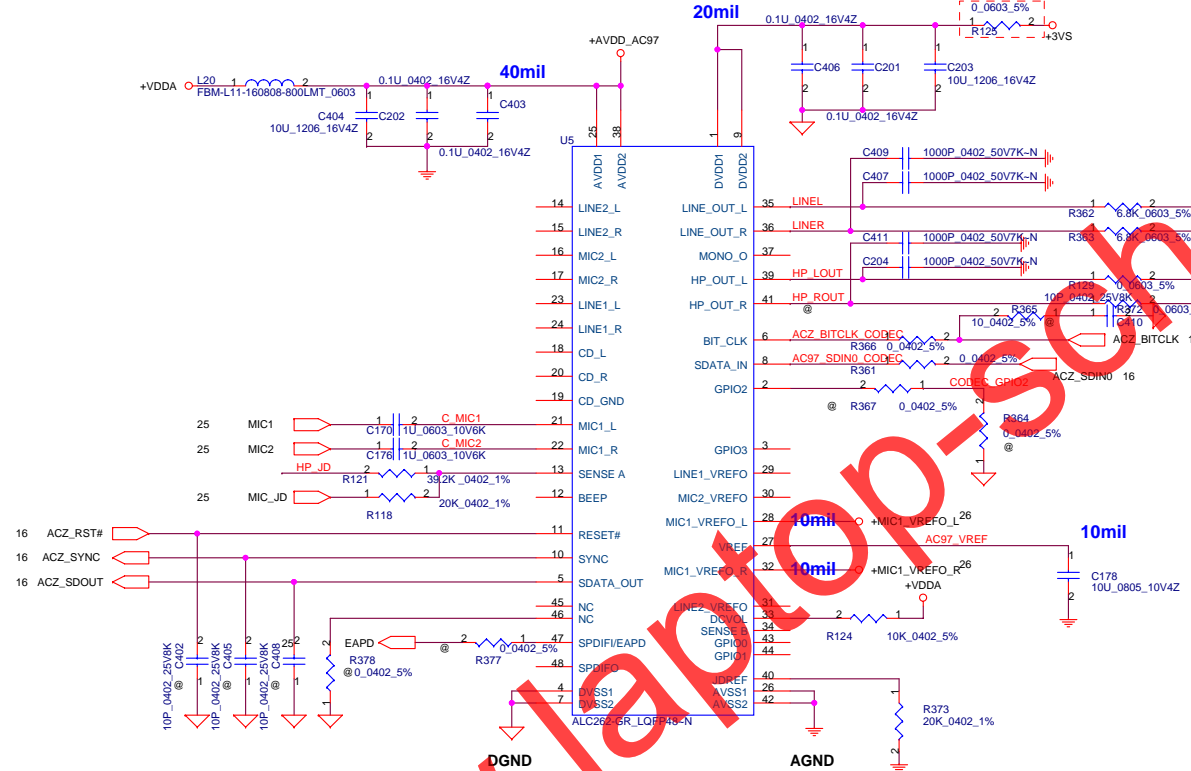
D1 Pin3 Open PAST & MASK layer



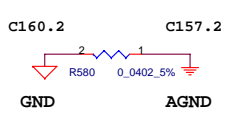
## MDC CONN.



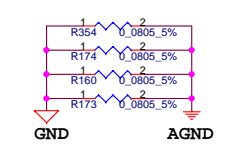
## HD Audio Codec



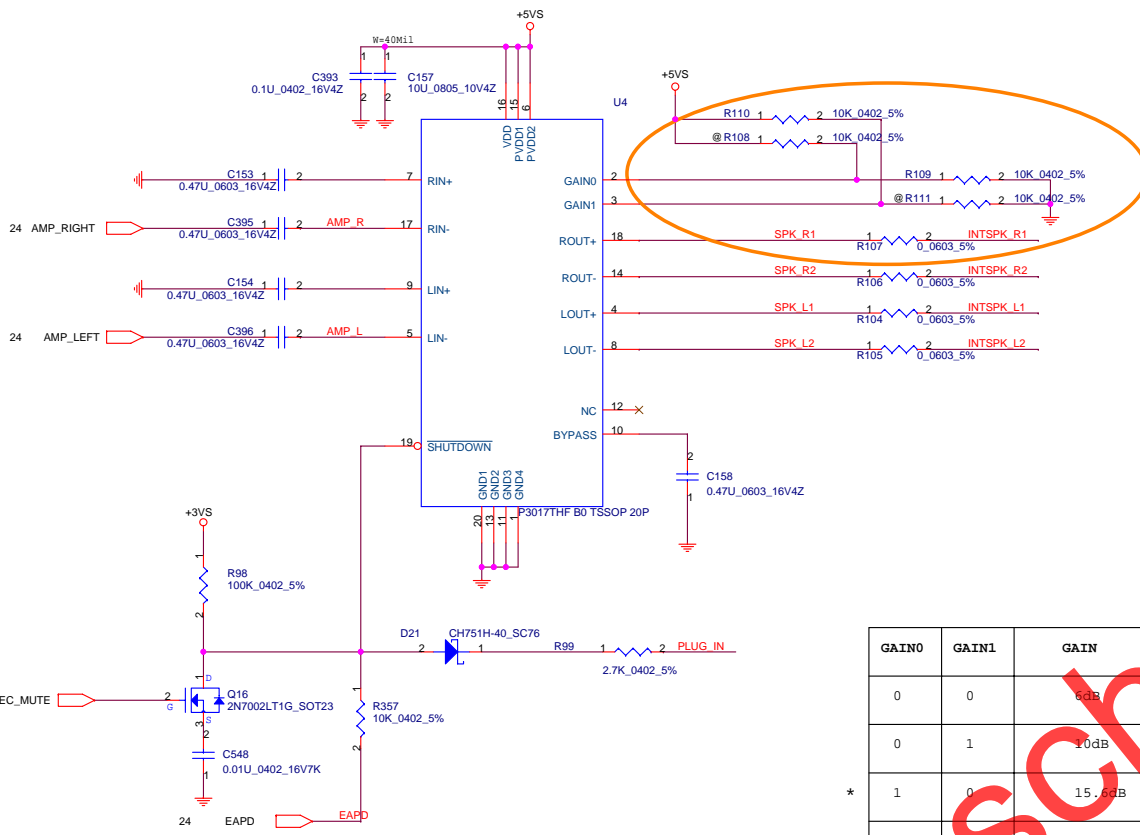
**Reserved for EMI**



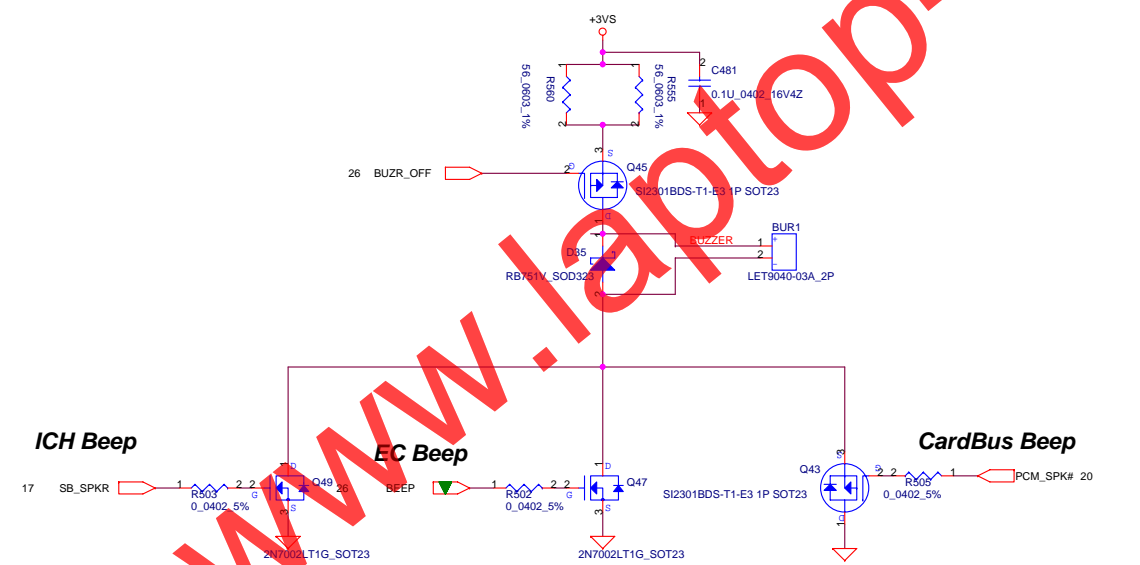
**Reserved for TEST**



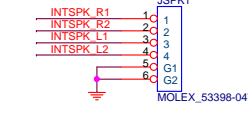
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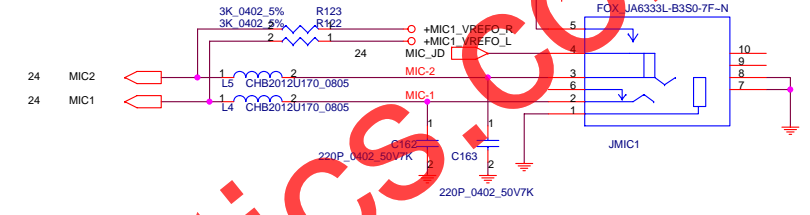
Buzzer need to support ICH/PCM\_SPK/Battery\_low and WL\_on/off



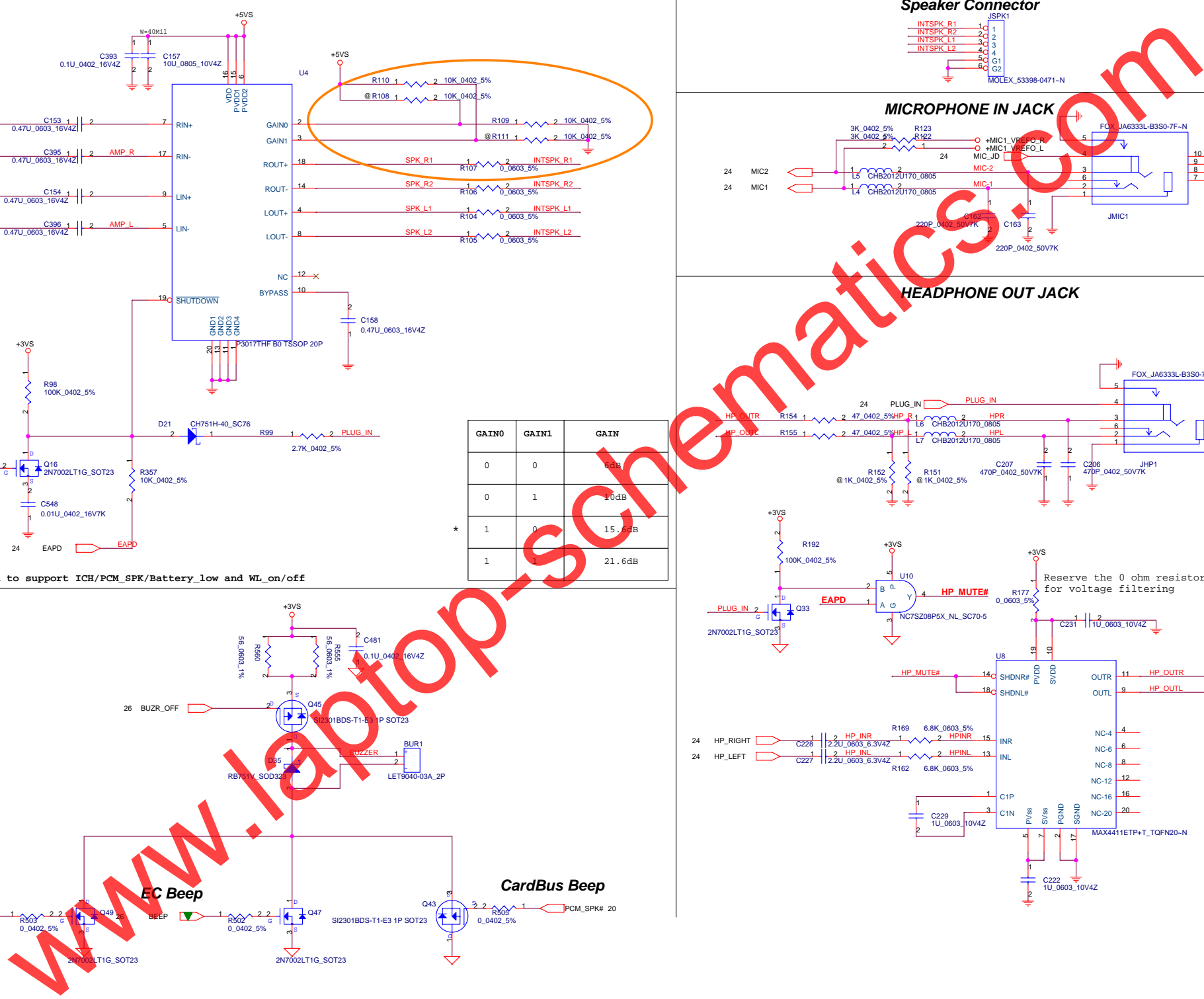
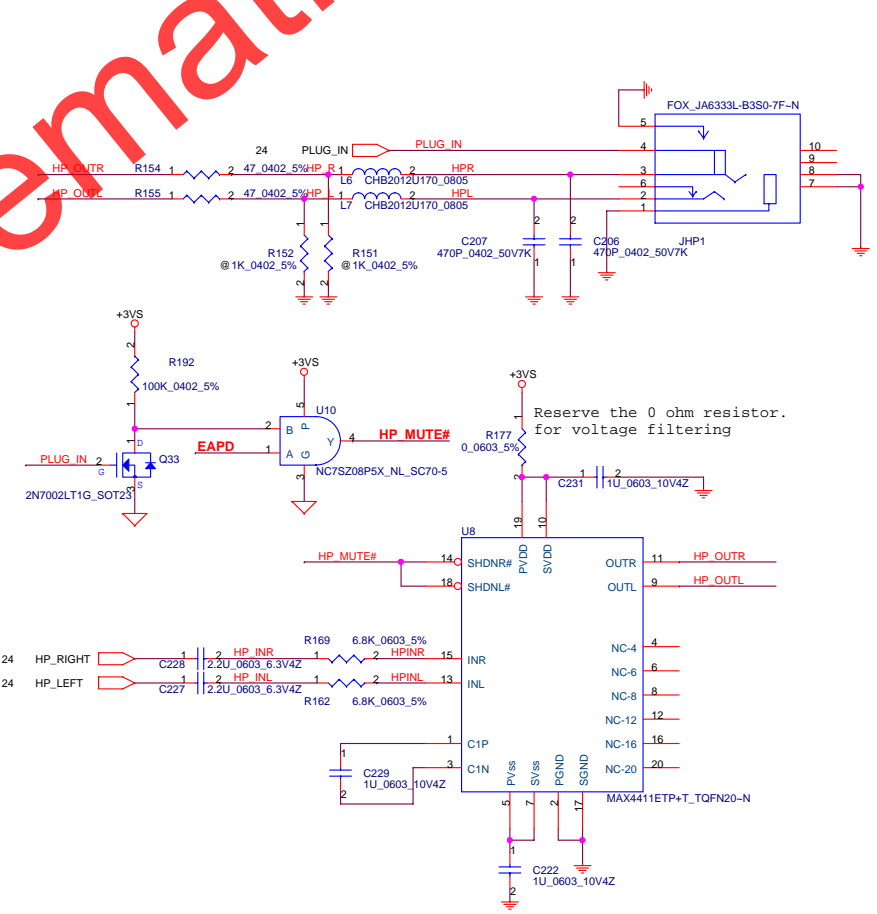
### Speaker Connector

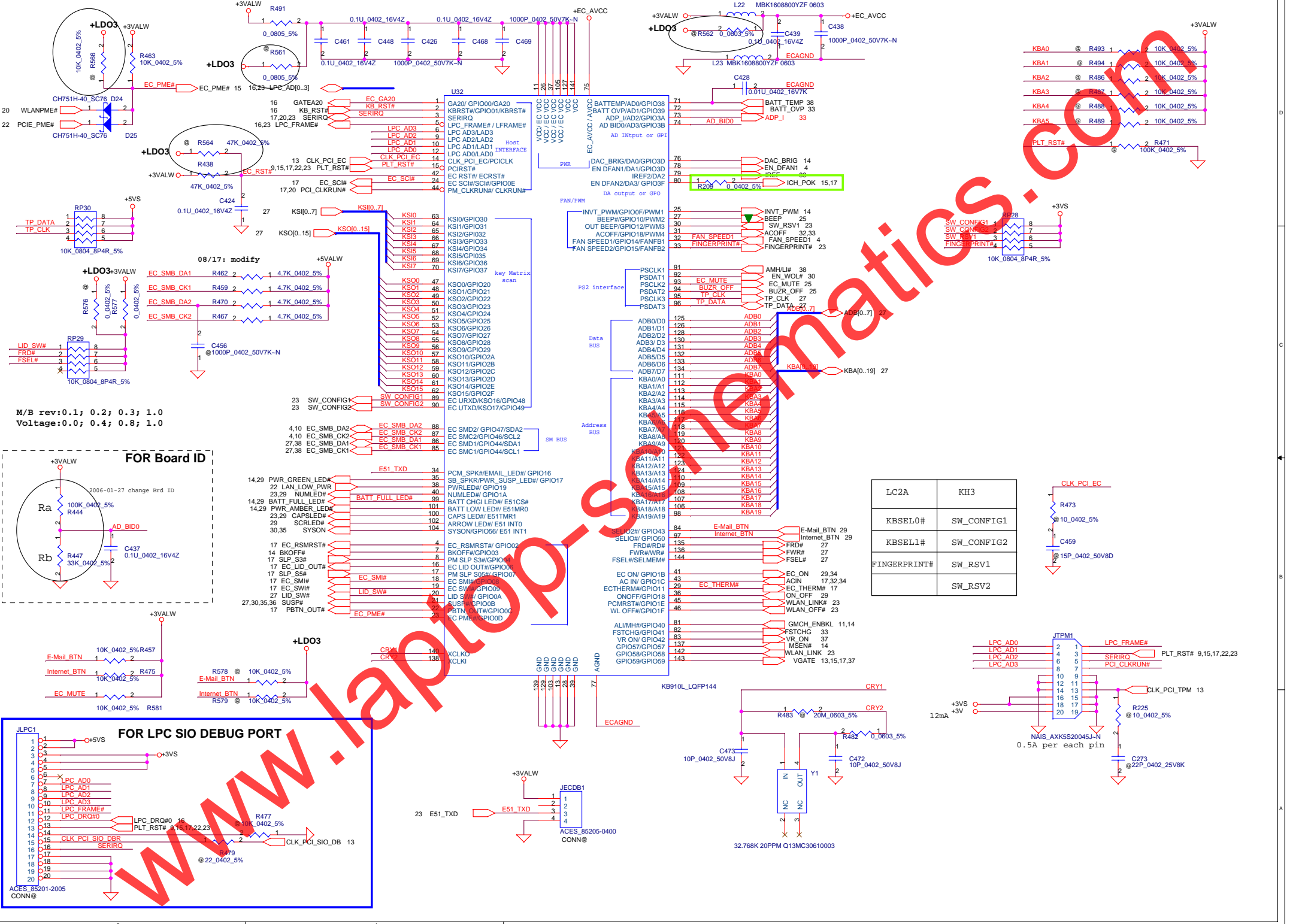


### MICROPHONE IN JACK



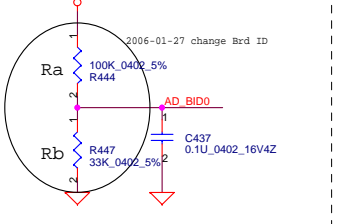
### HEADPHONE OUT JACK



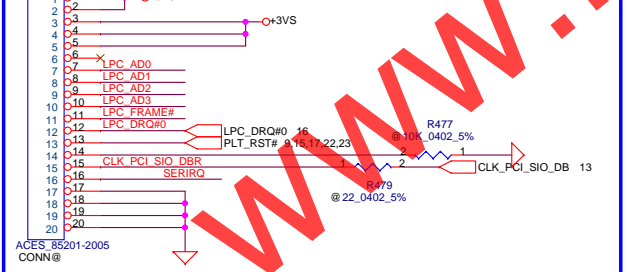


M/B rev:0.1; 0.2; 0.3; 1.0  
 Voltage:0.0; 0.4; 0.8; 1.0

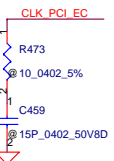
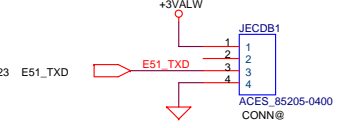
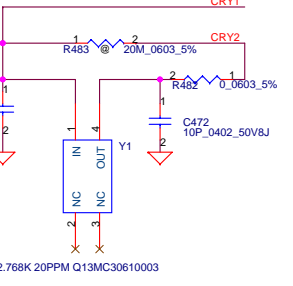
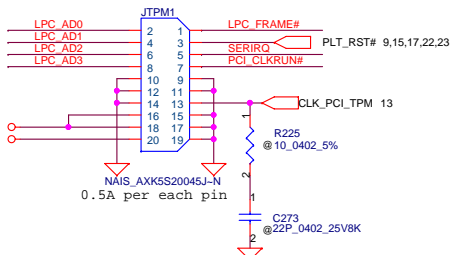
**FOR Board ID**

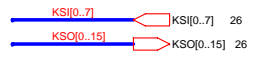
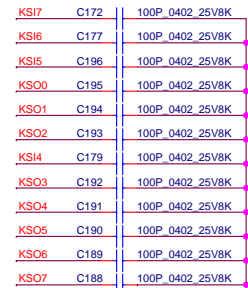
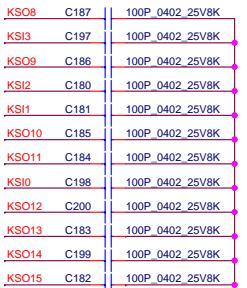


**FOR LPC SIO DEBUG PORT**



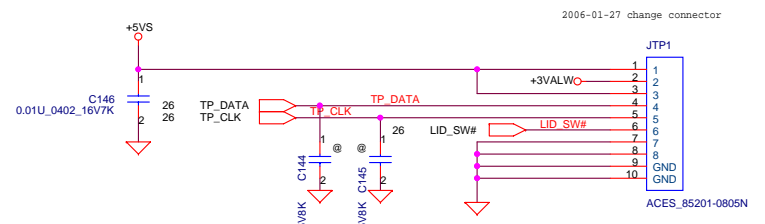
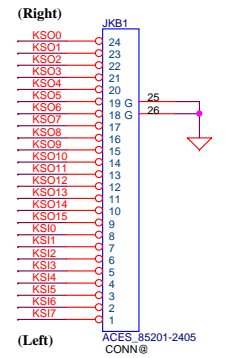
LC2A	KH3
KBSEL0#	SW_CONFIG1
KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RS1
	SW_RS2



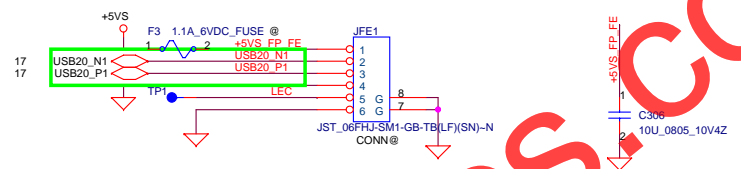


INT\_KBD\_CONN.

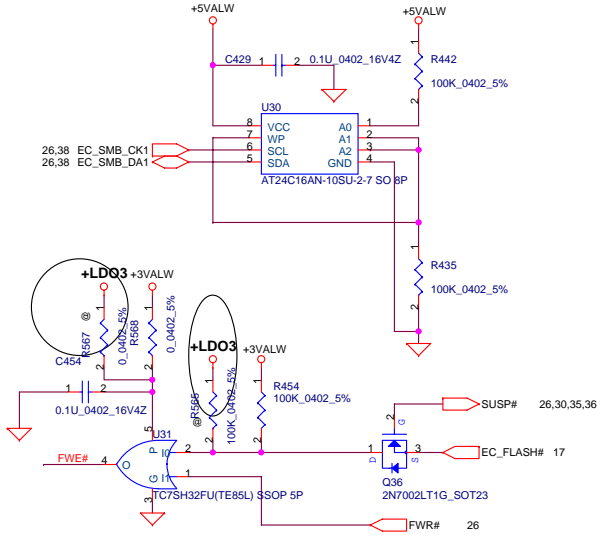
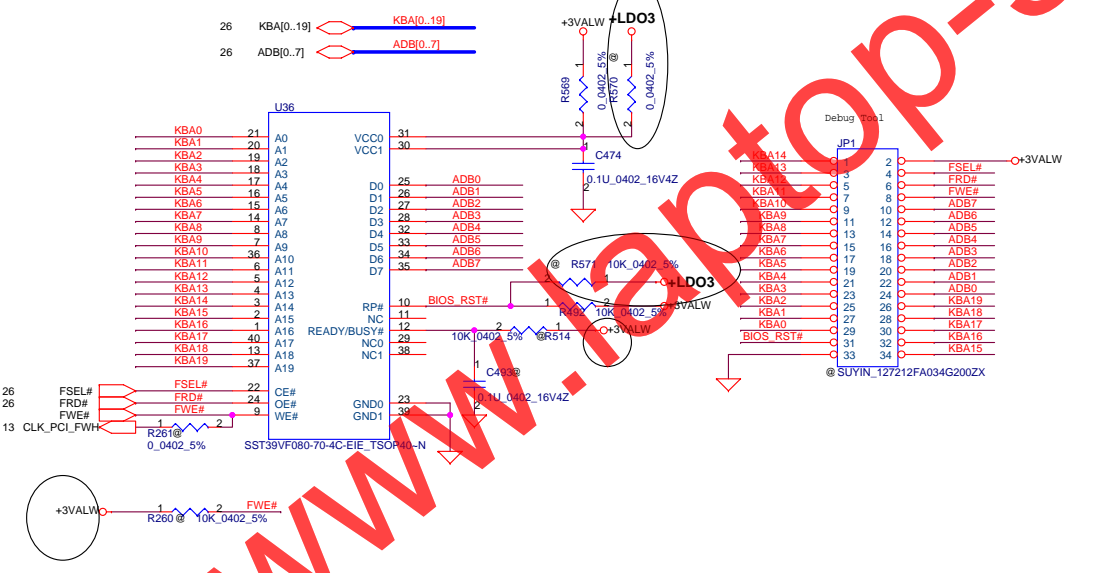
TO M/B

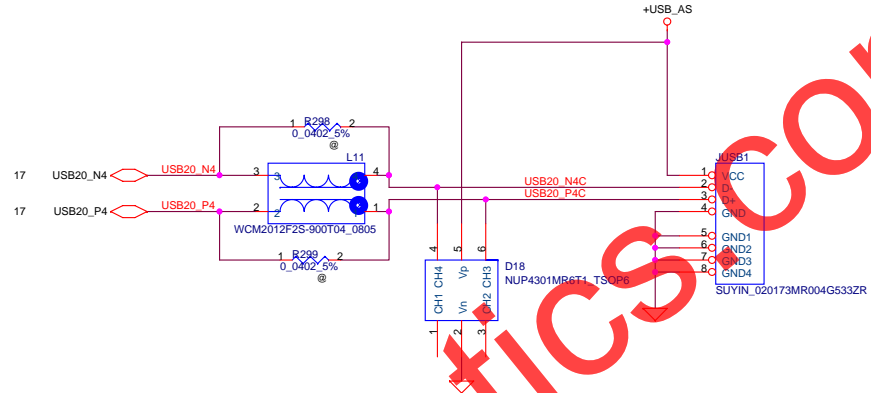
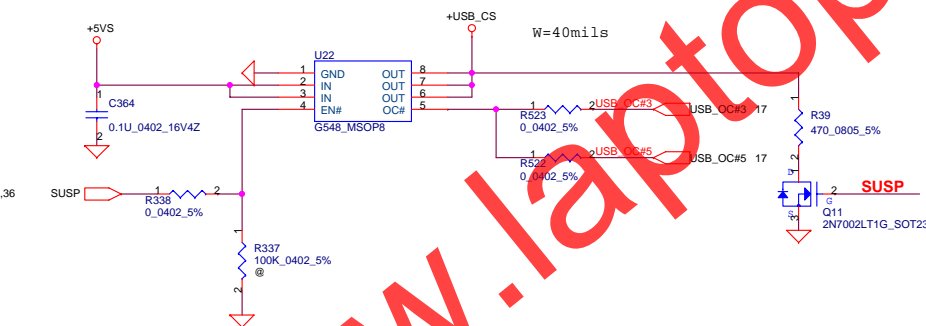
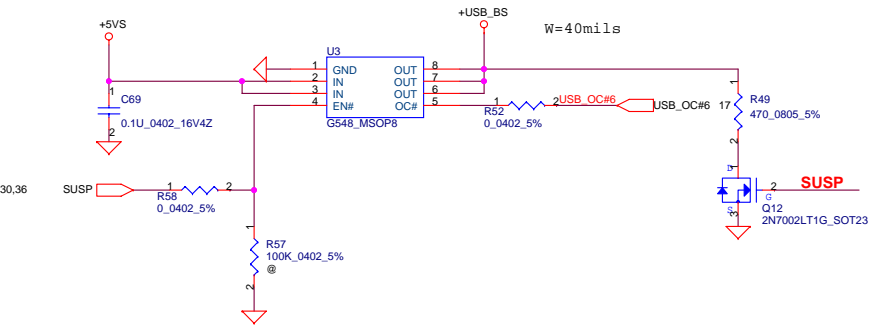
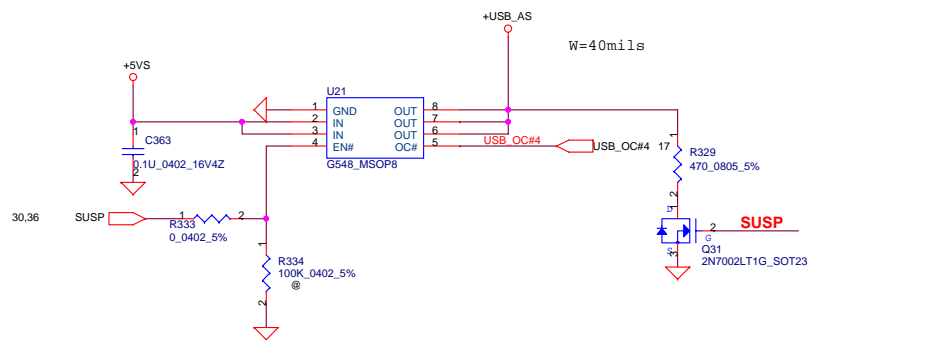


Felica Conn

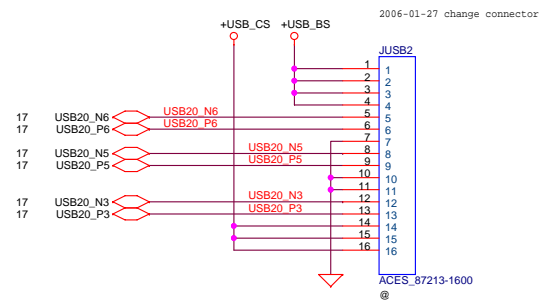
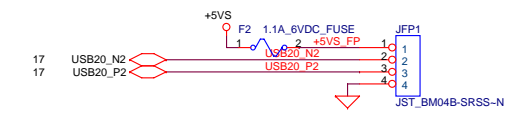


1M Byte BIOS ROM





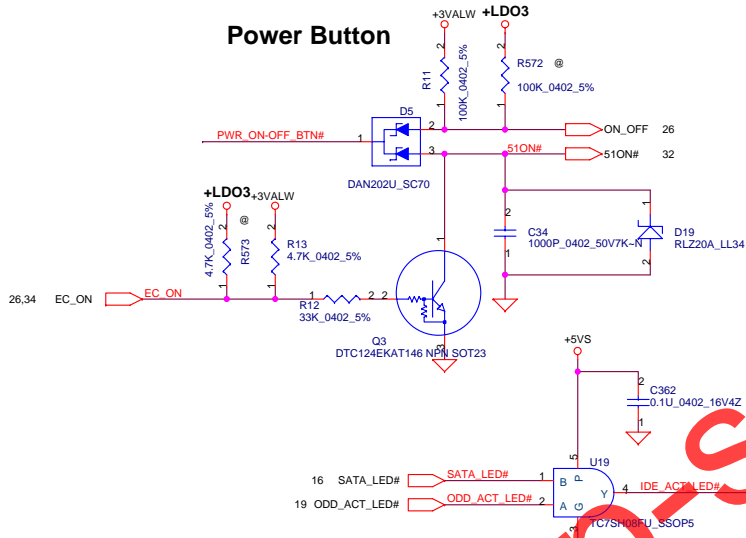
**FINGERPRINT**



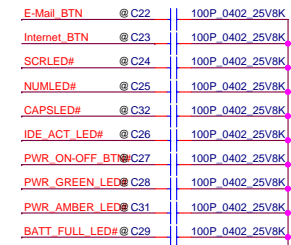
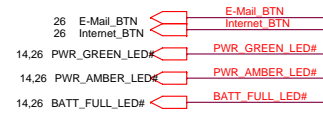
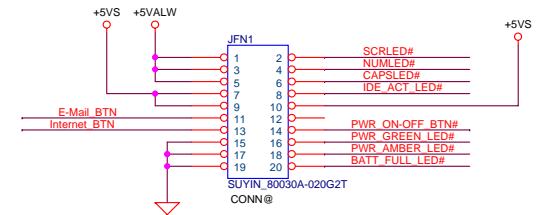
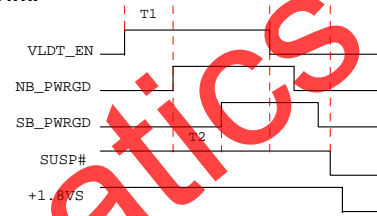
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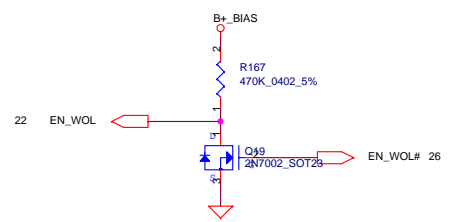
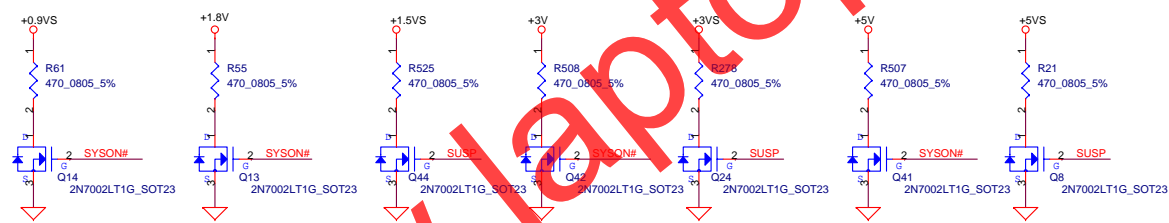
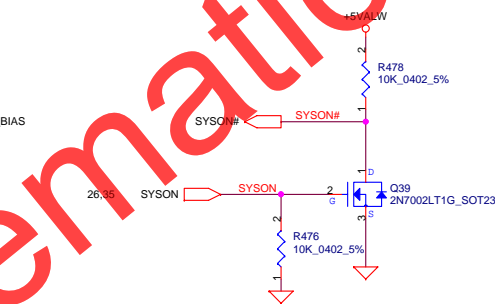
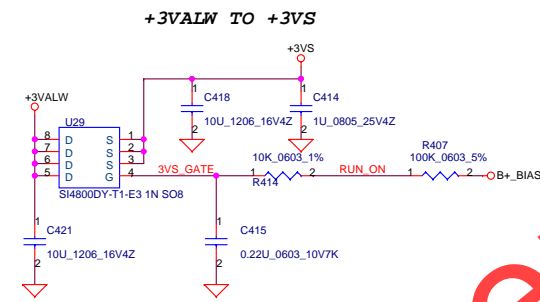
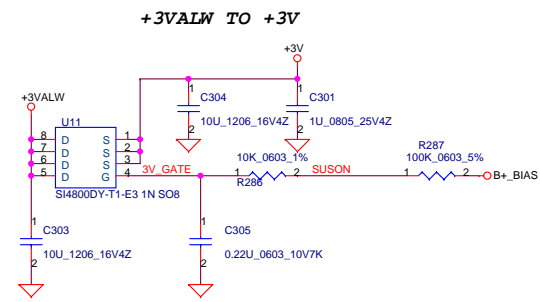
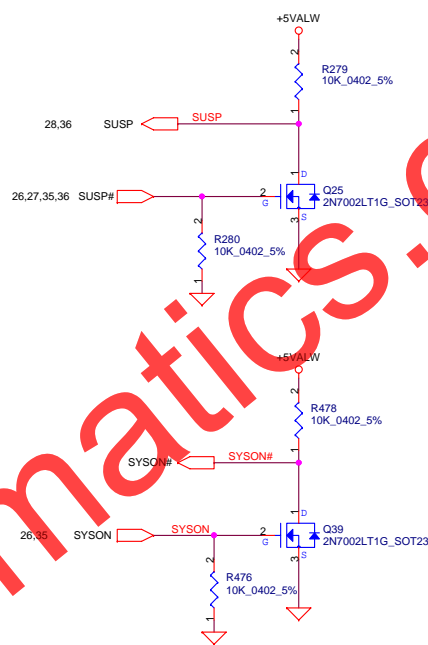
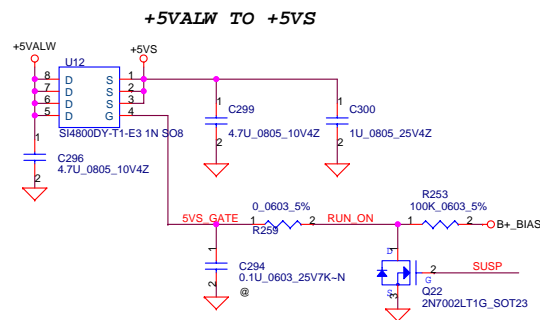
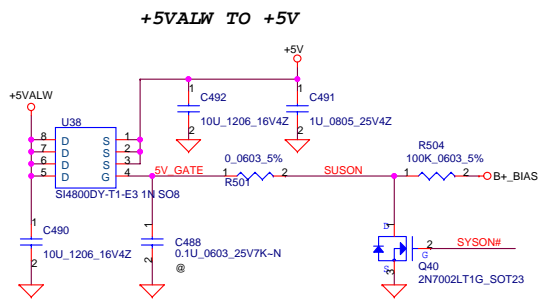
### Power Button



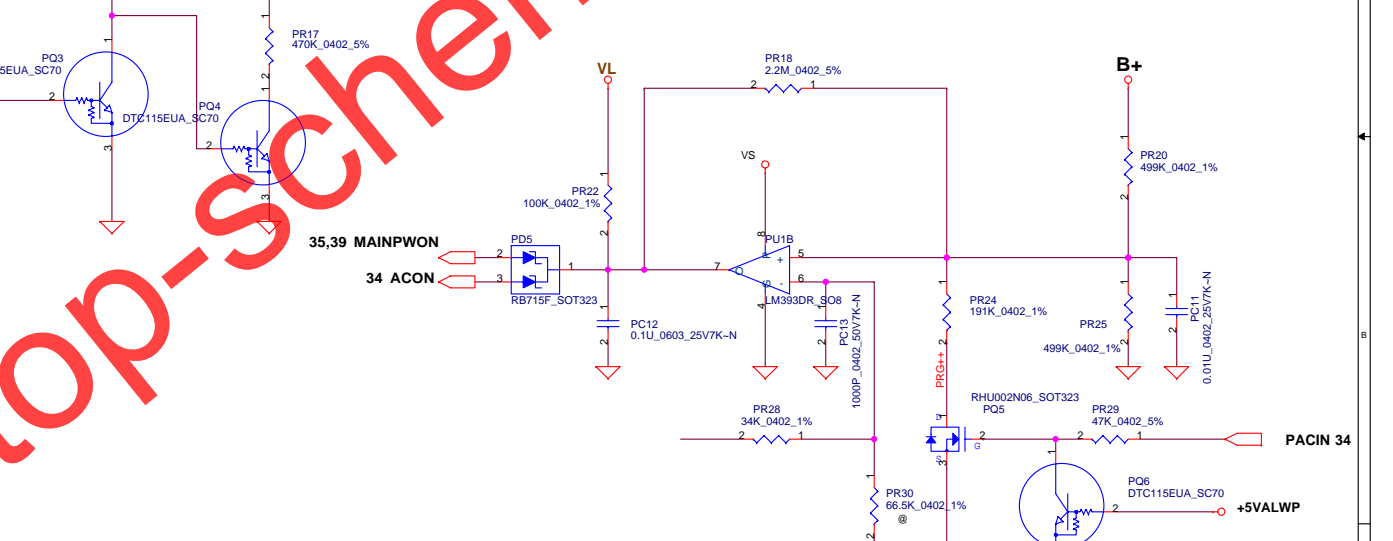
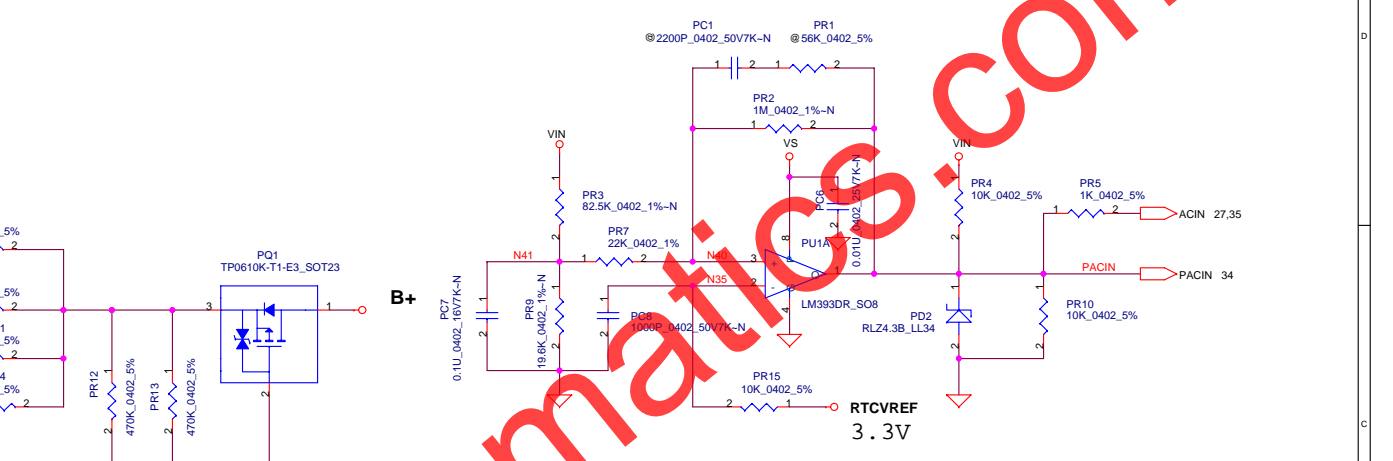
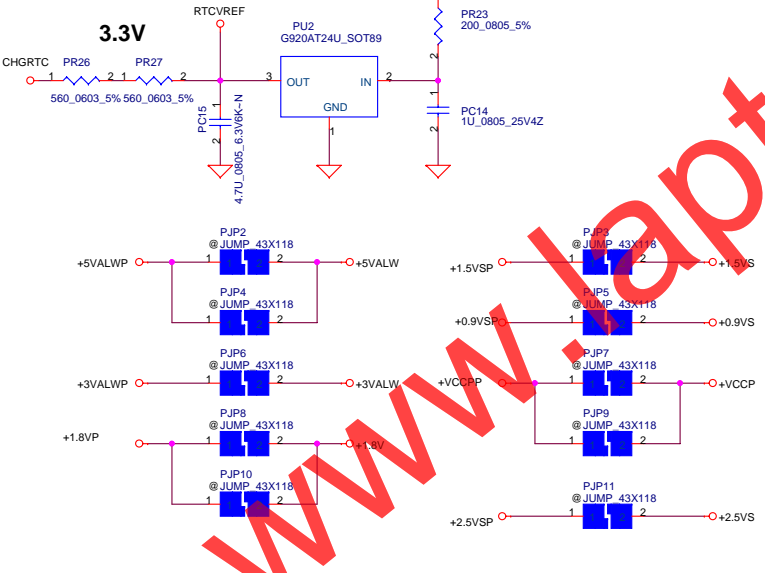
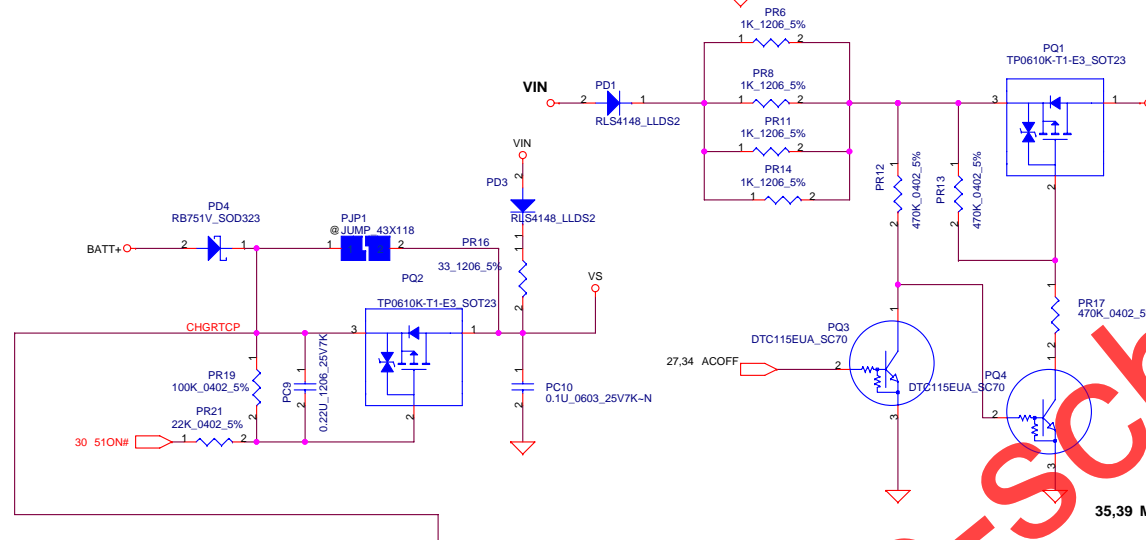
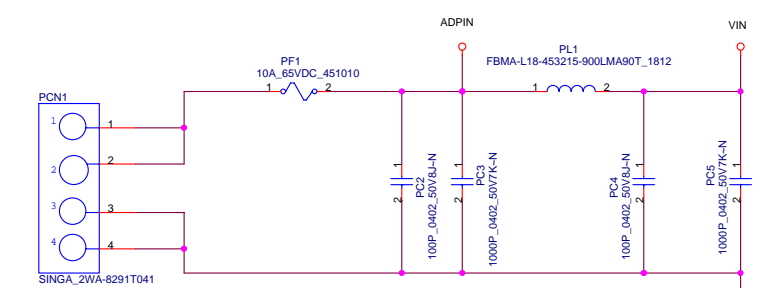
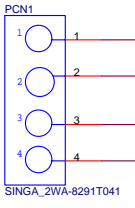
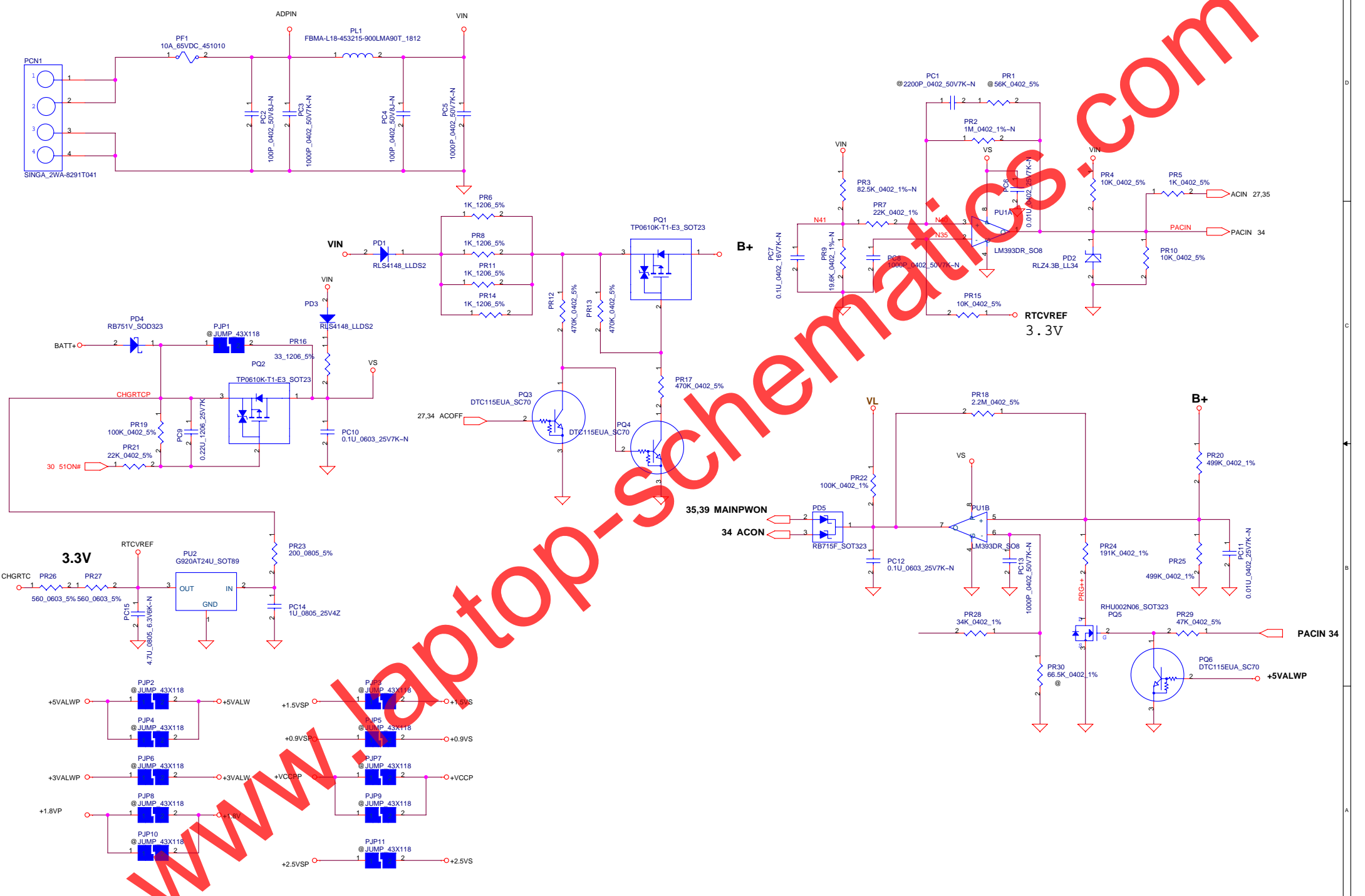
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,  
SUSP# goes to low after SB\_PWRGD goes to low for power down.



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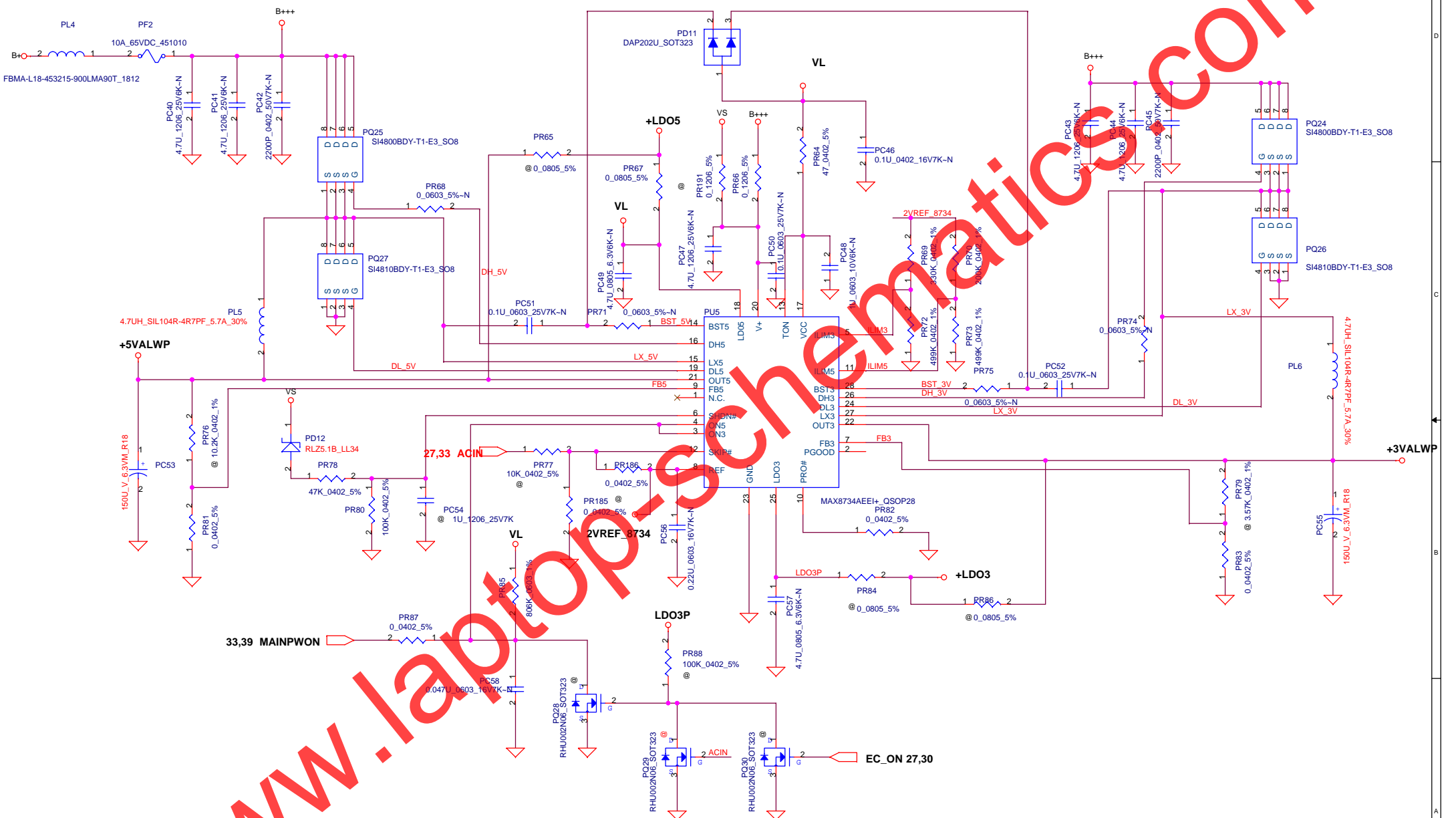
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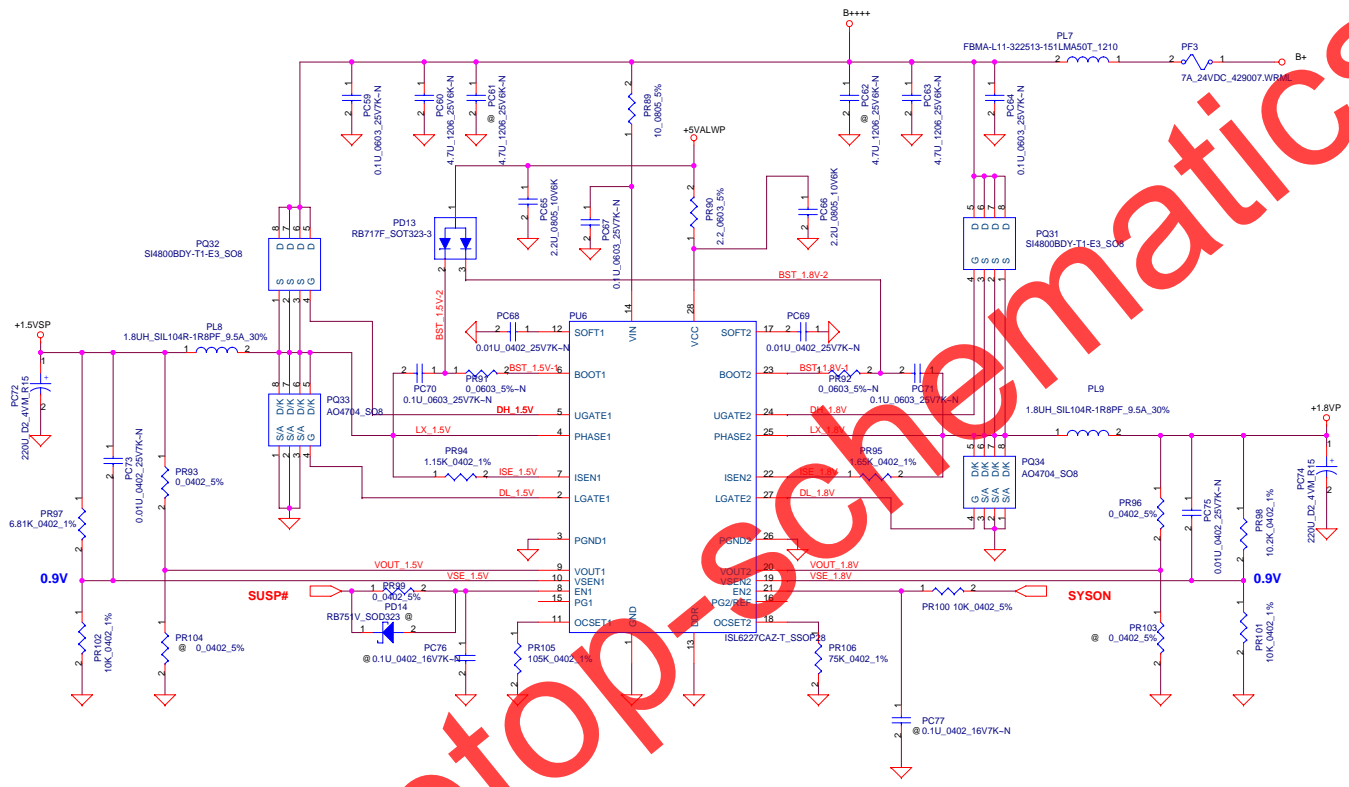


+3.3VALWP/+5VALWP

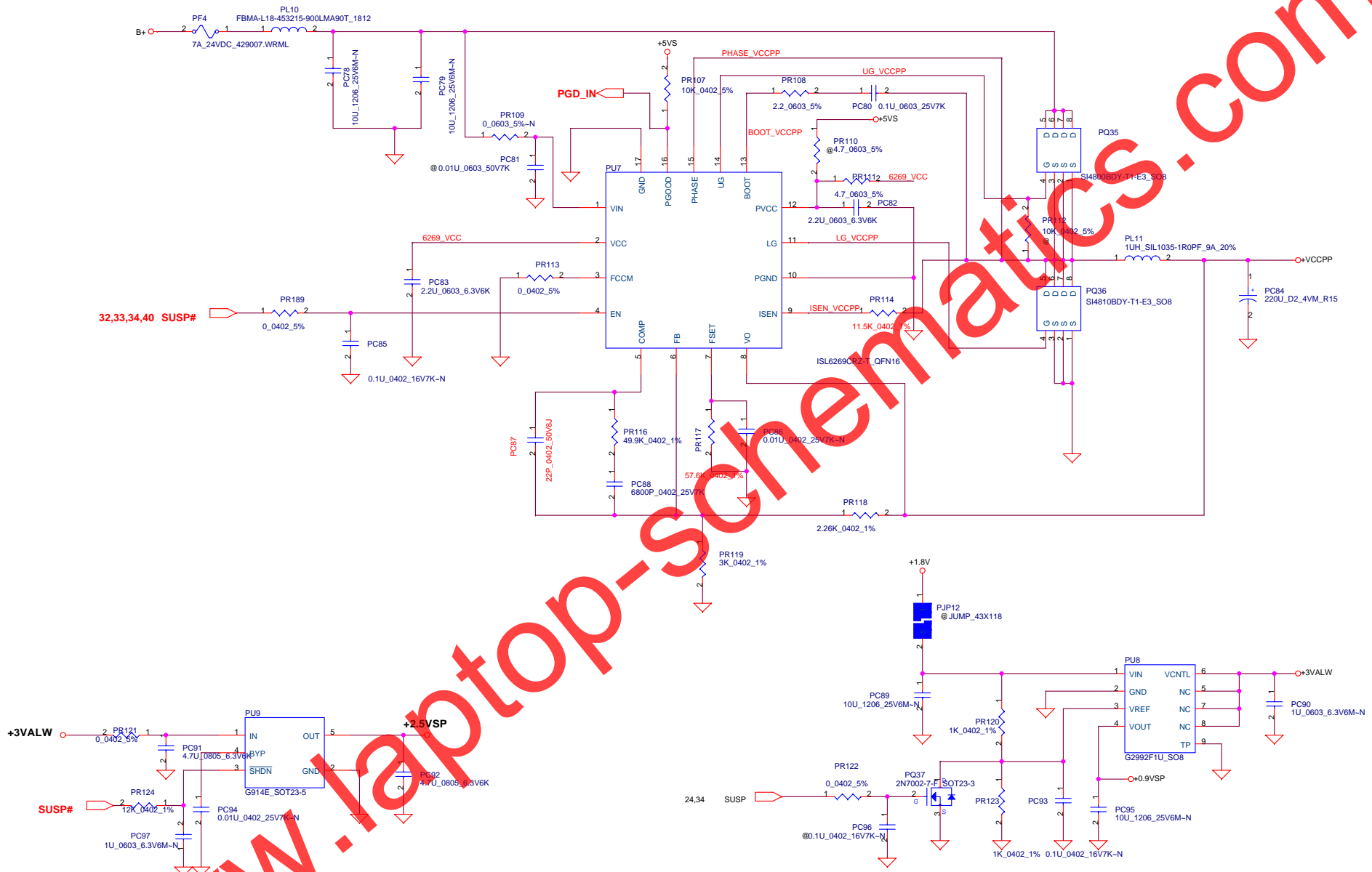


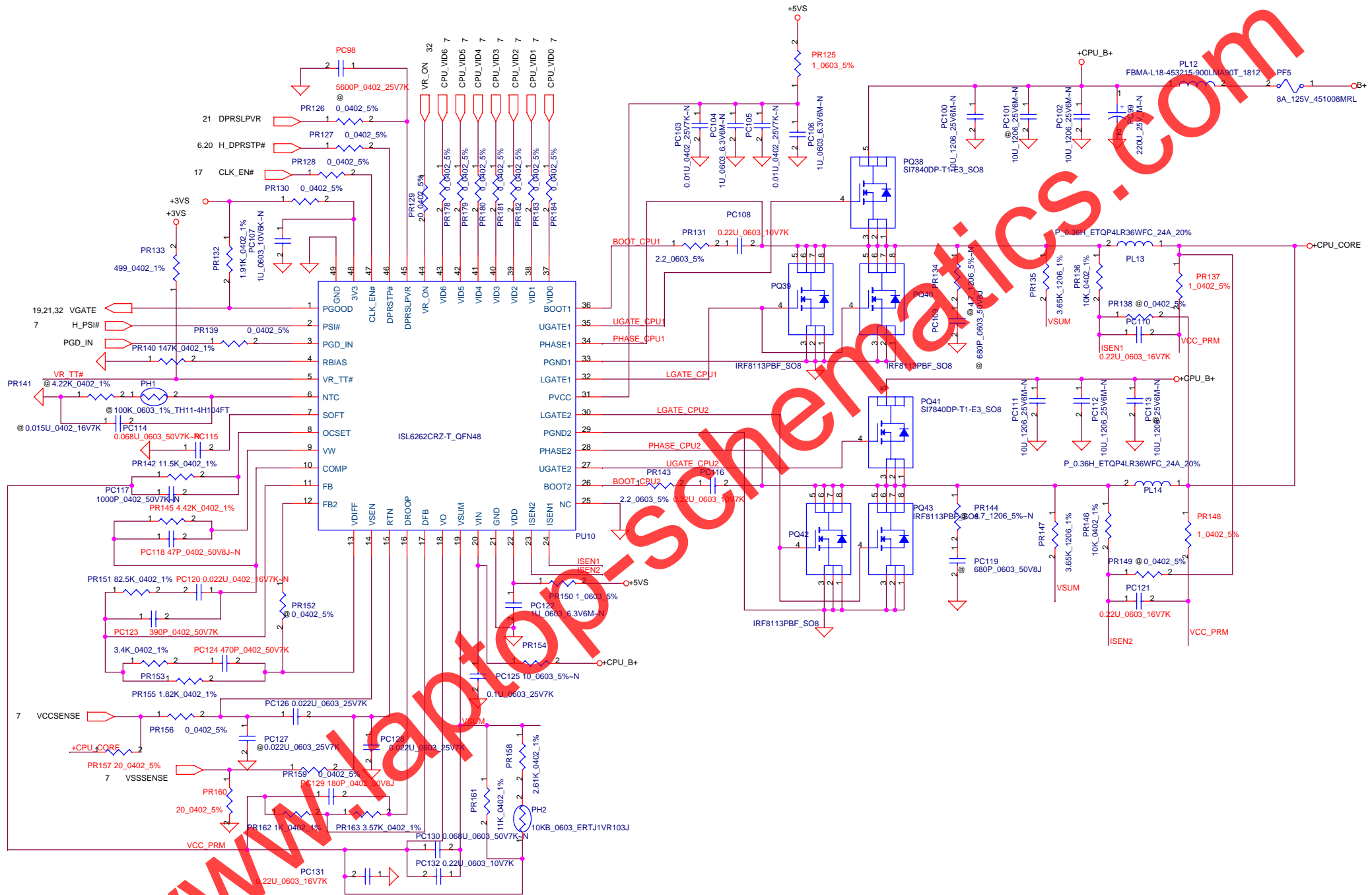
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www.laptopcircuitdiagramatics.com



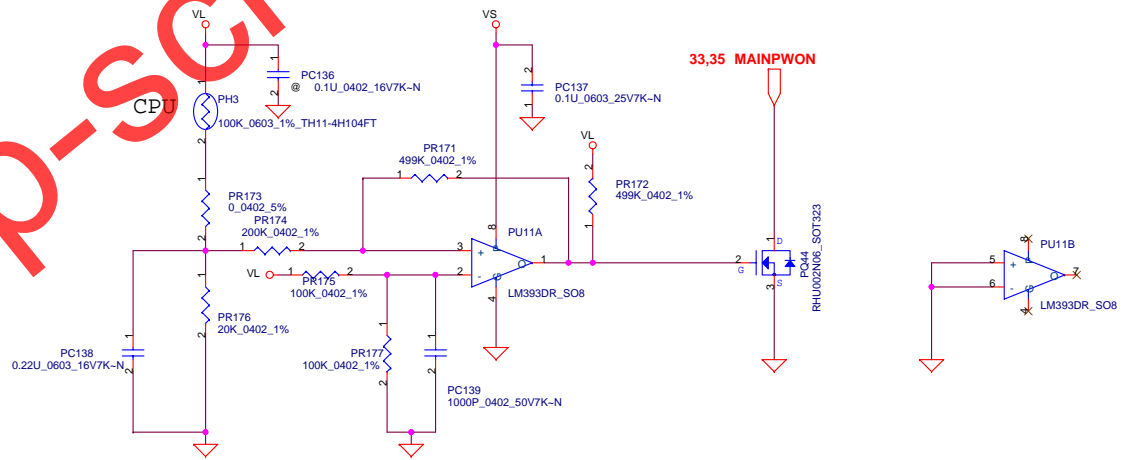
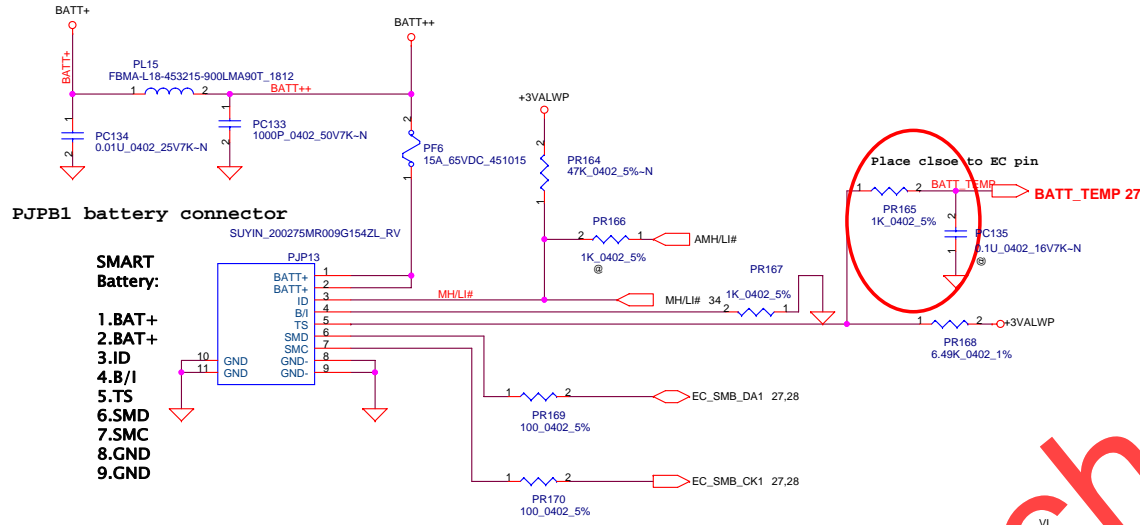






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Battery Connect/OTP



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