CT6 BLOCK DIAGRAM

Calistoga / Yonah /ICH-7m

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU Yonah/Merom
XXX Pins (uPGA)
PG 3,4

CPU THERMAL SENSOR
PG 5

14.318MHz

CLOCK GEN
IDTXXX/ ICSXXXX
56pins
PG 2

CPUCLK, CPUCLK#

SBLINKCLK, SBLINKCLK#
NBSRCCLK, NBSRCCLK#
HTREFCLK

HyperThansport I/O BUS
Link 16x16

OSC14M

NORTH BRIDGE Calistoga
XXX BGA
INTEGRADED VGA FUNCTION
PG 6,7,8,9,10,11

R.G,B
CRT port PG 29

LVDS X1
LCD Panel PG 18

TV-OUT
S-VIDEO PG 18

DDRII 266,333 MHz
DDRII-SODIMM1 PG 12,13

DDRII 266,333 MHz
DDRII-SODIMM2 PG 12,13

DMI LINK
2X PCI-E

32.768KHz

NBSRCCLK, NBSRCCLK#

33MHZ, 3.3V PCI

ICH-7m
XXX BGA
PG 14,15,16,17

PCLK_E

Azalia

24.576MHz

USB PORT 0, 1, 2 PG 21
USB 2.0

1st SATA - HDD PG 32
SATA 150MB

2nd IDE - CDROM PG 31
ATA 66/100/133

PWRCLKP
PWRCLKN
DIB_DATAN
DIB_DATAP

Azalia
CX20551-22
MBAMC20493-010
PG 22

LAN
Intel
Ekron
82562GT
PG 25

25MHz

MINI-Card PG 33

CARDREADER / IEEE 1394 CONTROLLER/CF
RICOH 832
PG 19,20,21

LPC
32.768KHz

PCLK_E
3.3V LPC, 33MHz

PC87541L
TQFP XXX
PG 28

Express Card x1 NEW CARD PG 33

SMARTDAA MODEM, PG 24

AMP
TPA0312
PG 23

WIRE

5 IN 1
CARD READER
SD/MMC, SM, MS, XD
PG 21

1394 CONN PG 20

FAN PG 29

Touchpad PG 31

Keyboard PG 31

FLASH PG 27

RJ11 JACK PG 24

JACK
HEADPHONE, 2ND HEADPHONE, MIC
PG 23

RJ45 JACK PG 25

CABLE DOCK PG 30

Daughter Board
TV, USB, BLUE TOOTH
PG 31

Power Board PG 31

SYSTEM POWER MAX1845 (1.2V/NB_CORE/1.25V) PG 38

CPU CORE MAX1544 POWER VCORE 1.2V /44A PG 39

SYSTEM MAX1999 POWER(3/5V) PG 36

SYSTEM POWER MAX1845 (1.8VSUS/0.9V SMDDR_VREF) PG 37

BATT CHARGER MAX1722 PG 35

DISCHARGE PG 34

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
INTEL ETHERNET	AD24 (D8)		C(A~E)
MINIPCI SLOT	AD22	1	C,D
CardBus/1394	AD25	0	E,F,G

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1B
Date: Friday, September 23, 2005	Sheet 1 of 44	

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

25 mils

L32 ACB2012L-120-T

120 ohms@100Mhz

SMbus address D2 /IDT

Close to IC <500mils

Y4 14.318MHZ CL=20 - 22P

CK-410M

ICS954206AG-

Use 33R/1%

Place these termination to close CK410M.

Use 1% R

BSEL strappings need to be set for 533MHz Moby Dick (Intel?915GM - Calistoga Interposer)
(if Calistoga is designed for 667MHz board).

Stuff 0 ohm for 533MHz, NC for 667MHz

DREFSSCLK Frequency Select.
"0" : 96MHz
"1" : 100MHz

IDT CV140 /56pins
ICS954206AGT /56pins

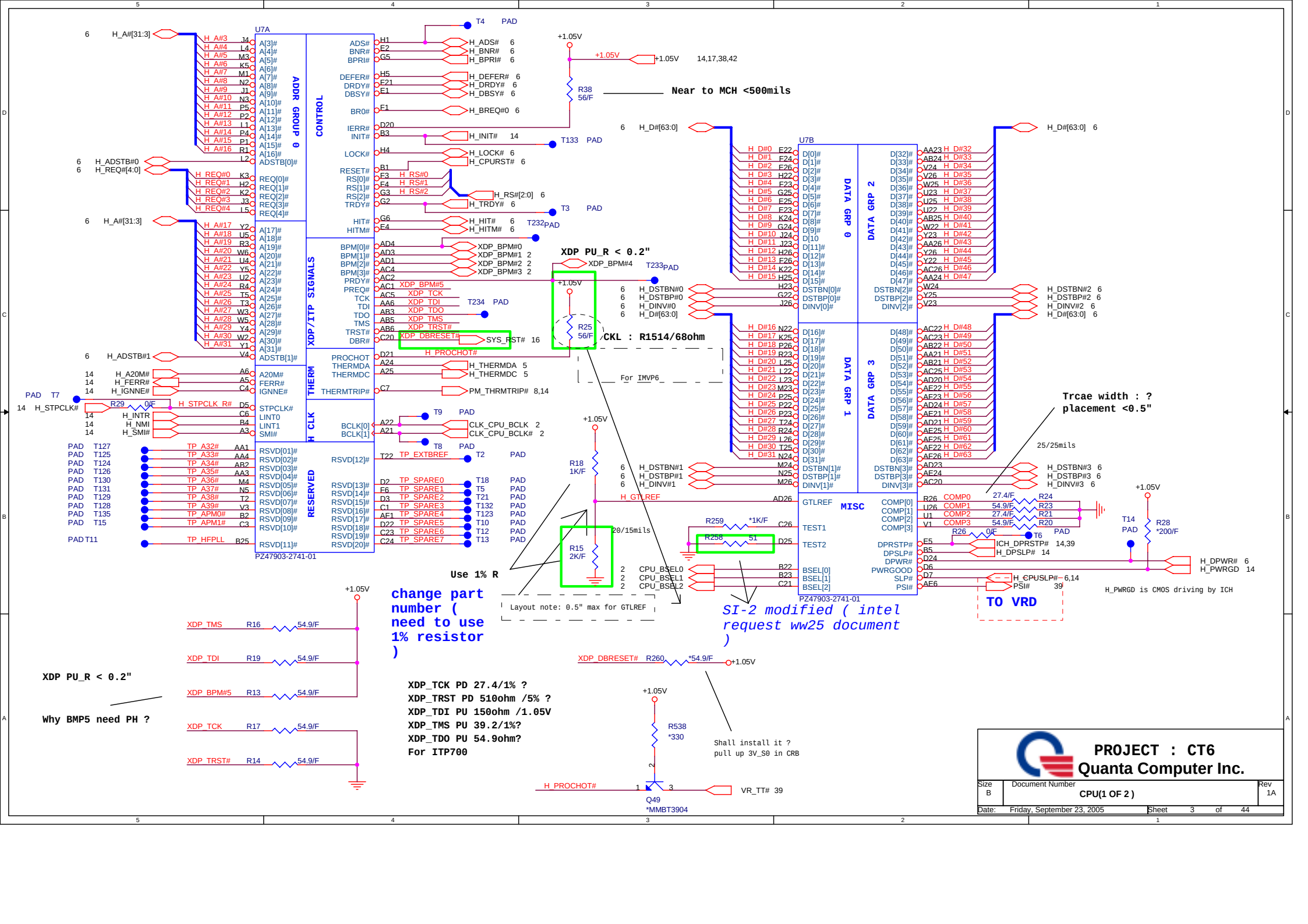
Cross moat

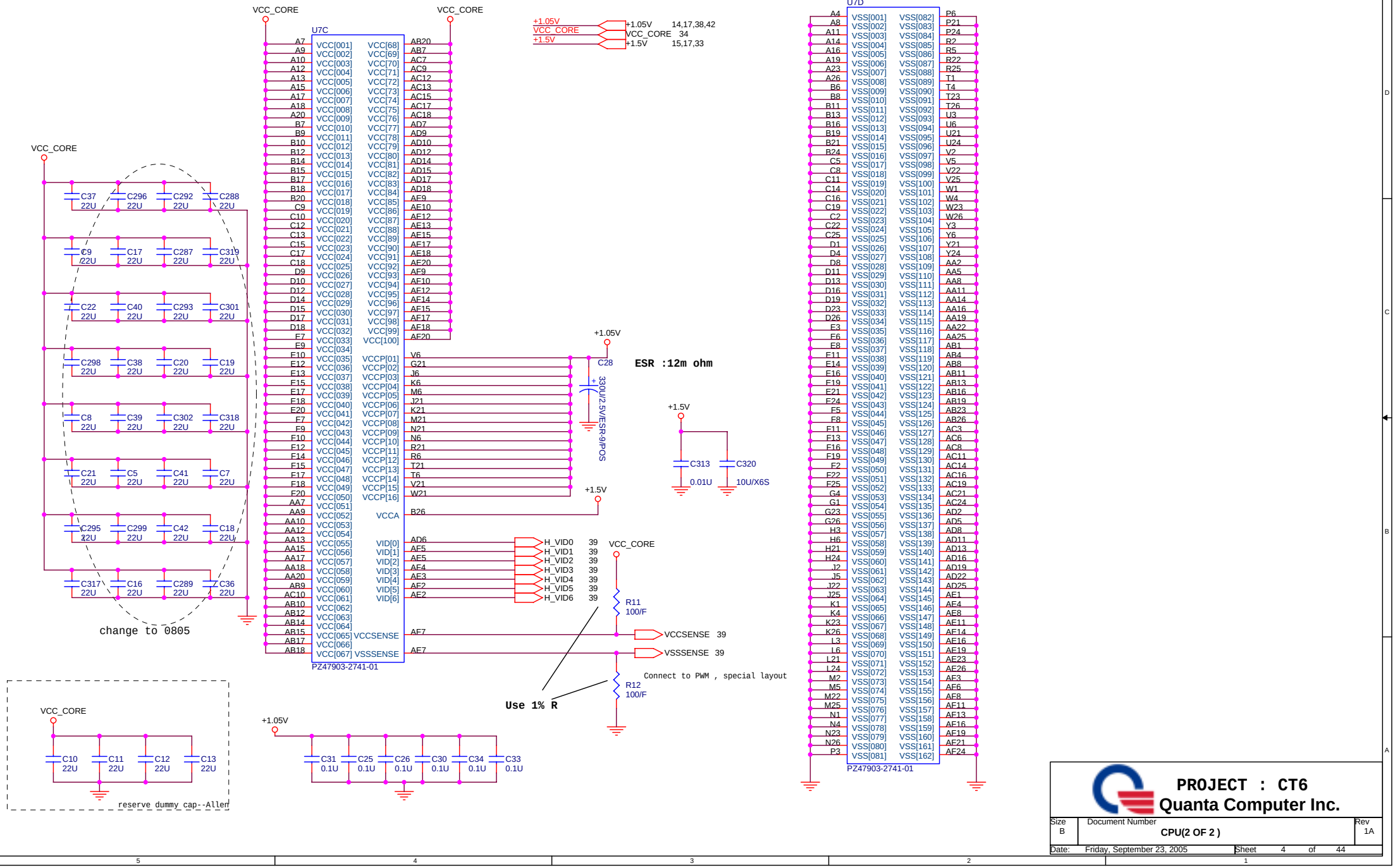
Check Intel

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Friday, September 23, 2005 Sheet 2 of 44


U7A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U7B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to MCH <500mils
XDP PU_R < 0.2"
CKL : R1514/68ohm
For IMVP6
Trcae width : ?
placement <0.5"
25/25mils
Use 1% R
change part number (need to use 1% resistor)
Layout note: 0.5" max for GTLREF
SI-2 modified (intel request ww25 document)
TO VRD
H_PWRGD is CMOS driving by ICH
XDP PU_R < 0.2"
Why BMP5 need PH ?
XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700
Shall install it ?
pull up 3V_S0 in CRB
*MMBT3904
PROJECT : CT6
Quanta Computer Inc.
CPU(1 OF 2)
Friday, September 23, 2005


VCC_CORE
U7C
PZ47903-2741-01
U7D
PZ47903-2741-01
+1.05V
VCC_CORE
+1.5V
+1.05V 14,17,38,42
VCC_CORE 34
+1.5V 15,17,33
C37 22U
C296 22U
C292 22U
C288 22U
C9 22U
C17 22U
C287 22U
C319 22U
C22 22U
C40 22U
C293 22U
C301 22U
C298 22U
C38 22U
C20 22U
C19 22U
C8 22U
C39 22U
C302 22U
C318 22U
C21 22U
C5 22U
C41 22U
C7 22U
C295 22U
C299 22U
C42 22U
C18 22U
C317 22U
C16 22U
C289 22U
C36 22U
change to 0805
C28
330U/2.5V/ESR-9/POS
ESR :12m ohm
C313 0.01U
C320 10U/X6S
R11 100/F
R12 100/F
VCCSENSE 39
VSSSENSE 39
Use 1% R
Connect to PWM , special layout
C31 0.1U
C25 0.1U
C26 0.1U
C30 0.1U
C34 0.1U
C33 0.1U
C10 22U
C11 22U
C12 22U
C13 22U
reserve dummy cap--Allen
PROJECT : CT6
Quanta Computer Inc.
Size B
Document Number
CPU(2 OF 2)
Rev 1A
Date: Friday, September 23, 2005
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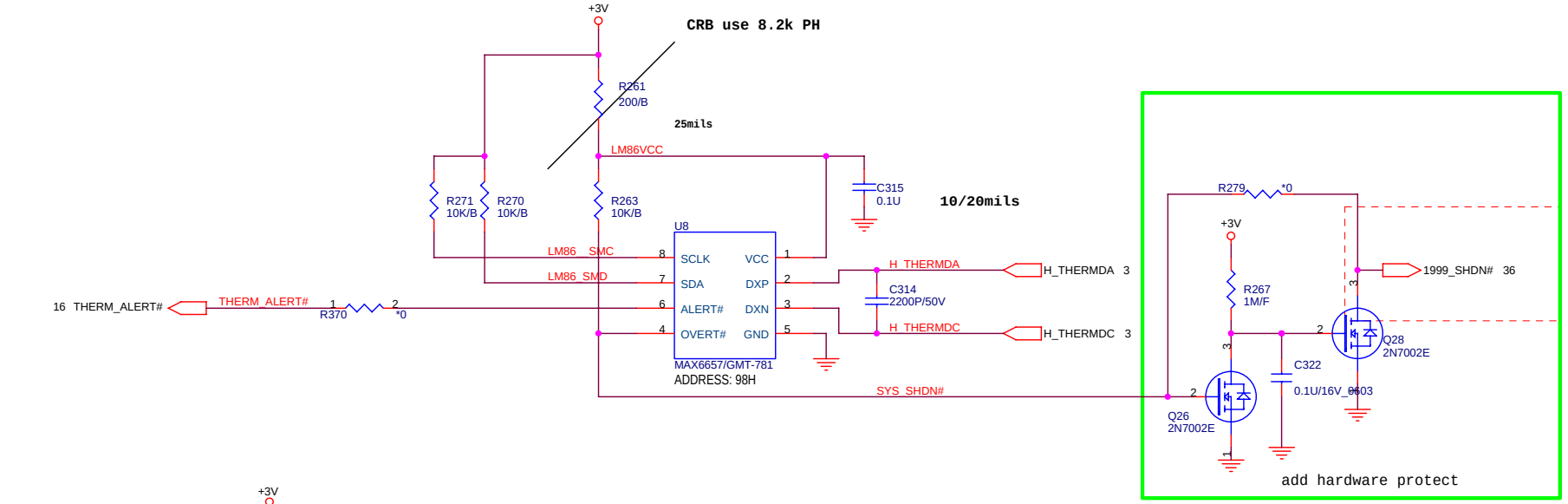
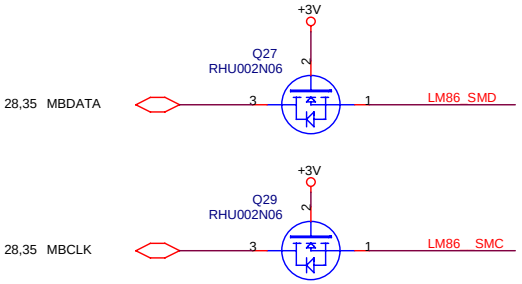
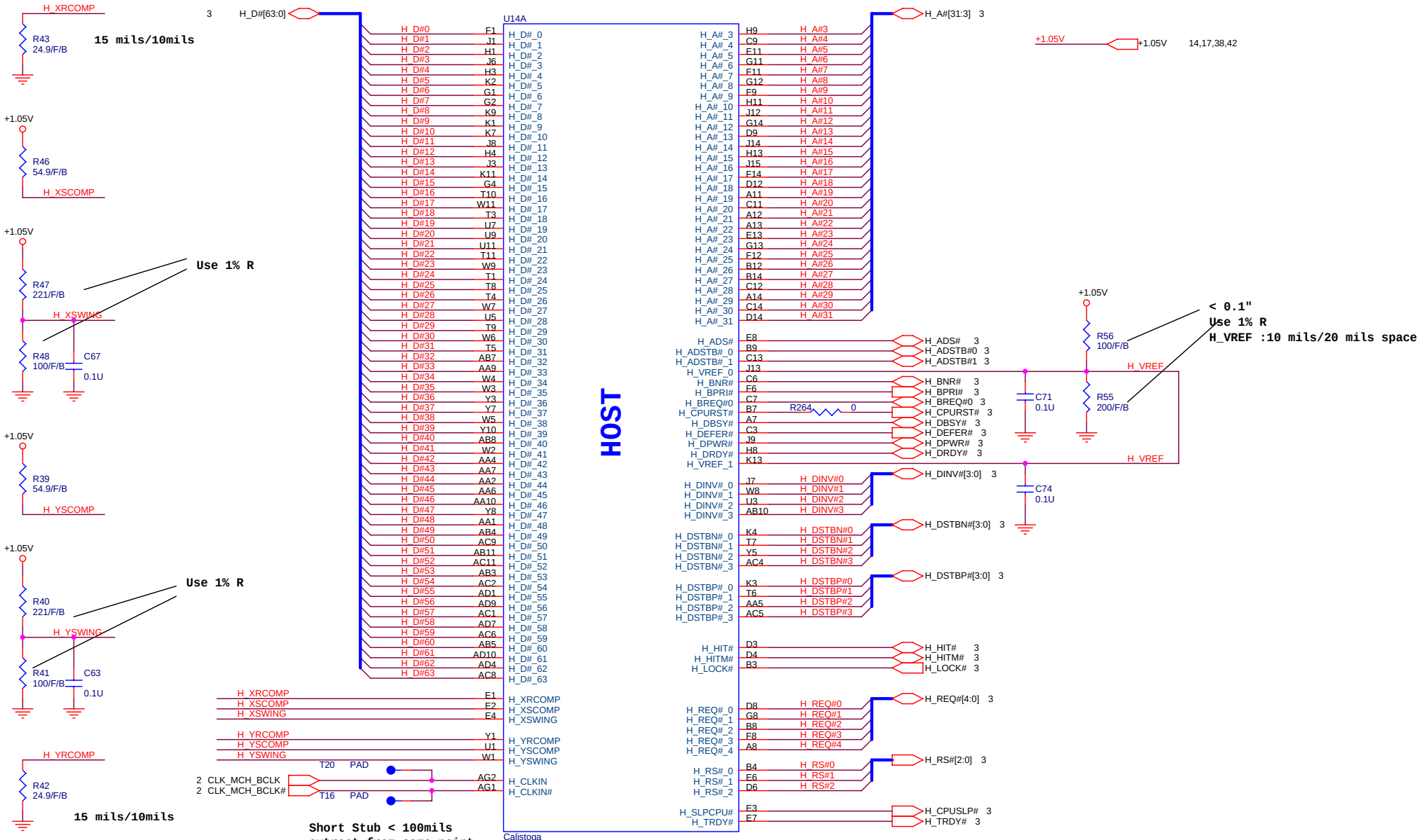




Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
B0 stepping CPU can fix this issue ..

PROJECT : CT6 Quanta Computer Inc.		
Size: B	Document Number: Thermal Sensor LM86	Rev: 1A
Date: Friday, September 23, 2005	Sheet 5 of 44	


H_XRCOMP
R43
24.9/F/B
15 mils/10mils
+1.05V
R46
54.9/F/B
H_XSCOMP
+1.05V
R47
221/F/B
Use 1% R
H_XSWING
R48
100/F/B
C67
0.1U
+1.05V
R39
54.9/F/B
H_YSCOMP
+1.05V
R40
221/F/B
Use 1% R
H_YSWING
R41
100/F/B
C63
0.1U
H_YRCOMP
R42
24.9/F/B
15 mils/10mils
3 H_D#[63:0]
U14A
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
2 CLK_MCH_BCLK
2 CLK_MCH_BCLK#
T20 PAD
T16 PAD
H_CLKIN AG2
H_CLKIN# AG1
Short Stub < 100mils
extract from same point
HOST
Calistoga
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
H_A#[31:3] 3
+1.05V
+1.05V 14,17,38,42
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_VREF_0 J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_VREF_1 K13
H_ADS# 3
H_ADSTB#0 3
H_ADSTB#1 3
H_BNR# 3
H_BPRI# 3
H_BREQ#0 3
H_CPURST# 3
H_DBSY# 3
H_DEFER# 3
H_DPWR# 3
H_DRDY# 3
R264 0
C71
0.1U
C74
0.1U
H_VREF
H_VREF
+1.05V
R56
100/F/B
R55
200/F/B
< 0.1"
Use 1% R
H_VREF :10 mils/20 mils space
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#[3:0] 3
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#[3:0] 3
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#[3:0] 3
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# 3
H_HITM# 3
H_LOCK# 3
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4:0] 3
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# 3
H_TRDY# 3
PROJECT : CT6
Quanta Computer Inc.
Size B
Document Number
GMCH HOST(1 OF 6)
Rev 1A
Date: Friday, September 23, 2005
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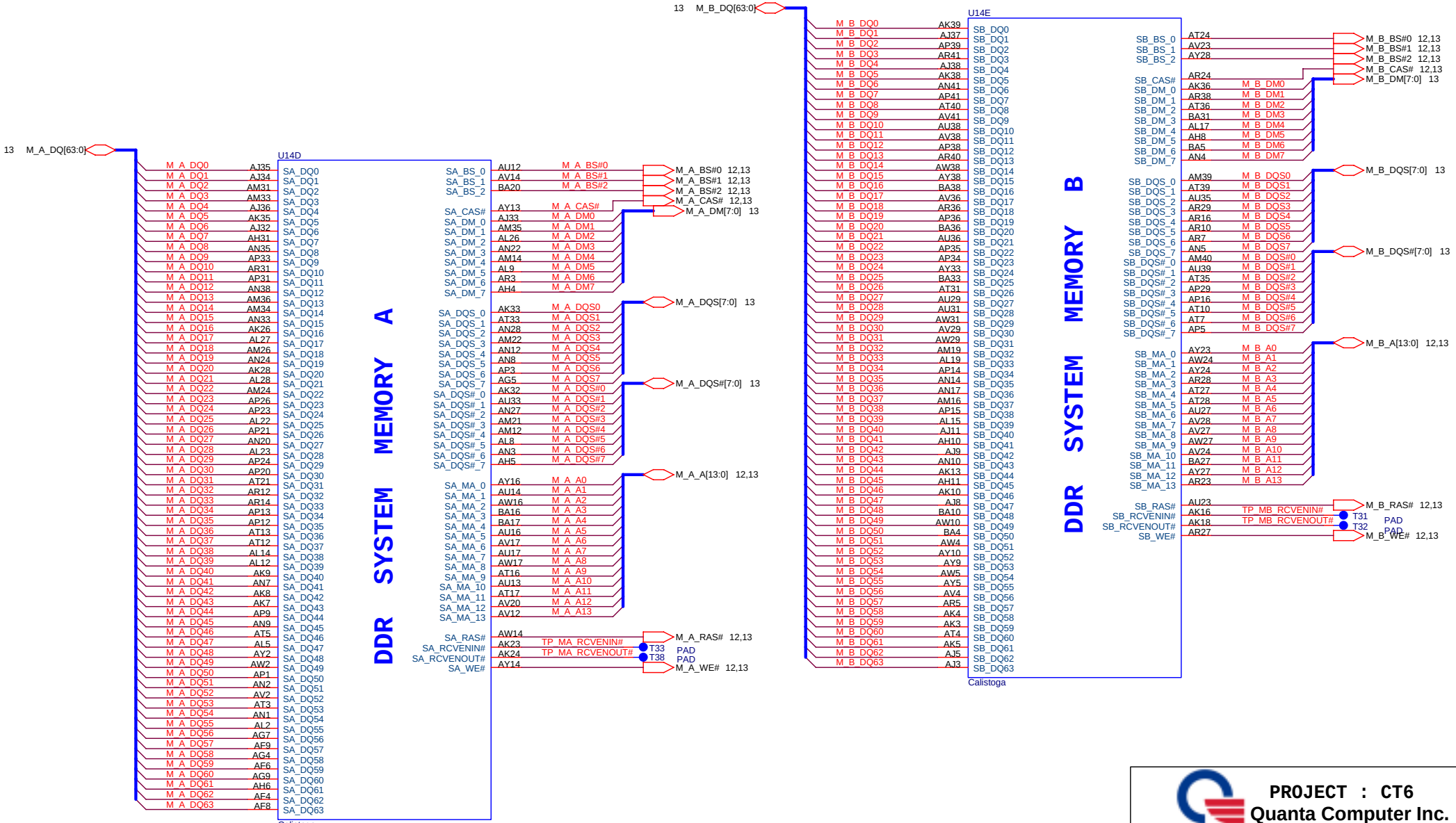
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M_A_DQ1 AJ34
M_A_DQ2 AM31
M_A_DQ3 AM33
M_A_DQ4 AJ36
M_A_DQ5 AK35
M_A_DQ6 AJ32
M_A_DQ7 AH31
M_A_DQ8 AN35
M_A_DQ9 AP33
M_A_DQ10 AR31
M_A_DQ11 AP31
M_A_DQ12 AN38
M_A_DQ13 AM36
M_A_DQ14 AM34
M_A_DQ15 AN33
M_A_DQ16 AK26
M_A_DQ17 AL27
M_A_DQ18 AM26
M_A_DQ19 AN24
M_A_DQ20 AK28
M_A_DQ21 AL28
M_A_DQ22 AM24
M_A_DQ23 AP26
M_A_DQ24 AP23
M_A_DQ25 AL22
M_A_DQ26 AP21
M_A_DQ27 AN20
M_A_DQ28 AL23
M_A_DQ29 AP24
M_A_DQ30 AP20
M_A_DQ31 AT21
M_A_DQ32 AR12
M_A_DQ33 AR14
M_A_DQ34 AP13
M_A_DQ35 AP12
M_A_DQ36 AT13
M_A_DQ37 AT12
M_A_DQ38 AL14
M_A_DQ39 AL12
M_A_DQ40 AK9
M_A_DQ41 AN7
M_A_DQ42 AK8
M_A_DQ43 AK7
M_A_DQ44 AP9
M_A_DQ45 AN9
M_A_DQ46 AT5
M_A_DQ47 AL5
M_A_DQ48 AY2
M_A_DQ49 AW2
M_A_DQ50 AP1
M_A_DQ51 AN2
M_A_DQ52 AV2
M_A_DQ53 AT3
M_A_DQ54 AN1
M_A_DQ55 AL2
M_A_DQ56 AG7
M_A_DQ57 AF9
M_A_DQ58 AG4
M_A_DQ59 AF6
M_A_DQ60 AG9
M_A_DQ61 AH6
M_A_DQ62 AF4
M_A_DQ63 AF8
U14D
SA_DQ0 SA_DQ1 SA_DQ2 SA_DQ3 SA_DQ4 SA_DQ5 SA_DQ6 SA_DQ7 SA_DQ8 SA_DQ9 SA_DQ10 SA_DQ11 SA_DQ12 SA_DQ13 SA_DQ14 SA_DQ15 SA_DQ16 SA_DQ17 SA_DQ18 SA_DQ19 SA_DQ20 SA_DQ21 SA_DQ22 SA_DQ23 SA_DQ24 SA_DQ25 SA_DQ26 SA_DQ27 SA_DQ28 SA_DQ29 SA_DQ30 SA_DQ31 SA_DQ32 SA_DQ33 SA_DQ34 SA_DQ35 SA_DQ36 SA_DQ37 SA_DQ38 SA_DQ39 SA_DQ40 SA_DQ41 SA_DQ42 SA_DQ43 SA_DQ44 SA_DQ45 SA_DQ46 SA_DQ47 SA_DQ48 SA_DQ49 SA_DQ50 SA_DQ51 SA_DQ52 SA_DQ53 SA_DQ54 SA_DQ55 SA_DQ56 SA_DQ57 SA_DQ58 SA_DQ59 SA_DQ60 SA_DQ61 SA_DQ62 SA_DQ63
DDR SYSTEM MEMORY A
SA_BS_0 AU12 M_A_BS#0
SA_BS_1 AV14 M_A_BS#1
SA_BS_2 BA20 M_A_BS#2
M_A_BS#0 12,13
M_A_BS#1 12,13
M_A_BS#2 12,13
M_A_CAS# 12,13
SA_CAS# AY13 M_A_CAS#
SA_DM_0 AJ33 M_A_DM0
SA_DM_1 AM35 M_A_DM1
SA_DM_2 AL26 M_A_DM2
SA_DM_3 AN22 M_A_DM3
SA_DM_4 AM14 M_A_DM4
SA_DM_5 AL9 M_A_DM5
SA_DM_6 AR3 M_A_DM6
SA_DM_7 AH4 M_A_DM7
M_A_DM[7:0] 13
SA_DQS_0 AK33 M_A_DQS0
SA_DQS_1 AT33 M_A_DQS1
SA_DQS_2 AN28 M_A_DQS2
SA_DQS_3 AM22 M_A_DQS3
SA_DQS_4 AN12 M_A_DQS4
SA_DQS_5 AN8 M_A_DQS5
SA_DQS_6 AP3 M_A_DQS6
SA_DQS_7 AG5 M_A_DQS7
M_A_DQS[7:0] 13
SA_DQS#_0 AK32 M_A_DQS#0
SA_DQS#_1 AU33 M_A_DQS#1
SA_DQS#_2 AN27 M_A_DQS#2
SA_DQS#_3 AM21 M_A_DQS#3
SA_DQS#_4 AM12 M_A_DQS#4
SA_DQS#_5 AL8 M_A_DQS#5
SA_DQS#_6 AN3 M_A_DQS#6
SA_DQS#_7 AH5 M_A_DQS#7
M_A_DQS#[7:0] 13
SA_MA_0 AY16 M_A_A0
SA_MA_1 AU14 M_A_A1
SA_MA_2 AW16 M_A_A2
SA_MA_3 BA16 M_A_A3
SA_MA_4 BA17 M_A_A4
SA_MA_5 AU16 M_A_A5
SA_MA_6 AV17 M_A_A6
SA_MA_7 AU17 M_A_A7
SA_MA_8 AW17 M_A_A8
SA_MA_9 AT16 M_A_A9
SA_MA_10 AU13 M_A_A10
SA_MA_11 AT17 M_A_A11
SA_MA_12 AV20 M_A_A12
SA_MA_13 AV12 M_A_A13
M_A_A[13:0] 12,13
SA_RAS# AW14
SA_RCVENIN# AK23 TP_MA_RCVENIN#
SA_RCVENOUT# AK24 TP_MA_RCVENOUT#
SA_WE# AY14
T33 PAD
T38 PAD
M_A_RAS# 12,13
M_A_WE# 12,13
Calistoga
13 M_B_DQ[63:0]
M_B_DQ0 AK39
M_B_DQ1 AJ37
M_B_DQ2 AP39
M_B_DQ3 AR41
M_B_DQ4 AJ38
M_B_DQ5 AK38
M_B_DQ6 AN41
M_B_DQ7 AP41
M_B_DQ8 AT40
M_B_DQ9 AV41
M_B_DQ10 AU38
M_B_DQ11 AV38
M_B_DQ12 AP38
M_B_DQ13 AR40
M_B_DQ14 AW38
M_B_DQ15 AY38
M_B_DQ16 BA38
M_B_DQ17 AV36
M_B_DQ18 AR36
M_B_DQ19 AP36
M_B_DQ20 BA36
M_B_DQ21 AU36
M_B_DQ22 AP35
M_B_DQ23 AP34
M_B_DQ24 AY33
M_B_DQ25 BA33
M_B_DQ26 AT31
M_B_DQ27 AU29
M_B_DQ28 AU31
M_B_DQ29 AW31
M_B_DQ30 AV29
M_B_DQ31 AW29
M_B_DQ32 AM19
M_B_DQ33 AL19
M_B_DQ34 AP14
M_B_DQ35 AN14
M_B_DQ36 AN17
M_B_DQ37 AM16
M_B_DQ38 AP15
M_B_DQ39 AL15
M_B_DQ40 AJ11
M_B_DQ41 AH10
M_B_DQ42 AJ9
M_B_DQ43 AN10
M_B_DQ44 AK13
M_B_DQ45 AH11
M_B_DQ46 AK10
M_B_DQ47 AJ8
M_B_DQ48 BA10
M_B_DQ49 AW10
M_B_DQ50 BA4
M_B_DQ51 AW4
M_B_DQ52 AY10
M_B_DQ53 AY9
M_B_DQ54 AW5
M_B_DQ55 AY5
M_B_DQ56 AV4
M_B_DQ57 AR5
M_B_DQ58 AK4
M_B_DQ59 AK3
M_B_DQ60 AT4
M_B_DQ61 AK5
M_B_DQ62 AJ5
M_B_DQ63 AJ3
U14E
SB_DQ0 SB_DQ1 SB_DQ2 SB_DQ3 SB_DQ4 SB_DQ5 SB_DQ6 SB_DQ7 SB_DQ8 SB_DQ9 SB_DQ10 SB_DQ11 SB_DQ12 SB_DQ13 SB_DQ14 SB_DQ15 SB_DQ16 SB_DQ17 SB_DQ18 SB_DQ19 SB_DQ20 SB_DQ21 SB_DQ22 SB_DQ23 SB_DQ24 SB_DQ25 SB_DQ26 SB_DQ27 SB_DQ28 SB_DQ29 SB_DQ30 SB_DQ31 SB_DQ32 SB_DQ33 SB_DQ34 SB_DQ35 SB_DQ36 SB_DQ37 SB_DQ38 SB_DQ39 SB_DQ40 SB_DQ41 SB_DQ42 SB_DQ43 SB_DQ44 SB_DQ45 SB_DQ46 SB_DQ47 SB_DQ48 SB_DQ49 SB_DQ50 SB_DQ51 SB_DQ52 SB_DQ53 SB_DQ54 SB_DQ55 SB_DQ56 SB_DQ57 SB_DQ58 SB_DQ59 SB_DQ60 SB_DQ61 SB_DQ62 SB_DQ63
DDR SYSTEM MEMORY B
SB_BS_0 AT24 M_B_BS#0
SB_BS_1 AV23 M_B_BS#1
SB_BS_2 AY28 M_B_BS#2
M_B_BS#0 12,13
M_B_BS#1 12,13
M_B_BS#2 12,13
M_B_CAS# 12,13
SB_CAS# AR24
SB_DM_0 AK36 M_B_DM0
SB_DM_1 AR38 M_B_DM1
SB_DM_2 AT36 M_B_DM2
SB_DM_3 BA31 M_B_DM3
SB_DM_4 AL17 M_B_DM4
SB_DM_5 AH8 M_B_DM5
SB_DM_6 BA5 M_B_DM6
SB_DM_7 AN4 M_B_DM7
M_B_DM[7:0] 13
SB_DQS_0 AM39 M_B_DQS0
SB_DQS_1 AT39 M_B_DQS1
SB_DQS_2 AU35 M_B_DQS2
SB_DQS_3 AR29 M_B_DQS3
SB_DQS_4 AR16 M_B_DQS4
SB_DQS_5 AR10 M_B_DQS5
SB_DQS_6 AR7 M_B_DQS6
SB_DQS_7 AN5 M_B_DQS7
M_B_DQS[7:0] 13
SB_DQS#_0 AM40 M_B_DQS#0
SB_DQS#_1 AU39 M_B_DQS#1
SB_DQS#_2 AT35 M_B_DQS#2
SB_DQS#_3 AP29 M_B_DQS#3
SB_DQS#_4 AP16 M_B_DQS#4
SB_DQS#_5 AT10 M_B_DQS#5
SB_DQS#_6 AT7 M_B_DQS#6
SB_DQS#_7 AP5 M_B_DQS#7
M_B_DQS#[7:0] 13
SB_MA_0 AY23 M_B_A0
SB_MA_1 AW24 M_B_A1
SB_MA_2 AY24 M_B_A2
SB_MA_3 AR28 M_B_A3
SB_MA_4 AT27 M_B_A4
SB_MA_5 AT28 M_B_A5
SB_MA_6 AU27 M_B_A6
SB_MA_7 AV28 M_B_A7
SB_MA_8 AV27 M_B_A8
SB_MA_9 AW27 M_B_A9
SB_MA_10 AV24 M_B_A10
SB_MA_11 BA27 M_B_A11
SB_MA_12 AY27 M_B_A12
SB_MA_13 AR23 M_B_A13
M_B_A[13:0] 12,13
SB_RAS# AU23
SB_RCVENIN# AK16 TP_MB_RCVENIN#
SB_RCVENOUT# AK18 TP_MB_RCVENOUT#
SB_WE# AR27
T31 PAD
T32 PAD
M_B_RAS# 12,13
M_B_WE# 12,13
Calistoga
PROJECT : CT6
Quanta Computer Inc.
Size B
Document Number
GMCH DDR(2 OF 6)
Rev 1A
Date: Friday, September 23, 2005
Sheet 7 of 44

change part number (need to use 1% resistor)

20mils/20mils space

PV-I modified for fix SMDDR_VREF_MCH power noise 15mils/15mils

Use 1% R

Shall be 10K divider of 1.8V_SUS

FROM VRD/1.05V ?

Added -Allen
SDVO_DATA is a strap pin

< 0.1" . 15mils/15mils space

< 0.1" . 15mils/15mils space
use 1% R

remove N/C PIN

remove it for intel spec

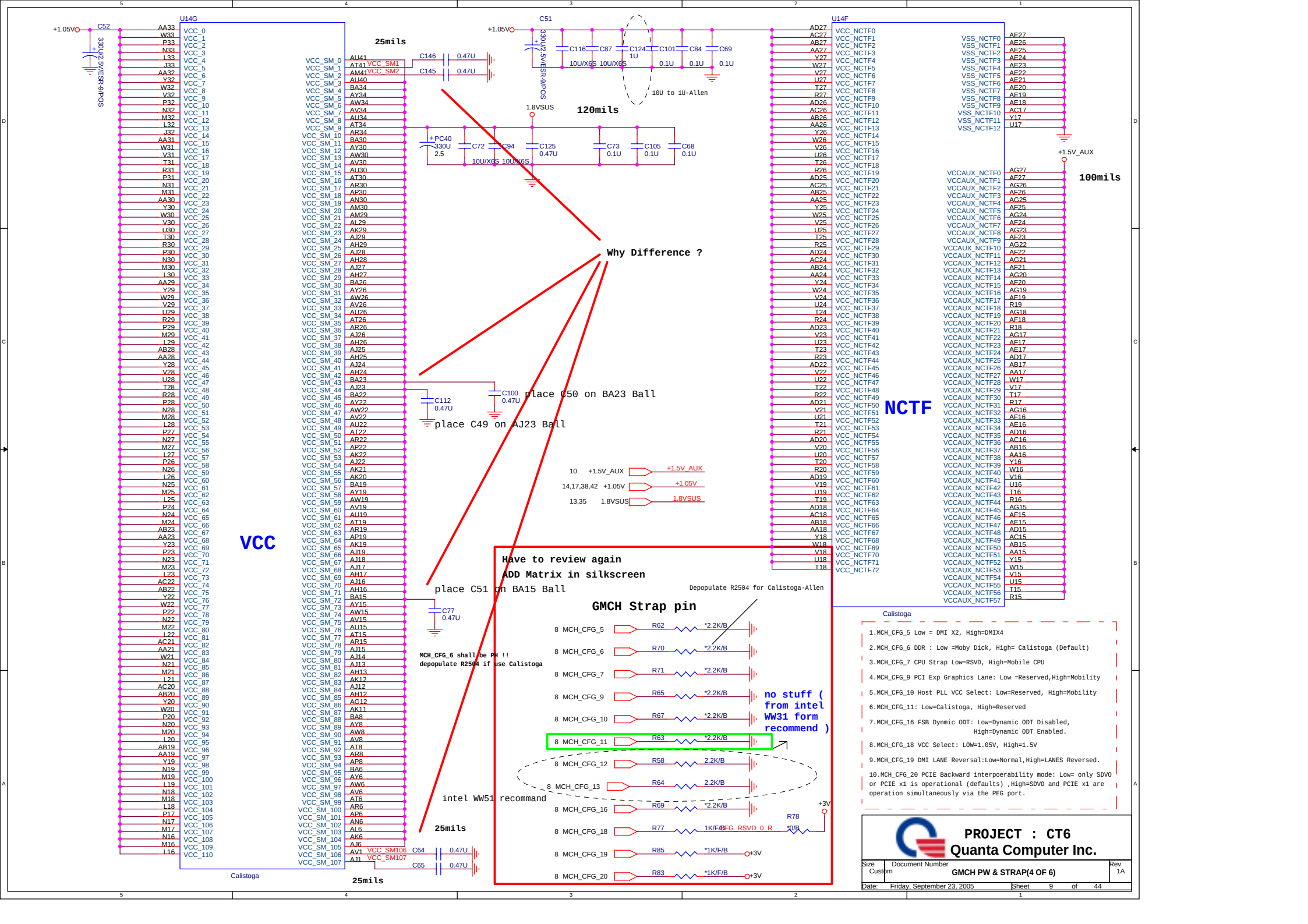
R66, R68 can be deleted --Allen

15mils/10mils

Calistoga

Calistoga

PROJECT :	CT6
Quanta Computer Inc.	
Size: Custom	Document Number: GMCH DMI VEDIO(3 OF 6)
Rev: 1A	
Date: Friday, September 23, 2005	Sheet 8 of 44


U14G
VCC
U14F
NCTF
+1.05V
C52
330U/2.5V/ESR-9/POS
C51
C116
C87
C124
1U
C101
C84
C69
0.1U
10U/X6S
10U to 1U-Allen
1.8VSUS
120mils
25mils
PC40
330U
2.5
C72
C94
C125
0.47U
C73
C105
C68
10U/X6S
Why Difference ?
C146
C145
0.47U
C112
C100
place C50 on BA23 Ball
place C49 on AJ23 Ball
place C51 on BA15 Ball
C77
+1.5V_AUX
100mils
+1.05V
1.8VSUS
Have to review again
ADD Matrix in silkscreen
Depopulate R2504 for Calistoga-Allen
GMCH Strap pin
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
no stuff (from intel WW31 form recommend)
intel WW51 recommand
R62
R70
R71
R65
R67
R63
R58
R64
R69
R77
R85
R83
R78
*2.2K/B
2.2K/B
1K/F/B
*1K/F/B
+3V
MCH_CFG_RSVD_0_R
Calistoga
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : CT6
Quanta Computer Inc.
GMCH PW & STRAP(4 OF 6)
Size Custom
Rev 1A
Date: Friday, September 23, 2005
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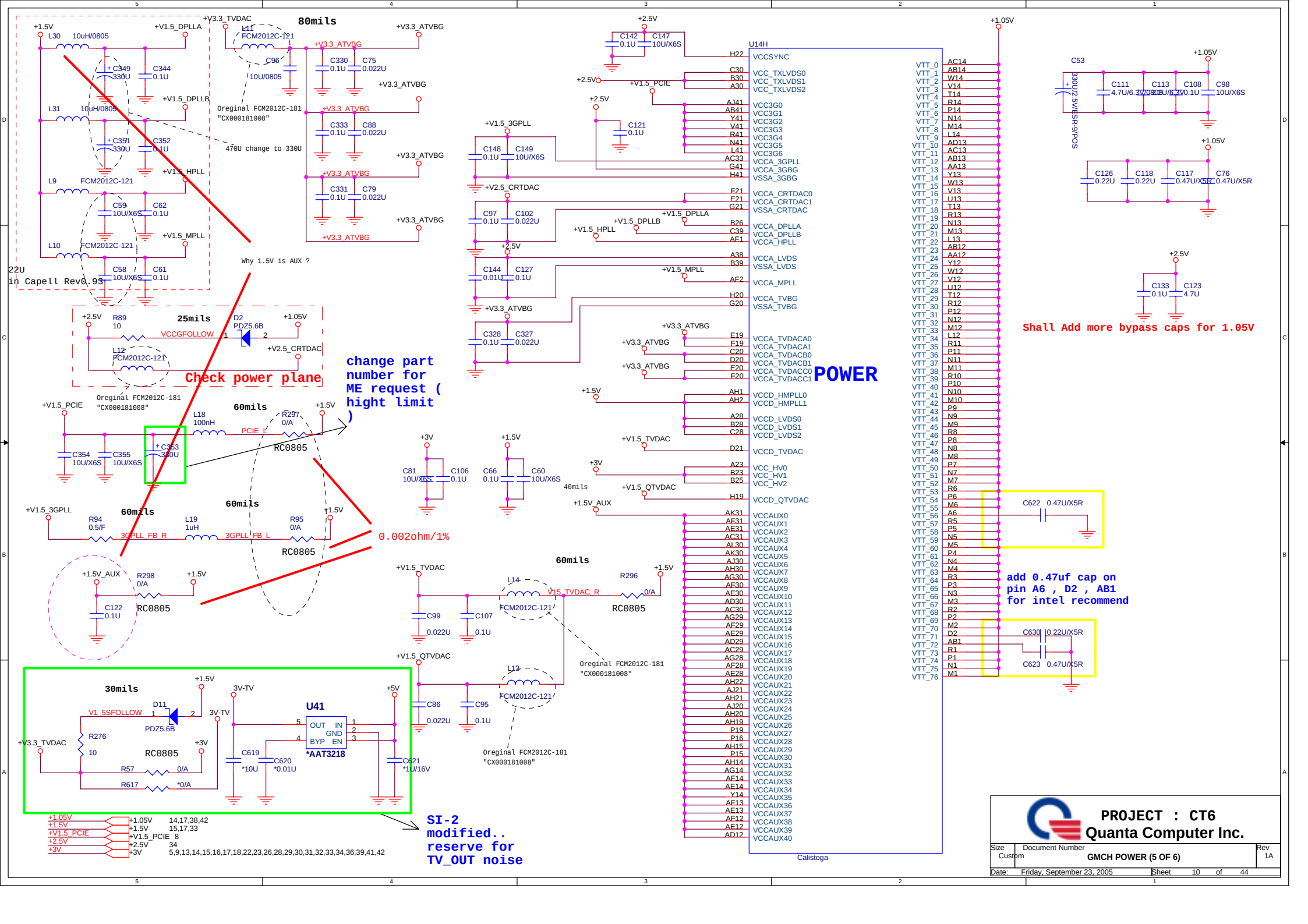
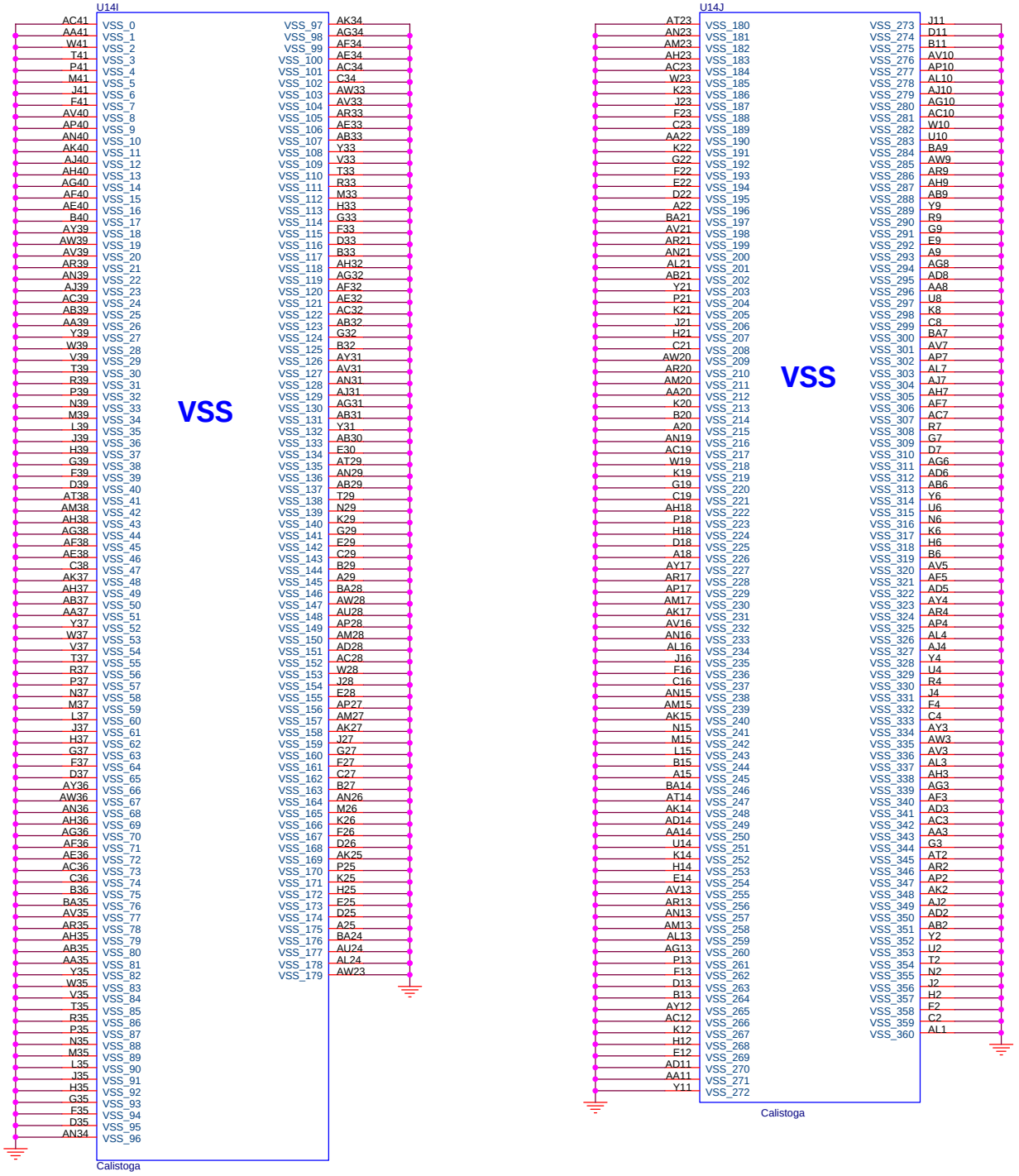
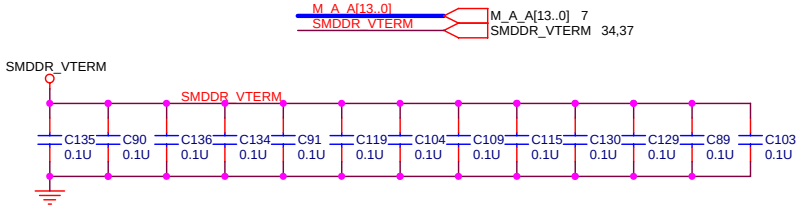

80mils
470U change to 330U
Why 1.5V is AUX ?
22U
in Capell Rev0.93
Check power plane
change part number for ME request (hight limit)
25mils
60mils
0.002ohm/1%
30mils
SI-2 modified.. reserve for TV_OUT noise
U14H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
Calistoga
POWER
Shall Add more bypass caps for 1.05V
add 0.47uf cap on pin A6 , D2 , AB1 for intel recommend
Oreginal FCM2012C-181 "CX000181008"
*AAT3218
PROJECT : CT6
Quanta Computer Inc.
GMCH POWER (5 OF 6)
Friday, September 23, 2005
Sheet 10 of 44

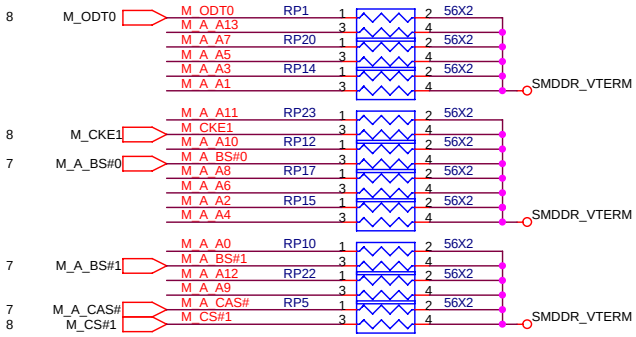


PROJECT : CT6		
Quanta Computer Inc.		
Size: Custom	Document Number: GMCH GND(6 OF 6)	Rev: 1A
Date: Friday, September 23, 2005	Sheet 11 of 44	

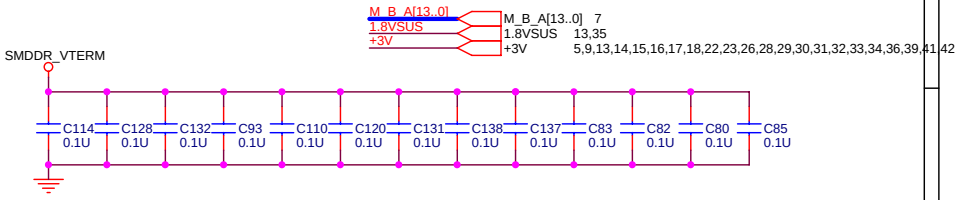
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

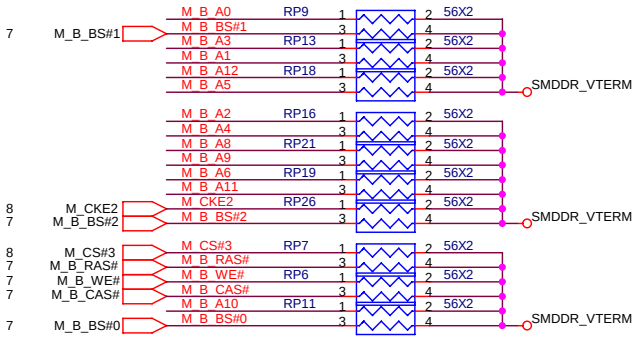


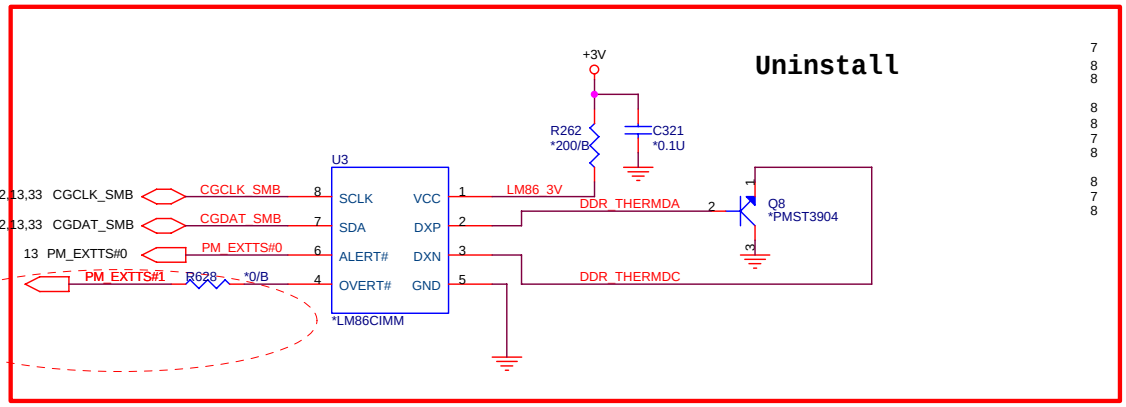


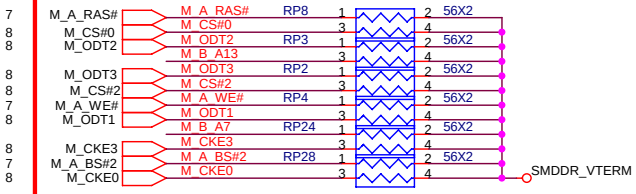
DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM







PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
B	DDR RES. ARRAY	1A

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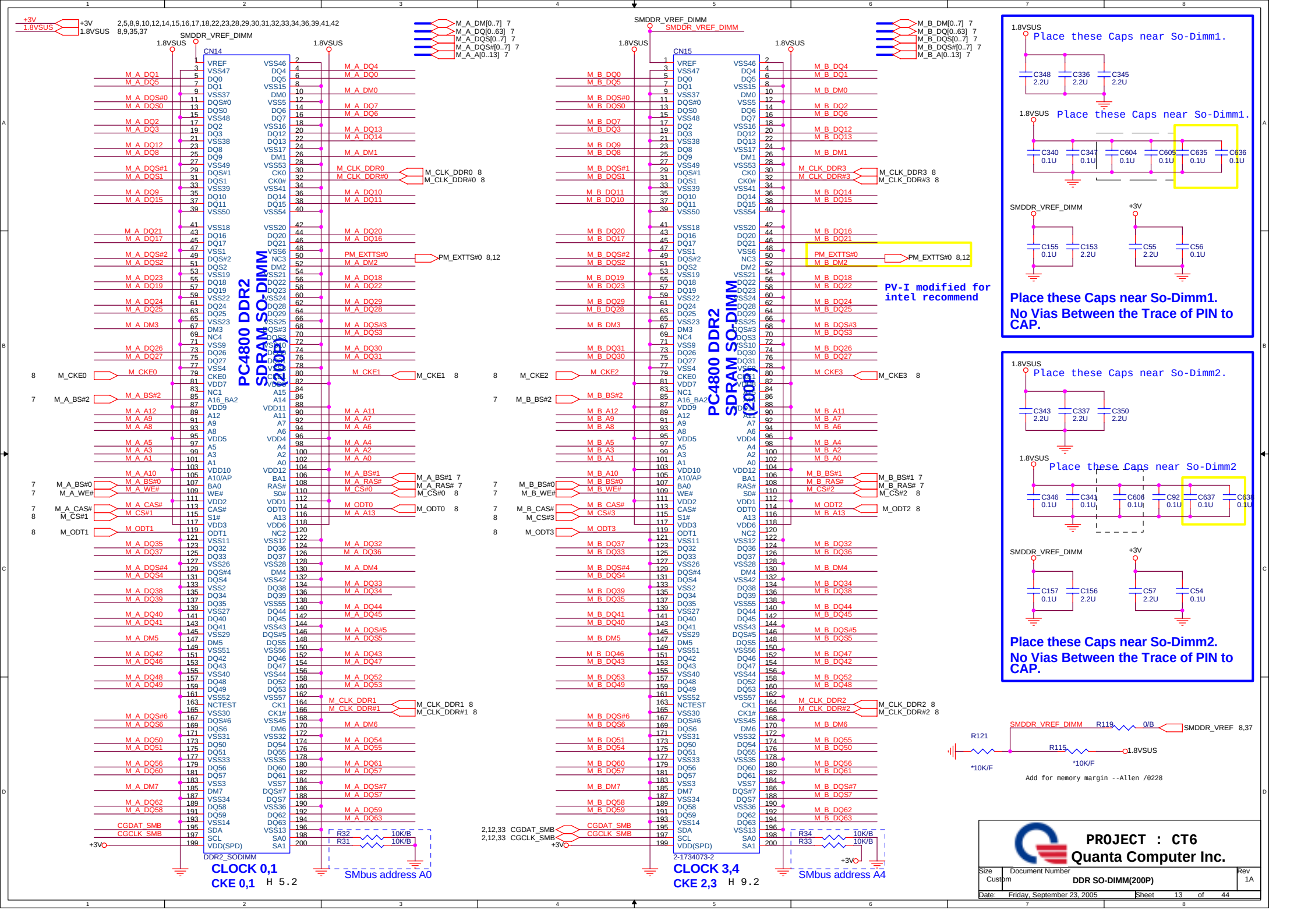
+3V
1.8VSUS
2,5,8,9,10,12,14,15,16,17,18,22,23,28,29,30,31,32,33,34,36,39,41,42
8,9,35,37
SMDDR_VREF_DIMM
CN14
DDR2_SODIMM
PC4800 DDR2 SDRAM SO-DIMM (200P)
M_A_DM[0..7] 7
M_A_DQ[0..63] 7
M_A_DQS[0..7] 7
M_A_DQS#[0..7] 7
M_A_A[0..13] 7
M_CLK_DDR0 8
M_CLK_DDR#0 8
PM_EXTTS#0 8,12
M_CLK_DDR1 8
M_CLK_DDR#1 8
M_CKE0 8
M_CKE1 8
M_A_BS#2 7
M_A_BS#1 7
M_A_RAS# 7
M_A_BS#0 7
M_A_WE# 7
M_CS#0 8
M_ODT0 8
M_A_CAS# 7
M_CS#1 8
M_ODT1 8
R32 10K/B
R31 10K/B
CGDAT_SMB
CGCLK_SMB
+3VO
CLOCK 0,1
CKE 0,1
H 5.2
SMbus address A0
SMDDR_VREF_DIMM
CN15
2-1734073-2
M_B_DM[0..7] 7
M_B_DQ[0..63] 7
M_B_DQS[0..7] 7
M_B_DQS#[0..7] 7
M_B_A[0..13] 7
M_CLK_DDR3 8
M_CLK_DDR#3 8
PM_EXTTS#0 8,12
M_CLK_DDR2 8
M_CLK_DDR#2 8
M_CKE2 8
M_CKE3 8
M_B_BS#2 7
M_B_BS#1 7
M_B_RAS# 7
M_B_BS#0 7
M_B_WE# 7
M_CS#2 8
M_ODT2 8
M_B_CAS# 7
M_CS#3 8
M_ODT3 8
R34 10K/B
R33 10K/B
2,12,33 CGDAT_SMB
2,12,33 CGCLK_SMB
CLOCK 3,4
CKE 2,3
H 9.2
SMbus address A4
PV-I modified for intel recommend
Place these Caps near So-Dimm1.
C348 2.2U
C336 2.2U
C345 2.2U
C340 0.1U
C347 0.1U
C604 0.1U
C605 0.1U
C635 0.1U
C636 0.1U
C155 0.1U
C153 2.2U
C55 2.2U
C56 0.1U
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
C343 2.2U
C337 2.2U
C350 2.2U
C346 0.1U
C341 0.1U
C606 0.1U
C92 0.1U
C637 0.1U
C157 0.1U
C156 2.2U
C57 2.2U
C54 0.1U
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.
R119 0/B
R121
R115
*10K/F
Add for memory margin --Allen /0228
PROJECT : CT6
Quanta Computer Inc.
Size: Custom
Document Number: DDR SO-DIMM(200P)
Rev: 1A
Date: Friday, September 23, 2005
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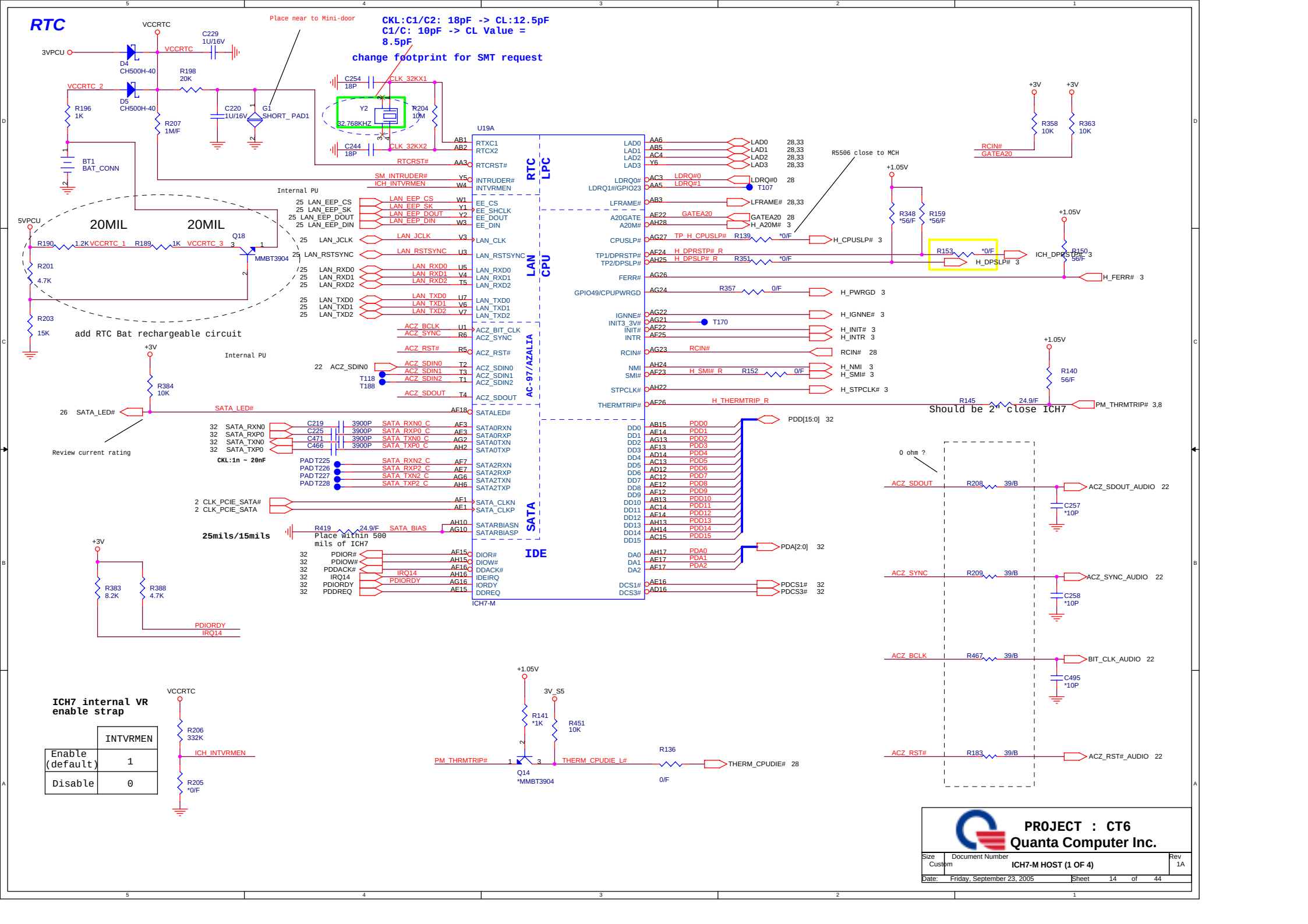
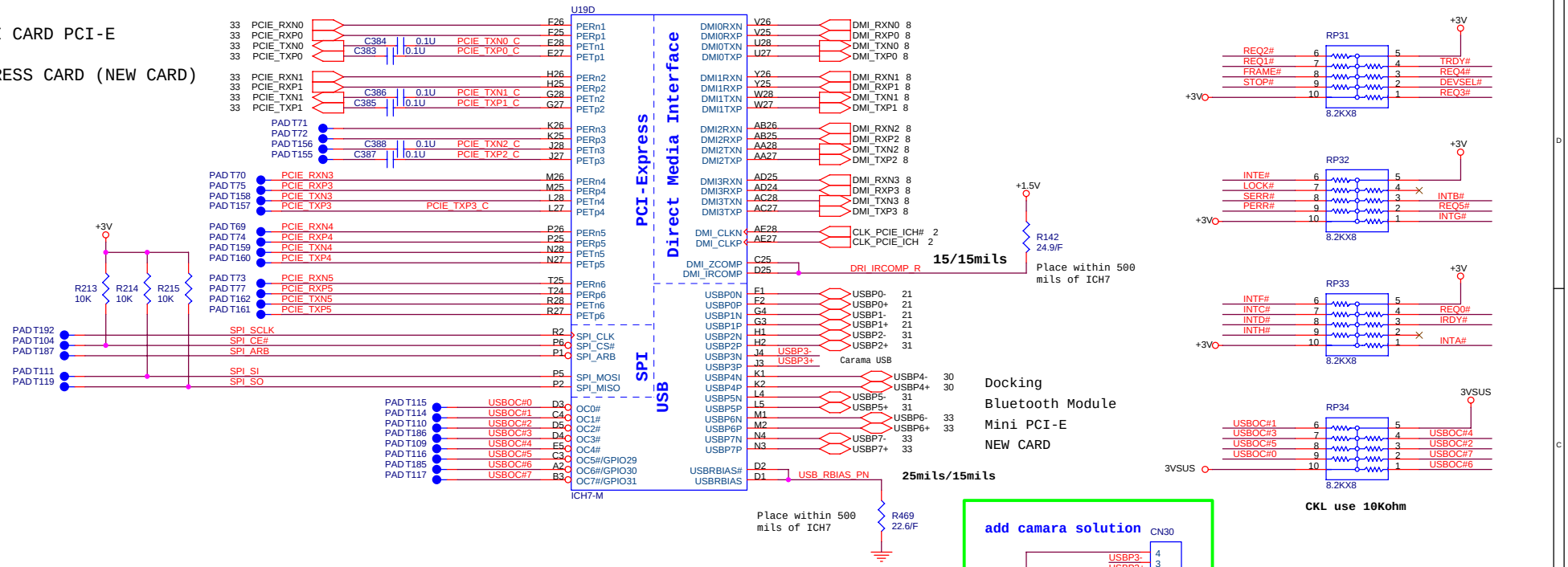

RTC
Place near to Mini-door
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
change footprint for SMT request
add RTC Bat rechargeable circuit
20MIL
20MIL
Internal PU
Review current rating
CKL:1n ~ 20nF
25mils/15mils
Place within 500 mils of ICH7
Should be 2" close ICH7
0 ohm ?
R5506 close to MCH
ICH7 internal VR enable strap
INTVRMEN
Enable (default) 1
Disable 0
U19A
ICH7-M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
PROJECT : CT6
Quanta Computer Inc.
ICH7-M HOST (1 OF 4)
Friday, September 23, 2005

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)



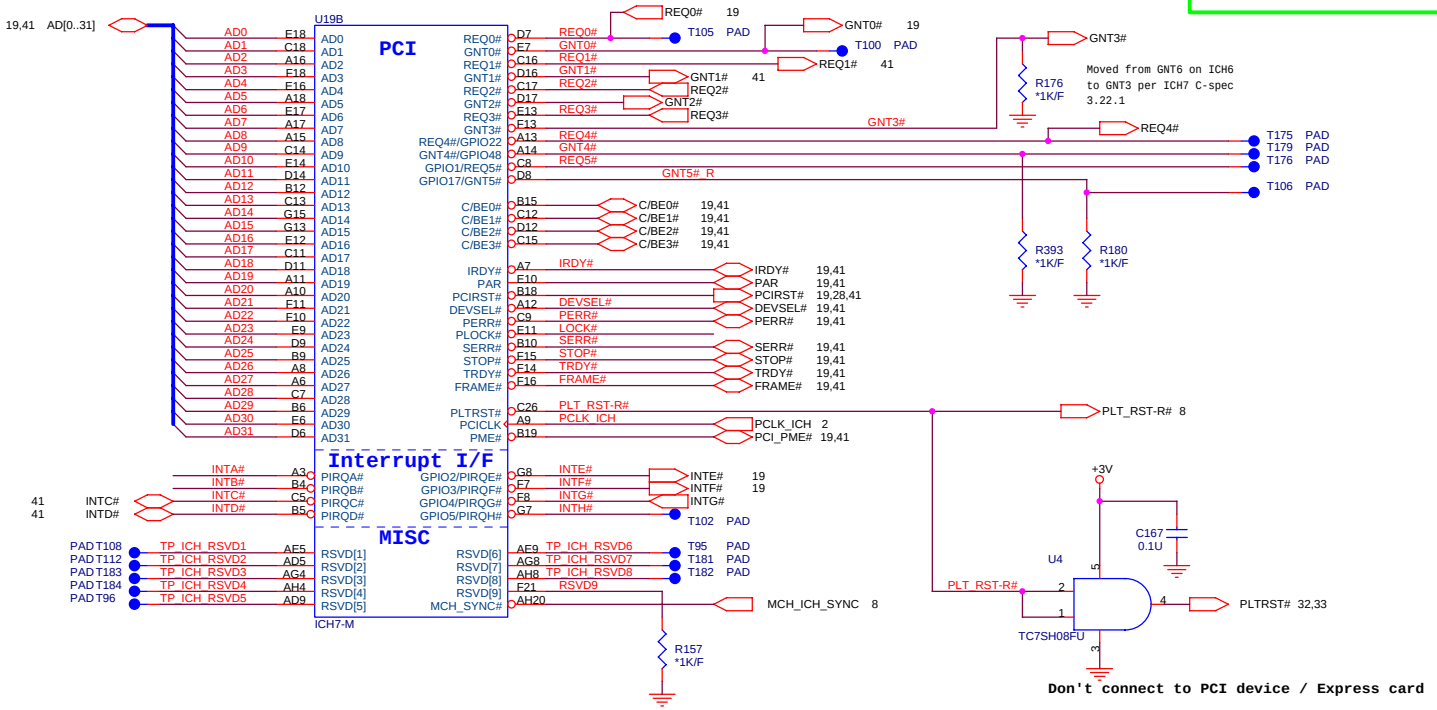
CKL use 10Kohm

Docking
Bluetooth Module
Mini PCI-E
NEW CARD

add camara solution

ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



Don't connect to PCI device / Express card

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ3# / GNT3#	INT B/C/G#
Relteck Lan	AD16	REQ2# / GNT2#	INT C#

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M PCI E (2 OF 4)	1A

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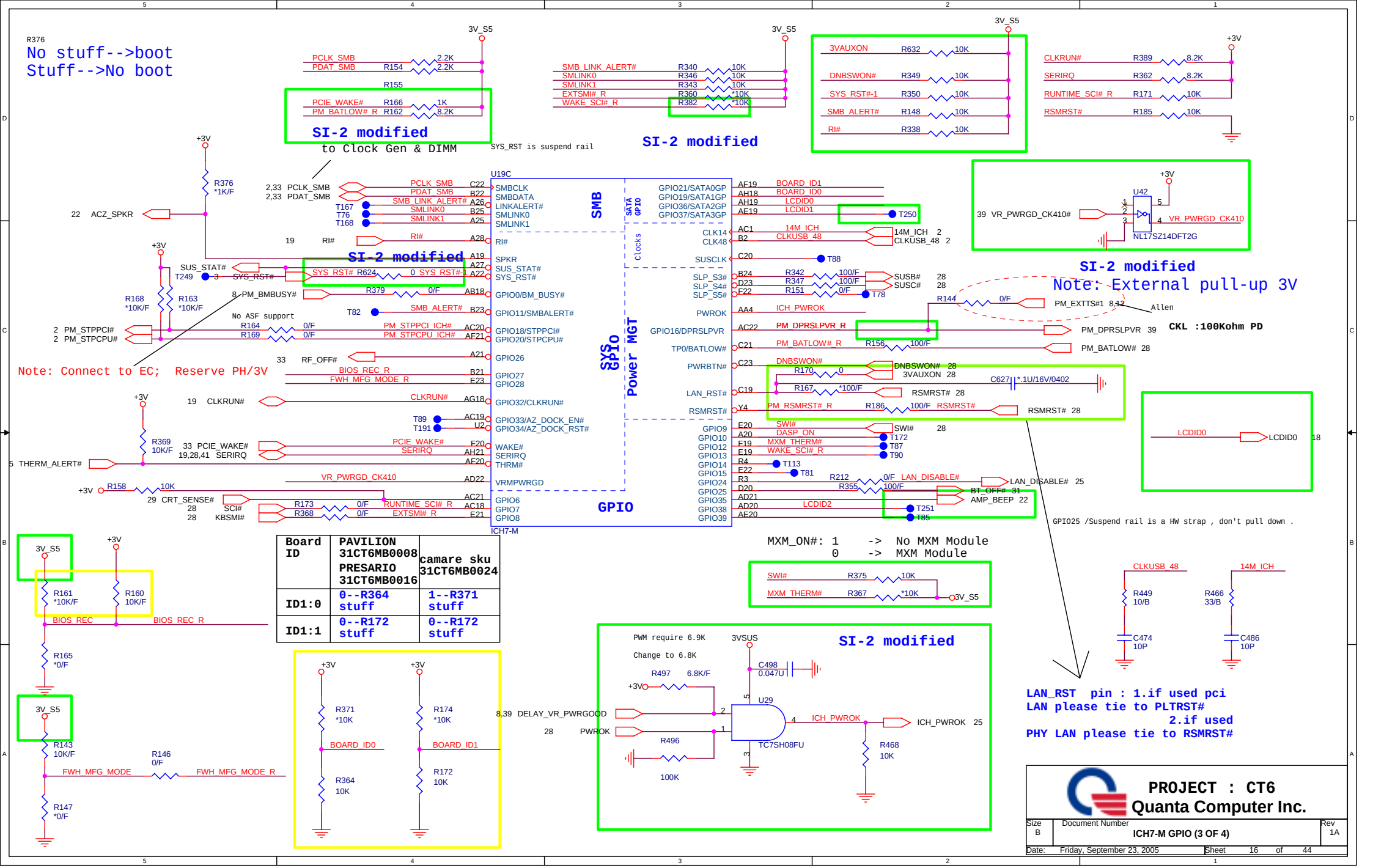
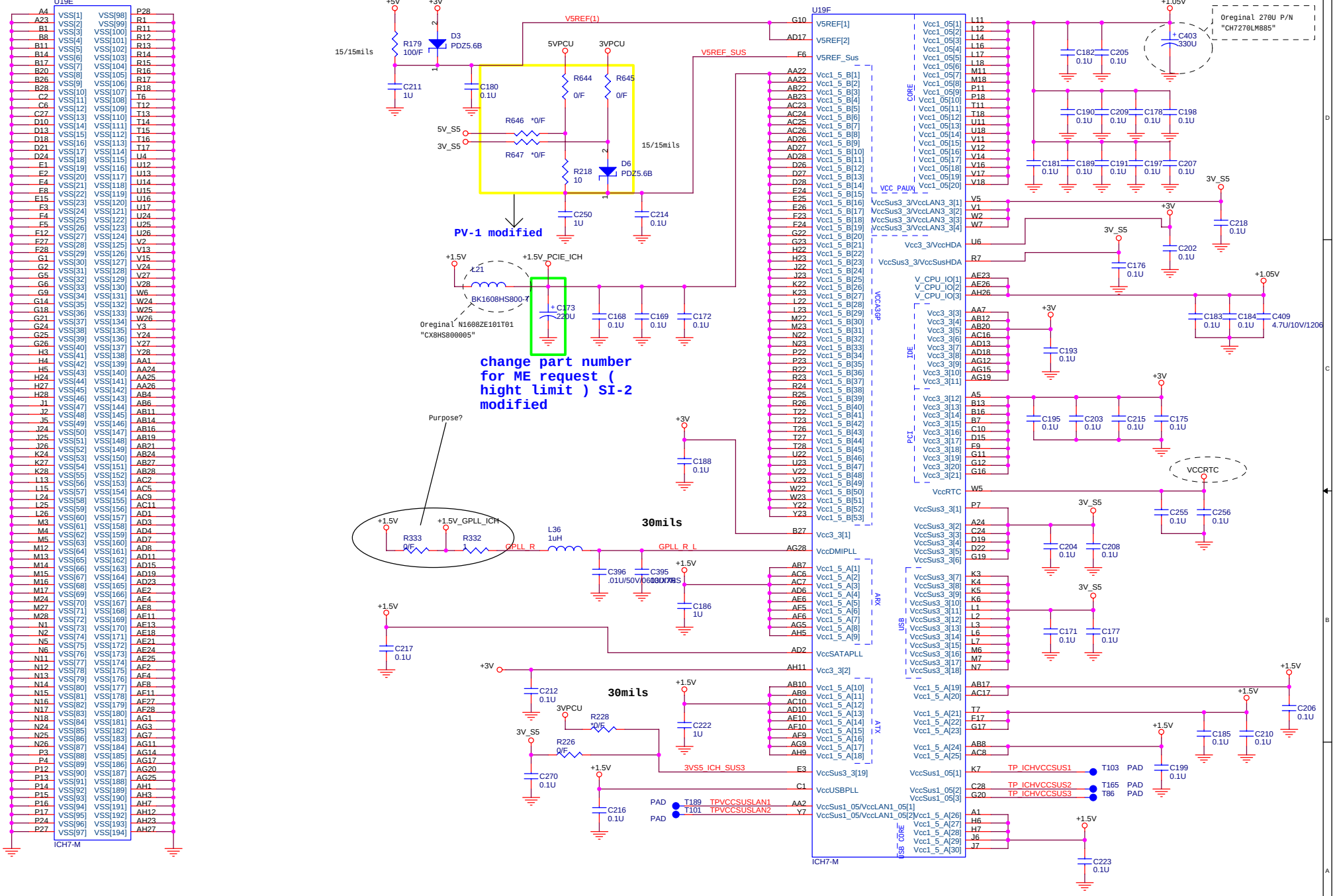
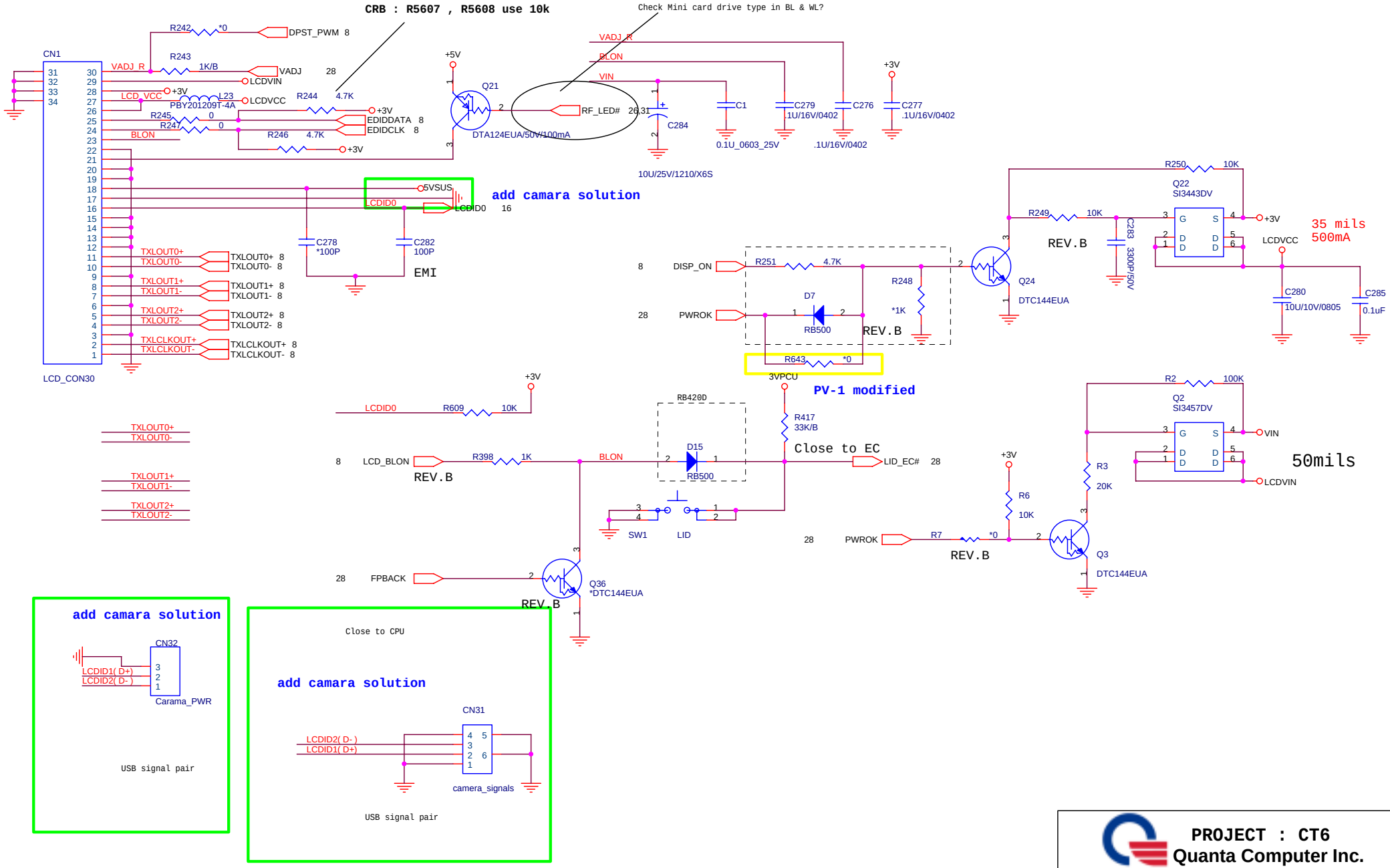

R376
No stuff-->boot
Stuff-->No boot
SI-2 modified
to Clock Gen & DIMM
SYS_RST is suspend rail
SI-2 modified
SI-2 modified
SI-2 modified
Note: External pull-up 3V
CKL :100Kohm PD
Note: Connect to EC; Reserve PH/3V
U19C
SMB
GPIO
Power MGT
SYS
ICH7-M
Board ID
PAVILION 31CT6MB0008 PRESARIO 31CT6MB0016
camare sku 31CT6MB0024
ID1:0
0--R364 stuff
1--R371 stuff
ID1:1
0--R172 stuff
0--R172 stuff
MXM_ON#: 1 -> No MXM Module
0 -> MXM Module
GPIO25 /Suspend rail is a HW strap , don't pull down .
LAN_RST pin : 1.if used pci
LAN please tie to PLTRST#
2.if used
PHY LAN please tie to RSMRST#
PROJECT : CT6
Quanta Computer Inc.
Size B
Document Number ICH7-M GPIO (3 OF 4)
Rev 1A
Date: Friday, September 23, 2005
Sheet 16 of 44


U19E
ICH7-M
U19F
ICH7-M
PV-1 modified
change part number
for ME request (
hight limit) SI-2
modified
30mils
30mils
Oreginal N1608ZE101T01
"CX8HS800005"
Oreginal 270U P/N
"CH7270LM885"
PROJECT : CT6
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
Size Custom
Document Number
Rev 1A
Date: Friday, September 23, 2005
Sheet 17 of 44



PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN	1A
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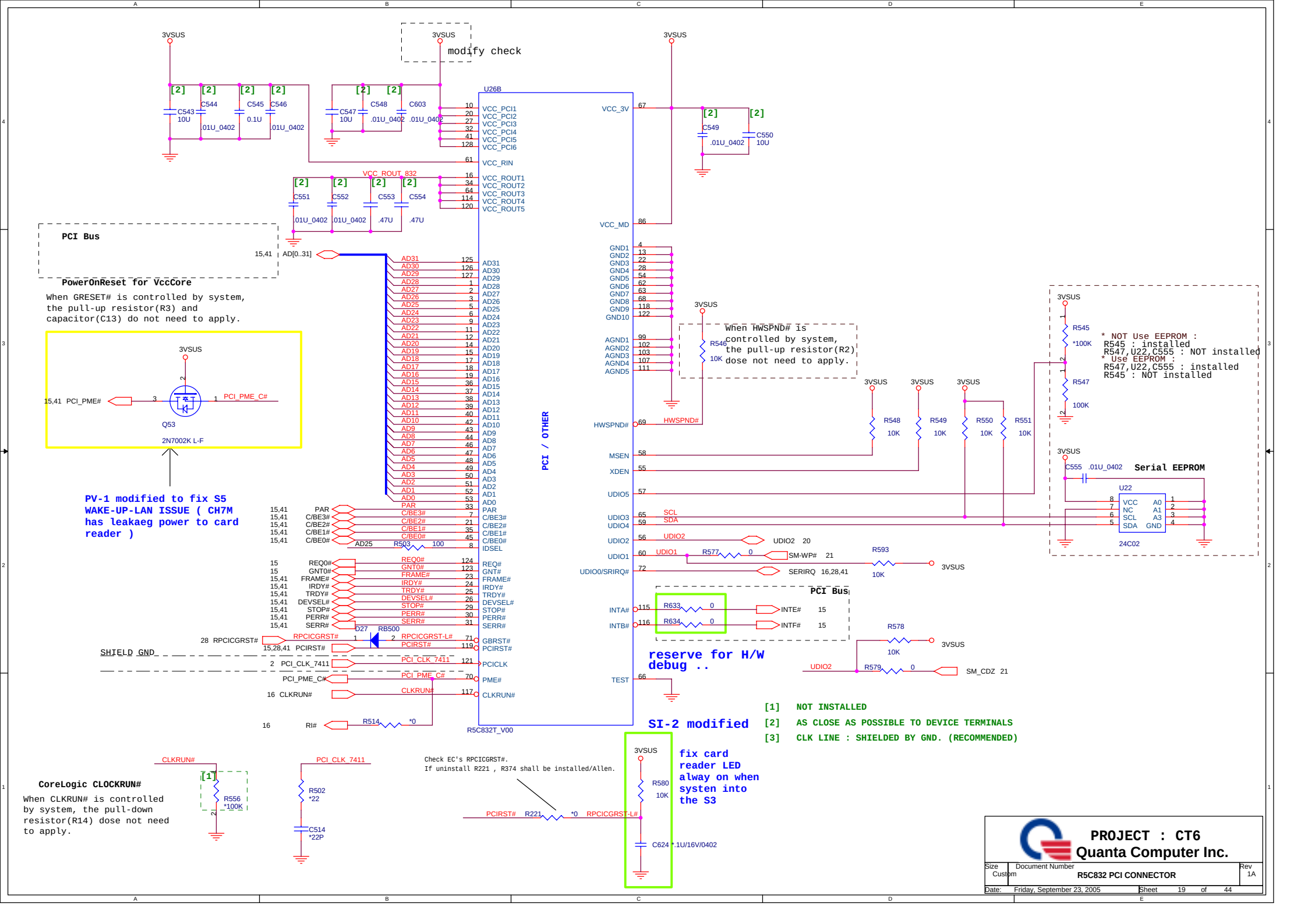

modify check
U26B
PCI / OTHER
R5C832T_V00
PCI Bus
PowerOnReset for VccCore
When GRESET# is controlled by system, the pull-up resistor(R3) and capacitor(C13) do not need to apply.
PV-1 modified to fix S5 WAKE-UP-LAN ISSUE (CH7M has leakaeg power to card reader)
Q53
2N7002K L-F
When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.
* NOT Use EEPROM :
R545 : installed
R547,U22,C555 : NOT installed
* Use EEPROM :
R547,U22,C555 : installed
R545 : NOT installed
Serial EEPROM
24C02
reserve for H/W debug ..
SI-2 modified
fix card reader LED alway on when systen into the S3
Check EC's RPCICGRST#.
If uninstall R221 , R374 shall be installed/Allen.
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.
SHIELD GND
[1] NOT INSTALLED
[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS
[3] CLK LINE : SHIELDED BY GND. (RECOMMENDED)
PROJECT : CT6
Quanta Computer Inc.
R5C832 PCI CONNECTOR
Size Custom
Rev 1A
Date: Friday, September 23, 2005
Sheet 19 of 44

AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.

80 mils

3VSUS

1394_AVDD

L44

FBM1608

modify

C557 10U

C558 0.1U

C559 .01U_0402

C600 .001U

U26A

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

AS CLOSE AS POSSIBLE TO R5C832

TPBIAS0 113

C560 0.33uF

R555 56.2/F

R558 56.2/F

C562 .01U_0402

TPBN0 104
TPBP0 105
TPAN0 108
TPAP0 109

TPB0N
TPB0P
TPA0N
TPA0P

GND Shields

GND Shields

R560 56.2/F

R561 56.2/F

C565 270P

R562 5.11K/F

Circuit area : As small as possible.

*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.

*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

CN20
1394_CONN

GND Shields

TPB0N R598 0 L1394_TPB0-
TPB0P R599 0 L1394_TPB0+

GND Shields

TPA0N R600 0 L1394_TPA0-
TPA0P R601 0 L1394_TPA0+

GUARD GND

C561 22P

1394_XOUT 94 XI

24.576MHz 50ppm 10pF Y9

C563 22P

1394_XIN 95 XO

FIL0_PWR 96 FIL0

C564 .01U_0402

REXT 101 REXT

R559 10K/F/B

VREF_PWR 100 VREF

C566 .01U_0402

GUARD GND

R559 :10K/1%

IEEE1394/SD

MDIO17 87
MDIO16 92
MDIO15 89
MDIO14 91
MDIO13 90
MDIO12 93
MDIO11 81
MDIO10 82
MDIO05 75
MDIO08 88
MDIO19 83
MDIO18 85
MDIO02 78
MDIO03 77
MDIO00 80
MDIO01 79
MDIO09 84
MDIO04 76
MDIO06 74
MDIO07 73

MDIO17 MDIO16 MDIO15 MDIO14 MDIO13 MDIO12 MDIO11 MDIO10 MDIO08 MDIO03 SD_CDZ MS_CDZ

MDIO17 21 MDIO16 21 MDIO15 21 MDIO14 21 MDIO13 21 MDIO12 21 MDIO11 21 MDIO10 21 MDIO08 21 MDIO03 21 SD_CDZ 21 MS_CDZ 21

MDIO05 MDIO19 MDIO18 MDIO02

MDIO05 21 MDIO19 21 MDIO18 21 MDIO02 21

close to CHIP

D25 RB500

D26 RB500

SD_CDZ MS_CDZ

close to conn

UDIO2

UDIO2 19

3VSUS

D28 RB500

R585 10K

XD_CD_L

XD_CD_L 21

GND Shields

MDIO09 21

MC_PWR_CTRL_0 21

CARD_LED 26

97 RSV

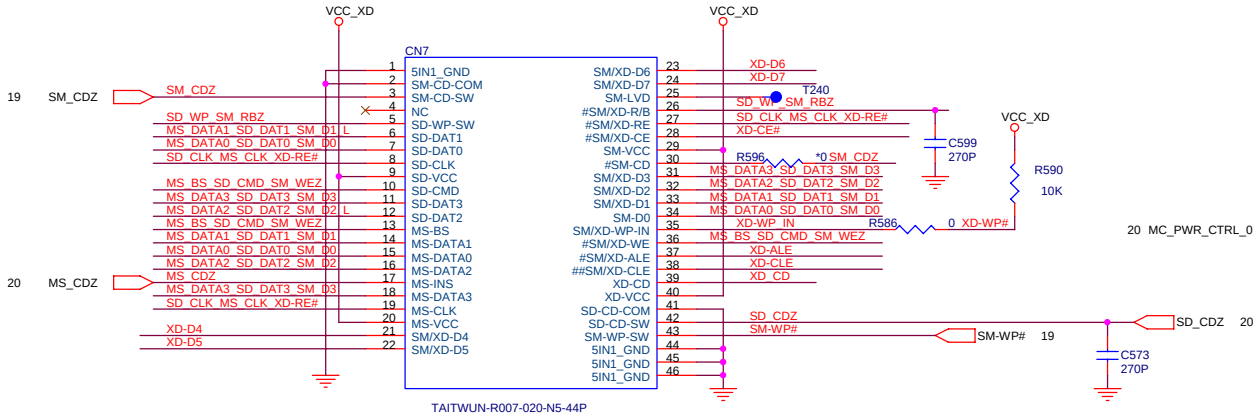
R5C832T_V00

PROJECT : CT6
Quanta Computer Inc.

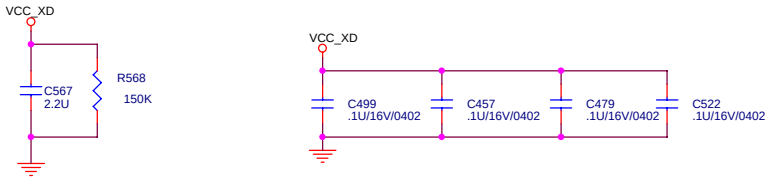
Size	Document Number	Rev
Custom	IEEE1394	1A

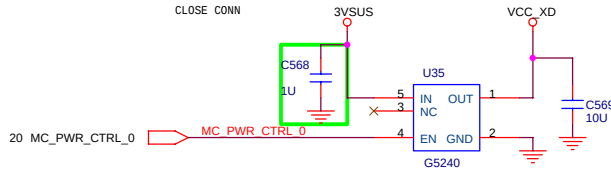
Date: Friday, September 23, 2005 Sheet 20 of 44

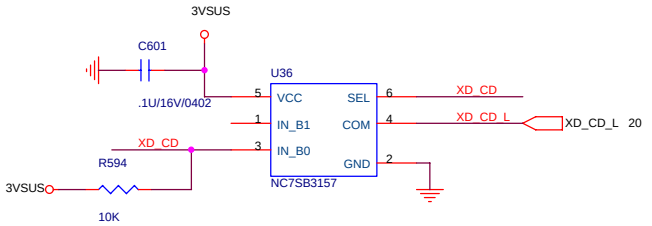
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

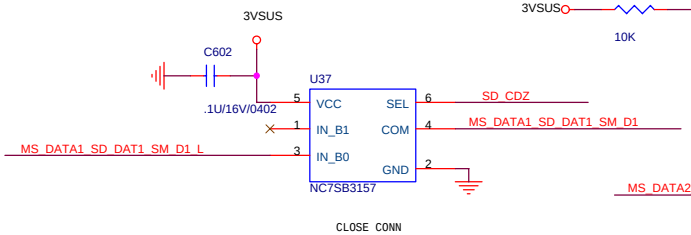


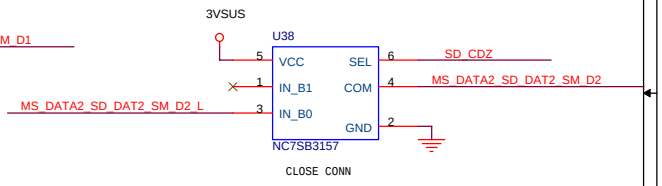
5 IN1 CARD READER

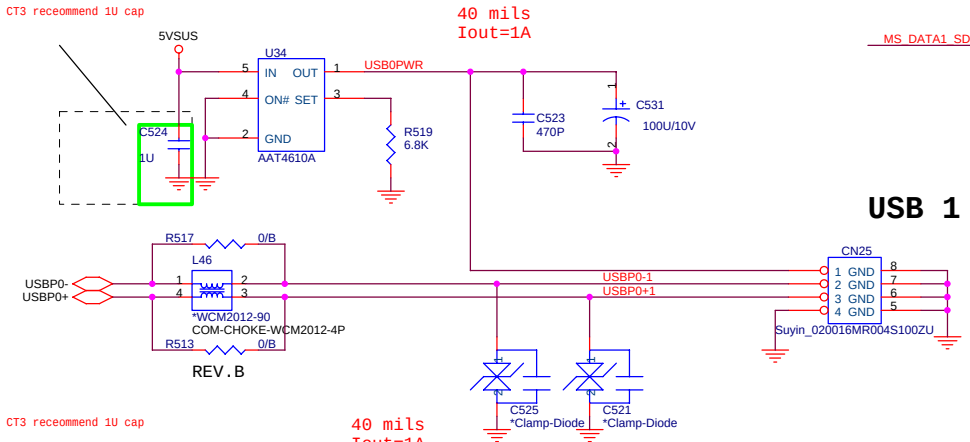


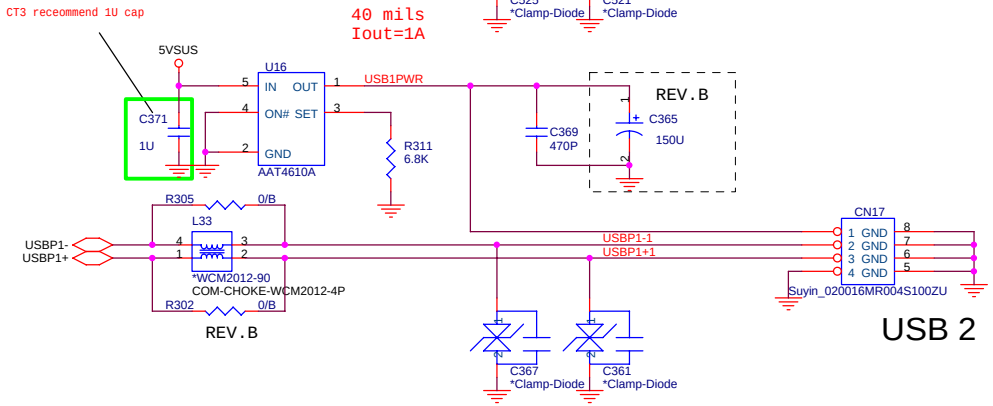


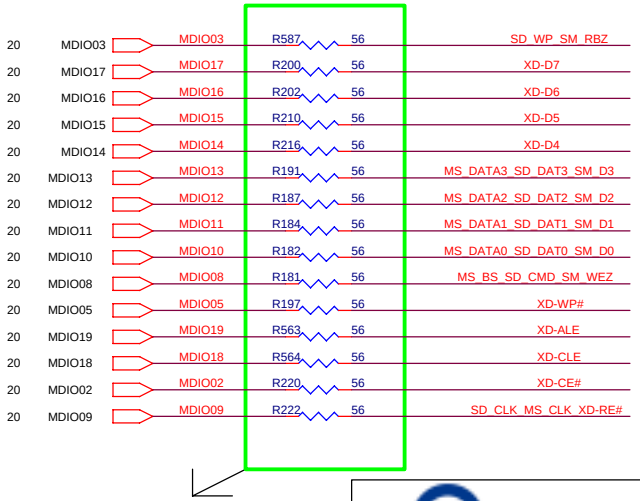








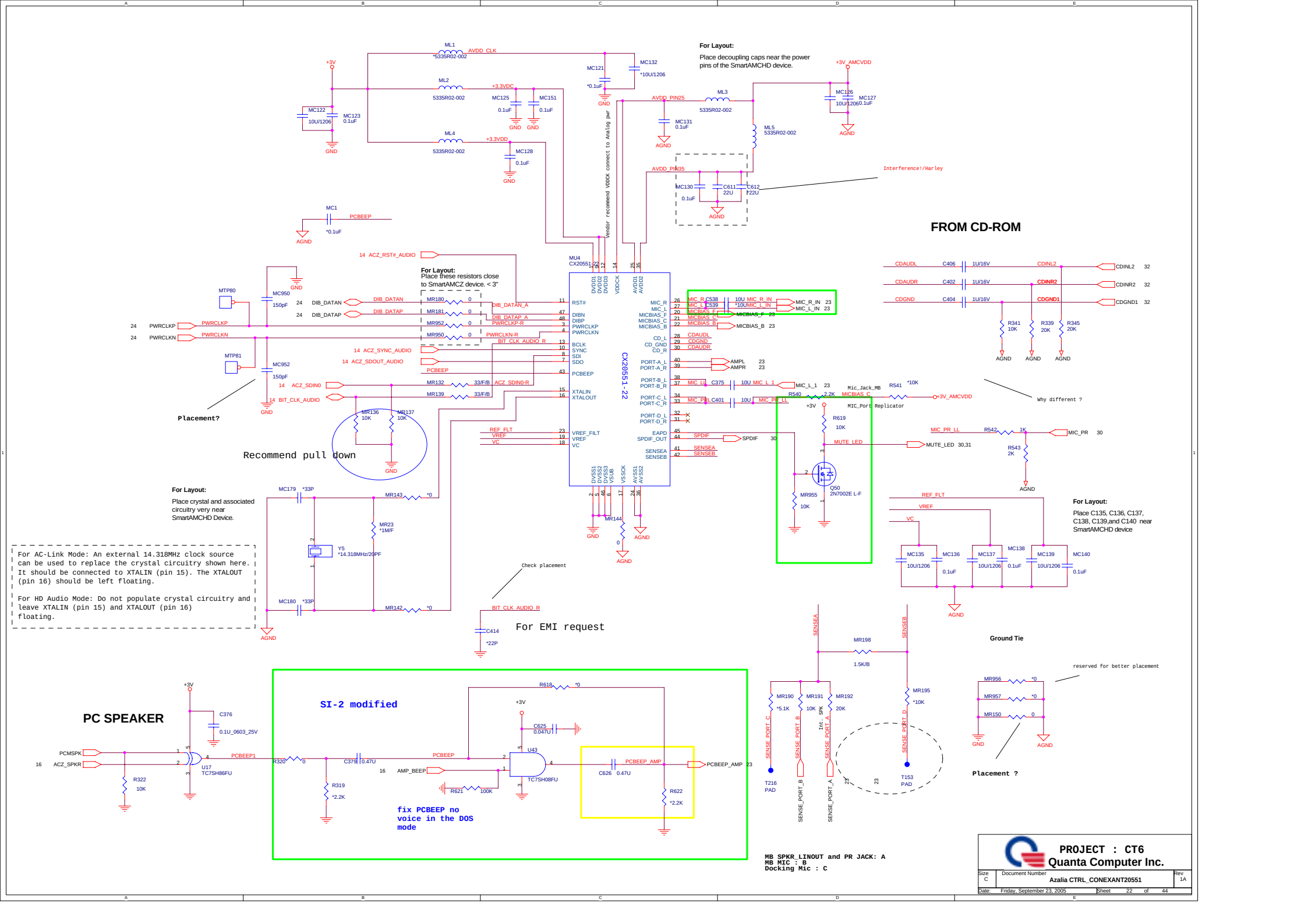




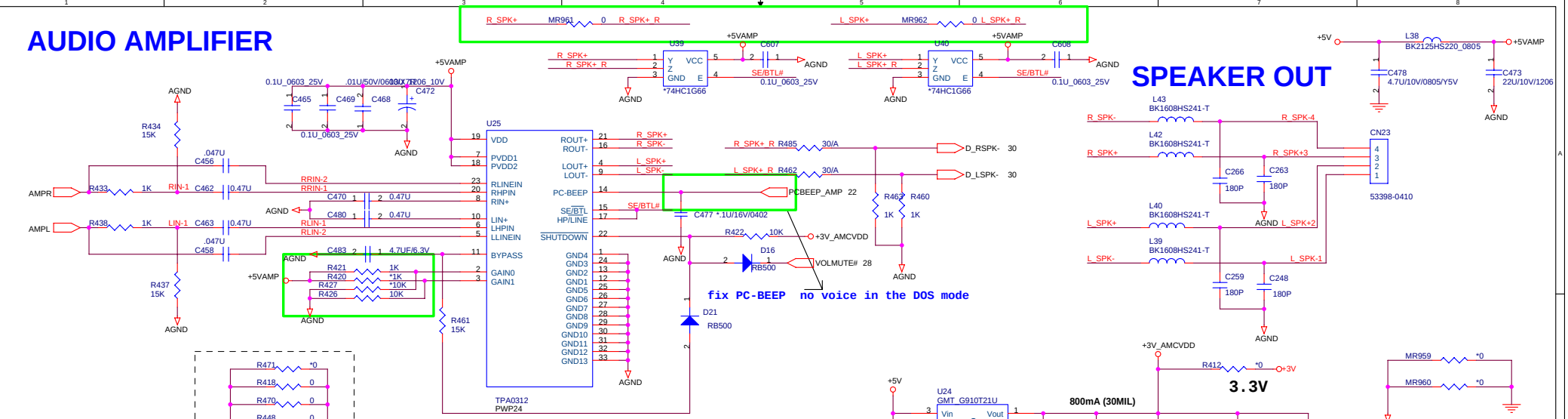
change from 0 ohm to 56 ohm (from vendor recommend)

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD READER CONN,USB x 2	1A
Date: Friday, September 23, 2005	Sheet 21 of 44	


For Layout:
Place decoupling caps near the power pins of the SmartAMCHD device.
FROM CD-ROM
Interference!/Harley
Placement?
Recommend pull down
For Layout:
Place these resistors close to SmartAMCZ device. < 3"
For Layout:
Place crystal and associated circuitry very near SmartAMCHD Device.
For AC-Link Mode: An external 14.318MHz clock source can be used to replace the crystal circuitry shown here. It should be connected to XTALIN (pin 15). The XTALOUT (pin 16) should be left floating.
For HD Audio Mode: Do not populate crystal circuitry and leave XTALIN (pin 15) and XTALOUT (pin 16) floating.
Check placement
For EMI request
For Layout:
Place C135, C136, C137, C138, C139,and C140 near SmartAMCHD device
Why different ?
Mic_Jack_MB
MIC_Port Replicator
Ground Tie
reserved for better placement
Placement ?
PC SPEAKER
SI-2 modified
fix PCBEEP no voice in the DOS mode
MB SPKR_LINOUT and PR JACK: A
MB MIC : B
Docking Mic : C
PROJECT : CT6
Quanta Computer Inc.
Azalia CTRL_CONEXANT20551
Friday, September 23, 2005

AUDIO AMPLIFIER

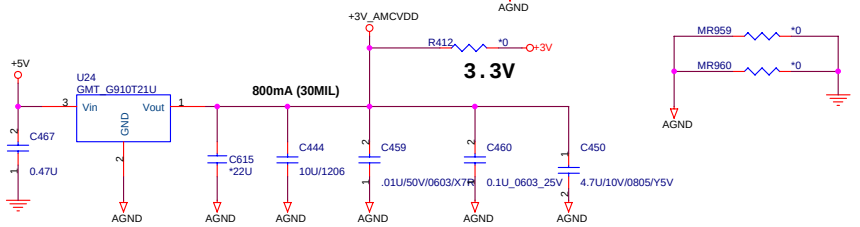


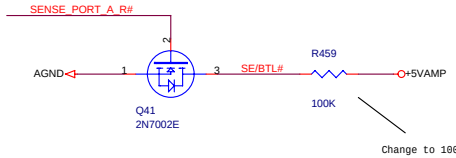
Placement ?

0312 Gain Table

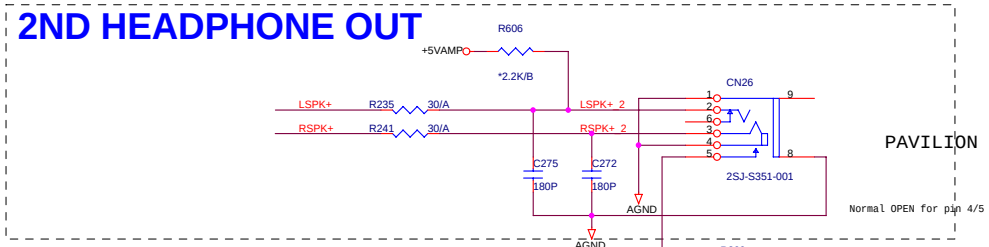
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

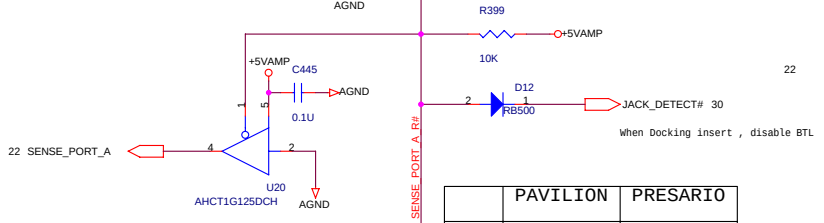
SPEAKER OUT





2ND HEADPHONE OUT

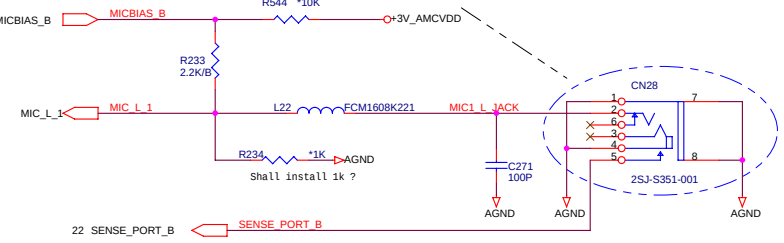




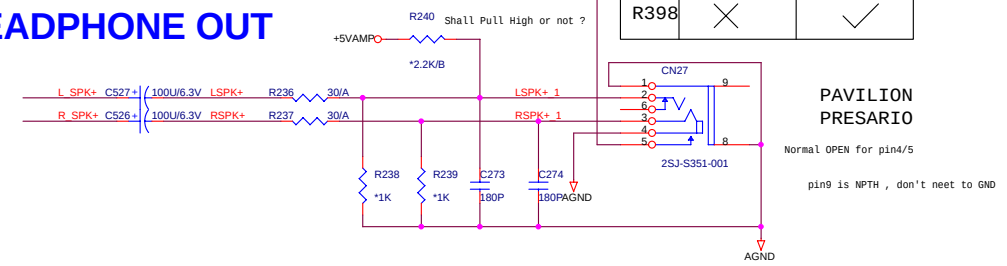
	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

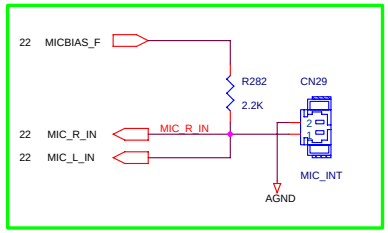
MIC JACK

Fox : JA6333L-1S0-TR => AC97
JA6333L-3S0-TR => Azalia



HEADPHONE OUT





Internal MIC

PROJECT : CT6
Quanta Computer Inc.

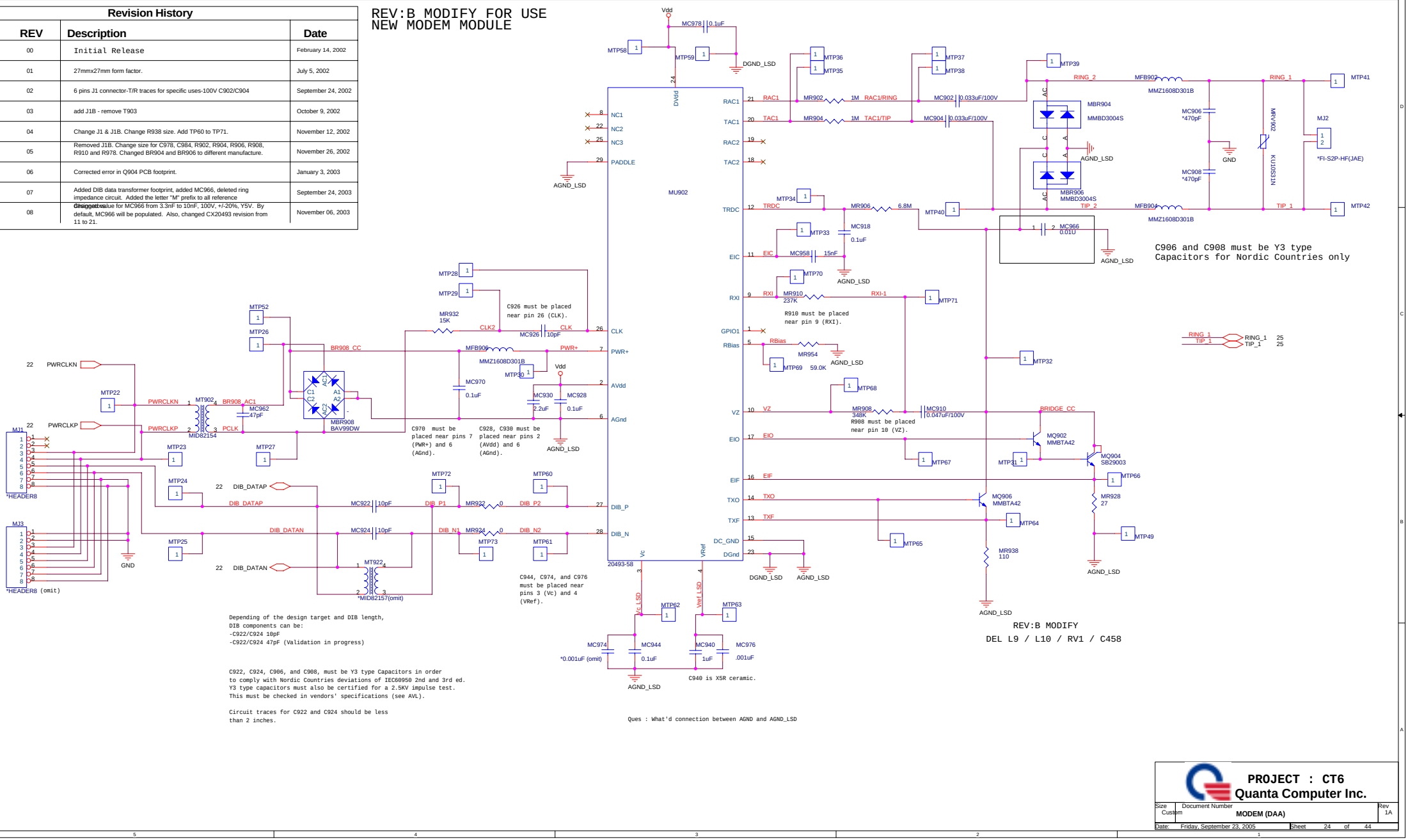
Size	Document Number	Rev
Custom	JACK,AMP_TPA0312	1A

Date: Friday, September 23, 2005 Sheet 23 of 44

Revision History

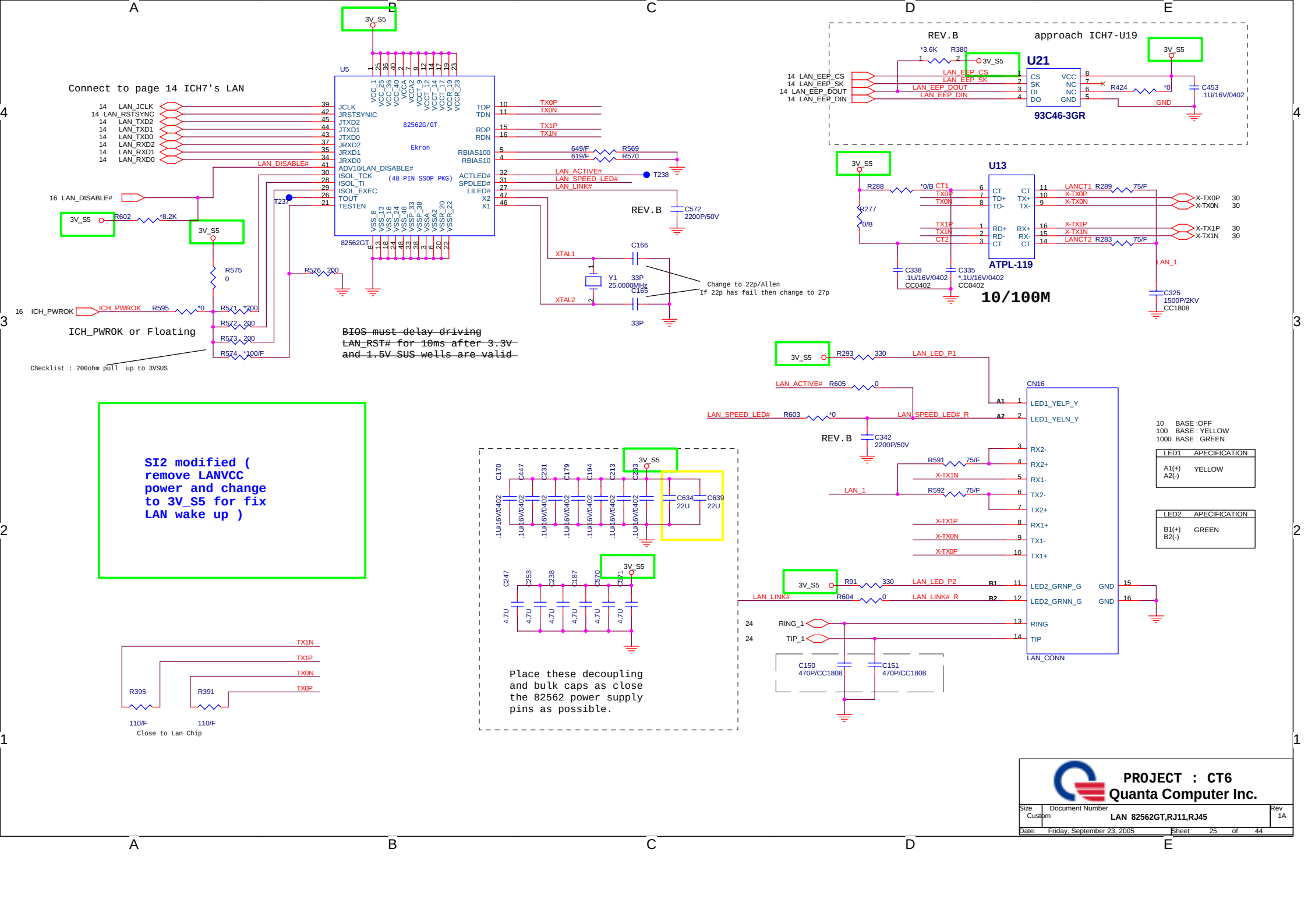
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

REV:B MODIFY FOR USE
NEW MODEM MODULE

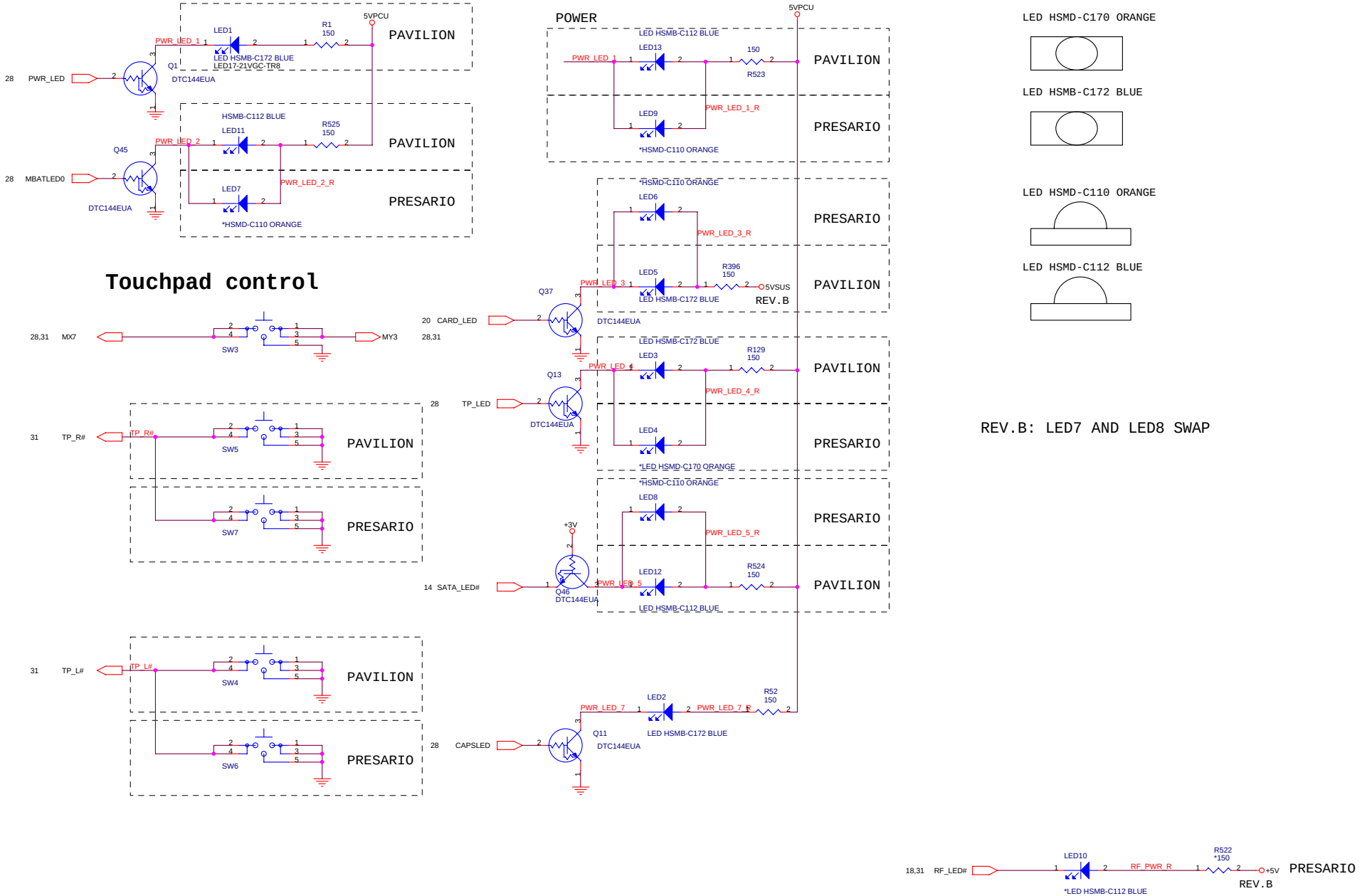


PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM (DAA)	1A
Date: Friday, September 23, 2005	Sheet 24 of 44	

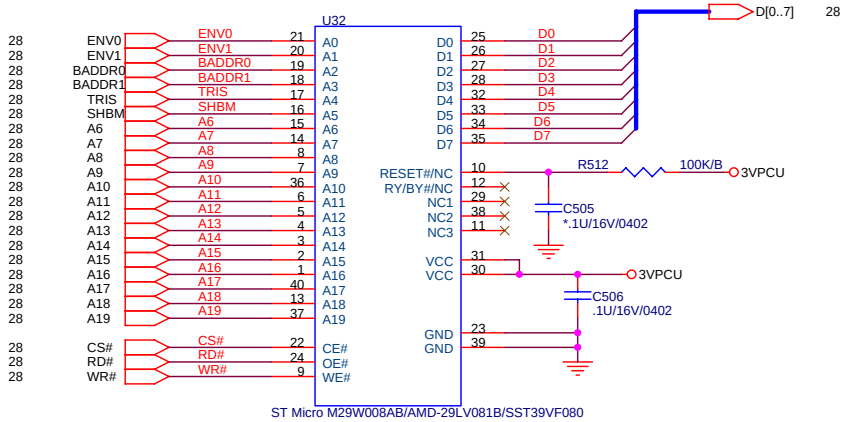


PROJECT :	CT6
Quanta Computer Inc.	
Size: Custom	Document Number: LAN 82562GT,RJ11,RJ45
Rev: 1A	
Date: Friday, September 23, 2005	Sheet 25 of 44



PROJECT : CT6			
Quanta Computer Inc.			
Size: Custom	Document Number: LED, SW		Rev: 1A
Date: Friday, September 23, 2005	Sheet 26 of 44		

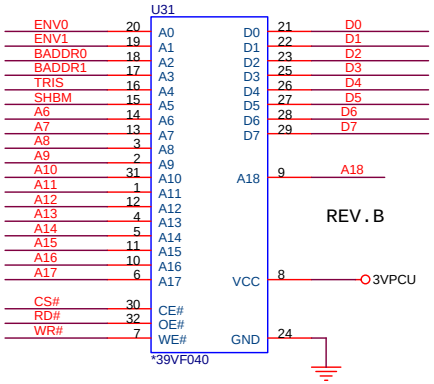
8Mbit (1M Byte), TSSOP40



AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

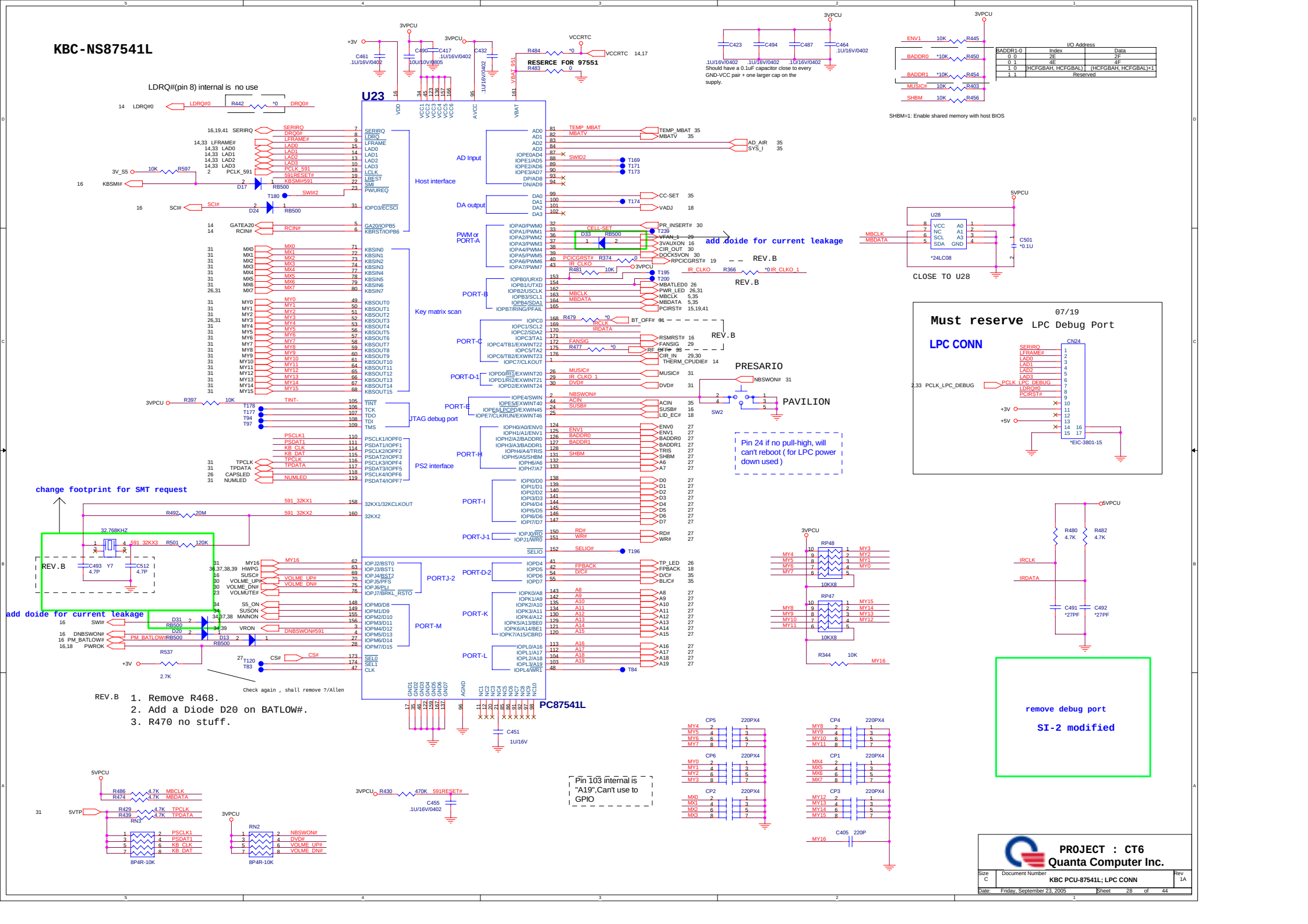
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

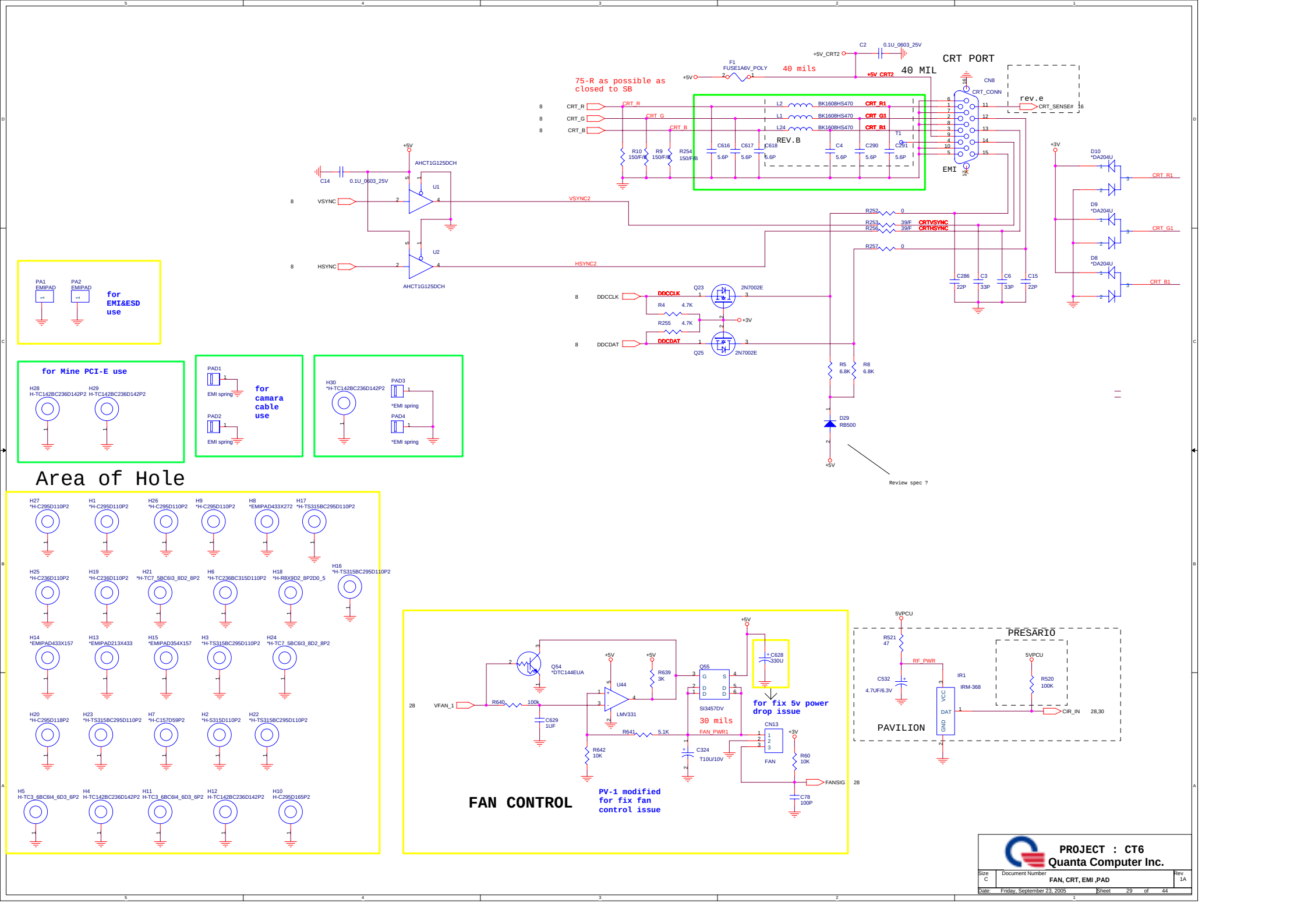
4Mbit (512k Byte), TSSOP32

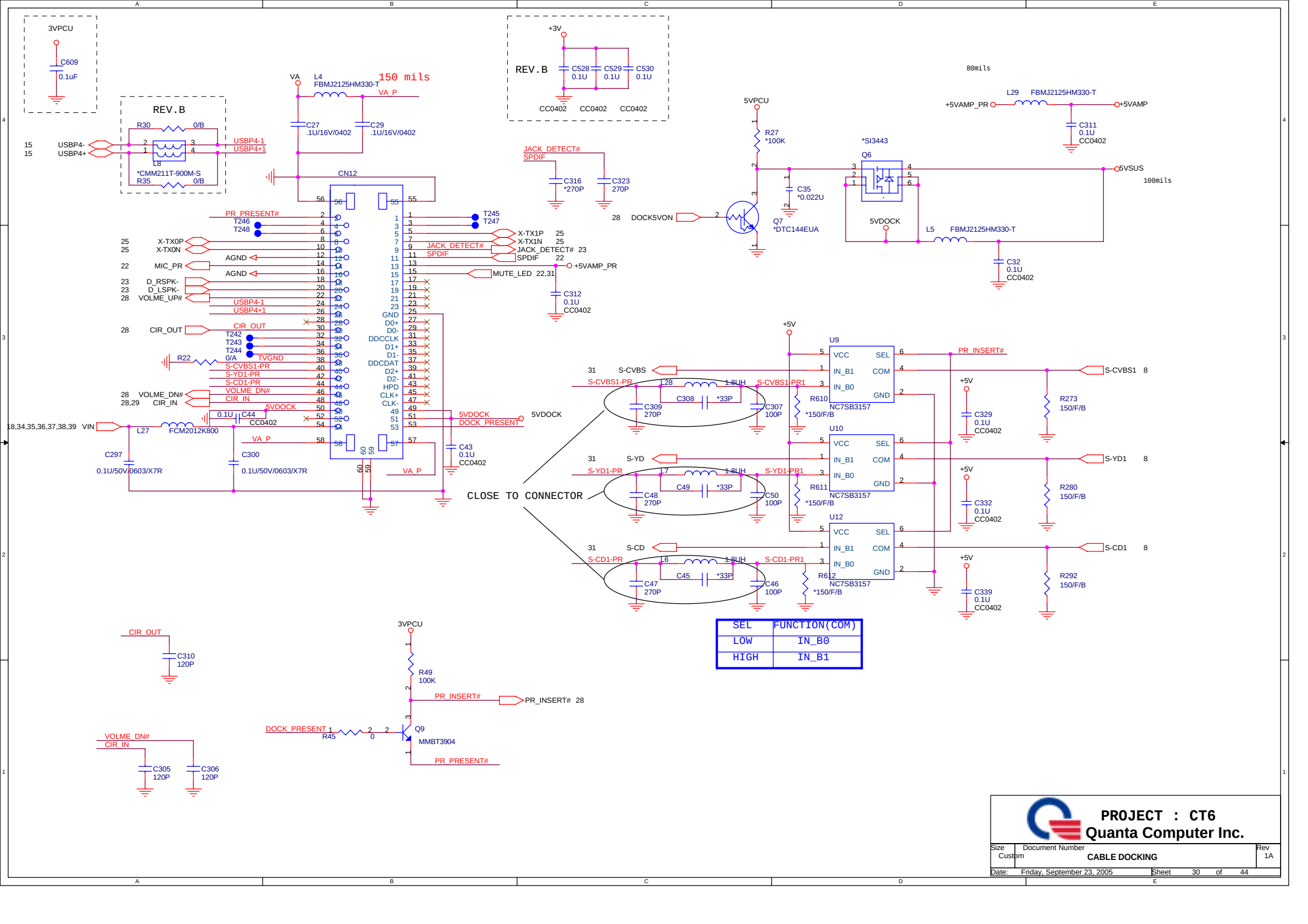


PROJECT : CT6		
Quanta Computer Inc.		
Size: B	Document Number: BIOS ROM	Rev: 1A
Date: Friday, September 23, 2005	Sheet 27 of 44	

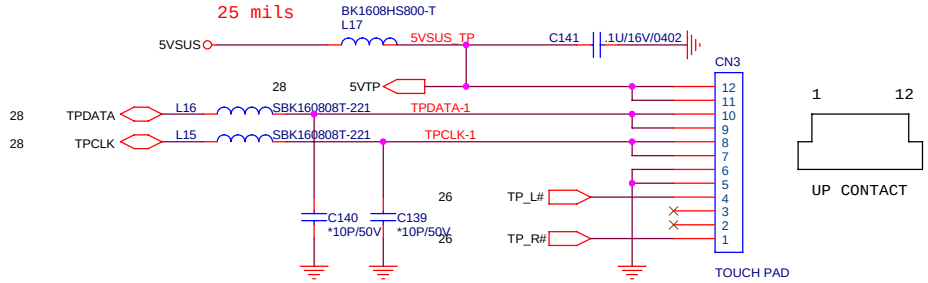
KBC-NS87541L




CRT PORT
40 MIL
40 mils
75-R as possible as closed to SB
REV.B
rev.e
EMI
for EMI&ESD use
for Mine PCI-E use
for camara cable use
Area of Hole
for fix 5v power drop issue
30 mils
FAN CONTROL
PV-1 modified for fix fan control issue
PRESARIO
PAVILION
Review spec ?
PROJECT : CT6
Quanta Computer Inc.
FAN, CRT, EMI ,PAD
Friday, September 23, 2005

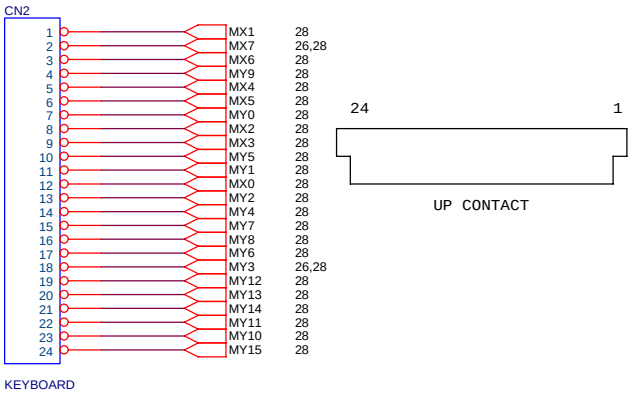

3VPCU
C609
0.1uF
REV.B
R30 0/B
R35 0/B
L8
*CMM211T-900M-S
15 USBP4-
15 USBP4+
USBP4-1
USBP4+1
VA
L4
FBMJ2125HM330-T
150 mils
VA_P
C27 .1U/16V/0402
C29 .1U/16V/0402
CN12
PR_PRESENT#
T246
T248
T245
T247
25 X-TX0P
25 X-TX0N
X-TX1P 25
X-TX1N 25
AGND
22 MIC_PR
JACK_DETECT#
SPDIF
JACK_DETECT# 23
SPDIF 22
MUTE_LED 22,31
+5VAMP_PR
23 D_RSPK-
23 D_LSPK-
28 VOLME_UP#
USBP4-1
USBP4+1
GND
D0+
D0-
DDCCLK
D1+
D1-
DDCDAT
D2+
D2-
HPD
CLK+
CLK-
28 CIR_OUT
CIR_OUT
T242
T243
T244
0/A
TVGND
R22
S-CVBS1-PR
S-YD1-PR
S-CD1-PR
28 VOLME_DN#
28,29 CIR_IN
VOLME_DN#
CIR_IN
5VDOCK
0.1U C44 CC0402
18,34,35,36,37,38,39 VIN
L27 FCM2012K800
VA_P
C43 0.1U CC0402
5VDOCK
DOCK_PRESENT
C297 0.1U/50V/0603/X7R
C300 0.1U/50V/0603/X7R
C316 *270P
C323 270P
C312 0.1U CC0402
28 DOCK5VON
REV.B
+3V
C528 0.1U
C529 0.1U
C530 0.1U
CC0402 CC0402 CC0402
5VPCU
R27 *100K
C35 *0.022U
Q7 *DTC144EUA
*SI3443
Q6
5VDOCK
80mils
L29 FBMJ2125HM330-T
+5VAMP_PR
+5VAMP
C311 0.1U CC0402
5VSUS
100mils
L5 FBMJ2125HM330-T
C32 0.1U CC0402
+5V
U9
U10
U12
VCC
SEL
IN_B1
IN_B0
COM
GND
NC7SB3157
31 S-CVBS
S-CVBS1-PR
L28 1.8UH
C308 *33P
C309 270P
C307 100P
R610 *150/F/B
PR_INSERT#
S-CVBS1 8
R273 150/F/B
C329 0.1U CC0402
31 S-YD
S-YD1-PR
L7 1.8UH
C49 *33P
C48 270P
C50 100P
R611 *150/F/B
S-YD1 8
R280 150/F/B
C332 0.1U CC0402
31 S-CD
S-CD1-PR
L6 1.8UH
C45 *33P
C47 270P
C46 100P
R612 *150/F/B
S-CD1 8
R292 150/F/B
C339 0.1U CC0402
CLOSE TO CONNECTOR
SEL FUNCTION(COM)
LOW IN_B0
HIGH IN_B1
CIR_OUT
C310 120P
3VPCU
R49 100K
PR_INSERT#
PR_INSERT# 28
DOCK_PRESENT
R45 0
Q9
MMBT3904
PR_PRESENT#
VOLME_DN#
CIR_IN
C305 120P
C306 120P
PROJECT : CT6
Quanta Computer Inc.
Size Custom
Document Number
CABLE DOCKING
Rev 1A
Date: Friday, September 23, 2005
Sheet 30 of 44

TOUCH PAD CONNECTOR

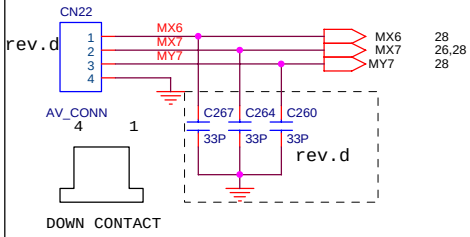


CHECK PIN DEFINE

KEYBOARD CONNECTOR



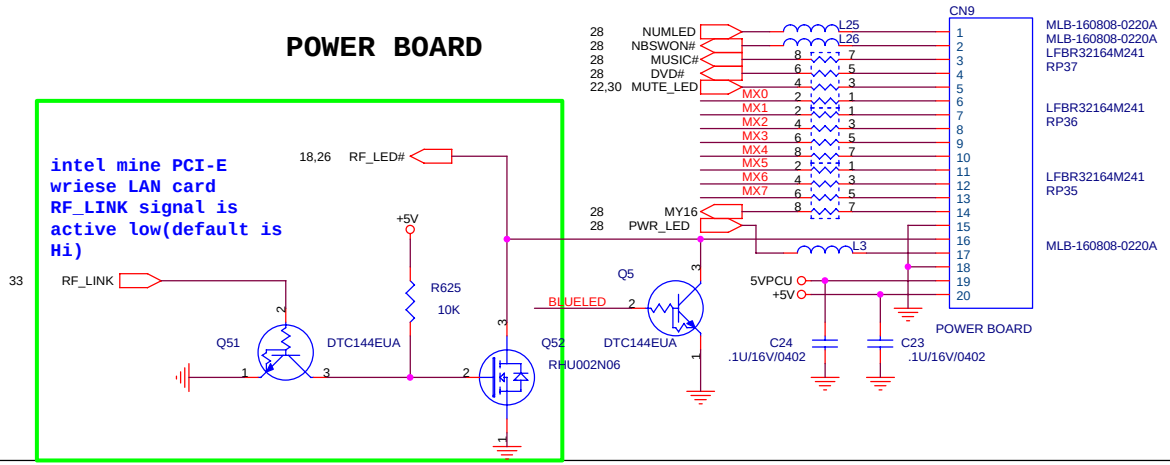
AV BOARD

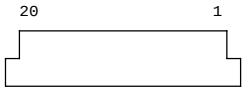


MX6	MX7
ENTER	MENU

POWER BOARD

intel mine PCI-E wriese LAN card RF_LINK signal is active low(default is Hi)

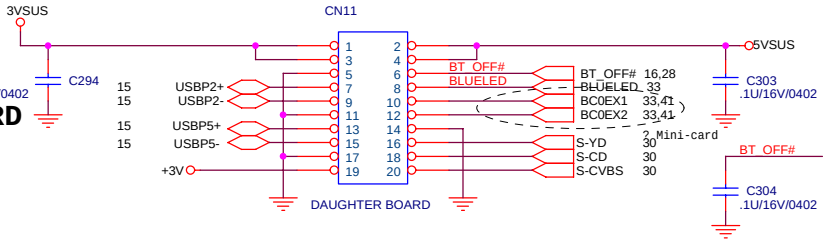


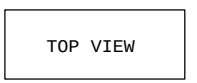


MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

STOP =>MX0+MY12
NEW=>MX1+MY12

DAUGHTER BOARD

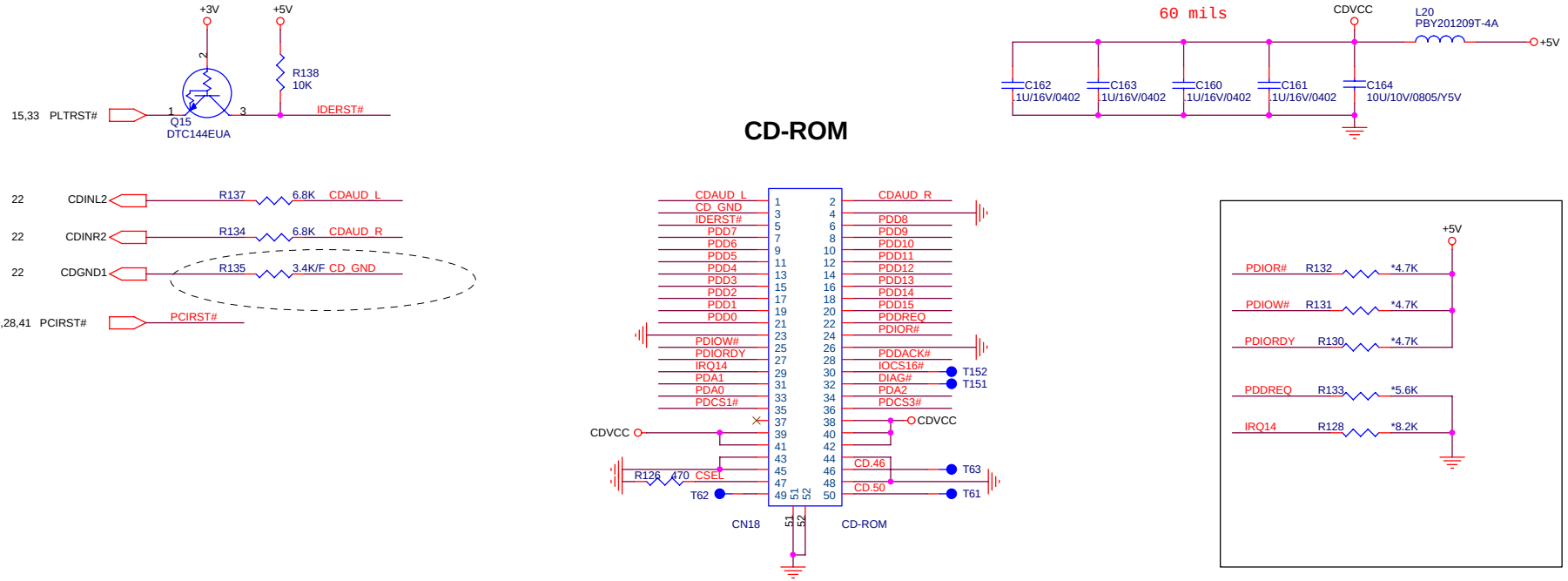




PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH/TP/KEY/BTB	1A

Date: Friday, September 23, 2005 Sheet 31 of 44


+3V
+5V
R138
10K
15,33 PLTRST#
Q15
DTC144EUA
IDERST#
60 mils
CDVCC
L20
PBY201209T-4A
+5V
C162
1U/16V/0402
C163
1U/16V/0402
C160
1U/16V/0402
C161
1U/16V/0402
C164
10U/10V/0805/Y5V
CD-ROM
22 CDINL2
R137 6.8K CDAUD_L
22 CDINR2
R134 6.8K CDAUD_R
22 CDGND1
R135 3.4K/F CD_GND
15,19,28,41 PCIRST#
PCIRST#
CDAUD_L
CD_GND
IDERST#
PDD7
PDD6
PDD5
PDD4
PDD3
PDD2
PDD1
PDD0
PDIOW#
PDIORDY
IRQ14
PDA1
PDA0
PDCS1#
CDAUD_R
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
PDDREQ
PDIOR#
PDDACK#
IOCS16#
DIAG#
PDA2
PDCS3#
T152
T151
CDVCC
CDVCC
R126 470 CSEL
T62
CD.46
CD.50
T63
T61
CN18
CD-ROM
+5V
PDIOR# R132 *4.7K
PDIOW# R131 *4.7K
PDIORDY R130 *4.7K
PDDREQ R133 *5.6K
IRQ14 R128 *8.2K
14 PDA[0..2]
PDA[0..2]
14 PDD[0..15]
PDD[0..15]
14 PDIOW#
14 PDDREQ
14 PDIORDY
14 PDIOR#
14 IRQ14
14 PDDACK#
14 PDCS1#
14 PDCS3#
PDIOW#
PDDREQ
PDIORDY
PDIOR#
IRQ14
PDDACK#
PDCS1#
PDCS3#
SATA CONNECTOR
CN19
GND1
TXP
TXN
GND2
RXN
RXP
GND3
3.3V
3.3V
3.3V
GND
GND
GND
5V
5V
5V
GND
RSVD
GND
12V
12V
12V
SATA_TXP0 14
SATA_TXN0 14
SATA_RXN0 14
SATA_RXP0 14
+3VSATA
R390 0/A +3V
HDD_VDD
T190
T194
T197
T198
127043FB022G201ZR
BOM P/N:DFHD07MS159
HDD_VDD R372 0/A +5V
+3VSATA
HDD_VDD
C436
C443
C449
4.7U/10V/0805
4.7U/10V/0805
0.1U
C633
22U
C613
22U
C614
0.1U
change footprint for SMT request(
add 防呆 pin)
PROJECT : CT6
Quanta Computer Inc.
Size Custom
Document Number
SATA HDD, CD-ROM
Rev 1A
Date: Friday, September 23, 2005
Sheet 32 of 44

Mini PCI-E Card

PV-1 modified (R478 need to stuff for fix wireless LED always on when wireless lan card and bluetooh module not inser)

to fix RF_LINK LED function

SI-2 modified

PV-I modified (mini PCI-E card internal has a serial cap,change component from 0.1u cap to 0 ohm)

PCI-Express TX and RX direct to connector

SI-2 modified

add minepci-e debug port function

SI-2 modified

add minepci-e debug port function

Need one more wireless LED /mini card on MB ?
currently , No LED here

RF_LINK# , check with KN1

NEWCARD (PCIEXPRESS*1 + USB*1)

UNISTALL R337 ,R336,R386,R387 due to internal R of R5538

PV-I modified (Epress card internal has a serial cap,change component from 0.1uf to 0 ohm)

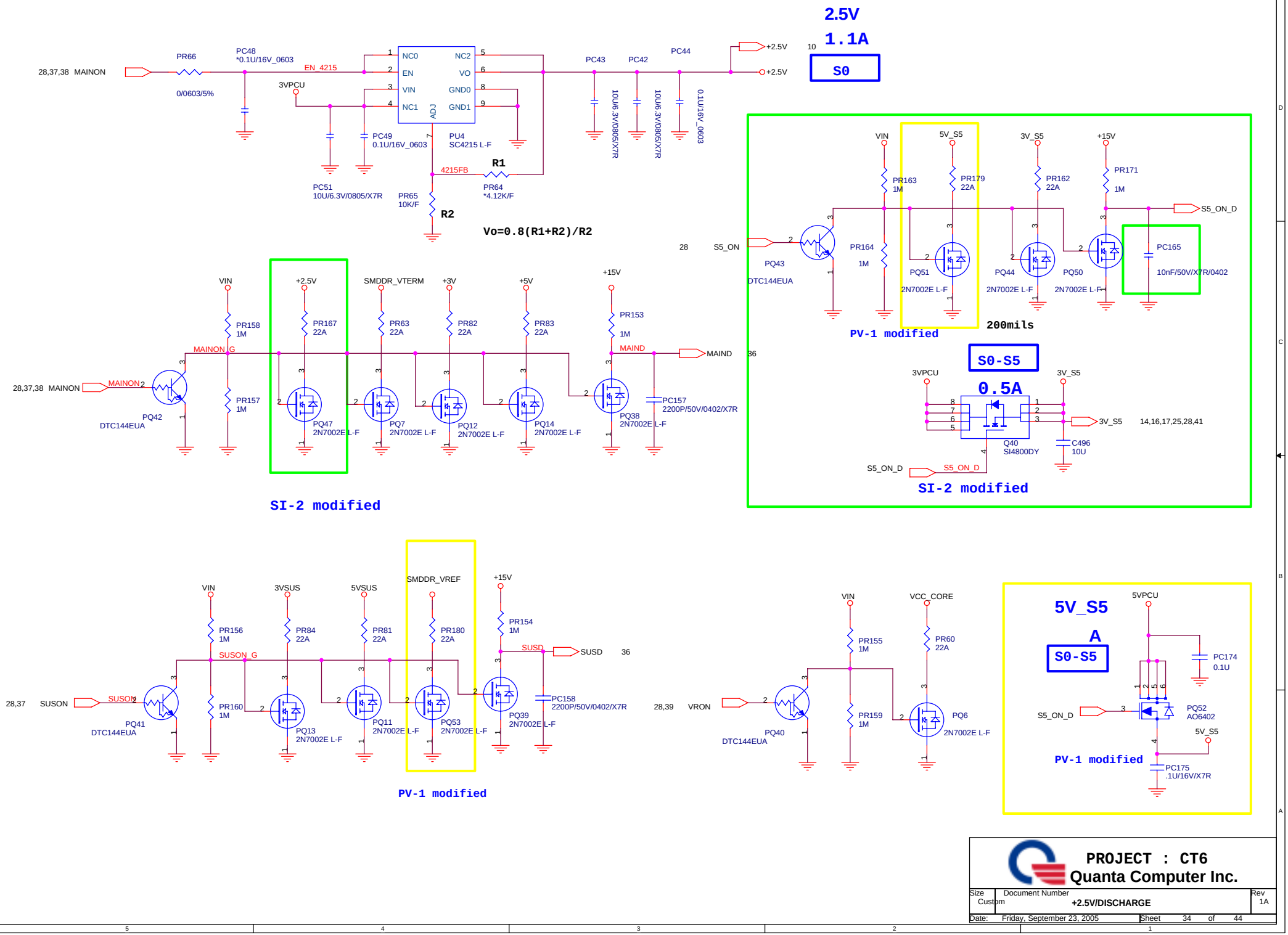
PCI-Express TX and RX direct to connector

JAE PX10FS16PH-26P

change footprint for ME request

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD, MINI CARD	1A
Date: Friday, September 23, 2005	Sheet 33 of 44	



PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+2.5V/DISCHARGE	1A
Date: Friday, September 23, 2005	Sheet 34 of 44	

BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A

Second:BAM66790014

From Docking CNN

20 MIL TO CABLE DOCK

EMI
SI-2 modified

Battery Low 7.5V

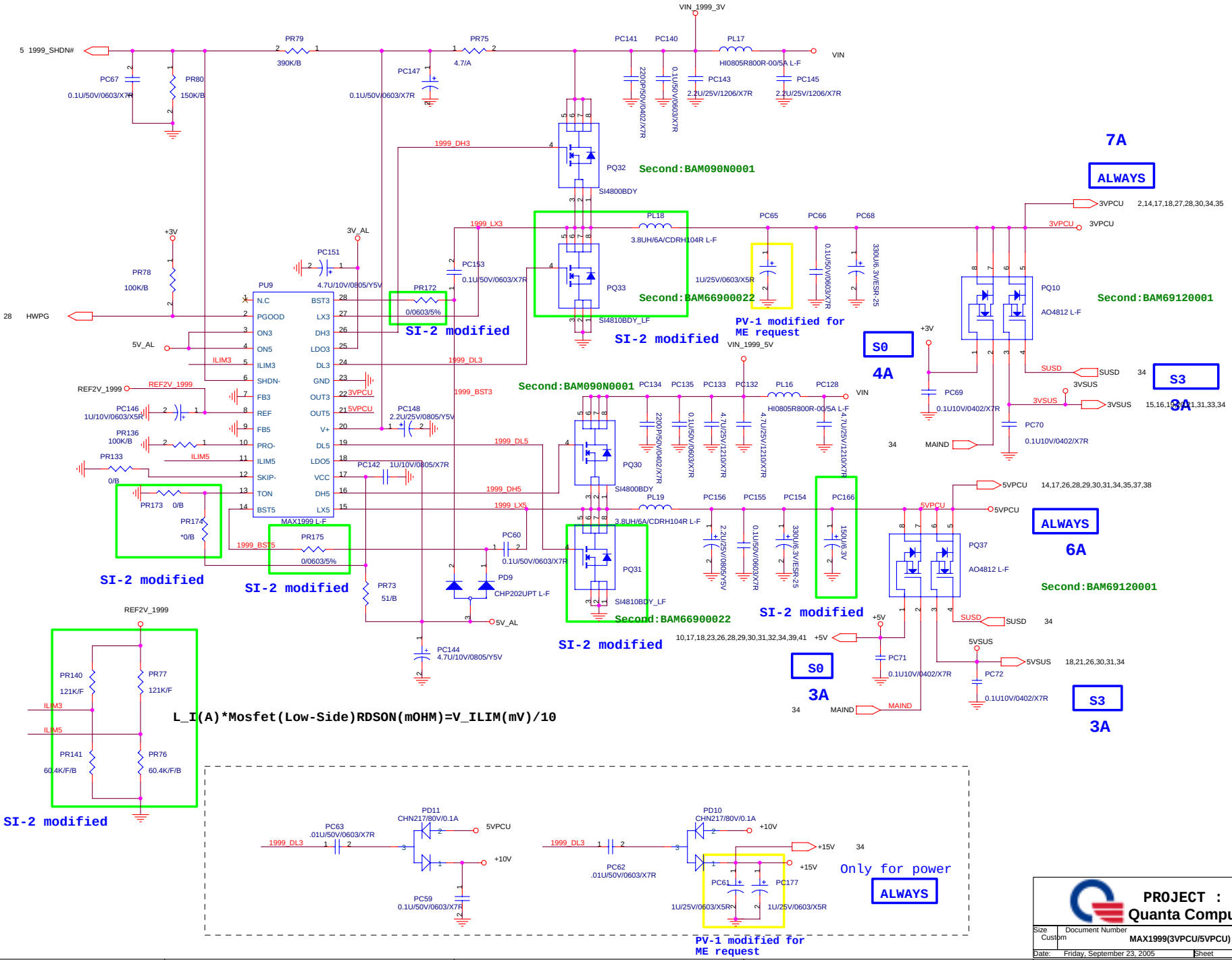
CELL-SET
HI = LDO = 4 CELL
LOW = LDO/2 = 3 CELL

CC-SET = 1.05V/A

EMI
SI-2 modified

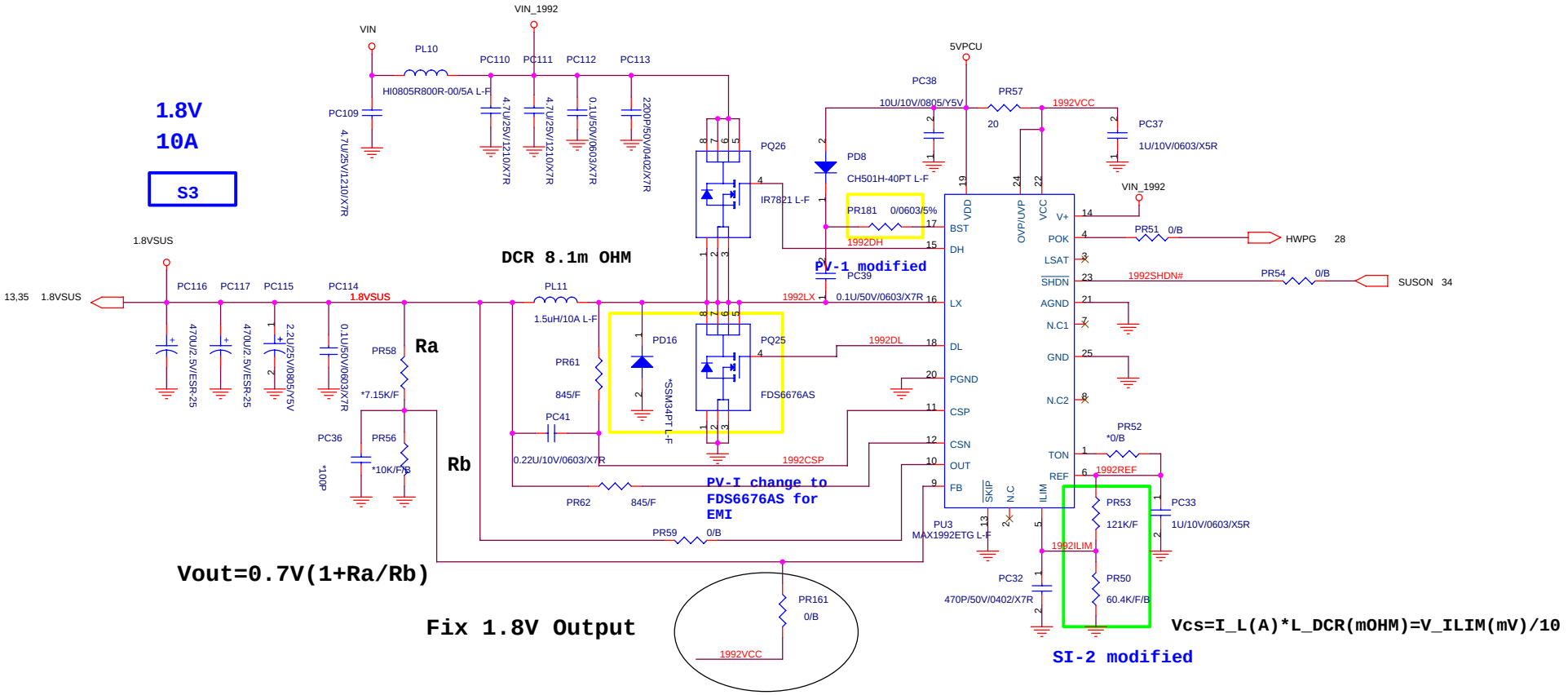
PROJECT : CT6
Quanta Computer Inc.

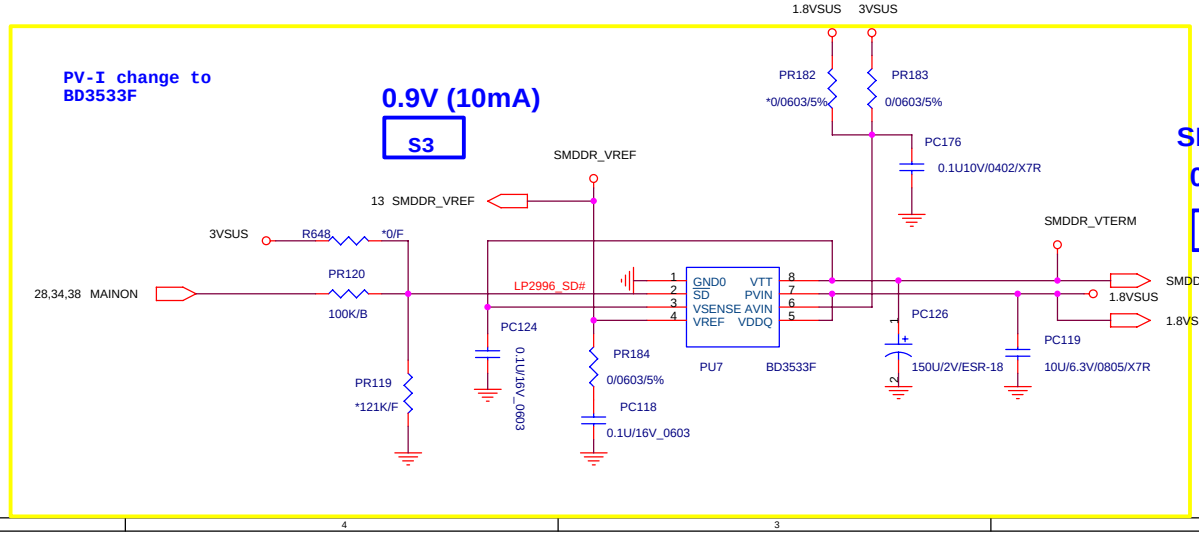
Size	Document Number	Rev
Custom	CHARGER MAX1772	1A
Date: Friday, September 23, 2005	Sheet 35 of 44	



Quanta Computer Inc.	PROJECT : CT6		
Size: Custom	Document Number: MAX1999(3VPCU/5VPCU)		Rev: 1A
Date: Friday, September 23, 2005	Sheet 36 of 44		

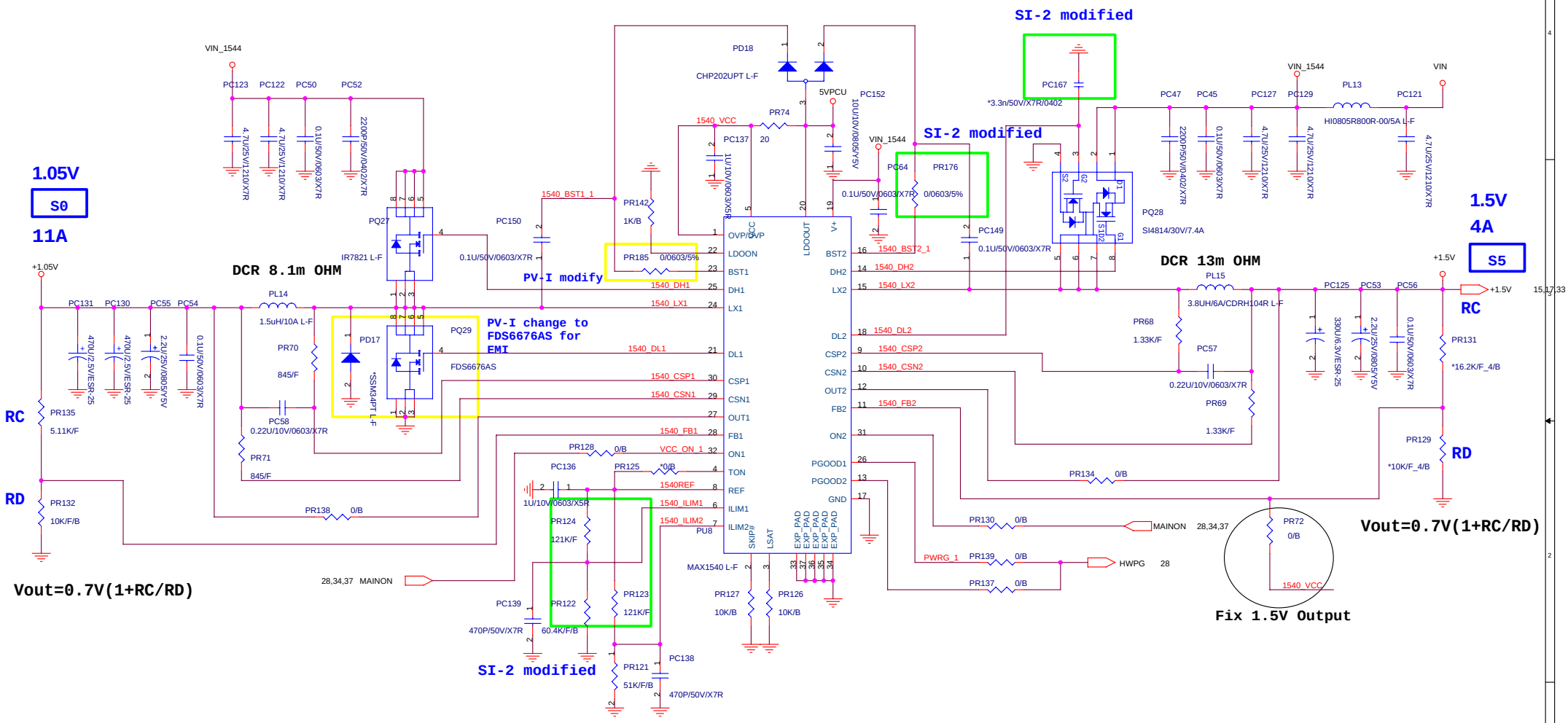
0.9V (0.1A)



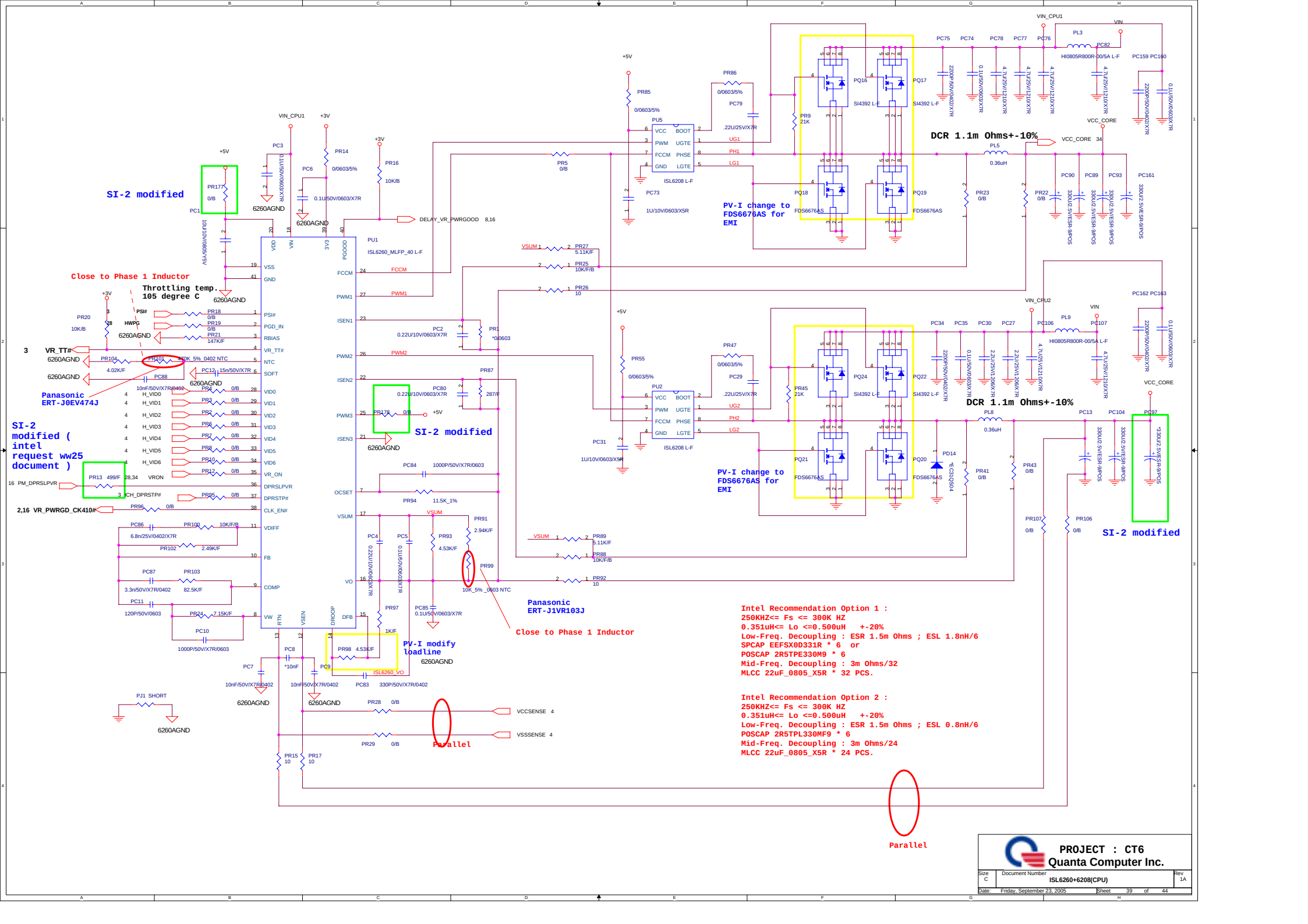


PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1992(1.8VSUS/DDR_VTERM)	1A
Date: Friday, September 23, 2005	Sheet 37 of 44	



PROJECT : CT6			
Quanta Computer Inc.			
Size: Custom	Document Number: MAX1540 (+1.05V/+1.5V)		Rev: 1A
Date: Friday, September 23, 2005		Sheet 38 of 44	


SI-2 modified
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
SI-2
modified (
intel
request ww25
document)
SI-2 modified
PV-I change to
FDS6676AS for
EMI
DCR 1.1m Ohms+-10%
PV-I change to
FDS6676AS for
EMI
DCR 1.1m Ohms+-10%
SI-2 modified
PV-I modify
loadline
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
Parallel
Intel Recommendation Option 1 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
SPCAP EEFSX0D331R * 6 or
POSCAP 2R5TPE330M9 * 6
Mid-Freq. Decoupling : 3m Ohms/32
MLCC 22uF_0805_X5R * 32 PCS.
Intel Recommendation Option 2 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
POSCAP 2R5TPL330MF9 * 6
Mid-Freq. Decoupling : 3m Ohms/24
MLCC 22uF_0805_X5R * 24 PCS.
PROJECT : CT6
Quanta Computer Inc.
ISL6260+6208(CPU)
Friday, September 23, 2005
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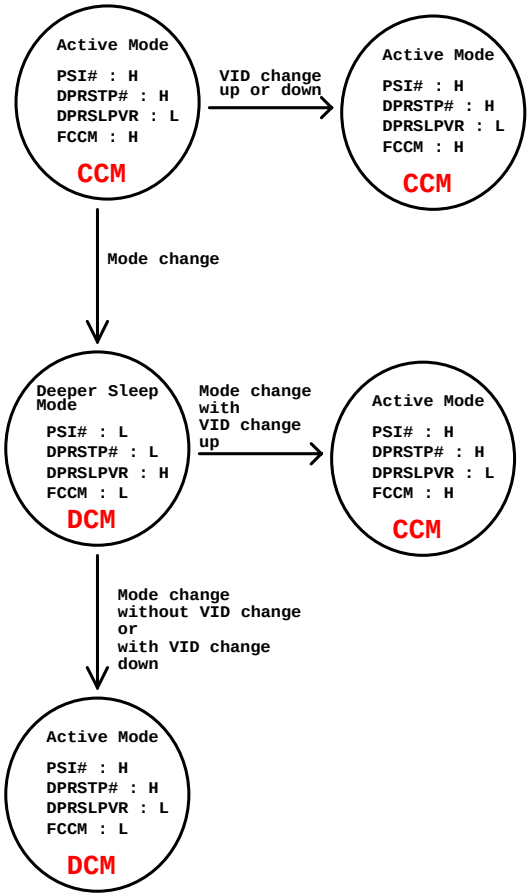
IMVP Spec. Rev. 0.8

(Nom.)	Yonah-2M	Meron
HFM	1.2875 V	1.1500 V
LFM	0.8375 V	0.8375 V
Deeper	0.7625 V	0.7625 V
VBOOT	1.2000 V	1.2000 V
SLOPE	-2.1 mV/A	-2.1 mV/A

(Max.)	Yonah-2M	Meron
HFM	36 A	44 A
LFM	9.5 A	12.5 A
Deeper	3.5 A	5.5 A
Dynamic	27 A	34.5 A
TDC	26 A	32 A

Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

CCM : Continuous Conduction Mode
DCM : Dis-Continuous Mode



PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_Operation State	1A

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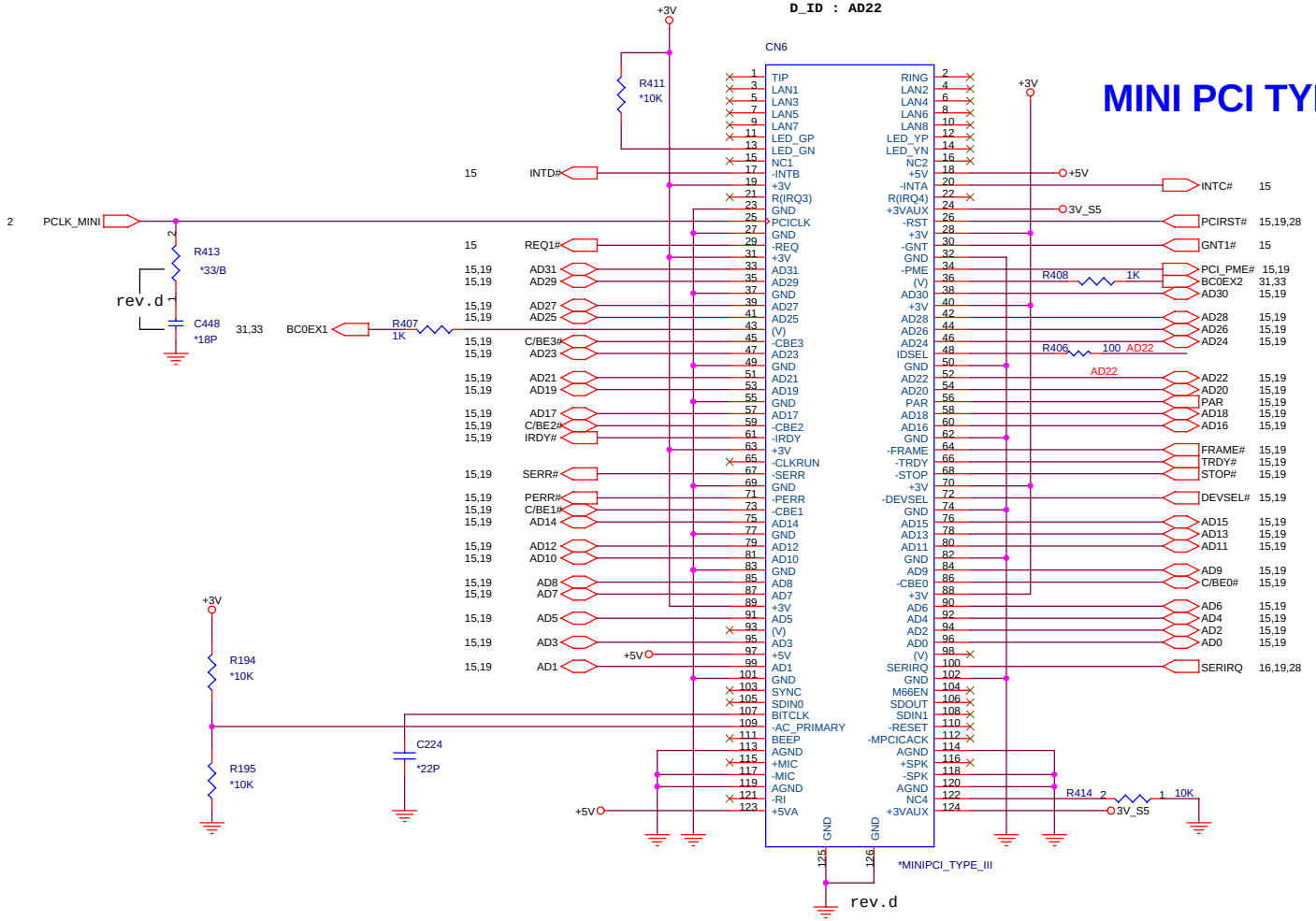
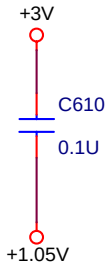
MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



	PROJECT : CT6 **Quanta Computer Inc.**		
Size: Custom	Document Number: **MINI PCI TYPE III SLOT**		Rev: 1A
Date: Friday, September 23, 2005		Sheet 41 of 44	



PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
A	**TPM**	1A

Date: Friday, September 23, 2005 Sheet 42 of 44

MODEL	REV	CHANGE LIST
CT6 MB 31CT6MBXXXX	1A	

Model	CT6 MB BOARD	
Page	FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	

PROJECT : CT6
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Size	Document Number	Rev
Custom	change list	1A

Date: Friday, September 23, 2005 Sheet 43 of 44

	description	31 BOM difference list (base on 31CT6MB0008 BOM)
31CT6MB0008	Pavilion FF	
31CT6MB0024	Pavilion FF+Camera/Mic	ADD : 1.CN30 2.CN31 3.CN32 → for camera connector 4.CN29 → for internal MIC connector
31CT6MB0016	Presario FF	ADD: LED 9 -- PWR_LED LED 8 --SATA_LED LED 7 --MBATLED LED4 --TP_LED LED2 --CAPD_LED LED6 --CARD_LED SW7 -- TP_R SWITCH SW6 -- TP_L SWITCH REMOVE: IR1--- IR component LED13--PWR_LED LED12 --SATA_LED LED11 --MBAT_LED C532 -- IR R521 -- IR CN22 -- AV BOARD CN26 -- 2ND H/P CON LED5 -- CARD LED LED3 -- TP_LED LED2 -- CAPS_LED LED1 -- PWR_LED C267 -- AV BOARD EMI C264 -- AV BOARD EMI C260 -- AV BOARD EMI C275 -- 2ND H/P EMI C272 -- 2ND H/P EMI R241 --2ND H/P damp res R235 --2ND H/P damp res R1 -- PWR RES SW5 -TP_R SWITCH SW4 -- TP_L SWITCH SW2-NBWON# SWITCH

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
B	change list	1A
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