

S-CLASS

Prince/Pearl

SI2 Build

2008/02/14

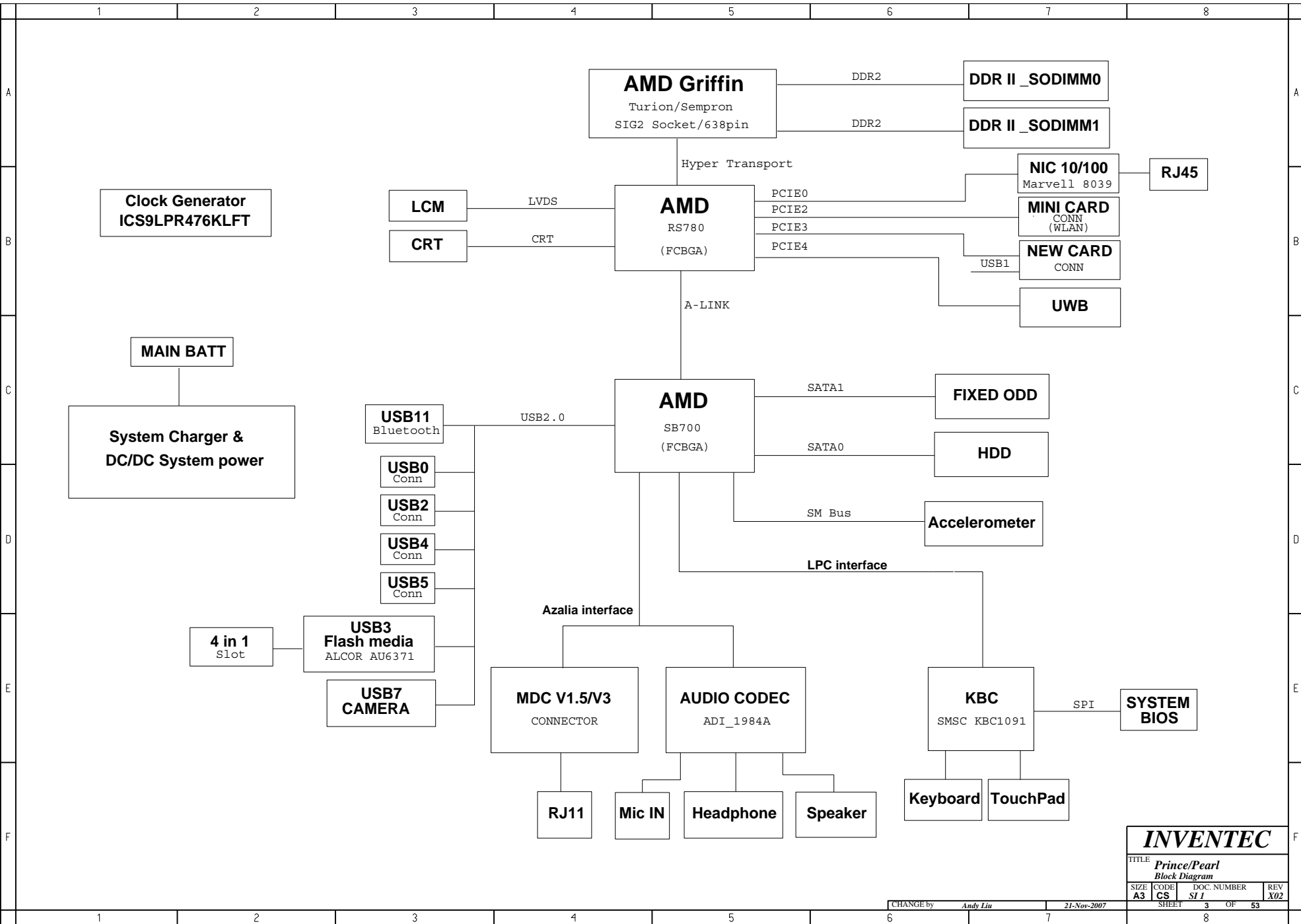
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					TITLE <i>Prince/Pearl</i>			
CHECK					RESPONSIBLE			
RESPONSIBLE					SIZE = 3 VER :			
FILE NAME :	XXXX-XXXXXX-XX				SIZE	CODE	DOC. NUMBER	REV
P/N	XXXXXXXXXXXX				A3	CS	SI1	X02
					SHEET	1 OF 53		

TABLE OF CONTENTS

<p>PAGE</p> <p>5- DC& BATTERY CHARGER</p> <p>6- SELECT & BATTERY CONN</p> <p>7- +V5A,+V3A & +V2.5S</p> <p>8- OCP</p> <p>9- +VCC_NB & +V1.2A</p> <p>10- +VCC_CORE</p> <p>11- POWER</p> <p>12- DDR2 POWER</p> <p>13- POWER(SLEEP)</p> <p>14- POWER(SEQUENCE)</p>	<p>PAGE</p> <p>15- CLOCK_GENERATOR</p> <p>16- CPU-1</p> <p>17- CPU-2</p> <p>18- CPU-3</p> <p>19- CPU-4</p> <p>20- THERMAL&FAN CONTROLLER</p> <p>21- RS780-1</p> <p>22- RS780-2</p> <p>23- RS780-3</p> <p>24- RS780-4</p> <p>25- DDR2-DIMM0</p> <p>26- DDR2-DIMM1</p> <p>27- DDR2-DAMPING</p> <p>28- CRT</p> <p>29- LCD CONN</p> <p>30- SB700-1</p> <p>31- SB700-2</p> <p>32- SB700-3</p> <p>33- SB700-4</p> <p>34- KBC</p>	<p>PAGE</p> <p>35- KB & TP CONN</p> <p>36- SPI & ACCELEROMETER</p> <p>37- HDD & ODD CONN</p> <p>38- USB CONN</p> <p>39- USB WEBCAM CONN</p> <p>40- FLASH MEDIA CARD</p> <p>41- AZALIA CODEC</p> <p>42- Earphone & MIC JACK</p> <p>43- AUDIO AMP & HP JACK</p> <p>44- MDC CNTR</p> <p>45- NIC 10/100- CONTROLLER</p> <p>46- NIC 10/100- RJ45 CONN</p> <p>47- MINICARD & BT CONN</p> <p>48- NEW CARD</p> <p>49- UWB CONN</p> <p>50- BUTTON & LED</p> <p>51- SCREW</p> <p>52- 15" ODD Extend Board</p> <p>53- SWITCH Board</p>
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INVENTEC			
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<i>Table Of Content</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>S11</i>	REV X02
CHANGE by <i>Andy Liu</i>		21-Nov-2007	
SHEET		2	OF 53

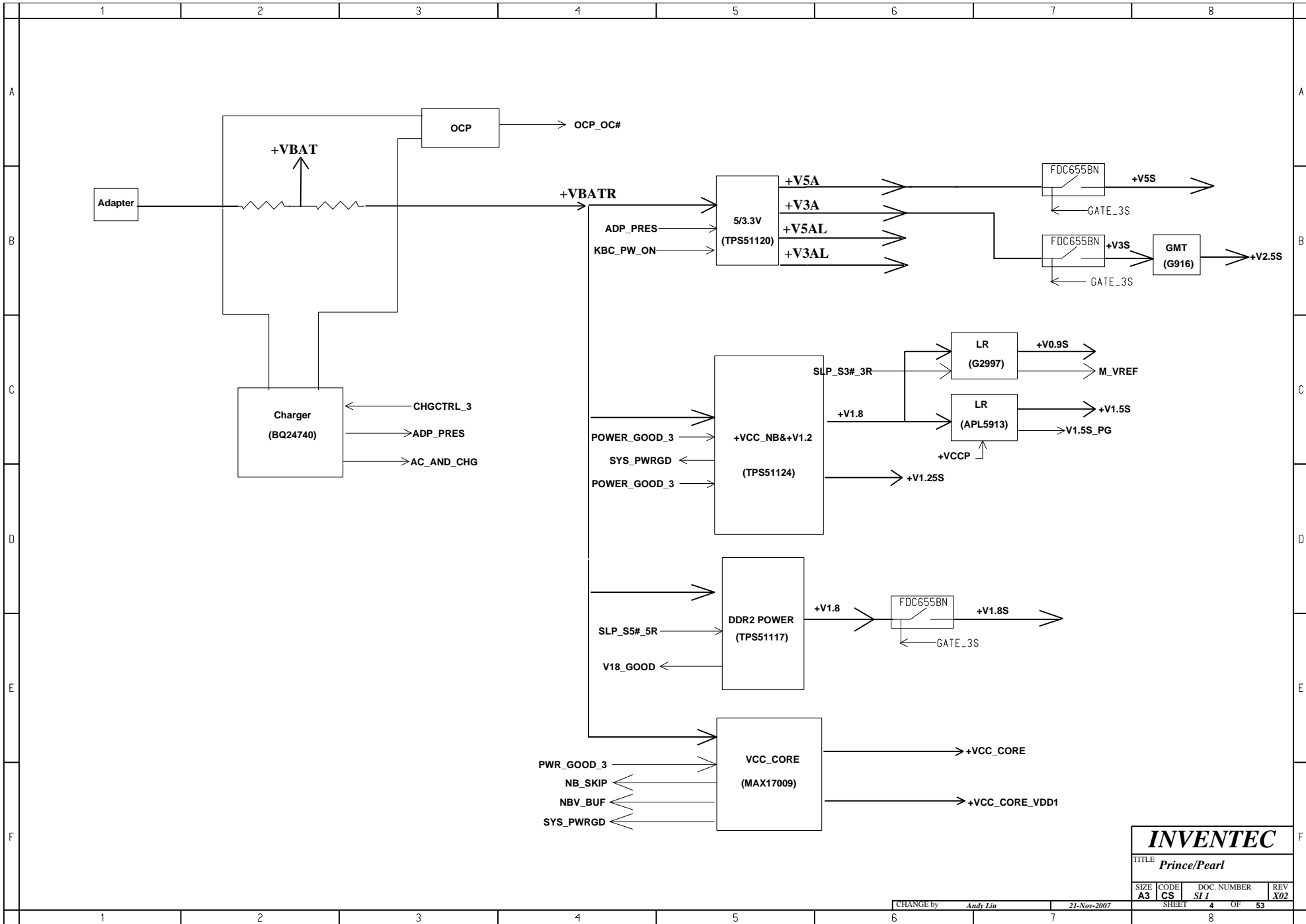


INVENTEC

TITLE
Prince/Pearl
Block Diagram

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by *Andy Liu* 21-Nov-2007
 SHEET 3 OF 53

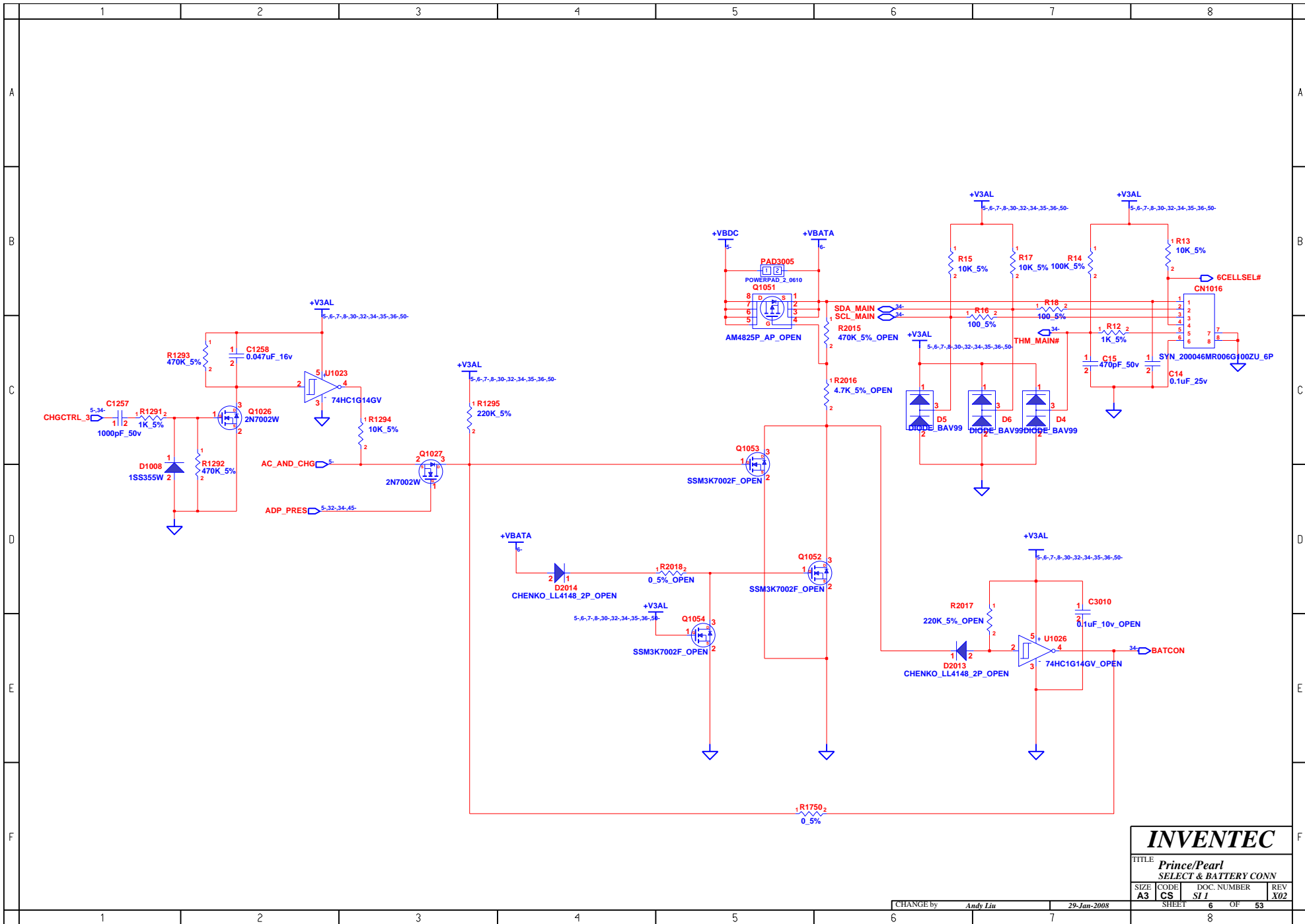


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CHANGE by *Andy Liu* 21-Nov-2007 SHEET 4 OF 53



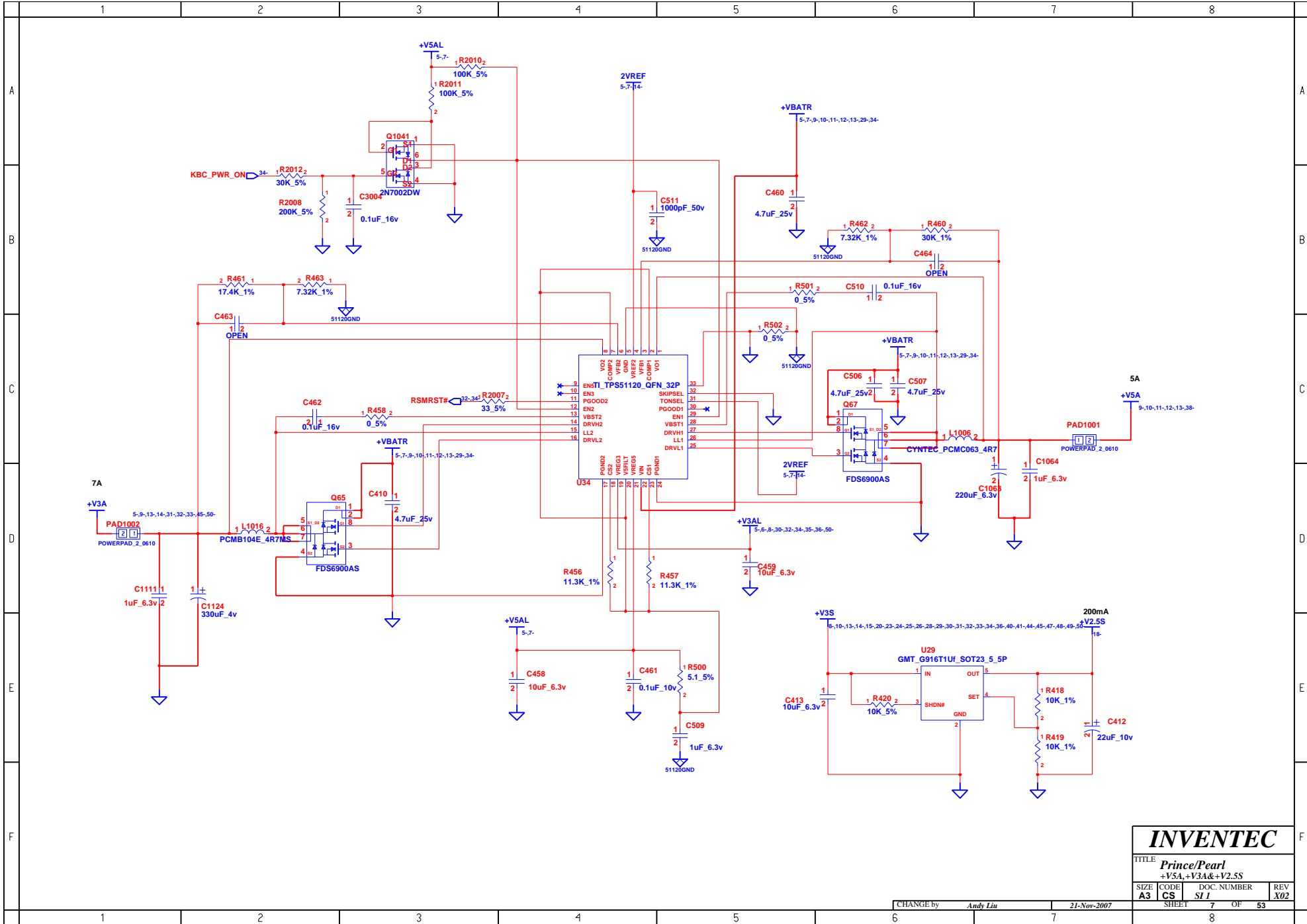
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TITLE
**Prince/Pearl
 SELECT & BATTERY CONN**

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CHANGE by *Andy Liu* 29-Jan-2008

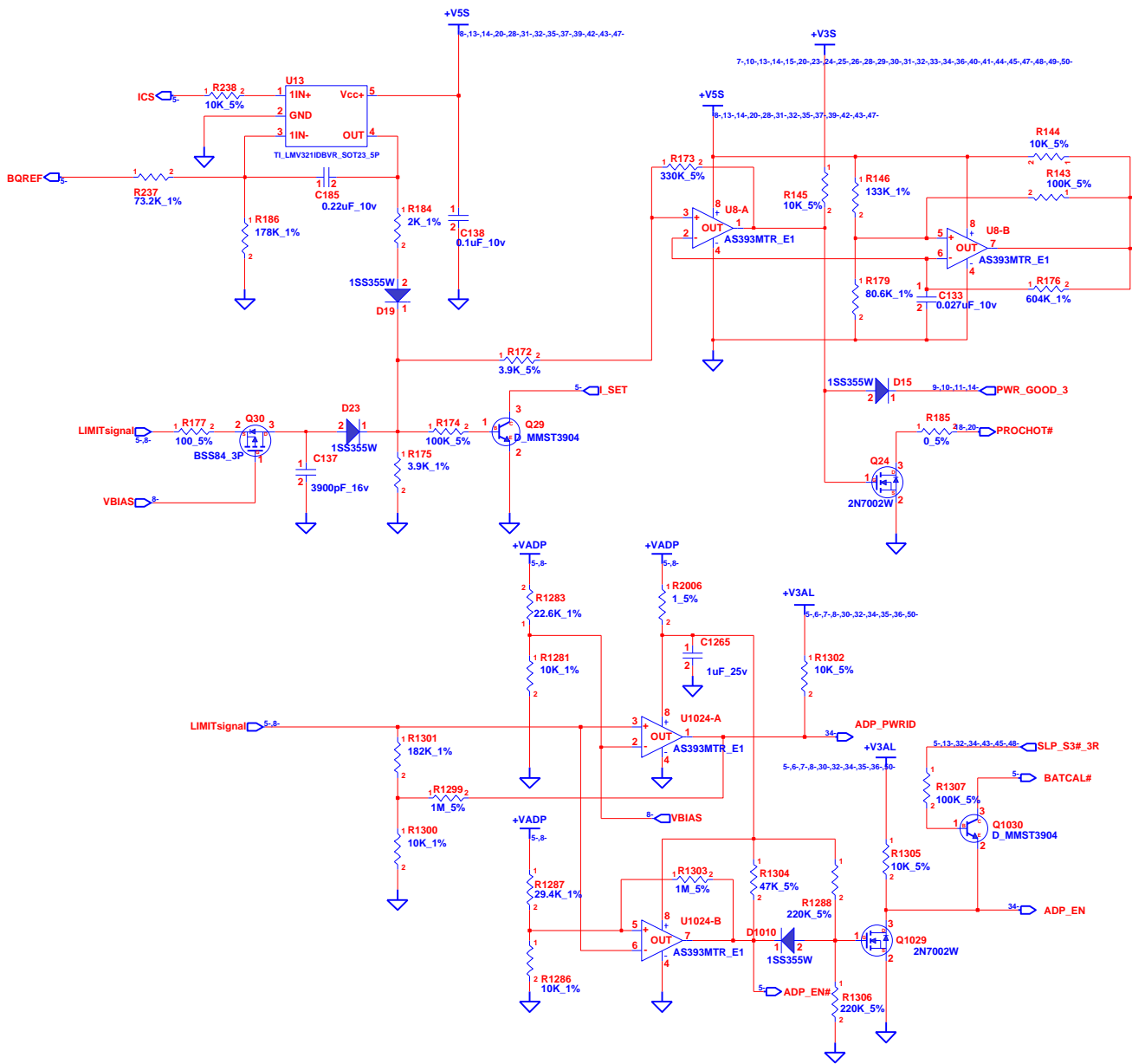
SHEET 6 OF 53



INVENTEC

TITLE
Prince/Pearl
 +V5A,+V3A&+V2.5S

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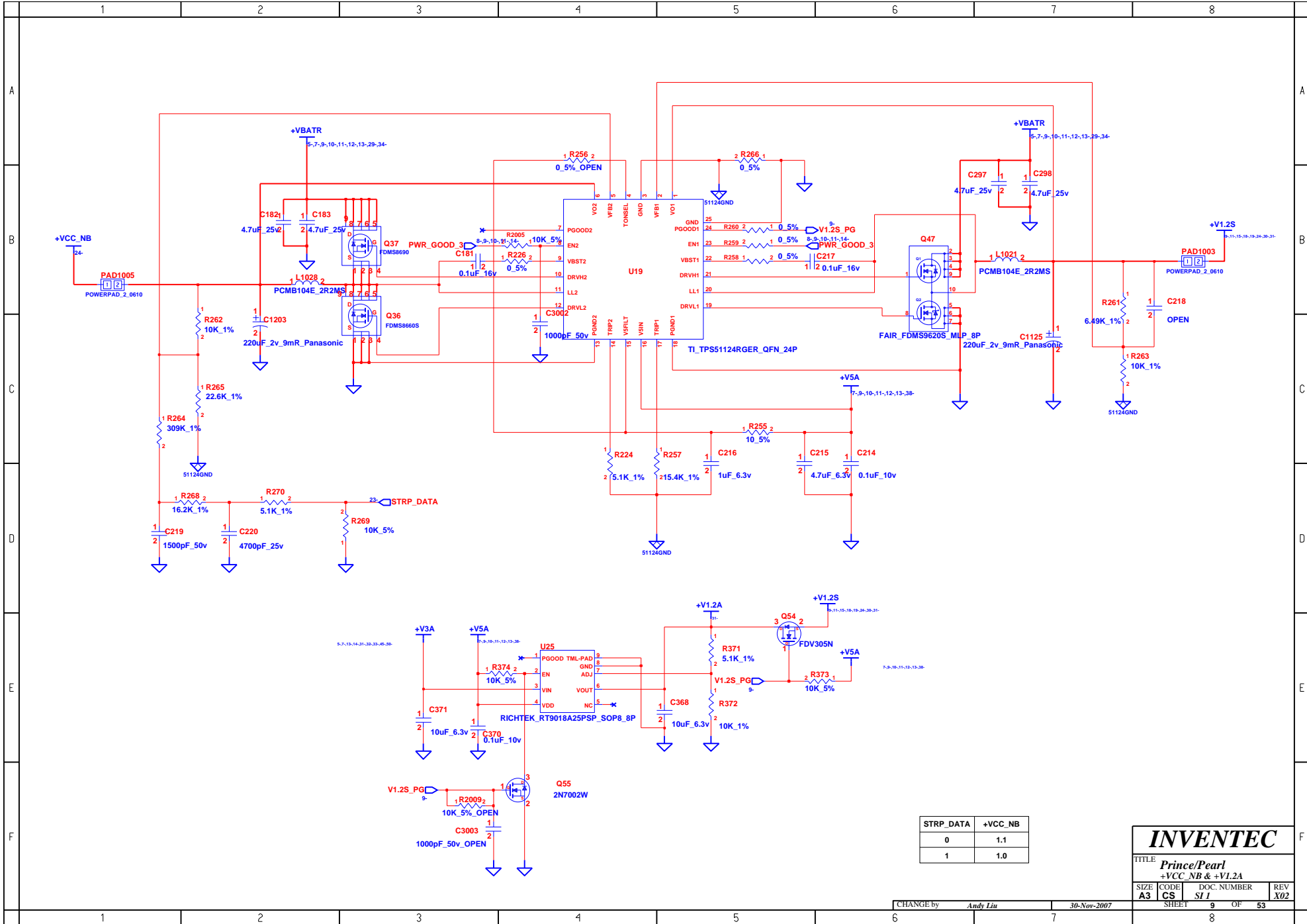
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TITLE
**Prince/Pearl
OCP**

SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
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CHANGE by *Andy Liu* 22-Jan-2008

SHEET 8 OF 53



STRP_DATA	+VCC_NB
0	1.1
1	1.0

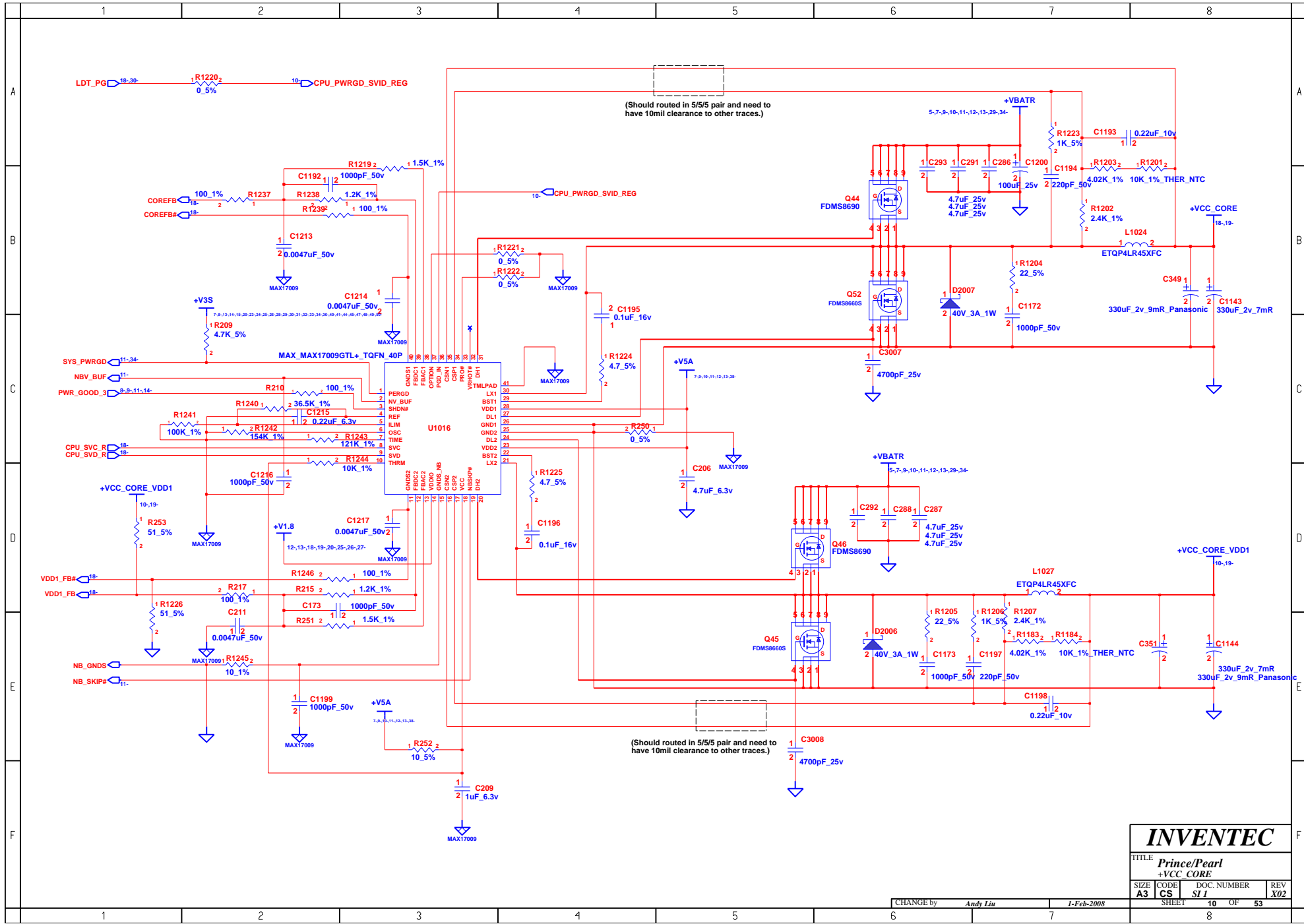
INVENTEC

TITLE
Prince/Pearl
 +VCC_NB & +V1.2A

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by *Andy Liu* 30-Nov-2007

SHEET 9 OF 53



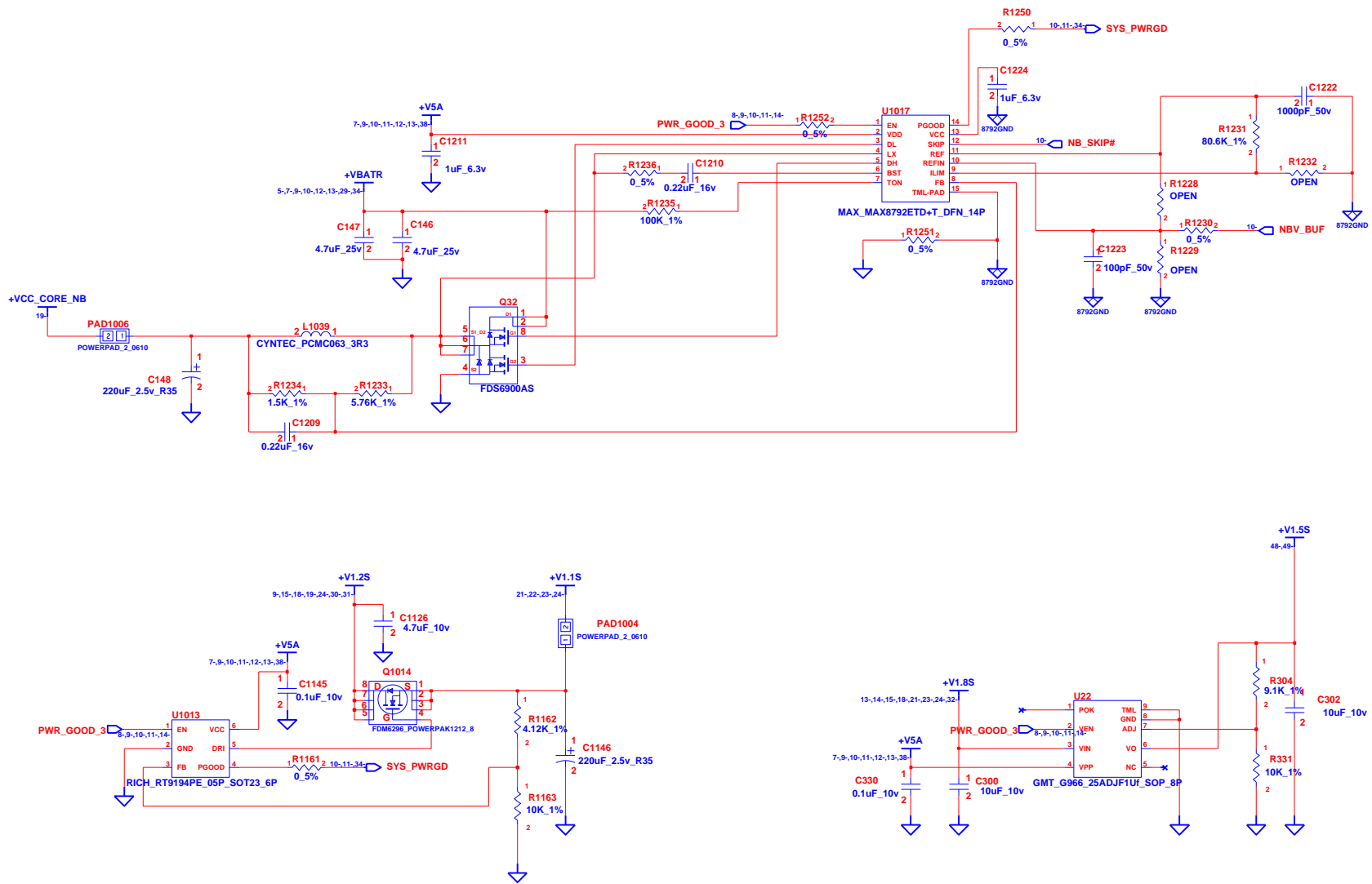
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TITLE
Prince/Pearl
+VCC_CORE

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI1	X02

CHANGE by *Andy Liu* 1-Feb-2008

SHEET 10 OF 53

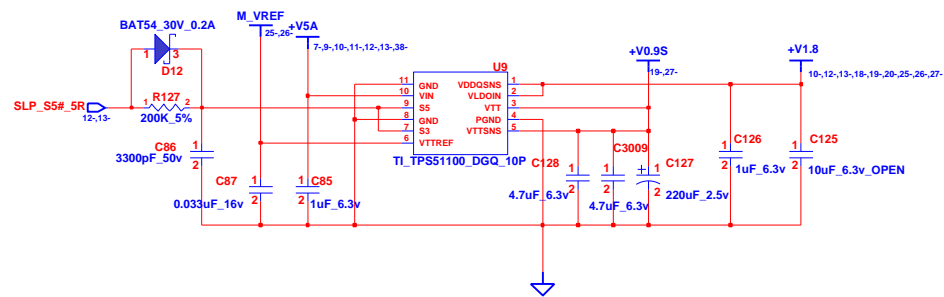
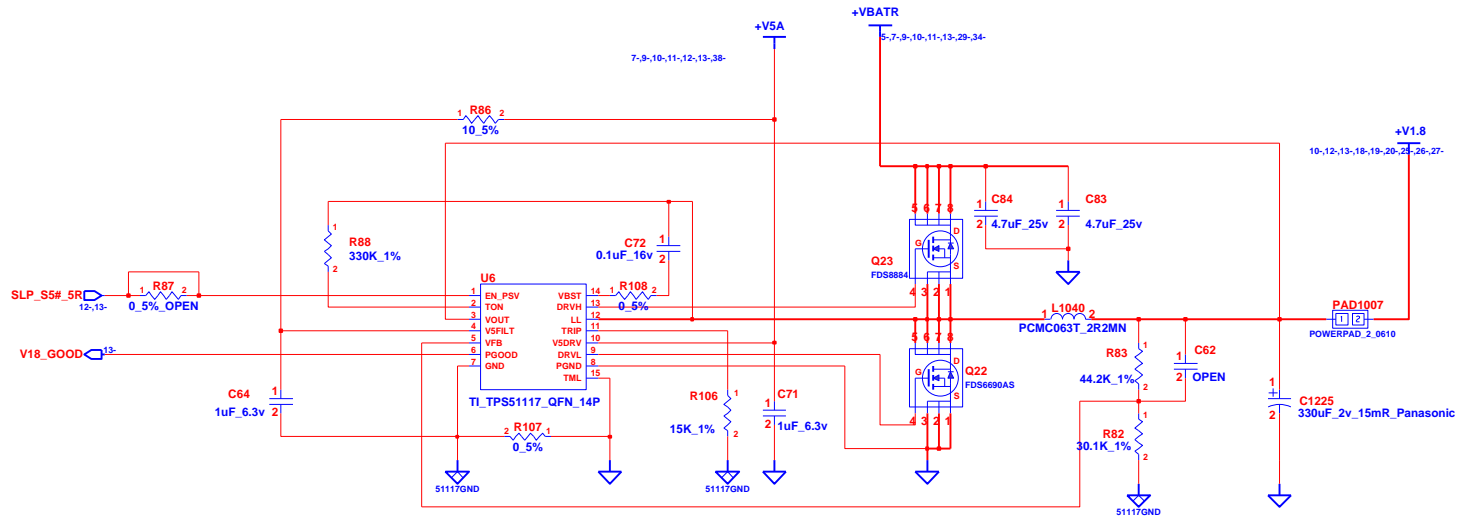


INVENTEC

TITLE
**Prince/Pearl
 POWER**

SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
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CHANGE by *Andy Liu* 22-Nov-2007



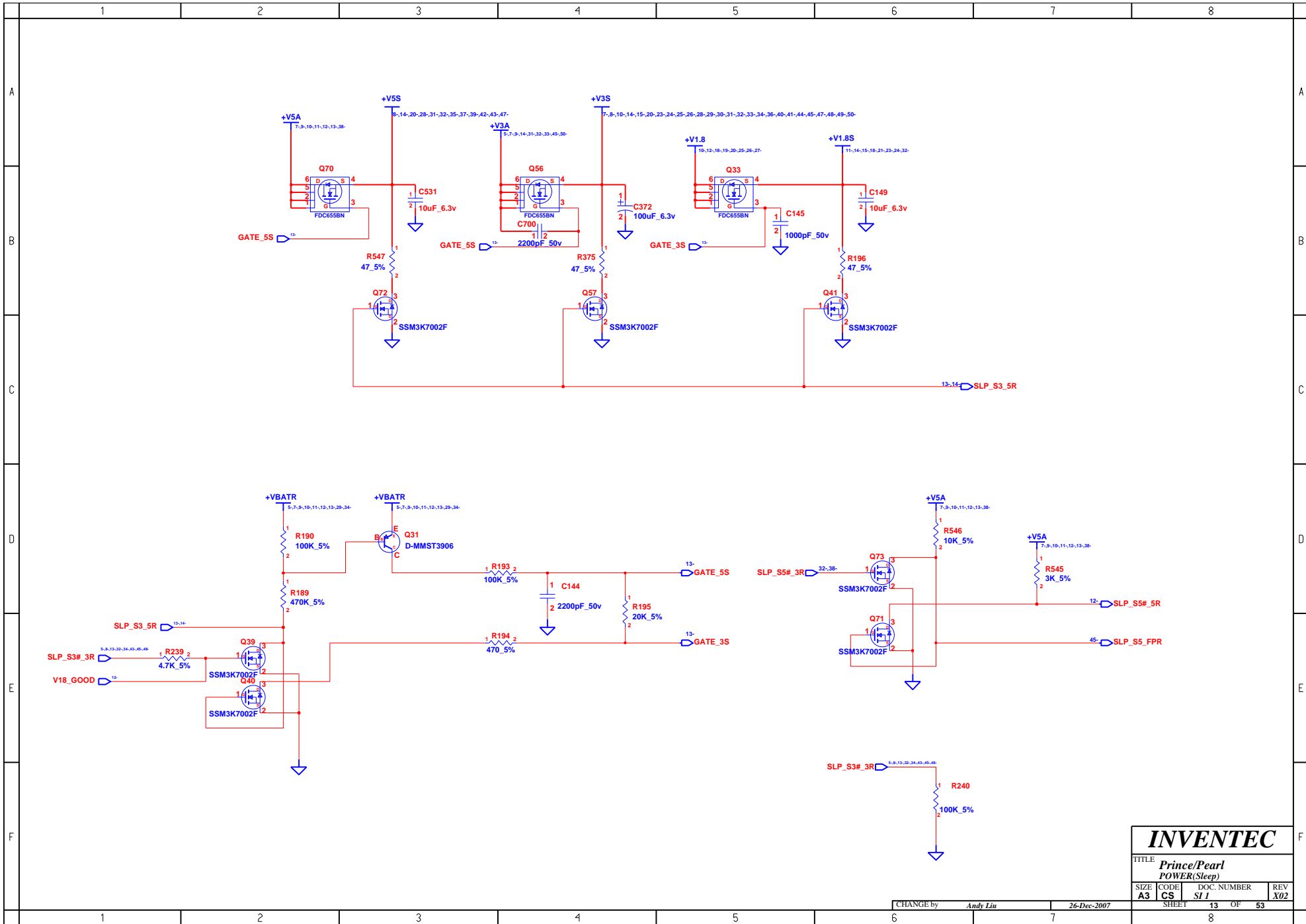
NOTE: DDR2 REGULATOR

INVENTEC

TITLE			
Prince/Pearl			
DDR2 POWER			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by Andy Liu 21-Nov-2007

SHEET 12 OF 53

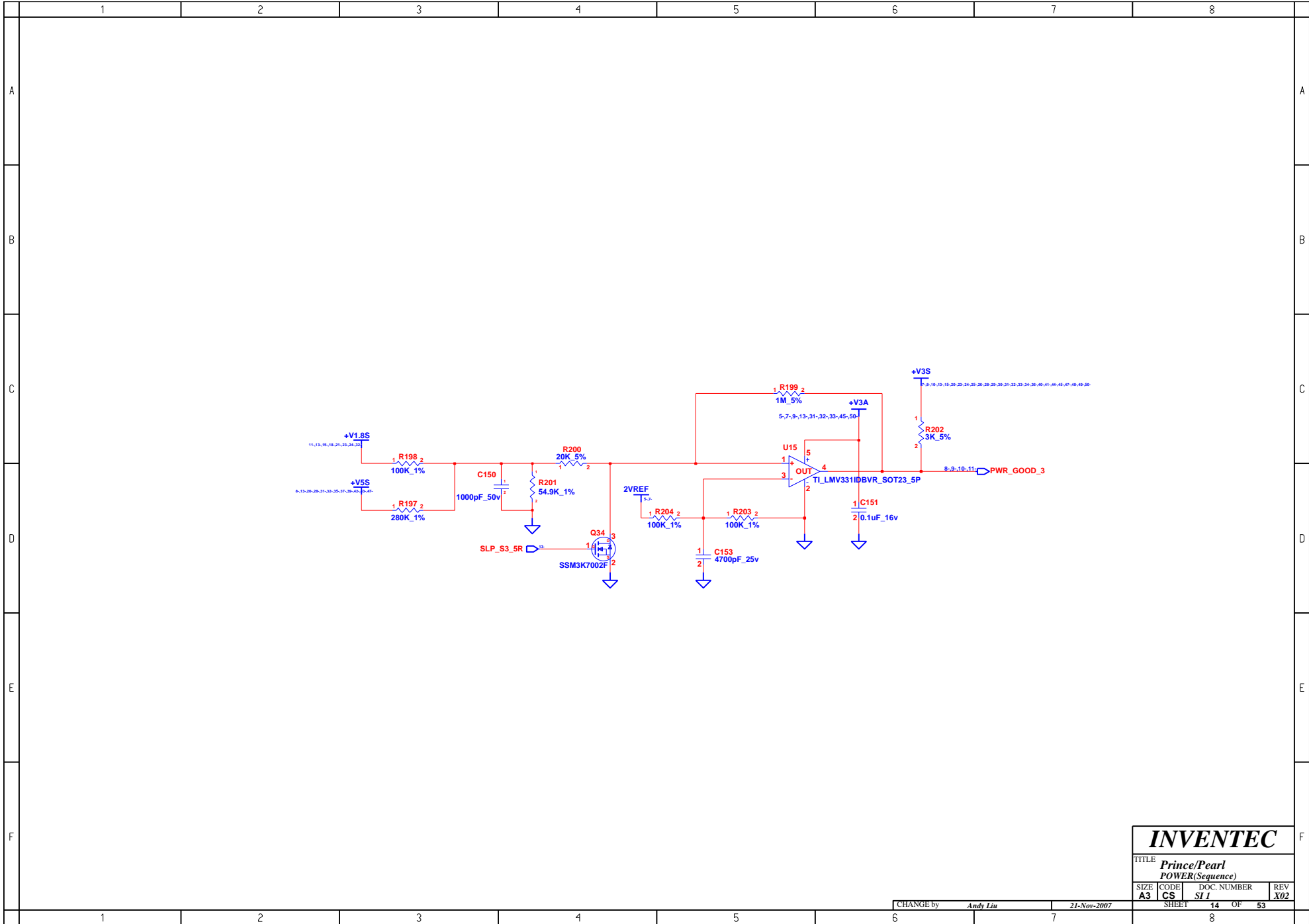


INVENTEC

TITLE
**Prince/Pearl
 POWER(Sleep)**

SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
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CHANGE by *Andy Liu* 26-Dec-2007 SHEET 13 OF 53



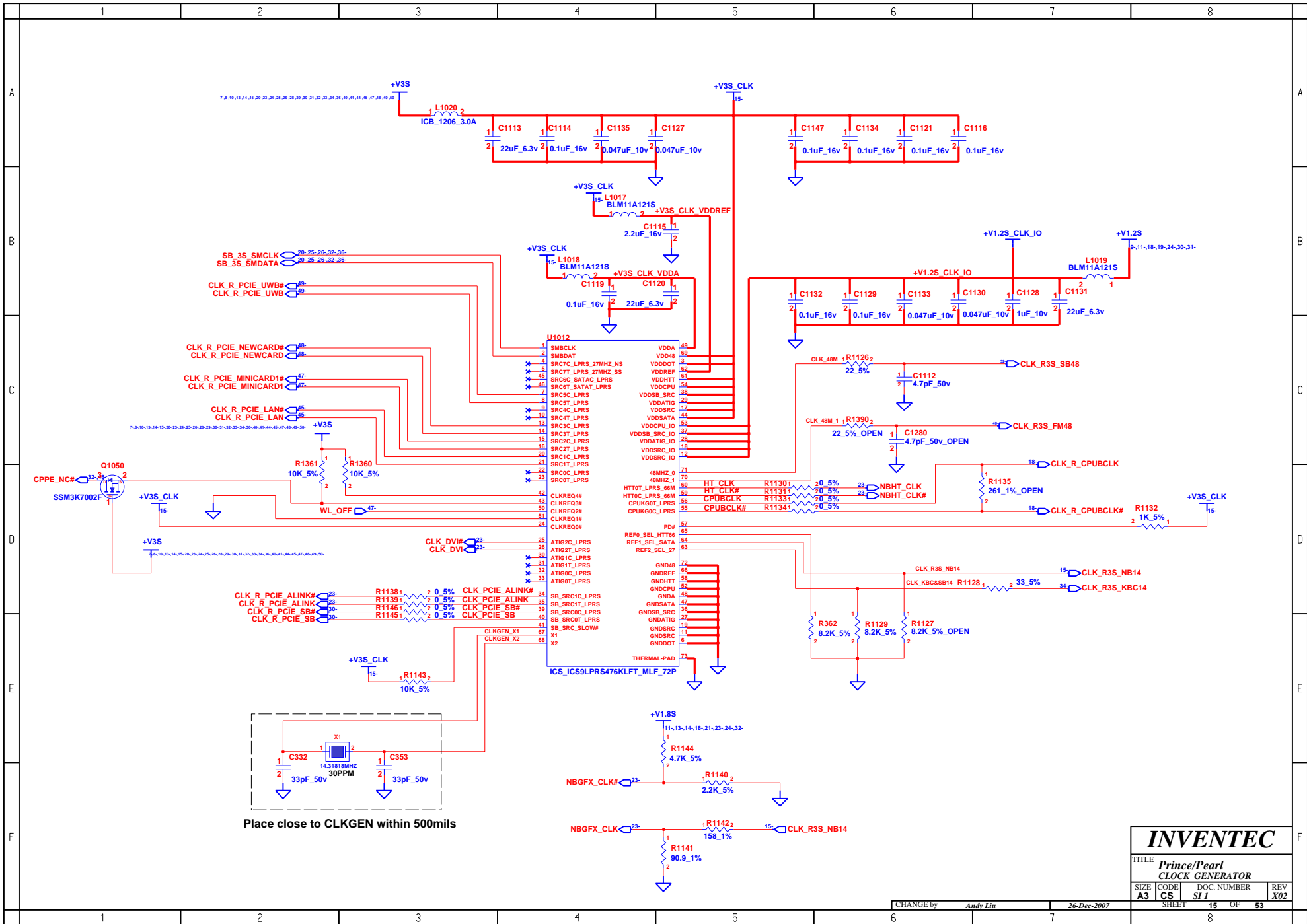
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TITLE
Prince/Pearl
POWER(Sequence)

SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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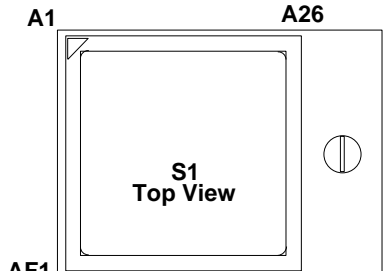
CHANGE by *Andy Liu* 21-Nov-2007

SHEET 14 OF 53

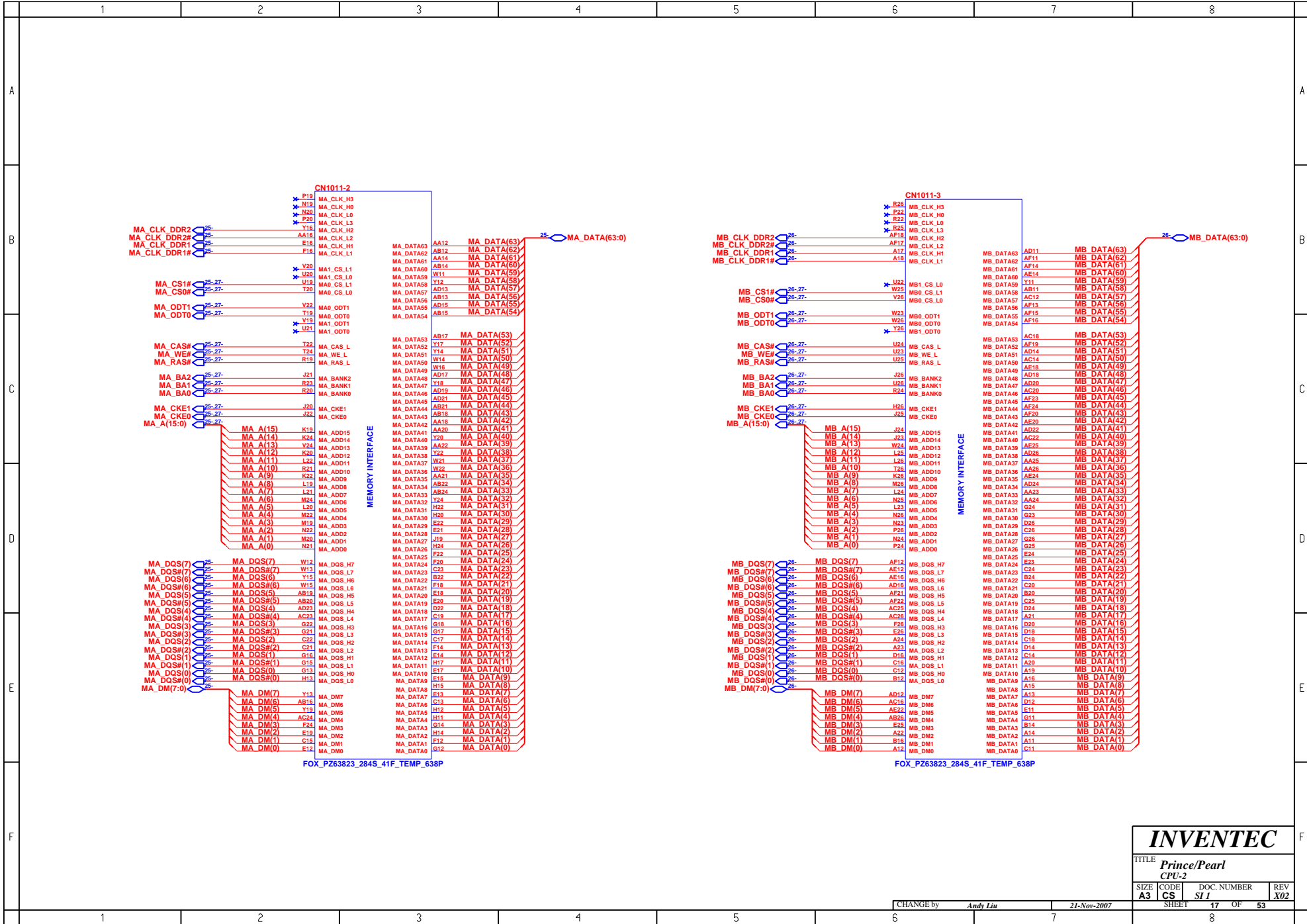


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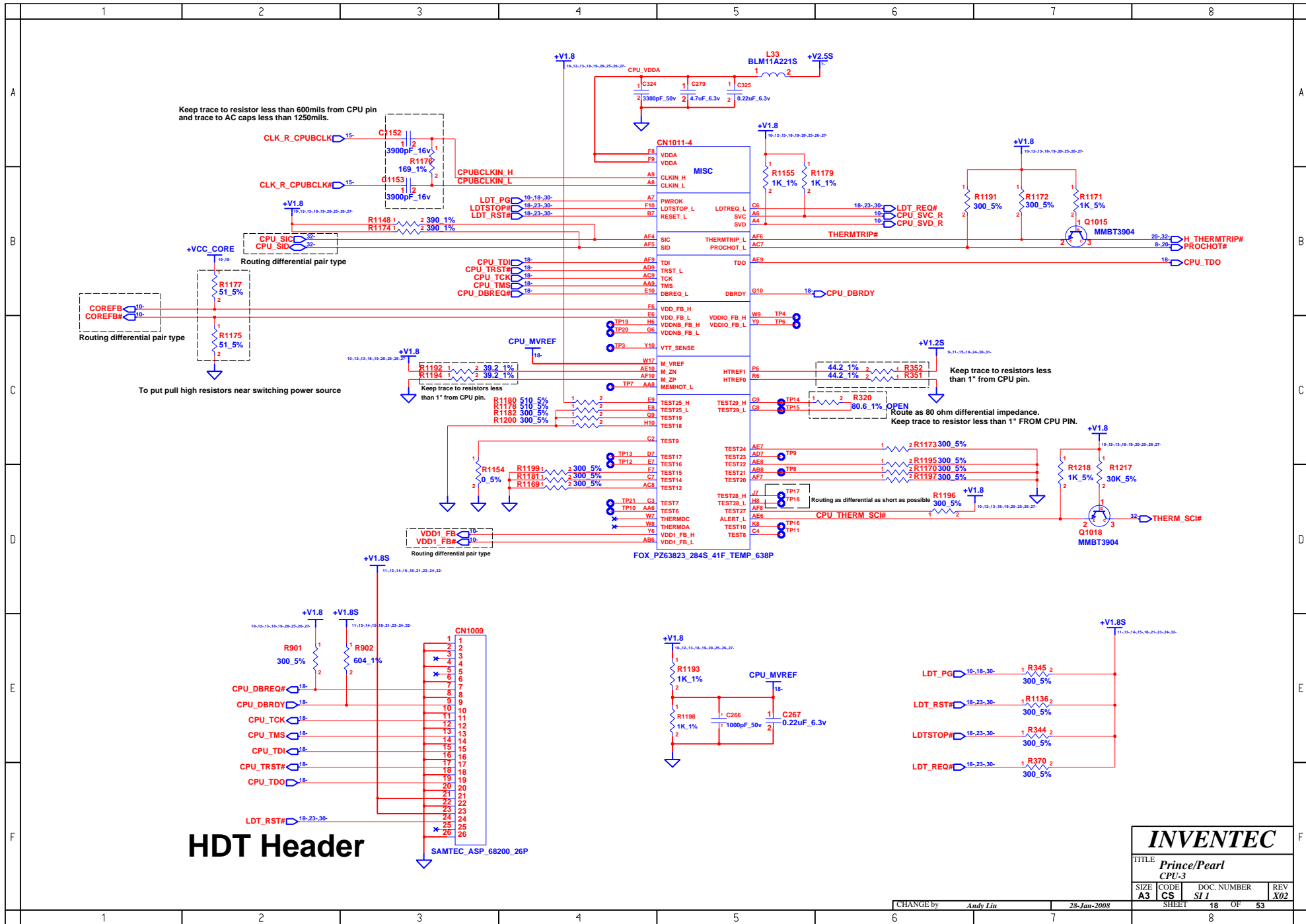
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SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
CHANGE by <i>Andy Liu</i>		26-Dec-2007	
SHEET		15 OF 53	
1		8	

	1	2	3	4	5	6	7	8																										
A	<p style="text-align: center;">CN1011-1</p> <table border="0" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; vertical-align: top;"> L0_CLKIN1 21- J5 L0_CLKIN1# 21- K5 L0_CLKIN0 21- J3 L0_CLKIN0# 21- J2 L0_CTLIN1 21- P3 L0_CTLIN1# 21- P4 L0_CTLIN0 21- N1 L0_CTLIN0# 21- P1 L0_CADIN15 21- N5 L0_CADIN15# 21- P5 L0_CADIN14 21- M3 L0_CADIN14# 21- M4 L0_CADIN13 21- L6 L0_CADIN13# 21- M5 L0_CADIN12 21- K3 L0_CADIN12# 21- K4 L0_CADIN11 21- H3 L0_CADIN11# 21- H4 L0_CADIN10 21- G5 L0_CADIN10# 21- H5 L0_CADIN9 21- F3 L0_CADIN9# 21- F4 L0_CADIN8 21- E5 L0_CADIN8# 21- F5 L0_CADIN7 21- N3 L0_CADIN7# 21- N2 L0_CADIN6 21- L1 L0_CADIN6# 21- M1 L0_CADIN5 21- L3 L0_CADIN5# 21- L2 L0_CADIN4 21- J1 L0_CADIN4# 21- K1 L0_CADIN3 21- G1 L0_CADIN3# 21- H1 L0_CADIN2 21- G3 L0_CADIN2# 21- G2 L0_CADIN1 21- E1 L0_CADIN1# 21- F1 L0_CADIN0 21- E3 L0_CADIN0# 21- E2 </td> <td style="width: 25%; vertical-align: top;"> L0_CLKIN_H1 L0_CLKIN_L1 L0_CLKIN_H0 L0_CLKIN_L0 L0_CTLIN_H1 L0_CTLIN_L1 L0_CTLIN_H0 L0_CTLIN_L0 L0_CADIN_H15 L0_CADIN_L15 L0_CADIN_H14 L0_CADIN_L14 L0_CADIN_H13 L0_CADIN_L13 L0_CADIN_H12 L0_CADIN_L12 L0_CADIN_H11 L0_CADIN_L11 L0_CADIN_H10 L0_CADIN_L10 L0_CADIN_H9 L0_CADIN_L9 L0_CADIN_H8 L0_CADIN_L8 L0_CADIN_H7 L0_CADIN_L7 L0_CADIN_H6 L0_CADIN_L6 L0_CADIN_H5 L0_CADIN_L5 L0_CADIN_H4 L0_CADIN_L4 L0_CADIN_H3 L0_CADIN_L3 L0_CADIN_H2 L0_CADIN_L2 L0_CADIN_H1 L0_CADIN_L1 L0_CADIN_H0 L0_CADIN_L0 </td> <td style="width: 25%; vertical-align: top;"> L0_CLKOUT_H1 L0_CLKOUT_L1 L0_CLKOUT_H0 L0_CLKOUT_L0 L0_CTLOUT_H1 L0_CTLOUT_L1 L0_CTLOUT_H0 L0_CTLOUT_L0 L0_CADOUT_H15 L0_CADOUT_L15 L0_CADOUT_H14 L0_CADOUT_L14 L0_CADOUT_H13 L0_CADOUT_L13 L0_CADOUT_H12 L0_CADOUT_L12 L0_CADOUT_H11 L0_CADOUT_L11 L0_CADOUT_H10 L0_CADOUT_L10 L0_CADOUT_H9 L0_CADOUT_L9 L0_CADOUT_H8 L0_CADOUT_L8 L0_CADOUT_H7 L0_CADOUT_L7 L0_CADOUT_H6 L0_CADOUT_L6 L0_CADOUT_H5 L0_CADOUT_L5 L0_CADOUT_H4 L0_CADOUT_L4 L0_CADOUT_H3 L0_CADOUT_L3 L0_CADOUT_H2 L0_CADOUT_L2 L0_CADOUT_H1 L0_CADOUT_L1 L0_CADOUT_H0 L0_CADOUT_L0 </td> <td style="width: 25%; vertical-align: top;"> Y4 Y3 Y1 W1 T5 R5 R2 R3 T4 T3 V5 V4 V3 V5 W5 AB5 AA5 AB4 AB3 AB5 AC5 AD4 AD3 T1 R1 U2 U3 V1 U1 W2 W3 AA2 AA3 AB1 AA1 AC2 AC3 AD1 AC1 </td> <td style="width: 25%; vertical-align: top;"> 21- L0_CLKOUT1 21- L0_CLKOUT1# 21- L0_CLKOUT0 21- L0_CLKOUT0# 21- L0_CTLOUT1 21- L0_CTLOUT1# 21- L0_CTLOUT0 21- L0_CTLOUT0# 21- L0_CADOUT15 21- L0_CADOUT15# 21- L0_CADOUT14 21- L0_CADOUT14# 21- L0_CADOUT13 21- L0_CADOUT13# 21- L0_CADOUT12 21- L0_CADOUT12# 21- L0_CADOUT11 21- L0_CADOUT11# 21- L0_CADOUT10 21- L0_CADOUT10# 21- L0_CADOUT9 21- L0_CADOUT9# 21- L0_CADOUT8 21- L0_CADOUT8# 21- L0_CADOUT7 21- L0_CADOUT7# 21- L0_CADOUT6 21- L0_CADOUT6# 21- L0_CADOUT5 21- L0_CADOUT5# 21- L0_CADOUT4 21- L0_CADOUT4# 21- L0_CADOUT3 21- L0_CADOUT3# 21- L0_CADOUT2 21- L0_CADOUT2# 21- L0_CADOUT1 21- L0_CADOUT1# 21- L0_CADOUT0 21- L0_CADOUT0# </td> </tr> <tr> <td colspan="5" style="text-align: center; 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L0_CLKIN1 21- J5 L0_CLKIN1# 21- K5 L0_CLKIN0 21- J3 L0_CLKIN0# 21- J2 L0_CTLIN1 21- P3 L0_CTLIN1# 21- P4 L0_CTLIN0 21- N1 L0_CTLIN0# 21- P1 L0_CADIN15 21- N5 L0_CADIN15# 21- P5 L0_CADIN14 21- M3 L0_CADIN14# 21- M4 L0_CADIN13 21- L6 L0_CADIN13# 21- M5 L0_CADIN12 21- K3 L0_CADIN12# 21- K4 L0_CADIN11 21- H3 L0_CADIN11# 21- H4 L0_CADIN10 21- G5 L0_CADIN10# 21- H5 L0_CADIN9 21- F3 L0_CADIN9# 21- F4 L0_CADIN8 21- E5 L0_CADIN8# 21- F5 L0_CADIN7 21- N3 L0_CADIN7# 21- N2 L0_CADIN6 21- L1 L0_CADIN6# 21- M1 L0_CADIN5 21- L3 L0_CADIN5# 21- L2 L0_CADIN4 21- J1 L0_CADIN4# 21- K1 L0_CADIN3 21- G1 L0_CADIN3# 21- H1 L0_CADIN2 21- G3 L0_CADIN2# 21- G2 L0_CADIN1 21- E1 L0_CADIN1# 21- F1 L0_CADIN0 21- E3 L0_CADIN0# 21- E2										L0_CLKIN_H1 L0_CLKIN_L1 L0_CLKIN_H0 L0_CLKIN_L0 L0_CTLIN_H1 L0_CTLIN_L1 L0_CTLIN_H0 L0_CTLIN_L0 L0_CADIN_H15 L0_CADIN_L15 L0_CADIN_H14 L0_CADIN_L14 L0_CADIN_H13 L0_CADIN_L13 L0_CADIN_H12 L0_CADIN_L12 L0_CADIN_H11 L0_CADIN_L11 L0_CADIN_H10 L0_CADIN_L10 L0_CADIN_H9 L0_CADIN_L9 L0_CADIN_H8 L0_CADIN_L8 L0_CADIN_H7 L0_CADIN_L7 L0_CADIN_H6 L0_CADIN_L6 L0_CADIN_H5 L0_CADIN_L5 L0_CADIN_H4 L0_CADIN_L4 L0_CADIN_H3 L0_CADIN_L3 L0_CADIN_H2 L0_CADIN_L2 L0_CADIN_H1 L0_CADIN_L1 L0_CADIN_H0 L0_CADIN_L0	L0_CLKOUT_H1 L0_CLKOUT_L1 L0_CLKOUT_H0 L0_CLKOUT_L0 L0_CTLOUT_H1 L0_CTLOUT_L1 L0_CTLOUT_H0 L0_CTLOUT_L0 L0_CADOUT_H15 L0_CADOUT_L15 L0_CADOUT_H14 L0_CADOUT_L14 L0_CADOUT_H13 L0_CADOUT_L13 L0_CADOUT_H12 L0_CADOUT_L12 L0_CADOUT_H11 L0_CADOUT_L11 L0_CADOUT_H10 L0_CADOUT_L10 L0_CADOUT_H9 L0_CADOUT_L9 L0_CADOUT_H8 L0_CADOUT_L8 L0_CADOUT_H7 L0_CADOUT_L7 L0_CADOUT_H6 L0_CADOUT_L6 L0_CADOUT_H5 L0_CADOUT_L5 L0_CADOUT_H4 L0_CADOUT_L4 L0_CADOUT_H3 L0_CADOUT_L3 L0_CADOUT_H2 L0_CADOUT_L2 L0_CADOUT_H1 L0_CADOUT_L1 L0_CADOUT_H0 L0_CADOUT_L0	Y4 Y3 Y1 W1 T5 R5 R2 R3 T4 T3 V5 V4 V3 V5 W5 AB5 AA5 AB4 AB3 AB5 AC5 AD4 AD3 T1 R1 U2 U3 V1 U1 W2 W3 AA2 AA3 AB1 AA1 AC2 AC3 AD1 AC1	21- L0_CLKOUT1 21- L0_CLKOUT1# 21- L0_CLKOUT0 21- L0_CLKOUT0# 21- L0_CTLOUT1 21- L0_CTLOUT1# 21- L0_CTLOUT0 21- L0_CTLOUT0# 21- L0_CADOUT15 21- L0_CADOUT15# 21- L0_CADOUT14 21- L0_CADOUT14# 21- L0_CADOUT13 21- L0_CADOUT13# 21- L0_CADOUT12 21- L0_CADOUT12# 21- L0_CADOUT11 21- L0_CADOUT11# 21- L0_CADOUT10 21- L0_CADOUT10# 21- L0_CADOUT9 21- L0_CADOUT9# 21- L0_CADOUT8 21- L0_CADOUT8# 21- L0_CADOUT7 21- L0_CADOUT7# 21- L0_CADOUT6 21- L0_CADOUT6# 21- L0_CADOUT5 21- L0_CADOUT5# 21- L0_CADOUT4 21- L0_CADOUT4# 21- L0_CADOUT3 21- L0_CADOUT3# 21- L0_CADOUT2 21- L0_CADOUT2# 21- L0_CADOUT1 21- L0_CADOUT1# 21- L0_CADOUT0 21- L0_CADOUT0#																					
HYPERTRANSPORT																																		
FOX_PZ63823_284S_41F_TEMP_638P																																		
B																																		
C																																		
D																																		
E	<div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 20%;"> <p>A1</p>  <p>AF1</p> </div> <div style="width: 60%; text-align: center;"> <p>Layout: Add stitching caps if crossing plane split.</p> </div> </div>																																	
F																																		
	1	2	3	4	5	6	7	8																										

INVENTEC			
TITLE <i>Prince/Pearl</i> CPU-1			
SIZE A3	CODE CS	DOC. NUMBER <i>SI 1</i>	REV X02
CHANGE by <i>Andy Liu</i>		21-Nov-2007	
SHEET		16	OF 53



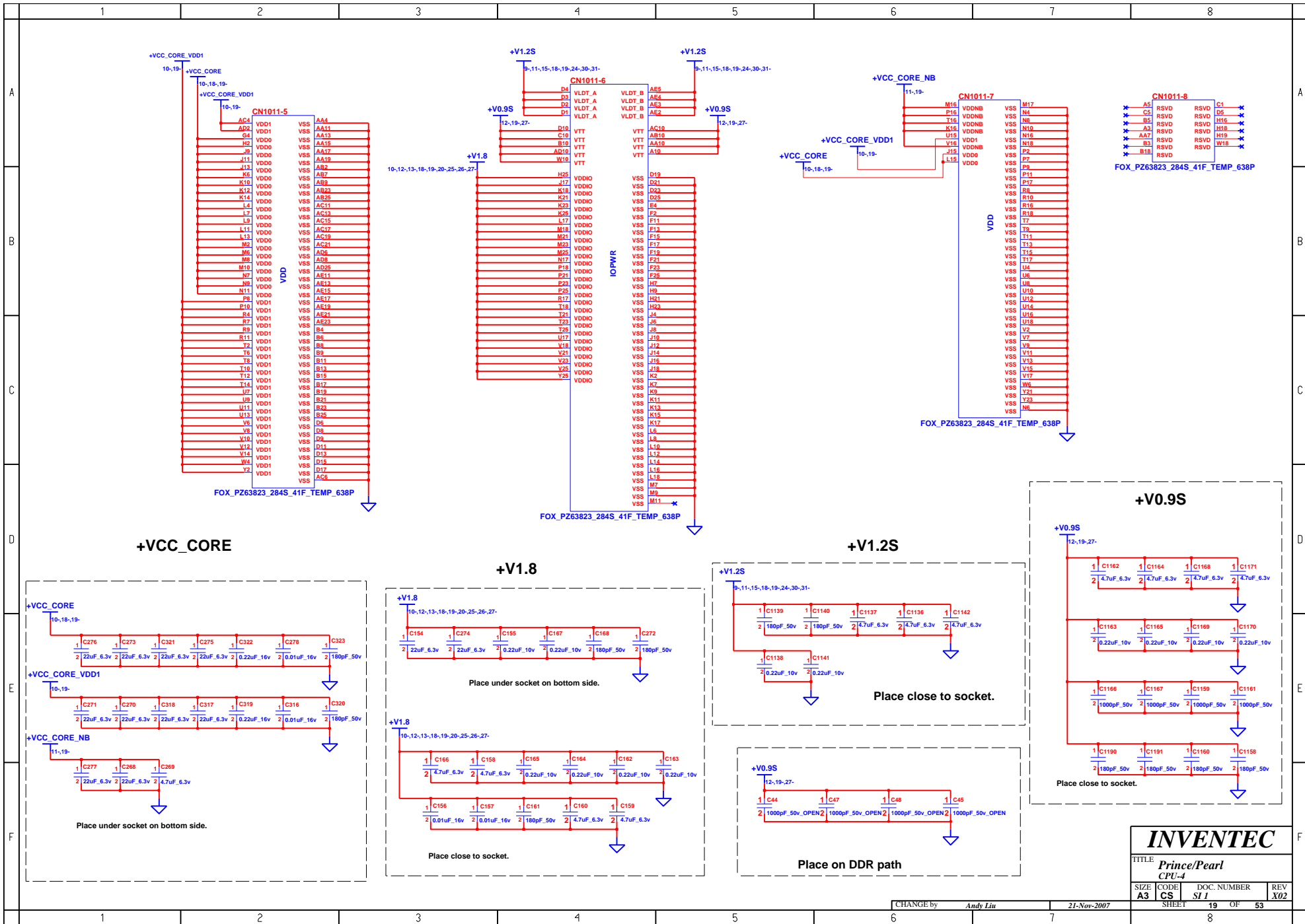
INVENTEC			
TITLE Prince/Pearl CPU-2			
SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
CHANGE by <i>Andy Liu</i>		21-Nov-2007	
SHEET		17	OF 53



HDT Header

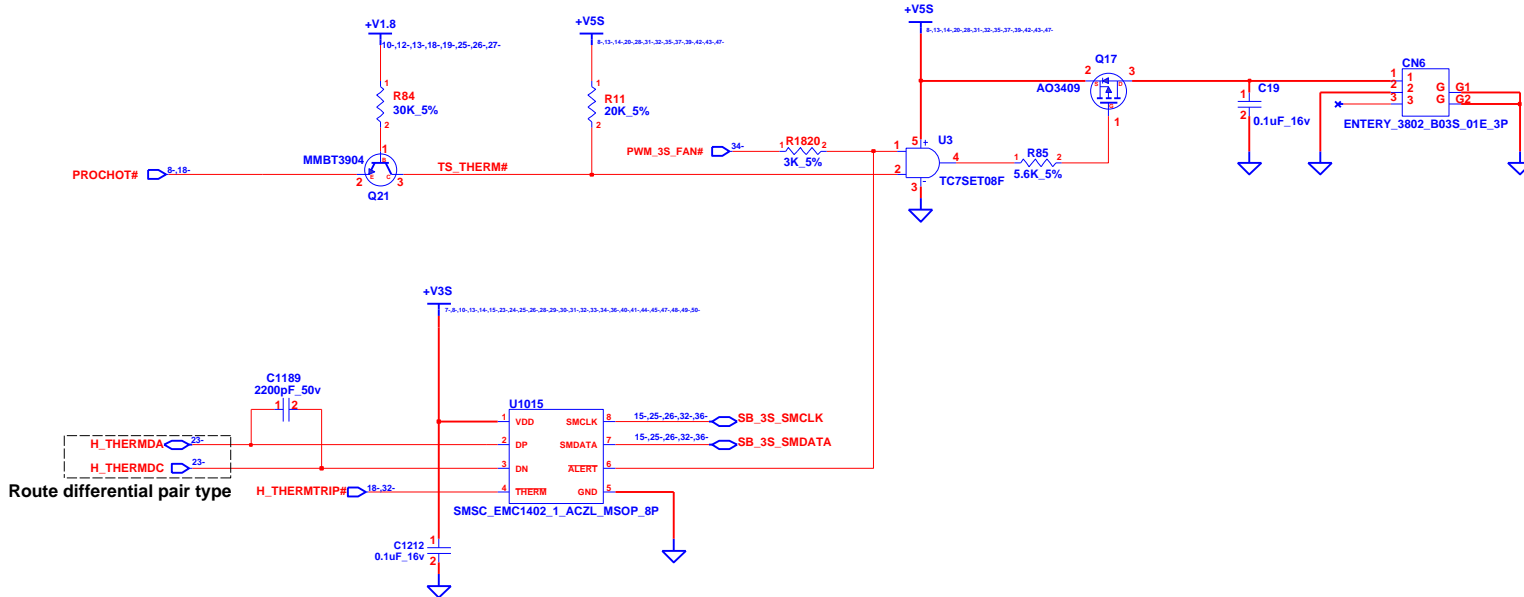
SAMTEC ASP_68200_26P

INVENTEC			
TITLE <i>Prince/Pearl</i> CPU-3			
SIZE A3	CODE CS	DOC. NUMBER <i>SI 1</i>	REV X02
CHANGE by <i>Andy Liu</i>		28-Jan-2008	
SHEET 18		OF 53	



INVENTEC			
TITLE: Prince/Pearl CPU-4			
SIZE: A3	CODE: CS	DOC. NUMBER: ST 1	REV: X02
SHEET: 19		OF: 53	

CHANGE by Andy Liu 21-Nov-2007



Route differential pair type

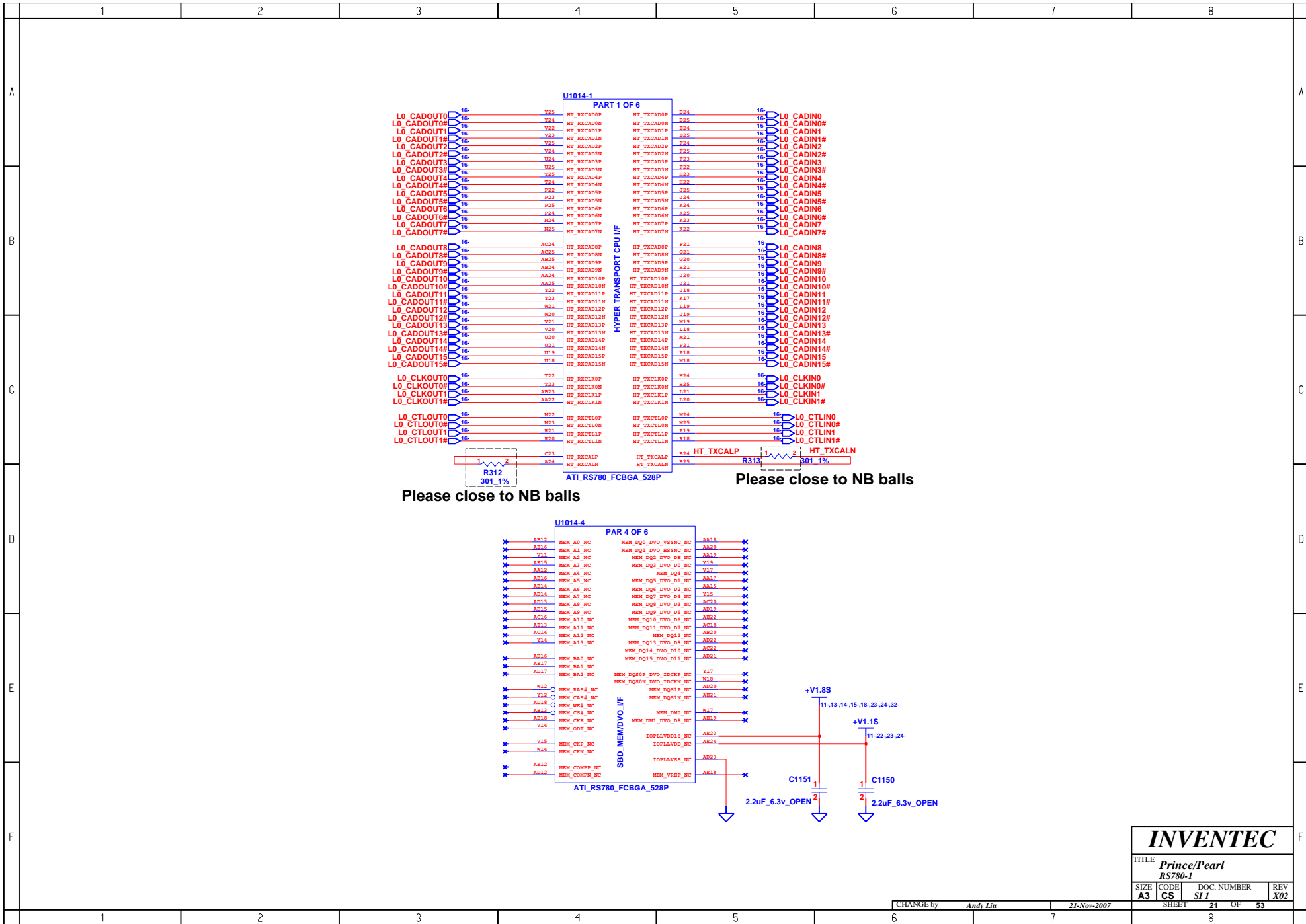
LAYOUT Note: Put the thermal sensor close to CPU.

INVENTEC

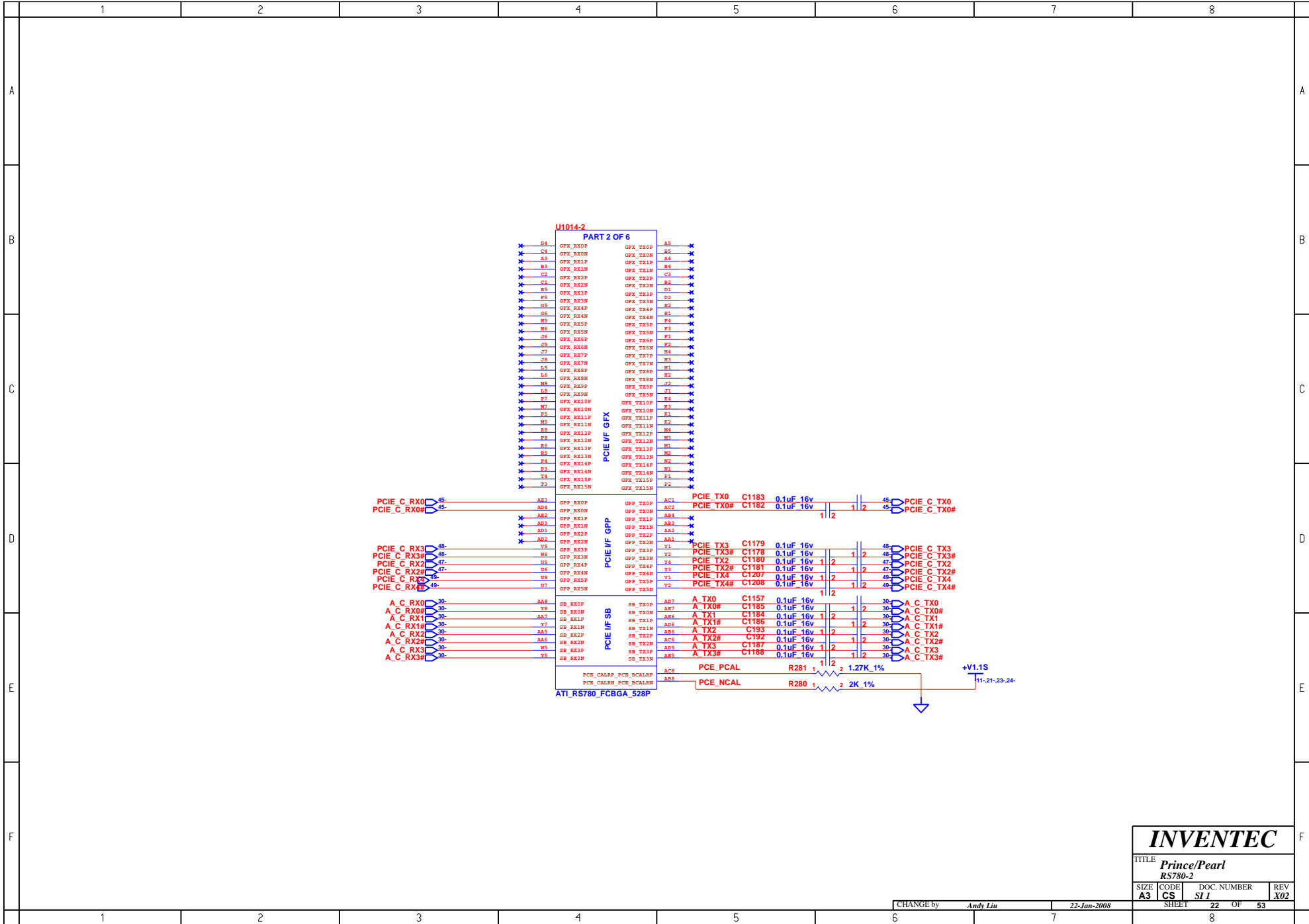
TITLE			
Prince/Pearl			
THERMAL & FAN CONTROLLER			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by Andy Liu 26-Nov-2007

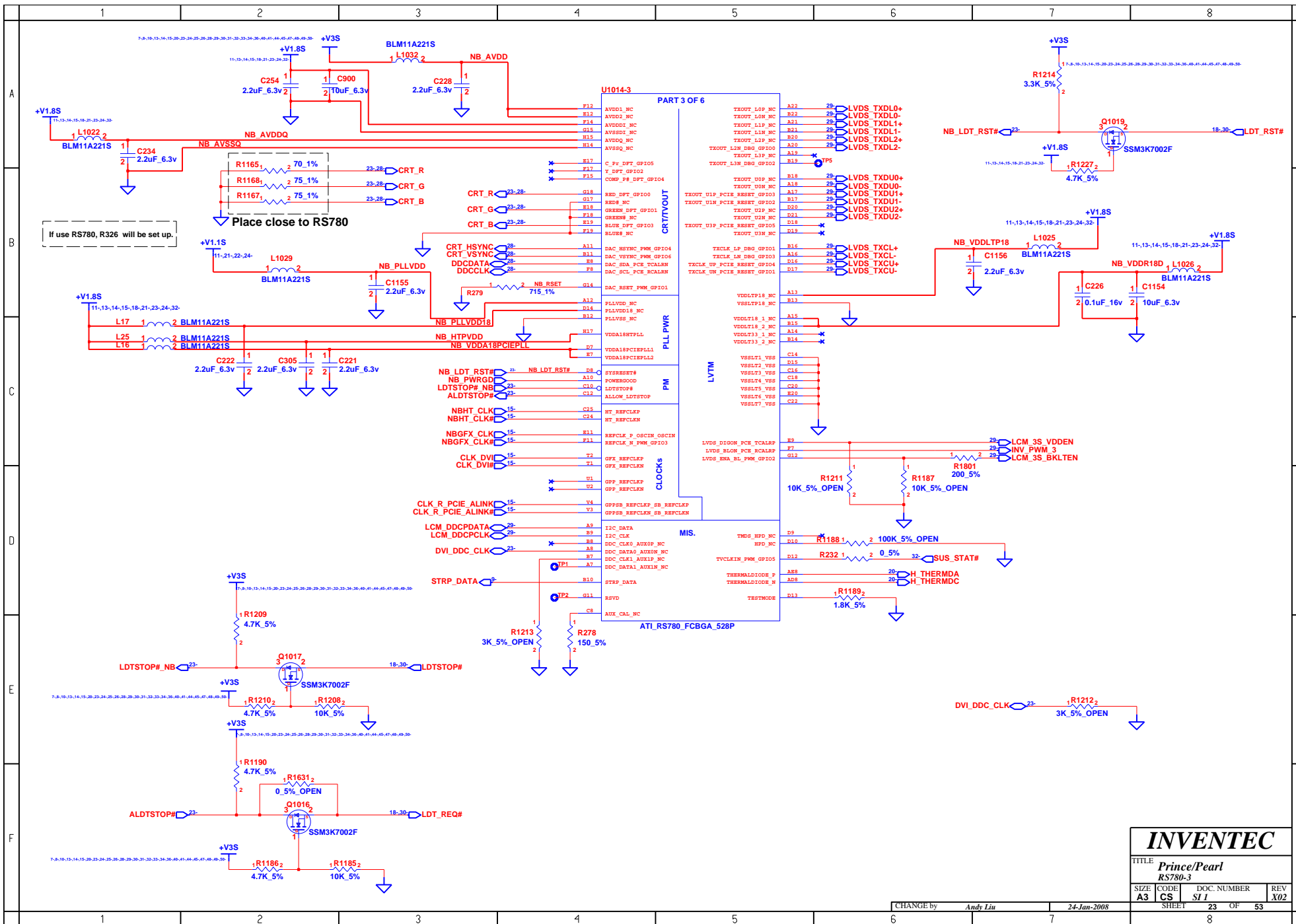
SHEET 20 OF 53



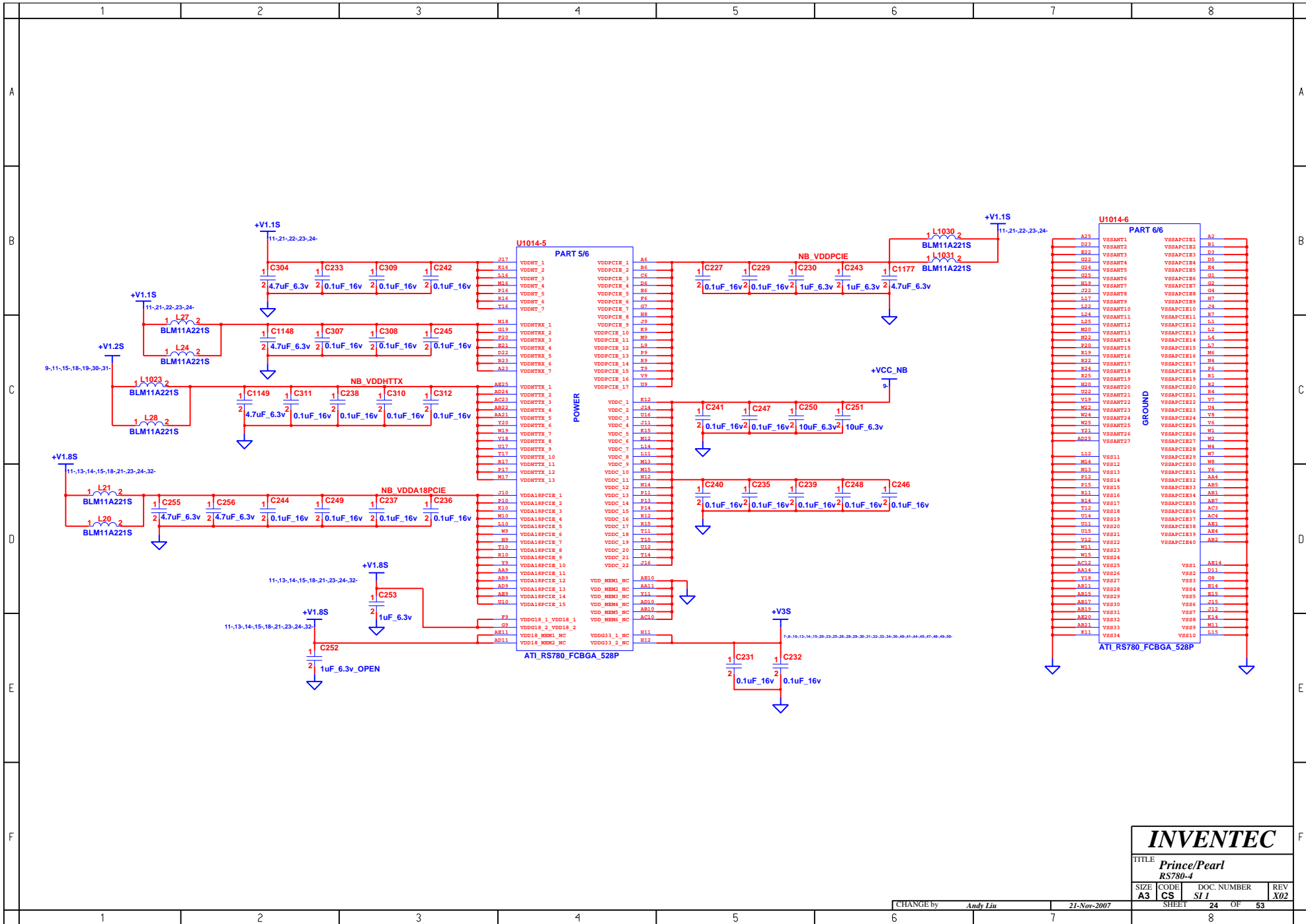
INVENTEC			
TITLE <i>Prince/Pearl</i> RS780-1			
SIZE A3	CODE CS	DOC. NUMBER <i>SI 1</i>	REV X02
CHANGE by <i>Andy Liu</i>		21-Nov-2007	
SHEET		21 OF 53	



INVENTEC			
TITLE Prince/Pearl RS780-2			
SIZE A3	CODE CS	DOC. NUMBER ST 1	REV X02
CHANGE by Andy Liu		22-Jan-2008	SHEET 22 OF 53



INVENTEC			
TITLE Prince/Pearl			
RS780-3			
SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
CHANGE by <i>Andy Liu</i>		24-Jan-2008	
SHEET 23		OF 53	



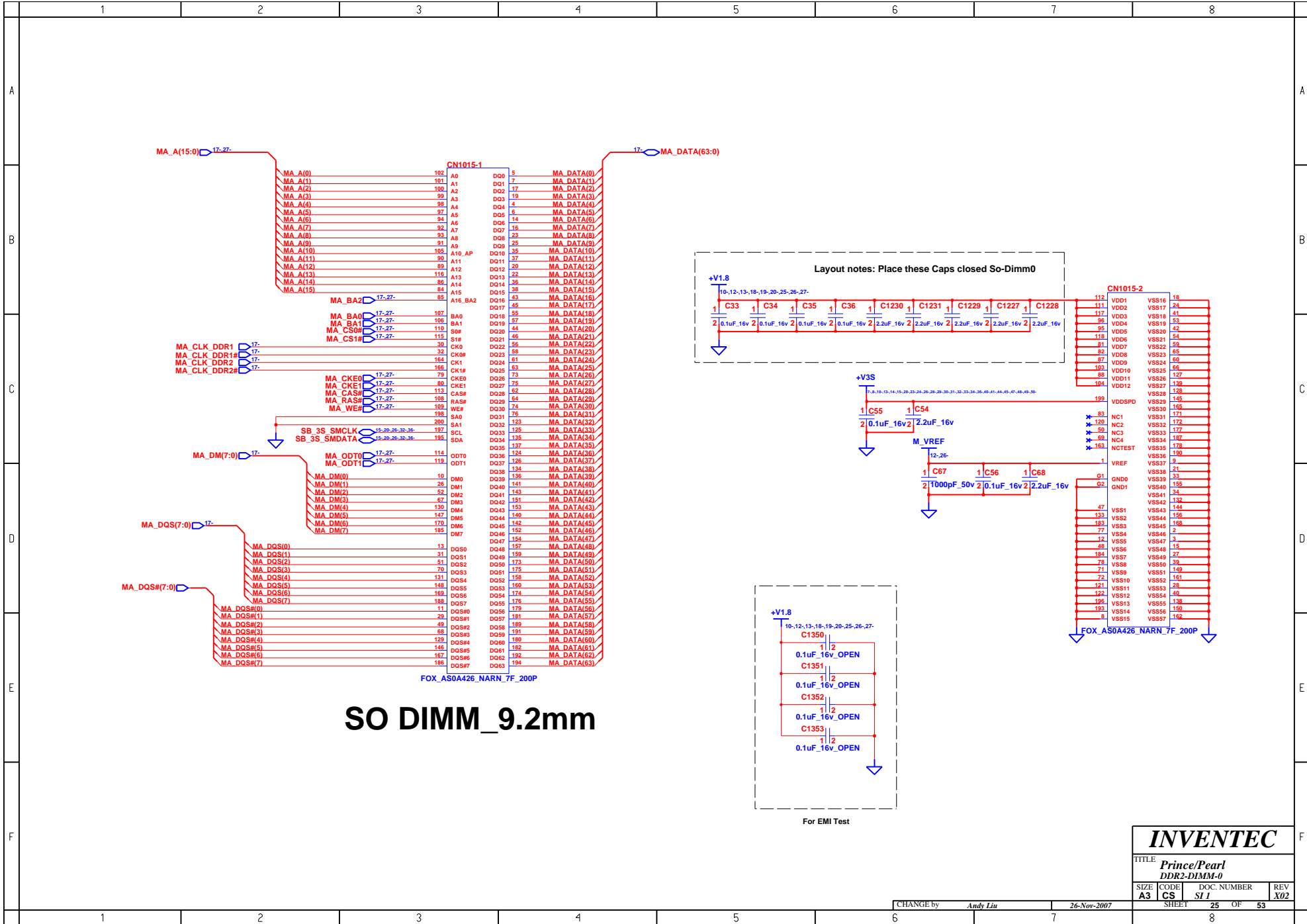
INVENTEC

TITLE
Prince/Pearl
RS780-4

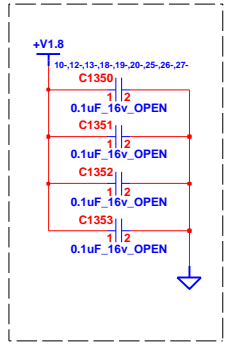
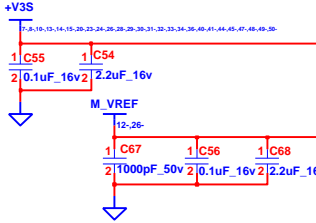
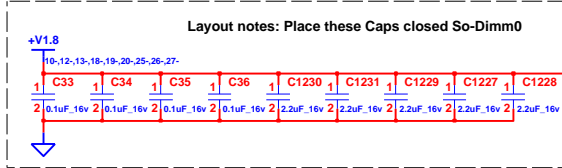
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by *Andy Liu* 21-Nov-2007

SHEET 24 OF 53

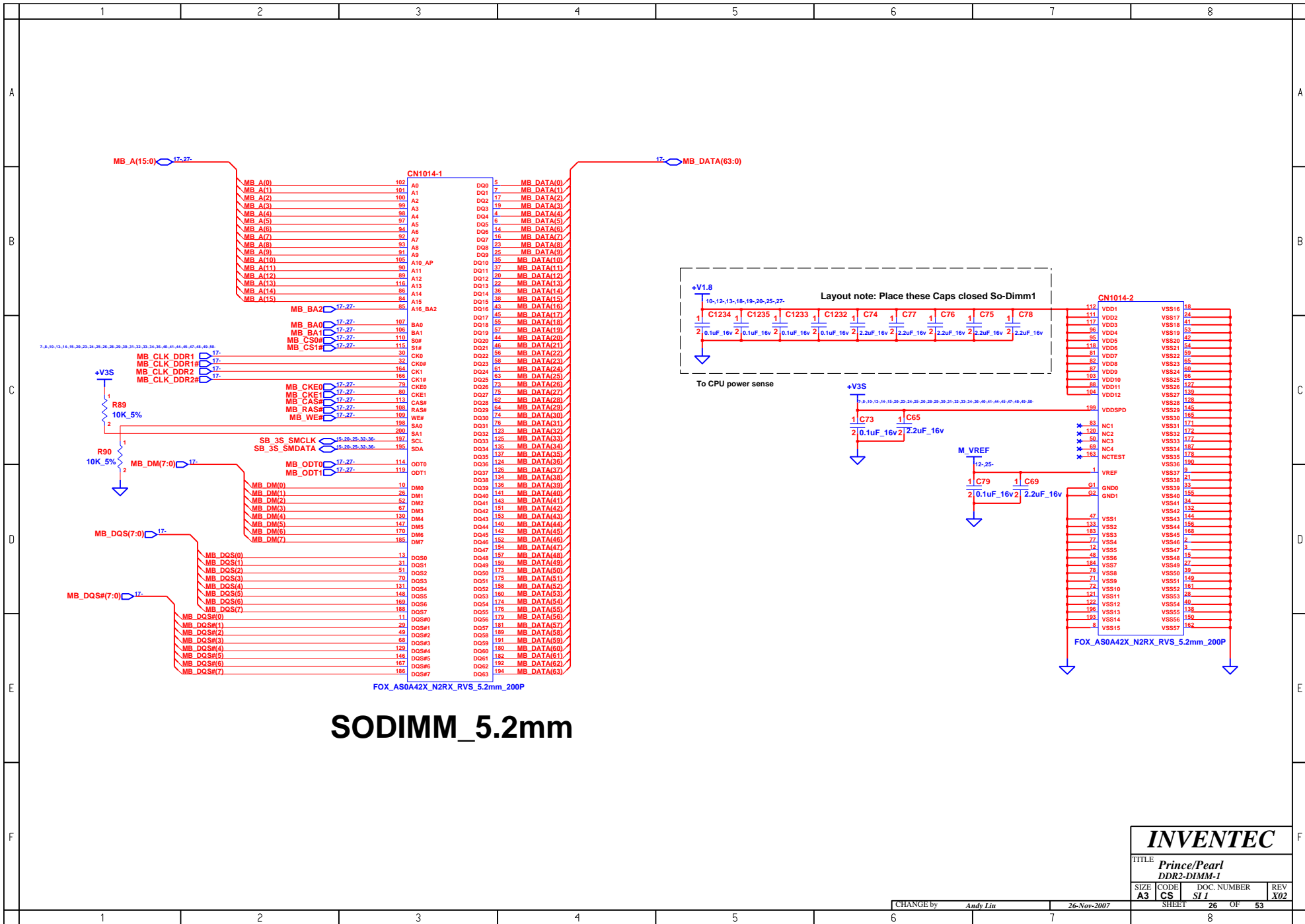


Pin	Signal	Pin	Signal
102	MA_A(0)	5	MA_DATA(0)
101	MA_A(1)	7	MA_DATA(1)
100	MA_A(2)	17	MA_DATA(2)
99	MA_A(3)	19	MA_DATA(3)
98	MA_A(4)	4	MA_DATA(4)
97	MA_A(5)	16	MA_DATA(5)
94	MA_A(6)	14	MA_DATA(6)
92	MA_A(7)	16	MA_DATA(7)
93	MA_A(8)	23	MA_DATA(8)
91	MA_A(9)	25	MA_DATA(9)
105	MA_A(10)	35	MA_DATA(10)
90	MA_A(11)	37	MA_DATA(11)
89	MA_A(12)	20	MA_DATA(12)
118	MA_A(13)	22	MA_DATA(13)
96	MA_A(14)	14	MA_DATA(14)
84	MA_A(15)	38	MA_DATA(15)
85	A16, BA2	43	MA_DATA(16)
107	MA_BA0	45	MA_DATA(17)
106	MA_BA1	55	MA_DATA(18)
110	MA_CS0#	87	MA_DATA(19)
115	MA_CS1#	20	MA_DATA(20)
30	CK0	46	MA_DATA(21)
32	CK0#	56	MA_DATA(22)
164	CK1	58	MA_DATA(23)
166	CK1#	63	MA_DATA(24)
79	CKE0	63	MA_DATA(25)
80	CKE1	75	MA_DATA(27)
113	CAS#	82	MA_DATA(28)
108	RAS#	84	MA_DATA(29)
109	WE#	74	MA_DATA(30)
200	SA0	76	MA_DATA(31)
197	SCL	129	MA_DATA(32)
195	SDA	125	MA_DATA(33)
114	MA_ODT0	137	MA_DATA(35)
118	MA_ODT1	124	MA_DATA(36)
119	ODT1	126	MA_DATA(37)
10	DM0	134	MA_DATA(38)
25	DM1	136	MA_DATA(39)
52	DM2	141	MA_DATA(40)
67	DM3	143	MA_DATA(41)
130	DM4	151	MA_DATA(42)
147	DM5	153	MA_DATA(43)
148	DM6	140	MA_DATA(44)
169	DM7	142	MA_DATA(45)
185	DM7	152	MA_DATA(46)
33	DQS0	154	MA_DATA(47)
31	DQS1	157	MA_DATA(48)
51	DQS2	159	MA_DATA(49)
70	DQS3	173	MA_DATA(50)
131	DQS4	175	MA_DATA(51)
148	DQS5	198	MA_DATA(52)
169	DQS6	190	MA_DATA(53)
188	DQS7	174	MA_DATA(54)
11	DQS#(0)	176	MA_DATA(55)
29	DQS#(1)	179	MA_DATA(56)
49	DQS#(2)	181	MA_DATA(57)
68	DQS#(3)	189	MA_DATA(58)
129	DQS#(4)	191	MA_DATA(59)
146	DQS#(5)	180	MA_DATA(60)
167	DQS#(6)	182	MA_DATA(61)
185	DQS#(7)	192	MA_DATA(62)
		194	MA_DATA(63)

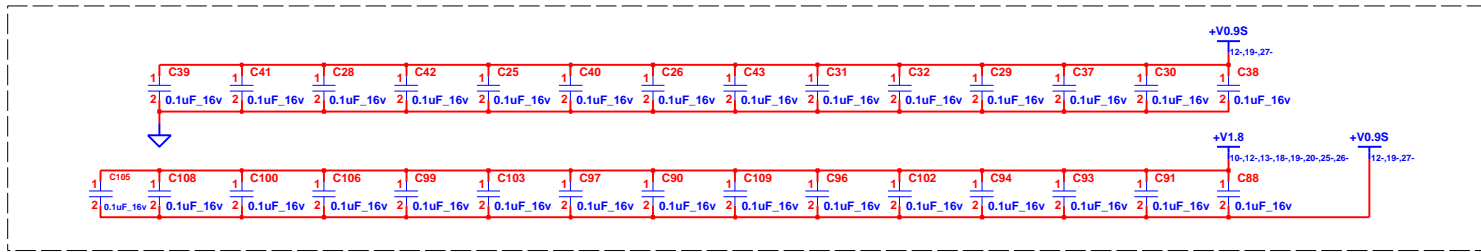


Pin	Signal	Pin	Signal
112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
116	VDD6	VSS21	54
81	VDD7	VSS22	69
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	127
88	VDD11	VSS26	127
104	VDD12	VSS27	138
199	VDDSPD	VSS28	145
199	VDDSPD	VSS29	155
83	NC1	VSS30	171
120	NC2	VSS32	172
50	NC3	VSS33	172
58	NC4	VSS34	187
153	NCTEST	VSS35	178
1	VREF	VSS36	190
91	GNDD	VSS37	9
92	GNDD	VSS38	21
92	GNDD	VSS39	33
92	GNDD	VSS40	155
92	GNDD	VSS41	34
47	VSS1	VSS42	132
133	VSS2	VSS43	144
183	VSS3	VSS44	168
77	VSS4	VSS45	168
12	VSS5	VSS46	2
48	VSS6	VSS47	15
184	VSS7	VSS48	27
78	VSS8	VSS49	27
71	VSS9	VSS50	38
72	VSS10	VSS51	39
121	VSS11	VSS52	28
122	VSS12	VSS53	40
196	VSS13	VSS54	138
193	VSS14	VSS55	150
8	VSS15	VSS56	162
8	VSS15	VSS57	162

FOX_AS0A426_NARN_7F_200P

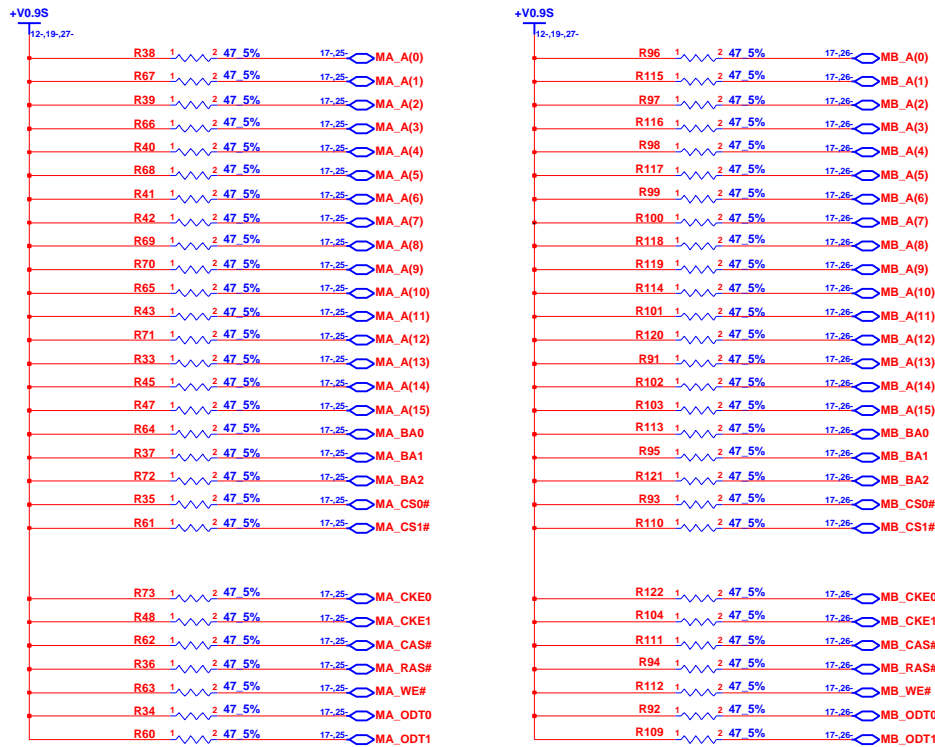


INVENTEC			
TITLE Prince/Pearl DDR2-DIMM-1			
SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
CHANGE by <i>Andy Liu</i>		26-Nov-2007	
SHEET		26 OF 53	
1		8	



To CPU power sense

Place CAPs close to DIMM

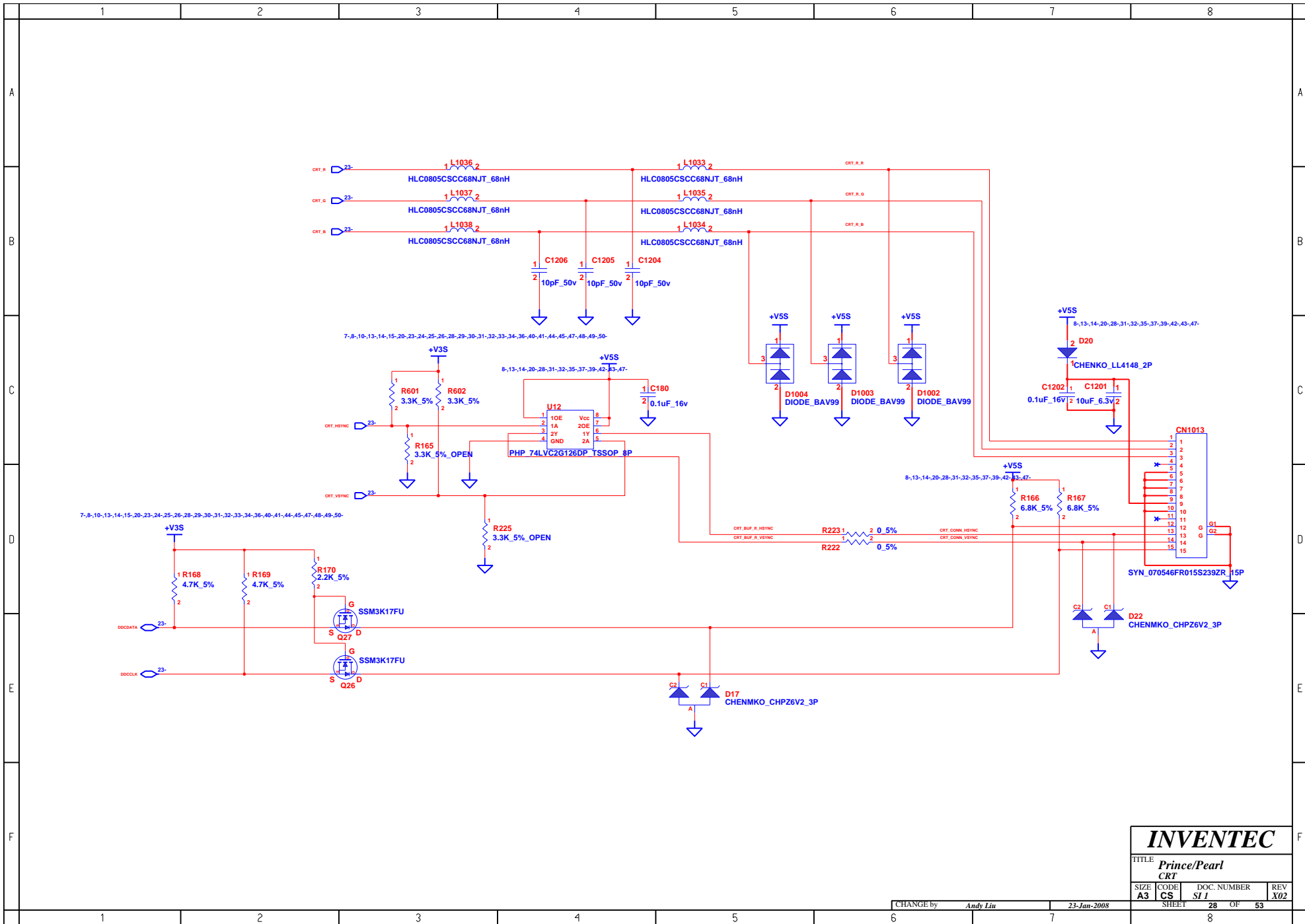


INVENTEC

TITLE			
Prince/Pearl DDR2-DAMPING			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02
CHANGE by		SHEET	OF
Andy Liu		27	53
21-Nov-2007		8	

CHANGE by Andy Liu 21-Nov-2007

SHEET 27 OF 53



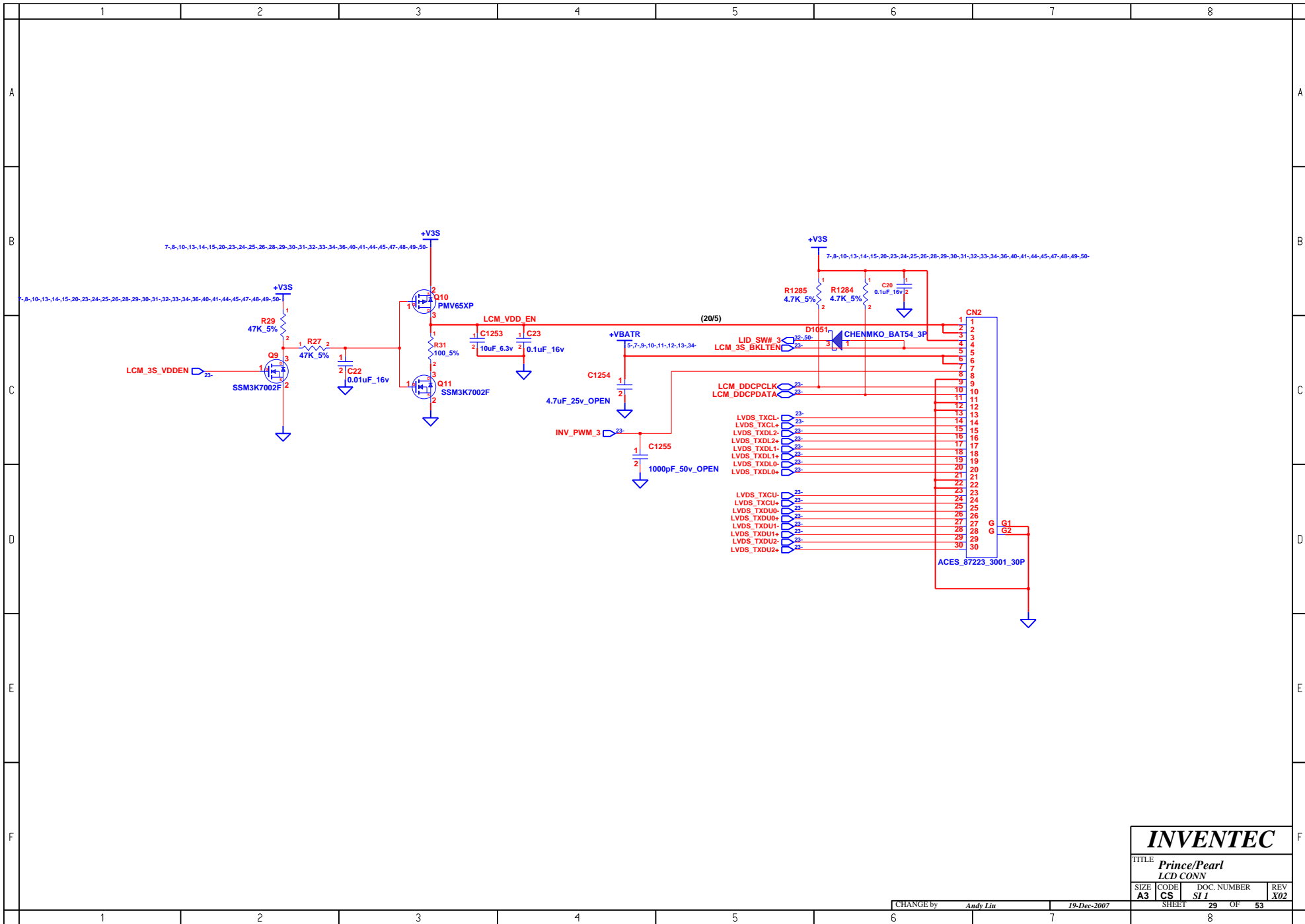
INVENTEC

TITLE
Prince/Pearl
CRT

SIZE A3	CODE CS	DOC. NUMBER ST1	REV X02
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CHANGE by *Andy Liu* 23-Jan-2008

SHEET 28 OF 53

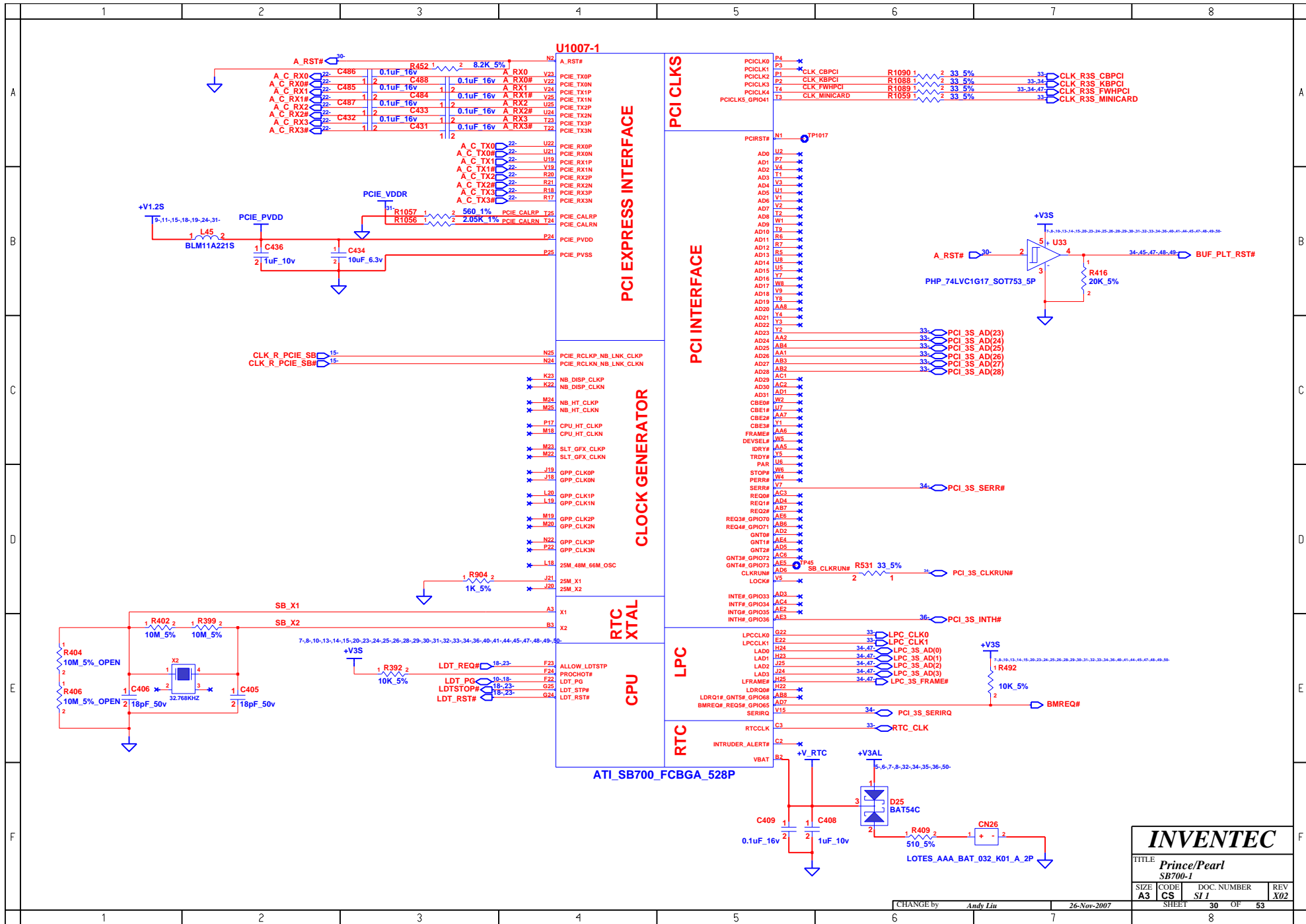


INVENTEC

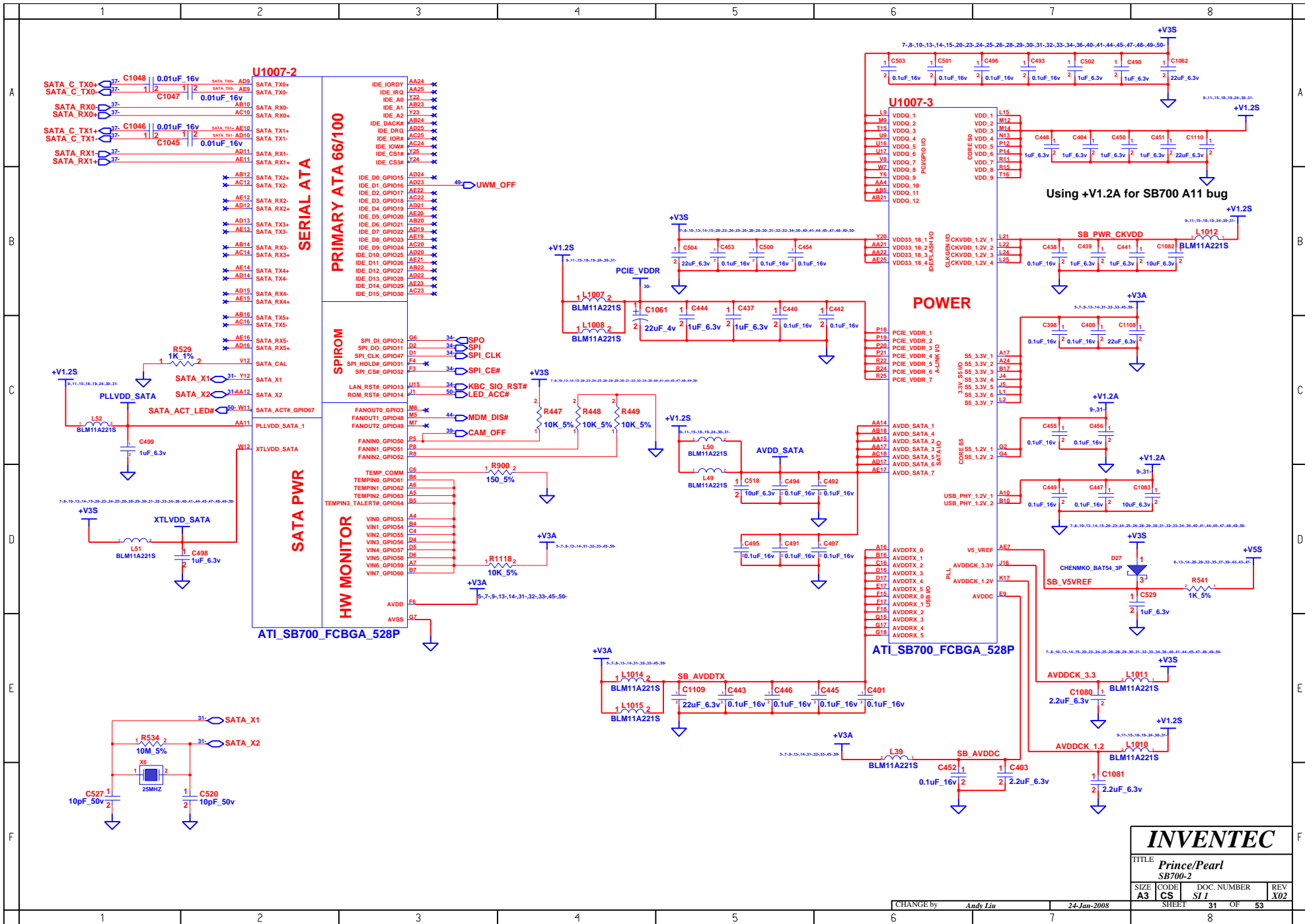
TITLE
Prince/Pearl
LCD CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI1	X02

CHANGE by	Andy Liu	19-Dec-2007	SHEET	29	OF	53
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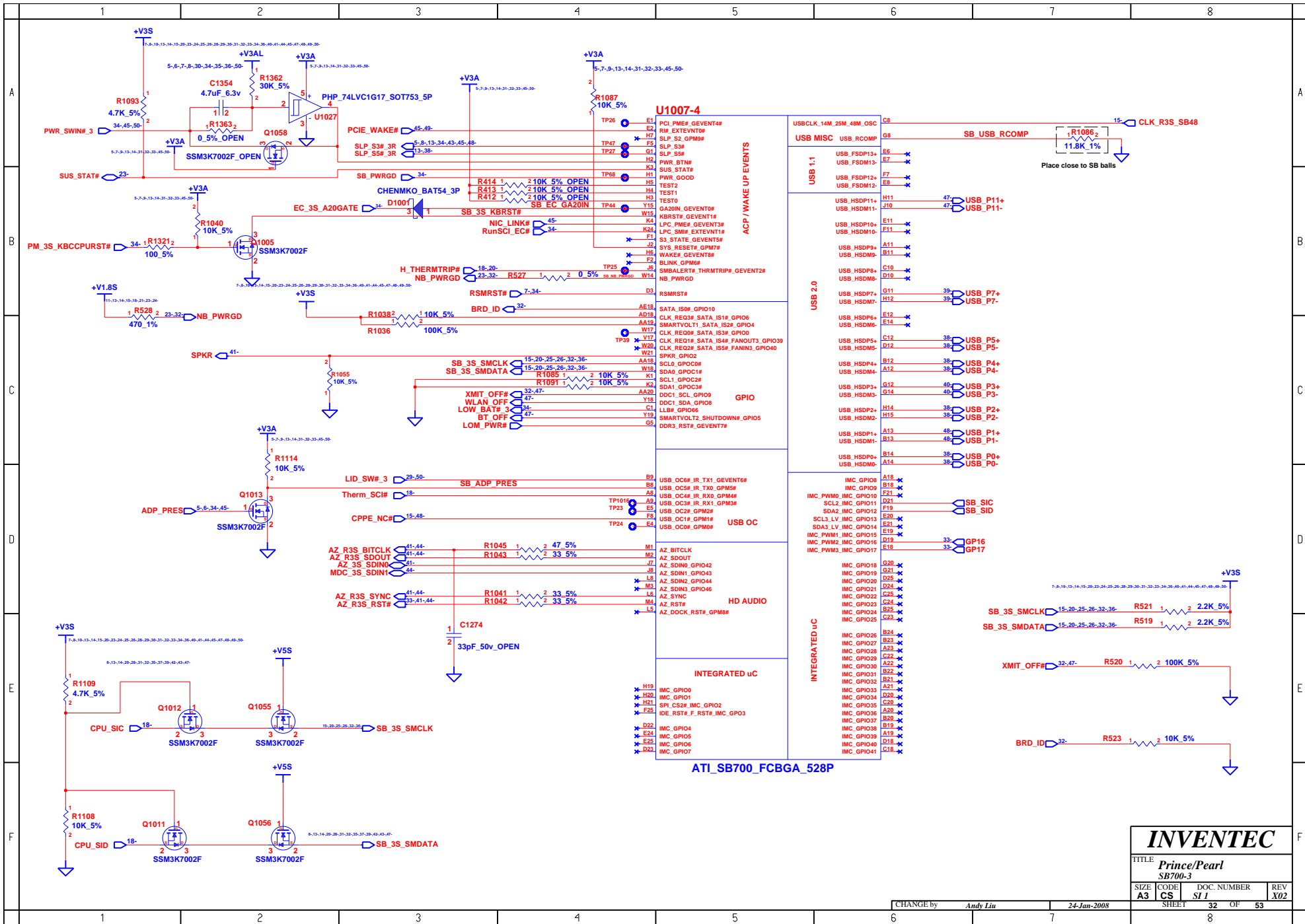
INVENTEC			
TITLE: Prince/Pearl SB700-1			
SIZE: A3	CODE: CS	DOC. NUMBER: ST1	REV: X02
CHANGE by: Andy Liu		26-Nov-2007	
SHEET: 30		OF: 53	



INVENTEC

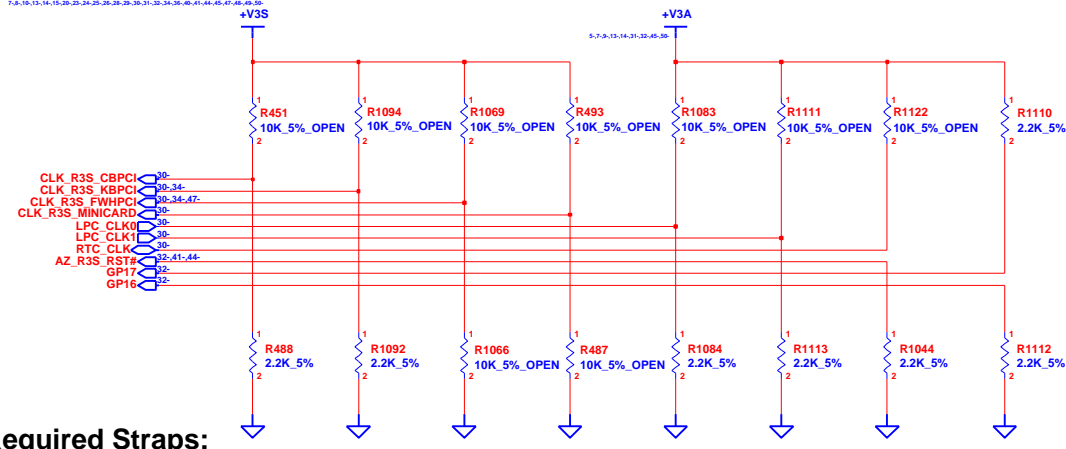
TITLE
Prince/Pearl
SB700-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02



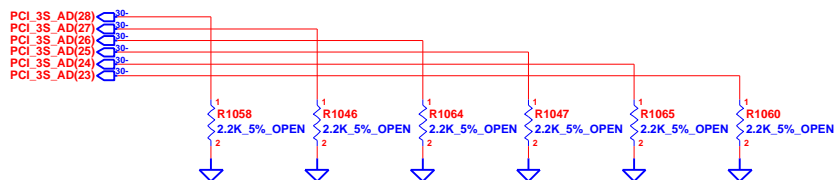
INVENTEC			
TITLE Prince/Pearl SB700-3			
SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
CHANGE by <i>Andy Liu</i>		24-Jan-2008	
SHEET 32		OF 53	

7,8,10,13,14,15,20,23,24,25,26,28,29,30,31,32,34,36,40,41,44,45,47,48,49,50



Required Straps:

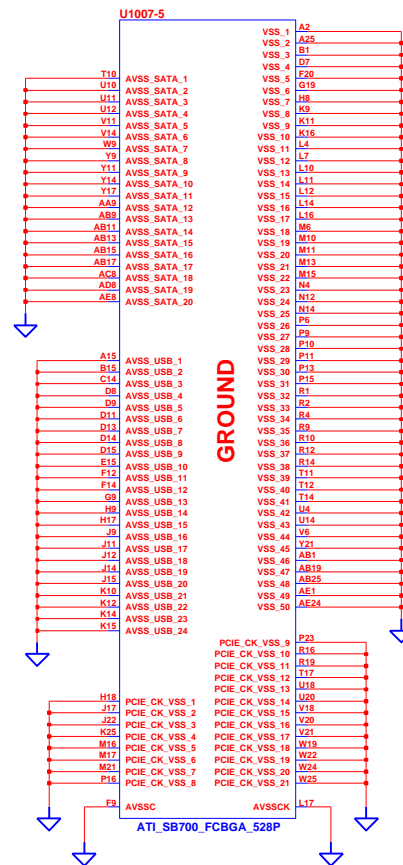
	CLK_R3S_CBPC1	CLK_R3S_KBPC1	CLK_R3S_FWHPC1	CLK_R3S_MINICARD	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE H, H = Reserved H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	



Debug Straps

SB700 HAS 15K INTERNAL PU FOR PCI_AD

	PCI_3S_AD(28)	PCI_3S_AD(27)	PCI_3S_AD(26)	PCI_3S_AD(25)	PCI_3S_AD(24)	PCI_3S_AD(23)
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

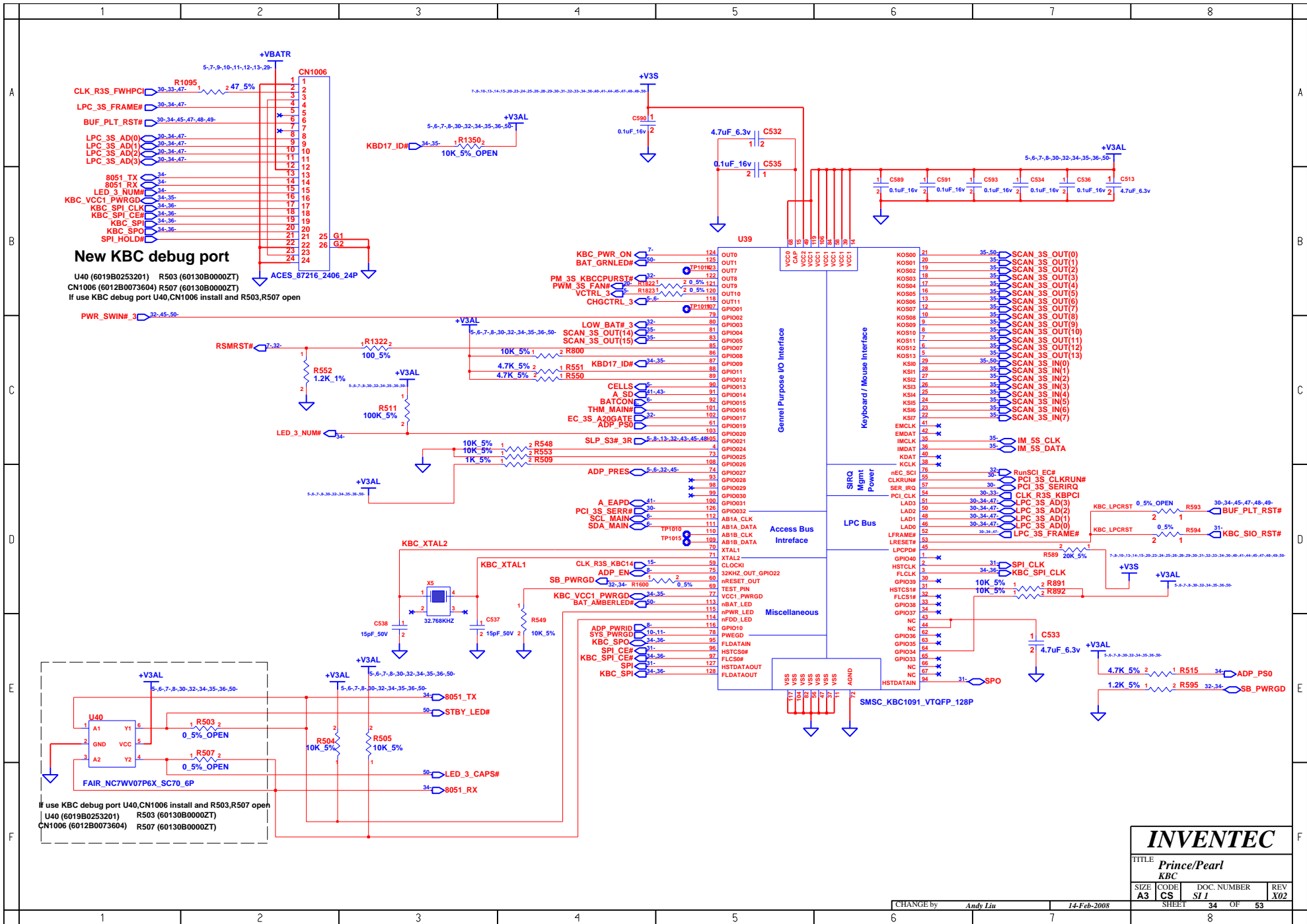


GROUND

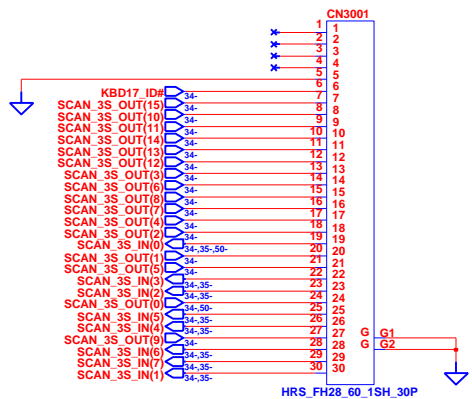
INVENTEC

TITLE
Prince/Pearl
SB700-4

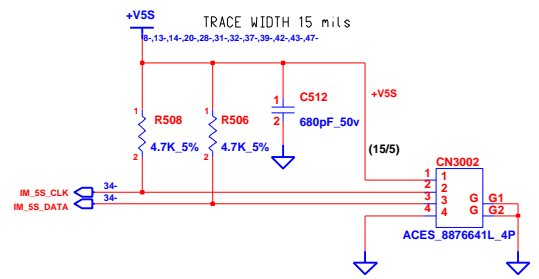
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02



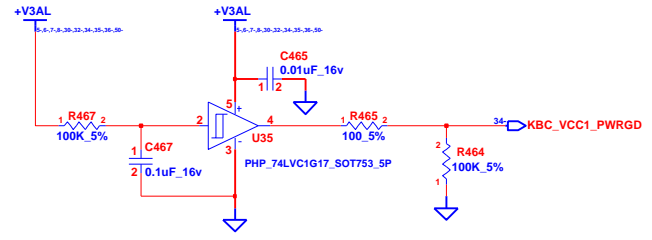
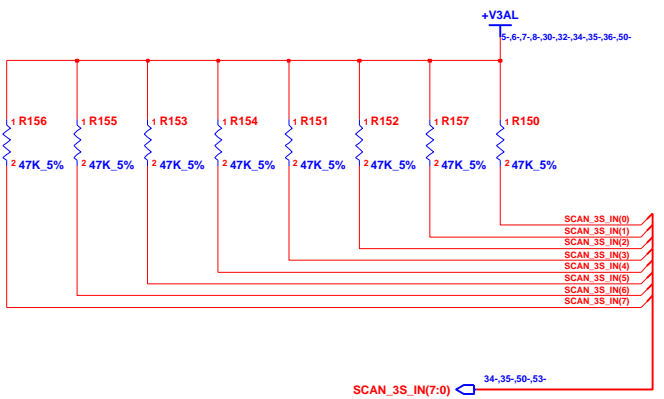
INVENTEC			
TITLE Prince/Pearl KBC			
SIZE A3	CODE CS	DOC NUMBER ST 1	REV X02
CHANGE by Andy Liu		14-Feb-2008	
SHEET 34		OF 53	



KEYBOARD CONN

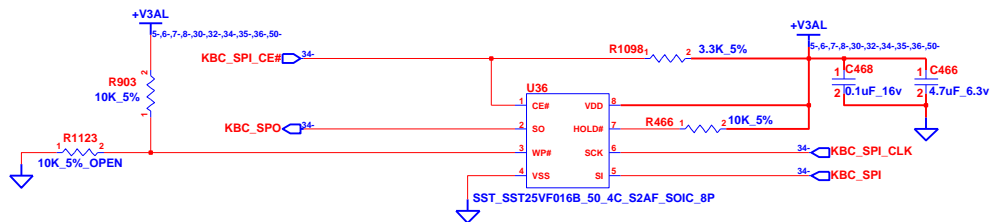


TOUCH PAD CNTR

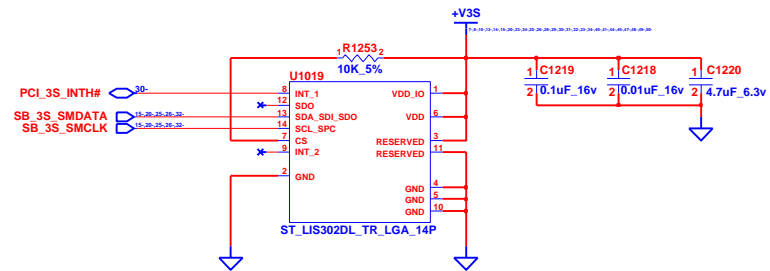


U35 should be placed close to U39.

INVENTEC			
TITLE Prince/Pearl KB&TP CONN			
SIZE A3	CODE CS	DOC. NUMBER S1 1	REV X02
CHANGE by Andy Liu		23-Jan-2008	
SHEET 35		OF 53	



SPI Flash



Accelerometer

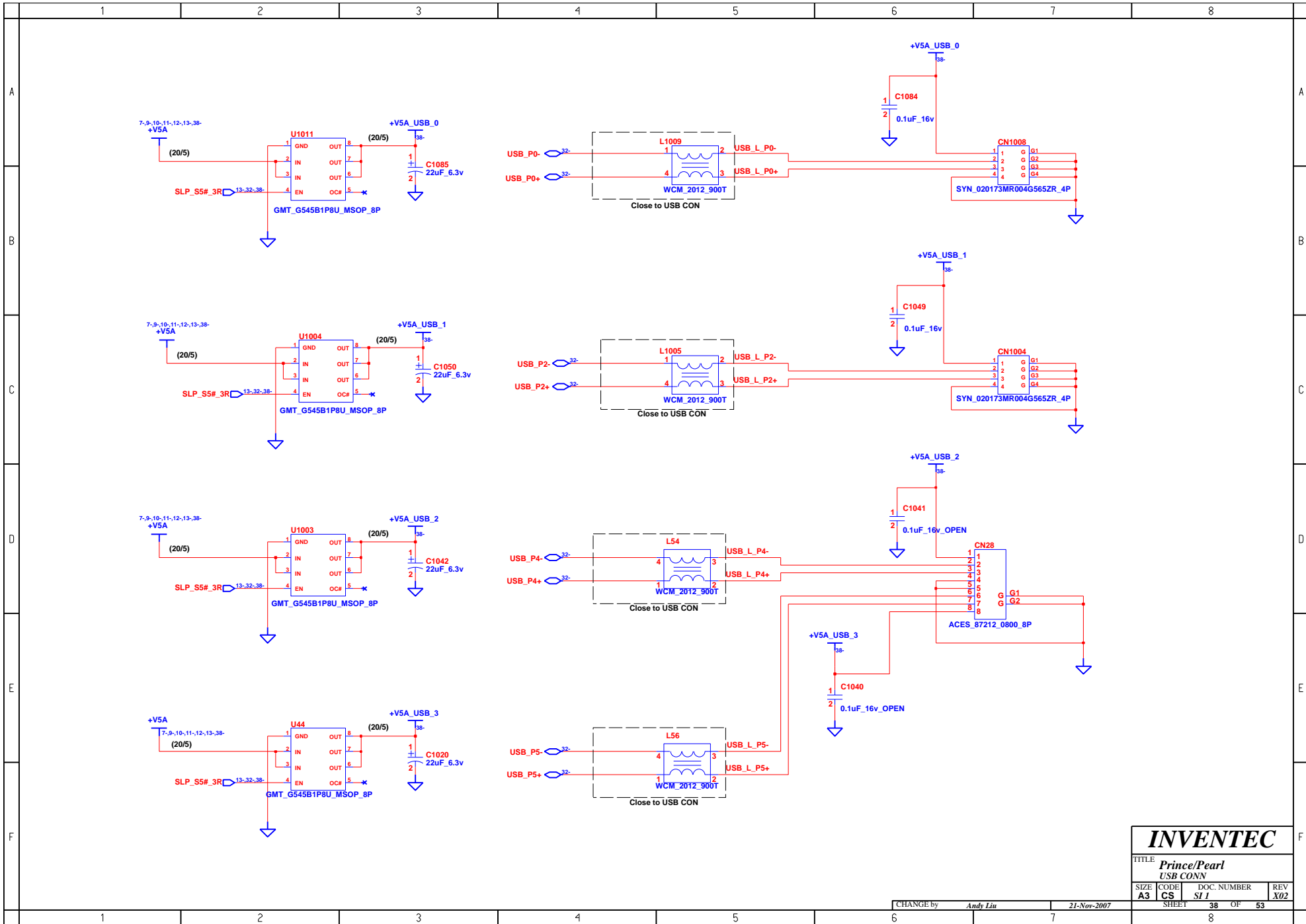
INVENTEC

TITLE *Prince/Pearl*
SPI & ACCELEROMETER

SIZE A3	CODE CS	DOC. NUMBER <i>SI1</i>	REV X02
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CHANGE by *Andy Liu* 28-Jan-2008

SHEET 36 OF 53



INVENTEC

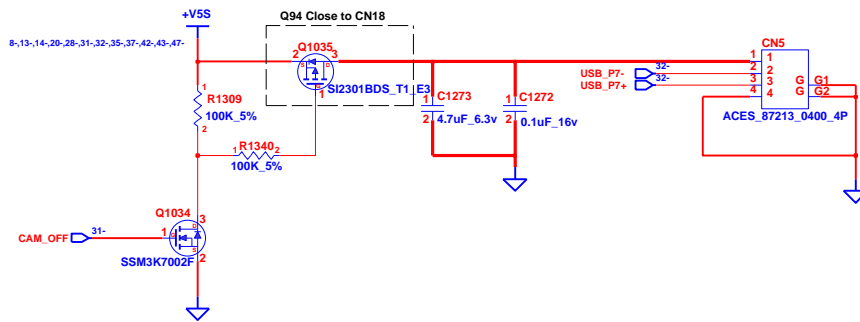
TITLE
Prince/Pearl
 USB CONN

SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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CHANGE by *Andy Liu* 21-Nov-2007

SHEET 38 OF 53

(At least 20mils.)



USB WEBCAM CONNECTOR

INVENTEC

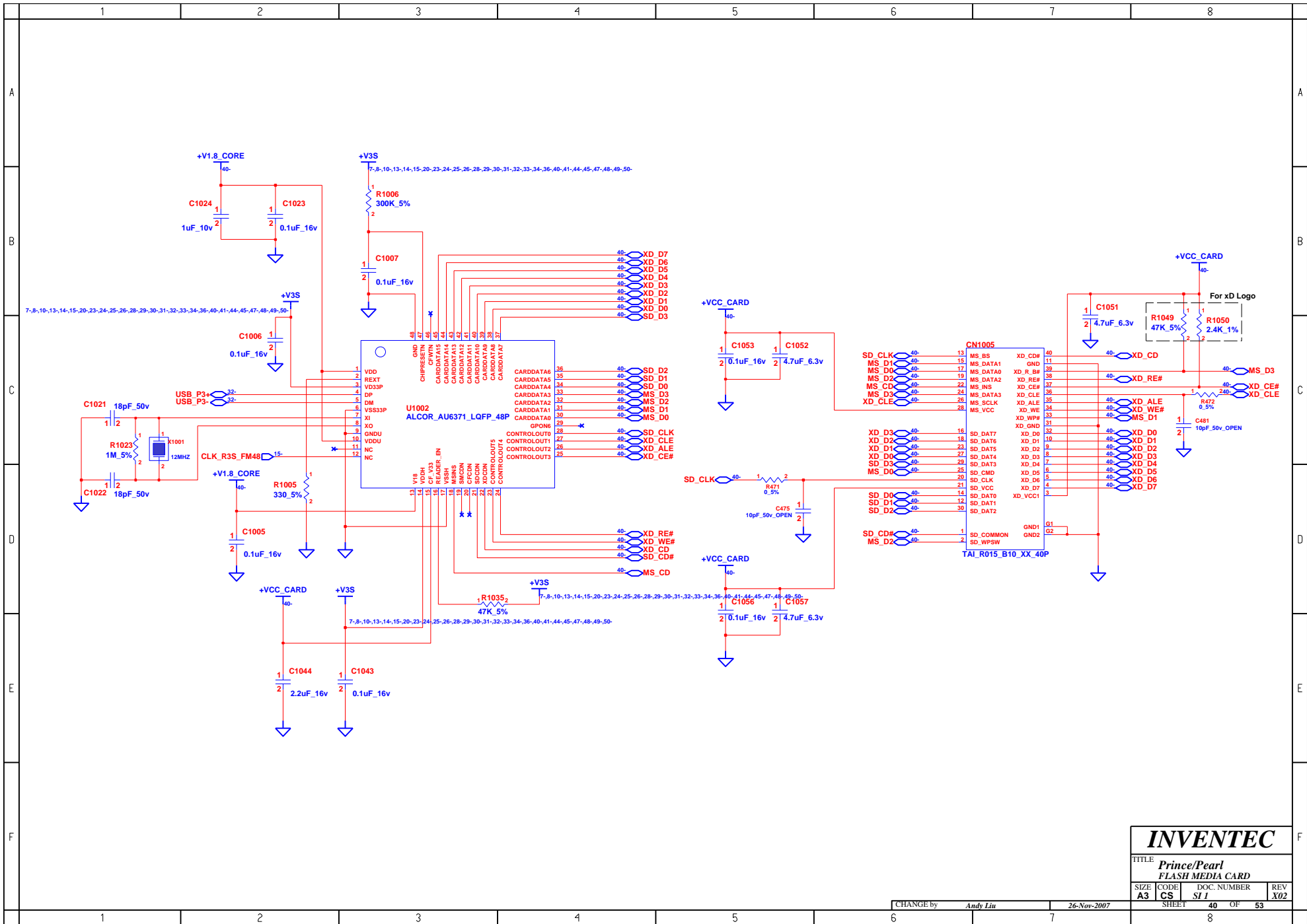
TITLE
Prince/Pearl
USB WEBCAM CONN

SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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CHANGE by *Andy Liu* 26-Nov-2007

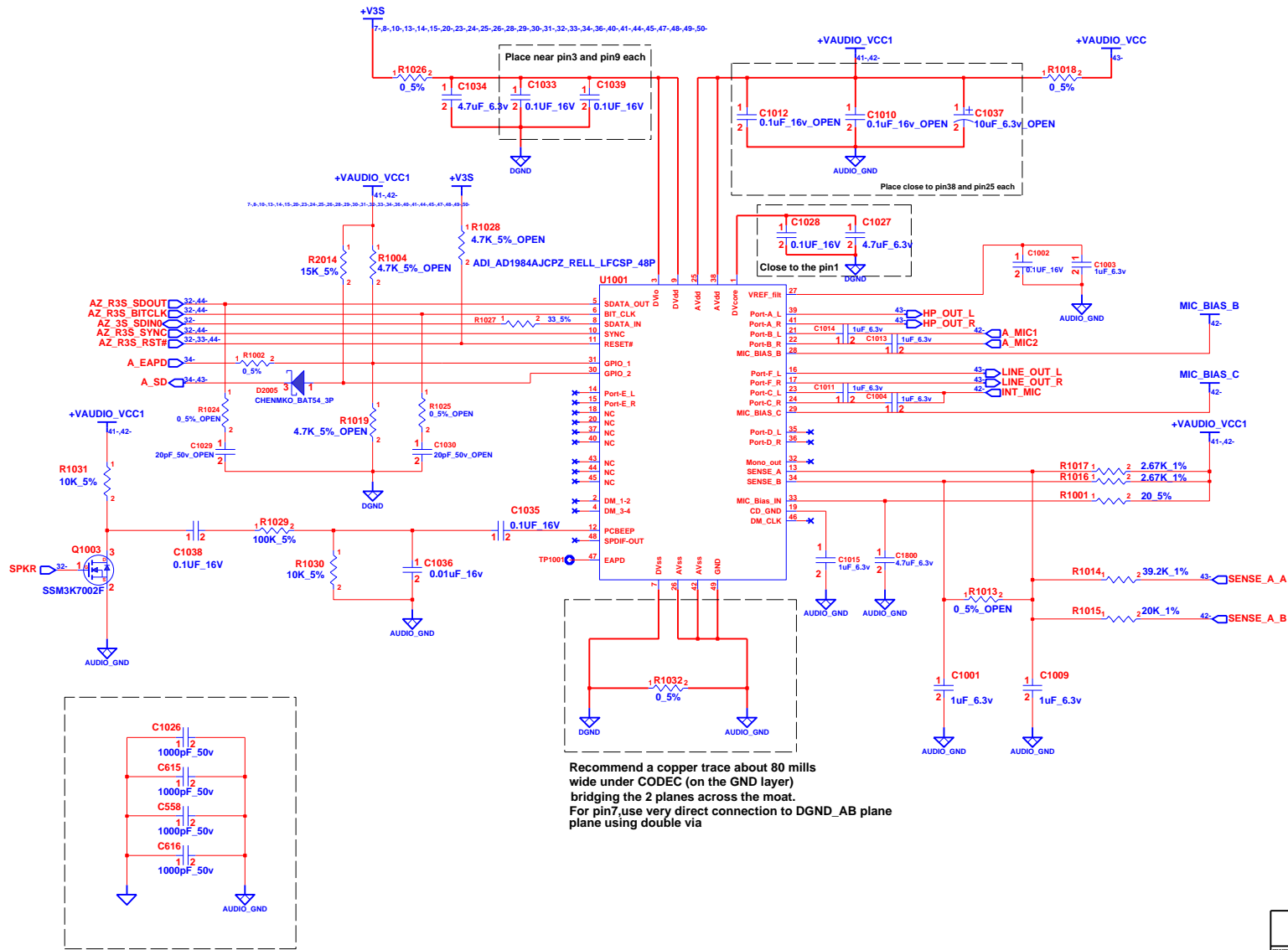
SHEET 39 OF 53

8

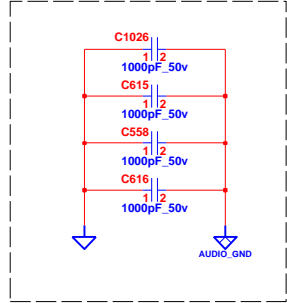


INVENTEC

TITLE			
Prince/Pearl FLASH MEDIA CARD			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02



Recommend a copper trace about 80 mills wide under CODEC (on the GND layer) bridging the 2 planes across the moat.
For pin7, use very direct connection to DGND_AB plane using double via

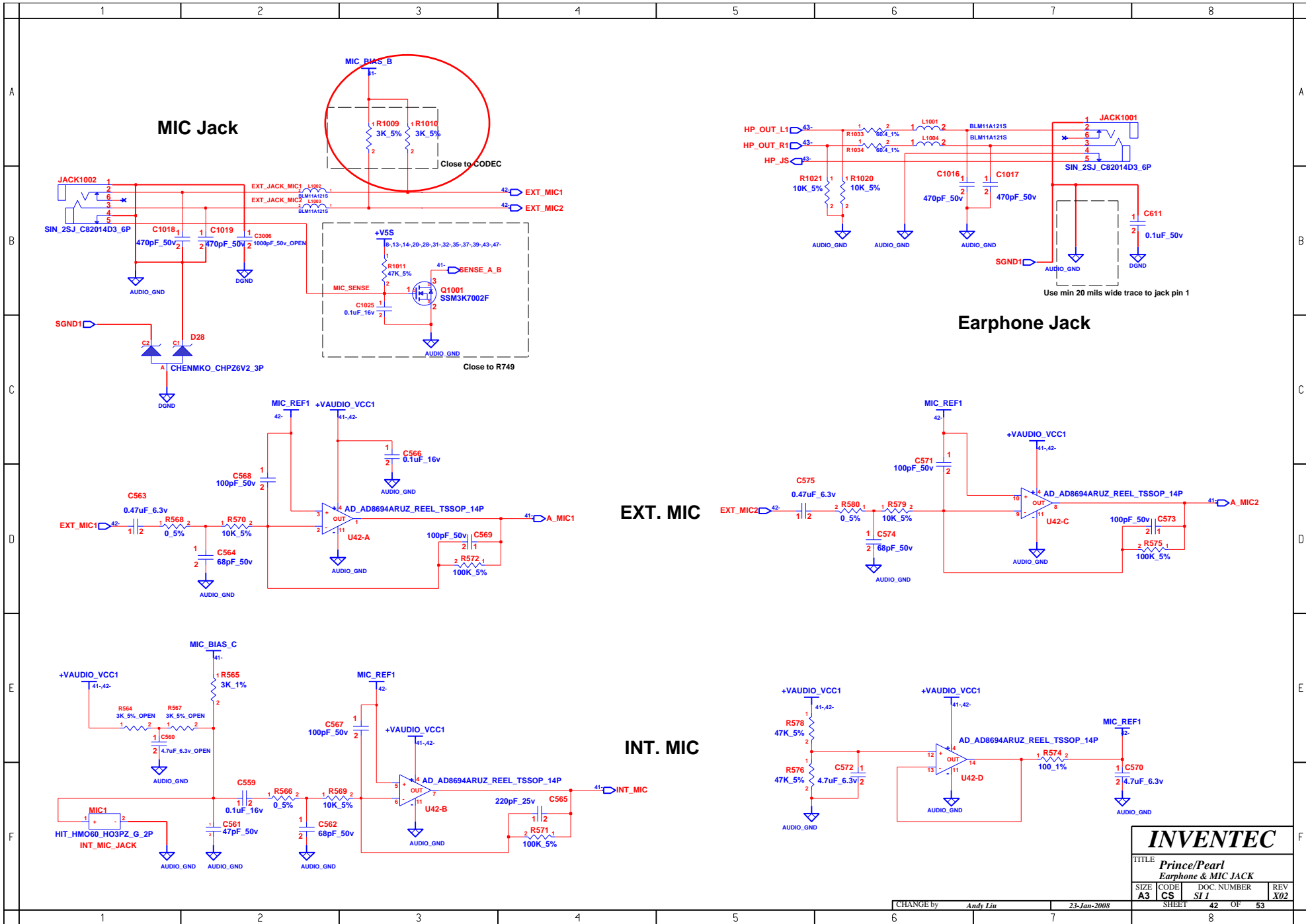


For EMI Test

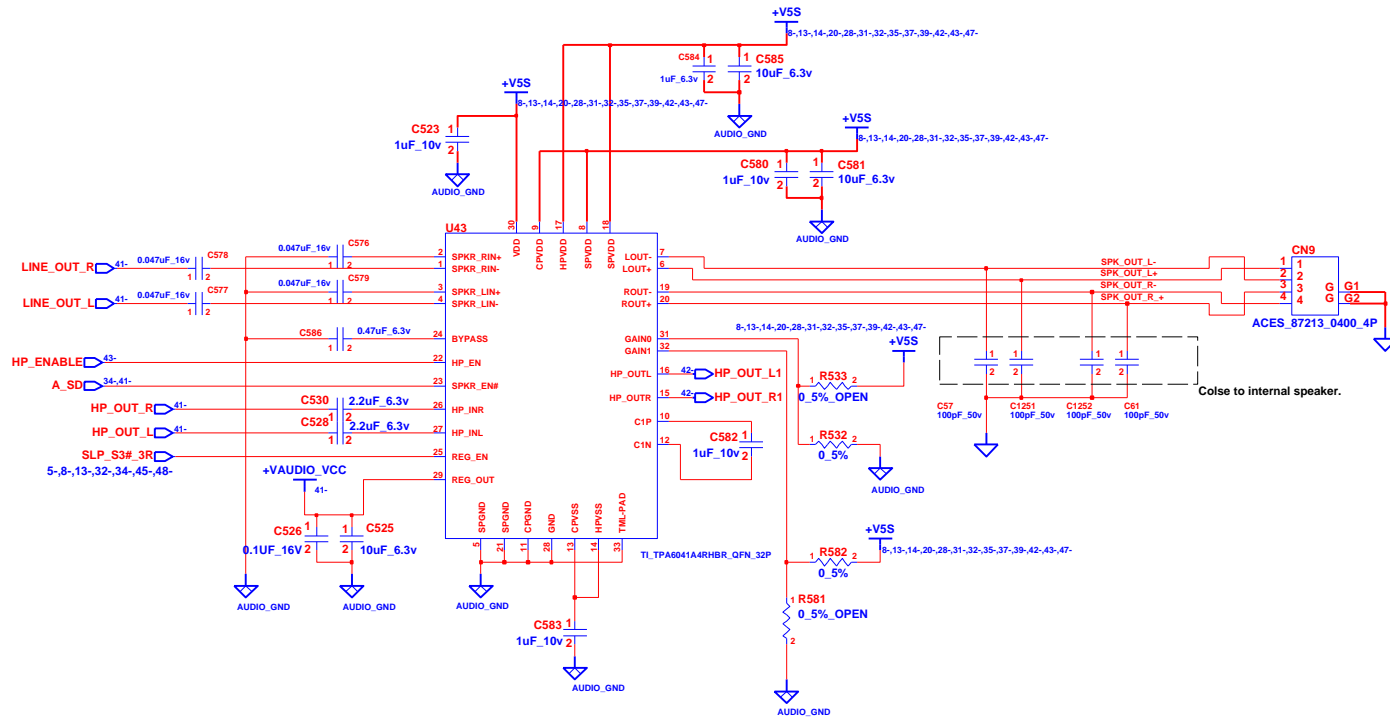
INVENTEC

TITLE
**Prince/Pearl
AZALIA CODEC**

SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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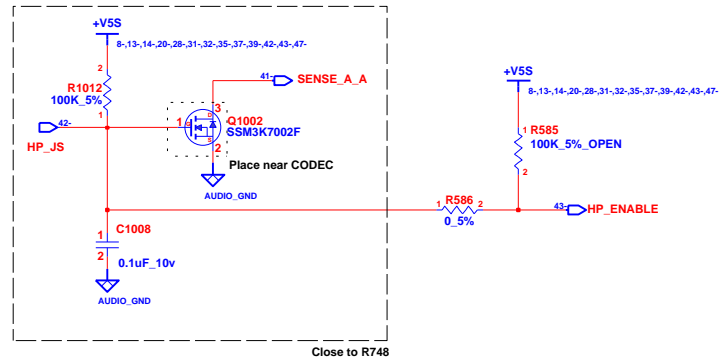


INVENTEC			
TITLE <i>Prince/Pearl</i> Earphone & MIC JACK			
SIZE A3	CODE CS	DOC. NUMBER S11	REV X02
CHANGE by <i>Andy Liu</i>		23-Jan-2008	
SHEET		42 OF 53	



Internal Speaker

Close to internal speaker.



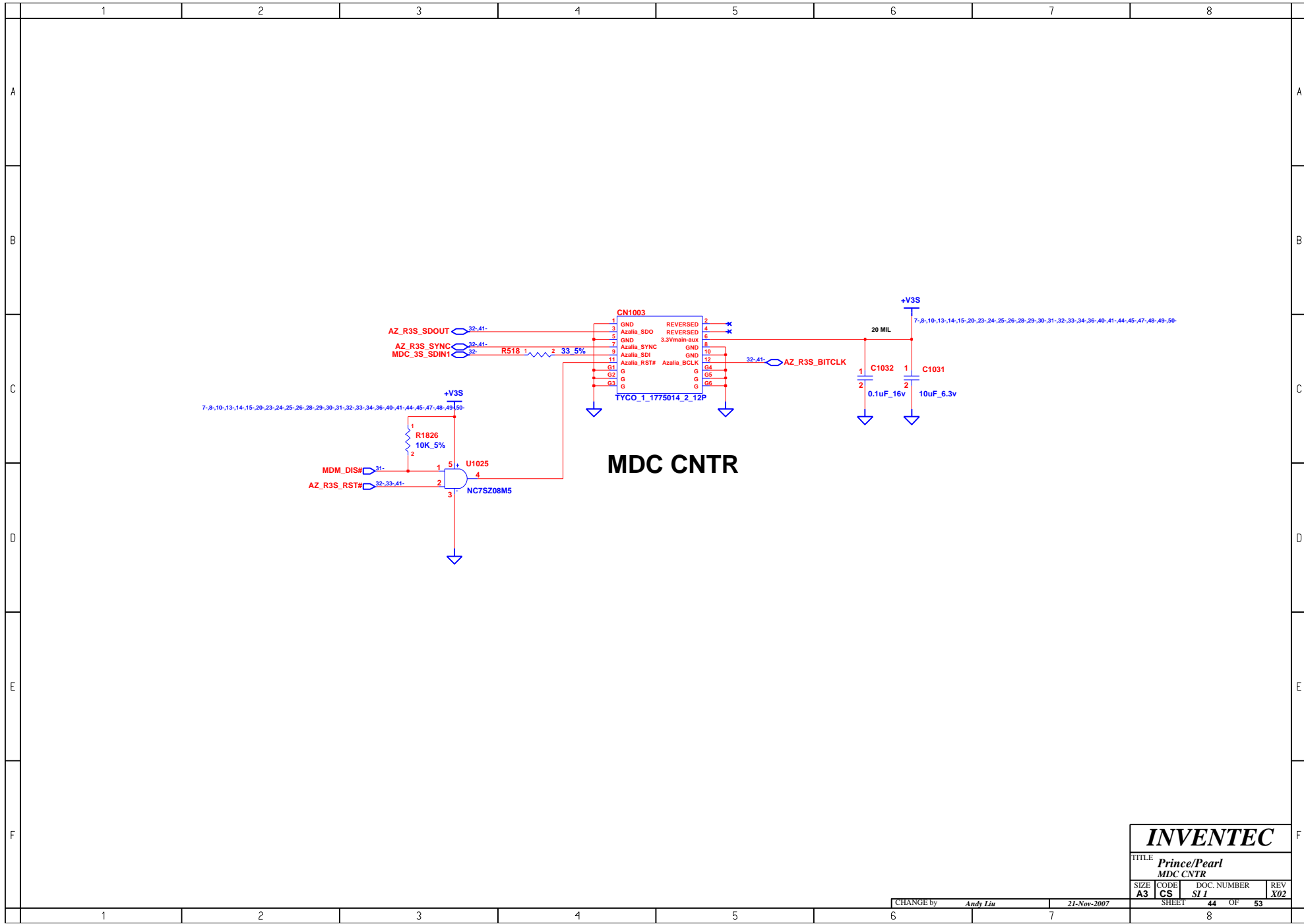
INVENTEC

TITLE
Prince/Pearl
AUDIO AMP & HP JACK

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

CHANGE by *Andy Liu* 21-Nov-2007

SHEET 43 OF 53



MDC CNTR

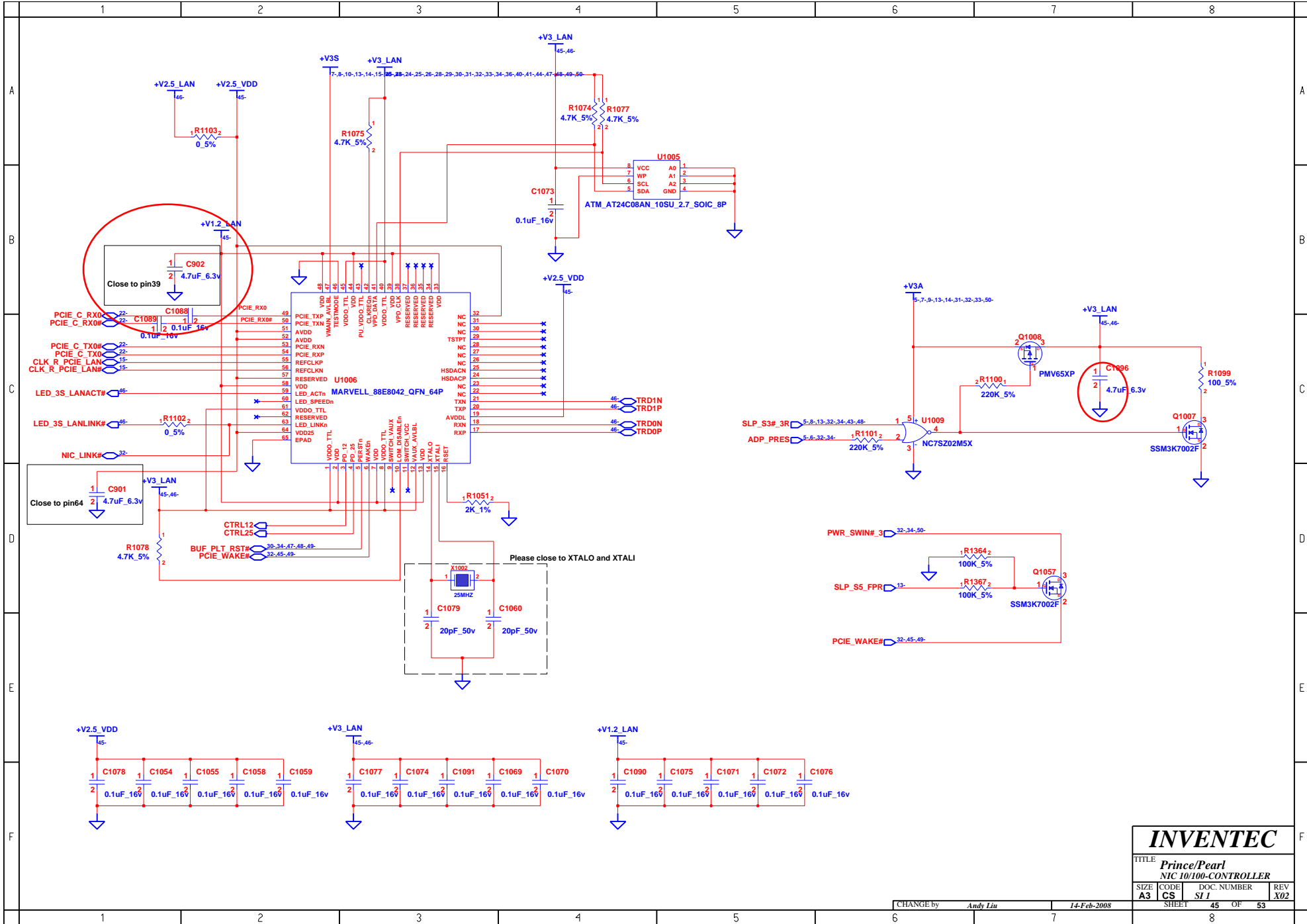
INVENTEC

TITLE *Prince/Pearl*
MDC CNTR

SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02

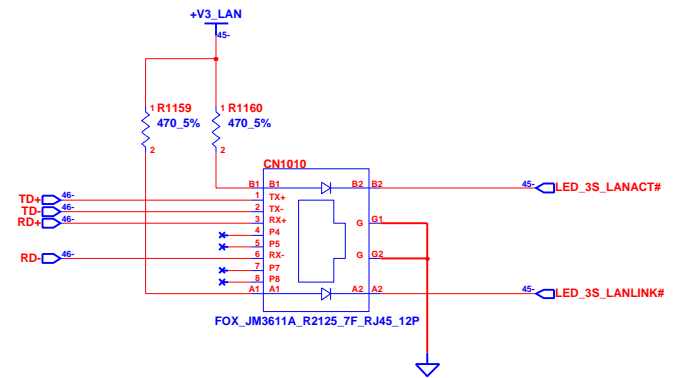
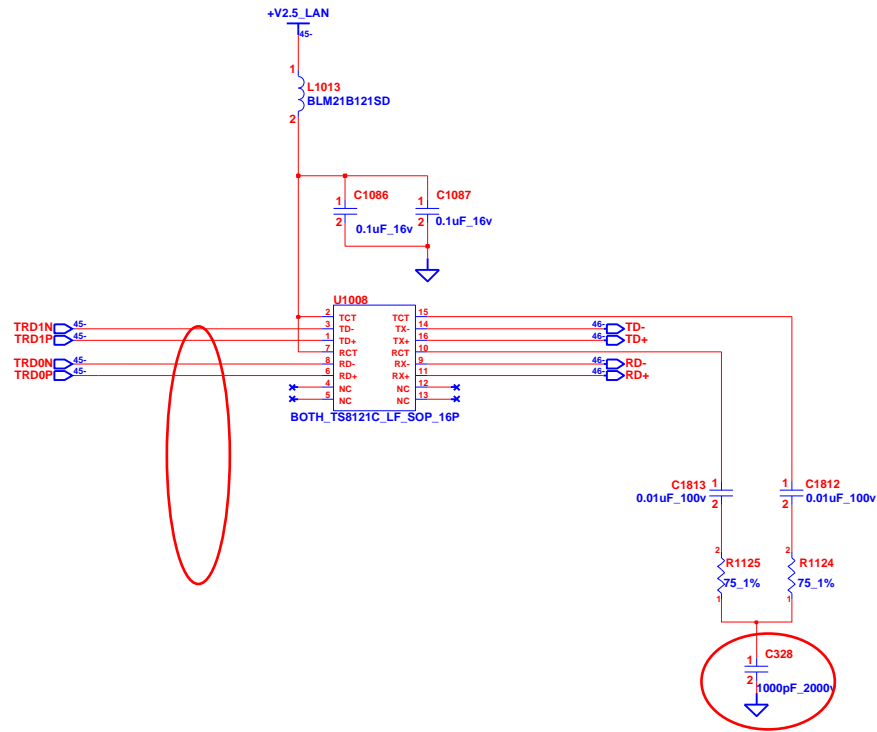
CHANGE by *Andy Liu* 21-Nov-2007

SHEET 44 OF 53



INVENTEC

TITLE			
Prince/Pearl			
NIC 10/100-CONTROLLER			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI 1	X02



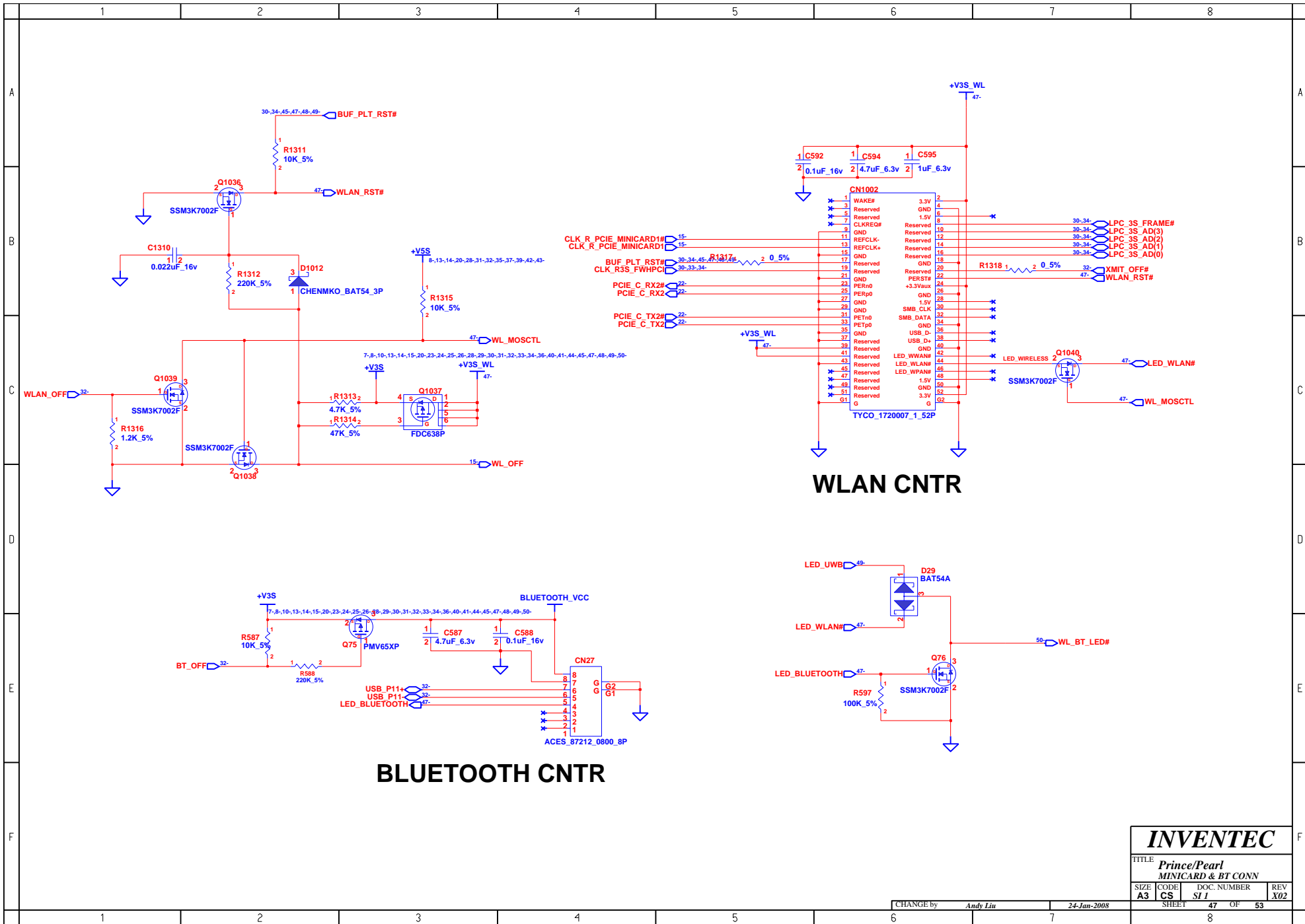
INVENTEC

TITLE
Prince/Pearl
 NIC 10/100-RJ45 CONN

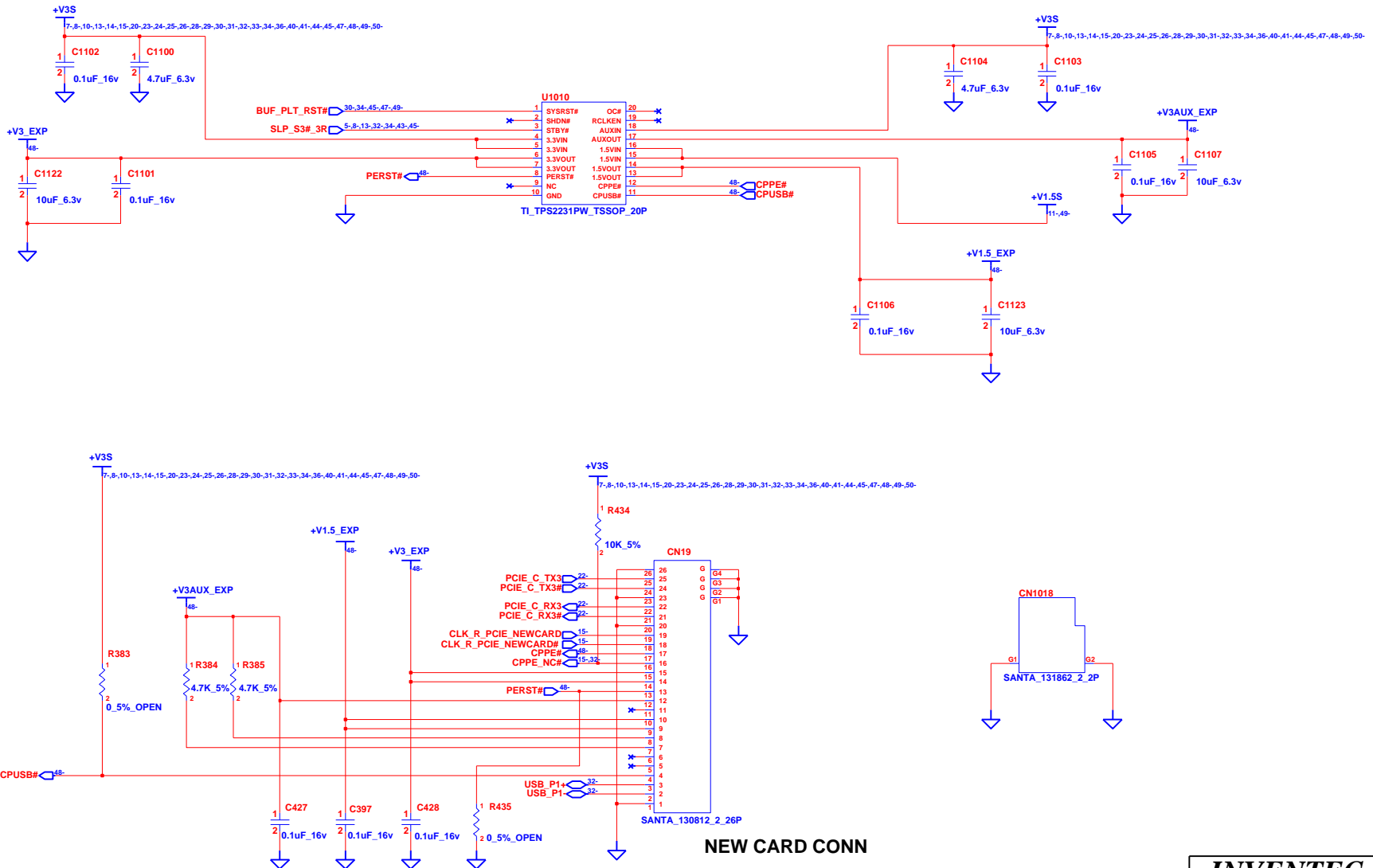
SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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CHANGE by *Andy Liu* 4-Feb-2008

SHEET 46 OF 53

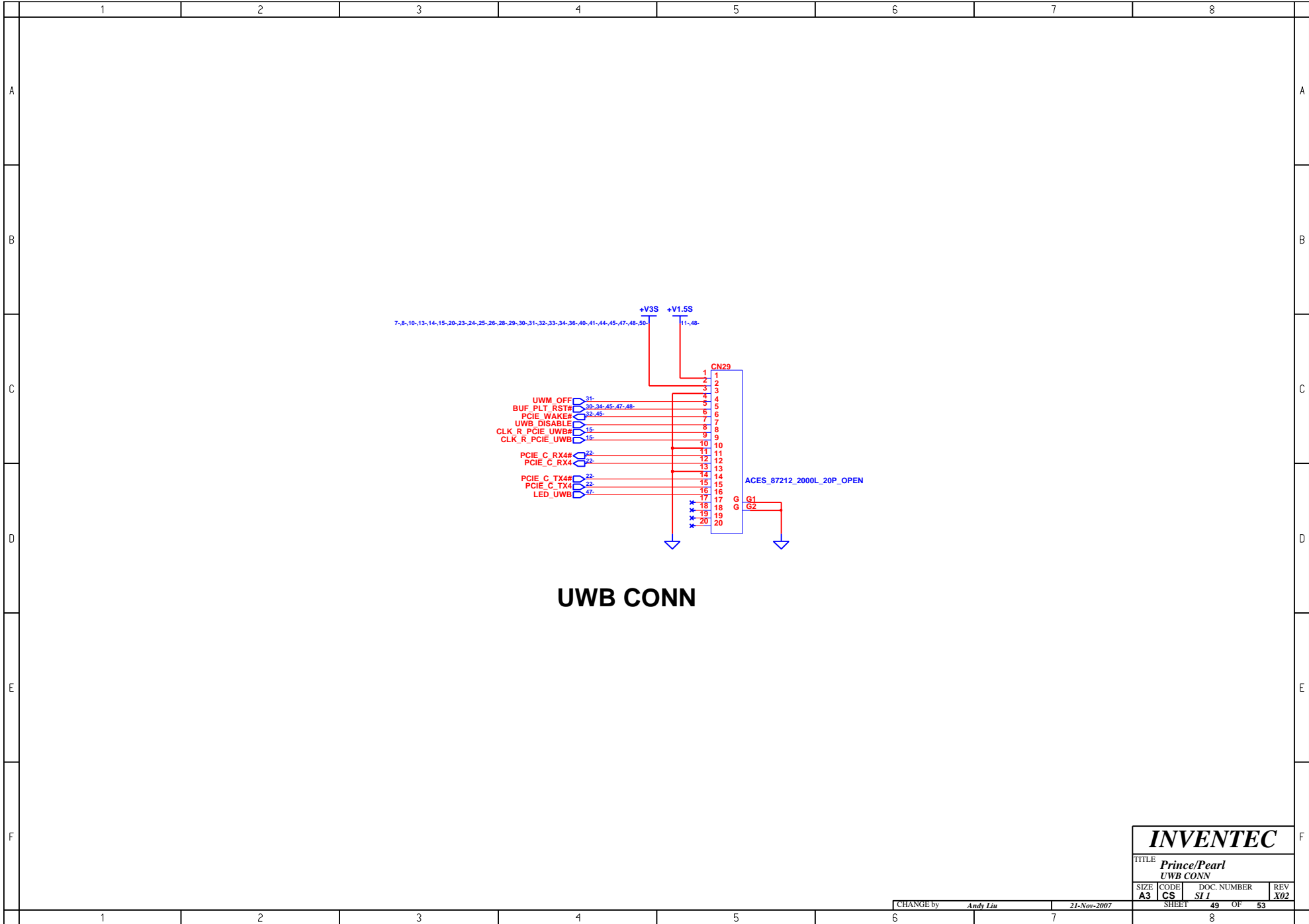


INVENTEC			
TITLE <i>Prince/Pearl</i> MINICARD & BT CONN			
SIZE A3	CODE CS	DOC. NUMBER <i>SI1</i>	REV X02
CHANGE by <i>Andy Liu</i>		24-Jan-2008	
SHEET 47		OF 53	



NEW CARD CONN

INVENTEC			
TITLE Prince/Pearl NEW CARD			
SIZE A3	CODE CS	DOC. NUMBER SI 1	REV X02
CHANGE by <i>Andy Liu</i>		19-Dec-2007	
SHEET		48 OF 53	
1		8	



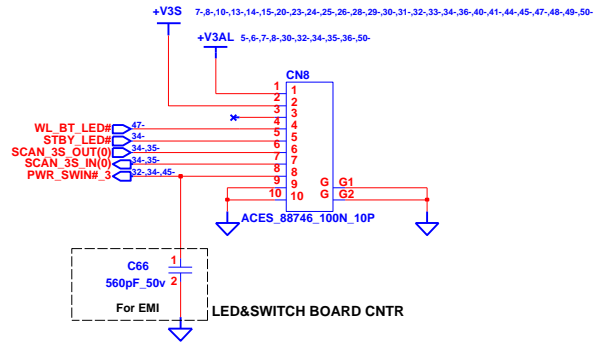
INVENTEC

TITLE
Prince/Pearl
UWB CONN

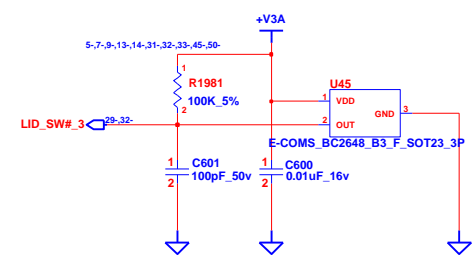
SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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CHANGE by *Andy Liu* 21-Nov-2007

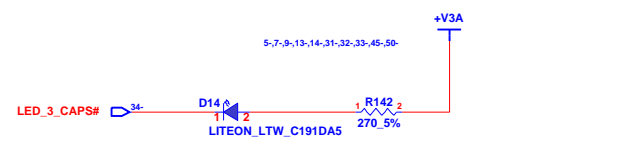
SHEET 49 OF 53



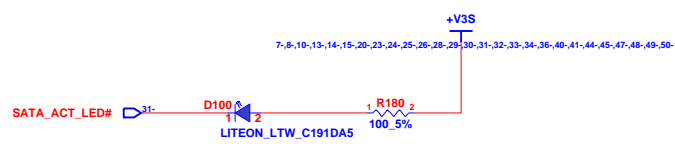
LED&SWITCH BOARD CNTR



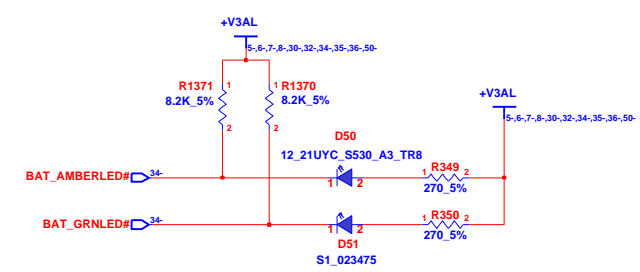
LID SWITCH



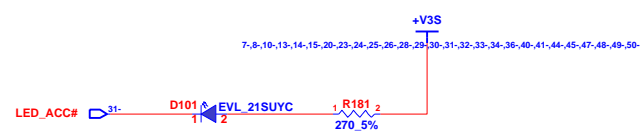
CAP LED



HDD & ODD LED

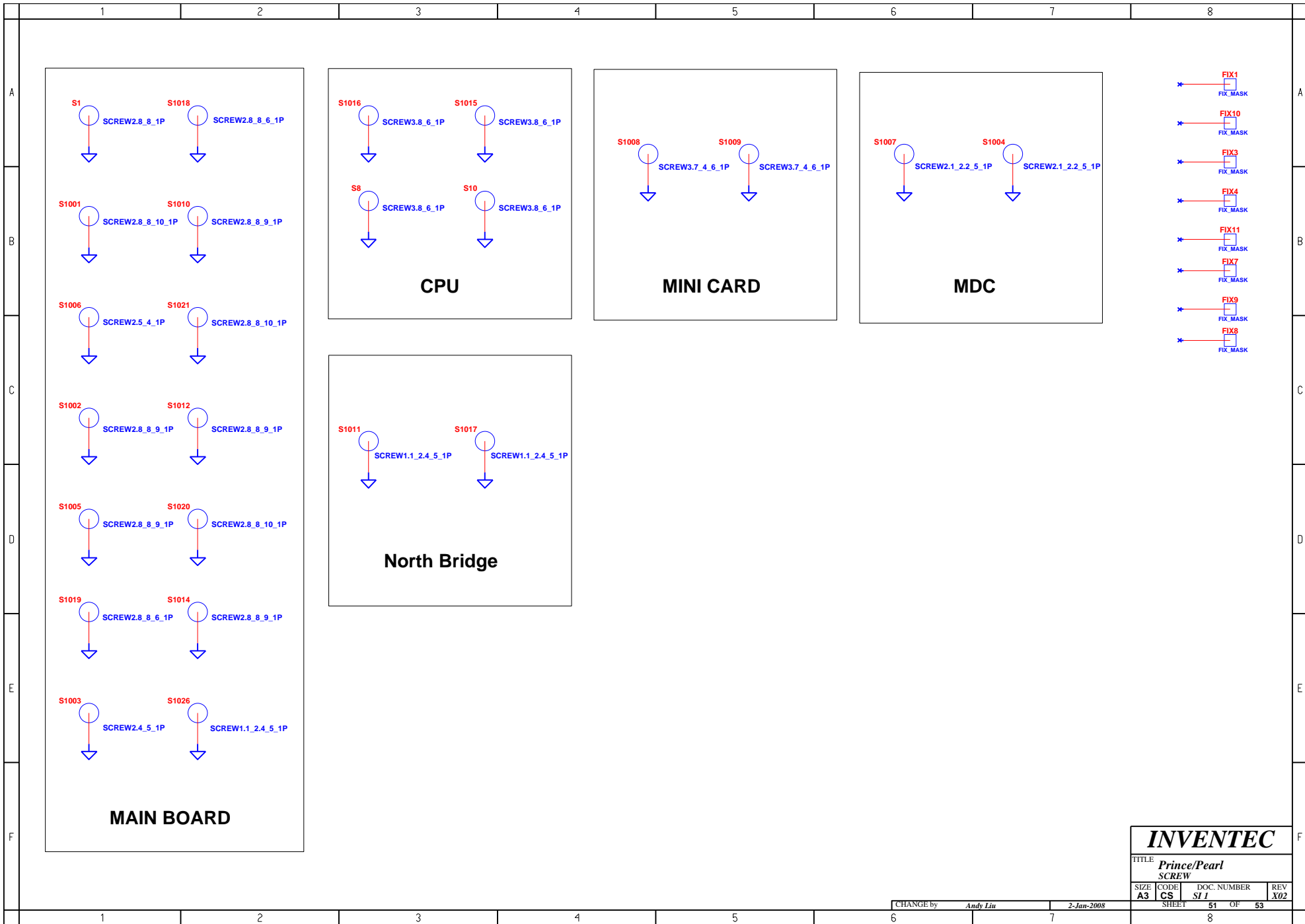


BATTERY-CHARGE LED



ACCELEROMETER LED

INVENTEC			
TITLE <i>Prince/Pearl</i> BUTTON & LED			
SIZE A3	CODE CS	DOC. NUMBER <i>SI 1</i>	REV X02
CHANGE by <i>Andy Liu</i>		3-Jan-2008	
SHEET 50		OF 53	
		8	

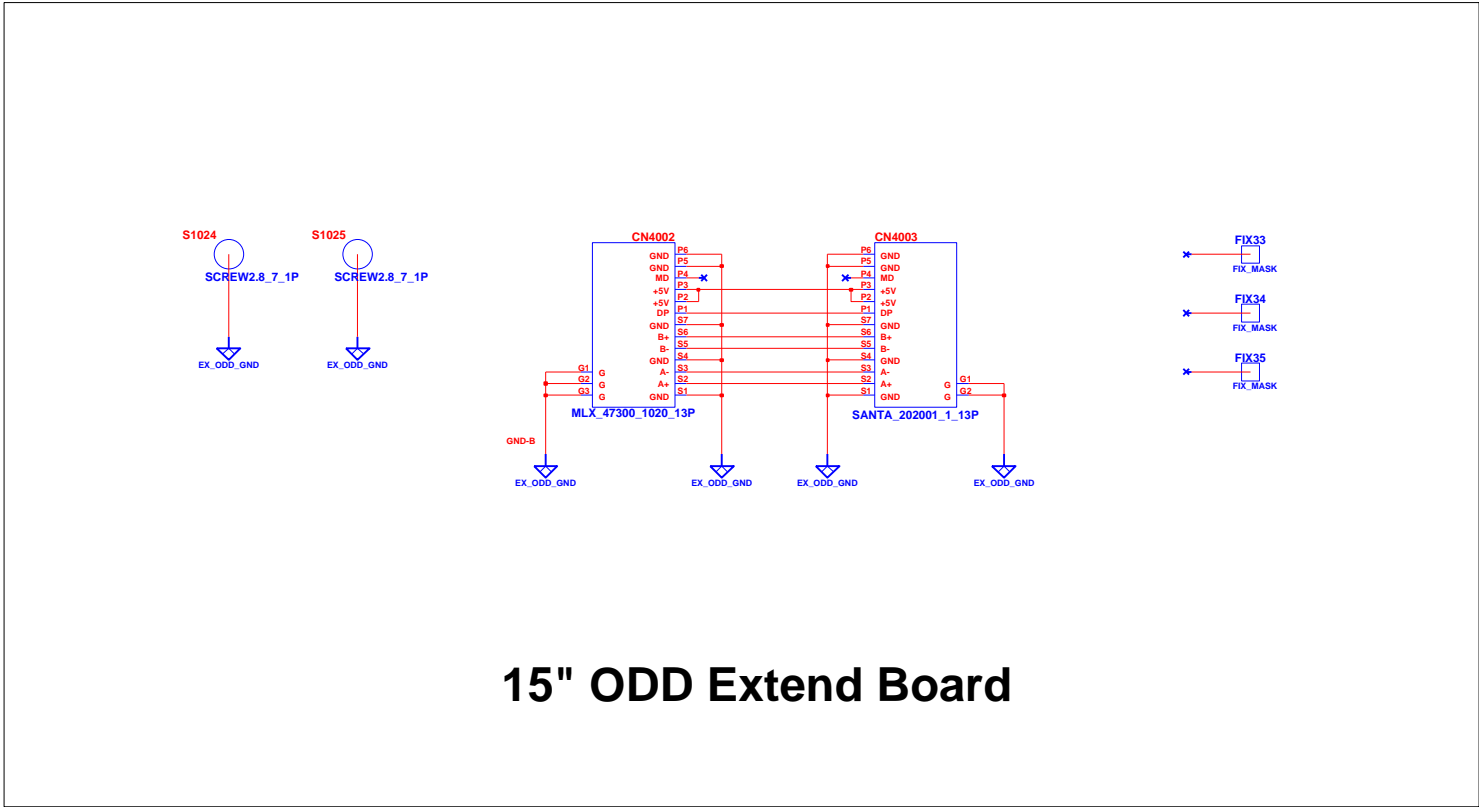


INVENTEC

TITLE			
Prince/Pearl			
SCREW			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	S11	X02

CHANGE by Andy Liu 2-Jan-2008

SHEET 51 OF 53



15" ODD Extend Board

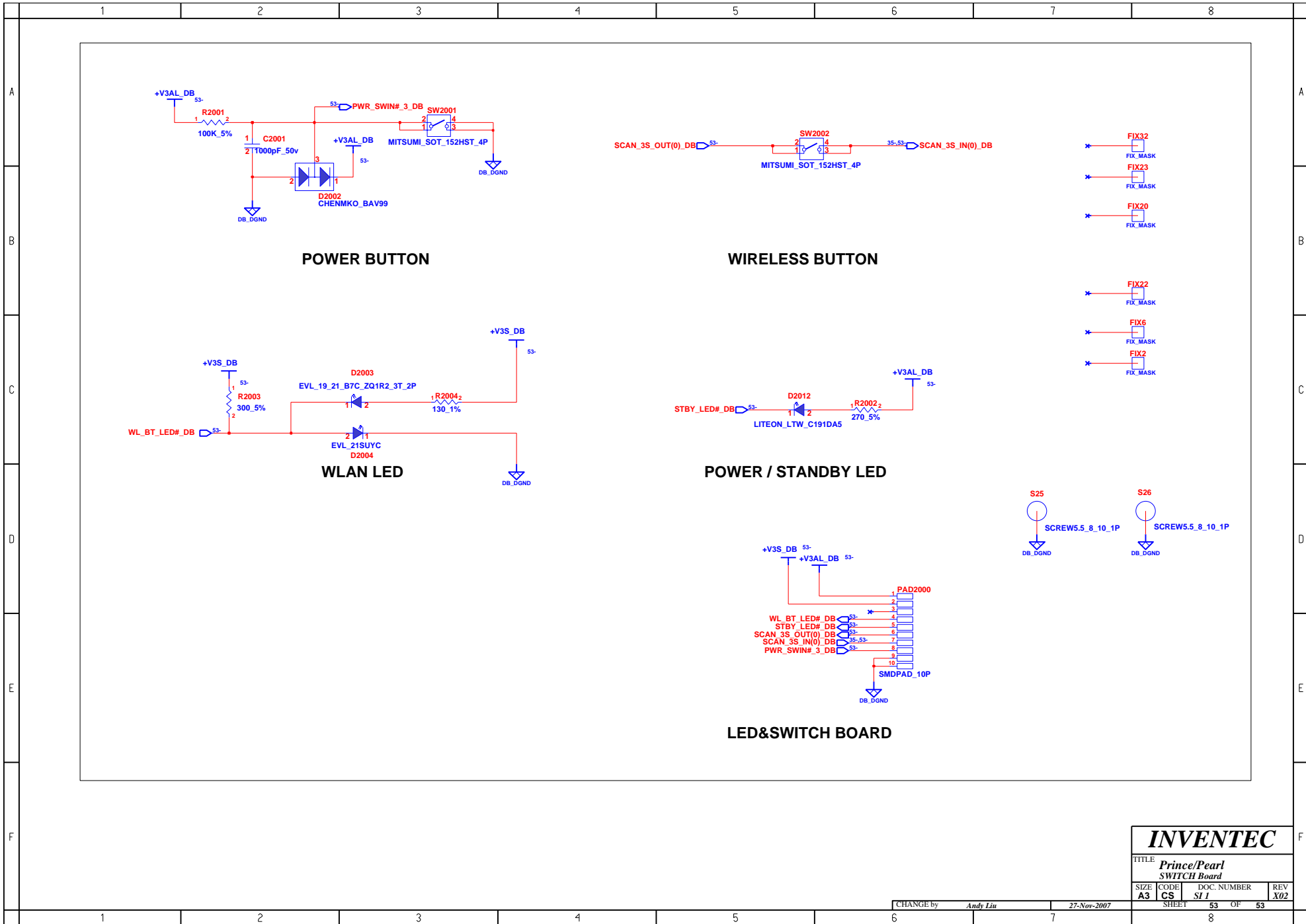
INVENTEC

TITLE
Prince/Pearl
15" ODD Extend Board

SIZE A3	CODE CS	DOC. NUMBER SI1	REV X02
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CHANGE by *Andy Liu* 24-Dec-2007

SHEET 52 OF 53



INVENTEC

TITLE			
Prince/Pearl SWITCH Board			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	SI1	X02

CHANGE by Andy Liu 27-Nov-2007

SHEET 53 OF 53