

# Compal confidential

## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-30

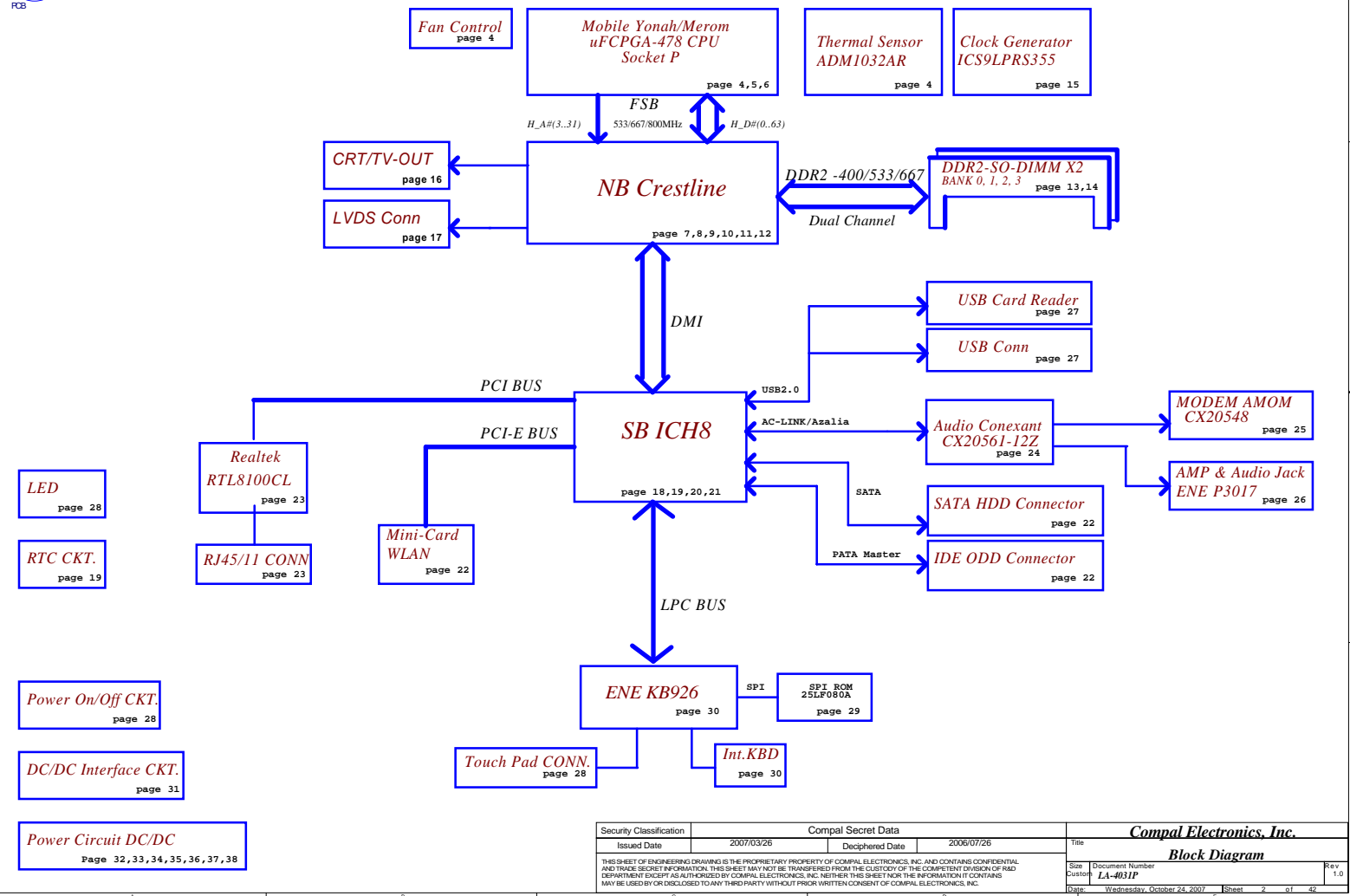
REV: 0.2

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				Customer	LA-4031P	1.0
				Date	Wednesday, October 24, 2007	Sheet 1 of 42

# Spartan 1.1 (Merom +Crestline+ICH8)



PCB



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Size	Document Number	Customer	Rev	1.0
	LA-4031P			
Date	Wednesday, October 24, 2007	Sheet	2	of 42

**Voltage Rails**

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**Symbol Note :**



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

**External PCI Devices**

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

**I2C / SMBUS ADDRESSING**

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

**SMBUS Control Table**

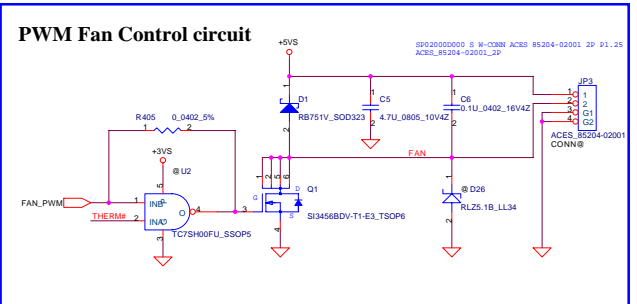
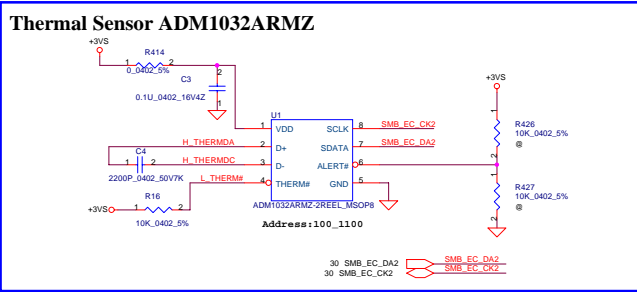
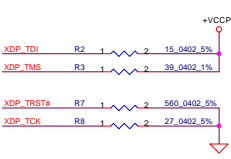
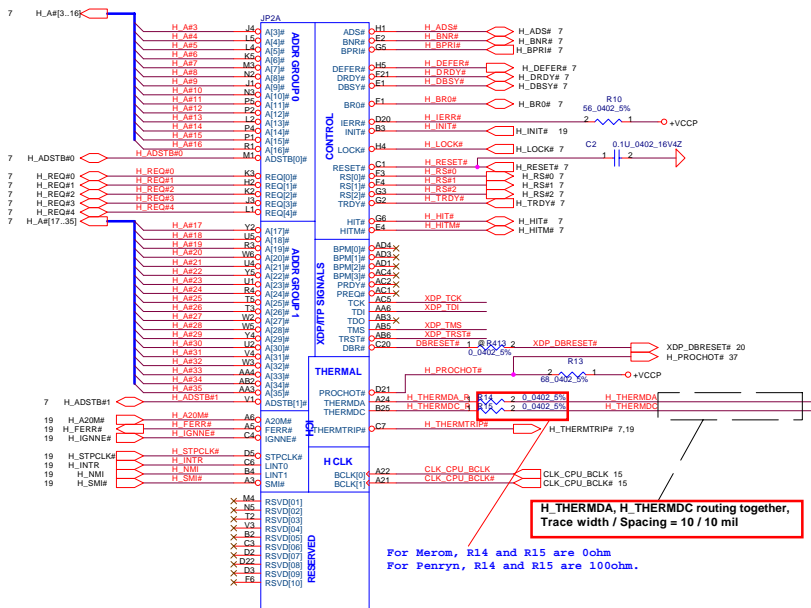
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

**BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader**

**BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader**

**Jump-Short: PJP?**

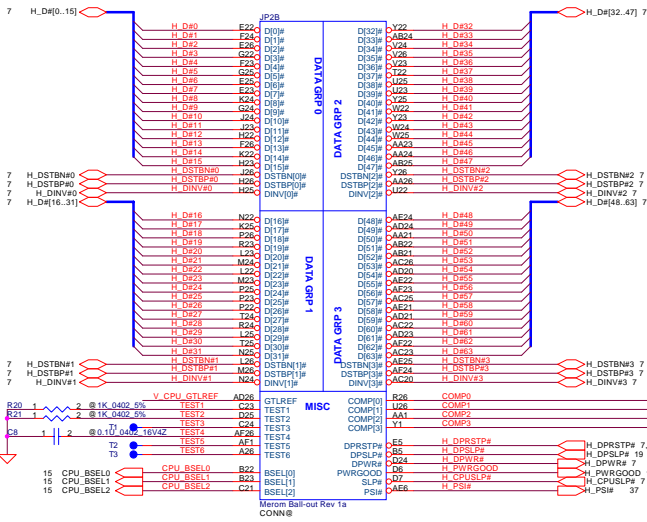
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				Size
				LA-403IP
				1.0
				Date: Wednesday, October 24, 2007 1 Sheet 3 of 42



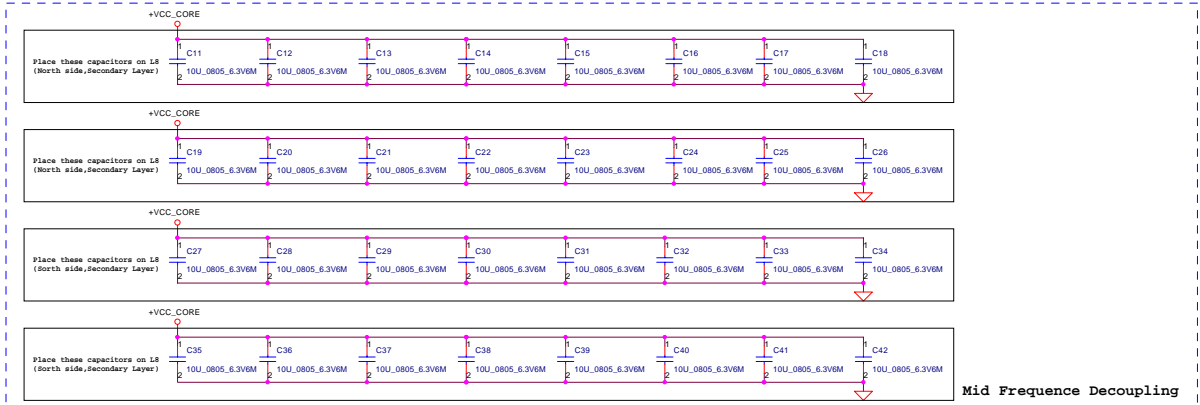
**H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm  
For Penryn, R14 and R15 are 100ohm.

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			Rev 1.0 Sheet 4 of 42

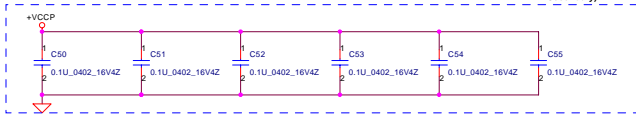
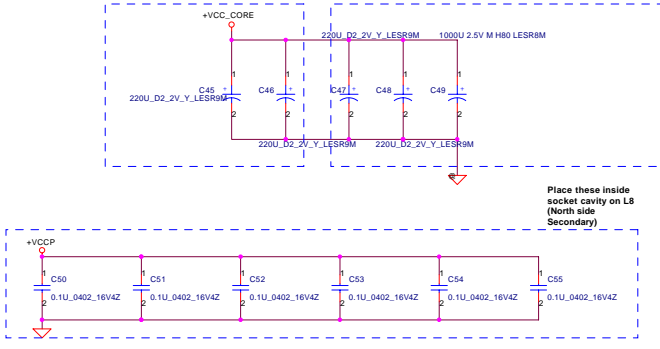


JP2D			
A4	VSS1001	VSS1080	P6
A5	VSS1002	VSS1083	P21
A6	VSS1003	VSS1084	P22
A14	VSS1004	VSS1085	R2
A16	VSS1006	VSS1087	R22
A19	VSS1009	VSS1090	R22
A22	VSS1012	VSS1093	T1
AF2	VSS1077	VSS1088	T1
BB	VSS1008	VSS1089	T4
BB	VSS1009	VSS1090	T4
B11	VSS1011	VSS1092	T26
B13	VSS1012	VSS1093	T27
B18	VSS1013	VSS1094	U6
B19	VSS1014	VSS1095	U2
B21	VSS1016	VSS1097	U24
B24	VSS1019	VSS1100	U2
C2	VSS1017	VSS1098	U2
C2	VSS1018	VSS1099	U22
C14	VSS1020	VSS1101	W1
C19	VSS1021	VSS1102	W2
C19	VSS1022	VSS1103	W22
C22	VSS1023	VSS1104	X3
C22	VSS1024	VSS1105	X3
C22	VSS1025	VSS1106	X3
D1	VSS1026	VSS1107	Y2
D4	VSS1027	VSS1108	Y24
D8	VSS1028	VSS1109	Y2
D11	VSS1029	VSS1110	Y24
D18	VSS1030	VSS1111	AA8
D19	VSS1031	VSS1112	AA14
D23	VSS1032	VSS1113	AA16
D28	VSS1034	VSS1115	AA19
E3	VSS1035	VSS1116	AA22
E8	VSS1036	VSS1117	AA25
E8	VSS1037	VSS1118	AB1
E11	VSS1038	VSS1119	AB4
E14	VSS1039	VSS1120	AB6
E16	VSS1040	VSS1121	AB11
E19	VSS1041	VSS1122	AB13
E21	VSS1042	VSS1123	AB16
E24	VSS1043	VSS1124	AB19
F4	VSS1044	VSS1125	AB23
F8	VSS1045	VSS1126	AB26
F11	VSS1046	VSS1127	AC2
F18	VSS1047	VSS1128	AC6
F19	VSS1048	VSS1129	AC11
F21	VSS1050	VSS1131	AC14
F22	VSS1051	VSS1132	AC16
F25	VSS1052	VSS1133	AC19
G4	VSS1053	VSS1134	AC21
G1	VSS1054	VSS1135	AC24
G2	VSS1055	VSS1136	AD2
G28	VSS1056	VSS1137	AD5
H4	VSS1057	VSS1138	AD8
H6	VSS1058	VSS1139	AD11
H21	VSS1059	VSS1140	AD13
H24	VSS1060	VSS1141	AD16
J2	VSS1061	VSS1142	AD19
J2	VSS1062	VSS1143	AD22
J2	VSS1063	VSS1144	AD25
K5	VSS1064	VSS1145	AE1
K1	VSS1065	VSS1146	AE4
K4	VSS1066	VSS1147	AE8
K29	VSS1067	VSS1148	AE11
K28	VSS1068	VSS1149	AE14
L3	VSS1069	VSS1150	AE16
L6	VSS1070	VSS1151	AE19
L21	VSS1071	VSS1152	AE23
L24	VSS1072	VSS1153	AE26
M2	VSS1073	VSS1154	AF
M5	VSS1074	VSS1155	AF3
M22	VSS1075	VSS1156	AF8
M28	VSS1076	VSS1157	AF11
N1	VSS1077	VSS1158	AF13
N4	VSS1078	VSS1159	AF16
N23	VSS1079	VSS1160	AF19
N28	VSS1080	VSS1161	AF21
P1	VSS1081	VSS1162	AZ2
		VSS1163	AZ5

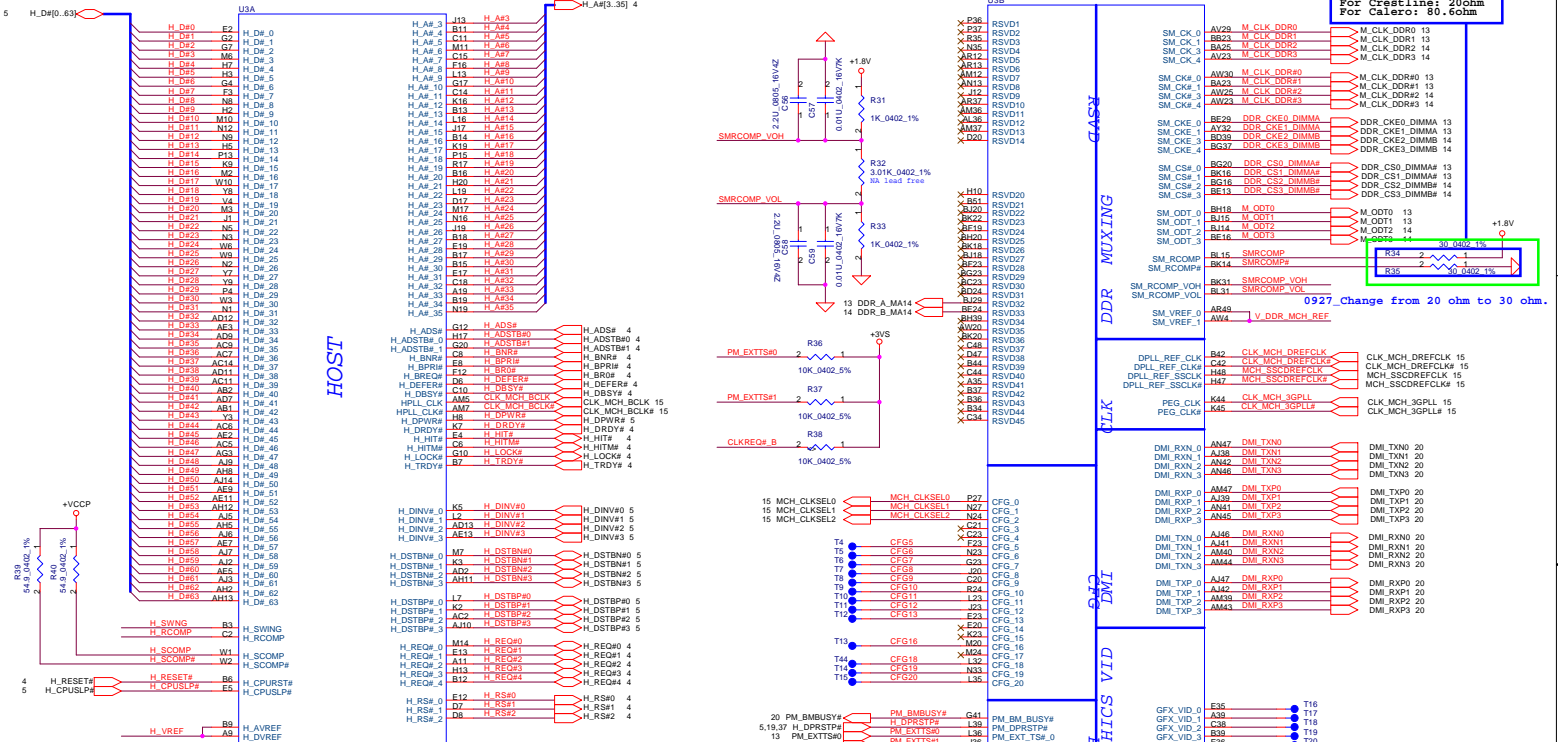


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



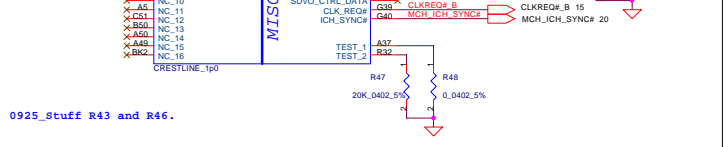
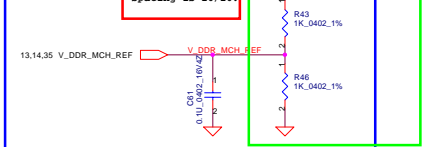
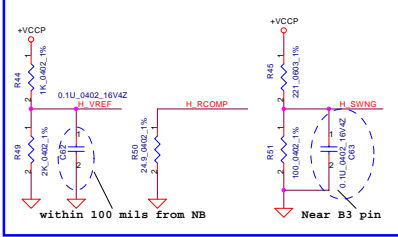
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				Customer	LA-403P
				Date	Wednesday, October 24, 2007
				Sheet	6 of 42
				Rev	1.0



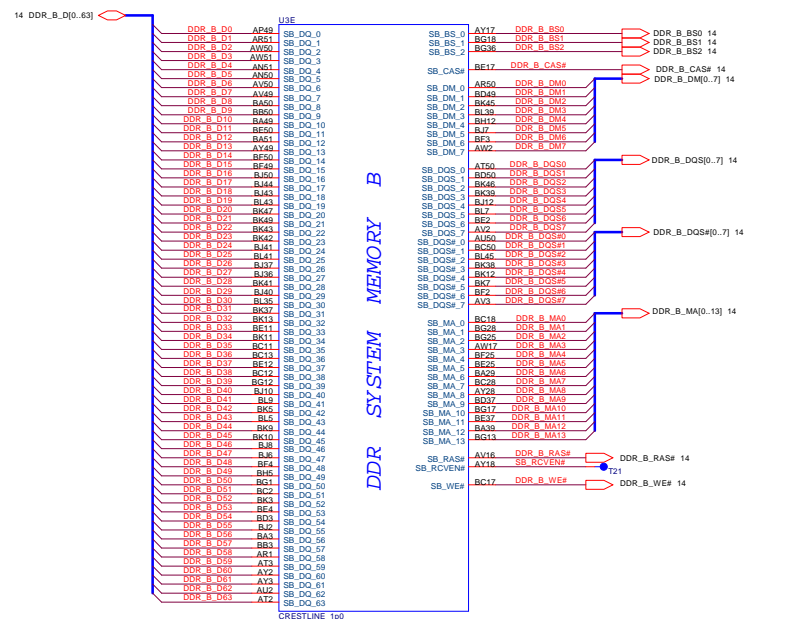
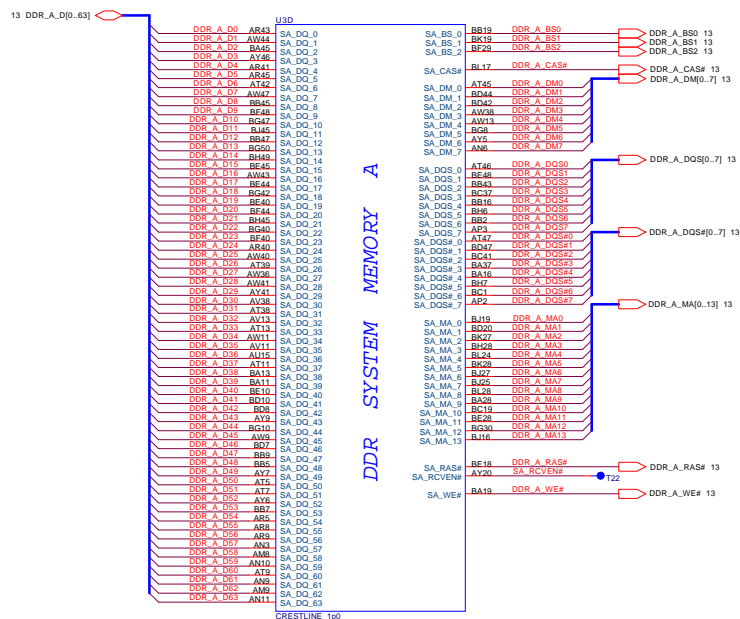
layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as F8B data traces

Layout Note:  
H\_RCMP / H\_VREF / H\_SWNG trace width and spacing is 10/20

Layout Note:  
V\_DDR\_MCH\_REF trace width and spacing is 20/20.



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Customer	LA-403P	Doc Number	719	Rev	1.0
Date	Wednesday, October 24, 2007	Sheet	7	of	42



CRESTLINE\_1p0

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Size	Document Number	Customer	Rev	Date	Sheet
	LA-031P		1.0	Wednesday, October 24, 2007	8 of 42



Strap Pin Table

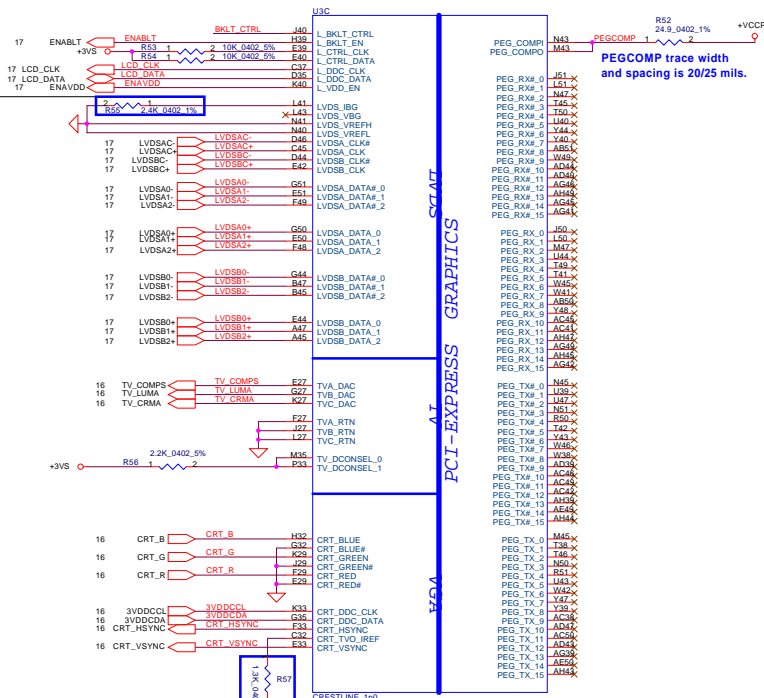
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

For Crestline: 2.4kohm  
For Calero: 1.5kohm

PEGCOMP trace width and spacing is 20/25 mils.

For Crestline: 1.3kohm  
For Calero: 255ohm



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				1.0
Date: Wednesday, October 24, 2007				Sheet 9 of 42

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CRESTLINE(3/6)-VGA/LVDS/TV

Customer: LA-4031P  
Date: Wednesday, October 24, 2007  
Sheet: 9 of 42





U31

A13	VSS_1	AW24
A15	VSS_2	AW23
A17	VSS_3	AW22
A2	VSS_4	AW21
AA21	VSS_5	AW20
AA24	VSS_6	AW19
AA25	VSS_7	AW18
AB20	VSS_8	AW17
AB23	VSS_9	AW16
AB26	VSS_10	AW15
AB28	VSS_11	AW14
AB31	VSS_12	AW13
AC10	VSS_13	AW12
AC13	VSS_14	AW11
AC14	VSS_15	AW10
AC3	VSS_16	AW9
AC43	VSS_17	AW8
AC47	VSS_18	AW7
AD1	VSS_19	AW6
AD21	VSS_20	AW5
AD26	VSS_21	AW4
AD29	VSS_22	AW3
AD3	VSS_23	AW2
AD41	VSS_24	AW1
AD49	VSS_25	
AD5	VSS_26	
AD50	VSS_27	
AE10	VSS_28	
AE14	VSS_29	
AE1	VSS_30	
AE11	VSS_31	
AE12	VSS_32	
AF23	VSS_33	
AF24	VSS_34	
AF3	VSS_35	
AF31	VSS_36	
AG2	VSS_37	
AG38	VSS_38	
AG43	VSS_39	
AG47	VSS_40	
AH3	VSS_41	
AH9	VSS_42	
AH41	VSS_43	
AH9	VSS_44	
AH7	VSS_45	
AI9	VSS_46	
AJ11	VSS_47	
AJ3	VSS_48	
AJ21	VSS_49	
AJ24	VSS_50	
AJ29	VSS_51	
AJ32	VSS_52	
AJ4	VSS_53	
AJ45	VSS_54	
AJ55	VSS_55	
AK20	VSS_56	
AK21	VSS_57	
AK28	VSS_58	
AK29	VSS_59	
AK31	VSS_60	
AK51	VSS_61	
AL1	VSS_62	
AM11	VSS_63	
AM3	VSS_64	
AM4	VSS_65	
AM41	VSS_66	
AN1	VSS_67	
AN45	VSS_68	
AN5	VSS_69	
AN38	VSS_70	
AN39	VSS_71	
AN43	VSS_72	
AN7	VSS_73	
AN7	VSS_74	
AP4	VSS_75	
AP48	VSS_76	
AP50	VSS_77	
AR11	VSS_78	
AR2	VSS_79	
AR29	VSS_80	
AR44	VSS_81	
AR7	VSS_82	
AT10	VSS_84	
AT14	VSS_85	
AT41	VSS_86	
AT6	VSS_87	
AU1	VSS_88	
AU23	VSS_89	
AU2	VSS_90	
AU3	VSS_91	
AU36	VSS_92	
AU49	VSS_93	
AU51	VSS_94	
AU58	VSS_95	
AV48	VSS_96	
AW1	VSS_97	
AW12	VSS_98	
AW16	VSS_99	

VSS

U31

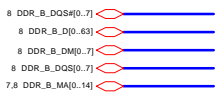
C46	VSS_199	W11
C50	VSS_200	W39
C7	VSS_201	W43
D13	VSS_202	W47
D24	VSS_203	W5
D3	VSS_204	W7
D32	VSS_205	Y13
D39	VSS_206	Y2
D45	VSS_207	Y41
D49	VSS_208	Y46
E10	VSS_209	Y49
E14	VSS_210	Y5
E24	VSS_211	Y50
E28	VSS_212	Y11
E32	VSS_213	Y29
E47	VSS_214	T29
F19	VSS_215	T31
F36	VSS_216	T33
F4	VSS_217	T35
F40	VSS_218	R28
F50	VSS_219	
G1	VSS_220	
G13	VSS_221	VSS_306
G16	VSS_222	AA32
G19	VSS_223	AD32
G24	VSS_224	VSS_308
G28	VSS_225	VSS_309
G29	VSS_226	VSS_310
G30	VSS_227	VSS_311
G42	VSS_228	VSS_312
G46	VSS_229	VSS_313
G48	VSS_230	
G4	VSS_231	
H24	VSS_232	
H28	VSS_233	
H4	VSS_234	
H45	VSS_235	
J11	VSS_236	
J16	VSS_237	
J2	VSS_238	
J24	VSS_239	
J28	VSS_240	
J33	VSS_241	
J36	VSS_242	
J39	VSS_243	
K12	VSS_245	
K47	VSS_246	
L1	VSS_247	
L17	VSS_248	
L20	VSS_249	
L24	VSS_250	
L28	VSS_251	
L3	VSS_252	
L33	VSS_253	
L48	VSS_254	
M28	VSS_255	
M42	VSS_256	
M48	VSS_257	
M49	VSS_258	
M5	VSS_259	
M5	VSS_260	
M50	VSS_261	
M9	VSS_262	
N14	VSS_263	
N17	VSS_264	
N29	VSS_265	
N32	VSS_266	
N33	VSS_267	
N39	VSS_268	
N44	VSS_269	
N49	VSS_270	
N7	VSS_271	
P19	VSS_272	
P2	VSS_273	
P23	VSS_274	
P2	VSS_275	
P3	VSS_276	
P30	VSS_277	
P49	VSS_278	
P59	VSS_279	
T43	VSS_280	
T47	VSS_281	
T47	VSS_282	
U41	VSS_283	
U50	VSS_284	
V2	VSS_285	
V3	VSS_286	

VSS

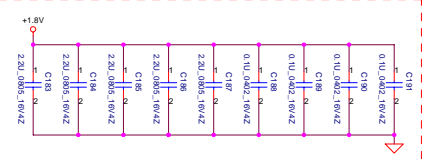
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Date: Wednesday, October 24, 2007				Sheet 12 of 42

Compal Electronics, Inc.  
CRESTLINE((6/6)-PWR/GND

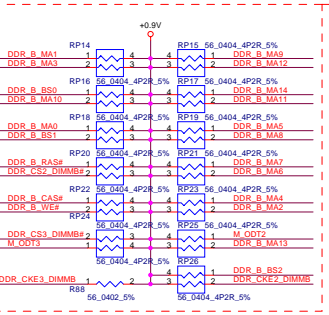
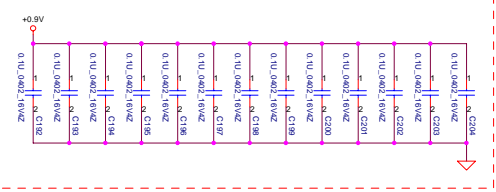




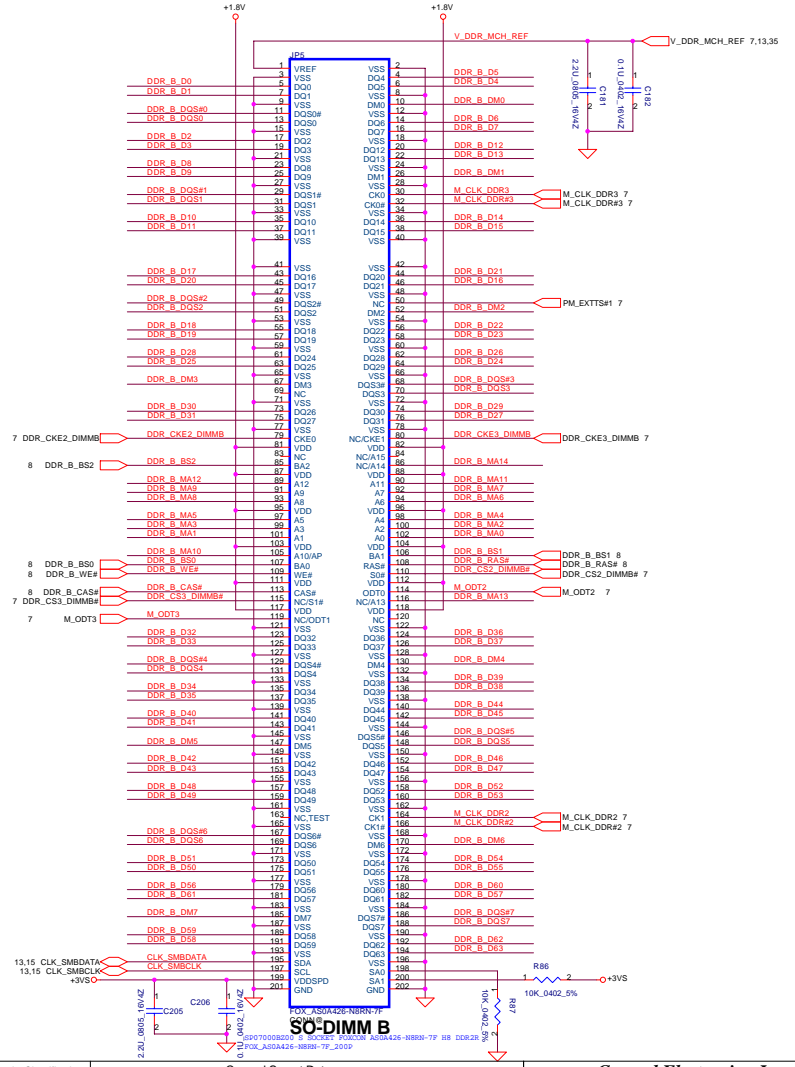
**Layout Note:**  
Place near JP10



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V

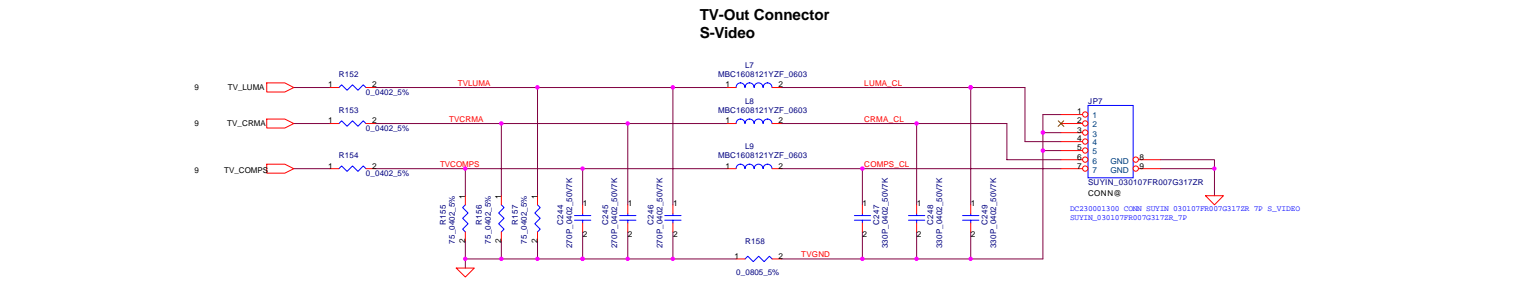
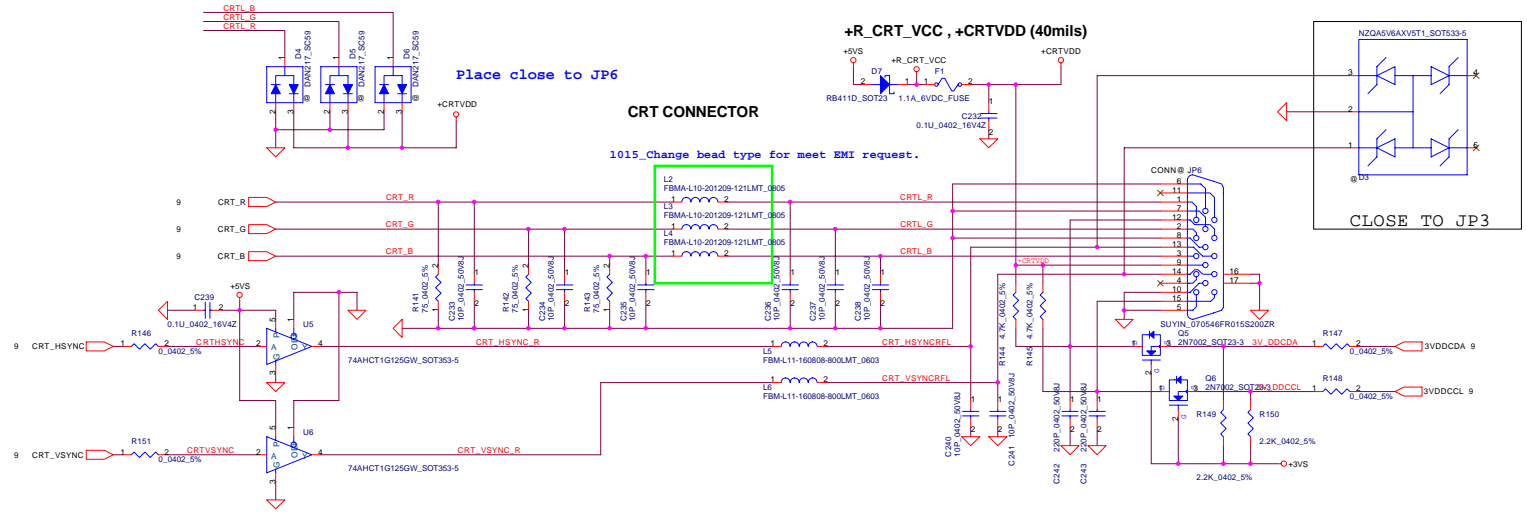


**Layout Note:**  
Place these resistor closely JP10, all trace length Max=1.5"



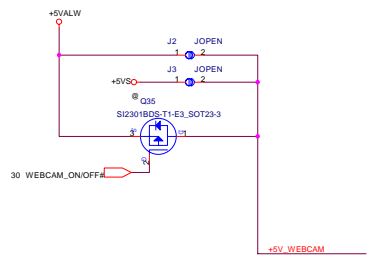
Compal Security Data				Title	
Security Classification	2007/03/26	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT2	
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				LA-4031P	Rev 1.0
				Date	Wednesday, October 24, 2007
				Sheet	14 of 42



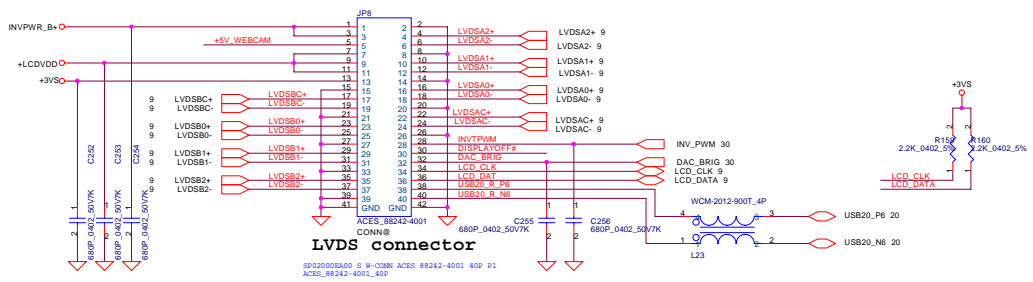
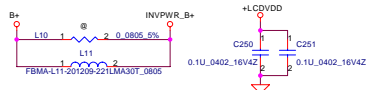


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Issued Date	2007/03/26	Deciphered Date	2006/07/26
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Title			<b>Compal Electronics, Inc.</b>
Size			<b>CRT &amp; TVout Connector</b>
Document Number			<b>LA-4031P</b>
Date	Wednesday, October 24, 2007	Sheet	16 of 42

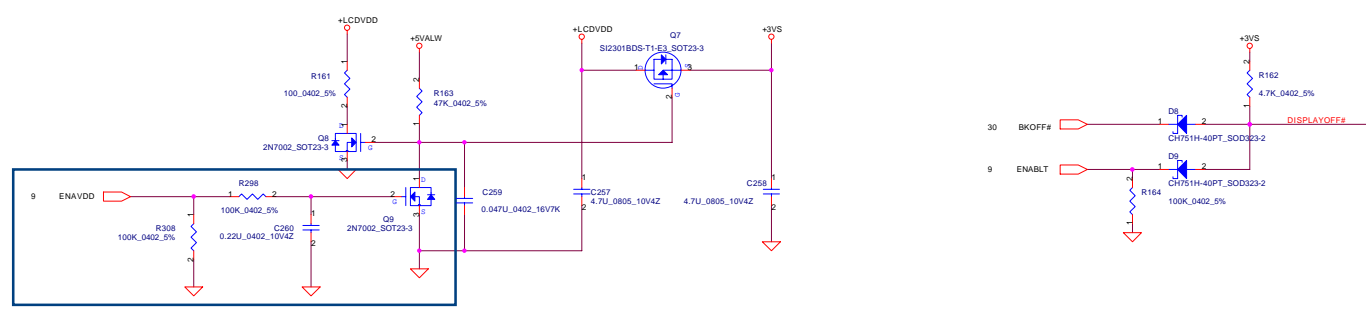




**LVDS CONN**

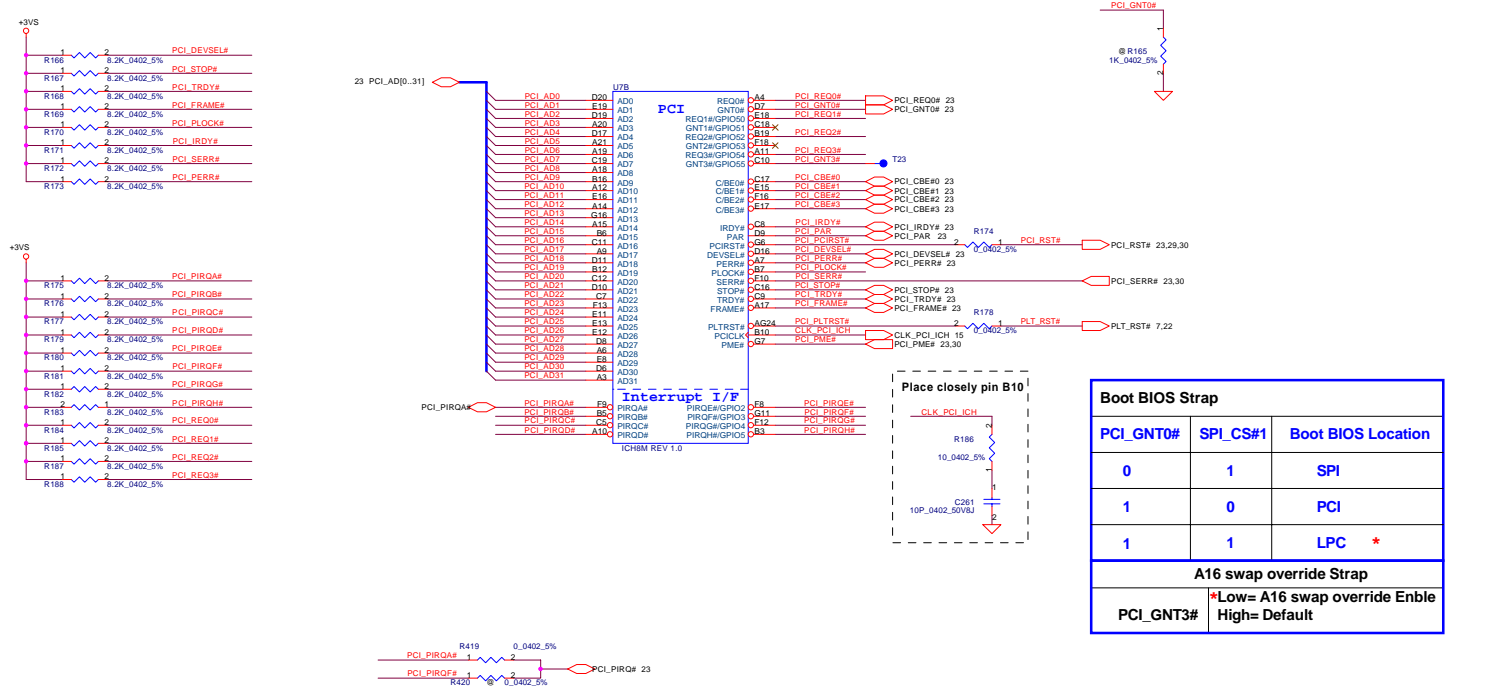


**LVDS connector**  
 ACES\_86242-4001  
 CONN18  
 680P\_0402\_50V7K  
 C255  
 680P\_0402\_50V7K  
 WCM-2012-900T\_4P  
 L23  
 ACES\_86242-4001\_40P P1  
 ACES\_86242-4001\_40P

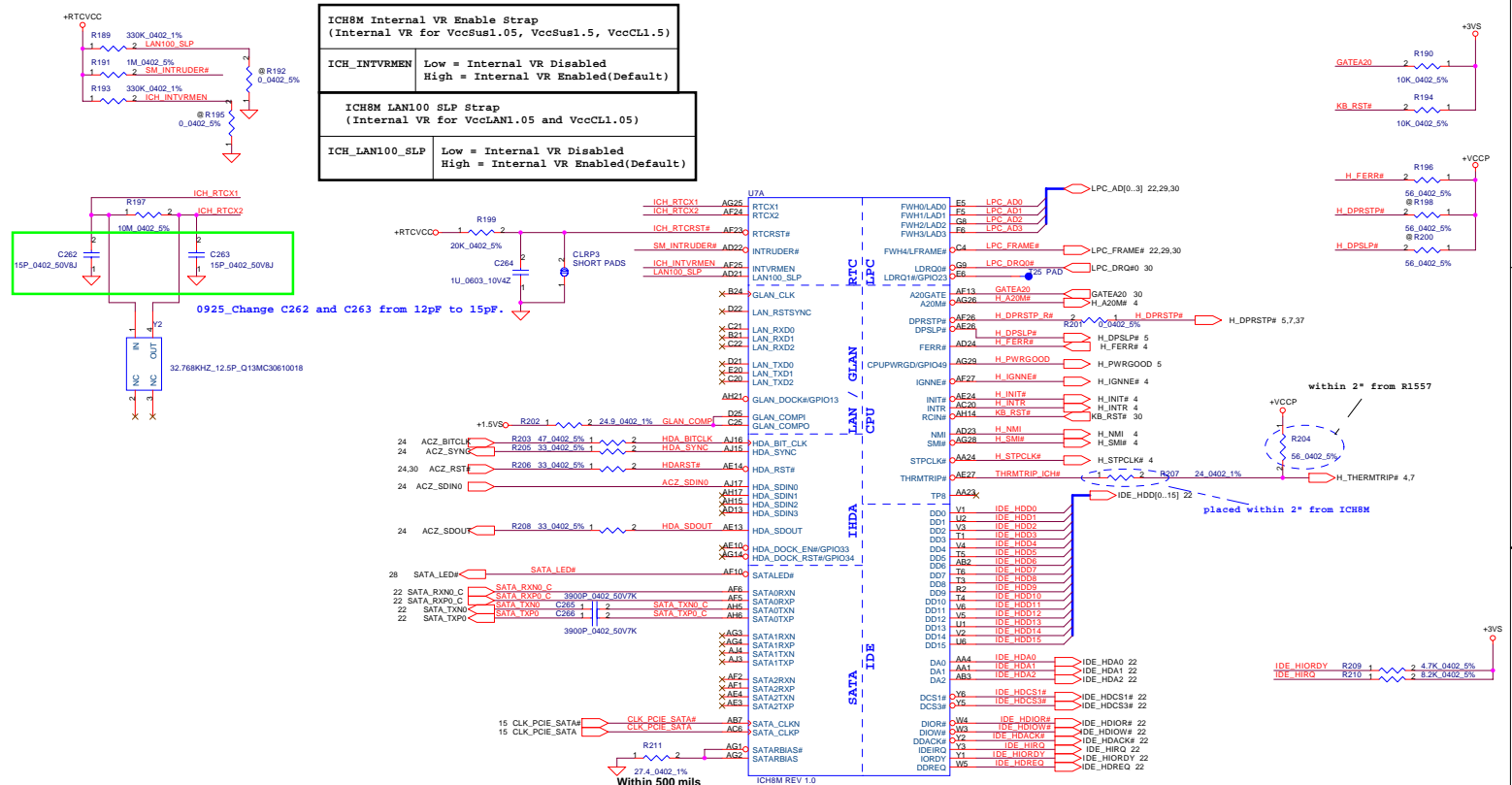


Avoid Panel display garbage after power on.

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Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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Size	Document Number	Rev	Date: Wednesday, October 24, 2007 Sheet 17 of 42		
	LA-403P	1.0			



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				LA-4031P	Rev
Date	Wednesday, October 24, 2007	Sheet	18	of	42



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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer	LA-4031P
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Date	Wednesday, October 24, 2007	Sheet	18	of	42

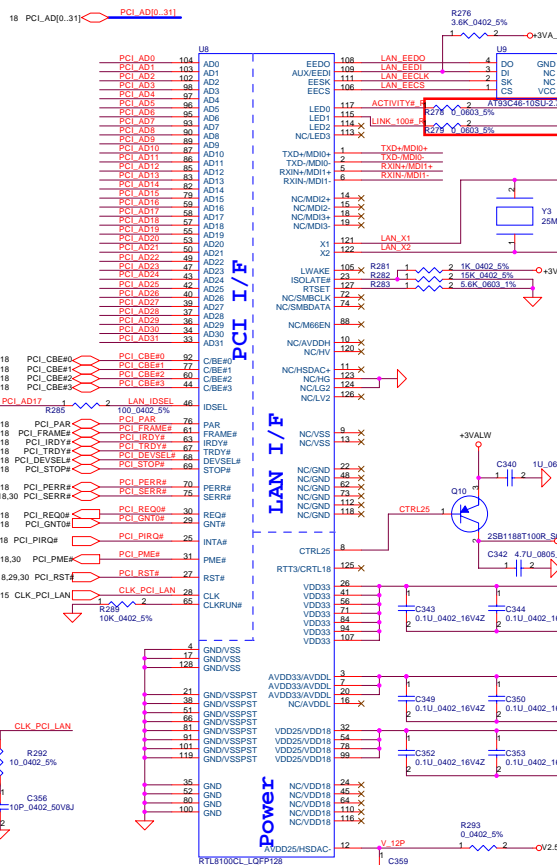
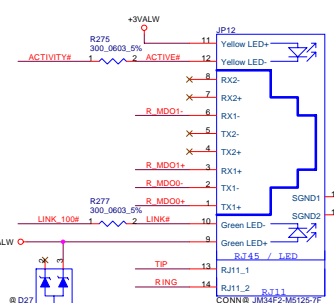
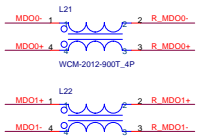
**Compal Electronics, Inc.**  
**ICH8(2/4) LAN,HD,IDE,LPC**







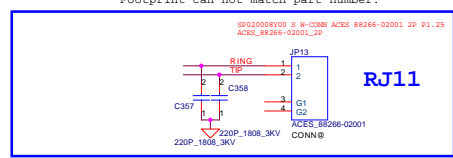
Close to JP12.



For RMI, locate close to LAN chip

close to chip

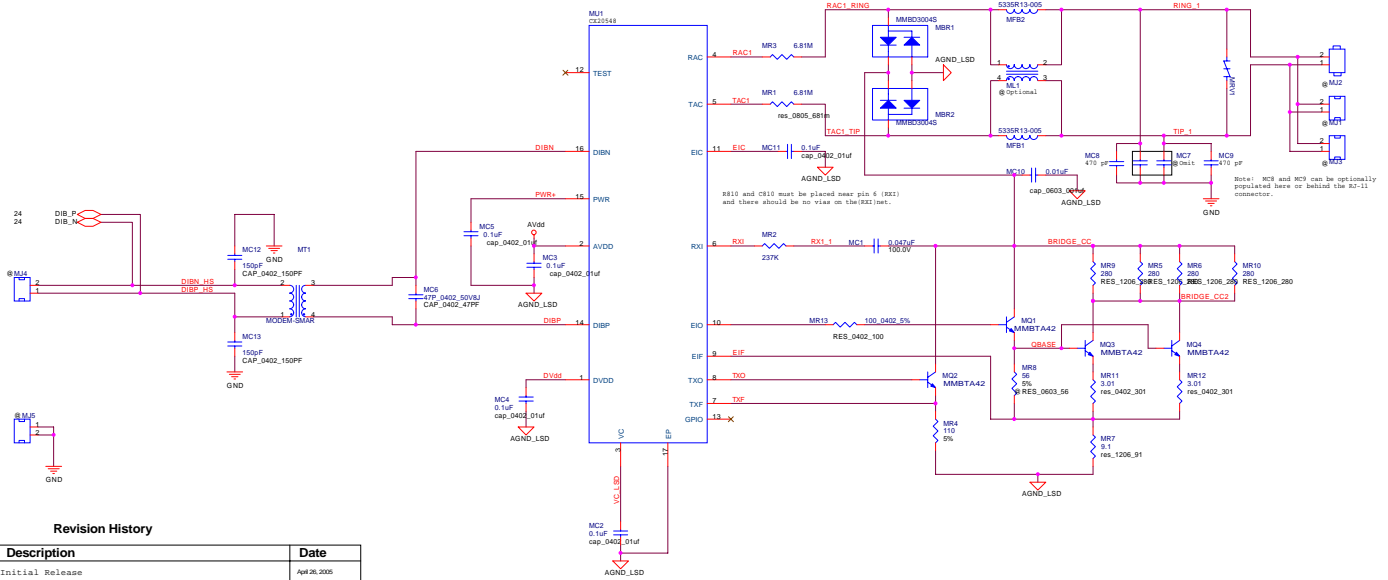
close to magnetic



Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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				LA-403P	Rev 1.0
				Date	Wednesday, October 24, 2007
				Sheet	23 of 42



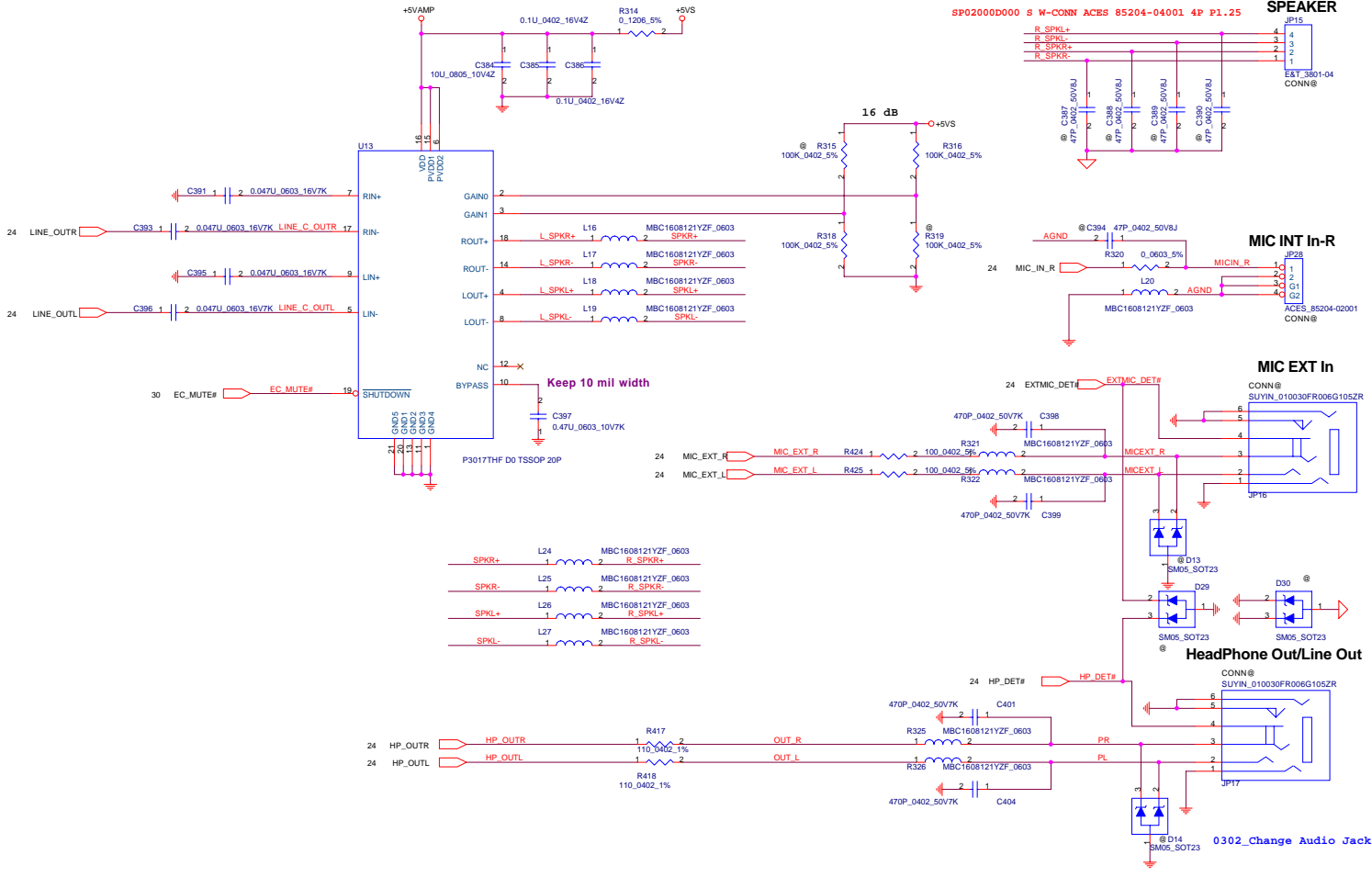




**Revision History**

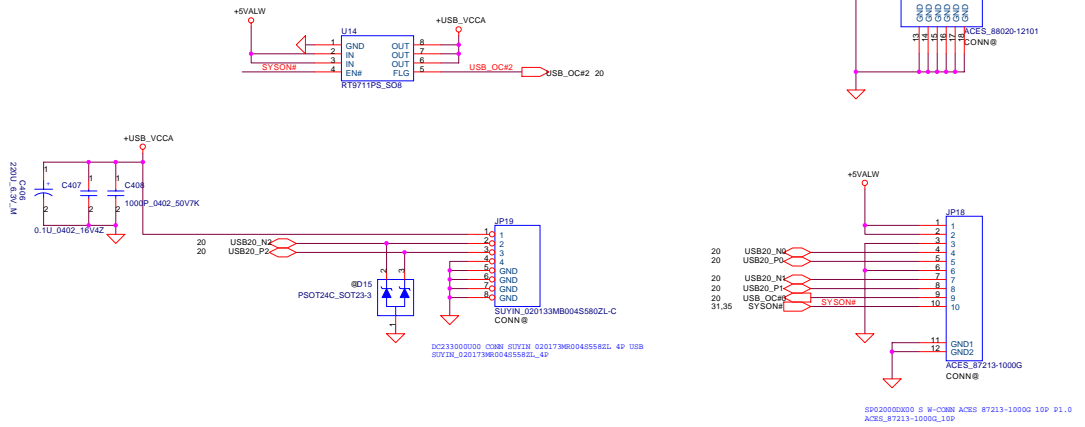
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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	2007/03/26	2007/07/26	Compal Electronics, Inc.
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Doc No.	LA-401P	Rev	1.0
Date	Wednesday, October 24, 2007	Sheet	25 of 42



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				LA-403IP	Rev 1.0
				Date	Wednesday, October 24, 2007
				Sheet	26 of 42

### USB Port

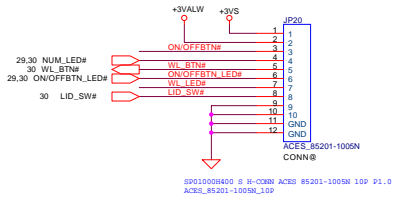


Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Compal Electronics, Inc.
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				Document Number
				LA-403P
				Rev
				1.0
				Date
				Wednesday, October 24, 2007
				Sheet
				27 of 42

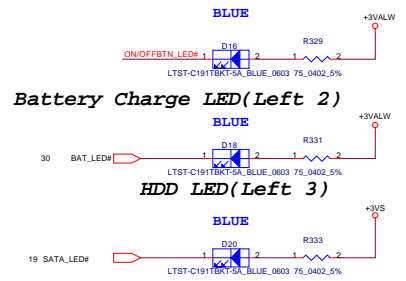
1015\_Remove U22 and U23.



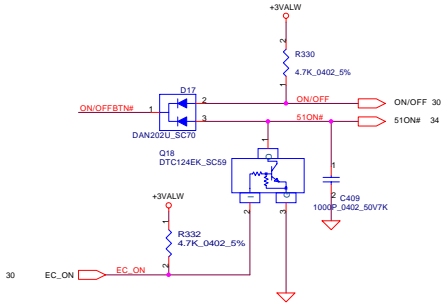
M/BtoS/B



POWER LED(Left 1)

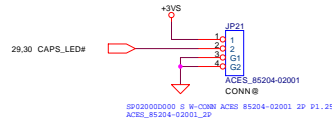


Power ON/OFF

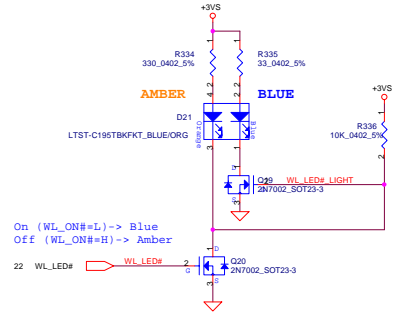


0426\_Change all LED power source from 5V to 3V.

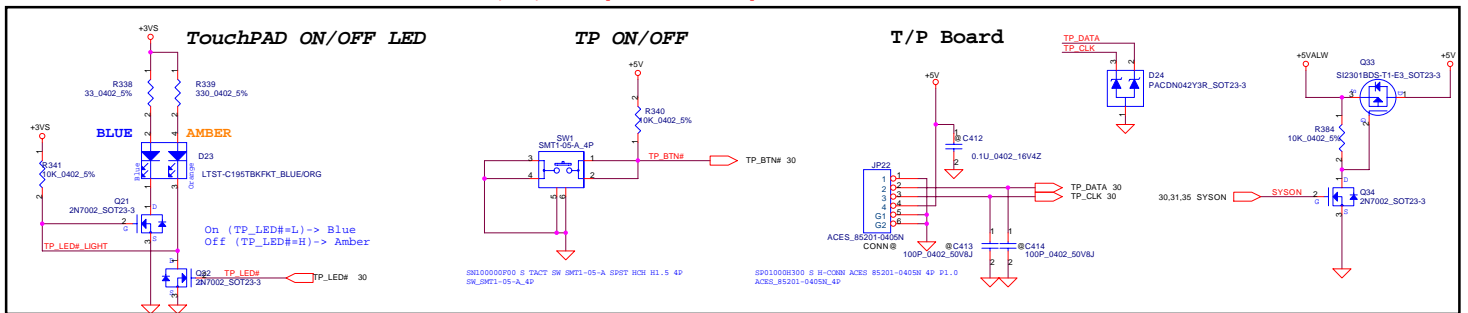
M/B to SB(Caps Lock LED)



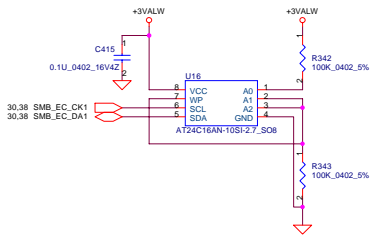
Wireless ON/OFF LED(Left 4)



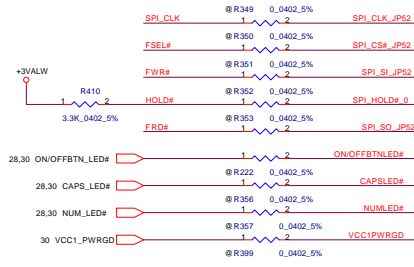
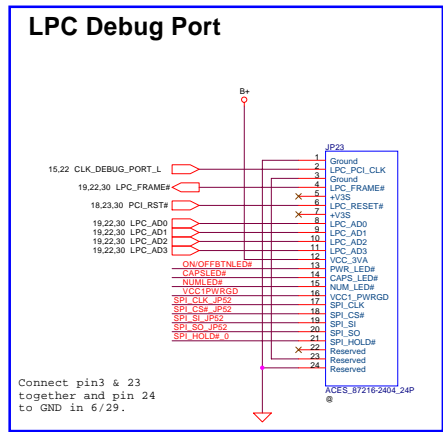
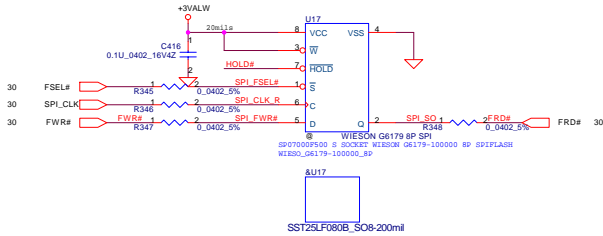
D21, D25, D23 Footprint can not match part number.



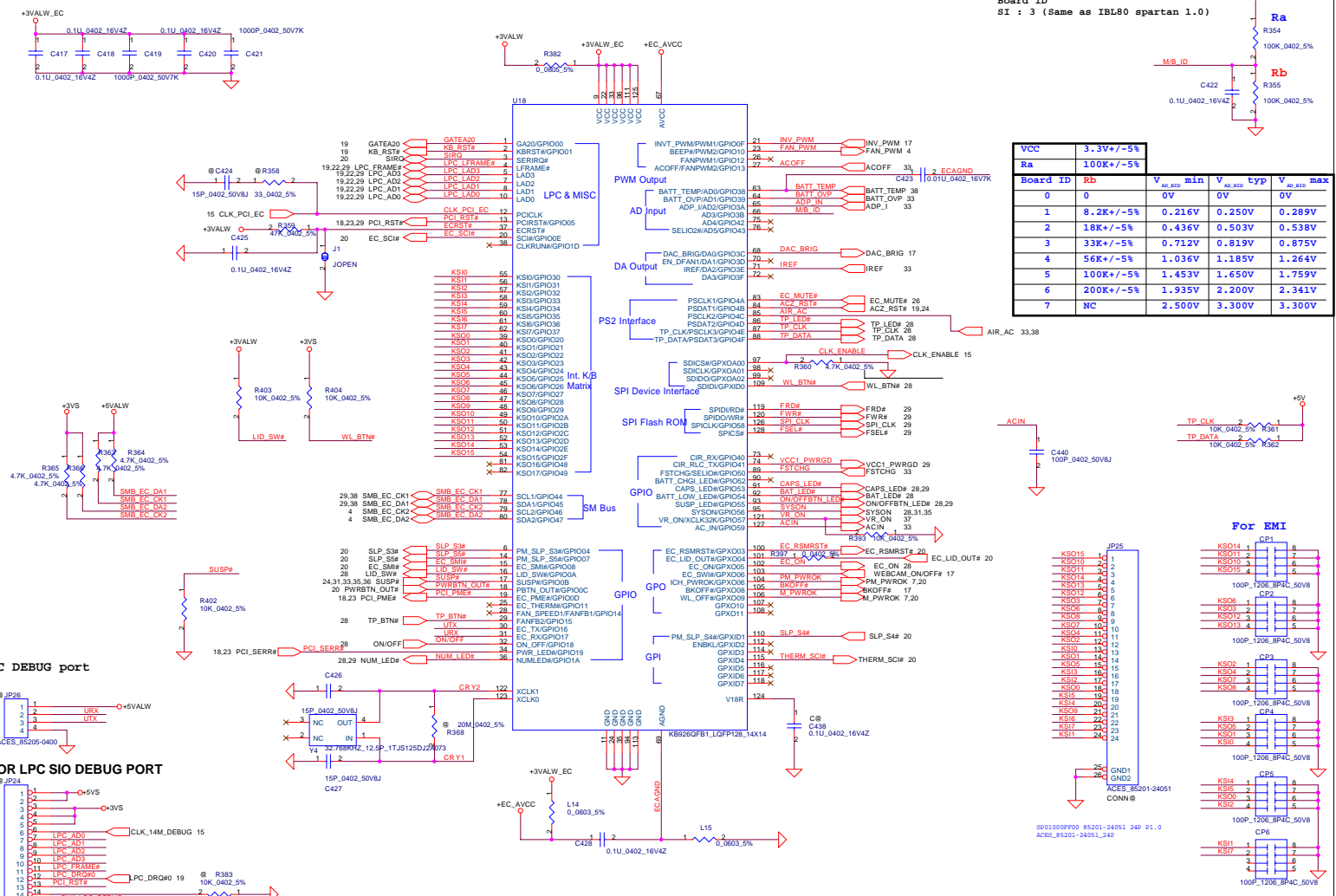
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title
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				Rev: 1.0



**SPI ROM**

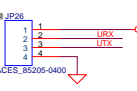


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				Size
Date	Wednesday, October 24, 2007	Sheet	29 of 42	LA-403IP Rev 1.0

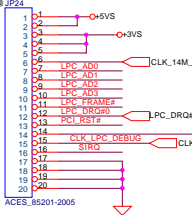


Board ID	Rb	V <sub>AD_MIN</sub>	V <sub>AD_TYP</sub>	V <sub>AD_MAX</sub>
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	1.8K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

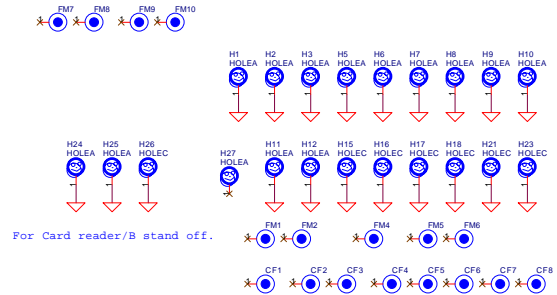
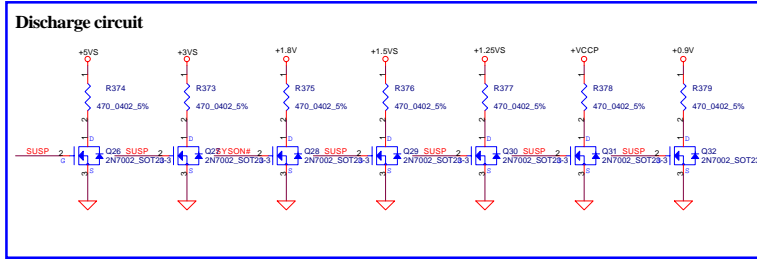
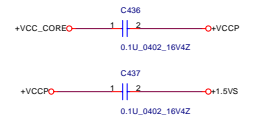
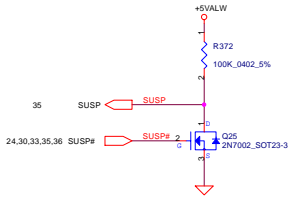
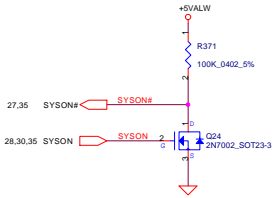
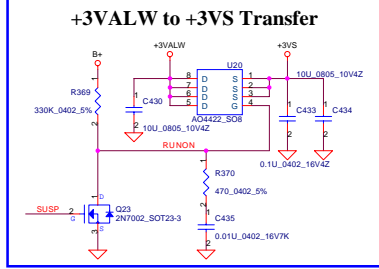
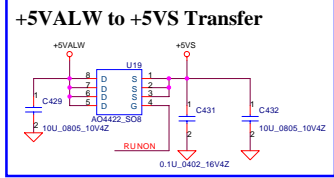
**EC DEBUG port**



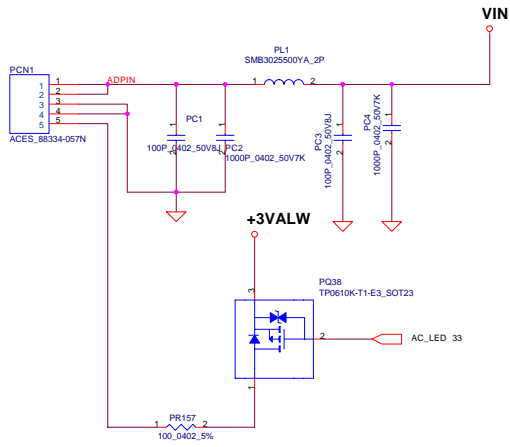
**FOR LPC SIO DEBUG PORT**



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Issued Date	2007/03/26	Deciphered Date	2006/07/26	EC KB926/KB con
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Size	Document Number	LA-401P	Sheet	30 of 42
Date	Wednesday, October 24, 2007	Rev	1.0	

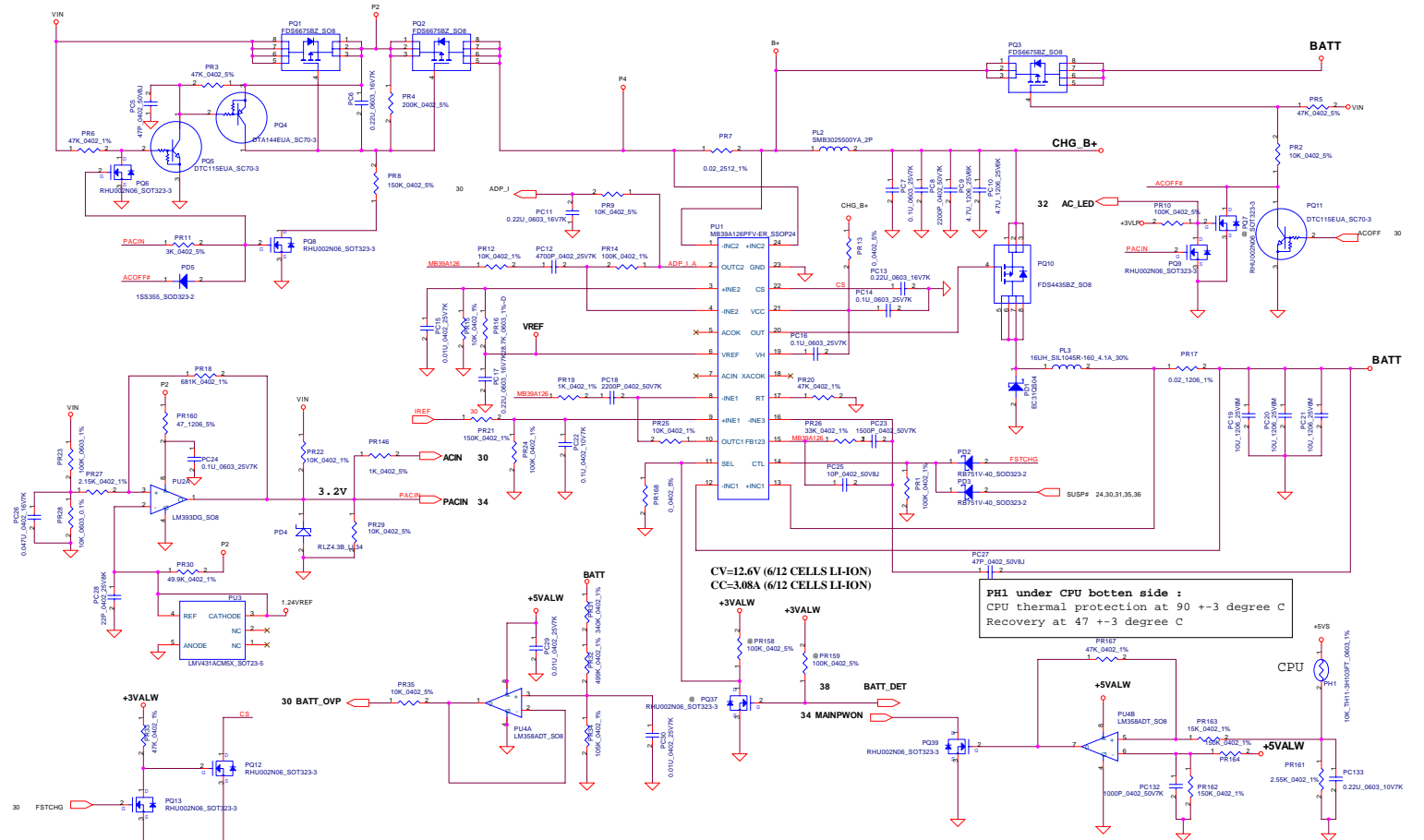


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Size	Document Number	LA-4031P		Rev	1.0
Date	Wednesday, October 24, 2007	Sheet	31	of	42

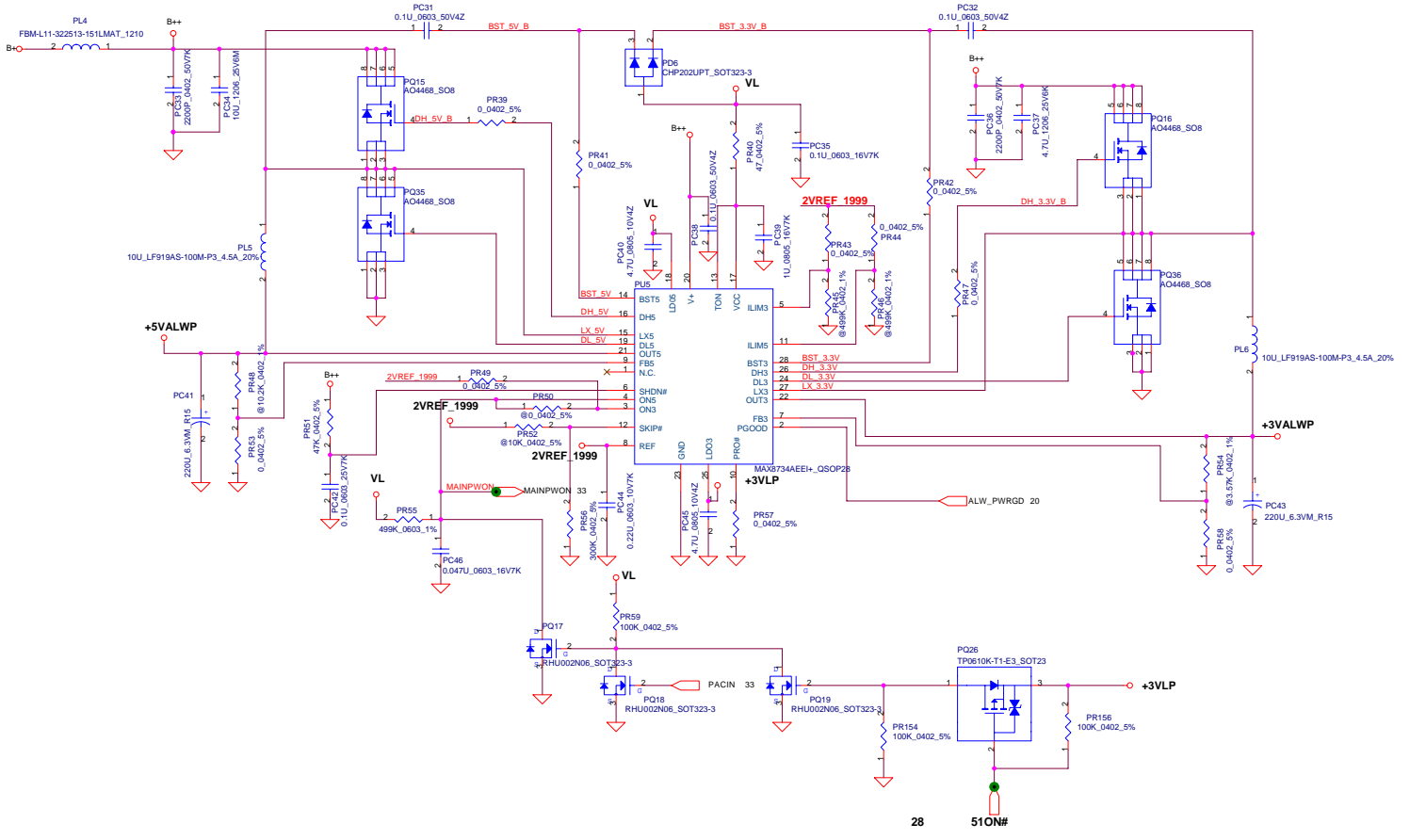


Security Classification	Compal Secret Data			Title
Issued Date	<issued_Date>	Deciphered Date	<Deciphered_Date>	<b>DC CONN</b>
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Date	Wednesday, October 24, 2007	Sheet	32	of 42

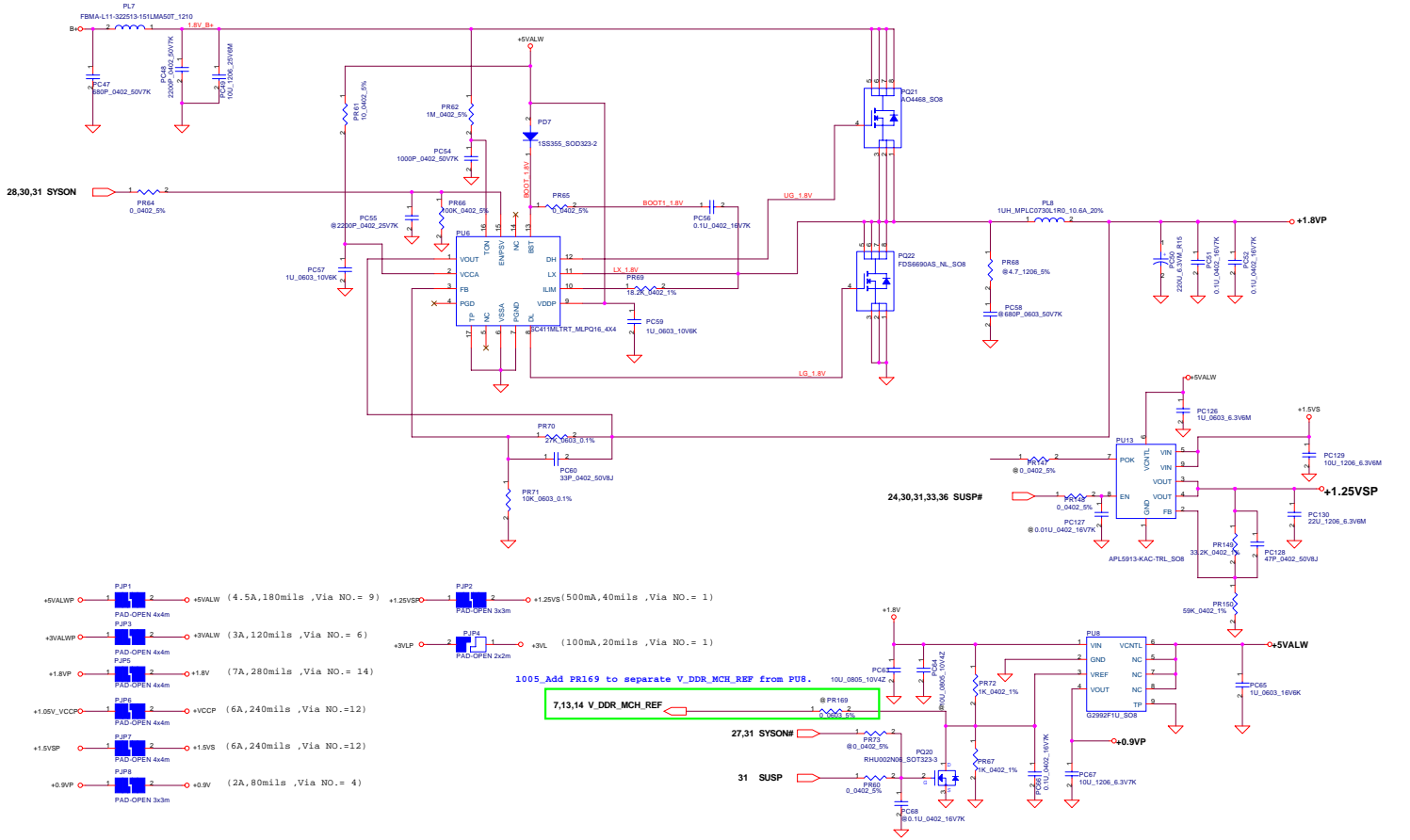




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			DATE	WSP0225EVU_030309 24_0007
			Sheet	53 of 42



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title: 3.3VALWP / 5VALWP	
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Date:	Wednesday, October 24, 2007	Sheet:	34	of 42	



28,30,31 SYSON

24,30,31,33,36 SUSP#

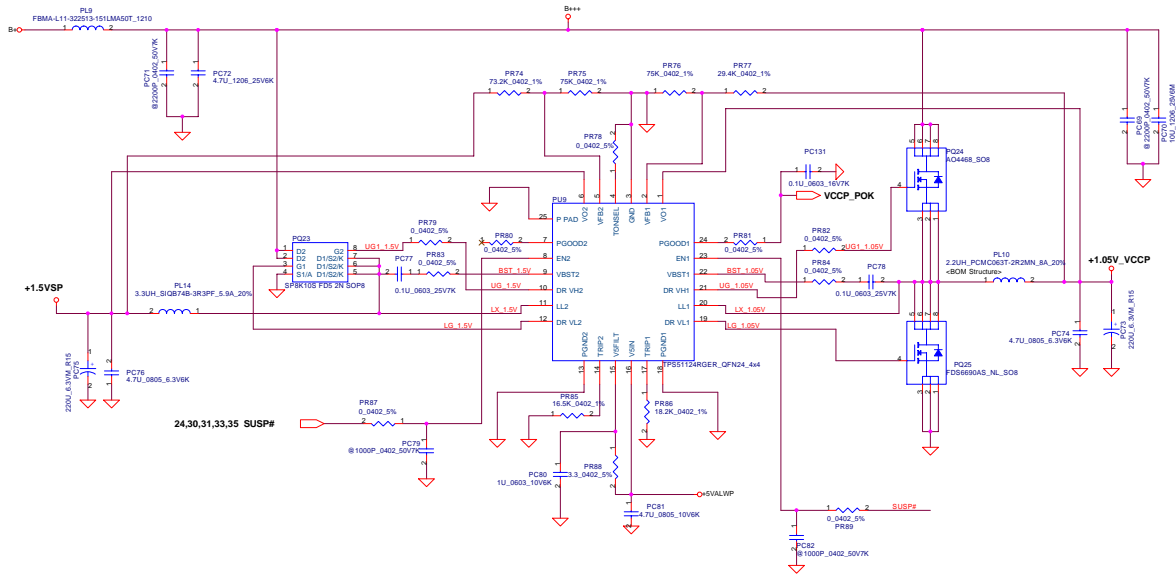
27,31 SYSON#

31 SUSP

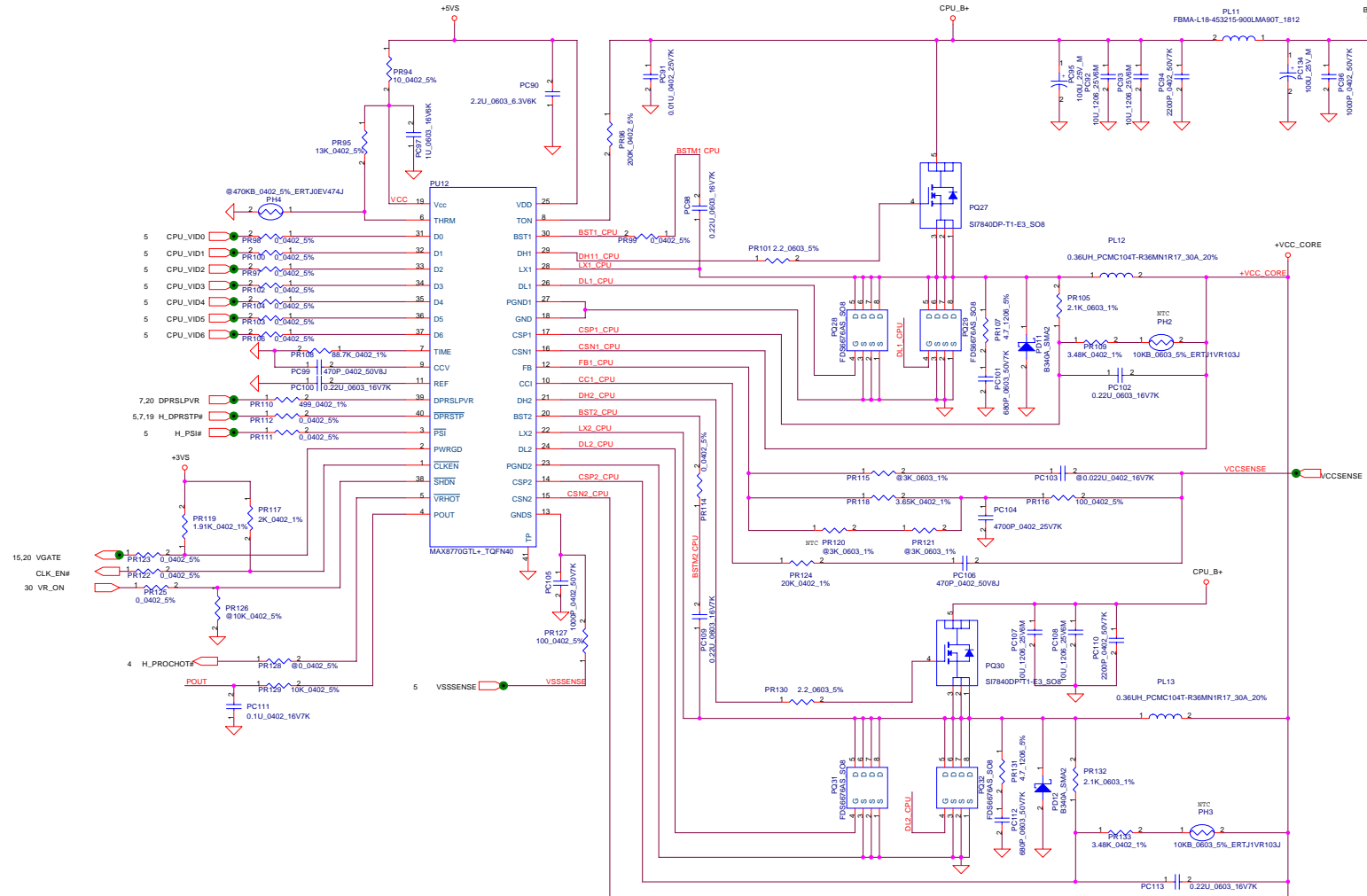
1005\_Add FR169 to separate V\_DDR\_MCH\_REF from PUS.  
7,13,14 V\_DDR\_MCH\_REF

- +5VALWP PJP1 2 +5VALW (4.5A,180mils ,Via NO.= 9)
- +5VALWP PJP2 2 +5VALW (3A,120mils ,Via NO.= 6)
- +1.8VP PJP3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V\_VCCP PJP6 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PJP7 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PJP8 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PJP9 2 +1.25VS (500mA,40mils ,Via NO.= 1)
- +3VP PJP4 1 +3V (100mA,20mils ,Via NO.= 1)

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				Date	Wednesday, October 28, 2009
				Sheet	35 of 49



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Date: Wednesday, October 25, 2006				Sheet: 36 of 42



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File	<b>+CPU CORE</b>	
Site	Document Number	Rev
Client	10KB_0603_5%_ERTJ1VR103J	1.0
Date	Wednesday, October 24, 2007	Sheet 37 of 42



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
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14					

Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/28	Deciphered Date	2007/02/28	<b>Compal Electronics, Inc.</b>
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				Size
Date: Wednesday, October 24, 2007				Sheet 39 of 42

Version Change List ( P. I. R. List ) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
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Security Classification	Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2007/03/26	Deciphered Date	2007/02/28	Title
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Date:	Wednesday, October 24, 2007	Sheet	40	of 42



Version Change List ( P. I. R. List ) for HW Circuit

Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV-->MV
2	Solve wave ripple on CRT and TV.	10	9/25	PV-->MV
3	Solve RTC timing too exceed.	18	9/25	PV-->MV
4	Reduce INT_MIC noise.	24	9/25	PV-->MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV-->MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV-->MV
7	Solve EMI fail for Memory module.	7	9/27	PV-->MV
8	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV-->MV
9	Remove U22 and U23.	28	10/15	PV-->MV
10	For EMI request.	16	10/15	PV-->MV
11	To avoid too easy to open solder for CLRP2.	15	10/15	PV-->MV
12	Solve acoustic noise issue.	10	10/22	PV-->MV
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Date:	Wednesday, October 24, 2007	Sheet	41	of 42

