UT12 SYSTEM DIAGRAM

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 7,8
DDRII-SODIMM2 PAGE 7,8
DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E

PCI-Express 16X

NORTH BRIDGE
RX781 / RS780MN
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

M96-SCE A11
64 Bit,DDR3*8
PAGE 17,18,19
20,21,22

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

Cable Docking PAGE 37
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

X1 LAN
Realtek PCIE-LAN
RTL8102E/8111C
(10/100/GagaLAN)
PAGE 31,32

X1 Express Card
(NEW CARD)
PAGE 33

X3 Mini PCI-E Card
(Wireless LAN/TV TUNNER)
PAGE 36

RJ45 PAGE 31

ALINK X4

USB2.0

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

1,8,9 USB2.0 Ports X3 PAGE 30
5 Blueflame PAGE 30
2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30

SATA0,1 150MB
TWO SATA - HDD PAGE 33

SATA0 150MB
SATA - CD-ROM PAGE 33

SATA4 150MB
E-SATA PAGE 30

Azalia

SMBUS

LPC

Accelerometer
LIS3LV02DL PAGE 28

Keyboard PAGE 34
Touch Pad PAGE 34

CIR (AUDIO CONN) PAGE 27

Capacitive Sense SW PAGE 34

ENE KBC
KB3926 Cx
PAGE 35

FAN PAGE 37

SPI PAGE 35

MDC CONN PAGE 29

IDT 92HD71B7 PAGE 27

AUDIO Amplifier TPA6017A2 PAGE 28

Digital MIC PAGE 30

AUDIO CONN (Phone/ MIC) PAGE 27

Audio Conn PAGE 28

SYSTEM CHARGER(ISL6251A) PAGE 44

SYSTEM POWER ISL6236IRZA-T PAGE 38

DDR II SMDDR_VTERM
1.8V/1.8VSUS(TPS51116REGR) PAGE 41

VCCP +1.1V AND +1.2V(MAX8717) PAGE 39

VGACORE(1.1V~1.2V)Oz8118 PAGE 42

CPU CORE ISL6265A PAGE 40

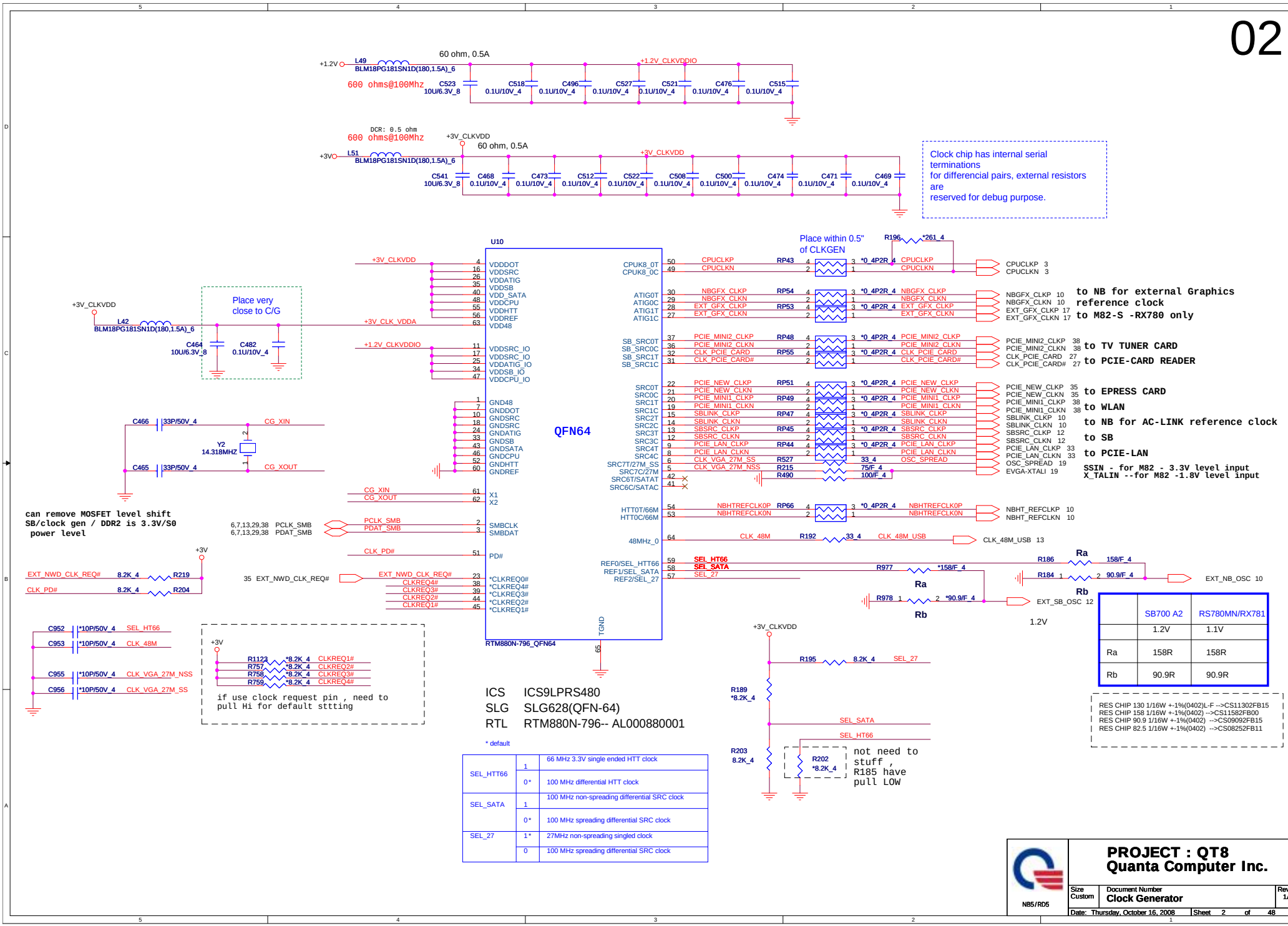
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Thursday, October 16, 2008 Sheet 1 of 48

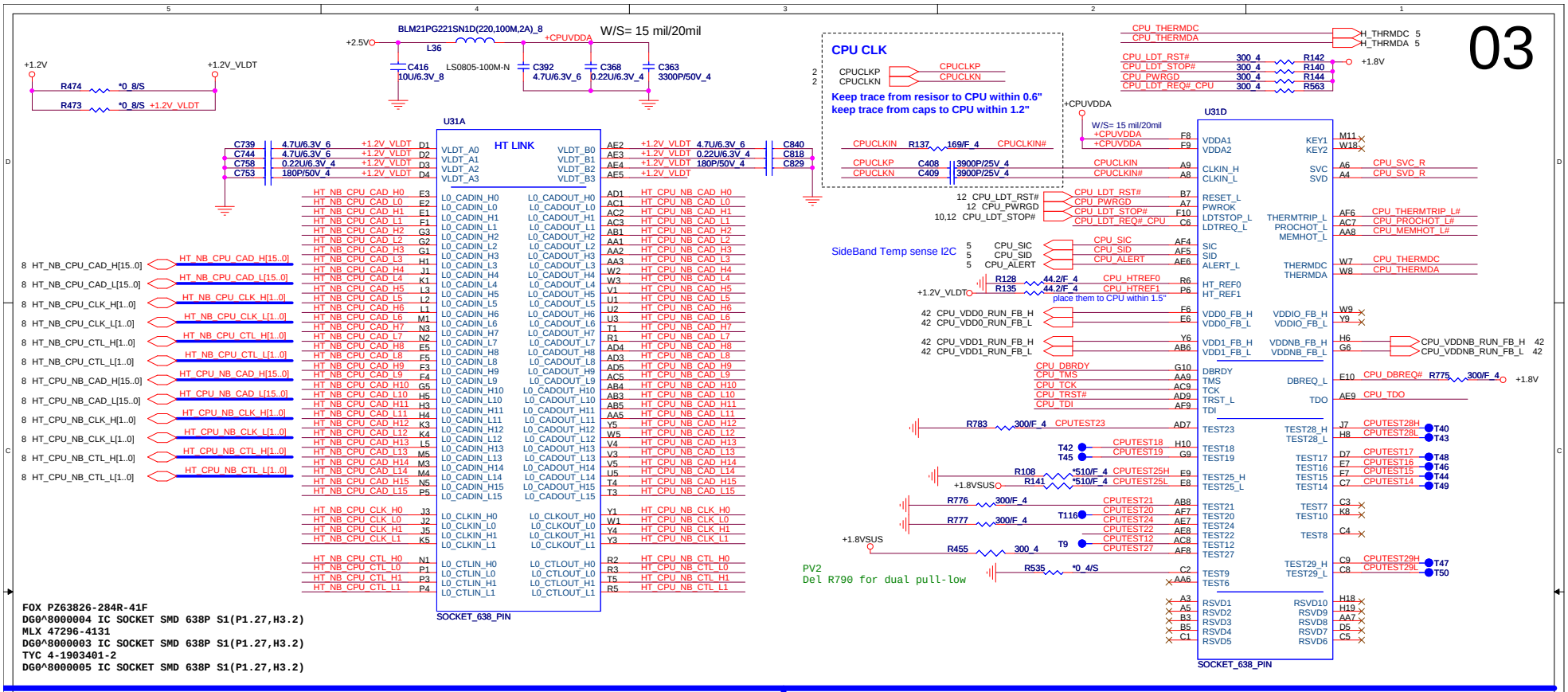


NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

Date: Thursday, October 16, 2008 Sheet 2 of 48



Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

Place close to socket

Close to CPU within 1500 mils

U31B

U31C

SOCKET_638_PIN

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	S1G2 DDRII MEMORY I/F 2/3	1A

Date: Thursday, October 16, 2008 Sheet 4 of 48

05

PROCESSOR POWER AND GROUND

BOTTOM SIDE DECOUPLING

+VCORE0: C287 22U/6.3V_8, C308 22U/6.3V_8, C307 22U/6.3V_8, C306 22U/6.3V_8, C285 0.22U/6.3V_4, C286 0.01U/16V_4, C301 180P/50V_4

+VCORE1: C230 22U/6.3V_8, C272 22U/6.3V_8, C273 22U/6.3V_8, C267 22U/6.3V_8, C206 0.22U/6.3V_4, C226 0.01U/16V_4, C205 180P/50V_4, C225 0.01U/16V_4

+CPUVDDNB: C264 22U/6.3V_8, C231 22U/6.3V_8, C279 22U/6.3V_8

+1.8VSUS: C248 22U/6.3V_8, C284 22U/6.3V_8, C309 0.22U/6.3V_4, C247 0.22U/6.3V_4, C214 180P/50V_4, C315 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.8VSUS: C750 4.7U/6.3V_6, C802 4.7U/6.3V_6, C236 4.7U/6.3V_6, C749 4.7U/6.3V_6, C803 0.22U/6.3V_4, C240 0.22U/6.3V_4

+1.8VSUS: C238 0.22U/6.3V_4, C751 0.22U/6.3V_4, C752 0.01U/16V_4, C120 0.01U/16V_4, C118 180P/50V_4

U31E SOCKET_638_PIN

+VCORE0: VDD0_1 G4, VDD0_2 H2, VDD0_3 J9, VDD0_4 J11, VDD0_5 J13, VDD0_6 J15, VDD0_7 K6, VDD0_8 K10, VDD0_9 K12, VDD0_10 K14, VDD0_11 L4, VDD0_12 L7, VDD0_13 L9, VDD0_14 L11, VDD0_15 L13, VDD0_16 L15, VDD0_17 M2, VDD0_18 M6, VDD0_19 M8, VDD0_20 M10, VDD0_21 N7, VDD0_22 N9, VDD0_23 N11

+VCORE1: VDD1_1 P8, VDD1_2 P10, VDD1_3 R4, VDD1_4 R7, VDD1_5 R9, VDD1_6 R11, VDD1_7 T2, VDD1_8 T6, VDD1_9 T8, VDD1_10 T10, VDD1_11 T12, VDD1_12 T14, VDD1_13 U7, VDD1_14 U9, VDD1_15 U11, VDD1_16 U13, VDD1_17 U15, VDD1_18 V6, VDD1_19 V8, VDD1_20 V10, VDD1_21 V12, VDD1_22 V14, VDD1_23 W4, VDD1_24 Y2, VDD1_25 AC4, VDD1_26 AD2

+CPUVDDNB 3A: VDDNB_1 K16, VDDNB_2 M16, VDDNB_3 P16, VDDNB_4 T16, VDDNB_5 V16

+1.8VSUS 2A: VDDIO1 H25, VDDIO2 J17, VDDIO3 K18, VDDIO4 K21, VDDIO5 K23, VDDIO6 K25, VDDIO7 L17, VDDIO8 M18, VDDIO9 M21, VDDIO10 M23, VDDIO11 M25, VDDIO12 N17

+1.8VSUS: VDDIO13 P18, VDDIO14 P21, VDDIO15 P23, VDDIO16 P25, VDDIO17 R17, VDDIO18 T18, VDDIO19 T21, VDDIO20 T23, VDDIO21 T25, VDDIO22 U17, VDDIO23 V18, VDDIO24 V21, VDDIO25 V23, VDDIO26 V25, VDDIO27 Y25

U31F SOCKET_638_PIN

VSS1 AA4, VSS2 AA11, VSS3 AA13, VSS4 AA15, VSS5 AA17, VSS6 AA19, VSS7 AB2, VSS8 AB7, VSS9 AB9, VSS10 AB23, VSS11 AB25, VSS12 AC11, VSS13 AC13, VSS14 AC15, VSS15 AC17, VSS16 AC19, VSS17 AC21, VSS18 AD6, VSS19 AD8, VSS20 AD25, VSS21 AE11, VSS22 AE13, VSS23 AE15, VSS24 AE17, VSS25 AE19, VSS26 AE21, VSS27 AE23, VSS28 B4, VSS29 B6, VSS30 B8, VSS31 B9, VSS32 B11, VSS33 B13, VSS34 B15, VSS35 B17, VSS36 B19, VSS37 B21, VSS38 B23, VSS39 B25, VSS40 D6, VSS41 D8, VSS42 D9, VSS43 D11, VSS44 D13, VSS45 D15, VSS46 D17, VSS47 D19, VSS48 D21, VSS49 D23, VSS50 D25, VSS51 E4, VSS52 F2, VSS53 F11, VSS54 F13, VSS55 F15, VSS56 F17, VSS57 F19, VSS58 F21, VSS59 F23, VSS60 F25, VSS61 H7, VSS62 H9, VSS63 H21, VSS64 H23, VSS65 J4

VSS66 J6, VSS67 J8, VSS68 J10, VSS69 J12, VSS70 J14, VSS71 J16, VSS72 J18, VSS73 K2, VSS74 K7, VSS75 K9, VSS76 K11, VSS77 K13, VSS78 K15, VSS79 K17, VSS80 L6, VSS81 L8, VSS82 L10, VSS83 L12, VSS84 L14, VSS85 L16, VSS86 L18, VSS87 M7, VSS88 M9, VSS89 AC6, VSS90 M17, VSS91 N4, VSS92 N8, VSS93 N10, VSS94 N16, VSS95 N18, VSS96 P2, VSS97 P7, VSS98 P9, VSS99 P11, VSS100 P17, VSS101 R8, VSS102 R10, VSS103 R16, VSS104 R18, VSS105 T7, VSS106 T9, VSS107 T11, VSS108 T13, VSS109 T15, VSS110 T17, VSS111 U4, VSS112 U6, VSS113 U8, VSS114 U10, VSS115 U12, VSS116 U14, VSS117 U16, VSS118 U18, VSS119 V2, VSS120 V7, VSS121 V9, VSS122 V11, VSS123 V13, VSS124 V15, VSS125 V17, VSS126 W6, VSS127 Y21, VSS128 Y23, VSS129 N6

+1.8VSUS: R164 390_4, R166 390_4, R167 1K/F_4

3 CNTR_VREF

21,37 MBCLK2 — MBCLK2 — Q14 *BSS138_NL/SOT23 — CPU_SIC — CPU_SIC 3

21,37 MBDATA2 — MBDATA2 — Q15 *BSS138_NL/SOT23 — CPU_SID — CPU_SID 3

SMBALERT# — Q13 *BSS138_NL/SOT23 — CPU_ALERT — CPU_ALERT 3

+3V: R149 10K/F_4, R151 10K/F_4, R148 10K/F_4

U36 G786P8 MSOP: SCLK, SDA, ALERT#, OVERT#, VCC, DXP, DXN, GND

21,37 MBCLK2, 21,37 MBDATA2, 13 PM_THERM#

+3V: R572 200/F_6, C856 0.1U/10V_4, C855 1000P/50V_4

H_THRMDA 3, H_THRMDC 3

reserve for power shutdown (if can)

R170 *0_4 — SYS_SHDN# — SYS_SHDN# 40,46

D34 *CH500H

R168 *0_4/S — 3920_RST# — 3920_RST# 37,46

Q16 MMBT3904 — D33 CH501H-40PT — ECPWROK — ECPWROK 16,37

R172 10K/F_4 — +3V

SMBALERT#

+1.8VSUS: R805 *10K/F_4 — Q71 *MMBT3904 — 3 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — SMBALERT#

PQ60 *2N7002E-G — R760 *10K/F_4 — TEMP_FAIL 19

ADD VGA TEMP_ FAIL function
M8X is active Hi , M7X acvite Low

+3VS5: EC13 *0.1U/10V_4, EC14 *0.1U/10V_4

+1.8V: EC12 *0.1U/10V_4

+1.8VSUS: EC10 0.01U/16V_4 — +3VPCU

+1.8V: EC5 0.01U/16V_4 — +3VPCU

+1.8V: EC4 0.01U/16V_4 — +3V

+3VPCU: EC7 0.01U/16V_4 — +3V

+5V: EC1 *0.01U/16V_4, EC2 *0.01U/16V_4 — +3V

+VGA_CORE: EC8 0.01U/16V_4, EC9 0.01U/16V_4 — +1.8V

For fix HyperTransport nets across plane splits

+VCORE0: C69 0.01U/16V_4, C71 0.01U/16V_4

+VCORE1: C67 0.01U/16V_4, C64 0.01U/16V_4

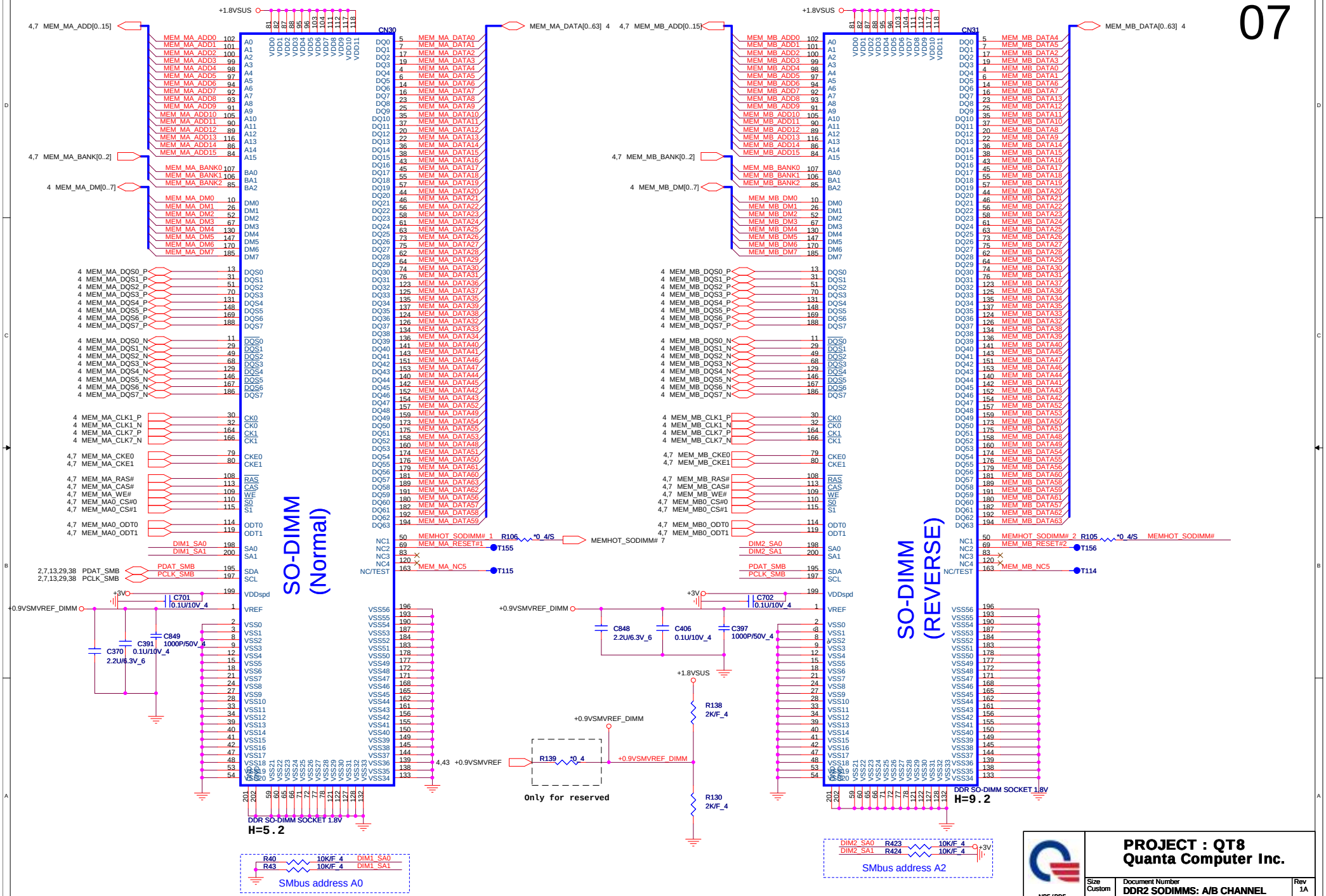
+5V: EC6 0.01U/16V_4 — +3VPCU

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

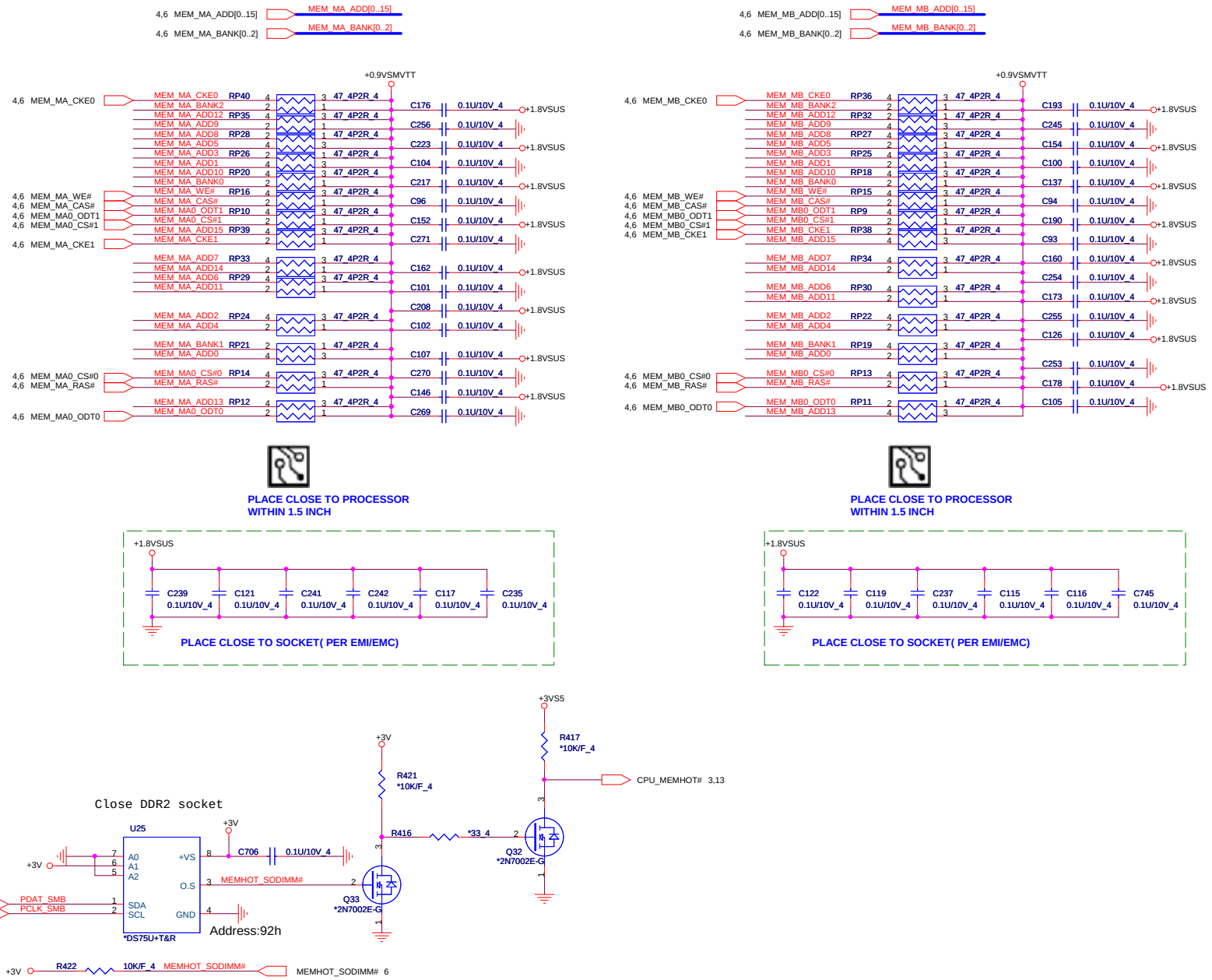
Date: Thursday, October 16, 2008 Sheet 5 of 48



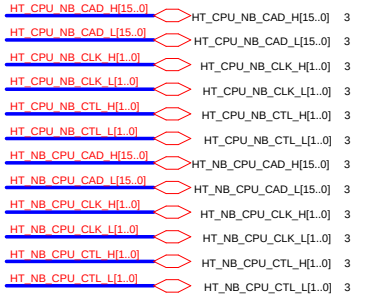
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	1A
Date: Thursday, October 16, 2008	Sheet 6 of 48	

NB5/RD5



NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: DDR2 SODIMMS TERMINATIONS	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 7 of 48	

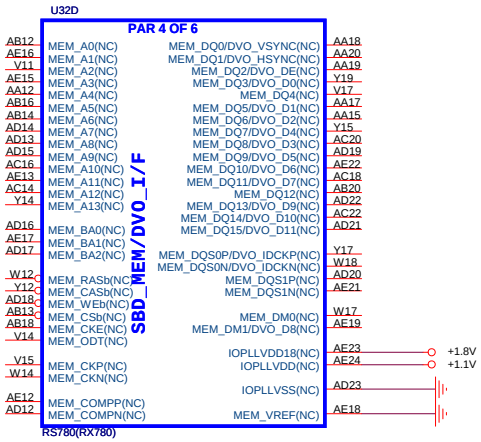


signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

This block is for UMA RS780 only , RX780 can remove all component



IOPLLVDD18 - memory PLL not applicable to RX780

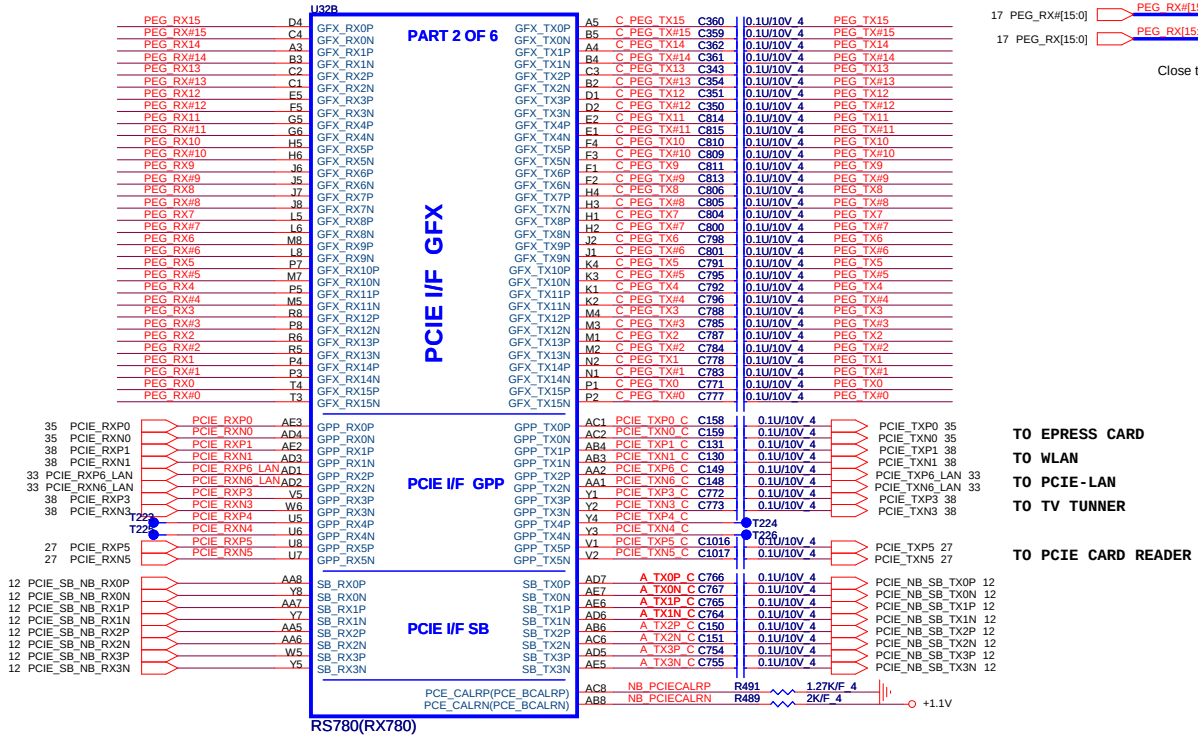
IOPLLVDD- memory PLL not applicable to RX780

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A

Date: Thursday, October 16, 2008 Sheet 8 of 48



17 PEG_RX#[15:0] → PEG_RX#[15:0]
17 PEG_RX[15:0] → PEG_RX[15:0]
PEG_TX#[15:0] → PEG_TX#[15:0] 17
PEG_TX[15:0] → PEG_TX[15:0] 17

Close to North Bridge

TO EPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

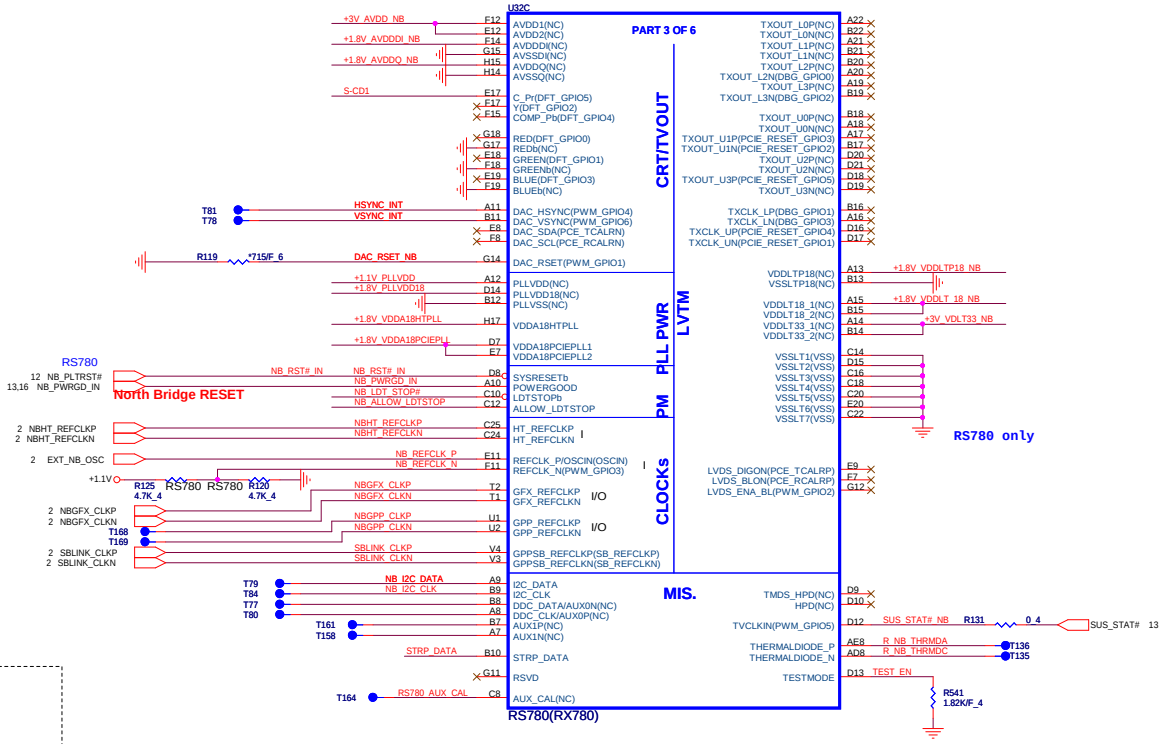
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

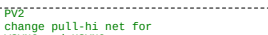
NB5/RD5

Date: Thursday, October 16, 2008 | Sheet 9 of 48



selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780



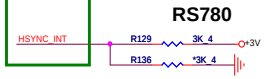
PV2
change pull-hi net for VSYNC and HSYNC

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

RS780

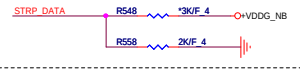
Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780



For extrnal EEPROM Debug only

RS780/RX780

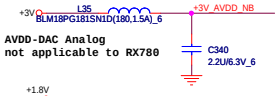


Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

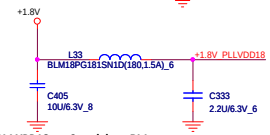
RX780

Reserved only

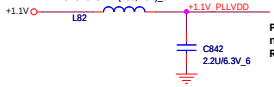
RX780 -->NC / RS780 --- ADD



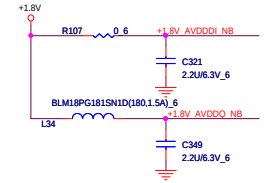
AVDD-DAC Analog
not applicable to RX780



PLLVDD18 - Graphics PLL
not applicable to RX780

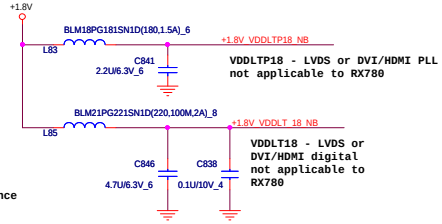


PLLVDD - Graphics PLL
not applicable to RX780



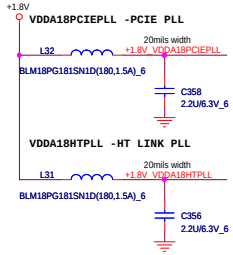
AVDDI-DAC Digital
not applicable to RX780

AVDDQ-DAC Bandgap Reference
not applicable to RX780

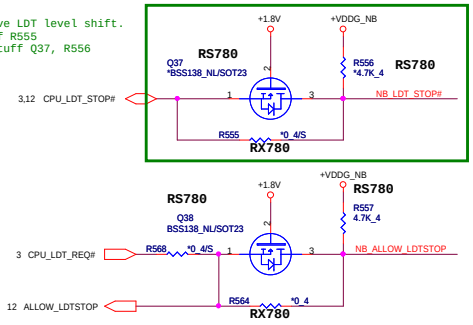


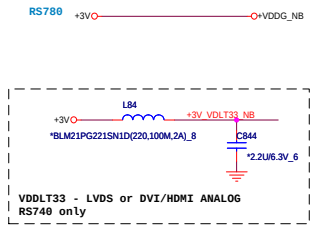
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780

VDDLT18 - LVDS or DVI/HDMI digital
not applicable to RX780



PV2
Remove LDT level shift.
stuff R555
no-stuff Q37, R556





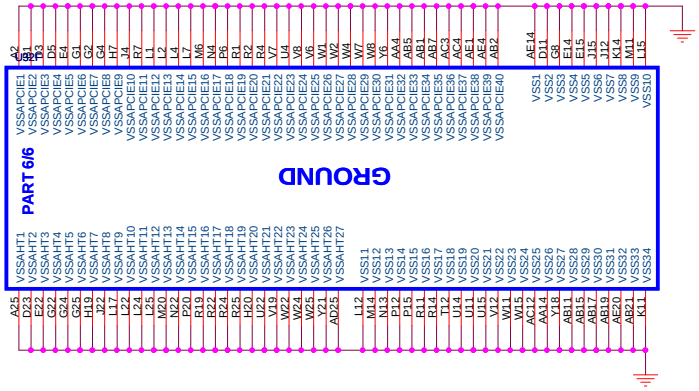
VDDLT33 - LVDS or DVI/HDMI ANALOG
RS740 only

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A

Date: Thursday, October 16, 2008 Sheet 10 of 48



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

PV2
Change L72, L81, L12 to 0 ohm

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V 2A for RS780M

0.6A — L72 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHT

C770 4.7U/6.3V_6, C274 0.1U/10V_4, C313 0.1U/10V_4, C280 0.1U/10V_4

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A — L81 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHTRX

C847 4.7U/6.3V_6, C323 0.1U/10V_4, C843 0.1U/10V_4, C839 0.1U/10V_4

VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.2V 2A for RS780M+SB700

+1.2V — 0.5A — L12 BLM21PG221SN1D(220,100M,2A)_8 — +1.2V_VDDHTTX

C124 4.7U/6.3V_6, C195 0.1U/10V_4, C194 0.1U/10V_4, C249 0.1U/10V_4, C199 0.1U/10V_4

+1.8V 1A for RS780M+SB700

+1.8V — 600mA — L22 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDA18PCIE

C188 4.7U/6.3V_6, C175 4.7U/6.3V_6, C258 0.1U/10V_4, C209 0.1U/10V_4, C302 0.1U/10V_4, C234 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V — R122 *0_6/S — 0.005A

C317 1U/10V_4

0.005A — +1.8V_VDDG18_NB

U32E

PART 5/6

POWER

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

RS780(RX780)

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE — 0.7A — R542 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V

C275 0.1U/10V_4, C337 0.1U/10V_4, C318 1U/10V_4, C328 1U/10V_4, C845 4.7U/6.3V_6

VDDC - Core Logic power

7A — +1.1V

C251 0.1U/10V_4, C292 0.1U/10V_4, C297 0.1U/10V_4, C303 0.1U/10V_4, C59 10U/6.3V_8

C281 0.1U/10V_4, C278 0.1U/10V_4, C250 0.1U/10V_4, C60 10U/6.3V_8

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+3V_VDDG33 — R123 RS780 *0_6/S — 3.3V(0.03A) — +3V

C336 0.1U/10V_4, C329 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

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DB-1 remove JMB380 reset signal

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

U37A
SB700
Part 1 of 5

PCIE_PVDD-- PCIE PLL POWER

40mA

100MHZ

FOR A14 chip
FOR A13 chip
FOR A12 chip

All the PCI bus has build-in Pull-UP/Down resistors

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	SB700-PCIE/PCI/CPU/LPC 1/4	1A

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NC only ,Can't be install

+3VSUS
R297 *2.2K_4 SB_TEST0
R240 *2.2K_4 SB_TEST1
R287 *2.2K_4 SB_TEST2

+3VSUS
R289 *10K/F_4 SWI#

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R245 2.2K_4 PCLK_SMB
R253 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner
/DDR2/DDR2
thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R648 10K/F_4 SB_SMBCLK1
R649 10K/F_4 SB_SMBDATA1

remove pull hi
(chip internal
have pull hi)

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R222 10K/F_4 SB_SCLK2
R227 10K/F_4 SB_SDATA2

+3V
R276 4.7K_4 SUS_STAT#
R349 *0_4 SYS_RST#

+3VS5
R763 2.2K_4 DNBSWON#

To Azalia

ACZ_SDOUT R644 33_4 ACZ_SDOUT_AUDIO 28
C908 *10P/50V_4
ACZ_SYNC R290 33_4 ACZ_SYNC_AUDIO 28
C569 *10P/50V_4
ACZ_BCLK R646 33_4 BIT_CLK_AUDIO 28
C910 10P/50V_4
ACZ_RST# R296 33_4 ACZ_RST#_AUDIO 28
ACZ_SDIN0_R ACZ_SDIN0 28

To Modem Board

ACZ_SDOUT R645 33_4 ACZ_SDOUT_AUDIO_MDC 31
C909 *10P/50V_4
ACZ_SYNC R292 33_4 ACZ_SYNC_AUDIO_MDC 31
C577 *10P/50V_4
ACZ_BCLK R647 33_4 BIT_CLK_AUDIO_MDC 31
C911 10P/50V_4
ACZ_RST# R293 33_4 ACZ_RST#_AUDIO_MDC 31
ACZ_SDIN1_R ACZ_SDIN1 31

35 NEWCARD_DETECT NEWCARD_DETECT R283 0_4 NEWCARD_DETECT_R
T211 RI#
T99 SLP_S2
37 SUSB# R271 *0_4/S SUSB#
37 SUSC# R191 *0_4/S SUSC#
37 DNBSWON# R233 *0_4/S DNBSWON#
16 SB_PWRGD_IN SB_PWRGD_IN
10 SUS_STAT# SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0
37 GATEA20 GATEA20
37 RCIN# RCIN#
37 SCI# SCI#
37 KBSMI# KBSMI#
T109 GEVENT5#
SYS_RST#
33,38 PCIE_WAKE# 37 PCIE_WAKE# R307 0_4 PCIE_WAKE#_R
SWI# R211 *0_4/S SWI#
3 CPU_THERMTRIP# R786 0_4 SB_THERMTRIP#
10,16 WD_PWRGD WD_PWRGD
37 RSMRST# R284 *0_4/S SMRST#

T63 SATA_IS1
T194
33,37 LAN_DISABLE# R217 *0_4 LAN_DISABLE#_SB
T222 SB_NWD_CLK_REQ#
28,29 ACZ_SPKR R302 *0_4/S ACZ_SPKR
2,6,7,29,38 PCLK_SMB PCLK_SMB
2,6,7,29,38 PDAT_SMB PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
T69
T75
37 PM_BATLOW# PM_BATLOW#
SES_INT
T72
27 D3E_SCI#

3,7 CPU_MEMHOT#
5 PM_THERM# R275 *0_4 SMBALERT#_1
+3VS5 R279 10K/F_4
CPU_MEMHOT#_IN
35 NEWCARD_WAKE# R285 *0_4 NEWCARD_WAKE#_R
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

ACZ_BCLK
ACZ_SDOUT
R246 10K/F_4 ACZ_SDIN0_R
R249 10K/F_4 ACZ_SDIN1_R
R254 10K/F_4 ACZ_SDIN2_R
R308 10K/F_4 ACZ_SDIN3_R
ACZ_SYNC
16 ACZ_RST# ACZ_RST#

HD audio
interface is
3.3S5 voltage

U37D

SB700

Part 4 of 5

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

H19 IMC_GPIO0
H20 IMC_GPIO1
H21 SPI_CS2#/IMC_GPIO2
F25 IDE_RST#/F_RST#/IMC_GPO3
D22 IMC_GPIO4
E24 IMC_GPIO5
E25 IMC_GPIO6
D23 IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC C8 CLK_48M_USB CLK_48M_USB 2
USB_RCOMP G8 USB_RCOMP_SB R267 11.8K/F_6

USB MISC

USB 1.1

USB_FSD13P E6 USB_FSD13P T101
USB_FSD13N E7 USB_FSD13N T199
USB_FSD12P F7 USB_FSD12P T91
USB_FSD12N E8 USB_FSD12N T93

USB_HSD11P H11 USBP11+ 38
USB_HSD11N J10 USBP11- 38 TV Min-Card
USB_HSD10P E11 USBP10+ 38
USB_HSD10N F11 USBP10- 38 WLAN Min-Card
USB_HSD9P A11 USBP5+ 32
USB_HSD9N B11 USBP5- 32 BLUETOOTH
USB_HSD8P C10 USBP8+ 32
USB_HSD8N D10 USBP8- 32 USB Connector
USB_HSD7P G11 USBP7+ 35
USB_HSD7N H12 USBP7- 35 NEW CARD
USB_HSD6P E12 USBP6+ 32
USB_HSD6N E14 USBP6- 32 FINGERPRINT
USB_HSD5P C12 USBP9+ 32
USB_HSD5N D12 USBP9- 32 USB Connector
USB_HSD4P B12 USBP4+ 39
USB_HSD4N A12 USBP4- 39 Docking
USB_HSD3P G12
USB_HSD3N G14
USB_HSD2P H14 USBP2+ 32
USB_HSD2N H15 USBP2- 32 Carama USB
USB_HSD1P A13 USBP1+ 32
USB_HSD1N B13 USBP1- 32 E-SATA and USB Connector
USB_HSD0P B14 USBP0+ 32
USB_HSD0N A14 USBP0- 32 USB Connector

USB 2.0

IMC_GPIO8 A18
IMC_GPIO9 B18
IMC_PWM0/IMC_GPIO10 F21
SCL2/IMC_GPIO11 D21 SB_SCLK2
SDA2/IMC_GPIO12 F19 SB_SDATA2
SCL3_LV/IMC_GPIO13 E20 SB_SCLK3 T64
SDA3_LV/IMC_GPIO14 E21 SB_SDATA3 T70
IMC_PWM1/IMC_GPIO15 E19
IMC_PWM2/IMC_GPO16 D19 SB_GPIO16 16
IMC_PWM3/IMC_GPO17 E18 SB_GPIO17 16 SPI/LPC define
IMC_GPIO18 G20
IMC_GPIO19 G21
IMC_GPIO20 D25
IMC_GPIO21 D24
IMC_GPIO22 C25
IMC_GPIO23 C24
IMC_GPIO24 B25
IMC_GPIO25 C23
IMC_GPIO26 B24
IMC_GPIO27 B23
IMC_GPIO28 A23
IMC_GPIO29 C22
IMC_GPIO30 A22
IMC_GPIO31 B22
IMC_GPIO32 B21
IMC_GPIO33 A21
IMC_GPIO34 D20
IMC_GPIO35 C20
IMC_GPIO36 A20
IMC_GPIO37 B20
IMC_GPIO38 B19
IMC_GPIO39 A19
IMC_GPIO40 D18
IMC_GPIO41 C18

for EMI & del R268
change 2.2P

CLK_48M_USB
C554 *2.2P/50V_4

+3VS5 R764 2K/04 +3V
35 SCLK_WLAN Q66 2N7002EPT PCLK_SMB
+3VS5 R765 2K/04 +3V
35 SDATA_WLAN 2N7002EPT Q67 PDAT_SMB

CN16
+3VSUS
C462 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
SB JTAG
*S/W JTAG DEBUG

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A
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SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

SATA HDD2

SATA PORT 4,5 are only support IDE mode

U37B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

SATA PWR

HW MONITOR

R361 1K/F_4

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:

R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Y4 25MHZ

AVDD AVSS

5mA

AVDD--H/W monitor Analog power

U20 TC7SH08FU

77mA

1mA

Place near ball

ID4 GP60	ID3 GP59	ID2 GP58	ID1 GP57	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

POWER

SB700 Part 3 of 5

VDDQ--3.3V I/O power 0.8A

+3V → C576 100U/6.3V_3528 → C557 10U/6.3V_8, C560 1U/10V_4, C573 1U/10V_4, C565 1U/10V_4, C547 1U/10V_4, C553 1U/10V_4, C574 1U/10V_4

VDDQ_1 … VDDQ_12 (L9, M9, T15, U9, U16, U17, V8, W7, Y6, AA4, AB5, AB21) — PCI/GPIO I/O

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 0.45A

+3V → R226 *0_8/S → +VDD33_18 → C486 10U/6.3V_8, C501 1U/10V_4, C487 1U/10V_4, C497 1U/10V_4, C488 1U/10V_4

VDD33_18_1 … VDD33_18_4 (Y20, AA21, AA22, AE25) — IDE/FLSH I/O

PCIE_VDDR--PCIE I/O power 844mA

+1.2V → L89 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_PCIE_VDDR → C477 10U/6.3V_8, C502 1U/10V_4, C484 1U/10V_4, C504 1U/10V_4, C492 1U/10V_4, C483 1U/10V_4

PCIE_VDDR_1 … PCIE_VDDR_7 (P18, P19, P20, P21, R22, R24, R25) — A-LINK I/O

AVDD_SATA--SATA phy power 0.2A

+1.2V → L92 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDD_SATA → C888 10U/6.3V_8, C880 0.1U/10V_4, C884 0.1U/10V_4, C883 1U/10V_4, C881 1U/10V_4

AVDD_SATA_1 … AVDD_SATA_7 (AA14, AB18, AA15, AA17, AC18, AD17, AE17) — SATA I/O

For support USB wakeup-->3V_S5

AVDDTX--USB Phy
Analog I/O power 0.2A

+3VS5 → L91 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDD_USB → C889 10U/6.3V_8, C882 10U/6.3V_8, C878 0.1U/10V_4, C886 0.1U/10V_4

C528 1U/10V_4, C537 1U/10V_4, C885 1U/10V_4, C511 0.1U/10V_4, C510 0.1U/10V_4, C879 0.1U/10V_4, C536 0.1U/10V_4

AVDDTX_0 … AVDDRX_5 (A16, B16, C16, D16, D17, E17, E15, F17, F18, G15, G17, G18) — USB I/O

VDD-- S/B CORE power

+1.2V_VCC_SB_R → C533 1U/10V_4, C545 1U/10V_4, C538 1U/10V_4, C532 1U/10V_4, C467 10U/6.3V_8 — 604mA

R198 *0_8/S → +1.2V

VDD_1 … VDD_9 (L15, M12, M14, N13, P12, P14, R11, R15, T16) — CORE S0

CKVDD_1.2V-- Internal
clock Generator I/O
power

+1.2V_CKVDD → C505 2.2U/6.3V_6, C489 0.1U/50V_6, C475 0.1U/50V_6, C478 2.2U/6.3V_6 — 286mA

L43 BLM18PG181SN1D(180,1.5A)_6 → +1.2V

CKVDD_1.2V_1 … CKVDD_1.2V_4 (L21, L22, L24, L25) — CLKGEN I/O

S5_3.3--3.3v standby power

+3VALW_R → C875 0.1U/10V_4, C570 0.1U/10V_4, C876 10U/6.3V_8 — 0.01A

R604 *0_6/S → +3VS5

Change to 0603

S5_3.3V_1 … S5_3.3V_7 (A17, A24, B17, J4, J5, L1, L2) — 3.3V_S5 I/O

S5_1.2V--1.2V standby power

0.22A → C903 0.1U/10V_4, C901 0.1U/10V_4 → +1.2V_S5

S5_1.2V_1, S5_1.2V_2 (G2, G4) — CORE S5

0.2A → +1.2V_USB_PHY_R

USB_PHY_1.2V_1, USB_PHY_1.2V_2 (A10, B10)

V5_VREF--PCI 5V TOLERANCE

+5V_VREF → R621 1K/F_4 → +5V

4mA

V5_VREF (AE7)

AVDDCK_3.3V (J16) → +3V_AVDDCK — 7mA

AVDDCK_1.2V (K17) → +1.2V_AVDDCK — 44mA

AVDDC (F9) → +3V_AVDDC — 16mA

D36 CH501H-40PT → +3V

C898 1U/10V_4

PLL

SB700

U37E

SB700

Part 5 of 5

AVSS_SATA_1 … AVSS_SATA_20 (T10, U10, U11, U12, V11, V14, W9, Y9, Y11, Y14, Y17, AA9, AB9, AB11, AB13, AB15, AB17, AC8, AD8, AE8)

AVSS_USB_1 … AVSS_USB_24 (A15, B15, C14, D8, D9, D11, D13, D14, D15, E15, F12, F14, G9, H9, H17, J9, J11, J12, J14, J15, K10, K12, K14, K15)

PCIE_CK_VSS_1 … PCIE_CK_VSS_8 (H18, J17, J22, K25, M16, M17, M21, P16)

AVSSC (F9)

VSS_1 … VSS_50 (A2, A25, B1, D7, F20, G19, H8, K9, K11, K16, L4, L7, L10, L11, L12, L14, L16, M6, M10, M11, M13, M15, N4, N12, N14, P6, P9, P10, P11, P13, P15, R1, R2, R4, R9, R10, R12, R14, T11, T12, T14, U4, U14, V6, Y21, AB1, AB19, AB25, AE1, AE24)

PCIE_CK_VSS_9 … PCIE_CK_VSS_21 (P23, R16, R19, T17, U18, U20, V18, V20, V21, W19, W22, W24, W25)

AVSSCK (L17)

GROUND

USB_PHY_1.2V--USB Phy
digital power

+1.2V_S5 → R616 0_6 → +1.2V_USB_PHY_R → C890 0.1U/10V_4, C891 0.1U/10V_4, C892 10U/6.3V_8

AVDDC--USB Analog PLL power

+3VS5 → L50 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDC → C546 0.1U/10V_4, C540 10U/6.3V_8

AVDDCK_1.2--USB Phy
digital power

+1.2V → L45 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDDCK → C509 2.2U/6.3V_6

AVDDCK_3.3--Analog
system PLL power

+3V → L48 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDCK → C516 2.2U/6.3V_6

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

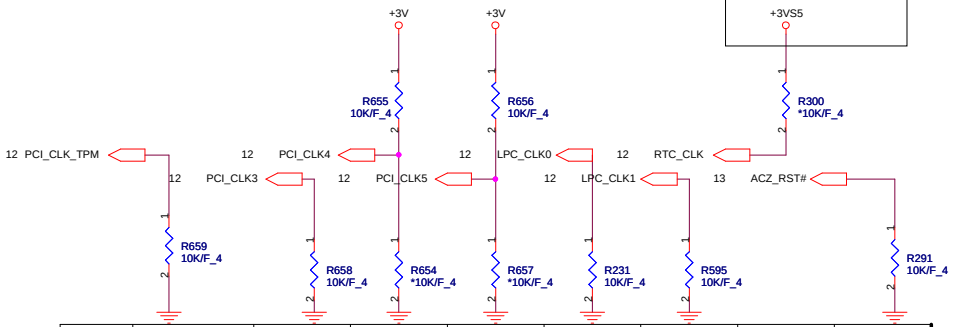
Size	Document Number	Rev
Custom	SB700-PWR/DECOUPLING 4/4	1A

Date: Thursday, October 16, 2008 Sheet 15 of 48

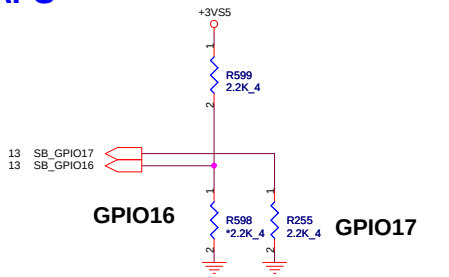
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



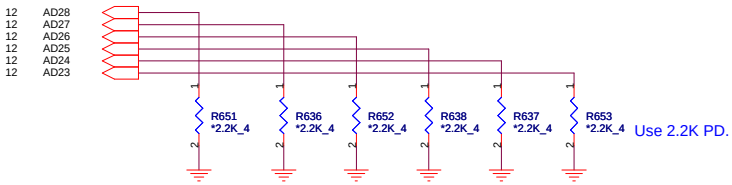
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

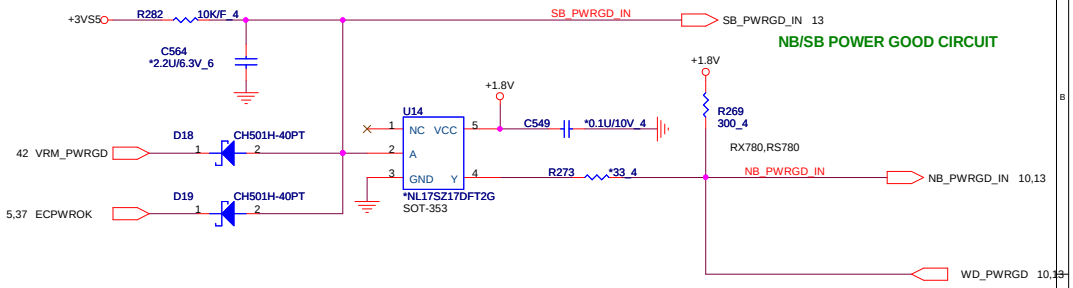
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



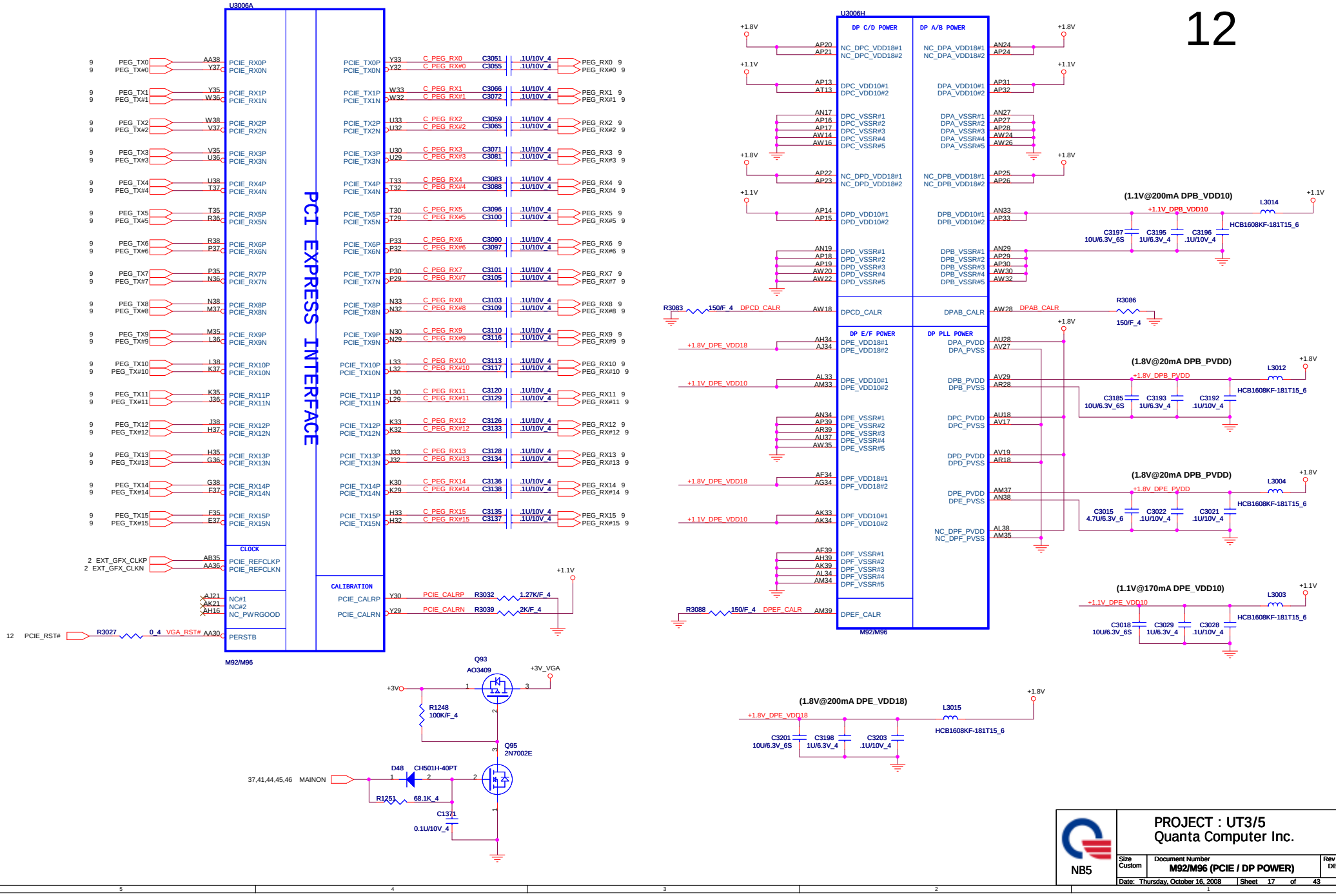
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

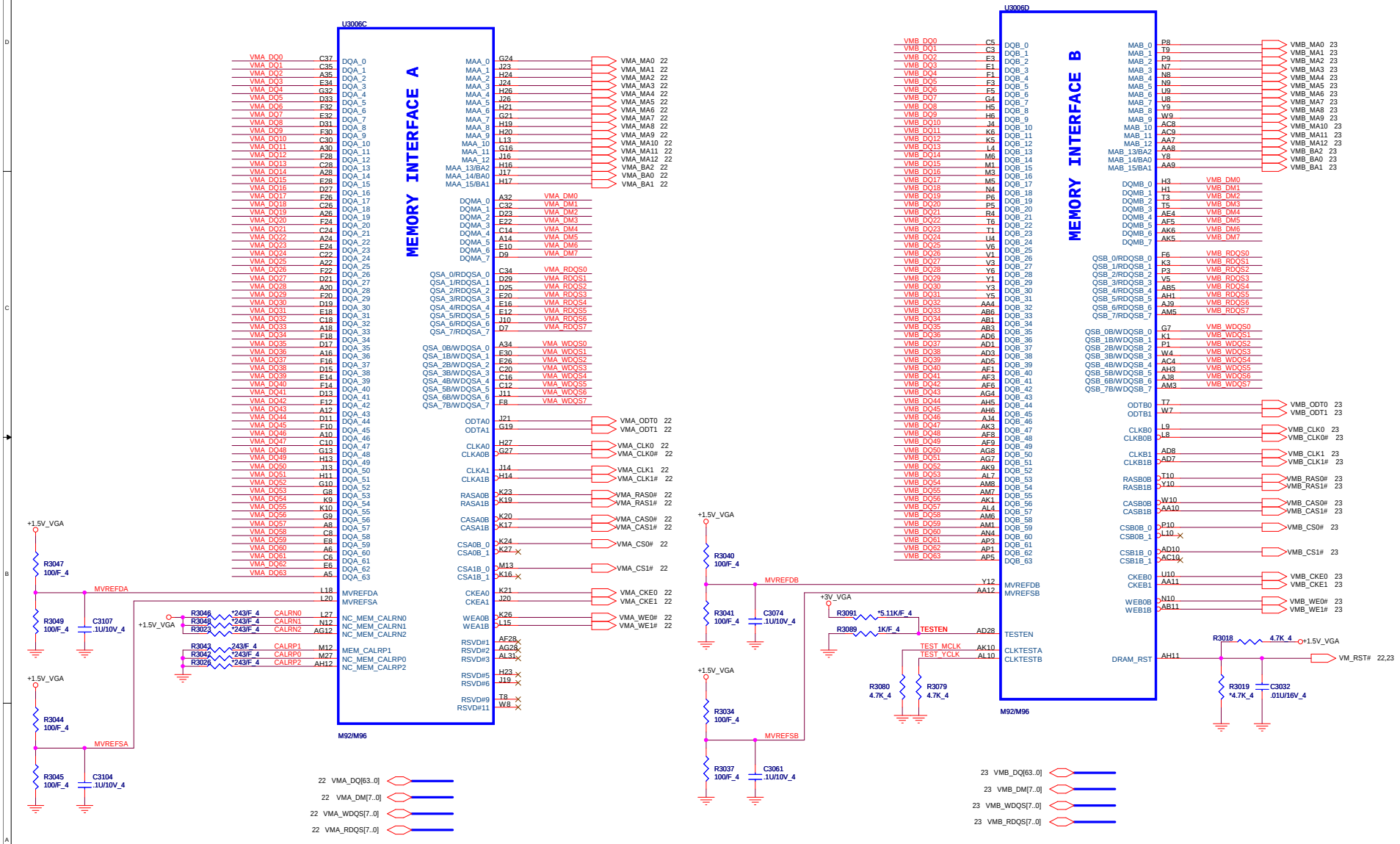
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

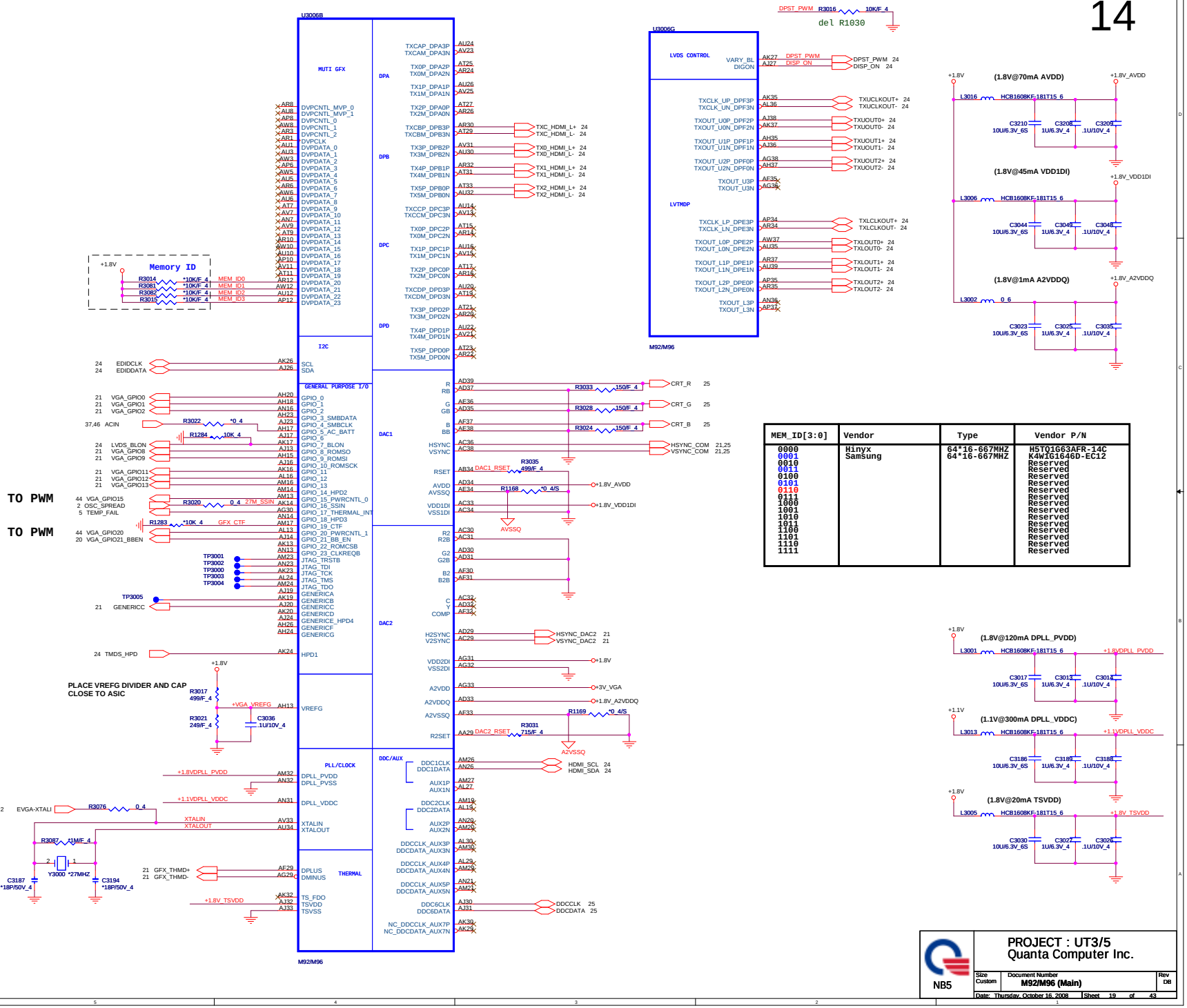
Size	Document Number	Rev
Custom	SB700-STRAPS	1A

Date: Thursday, October 16, 2008 | Sheet 16 of 48





PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: M92/M96 (Memory I/F)
Rev: DB	
Date: Thursday, October 16, 2008	Sheet 18 of 43



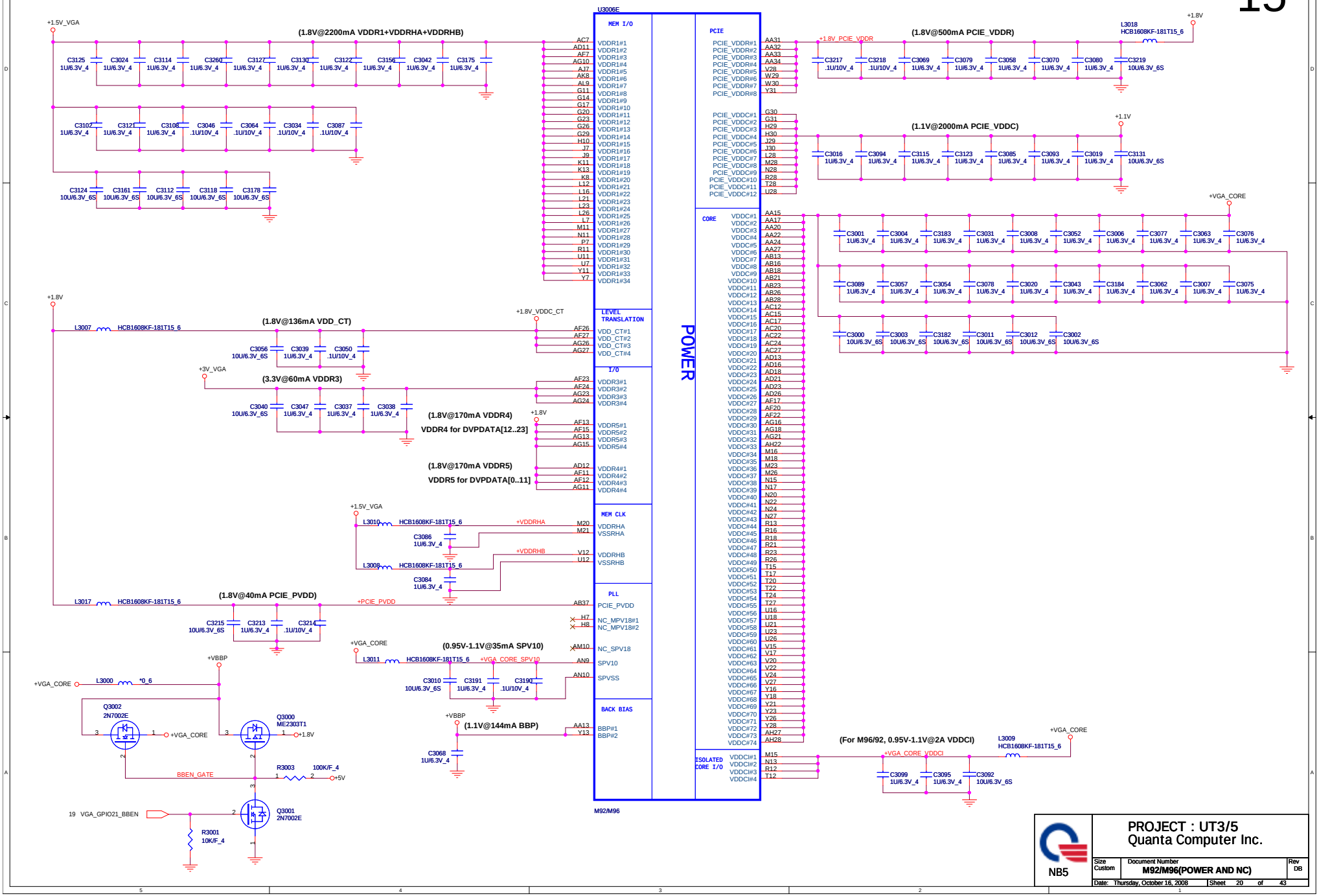
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinyx	64*16-667MHZ	H5TQ1G63AFR-14C
0001	SamSung	64*16-667MHZ	K4W1G1646D-EC12
0010			Reserved
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

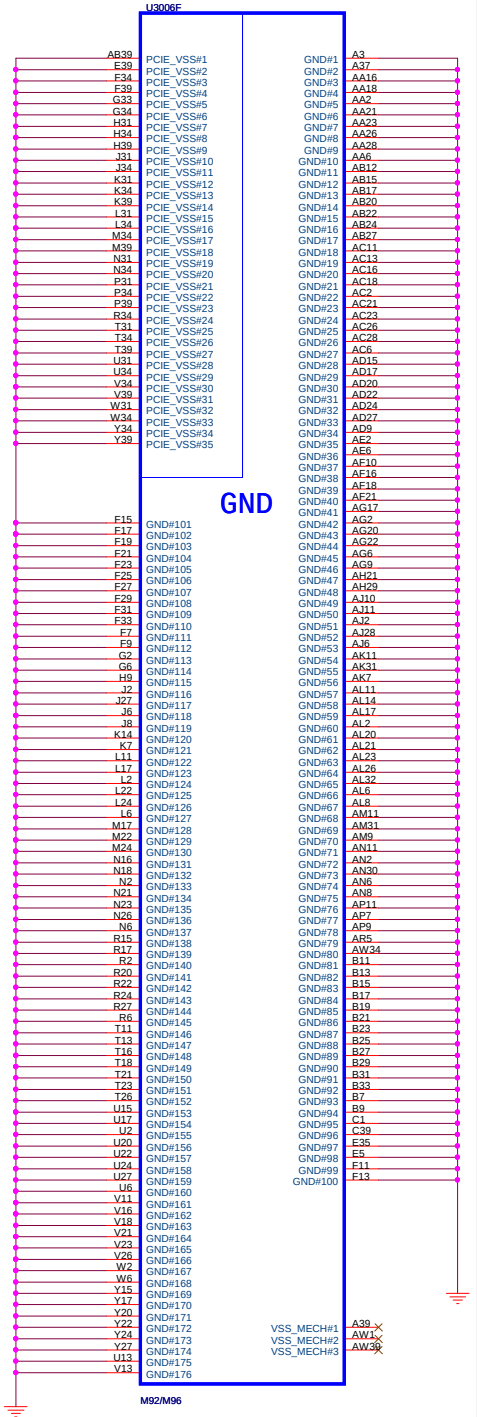
NB5

PROJECT : UT3/5
Quanta Computer Inc.

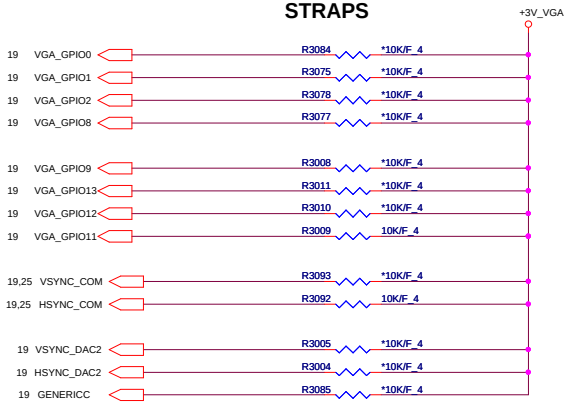
Size: Custom | Document Number: M92/M96 (Main) | Rev: DB

Date: Thursday, October 16, 2008 | Sheet 19 of 43


U3006E
MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
POWER
PCIE
CORE
ISOLATED CORE I/O
M92/M96
(1.8V@2200mA VDDR1+VDDRHA+VDDRHB)
(1.8V@500mA PCIE_VDDR)
(1.1V@2000mA PCIE_VDDC)
(1.8V@136mA VDD_CT)
(3.3V@60mA VDDR3)
(1.8V@170mA VDDR4)
VDDR4 for DVPDATA[12..23]
(1.8V@170mA VDDR5)
VDDR5 for DVPDATA[0..11]
(1.8V@40mA PCIE_PVDD)
(0.95V-1.1V@35mA SPV10)
(1.1V@144mA BBP)
(For M96/92, 0.95V-1.1V@2A VDDCI)
PROJECT : UT3/5
Quanta Computer Inc.
NB5
M92/M96(POWER AND NC)
Date: Thursday, October 16, 2008
Sheet 20 of 43

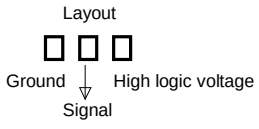


STRAPS

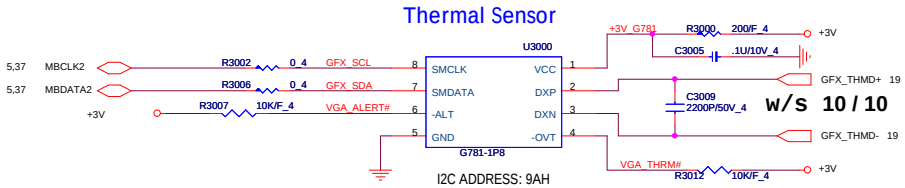


Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0

Overlap pads to save space and to prevent assembly of both resistors.



Thermal Sensor



I2C ADDRESS: 9AH

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	M92/M96 (GND/Straps/Therm)	DB

Date: Thursday, October 16, 2008 Sheet 21 of 43

CHANNEL A: 256MB/512MB DDR3

18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

U3004 / U3009 / U3008 / U3003 — VRAM_DDR3 — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R3072 243/F_4 — R3108 243/F_4 — R3109 243/F_4 — R3061 243/F_4

18,23 VM_RST#

+1.5V_VGA

R3071 4.99K/F_4 — R3070 4.99K/F_4 — VREFC_VMA1 — C3159 .1U/10V_4
R3060 4.99K/F_4 — R3062 4.99K/F_4 — VREFD_VMA1 — C3143 .1U/10V_4
R3058 4.99K/F_4 — R3059 4.99K/F_4 — VREFC_VMA2 — C3142 .1U/10V_4
R3112 4.99K/F_4 — R3113 4.99K/F_4 — VREFD_VMA2 — C3261 .1U/10V_4
R3111 4.99K/F_4 — R3110 4.99K/F_4 — VREFC_VMA3 — C3253 .1U/10V_4
R3063 4.99K/F_4 — R3057 4.99K/F_4 — VREFD_VMA3 — C3141 .1U/10V_4
R3064 4.99K/F_4 — R3065 4.99K/F_4 — VREFC_VMA4 — C3144 .1U/10V_4
R3067 4.99K/F_4 — R3066 4.99K/F_4 — VREFD_VMA4 — C3153 .1U/10V_4

VMA_CLK0 — R3074 56.2/F_4 — VMA_CLK0_COMM — C3169 .01U/16V_4
VMA_CLK0# — R3073 56.2/F_4
VMA_CLK1 — R3068 56.2/F_4 — VMA_CLK1_COMM — C3174 .01U/16V_4
VMA_CLK1# — R3069 56.2/F_4

+1.5V_VGA
C3256 C3255 C3254 C3249 C3252 C3258 C3257 C3259 — 1U/6.3V_4
C3244 C3243 C3246 C3247 C3262 C3154 C3251 C3250 — 1U/6.3V_4
C3155 C3173 C3172 C3168 C3177 C3158 C3157 C3167 — 1U/6.3V_4
C3166 C3163 C3162 C3165 C3170 C3176 C3164 C3171 — 1U/6.3V_4
C3245 C3248 C3229 C3160 C3180 — 10U/6.3V_6S
C3181 C3179 C3151 C3152 C3106 — 10U/6.3V_6S

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A(DDR3 BGA96)	DB

Date: Thursday, October 16, 2008 Sheet 22 of 43

CHANNEL B: 256MB/512MB DDR3

18 VMB_DQ[63..0]
18 VMB_DM[7..0]
18 VMB_WDQS[7..0]
18 VMB_RDQS[7..0]

U3007 — VRAM_DDR3 — 100-BALL SDRAM DDR3
U3002 — VRAM_DDR3 — 100-BALL SDRAM DDR3
U3001 — VRAM_DDR3 — 100-BALL SDRAM DDR3
U3005 — VRAM_DDR3 — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R3103 243/F_4
R3054 243/F_4
R3025 243/F_4
R3098 243/F_4

+1.5V_VGA

R3104 4.99K/F_4
R3102 4.99K/F_4
R3056 4.99K/F_4
R3055 4.99K/F_4
R3051 4.99K/F_4
R3053 4.99K/F_4
R3050 4.99K/F_4
R3052 4.99K/F_4
R3038 4.99K/F_4
R3036 4.99K/F_4
R3029 4.99K/F_4
R3030 4.99K/F_4
R3099 4.99K/F_4
R3100 4.99K/F_4
R3094 4.99K/F_4
R3096 4.99K/F_4

VREFC_VMB1 VREFD_VMB1 VREFC_VMB2 VREFD_VMB2 VREFC_VMB3 VREFD_VMB3 VREFC_VMB4 VREFD_VMB4

C3225 .1U/10V_4
C3139 .1U/10V_4
C3132 .1U/10V_4
C3119 .1U/10V_4
C3053 .1U/10V_4
C3060 .1U/10V_4
C3216 .1U/10V_4
C3212 .1U/10V_4

VMB_CLK0
R3107 56.2/F_4
VMB_CLK0_COMM
C3233 .01U/16V_4
R3106 56.2/F_4
VMB_CLK0#
VMB_CLK1
R3095 56.2/F_4
VMB_CLK1_COMM
C3211 .01U/16V_4
R3097 56.2/F_4
VMB_CLK1#

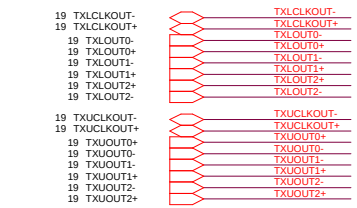
C3149 C3146 C3150 C3148 C3140 C3147 C3111 C3145 1U/6.3V_4
C3234 C3239 C3237 C3241 C3232 C3236 C3242 C3235 1U/6.3V_4
C3230 C3231 C3221 C3199 C3206 C3220 C3223 C3224 1U/6.3V_4
C3091 C3033 C3041 C3098 C3045 C3204 C3073 C3082 1U/6.3V_4
C3207 C3240 C3067 C3205 C3202 10U/6.3V_6S
C3200 C3227 C3222 C3238 C3226 10U/6.3V_6S

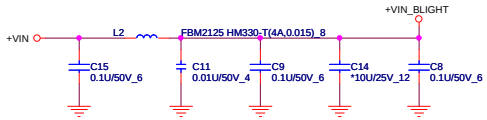
NB5

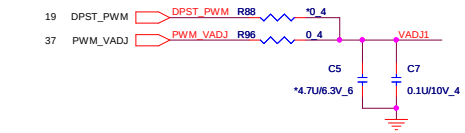
PROJECT : UT3/5
Quanta Computer Inc.

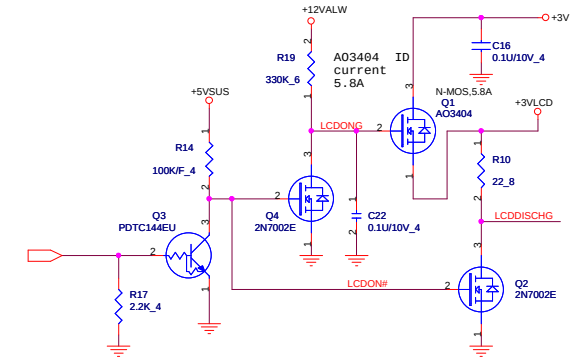
Size	Document Number	Rev
Custom	VRAM-B(DDR3 BGA96)	DB

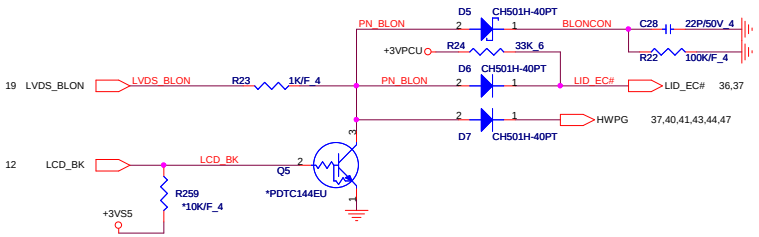
Date: Thursday, October 16, 2008 Sheet 23 of 43

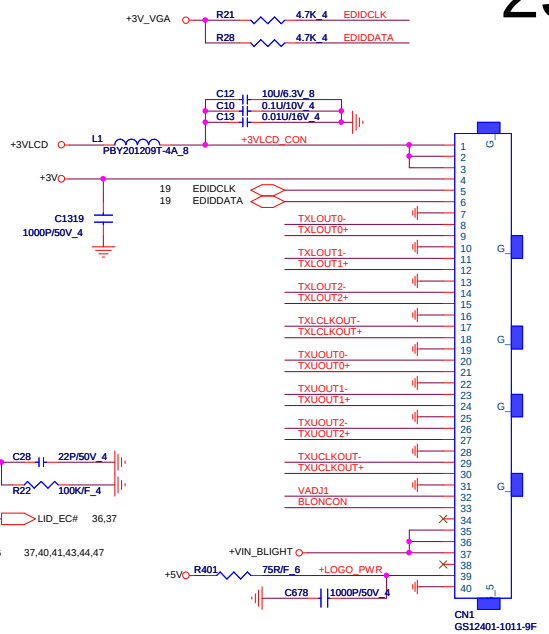


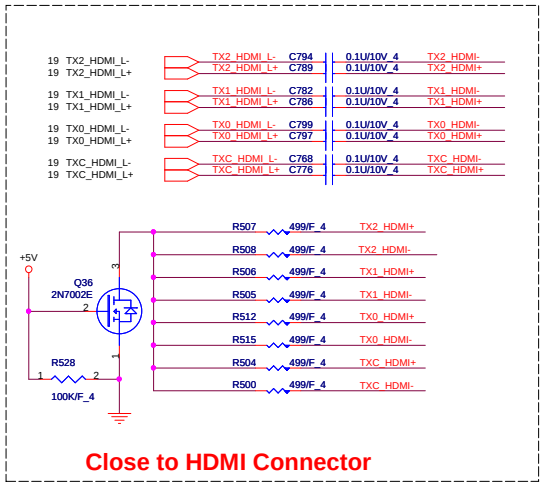






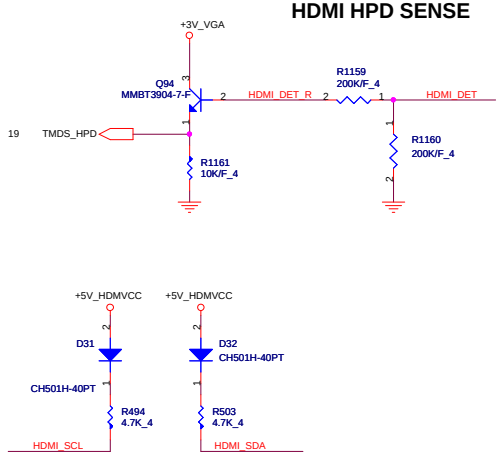






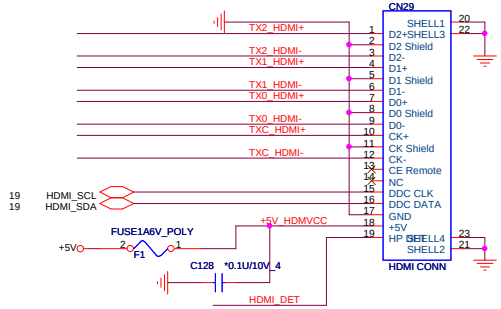
Close to HDMI Connector

HDMI HPD SENSE

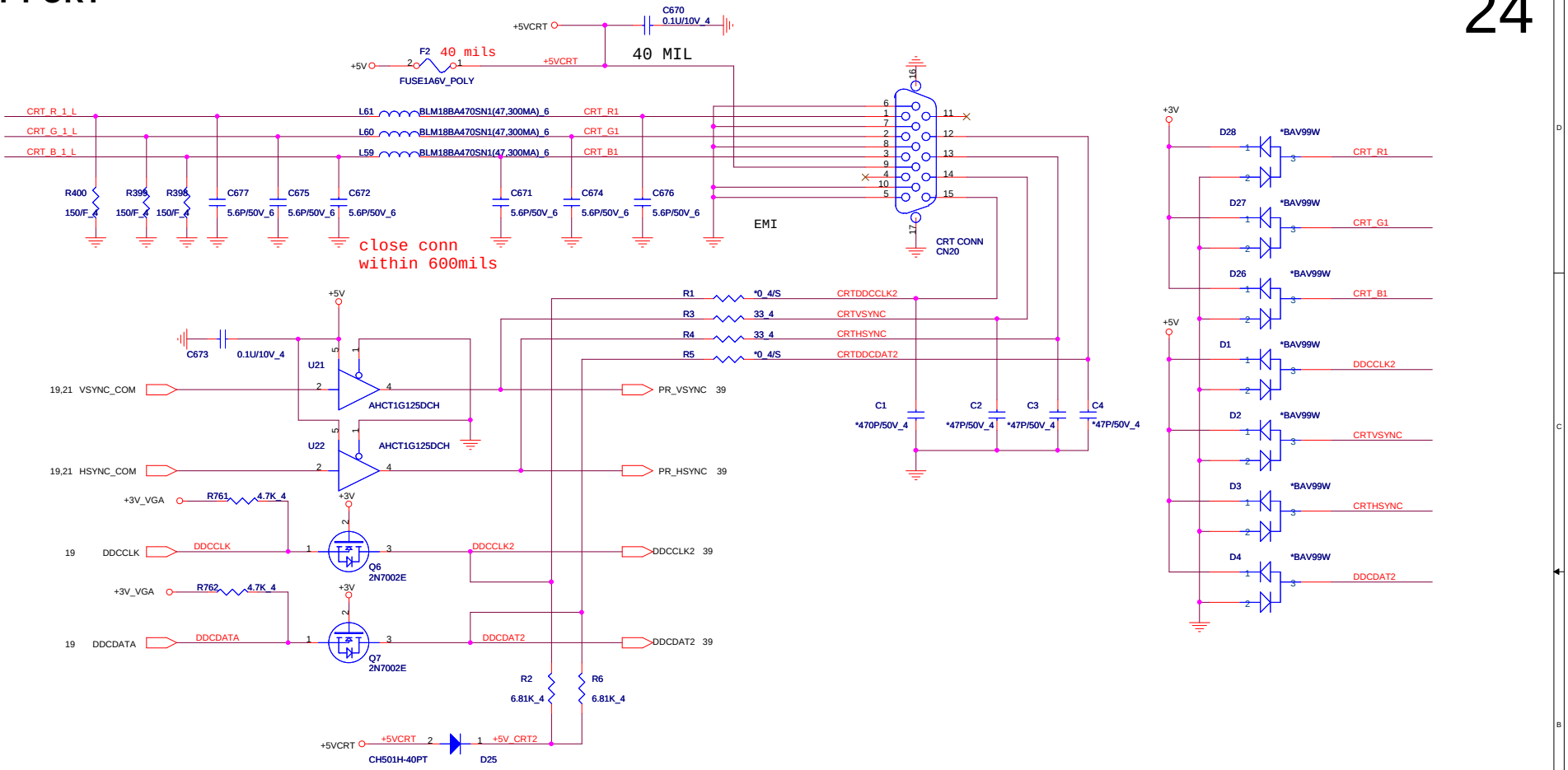


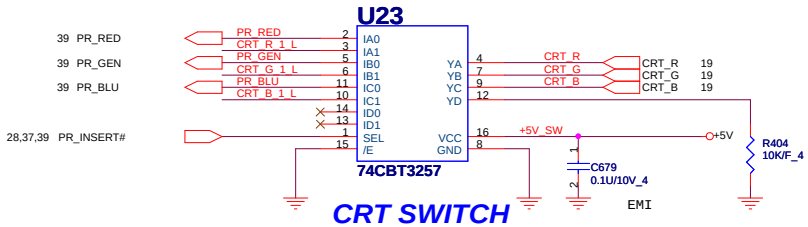
Change R494, R503 to 4.7K for AMD on PV2
DIS use 4.7K
UMA use 2K

HDMI PORT



CRT PORT





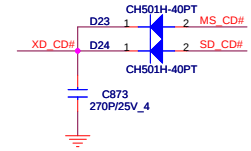
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

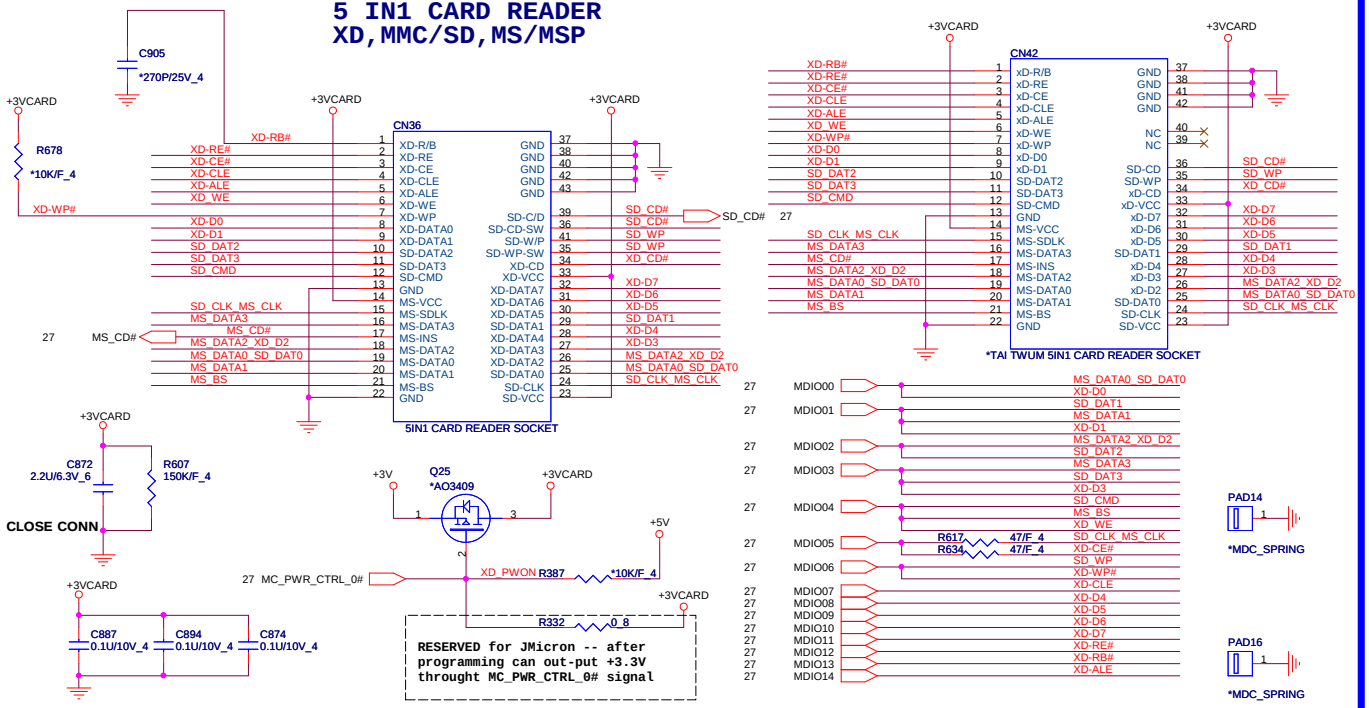
NB5/RD5

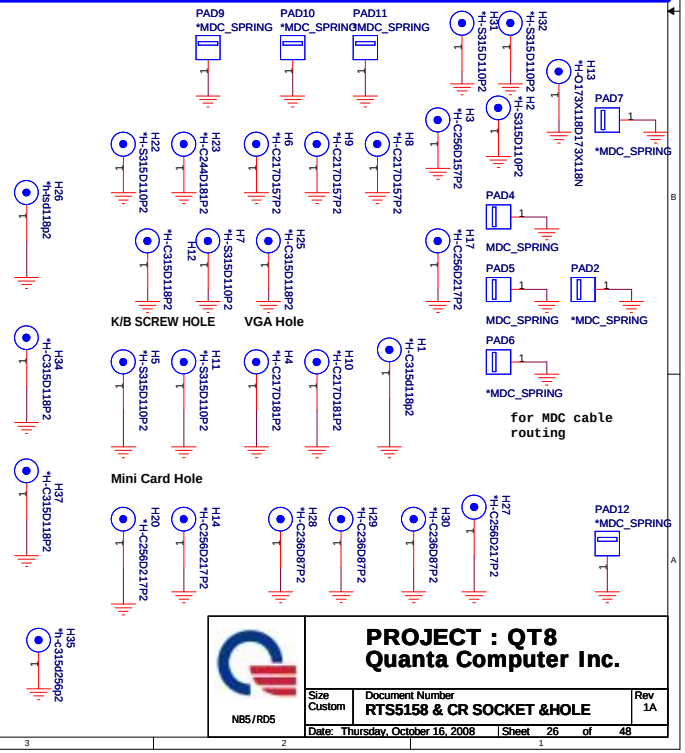
Date: Thursday, October 16, 2008 Sheet 25 of 48



PAD13 *GND PAD
PAD15 *GND PAD
PAD17 *GND PAD
PAD18 *GND PAD
PAD19 *GND PAD
PAD20 *GND PAD

5 IN1 CARD READER
XD,MMC/SD,MS/MSP



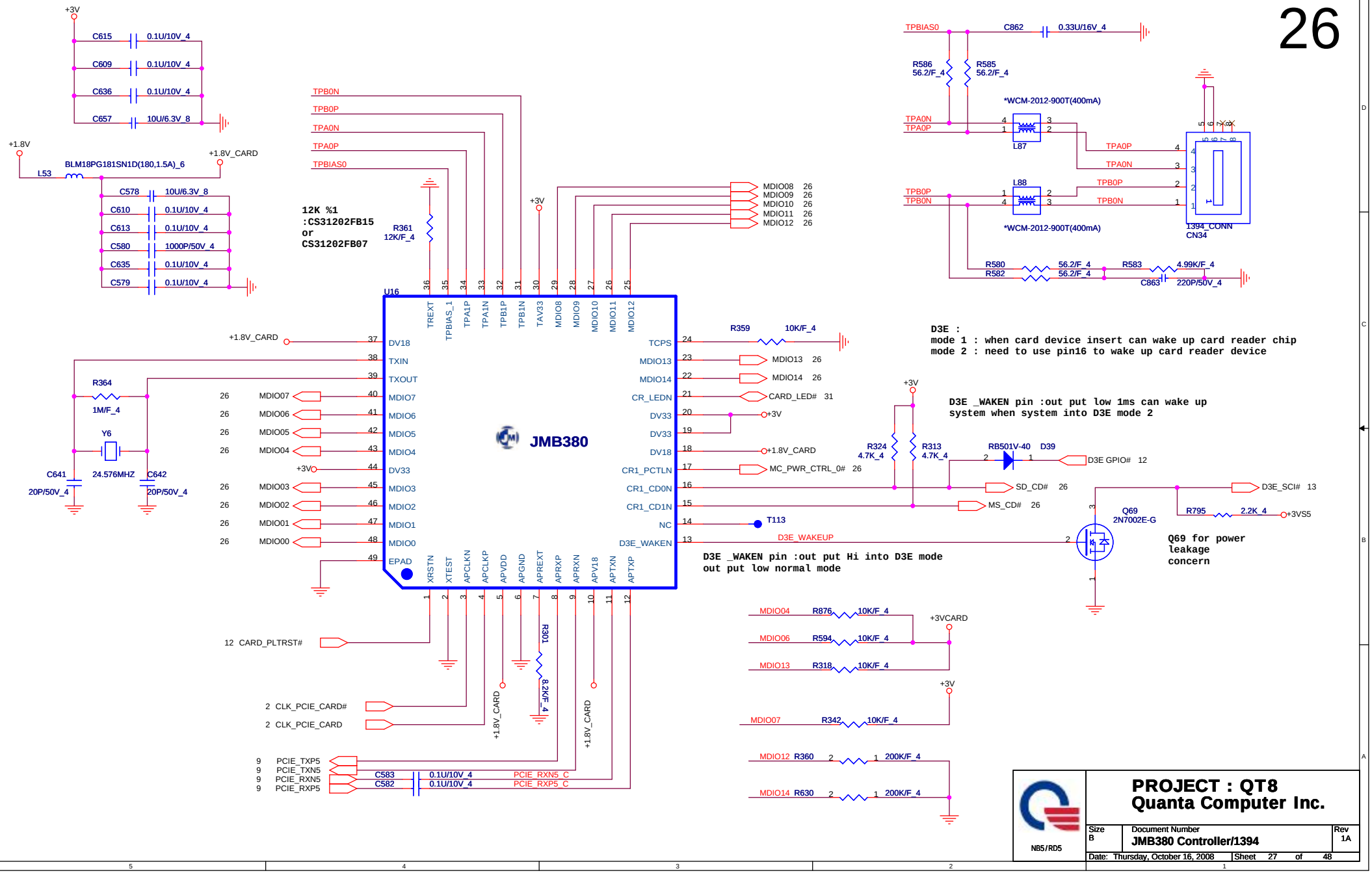


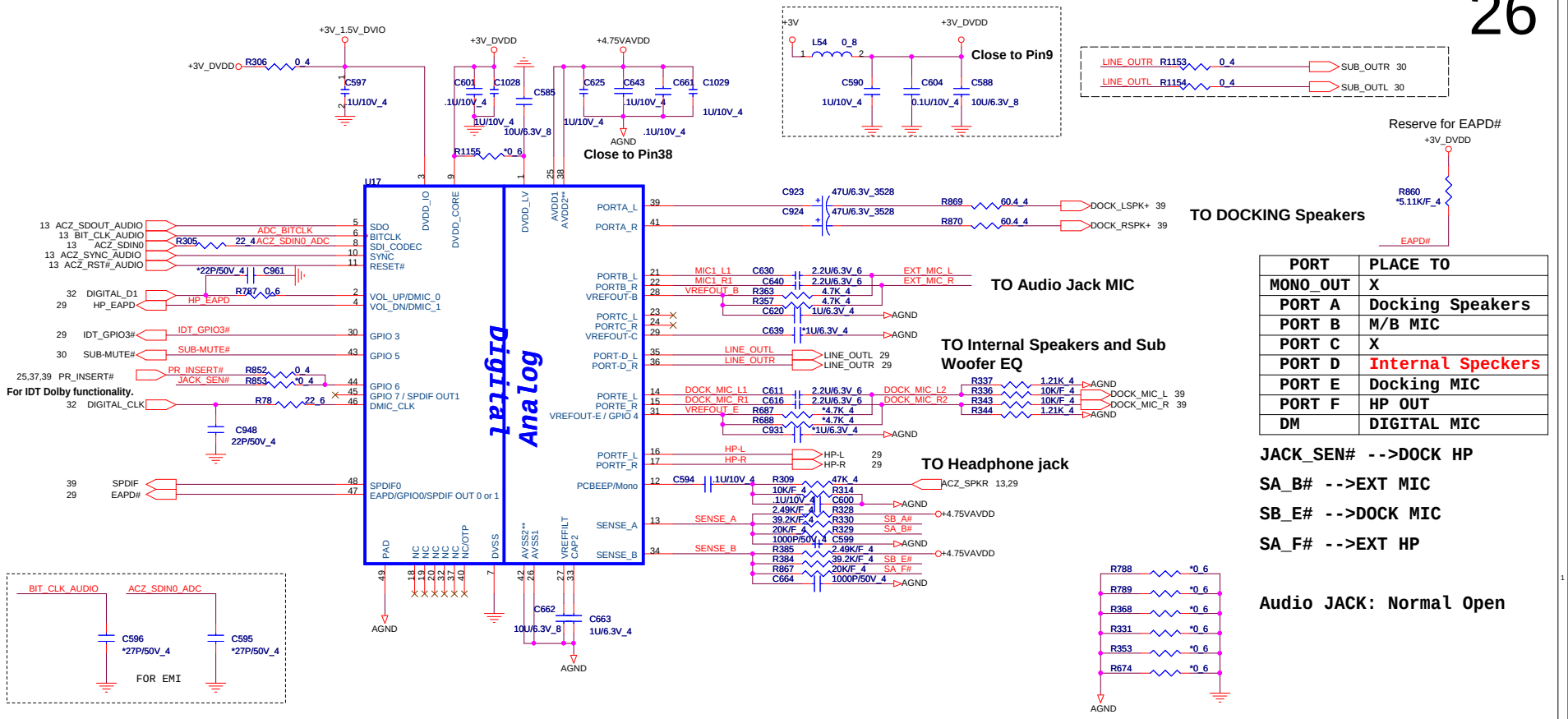
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

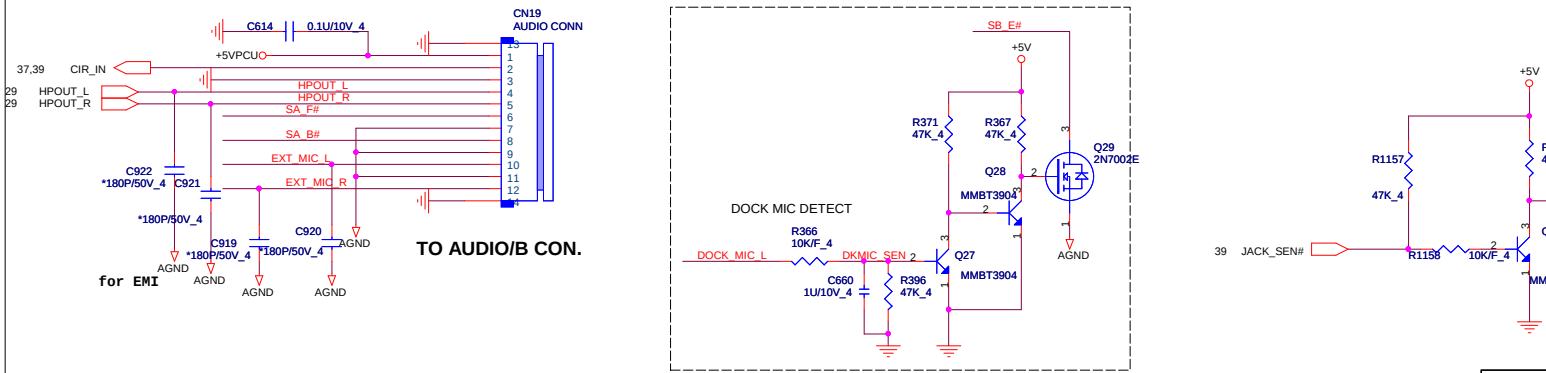
NB5/RD5

Date: Thursday, October 16, 2008 Sheet 26 of 48





PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC



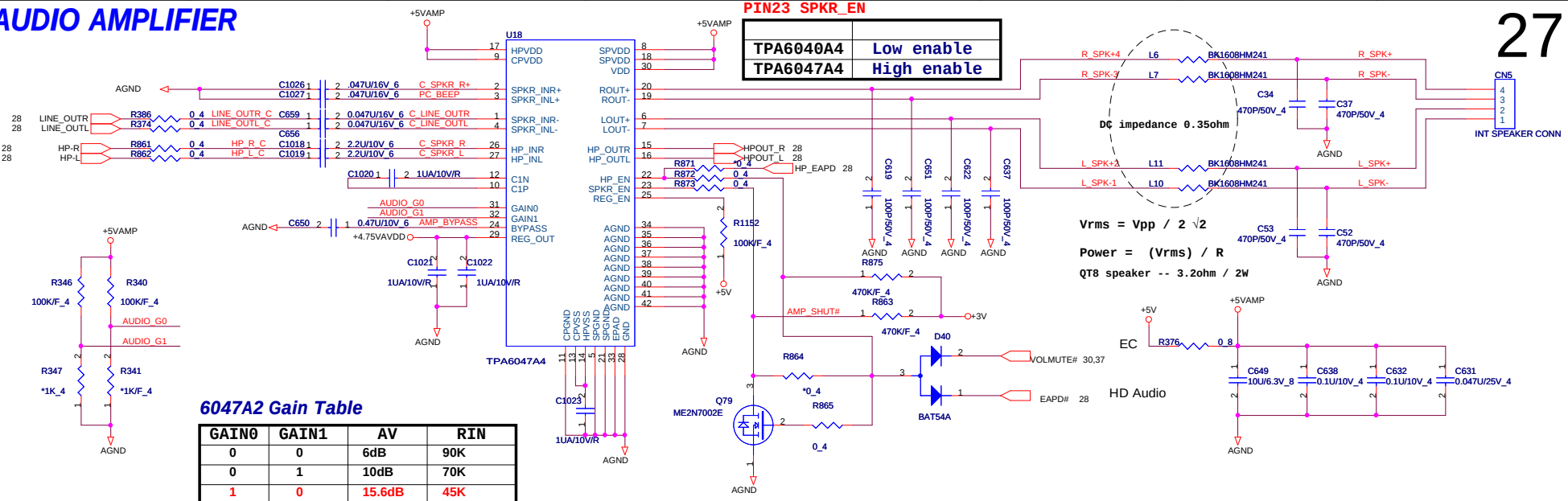
PROJECT :	QT8
	Quanta Computer Inc.
Size: Custom	Document Number: Azalia AD1883
Rev:	1A
Date: Thursday, October 16, 2008	Sheet 28 of 48

NB5/RD5

AUDIO AMPLIFIER

PIN23 SPKR_EN

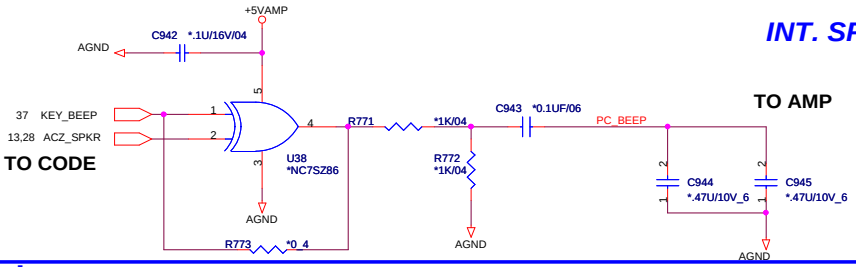
TPA6040A4	Low enable
TPA6047A4	High enable



6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

PC-BEEP



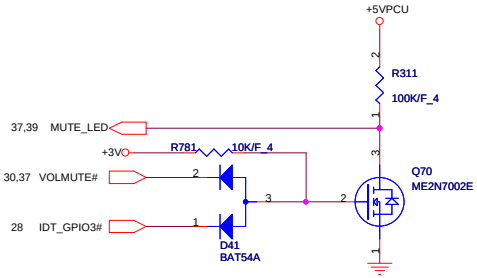
INT. SPEAKER

TO AMP

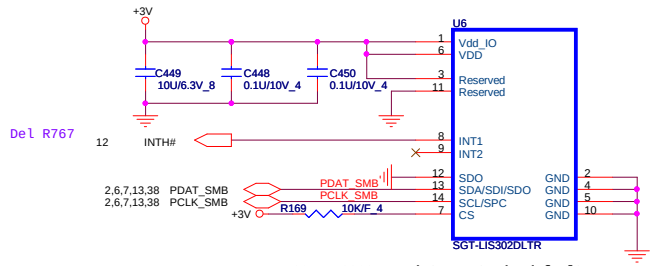
MUTE_LED

Low -->un-MUTE

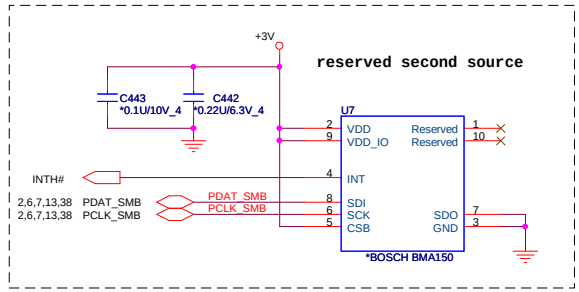
High-->Mute



Acceleration sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/INT SPK	1A

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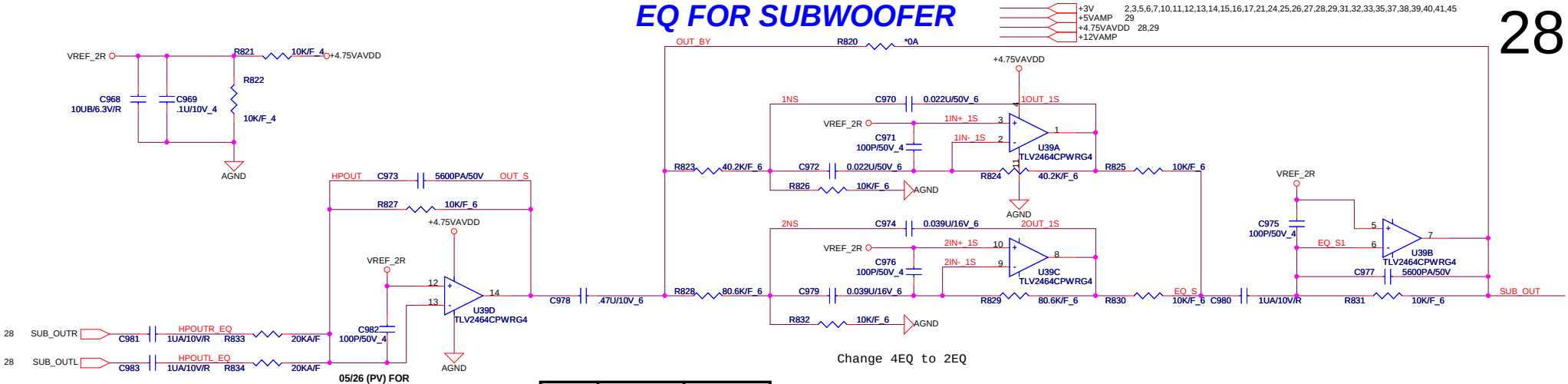
NB5/RD5

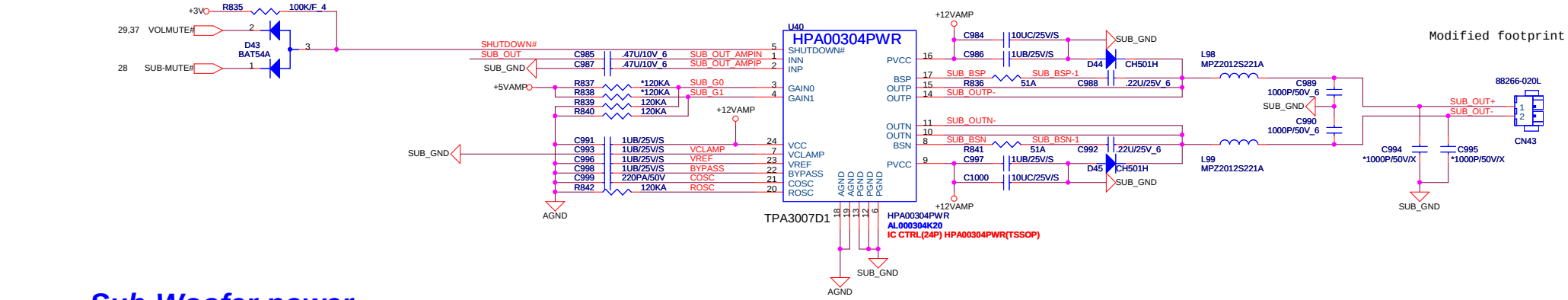
EQ FOR SUBWOOFER



05/26 (PV) FOR BOM update.

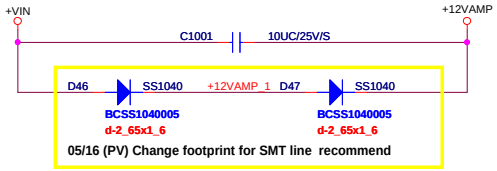
Change 4EQ to 2EQ

MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C979	0.027U/25V_6	0.039U/16V_6

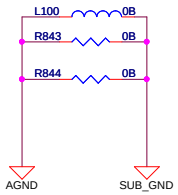


Modified footprint

Sub-Woofer power



05/16 (PV) Change footprint for SMT line recommend



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	DB

Date: Thursday, October 16, 2008 Sheet 30 of 48

Modem CONN

DB-1 Change FP

H21 H-C217D63P2

H19 H-C217D63P2

MDC

CN18

13 ACZ_SDOUT_AUDIO_MDC → ACZ_SDOUT_AUDIO_MDC

13 ACZ_SYNC_AUDIO_MDC → ACZ_SYNC_AUDIO_MDC

13 ACZ_SDIN1 ← AC_SDIN1_MDC

13 ACZ_RST#_AUDIO_MDC

1	GND	REV	2
3	A_SDO	REV	4
5	GND	VCC	6
7	A_SYNC	GND	8
9	A_SDI	GND	10
11	A_RST#	A_BCLK	12

MDC CONN

R326 33_4

C603 *10P/50V_4

+3V

C653 0.1U/10V_4

C654 2.2U/6.3V_6

C658 1000P/50V_4

R377 0_4 → BIT_CLK_AUDIO_MDC 13

C652 *10P/50V_4

For EMI

LED

R750 *10K/F_4

37 LEDVCC_EN# → Q65 *PDTC144EU

Q64 *PDTC144EU

R766 0_6

14 SATA_LED#

14 ACCLED_EN → Q26 PDTC144EU

R767 200/F_6

(White) / (Amber)

SATA_R_LED1 R381 39_6 → +3V

LED4 LED 3P WHITE/AMBER

SI-1 modified -- for fix SATA LED no support LED light control

PV2
Change R381, R767 value for HDD LED

Single Color ,Right angle
LTW-110TLA

LED PWR CONTROL

+15VALW

R180 *1M_4

R178 *1M/F_4 LED_CTL

37 LEDVCC_EN# → LEDVCC_EN# → *2N7002E Q17

R817 0_8

Q18 *2N7002E

+3V → +3V_LED → +3V_LED

20~40mils

C457 10U/6.3V_8

C460 0.1U/10V_4

C451 *1U/25V_8

C932 *.22U/25V_6

C933 *.22U/25V_6

add LED auto dim function

R818 0_8

Q23 *2N7002E

+3VPCU → +3VPCU_LED

20~40mils

LED_CTL

C566 10U/6.3V_8

C568 0.1U/10V_4

R819 0_8

Q12 *AO3404

+5V → +5V_LED

20~40mils

LED_CTL

C410 0.1U/10V_4

C556 *10U/6.3V_8

36,37 PWR_LED# → LED6 2P WHITE LED → PWR_R_LED1 R378 39_6 → +3VPCU_LED

37 MBATLED0# → LED5 2P WHITE LED → MBAT_R_LED1 R379 39_6 → +3VPCU_LED

27 CARD_LED# → LED7 2P WHITE LED → CARD_LED1 R584 39_6 → +3V

SI-1 modified -- change LED part number

3 White
Anode 2
1 Amber
Dual Color ,Right angle
LTW-326DSKF-5A

LED1 for 17.3"

37 CAPSLED# → LED1 2P WHITE → CAP_LED R185 39_6 → +3V_LED

LED9 for 16.3"

37 CAPSLED# → LED9 *2P WHITE → CAP_LED

PV2
Change to 39ohm

LED Vf

I = Vcc -Vf / R

LED3 for 16.3"

37 TP_LED1# → TP_LED1# → TPLD3 R183 200/F_6 → +3V_LED

37 TP_LED2# → TP_LED2# → TPLD4 R182 39_6 → +3V_LED

(Amber) / (White)

LED3 *LED 4P WHITE/AMBER

LED8 for 17.3"

朝上

37 TP_LED1# → TP_LED1# → TPLD3

37 TP_LED2# → TP_LED2# → TPLD4

(White) / (Amber)

LED8 LED 4P WHITE/AMBER

Amber
4 2 +
Anode
3 1 +
White

Vcc

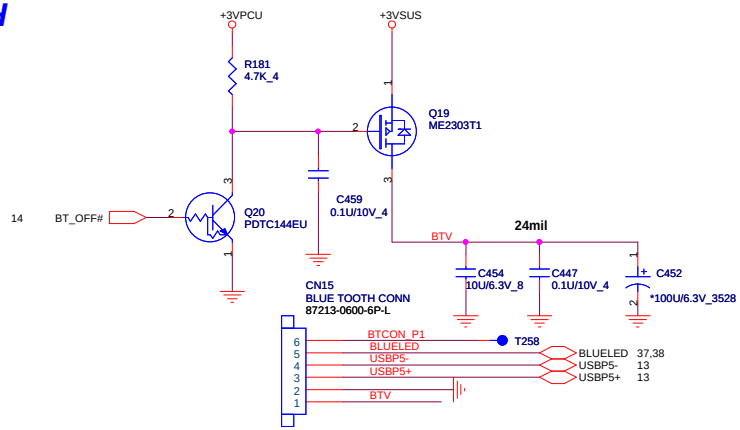
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

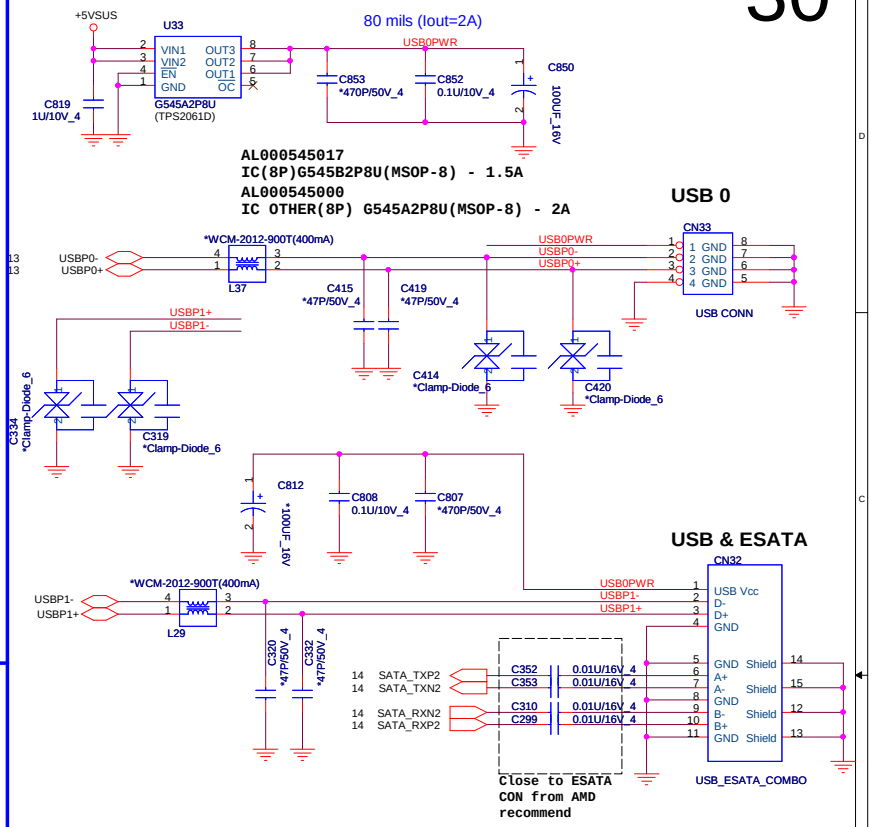
Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

Date: Thursday, October 16, 2008 Sheet 31 of 48

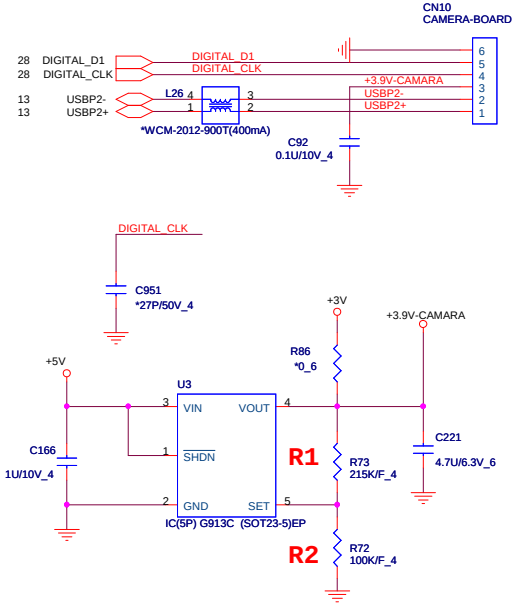
BLUETOOTH



LEFT SIDE USBX1 and E-SATA/USB COMBO

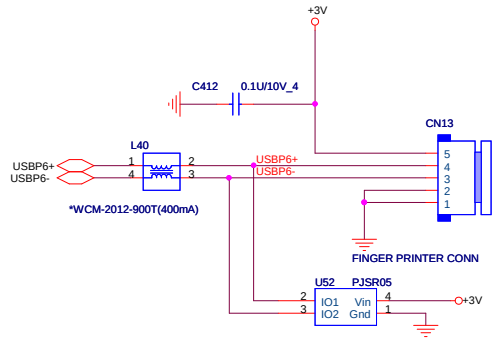


USB CAMERA CONNECT

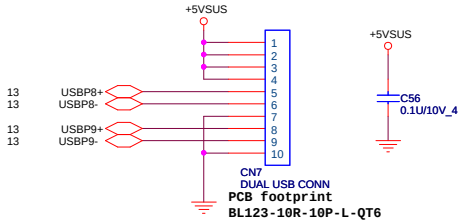


USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



RIGHT SIDE USBX2



NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: BT/WEBCAM/FT/USBX4/ESATA	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 32 of 48	

for RTL8111DL use

close to pin44,45

C1342 10U/6.3V_8
C1340 *10U/6.3V_8
C1341 0.1U/10V_4

+CTRL12DVDD

for RTL8111DL use
R462 0_6 +3V_LAN

+CTRL12DVDD R38 *0_6 +DVDD12_LAN
for RTL8103E use

R461

ENSWREG R461 0_6 +3V_LAN
R463 *0_6

R463

R461 and R463 are used in RTL8111DL , remove R463 if switching regulator is enable , Remove R461 external power is used.

Y1 25MHZ
C45 30P/50V_4
C44 30P/50V_4
XTAL1
XTAL2
+CTRL12DVDD
R37 2.49K/F_4 LANRSET
34 +CTRL12A
+CTRL12A
ENSWREG
+3V_LAN
+DVDD12_LAN
LAN_TX#
+3V_LAN

U2 RTL8103EL/8111DL

+3V_A_LAN
MDI0+
MDI0-
+DVDD12_LAN
MDI1+
MDI1-
MDI2+
MDI2-
+DVDD12_LAN
MDI3+
MDI3-
+DVDD12_LAN

AVDD33 MDIP0 MDIN0 NC/FB12 MDIP1 MDIN1 GND1 NC/MDIP2 NC/MDIN2 DVDD12/AVDD12 NC/MDIP3 NC/MDIN3

VCTRL12A SROUT12 GND4 RSET VCTRL12DVDDR NCVDDSR NC/ENSWREG CKTAL2 CKTAL1 NC/AVDD33 NC/LX_FIL LED0 VDD33B

DVDD12B LED1/EESK LED2/EEDI LED3/EEDO EECS GND3 DVDD12A VDD33A ISOLATEB PERSTB LANWAKEB CLKREQB

LAN_GLINK100#
LAN_GLINK10#
LAN_GLINK1000#
+DVDD12_LAN
+3V_LAN
R427 3.6K_6
ISOLATEB
LAN_REST_R#
PCIE_WAKE#
R460 *0_4
LAN_REST# 37
PCIE_WAKE# 13,38

DVDD12 GND2 HSIP HSIN REFCLK_P REFCLK_N EVDD12 HSOP HSON ISOLATE NC/GPO NC/NC

+DVDD12_LAN
LAN CABLE DETECT 37

PCIE_RXN6_LAN_L C82 0.1U/10V_4 PCIE_RXN6_LAN 9
PCIE_RXP6_LAN_L C81 0.1U/10V_4 PCIE_RXP6_LAN 9

9 PCIE_TXP6_LAN
9 PCIE_TXN6_LAN
2 PCIE_LAN_CLKP
2 PCIE_LAN_CLKN
PCIE_TXP6_LAN
PCIE_TXN6_LAN
PCIE_LAN_CLKP
PCIE_LAN_CLKN
EVDD12

AL08111DB00 RTL8111DL-GR

AL08103EB00 RTL8103EL-GR

+3V
R456 *1K/F_4
ISOLATEB
R457 100_4
LAN_DISABLE# 13,37
*RB501V-40
D42
R441 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

RJ45
CN27
+3V_LAN R58 330_4 LAN_GLED LAN_GLED#
LED_GRE_P LED_GRE_N
LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+
RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND
+3V_LAN R34 330_4 LAN_YLED LAN_YLED#
LED_YEL_P LED_YEL_N
RJ45_CONN

LAN_GLINK10# LAN_GLINK100# D37 BAT54A
LAN_GLINK1000# D38 RB501V-40 LAN_GLED#
LAN_TX# LAN_YLED#
Link
C39 *0.01U/16V_4 C85 *0.01U/16V_4

12 LAN_PLTRST#
+3V_LAN
C733 0.1U/10V_4
U28 TC7SH08FU
LAN_PLTRST# LAN_REST_R#

U26 NS892402

C709 0.01U/16V_4 V_DAC
MDI0+ MDI0-
C68 0.01U/16V_4 V_DAC
MDI1+ MDI1-
C62 0.01U/16V_4 V_DAC
MDI2+ MDI2-
C65 0.01U/16V_4 V_DAC
MDI3+ MDI3-

TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4-

LAN_MCT0 C927 0.01U/100V_6 R39 75/F_4 LAN_MX0+ 39 LAN_MX0- 39
LAN_MCT1 C928 0.01U/100V_6 R44 75/F_4 LAN_MX1+ 39 LAN_MX1- 39
LAN_MCT2 C929 0.01U/100V_6 R47 75/F_4 LAN_MX2+ 39 LAN_MX2- 39
LAN_MCT3 C930 0.01U/100V_6 R51 75/F_4 LAN_MX3+ 39 LAN_MX3- 39

C708 1000P/3KV_1808

LAN_YLED LAN_GLED
EMI
C88 *0.1U/50V_6 C40 *0.1U/50V_6

NS892402:GIGABIT DB0AT9LAN05
NS892405:10/100 DB0ZB1LAN04

NB5

PROJECT : UT12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ11-RJ45 CN	1A

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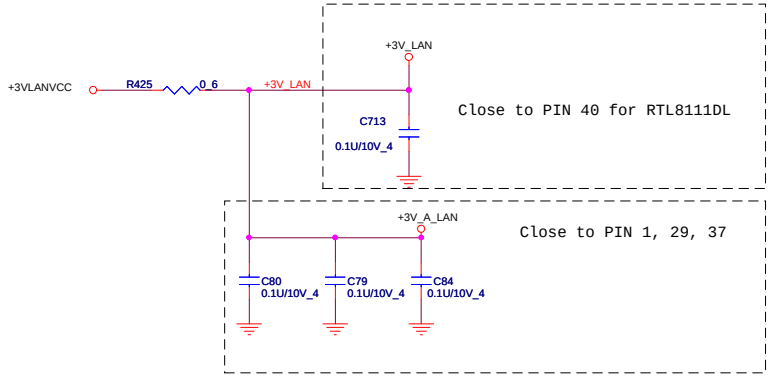
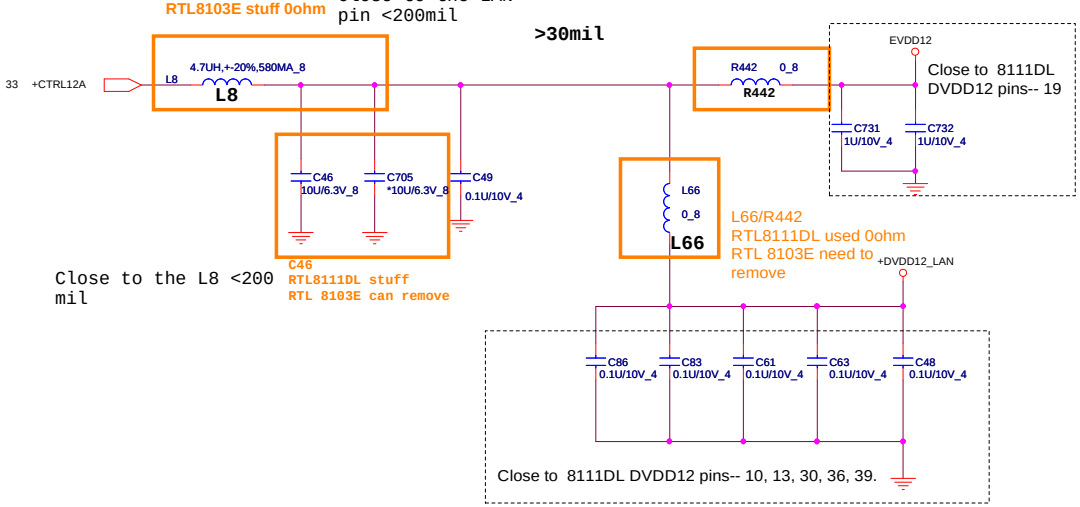


L8
RTL8111DL (Gaga lan) use 4.7uH
power choke A>500mA tolerance
±15%
RTL8103E stuff 0ohm

Close to the LAN pin <200mil

>30mil

Power trace Layout 寬度> 30mil



Close to the L8 <200 mil

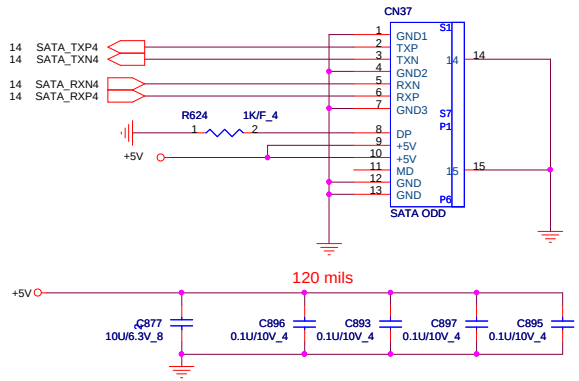
C46
RTL8111DL stuff
RTL 8103E can remove

>30mil

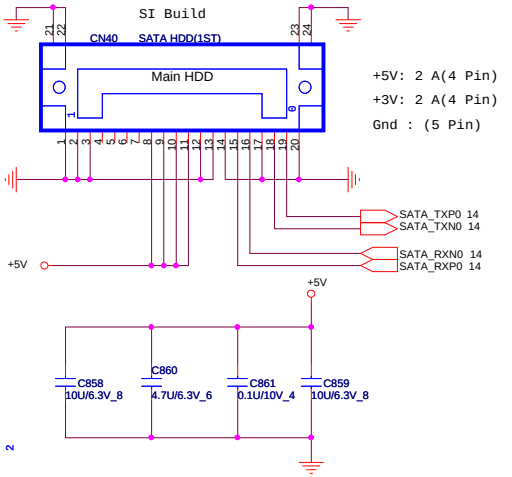
Power trace Layout 寬度> 30mil

NB5	PROJECT : UT12 Quanta Computer Inc.	
Size: Custom	Document Number: LAN Power	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 34 of 47	

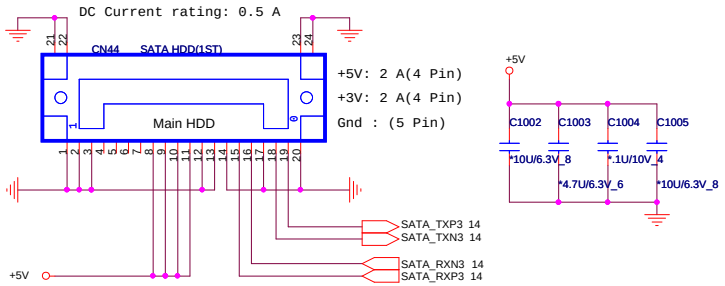
SATA CD-ROM



SATA_1 HDD CONNECTOR



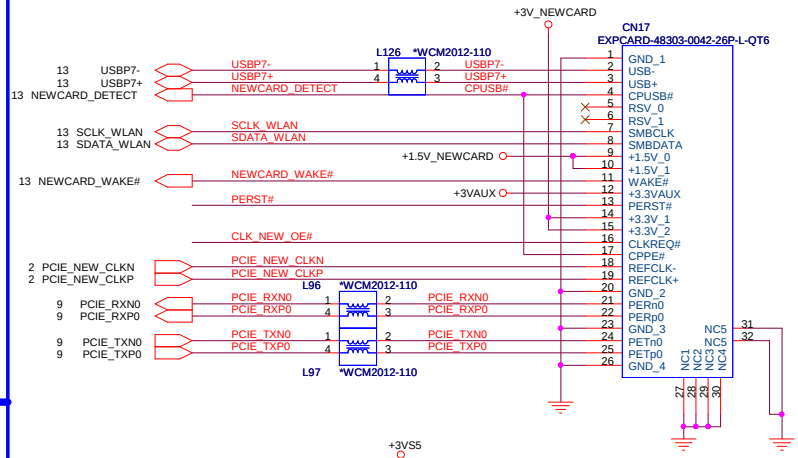
SATA_2 CONNECTOR

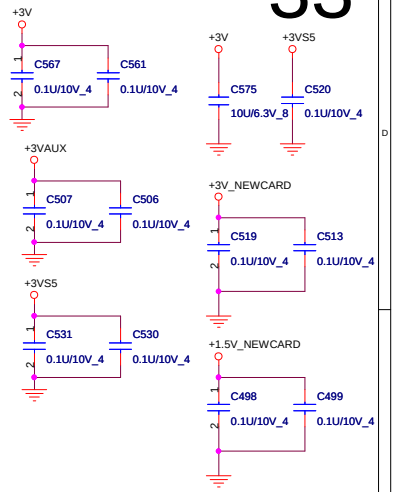


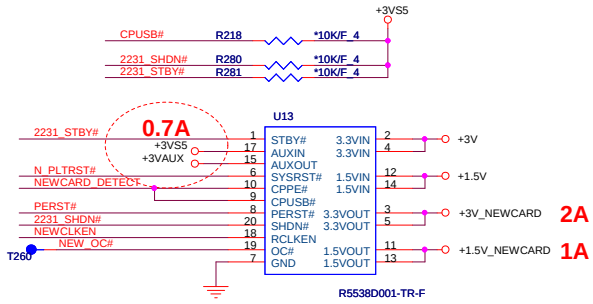
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

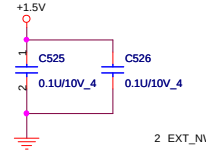
33

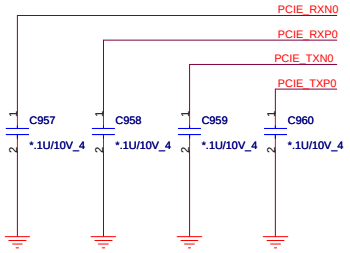


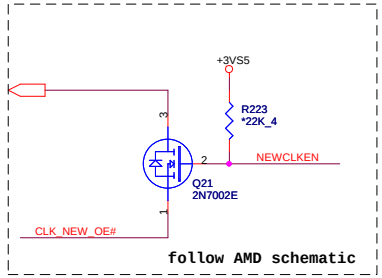


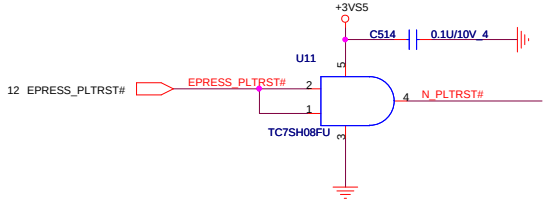


R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN









NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/SATA ODD/SATA HDD	1A

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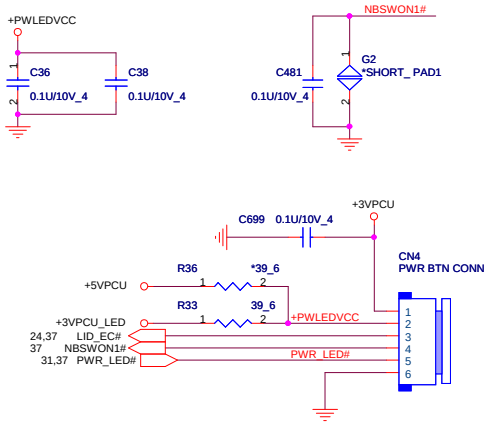
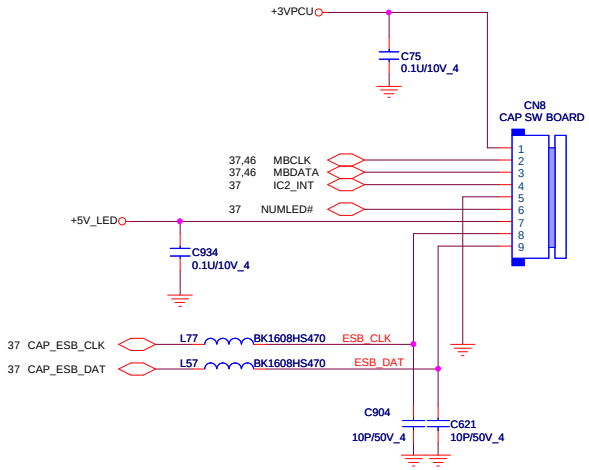
POWER BUTTON CONNECT

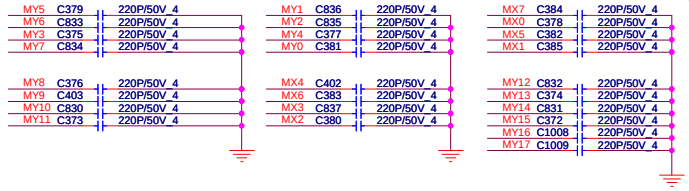


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

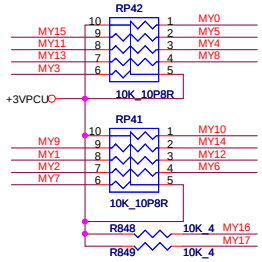
CAP SW CONNECT

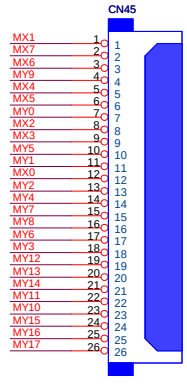


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

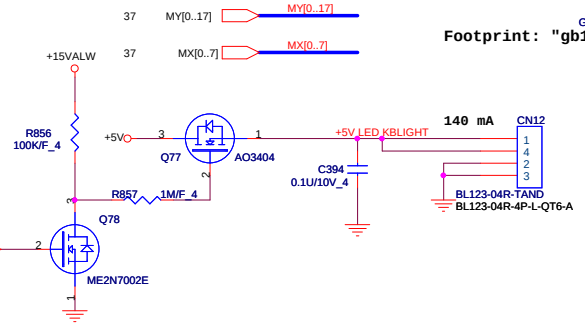


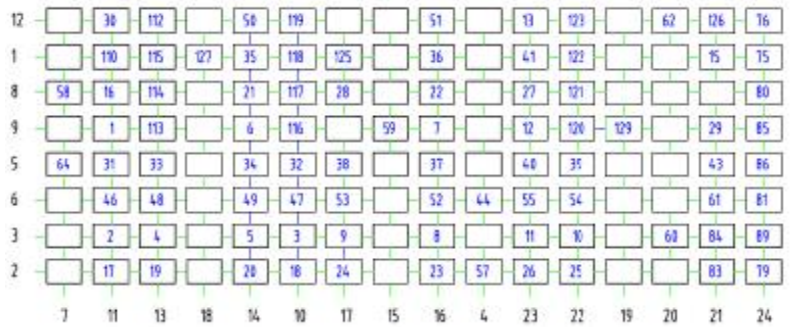
KEYBOARD PULL-UP





Footprint: "gb1rf260-1253-7f-26p-l





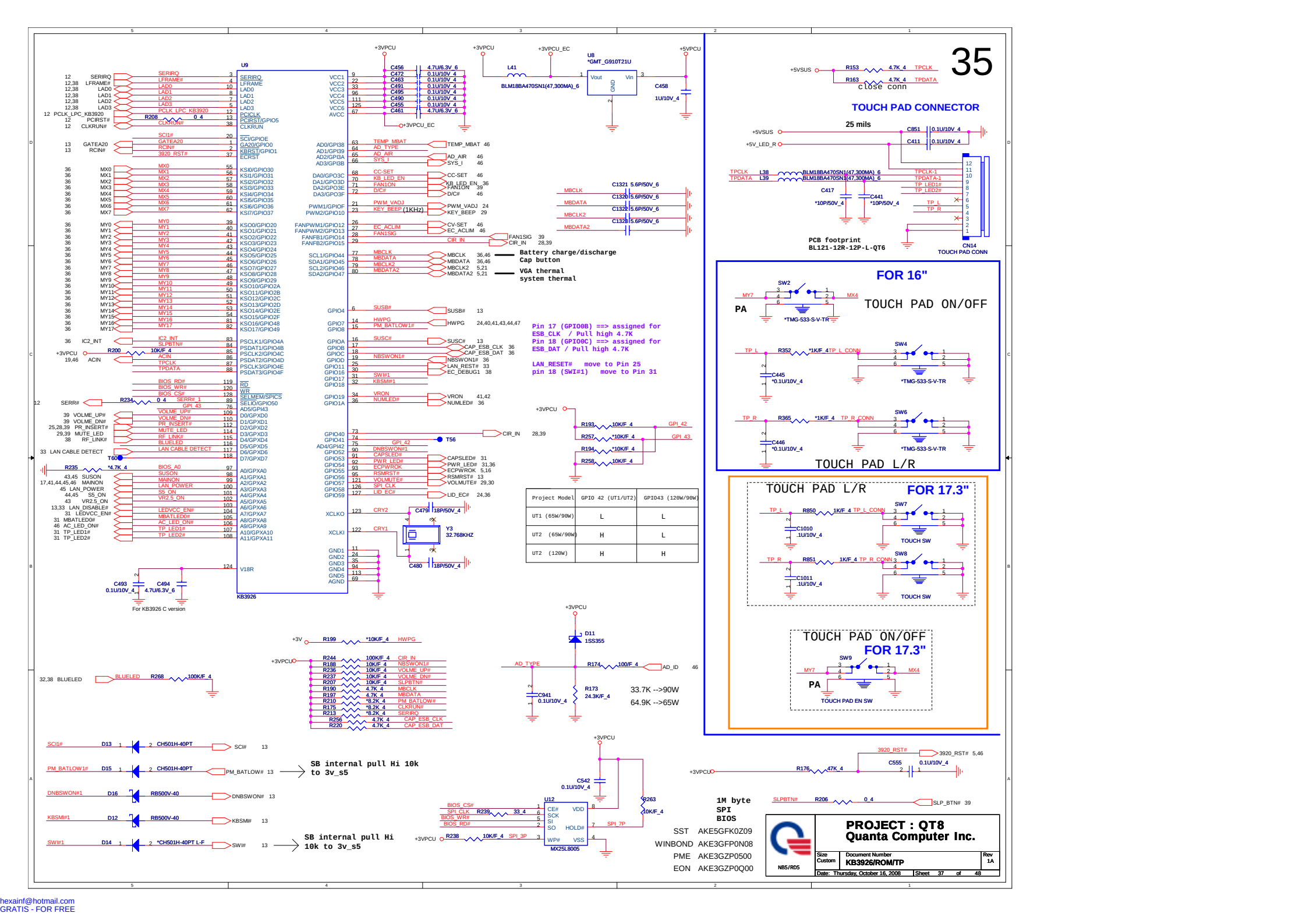
12		38	112		58	119			51		13	123		62	126	76
1		130	115	127	35	118	125		36		41	122			15	75
8	58	16	114		21	117	28		22		27	121				80
9		1	113		6	116		59	7		12	120	129		29	85
5	64	31	33		34	32	38		37		40	35			43	86
6		46	48		49	47	53		52	44	55	54			61	81
3		2	4		5	3	9		8		11	10		60	84	89
2		17	19		20	18	24		23	57	26	25			83	79
	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

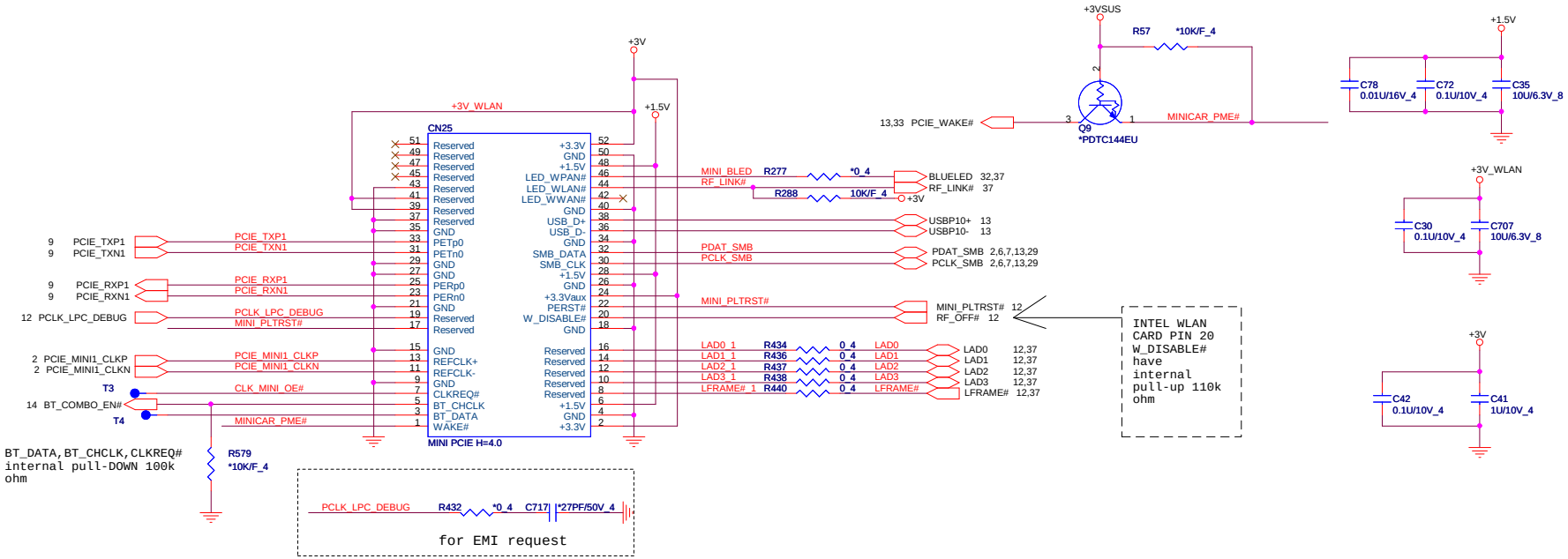
Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

Date: Thursday, October 16, 2008 | Sheet 36 of 48

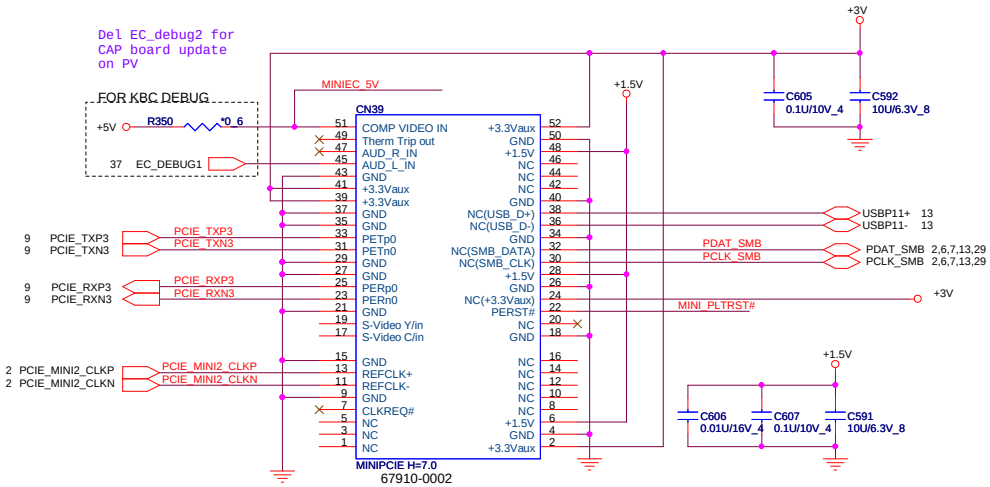


Project Model	GPIO 42 (UT1/UT2)	GPIO43 (120W/90W)
UT1 (65W/90W)	L	L
UT2 (65W/90W)	H	L
UT2 (120W)	H	H

Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 TV tuner card

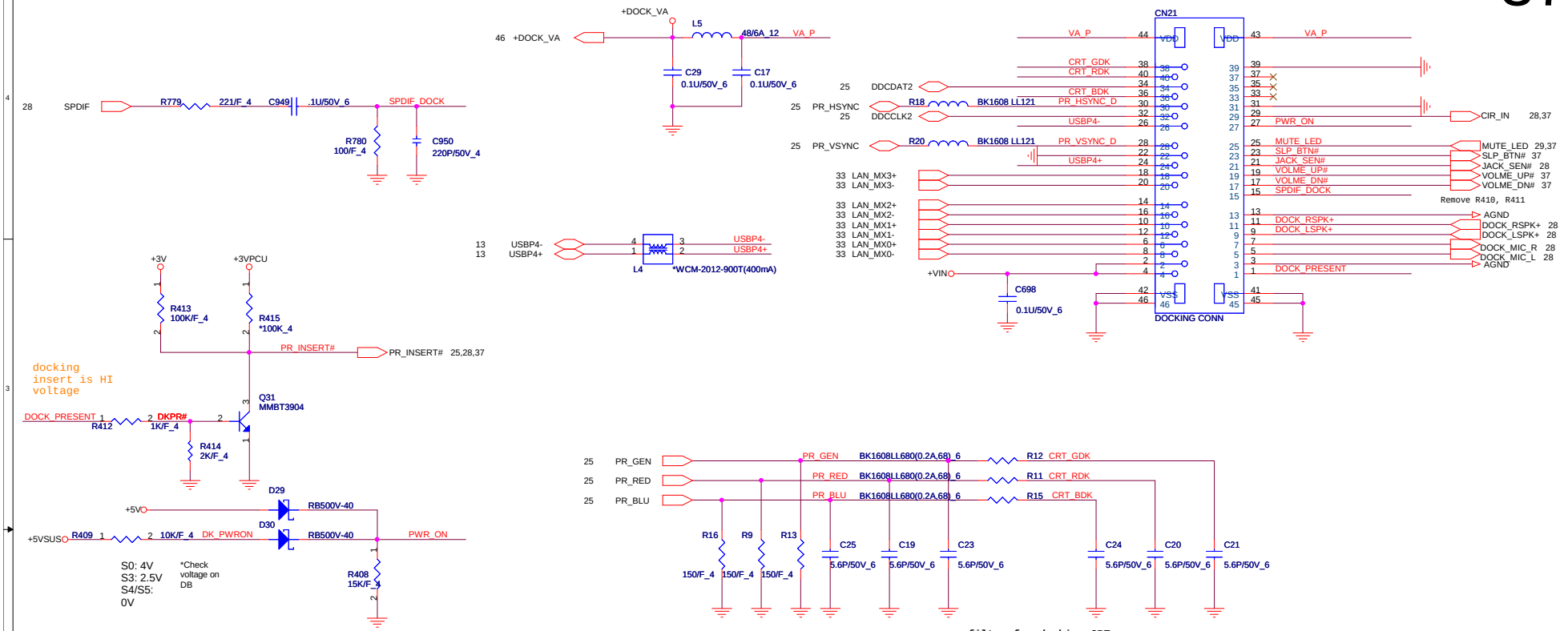


NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: Mini CARD X 3	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 38 of 48	

CABLE DOCK

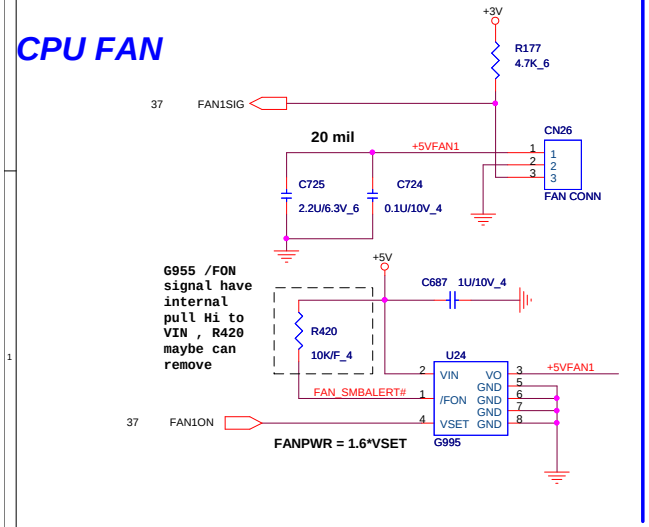
support 6A 200mils
CX000480005

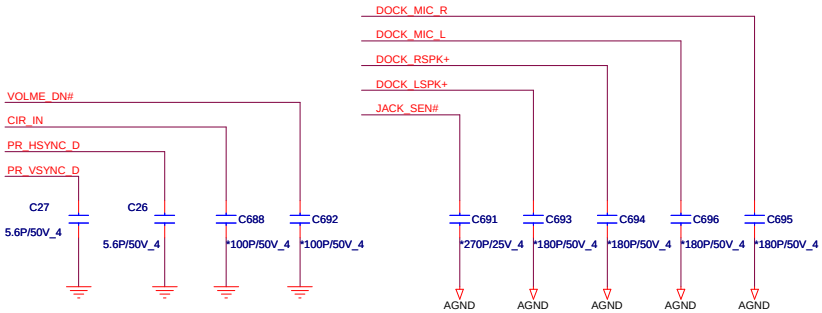
37

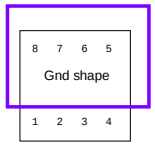


filter for docking CRT

CPU FAN







G995 layout notice

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

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+3V 2,3,5,6,7,10,11,12,13,14,15,16,17,21,24,25,26,27,28,29,30,31,32,33,35,37,38,39,41,45

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+5VPCU 28,29,36,37,41,42,43,44,47
+3VPCU 5,12,24,31,32,36,37,39,42,43,44,46
+3VSUS 13,32,38,41,43,44,45
+3VS5 5,7,12,13,14,15,16,24,27,35,45
+5VSUS 24,32,37,39,45
+5V 5,15,20,24,25,26,28,29,31,32,35,36,38,39,44,45
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Del PR159 for TP on PV

Rds(on) 15m ohm

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1
For EMI-SI

+5VSUS
4.5A
S0-S3
For EMI-SI

+LANVCC
0.27A

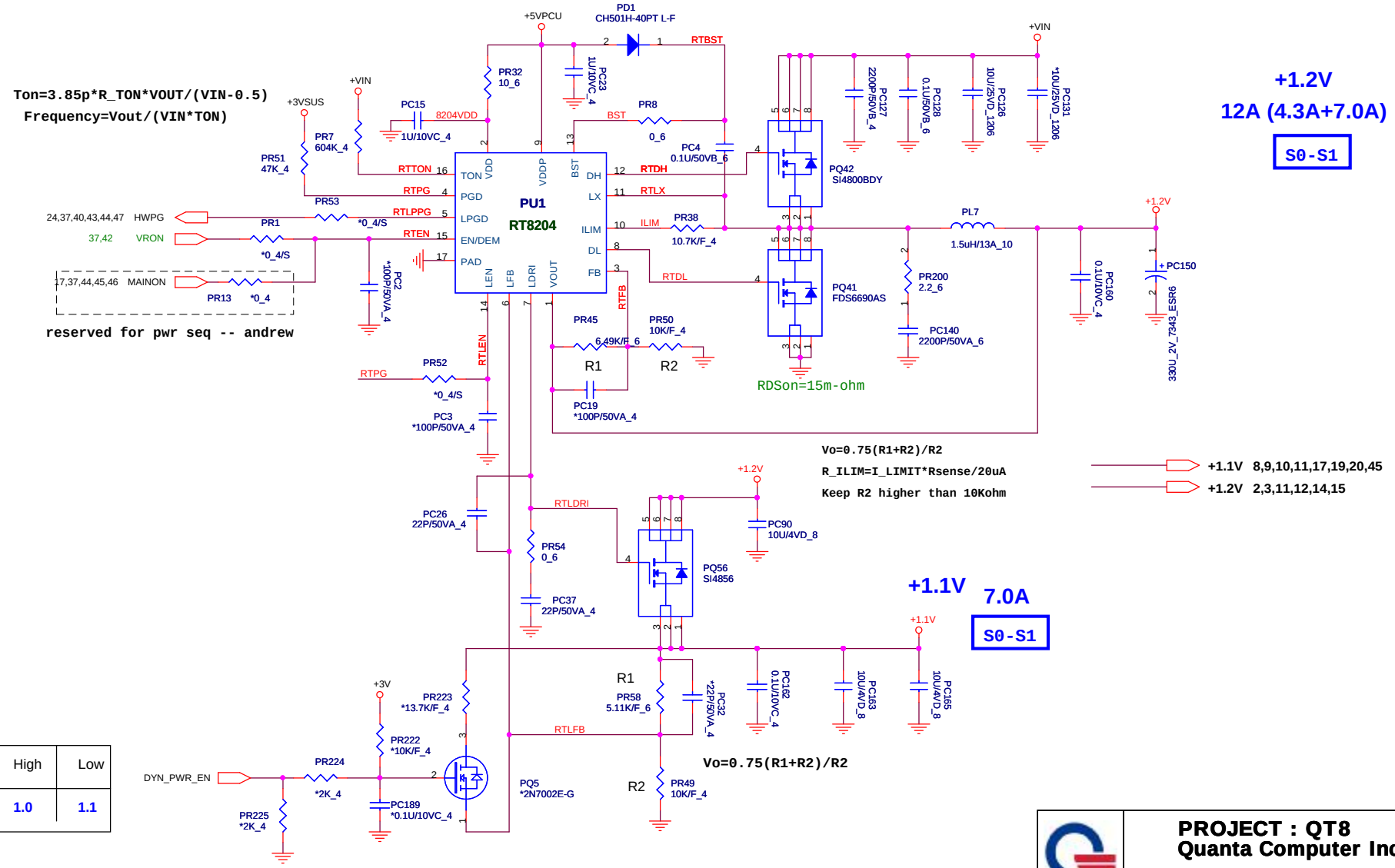
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V(ISL6237)	1A

Date: Thursday, October 16, 2008 Sheet 40 of 48

NB5/RD5

+1.1V & +1.2V



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

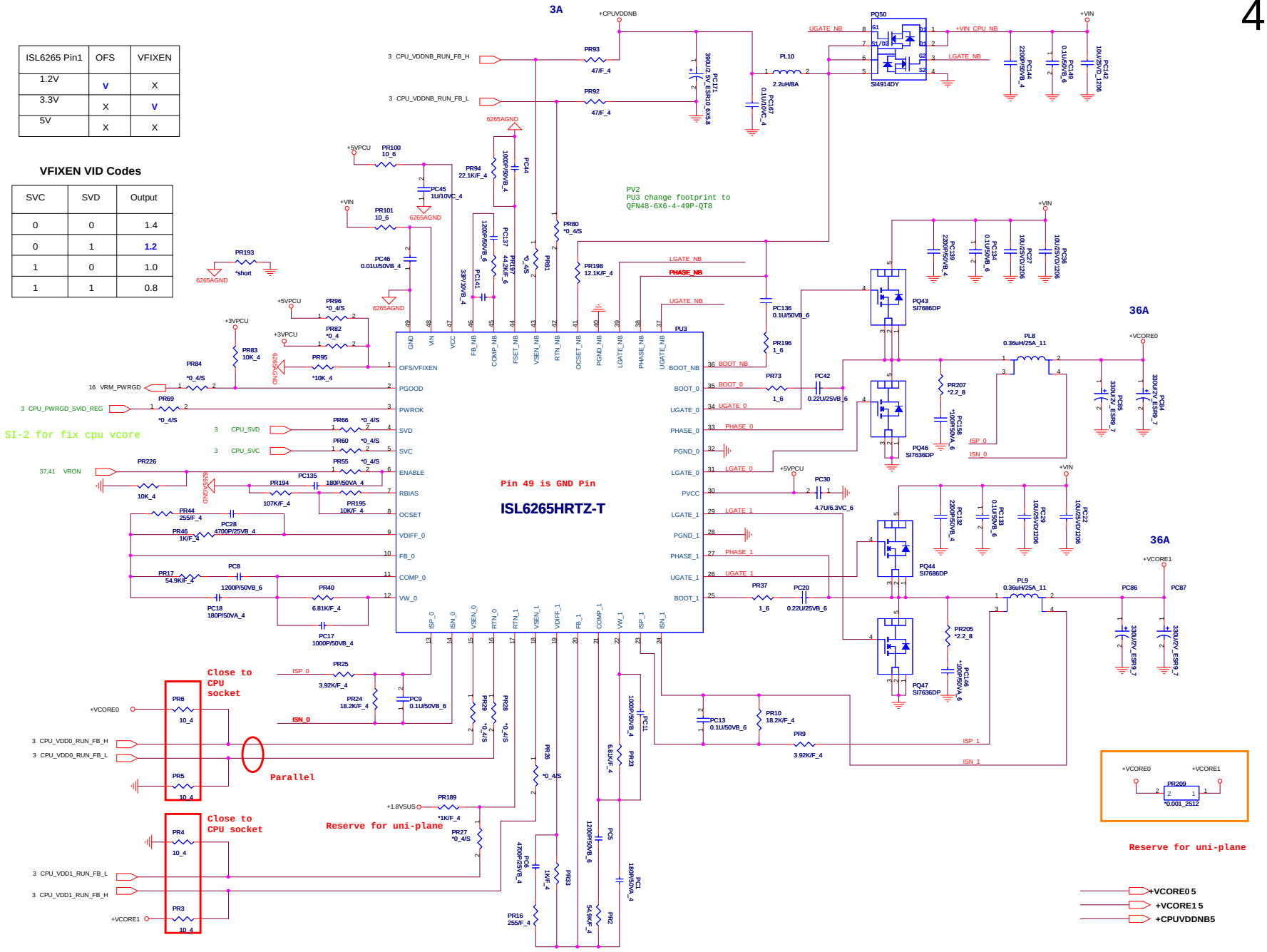
Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	1A

Date: Thursday, October 16, 2008 | Sheet 41 of 48

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_CORE(ISL6265)	1A

N85/RD5

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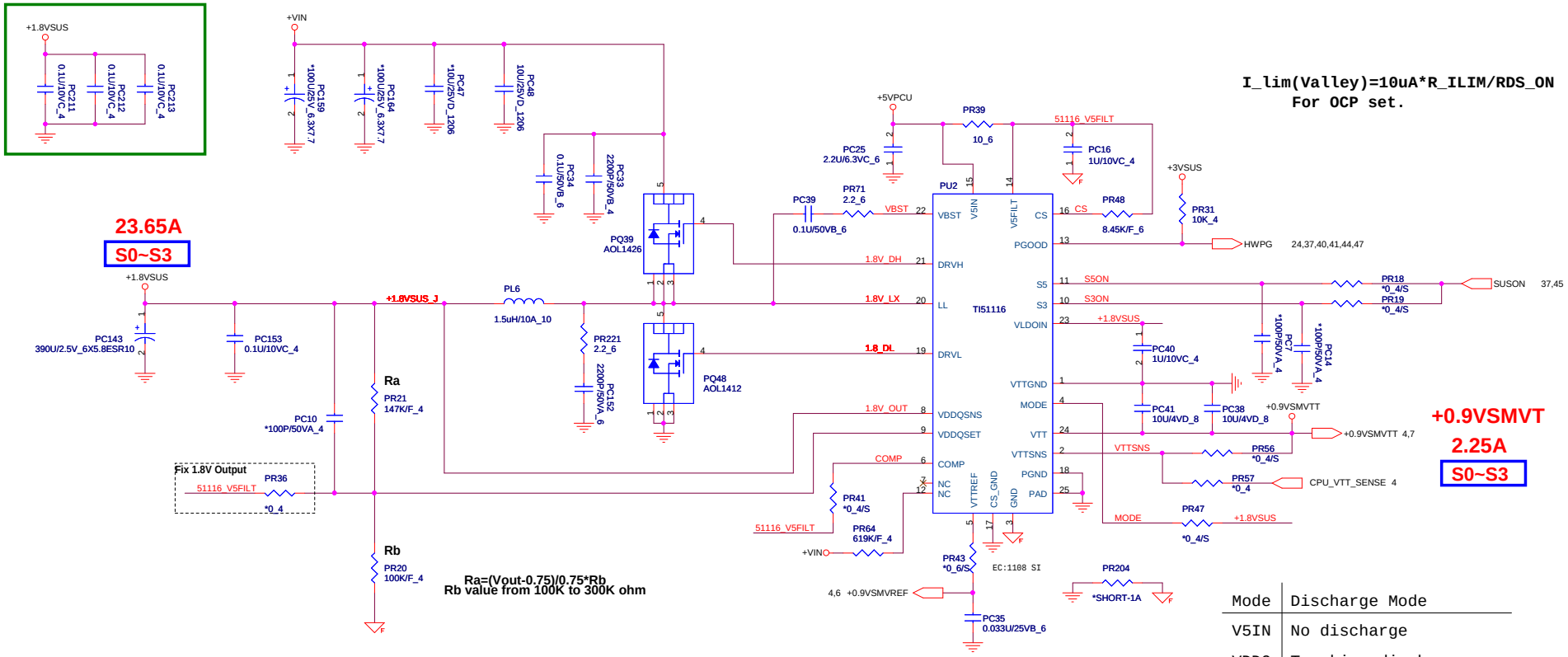
+2.5V 3
+1.8VSUS 3,4,5,6,7,42,44,47

Add 0.1u CAP PC211, PC212, PC213 for EMI



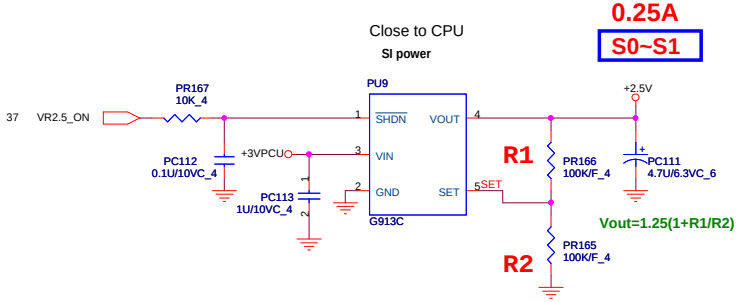
I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

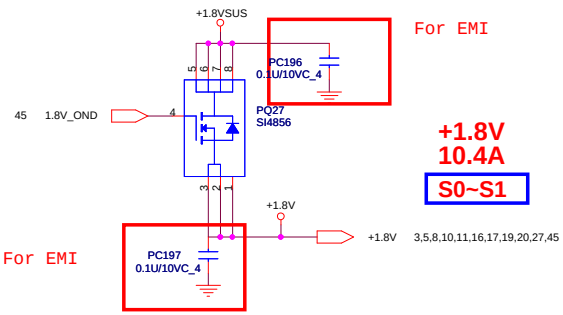
Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V





For EMI

Discrete:SI4856
UMA:SI4800

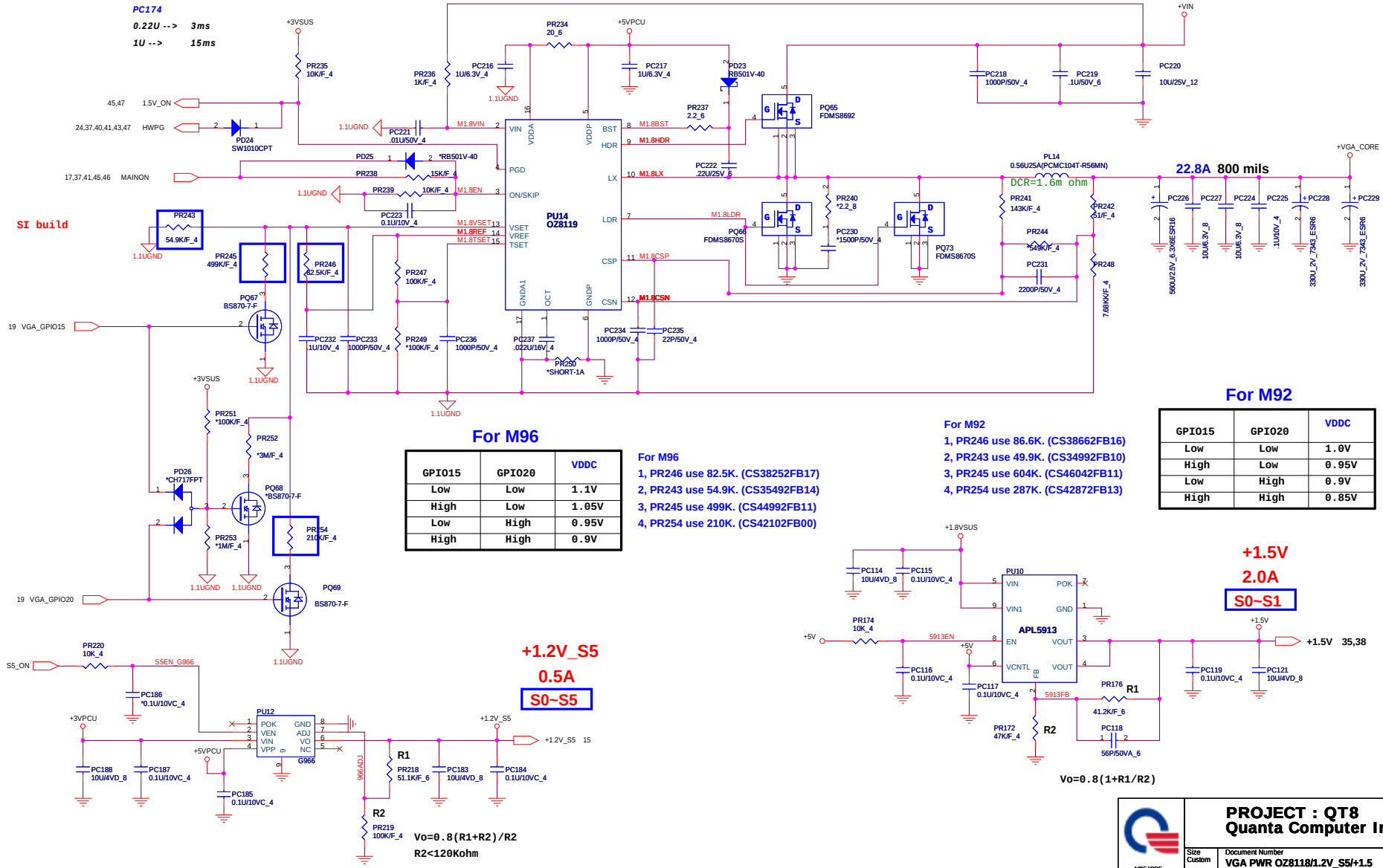
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A
Date: Thursday, October 16, 2008	Sheet 43 of 48	

NB5/RD5

VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



For M96

GPIO15	GPIO20	VDDC
Low	Low	1.1V
High	Low	1.05V
Low	High	0.95V
High	High	0.9V

For M96
1, PR246 use 82.5K. (CS38252FB17)
2, PR243 use 54.9K. (CS35492FB14)
3, PR245 use 499K. (CS44992FB11)
4, PR254 use 210K. (CS42102FB00)

For M92
1, PR246 use 86.6K. (CS38662FB16)
2, PR243 use 49.9K. (CS34992FB10)
3, PR245 use 604K. (CS46042FB11)
4, PR254 use 287K. (CS42872FB13)

For M92

GPIO15	GPIO20	VDDC
Low	Low	1.0V
High	Low	0.95V
Low	High	0.9V
High	High	0.85V

+1.2V_S5
0.5A
S0~S5

+1.5V
2.0A
S0~S1

Vo=0.8(R1+R2)/R2
R2<120Kohm

Vo=0.8(1+R1/R2)

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	VGA PWR OZ8118/1.2V_S5/+1.5	1A

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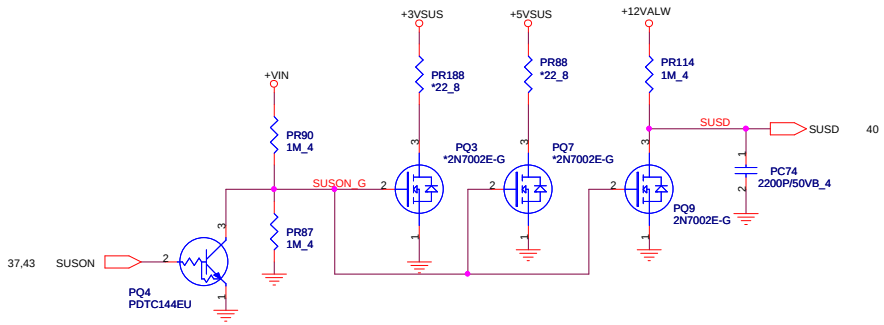
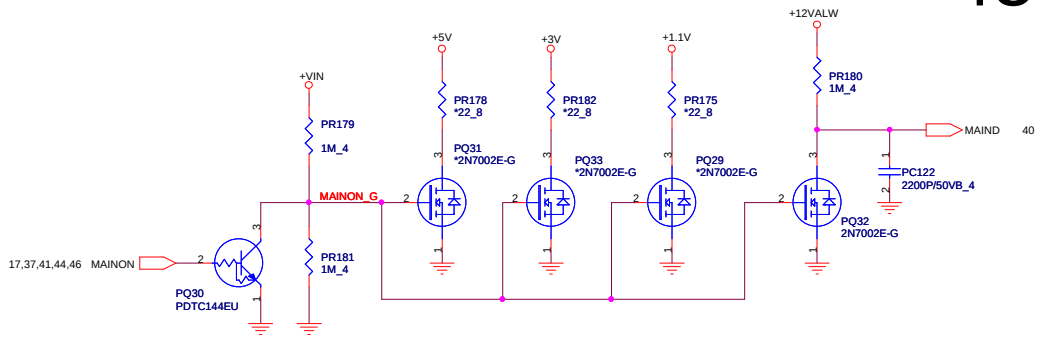
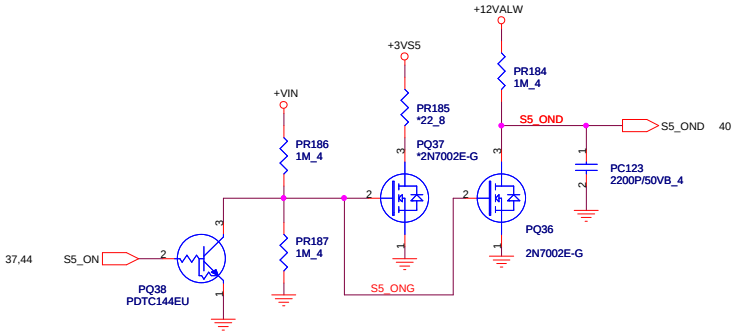
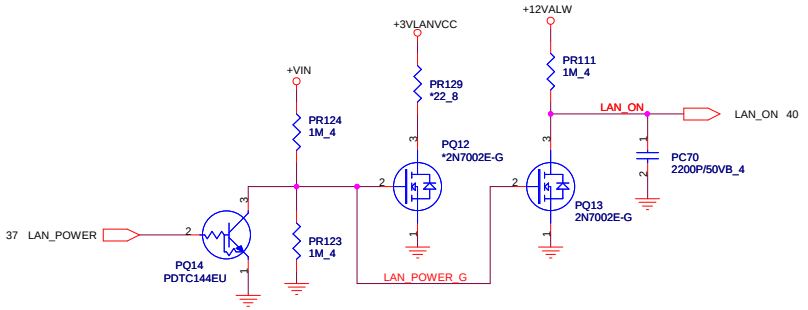
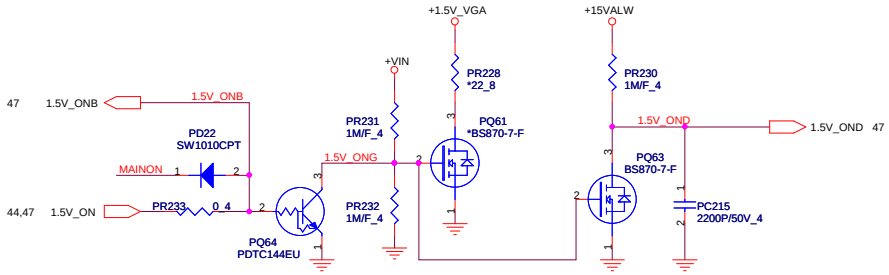


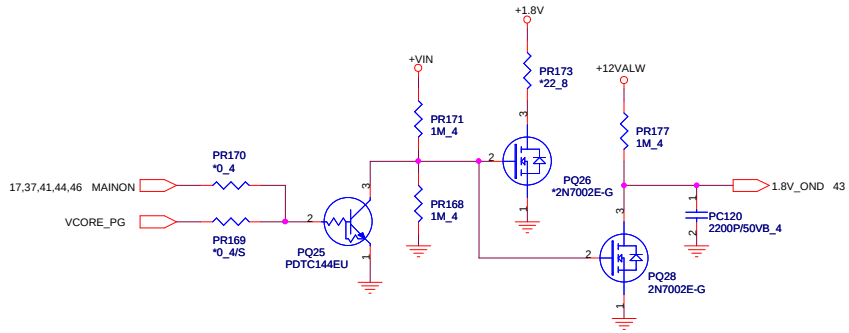




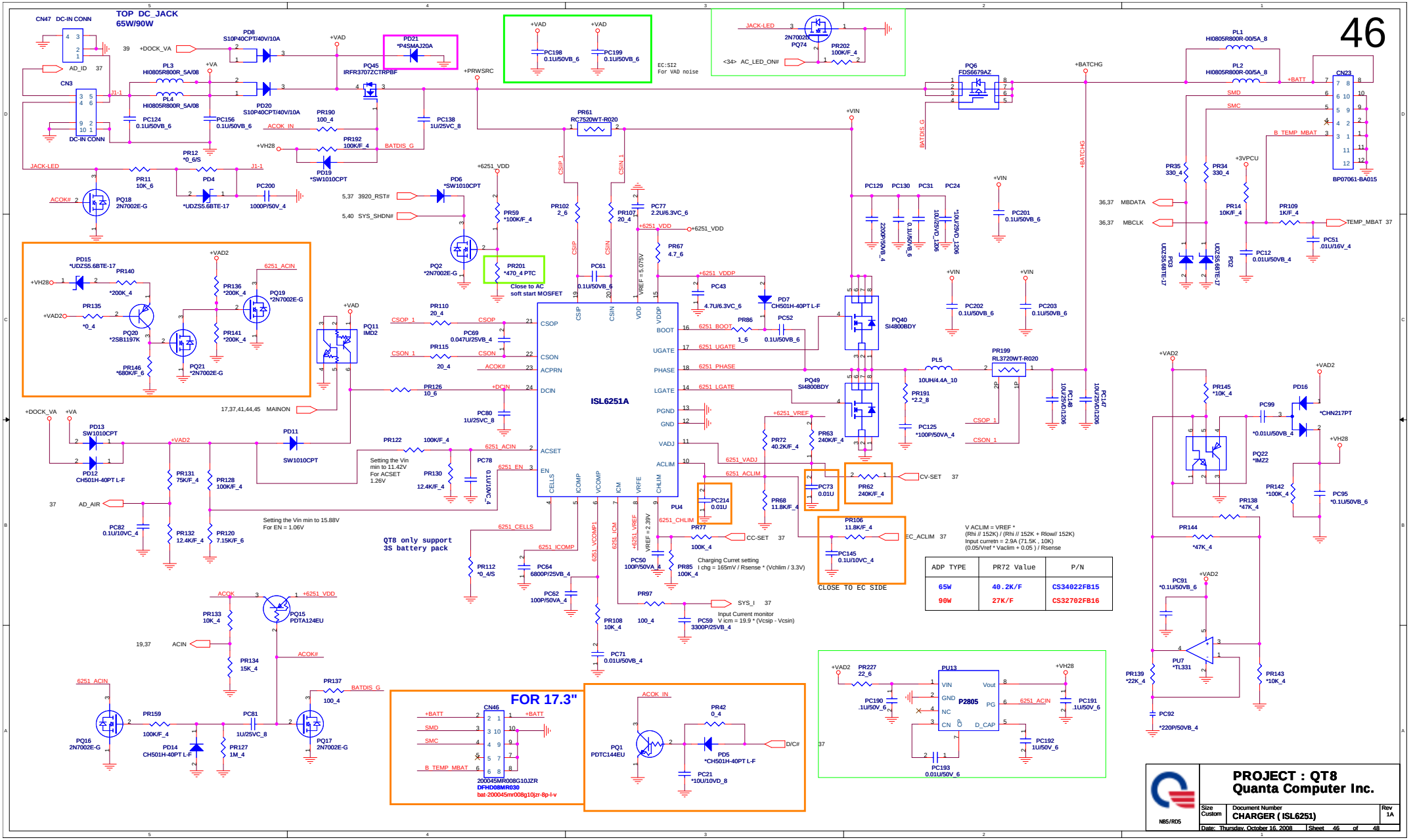


For Discrete Only





NB5/RD5	**PROJECT : QT8** **Quanta Computer Inc.**	
Size: Custom	Document Number: **DISCHARGE**	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 45 of 48	


TOP DC_JACK
65W/90W
CN47 DC-IN CONN
DC-IN CONN
CN3
PL3 HI0805R800R-5A/08
PL4 HI0805R800R-5A/08
PD8 S10P40CPT/40V/10A
PD20 S10P40CPT/40V/10A
PD21 *P4SMAJ20A
PQ45 IRFR3707ZCTRPBF
PR61 RC7520WT-R020
PQ6 FDS6679AZ
PL1 HI0805R800R-00/5A_8
PL2 HI0805R800R-00/5A_8
CN23
BP07061-BA015
ISL6251A
PQ40 SI4800BDY
PQ49 SI4800BDY
PL5 10UH/4.4A_10
PD7 CH501H-40PT L-F
PD11 SW1010CPT
PD12 CH501H-40PT L-F
PD13 SW1010CPT
PQ11 IMD2
PU4
PU7 *TL331
PU13 P2805
PQ1 PDTC144EU
PQ15 PDTA124EU
PQ16 2N7002E-G
PQ17 2N7002E-G
PQ18 2N7002E-G
PQ2 *2N7002E-G
PQ19 *2N7002E-G
PQ20 *2SB1197K
PQ21 *2N7002E-G
PQ22 *IMZ2
PD14 CH501H-40PT L-F
PD15 *UDZS5.6BTE-17
PD16 *CHN217PT
PD17 *UDZS5.6BTE-17
PD18 *UDZS5.6BTE-17
PD19 *SW1010CPT
PD6 *SW1010CPT
PQ74 2N7002E
FOR 17.3"
CN46
200045MR008G10JZR
DFHD08MR030
bat-200045mr008g10jzr-8p-l-v
CLOSE TO EC SIDE
Close to AC soft start MOSFET
Setting the Vin min to 11.42V For ACSET 1.26V
Setting the Vin min to 15.88V For EN = 1.06V
QT8 only support 3S battery pack
Charging Curret setting I chg = 165mV / Rsense * (Vchlim / 3.3V)
Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)
V ACLIM = VREF * (Rhi // 152K) / (Rhi // 152K + Rlow// 152K)
Input curretn = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense
EC:SI2 For VAD noise
ADP TYPE | PR72 Value | P/N
65W | 40.2K/F | CS34022FB15
90W | 27K/F | CS32702FB16
PROJECT : QT8
Quanta Computer Inc.
CHARGER (ISL6251)
Size Custom
Document Number
Rev 1A
Date: Thursday, October 16, 2008
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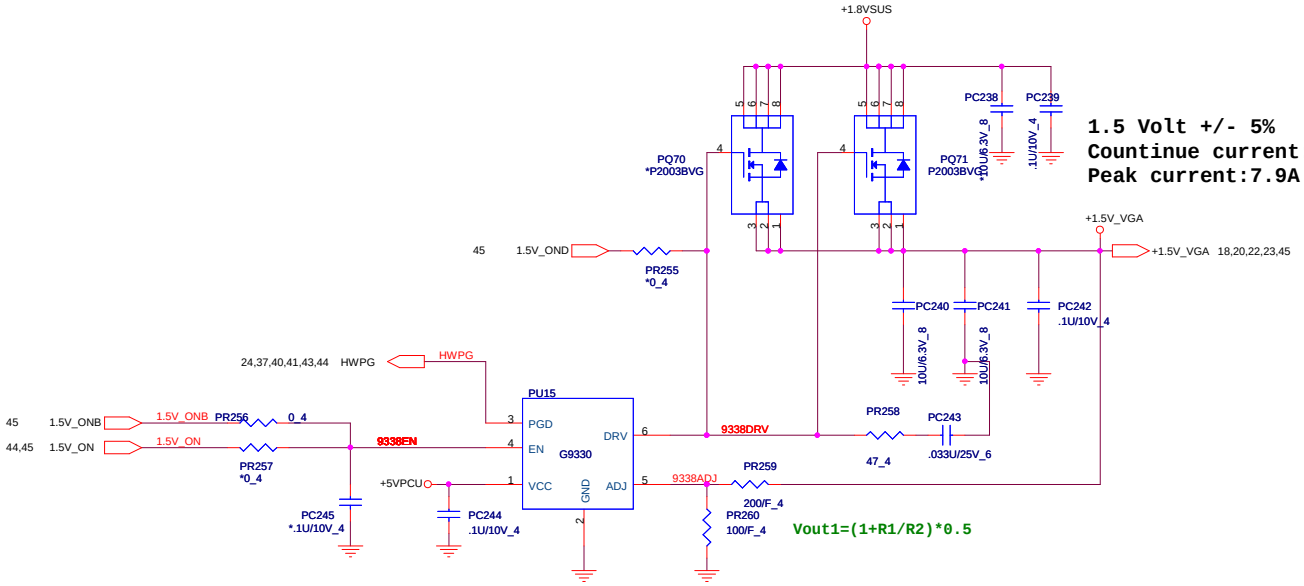
N85/RD5



VRAM	Mounted	N/A	PQ33 P/N
Others	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	PR232	BAM44960000
Samsung	PR232	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	BAM48560029

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5V_VGA	DB

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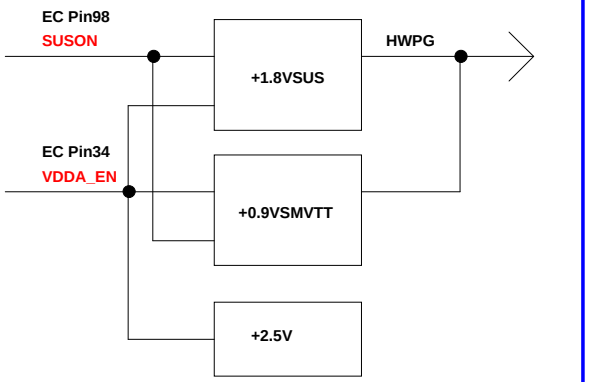
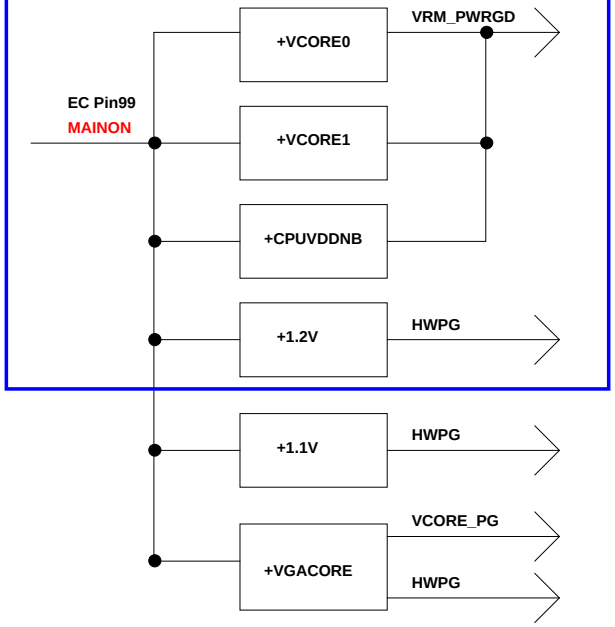
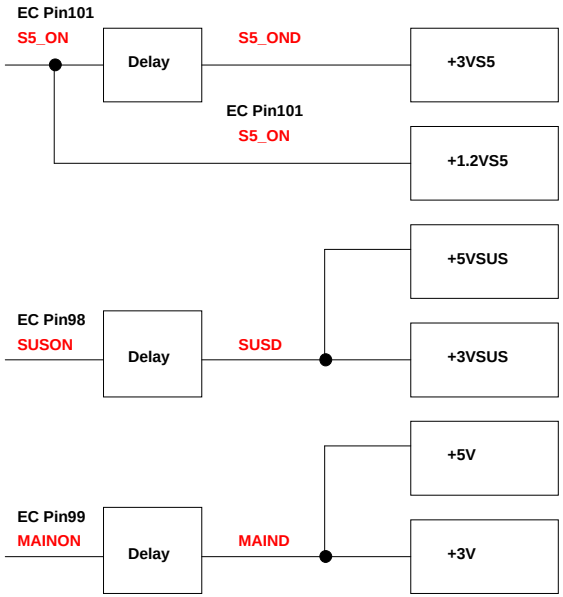
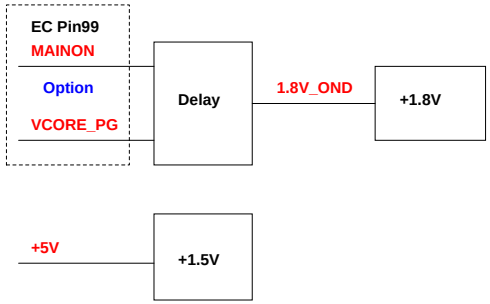
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

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