

**PCB STACK UP**  
6L Dis.

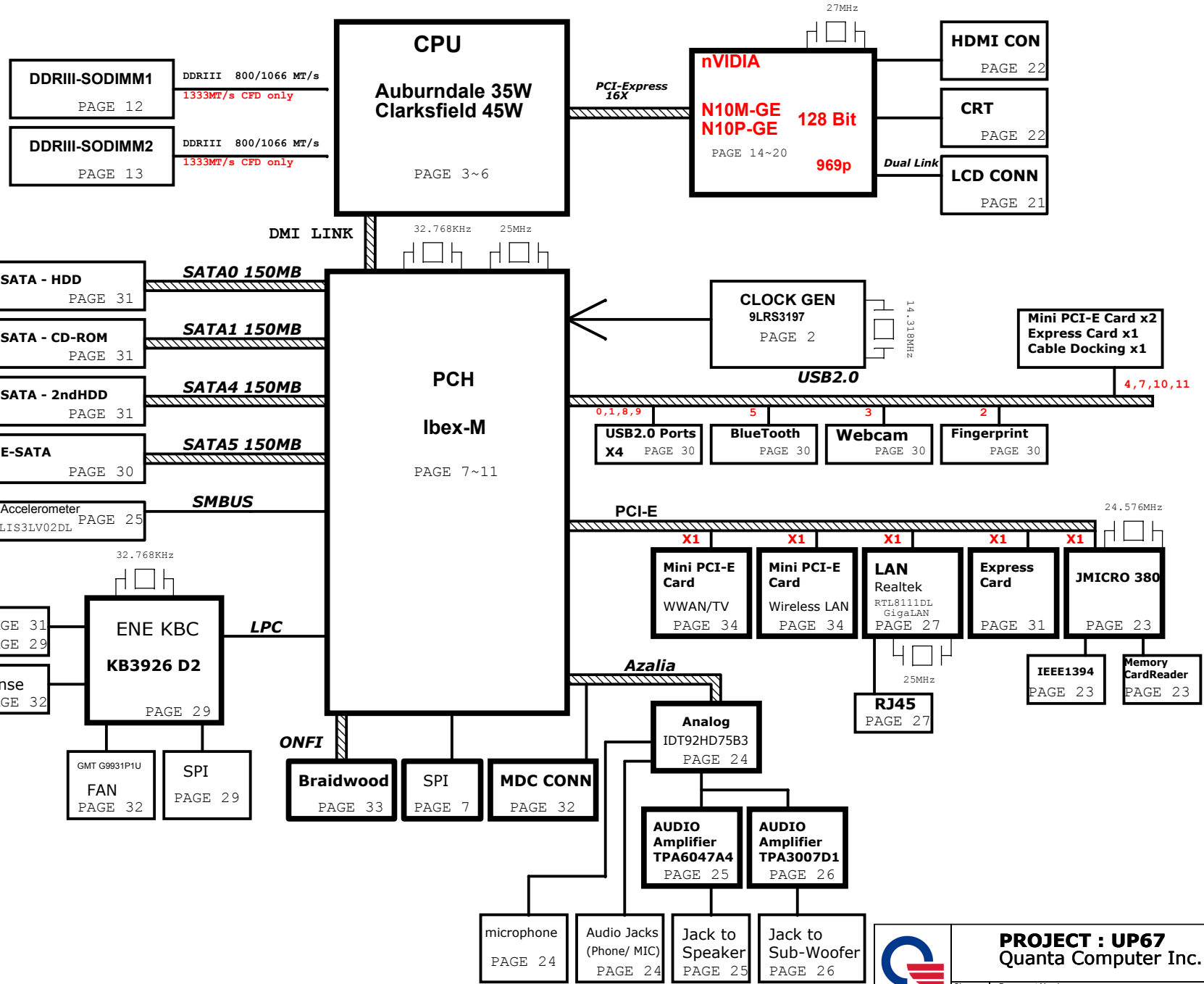
# Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

01

- LAYER 1 : TOP**  
**LAYER 2 : SGND**  
**LAYER 3 : IN1**  
**LAYER 4 : IN2**  
**LAYER 5 : SVCC**  
**LAYER 6 : BOT**

- Cable Docking**
- VGA
  - RJ-45
  - CIR/Pwr btn
  - SPDIF Out
  - Stereo MIC
  - Headphone Jack
  - USB Port
  - VOL Cntr
- PAGE 32

- SYSTEM POWER RT8206B** PAGE 35
- VCCP +1.1VT(RT8208A) AND PCH 1.05V(RT8204)** PAGE 36
- CPU CORE ISL6251A** PAGE 41
- VGACORE(1.025V) RT8208A** PAGE 38
- DDR III SMD DR\_VTERM 1.5V/1.5VSUS(RT8207)** PAGE 39
- SYSTEM CHARGER(ISL6251AHAZ-T)** PAGE 40

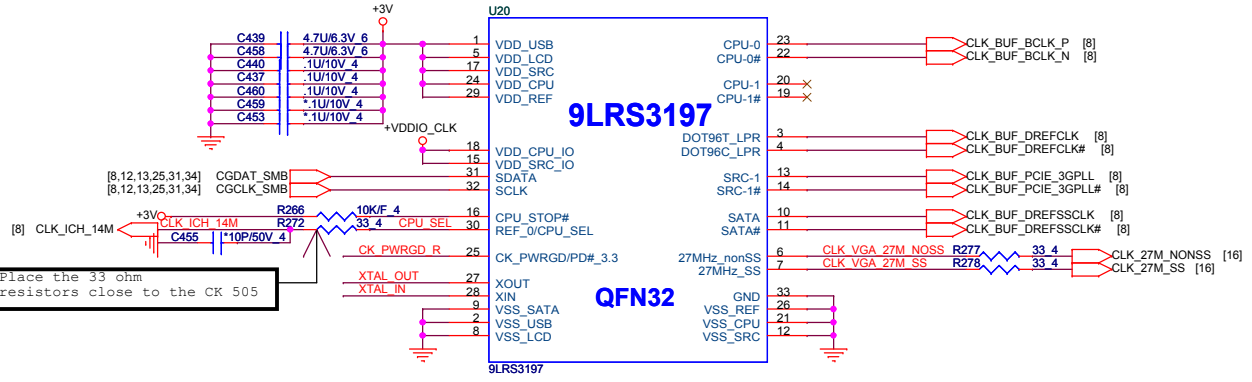
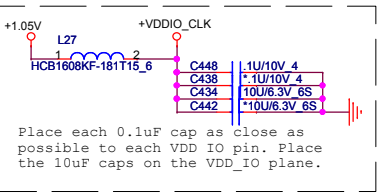


**PROJECT : UP67**  
Quanta Computer Inc.

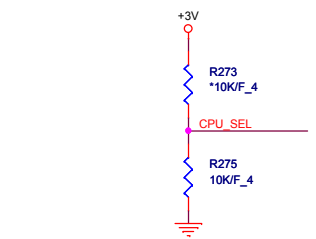
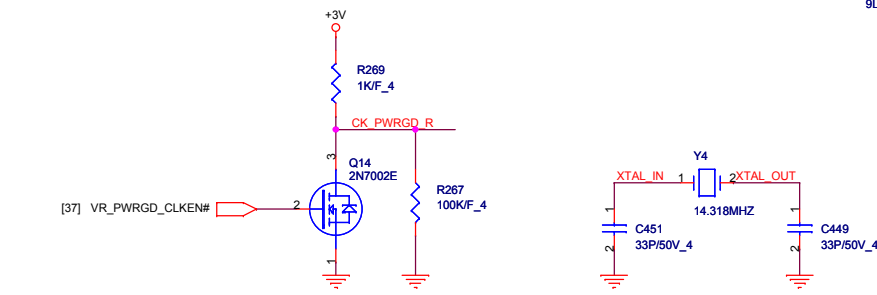
Size Custom Document Number BLOCK DIAGRAM Rev 1A

NB5

Date: Monday, October 26, 2009 | Sheet 1 of 45

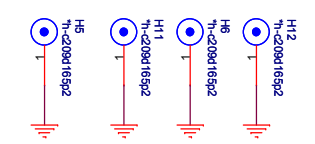


Place the 33 ohm resistors close to the CK 505

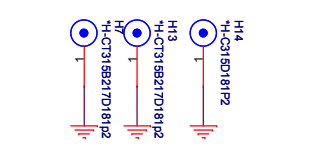


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

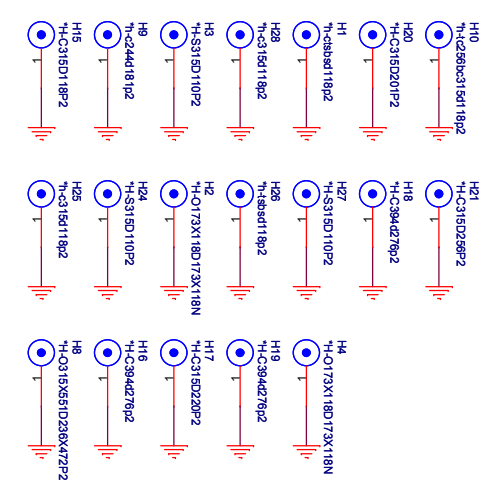
**CPU bracket Hole.**



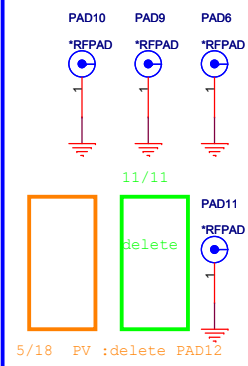
**VGA bracket Hole.**



**M/B Screw Hole**



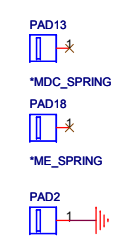
**RF PAD**



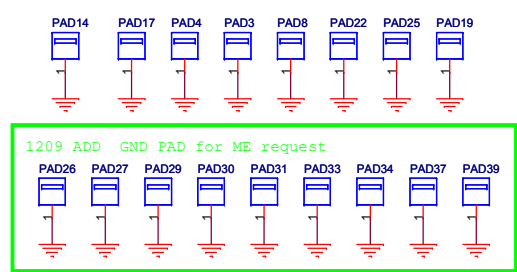
**ME PAD**



**Routed spring**



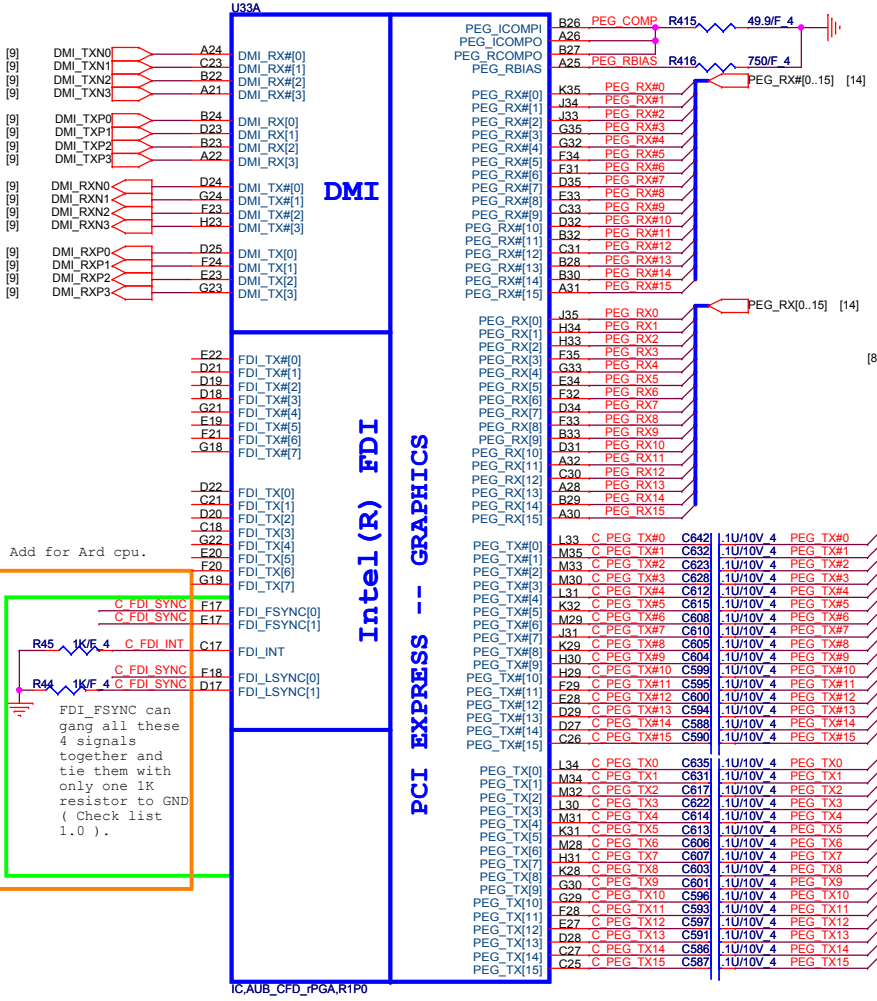
**ME-Ground Pad**



5/18 PV :delete PAD12

**PROJECT : UP67**  
Quanta Computer Inc.

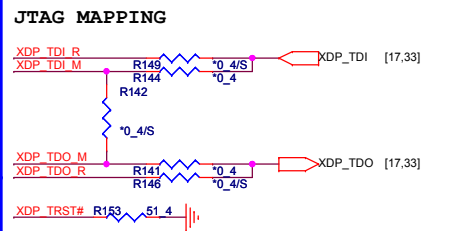
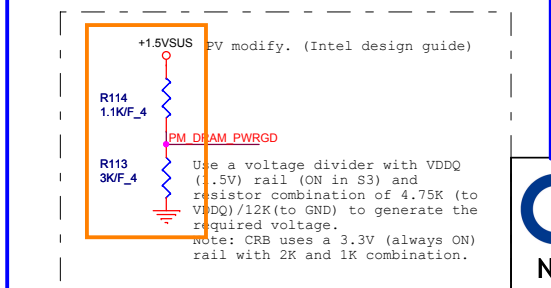
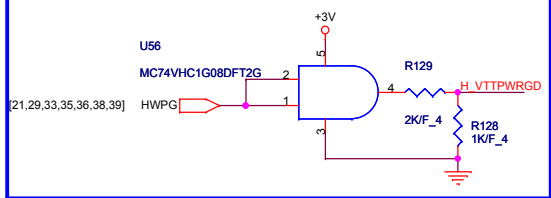
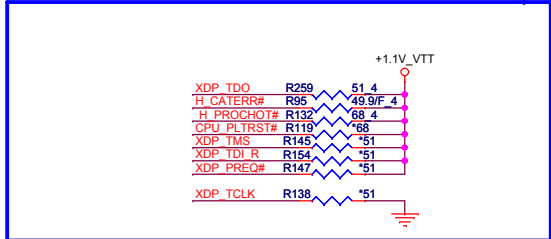
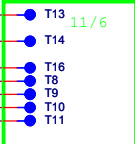
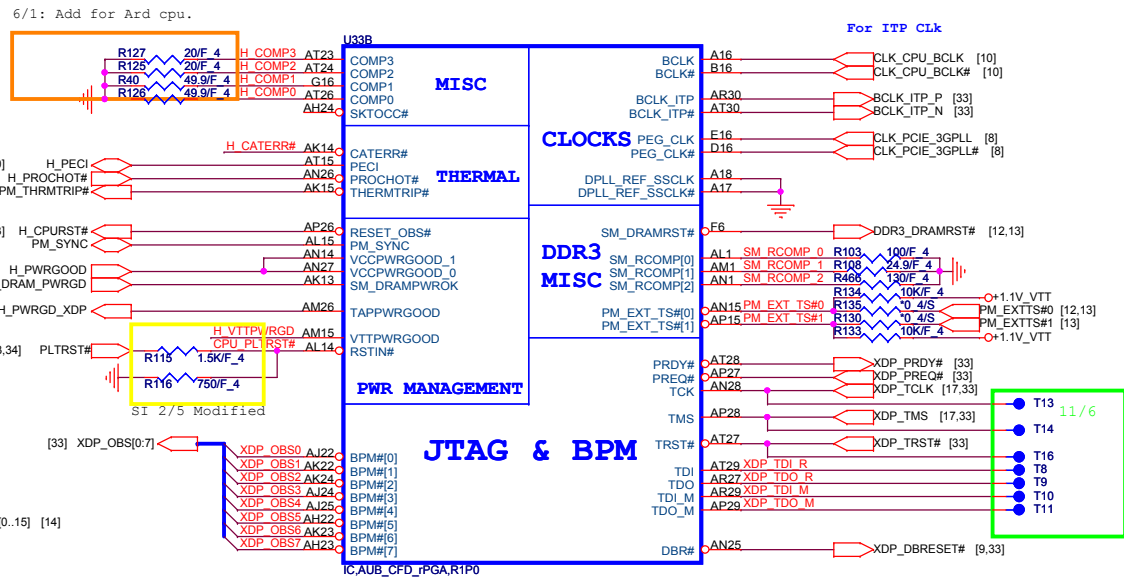
Size Custom	Document Number <b>CLOCK &amp; Screw Holes</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 2 of 45		



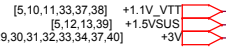
C FDI SYNC  
C FDI SYNC  
C FDI INT  
C FDI SYNC  
C FDI SYNC

R45 1K/F\_4  
R44 1K/F\_4

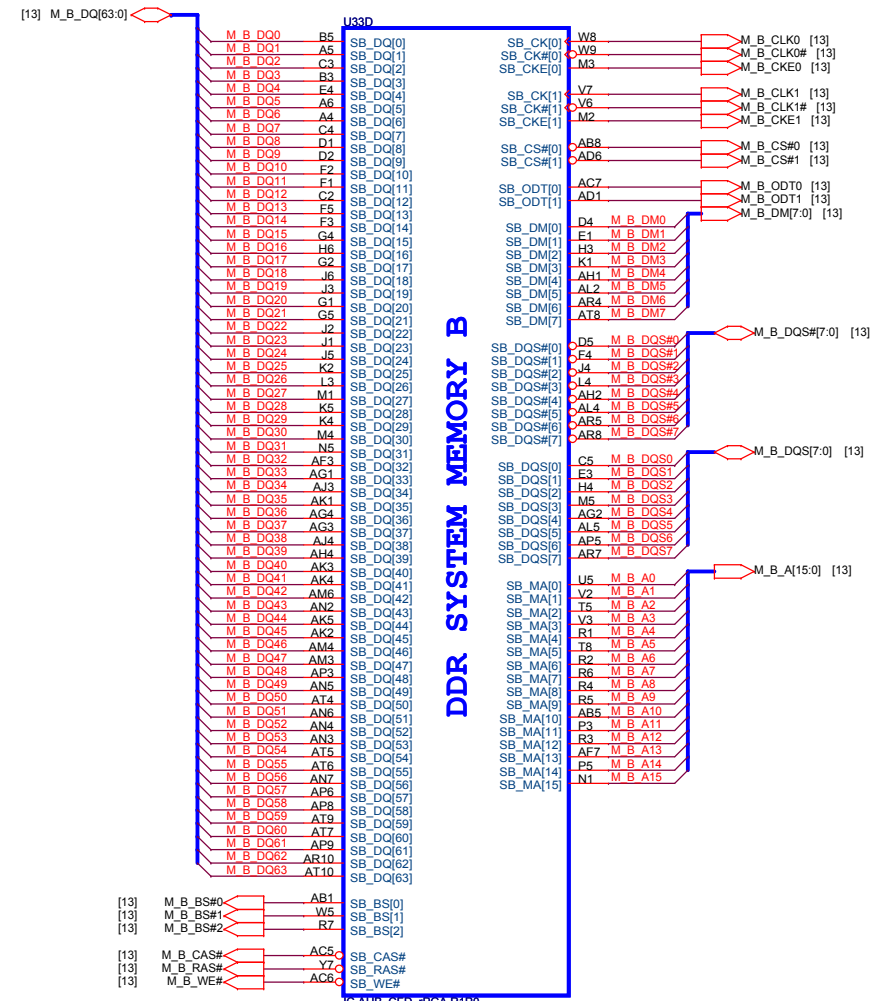
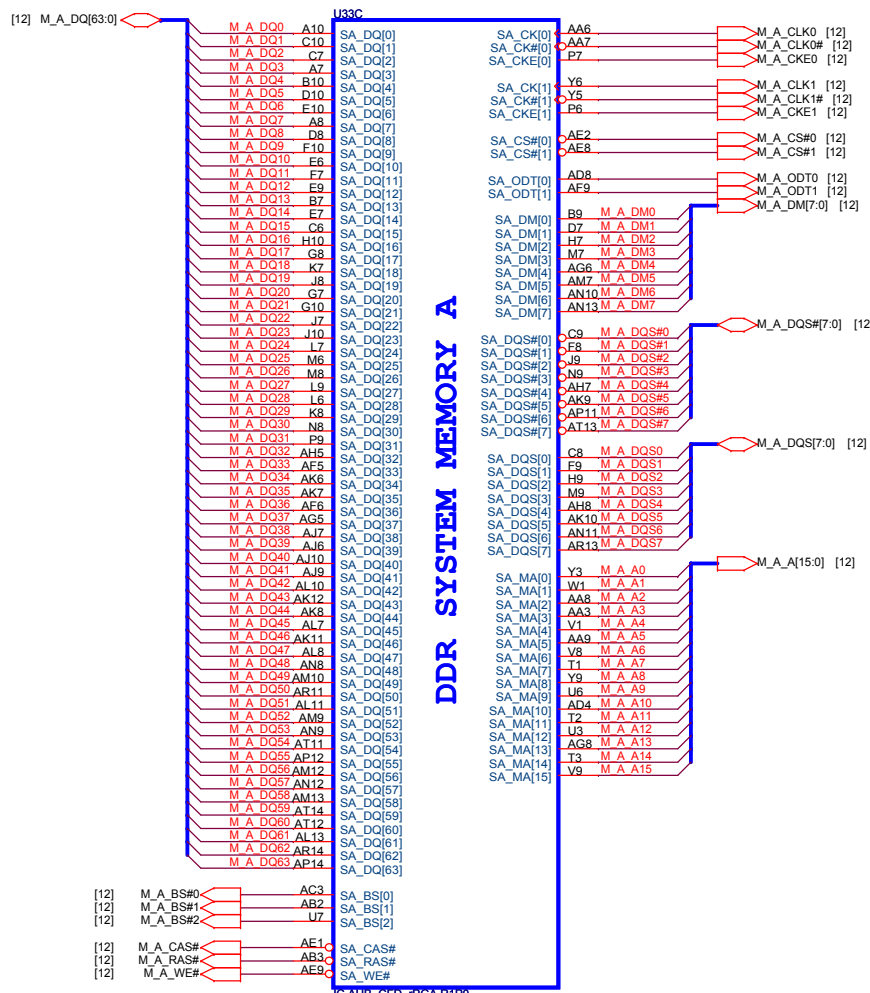
FDI\_FSXNC can gang all these 4 signals together and tie them with only one 1K resistor to GND ( Check list 1.0 ).

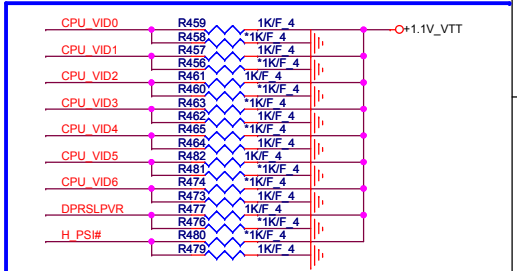
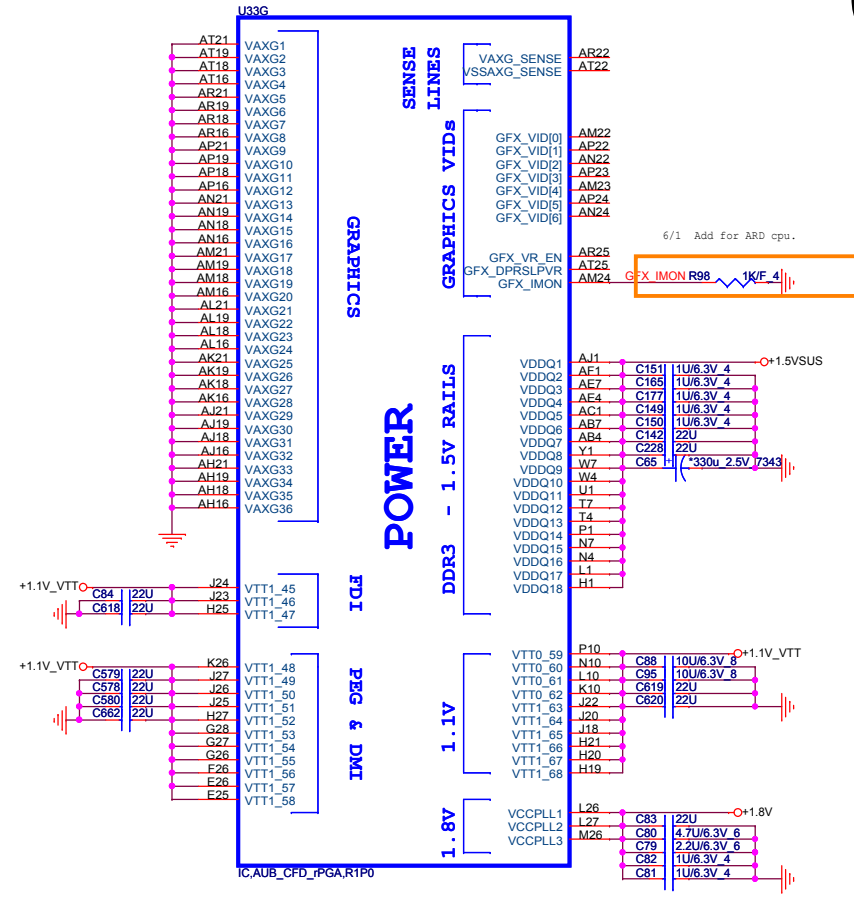
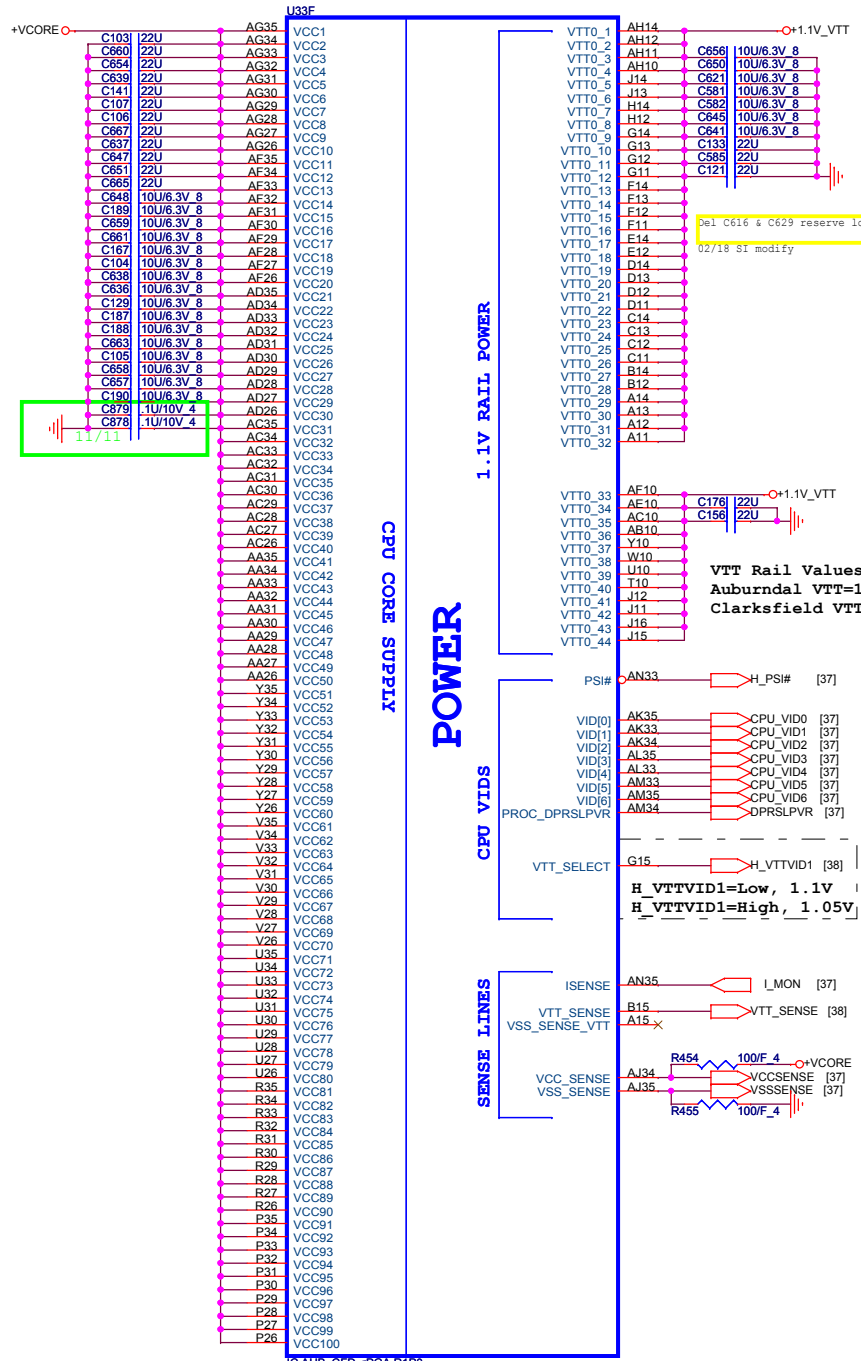


Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





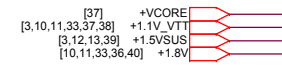
HFM\_VID : Max 1.4V  
LFM\_VID : Min 0.65V

**PROJECT : UP67**  
**Quanta Computer Inc.**

**NB5**

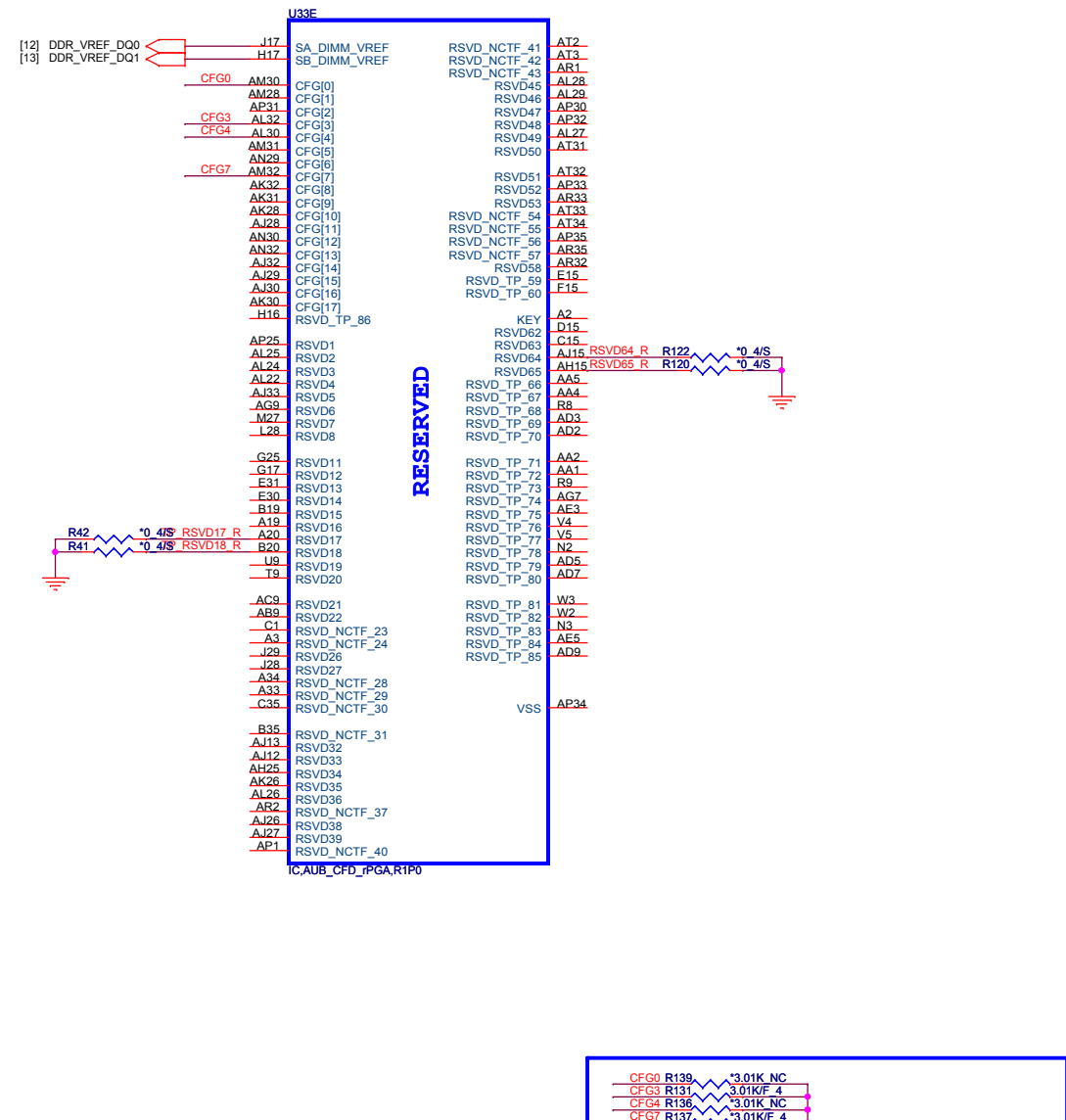
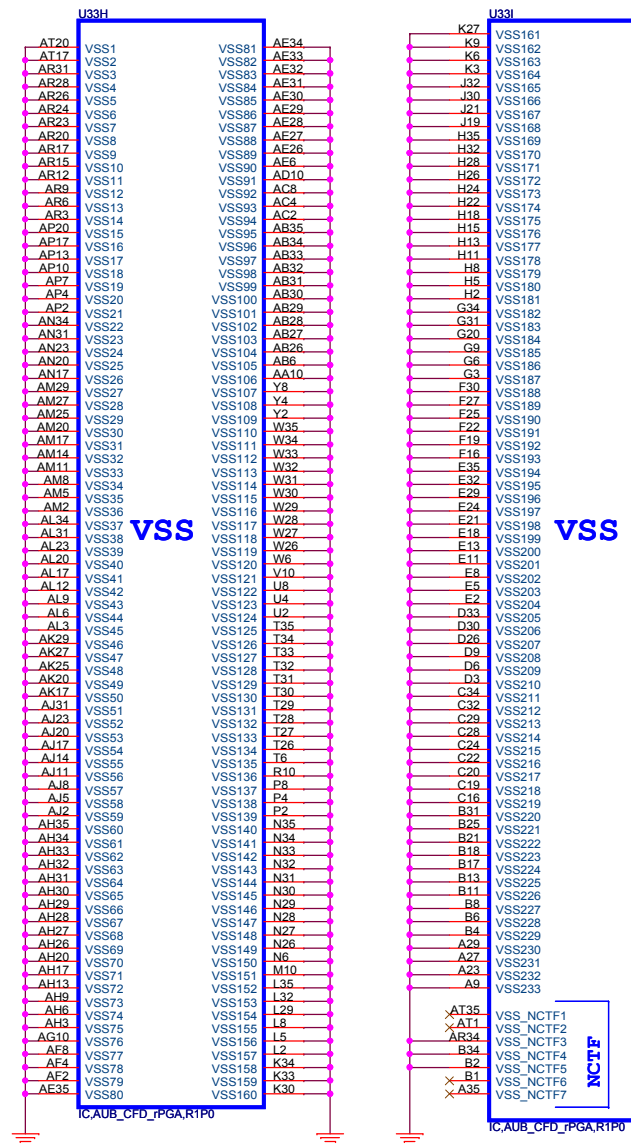
Size Custom Document Number **PROCESSOR 3/4(POWER)** Rev 1A

Date: Monday, October 26, 2009 | Sheet 5 of 45



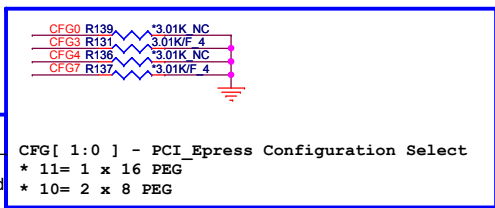
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



CFG[ 1:0 ] - PCI\_Epress Configuration Select  
\* 11= 1 x 16 PEG  
\* 10= 2 x 8 PEG

**PROJECT : UP67**  
**Quanta Computer Inc.**

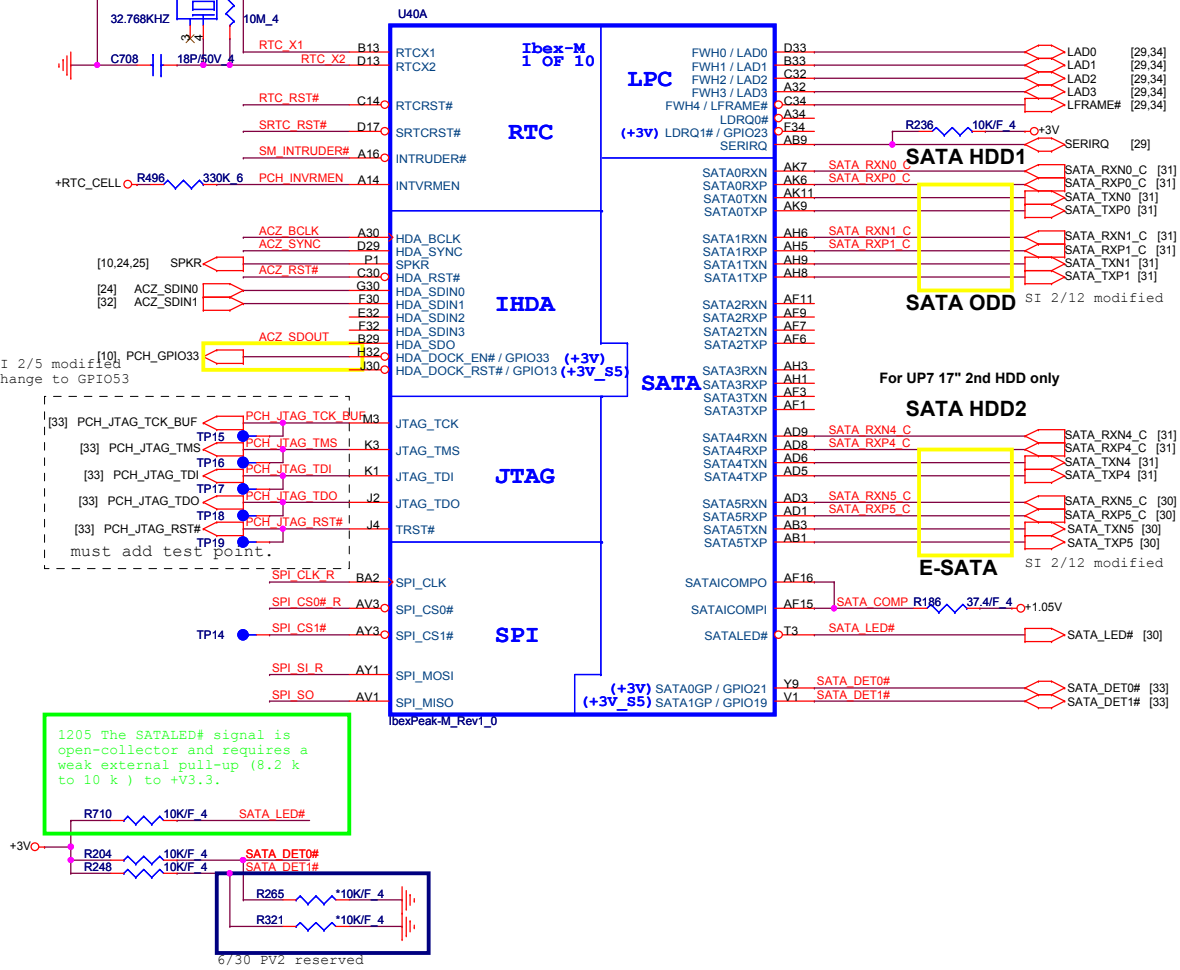
NB5

Size Custom Document Number  
**PROCESSOR 4/4(GND)**

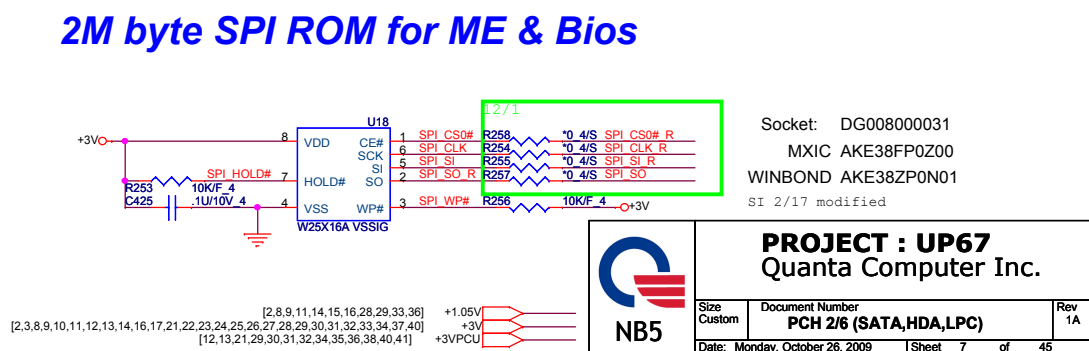
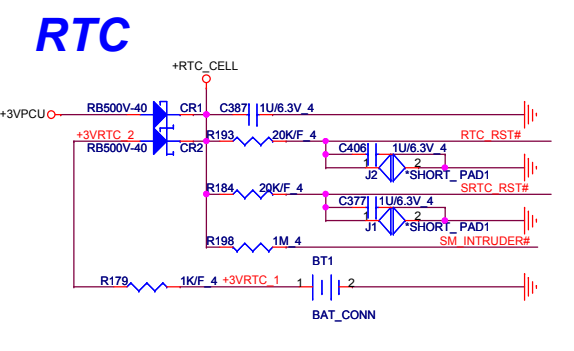
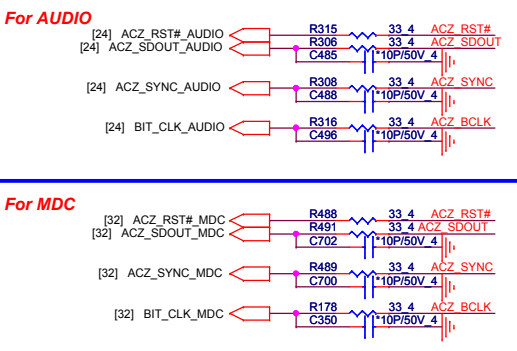
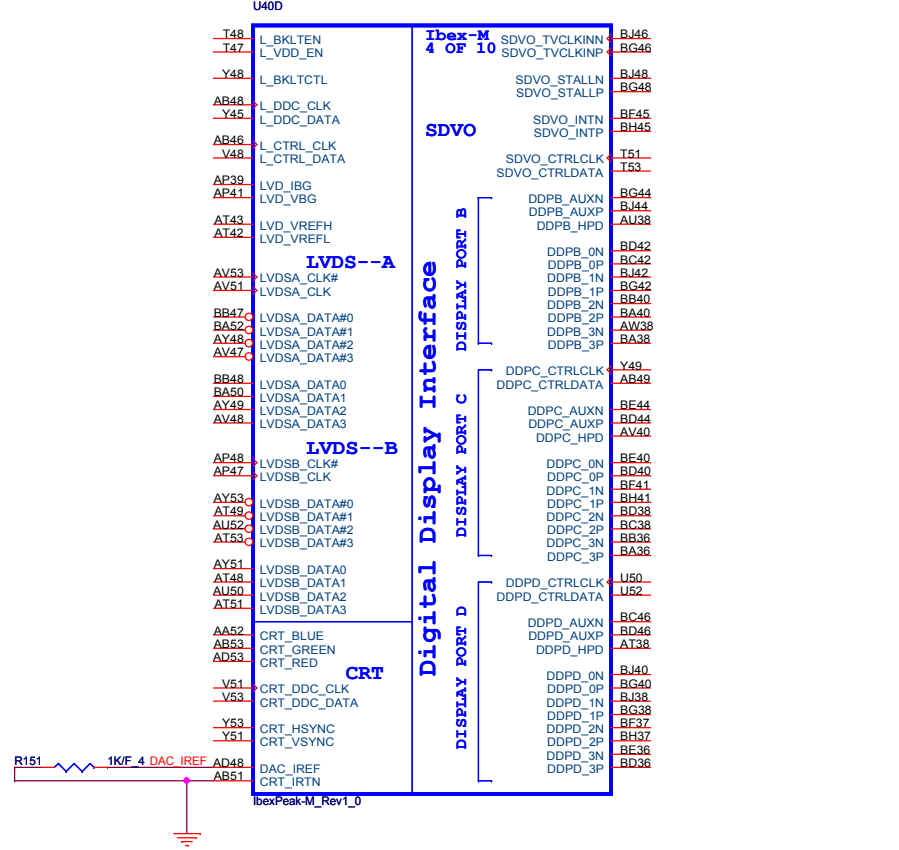
Date: Monday, October 26, 2009 | Sheet 6 of 45

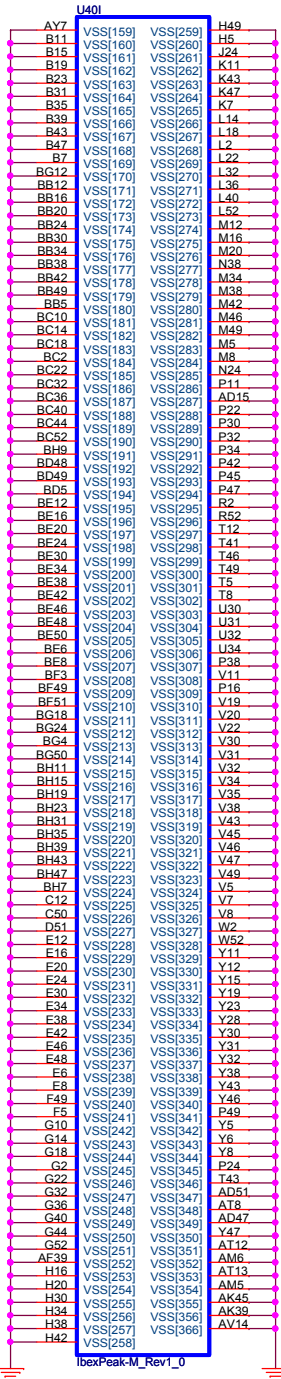
INTVRMEN - Integrated SUS 1.1V VRM Enable High - Enable Internal VRs

### IBEX PEAK-M (HDA,JTAG,SATA)

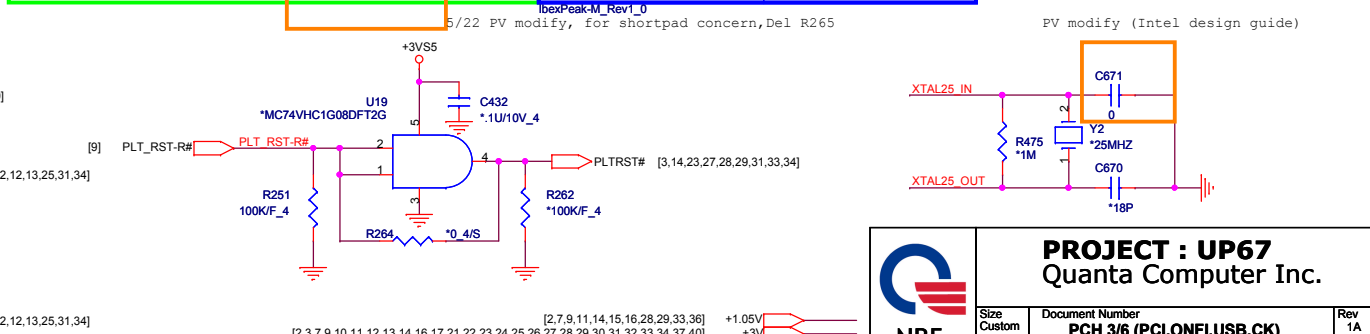
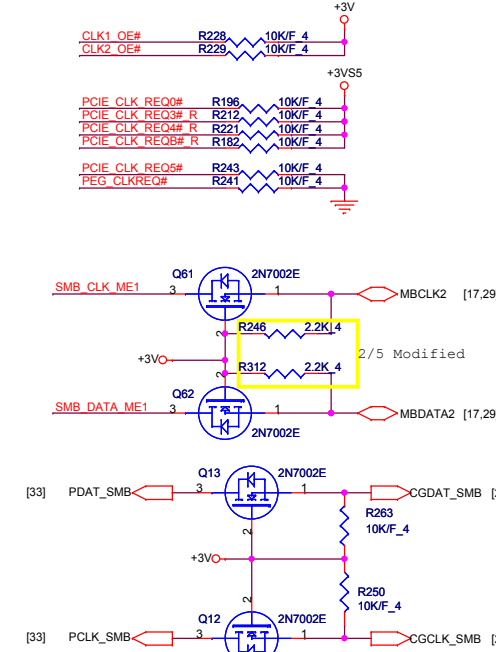
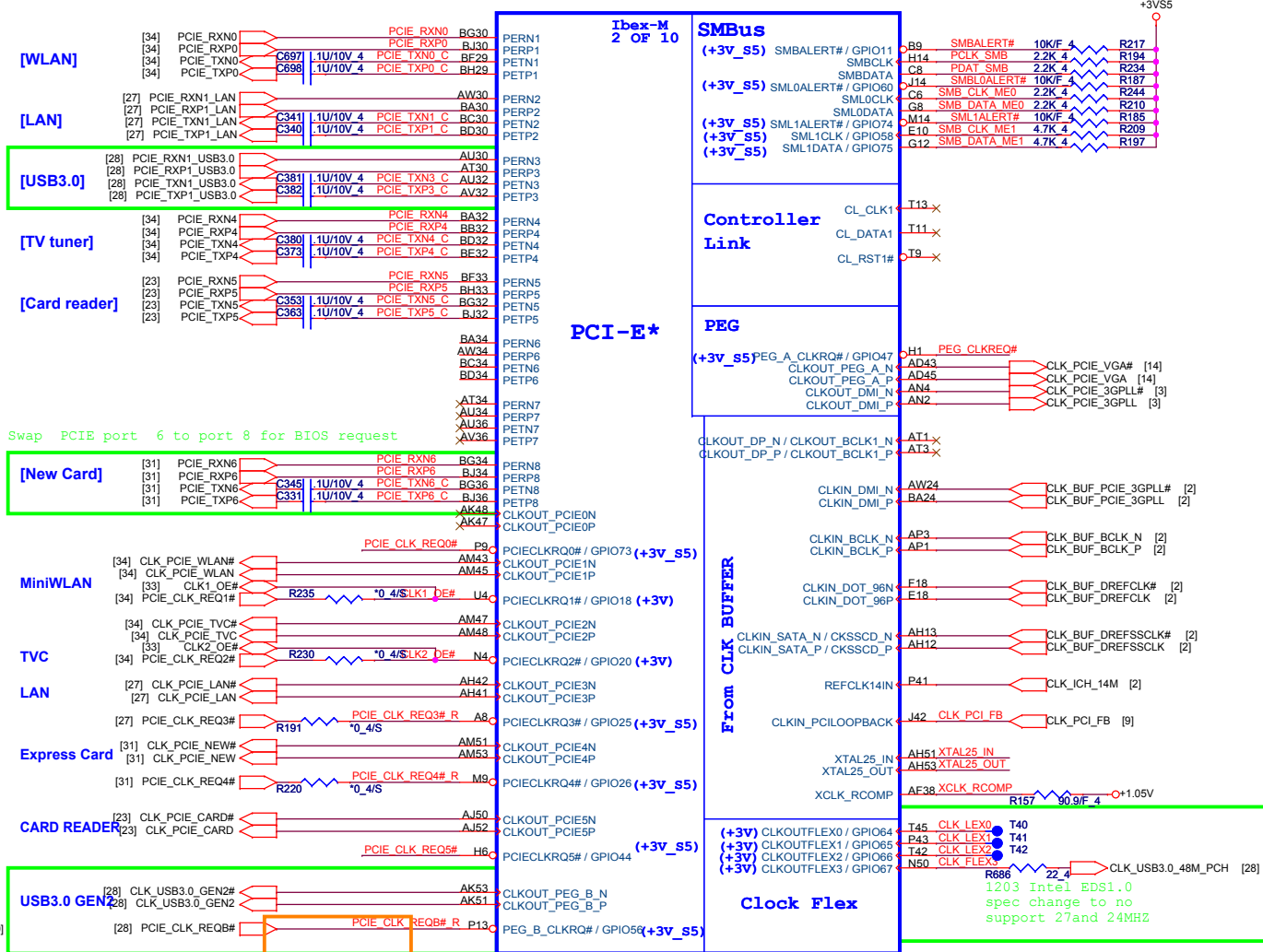


### IBEX PEAK-M (LVDS,DDI)





IBEX PEAK-M (PCI-E, SMBUS, CLK)



**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number **PCH 3/6 (PCI,ONFI,USB,CK)** Rev 1A

Date: Monday, October 26, 2009 | Sheet 8 of 45

[2,3,7,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]  
[7,9,11,14,15,16,28,29,33,36]  
[7,12,13,21,29,30,31,32,34,35,36,38,40,41]

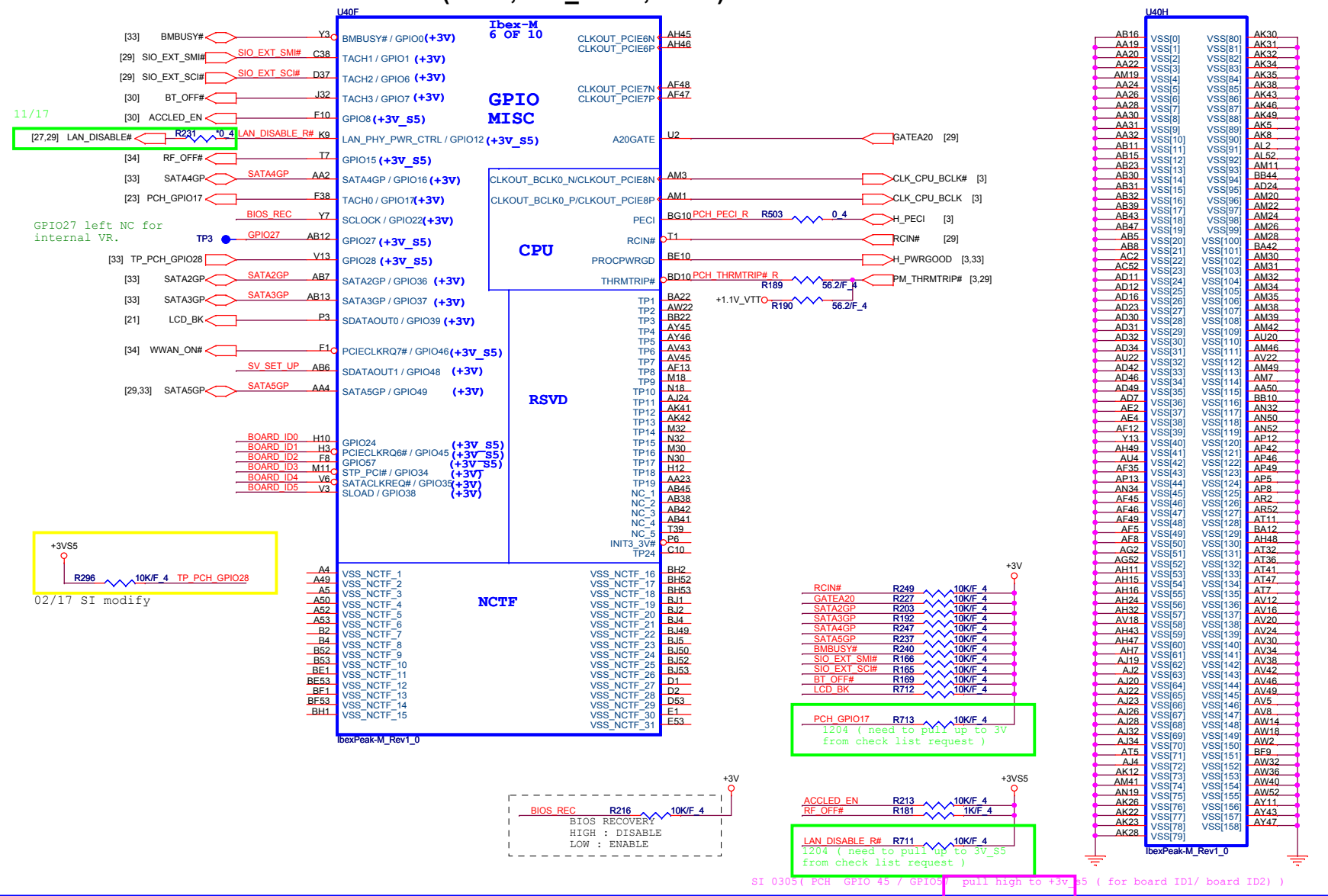
+1.05V  
+3V  
+3VPCU





# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

# IBEX PEAK-M (GND)



## BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RDO (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			0=Jones/Cujo 2.0 (Clarkfield) 10=Jones/Cujo 2.1 (Auburndate UMA)			
ROM Size				0= 2M 1= 4M		

**A16 swap override Strap/Top-Block Swap Override jumper**

GNT3#

Low = A16 swap override/Top-Block Swap Override enabled  
High = Default

**SV SET UP R223**

1-X High = Strong (Default)

**GNT0# GNT1#**

BIOS boot from SPI S1 2/5 modified

**Boot BIOS Strap**

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

**NV\_ALE NV\_CLE**

11/17

**Danbury Technology Enabled**

NV\_ALE High = Enable  
Low = Disable

**DMI Termination Voltage**

NV\_CLE Set to Vcc when LOW  
Set to Vcc/2 when HIGH

**No Reboot Strap**

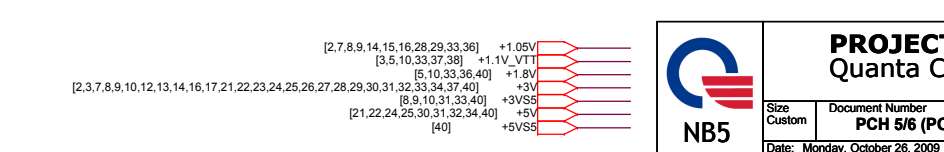
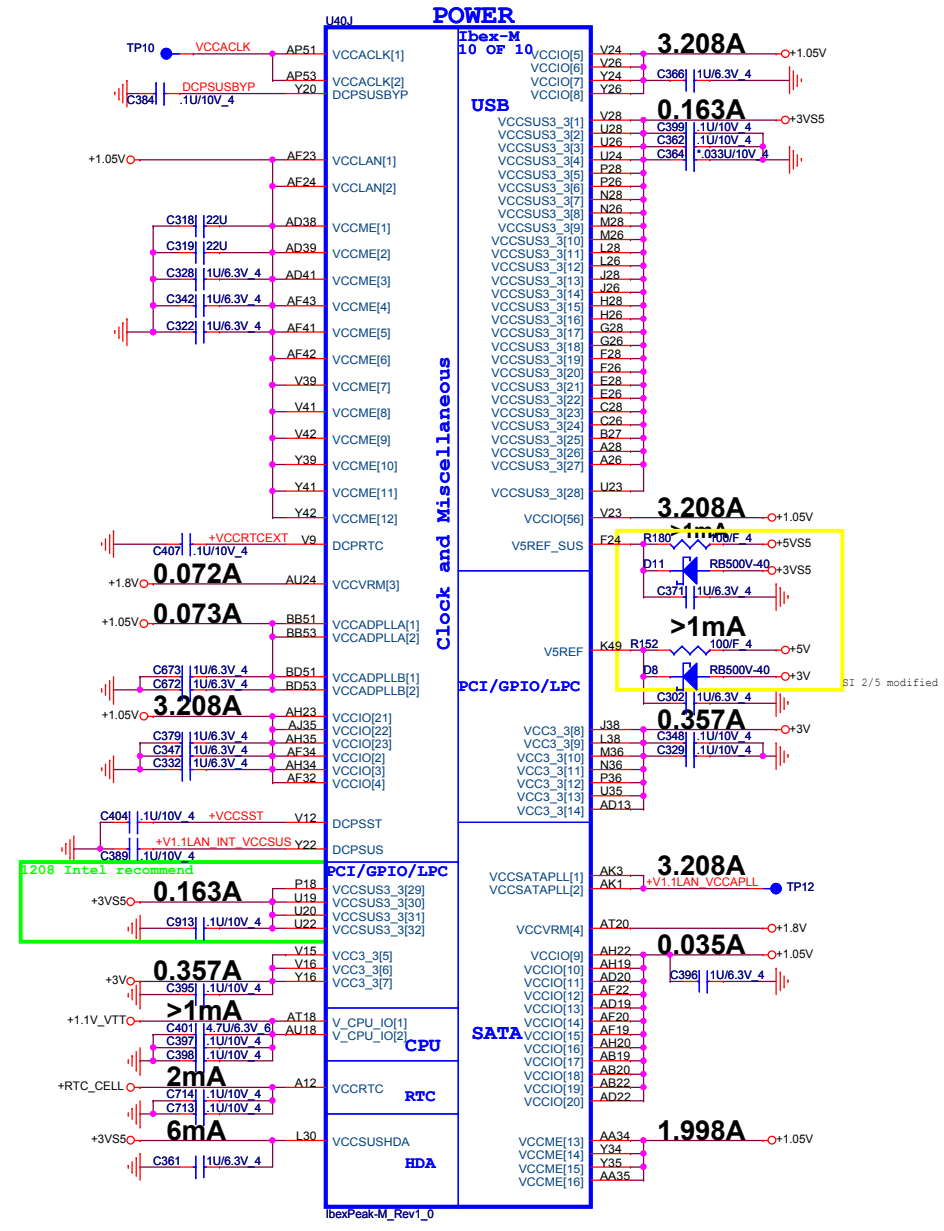
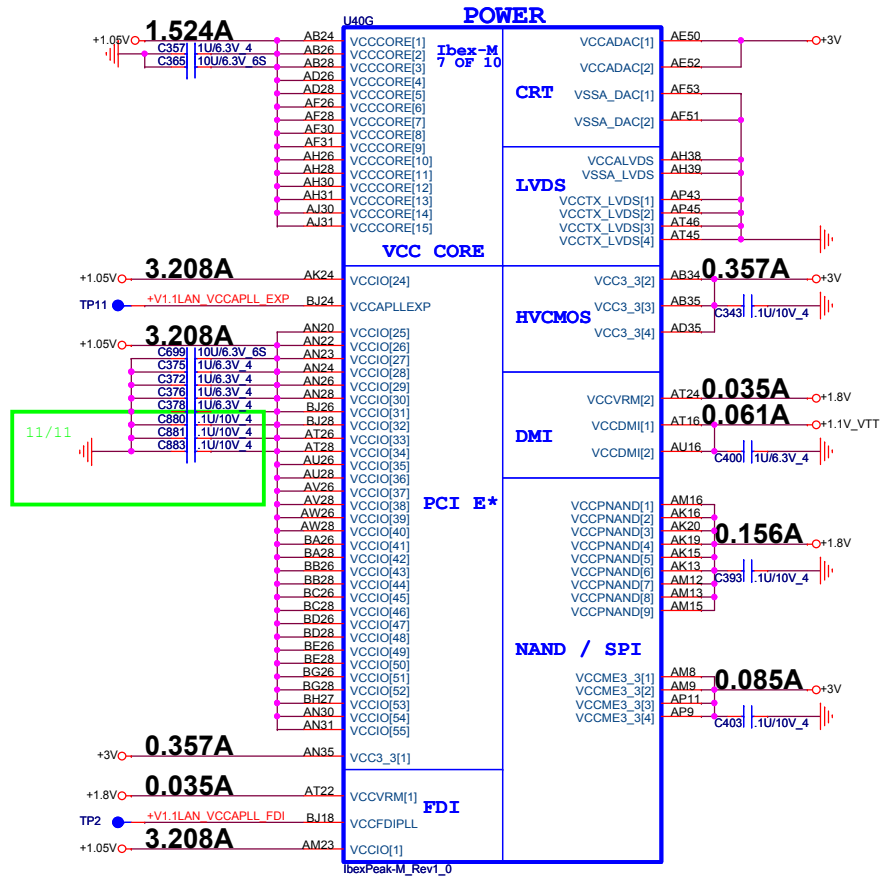
PCH\_GPIO33

**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number **PCH 4/6 (GPIO & Strap)** Rev 1A

Date: Monday, October 26, 2009 | Sheet 10 of 45

[3,5,11,33,37,38] +1.1V\_VTTT  
[5,11,33,36,40] +1.8V  
[2,3,7,8,9,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +1.9V  
[8,9,11,31,33,40] +3VSS

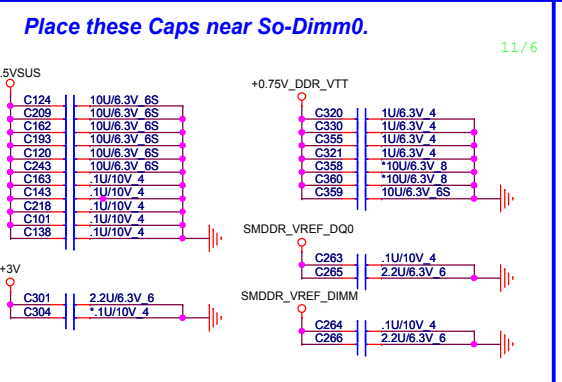
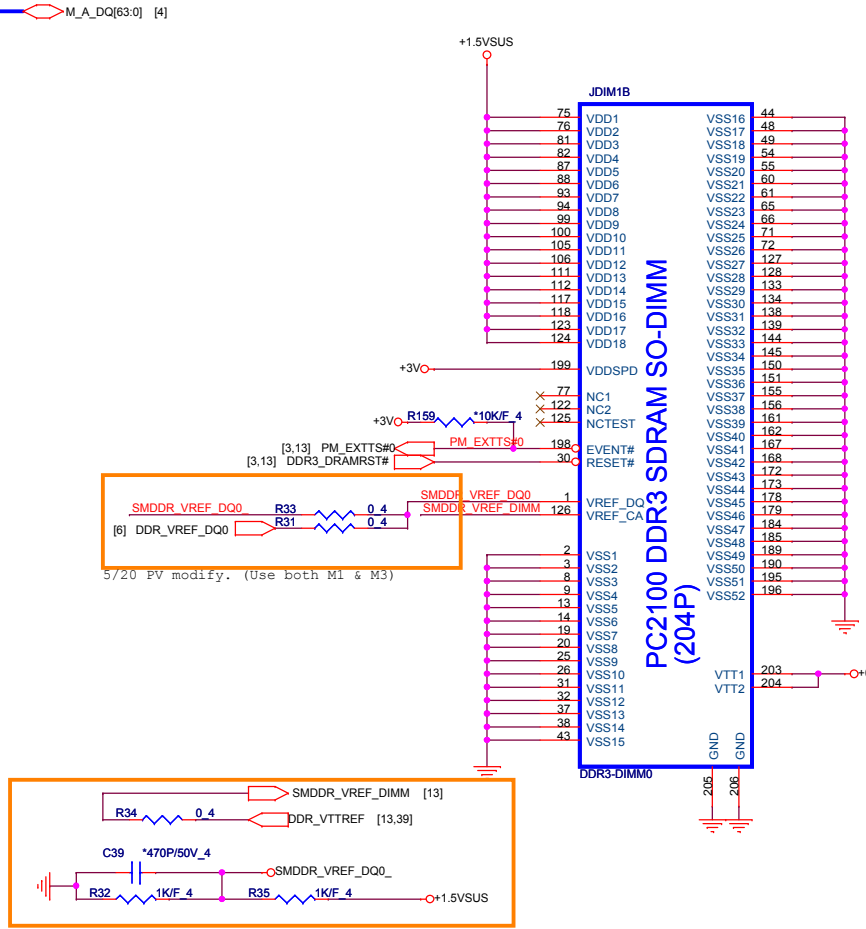
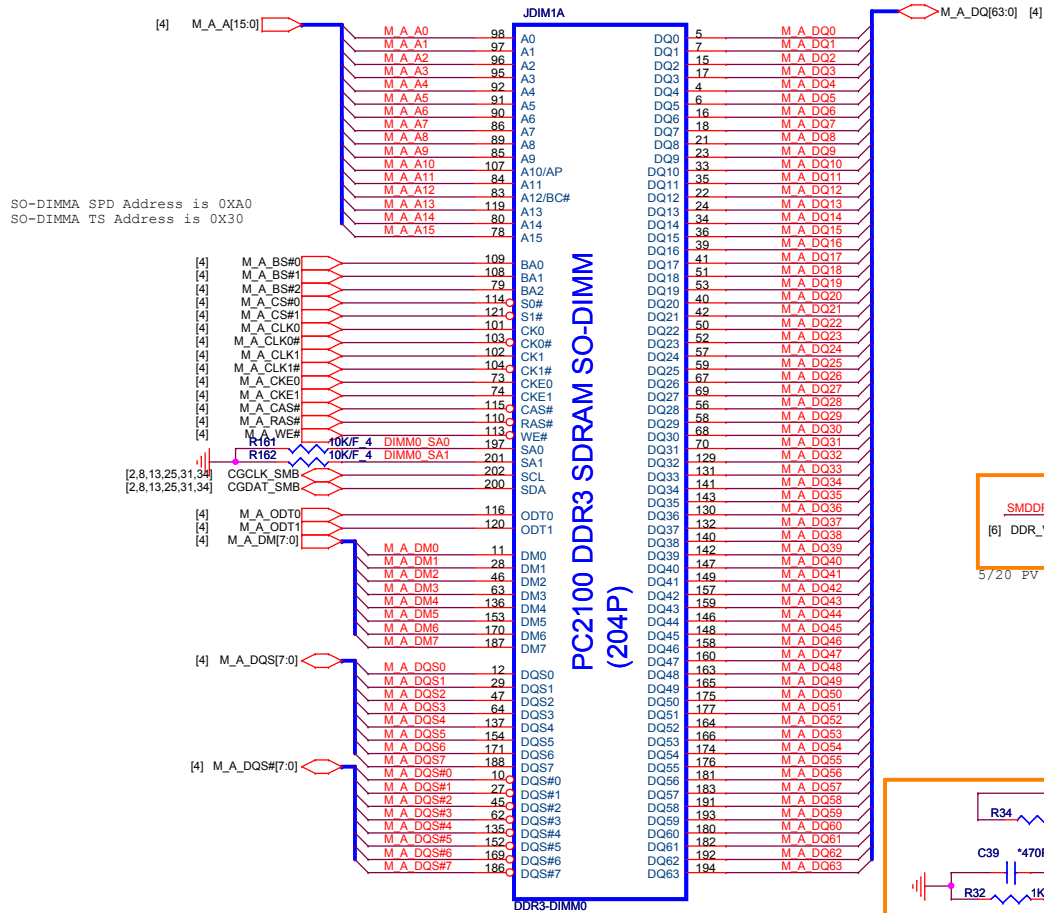


[2,7,8,9,14,15,16,28,29,33,36]	+1.05V
[3,5,10,33,37,38]	+1.1V_VTT
[5,10,33,36,40]	+1.8V
[2,3,7,8,9,10,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]	+3V
[8,9,10,31,33,40]	+3VS5
[21,22,24,25,30,31,32,34,40]	+5V
[40]	+5VS5

**PROJECT : UP67**

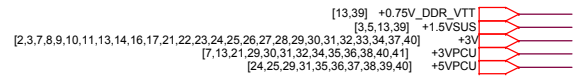
**Quanta Computer Inc.**

Size Custom	Document Number <b>PCH 5/6 (POWER)</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 11 of 45		



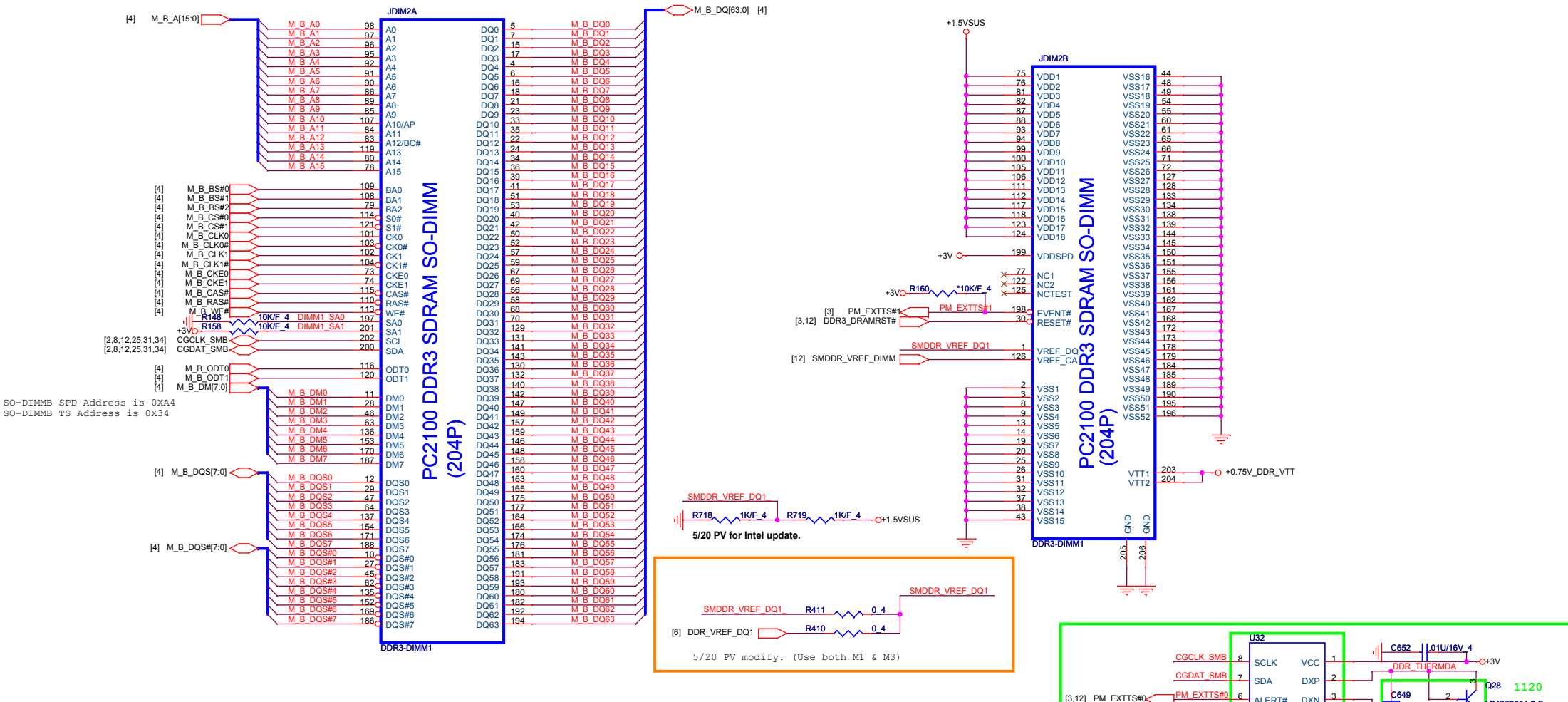
5/20: NA for INT recommend

reserve only...  
can let it NC at this block components if DB stage not trouble found



**PROJECT : UP67**  
**Quanta Computer Inc.**

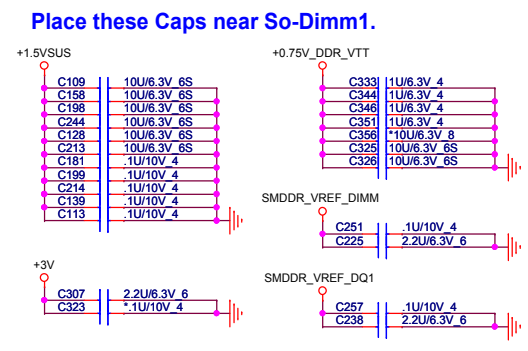
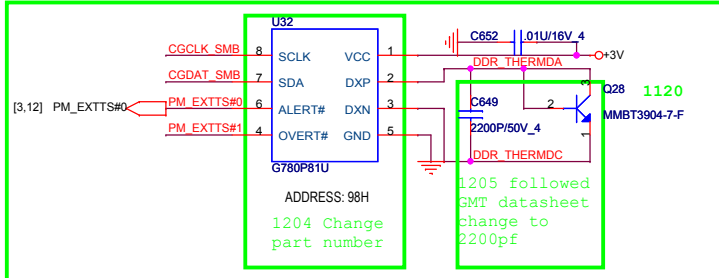
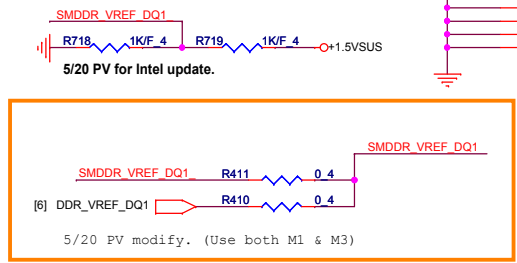
Size Custom	Document Number <b>DDR3 DIMM-0</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 12 of 45		



SO-DIMM SPD Address is 0XA4  
SO-DIMM TS Address is 0X34

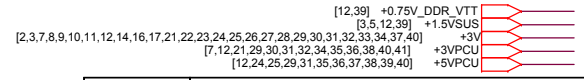
**PC2100 DDR3 SDRAM SO-DIMM (204P)**

**PC2100 DDR3 SDRAM SO-DIMM (204P)**



5/20: NA for for INT recommend

reserve only..  
can let it NC at this block components if DB stage not trouble found



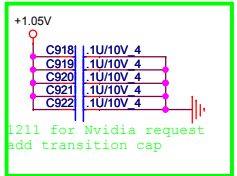
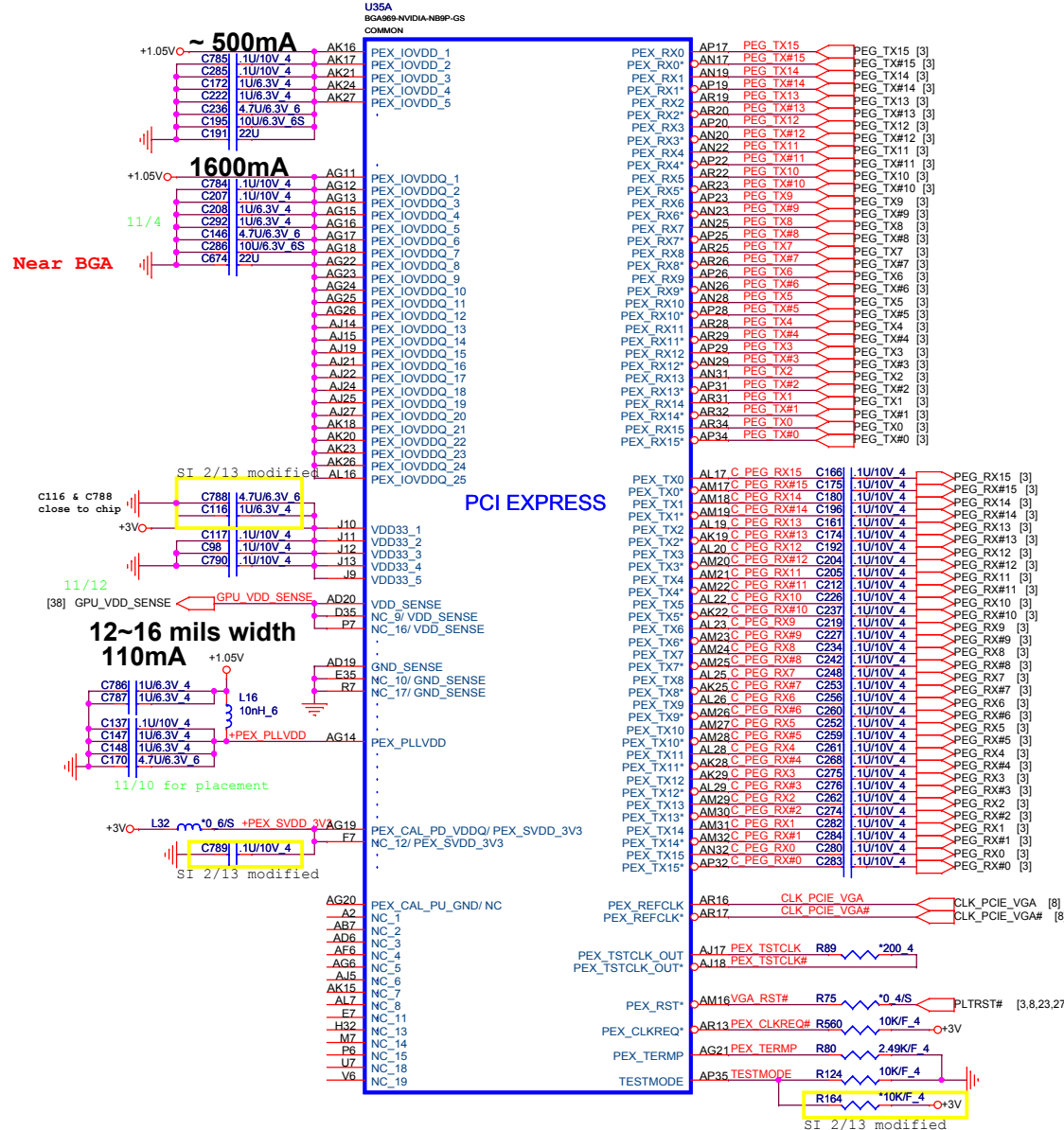
**PROJECT : UP67**  
**Quanta Computer Inc.**

**NB5**

Size Custom Document Number **DDR3 DIMM-1** Rev 1A

Date: Monday, October 26, 2009 Sheet 13 of 45

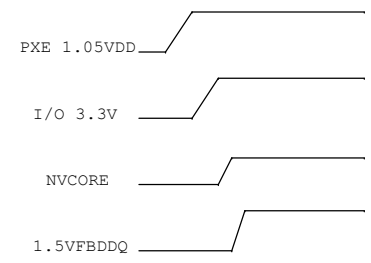
PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD > 2.2A



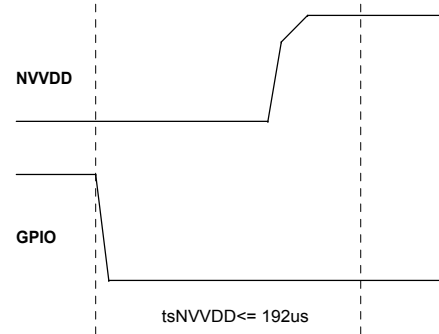
VGA Thermal Circuit

0514: PV modify  
Delete Reserved thermal circuit

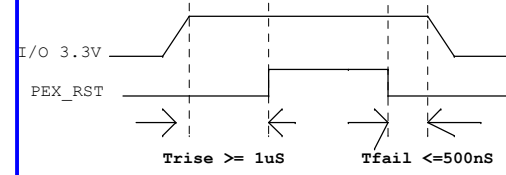
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V  
NVVDD Maximum Settling Time



PEX\_RST timing



[2,3,7,8,9,10,11,12,13,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] [2,7,8,9,11,15,16,28,29,33,36] +1.05V  
+3V

**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number N10X (PCIE I/F) 1/5 Rev 1A

Date: Monday, October 26, 2009 Sheet 14 of 45

U35B  
BG969-NVIDIA-NBSP-GS  
COMMON

12/02 modify  
package for N10

[19] FBA_CMD0	V32	FBA_CMD0
[19] FBA_CMD1	U31	FBA_CMD1
[19] FBA_CMD2	Y32	FBA_CMD2
[19] FBA_CMD3	AB35	FBA_CMD3
[19] FBA_CMD4	AB34	FBA_CMD4
[19] FBA_CMD5	W35	FBA_CMD5
[19] FBA_CMD6	W33	FBA_CMD6
[19] FBA_CMD7	W34	FBA_CMD7
[19] FBA_CMD8	T34	FBA_CMD8
[19] FBA_CMD9	T35	FBA_CMD9
[19] FBA_CMD10	AB31	FBA_CMD10
[19] FBA_CMD11	Y30	FBA_CMD11
[19] FBA_CMD12	Y34	FBA_CMD12
[19] FBA_CMD13	W32	FBA_CMD13
[19] FBA_CMD14	AA30	FBA_CMD14
[19] FBA_CMD15	AA32	FBA_CMD15
[19] FBA_CMD16	Y33	FBA_CMD16
[19] FBA_CMD17	U32	FBA_CMD17
[19] FBA_CMD18	U31	FBA_CMD18
[19] FBA_CMD19	U34	FBA_CMD19
[19] FBA_CMD20	Y35	FBA_CMD20
[19] FBA_CMD21	W34	FBA_CMD21
[19] FBA_CMD22	W30	FBA_CMD22
[19] FBA_CMD23	U35	FBA_CMD23
[19] FBA_CMD24	U30	FBA_CMD24
[19] FBA_CMD25	U33	FBA_CMD25
[19] FBA_CMD26	AB30	FBA_CMD26
[19] FBA_CMD27	AB33	FBA_CMD27
[19] FBA_CMD28	T33	FBA_CMD28
[19] FBA_CMD29	W29	FBA_CMD29
[19] FBA_CMD30	W29	FBA_CMD30

12/02 modify package for N10

VMA_DM0	P32	FBA_DQM0
VMA_DM1	H34	FBA_DQM1
VMA_DM2	J30	FBA_DQM2
VMA_DM3	P30	FBA_DQM3
VMA_DM4	AF32	FBA_DQM4
VMA_DM5	AL32	FBA_DQM5
VMA_DM6	AE34	FBA_DQM6
VMA_DM7	AF35	FBA_DQM7

VMA_WDQS0	L34	FBA_DQS_WP0
VMA_WDQS1	H35	FBA_DQS_WP1
VMA_WDQS2	J32	FBA_DQS_WP2
VMA_WDQS3	N31	FBA_DQS_WP3
VMA_WDQS4	AE31	FBA_DQS_WP4
VMA_WDQS5	AJ32	FBA_DQS_WP5
VMA_WDQS6	AJ34	FBA_DQS_WP6
VMA_WDQS7	AC33	FBA_DQS_WP7

VMA_RDQS0	L35	FBA_DQS_RN0
VMA_RDQS1	G35	FBA_DQS_RN1
VMA_RDQS2	H31	FBA_DQS_RN2
VMA_RDQS3	N32	FBA_DQS_RN3
VMA_RDQS4	AD32	FBA_DQS_RN4
VMA_RDQS5	AJ31	FBA_DQS_RN5
VMA_RDQS6	AJ35	FBA_DQS_RN6
VMA_RDQS7	AC34	FBA_DQS_RN7

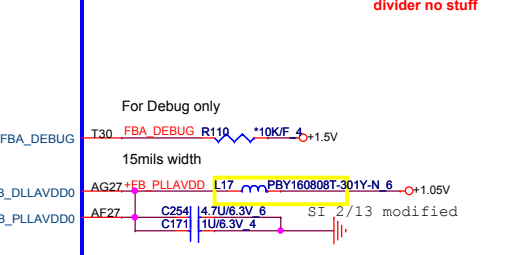
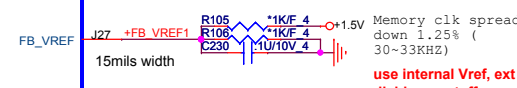
P29	FBA_WCK0
R29C	FBA_WCK0_N
L28	FBA_WCK1
M29	FBA_WCK1_N
AG29	FBA_WCK2
AH29	FBA_WCK2_N
AD29	FBA_WCK3
AE29C	FBA_WCK3_N

AA27	FBVDDQ_1
AA29	FBVDDQ_2
AA31	FBVDDQ_3
AB27	FBVDDQ_4
AB29	FBVDDQ_5
AC27	FBVDDQ_6
AD27	FBVDDQ_7
AE27	FBVDDQ_8
AJ28	FBVDDQ_9
B18	FBVDDQ_10
E21	FBVDDQ_11
G12	FBVDDQ_12
G15	FBVDDQ_13
G22	FBVDDQ_14
G8	FBVDDQ_15
G9	FBVDDQ_16
H29	FBVDDQ_17
J14	FBVDDQ_18
J15	FBVDDQ_19
J16	FBVDDQ_20
J17	FBVDDQ_21
J20	FBVDDQ_22
J21	FBVDDQ_23
J22	FBVDDQ_24
J23	FBVDDQ_25
J24	FBVDDQ_26
J29	FBVDDQ_27

MEMORY I/F A

FBA_D00	L32	VMA_D00
FBA_D01	N33	VMA_D01
FBA_D02	L33	VMA_D02
FBA_D03	N34	VMA_D03
FBA_D04	N35	VMA_D04
FBA_D05	P35	VMA_D05
FBA_D06	E33	VMA_D06
FBA_D07	K35	VMA_D07
FBA_D08	K33	VMA_D08
FBA_D09	K34	VMA_D09
FBA_D10	K34	VMA_D010
FBA_D11	H33	VMA_D011
FBA_D12	G34	VMA_D012
FBA_D13	G33	VMA_D013
FBA_D14	E34	VMA_D014
FBA_D15	E33	VMA_D015
FBA_D16	G31	VMA_D016
FBA_D17	F30	VMA_D017
FBA_D18	G32	VMA_D018
FBA_D19	K30	VMA_D019
FBA_D20	K32	VMA_D020
FBA_D21	H30	VMA_D021
FBA_D22	K31	VMA_D022
FBA_D23	L31	VMA_D023
FBA_D24	L31	VMA_D024
FBA_D25	M32	VMA_D025
FBA_D26	N30	VMA_D026
FBA_D27	N30	VMA_D027
FBA_D28	M30	VMA_D028
FBA_D29	P31	VMA_D029
FBA_D30	R32	VMA_D030
FBA_D31	R32	VMA_D031
FBA_D32	AG30	VMA_D032
FBA_D33	AG32	VMA_D033
FBA_D34	AH31	VMA_D034
FBA_D35	AE31	VMA_D035
FBA_D36	AE30	VMA_D036
FBA_D37	AC32	VMA_D037
FBA_D38	AD30	VMA_D038
FBA_D39	AN33	VMA_D039
FBA_D40	AL31	VMA_D040
FBA_D41	AM33	VMA_D041
FBA_D42	AL33	VMA_D042
FBA_D43	AK30	VMA_D043
FBA_D44	AK32	VMA_D044
FBA_D45	AJ30	VMA_D045
FBA_D46	AH30	VMA_D046
FBA_D47	AH33	VMA_D047
FBA_D48	AH35	VMA_D048
FBA_D49	AH34	VMA_D049
FBA_D50	AH32	VMA_D050
FBA_D51	AJ33	VMA_D051
FBA_D52	AL35	VMA_D052
FBA_D53	AM34	VMA_D053
FBA_D54	AM35	VMA_D054
FBA_D55	AE33	VMA_D055
FBA_D56	AE32	VMA_D056
FBA_D57	AE34	VMA_D057
FBA_D58	AE35	VMA_D058
FBA_D59	AE34	VMA_D059
FBA_D60	AE33	VMA_D060
FBA_D61	AB32	VMA_D061
FBA_D62	AC35	VMA_D062
FBA_D63	AC35	VMA_D063

FBA_CLK0	T32	VMA_CLK0
FBA_CLK0*	T31	VMA_CLK0#
FBA_CLK1	AC31	VMA_CLK1
FBA_CLK1*	AC30	VMA_CLK1#



U35C  
BG969-NVIDIA-NBSP-GS  
COMMON

12/02 modify  
package for N10

[20] FBC_CMD0	C17	FBC_CMD0
[20] FBC_CMD1	D18	FBC_CMD1
[20] FBC_CMD2	F21	FBC_CMD2
[20] FBC_CMD3	A23	FBC_CMD3
[20] FBC_CMD4	D21	FBC_CMD4
[20] FBC_CMD5	B23	FBC_CMD5
[20] FBC_CMD6	E20	FBC_CMD6
[20] FBC_CMD7	G21	FBC_CMD7
[20] FBC_CMD8	F20	FBC_CMD8
[20] FBC_CMD9	F19	FBC_CMD9
[20] FBC_CMD10	F23	FBC_CMD10
[20] FBC_CMD11	A22	FBC_CMD11
[20] FBC_CMD12	G22	FBC_CMD12
[20] FBC_CMD13	B17	FBC_CMD13
[20] FBC_CMD14	F24	FBC_CMD14
[20] FBC_CMD15	C25	FBC_CMD15
[20] FBC_CMD16	E22	FBC_CMD16
[20] FBC_CMD17	C20	FBC_CMD17
[20] FBC_CMD18	A19	FBC_CMD18
[20] FBC_CMD19	D22	FBC_CMD19
[20] FBC_CMD20	D20	FBC_CMD20
[20] FBC_CMD21	D22	FBC_CMD21
[20] FBC_CMD22	E19	FBC_CMD22
[20] FBC_CMD23	D19	FBC_CMD23
[20] FBC_CMD24	F18	FBC_CMD24
[20] FBC_CMD25	C19	FBC_CMD25
[20] FBC_CMD26	F22	FBC_CMD26
[20] FBC_CMD27	C23	FBC_CMD27
[20] FBC_CMD28	B20	FBC_CMD28
[20] FBC_CMD29	A20	FBC_CMD29
[20] FBC_CMD30	A20	FBC_CMD30

12/02 modify package for N10

VMC_DM0	A16	FBC_DQM0
VMC_DM1	D10	FBC_DQM1
VMC_DM2	F11	FBC_DQM2
VMC_DM3	D15	FBC_DQM3
VMC_DM4	D27	FBC_DQM4
VMC_DM5	D34	FBC_DQM5
VMC_DM6	A34	FBC_DQM6
VMC_DM7	D28	FBC_DQM7

VMC_WDQS0	C14	FBC_DQS_WP0
VMC_WDQS1	A10	FBC_DQS_WP1
VMC_WDQS2	E10	FBC_DQS_WP2
VMC_WDQS3	D14	FBC_DQS_WP3
VMC_WDQS4	E26	FBC_DQS_WP4
VMC_WDQS5	D32	FBC_DQS_WP5
VMC_WDQS6	A32	FBC_DQS_WP6
VMC_WDQS7	B26	FBC_DQS_WP7

VMC_RDQS0	B14	FBC_DQS_RN0
VMC_RDQS1	B10	FBC_DQS_RN1
VMC_RDQS2	D9	FBC_DQS_RN2
VMC_RDQS3	E14	FBC_DQS_RN3
VMC_RDQS4	F26	FBC_DQS_RN4
VMC_RDQS5	A31	FBC_DQS_RN5
VMC_RDQS6	A31	FBC_DQS_RN6
VMC_RDQS7	A26	FBC_DQS_RN7

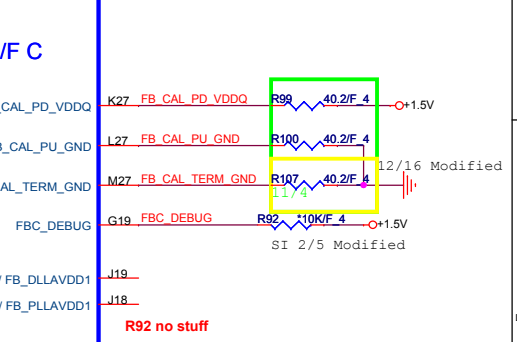
G14	FBC_WCK0
G15C	FBC_WCK0_N
G11	FBC_WCK1
G12C	FBC_WCK1_N
G27	FBC_WCK2
G28	FBC_WCK2_N
G24	FBC_WCK3
G25C	FBC_WCK3_N

N27	FBVDDQ_28
P27	FBVDDQ_29
R27	FBVDDQ_30
T27	FBVDDQ_31
U27	FBVDDQ_32
U29	FBVDDQ_33
V27	FBVDDQ_34
V29	FBVDDQ_35
V34	FBVDDQ_36
W27	FBVDDQ_37
Y27	FBVDDQ_38

MEMORY I/F C

FBC_D00	B13	VMC_D00
FBC_D01	D13	VMC_D01
FBC_D02	A14	VMC_D02
FBC_D03	A14	VMC_D03
FBC_D04	C16	VMC_D04
FBC_D05	B16	VMC_D05
FBC_D06	A17	VMC_D06
FBC_D07	D16	VMC_D07
FBC_D08	C14	VMC_D08
FBC_D09	B11	VMC_D09
FBC_D10	A11	VMC_D010
FBC_D11	A11	VMC_D011
FBC_D12	C10	VMC_D012
FBC_D13	C8	VMC_D013
FBC_D14	A8	VMC_D014
FBC_D15	A8	VMC_D015
FBC_D16	E8	VMC_D016
FBC_D17	F8	VMC_D017
FBC_D18	F10	VMC_D018
FBC_D19	F9	VMC_D019
FBC_D20	E12	VMC_D020
FBC_D21	D8	VMC_D021
FBC_D22	D11	VMC_D022
FBC_D23	E11	VMC_D023
FBC_D24	D12	VMC_D024
FBC_D25	E13	VMC_D025
FBC_D26	F13	VMC_D026
FBC_D27	E14	VMC_D027
FBC_D28	F15	VMC_D028
FBC_D29	E16	VMC_D029
FBC_D30	F16	VMC_D030
FBC_D31	D20	VMC_D031
FBC_D32	E27	VMC_D032
FBC_D33	F28	VMC_D033
FBC_D34	E28	VMC_D034
FBC_D35	D26	VMC_D035
FBC_D36	D26	VMC_D036
FBC_D37	F25	VMC_D037
FBC_D38	D24	VMC_D038
FBC_D39	E25	VMC_D039
FBC_D40	E32	VMC_D040
FBC_D41	F32	VMC_D041
FBC_D42	E33	VMC_D042
FBC_D43	F31	VMC_D043
FBC_D44	F30	VMC_D044
FBC_D45	D30	VMC_D045
FBC_D46	F29	VMC_D046
FBC_D47	E29	VMC_D047
FBC_D48	B29	VMC_D048
FBC_D49	C33	VMC_D049
FBC_D50	B31	VMC_D050
FBC_D51	C32	VMC_D051
FBC_D52	C32	VMC_D052
FBC_D53	B32	VMC_D053
FBC_D54	B35	VMC_D054
FBC_D55	B34	VMC_D055
FBC_D56	A28	VMC_D056
FBC_D57	B28	VMC_D057
FBC_D58	A28	VMC_D058
FBC_D59	C28	VMC_D059
FBC_D60	C26	VMC_D060
FBC_D61	B25	VMC_D061
FBC_D62	A25	VMC_D062
FBC_D63	A25	VMC_D063

FBC_CLK0	E17	VMC_CLK0
FBC_CLK0*	D17	VMC_CLK0#
FBC_CLK1	D23	VMC_CLK1
FBC_CLK1*	E23	VMC_CLK1#

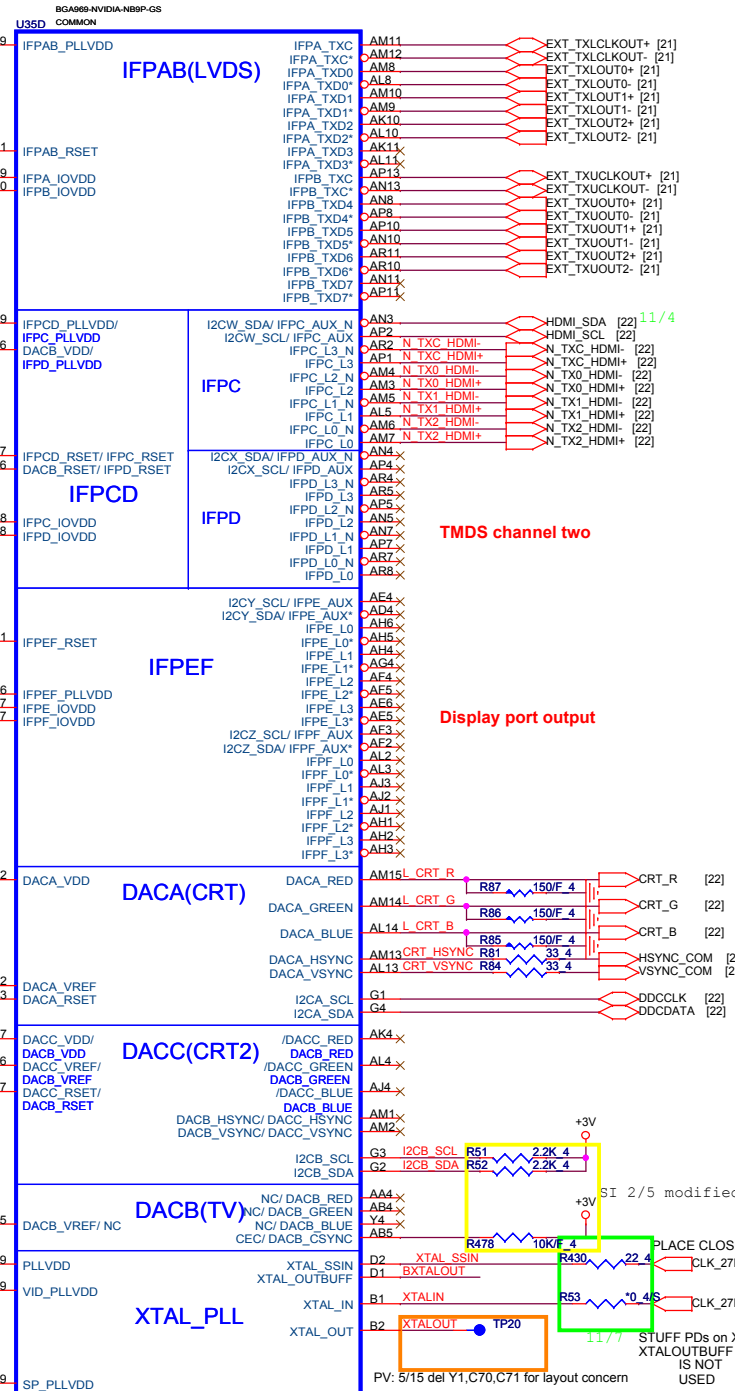
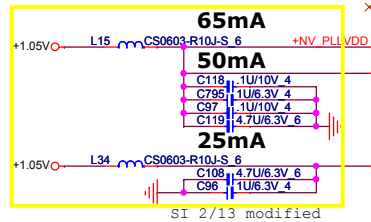
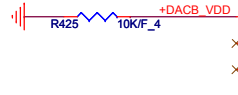
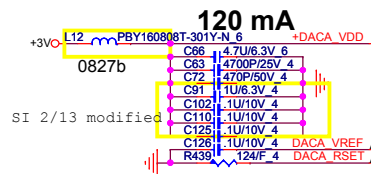
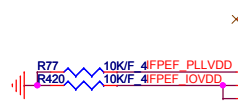
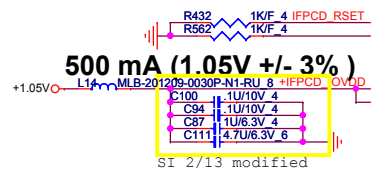
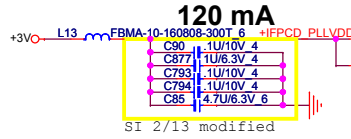
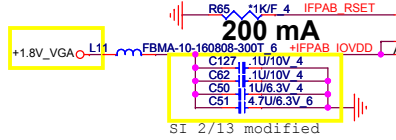
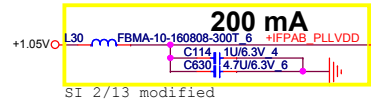


**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number **N10X (MEMORY I/F) 2/5** Rev 1A

Date: Monday, October 26, 2009 | Sheet 15 of 45

[2,7,8,9,11,14,16,28,29,33,36] +1.05V  
[19,20,31,34,36,39,40] +1.5V

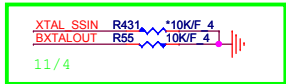


LVDS clk spread : Center  
+/-0.5% ( 30-33KHz)

TMD5 channel two

Display port output

SI 2/5 modified



11/4  
10 KΩ pull-down only if no spread chip used.

[2,7,8,9,11,14,15,28,29,33,36] [5,10,11,33,36,40]  
[3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]

**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom Document Number **N10X (DISPLAY) 3/5** Rev 2A

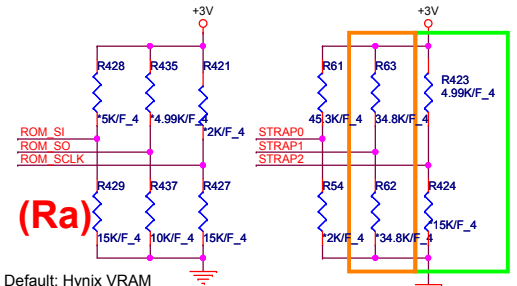
Date: Monday, October 26, 2009 Sheet 16 of 45



SEE Datasheet for details on N10P Straps!

CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

PCI\_DEVID[4]/SUBVENDOR 1211 DEVICE ID CHANGE



### Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

```
CS31002PB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502PB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002PB02 (RES CHIP 20K 1/16W +-1% (0402))
```

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

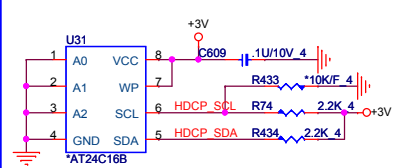
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

## GPIO ASSIGNMENTS

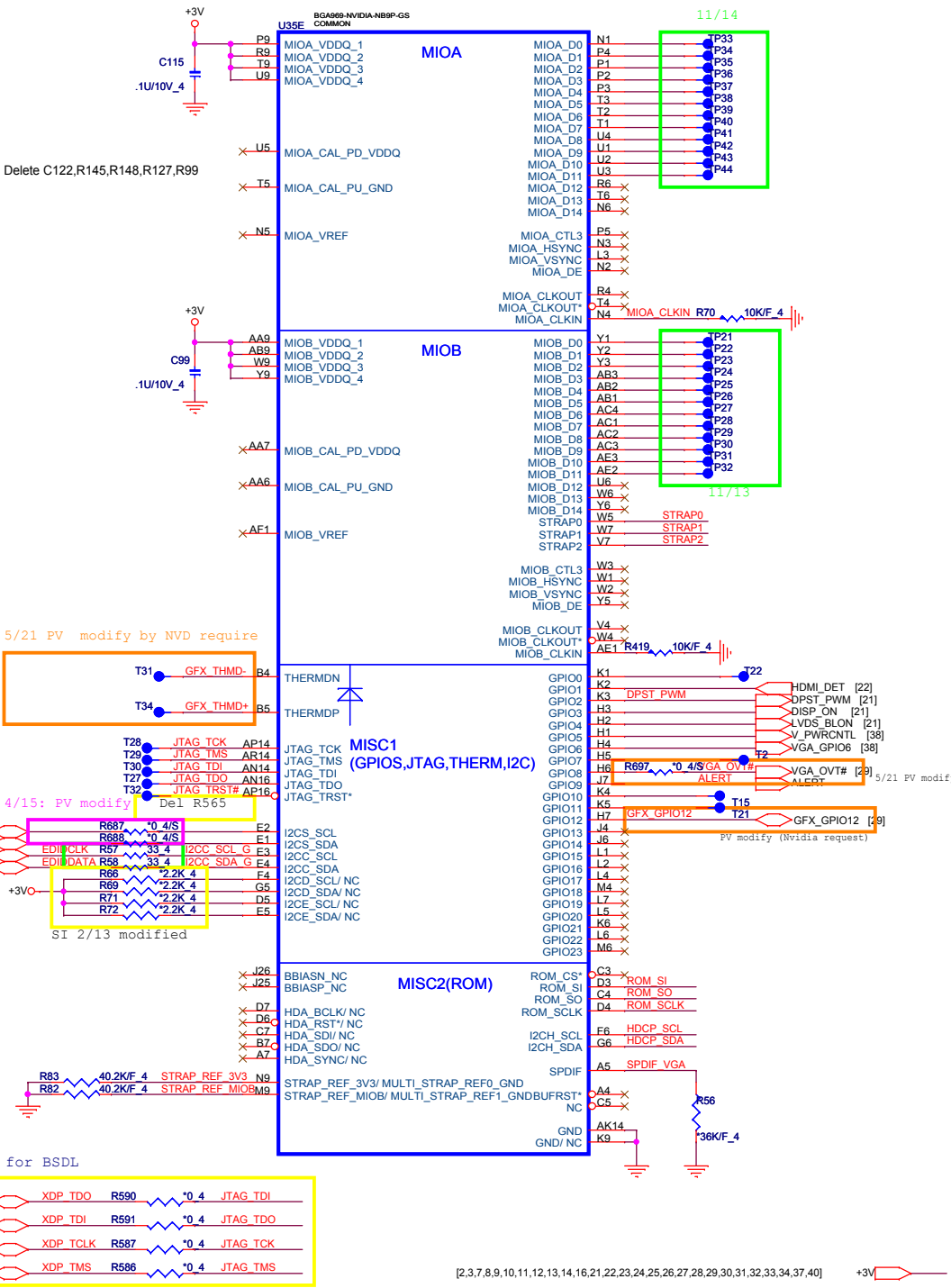
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

## HDCP ROM



Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM
	Hi: I2C ROM



Reserve for BSDL

XDP_TDO	XDP_TDO	R590	*0.4	JTAG TDI
XDP_TDI	XDP_TDI	R591	*0.4	JTAG TDO
XDP_TCLK	XDP_TCLK	R587	*0.4	JTAG TCK
XDP_TMS	XDP_TMS	R586	*0.4	JTAG TMS

[2,3,7,8,9,10,11,12,13,14,16,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]

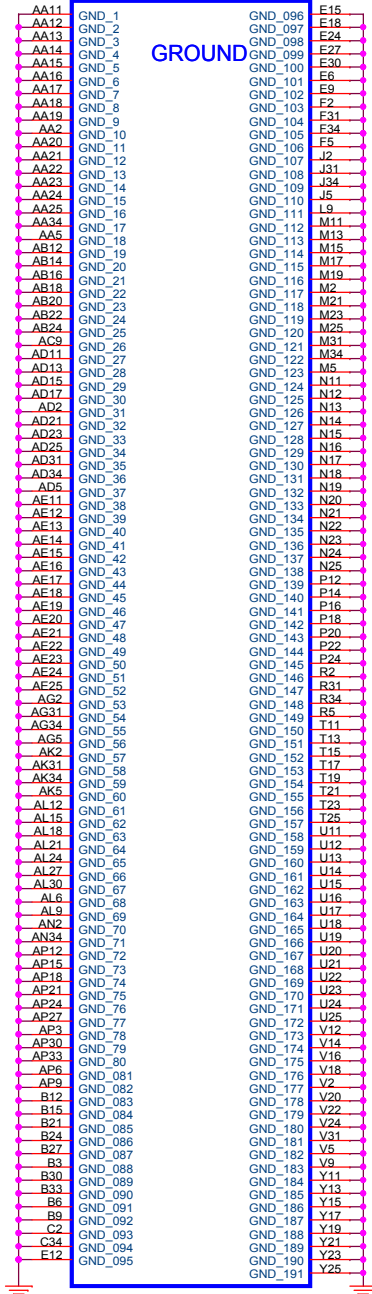
**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom Document Number  
**N10X (GPIO & STRAPS) 4/5**

Date: Monday, October 26, 2009 | Sheet 17 of 45

U35G

BGA969-NVIDIA-NB9P-GS  
COMMON



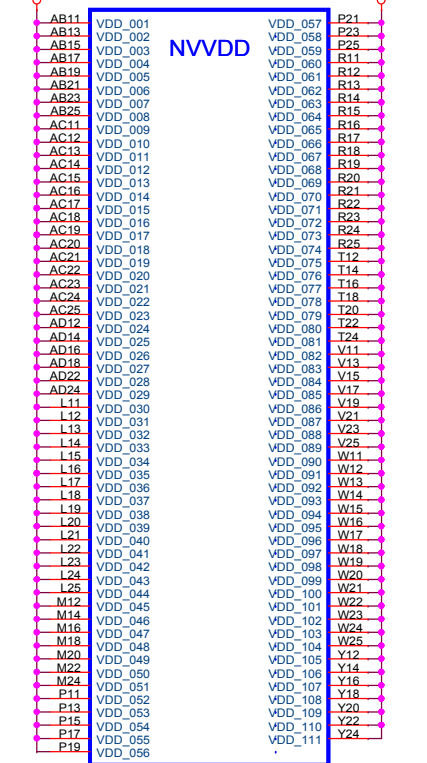
GROUND

Del all VRAM termination (RP16~RP75)

SI 2/5 modified

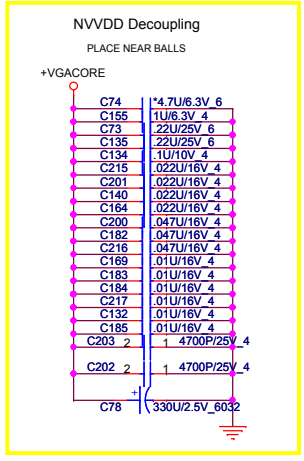
U35F

BGA969-NVIDIA-NB9P-GS  
COMMON



NVWDD

02/16 SI modify

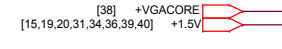


**PROJECT : UP67**  
Quanta Computer Inc.

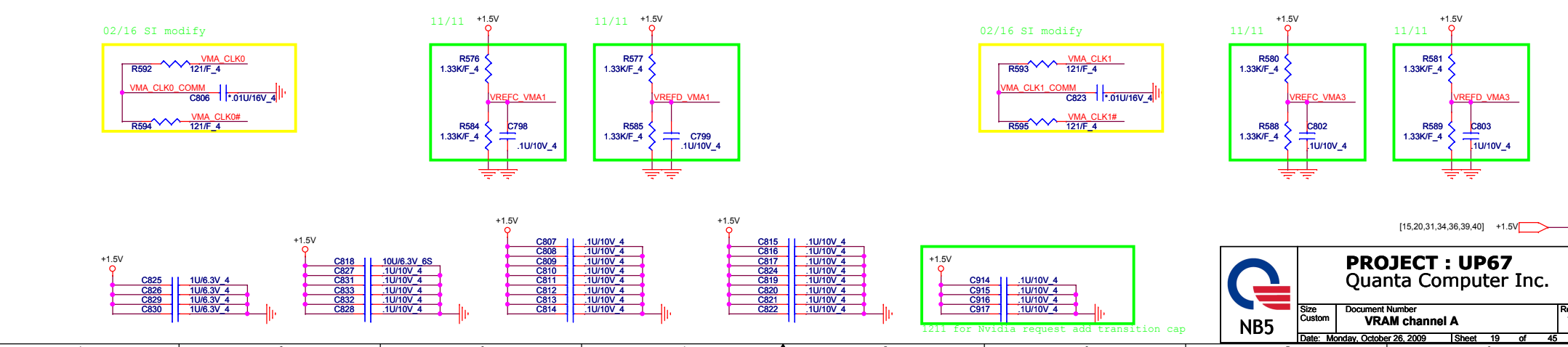
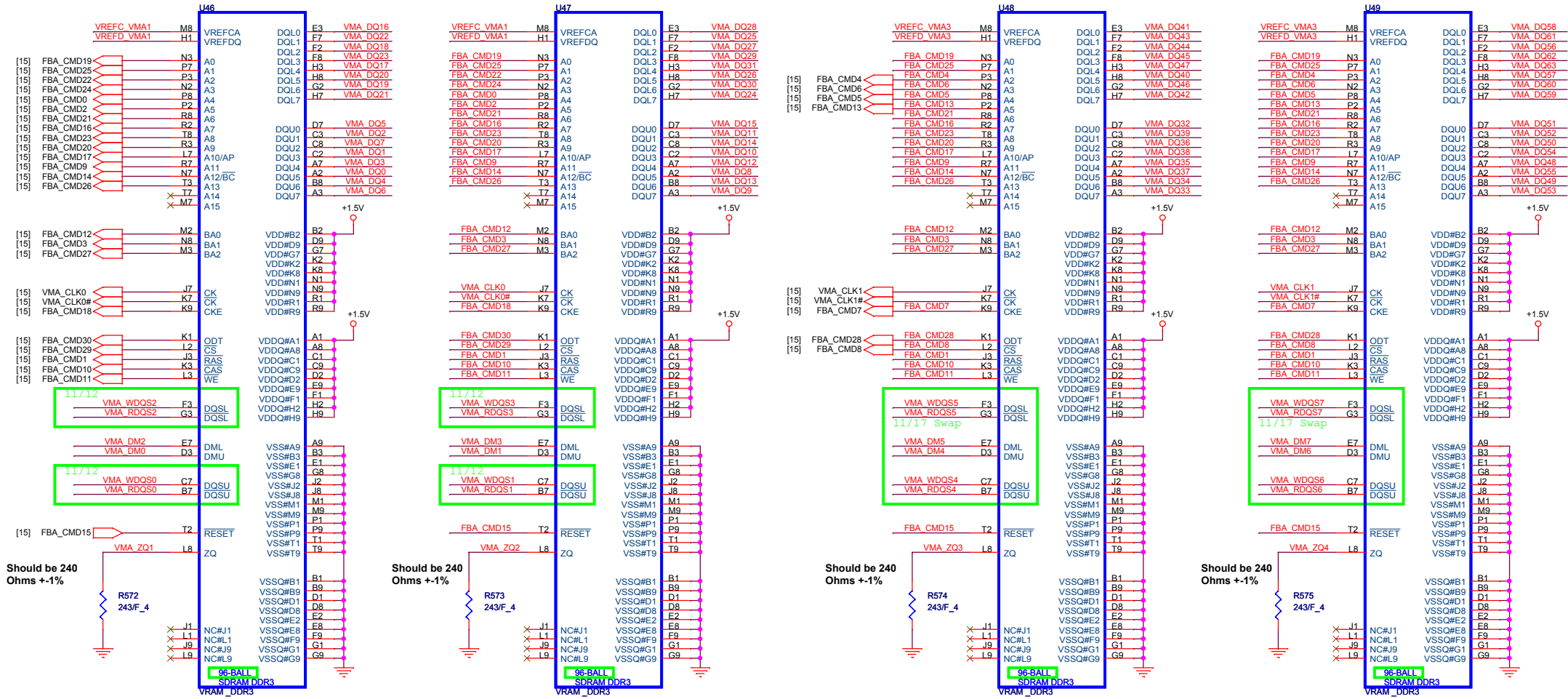
Size Custom Document Number **N10X (POWER & GND) 5/5** Rev 2A

Date: Monday, October 26, 2009 | Sheet 18 of 45

NB5



# CHANNEL A: 256MB/512MB DDR3

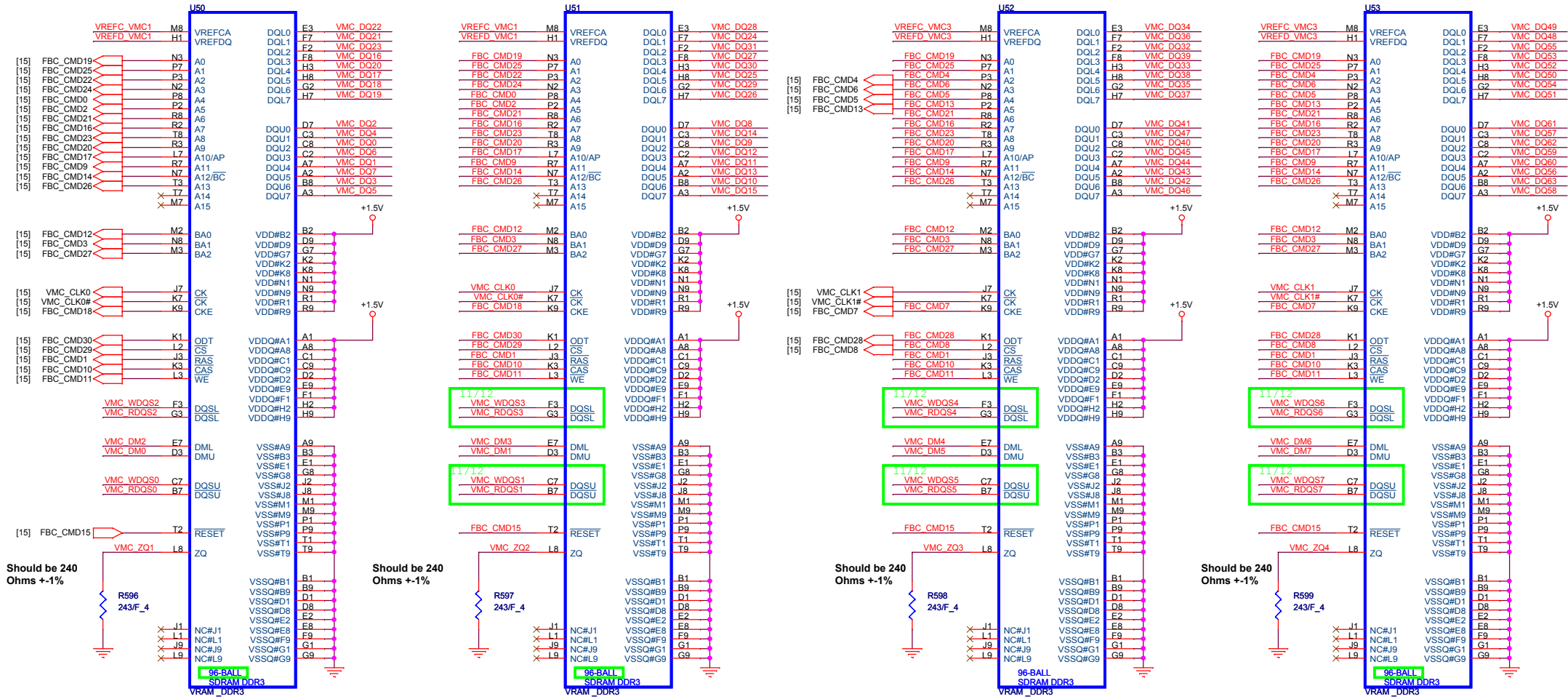


**PROJECT : UP67**  
 Quanta Computer Inc.

Size Custom Document Number VRAM channel A Rev 1A  
 Date: Monday, October 26, 2009 Sheet 19 of 45

NB5

# CHANNEL B: 256MB/512MB DDR3

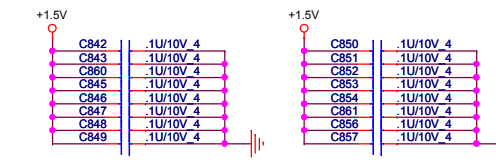
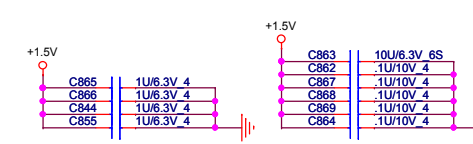
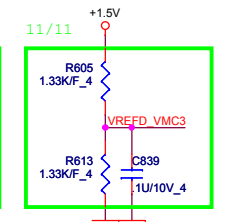
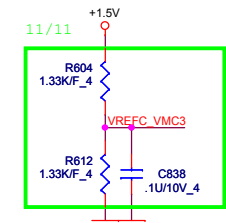
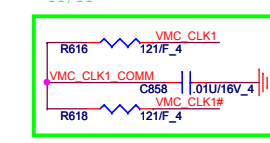
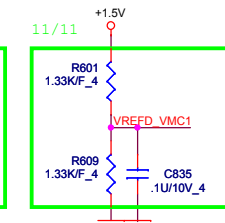
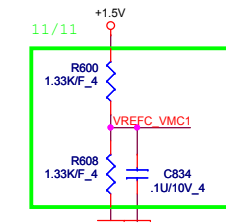
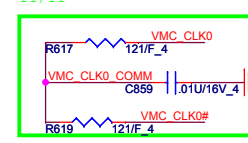


Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

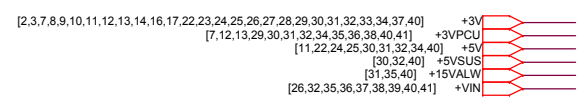
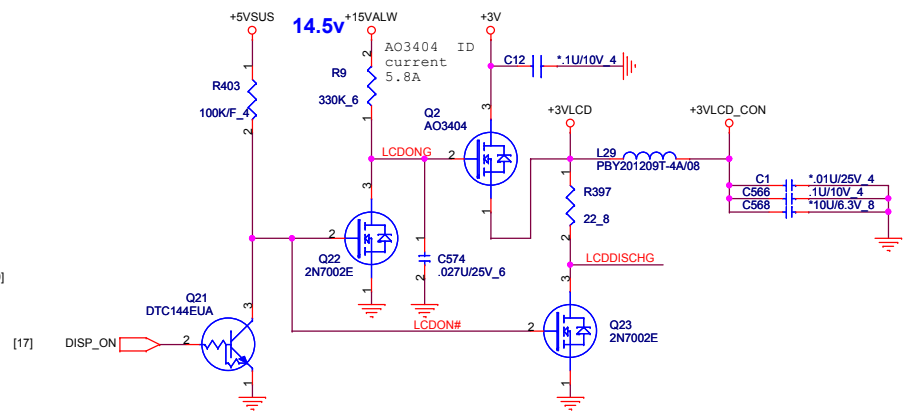
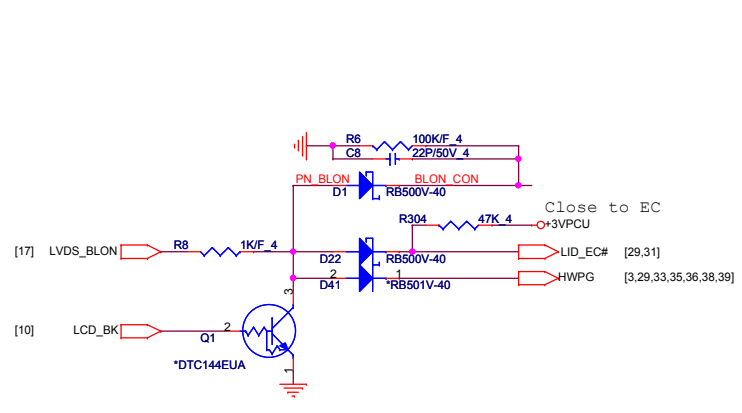
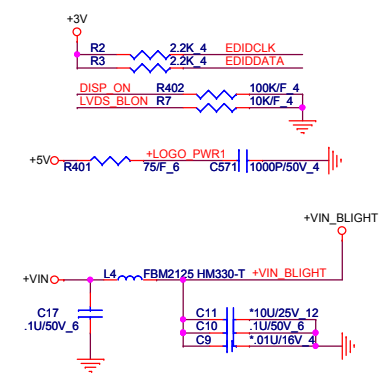
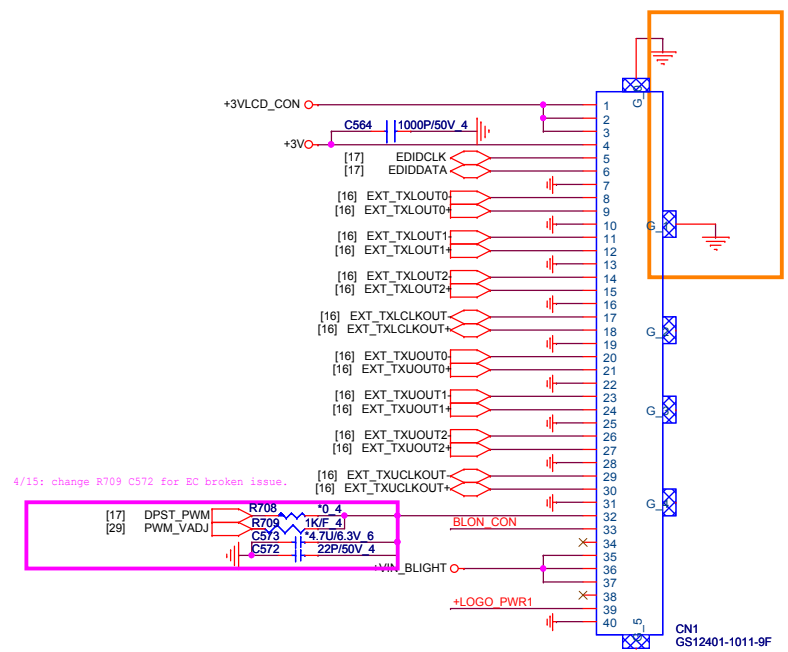


[15,19,31,34,36,39,40] +1.5V

**PROJECT : UP67**  
**Quanta Computer Inc.**

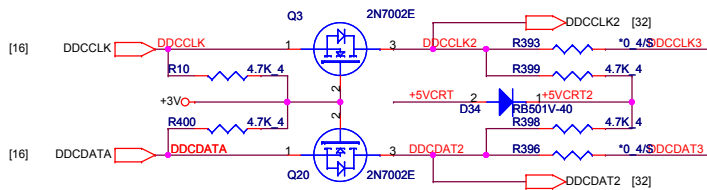
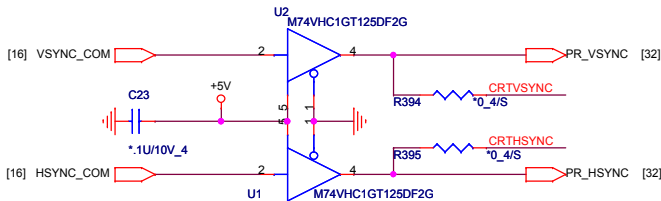
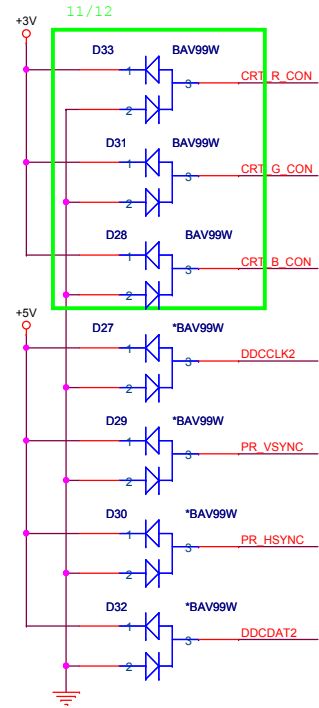
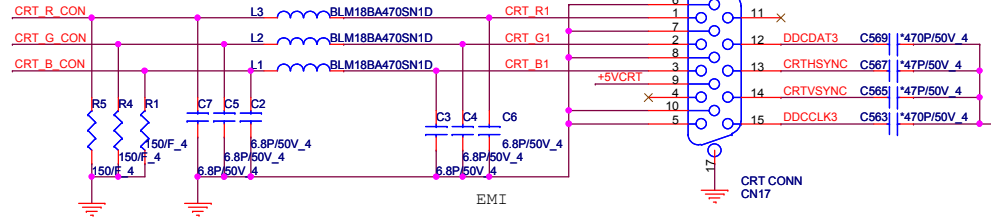
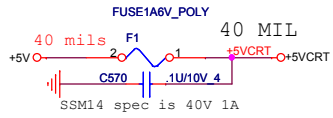
Size Custom	Document Number <b>VRAM channel B</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 20 of 45		

5/20: change PIN 41, PIN42 to GND pad for EMI.

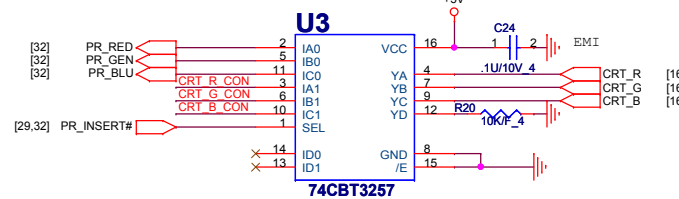


	<b>PROJECT : UP67</b> Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number <b>LCD CONN/LID function</b>	

### CRT PORT

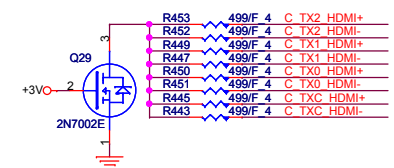
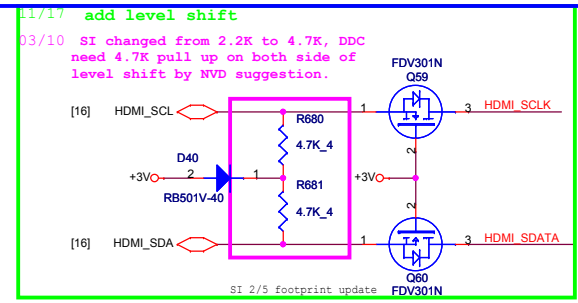
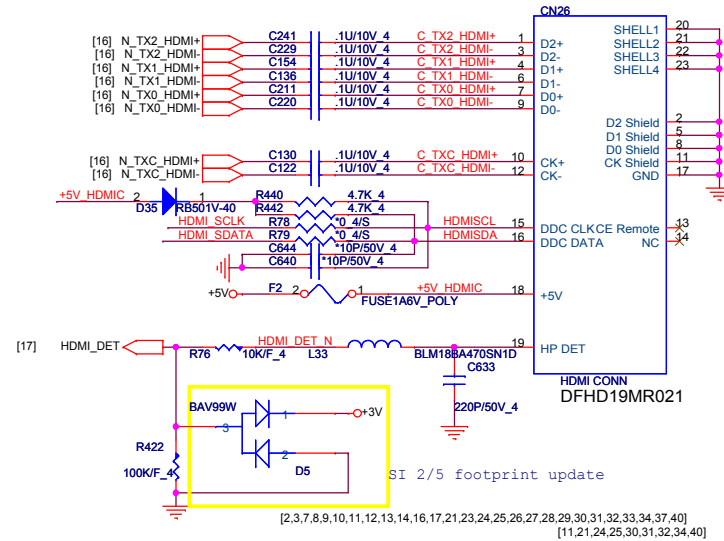


### CRT SWITCH



inputs	function
/E SET	
L L	Y - port 0
L H	Y - port 1
H X	Disconnect

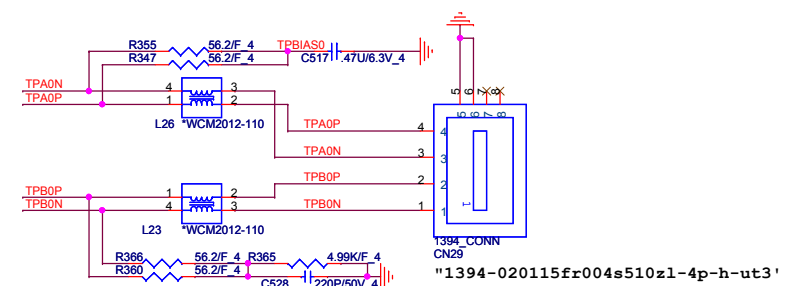
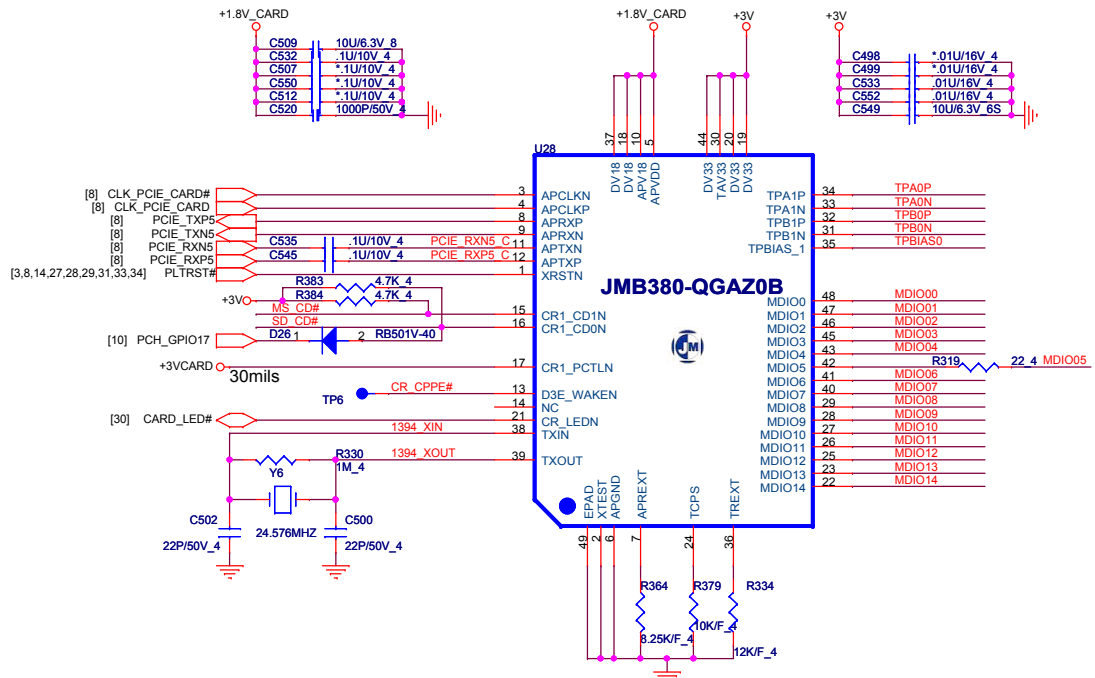
### HDMI PORT



**PROJECT : UP67**  
Quanta Computer Inc.

**NB5**

Size Custom	Document Number CRT/HDMI Conn	Rev 1A
Date: Monday, October 26, 2009		Sheet 22 of 45

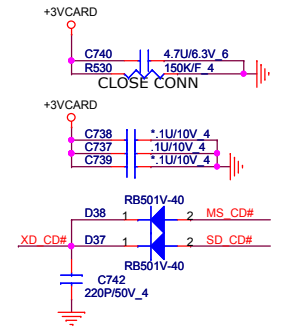
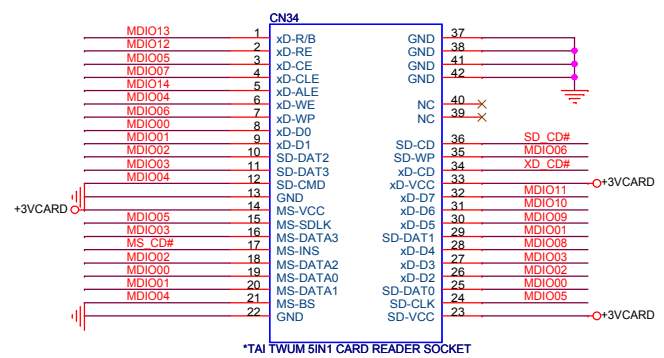
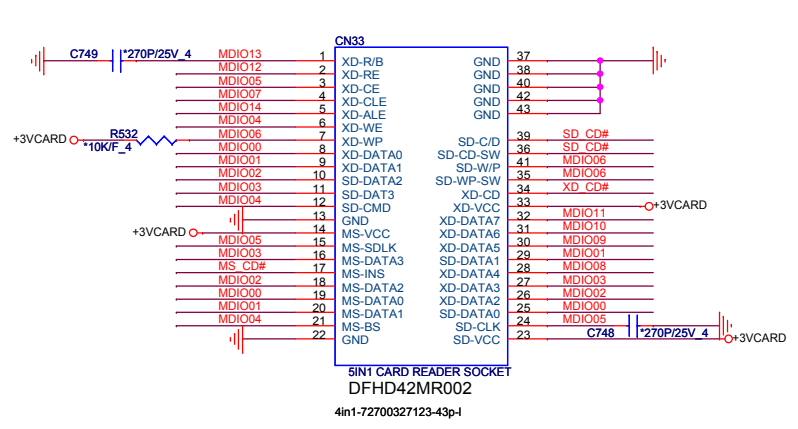


"1.394-020115fr004s510z1-4p-h-ut3"

**JMB 380 Note:**

SD/MMC	MS	XD
MDIO0	SD DAT0	MS D0
MDIO1	SD DAT1	MS D1
MDIO2	SD DAT2	MS D2
MDIO3	SD DAT3	MS D3
MDIO4	SD CMD	MS BS
MDIO5	SD CLK	MS SCLK
MDIO6	SD WP	XD WP#
MDIO7		XD CLE
MDIO8	SD DAT4	XD D4
MDIO9	SD DAT5	XD D5
MDIO10	SD DAT6	XD D6
MDIO11	SD DAT7	XD D7
MDIO12		XD RE#
MDIO13		XD RB#
MDIO14		XD LE
CR1_LEDN	SD1 LED#	MS1 LED#
CR1_PCTLN	SD1 PCTL#	MS1 PCTL#
CR1_CD0	SD1 CD#	MS1 CD#
CR1_CD1		MS1 CD#

**5 IN1 CARD READER  
XD, MMC/SD, MS/MSP**

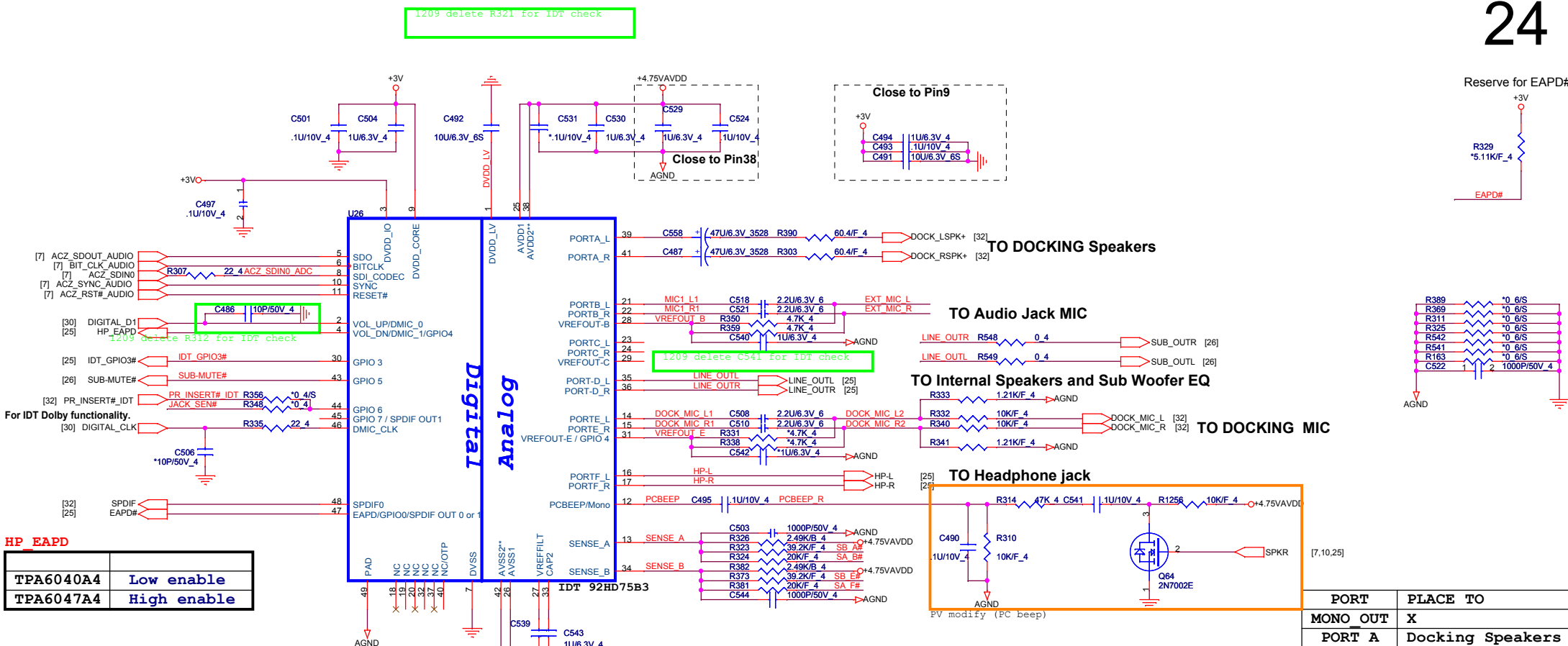


[2,3,7,8,9,10,11,12,13,14,16,17,21,22,24,25,26,27,28,29,30,31,32,33,34,37,40]

**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>JMB380 &amp; CR SOCKET</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 23 of 45		

Reserve for EAPD#



**HP\_EAPD**

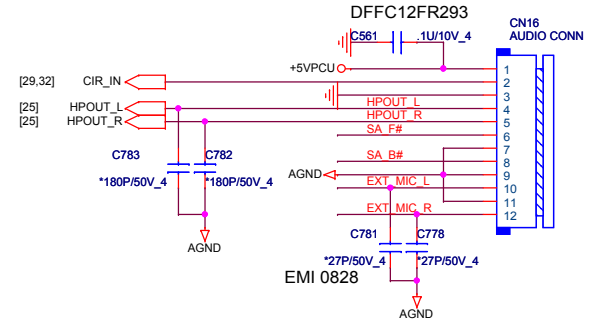
TPA6040A4	Low enable
TPA6047A4	High enable

<b>Codec</b>	<b>92HD71</b>	<b>92HD75</b>
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

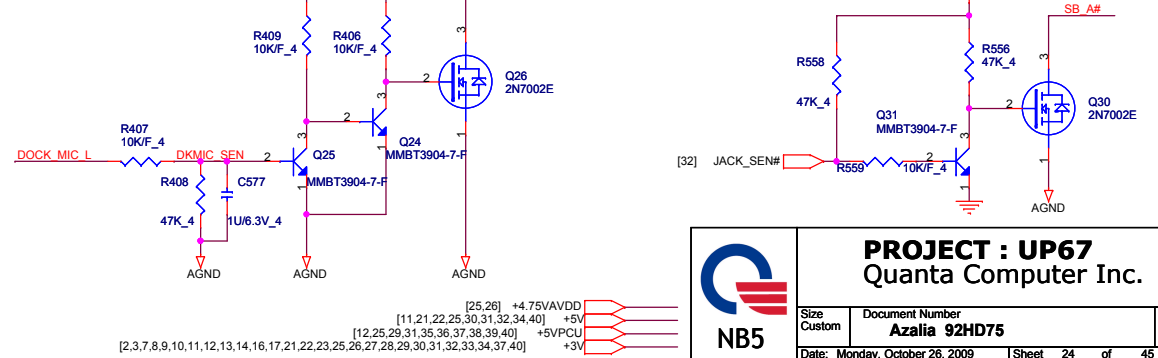
5.11K P/N: CS25112FB15

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

## TO AUDIO/B CON.



## DOCK MIC DETECT



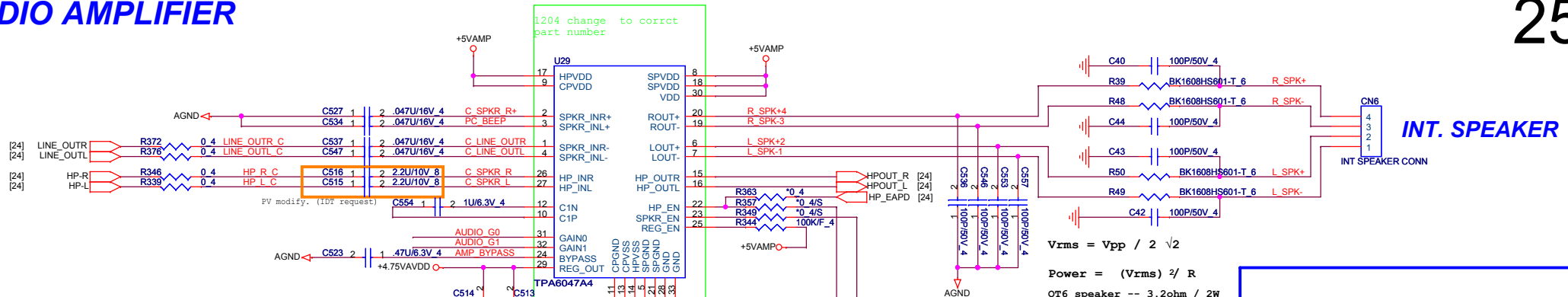
**PROJECT : UP67**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Azalia 92HD75</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 24 of 45		

[11,21,22,25,30,31,32,34,40] +5V  
 [12,25,29,31,35,36,37,38,39,40] +5VPCU  
 [2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,25,26,27,28,29,30,31,32,33,34,37,40] +3V

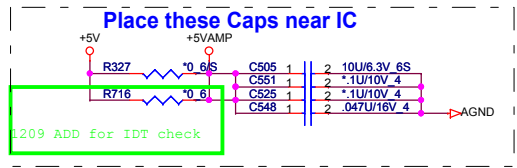


# AUDIO AMPLIFIER



## INT. SPEAKER

$V_{rms} = V_{pp} / 2 \sqrt{2}$   
 Power =  $(V_{rms})^2 / R$   
 QT6 speaker -- 3.2ohm / 2W

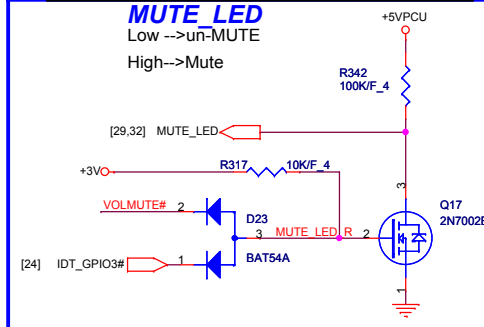


### 6040A Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

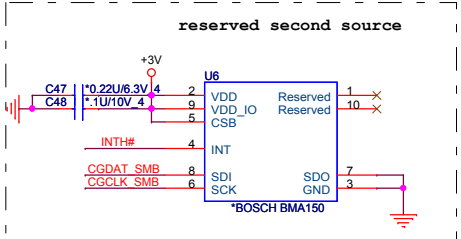
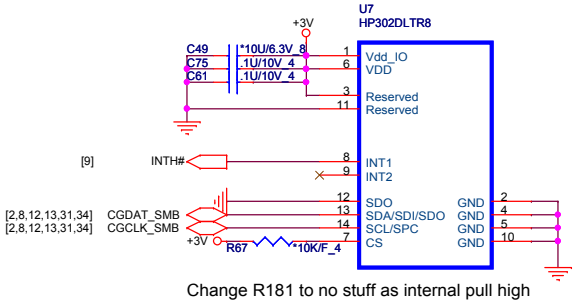
### PIN23 SPKR\_EN

TPA6040A4	Low enable
TPA6047A4	High enable



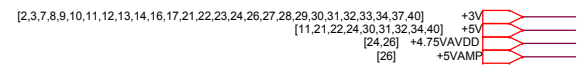
# Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

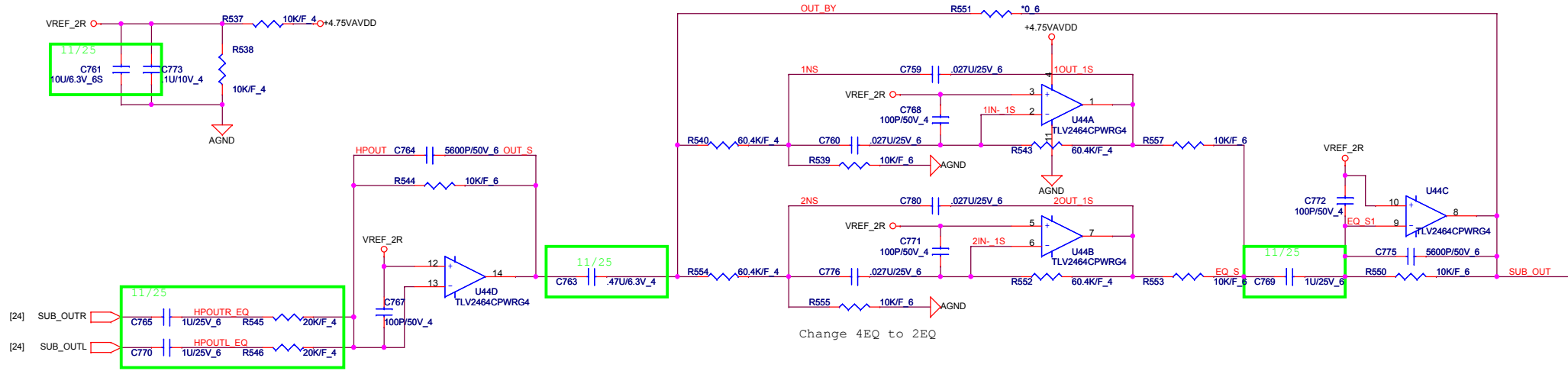
Pin 12: Low 38hex  
 Pin 12: unconnected/floating 3Ahex



**PROJECT : UP67**  
 Quanta Computer Inc.

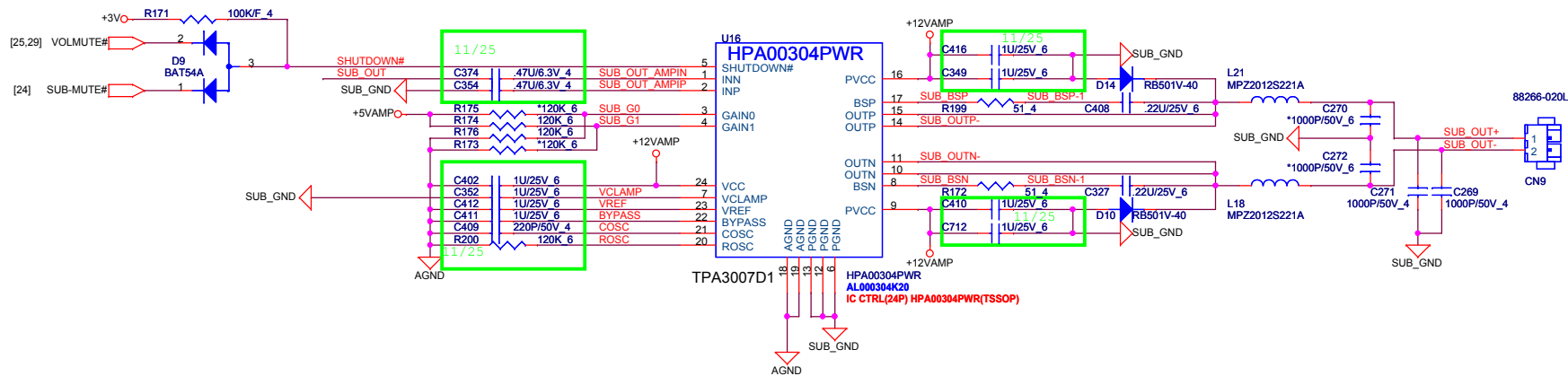
Size Custom Document Number AMP\_TPA6047/Accelerometer Rev 1A

Date: Monday, October 26, 2009 | Sheet 25 of 45



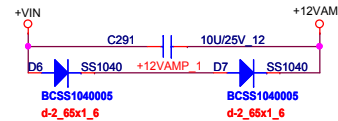
MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

Change 4EQ to 2EQ



## Sub-Woofer power

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

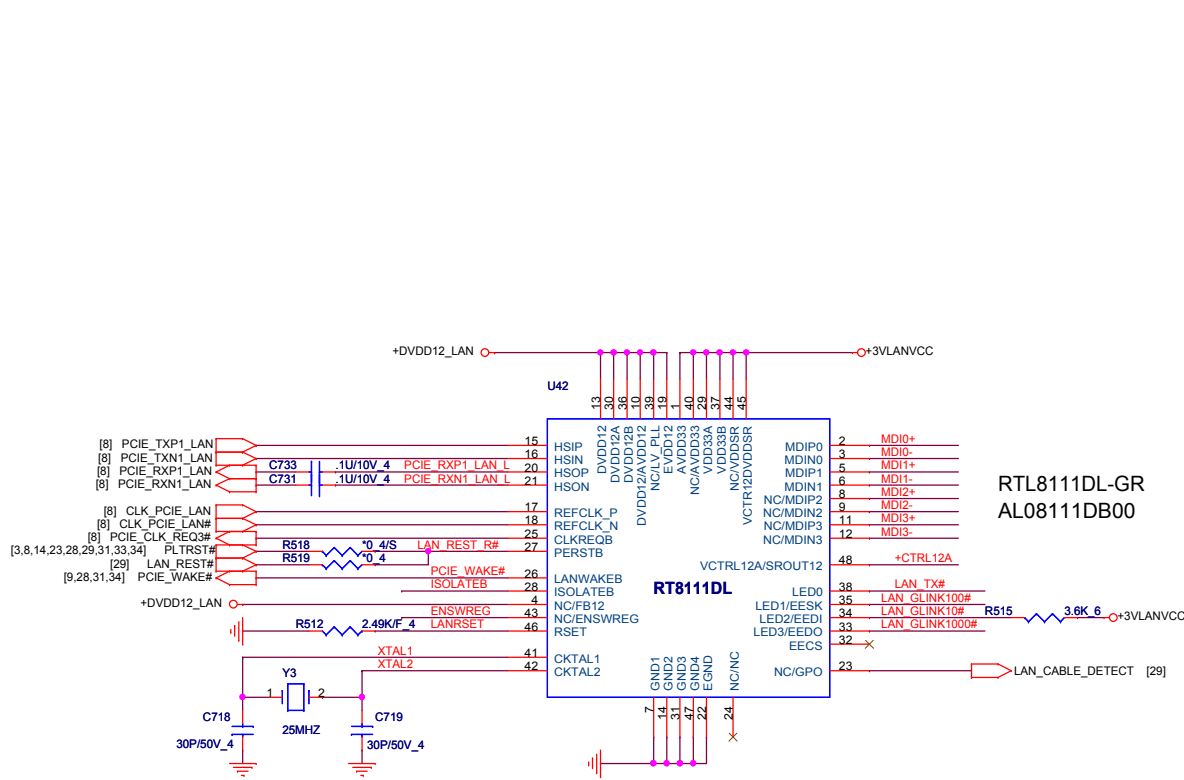


[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V  
 [21,32,35,36,37,38,39,40,41] +VIN  
 [25] +5VAMP  
 [24,25] +4.75VAVDD

### PROJECT : UP67

### Quanta Computer Inc.

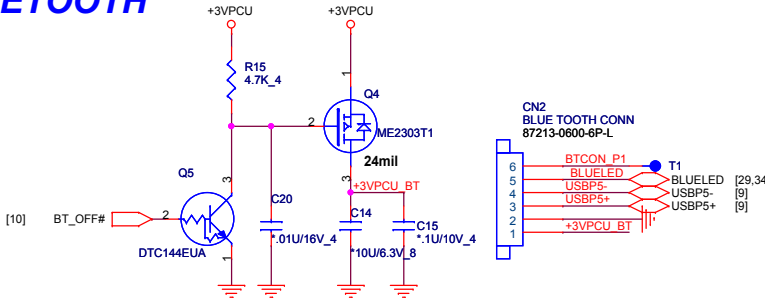
Size Custom	Document Number <b>SUBWOOFER (EQ &amp; AMP.)</b>	Rev 1A
Date: Monday, October 26, 2009   Sheet 26 of 45		



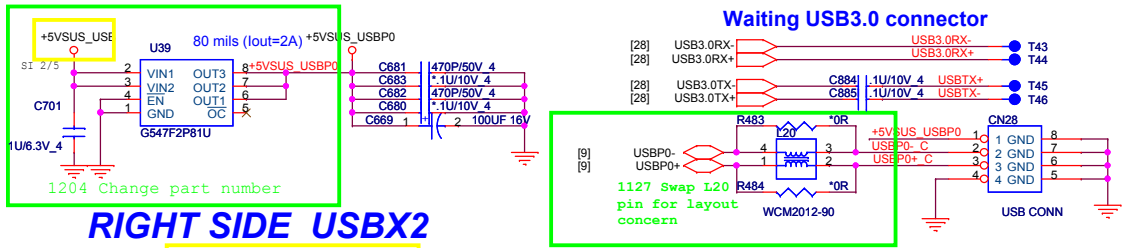




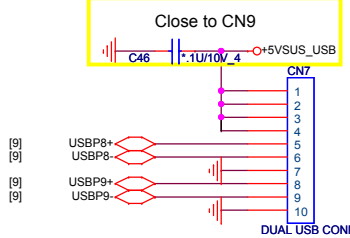
**BLUETOOTH**



**LEFT SIDE USBX1 and E-SATA/USB COMBO**

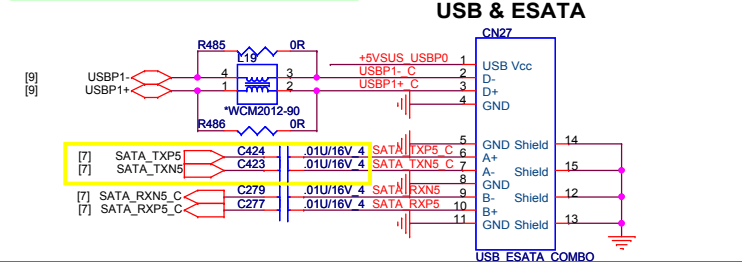
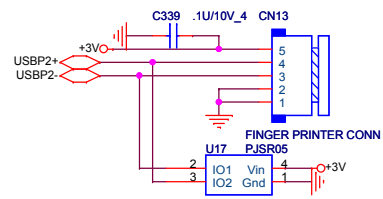


**RIGHT SIDE USBX2**



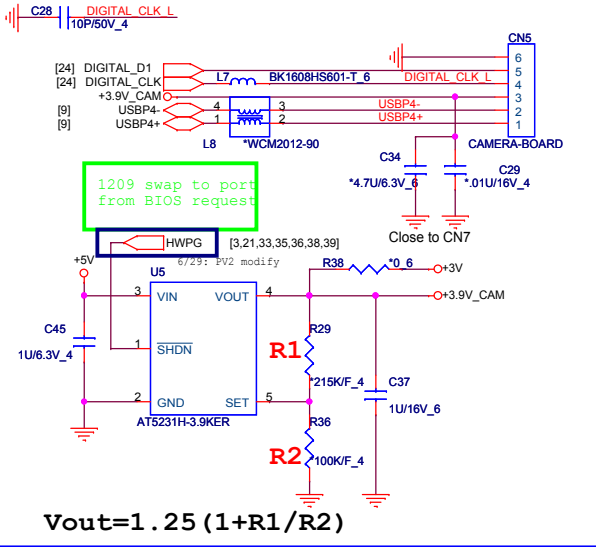
**USB fingerprint CON**

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

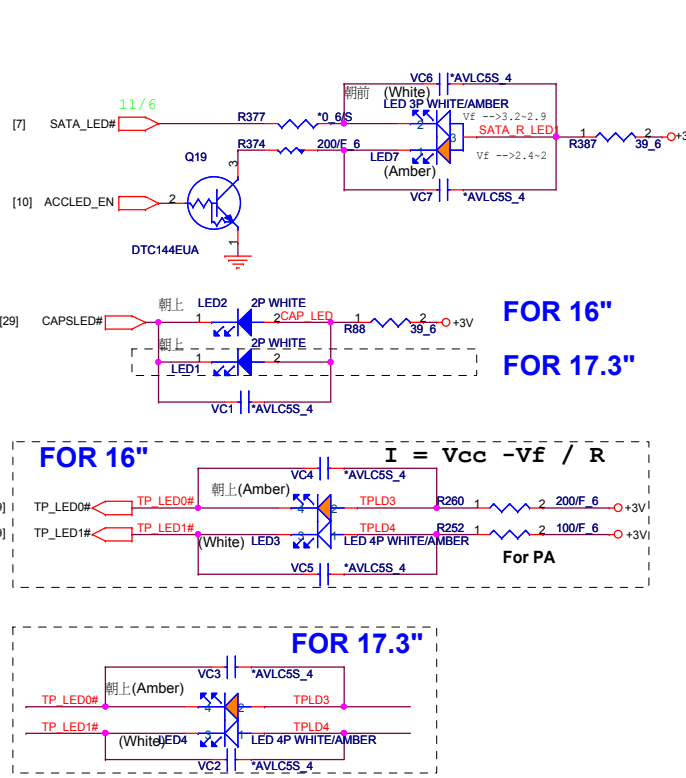


**USB CAMERA /DIGITAL MIC CONNECT**

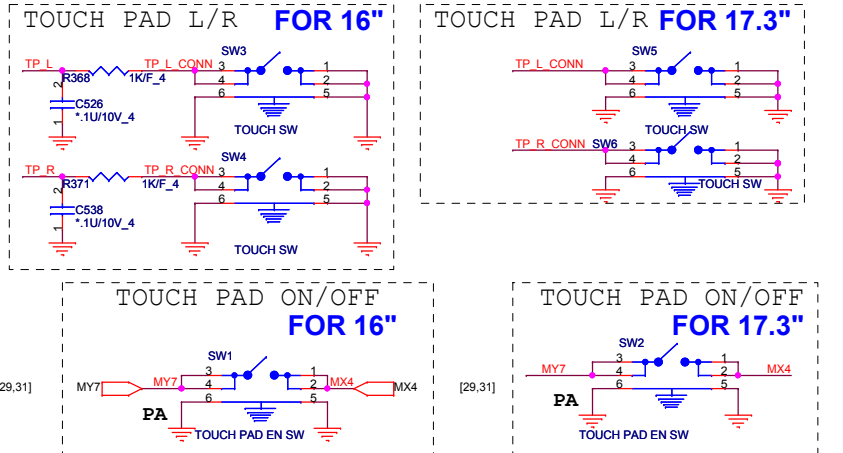
Add for EMI solution



**LED**

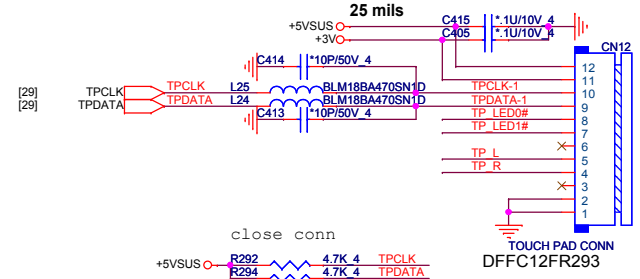
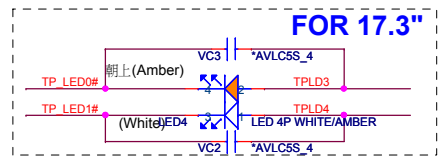
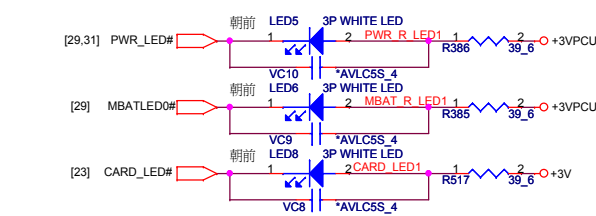


**TOUCH PAD CONNECTOR & ON/OFF BOTTOM**



$V_{out} = 1.25 (1 + R1/R2)$

$I = \frac{V_{cc} - V_f}{R}$



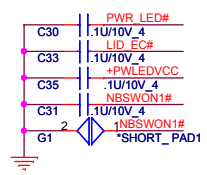
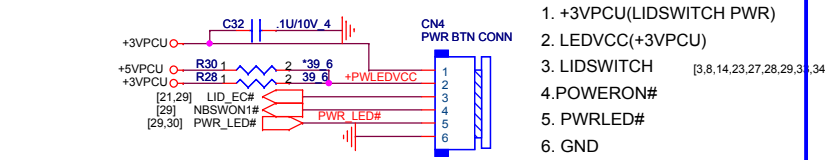
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40] +3VPCU  
 [7,12,13,21,29,31,32,34,35,36,38,40,41] +5V  
 [11,21,22,24,25,31,32,34,40] +5VSUS  
 [21,32,40] +3V

**PROJECT : UP67**  
**Quanta Computer Inc.**

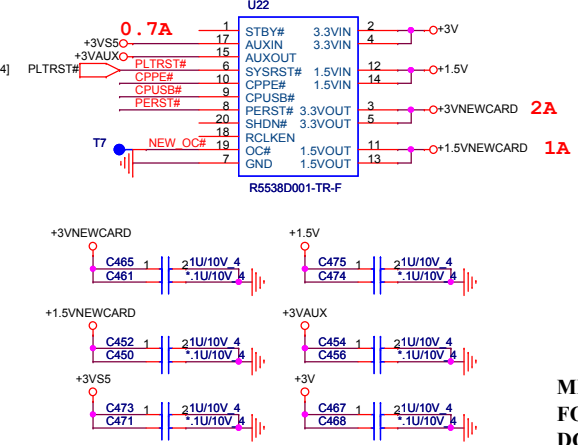
Size: Custom Document Number: BT/WC/F/ESATA/USB/LED Rev: 1A

Date: Monday, October 26, 2009 | Sheet 30 of 45

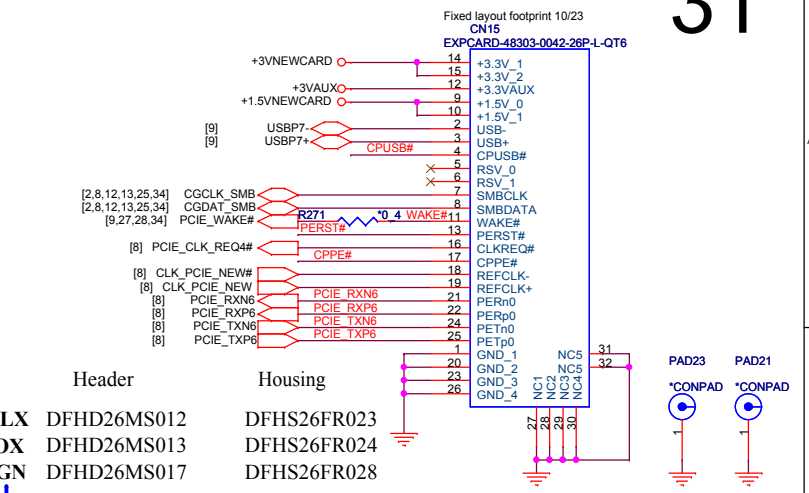
# POWER BOTTON CONNECT



# NEWCARD

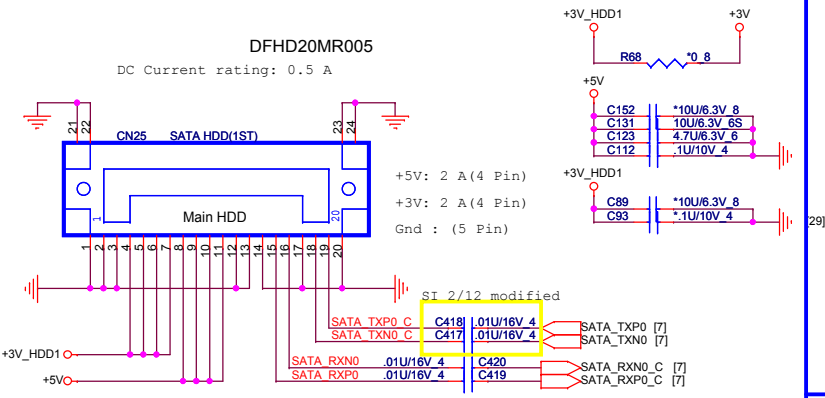


# NEWCARD (PCIEXPRESS\*1 + USB\*1)

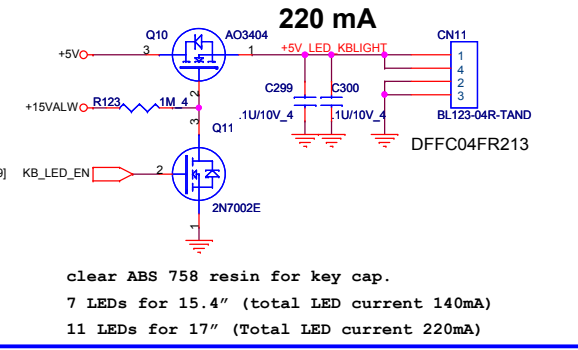


31

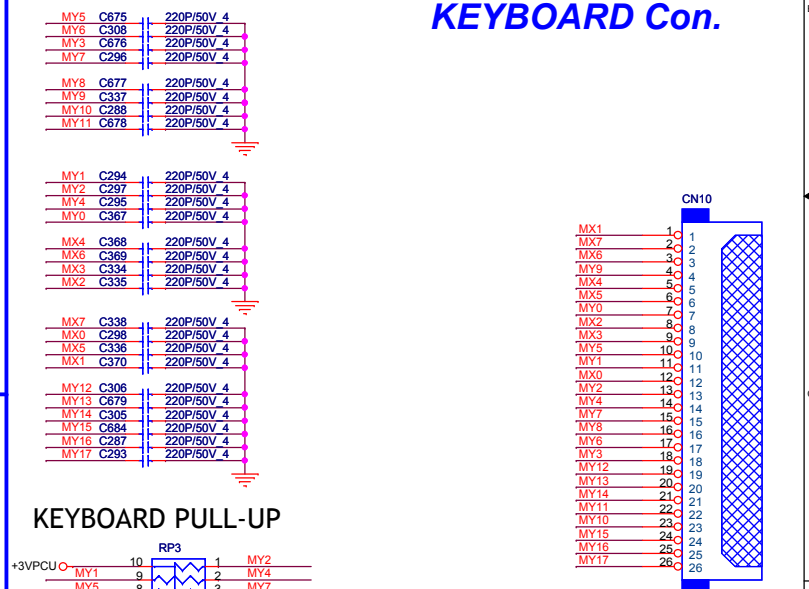
# SATA HDD CONNECTOR



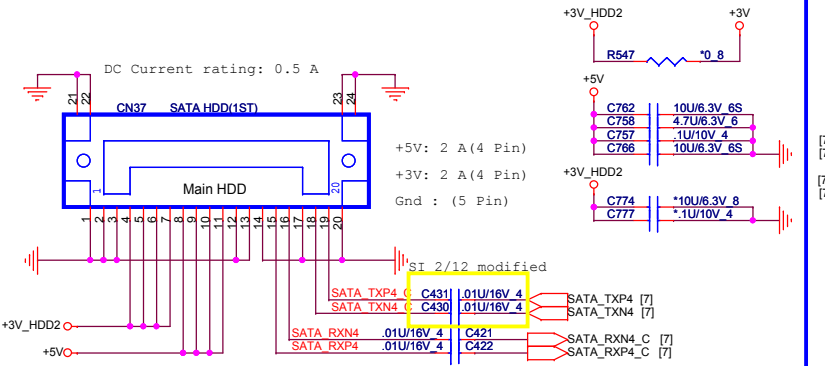
# Backlight Keyboard Con.



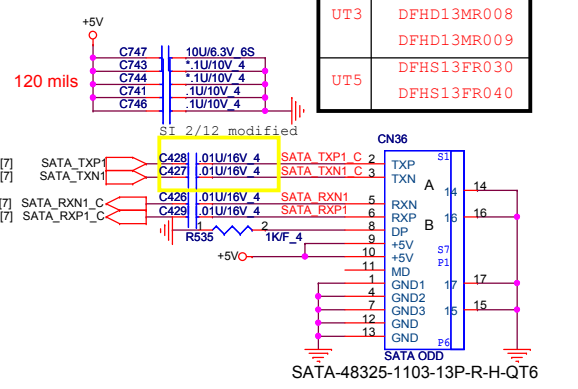
# KEYBOARD Con.



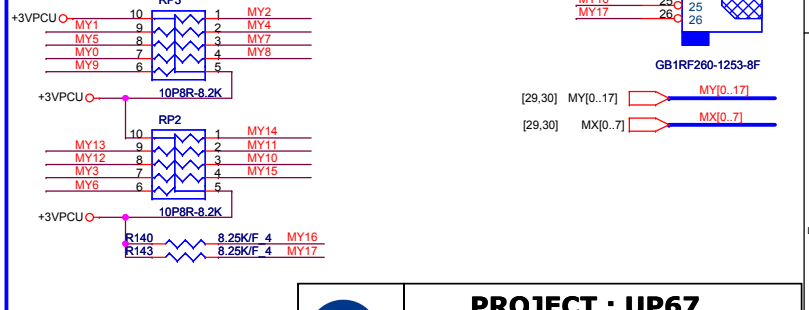
# SATA\_2 CONNECTOR



# SATA CD-ROM



# KEYBOARD PULL-UP

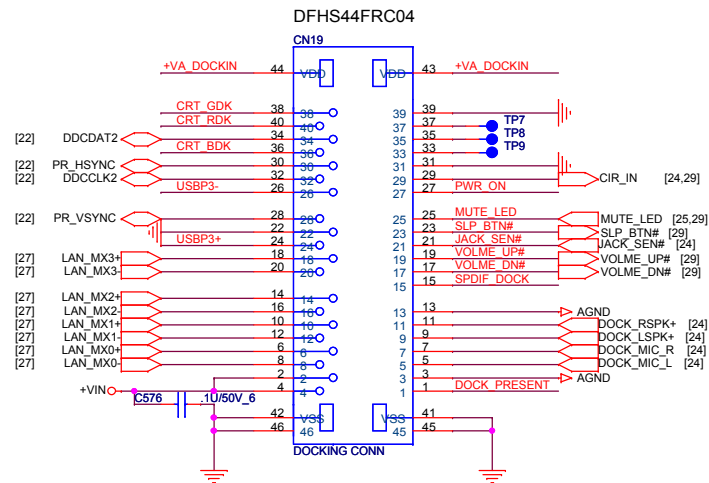


**PROJECT : UP67**  
 Quanta Computer Inc.

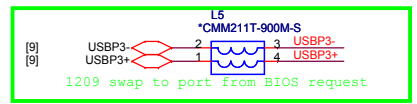
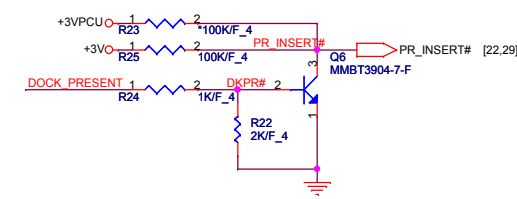
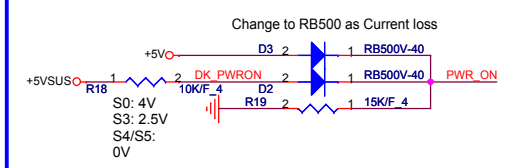
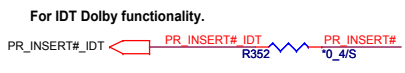
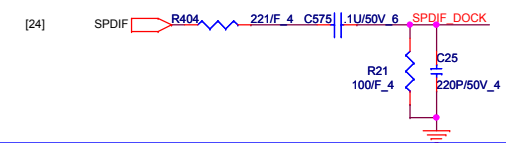
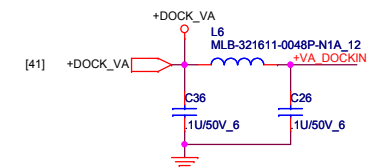
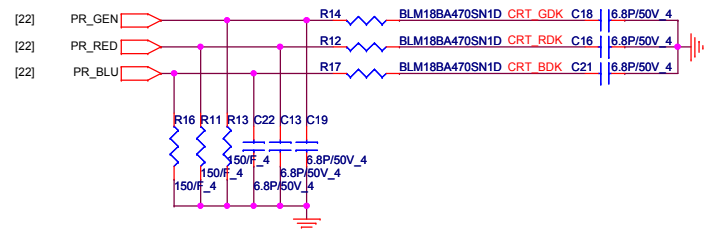
NB5

Size Custom	Document Number ODD/HDD/NEW CARD/PW/KB	Rev 1A
Date: Monday, October 26, 2009		Sheet 31 of 45

# CABLE DOCK

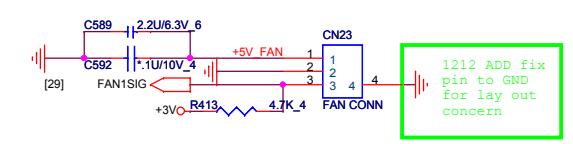


Delete CX08T470000 as CRT rising time and falling time request

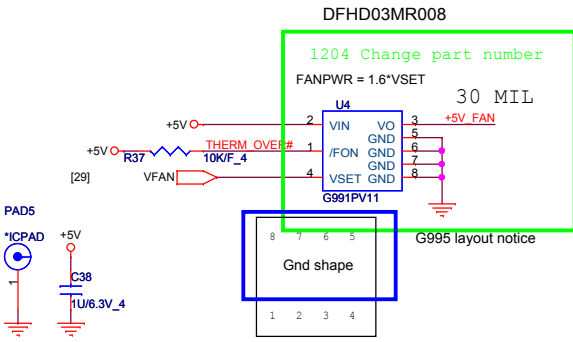


6/1 : PV For EMI request

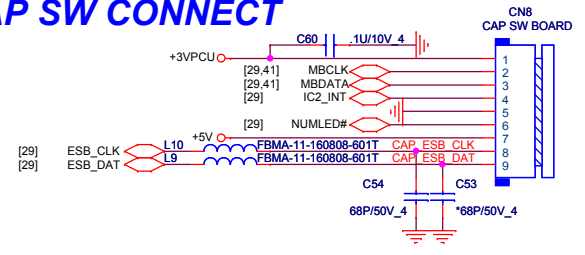
## CPU FAN



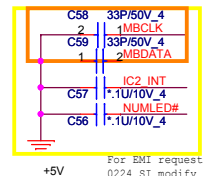
1212 ADD fix pin to GND for lay out concern



## CAP SW CONNECT

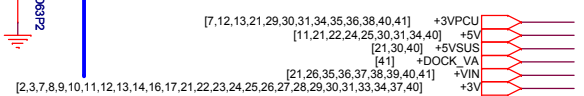
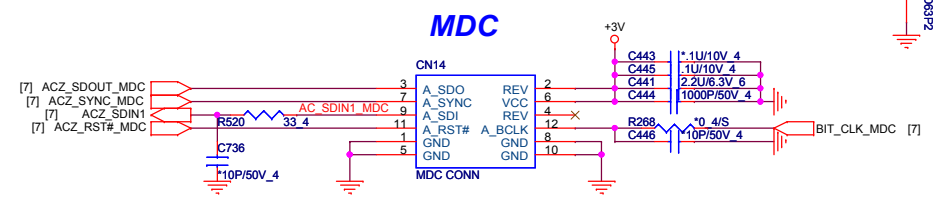


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP\_INT
5. GND
6. NUM LOCK LED
7. +5V\_LED
8. ESB\_CLK
9. ESB\_DAT

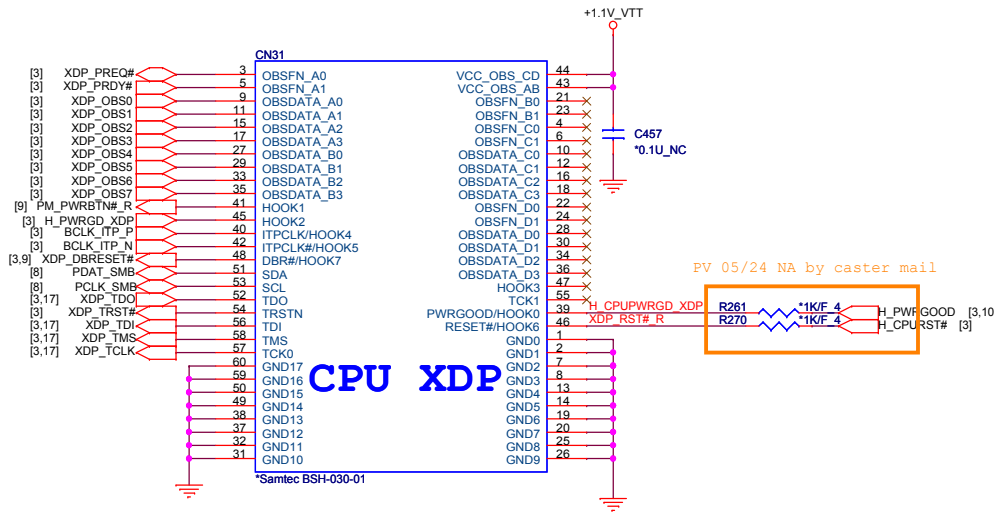


For EMI request 0224 S1 modify

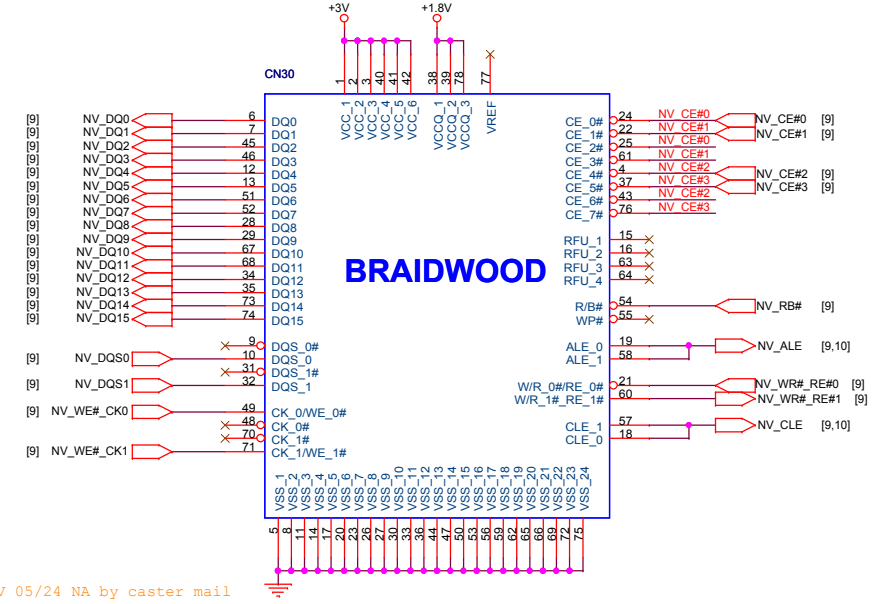
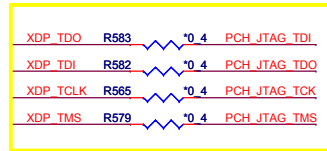
## Modem CONN



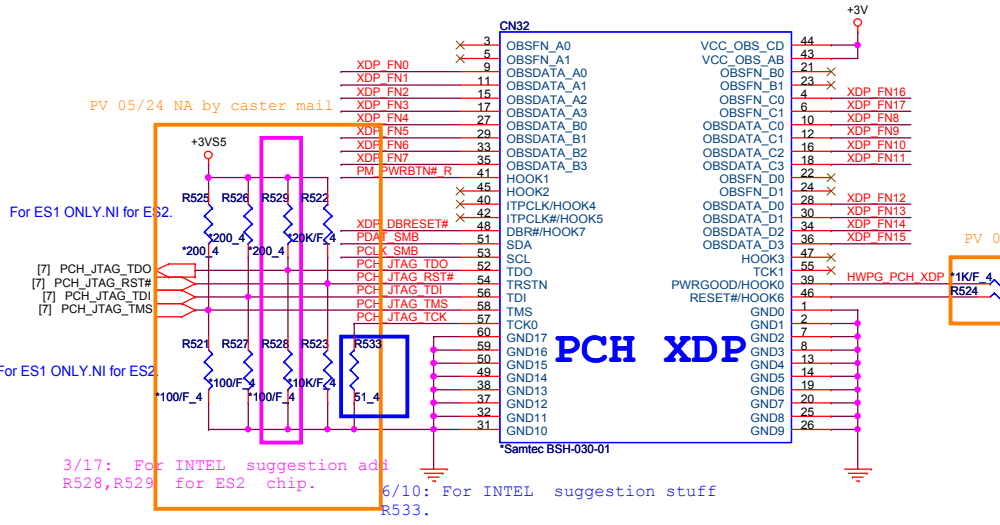
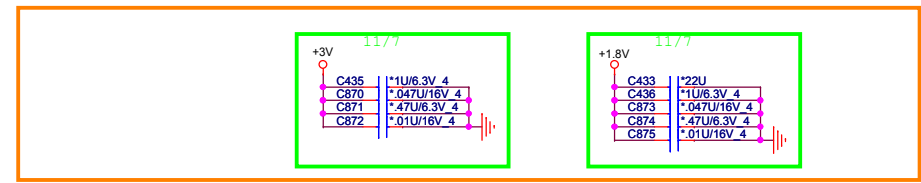




Reserve for BSDL



PV 05/24 NA by caster mail

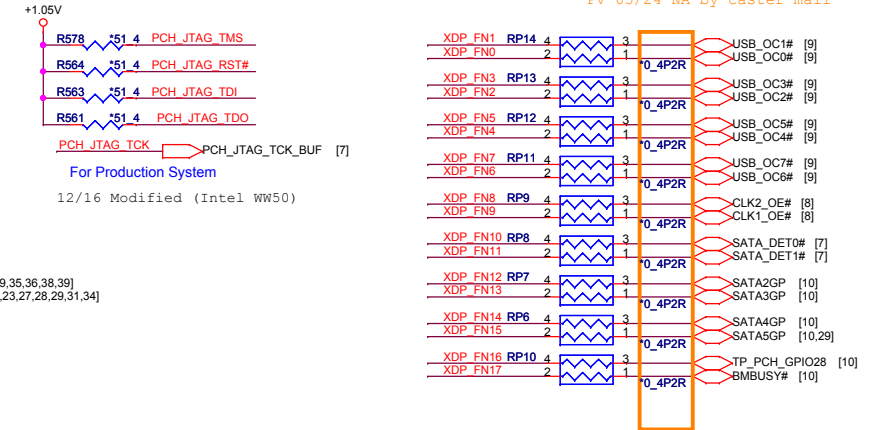


For ES1 ONLY.NI for ES2.

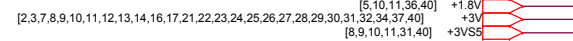
For ES1 ONLY.NI for ES2


3/17: For INTEL suggestion add R528,R529 for ES2 chip.

6/10: For INTEL suggestion stuff R533.



For Production System  
12/16 Modified (Intel WW50)





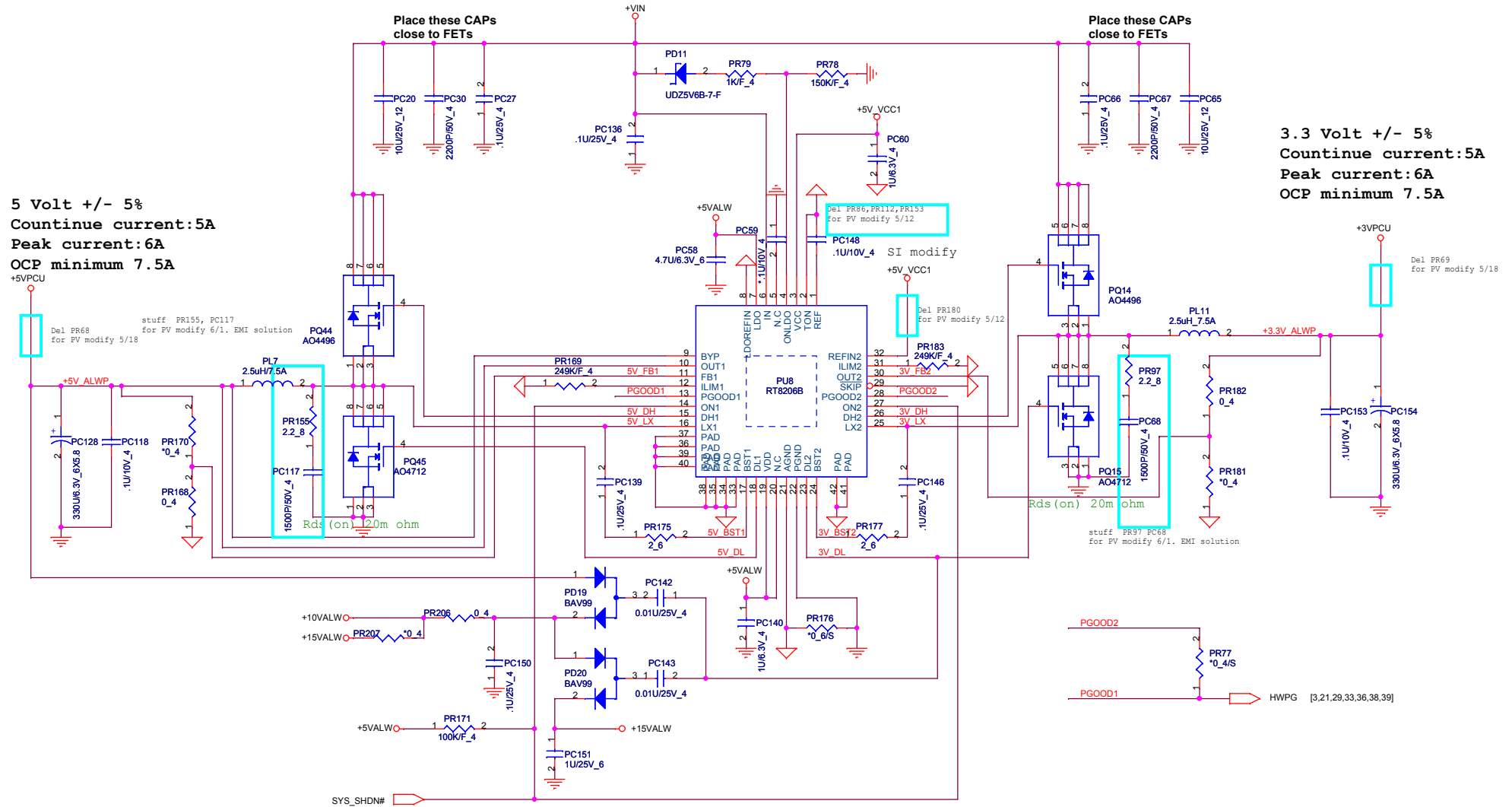
**NB5**

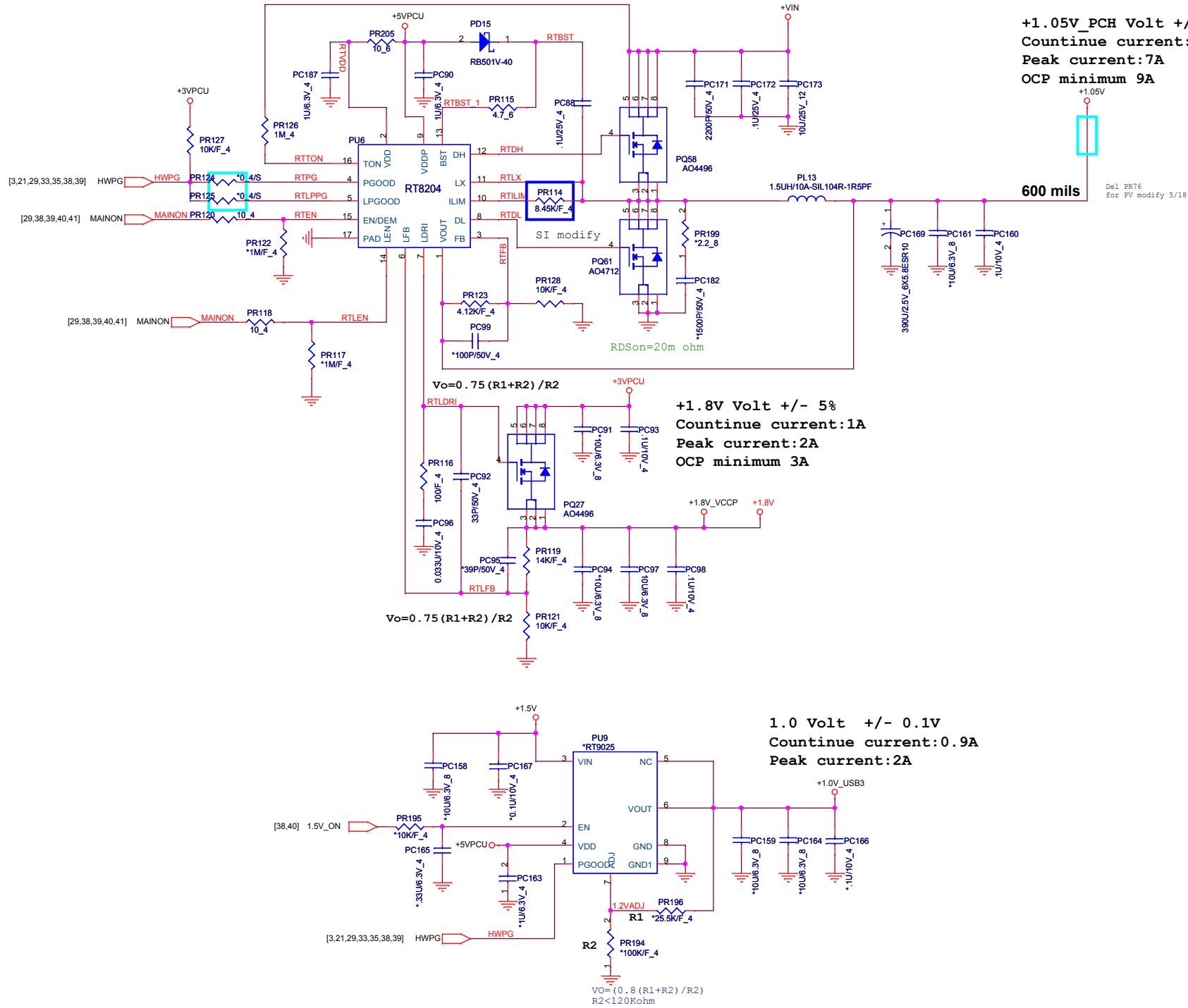
**PROJECT : UP67**  
**Quanta Computer Inc.**


Rev 1A

Size Custom	Document Number <b>XDP/BRAIDWOOD</b>	Date Monday, October 26, 2009
Sheet 33 of 45		







	<b>PROJECT : UP67</b> Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number +5V/+3V (RT8206B)	

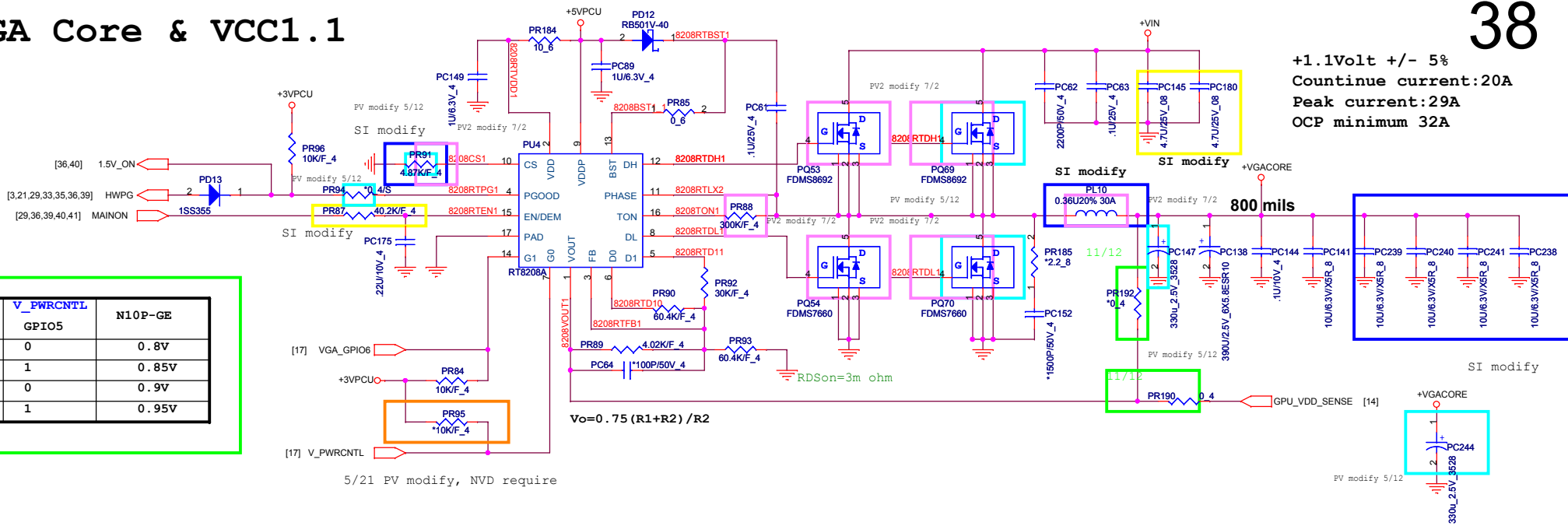


# VGA Core & VCC1.1

**+1.1Volt +/- 5%**  
**Countinue current:20A**  
**Peak current:29A**  
**OCp minimum 32A**

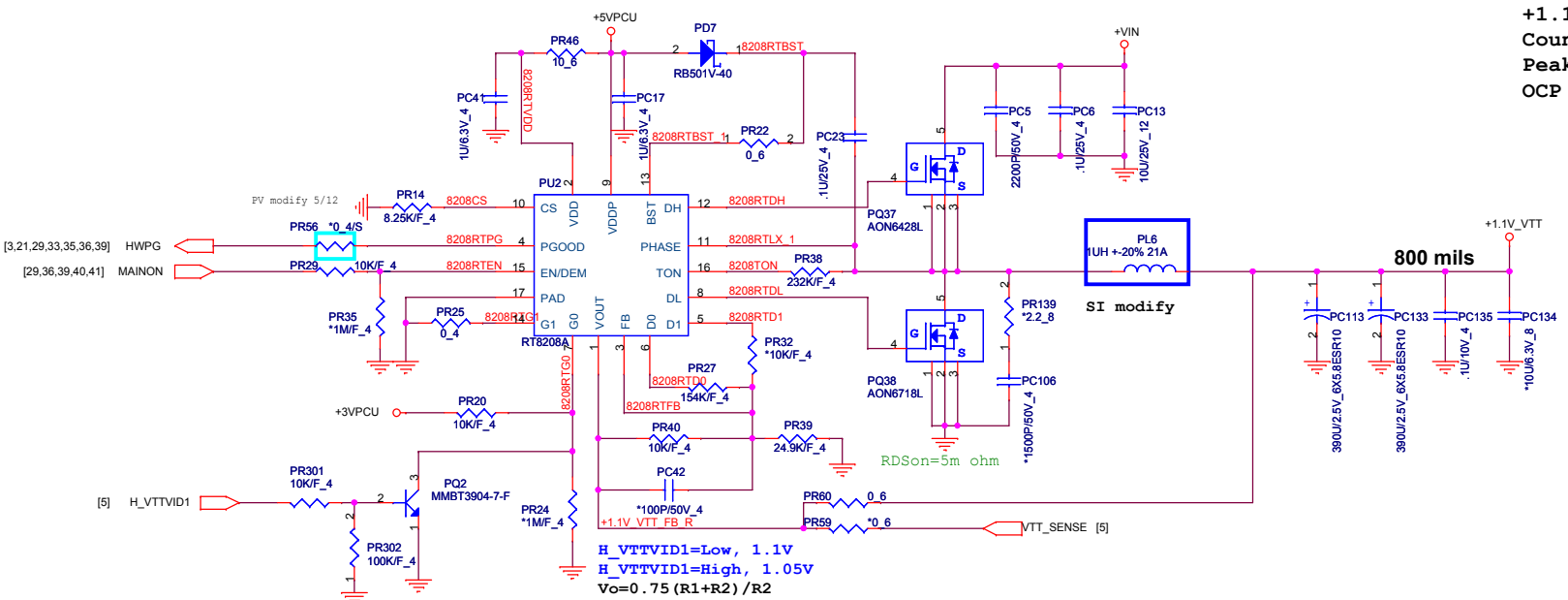
11/13

VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



5/21 PV modify, NVD require

**+1.1V\_PCH Volt +/- 5%**  
**Countinue current:12A**  
**Peak current:15A**  
**OCp minimum 18A**



H\_VTTVID1=Low, 1.1V  
 H\_VTTVID1=High, 1.05V  
 $V_o = 0.75 (R1+R2) / R2$

	<b>PROJECT : UP67</b> Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number <b>+1.1V_VTT/VGA Core (RT8208)</b>		
	Date: Monday, October 26, 2009   Sheet 38 of 45			

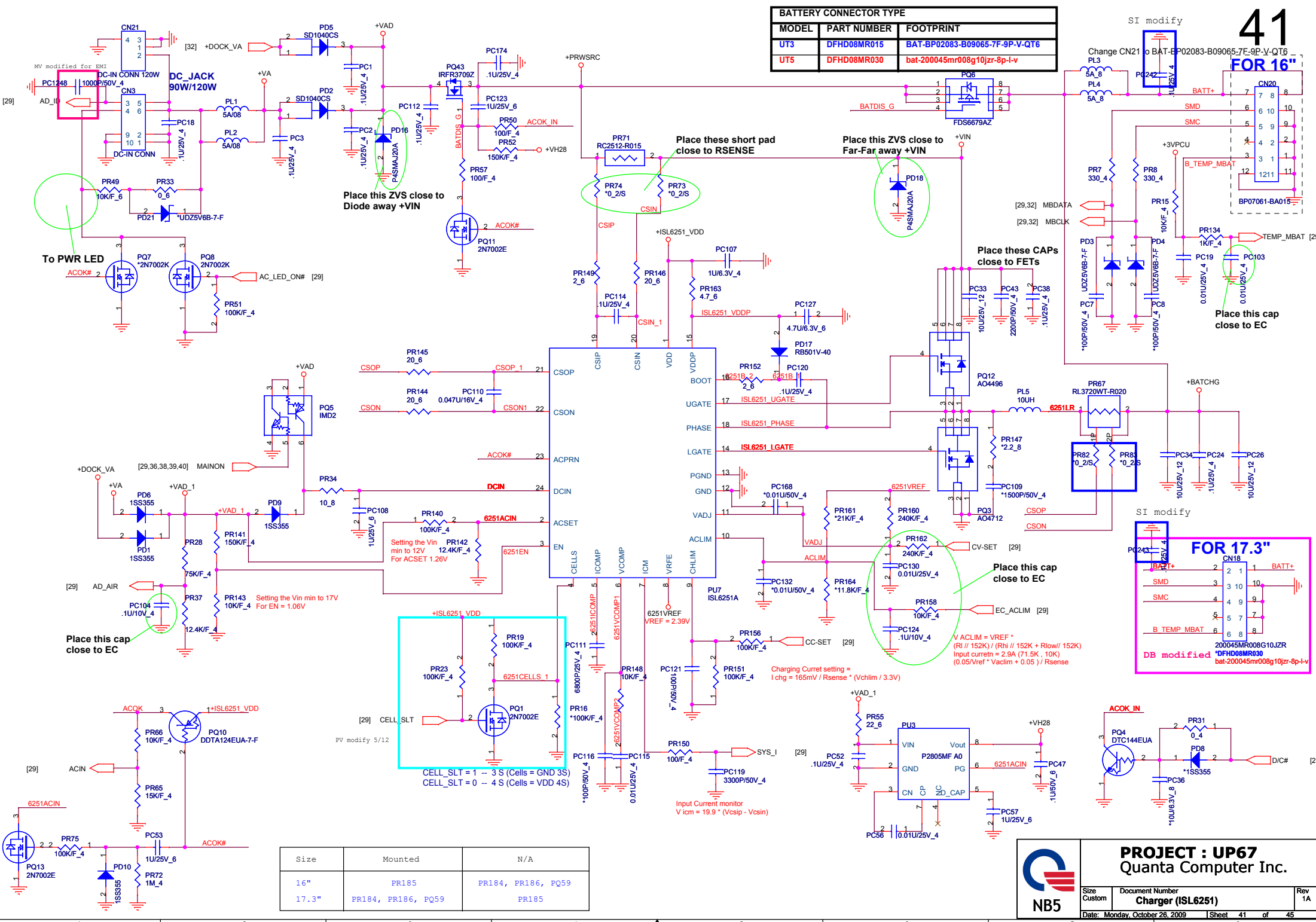




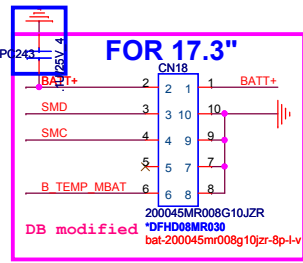


BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

41  
FOR 16"



Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185



**PROJECT : UP67**  
Quanta Computer Inc.

Size Custom	Document Number <b>Charger (ISL6251)</b>	Rev 1A
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Date: Monday, October 26, 2009 | Sheet 41 of 45

# Power up sequence

