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HP laptop notebook power leakage BBHP timing

Notebook , timing , BBHP , leakage

Electrical maintenance on the motherboard:

1. the electrical timing

When we plugged in Adapter19VIN, the power flows to have a 5VPCU, 3VPCU voltage, it is by the PU10 (MAX1999) automatically generated, then the machine is in standby mode.

When we press the Power Button, NBSWON # moment there is a low level, which gave low 97551,97551 received signal to generate signals DNBSWON #, DNBSWON distributed to South Bridge, also issued S5-ON 11th pin to 1845 produce 1.5V_S5. S5-ON input PQ128 PQ132 generated through S5-OND.

S5-OND and PQ141 PQ127 were generated by 5V_S5 and 3V_S5.

3V_S5, 5V_S5, 1.5V_S5 time power to the South Bridge.

South Bridge received DNBSWON low, it occurs SUSB #, SUSC # 2 high sent to 97551, 97551 received SUSB #, SUSC # after have had a SUSON, MAINON #, VRON. SUSON signals into SUSD signal sent PQ143, PQ145 tube arises 3VSUS, 5VSUS, and SUSON sent to MAX1845 generate 2.5VSUS.

MAINON # generated by PU7 SMDDR-VTERM. At the same time and by PQ119 PQ125 into MAIND send PQ143, PQ145, PQ148, PQ153 produce +3 V, +5 V, +2.5 V, +1.5 V voltages.

VRON gave PU9 (MAX1907), PU5 (1992E) generated VCC-CORE and VCCP voltage. PU6, PU4 signals generated HWPG to 97,551, then PU3, PU5 also various feedback signals to generate a HWPG 97551.

At this point the M / B of the main voltage in each group have been OK back HWPG voltage feedback signal with convergence, the equivalent of a HWPG "and" relationship, such as including any group for the low feedback HWPG this POWER OK 97551 occurs when the instruction to turn off opening of voltage, such as the OK is HWPG constant as high as 97,551, after receiving HWPG produce PWROK signal sent to SB Southbridge, Southbridge SB produced after the PCI RST # generated through U42 PCIRST # passed to North Bridge. North Bridge before they produce the CPURST #. Signal

The IC has the **engine, Album Download** 4.5V to 24V input voltage range, 1.5% output voltage accuracy, 3.3V and 5V two modules, with software control within the opening, closing fast power management system and over-voltage protection function.

Main fault: 3VPCU or 5VPCU bad output (usually board plug 19vin, there are two voltage output)

1. VIN_1999 input 19V voltage problems.
2. Test 8 pin reference voltage is 2V.
3. Check whether PQ103 PQ101 or bad.
4. Measured with a Multimeter or 5VPCU 3VPCU ground impedance, small or short-circuit impedance for RMA board, the general line of parts for the burn. (PU10, PQ101, PQ103, PQ104, PQ102, PQ105, U23, etc.).

Signal description

The IC is a voltage generated 2.5VSUS and 1.5V_S5 two groups, in 19VIN added after S5_ON, SUSON under normal circumstances, the two signals, that can generate the two voltages.

Main fault: 2.5VSUS or 1.5V_S5 output bad (not voltage output and low).

1. VIN_1845 input 19V voltage problems.
2. Open bad.
3. S5_ON, SUSON poor or no signals sent 1845IC.
4. 2.5 VSUS and 1.5V_S5 two smaller voltage-to-ground impedance or short circuit, for the RMA board, the general line of parts for the burn (PU5, PQ82, PQ99, PQ83, PQ106, PQ87, U16)

Signal description!

is the speed of the IC chip power management control, supply CPU CORE voltage, can automatically correct the offset, $\pm 0.75\%$ output voltage accuracy, a 0.700V-1.708V to voltage output range, 2V-28V power supply input voltage range and output over-voltage protection function.

Main fault: Insert **Shenyang Rittal Cabinets** CPU no voltage output.

1. VIN19V no input, PL12, PL18 bad.
2. PQ107, PQ108, PQ109, PQ110 bad.
3. 5 VPCU not enter into MAX1907IC the 30PIN.
4. Control signal VRON, STP-CPU, DPRSLPVR, PWROK problems.
5. CPU_VID0-5 signal not sent to the MAX1907.
6. MAX1907
7. Peripheral resistance, capacitance, diode and circuit problem.

Corresponding voltage generated the following way:

1. 5 VSUS issued by PC97551 SUSD signal to control PQ105 (4812IC), from the conversion over from 5VPCU

2. +5 issued by PC97551 MAIND signal to control PQ105 (4812IC), conversion from 5VPCU over the.
3. 3 VSUS: PC97551 issued by SUSD signal to control PQ102 (4812IC), conversion from 3VPCU them there.
4. +3 V: issued by PC97551 MAIND signal to control PQ102 (4812IC), conversion from 3VPCU them there.
5. +1.5 issued by PC97551 MAIND signal to control the PQ87 (4800IC), conversion from 1.5V_S5 them there.
6. 1.2 V: is the +5 V through PQ113, PQ112, PU6B and 1845REF2V signal to control the PQ89 (4800), from 1.5V_S5 convert them there.
7. VCCP is VRON by PQ91, PQ90, PU6A and 1845REF2V signal to control the PQ88 (4800), from 1.5V_S5 convert them there.

SMDDR_VTERM (1.25V issued by PC97551 MAIND signal to control PU7 (LP2996IC), conversion from 2.5VSUS them there.
from the 97,551 issued S5_ON signals PQ73-PQ70-PQ70 parts produced S5_OND signal to control PQ100 the first 3 PIN, from 3VPCU conversion over the.

One main voltage: 19VIN: the total power input.
5VPCU: MAX1999IC generated.
3VPCU: MAX1999IC generated. Generated.
1.5V_S5: MAX1845IC generated.
CPU CORE: MAX1907IC generated.

Some of the main power is not the point of failure:

1. 0.001 A current fixed: generally 3VPCU, 5VPCU, 19VIN problems.

A current fixed: 3VPCU, 5VPCU, 19VPCU normal, 2.5VSUS, 1.5V_S5, +5 V, +3 V, 1.5V, 1.2V, 1.05V whether short circuit.

General short-circuit condition: 5VPCU ground short circuit, MOSFE tube, MAX1999
3VPCU ground short circuit, MOSFE tube, MAX1999, 97551 chips.

First horse on the ground a short **chassis** Road, South Bridge bad.

- To ground short circuit, Northbridge bad
A current fixed: 3VPCU, 5VPCU, 19VPCU normal, generally bad for the BIOS, 97551, South Bridge.

4, a plug power supply, current has been increased from 0.002A to zero a few amps, usually 97551 chip burned. (97 551 poor, the temperature is high, hope the maintenance of attention, to avoid burns).

high-current, generally short, carefully measuring the voltage of each group on the ground impedance, replacement parts excluded failure.

POST self maintenance: self-test process

POST self-test code table:

- A system does not boot: DEBUG CARD run 00 of the state.
 1. the first of each group should measure the voltage supply is
 2. and then check whether the circuit and chip fat, warm, odor and other anomalies, timely treatment.
 3. E clock IC clock signal is sent to the pin on each chip.
 4. ensure the chip RESET signal is sent or received.
 5. Load the BIOS.
 6. the main signal for the
 - 1). with empty CPU socket board installed in the machine, check the CPU to the Northbridge Block signal impedance:
- # 3-31 address signal, HD # 0-63 data signals, ADS address status, and control signals, determine whether the CPU and North Bridge air welding, poor
- 2). North Bridge main signal check: HL0-10 South Bridge HUB bus interface connectivity.
- South Bridge, the main signal checking: AD0-31 composite address data signal line, C/BE0-3 bytes to allow the signal line, the control signal line, LAD0 -3 + LDRQ0 + LFRAME # even the **case in which the hard disk access 97,551 chips in the LPC bus interface.**
 - 4). MINI PCI slot on the PCI bus can be measured to check the appropriate bus plug-in circuit.
 - 5). 97 551 chip, the signal inspection: LAD0-3 + LDRQ0 + LFRAME # signal.
 - 6). BIOS checks on the signal: A0-19 address lines, D0-7 data lines, CS # chip select signals, RD # read the signal, WR # write signal and power ground.
 - 7). Try to make it clear fault region, to facilitate maintenance.If the above does not find problems, from the perspective of poor parts replacement parts to repair.

Memory does not boot: DEBUG CARD running 28, 38 and so on.

1. Mainly the memory part.

2. BIOS can also cause bad run of 38.
3. The memory part of the main North Bridge Control: R_MD0-63, R_MA0-12, R_SM_DQS0-8, SM_B1-5, SM_CS0-3, M_DM0-8, CKE0-3, CLK_SDRAM0-4 and other signals.
4. In the inspection process must be carefully measured: North Bridge - exclusive group - the memory slot of the signal, open circuit, short circuit and other undesirable phenomena.
5. Check SMDDR_VREF reference voltage is normal.
6. Northbridge, memory slots: empty and bad welding, welding or replacement material.

- Shown: DEBUG CARD running 59, 69 and so on.

1. Northbridge peripheral circuits for voltage
 2. Northbridge bad.
 3. Clock parts and clock IC bad.
 4. U15, CH7015IC bad.
- FUNTION poor maintenance of the
1. Battery charge and discharge bad: PQ45, PQ44, PQ42 poor more.
 2. 5 IN 1CARD bad: bad need of replacement slot; slot in the foot air welding; lines and for the voltage problems; PCI7411 chip air welding and bad need of replacement.
 3. Bad: Interface bad need of replacement; 1394 24.576 MHZ clock is **the official website** from the **first horse chassis** vibration; PCI7411 chip problem.
 4. CARDBUS bad: Interface problems; PCI7411 chip problem.
 5. USB bad: Line Interface problems; Southbridge bad.
 6. LAN bad: Interface loose dirt poor replacement; U18IC impedance bad; clock could not afford to vibration; chips RTL8100 bad; around bad filter capacitor leakage.
 7. MODEN and sound bad: MU2 chip bad; power supply; clock; amplifier and line. MU1 and peripheral circuits.
 8. HDD bad: Interface circuit; Southbridge bad.
 9. CD-ROM bad: Interface circuit; Southbridge bad.
 10. KEYBOARD bad: bad interface circuit; Pai Yung CP1-6 poor; 97551 chip, bad; BIOS program problems, need to replace the BIOS. 4
 11. TOUCH PAD bad: bad interface circuit; 97551 chip bad.
 12. FAN bad: Interface, Q11, Q12, and the 97551 chip bad.

OTHER NOTES FOR IMPORTANT

Power management chips and BIOS chips, where 3.3VPCU, VC CRT C where normal electricity supply, will enter the working state. One-chip power management system can be understood as moments in the work of the monitoring status. Connected to the power management chip clock oscillator Y6 external power management chip to monitor the line to provide the basis 32.768kHz clock signal. If you do not have this clock signal, the power management chip will also be in a "paralyzed" state. -

Power Management IC 2 feet for the start signal to detect motion foot NBSWON #. Under normal circumstances, when the pin is detected over a negative pulse signal, the chip that was press the power button on the boot, and immediately turn signal through the first 4PIN of DNBSWON # "reported to the South Bridge chips."

South Bridge chip part of the line is always in working condition. Likewise, it is also connected to a 32.768kHz external when Zhong Jingzhen Y5, its role is to South Bridge chip modules RTC and basic detection module reference clock.

Southbridge chip power management chip receiving the boot action to issue a pulse signal, this chip will be the first 26PIN the S USB #, the first 69PIN high of SUSC # set to an invalid state, the power management chip, boot up action to provide necessary conditions.

Parts.

Power management chip in the receiver to the South Bridge chip SUSB #, SUSC # control signal "Reply" In the future, it began to issue secondary power control signal (S5-ON, SUSON , MAINON, VRON) to each computer motherboard chip supply voltage generated. 3 N3 j8 H1 z I1 Z

DC / DC power supply generating circuit will have all the appropriate supply voltage to achieve stability in their output will be issued PWRGD high effective signal back to the power management chip, meaning that tell it, had now been given the task of successfully completed. Next, the power management chip control chip can be reported to the superior work. 4 Z5 c-u \$ d5 @.] - G1 D

When the power management chip to the PWRGD signal received after certain Delay period, to again PWROK signal to the corresponding delay circuit. Delay circuits at different delay, the order issued by the appropriate power supply OK signal. One, SB-PWROK signal to the South Bridge chip, NB-PWROK signal to

the North Bridge chip, CPU-PWROK signal to CPU. Next, the system chipset will issue a reset signal, first issued by the South Bridge PCI RST # signal to the PCI bus and other related equipment and the North Bridge chip. Meanwhile, the North Bridge chip in the receiver to the South Bridge chip issued PCIRST # reset signal, we will send CPURST # signal to the CPU.

Check sequence :;)

The first step, check whether the normal voltage VA, VA voltage is the voltage through PJ1 Power connector adapter input voltage. If the inductor PL17, PL18 and diode PD21, PD22 open the case there, VA voltage would not normally produce.

The second step, check the VIN voltage is normal, VIN voltage is the voltage from the VA conduction through the MOS conversion from the tube. (P-channel type MOS control provided that pin gate voltage only for the relatively low turn-on. N-channel type MOS tube, G is high voltage. DS conduction.)

The third step is to check 3.3/5VPCU voltage is normal. VIN voltage is generated 3.3/5VPCU basic premise of the system voltage. However, it only produced the two basic voltages necessary terms and conditions. To (MAX8734 check an example):

- (1) Check whether the MAX8734 20PIN 19V input.
- (2) Check whether the chip first 6PIN high. When the pin is low when. MAX8734

Will be shut down, stop working.

- (3) Check whether the chip 5V-AL 18PIN linear voltage is generated. Note that the Department of 5V-AL voltage does not mean 5VPCU voltage. As a linear voltage, its current output is very small. Only available in 3.3/5VPCU voltage generator start voltage before it. When 3.3/5VPCU voltage stability after, 5V-AL output pin voltage will be 5VPCU to take over and provide. If the PIN normal voltage output pin, then at least tell MAX8734 internal part of the line has already begun work. If not, the exclusion of other chip pin exceptional circumstances, consider replacing MAX8734 power chips.

- (4) Check the chip section 3, 4PIN the ON3, ON5 it is high. The role of these two pins is open 3.3VPCU and 5VPCU voltage. If the two pins are low here, that certainly would not have 3.3/5VPCU voltage.

- (5) Check 3.3/5VPCU output voltage, short circuit to ground impedance of the existence of such anomalies. If the voltage output short circuit, MAX8734 will soon be in line to protect their own state, to stop the output voltage.

(6) Were examined on both sides of the MOS 3.3/5VPCU tube and connected to the control circuit is abnormal. We may control ON3 and ON5 pins were examined.

The first step: Check the South Bridge, power management and BIOS chips are all the normal power supply voltage.

Step Two: clock investigation; possibly through a direct oscilloscope measurements Zhong Jingzhen have generated clock waveform.

The third step, check the power management chip, the first 29PIN the ACIN input pin, the motherboard if the power supply situation in the adapter, this pin must be high.

The fourth step, observed pin BIOS chip waveform.

The fifth step, press the start button on the power board, measuring whether the power management chip first 2PIN high to low transition of the Movements.

The sixth step, power management chip to detect whether the first 4PIN instant boot button is pressed, a high to a low negative pulse transition. If not, it indicates the power management chip does not do it the right thing.

Seventh step, check SUSB # and S USC # pin is in high state, if one foot is in low state, is unable to achieve power management chip boot action

Step eight, with a Multimeter measuring the SUSON power management chip 149PIN low signal whether the high jump. This situation can be divided into two types: one is not any action; the other is a jump, but not high maintenance. A focused inspection input pin voltage, the signal is abnormal. The second case shows the power management chip to respond to the boot action, and began to "work up" but, unfortunately, the control module to a voltage generated a problem, can not properly generate the corresponding voltage and the voltage OK signal similar back to power management chip. Here 63PIN under normal circumstances should send a high signal to the power management chip.

Ninth step, which is part of the final step in the boot power, the ultimate PWROK signal. Power Management IC s 28PIN here we are looking for the pin.

Generally, if the pin to maintain high, it indicates the boot was successful, all the motherboard power supply module and voltage stability are maintained.

I / O chip boot sequence (income chinafix)

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1: IT8712: Press the switch trigger signal by the construction, through I / O chips PANSWH # GP43 (75 feet) functional pin sent to the I / O chip, through the I / O test chip of the trigger circuit, then by the I / O chips PWRON # GP44 (72 feet) features a control signal output pin to South Bridge chips PWRBTN function pins, the last South Bridge chips, SLP-S3 features pin outputs a "SLP-S3" control signal to the I / O chip PSIN/GP45 function pin (71 feet), from I / O chip PSON # GP42 (76 feet) feature low output signal pin, the ATX 14 pin power supply Standby is a high level into the low to achieve the boot operation.

2: IT8712GB: Works by several signals that foot work, but to note that the IT8712 and IT8712GB pins is different, IT8712GB (PWRON # GP44 is 103 feet, PSON # GP42 is 107 feet, PANSWH # GP43 is 106 feet, PSIN/GP45 102 feet).

3: W83627: W83627HF 61 feet purple from the 5VSB standby voltage provided by the provision of I / O within the boot needed to trigger the power supply circuit. If point PWR switch, W83627HF get a 6-foot high, 67 feet by the South Bridge via the internal logic circuit sends a voltage of 3.3V to 0V transition, what the letter called PWR-BTN-SB # signal, Southbridge receive this signal to I / O chip 73 feet sending SLP-S3 # signal, I / O receive this signal, sent in a continuous 72-foot low, the green line voltage down to complete the boot

HP notebook power timing (for DV1000/DV2000/M2000/NX4800) - Part

When we plug in Adapter 19VIN When there is a power flow 5 VPCU, 3VPCU Voltage, it is PU10 (MAX1999) automatically generated, then the machine is in standby mode.

When we press Power Button When NBSWON# Moment there is a low level, which gave low 97551, 97551 Received signal, resulting in signal DNBSWON#, DNBSWON Distributed to South Bridge, also issued S5-ON to 1845 Produce 1.5V_S5. S5-ON Enter

PQ128 after PQ132 Produce S5 – OND。 S5 – OND by PQ127 and PQ141 Were produced 5V_S5And3V_S5。 3V_S5, 5V_S5, 1.5V_S5

At this time electricity to the South Bridge. South Bridge receivedDNBSWON Low, it occurs SUSB#, SUSC# Sent to the two high 97551, 97551 ReceiveSUSB#, SUSC# Have resulted after Layer, MAINON#, VRON。 Layer Signals into SUSD Signal sent PQ143 , PQ145Tube will produce 3VSUS, 5VSUS, and Layer Sent MAX1845

Produce 2.5VSUS。 MAINON# after PU7 Produce SMDDR—VTERM. At the same time by PQ119 and PQ125 into MAIND Send PQ143 , PQ145, PQ148 , PQ153Produce+3 V , +5 V , +2.5 V + 1.5VVoltage .

VRON Given PU3 (MAX1907) , PU5 (1992e) Produce-CORE And VCCPVoltage .PU6 , PU4 Produce HWPG Signal to97551, NowPU3, PU5Also produce a different HWPG Signal feedback 97551. At this point the whole M/BHave been the main voltage OKVoltage feedback in each group returnedHWPGThe convergence of the signal for aHWPG

Equivalent “And” Relationships such as these, any group feedback HWPG Time for low 97551 Occur POWER OK Instructions , turn off the voltage , such as OK

Then HWPG Constant is high when 97551 Receive HWPG Resulting from PWROK Signal sent SB South Bridge and then by SB Southbridge producePCI RST #After U42 Produce PCIRST# Pass North Bridge . North Bridge before they produceCPURST#.

MAX1999 IC: Signals description

That IC Have 4.5VTo 24VThe input voltage range 1.5%Output voltage accuracy,3.3VAnd5 VTwo modules , with software control within the opening , closing fast power management system and over-voltage protection function .

[Main fault :3VPCU or 5VPCU Output bad (usually board plug19vin, There are two voltage output)

- 1, VIN_1999 Enter19VVoltage problems.
- 2, Testing of8Reference voltage pin2V。
- 3, Inspection PQ101OrPQ103 is bad .
- 4, Measured with a Multimeter 3VPCU Or 5VPCU Ground impedance , small or short-circuit impedance for RMA Board , the general line of parts for the burn . (PU10,PQ101,PQ103,PQ104,PQ102,PQ105,U23等) 。

MAX1845 IC: Signal description

That IC I s to produce 2.5VSUSAnd 1.5V_S5 Two sets of voltage , in19VINAdded afterS5_ON,SUSON Under normal circumstances the two signals , which can generate the

two voltages .

Main fault :2.5VSUSOr1.5V_S5Output bad (not voltage output and low) .

- 1, VIN_1845Enter19V Voltage problems.
- 2, PL17 , PL9Open bad .
- 3, S5_ON,SUSONPoor or no signal sent to1845IC。
- 4, 2.5VSUSAnd1.5V_S5Two voltage -to-ground resistance becomes smaller or short-circuits for RMA Board , the general line of components for the burn (PU5,PQ82,PQ99,PQ83,PQ106,PQ87,U16)

HP notebook power timing (for DV1000/DV2000/M2000/NX4800) - medium-length

MAX1907 IC: Signal description!

The IC chip high-speed power management control, supply CPU CORE voltage, can automatically correct the offset, $\pm 0.75\%$ output voltage accuracy, a 0.700V-1.708V output voltage range, 2V-28V power supply input voltage range and output over voltage protection function.

Major fault: no-voltage output plug CPU.

1. VIN19V no input, PL12, PL18 bad.
2. PQ107, PQ108, PQ109, PQ110 bad.
3. 5VPCU not enters into MAX1907 IC the 30PIN.
4. Control signal VRON, STP-CPU, DPRSLPVR, PWROK problems.
5. CPU_VID0-5 signal not sent to the MAX1907.
6. MAX1907 bad.
7. around the resistors, capacitors, diodes, and the line goes.

Following is the corresponding voltage generated by:

1. 5VSUS issued by PC97551 SUSD signal to control PQ105 (4812IC), from the conversion over from 5VPCU
2. + 5V: MAIND issued by PC97551 signal to control PQ105 (4812IC), conversion from 5VPCU them there.
3. 3VSUS: PC97551 issued by SUSD signal to control PQ102 (4812IC), conversion from 3VPCU them there.
4. + 3V: MAIND issued by PC97551 signal to control PQ102 (4812IC), conversion from 3VPCU them there.
5. + 1.5V: MAIND issued by PC97551 signal to control PQ87 (4800IC), conversion from 1.5V_S5 them there.

6. 1.2 V: is + 5V through PQ113, PQ112, PU6B and 1845REF2V signal to control the PQ89 (4800), from 1.5V_S5 convert them there.
 7. VCCP (1.05V 2.5A): is VRON by PQ91, PQ90, PU6A and 1845REF2V signal to control the PQ88 (4800), from 1.5V_S5 convert them there.
 8. SMDDR_VTERM (1.25V 2.4A): issued by PC97551 MAIND signal to control PU7 (LP2996IC), from 2.5VSUS conversion over the.
- 69,3 V_S5: S5_ON signals from the 97,551 issued by PQ73-PQ70-PQ70 parts produced S5_OND signal to control PQ100 first 3PIN, conversion from 3VPCU them there.

One main voltage: 19VIN: the total power input.

5VPCU: MAX1999 IC generated.

3VPCU: MAX1999 IC generated.

2.5VSUS: MAX1845 IC generated.

1.5V_S5: MAX1845 IC generated.

CPU CORE: MAX1907 IC generated.

Some of the main power is not the point of failure:

- 1, 0.001A current fixed: generally 3VPCU, 5VPCU, 19VIN problems.
- 2, 0.002A current fixed: 3VPCU, 5VPCU, 19VPCU normal, 2.5VSUS, 1.5V_S5, +5 V, +3 V, 1.5V, 1.2V, 1.05V for shorts.

General short-circuit conditions: 5VPCU ground short circuit, MOSFE tube, MAX1999 3VPCU ground short circuit, MOSFE tube, MAX1999, 97551 chips.

1. 5V_S5 ground short circuit, Southbridge bad.
2. 5VSUS ground short, North Bridge poor
3. 0.002A current fixed: 3VPCU, 5VPCU, 19VPCU normal, generally bad for the BIOS, 9 7551, South Bridge.
4. A plug power supply, current has been increased from 0.002A to zero a few amps, usually 97551 chip burned. (97 551 poor, only the temperature is high and hope maintenance attention to avoid burns).
5. high-current, generally short, carefully measuring the voltage of each group on the ground impedance, fault replacement parts excluded.

Timing Power- IBM T61

When 20V power inserted into the notebook interface, in turn will produce DOCK_PWR20, DOCK_PWR20_F, DCIN_AMP_20, VINT20 I am sure you will be wondering , are 20V voltage , why engage in such trouble , in fact, changed so many 20V voltage, their role in each group is different , which is used in part on the motherboard 20V voltage is not the same. DOCK_PWR20, DOCK_PWR20_F provide voltage to the external docking station , the back board on the charge voltage chips , also , DOCK_PWR20_F VREGIN20 will continue to produce a 20V voltage , VREGIN20 this voltage chip TB6251 TOSHIBA mainly to provide the operating voltage of the chip The chip 's main role is to generate control signals . The VINT20 the 20V voltage is to control or produce other voltage MOS chip to provide the operating voltage . Clearly, though both are 20V voltage , but have been split into two , and the role of the chips for different operating voltage .

DOCK_PWR20_F voltage is 20V voltage front-end , after it converted to TB6251 VREGIN20 provide voltage to work , produce VCC3SW and DCIN_DRV,-WRSHUTDOWN such as voltage and signal , VCC3SW to PMH-7 provides the operating voltage , TB6251 work will be issued DCIN_DRV ,-PWRSHUTDOWN two signals , generated two high , PWRSHUTDOWN with a group composed of a transistor circuit , resulting in a low turn-Q34, thus producing a high DCIN_AMP_20.DCIN_DRV Q36 to produce direct conduction VINT20.

T61 power supply voltage divided up into many groups , such as the M series of voltage , a series of voltage and B series of voltage between the layers are stacked into a mutually dependent .

First, the voltage M series is not after power broke in press the power button , it should have the following groups of voltage , that is,

VCC3M, VCC5M, VCC1R8M, VCC1R5M, VCC1R05M. When the PMH-7 work , it will produce M1_ON, through resistor R866 into ;

VCC5M_ON, through resistor R405 into VCC3M_ON, these two sets of control signals control the MAX1700 will have VCC3M and VCC5M; also produced .

M2_ON, through resistor R373 into VCC1R8M_ON, it will control the MAX8632 produces VCC1R8M, and produce APWRG. through the resistor R470 conversion

Into VCC1R5M_ON, it will control the MAX1540 generate VCC1R5M, through resistor R382 into VCC1R05M_ON, it will generate control BD3508

VCC1R05M, as chip BD3508 operating voltage is VCC5M and VCC1R5M, so VCC1R05M

generation than the other M series of voltage Cycles to chew . Only the M series of voltage are produced , the voltage on the motherboard is all ready, waiting for the press the power button .

When you press the start button, start button on the PWRSWITCH This signal is pulled down to produce a low trigger PMH-7, PMH-7 will be issued A1_ON signal , through resistor into VCC0R9A_ON, it will control the MAX8632 produces VCC0R9A, and issued APWRG, pMH-7 also issued B1_ON, through resistor R867 into B_ON, it will control the MAX1540 produces VCC1R05B, and issued two sets of signals VTT_PWRG and BPWRG . Chip ADP3207 receive signals from the two groups come B2_ON and VTT_PWRG conversion issued DPRSLPVR_IMVP VCORE_ON and South Bridge when , under normal circumstances will produce VCCCPUCORE voltage , that is, CPU supply voltage , and will send a signal to the South Bridge VR_PWRGD , Southbridge receive this series of PWRGD signal will produce CKPWRGD signal to the time Zhongjing Zhen , both the voltage and crystal , the system north and south bridge after another reset , the normal power .

VINT20 to some other voltage chips generated voltage , such as : MAX1700, MAX8632, MAX1540, ADP3207 , etc. . To provide the operating voltage VINT20 and PMH-7 provides a control signal , MAX1700 will have VCC3M and VCC5M voltage , MAX8632 will have VCC1R8M and VCC0R9A voltage .

MAX1700 to normal work, and requires the following conditions:

- 1 . Supply voltage must be satisfied that the VINT20 must be 20V and should be stable, can not appear or square wave voltage instability problems .
- 2 . Control signal VCC3M_ON, VCC5M_ON must be normal, must be if the 3V, can not or do not appear below 3V and other phenomena , or MAX1700 will not function properly.
- 3 . Some other signals, such as -PWRSHUTDOWN,-SHUTDOWN2 also normal , REF reference signal and can not be pulled down .

Has been highlighted , in this not to repeat , though a bit different, but the basic principle is the same .

ADP3207 produces the chip CPU voltage is provided for the CPU working voltage . To make it work properly , needs the following , conditions:

- 1 . Supply voltage must be satisfied that the VINT20 must be 20V and should be stable, can not appear or square wave voltage instability problems .
- 2 . Control signals DPRSLPVR_IMVP, VCORE_ON must be normal .
- 3 . some other signals, such as CPUSENSE_CSREF, CPUSENSE_CSCOMP also normal, not

normal, CPU voltage does not cause Stability, and even power-down , VID0-VID6 can not have short circuit between , REF reference signal and can not be pulled down.

INTERSOFT