QT8 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 7,8
DDRII-SODIMM2 PAGE 7,8
DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E
PCI-Express 16X

NORTH BRIDGE
RX781 / RS780MN
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

Side port
256mb RAM for UMA only
PAGE 8

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

ATI M82-S for Discrete only
64 Bit,DDR2*4
M82-SCE A11
PAGE 17,18,19 20,21,22

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

Cable Docking PAGE 37
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

X1 LAN
Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN)
PAGE 31,32

RJ45 PAGE 31

X1 Express Card (NEW CARD) PAGE 33

X3 Mini PCI-E Card (Wireless LAN/TV TUNNER) PAGE 36

ALINK X4

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

USB2.0
1,8,9 USB2.0 Ports X3 PAGE 30
5 Blueflame PAGE 30
2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30
3 Flash Media for UMA only RTS5158 PAGE 25
Touch Screen for Discrete only

SATA0,1 150MB
TWO SATA - HDD PAGE 33

SATA0 150MB
SATA - CD-ROM PAGE 33

SATA4 150MB
E-SATA PAGE 30

PCIE BUS
JMICRON JMD380 for Discrete only PAGE 27

Azalia
IDT 92HD71B7 PAGE 27

AUDIO Amplifier TPA6017A2 PAGE 28

IEEE1394 connect for Discrete only PAGE 26

Memory CardReader PAGE 25

SMBUS
LPC

Accelerometer LIS3LV02DL PAGE 28
Keyboard PAGE 34
Touch Pad PAGE 34
CIR (AUDIO CONN) PAGE 27
Capacitive Sense SW PAGE 34

ENE KBC
KB3926 Cx
PAGE 35

MDC CONN PAGE 29

Digital MIC PAGE 30
AUDIO CONN (Phone/ MIC) PAGE 27
Audio Conn PAGE 28

FAN PAGE 37
SPI PAGE 35

SYSTEM CHARGER(ISL6251A) PAGE 44
SYSTEM POWER ISL6236IRZA-T PAGE 38
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
VGACORE(1.1V~1.2V)Oz8118 PAGE 42
CPU CORE ISL6265A PAGE 40

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, February 19, 2008 Sheet 1 of 45

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653,R656,R612 STUFF	R653,R656,R612 NC	To M82-S 27Mhz - RX780 only

+1.2V L49 BLM18PG181SN1D(180,1.5A)_6 60 ohm, 0.5A
600 ohms@100Mhz
C523 10U/6.3V_8 C518 C496 C527 C521 C476 C515 0.1U/10V_4
+1.2V_CLKVDDIO

DCR: 0.5 ohm
600 ohms@100Mhz
+3V L51 BLM18PG181SN1D(180,1.5A)_6 +3V_CLKVDD 60 ohm, 0.5A
C541 10U/6.3V_8 C468 C473 C512 C522 C508 C500 C474 C471 C469 0.1U/10V_4

+3V_CLKVDD L42 BLM18PG181SN1D(180,1.5A)_6 +3V_CLK_VDDA
C464 10U/6.3V_8 C482 C470 0.1U/10V_4
Place very close to C/G

U10A
VDDA GNDA VDDREF GNDREF VDD48 VDDATIG VDDCPU VDDHTT VDDSB_SRC VDDSRC VDDSATA VDDDOT VDDCPU_IO VDDATIG_IO VDDSB_SRC_IO VDDSRC_IO1 VDDSRC_IO2
GND48 GNDATIG1 GNDDOT GNDCPU GNDHTT GNDSATA GNDSB_SRC GNDSRC1 GNDSRC2
X1 X2 PD# SMBCLK SMBDAT SB_SRC_SLOW#
CPUKG0T_LPRS CPUKG0C_LPRS ATIG0T_LPRS ATIG0C_LPRS ATIG1T_LPRS ATIG1C_LPRS ATIG2T_LPRS ATIG2C_LPRS SB_SRC0T_LPRS SB_SRC0C_LPRS SB_SRC1T_LPRS SB_SRC1C_LPRS SRC0T_LPRS SRC0C_LPRS SRC1T_LPRS SRC1C_LPRS SRC2T_LPRS SRC2C_LPRS SRC3T_LPRS SRC3C_LPRS SRC4T_LPRS SRC4C_LPRS SRC5T_LPRS SRC5C_LPRS SRC6T/SATAT_LPRS SRC6C/SATAC_LPRS SRC7T_LPRS/27Mhz_SS SRC7C_LPRS/27Mhz_NS HTT0T/66M_LPRS HTT0C/66M_LPRS 48MHz_0 48MHz_1 REF0/SEL_HTT66 REF1/SEL_SATA REF2/SEL_27 CLKREQ0# CLKREQ1# CLKREQ2# CLKREQ3# CLKREQ4#
SLG8SP626VTR

C466 33P/50V_4 CG_XIN Y2 14.318MHZ C465 33P/50V_4 CG_XOUT
CG_XIN CG_XOUT CLK_PD# PCLK_SMB PDAT_SMB
6,7,13,28,36 PCLK_SMB 6,7,13,28,36 PDAT_SMB
14 CHIPSET_PCIE_SLOW_SB# D17 *CH501H-40PT L-F SB_SRC_SLOW#

can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/S0 power level

when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

THERMAL GND
eGND73 eGND74 eGND75 eGND77 eGND76 eGND78
U10B SLG8SP626VTR

Place within 0.5" of CLKGEN
R196 *261_4
Del RP for TP on PV

RP43 CPUCLKP CPUCLKN
RP54 NBGFX_CLKP NBGFX_CLKN
RP53 EXT_GFX_CLKP EXT_GFX_CLKN
T196 T84
RP48 PCIE_MINI2_CLKP PCIE_MINI2_CLKN
RP55 CLK_PCIE_CARD CLK_PCIE_CARD#
Del RP52 for NBGPP CLK
T59 T62
RP51 PCIE_NEW_CLKP PCIE_NEW_CLKN
RP49 PCIE_MINI1_CLKP PCIE_MINI1_CLKN
RP47 SBLINK_CLKP SBLINK_CLKN
RP45 SBSRC_CLKP SBSRC_CLKN
RP44 PCIE_LAN_CLKP PCIE_LAN_CLKN
*0_4P2R_4

CPUCLKP 3 CPUCLKN 3
NBGFX_CLKP 10 NBGFX_CLKN 10 EXT_GFX_CLKP 17 EXT_GFX_CLKN 17
to NB for external Graphics reference clock
to M82-S -RX780 only
PCIE_MINI2_CLKP 36 PCIE_MINI2_CLKN 36 CLK_PCIE_CARD 26 CLK_PCIE_CARD# 26
to TV TUNER CARD
to PCIE-CARD READER
PCIE_NEW_CLKP 33 PCIE_NEW_CLKN 33 PCIE_MINI1_CLKP 36 PCIE_MINI1_CLKN 36 SBLINK_CLKP 10 SBLINK_CLKN 10 SBSRC_CLKP 12 SBSRC_CLKN 12 PCIE_LAN_CLKP 31 PCIE_LAN_CLKN 31
to EPRESS CARD
to WLAN
to NB for AC-LINK reference clock
to SB
to PCIE-LAN
SI-1 Modified --remove to ROBSON

NBGPP_CLKN_R NBGPP_CLKN_L
CLK_VGA_27M_SS CLK_VGA_27M_NSS
R527 33_4 R415 75/F_4 R490 100/F_4 OSC_SPREAD
OSC_SPREAD 18 EVGA-XTALI 18
SSIN - for M82 - 3.3V level input
X_TALIN --for M82 -1.8V level input

NBHTREFCLK0P NBHTREFCLK0N CLK_48M_CR_L CLK48MUSB
R193 0_4 R194 0_4 R201 33_4 R192 33_4
NBHT_REFCLKP NBHT_REFCLKN CLK_48M_CR CLK_48M_USB
NBHT_REFCLKP 10 NBHT_REFCLKN 10 CLK_48M_CR 25 CLK_48M_USB 13
SEL_HT66 SEL_SATA SEL_27
T58 T167
CLKREQ0# EXT_NWD_CLK_REQ# CLKREQ2# CLKREQ3# CLKREQ4#
EXT_NWD_CLK_REQ# 33

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

R186 Ra 158/F_4
R184 1 2 90.9/F_4 Rb
EXT_NB_OSC 10

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

C952 C953 C954 C955 C956 *10P/50V_4
EXT_NB_OSC CLK_48M_USB CLK_48M_CR EVGA-XTALI OSC_SPREAD
SI-1 modified -- reserve for EMT

+3V
R756 R757 R758 R759 *8.2K_4
CLKREQ0# CLKREQ2# CLKREQ3# CLKREQ4#
if use clock request pin , need to pull Hi for default sttting

ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

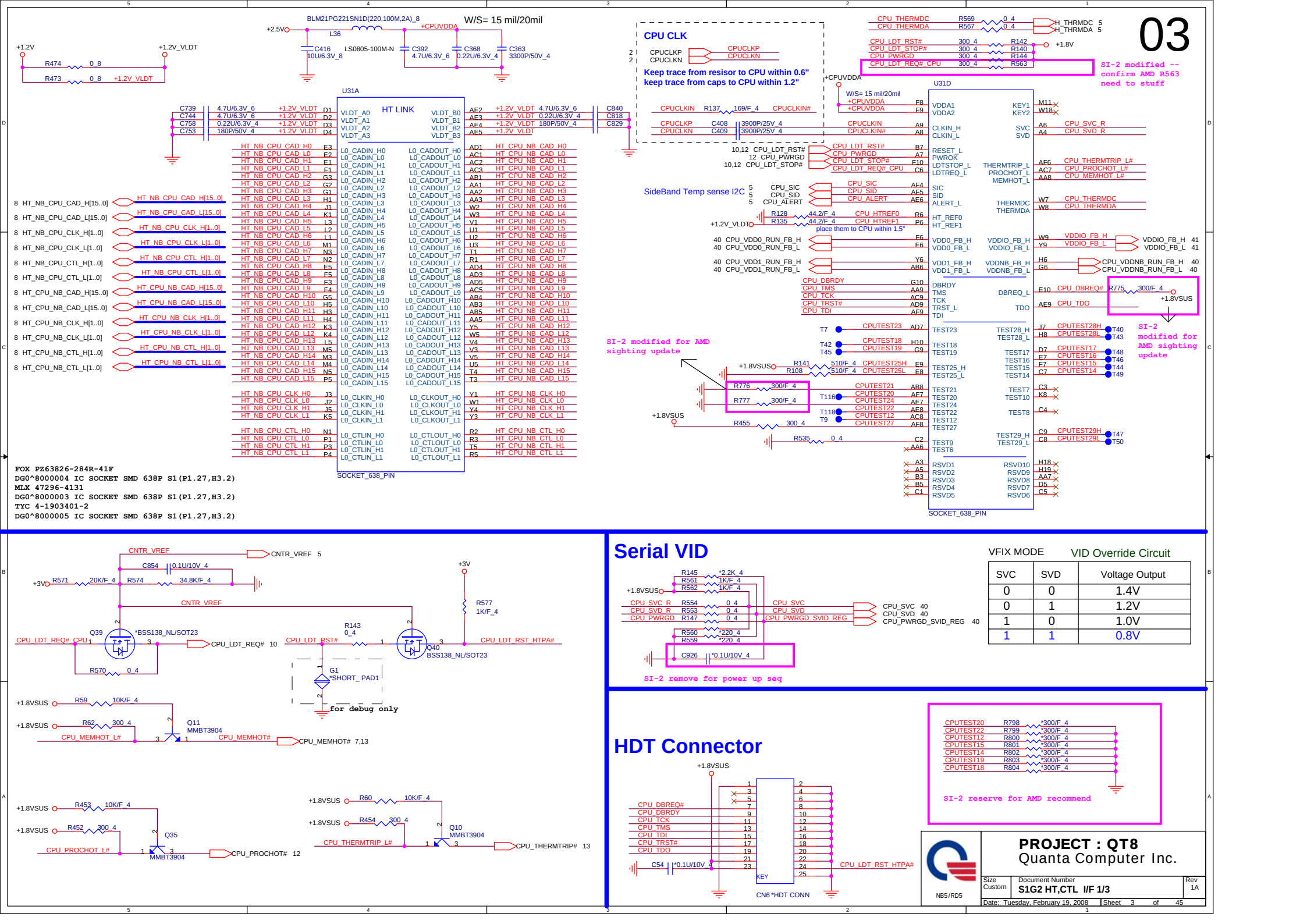
+3V_CLKVDD
R189 *8.2K_4 R195 8.2K_4
SEL_27 SEL_SATA SEL_HT66
R203 8.2K_4 R202 *8.2K_4
RS780M/RX780M

+3V
EXT_NWD_CLK_REQ# 8.2K_4 R219
CLK_PD# 8.2K_4 R204
SB_SRC_SLOW# 8.2K_4 R261

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A
Date: Tuesday, February 19, 2008	Sheet 2 of 45	


03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
SI-2 modified -- confirm AMD R563 need to stuff
U31A
HT LINK
SOCKET_638_PIN
U31D
SOCKET_638_PIN
SideBand Temp sense I2C
place them to CPU within 1.5"
SI-2 modified for AMD sighting update
SI-2 modified for AMD sighting update
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
Serial VID
SI-2 remove for power up seq
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
HDT Connector
SI-2 reserve for AMD recommend
CN6 *HDT CONN
for debug only
PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 1A
Date: Tuesday, February 19, 2008
Sheet 3 of 45

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

U31B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

750 mA

U31C

MEM:DATA

SOCKET_638_PIN

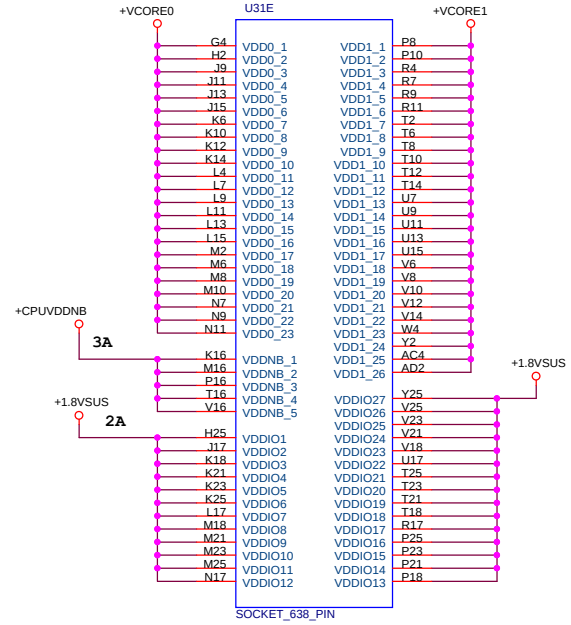
Place close to socket

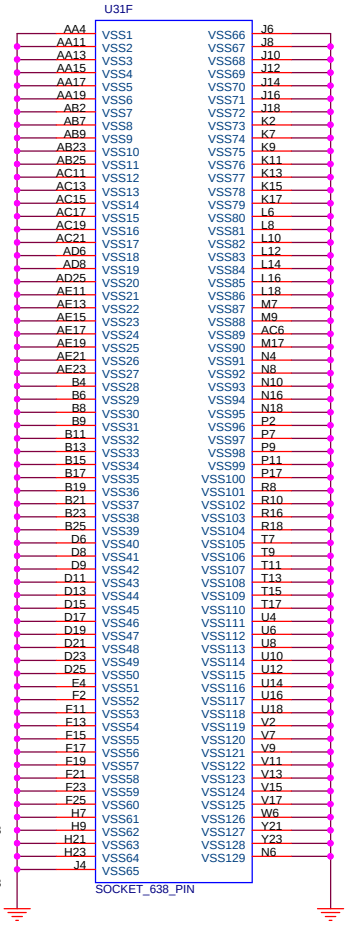
Close to CPU within 1500 mils

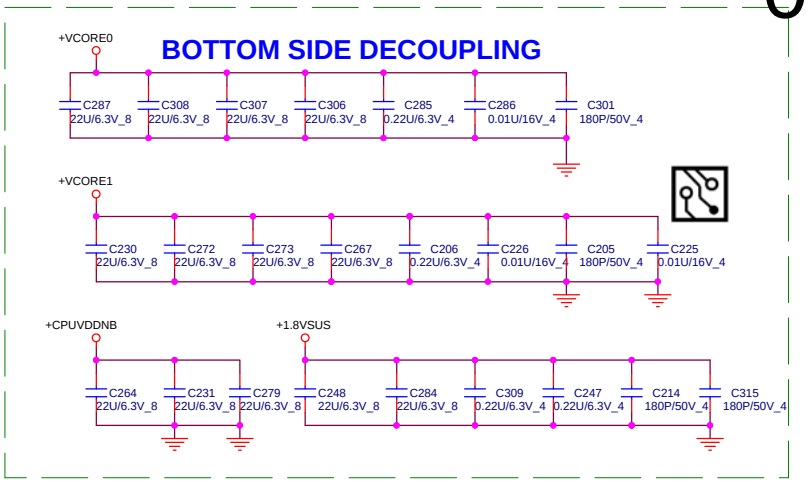
PROJECT :	QT8
Quanta Computer Inc.	
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 4 of 45

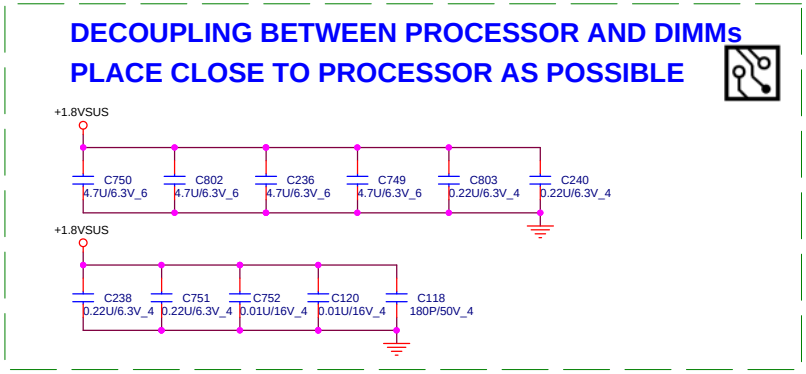
NB5/RD5

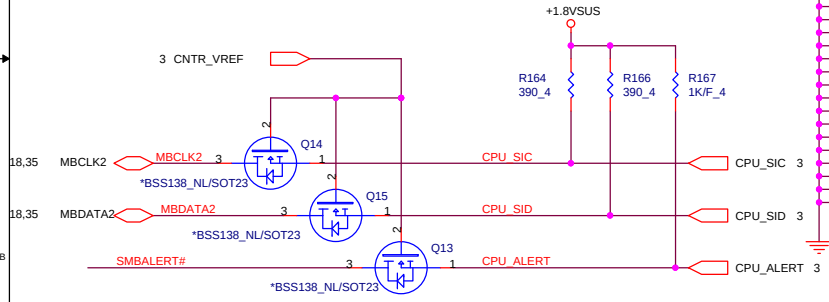
PROCESSOR POWER AND GROUND

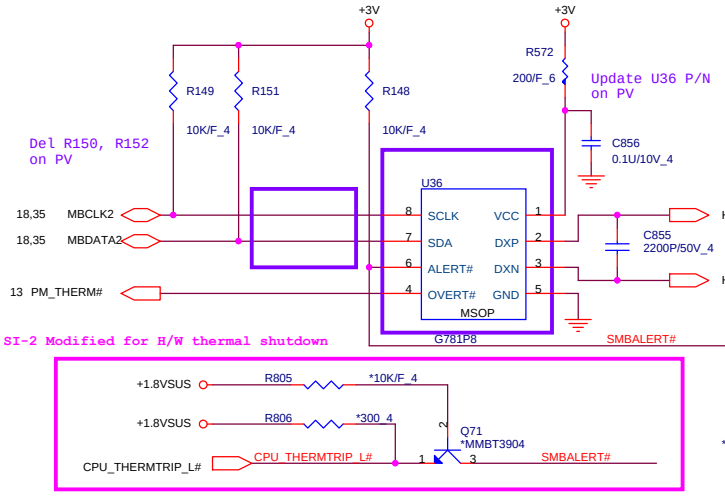


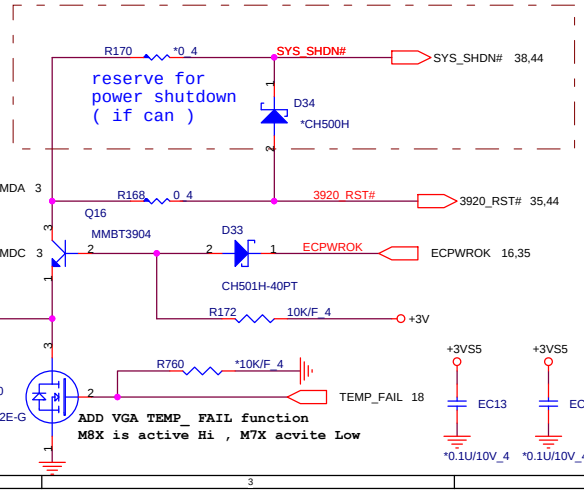


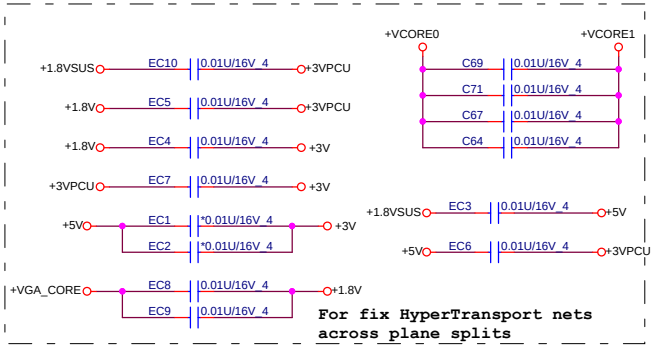


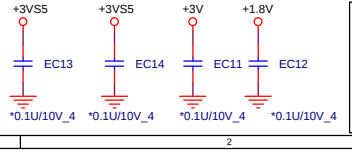




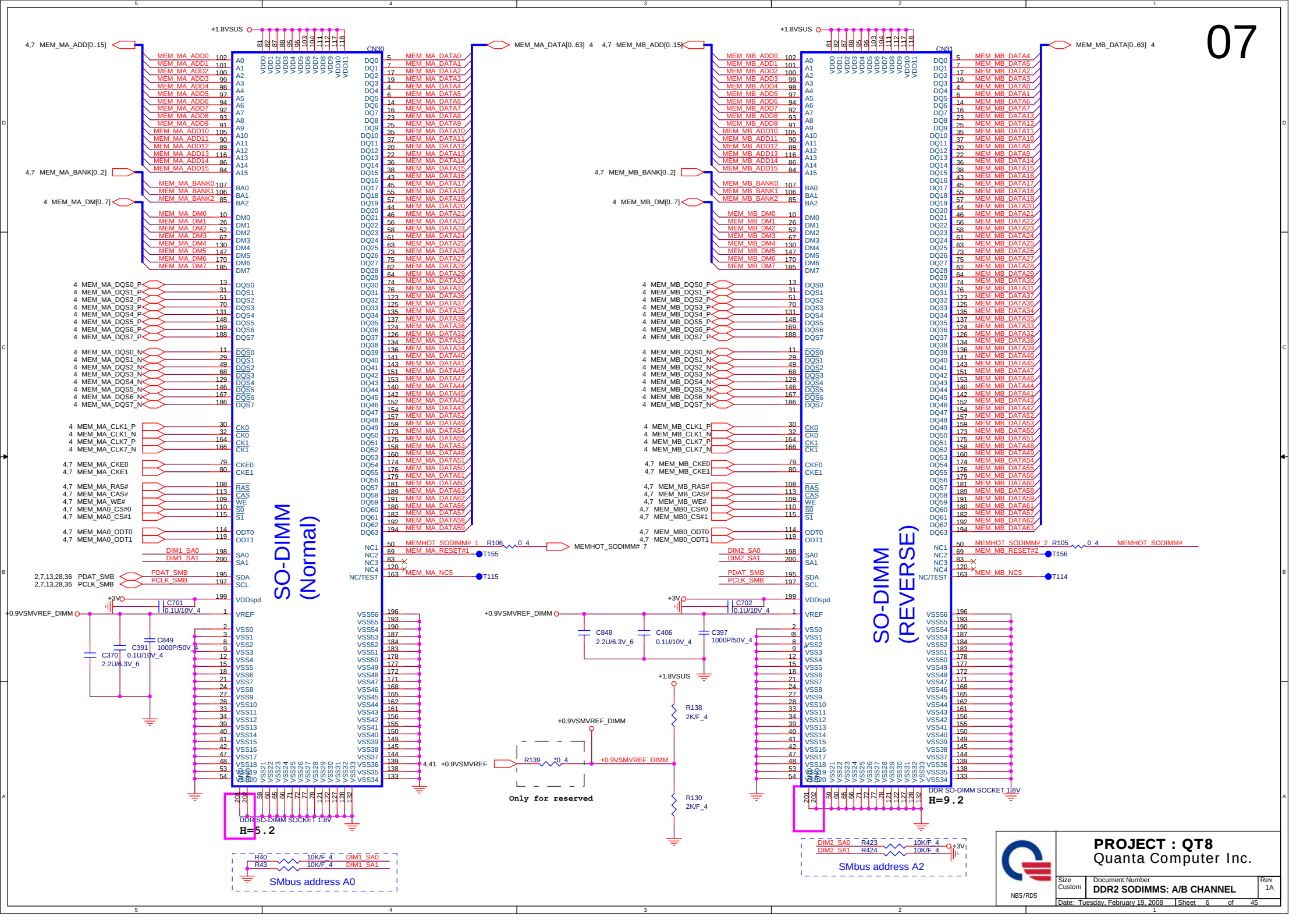






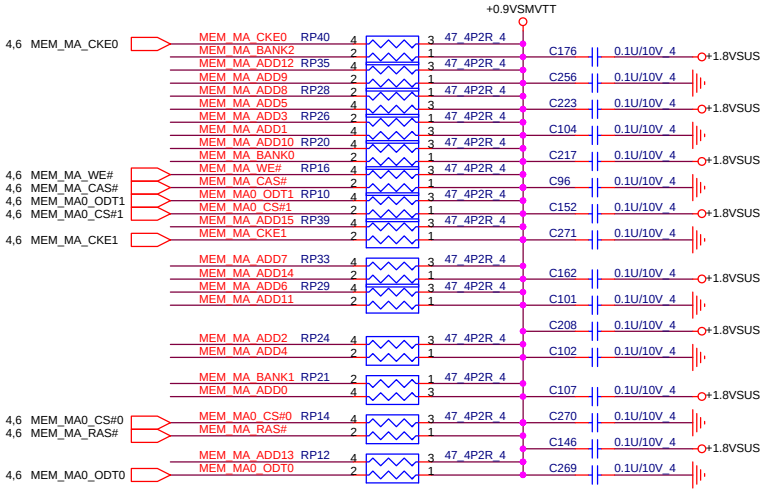


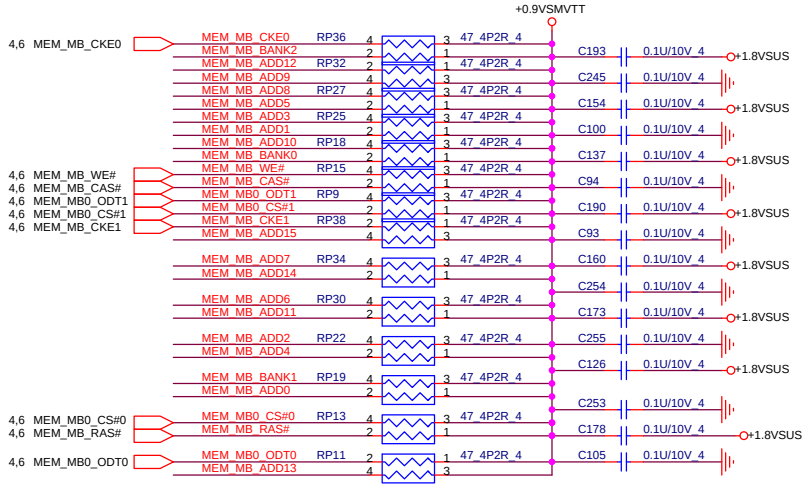
	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: **S1G2 PWR & GND 3/3**	Rev: 1A
NB5/RD5	Date: Tuesday, February 19, 2008	Sheet 5 of 45


07
SO-DIMM (Normal)
SO-DIMM (REVERSE)
CN30
CN31
+1.8VSUS
+3V
+0.9VSMVREF_DIMM
MEM_MA_ADD[0..15]
MEM_MA_BANK[0..2]
MEM_MA_DM[0..7]
MEM_MA_DATA[0..63]
MEM_MB_ADD[0..15]
MEM_MB_BANK[0..2]
MEM_MB_DM[0..7]
MEM_MB_DATA[0..63]
MEMHOT_SODIMM#
MEM_MA_RESET#1
MEM_MB_RESET#2
MEM_MA_NC5
MEM_MB_NC5
PDAT_SMB
PCLK_SMB
DDR SO-DIMM SOCKET 1.8V
H=5.2
H=9.2
Only for reserved
SMbus address A0
SMbus address A2
NB5/RD5
PROJECT : QT8
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Size Custom
Rev 1A
Date: Tuesday, February 19, 2008
Sheet 6 of 45

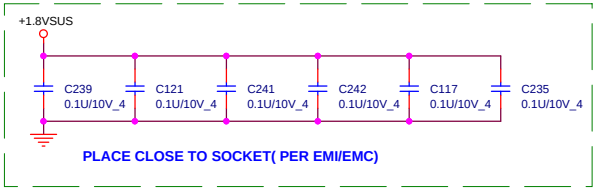
4,6 MEM_MA_ADD[0..15] — MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] — MEM_MA_BANK[0..2]

4,6 MEM_MB_ADD[0..15] — MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] — MEM_MB_BANK[0..2]





PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



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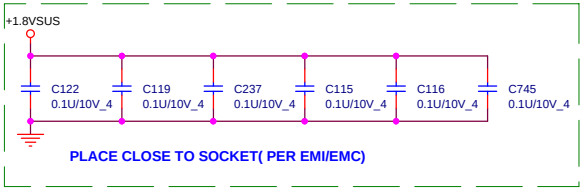
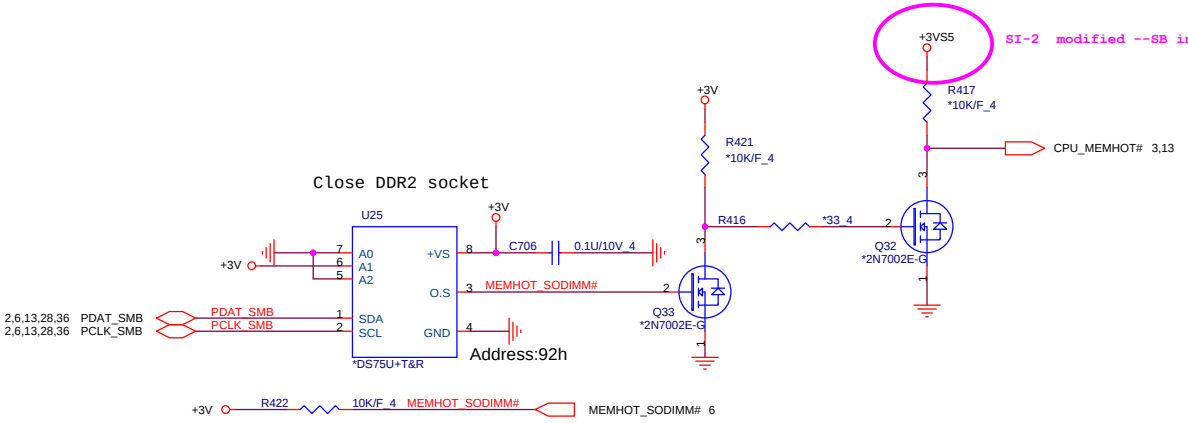




PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

NB5/RD5

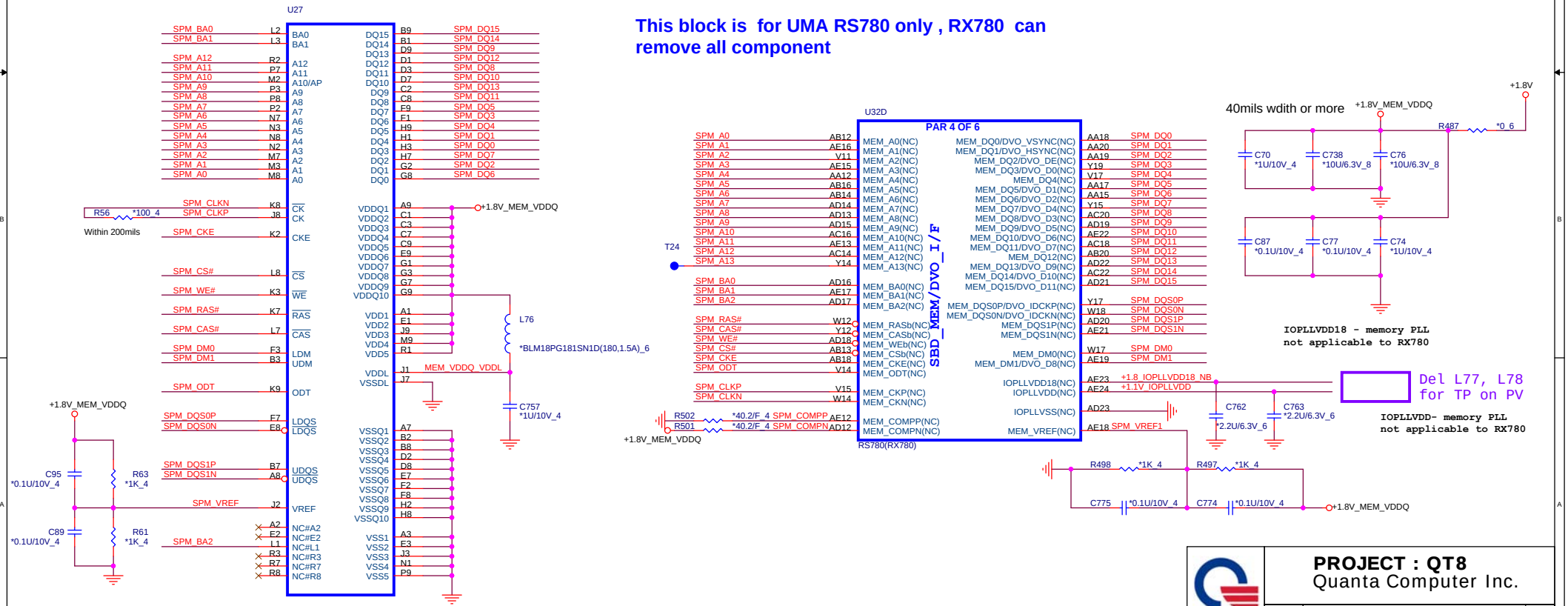
Date: Tuesday, February 19, 2008 | Sheet 7 of 45

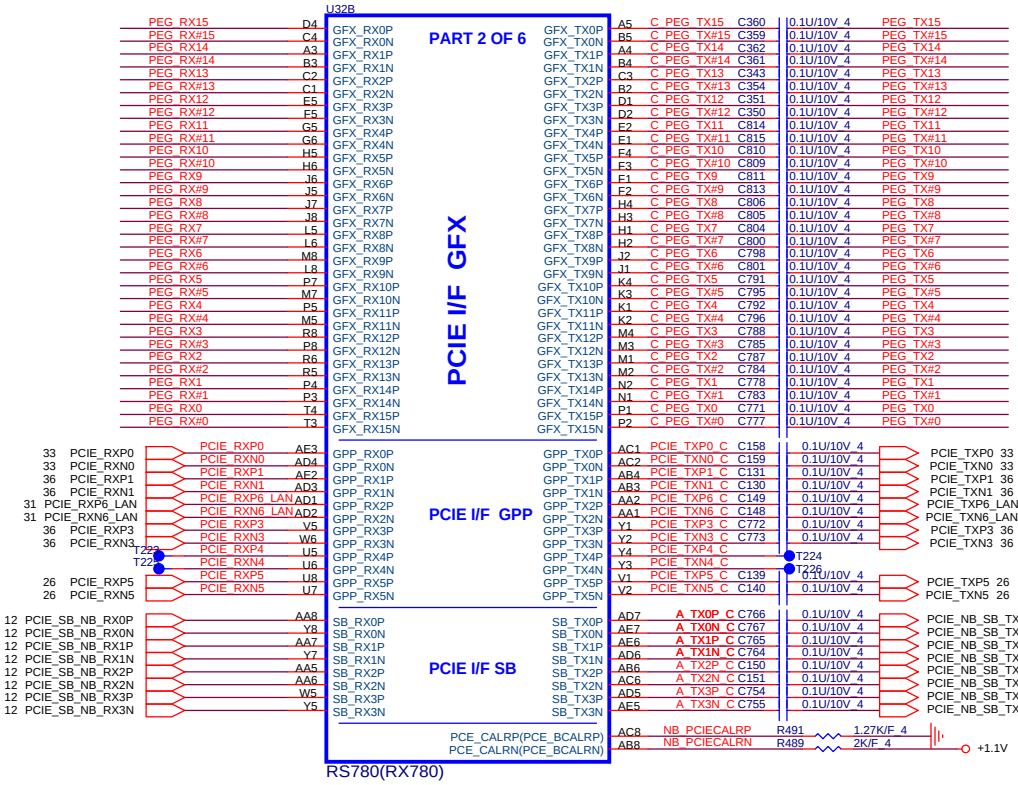
signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

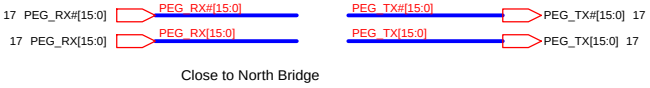
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

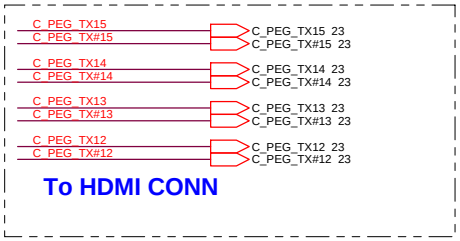
This block is for UMA RS780 only , RX780 can remove all component







Close to North Bridge



TO EPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

Date: Tuesday, February 19, 2008 | Sheet 9 of 45

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
3,12 CPU_LDT_RST# — R157 *0_4 — NB_RST# IN
RS780
12 NB_PLTRST# — R160 0_4
North Bridge RESET

R109 for UAM use 140 ohm

U32C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
18,24 CRT_R — R446 *0_4, R109 *150/F_4 — CRT_R_1 — G18
18,24 CRT_G — R445 0_4, R110 *150/F_4 — CRT_G_1 — G17, F18
18,24 CRT_B — R444 0_4, R111 *150/F_4 — CRT_B_1 — F18, F19
18,19,24 HSYNC_COM — R549 *0_4 — HSYNC_INT — A11
18,19,24 VSYNC_COM — R540 *0_4 — VSYNC_INT — B11
18,24 DDCDATA — R133 *0_4 — DDCDATA_INT — E8
18,24 DDCCLK — R134 *0_4 — DDCCLK_INT — F8
R119 *715/F_6 — DAC_RSET_NB — G14

PLL PWR LVTM
+1.1V_PLLVDD — A12
+1.8V_PLLVDD18 — D14, B12
+1.8V_VDDA18HTPLL — H17
+1.8V_VDDA18PCIEPLL — D7, E7

PM
16 NB_PWRGD_IN — NB_RST#_IN — D8
NB_PWRGD_IN — A10
NB_LDT_STOP# — C10
NB_ALLOW_LDTSTOP — C12

CLOCKS
2 NBHT_REFCLKP — NBHT_REFCLKP — C25
2 NBHT_REFCLKN — NBHT_REFCLKN — C24
2 EXT_NB_OSC — R117 0_4 — NB_REFCLK_P — E11
NB_REFCLK_N — F11
+1.1V — R125 4.7K_4, R520 RS780, R120 4.7K_4
Del NBGPP CLK
2 NBGFX_CLKP — NBGFX_CLKP — T2
2 NBGFX_CLKN — NBGFX_CLKN — T1
T168, T169
NBGPP_CLKP — U1
NBGPP_CLKN — U2
2 SBLINK_CLKP — SBLINK_CLKP — V4
2 SBLINK_CLKN — SBLINK_CLKN — V3
GFX_REFCLKP I/O
GFX_REFCLKN I/O
GPP_REFCLKP I/O
GPP_REFCLKN I/O
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)

MIS.
18,23 EDIDDATA — R547 *0_4 — NB_I2C_DATA — A9
18,23 EDIDCLK — R546 *0_4 — NB_I2C_CLK — B9
23 HDMI_DDC_DATA — R537 *0_4 — HDTV_DET — B8
23 HDMI_DDC_CLK — R544 *0_4 — RS740_DFT_GPIO0 — A8
RS740_DFT_GPIO1 — B7
T161, T158 — A7
39 DYN_PWR_EN — R27 0_4 — STRP_DATA — B10
G11
T164 — RS780_AUX_CAL — C8

RS780 only
+3V — R536 4.7K_4 — HDTV_DET
R539 4.7K_4 — NB_I2C_DATA
R538 4.7K_4 — NB_I2C_CLK

+3V_AVDD_NB — F12
+1.8V_AVDDDI_NB — F12, F14
+1.8V_AVDDQ_NB — G15, H15, H14
S-CD1 — F17, F15
C_Pr(DFT_GPIO5), Y(DFT_GPIO2), COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0), REDb(NC), GREEN(DFT_GPIO1), GREENb(NC), BLUE(DFT_GPIO3), BLUEb(NC)
DAC_HSYNC(PWM_GPIO4), DAC_VSYNC(PWM_GPIO6), DAC_SDA(PCE_TCALRN), DAC_SCL(PCE_RCALRN)
DAC_RSET(PWM_GPIO1)
PLLVDD(NC), PLLVDD18(NC), PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1, VDDA18PCIEPLL2
SYSRESETb, POWERGOOD, LDTSTOPb, ALLOW_LDTSTOP
HT_REFCLKP, HT_REFCLKN
REFCLK_P/OSCIN(OSCIN), REFCLK_N(PWM_GPIO3)
I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)

TXOUT_L0P(NC) A22 — LA_DATAP0 — LA_DATAP0 23
TXOUT_L0N(NC) B22 — LA_DATAN0 — LA_DATAN0 23
TXOUT_L1P(NC) A21 — LA_DATAP1 — LA_DATAP1 23
TXOUT_L1N(NC) B21 — LA_DATAN1 — LA_DATAN1 23
TXOUT_L2P(NC) B20 — LA_DATAP2 — LA_DATAP2 23
TXOUT_L2N(DBG_GPIO0) A20 — LA_DATAN2 — LA_DATAN2 23
TXOUT_L3P(NC) A19 — LA_DATAP3 — T159
TXOUT_L3N(DBG_GPIO2) B19 — LA_DATAN3 — T157
TXOUT_U0P(NC) B18 — LB_DATAP0 — LB_DATAP0 23
TXOUT_U0N(NC) A18 — LB_DATAN0 — LB_DATAN0 23
TXOUT_U1P(PCIE_RESET_GPIO3) A17 — LB_DATAP1 — LB_DATAP1 23
TXOUT_U1N(PCIE_RESET_GPIO2) B17 — LB_DATAN1 — LB_DATAN1 23
TXOUT_U2P(NC) D20 — LB_DATAP2 — LB_DATAP2 23
TXOUT_U2N(NC) D21 — LB_DATAN2 — LB_DATAN2 23
TXOUT_U3P(PCIE_RESET_GPIO5) D18 — LB_DATAP3 — T163
TXOUT_U3N(NC) D19 — LB_DATAN3 — T160
TXCLK_LP(DBG_GPIO1) B16 — LA_CLK — LA_CLK 23
TXCLK_LN(DBG_GPIO3) A16 — LA_CLK# — LA_CLK# 23
TXCLK_UP(PCIE_RESET_GPIO4) D16 — LB_CLK — LB_CLK 23
TXCLK_UN(PCIE_RESET_GPIO1) D17 — LB_CLK# — LB_CLK# 23
VDDLTP18(NC) A13 — +1.8V_VDDLTP18_NB — B13
VSSLTP18(NC)
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB — B15
VDDLT18_2(NC)
VDDLT33_1(NC) A14 — +3V_VDLT33_NB — B14
VDDLT33_2(NC)
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

RS780 only
LVDS_DIGON(PCE_TCALRP) E9 — R132 *0_4 — DISP_ON — DISP_ON 19,23
LVDS_BLON(PCE_RCALRP) E7 — R126 *0_4 — LVDS_BLON — LVDS_BLON 18,23
LVDS_ENA_BL(PWM_GPIO2) G12 — R118 *0_4 — DPST_PWM — DPST_PWM 19,23
R121 *1.27K/F_4
R127 *1.27K/F_4
For RX780 only

TMDS_HPD(NC) D9 — TMDS_HPD0 — R545 *0_4 — TMDS_HPD 18,23
HPD(NC) D10 — TMDS_HPD1 — T162
UMA only
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB — R131 0_4 — SUS_STAT# 13
THERMALDIODE_P AE8 — R_NB_THRMDA — T136
THERMALDIODE_N AD8 — R_NB_THRMDC — T135
TESTMODE D13 — TEST_EN — R541 1.82K/F_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
RX780: RS780_AUX_CAL — R543 3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780: VSYNC_COM — R124 3K_4 — +3V

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780: HSYNC_COM — R129 3K_4 — +3V, R136 *3K_4

For extrnal EEPROM Debug only
RS780/RX780: STRP_DATA — R548 10K/F_4 — +VDDG_NB, R558 *10K/F_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780
RX780: S-CD1 — R810 *3K_4
Reserved only

RX780 -->NC / RS780 --- ADD

AVDD-DAC Analog not applicable to RX780
+3V — L35 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB — C340 2.2U/6.3V_6

PLLVDD - Graphics PLL not applicable to RX780
+1.1V — BLM18PG181SN1D(180,1.5A)_6 — L82 — +1.1V_PLLVDD — C842 2.2U/6.3V_6

PLLVDD18 - Graphics PLL not applicable to RX780
+1.8V — L33 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18 — C405 10U/6.3V_8, C333 2.2U/6.3V_6

AVDDI-DAC Digital not applicable to RX780
+1.8V — R107 0_6 — +1.8V_AVDDDI_NB — C321 2.2U/6.3V_6

AVDDQ-DAC Bandgap Reference not applicable to RX780
BLM18PG181SN1D(180,1.5A)_6 — L34 — +1.8V_AVDDQ_NB — C349 2.2U/6.3V_6

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
+1.8V — BLM18PG181SN1D(180,1.5A)_6 — L83 — +1.8V_VDDLTP18_NB — C841 2.2U/6.3V_6

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
BLM21PG221SN1D(220,100M,2A)_8 — L85 — +1.8V_VDDLT_18_NB — C846 4.7U/6.3V_6, C838 0.1U/10V_4

VDDA18PCIEPLL -PCIE PLL
+1.8V — L32 BLM18PG181SN1D(180,1.5A)_6 — 20mils width — +1.8V_VDDA18PCIEPLL — C358 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L31 BLM18PG181SN1D(180,1.5A)_6 — 20mils width — +1.8V_VDDA18HTPLL — C356 2.2U/6.3V_6

RS780
Q37 BSS138_NL/SOT23
3,12 CPU_LDT_STOP# — R555 *0_4 — NB_LDT_STOP#
+1.8V — R556 4.7K_4 — +VDDG_NB
RX780

RS780
Q38 BSS138_NL/SOT23
3 CPU_LDT_REQ# — R568 0_4 — NB_ALLOW_LDTSTOP
12 ALLOW_LDTSTOP — R564 *0_4
+1.8V — R557 4.7K_4 — +VDDG_NB
RX780

RX780: R566 *0_6 — +1.8V — +VDDG_NB
RS780: R565 0_6 — +3V

VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only
+3V — L84 *BLM21PG221SN1D(220,100M,2A)_8 — +3V_VDLT33_NB — C844 *2.2U/6.3V_6

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A

Date: Tuesday, February 19, 2008 Sheet 10 of 45

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

PART 6/6 — GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

+1.1V 2A for RS780M

VDDHT - HT LINK digital I/O for RX780/RS780

0.6A — L72 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHT

C770 4.7U/6.3V_6, C274 0.1U/10V_4, C313 0.1U/10V_4, C280 0.1U/10V_4

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A — L81 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHTRX

C847 4.7U/6.3V_6, C323 0.1U/10V_4, C843 0.1U/10V_4, C839 0.1U/10V_4

+1.2V 2A for RS780M+SB700

+1.2V — L12 BLM21PG221SN1D(220,100M,2A)_8

+1.35V — L13 BLM21PG221SN1D(220,100M,2A)_8

0.5A — +1.2V_VDDHTTX

C124 4.7U/6.3V_6, C195 0.1U/10V_4, C194 0.1U/10V_4, C249 0.1U/10V_4, C199 0.1U/10V_4

+1.35V for A1-1 chip bug , A1-2 can remove

VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.8V 1A for RS780M+SB700

+1.8V — L22 BLM21PG221SN1D(220,100M,2A)_8 — 600mA — +1.8V_VDDA18PCIE

C188 4.7U/6.3V_6, C175 4.7U/6.3V_6, C258 0.1U/10V_4, C209 0.1U/10V_4, C302 0.1U/10V_4, C234 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V — R122 0_6 — 0.005A — C317 1U/10V_4 — +1.8V_VDDG18_NB

+1.8V — R499 0_6 — 0.005A — C769 1U/10V_4 — +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

U32E — PART 5/6 — POWER — RS780(RX780)

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC)

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC)

VDDG33_1(NC) VDDG33_2(NC)

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE — 0.7A — R542 0_8 — +1.1V

C275 0.1U/10V_4, C337 0.1U/10V_4, C318 1U/10V_4, C328 1U/10V_4, C845 4.7U/6.3V_6

7A — VDDC - Core Logic power — +1.1V_DYN

C251 0.1U/10V_4, C292 0.1U/10V_4, C297 0.1U/10V_4, C303 0.1U/10V_4, C59 10U/6.3V_8

C281 0.1U/10V_4, C278 0.1U/10V_4, C250 0.1U/10V_4, C60 10U/6.3V_8

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+1.8V_VDD_MEM — 1.8V(0.15A) — L23 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V

C192 0.1U/10V_4, C179 0.1U/10V_4, C172 0.1U/10V_4, C216 0.1U/10V_4, C153 4.7U/6.3V_6

+3V_VDDG33 — R123 RS780 0_6 — 3.3V(0.03A) — +3V

C336 0.1U/10V_4, C329 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

Date: Tuesday, February 19, 2008 | Sheet 11 of 45

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

SB700
Part 1 of 5
U37A

PCIE_PVDD-- PCIE PLL POWER

Del R639, R640, R641, R642 on PV

change D21, D20 type for PV

All the PCI bus has build-in Pull-UP/Down resistors

SI-2 mofified for satify -- remove R560 , add R796 ,R797

SI-2 Modified-- for power leakage issue

Del R783 for TP on PV

SI-2 Modified-- Add GPIO pin for control D3E wake up (need low 1ms for Jmicron request)

R589 change to 10 ohm on PV

If CPU have pull Hi ,this pin should be not need

PV-1 Modified -- change to pull hi to 3VS5 for power leakage issue

SI-1 Modified - for EMI

SI-2 modified -- for EMI suggestion

SI-2 Modified--reserve

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

PROJECT : QT8	
Quanta Computer Inc.	
Size: Custom	Document Number: SB700-PCIE/PCI/CPU/LPC 1/4
Rev: 1A	
NB5/RD5	
Date: Tuesday, February 19, 2008	Sheet 12 of 45

NC only ,Can't be install

+3VSUS
R297 *2.2K_4 SB_TEST0
R240 *2.2K_4 SB_TEST1
R287 *2.2K_4 SB_TEST2

+3VSUS
R289 *10K/F_4 SWI#

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R245 2.2K_4 PCLK_SMB
R253 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3VS5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R648 *2.2K_4 SB_SMBCLK1
R649 *2.2K_4 SB_SMBDATA1

remove pull hi (chip internal have pull hi)

+3VS5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R222 *2.2K_4 SB_SCLK2
R227 *2.2K_4 SB_SDATA2

+3V
R276 4.7K_4 SUS_STAT#
G4
2 1 SYS_RST#
*SHORT_ PAD1

+3VS5
R763 2.2K_4 DNBSWON#

U37D
SB700
Part 4 of 5

33 NEWCARD_DETECT
T211
T99
35 SUSB#
35 SUSC#
35 DNBSWON#
16 SB_PWRGD_IN
10 SUS_STAT#
R271 *0_4
R191 *0_4
R233 *0_4
NEWCARD_DETECT
RI#
SLP_S2
SUSB#
SUSC#
DNBSWON#
SB_PWRGD_IN
SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0

SI-2 modified add D3E function

35 GATEA20
35 RCIN#
35 SCI#
35 KBSMI#
T109
31,33,36 PCIE_WAKE#
35 SWI#
3 CPU_THERMTRIP#
16 WD_PWRGD
R211 *0_4
R786 0_4
GATEA20
RCIN#
SCI#
KBSMI#
GEVENT5#
SYS_RST#
PCIE_WAKE#
SWI#
SB_THERMTRIP#
WD_PWRGD

35 RSMRST#
R284 *0_4 RSMRST#

SI-2 modified -- Change lan disable control from SB to EC SB reserve

T63
T194
31,35 LAN_DISABLE#
R217 *0_4
T222
SATA_IS1
LAN_DISABLE# SB
SB_NWD_CLK_REQ#

27,28 ACZ_SPKR
2,6,7,28,36 PCLK_SMB
2,6,7,28,36 PDAT_SMB
R302 *0_4
ACZ_SPKR
PCLK_SMB
PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1

T69
T75
35 PM_BATLOW#
T72
26 D3E_SCI#
PM_BATLOW#
SES_INT

D3E_SCI# from Gevent5# change to Gevent7# on PV

SI-2 modified Del D35

3,7 CPU_MEMHOT#
5 PM_THERM#
+3VS5
R275 *0_4
R279 *10K/F_4
CPU_MEMHOT# IN
SMBALERT# 1
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_R
ACZ_SDIN1_R
T98
T209
16 ACZ_RST#
ACZ_SYNC
ACZ_RST#

HD audio interface is 3.385 voltage

+3VS5
R592 22K_4 HDD_AUX_RST#

SB700

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N

USB 1.1

USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB 2.0

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

CLK_48M_USB
USB_RCOMP_SB R267 11.8K/F_6
CLK_48M_USB 2
C554 *2.2P/50V_4

for EMI & del R268 change 2.2P

T101
T199
T91
T93

USBP11+ 36
USBP11- 36
TV Min-Card

USBP10+ 36
USBP10- 36
WLAN Min-Card

USBP9+ 30
USBP9- 30
USB Connector

USBP8+ 30
USBP8- 30
USB Connector

USBP7+ 33
USBP7- 33
NEW CARD

USBP6+ 30
USBP6- 30
FINGERPRINT

USBP5+ 30
USBP5- 30
BLUETOOTH

USBP4+ 37
USBP4- 37
Docking

USBP3+
USBP3-
USB card reader or Touch screen

USBP2+ 30
USBP2- 30
Carama USB

USBP1+ 30
USBP1- 30
E-SATA and USB Connector

USBP0+ 30
USBP0- 30
USB Connector

SB_SCLK2
SB_SDATA2
SB_SCLK3
T64
SB_SDATA3
T70
SB_GPIO16
SB_GPIO17
SB_GPIO16 16
SB_GPIO17 16
SPI/LPC define

+3VS5
R764 2K/04
+3V
33,36 SCLK_WLAN
PCLK_SMB
Q66
2N7002EPT

+3VS5
R765 2K/04
+3V
33,36 SDATA_WLAN
PDAT_SMB
2N7002EPT Q67

To Azalia

ACZ_SDOUT R644 33_4 ACZ_SDOUT_AUDIO 27
C908 *10P/50V_4

ACZ_SYNC R290 33_4 ACZ_SYNC_AUDIO 27
C569 *10P/50V_4

ACZ_BCLK R646 33_4 BIT_CLK_AUDIO 27
C910 10P/50V_4

ACZ_RST# R296 33_4 ACZ_RST#_AUDIO 27

ACZ_SDIN0_R R295 0_4 ACZ_SDIN0 27

SI-2 Modified --for EMI suggestion

To Modem Board

ACZ_SDOUT R645 33_4 ACZ_SDOUT_AUDIO_MDC 29
C909 *10P/50V_4

ACZ_SYNC R292 33_4 ACZ_SYNC_AUDIO_MDC 29
C577 *10P/50V_4

ACZ_BCLK R647 33_4 BIT_CLK_AUDIO_MDC 29
C911 10P/50V_4

ACZ_RST# R293 33_4 ACZ_RST#_AUDIO_MDC 29

ACZ_SDIN1_R R286 0_4 ACZ_SDIN1 29

SB JTAG

CN16
+3VSUS
C462 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

SI-2 Modified -- discrete remove RP56

CLOSE TO SB
USBP3-
USBP3+
RP50 *0_4P2R_4
USBP6_CR- 25
USBP6_CR+ 25
UMA

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Tuesday, February 19, 2008 Sheet 13 of 45

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

SATA PORT 4,5 are only support IDE mode

U37B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SATA PWR

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE :

R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Del R220 for TP on PV

Del WAN off# and R597 on PV

SI-2 modified -- SB internal pull Hi to 3VS5 , modified to same power rail with SB

SI-2 modified -- for fix +3V power leakage in S5 mode

AVDD--H/W monitor Analog power

SI-2 modified for SATA LED fail issue

Place near ball

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Tuesday, February 19, 2008 Sheet 14 of 45

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Del R285 for TP on PV

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

POWER

SB700 Part 3 of 5

VDDQ--3.3V I/O power — 0.8A

+3V → C576 100U/6.3V_3528 + C557 10U/6.3V_8 + C560 1U/10V_4 + C573 1U/10V_4 + C565 1U/10V_4 + C547 1U/10V_4 + C553 1U/10V_4 + C574 1U/10V_4

U37C VDDQ_1..12 (L9, M9, T15, U9, U16, U17, V8, W7, Y6, AA4, AB5, AB21) — PCI/GPIO I/O

VDD-- S/B CORE power

+1.2V_VCC_SB_R → R590 *0_8 → +1.2V_S5

CORE S0: VDD_1..9 (L15, M12, M14, N13, P12, P14, R11, R15, T16)

+1.2V_VCC_SB_R — 604mA: C533 1U/10V_4 + C545 1U/10V_4 + C538 1U/10V_4 + C532 1U/10V_4 + C467 10U/6.3V_8

R198 0_8 → +1.2V

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power — 0.45A

+3V → R226 0_8; +1.8V → R751 *0_8 → +VDD33_18

C486 10U/6.3V_8 + C501 1U/10V_4 + C487 1U/10V_4 + C497 1U/10V_4 + C488 1U/10V_4

Y20, AA21, AA22, AE25 (VDD33_18_1..4) — IDE/FLSH I/O

CKVDD_1.2V-- Internal clock Generator I/O power

+1.2V_CKVDD — 286mA

CLKGEN I/O: CKVDD_1.2V_1..4 (L21, L22, L24, L25)

C505 2.2U/6.3V_6 + C489 0.1U/50V_6 + C475 0.1U/50V_6 + C478 2.2U/6.3V_6

L43 BLM18PG181SN1D(180,1.5A)_6 → +1.2V

PCIE_VDDR--PCIE I/O power — 844mA

+1.2V_PCIE_VDDR → +1.2V → L89 BLM18PG181SN1D(180,1.5A)_6

C477 10U/6.3V_8 + C502 1U/10V_4 + C484 1U/10V_4 + C504 1U/10V_4 + C492 1U/10V_4 + C483 1U/10V_4

P18, P19, P20, P21, R22, R24, R25 (PCIE_VDDR_1..7) — A-LINK I/O

S5_3.3--3.3v standby power

+3VALW_R — 0.01A

3.3V_S5 I/O: S5_3.3V_1..7 (A17, A24, B17, J4, J5, L1, L2)

C875 0.1U/10V_4 + C570 0.1U/10V_4 + C876 10U/6.3V_8

R604 0_6 → +3VS5 (Change to 0603)

S5_1.2V--1.2V standby power

CORE S5: S5_1.2V_1..2 (G2, G4) — 0.22A → +1.2V_S5

C903 0.1U/10V_4 + C901 0.1U/10V_4

Del R661 for TP on PV

AVDD_SATA--SATA phy power — 0.2A

+1.2V_AVDD_SATA → +1.2V → L92 BLM18PG181SN1D(180,1.5A)_6

C888 10U/6.3V_8 + C880 0.1U/10V_4 + C884 0.1U/10V_4 + C883 1U/10V_4 + C881 1U/10V_4

AA14, AB18, AA15, AA17, AC18, AD17, AE17 (AVDD_SATA_1..7) — SATA I/O

USB_PHY_1.2V_1..2 (A10, B10) — 0.2A → +1.2V_USB_PHY_R

For support USB wakeup-->3V_S5
AVDDTX--USB Phy Analog I/O power — 0.2A

+3V_AVDD_USB → +3VS5 → L91 BLM18PG181SN1D(180,1.5A)_6

C889 10U/6.3V_8 + C882 10U/6.3V_8 + C878 0.1U/10V_4 + C886 0.1U/10V_4

C528 1U/10V_4 + C537 1U/10V_4 + C885 1U/10V_4 + C511 0.1U/10V_4 + C510 0.1U/10V_4 + C879 0.1U/10V_4 + C536 0.1U/10V_4

A16, B16, C16, D16, D17, E17, F15, F17, F18, G15, G17, G18 (AVDDTX_0..5, AVDDRX_0..5) — USB I/O

V5_VREF--PCI 5V TOLERANCE

V5_VREF: AE7 +5V_VREF — 4mA → R621 1K/F_4 → +5V

PLL: AVDDCK_3.3V J16 +3V_AVDDCK — 7mA; AVDDCK_1.2V K17 +1.2V_AVDDCK — 44mA; AVDDC F9 +3V_AVDDC — 16mA

C898 1U/10V_4

D36 CH501H-40PT → +3V

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R616 0_6 → +1.2V_USB_PHY_R

C890 0.1U/10V_4 + C891 0.1U/10V_4 + C892 10U/6.3V_8

AVDDC--USB Analog PLL power

+3VS5 → L50 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDC

C546 0.1U/10V_4 + C540 10U/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L45 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDDCK

C509 2.2U/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L48 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDCK

C516 2.2U/6.3V_6

U37E SB700 Part 5 of 5 — GROUND

AVSS_SATA_1..20 (T10, U10, U11, U12, V11, V14, W9, Y9, Y11, Y14, Y17, AA9, AB9, AB11, AB13, AB15, AB17, AC8, AD8, AE8)

AVSS_USB_1..24 (A15, B15, C14, D8, D9, D11, D13, D14, D15, E15, F12, F14, G9, H9, H17, J9, J11, J12, J14, J15, K10, K12, K14, K15)

PCIE_CK_VSS_1..8 (H18, J17, J22, K25, M16, M17, M21, P16)

AVSSC F9; AVSSCK L17

VSS_1..50 (A2, A25, B1, D7, F20, G19, H8, K9, K11, K16, L4, L7, L10, L11, L12, L14, L16, M6, M10, M11, M13, M15, N4, N12, N14, P6, P9, P10, P11, P13, P15, R1, R2, R4, R9, R10, R12, R14, T11, T12, T14, U4, U14, V6, Y21, AB1, AB19, AB25, AE1, AE24)

PCIE_CK_VSS_9..21 (P23, R16, R19, T17, U18, U20, V18, V20, V21, W19, W22, W24, W25)

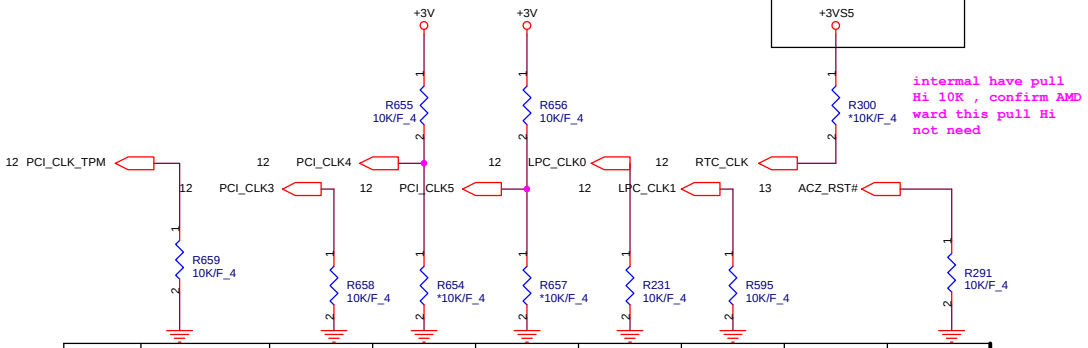
SB700

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.		
Size: Custom	Document Number: SB700-PWR/DECOUPLING 4/4		Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 15 of 45		

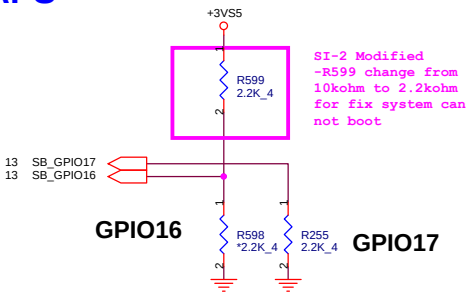
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



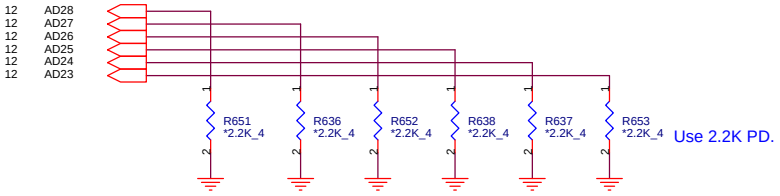
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

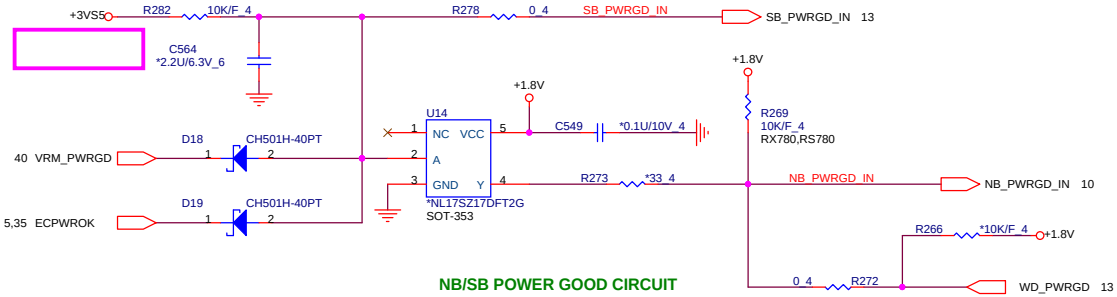


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove +3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

Date: Tuesday, February 19, 2008 Sheet 16 of 45

IC CTRL(632P) 216-0707001-00(BGA)
VGA P/N : AJ070700T00

2.5Gb/s bit rate

PART 1 OF 6

PCI-EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AC30	PCIE_RX0P	PCIE_TX0P	AA28	C_PEG_RXP0	C163	0.1U/10V_4	PEG_RX0	9
9	PEG_TX#0	PEG_TX#0	AC31	PCIE_RX0N	PCIE_TX0N	AA27	C_PEG_RXN0	C156	0.1U/10V_4	PEG_RX#0	9
9	PEG_TX1	PEG_TX1	AC29	PCIE_RX1P	PCIE_TX1P	AA25	C_PEG_RXP1	C167	0.1U/10V_4	PEG_RX1	9
9	PEG_TX#1	PEG_TX#1	AB29	PCIE_RX1N	PCIE_TX1N	AA24	C_PEG_RXN1	C170	0.1U/10V_4	PEG_RX#1	9
9	PEG_TX2	PEG_TX2	AB31	PCIE_RX2P	PCIE_TX2P	Y28	C_PEG_RXP2	C180	0.1U/10V_4	PEG_RX2	9
9	PEG_TX#2	PEG_TX#2	AB30	PCIE_RX2N	PCIE_TX2N	Y27	C_PEG_RXN2	C196	0.1U/10V_4	PEG_RX#2	9
9	PEG_TX3	PEG_TX3	AA31	PCIE_RX3P	PCIE_TX3P	Y25	C_PEG_RXP3	C164	0.1U/10V_4	PEG_RX3	9
9	PEG_TX#3	PEG_TX#3	AA30	PCIE_RX3N	PCIE_TX3N	Y24	C_PEG_RXN3	C157	0.1U/10V_4	PEG_RX#3	9
9	PEG_TX4	PEG_TX4	W30	PCIE_RX4P	PCIE_TX4P	V28	C_PEG_RXP4	C218	0.1U/10V_4	PEG_RX4	9
9	PEG_TX#4	PEG_TX#4	W31	PCIE_RX4N	PCIE_TX4N	V27	C_PEG_RXN4	C204	0.1U/10V_4	PEG_RX#4	9
9	PEG_TX5	PEG_TX5	W29	PCIE_RX5P	PCIE_TX5P	V25	C_PEG_RXP5	C203	0.1U/10V_4	PEG_RX5	9
9	PEG_TX#5	PEG_TX#5	V29	PCIE_RX5N	PCIE_TX5N	V24	C_PEG_RXN5	C187	0.1U/10V_4	PEG_RX#5	9
9	PEG_TX6	PEG_TX6	V31	PCIE_RX6P	PCIE_TX6P	T28	C_PEG_RXP6	C220	0.1U/10V_4	PEG_RX6	9
9	PEG_TX#6	PEG_TX#6	V30	PCIE_RX6N	PCIE_TX6N	T27	C_PEG_RXN6	C224	0.1U/10V_4	PEG_RX#6	9
9	PEG_TX7	PEG_TX7	U31	PCIE_RX7P	PCIE_TX7P	T25	C_PEG_RXP7	C243	0.1U/10V_4	PEG_RX7	9
9	PEG_TX#7	PEG_TX#7	U30	PCIE_RX7N	PCIE_TX7N	T24	C_PEG_RXN7	C252	0.1U/10V_4	PEG_RX#7	9
9	PEG_TX8	PEG_TX8	P30	PCIE_RX8P	PCIE_TX8P	P28	C_PEG_RXP8	C276	0.1U/10V_4	PEG_RX8	9
9	PEG_TX#8	PEG_TX#8	P31	PCIE_RX8N	PCIE_TX8N	P27	C_PEG_RXN8	C268	0.1U/10V_4	PEG_RX#8	9
9	PEG_TX9	PEG_TX9	P29	PCIE_RX9P	PCIE_TX9P	P25	C_PEG_RXP9	C259	0.1U/10V_4	PEG_RX9	9
9	PEG_TX#9	PEG_TX#9	N29	PCIE_RX9N	PCIE_TX9N	P24	C_PEG_RXN9	C246	0.1U/10V_4	PEG_RX#9	9
9	PEG_TX10	PEG_TX10	N31	PCIE_RX10P	PCIE_TX10P	M28	C_PEG_RXP10	C289	0.1U/10V_4	PEG_RX10	9
9	PEG_TX#10	PEG_TX#10	N30	PCIE_RX10N	PCIE_TX10N	M27	C_PEG_RXN10	C277	0.1U/10V_4	PEG_RX#10	9
9	PEG_TX11	PEG_TX11	M31	PCIE_RX11P	PCIE_TX11P	M25	C_PEG_RXP11	C290	0.1U/10V_4	PEG_RX11	9
9	PEG_TX#11	PEG_TX#11	M30	PCIE_RX11N	PCIE_TX11N	M24	C_PEG_RXN11	C296	0.1U/10V_4	PEG_RX#11	9
9	PEG_TX12	PEG_TX12	K30	PCIE_RX12P	PCIE_TX12P	L28	C_PEG_RXP12	C288	0.1U/10V_4	PEG_RX12	9
9	PEG_TX#12	PEG_TX#12	K31	PCIE_RX12N	PCIE_TX12N	L27	C_PEG_RXN12	C295	0.1U/10V_4	PEG_RX#12	9
9	PEG_TX13	PEG_TX13	K29	PCIE_RX13P	PCIE_TX13P	L25	C_PEG_RXP13	C330	0.1U/10V_4	PEG_RX13	9
9	PEG_TX#13	PEG_TX#13	J29	PCIE_RX13N	PCIE_TX13N	L24	C_PEG_RXN13	C324	0.1U/10V_4	PEG_RX#13	9
9	PEG_TX14	PEG_TX14	J31	PCIE_RX14P	PCIE_TX14P	J28	C_PEG_RXP14	C325	0.1U/10V_4	PEG_RX14	9
9	PEG_TX#14	PEG_TX#14	J30	PCIE_RX14N	PCIE_TX14N	J27	C_PEG_RXN14	C331	0.1U/10V_4	PEG_RX#14	9
9	PEG_TX15	PEG_TX15	H31	PCIE_RX15P	PCIE_TX15P	G28	C_PEG_RXP15	C304	0.1U/10V_4	PEG_RX15	9
9	PEG_TX#15	PEG_TX#15	H30	PCIE_RX15N	PCIE_TX15N	G27	C_PEG_RXN15	C316	0.1U/10V_4	PEG_RX#15	9

Clock

2	EXT_GFX_CLKP	EXT_GFX_CLKP	AD29	PCIE_REFCLKP
2	EXT_GFX_CLKN	EXT_GFX_CLKN	AD30	PCIE_REFCLKN

100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing

SM BUS

AC28	NC_SMBCLK	
AC27	NC_SMBDATA	

12	PCIE_RST#	R71 0_4	AG25	PERSTB

Calibration

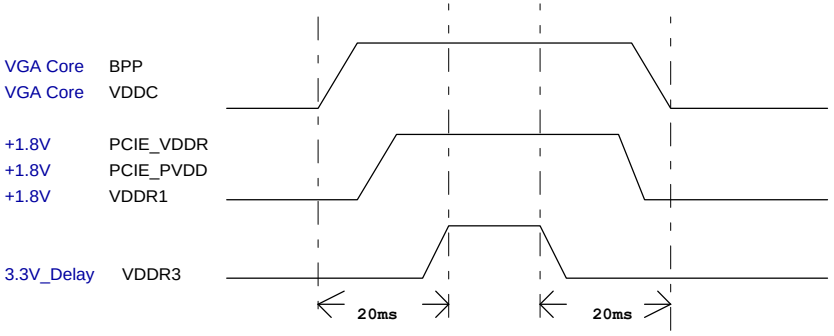
PCIE_CALRN	AF25	M72_PCIE_CALRN	R74	2K/F_4	+1.1V_PCIE_VDDC	
PCIE_CALRP	AE25	M72_PCIE_CALRP	R70	1.27K/F_4		

1.27K for M82-S

NC_1	AE23	
NC_2	AH30	

M72-S/M82-S
U29A

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_PCIE_Interface	1A

NB5/RD5

Date: Tuesday, February 19, 2008 | Sheet 17 of 45

R100 1K/F_4 GPIO_24_JMODE — NA- M62S,M71S PD 1K- M72S

R522 10K/F_4 ROMCS# — GPIO22(ROMCS#) PD without external VBIOS ROM

R87 10K/F_4 BBEN — NA - M64/M62, M71 BBEN- M66 BBEN(10K PD)- M76

R95 10K/F_4 TEMP_FAIL — NA- M62S,M71S PU to 3.3V- M72S

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161B2F-20
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16-500MHZ	H5PS5162FFR-20L
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-HC20
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

U29B PART 2 OF 6 — INTEGRATED TMDS/DP PORT

TXCM_DPA0P / TXCP_DPA0N — TXC_HDMI_L- / TXC_HDMI_L+ — TXC_HDMI_L- 23, TXC_HDMI_L+ 23

TX0M_DPA1P / TX0P_DPA1N — TX0_HDMI_L- / TX0_HDMI_L+ — TX0_HDMI_L- 23, TX0_HDMI_L+ 23

TX1M_DPA2P / TX1P_DPA2N — TX1_HDMI_L- / TX1_HDMI_L+ — TX1_HDMI_L- 23, TX1_HDMI_L+ 23

TX2M_DPA3P / TX2P_DPA3N — TX2_HDMI_L- / TX2_HDMI_L+ — TX2_HDMI_L- 23, TX2_HDMI_L+ 23

Remove 180R SHUNT RESISTOR for M82-S from AMD Jackson confirm

19 PSYNC — PSYNC — DVALID, PSYNC_NEW

DPA_PVDD / DPA_PVSS — +1.8V_TPVDD

DPB_PVDD / DPB_PVSS — DPB_PVDD

DPA_VDDR_1 / DPA_VDDR_2 — DPA_B_VDDR

DPB_VDDR_1 / DPB_VDDR_2 — DPA_B_VDDR

DPA_PVDD / DP_TMDS PLL Power (Link A) / DP/TMDS PLL Power (Link B) / 1.8 V ± 3%

DPA_VDDR / DPB_VDDR / DP/TMDS Transmitter Power (Link A) / DP/TMDS Transmitter Power (Link B) / 1.1 V ± 3%

ENABLE HD AUDIO (M8X-M)

R488 *0_4 — VIP_3 — VIP_3 19

M82-S — R476 0_4 150 OHM — DPA_VSSR_2

DP_CALR — TMDS_HPD — TMDS_HPD 10,23

HPD1 — TMDS_HPD

DVPDATA_0 … DVPDATA_23 — EXT TMDS DVO

R / RB — L_CRT_R — R465 *100K/F_4, R463 150/F_4, R449 0_4 — CRT_R 10,24

G / GB — L_CRT_G — R462 150/F_4, R448 0_4 — CRT_G 10,24

B / BB — L_CRT_B — R461 150/F_4, R447 0_4 — CRT_B 10,24

Del R481, R482, R483, R68, R464, R486 for TP on PV

DAC1 / CRT — HSYNC, VSYNC — HSYNC_COM 10,19,24 / VSYNC_COM 10,19,24

RSET — R484 499/F_4

AVDD — +1.8V_A2VDD_Q — C111 0.1U/10V_4

AVDD / DAC1 Analog Power / Dedicated power for DAC1. / 1.8 V ± 5%

AVSSQ

VDD1DI — +VDDD1 — C127 0.1U/10V_4

VDD1DI / DAC1 Digital Power. / 1.8 V ± 5%

VSS1DI

R2 / R2B, G2 / G2B, B2 / B2B — DAC2 (TV/CRT2)

Del R470, R478, R450, R472, R471, R469, R451 for TP on PV

A2VDD / DAC2 Analog Power. / 3.3 V ± 5%

A2VDDQ / DAC2 Band Gap (clean) power supply. / 1.8 V ± 5%

C — Y — COMP

VDD2DI / DAC2 Digital Power. / 1.8 V ± 5%

V2SYNC / H2SYNC — DAC2_VSY, DAC2_HSY — T13, T10

A2VDD

A2VDDQ — +1.8V_A2VDD_Q — C136 0.1U/10V_4 — +3V_DELAY

Del L25 for TP on PV

A2VSSQ

VDD2DI — +VDDD1 — C171 0.1U/10V_4

VSS2DI

R2SET — R69 715/F_4

SCL / SDA — EDIDCLK 10,23, EDIDDATA 10,23

SERIAL BUSES — DDC1DATA / DDC1CLK — DDCDATA 10,24, DDCCLK 10,24 — R511 *4.7K_4 — +3V_DELAY

DDC2DATA / DDC2CLK — VTHM_DAT, VTHM_CLK — R510 *4.7K_4 — +3V_DELAY

Del R84, R85, R466, R467 for TP on PV

DDC3DATA_DP3_AUXN / DDC3CLK_DP3_AUXP — T12, T11

DDC4DATA_DP4_AUXN / DDC4CLK_DP4_AUXP — HDMI_SDA 23, HDMI_SCL 23

DDC 3V tolerance --DDC1,DDC2,SDA/SCL

DDC 5V tolerance --DDC3,DDC4

TS_FDO

THERMAL — DPLUS / DMINUS — VGATHRM+ / VGATHRM-

GENERAL PURPOSE I/O — GPIO_0 … GPIO_28_TDO

GEN_A … GEN_E — GENERICC — T123

VREFG — +0.6V_M72_VREFG — AC11

DPLL_PVDD / DPLL_PVSS — +1.8V_DPLL_PVDD — AH12, AG12

PCIE_PVDD — +1.8V_VPCIE_PVDD — AH31

MPVDD / MPVSS — +VGACORE_MPVDD — A9, B9

DPLL_VDDC — +1.1V_DPLL_VDDC — AE12

XTALIN — EVGA-XTALI — AJ31

XTALOUT — EVGA-XTALO — AJ30

PLL & XTAL

TESTEN / PLLTEST — TEST — R67 1K/F_4 — AH26, AD12

M72-S/M82-S

Memory ID — +VDDR4 — R495, R496, R493, R492 10K/F_4 *10K/F_4 — MEM_ID0 … MEM_ID3

GPIO0 … GPIO5 — 19 GPIO0, 19 GPIO1, T151, T18, T152, 19 GPIO5

10,23 LVDS_BLON — R93 0_4 — EXT_LVDS_BLON

GPIO8 … GPIO13 — 19 GPIO8, 19 GPIO9, T153, 19 GPIO11, 19 GPIO12, 19 GPIO13, T154

HDMI_HP2

42 GFX_CORE_CNTRL0 — R526 0_4 — OSC_SPREAD

2 OSC_SPREAD — VGA_ALERT

5 TEMP_FAIL — T37 — HPD3

42 GFX_CORE_CNTRL1 — R99 0_4 — TEMP_FAIL, PWRCNTL_1

20 BBEN — R91 10K/F_4 — BBEN, ROMCS#

GPIO_23_CLKREQB, GPIO_24_JMODE

+3VDD — T36, T34, T35, T38

DPLL_PVDD Phase Lock Loop Power Dedicated analog power pin for display PLLs. 1.8 V ± 3%

+1.8V — BLM18PG181SN1D(180,1.5A)_6 — L17 — 1.8V(40mA) — C114 10U/6.3V_8, C147 0.1U/10V_4

1.8V+R6043(249R)=1.8V/3=0.6V — R75 499/F_4, R76 249/F_4

PCIE_PVDD PCI-E PLL power. 1.8 V ± 5%

+1.8V — BLM18PG181SN1D(180,1.5A)_6 — L71 — 1.8V(40mA) — C743 10U/6.3V_8, C747 1U/10V_4, C746 0.1U/10V_4

MPVDD Memory Phase Lock Loop Power Same as VDDC

+VGA_CORE — BLM18PG181SN1D(180,1.5A)_6 — L79 — VDDC(345mA) — C822 10U/6.3V_8, C824 1U/10V_4, C823 0.1U/10V_4

DPLL_VDDC Phase Lock Loop Power Dedicated digital power pin for display PLLs. 1.1 V ± 5%

+1.1V — BLM18PG181SN1D(180,1.5A)_6 — L18 — 1.1V(100mA) — C106 10U/6.3V_8, C169 1U/10V_4, C161 0.1U/10V_4

2 EVGA-XTALI — C741 *22P/50V_4 — Y7 *27MHZ — R468 *10M_6 — C735 *22P/50V_4 — EVGA-XTALO — CL=20PF — For Int Clk 27Mhz

Thermal Sensor

5,35 MBCLK2 — R524 0_4 — MBCLK2

5,35 MBDATA2 — R525 0_4 — MBDATA2

VTHM_CLK — R518 *0_4

VTHM_DAT — R519 *0_4

+3V_DELAY — R516 10K/F_4 — VGA_ALERT

U30 — SMCLK, SMDATA, -ALT, GND, VCC, DXP, DXN, -OVT — G781-1P8@EV

761-1_3V — R509 200/F_6 — +3V_DELAY

C790 0.1U/10V_4

VGATHRM+

C793 2200P/50V_4

VGATHRM-

-VGATHRM — R513 10K/F_4 — +3V_DELAY

w/s 10 / 10

I2C ADDRESS: 9AH

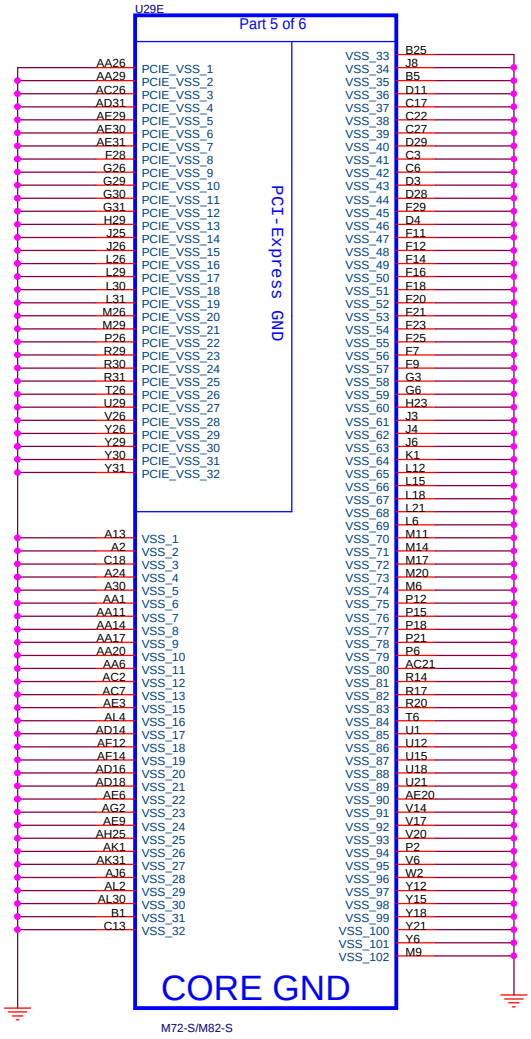
+1.8V_A2VDD_Q — L16 — 1.8V(65mA) — C129 0.1U/10V_4, C168 1U/10V_4, C98 10U/6.3V_8

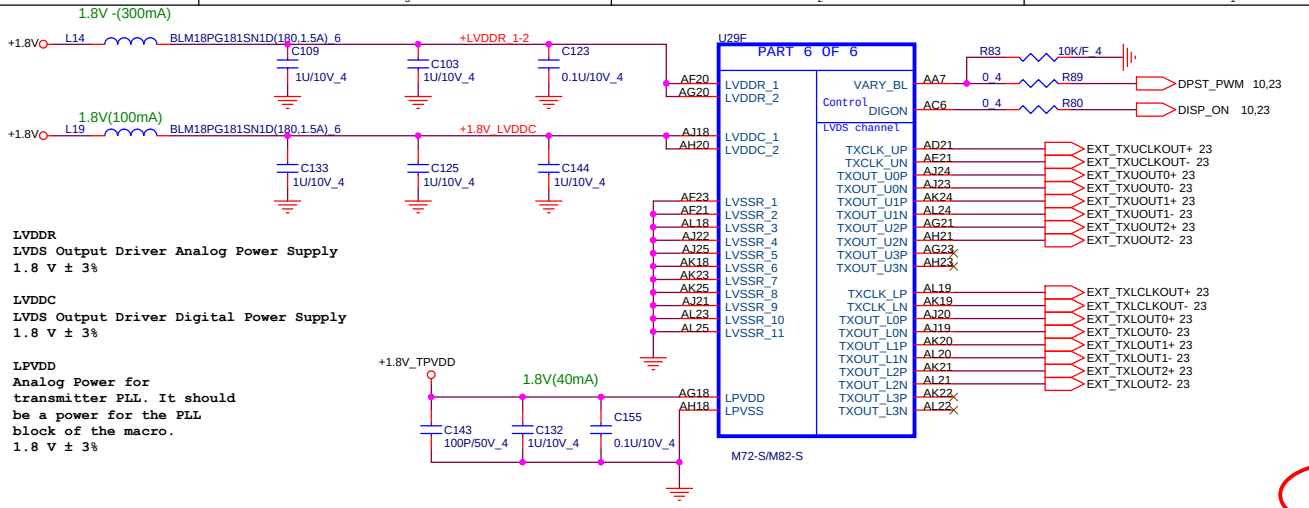
DPB_PVDD — L24 — 1.8V(20mA) — C165 0.1U/10V_4, C182 1000P/50V_4, C145 10U/6.3V_8

+VDDD1 — L15 — 1.8V(100mA) — C110 0.1U/10V_4, C135 1U/10V_4, C97 10U/6.3V_8

+1.8V_TPVDD — L20 — 1.8V(20mA) — C113 0.1U/10V_4, C108 1000P/50V_4, C134 10U/6.3V_8

DPA_B_VDDR — L70 — 1.1V(S100,D200mA) — C740 0.1U/10V_4, C742 1000P/50V_4, C737 10U/6.3V_8





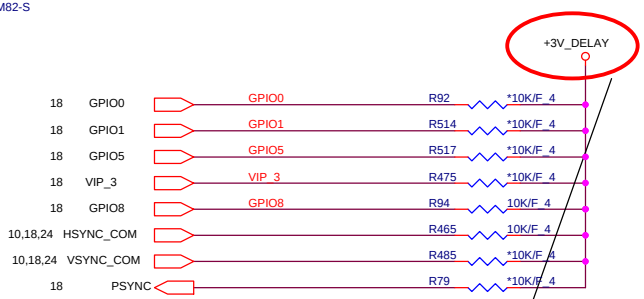
LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%

CONFIGURATION STRAPS

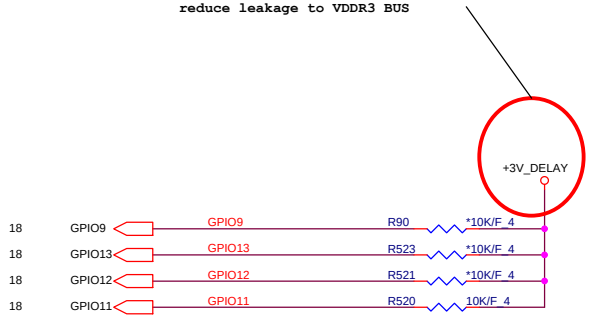
PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows eitherPCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1



SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1



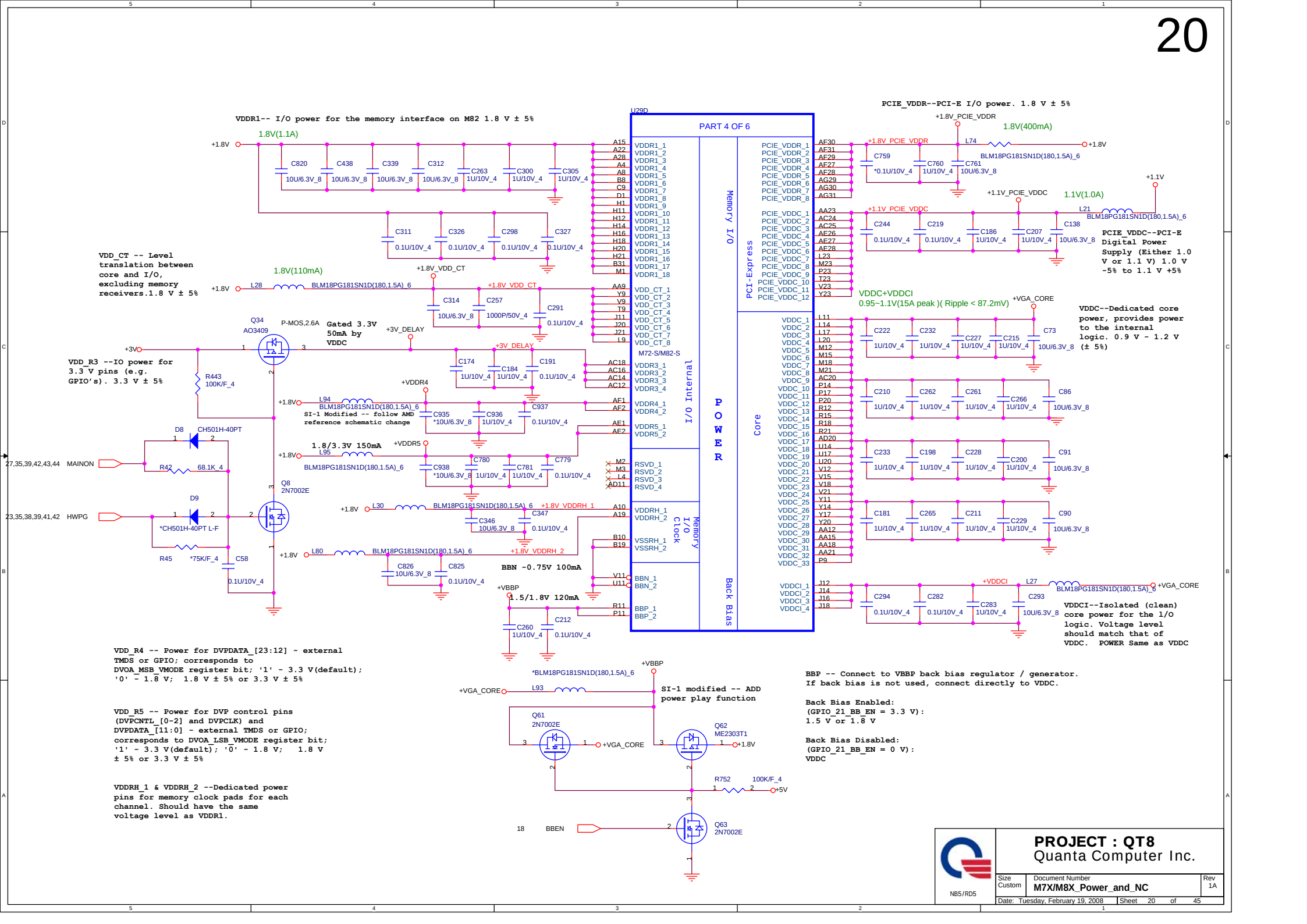
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M7X/M8X_GND / LVDS/ Straps	1A

Date: Tuesday, February 19, 2008 | Sheet 19 of 45



NB5/RD5	PROJECT : QT8 Quanta Computer Inc.		
	Size: Custom	Document Number: M7X/M8X_Power_and_NC	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 20 of 45	

U29C

Part 3 of 6

MEMORY INTERFACE

M72-S/M82-S

MDA0	E29	DQ_0	MA_0	B14	MAA0		
MDA1	E30	DQ_1	MA_1	A14	MAA1		
MDA2	E31	DQ_2	MA_2	B13	MAA2		
MDA3	D31	DQ_3	MA_3	E14	MAA3		
MDA4	C29	DQ_4	MA_4	B17	MAA4		
MDA5	B29	DQ_5	MA_5	A17	MAA5		
MDA6	B30	DQ_6	MA_6	C15	MAA6		
MDA7	A29	DQ_7	MA_7	G16	MAA7		
MDA8	E26	DQ_8	MA_8	E16	MAA8		
MDA9	D26	DQ_9	MA_9	C14	MAA9		
MDA10	E25	DQ_10	MA_10	A12	MAA10		
MDA11	D25	DQ_11	MA_11	B12	MAA11		
MDA12	G23	DQ_12	MA_BA0	C12	A_BA0		
MDA13	G21	DQ_13	MA_BA1	D14	A_BA1		
MDA14	E21	DQ_14	MA_A12	B15	MAA12		
MDA15	D21	DQ_15	MA_BA2	G14	A_BA2		
MDA16	C28	DQ_16					
MDA17	B28	DQ_17	DQMb_0	D30	DQMA#0		
MDA18	B27	DQ_18	DQMb_1	G25	DQMA#1		
MDA19	A27	DQ_19	DQMb_2	C26	DQMA#2		
MDA20	C25	DQ_20	DQMb_3	C21	DQMA#3		
MDA21	A25	DQ_21	DQMb_4	C5	DQMA#4		
MDA22	C24	DQ_22	DQMb_5	D6	DQMA#5		
MDA23	B24	DQ_23	DQMb_6	D2	DQMA#6		
MDA24	C23	DQ_24	DQMb_7	K3	DQMA#7		
MDA25	B23	DQ_25					
MDA26	A23	DQ_26	QS_0	C30	QSA0		
MDA27	B22	DQ_27	QS_1	D23	QSA1		
MDA28	C20	DQ_28	QS_2	B26	QSA2		
MDA29	B20	DQ_29	QS_3	B21	QSA3		
MDA30	A20	DQ_30	QS_4	B6	QSA4		
MDA31	C19	DQ_31	QS_5	E7	QSA5		
MDA32	C8	DQ_32	QS_6	E2	QSA6		
MDA33	C7	DQ_33	QS_7	J2	QSA7		
MDA34	B7	DQ_34					
MDA35	A7	DQ_35	QS_0B	C31	QSA#0		
MDA36	A5	DQ_36	QS_1B	E23	QSA#1		
MDA37	C4	DQ_37	QS_2B	A26	QSA#2		
MDA38	B4	DQ_38	QS_3B	A21	QSA#3		
MDA39	A3	DQ_39	QS_4B	A6	QSA#4		
MDA40	G9	DQ_40	QS_5B	D7	QSA#5		
MDA41	E9	DQ_41	QS_6B	E1	QSA#6		
MDA42	D9	DQ_42	QS_7B	J1	QSA#7		
MDA43	G7	DQ_43					
MDA44	G5	DQ_44	ODT0	E20	ODTA0		
MDA45	F5	DQ_45	ODT1	C11	ODTA1		
MDA46	G4	DQ_46					
MDA47	F4	DQ_47	CLK0	A18	CLKA0		
MDA48	B3	DQ_48	CLK1	A11	CLKA1		
MDA49	B2	DQ_49					
MDA50	C2	DQ_50	CLK0b	B18	CLKA0#		
MDA51	C1	DQ_51	CLK1b	B11	CLKA1#		
MDA52	E3	DQ_52					
MDA53	F3	DQ_53	RAS0b	G20	RASA0#		
MDA54	F2	DQ_54	RAS1b	D12	RASA1#		
MDA55	F1	DQ_55					
MDA56	G2	DQ_56	CAS0b	D20	CASA0#		
MDA57	G1	DQ_57	CAS1b	E12	CASA1#		
MDA58	H3	DQ_58					
MDA59	H2	DQ_59	CS0b_0	E18	CSA0# 0		
MDA60	K2	DQ_60	CS0b_1	G18			
MDA61	L3	DQ_61					
MDA62	L2	DQ_62	CS1b_0	G11	CSA1# 0		
MDA63	L1	DQ_63	CS1b_1	E11			
	F30	MVREFD	CKE0	D18	CKEA0		
	F31	MVREFS	CKE1	G12	CKEA1		
	L5	TEST_MCLK	WE0b	D16	WEA0#		
	L7	TEST_YCLK	WE1b	C10	WEA1#		
	J7	MEMTEST					
			DRAM_RST	J5			

read strobe

write strobe

22 ODTA0 — ODTA0
22 ODTA1 — ODTA1

22 RASA0# — RASA0#
22 RASA1# — RASA1#

22 CASA0# — CASA0#
22 CASA1# — CASA1#

22 WEA0# — WEA0#
22 WEA1# — WEA1#

22 CSA0#_0 — CSA0# 0

22 CSA1#_0 — CSA1# 0

22 CKEA0 — CKEA0
22 CKEA1 — CKEA1

22 CLKA0 — CLKA0
22 CLKA0# — CLKA0#

22 CLKA1 — CLKA1
22 CLKA1# — CLKA1#

22 QSA#[7..0] — QSA#[7..0]

22 QSA[7..0] — QSA[7..0]

22 DQMA#[7..0] — DQMA#[7..0]

22 MDA[63..0] — MDA[63..0]

22 MAA[12..0] — MAA[12..0]

22 A_BA0 — A_BA0
22 A_BA1 — A_BA1

A_BA2 — 22

SI-1 modified -- for support 1Gbit VRAM (64M X 16)

+1.8V

R116 100/F_4

MVREFD

+1.8V

C338 0.1U/10V_4

R113 100/F_4

R532 100/F_4

MVREFS

C817 0.1U/10V_4

R529 100/F_4

R98 4.7K_4

R102 4.7K_4

R97 240/F_4

Change MEMTEST to 240 1% ohm to GND , AMD update

R101 4.7K_4 — +1.8V

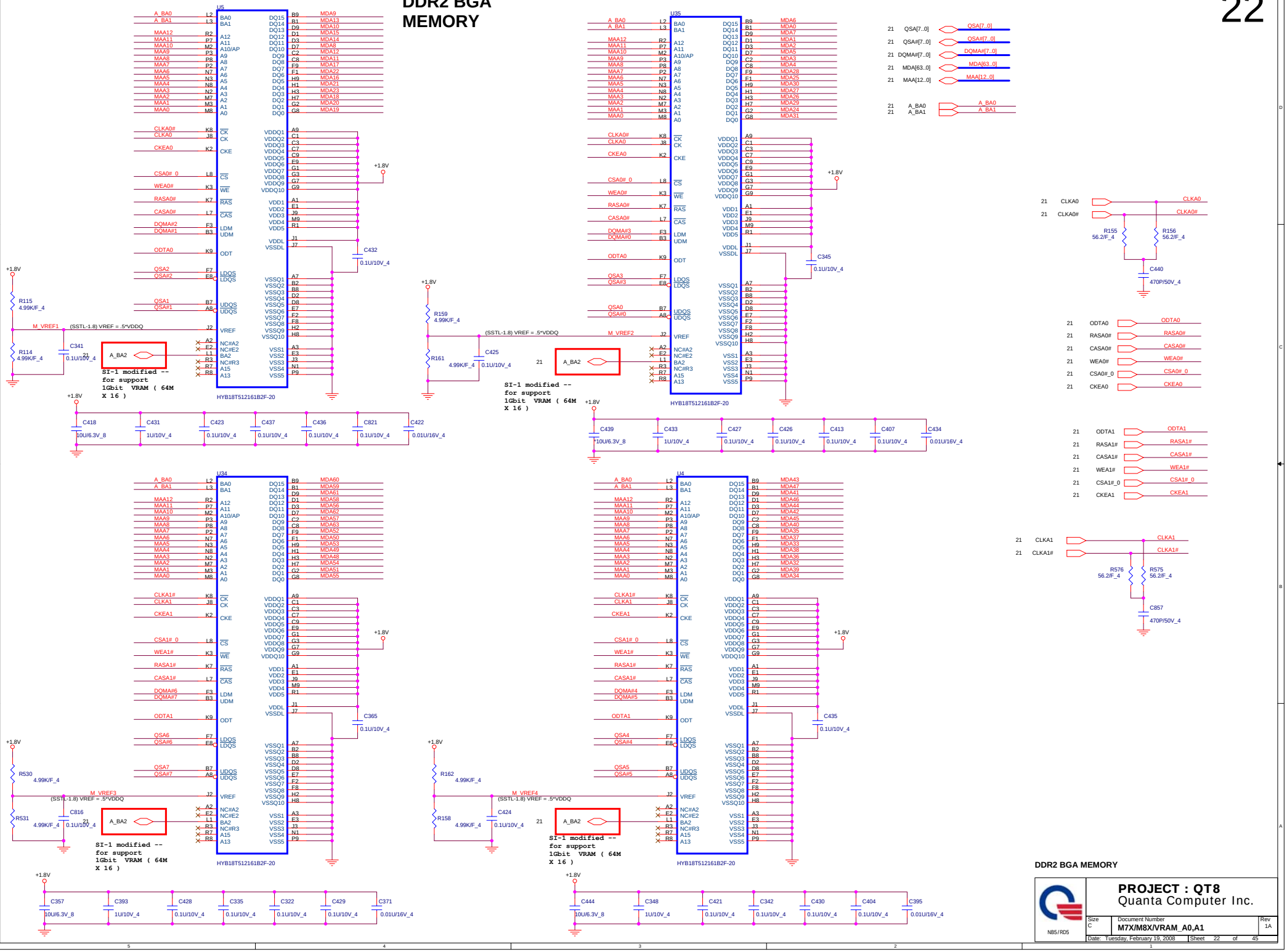
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	M7X/M8X/MEM_Interface	1A

Date: Tuesday, February 19, 2008 Sheet 21 of 45

DDR2 BGA MEMORY



DDR2 BGA MEMORY

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size: C Document Number: M7X/M8X/VRAM_A0,A1	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 22 of 45

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

23

OPTION SIGNAL FROM NB to LVDS for UMA

LA_CLK, LA_CLK#, LA_DATAP0, LA_DATAN0, LA_DATAP1, LA_DATAN1, LA_DATAP2, LA_DATAN2 → RP3, RP1, RP4, RP5 (*0_4P2R_4) → TXLCLKOUT+, TXLCLKOUT-, TXLOUT0+, TXLOUT0-, TXLOUT1+, TXLOUT1-, TXLOUT2+, TXLOUT2-

LB_CLK, LB_CLK#, LB_DATAP0, LB_DATAN0, LB_DATAP1, LB_DATAN1, LB_DATAP2, LB_DATAN2 → RP2, RP6, RP8, RP7 (*0_4P2R_4) → TXUCLKOUT+, TXUCLKOUT-, TXUOUT0+, TXUOUT0-, TXUOUT1+, TXUOUT1-, TXUOUT2+, TXUOUT2-

OPTION SIGNAL FROM M8X to LVDS for discrete

EXT_TXLCLKOUT-, EXT_TXLCLKOUT+, EXT_TXLOUT0-, EXT_TXLOUT0+, EXT_TXLOUT1-, EXT_TXLOUT1+, EXT_TXLOUT2+, EXT_TXLOUT2- → RP59, RP57, RP60, RP61 (0_4P2R_4) → TXLCLKOUT-, TXLCLKOUT+, TXLOUT0-, TXLOUT0+, TXLOUT1-, TXLOUT1+, TXLOUT2+, TXLOUT2-

EXT_TXUCLKOUT-, EXT_TXUCLKOUT+, EXT_TXUOUT0+, EXT_TXUOUT0-, EXT_TXUOUT1-, EXT_TXUOUT1+, EXT_TXUOUT2-, EXT_TXUOUT2+ → RP58, RP62, RP64, RP63 (0_4P2R_4) → TXUCLKOUT-, TXUCLKOUT+, TXUOUT0+, TXUOUT0-, TXUOUT1-, TXUOUT1+, TXUOUT2-, TXUOUT2+

+12VALW → R19 330K_6 → LCDONG; A03404 current 5.8A ID; N-MOS,5.8A Q1 AO3404; +3V → C16 0.1U/10V_4; +3VLCD

+5VSUS → R14 100K/F_4 → Q4 2N7002E; C22 0.1U/10V_4; R10 22_8 → LCDDISCHG; Q3 PDTC144EU; R17 2.2K_4; 10,19 DISP_ON; LCDON# → Q2 2N7002E

+5V → R401 75R/F_6 → +LOGO_PWR

SI-2 modified-delete R402 and R401 from 0ohm to 75ohm

+3V → R8 2.2K_4 EDIDCLK; R7 2.2K_4 EDIDDATA

+3VLCD → L1 PBY201209T-4A_8 → +3VLCD_CON; C12 10U/6.3V_8; C10 0.1U/10V_4; C13 0.01U/16V_4

+VIN_BLIGHT; +3VLCD_CON; C6 1000P/50V_4; C678 1000P/50V_4; 10,18 EDIDDATA; +LOGO_PWR; BLONCON

CN1 (41/42): VADJ1, EDIDCLK 10,18, Camera Pin; TXLCLKOUT+/-, TXLOUT0+/-, TXLOUT1+/-, TXLOUT2+/-, TXUCLKOUT+/-, TXUOUT0+/-, TXUOUT1+/-, TXUOUT2+/-

PN_BLON → D5 CH501H-40PT → BLONCON; C28 22P/50V_4; R22 100K/F_4; +3VPCU → R24 33K_6 → D6 CH501H-40PT → LID_EC#; LID_EC# 34,35

10,18 LVDS_BLON → LVDS_BLON R23 1K/F_4 → PN_BLON; D7 CH501H-40PT → HWPG 20,35,38,39,41,42

12 LCD_BK → LCD_BK → Q5 PDTC144EU; R259 *10K/F_4 → +3VS5

Del R21 and Pull hi R259 to +3VS5, add D7 to HWPG on PV

PV del logo light

10,19 DPST_PWM → DPST_PWM R88; 35 PWM_VADJ → PWM_VADJ R96; LCD CONN *0_4; 0_4 → VADJ1; C5 *4.7U/6.3V_6; C7 0.1U/10V_4

UMA/DISCRETE select for HDMI

From RS780M

for Layout concern ,placement close north bridge

C_PEG_TX#15 C386 / C_PEG_TX15 C387; C_PEG_TX#14 C388 / C_PEG_TX14 C389; C_PEG_TX#13 C355 / C_PEG_TX13 C344; C_PEG_TX#12 C827 / C_PEG_TX12 C828 (*0.1U/10V_4) → TX2_HDMI-L/+L, TX1_HDMI-L/+L, TX0_HDMI-L/+L, TXC_HDMI-L/+L

for Layout concern ,placement close HDMI conn

RP31, RP23, RP37, RP17 (*0_4P2R_4) → TX2_HDMI-/+, TX1_HDMI-/+, TX0_HDMI-/+, TXC_HDMI-/+

From M82-S

18 TX2_HDMI_L-/L+; 18 TX1_HDMI_L-/L+; 18 TX0_HDMI_L-/L+; 18 TXC_HDMI_L-/L+ → C794 / C789, C782 / C786, C799 / C797, C768 / C776 (0.1U/10V_4) → TX2_HDMI-/+, TX1_HDMI-/+, TX0_HDMI-/+, TXC_HDMI-/+

for Layout concern ,placement close HDMI conn

+5V → Q36 2N7002E; R528 100K/F_4

R507 499/F_4 TX2_HDMI+; R508 499/F_4 TX2_HDMI-; R506 499/F_4 TX1_HDMI+; R505 499/F_4 TX1_HDMI-; R512 499/F_4 TX0_HDMI+; R515 499/F_4 TX0_HDMI-; R504 499/F_4 TXC_HDMI+; R500 499/F_4 TXC_HDMI-

UMA RS780M → 750 ohm CS17502FB19

DIS M82-S → 499 ohm CS14992FB24

Close to HDMI Connector

+VIN → L2 FBM2125 HM330-T(4A,0.015) 8 → +VIN_BLIGHT

C15 0.1U/50V_6; C11 0.01U/50V_4; C9 0.1U/50V_6; C14 *10U/25V_12; C8 0.1U/50V_6

+5V_HDMVCC → D31 CH501H-40PT; +5V_HDMVCC → D32 CH501H-40PT

R494 4.7K_4; R503 4.7K_4 → HDMI_SCLK, HDMI_SDATA

Change R494, R503 to 4.7K for AMD on PV

Del C748, C756 for HDMI on PV

HDMI PORT

CN29 HDMI CONN: TX2_HDMI+/-, TX1_HDMI+/-, TX0_HDMI+/-, TXC_HDMI+/-, SHELL1/3, D2 Shield, D1 Shield, D0 Shield, CK Shield, CE Remote, NC, DDC CLK, DDC DATA, GND, +5V, HP DET, SHELL4, SHELL2

HDMI_SCLK, HDMI_SDATA → L73, L75 0_6 → HDMISCL, HDMISDA

+5V → F1 FUSE1A6V_POLY; +5V_HDMVCC; C128 *0.1U/10V_4; HDMI_DET

HDMI HPD SENSE

10,18 TMDS_HPD → TMDS_HPD R66 20K/F_4 HDMI_DET

check 3v or 5v

D10 UDZS2.7BTE-17; R64 100K/F_4

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

18 HDMI_SDA, 18 HDMI_SCL → RP65 0_4P2R_4 → HDMI_SDATA, HDMI_SCLK

Discrete DDC4 is 5V tolerance , the MOSFET level shifter no need

UMA DDC is 3V tolerance,the MOSFET level shifter is need

DIS

+3V → R680 *2K/04; +5V

10 HDMI_DDC_CLK → Q59 *FDV301N → HDMI_SCLK

HDMI_DDC_CLK R753 *0_4 HDMI_SCLK; HDMI_DDC_DATA R755 *0_4 HDMI_SDATA

+3V → R681 *2K/04; +5V

10 HDMI_DDC_DATA → Q60 *FDV301N → HDMI_SDATA

Change 2N7002 to FDV301N for AMD on PV

UMA

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN,HDMI CONN	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 23 of 45	

CRT PORT

SI-2 modified --Change Layout footprint 12/27

+5VCRT — C670 0.1U/10V_4

+5V — F2 40 mils — +5VCRT

40 MIL

FUSE1A6V_POLY

CRT_R_1_L — L61 BLM18BA470SN1(47,300MA)_6 — CRT_R1

CRT_G_1_L — L60 BLM18BA470SN1(47,300MA)_6 — CRT_G1

CRT_B_1_L — L59 BLM18BA470SN1(47,300MA)_6 — CRT_B1

R400 150/F_4 · R399 150/F_4 · R398 150/F_4 · C677 5.6P/50V_6 · C675 5.6P/50V_6 · C672 5.6P/50V_6 · C671 5.6P/50V_6 · C674 5.6P/50V_6 · C676 5.6P/50V_6

EMI

CRT CONN CN20

close conn within 600mils

R400 for UAM use 140 ohm on PV(AMD)

+5V — C673 0.1U/10V_4

U21 AHCT1G125DCH

U22 AHCT1G125DCH

10,18,19 VSYNC_COM → PR_VSYNC 37

10,18,19 HSYNC_COM → PR_HSYNC 37

R1 0_4 CRTDDCCLK2

R3 33_4 CRTVSYNC

R4 33_4 CRTHSYNC

R5 0_4 CRTDDCDAT2

C1 *470P/50V_4 · C2 *47P/50V_4 · C3 *47P/50V_4 · C4 *47P/50V_4

follow AMD reference schematic change for reduce leakage to VDDR3 BUS

+3V_DELAY — R761 4.7K_4 — +3V — R25 *4.7K_4

10,18 DDCCLK — DDCCLK — Q6 2N7002E — DDCCLK2 — DDCCLK2 37

+3V_DELAY — R762 4.7K_4 — +3V — R26 *4.7K_4

10,18 DDCDATA — DDCDATA — Q7 2N7002E — DDCDAT2 — DDCDAT2 37

R2 6.81K_4 · R6 6.81K_4

+5VCRT — +5VCRT — CH501H-40PT — D25 — +5V_CRT2

+3V

D28 *BAV99W — CRT_R1

D27 *BAV99W — CRT_G1

D26 *BAV99W — CRT_B1

D1 *BAV99W — DDCCLK2

D2 *BAV99W — CRTVSYNC

D3 *BAV99W — CRTHSYNC

D4 *BAV99W — DDCDAT2

U23

37 PR_RED — PR_RED — CRT_R_1_L

37 PR_GEN — PR_GEN — CRT_G_1_L

37 PR_BLU — PR_BLU — CRT_B_1_L

35,37 PR_INSERT#

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E

YA YB YC YD

CRT_R CRT_G CRT_B → CRT_R 10,18 · CRT_G 10,18 · CRT_B 10,18

VCC GND

+5V_SW — R403 0_6 — +5V

C679 0.1U/10V_4

R404 10K/F_4

74CBT3257

EMI

CRT SWITCH

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8	Quanta Computer Inc.
NB5/RD5	
Size: Custom	Document Number: CRT
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 24 of 45

For 5158E

2 CLK_48M_CR — R397 *0_4 XTLO — UMA BOM need to add

+3VSUS — R321 *100K/F_4

26,29 CARD_LED# — R320 *0_4 CARD_LEDO

U19 *RTS5158

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ

XD_CD# — SP2 — SD_CD# — SP4

SI-2 modified --Fix Y5 layout footprint to XTAL-5X3_2-3_8 (ME placement)

R362 *6.19K/F_4 RREF — RREF

13 USBP6_CR- — DM — 4
13 USBP6_CR+ — DP — 5

C665 *5.6P/50V_4 — XTLO — 48
R395 *270K_4 — *12MHz — Y5
C668 *5.6P/50V_4 — XTLI — 47

For 5158 BG6120000717

MODE_SEL — 45
R394 *10K/F_4 — C667 *47P/50V_4

For 5158

+3VSUS — R667 *100K/F_4 — 5158_RST# — 44
C925 *1U/10V_4

If SD_DAT1 connect to SP4 , MOD_SEL need to let it to N.C

XD_CLE/CF_D3 — 43 SP19
XD_CE#/CF_D11 — 42 SP18
XD_ALE/CF_D4 — 41 SP17
SD_DAT2/XD_RE#/CF_D12 — 40 SP16
SD_DAT3/XD_WE#/CF_D5 — 39 SP15
XD_RDY/CF_D13 — 38 SP14
SD_DAT4/XD_WP#/CF_D6 — 37 SP13
SD_CMD — 36 SD_CMD_R
SD_DAT5/XD_D0/CF_D14 — 35 SP12
SD_CLK/XD_D1/MS_CLK/CF_D7 — 34 SP11
SD_DAT6/XD_D7/MS_D3/CF_D15 — 33 SP10
CF_CS0# — 30
MS_INS#/CF_IORD# — 29 MS_CD#
SD_DAT7/XD_D2/MS_D2/CF_IOWR# — 28 SP8
SD_DAT0/XD_D6/MS_D0/CF_RST# — 27 SP7
SD_DAT1/XD_D3/MS_D1/CF_IORDY — 26 SP6
XD_D5/MS_BS/CF_A2 — 25 SP5

AV_PLL_IN — 1 — C647 *0.1U/10V_4 — C918 *1U/10V_4

VREG_OUT — 10 VREG
5V_IN — 8
A3V3_IN — 3
D3V3_IN — 33

+3VSUS_RTS — C593 *0.1U/10V_4 — C598 *4.7U/6.3V_6 — R323 *0_6 — +3VSUS

*0.1U/10V_4 — C633 — C634 *0.1U/10V_4

D3V3_OUT — 11 — *0.1U/10V_4 — C612 — C589 *4.7U/6.3V_6 — +3VSUS

A3V3_OUT — 7 — +3VSUS

CARD_3V3_OUT — 9 — +3VCARD

AG33 — 6
AG_PLL — 46
DGND2 — 32
DGND1 — 12

C629 *1U/10V_4 — C624 *0.1U/10V_4 — C917 *0.1U/10_4

+3VCARD — C628 *0.1U/10V_4 — C618 *0.1U/10V_4 — C617 *0.1U/10V_4

SI-2 remove R673 not need -- UMA BOM remove

For 5158
SP6 — R339 *0_4 — SD_DAT1
SP4 — R333 *0_4
For 5158E

AL005158B10 -->RTS5158E
AL005158B00 -->RTS5158

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7	R315 *0_4	MS_DATA0_SD_DAT0	
	R316 *0_4	XD-D6	
SP6	R334 *0_4	MS_DATA1	
	R338 *0_4	XD-D3	
SP8	R345 *0_4	MS_DATA2_XD_D2	
SP16	R666 *0_4	SD_DAT2	
	R676 *0_4	XD-RE#	
SP5	R327 *0_4	MS_BS	
	R335 *0_4	XD-D5	
SP15	R675 *0_4	SD_DAT3	
	R390 *0_4	XD_WE	
SP11	R354 *0_4	SD_CLK_MS_CLK	
	R358 *0_4	XD-D1	
SP2	R319 *0_4	SD_WP	
SP13	R677 *0_4	XD-WP#	
SP19	R393 *0_4	XD-CLE	
SP4	R317 *0_4	XD-D4	
SP10	R351 *0_4	MS_DATA3	
	R348 *0_4	XD-D7	
SP14	R389 *0_4	XD-RB#	
SP12	R369 *0_4	XD-D0	
SP17	R391 *0_4	XD-ALE	
SP18	R392 *0_4	XD-CE#	
SD_CMD_R	R372 *0_4	SD_CMD	

CH501H-40PT
D23 — MS_CD#
XD_CD# — SD_CD#
CH501H-40PT
C873 270P/25V_4

RTS5158 need to remove D23/D24/C873

JMB 380 Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

C905 *270P/25V_4

+3VCARD — R678 *10K/F_4 — XD-WP#

Del R625 for TP on PV

CN36 — 5IN1 CARD READER SOCKET

XD-RB# — XD-RE# — XD-CE# — XD-CLE — XD-ALE — XD_WE — XD-WE — XD-WP — XD-D0 — XD-D1 — SD_DAT2 — SD_DAT3 — SD_CMD

SD_CLK_MS_CLK — MS_DATA3 — MS_CD# — MS_DATA2_XD_D2 — MS_DATA0_SD_DAT0 — MS_DATA1 — MS_BS

26 MS_CD#

XD-DATA0 XD-DATA1 XD-DATA2 XD-DATA3 XD-CMD GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

XD-DATA7 XD-DATA6 XD-DATA5 XD-DATA4 XD-DATA3 XD-DATA2 XD-DATA1 XD-DATA0 SD-CLK SD-VCC

SD-C/D SD-CD-SW SD-W/P SD-WP-SW XD-CD XD-VCC

SD_CD# SD_CD# SD_WP SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

SD_CD#

+3VCARD — C872 2.2U/6.3V_6 — R607 150K/F_4

CLOSE CONN

+3V — Q25 *AO3409 — +3VCARD — +5V

26 MC_PWR_CTRL_0# — XD_PWON R387 *10K/F_4 — +3VCARD

R332 0_8

RESERVED for JMicron -- after programming can out-put +3.3V throught MC_PWR_CTRL_0# signal

+3VCARD — C887 0.1U/10V_4 — C894 0.1U/10V_4 — C874 0.1U/10V_4

SI-2 for 台端Conn

CN42 — *TAI TWUM 5IN1 CARD READER SOCKET

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

26

xD-R/B xD-RE xD-CE xD-CLE xD-ALE xD-WE xD-WP xD-D0 xD-D1 SD-DAT2 SD-DAT3 SD-CMD GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

NC NC

xD-D7 xD-D6 xD-D5 xD-D4 xD-D3 xD-D2 SD-DAT0 SD-CLK SD-VCC

SD-CD SD-WP xD-CD xD-VCC

GND GND GND GND

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

+3VCARD +3VCARD

26	MDIO00	R611 0_4	MS_DATA0_SD_DAT0
26	MDIO01	R623 0_4	XD-D0
		R608 0_4	SD_DAT1
		R610 0_4	MS_DATA1
		R622 0_4	XD-D1
26	MDIO02	R612 0_4	MS_DATA2_XD_D2
		R620 0_4	SD_DAT2
26	MDIO03	R614 0_4	MS_DATA3
		R619 0_4	SD_DAT3
		R606 0_4	XD-D3
26	MDIO04	R618 0_4	SD_CMD
		R609 0_4	MS_BS
		R627 0_4	XD_WE
26	MDIO05	R617 47/F_4	SD_CLK_MS_CLK
		R634 47/F_4	XD-CE#
26	MDIO06	R593 0_4	SD_WP
		R591 0_4	XD-WP#
		R633 0_4	XD-CLE
26	MDIO07	R605 0_4	XD-D4
26	MDIO08	R603 0_4	XD-D5
26	MDIO09	R602 0_4	XD-D6
26	MDIO10	R601 0_4	XD-D7
26	MDIO11	R679 0_4	XD-RE#
26	MDIO12	R635 0_4	XD-RB#
26	MDIO13	R628 0_4	XD-ALE
26	MDIO14		

SI-2 modified - for Jmicron updae

PAD8 MDC_SPRING — PAD9 MDC_SPRING — PAD10 MDC_SPRING — PAD11 MDC_SPRING

H32 *H-S315D110P2 — H31 *H-S315D110P2 — H13 *H-C173X118D173X118N — PAD7 — *MDC_SPRING

H22 *H-S315D110P2 — H23 *H-C244D186P2 — H6 *H-C217D157P2 — H9 *H-C217D157P2 — H8 *H-C217D157P2 — H3 *H-C256D157P2

H12 *H-C315D118P2 — H7 *H-S315D110P2 — H25 *H-C315D118P2 — H18 *H-C256D217P2 — H17 *H-C256D217P2

K/B SCREW HOLE — VGA Hole

H5 *H-S315D110P2 — H11 *H-S315D110P2 — H4 *H-C217D181P2 — H10 *H-C217D181P2 — H1 *H-C315D118P2

PAD4 — PAD5 — PAD6 — MDC_SPRING — *MDC_SPRING

Del PAD1 for TP on PV

PAD2 — PAD3 — *MDC_SPRING

for MDC cable routing

Mini Card Hole

H20 *H-C256D217P2 — H14 *H-C256D217P2

SI-2 for CN37

H28 *H-C236D87P2 — H29 *H-C236D87P2 — H30 *H-C236D87P2

H26 *H-C256D217P2 — H27 *H-C256D217P2

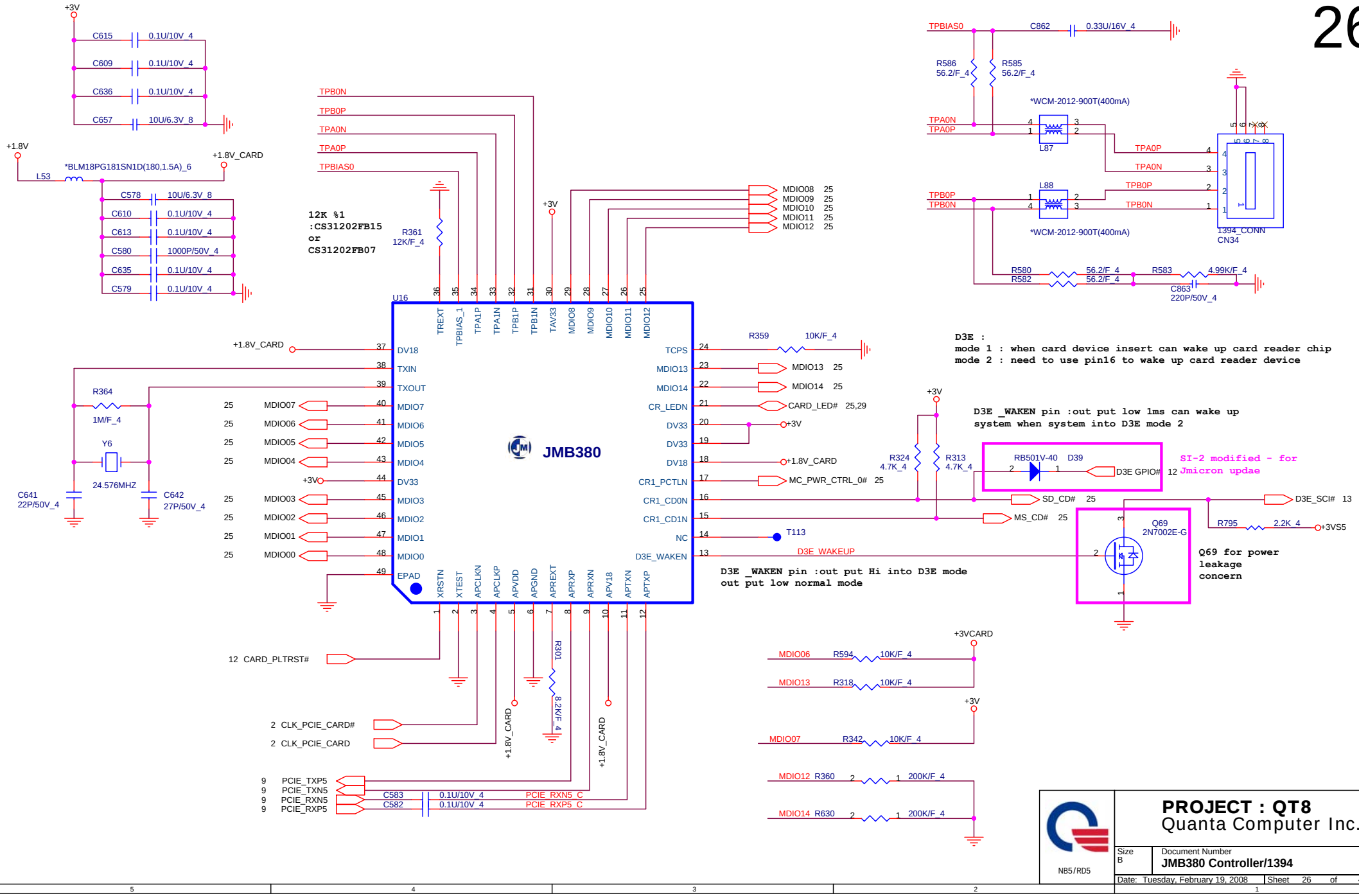
PAD12 — MDC_SPRING

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

Date: Tuesday, February 19, 2008 — Sheet 25 of 45



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	1A

Date: Tuesday, February 19, 2008 Sheet 26 of 45

NB5/RD5

SI-2 Modified -- change footrint QFN48-7X7-5-49P-1H for datasheet update

SI-2 Modified

EAPD#--DEFAULT is Hi

Del R672 direct on PV

Del R686, R356, R349 direct on PV

Change C923, 924 footprint

TO Headphone jack

TO Internal Speakers

92HD71B7

SI-2 for EMI

recommand use X7R /10V

TO EXTERNAL MIC

TO DOCK MIC

Audio JACK: Normal Open
SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#-->DOCK MIC

Change to SHORT-1A for EMI on PV

R807 change to 330K for HP on PV

Change C962, 963 footprint

Del R814, R815 on PV

TO DOCK Headphone

Add C141 for soft star on PV

TO AUDIO/B CON.

SI-2 modified -- Change footprint for ME request , pin 13,14 are 固定pin

TO Headphone jack

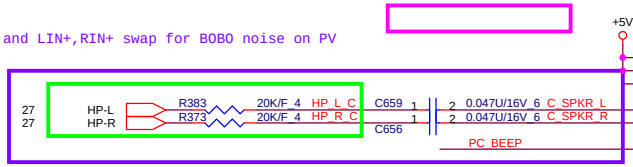
DOCK MIC DETECT

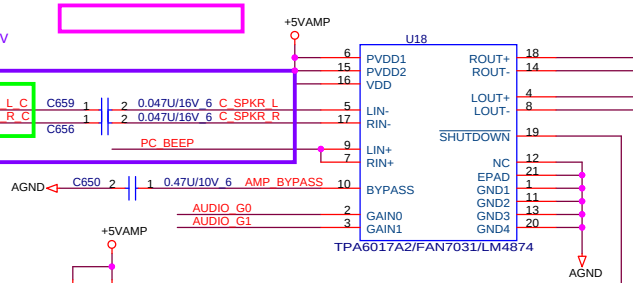
PROJECT : QT8	
Quanta Computer Inc.	
Size: Custom	Document Number: Azalia AD1883
Rev: 1A	
NB5/RD5	
Date: Tuesday, February 19, 2008	Sheet 27 of 45

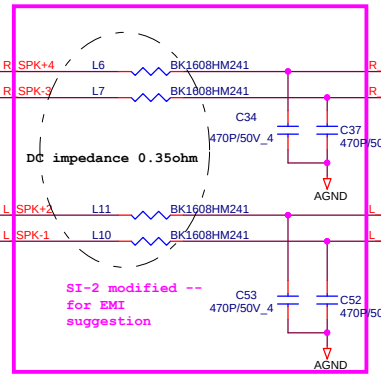
AUDIO AMPLIFIER

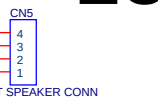
SI-2 Modified -- remove C621/C623

LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV









INT. SPEAKER

Vrms = Vpp / 2 √2

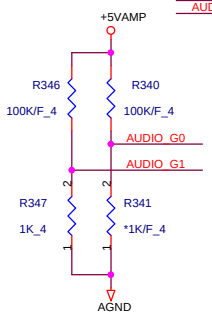
Power = (Vrms)²/ R

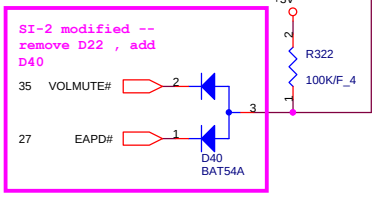
QT8 speaker -- 3.2ohm / 2W

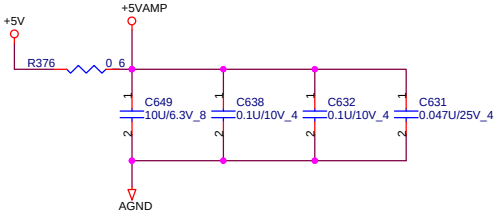
PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue

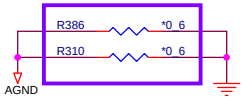
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

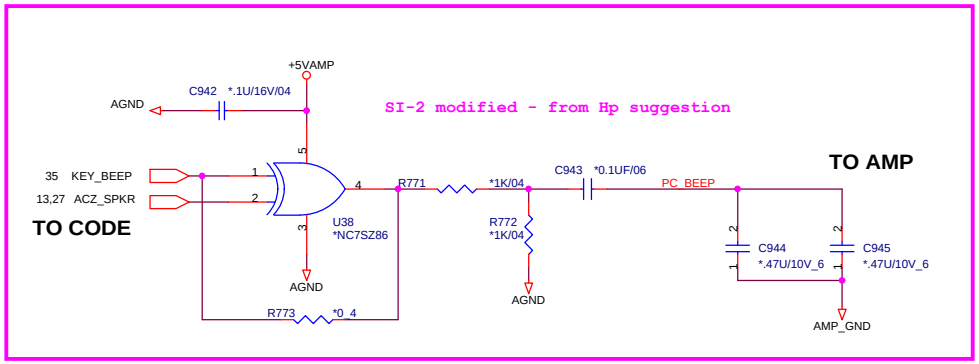








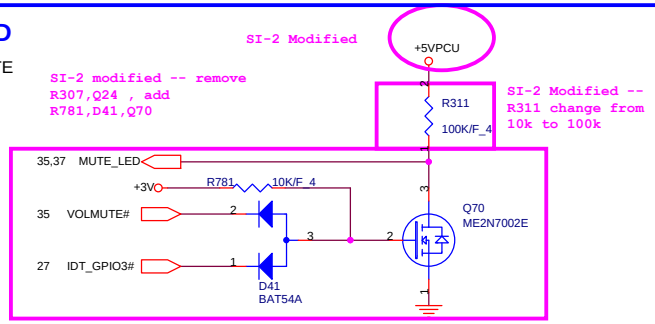
PC-BEEP



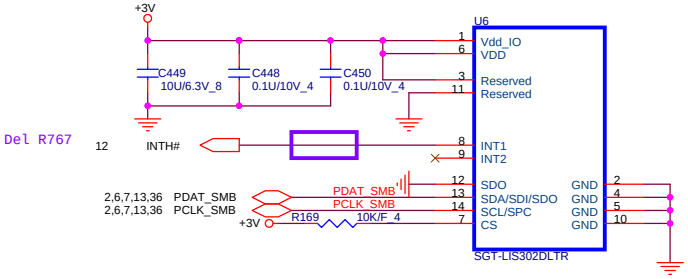
MUTE_LED

Low -->un-MUTE

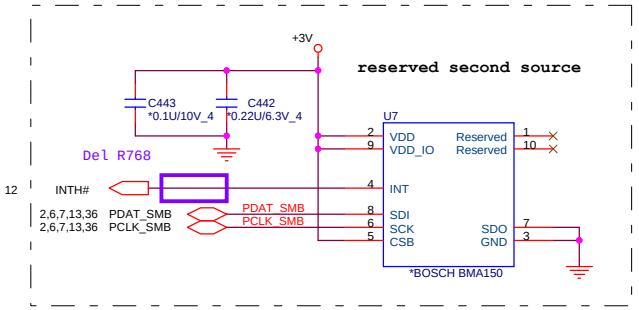
High-->Mute



Acceleration sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



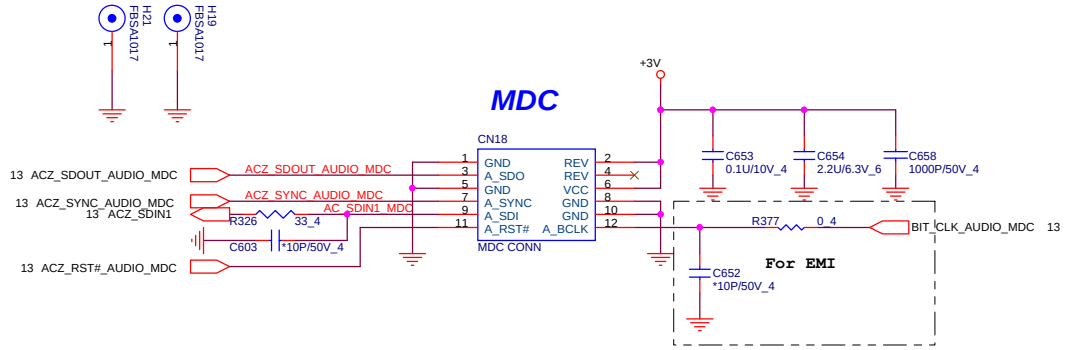
PROJECT : QT8
Quanta Computer Inc.

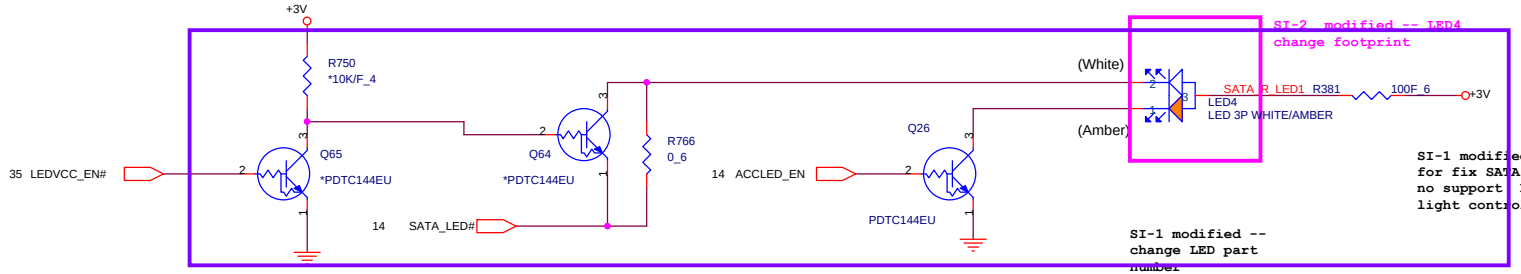
Size	Document Number	Rev
Custom	AMP_TPA6017/INT SPK	1A

Date: Tuesday, February 19, 2008 Sheet 28 of 45

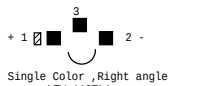
NB5/RD5

Modem CONN

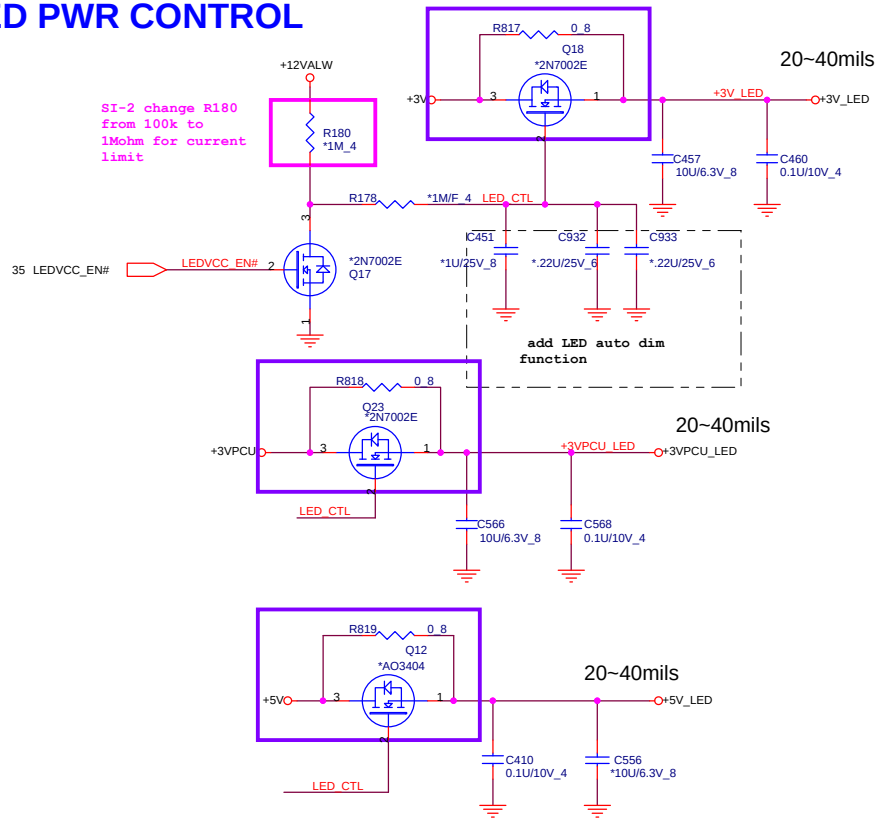




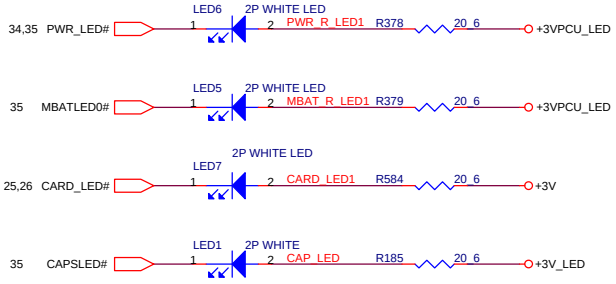
LED

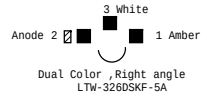


LED PWR CONTROL

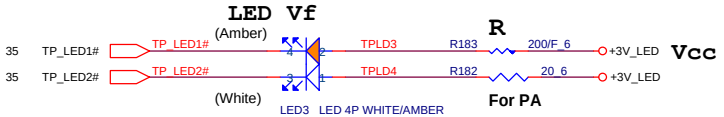


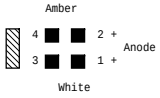
Del R380
Change R381 to 100
Add R766, R817, R818, R819
LED PWR control no-stuff on PV





I = Vcc -Vf / R





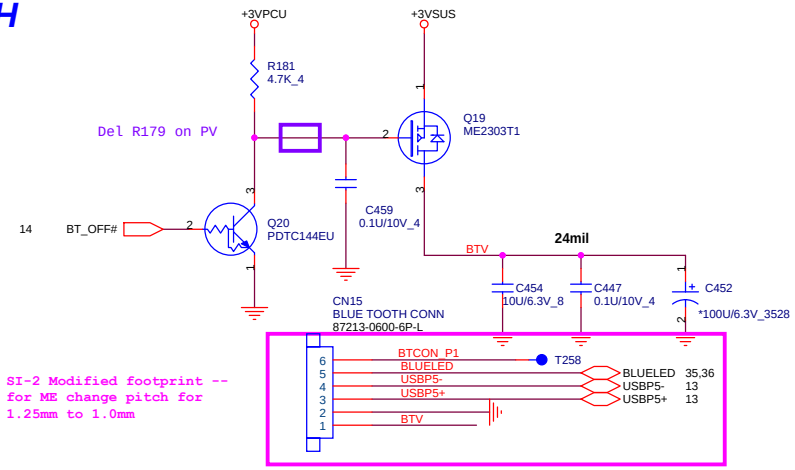
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

Date: Tuesday, February 19, 2008 | Sheet 29 of 45

NB5/RD5

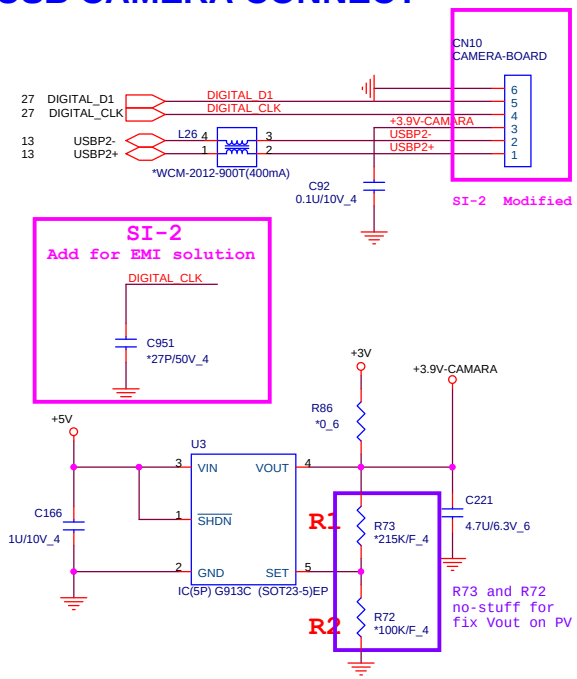
BLUETOOTH



For Discrete Touch-Screen

SI-2 Modified -- remove touch-screen function

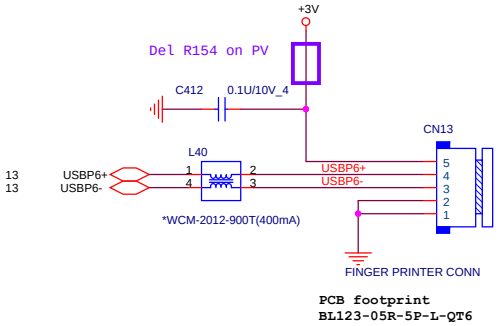
USB CAMERA CONNECT



Vout=1.25(1+R1/R2)

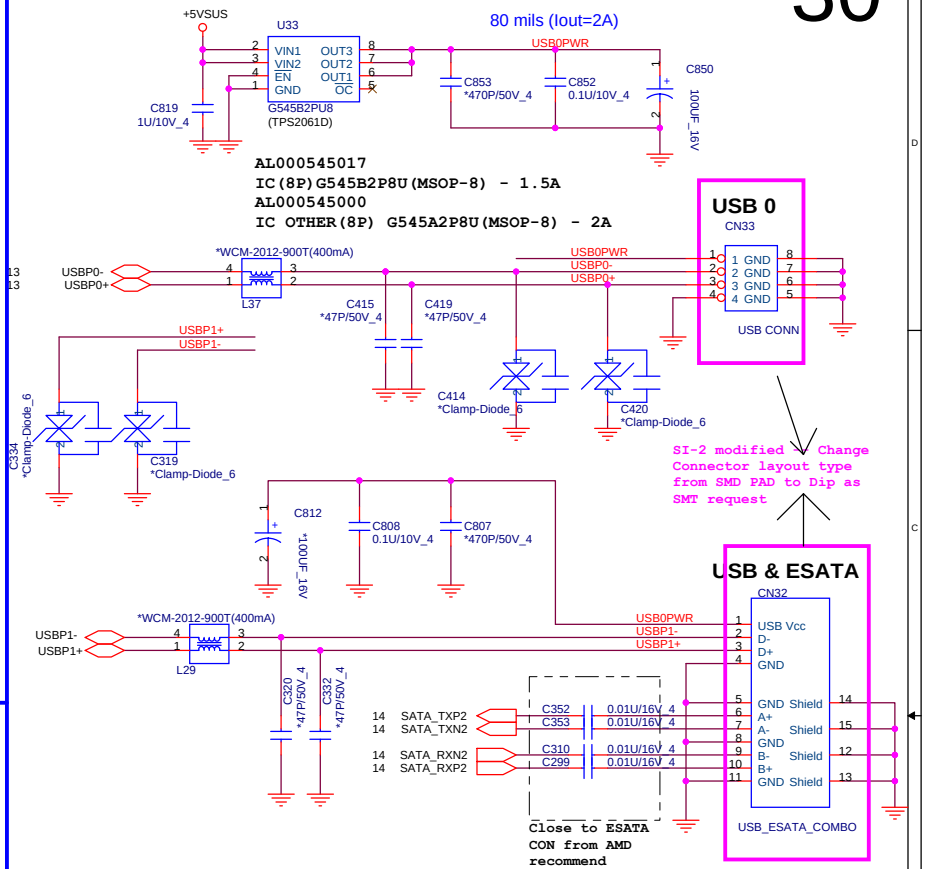
USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

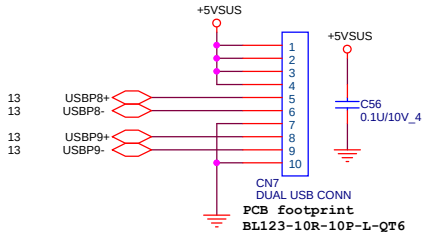


PCB footprint
BL123-05R-5P-L-QT6

LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



PCB footprint
BL123-10R-10P-L-QT6

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WEBCAM/FT/USBX4/ESATA	1A

Date: Tuesday, February 19, 2008 Sheet 30 of 45

Stuffed for 8101E/8102E/RTL8111C

Stuffed for RTL8111C(10/100/1000)

Stuffed for 8102E/RTL8101E

Del R50 on PV

Del R36, C712, C710 on PV

Del R766 for TP on PV

Del U1, R46 on PV

use BIOS to programming EEPROM , EEDI should be pull Hi

R46 only for 8111B, 8101E&8102E&8111C can remove

Remove R456 and Add D42 on PV

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R778 SI-2 modified -- RTL8111C remove , RTL8111B,8101E,8102E need to stuff

Del R429, R431, R433, R435, C718, C726 for 8111B on PV

Del R428 on PV

SI-2 modified -- LAN_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

Link

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

AL08101E005 IC(64P)RTL8101E-GR(QFN)

NS892402:GIGABIT DB0AT9LAN05

NS892405:10/100 DB0ZB1LAN04

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ11-RJ45 CN	1A

Date: Tuesday, February 19, 2008 Sheet 31 of 45

NB5/RD5

LANVCC
1.2W
364mA

+3VLANVCC

>30mil

Power trace Layout 寬度> 30mil

+3V_LAN

Del L68, L69 direct on PV

C720 10U/6.3V_8
C723 0.1U/10V_4

placement close to lan chipset

C719 0.1U/10V_4
C722 0.1U/10V_4
C716 0.1U/10V_4
C729 0.1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

+3V_A_LAN

>30mil

C715 0.1U/10V_4
C714 0.1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

L8
RTL8111C (Gaga lan) use 4.7uH power choke A>500mA tolerance ±15%
RTL8101E & RTL8102E stuff 0ohm

+FB12 31

L9
RTL8111C stuff
RTL8102E need to remove L9

+CTRL18

L8 4.7UH,+-20%,580MA_8

L9 0_8

+LAN_A1.8

Power trace Layout 寬度> 30mil

>30mil

+LAN_A1.8

C50 *10U/6.3V_8

RTL 8101E /8102E stuff , RTL 8111C need to remove

C46 10U/6.3V_8

C46

C51 10U/6.3V_8
C57 0.1U/10V_4

placement close to lan chipset

C728 0.1U/10V_4
C727 0.1U/10V_4
C721 0.1U/10V_4
C730 0.1U/10V_4

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

C46
RTL8111C stuff
RTL8101E / 8102E can remove

+LAN_E1.8

R442 0_8
R220

R220
8102E need to remove
8101E use 0 ohm
8111C use 4.7uH

C731 0.1U/10V_4
C732 1U/10V_4

C732 change to 1U on PV

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

L66 0_8
L66

L66
RTL8111C used 0ohm
RTL 8101E/8102E need to remove

C705
RTL8111C stuff
RTL8101E / 8102E can remove

Power trace Layout 寬度> 30mil

+CTRL15

L67 L67 *0_8

C704

L67 & C704
8101E/8102E stuff
8111C need to remove

C704 *10U/6.3V_8

C705

C705 10U/6.3V_8
C711 10U/6.3V_8
C49 0.1U/10V_4
C79 0.1U/10V_4
C84 0.1U/10V_4
C83 0.1U/10V_4
C61 0.1U/10V_4
C63 0.1U/10V_4
C48 0.1U/10V_4
C47 0.1U/10V_4
C80 0.1U/10V_4
C55 0.1U/10V_4
C66 0.1U/10V_4

>30mil

+LAN_D1.5

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

NB5/RD5

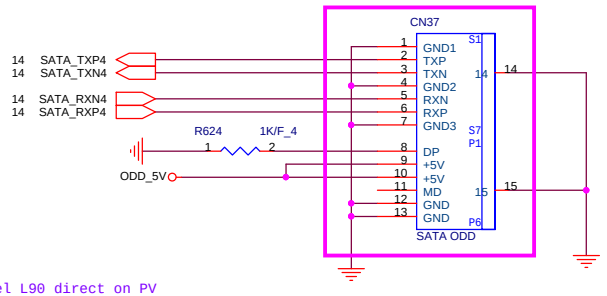
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A

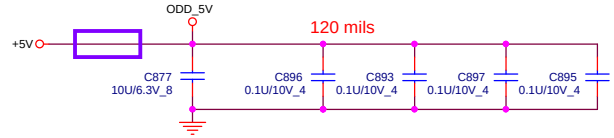
Date: Tuesday, February 19, 2008 | Sheet 32 of 45

SATA CD-ROM

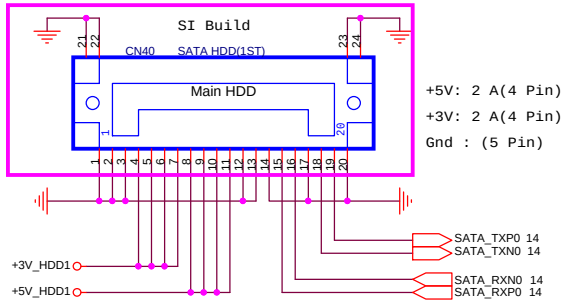
SI-2 Modified footprint -- Modify 12/27

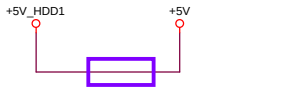


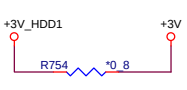
Del L90 direct on PV



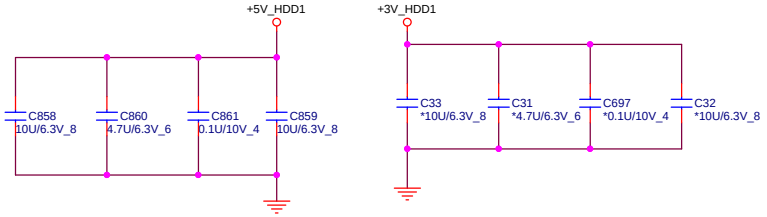
SI-2 Modified footprint -- Modify 固定孔 Size as SMT request







Del R578 direct on PV

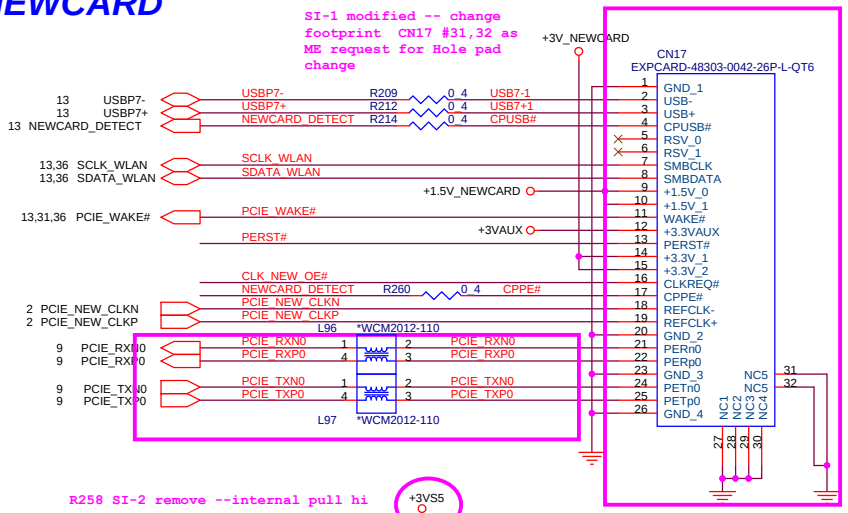


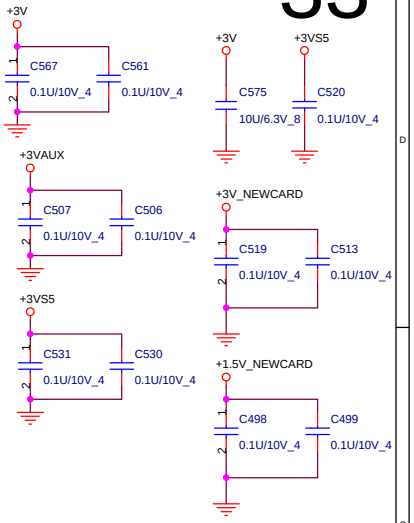
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

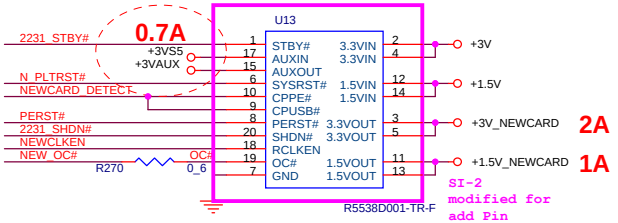
33

SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change





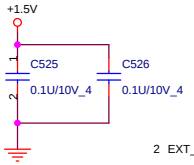
R258 SI-2 remove --internal pull hi



SI-2 modified for add Pin 21~25 as U25 Thermal pad tied to Gnd

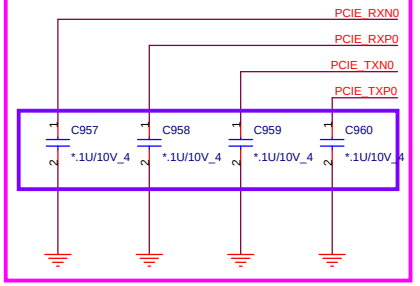
Del R790, R791, R792, R793 for RF on PV

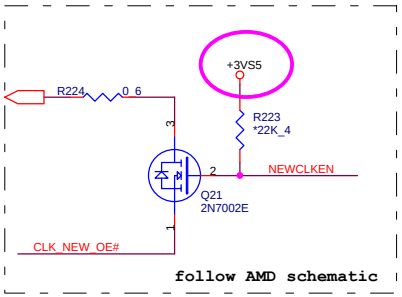
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

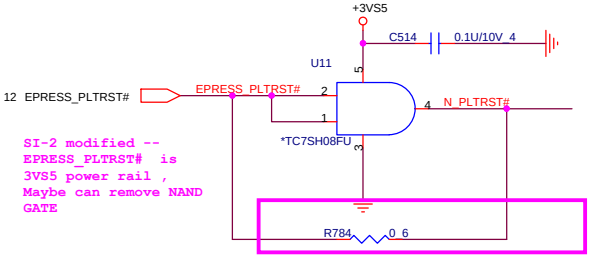


SI-2

For HP request to reserve

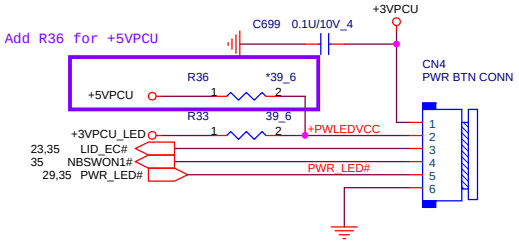






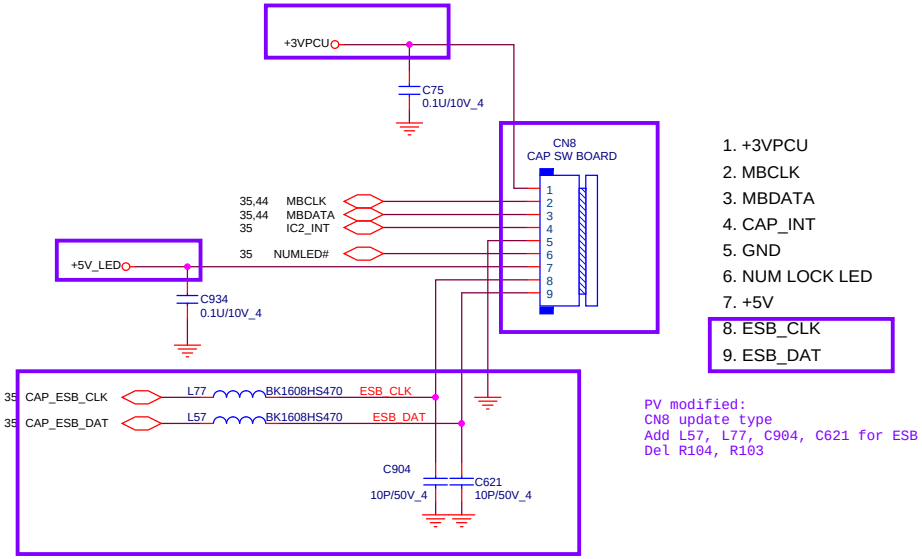
SI-2 modified -- EPRESS_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

POWER BUTTON CONNECT



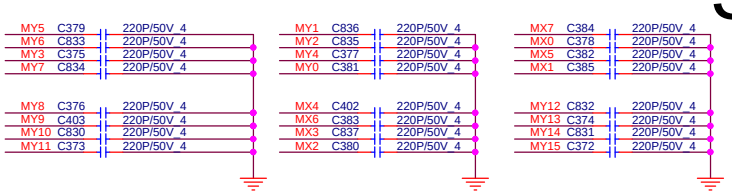
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

CAP SW CONNECT



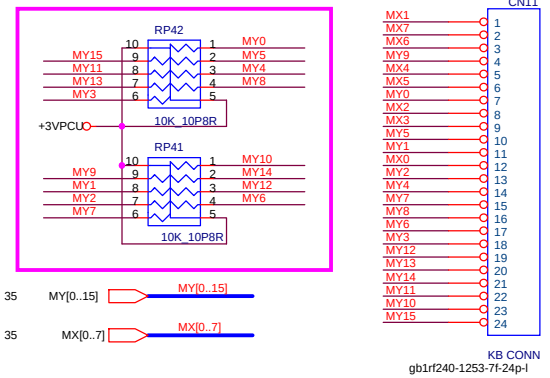
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103



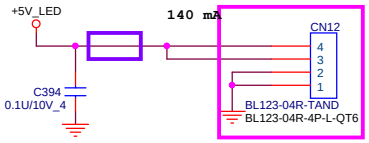
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



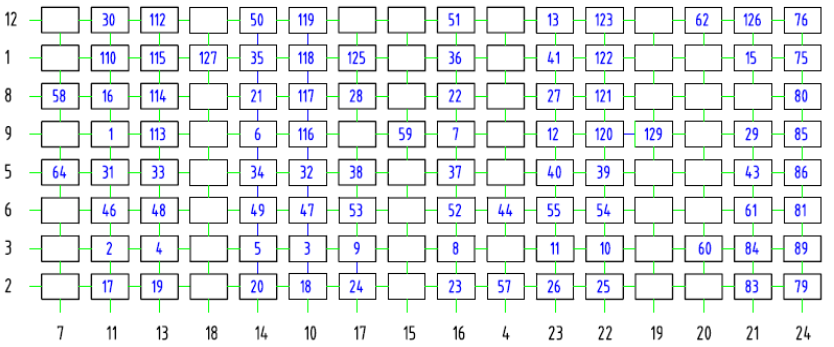
Del R770 on PV

SI-2 Modified 12/27



1.LEDVCC
2.LEDVCC
3. NC
4. GND

SI-2 Modified



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

Date: Tuesday, February 19, 2008 Sheet 34 of 45

Change U9 layout footprint
to LQFP128-16X16-4-AA1

U9

KB3926

For KB3926 C version

SI-2 for fix cpu vcore

SI-2 Modified for hp request

Del R249 on PV

Battery charge/discharge
Cap button

VGA thermal
system thermal

Pin 17 (GPIO0B) ==> assigned for ESB_CLK / Pull high 4.7K
Pin 18 (GPIO0C) ==> assigned for ESB_DAT / Pull high 4.7K

LAN_RESET# move to Pin 25
pin 18 (SWI#1) move to Pin 31

reserved for H/W CIR

Del R256 for TP on PV

SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

change D11 type for PV

UMA BOM missing

64.9K -->65W
33.7K -->90W

SI-2 Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

SI-2 modified for avoid AD-_ID noise

SB internal pull Hi 10k to 3v_s5

Change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

close conn

TOUCH PAD CONNECTOR

Del L86 on PV

25 mils

PCB footprint
BL121-12R-12P-L-QT6

PA

Update SW2, SW4, SW6 P/N on PV

TOUCH PAD ON/OFF

TOUCH PAD L/R

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

SST	AKE5GFK0Z09	1M byte SPI BIOS
WINBOND	AKE3GFP0N08	
PME	AKE3GZP0500	
EON	AKE3GZP0Q00	

CS36492FB17	RES CHIP 64.9K 1/16W +-1%(0402)
CS33322FB13	RES CHIP 33.2K 1/16W +-1% (0402)

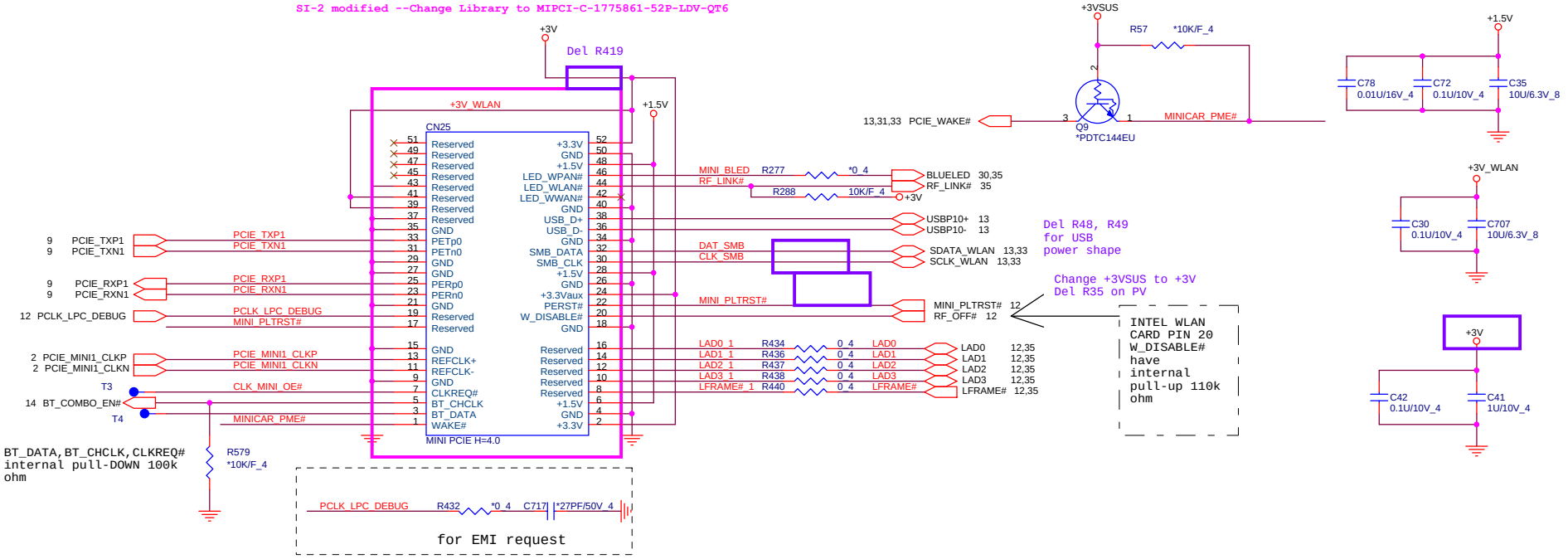
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

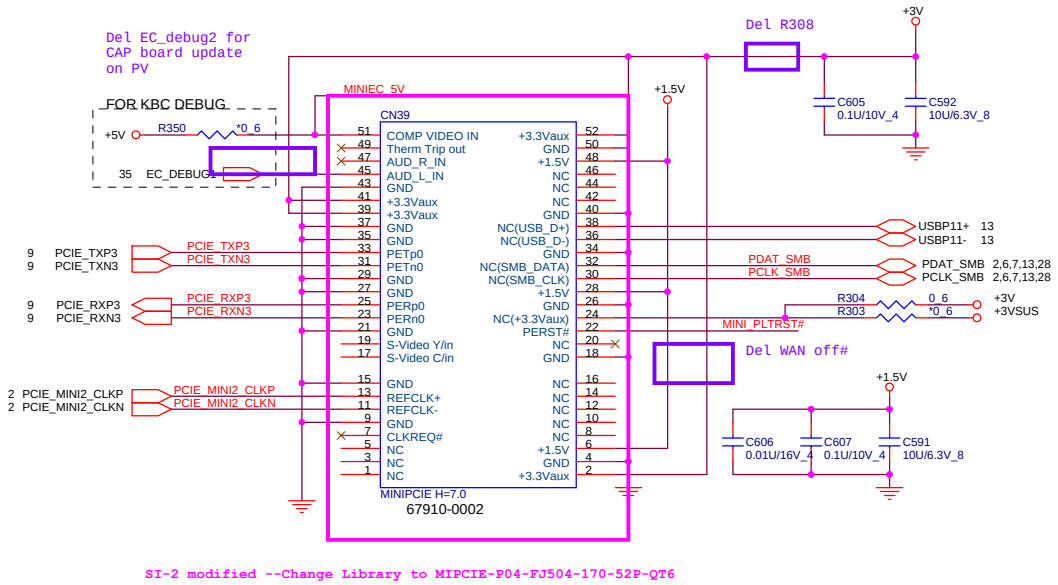
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Tuesday, February 19, 2008 | Sheet 35 of 45

Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 TV tuner card

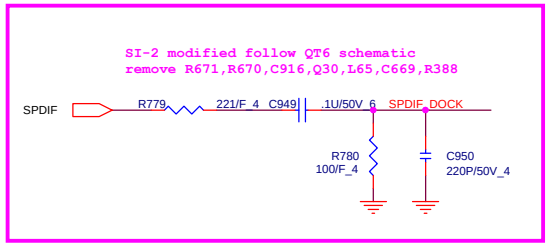


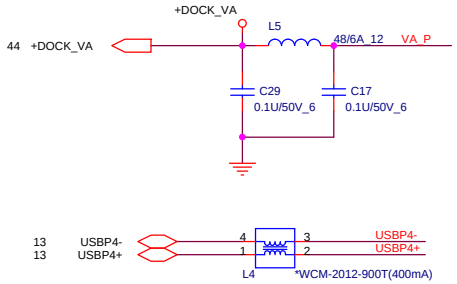
SI-2 modified --Change Library to MIPCIE-P04-FJ504-170-52P-QT6

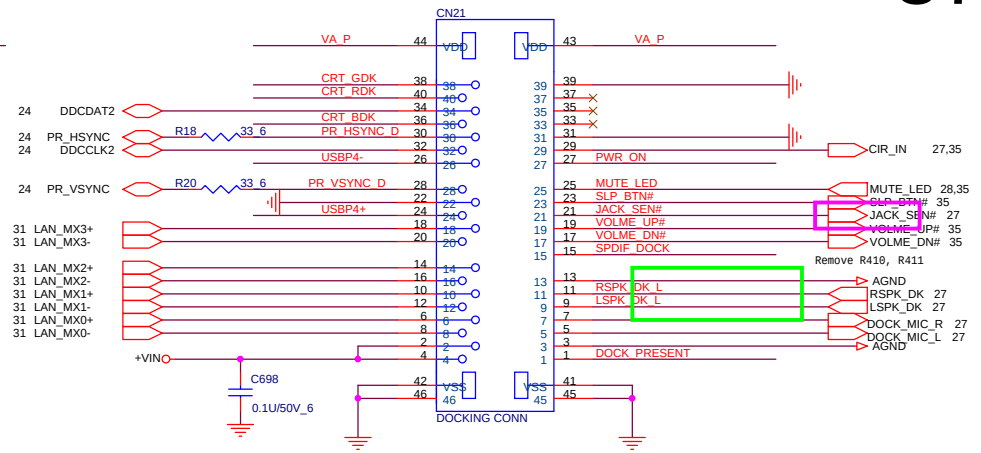
NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size: Custom Document Number: Mini CARD X 3	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 36 of 45

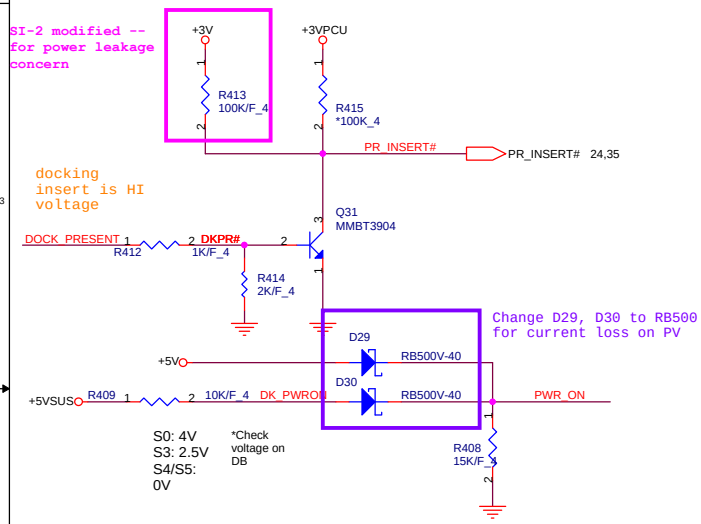
CABLE DOCK

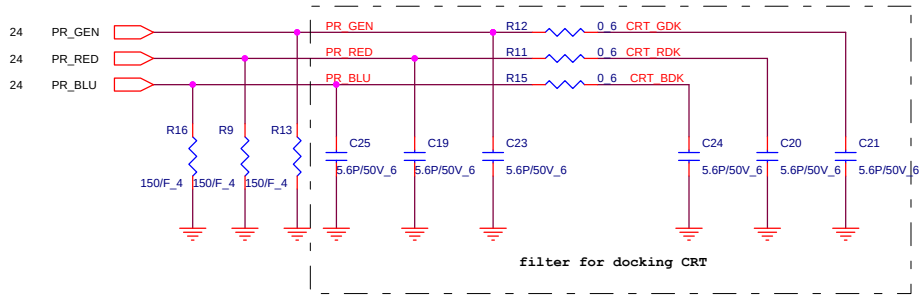
support 6A 200mils
CX000480005



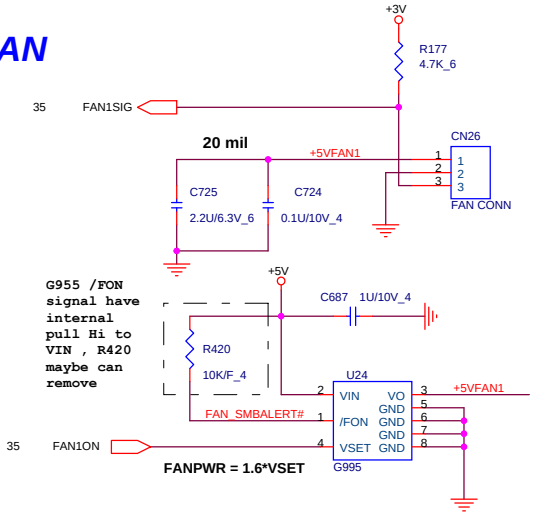


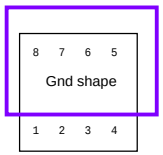




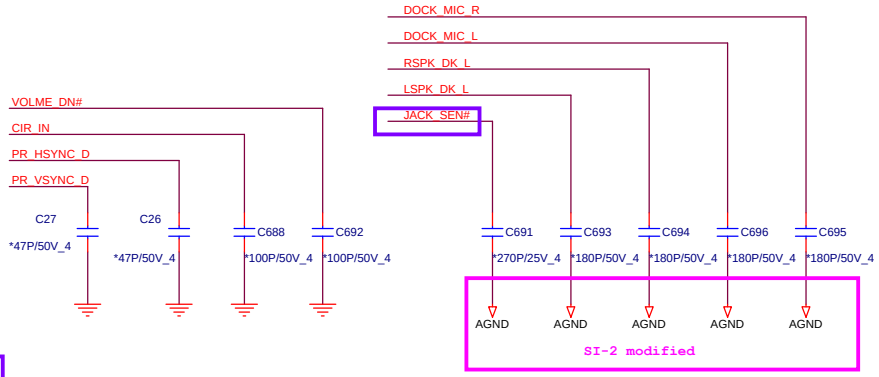


CPU FAN





G995 layout notice



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

NB5/RD5

Date: Tuesday, February 19, 2008 | Sheet 37 of 45

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,18,20,23,24,25,26,27,28,29,30,31,33,35,36,37,39,43

+5VPCU 27,28,34,35,39,40,41,42,43
+3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
+3VSUS 13,25,30,36,39,41,43
+3VS5 5,7,12,13,14,15,16,23,26,33,43
+5VSUS 23,30,35,37,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

Rds(on) 15m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Del PR159 for TP on PV

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

SI-1 Modified -ECAP6_3X6_1-7_2-QT8

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

+5VSUS
4.5A
S0-S3

+LANVCC
0.27A

5,7,12,13,14,15,16,23,26,33,43 +3VS5
+3VSUS 13,25,30,36,39,41,43
SUSD 43
43 S5_OND
43 LAN_ON
+3VLANVCC 31,32,43
+3V 20,23,35,39,41,42
HWPG
PGOOD1
PGOOD2
43 MAIND
43 SUSD
5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43 +5V
+5VSUS 23,30,35,37,43
5,44 SYS_SHDN#

For EMI-SI

PU8 ISL6237

PQ58 SI4800BDY
PQ53 SI4800BDY
PQ54 FDS6690AS
PQ59 FDS6690AS
PQ34 SI4800BDY
PQ24 SI4800BDY
PQ23 SI4800BDY
PQ35 AP4228
PQ51 SI3456

PD18 CHN217PT
PD17 CHN217PT

PL12 2.5uH/7.5A_10
PL13 2.5uH/7.5A_10

PR160 *47_6
PR162 150K/F_4
PR163 390K_4
PR164 0_8
PR158 0_4
PR217 309K/F_4
PR153 309K/F_4
PR214 *2.2_6
PR208 *2.2_6
PR155 *0_4
PR156 0_4
PR157 0_4
PR154 *0_4
PR183 0_4
PR152 0_4
PR147 0_6
PR161 100K_4
PR151 0_4
PR150 0_4
PR149 1_6
PR148 1_6
PR216 *SHORT-1A

PC174 *100P/50VA_6
PC161 *100P/50VA_6

PC105 *0.1U/10VC_4
PC104 *0.1U/10VC_4
PC106 0.1U/10VC_4
PC107 1U/10VC_4
PC108 *1U/10VC_4
PC180 1U/10VC_4
PC182 0.1U/10VC_4
PC103 0.1U/50VB_6
PC102 0.1U/50VB_6
PC101 0.1U/50VB_6
PC100 0.1U/50VB_6
PC97 0.1U/50VB_6
PC96 2.2U/50VB_8
PC109 0.1U/50VB_6
PC110 4.7U/63VC_6
PC157 10U/25VD_1206
PC76 0.1U/50VB_6
PC79 2200P/50VB_4
PC94 2200P/50VB_4
PC93 0.1U/50VB_6
PC98 10U/25VD_1206
PC177 330U/6.3V_ESR25_6X5.8
PC179 0.1U/10VC_4
PC181 330U/6.3V_ESR25_6X5.8
PC195 0.1U/10VC_4
PC194 0.1U/10VC_4

6236AGND
6237ON1
6237ON2
6237ONLDO
6237VIN
6236FB1
5V_DH
5V_LX
5V_DL
3V_LX
3V_DH
REFIN2
PGOOD1
PGOOD2
5VBST1
3VBST2
5VBST2R
3VBST2R
+VIN_6237
+5VAL
+5V_VCC1
+12V_ALWP
+5V_ALWP
+12VALW
+VIN
+5VPCU
+3VPCU
+5V
+3V
+3VS5
+3VSUS
+3VLANVCC
+5VSUS
MAIND
SUSD
S5_OND
LAN_ON
HWPG

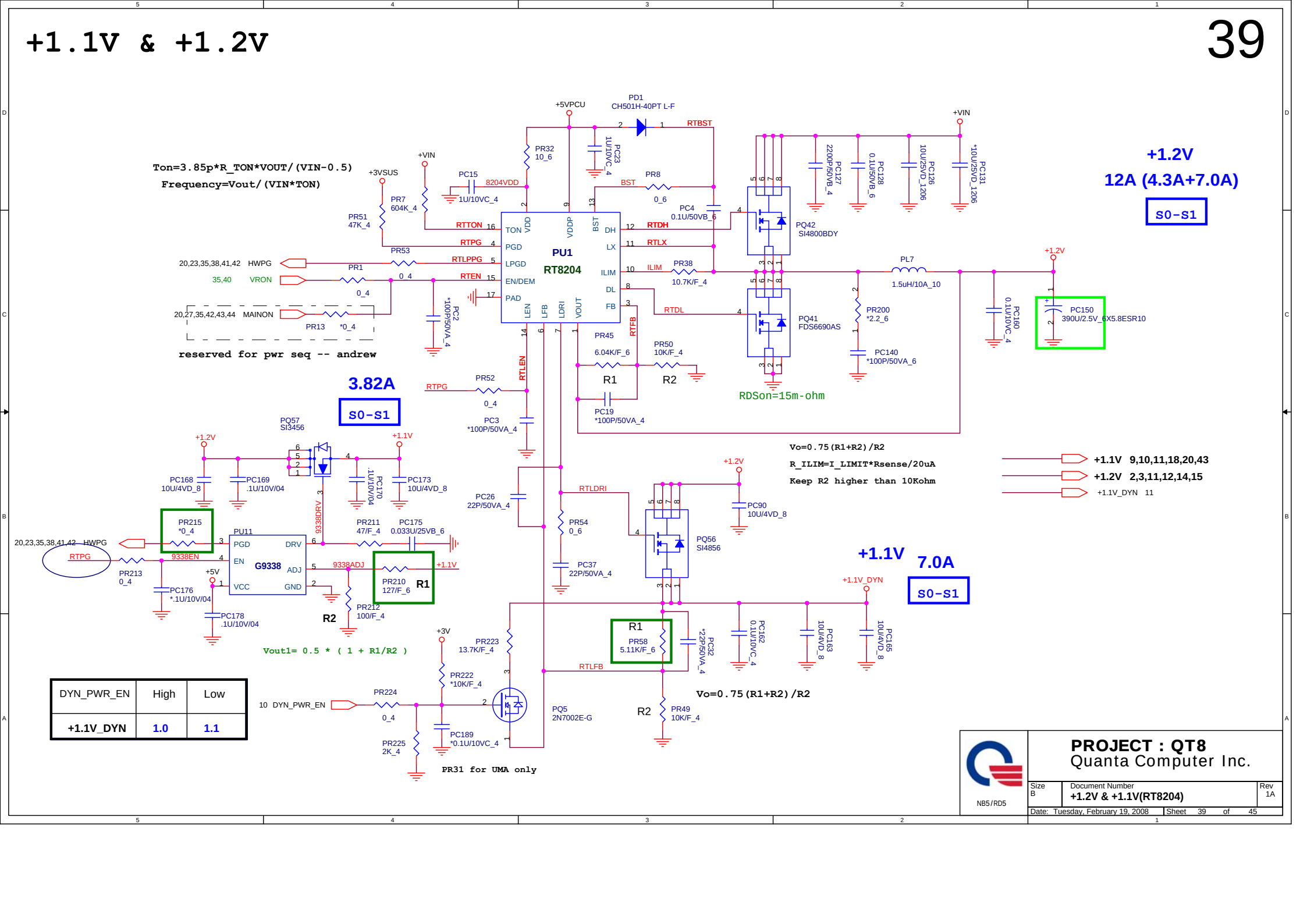
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V(ISL6237)	1A

Date: Tuesday, February 19, 2008 Sheet 38 of 45

+1.1V & +1.2V

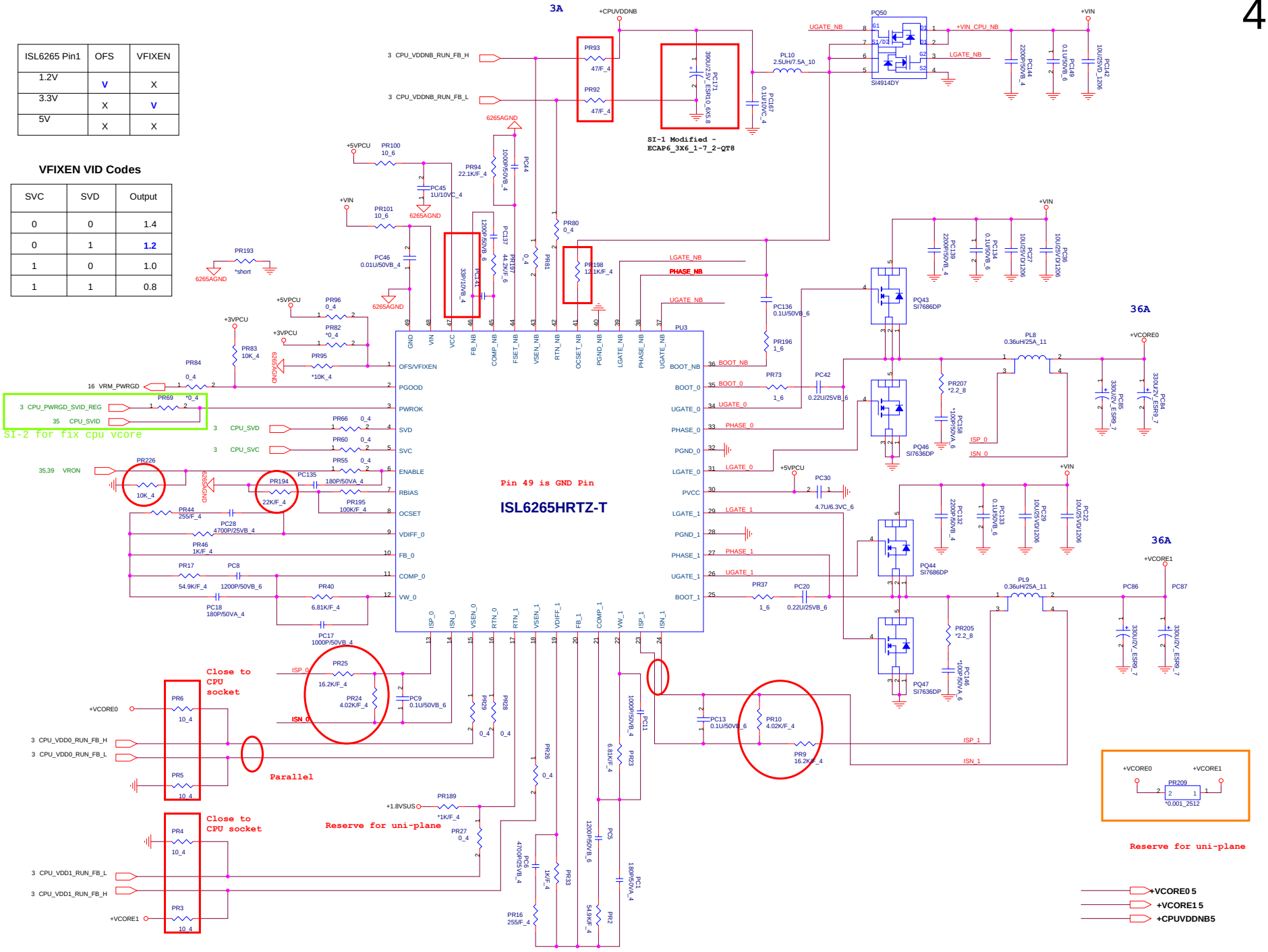


DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

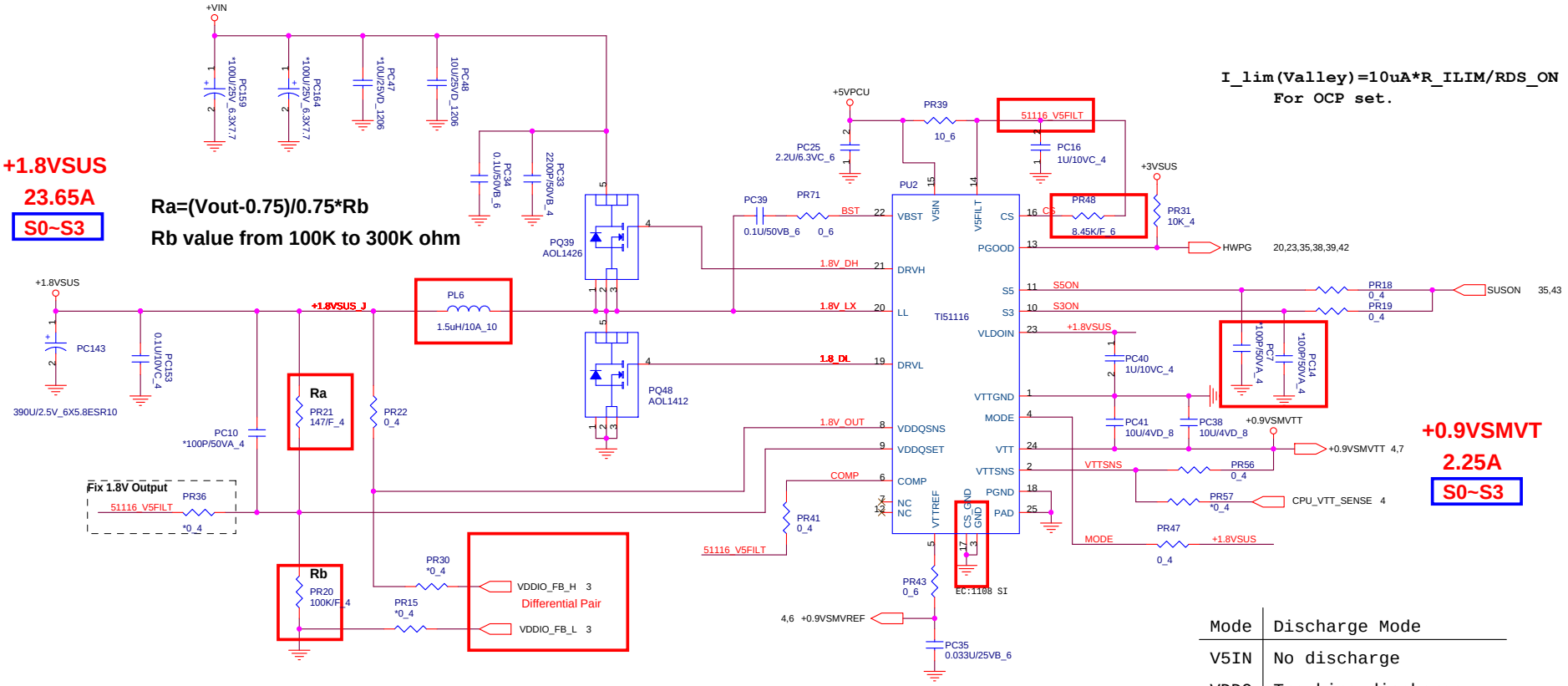


+2.5V 3
+1.8VSUS 3,4,5,6,7,40,42,43

+1.8VSUS
23.65A
S0~S3

Ra=(Vout-0.75)/0.75*Rb
Rb value from 100K to 300K ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

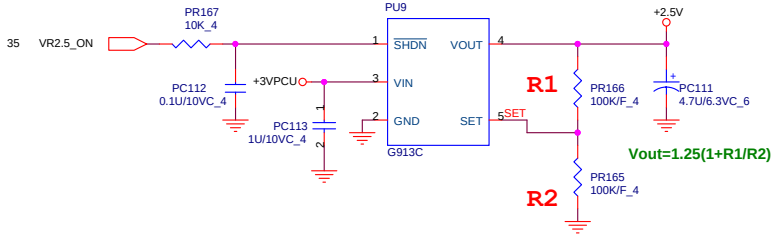


+0.9VSMVT
2.25A
S0~S3

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

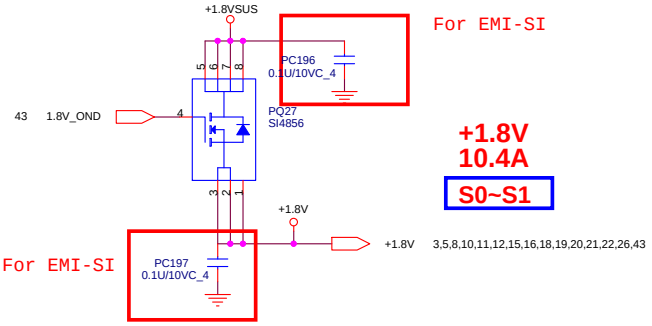
+2.5V
0.25A
S0~S1

Close to CPU
SI power



V_TRIP(mV)=R_TRIP(Kohm)*10(uA)
I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V



+1.8V
10.4A
S0~S1

Discrete:SI4856
UMA:SI4800

PROJECT : QT8
Quanta Computer Inc.

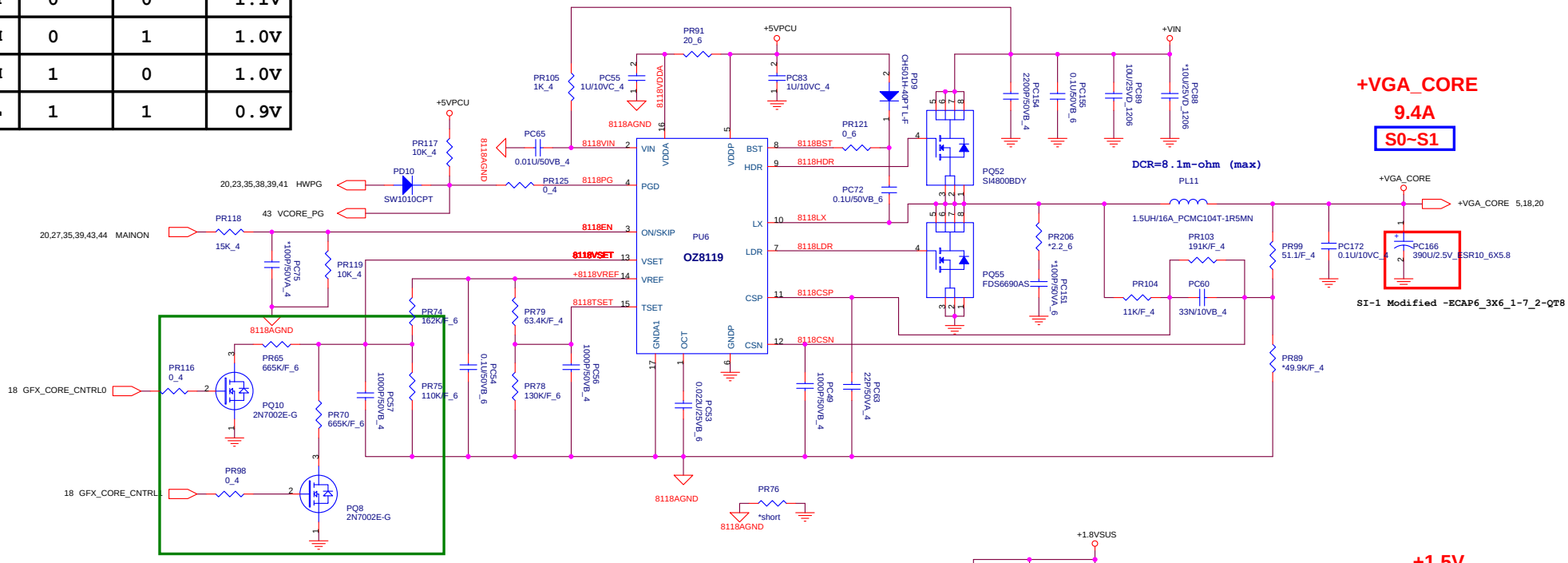
NB5/RD5

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A
Date: Tuesday, February 19, 2008	Sheet 41 of 45	

ATI M82-SE

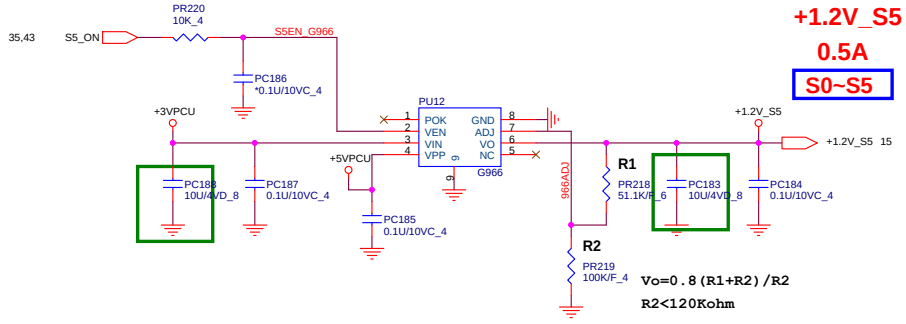
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

+VGA_CORE5,18,20
+1.2V_S5 15
+1.5V 33,36



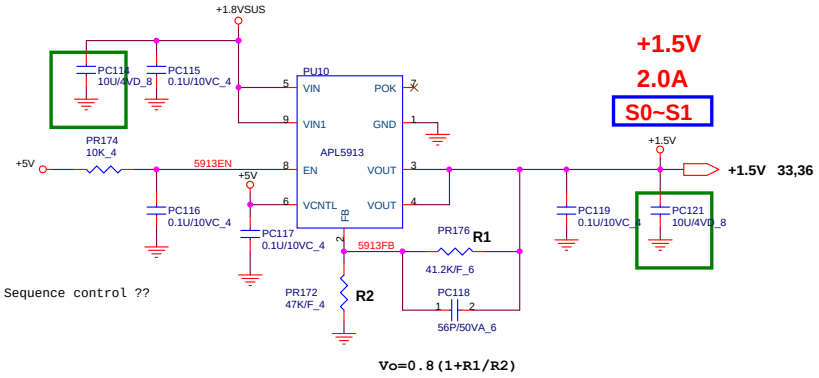
DCR=8.1m-ohm (max)

+VGA_CORE
9.4A
S0~S1



+1.2V_S5
0.5A
S0~S5

Vo=0.8(R1+R2)/R2
R2<120Kohm



+1.5V
2.0A
S0~S1

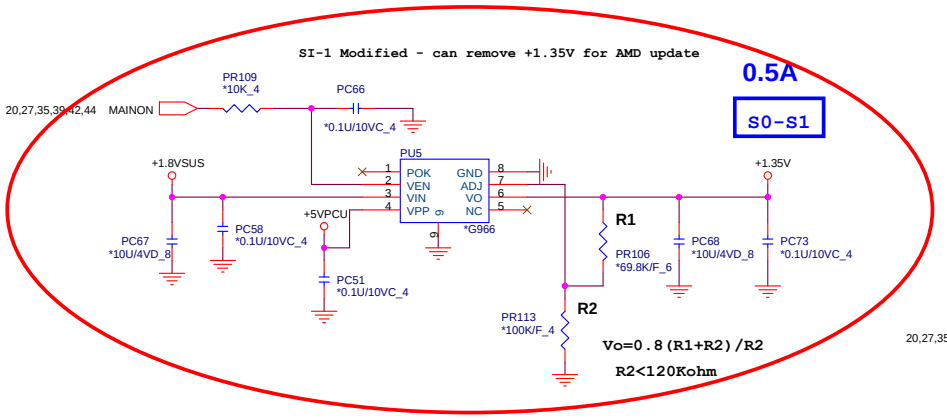
Sequence control ??

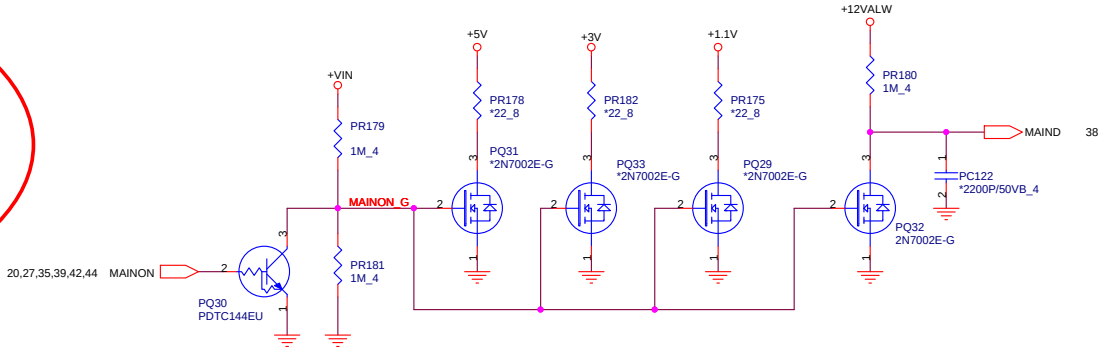
Vo=0.8(1+R1/R2)

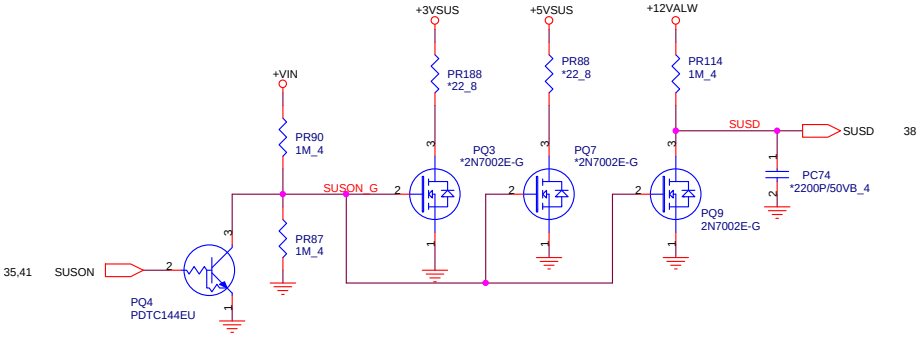
PROJECT : QT8
Quanta Computer Inc.

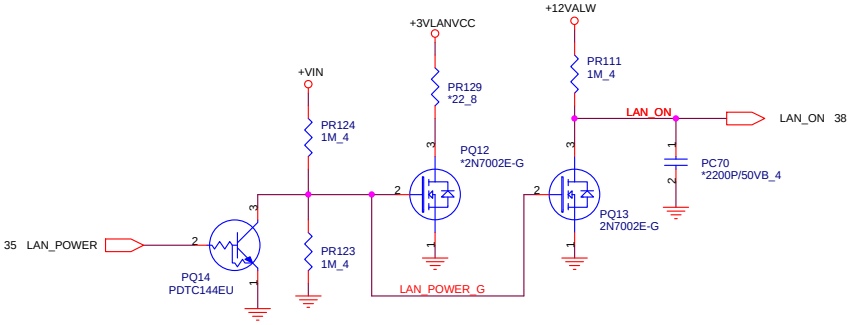
Size	Document Number	Rev
Custom	VGA PWR OZ8118/1.2V_S5/+1.5	1A
Date: Tuesday, February 19, 2008	Sheet 42 of 45	

N85/RD5

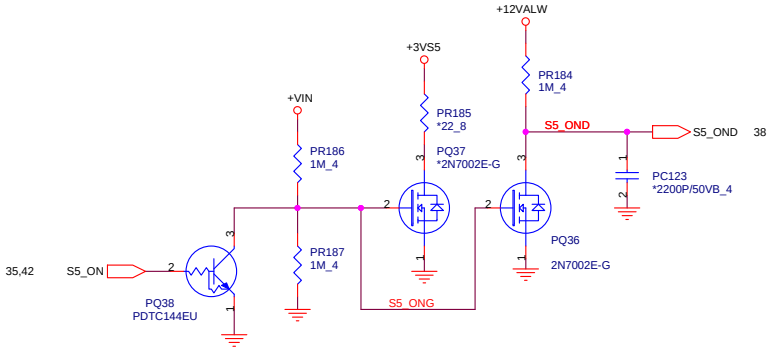


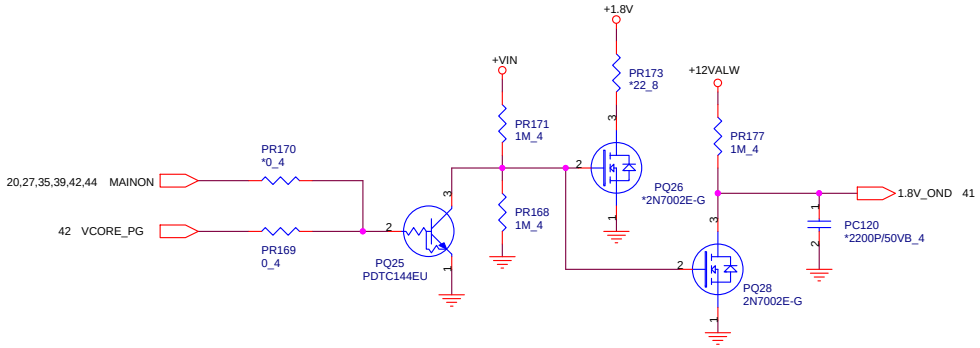






For Discrete Only





PROJECT : QT8 Quanta Computer Inc.		
Size: Custom	Document Number: DISCHARGE	Rev: 1A
N85/RD5	Date: Tuesday, February 19, 2008	Sheet 43 of 45

TOP DC_JACK
65W/90W

ISL6251A

SI-2 modified -- EMI

Close to AC soft start MOSFET

ONLY for 3S battery pack

Setting the Vin min to 11.42V For ACSET 1.26V

Setting the Vin min to 15.88V For EN = 1.06V

VADJ = VERF >> 4.2V +5% Float >> 4.2V GND >> 4.2 -5%

V ACLIM = VREF * (Rhi // 152K) / (Rhi // 152K + Rlow// 152K) Input curretn = 2.9A (71.5K , 10K) (0.05/Vref * Vaclim + 0.05) / Rsense

Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)

Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)

ADP TYPE	PR72 Value	P/N
65W	102K/F	CS41022FB19
90W	7.5K/F	CS27502FB11

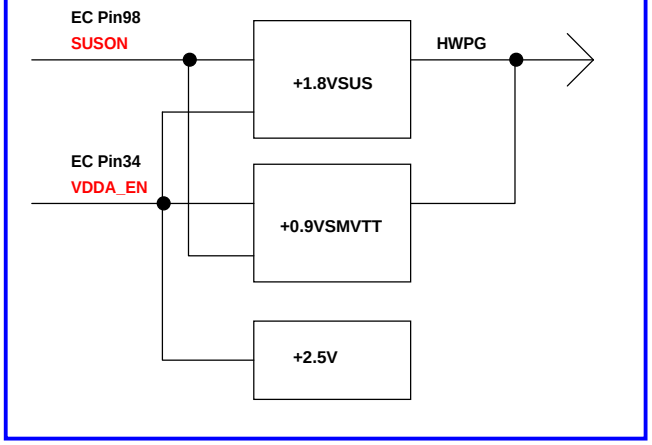
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251)	1A

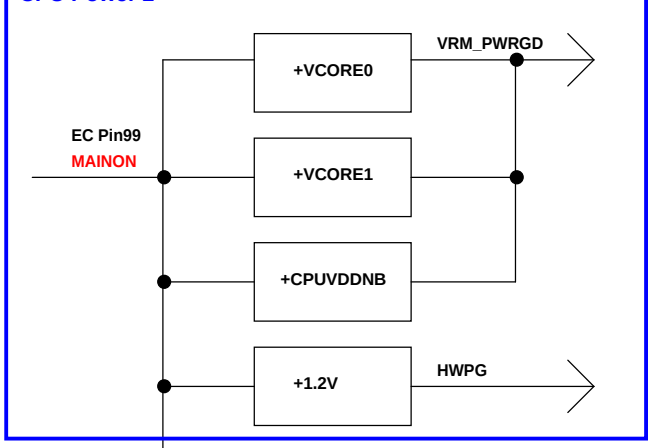
Date: Tuesday, February 19, 2008 Sheet 44 of 45

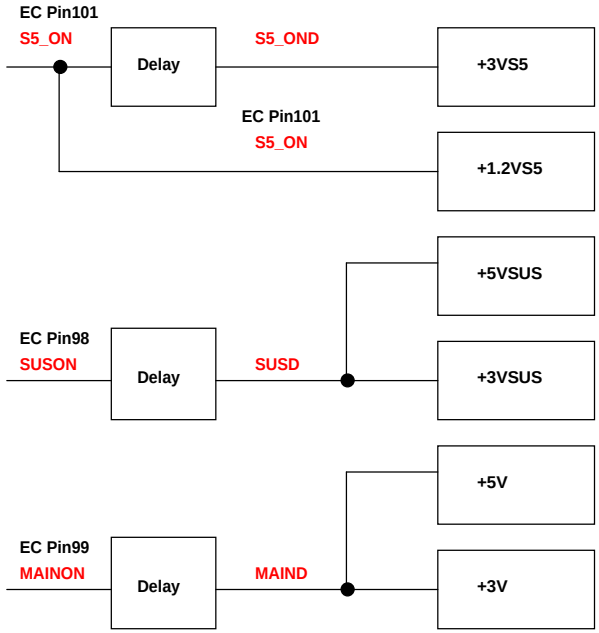
NB5/RD5

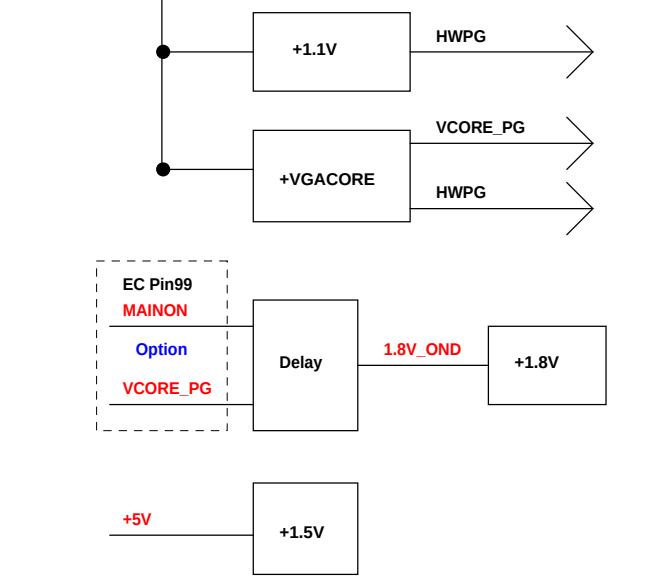
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

Date: Tuesday, February 19, 2008 | Sheet 45 of 45