

Compal confidential

JBK00 LA-4091P Schematics Document

Mobile AMD S1G2 CPU with ATI
RS780M & SB700 core logic

2007-10-30

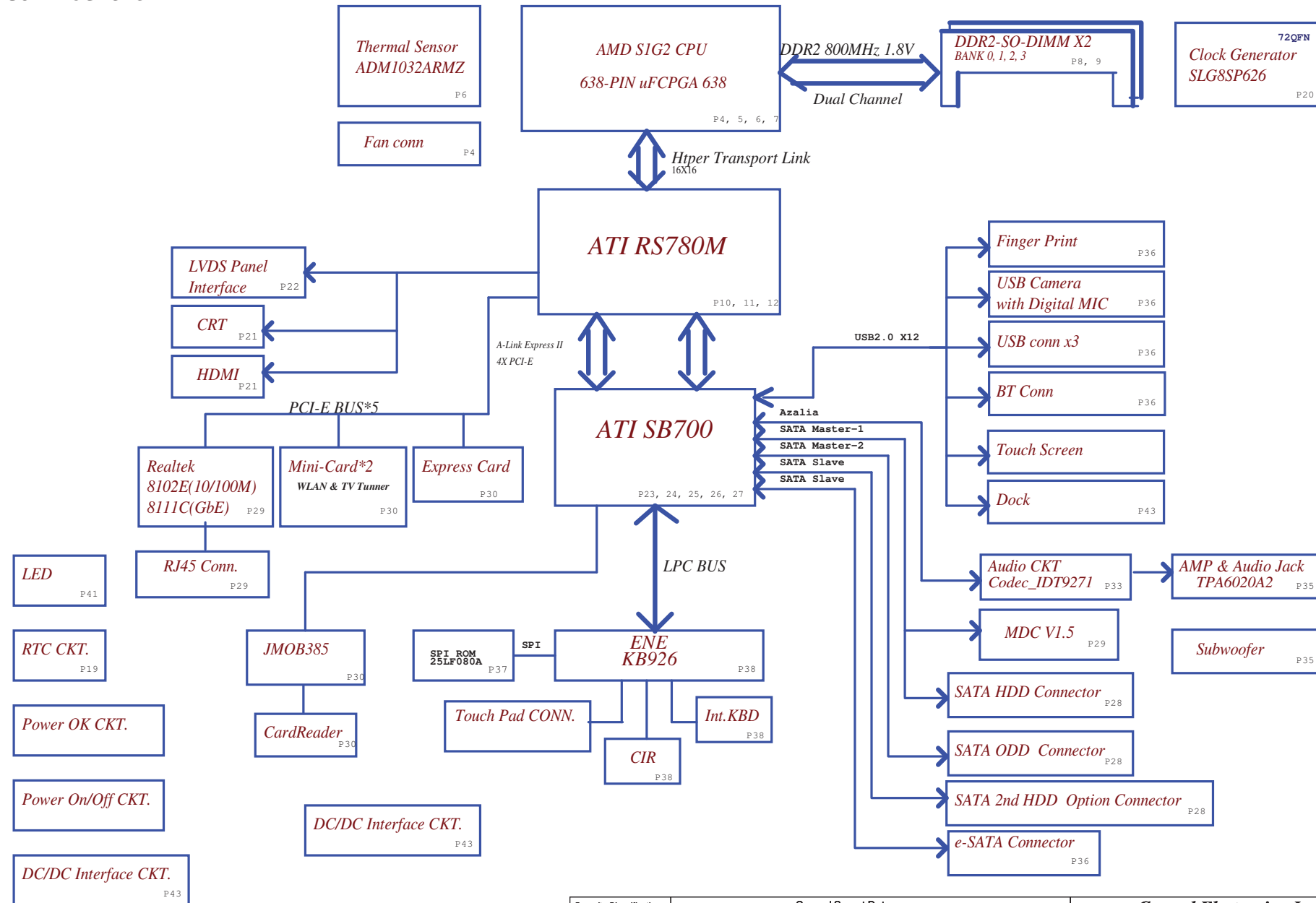
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Consumer AMD UMA 17"



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Voltage Rails ○ MEANS ON X MEANS OFF

power plane					+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
State	+B +3VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V		
S0	○	○	○	○	
S1	○	○	○	○	
S3	○	○	○	X	
S5 S4/AC	○	○	X	X	
S5 S4/ Battery only	○	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

 Layout Notes

UMA@ : means for RS780M.

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM 1 / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK	RS780M	X	X	X	X	X	X	X	V	X	X
I2C_DATA	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	X	X
DDC_CLK1	RS780M	X	X	X	X	X	X	X	X	X	X
DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0	SB700	X	X	X	X	V	V	X	X	X	V
SDA0	SB700	X	X	X	X	X	X	V	X	X	X
SCL1	SB700	X	X	X	X	X	X	V	X	X	X
SDA1	SB700	X	X	X	X	X	X	X	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X

EC SM Bus1 address

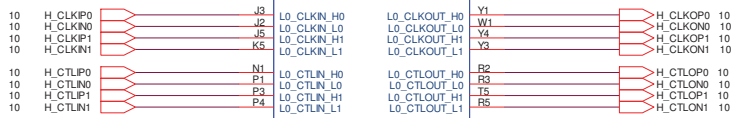
EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	AD1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b			
CPU SIC interface	98H	1001 100X b			

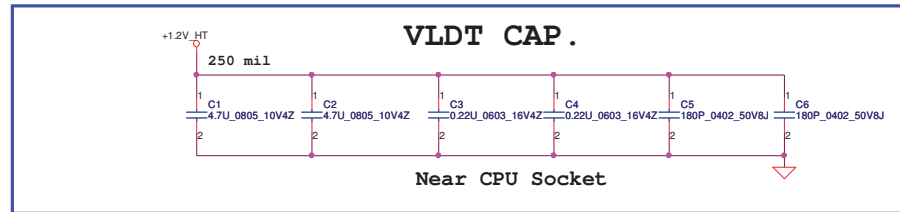
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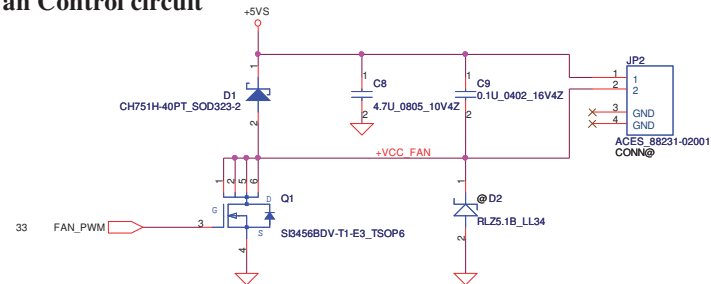
H_CADIP0	E3	L0_CADN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIP1	E2	L0_CADN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP2	E1	L0_CADN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIP3	F1	L0_CADN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP4	G3	L0_CADN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIP5	G2	L0_CADN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP6	G1	L0_CADN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIP7	H1	L0_CADN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP8	J1	L0_CADN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIP9	K1	L0_CADN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP10	L3	L0_CADN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIP11	L2	L0_CADN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP12	M1	L0_CADN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIP13	N3	L0_CADN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP14	N2	L0_CADN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIP15	N1	L0_CADN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP16	E5	L0_CADN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIP17	F5	L0_CADN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP18	F3	L0_CADN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIP19	F4	L0_CADN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP20	G5	L0_CADN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIP21	H5	L0_CADN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP22	H3	L0_CADN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIP23	K3	L0_CADN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP24	K4	L0_CADN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIP25	K5	L0_CADN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP26	L5	L0_CADN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIP27	M5	L0_CADN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP28	M3	L0_CADN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIP29	M4	L0_CADN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP30	N5	L0_CADN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIP31	P5	L0_CADN_L15	L0_CADOUT_L15	T3	H_CADON15



CONN@ 6090022100G_B



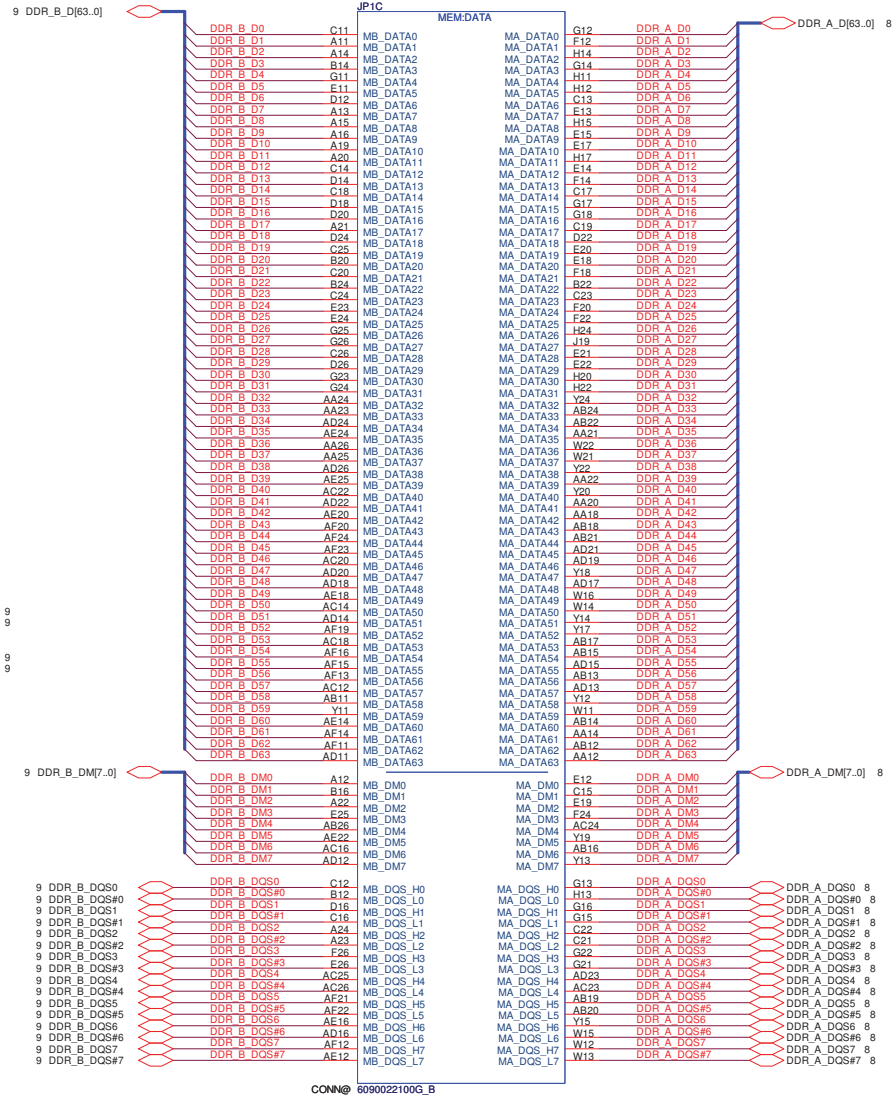
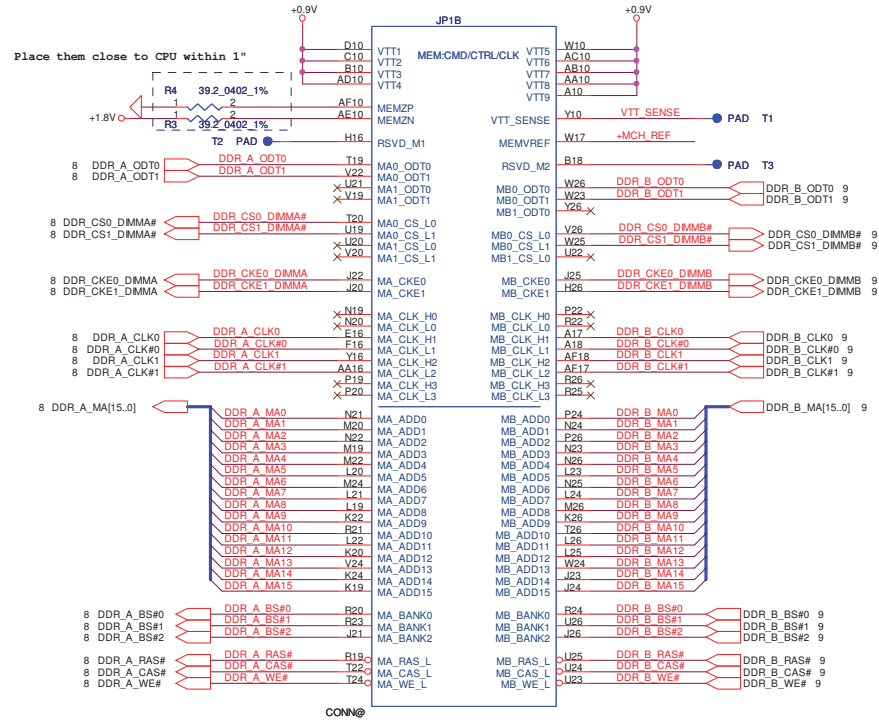
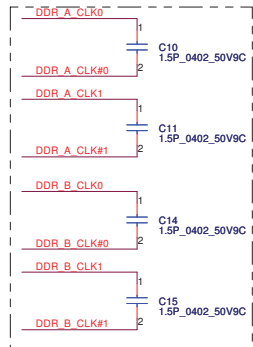
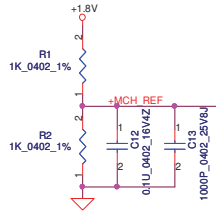
PWM Fan Control circuit



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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

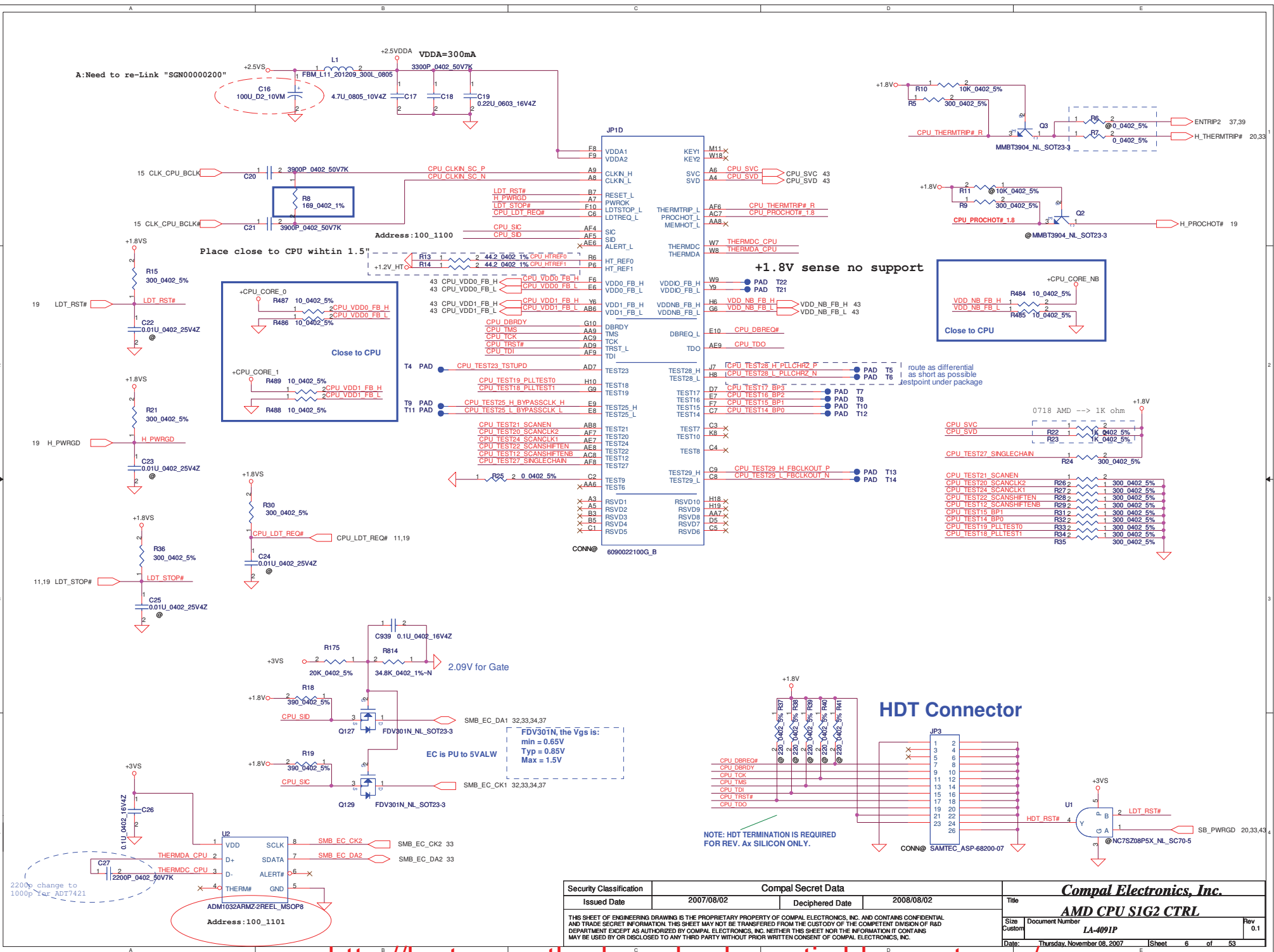


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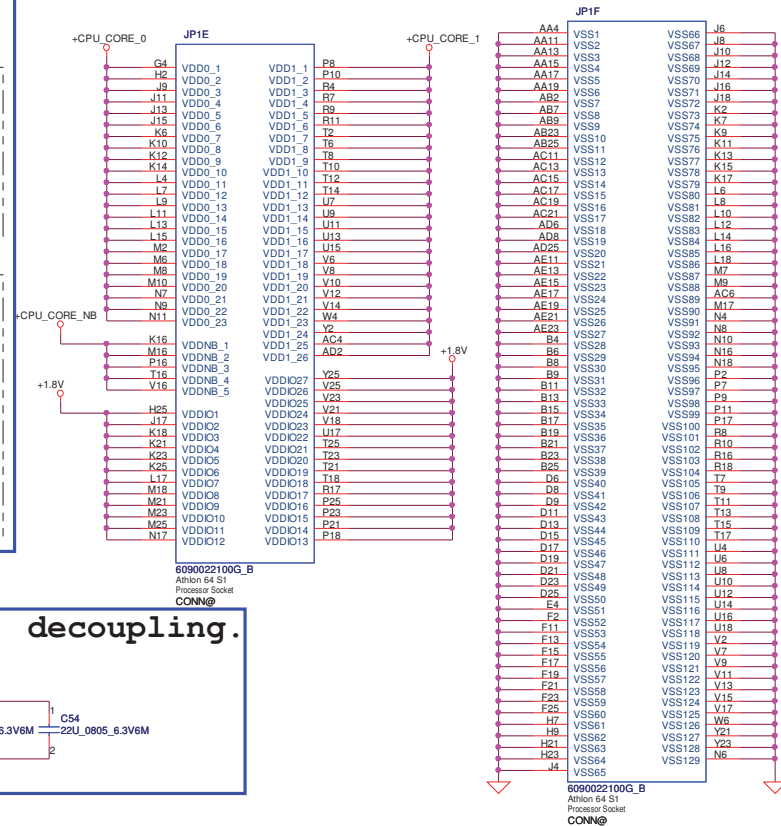
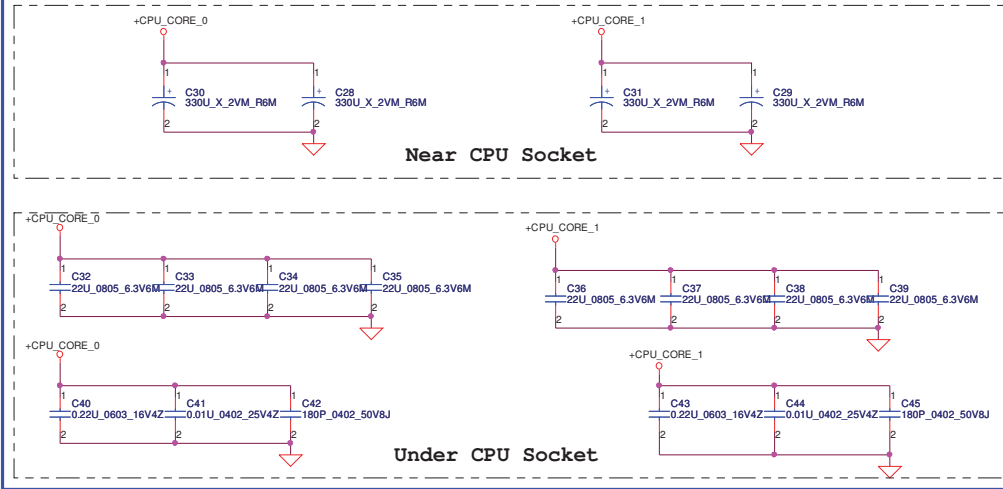
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Title		
AMD CPU S1G2 DDRII I/F		
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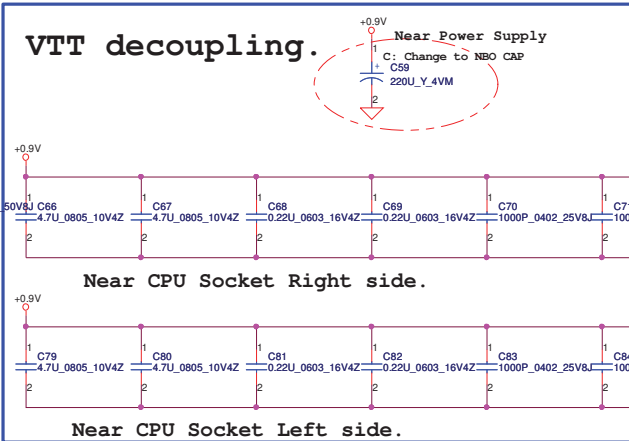
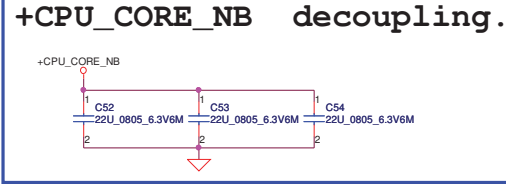
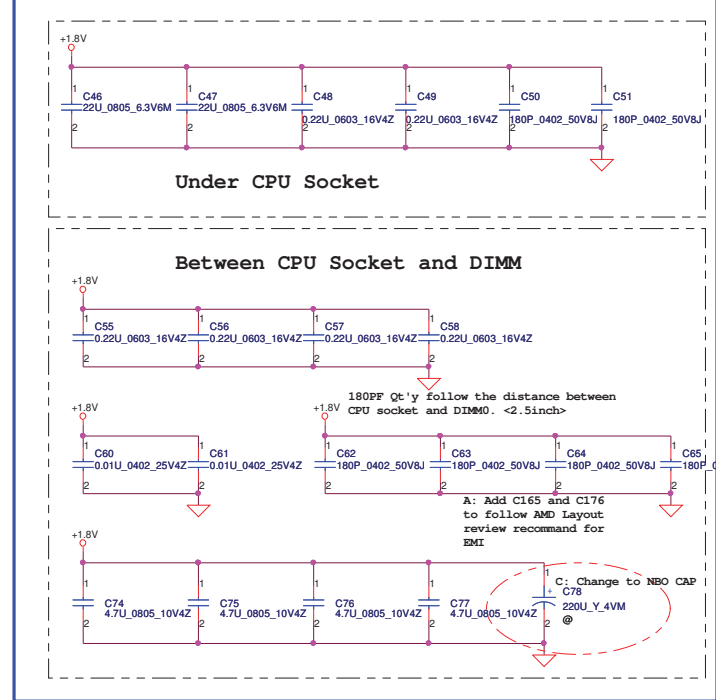


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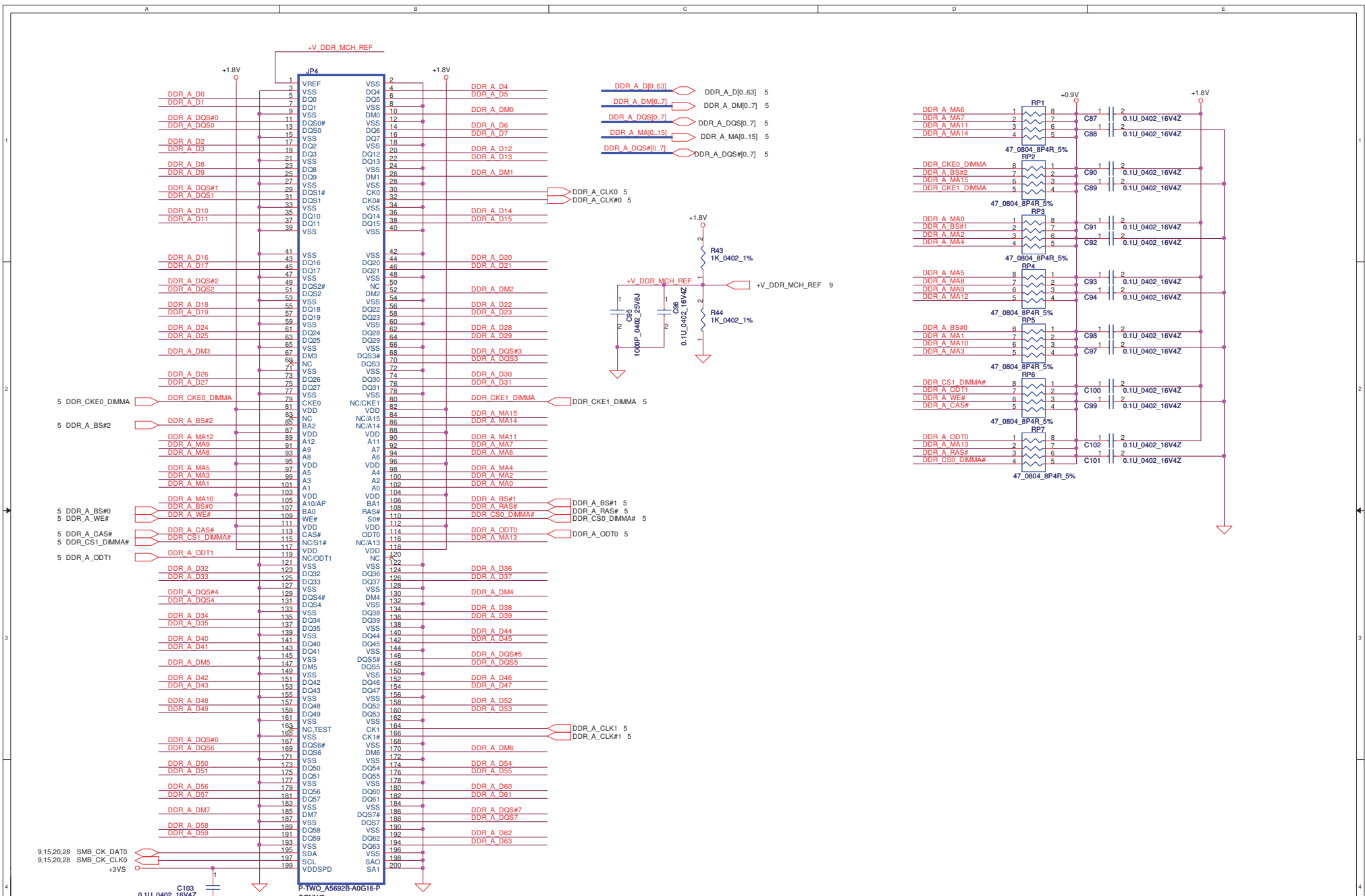
VDD (+CPU_CORE) decoupling.



VDDIO decoupling.

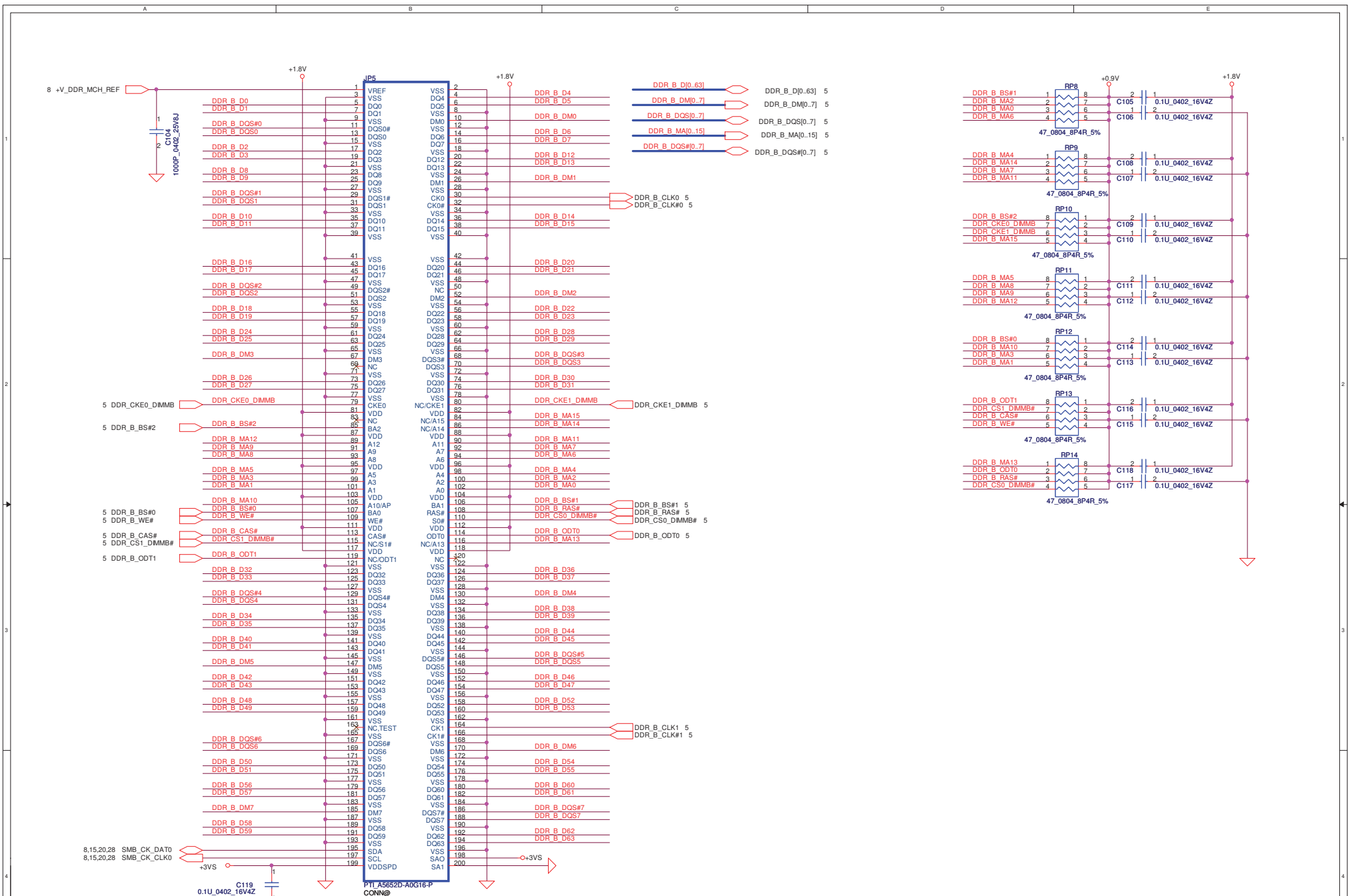


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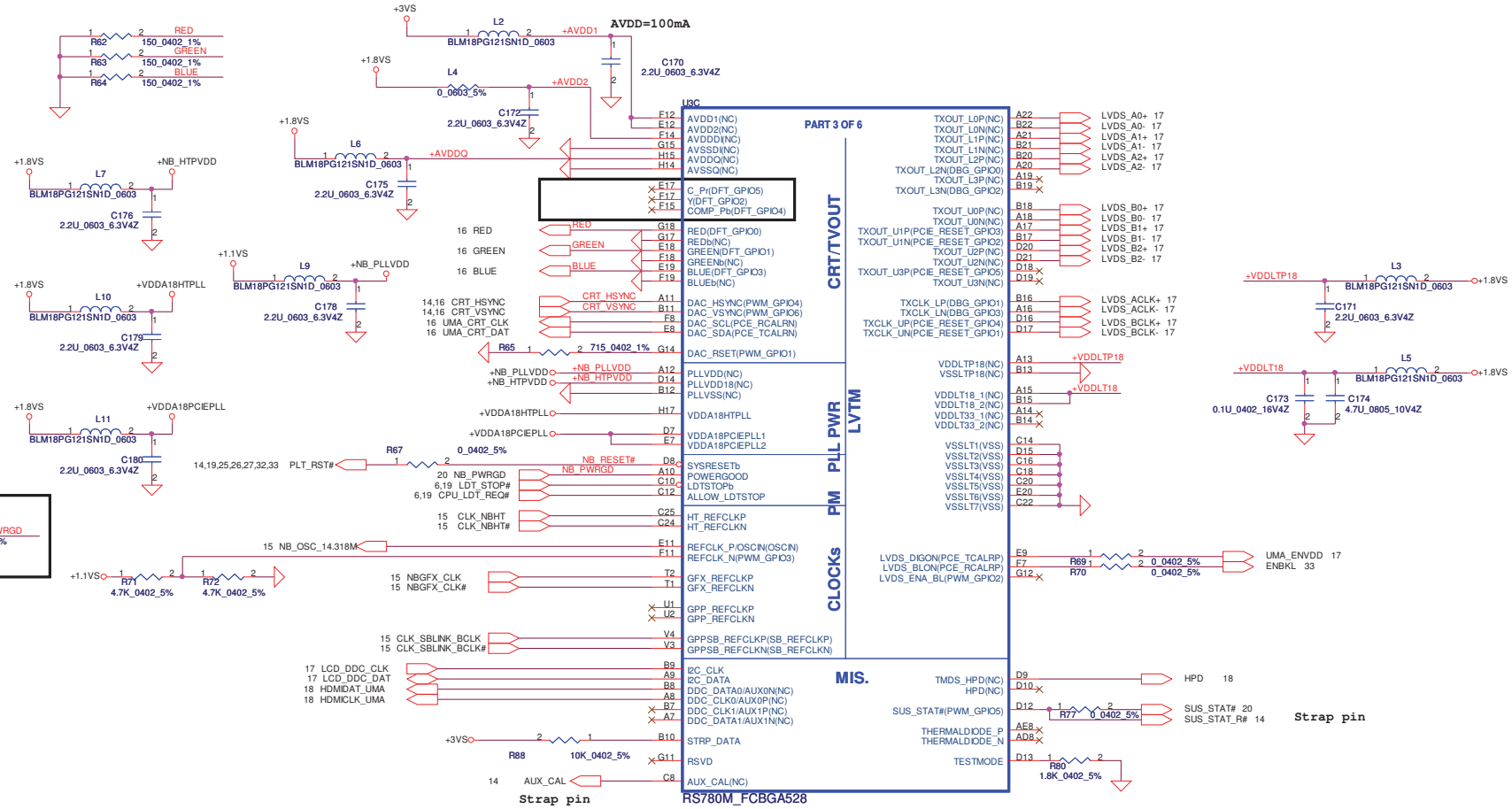
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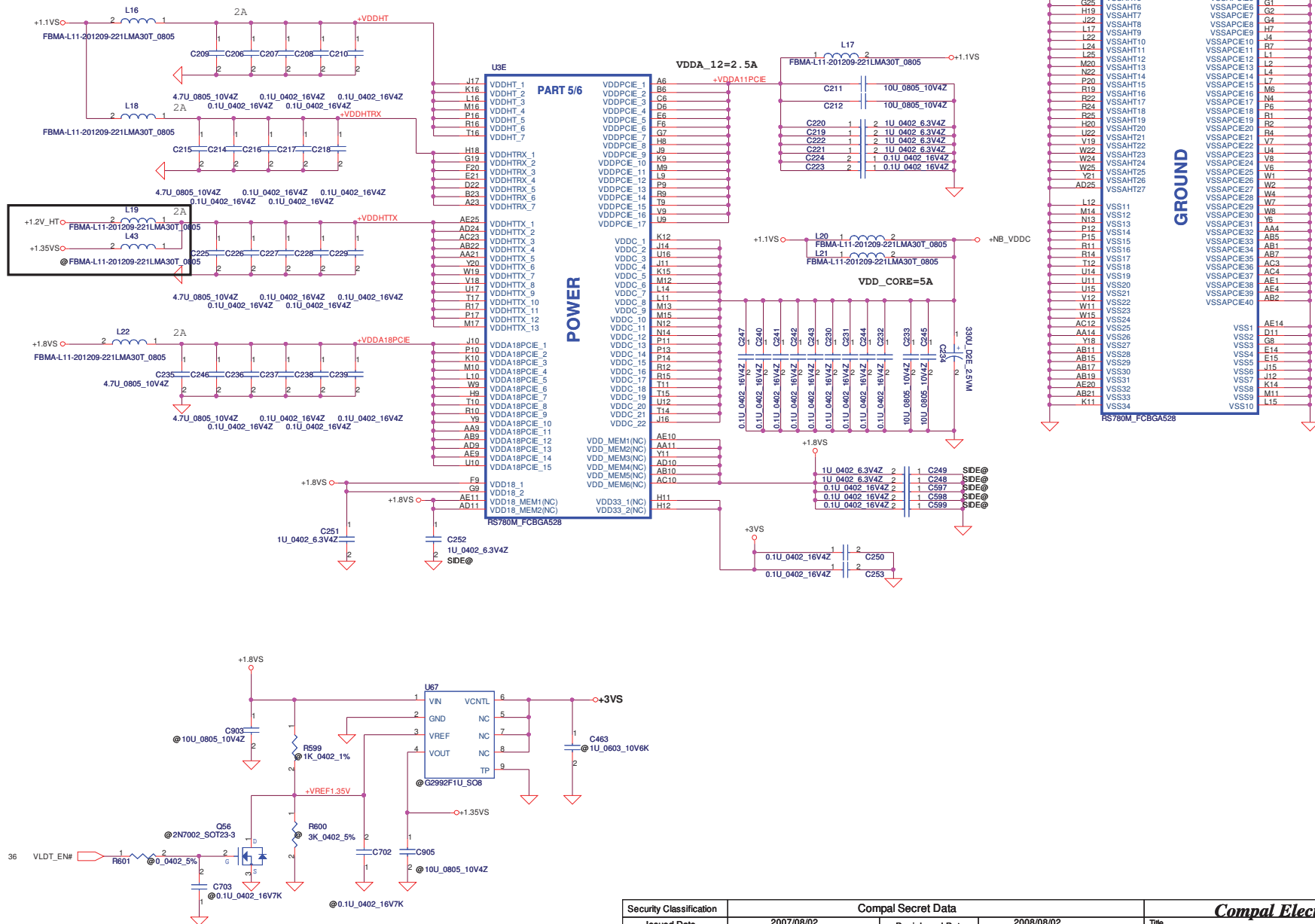
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For SB700 A12 use

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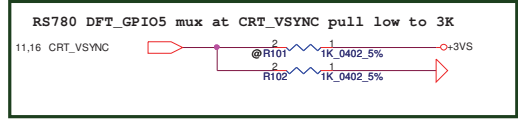
Title			Compal Electronics, Inc.		
Size			RS780 VEDIO/CLK GEN		
Custom	Document Number	Rev			
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Compal Electronics, Inc.		
RS780 PWR/GND		
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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

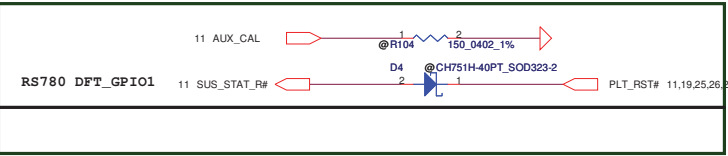
Enables the Test Debug Bus using GPIO.
 1 : Enable (RX780, RS780)
 0 : Disable (RX780, RS780)
 PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

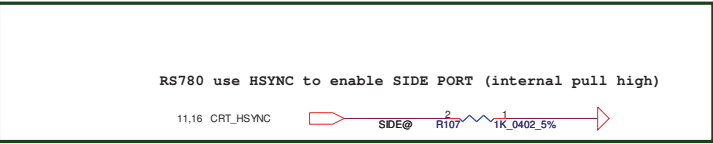
These pin straps are used to configure PCI-E GPP mode.

```
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

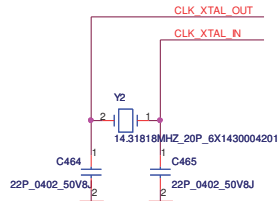
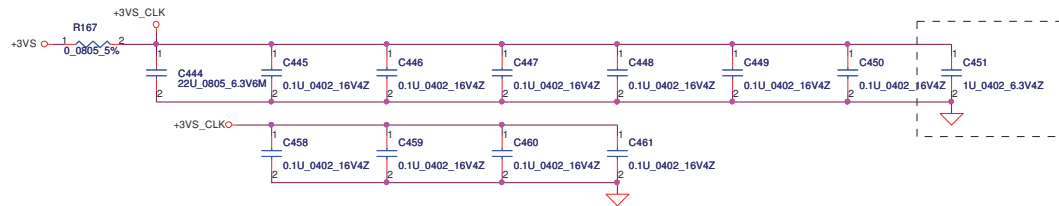
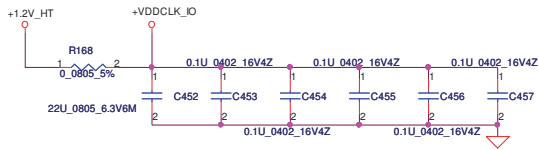


DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

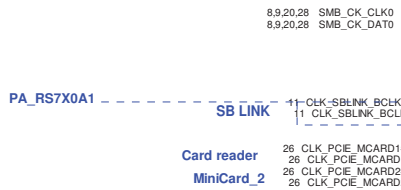
RX780: Enables the Test Debug Bus using PCIE bus
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
 1. Disable (RS780)
 0 : Enable (RS780)

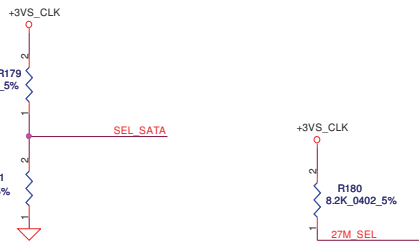
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Routing the trace at least 10mil



Card reader
MiniCard_2

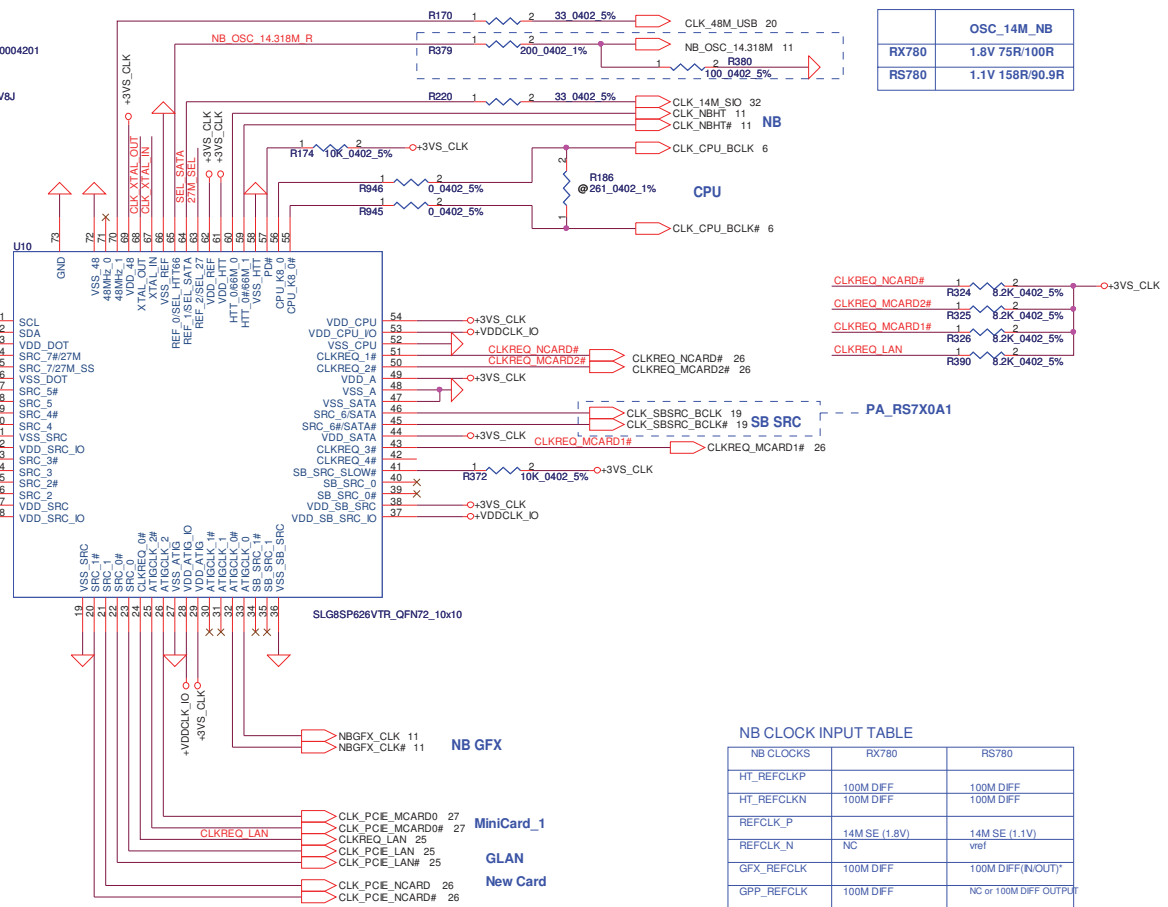


SEL_SATA	1	configure as SATA output
	0	configure as normal SRC(SRC_6) output * default

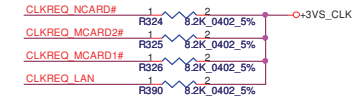
27M_SEL	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output * default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0	configure as differential 100MHz output * default



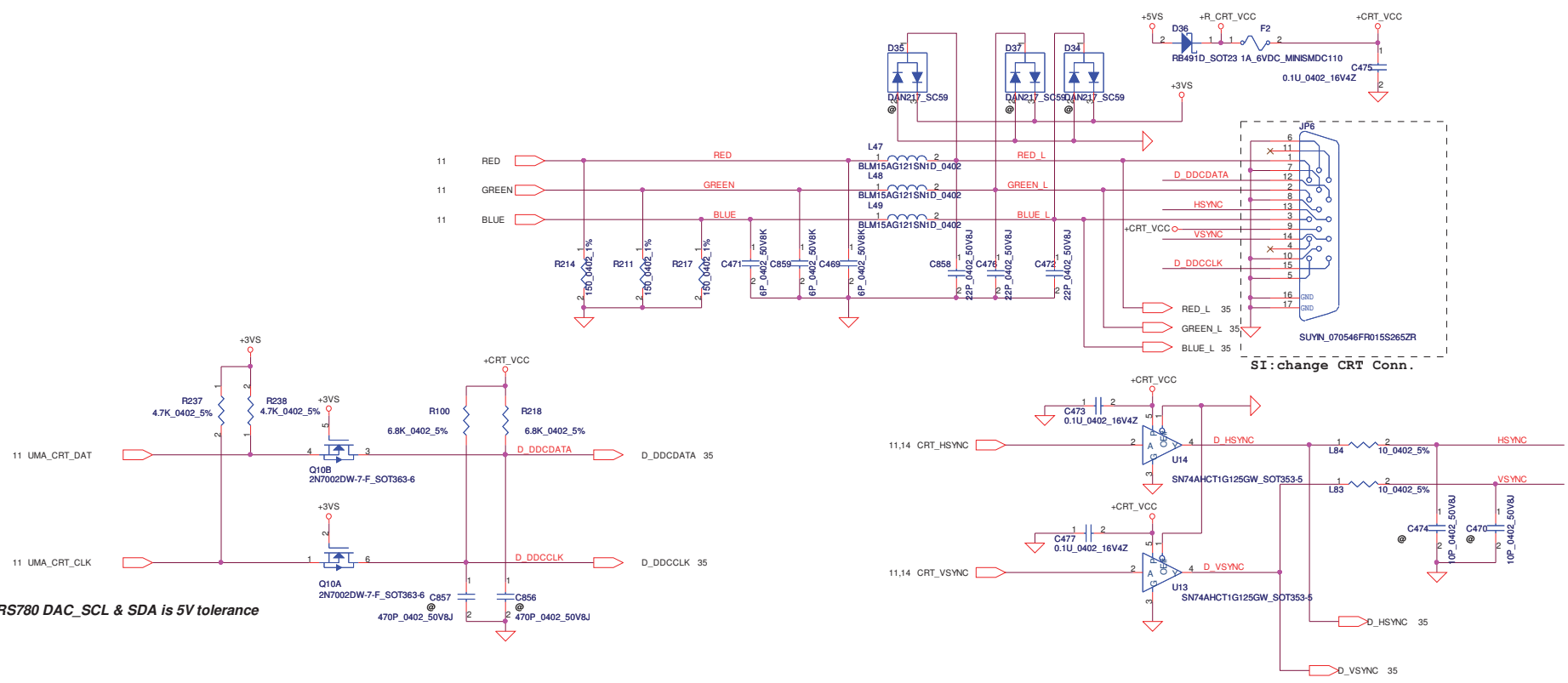
	OSC_14M_NB
RX780	1.8V 75R/100R
RS780	1.1V 158R/90.9R



NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vef
GFX_REFCLK	100M DIFF	100M DIFF(OUT)
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTP
GPPSB_REFCLK	100M DIFF	100M DIFF

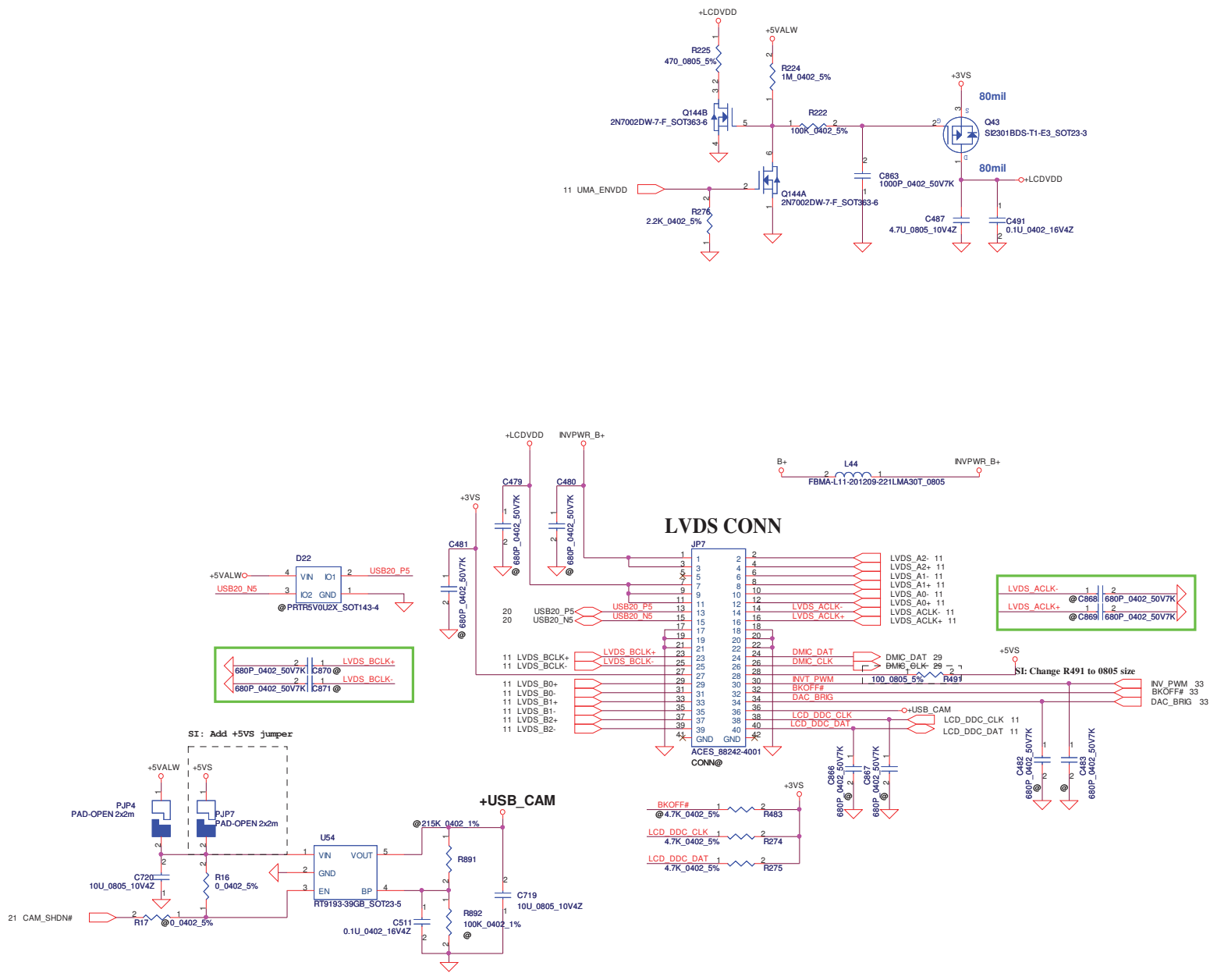
Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Clock generator		
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CRT CONNECTOR



RS780 DAC_SCL & SDA is 5V tolerance

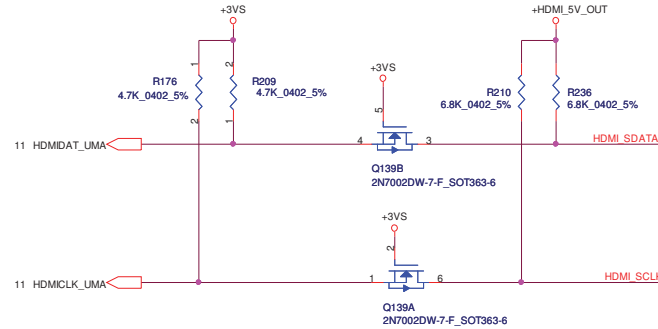
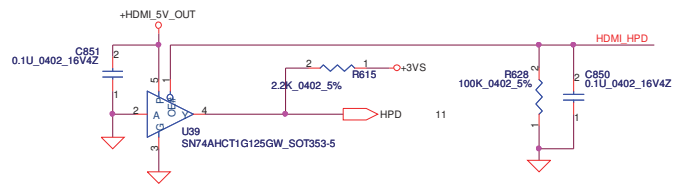
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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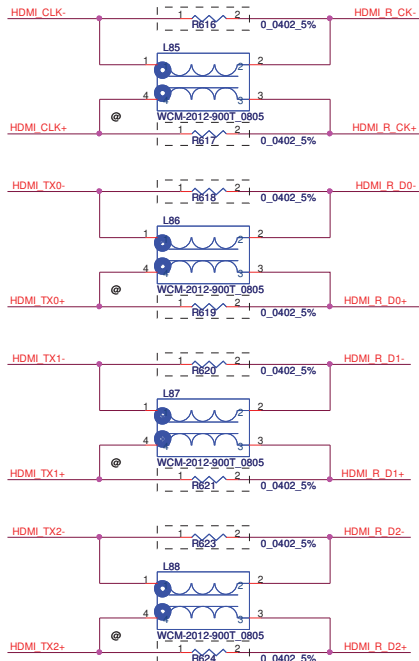
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Issued Date	2007/08/02	Deciphered Date	2008/08/02
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Compal Electronics, Inc.		
Title LCD CONN.		
Size Custom	Document Number LA-4091P	Rev 0.1
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<http://laptop-motherboard-schematic.blogspot.com/>

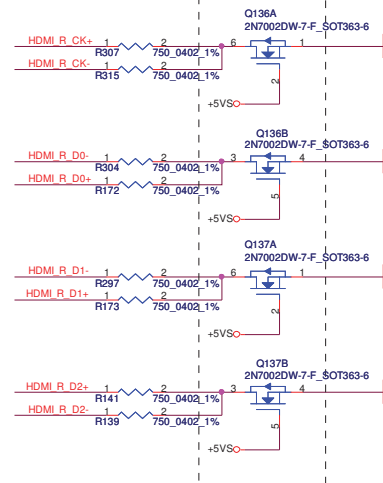


SI:Add R6161-R624 for EMI request

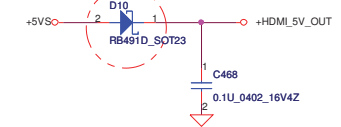


10	TMDS_B_CLK	C507	1	2	0.1U_0402_16V7K	HDMI_CLK+
10	TMDS_B_CLK#	C508	1	2	0.1U_0402_16V7K	HDMI_CLK-
10	TMDS_B_DATA0	C855	1	2	0.1U_0402_16V7K	HDMI_TX0+
10	TMDS_B_DATA0#	C875	1	2	0.1U_0402_16V7K	HDMI_TX0-
10	TMDS_B_DATA1	C804	1	2	0.1U_0402_16V7K	HDMI_TX1+
10	TMDS_B_DATA1#	C827	1	2	0.1U_0402_16V7K	HDMI_TX1-
10	TMDS_B_DATA2	C852	1	2	0.1U_0402_16V7K	HDMI_TX2+
10	TMDS_B_DATA2#	C853	1	2	0.1U_0402_16V7K	HDMI_TX2-

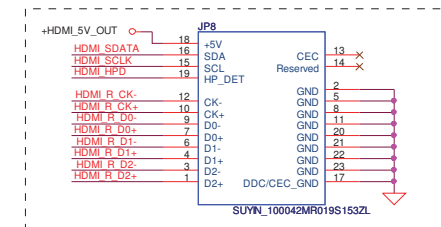
SI:Add Q136 & Q137 for AMD request



MP:Update D10 to meet HDMI.



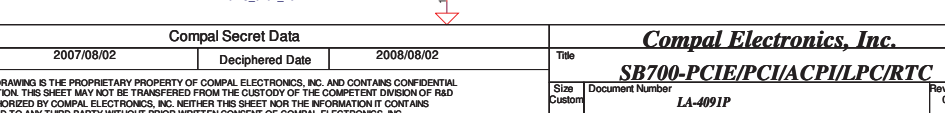
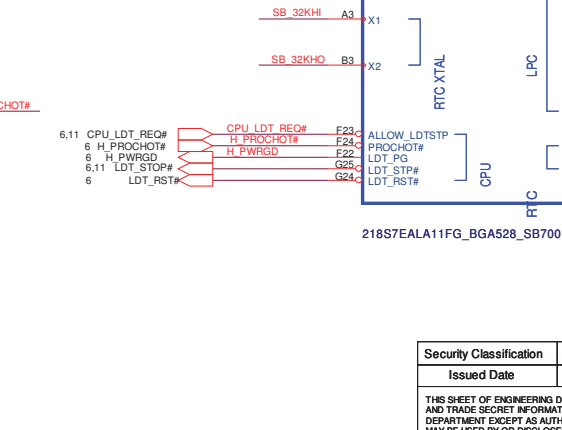
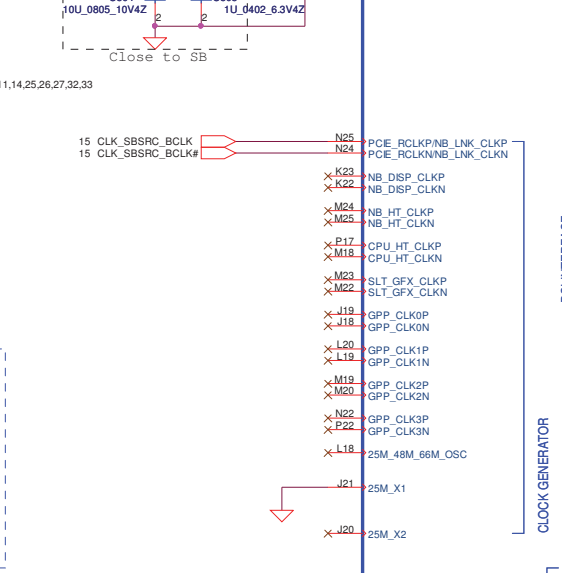
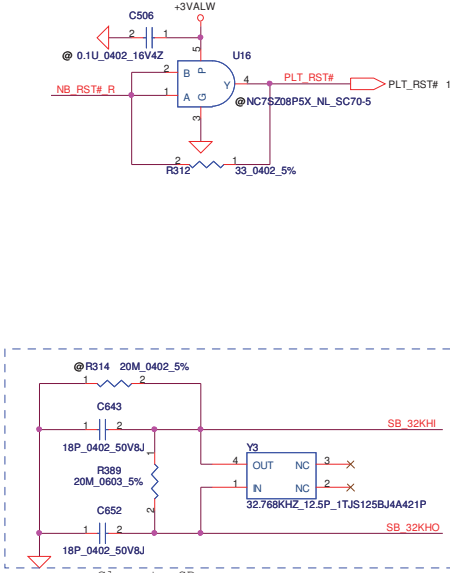
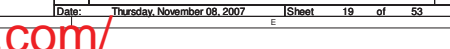
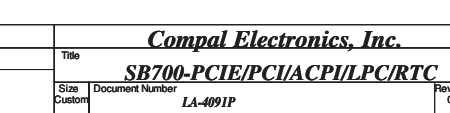
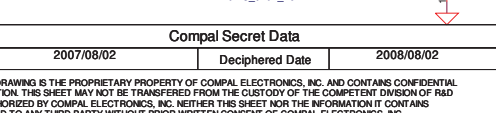
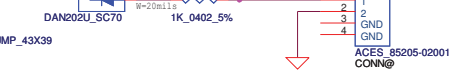
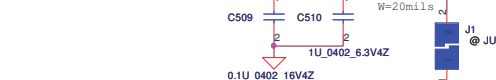
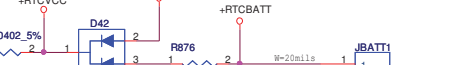
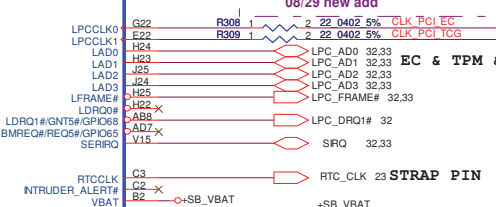
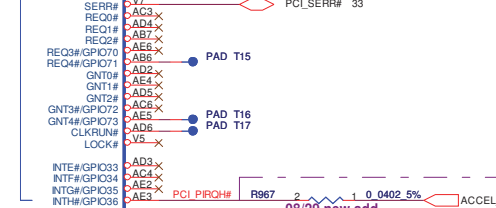
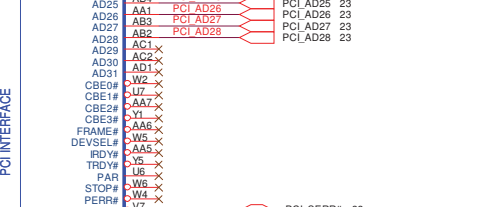
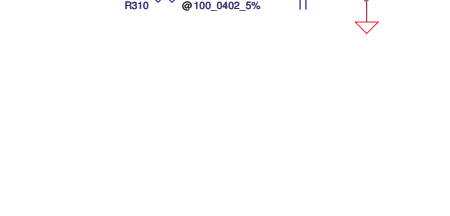
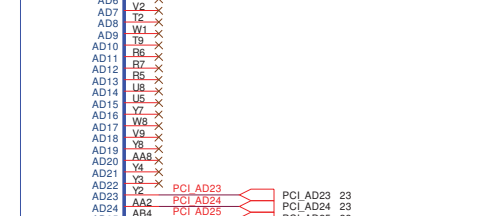
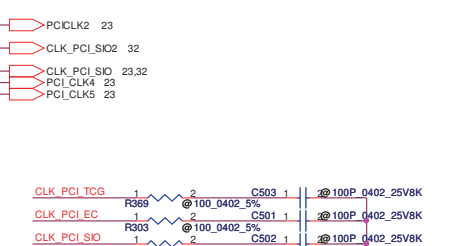
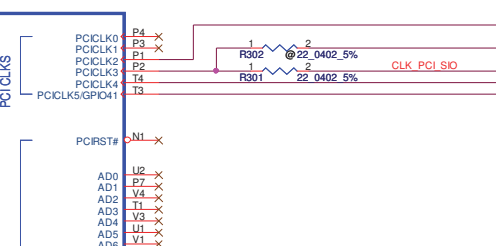
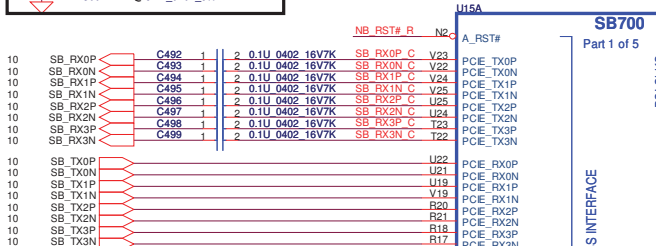
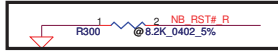
HDMI Connector



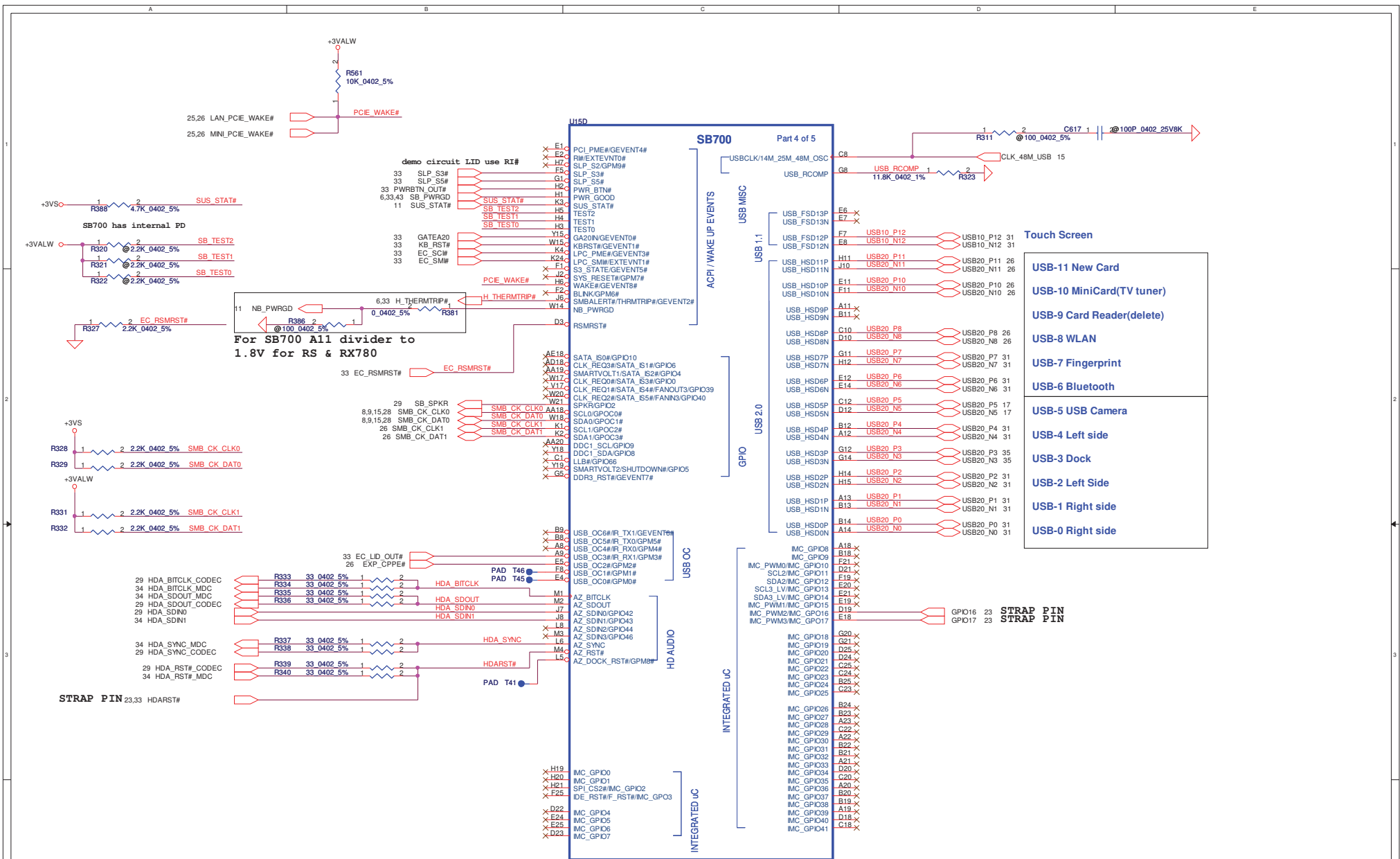
SI:Update HDMI footprint

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	HDMI			
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Date: Thursday, November 08, 2007				Sheet	18	of 53	

Check AMD need pull low or not

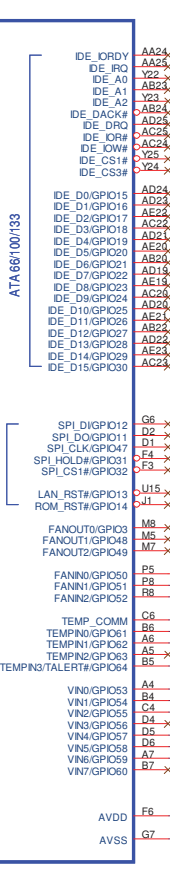
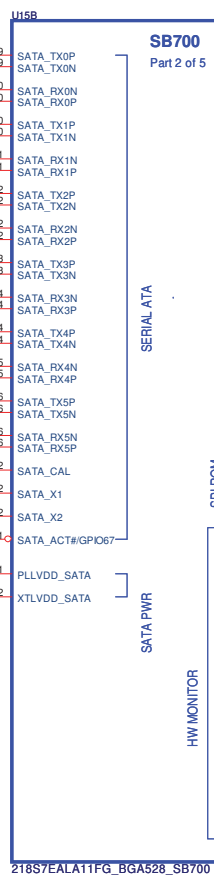


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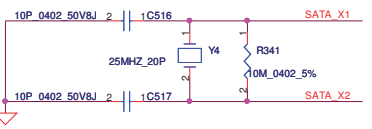
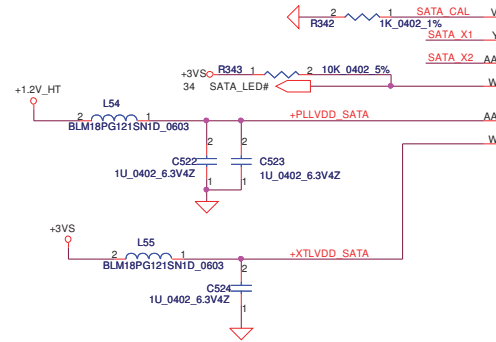
Compal Electronics, Inc.		
Title SB700 USB/AC97		
Size Custom	Document Number LA-4091P	Rev 0.1
Date	Thursday, November 08, 2007	Sheet 20 of 53



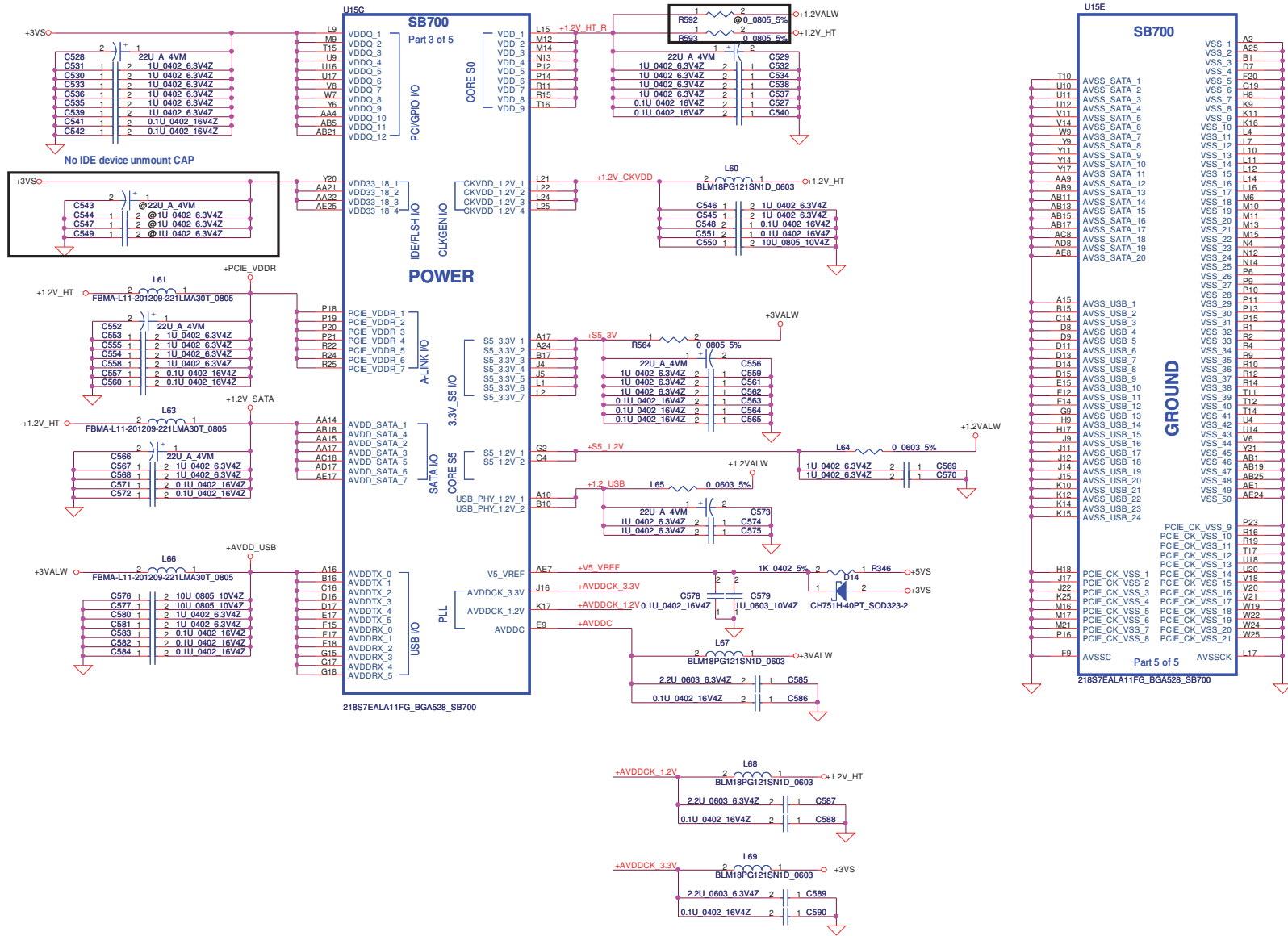
Local Frame Buffer Strapping List
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0
Hynix32M*16	1	1	0
Samsung32M*16	1	0	1

LFB_ID0 to LFB_ID2 got internal PU 10K to S5.



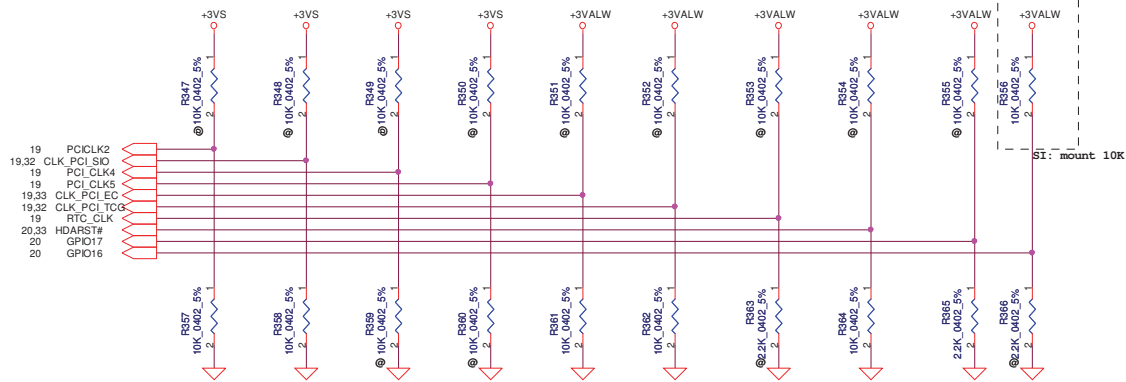
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

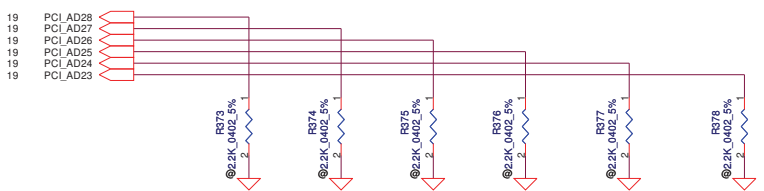
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



DEBUG STRAPS

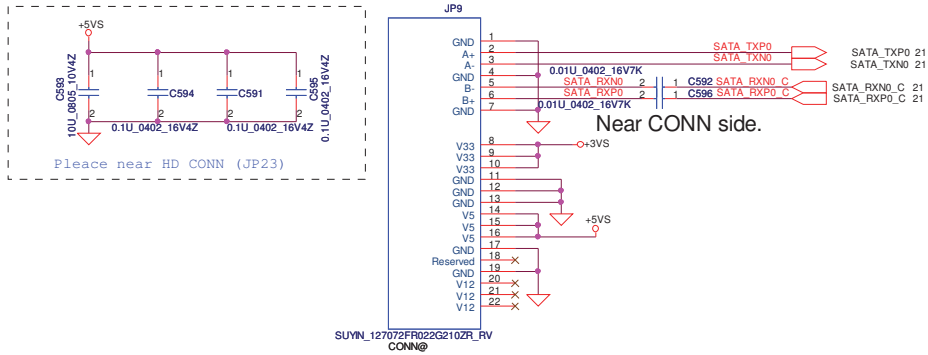
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



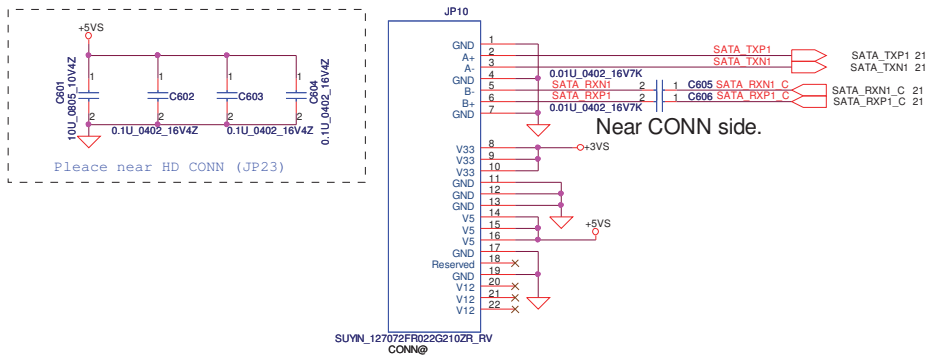
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Size	Document Number	Rev		
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HDD Connector



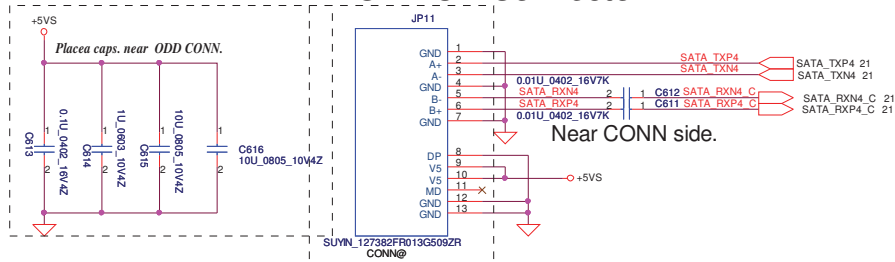
DC010003M00 HOUSING SUYIN 127043FR022G204ZL 22P SATA
SUYIN_127043FR022G204ZL_22P_NR

2nd HDD Connector-option



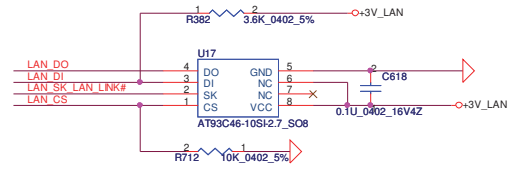
DC010003M00 HOUSING SUYIN 127043FR022G204ZL 22P SATA
SUYIN_127043FR022G204ZL_22P_NR

CD-ROM Connector

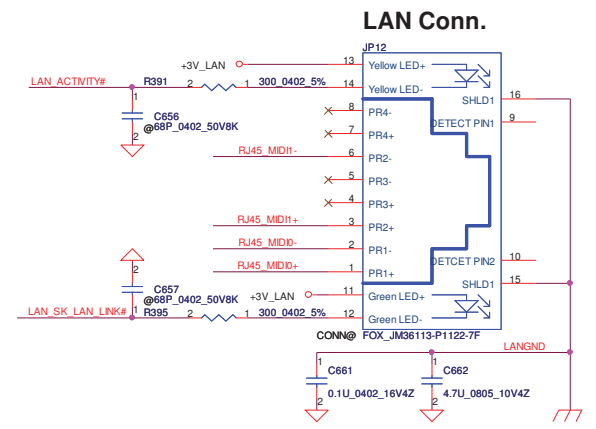
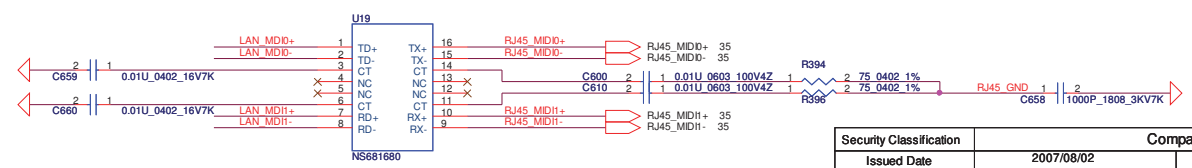
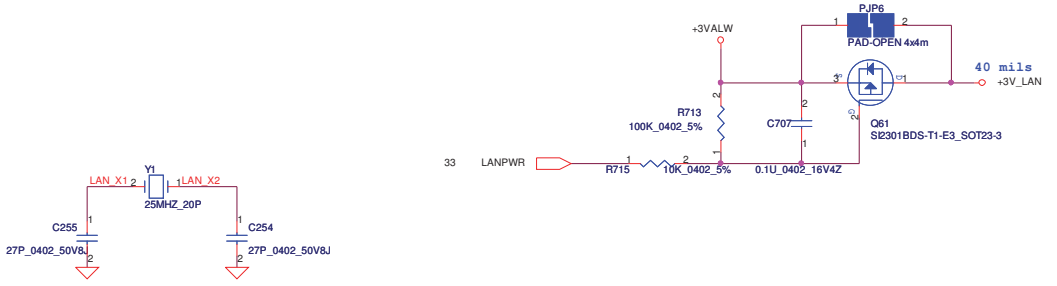
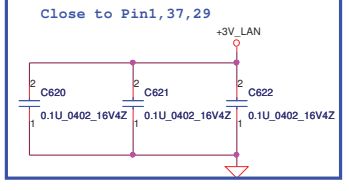
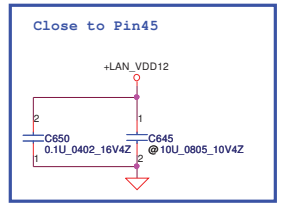
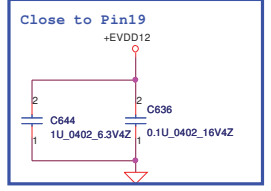
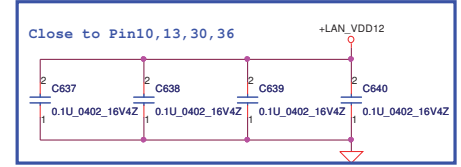
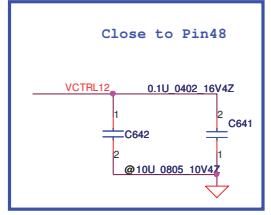
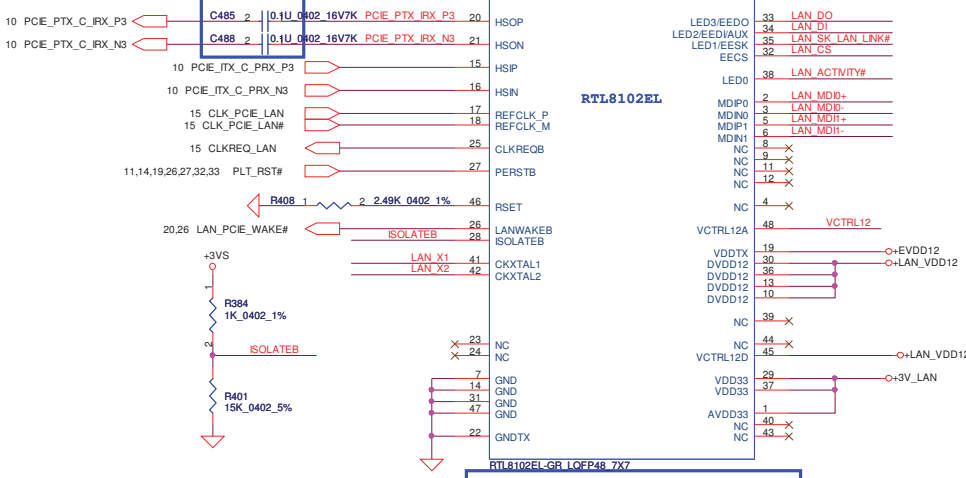


SI: Update ODD footprint to fix pin reverse issue

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	HDD/CDROM	
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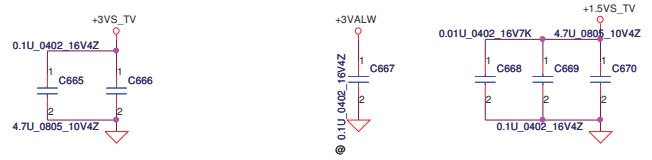
Place Close to Chip



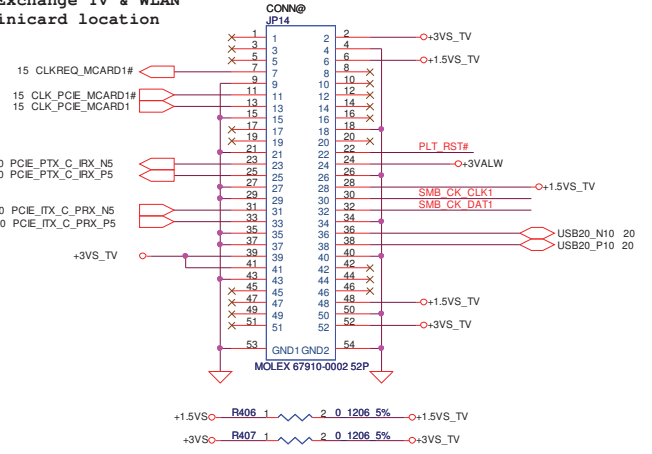
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Compal Electronics, Inc.		
Title RTL8111C/8102E 10/100/1000 LAN		
Size Custom	Document Number LA-4091P	Rev 0.1
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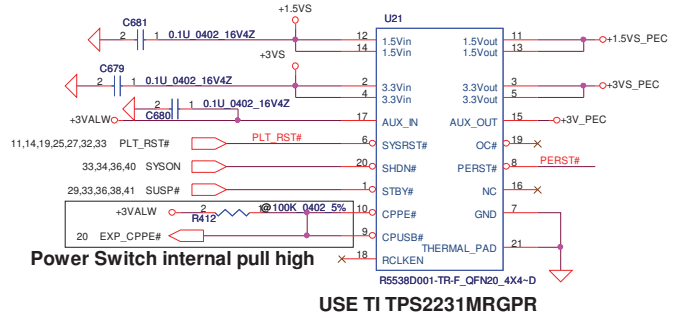
Mini Card--TV tuner



SI: Exchange TV & WLAN minicard location

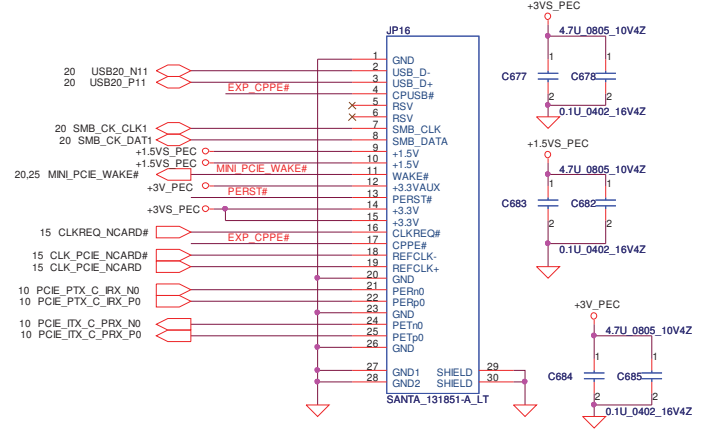


New Card

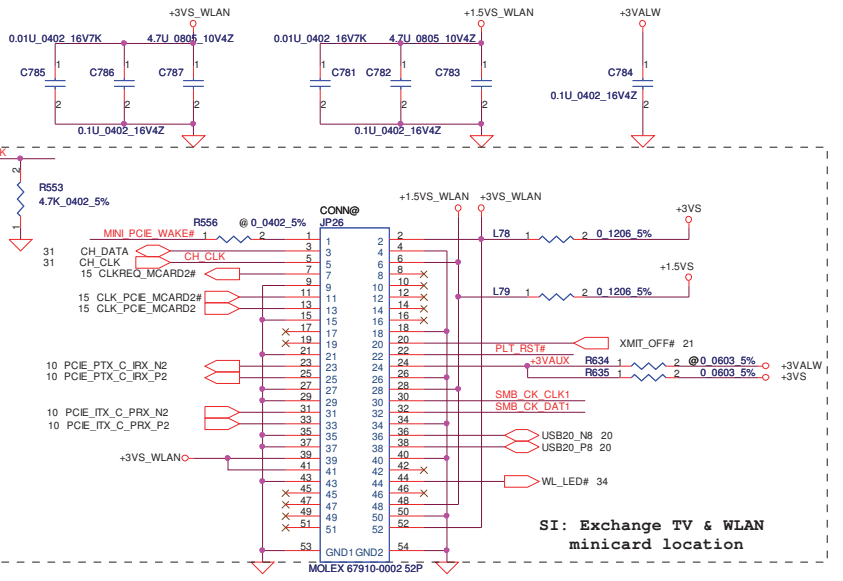


USE TI TPS2231MRGPR

Near to Express Card slot.

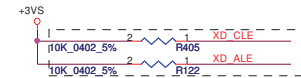
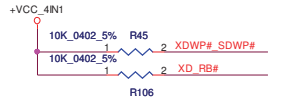
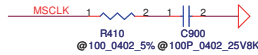
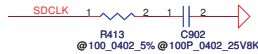
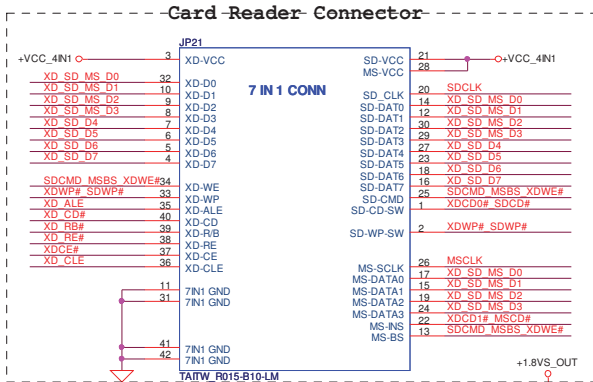


Mini-Express Card--WLAN



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SI:Per ME request change
JP21 to new one



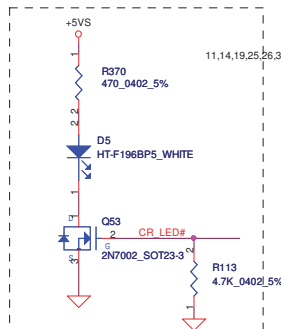
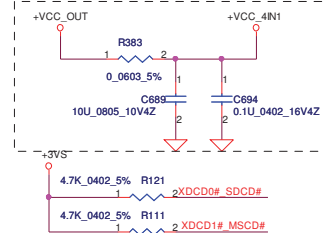
SI:Per Jmicro request change
R405 & R122 from 200K to 10K

SI:Use build in Regulator
Chip unmount R387

Power Circuit

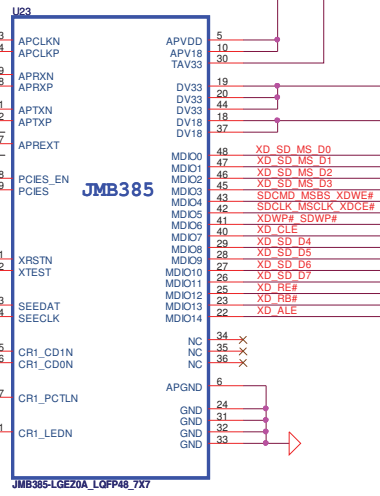
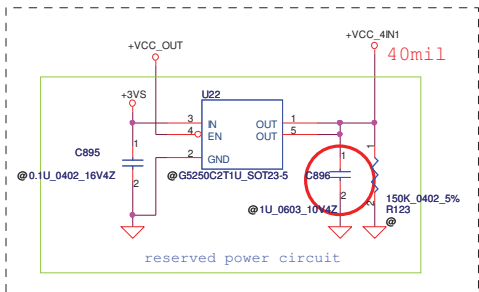
SI:Per Jmicro request change
R114 from 10K to 8.2K

SI:Use build in Regulator
Chip mount R383, C689, C694

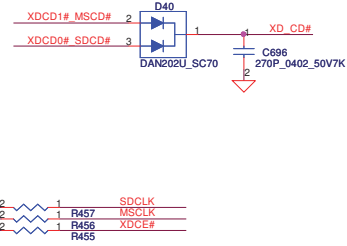


SI:Use new chip, change to
High active control

SI:Use build in Regulator
Chip unmount U22 and relation parts



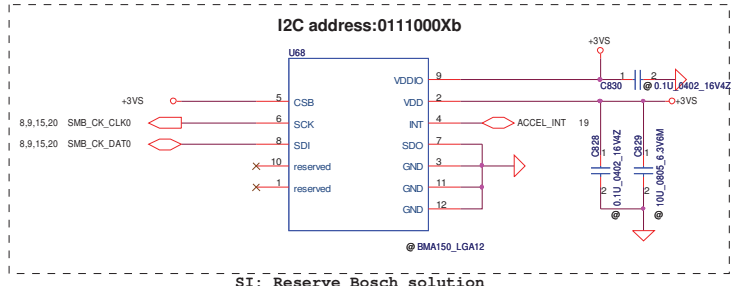
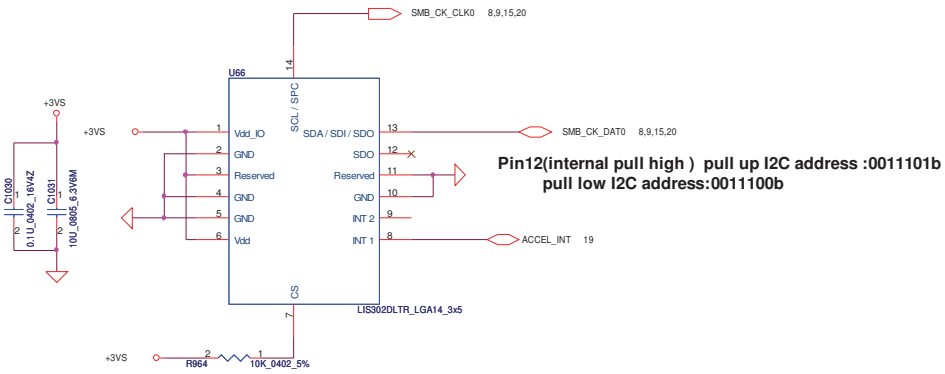
SI: Use 0740 date code chip



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		2008/08/02
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Compal Electronics, Inc.		
Title		
JMB380/385 card reader/1394		
Size	Document Number	Rev
Custom	LA-4091P	0.1
Date:	Thursday, November 08, 2007	Sheet 27 of 53

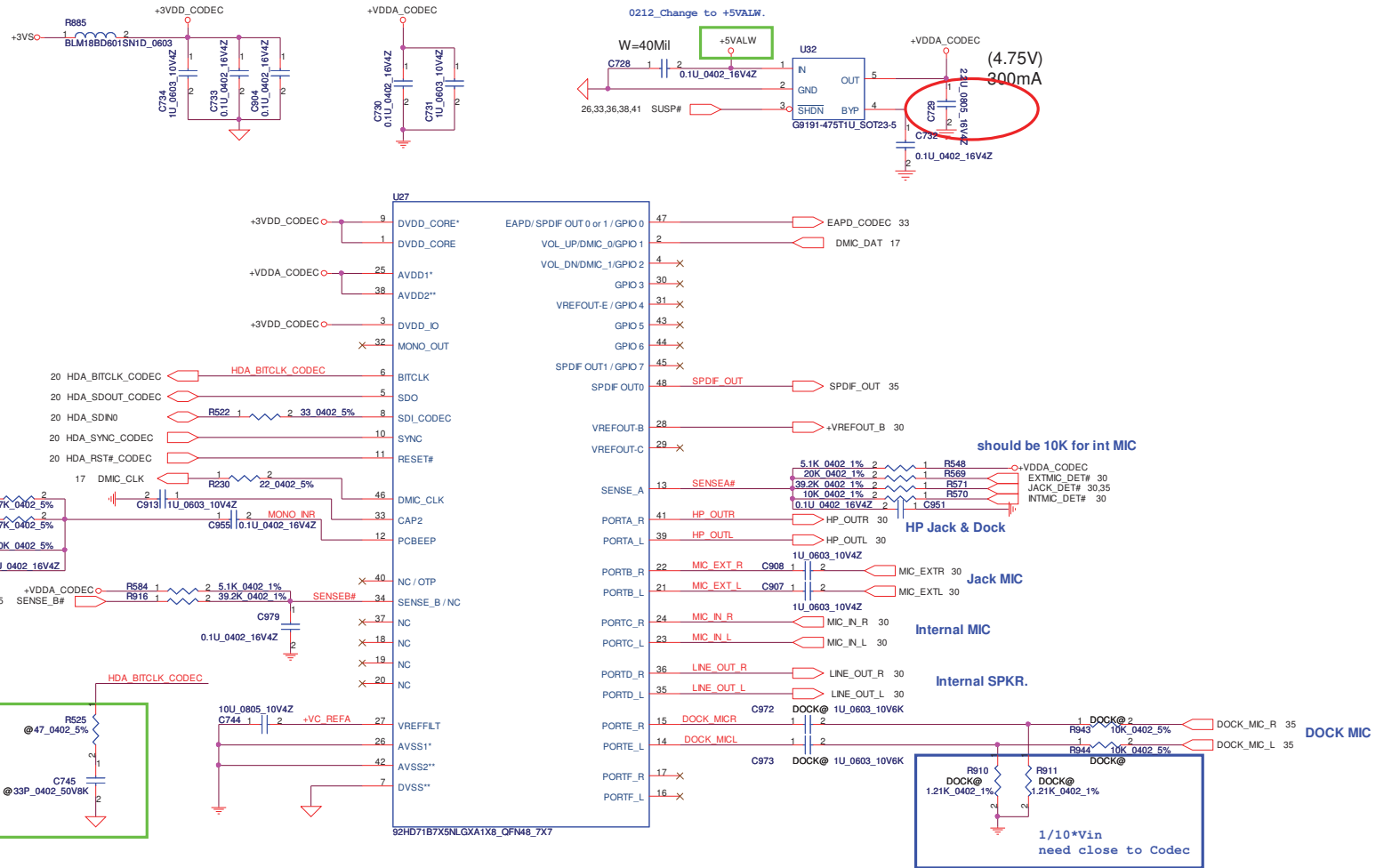
ACCELEROMETER



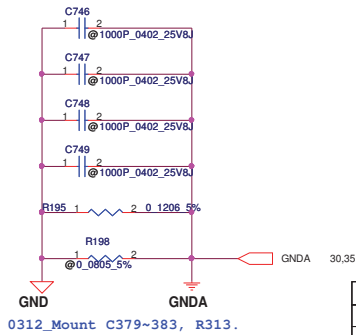
SI: Reserve Bosch solution

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Compal Electronics, Inc.
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CODEC POWER

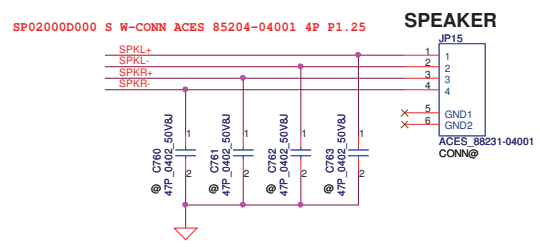
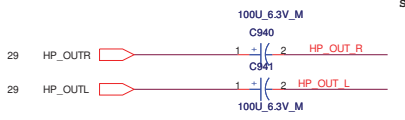
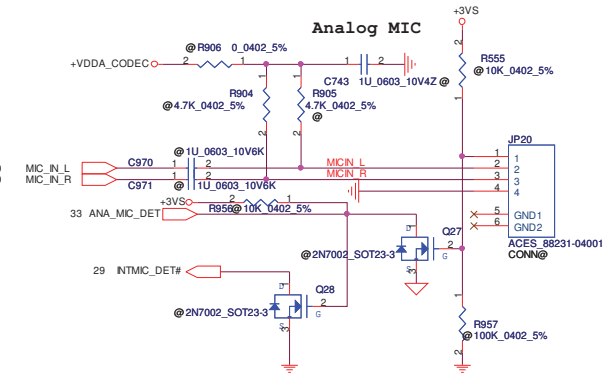
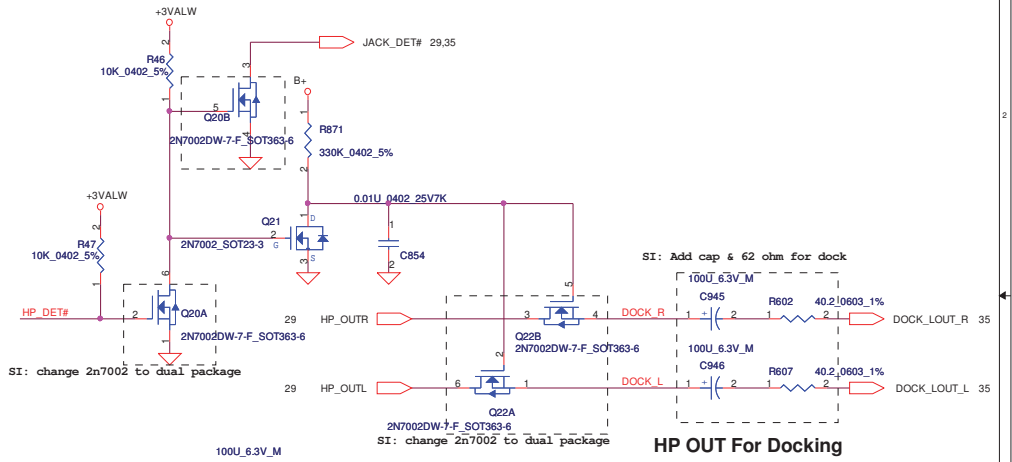
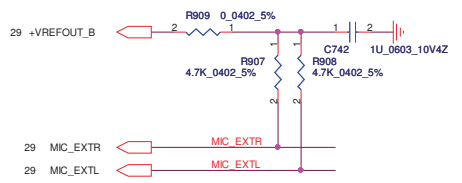
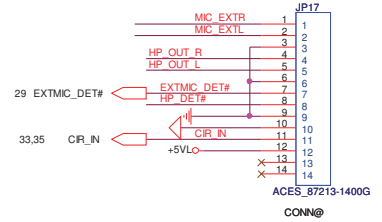
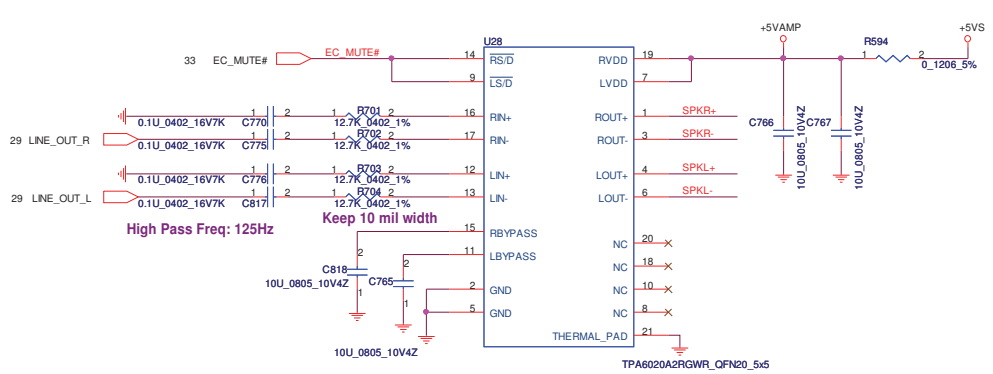


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



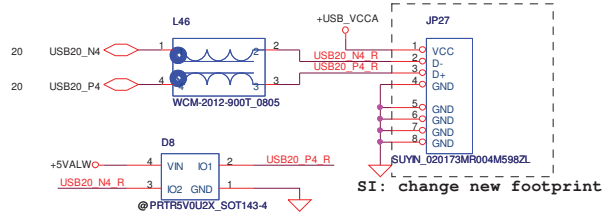
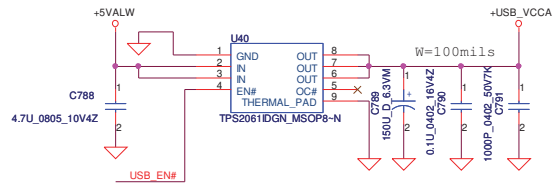
HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	OFF	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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Size	Document Number	Rev	Date: Thursday, November 08, 2007 Sheet 29 of 53	
Custom	LA-4091P	0.1		

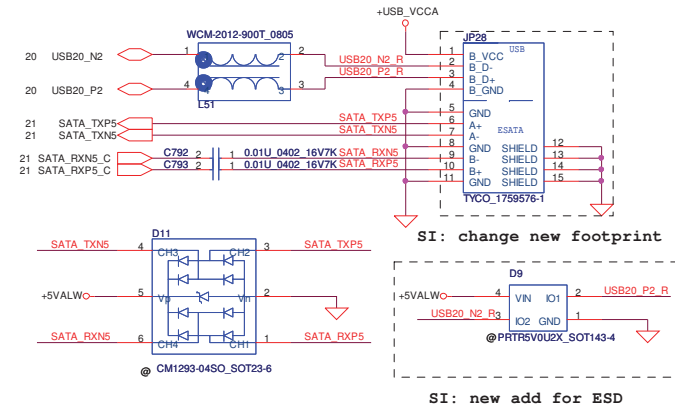


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				LA-4091P	0.1	
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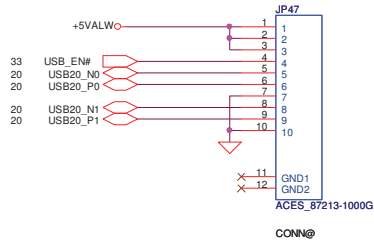
Left side USB CONNECTOR 0



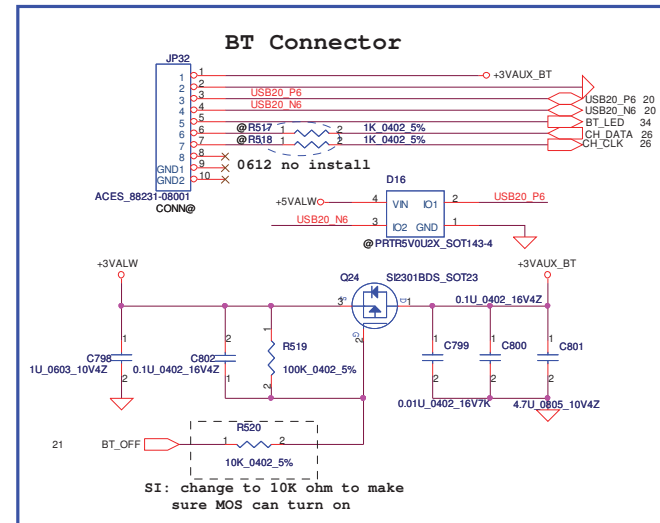
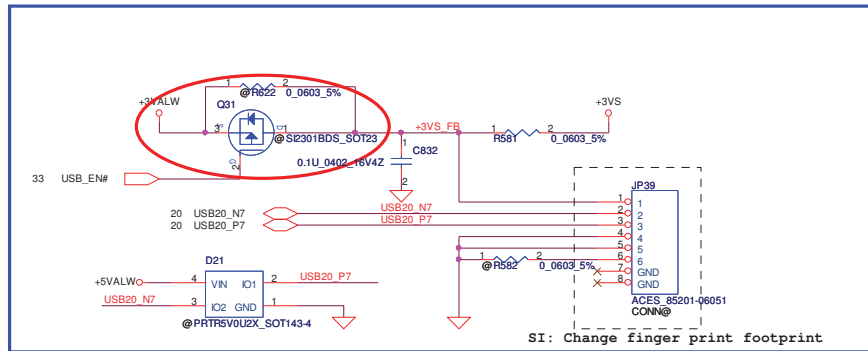
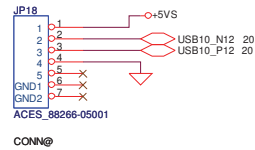
Left side ESATA/USB combination Connector



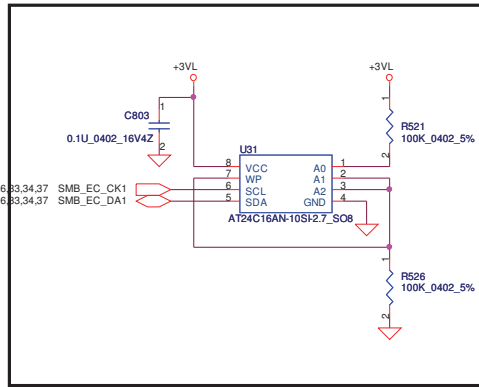
USB Board Conn



Touch screen

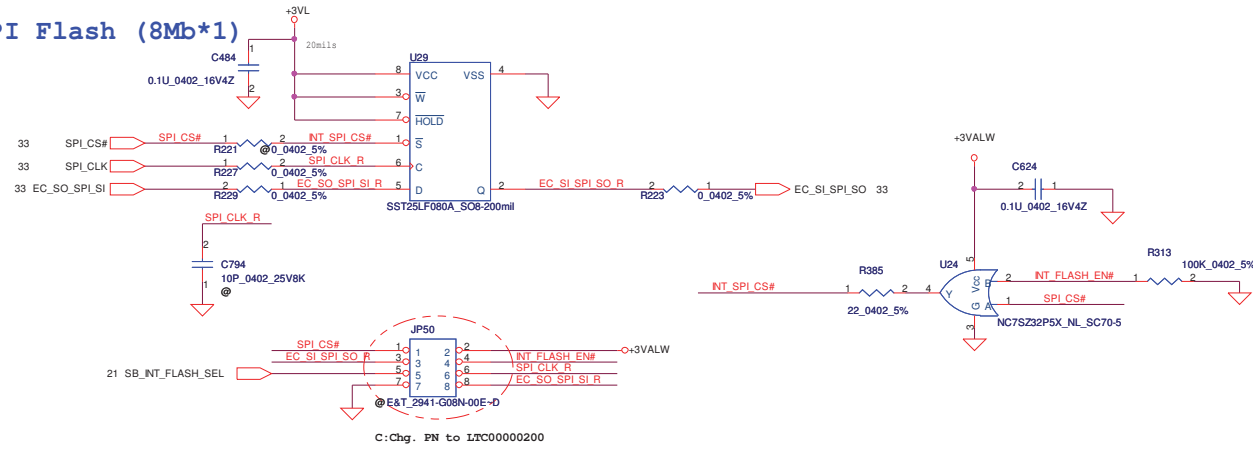


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Size	Document Number	Rev		0.1
Custom	LA-4091P	Date:		Thursday, November 08, 2007
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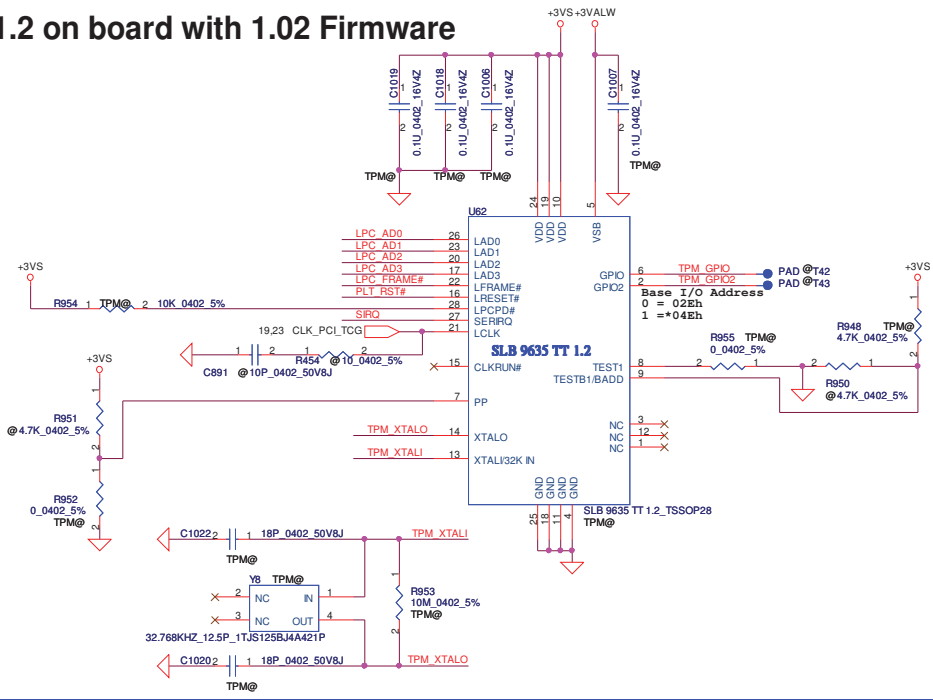


EEPROM need merge to BIOS ROM

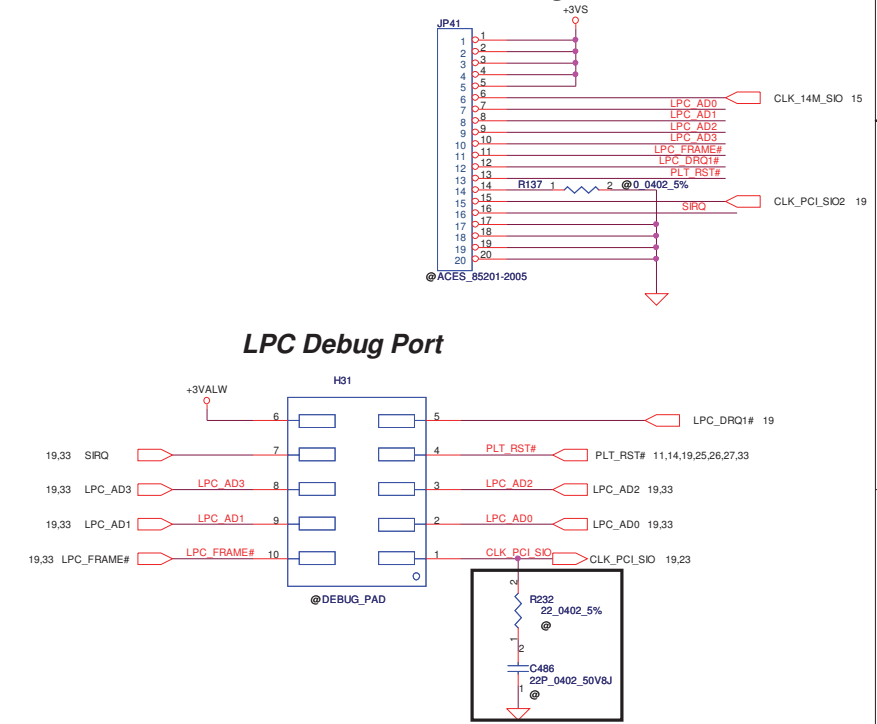
SPI Flash (8Mb*1)



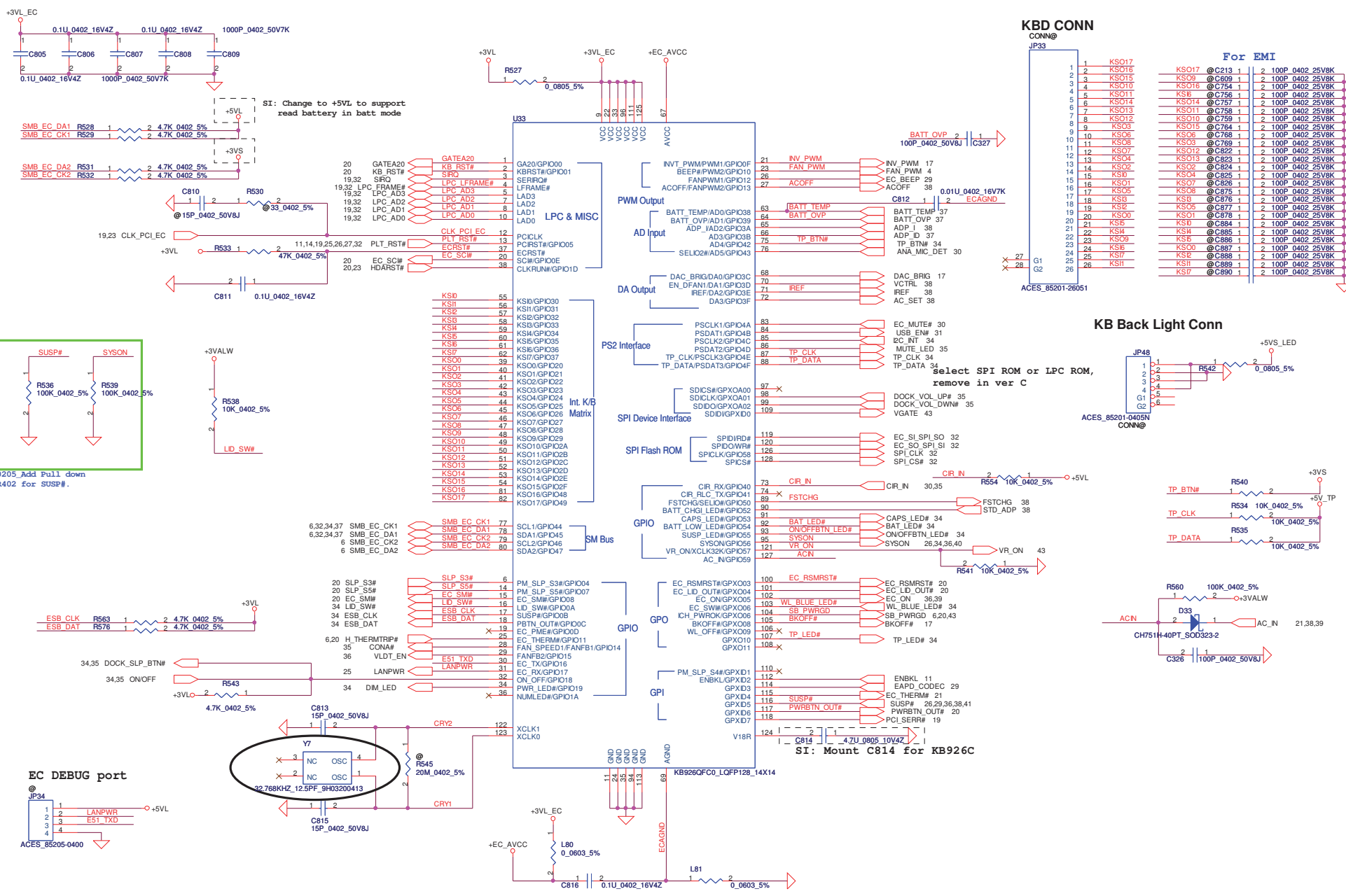
TPM1.2 on board with 1.02 Firmware



LPC Debug Port



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	TCG/BIOS ROM/PS2/LED/SW	
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Size Custom	Document Number	Rev	Date: Thursday, November 08, 2007 Sheet 32 of 53		
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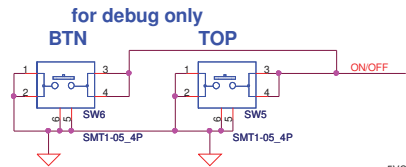
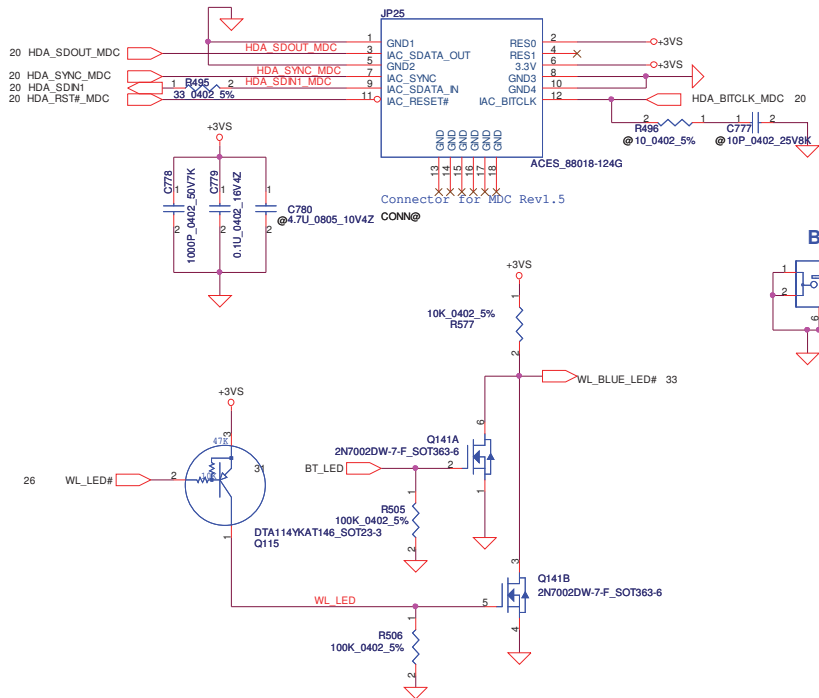


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Compal Electronics, Inc.		
Title EC KB926/KB conn		
Size Custom	Document Number LA-4091P	Rev 0.1
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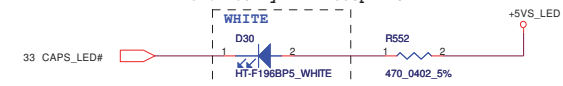
MDC 1.5 Conn.

Change type 4/25



CAPS LOCK LED

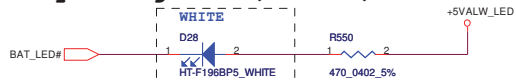
SI: Modify LED footprint



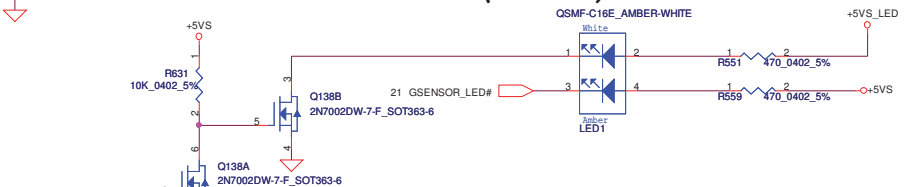
POWER LED (Left 1)



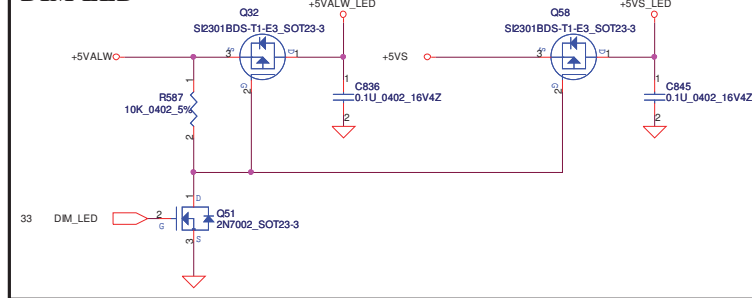
Battery Charge LED (Left 2)



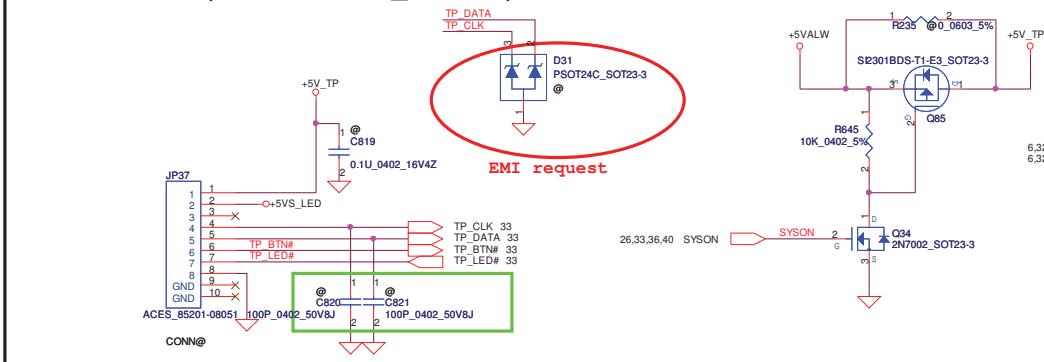
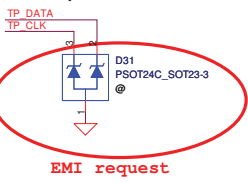
HDD LED (Left 3)



DIM LED

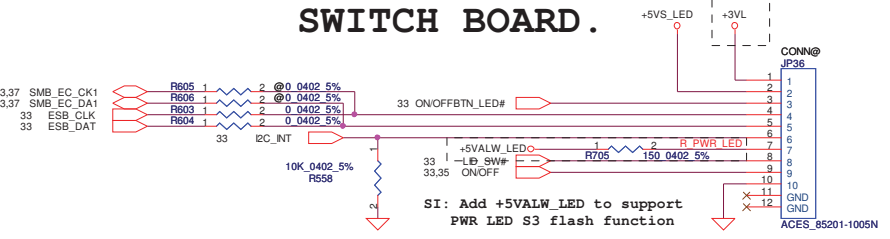


T/P Board (Include T/P_ON/OFF)



SI: Change to +3VL to support Qplay bottom boot in BATT mode

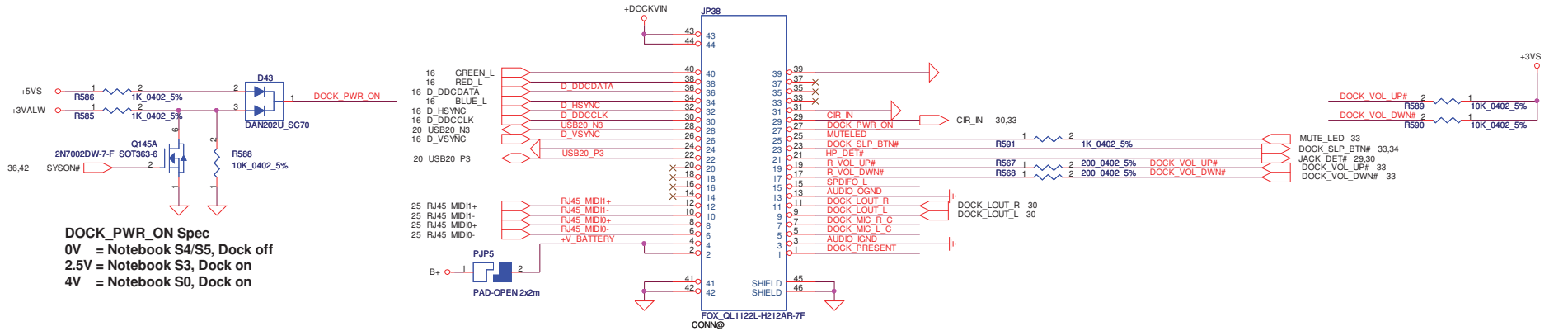
SWITCH BOARD.



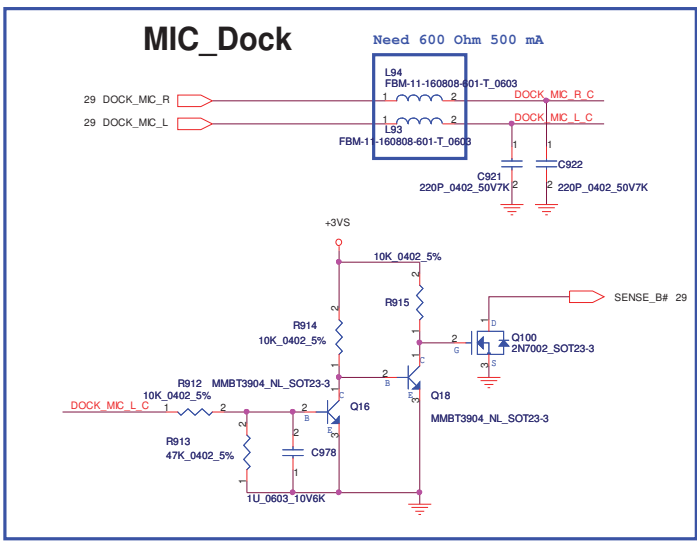
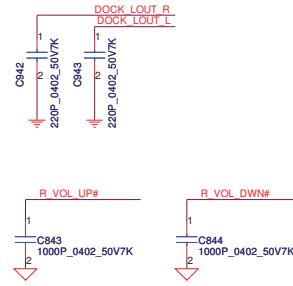
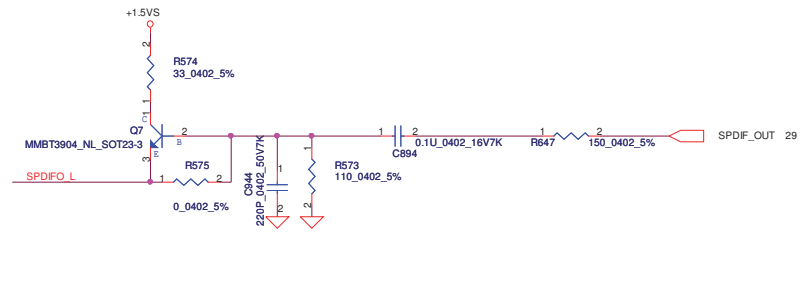
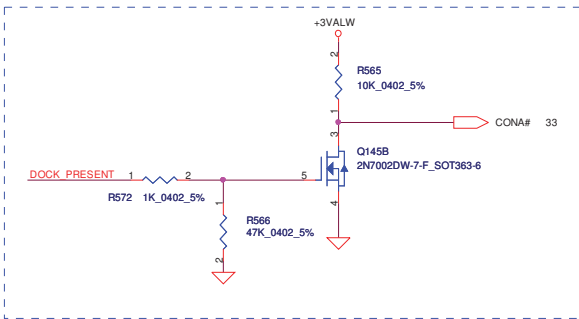
SI: Add +5VALW_LED to support PWR LED S3 flash function

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Atlas/ Saturn Dock

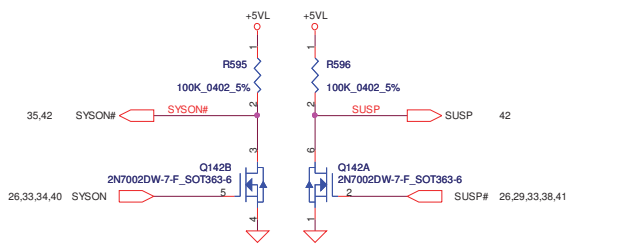
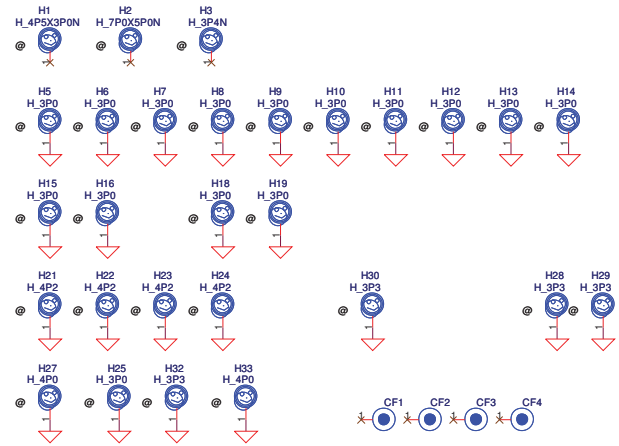


need change to reverse type connector

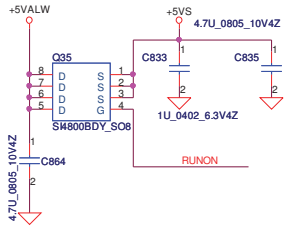


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Size	Document Number	Rev		
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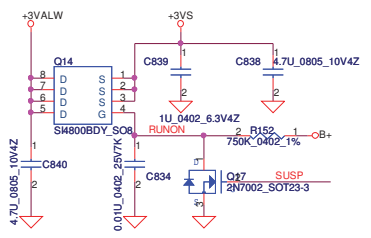
Screw Hole



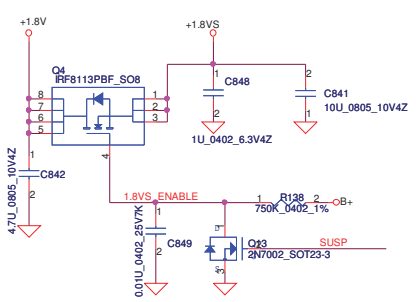
+5VALW TO +5VS



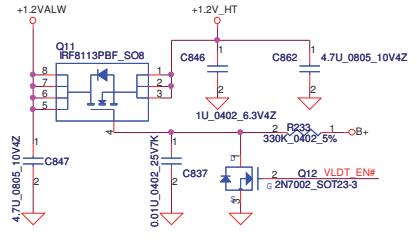
+3VALW TO +3VS



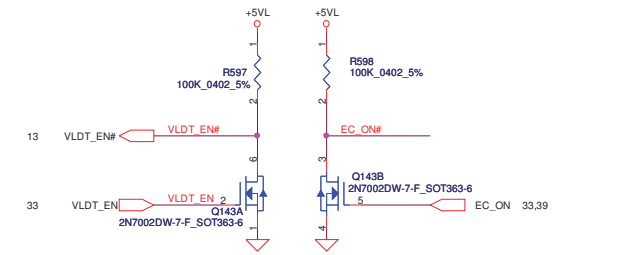
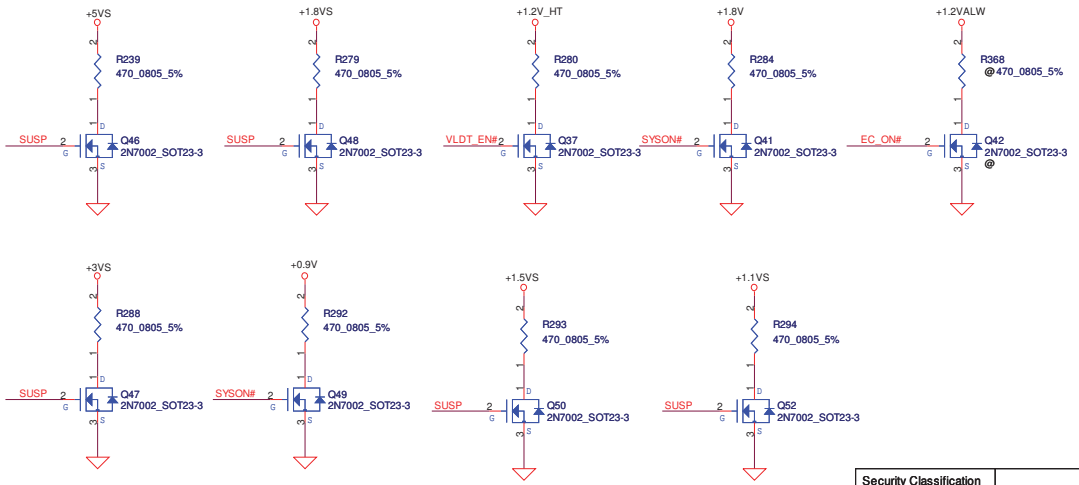
+1.8V TO +1.8VS



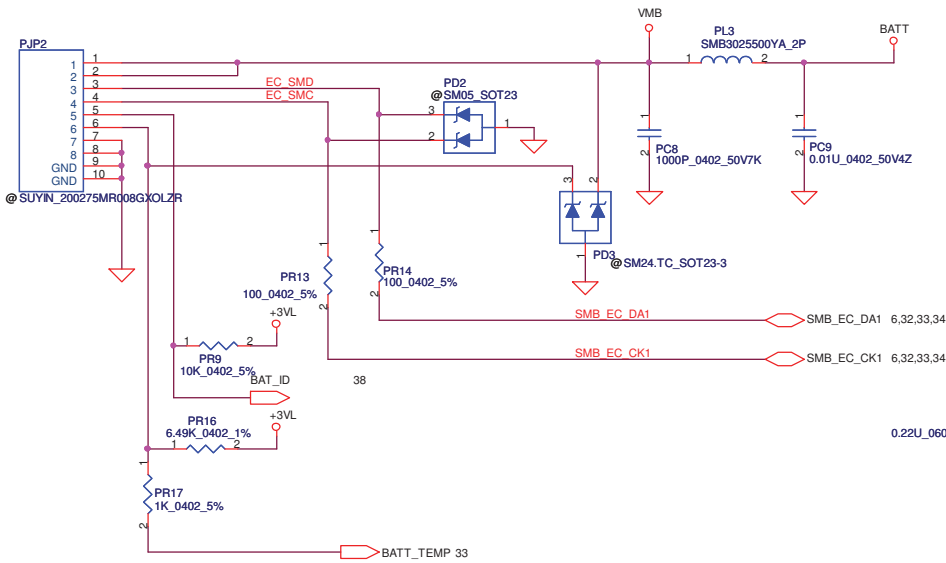
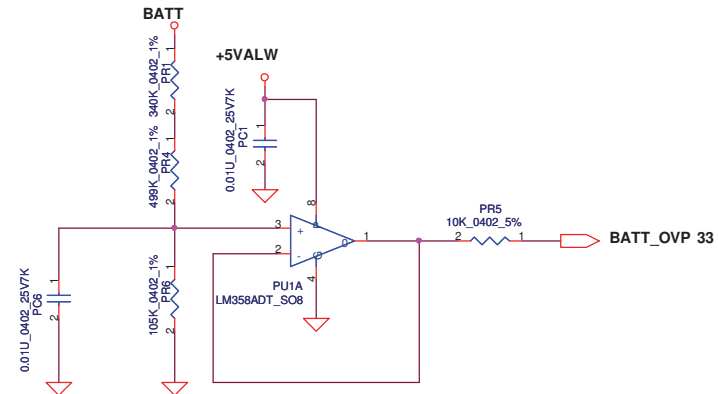
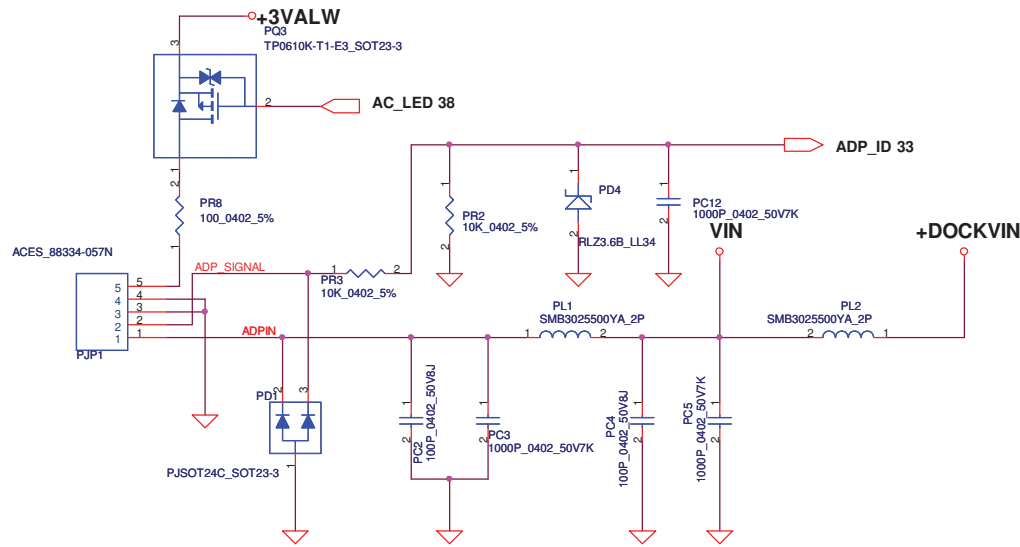
+1.2VALW TO +1.2V_HT



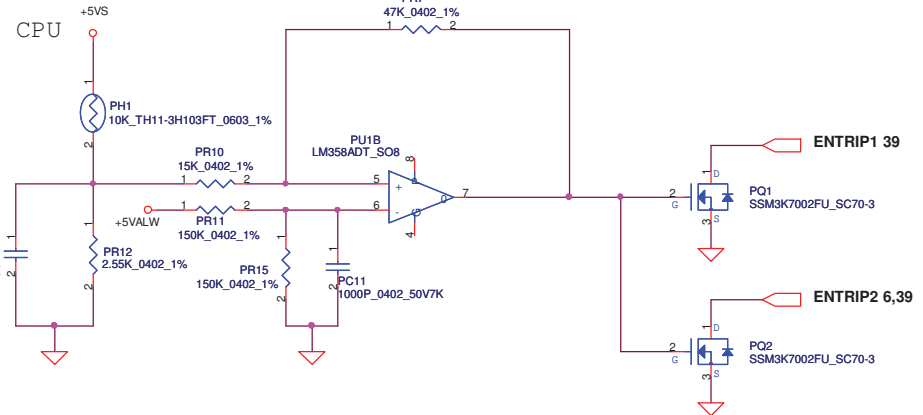
Discharge circuit



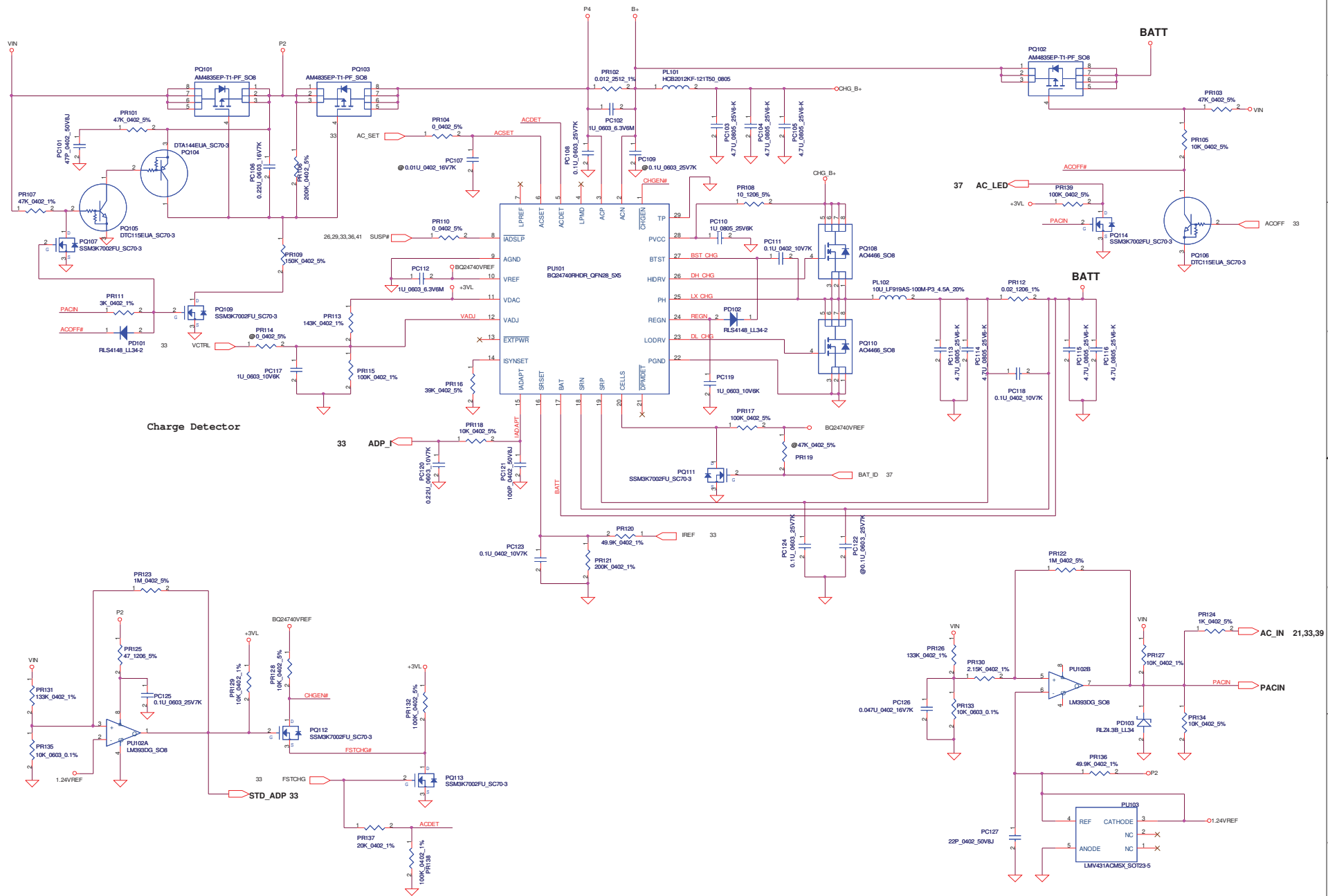
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	DC/DC Circuits	
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 47 +-3 degree C

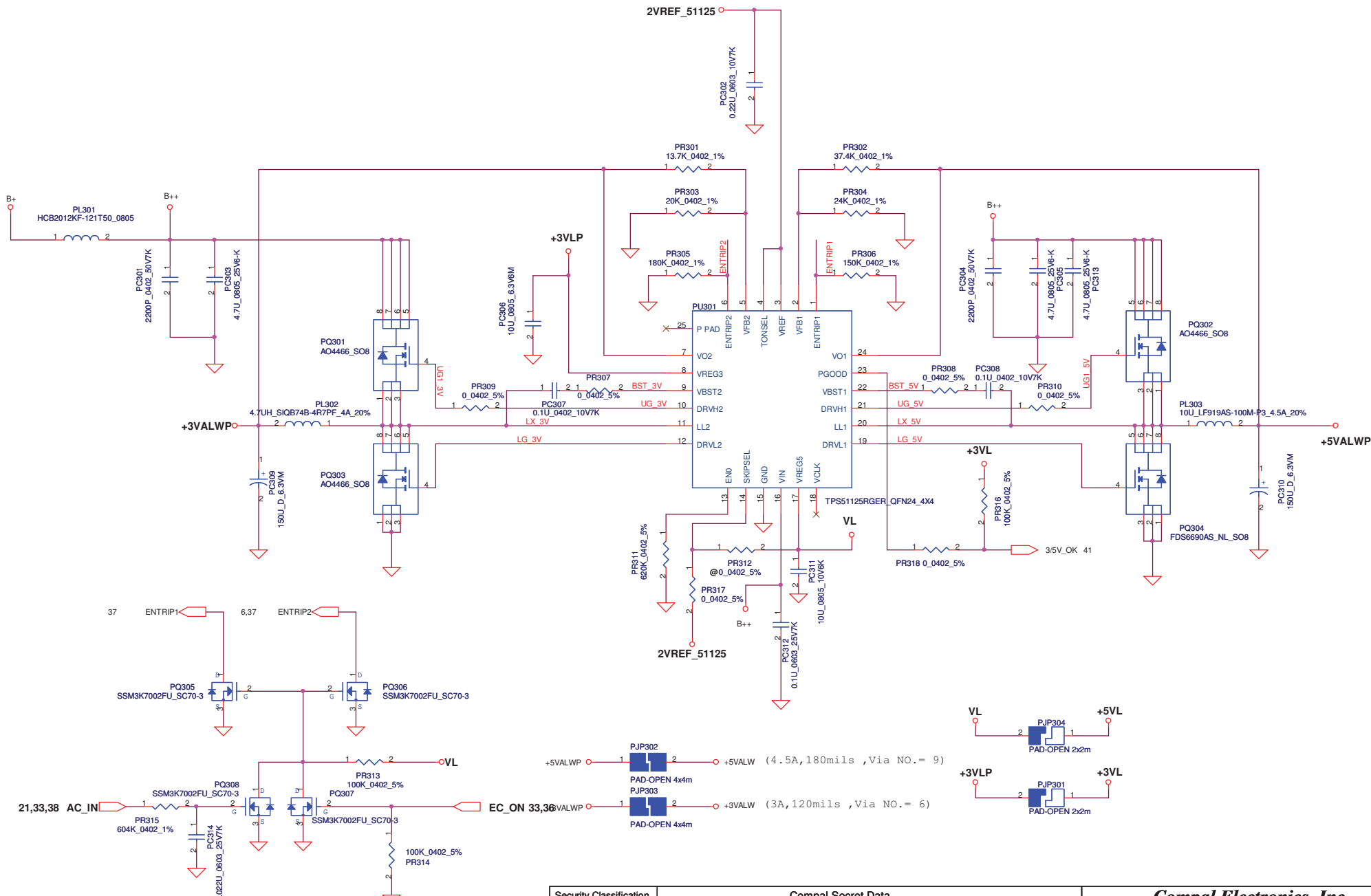


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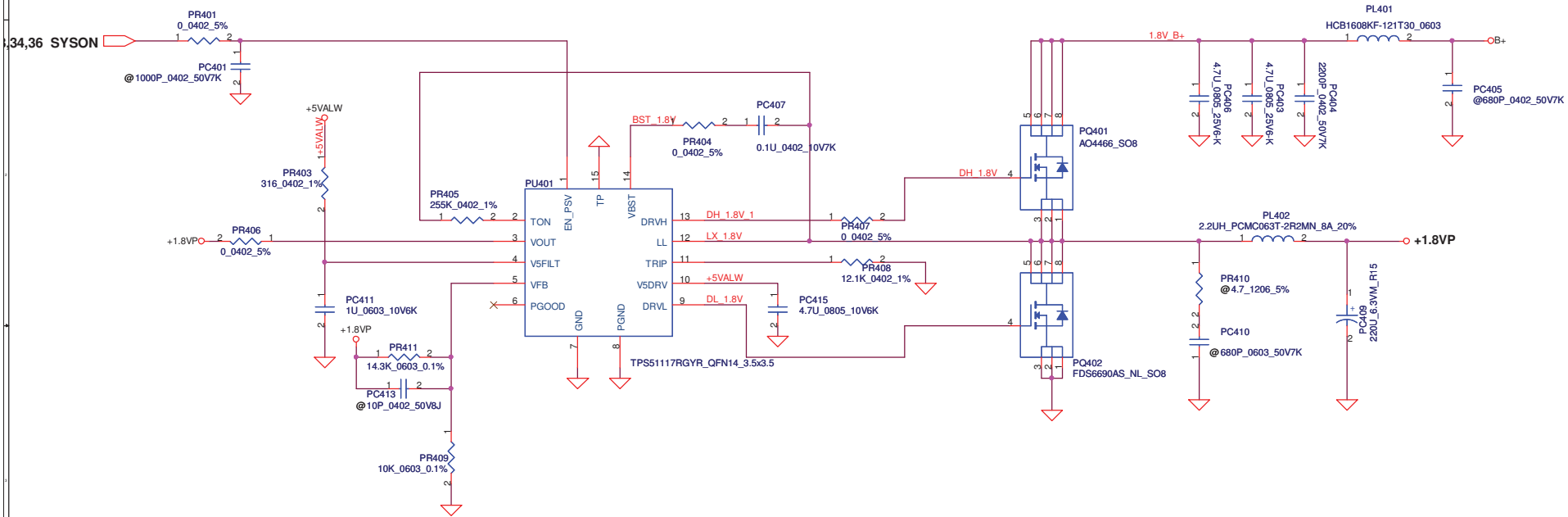
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<http://laptop-motherboard-schematic.blogspot.com/>

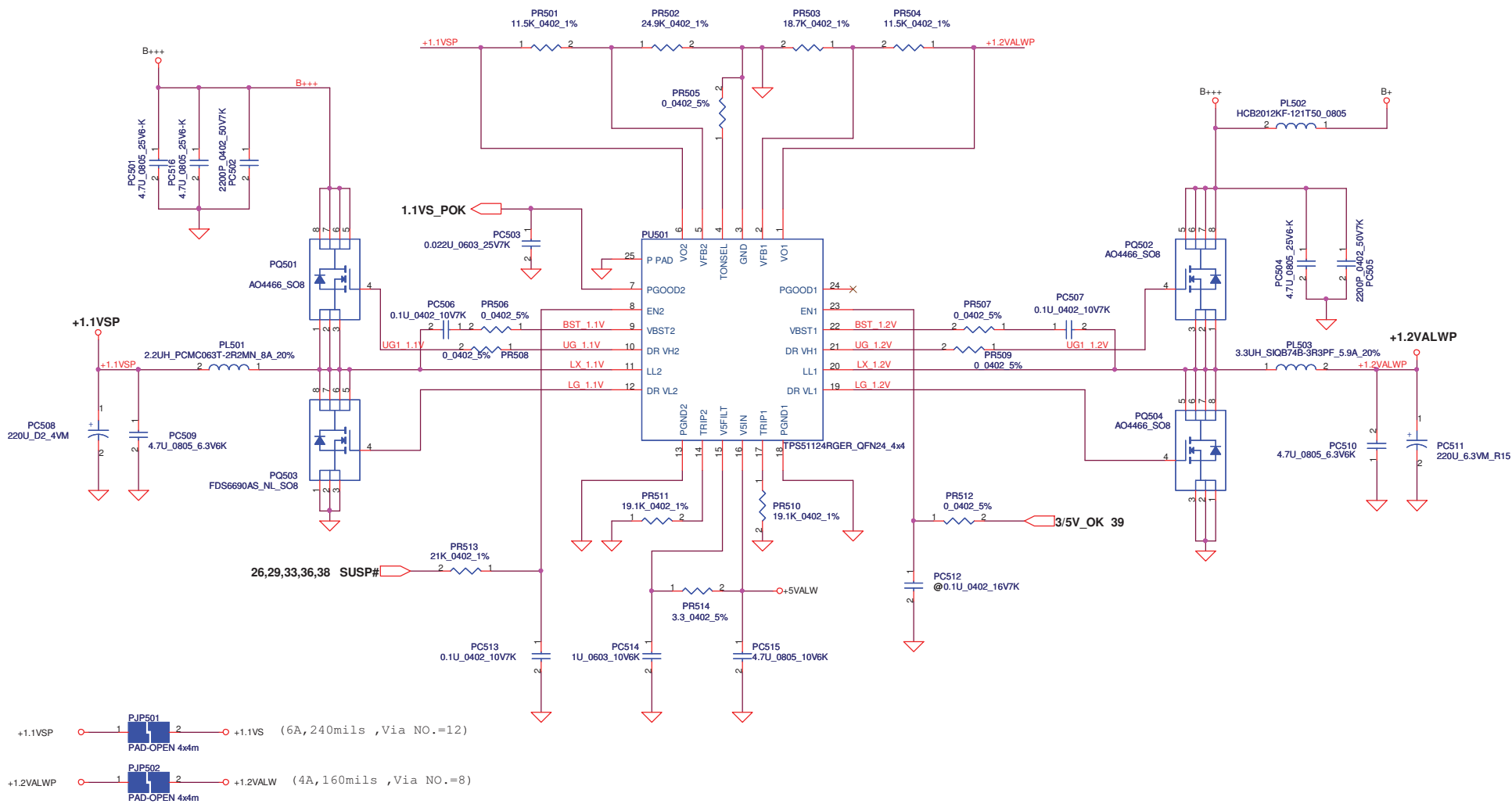


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Title			
3.3VALWP/5VALWP			
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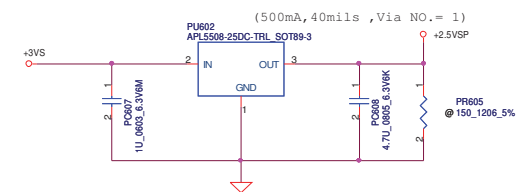
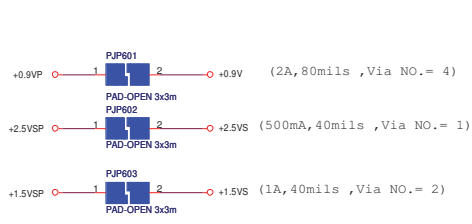
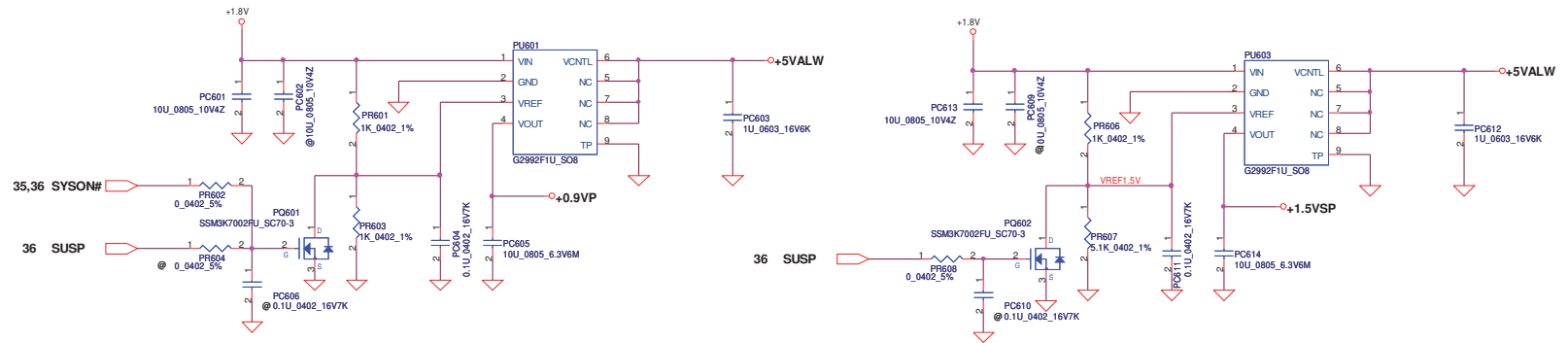


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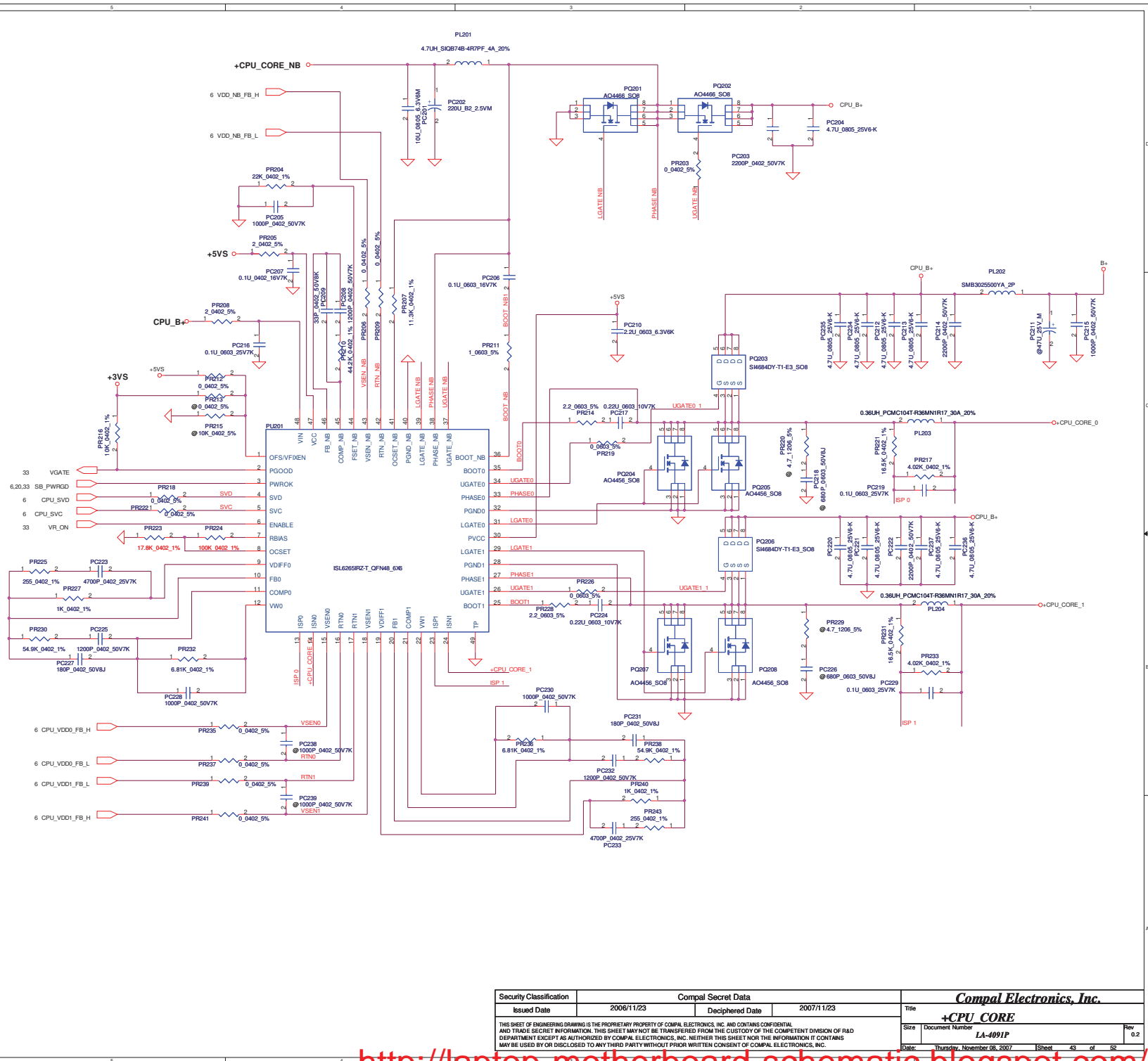
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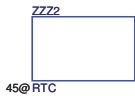
Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	1.8VP	10/23	Compal	for power request	PU401 change the IC from "S IC RT8204PQW WQFN I6P" to "S IC TPS51117RGYR QFN 14P".	
2	38	Charger	10/30	Compal	for power request	PQ104 swap the PQ104 1,3 Pin	
3	39	3V/5V	10/30	Compal	for power request	Change PR301 to 13.7K modify output voltage	
4	39	3V/5V	10/30	Compal	for power request	Change PR305 to 180K modify OCP	
5	39	3V/5V	10/30	Compal	for power request	Change PR306 to 150K modify OCP	
6	39	3V/5V	10/30	Compal	for power request	Change PR311 to 620K	
7	39	3V/5V	10/30	Compal	for power request	Change PR315 to 604K modify sequence	
8	41	+1.1VSP	10/30	Compal	for power request	Change PR510 to 19.1K modify OCP	
9	41	+1.2VALWP	10/30	Compal	for power request	Change PR511 to 19.1K modify OCP	
10	38	Charger	10/30	Compal	for power request	Del PR119	
11	43	CPU_CORE	10/30	Compal	for power request	Change PC202 to B2 type for ME limit	
12	43	CPU_CORE	10/30	Compal	for power request	Change PR223 to 17.8K and PR224 to 100K modify OCP	
13	43	CPU_CORE	10/30	Compal	for power request	Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation	
14	37	DC connector	10/30	Compal	for power request	Add PR3,PD4,PC12 for ADP_ID function	
15	39	3V/5V	10/30	Compal	for power request	Add PR317,PR318	
16	38	Charger	10/30	Compal	for power request	Change net from +3VLP to +3VL	
17	41	+1.1VSP	10/30	Compal	for power request	Change PR513 to 21K for HW power scquence.	

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HW4 Product Improvement Record (P.I.R.)

RTC



PCB



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