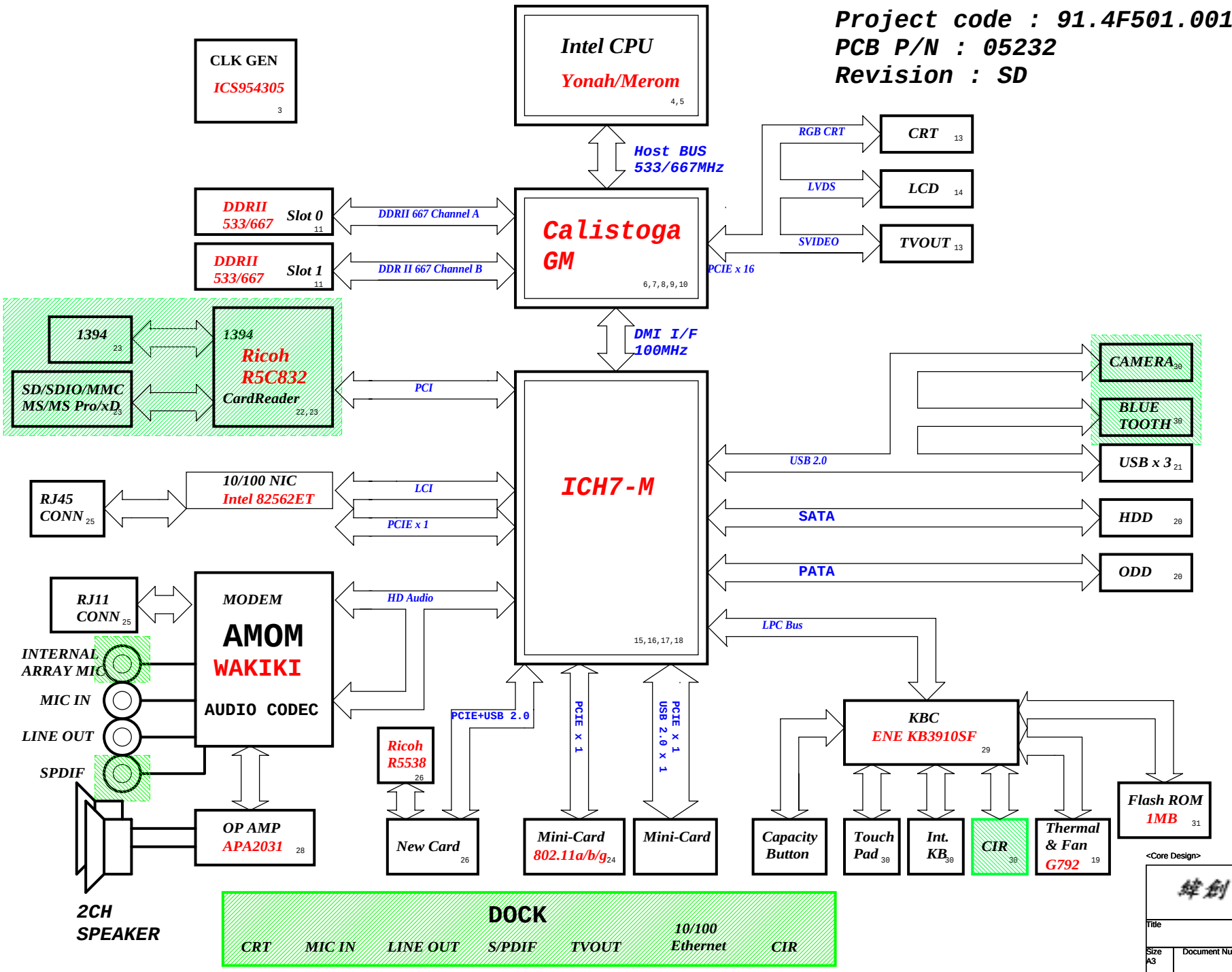
Akita Block Diagram

Project code : 91.4F501.001
PCB P/N : 05232
Revision : SD



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: **Block Diagram**

Size: A3 | Document Number: Akita | Rev: SD

Date: Monday, February 06, 2006 | Sheet 1 of 39

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

125CV Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

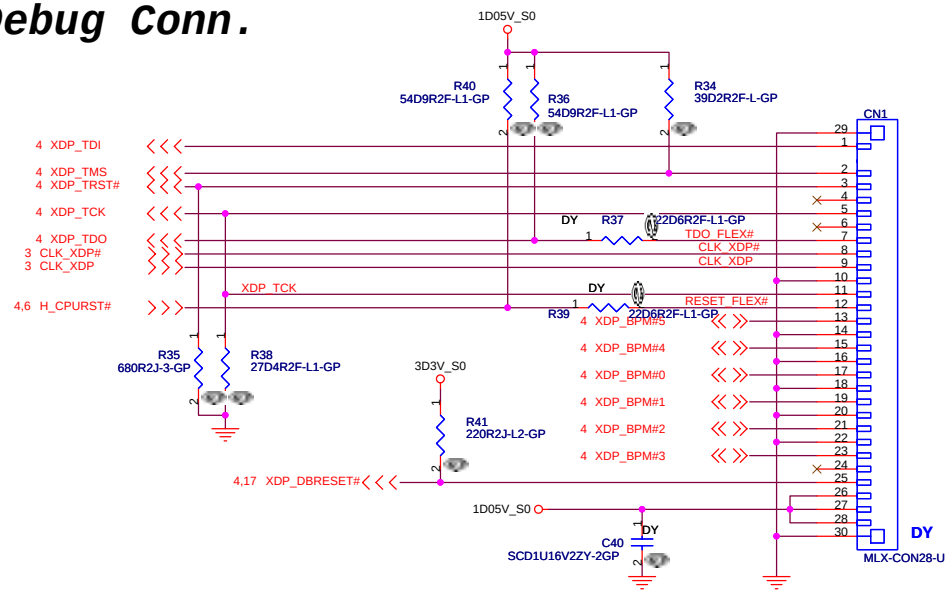
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

11.18.2004: mini card not ready

ITP Debug Conn.



<Core Design>

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Title	ITP	
Size A3	Document Number: Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 2 of 39	

IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

<Core Design>

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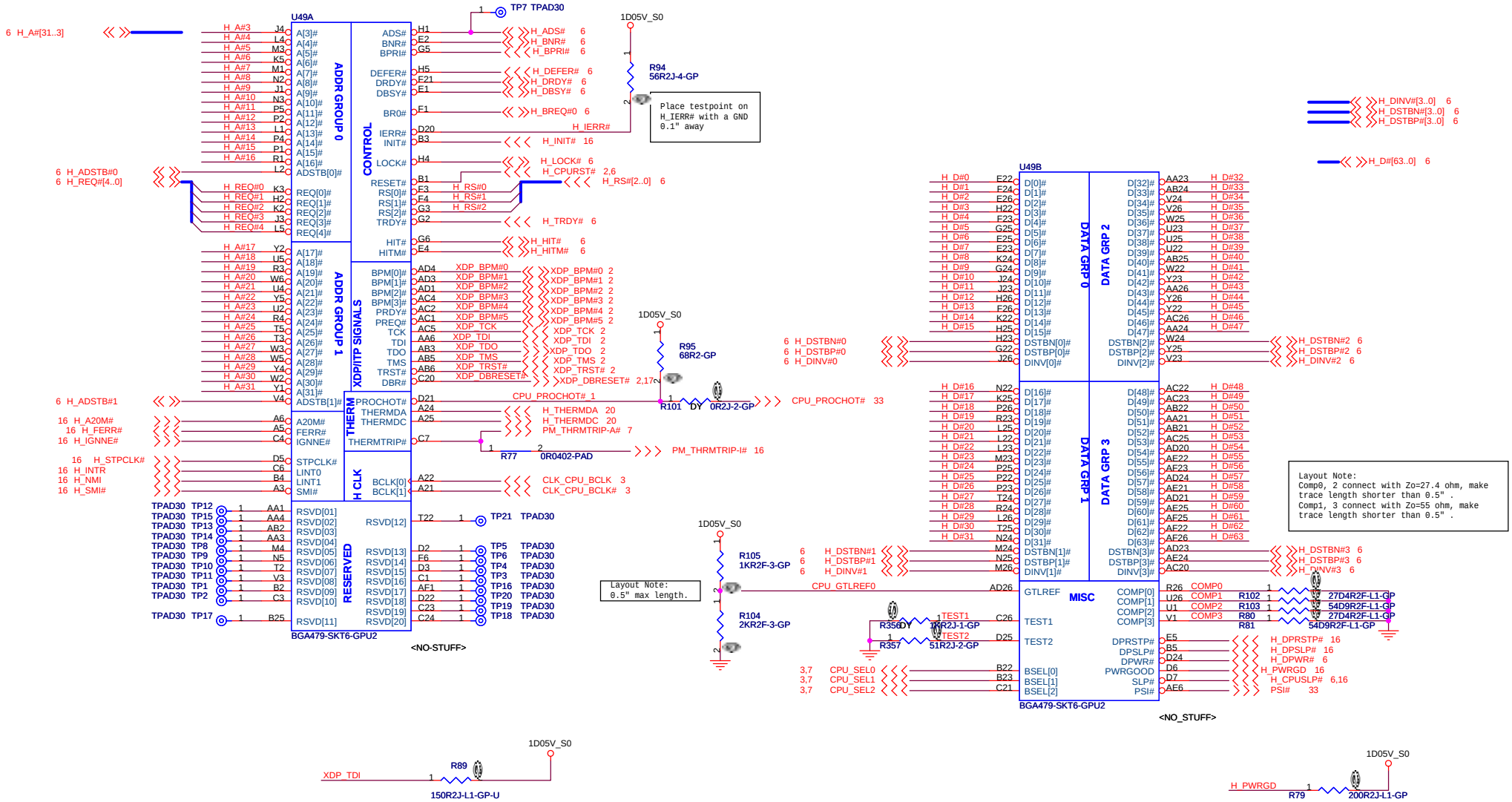
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator (IDTCV125PA)

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 3 of 39



<Core Design>

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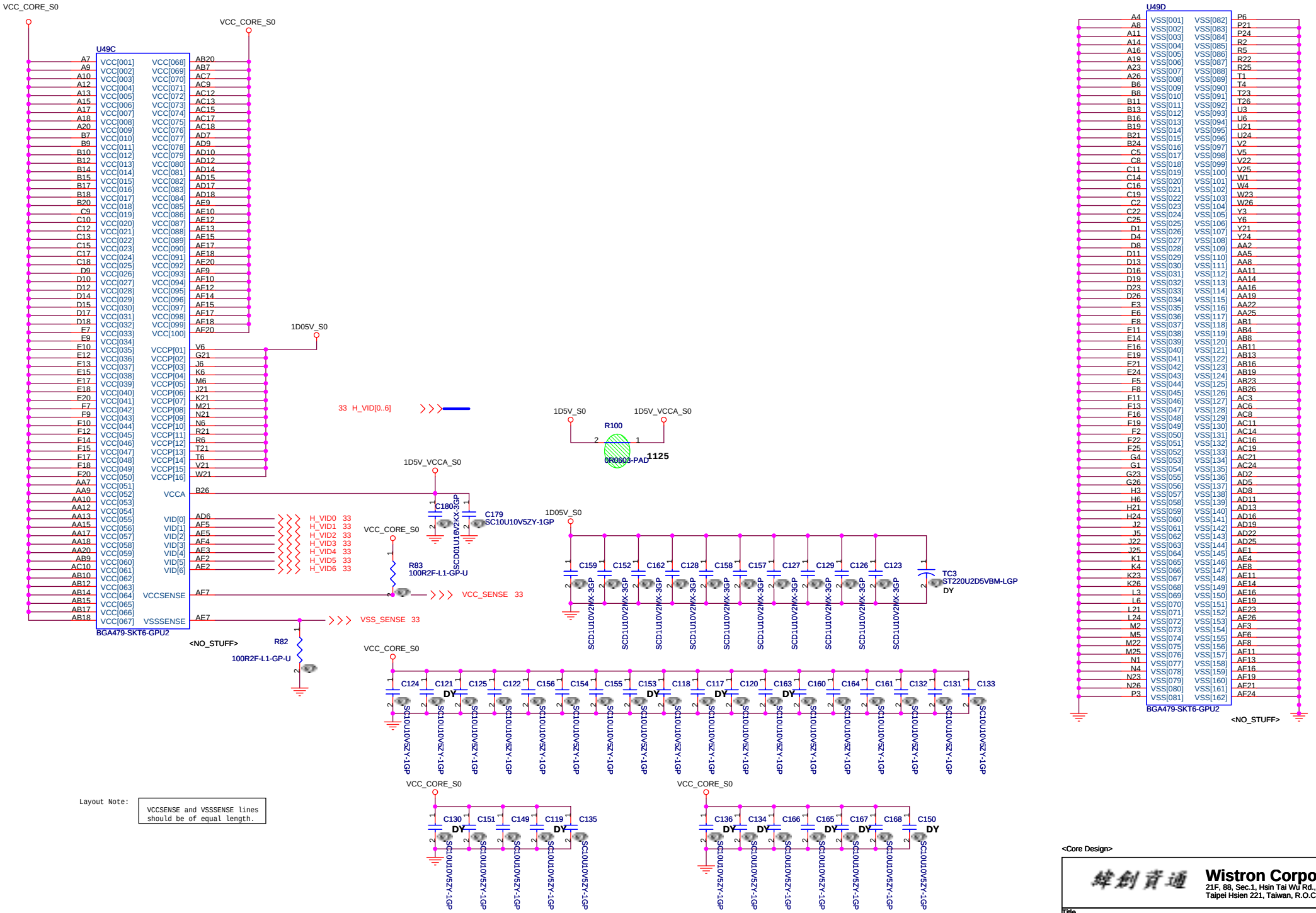
Title: **CPU (1 of 2)**

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 4 of 39


VCC_CORE_S0
U49C
BGA479-SKT6-GPU2
1D05V_S0
1D05V_VCCA_S0
33 H_VID[0..6]
R100
0R0603-PAD
1125
C180
SCD0U16V2KX-3GP
C179
SC10U10V5ZY-1GP
R83
100R2F-L1-GP-U
VCC_SENSE 33
VSS_SENSE 33
R82
100R2F-L1-GP-U
<NO_STUFF>
TC3
ST220U2D5VBM-LGP
DY
SCD1U10V2MX-3GP
SC10U10V5ZY-1GP
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
U49D
BGA479-SKT6-GPU2
<NO_STUFF>
<Core Design>
Wistron Corporation
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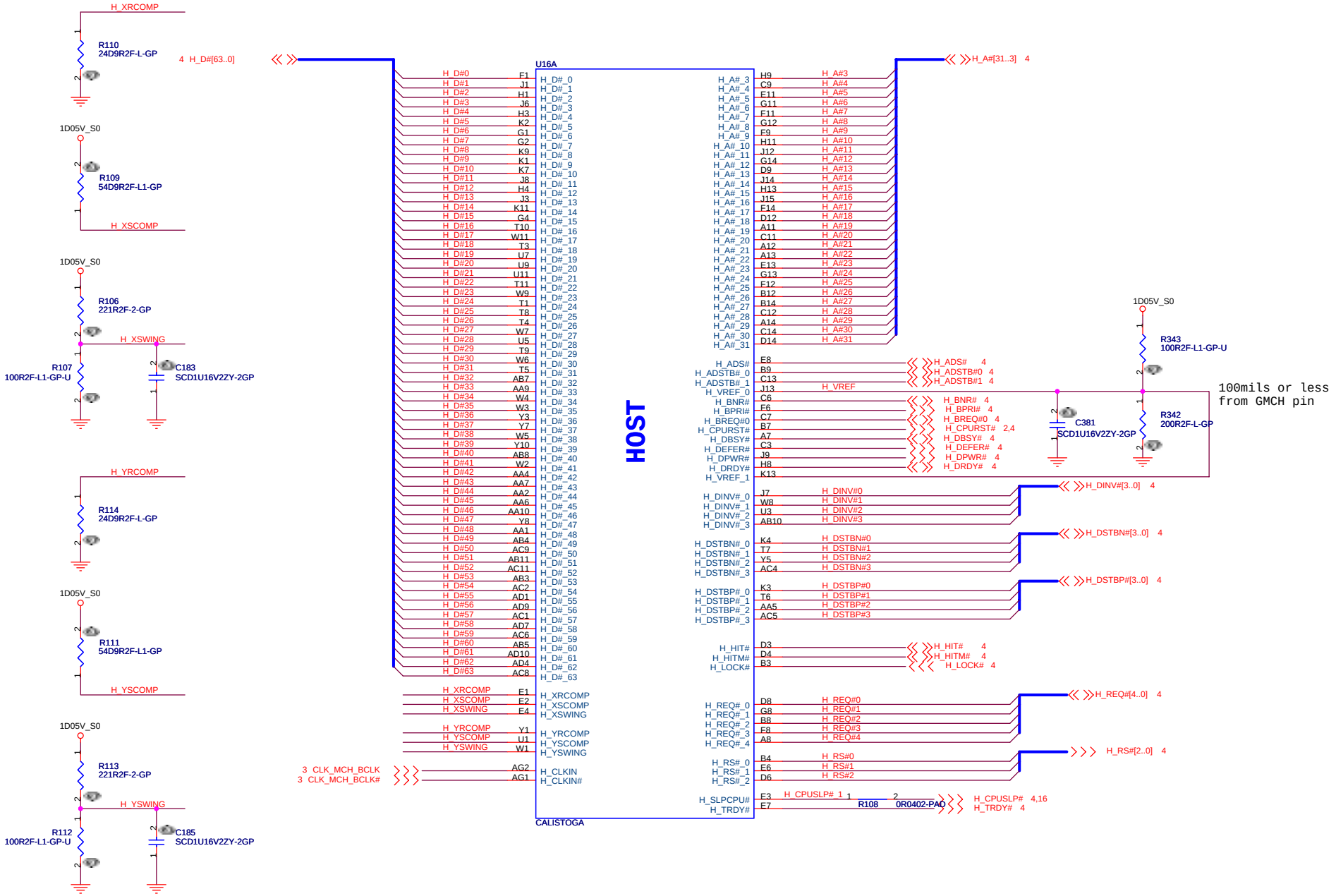
Title
CPU (2 of 2)
Size A3
Document Number
Akita
Rev SD
Date: Friday, March 31, 2006
Sheet 5 of 39



Place them near to the chip

<Core Design>

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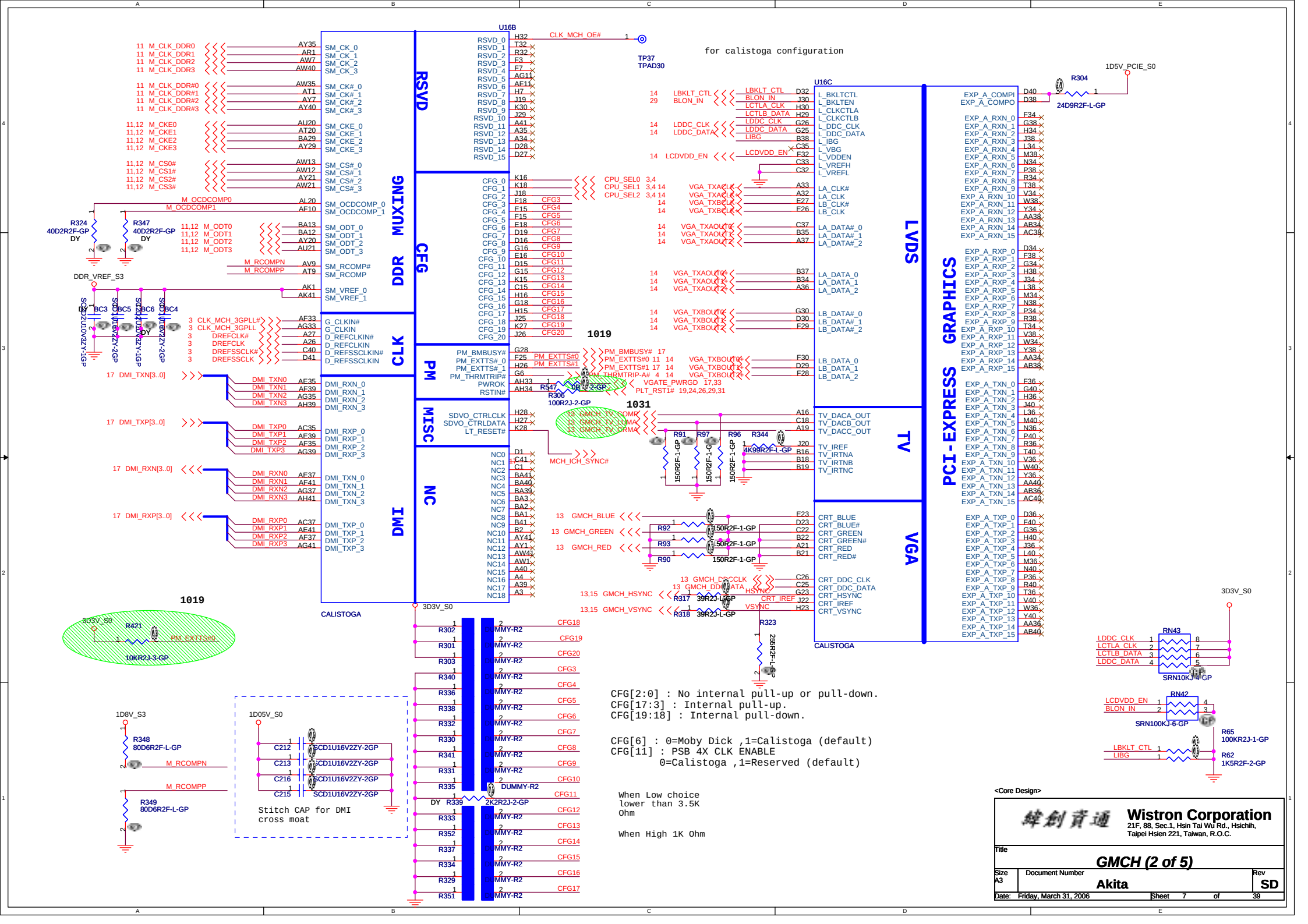
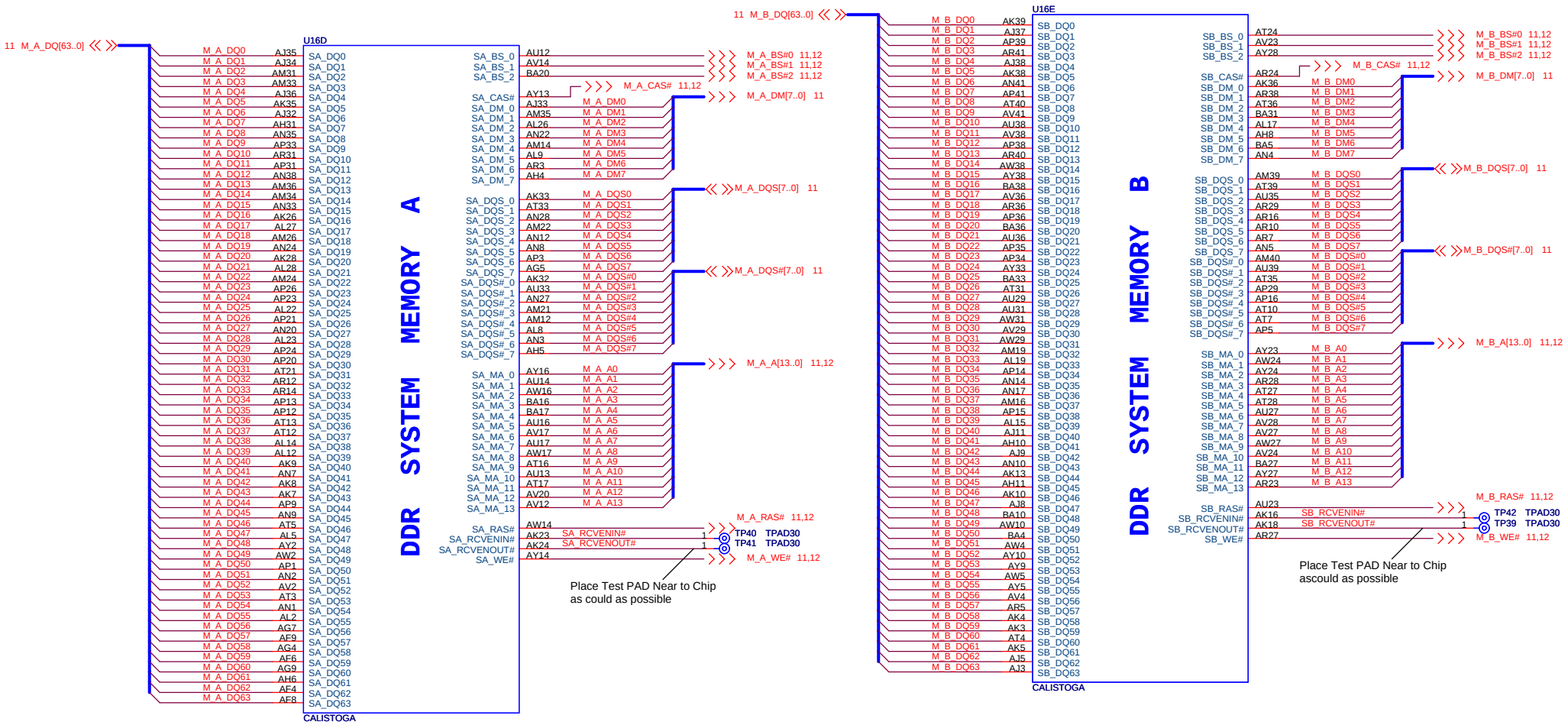
Title: GMCH (1 of 5)

Size: A3 | Document Number: Akita | Rev: SD

Date: Monday, February 06, 2006 | Sheet 6 of 39


U16B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
CALISTOGA
U16C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
for calistoga configuration
TP37
TPAD30
CLK_MCH_OE#
1019
1031
DDR_VREF_S3
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS0#
M_CS1#
M_CS2#
M_CS3#
M_ODCOMP0
M_ODCOMP1
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_RCOMPN
M_RCOMPP
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
DREFCLK#
DREFCLK
DREFSSCLK#
DREFSSCLK
DMI_TXN[3..0]
DMI_TXP[3..0]
DMI_RXN[3..0]
DMI_RXP[3..0]
PM_BMBUSY#
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP#
PWROK
RSTIN#
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
MCH_ICH_SYNC#
PLT_RST1# 19,24,26,29,31
LBKLT_CTL
BLON_IN
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LIBG
LCDVDD_EN
CPU_SEL0 3,4
CPU_SEL1 3,4
CPU_SEL2 3,4
VGA_TXACLK#
VGA_TXACLK
VGA_TXBCLK#
VGA_TXBCLK
VGA_TXAOUT0#
VGA_TXAOUT1#
VGA_TXAOUT2#
VGA_TXAOUT0
VGA_TXAOUT1
VGA_TXAOUT2
VGA_TXBOUT0#
VGA_TXBOUT1#
VGA_TXBOUT2#
VGA_TXBOUT0
VGA_TXBOUT1
VGA_TXBOUT2
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
GMCH_TV_COMP
GMCH_TV_LUMA
GMCH_TV_CRMA
GMCH_BLUE
GMCH_GREEN
GMCH_RED
GMCH_HSYNC
GMCH_VSYNC
1D5V_PCIE_S0
R304
24D9R2F-L-GP
3D3V_S0
1D8V_S3
1D05V_S0
R324 40D2R2F-GP DY
R347 40D2R2F-GP DY
R348 80D6R2F-L-GP
R349 80D6R2F-L-GP
R421 10KR2J-3-GP
R547 0R2J-2-GP
R308 100R2J-2-GP
R339 2K2R2J-2-GP
R317 39R2J-L-GP
R318 39R2J-L-GP
R323 25R2F-L-GP
R91 R97 R96 R344 150R2F-1-GP 4K99R2F-L-GP
R92 R93 R90 150R2F-1-GP
RN43 SRN10KJ-4-GP
RN42 SRN100KJ-6-GP
R65 100KR2J-1-GP
R62 1K5R2F-2-GP
SCD1U16V2ZY-2GP
DUMMY-R2
Stitch CAP for DMI cross moat
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-down.
CFG[19:18] : Internal pull-down.
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)
When Low choice lower than 3.5K Ohm
When High 1K Ohm
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number
Akita
Rev SD
Date: Friday, March 31, 2006
Sheet 7 of 39



<Core Design>

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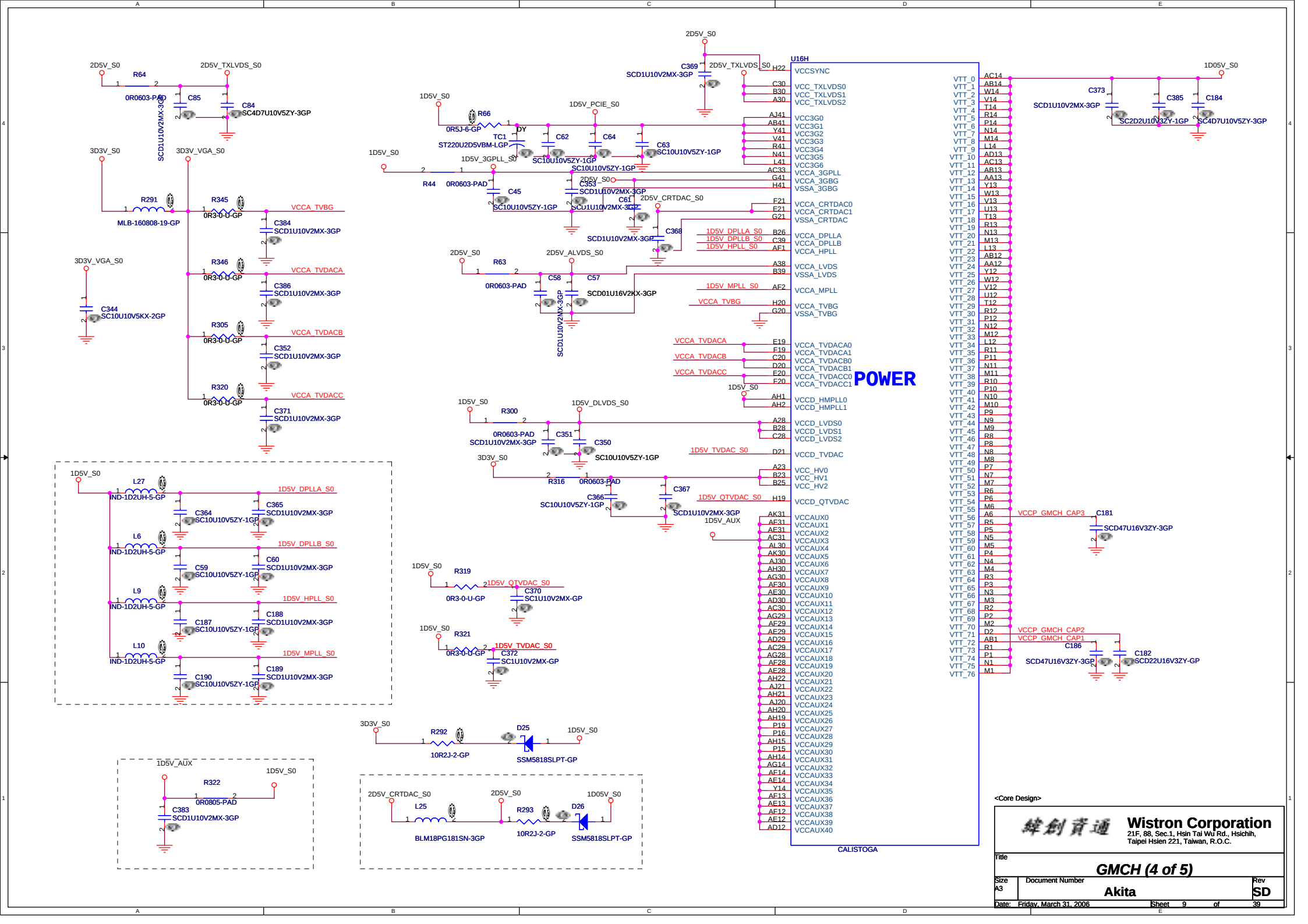
Title: GMCH (3 of 5)

Size: A3 | Document Number: Akita | Rev: SD

Date: Monday, February 06, 2006 | Sheet 8 of 39


POWER
U16H
CALISTOGA
<Core Design>
Wistron Corporation
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Title
GMCH (4 of 5)
Size A3
Document Number
Akita
Rev SD
Date: Friday, March 31, 2006
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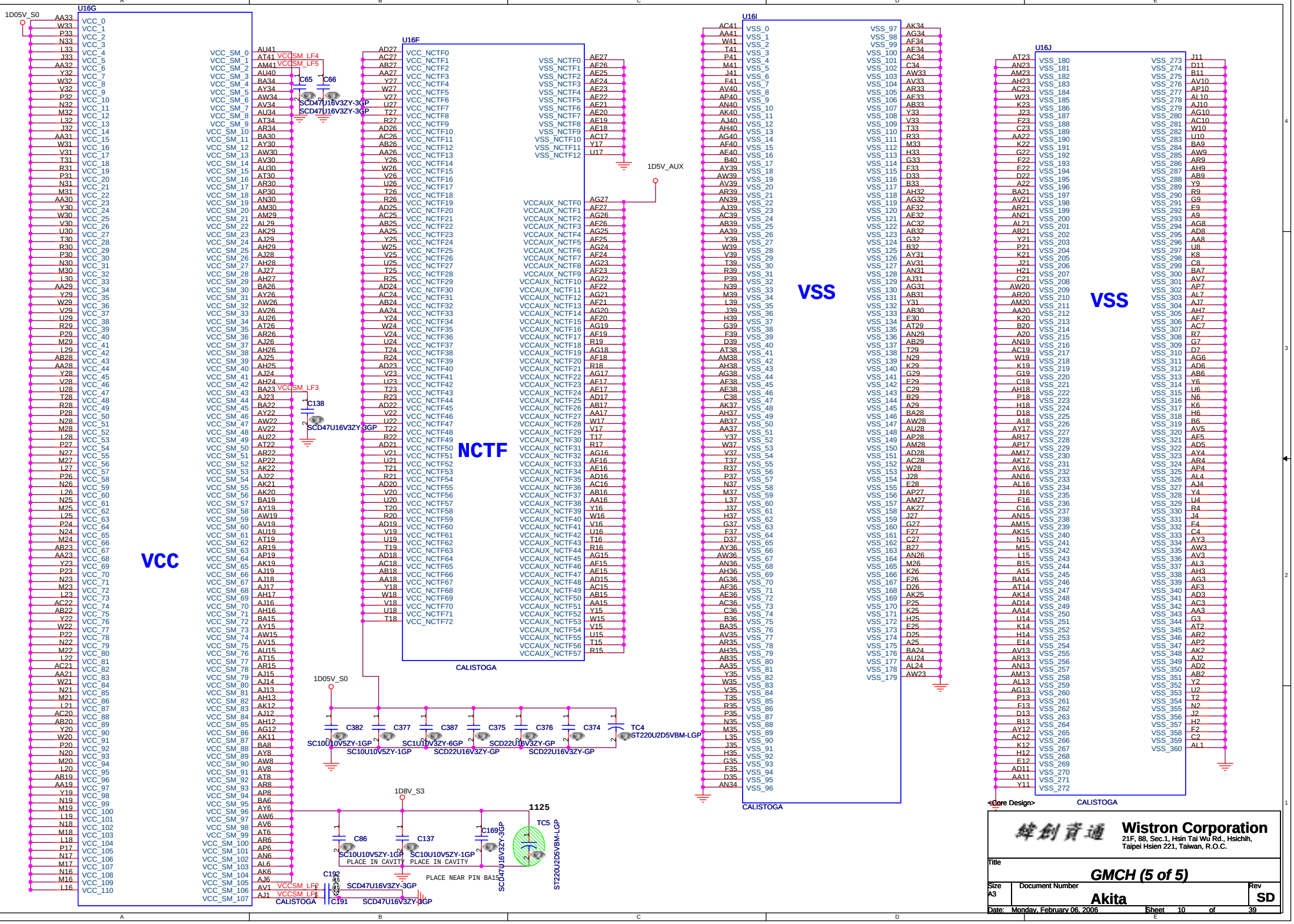

Core Design	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GMCH (5 of 5)
Size	A3
Document Number	Akita
Rev	SD
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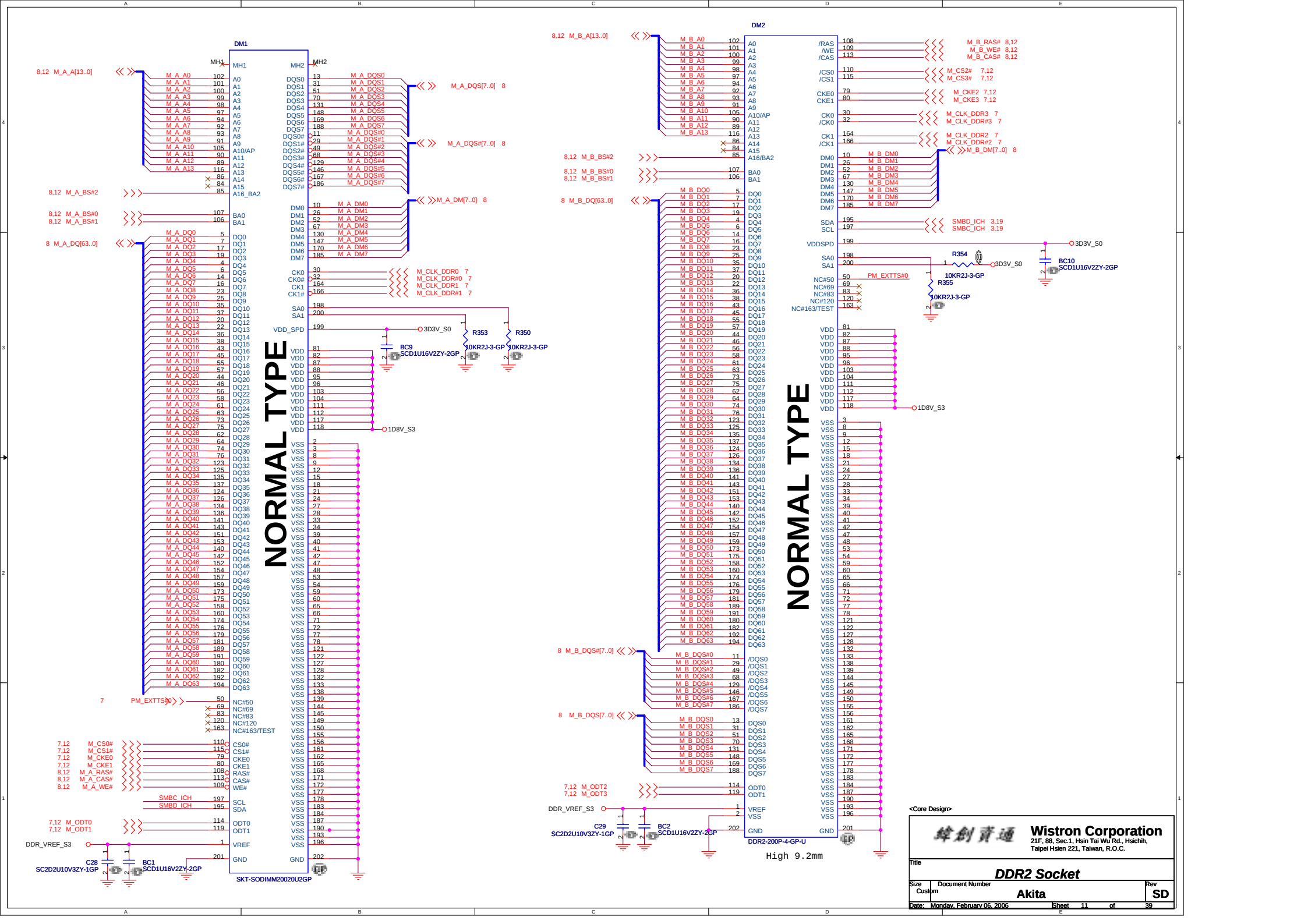

<Core Design>

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Title: ***DDR2 Socket***

Size	Document Number	Rev
Custom	Akita	SD

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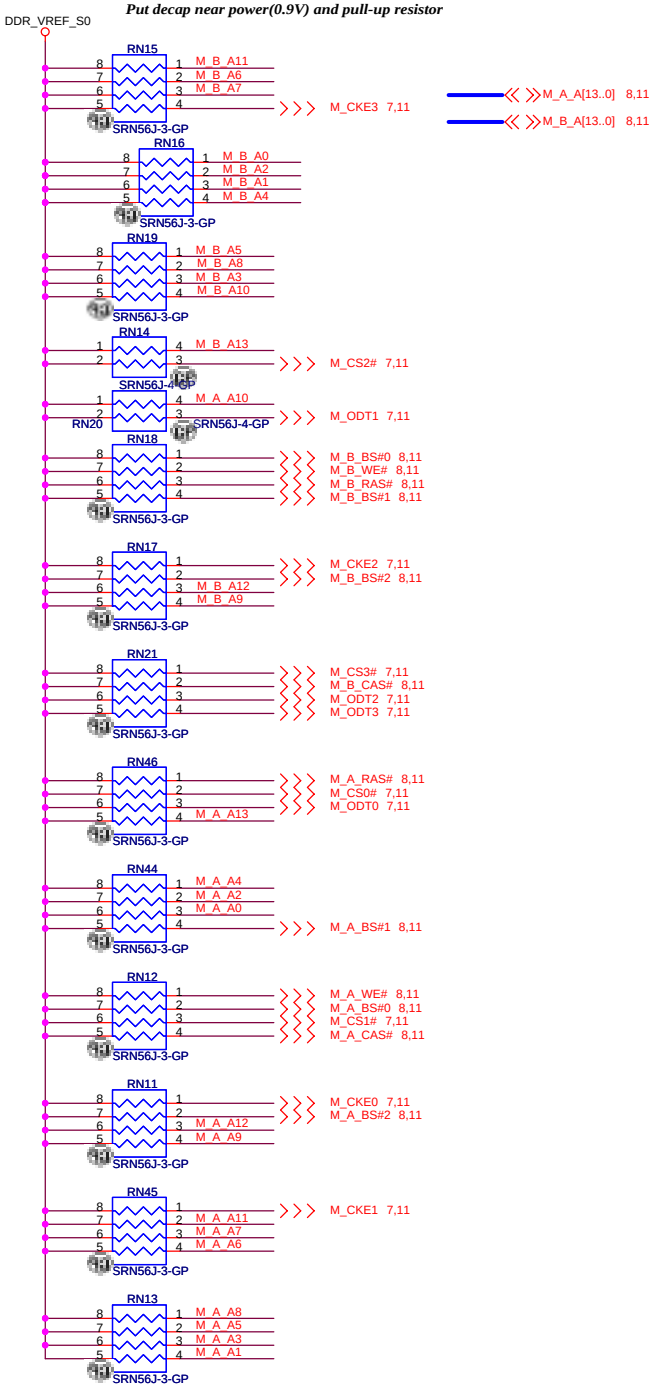
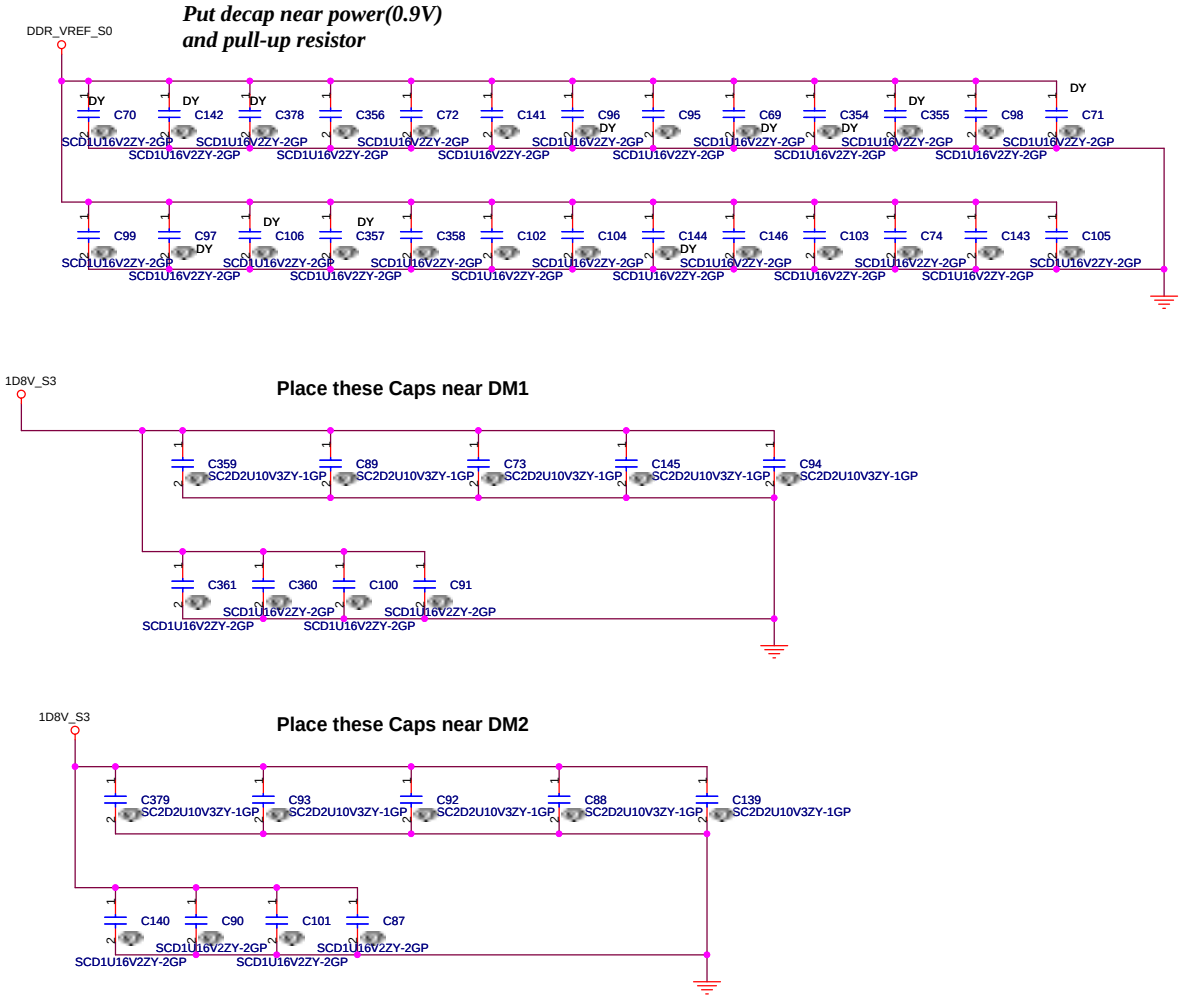
PARALLEL TERMINATION



Decoupling Capacitor



<Core Design>

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Title: DDR2 Termination Resistor

Size	Document Number	Rev
A3	Akita	SD

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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

1122

7 GMCH_RED — L2 BLM18BB470SN1-GP — CRT_R — CRT_R 15
7 GMCH_GREEN — L3 BLM18BB470SN1-GP — CRT_G — CRT_G 15
7 GMCH_BLUE — L1 BLM18BB470SN1-GP — CRT_B — CRT_B 15

R5 150R2F-1-GP, R4 150R2F-1-GP, R3 150R2F-1-GP
C14 SC22P50V2JN-4GP, C15 SC22P50V2JN-4GP, C11 SC22P50V2JN-4GP
C12 SC2P50V2CN-GP, C13 SC2P50V2CN-GP, C9 SC2P50V2CN-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0 — C10 SCD01U16V2KX-3GP — F1 FUSE-1D1A6V-8GP — 5V_S0
D3 CH751H-40PT-1GP — 1124 — 5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U
CRT_R, CRT_G, CRT_B
DDC_DATA_CON, JVGA_HS, JVGA_VS, DDC_CLK_CON
C7 SC33P50V2JN-3GP DY, C6 SC33P50V2JN-3GP DY
C8 SC22P50V2JN-4GP, C1 SC22P50V2JN-4GP

D10 BAV99-7-F-GP DY — DDC_DATA_CON
D9 BAV99-7-F-GP DY — DDC_CLK_CON
5V_CRT1_S0

1124
U2 PACDN009MR-GP-U DY
GMCH_HSYNC, GMCH_VSYNC, CRT_R → CRT_G, CRT_B

5V_S0
C21 SCD1U16V2ZY-2GP
PR_INSERT 15
7,15 GMCH_HSYNC — U5A TSAHCT125PW-GP — HSYNC_5
7,15 GMCH_VSYNC — U5B TSAHCT125PW-GP — VSYNC_5
RN4 SRN33J-5-GP-U — JVGA_HS, JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP
U1 2N7002DW-7F-GP
7 GMCH_DDCDATA ↔ DDC_DATA_CON ↔ DDC_DATA_CON 15
15 DDC_CLK_CON ↔ DDC_CLK_CON ↔ GMCH_DDCCLK 7
RN6 SRN0J-6-GP DY

5V @ ext. CRT side

TV OUT CONN

connector

7 GMCH_TV_CRMA — L18 BLM18BB151SN-1GP — C328 SC10P50V2JN-4GP — C324 SC10P50V2JN-4GP — R272 150R2F-1-GP — TV_CRMA 15
7 GMCH_TV_COMP — L20 BLM18BB151SN-1GP — C326 SC10P50V2JN-4GP — C327 SC10P50V2JN-4GP — R271 150R2F-1-GP — TV_COMP 15
7 GMCH_TV_LUMA — L19 BLM18BB151SN-1GP — C329 SC10P50V2JN-4GP — C325 SC10P50V2JN-4GP — R270 150R2F-1-GP — TV_LUMA 15

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP
TV_LUMA, TV_CRMA, TV_COMP
LUMA, CRMA, COMP, NC#2, NC#5, GND, GND, GND, GND

D2 BAV99-7-F-GP DY — TV_COMP — C3 SCD1U16V2ZY-2GP DY
D1 BAV99-7-F-GP DY — TV_LUMA — C2 SCD1U16V2ZY-2GP DY
D4 BAV99-7-F-GP DY — TV_CRMA — C4 SCD1U16V2ZY-2GP DY
3D3V_S0

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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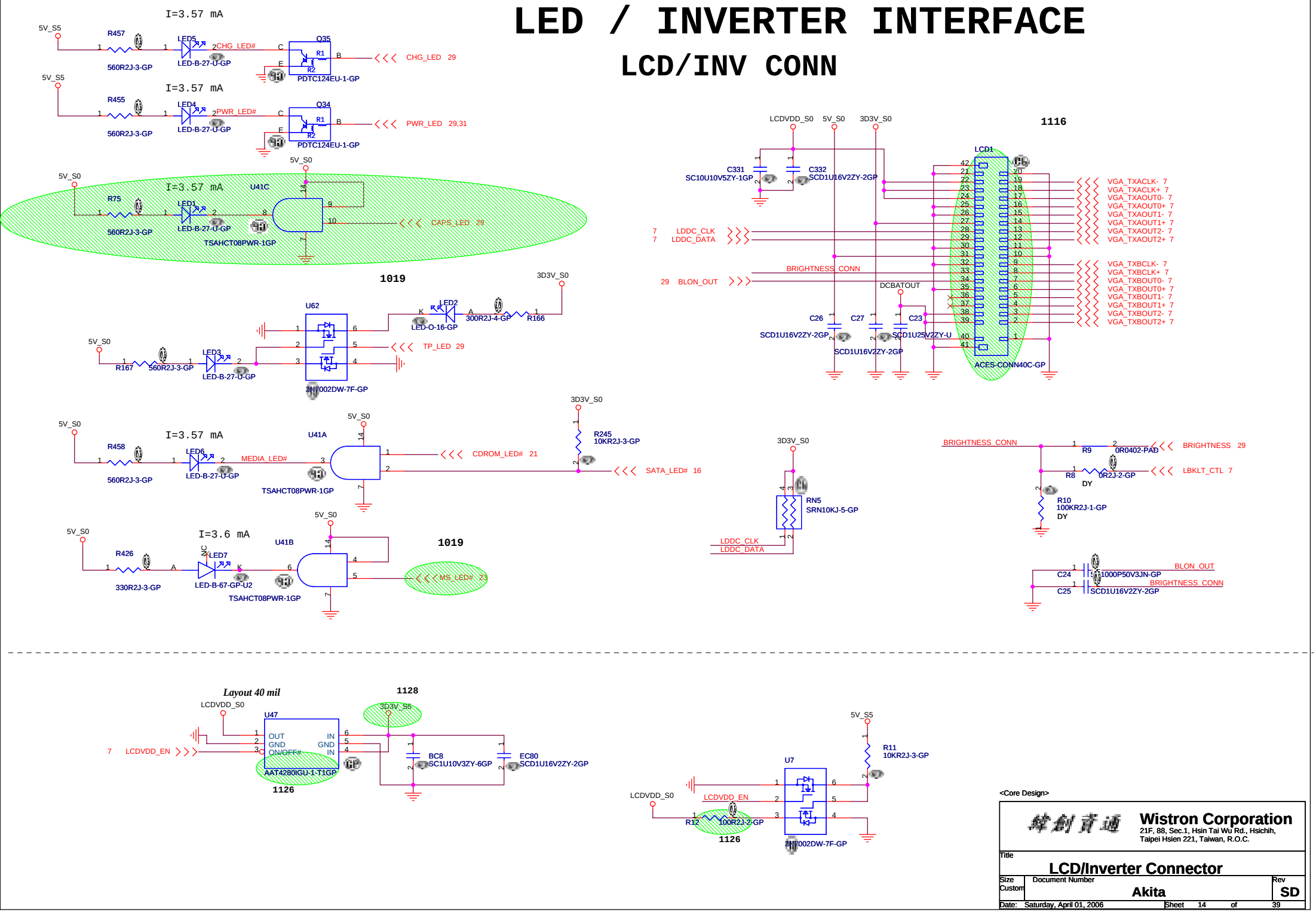
Title: CRT/TV Connector
Size: A3 | Document Number: Akita | Rev: SD
Date: Saturday, April 01, 2006 | Sheet 13 of 39

LED / INVERTER INTERFACE

LCD/INV CONN



<Core Design>

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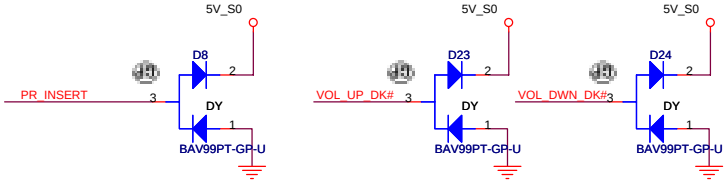
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

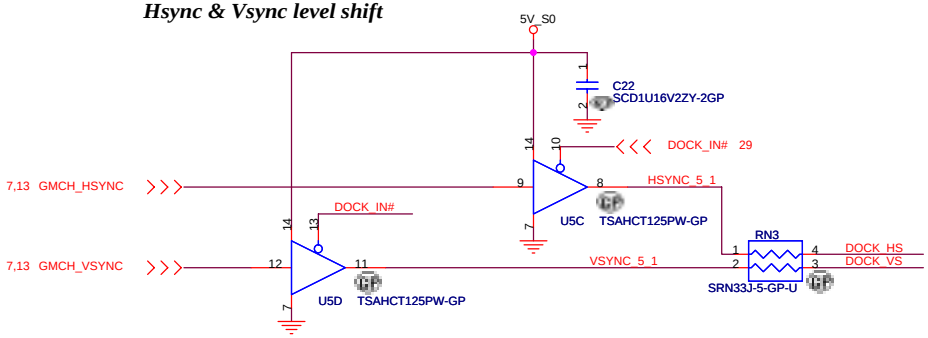
Size: Custom | Document Number: Akita | Rev: SD

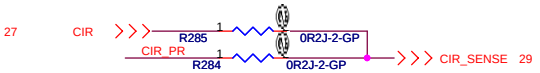
Date: Saturday, April 01, 2006 | Sheet 14 of 39

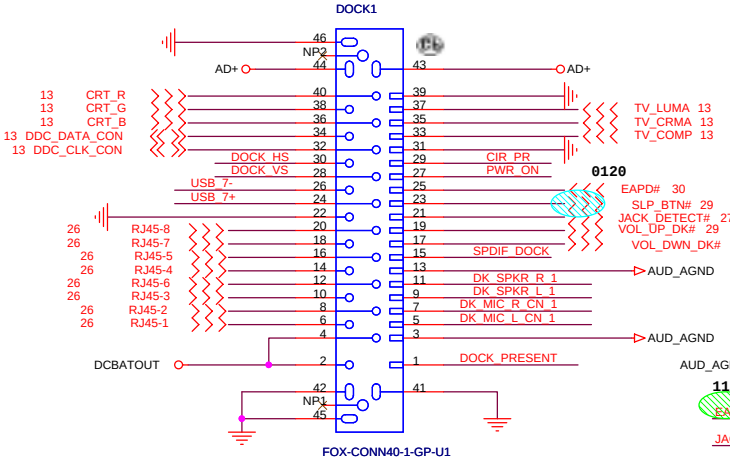
Docking Connector

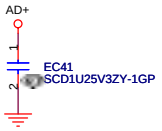


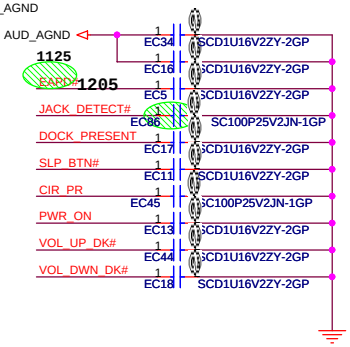
Hsync & Vsync level shift

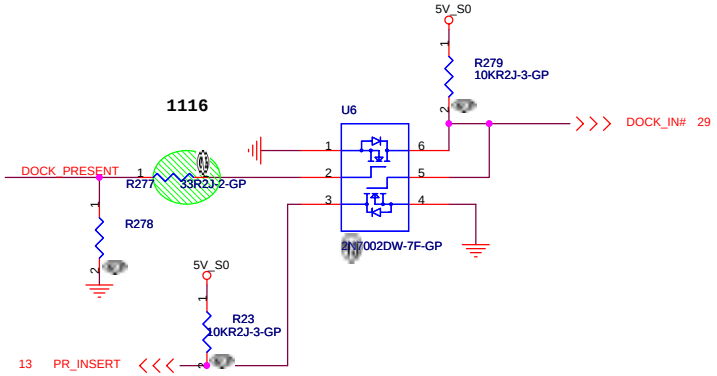


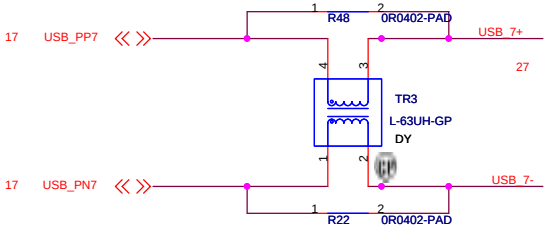


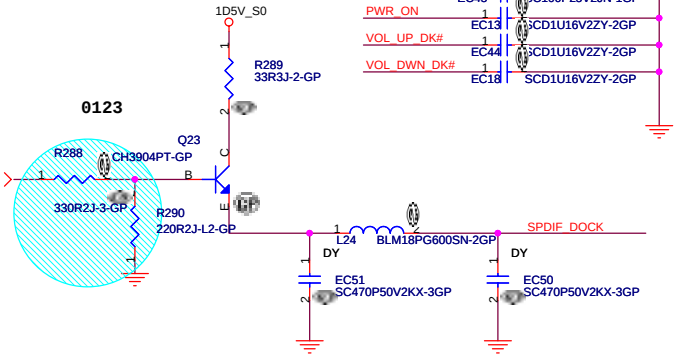


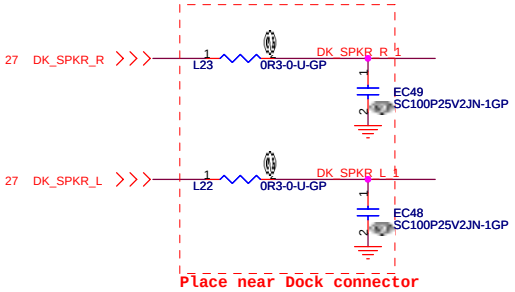


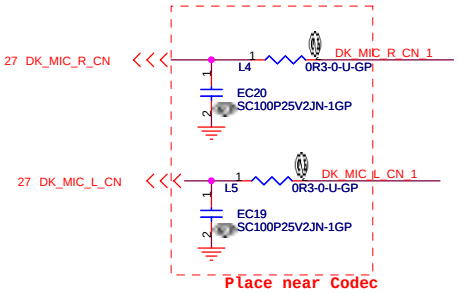


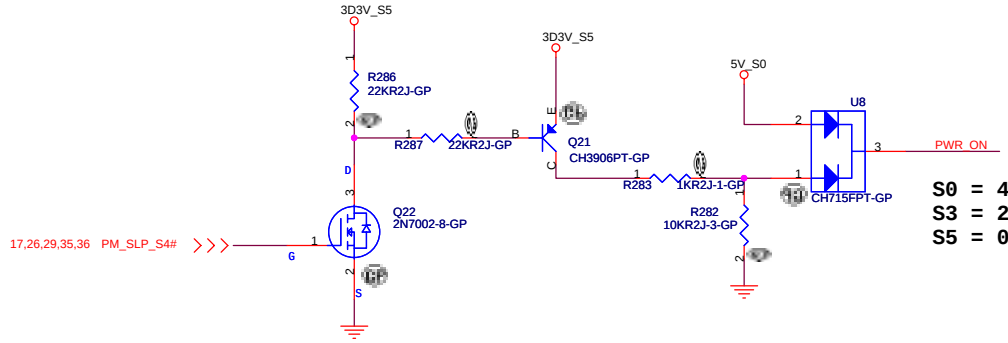












S0 = 4V
S3 = 2.5V
S5 = 0V

<Core Design>

Wistron Corporation
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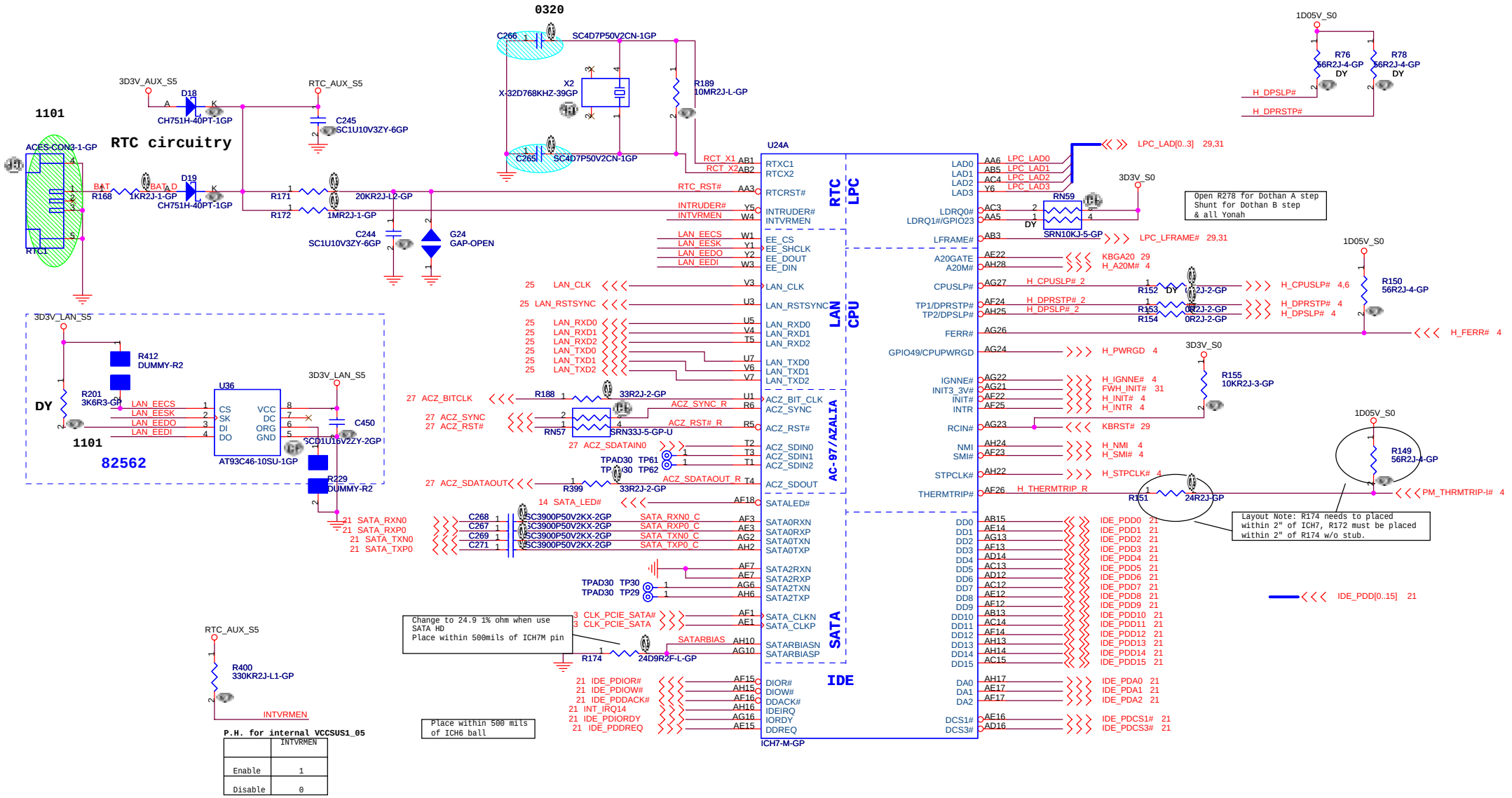
Taipei Hsien 221, Taiwan, R.O.C.

Title	Board to board conn/ Docking	
Size A3	Document Number Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 15 of 39	



<Core Design>

Wistron Corporation
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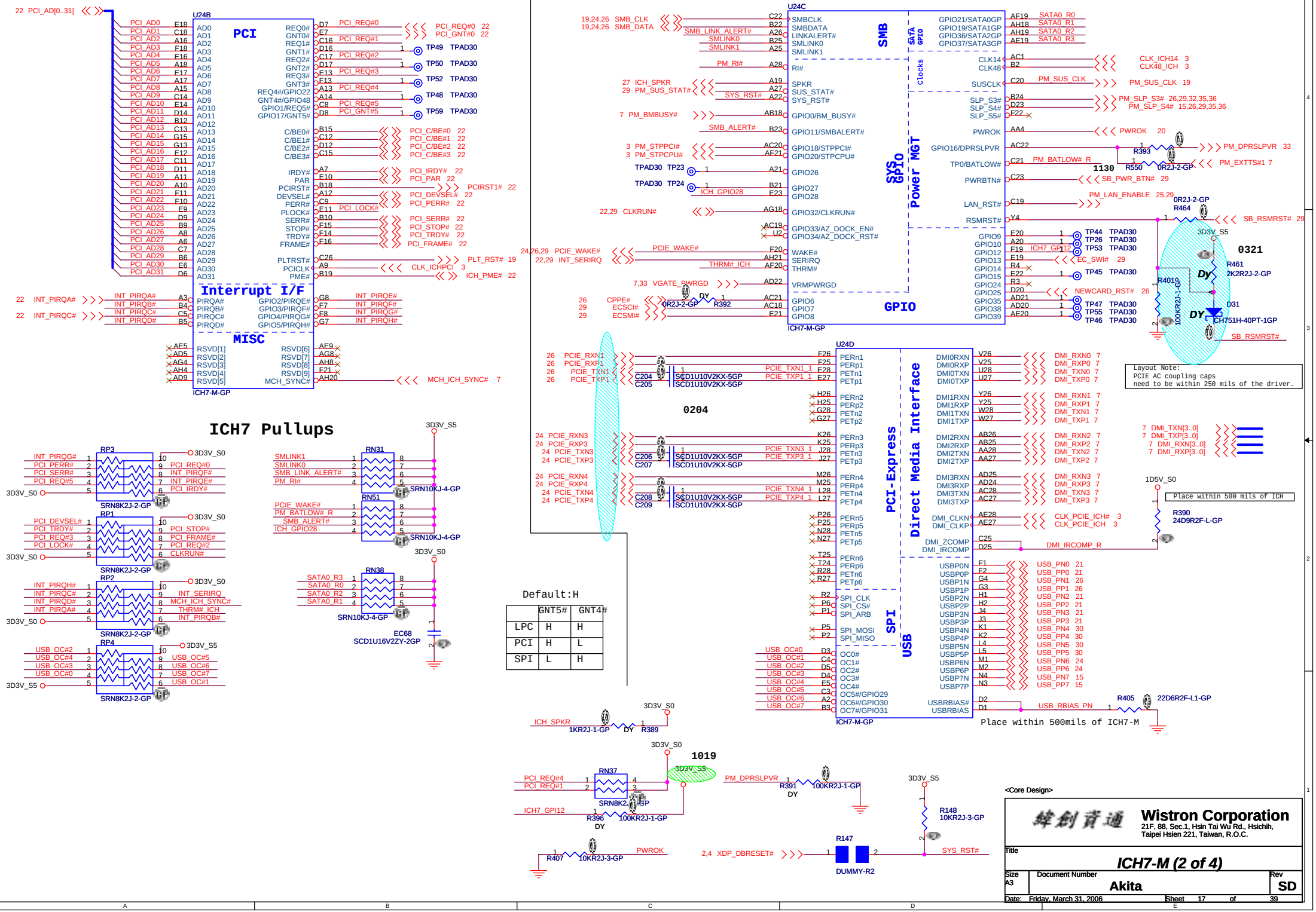
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (1 of 4)

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 16 of 39


U24B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U24C
SMB
SYS GPIO
Power MGT
GPIO
ICH7-M-GP
U24D
PCI-Express
Direct Media Interface
SPI
USB
ICH7 Pullups
Default:H
GNT5#
GNT4#
LPC
PCI
SPI
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500mils of ICH7-M
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH7-M (2 of 4)
Akita
Size A3
Document Number
Rev SD
Date: Friday, March 31, 2006
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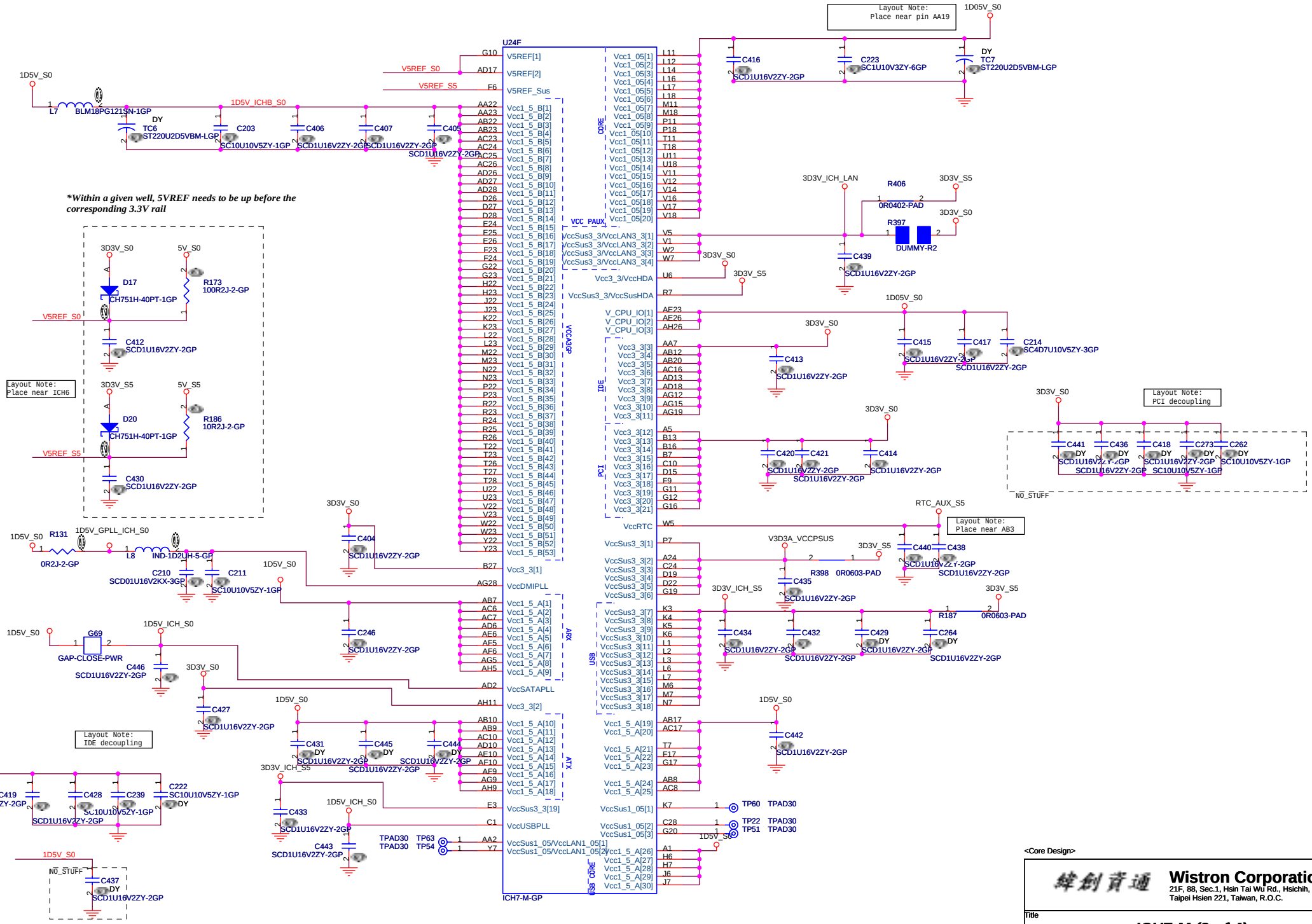
U24F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near AB3
NO_STUFF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
Akita
Rev SD
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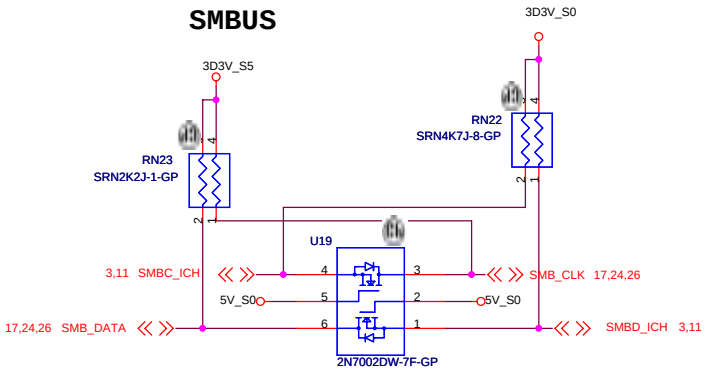
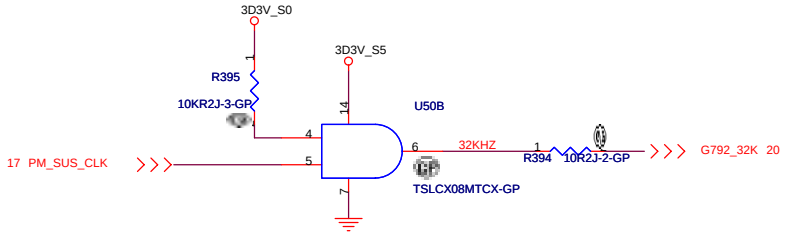
Sheet 18 of 39

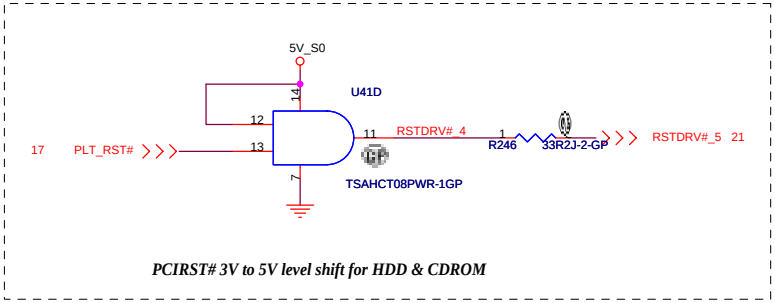
SMBUS



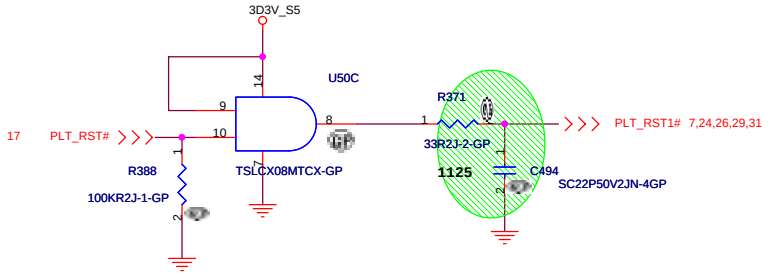
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

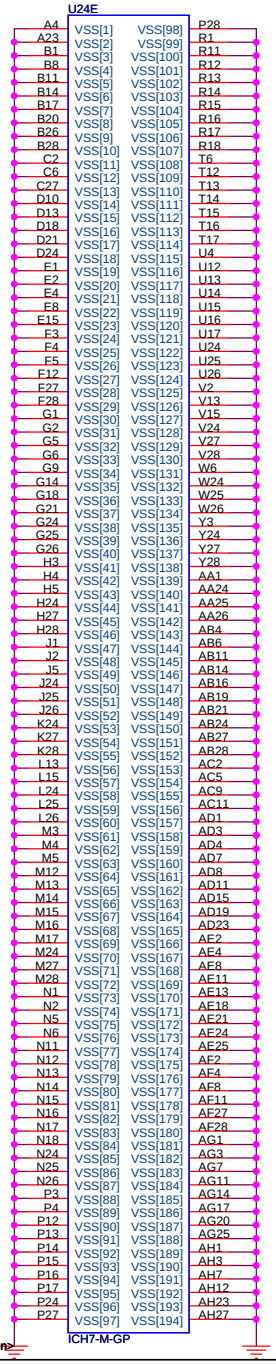
32K suspend clock output





PCIRST# 3V to 5V level shift for HDD & CDROM





<Core Design>

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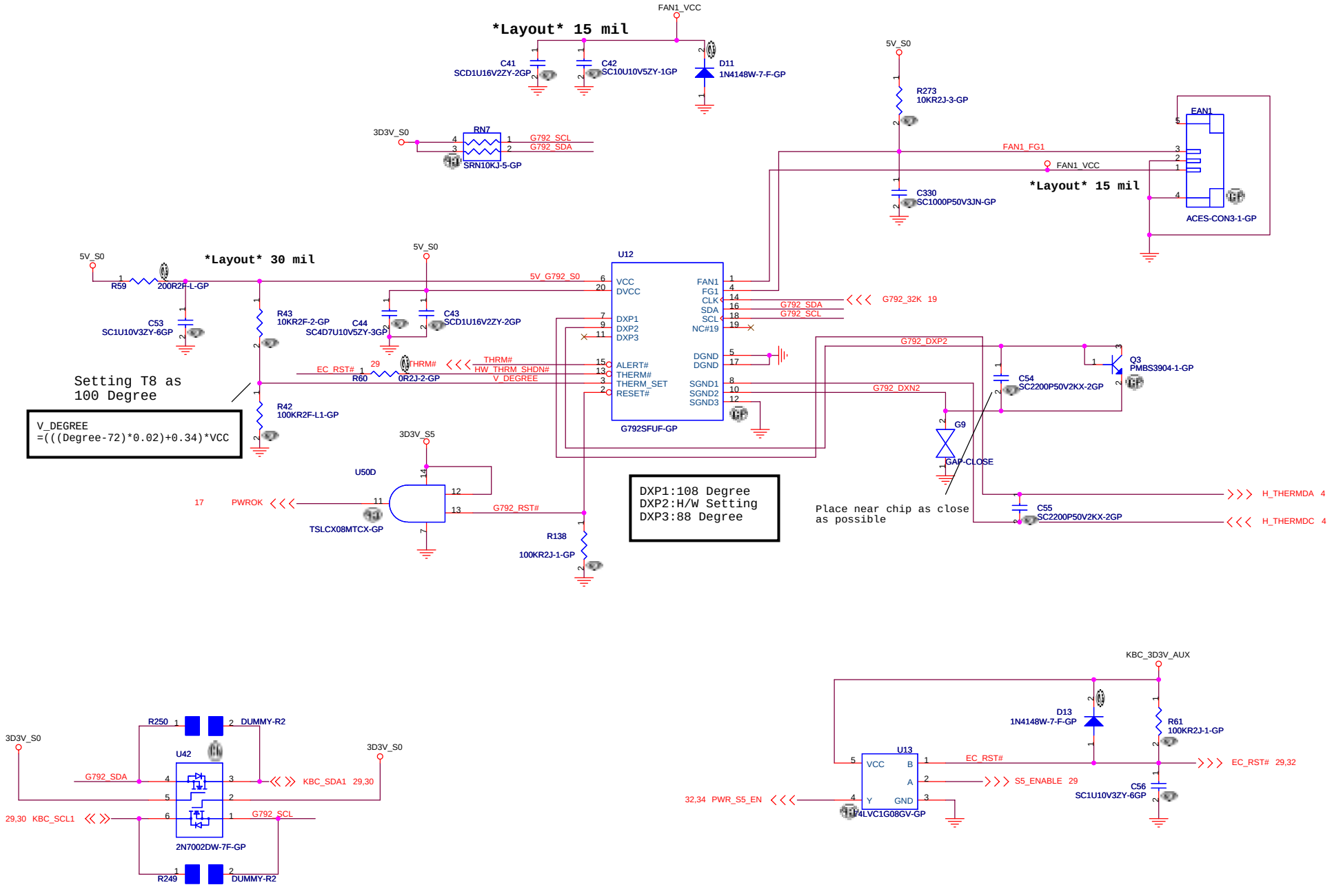
Title: ICH7-M (4 of 4)

Size	Document Number	Rev
A3	Akita	SD

Date: Monday, February 06, 2006 Sheet 19 of 39



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
Custom	Akita	SD

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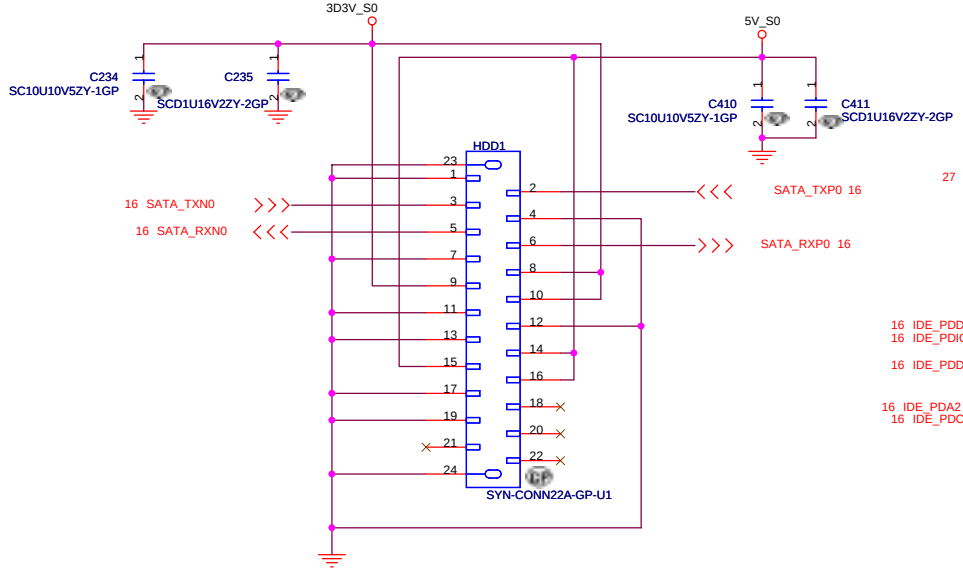
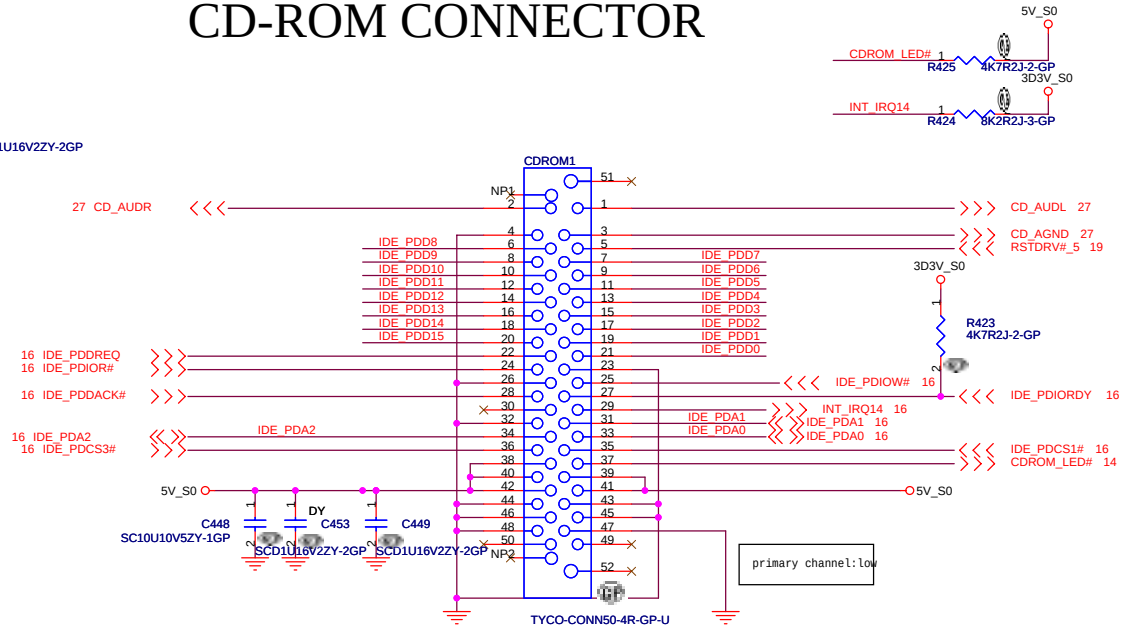
IDE_PDD[0..15] 16

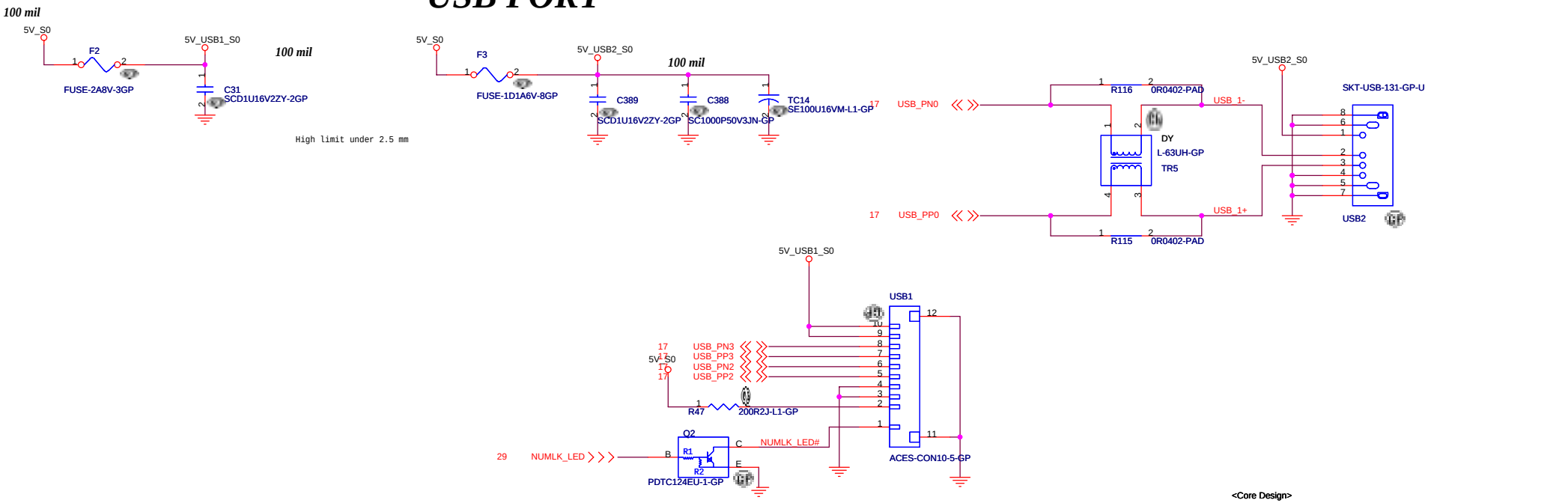
SATA HD Connector



CD-ROM CONNECTOR



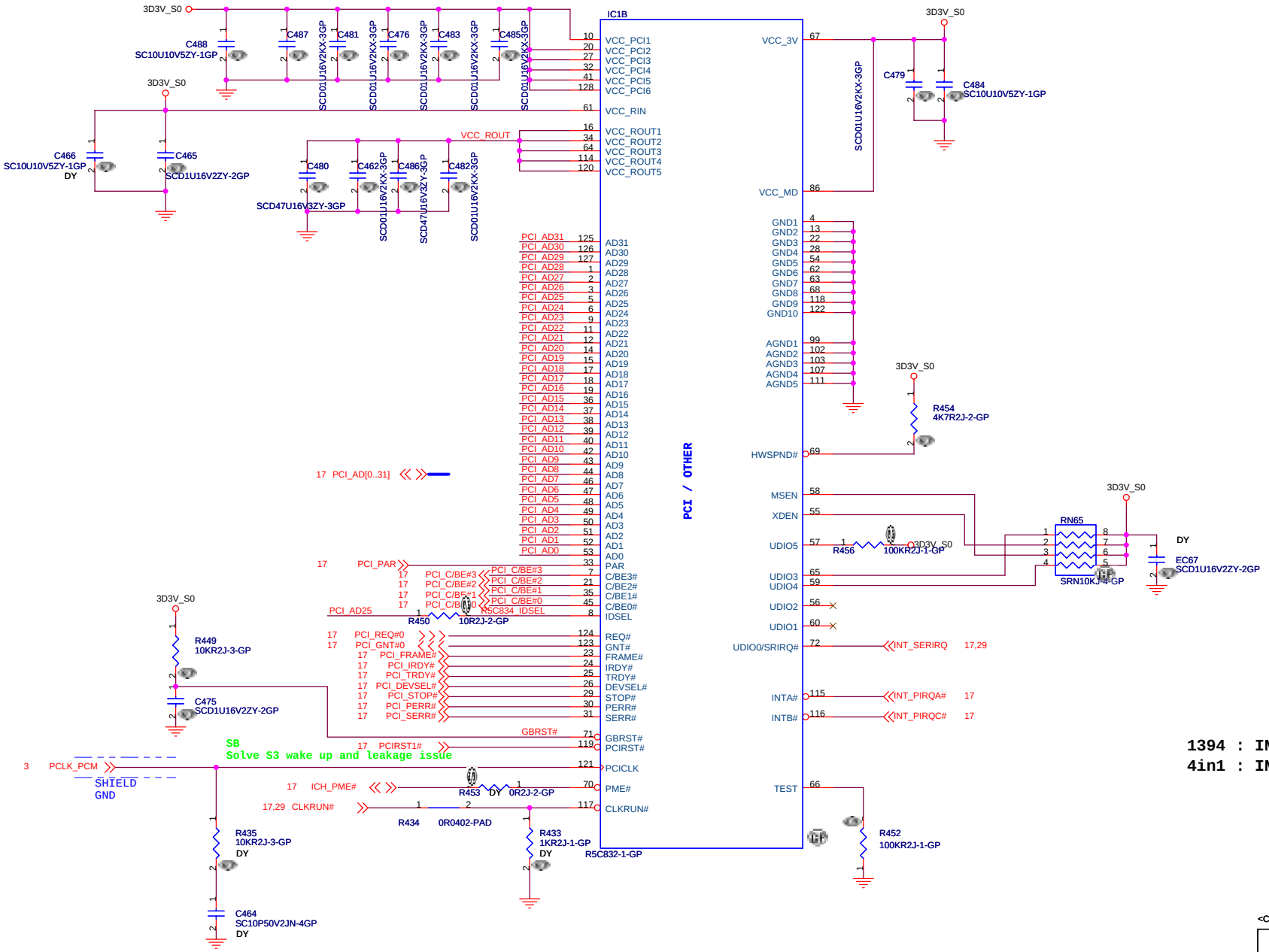
USB PORT



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HD/CDROM	
Size A3	Document Number: Akita	Rev: SD
Date: Friday, March 31, 2006	Sheet 21 of 39	



<Core Design>

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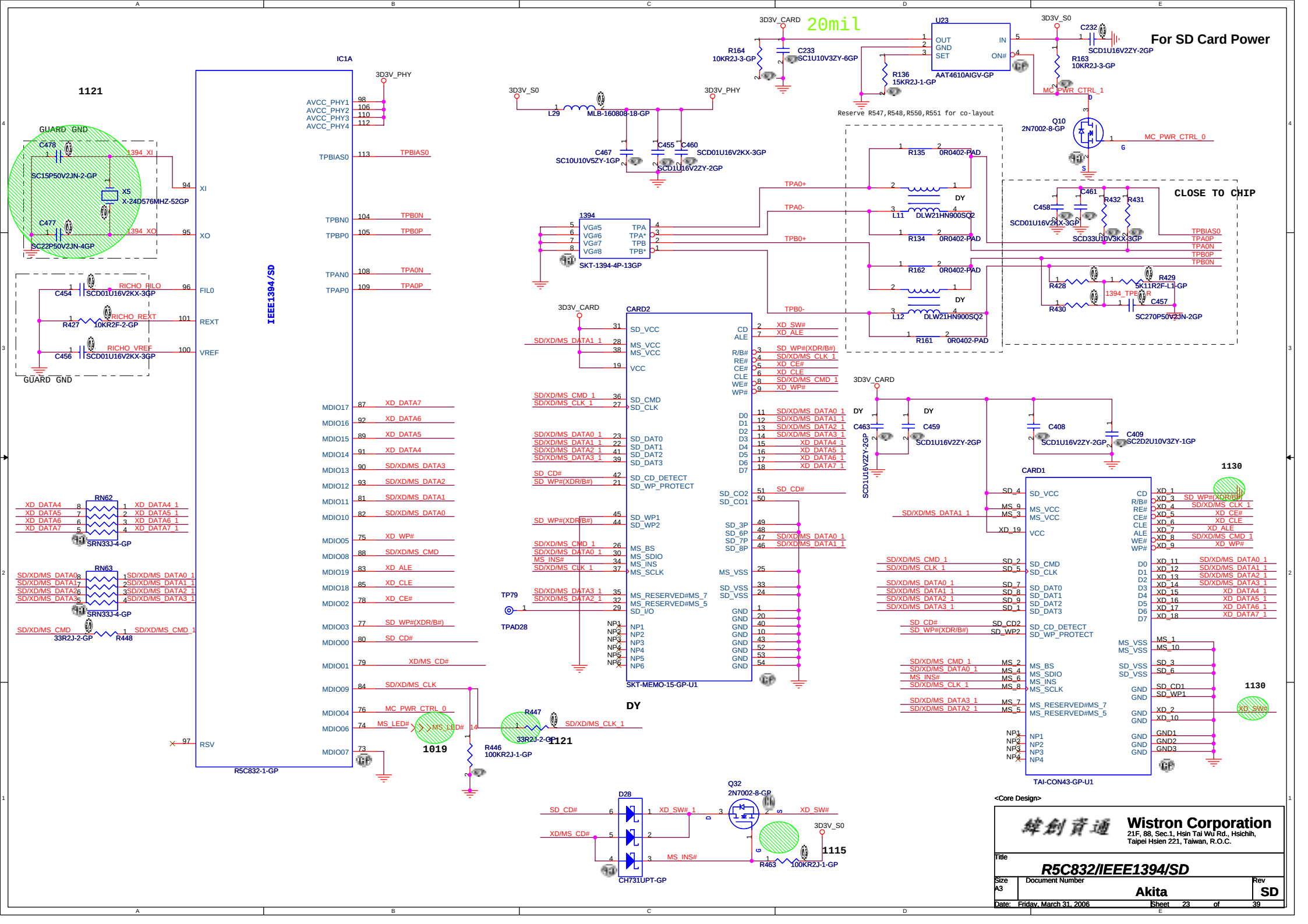
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

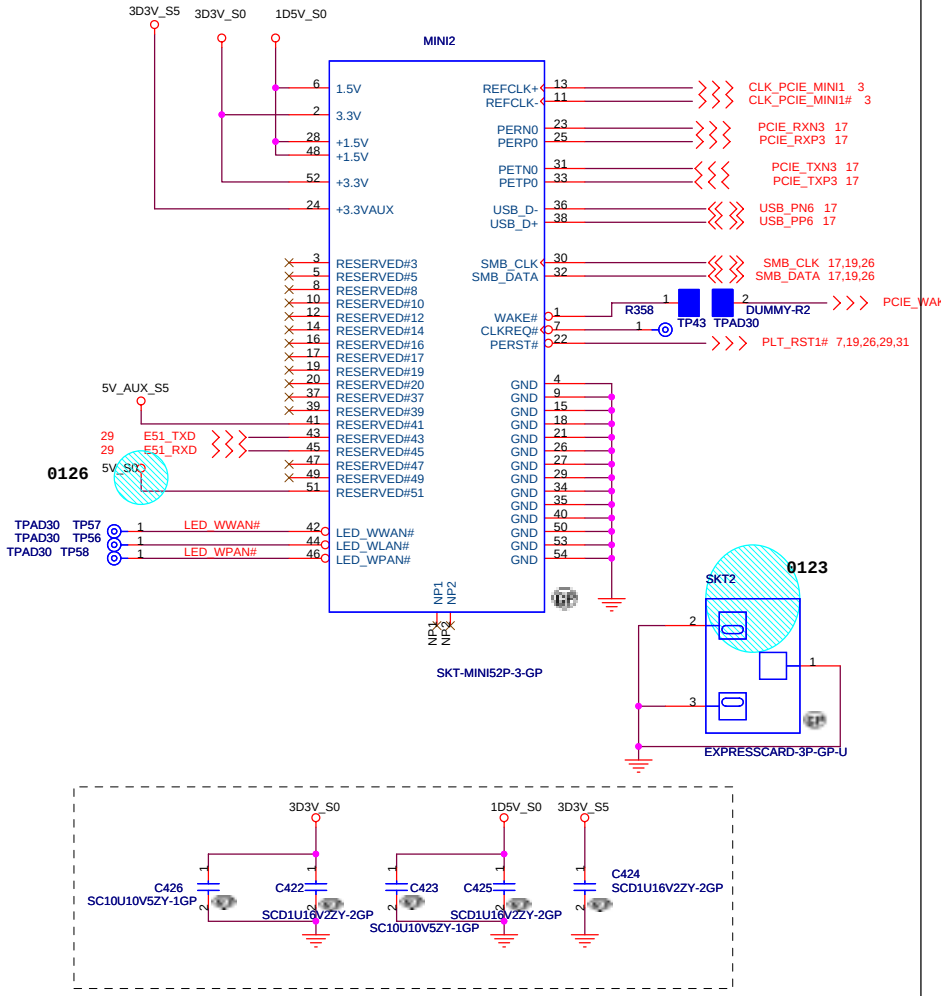
Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 22 of 39

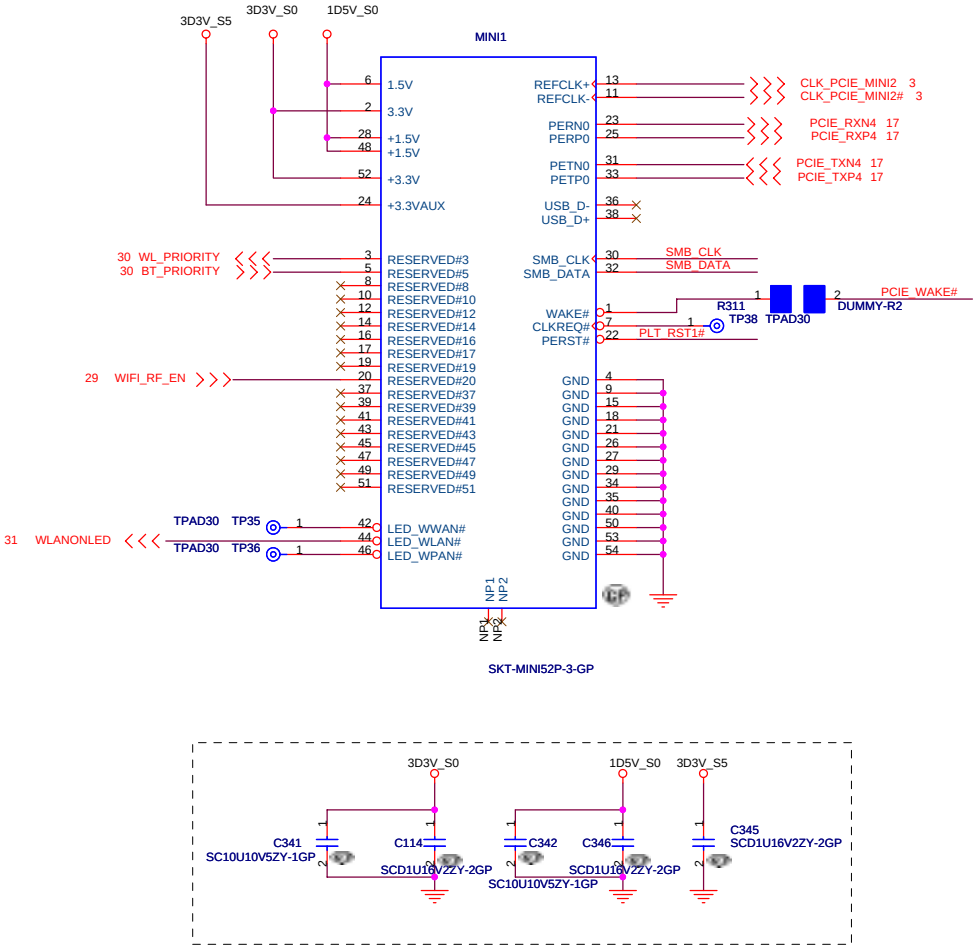

For SD Card Power
CLOSE TO CHIP
IC1A
IEEE1394/SD
CARD2
CARD1
SKT-MEMO-15-GP-U1
TAI-CON43-GP-U1
R5C832-1-GP
SKT-1394-4P-13GP
AAT4610AIGV-GP
CH731UPT-GP
SRN33J-4-GP
Reserve R547,R548,R550,R551 for co-layout
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Akita
Friday, March 31, 2006
23
39

Mini Card Connector

Mini Card Connector 1



Mini Card Connector 2



<Core Design>

Wistron Corporation
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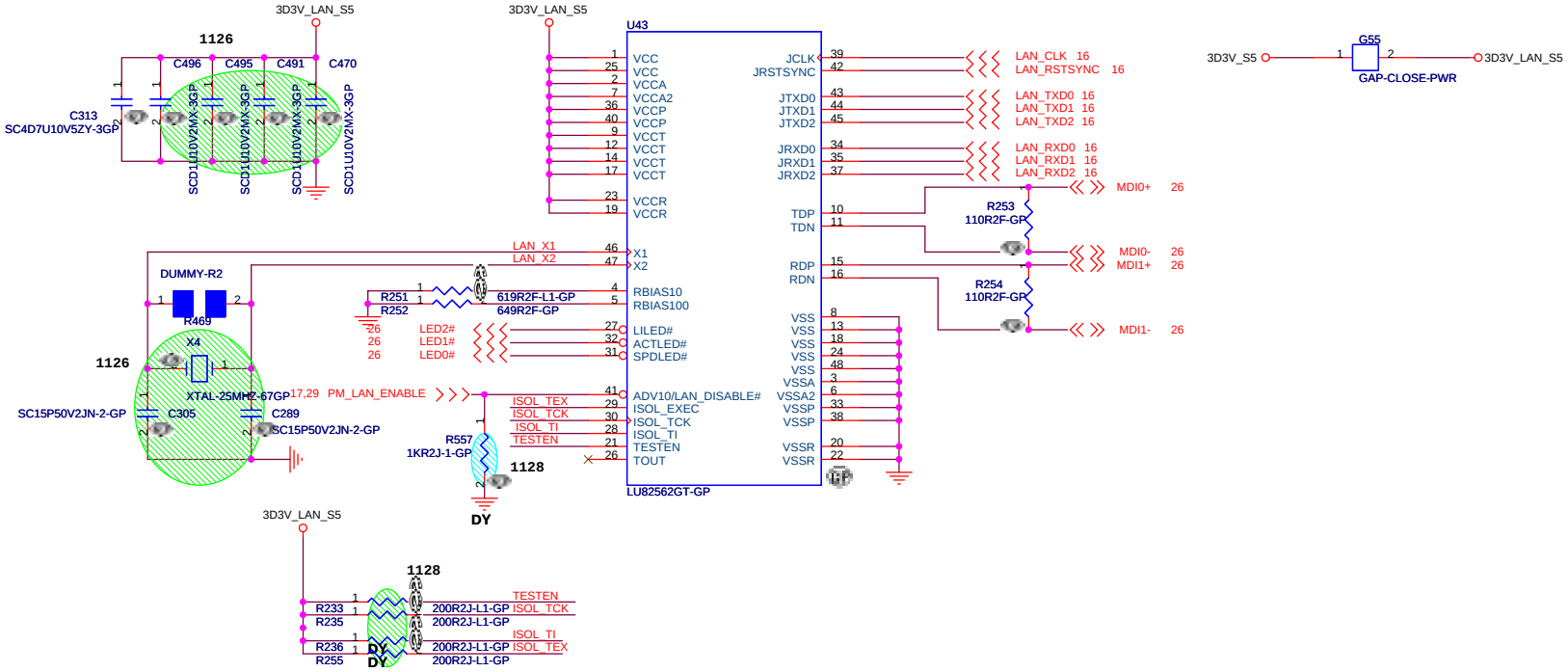
Title: **MINI CARD CONN .**

Size	Document Number	Rev
A3	Akita	SD

Date: Thursday, March 23, 2006 Sheet 24 of 39



<Core Design>

Wistron Corporation
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Title: LAN TEKOA

Size	Document Number	Rev
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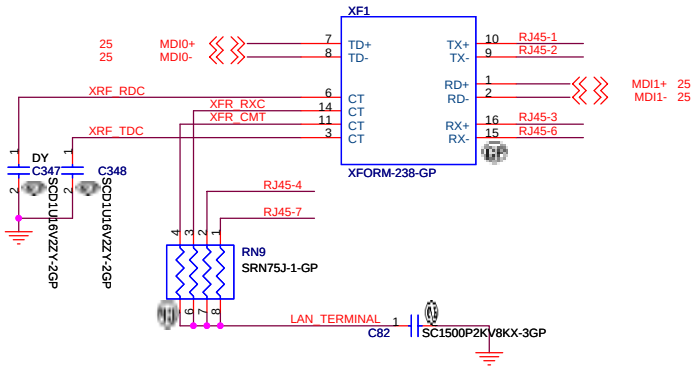
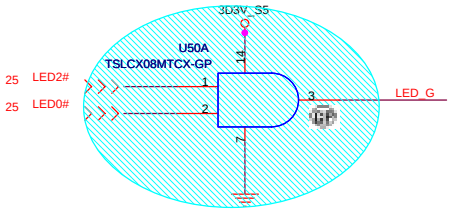
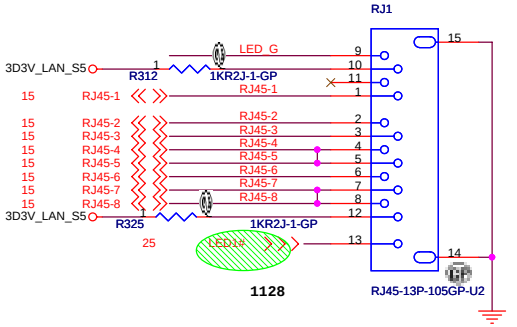
10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps

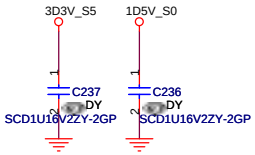


Green : Link up
Blinking : TX/RX activity

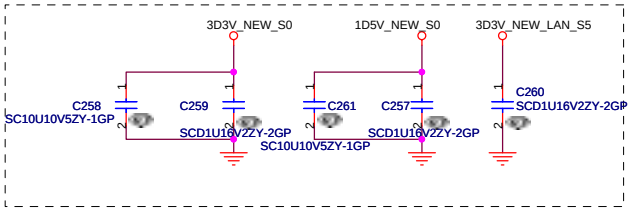
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

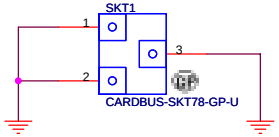
NEWCARD Connector

Place them Near to Chip

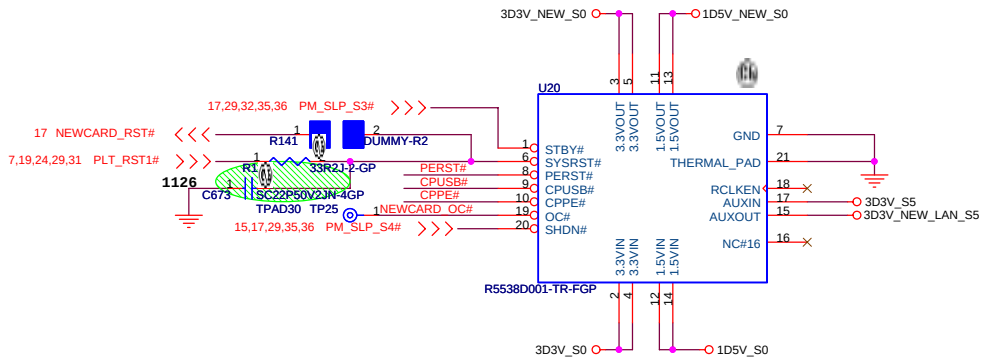


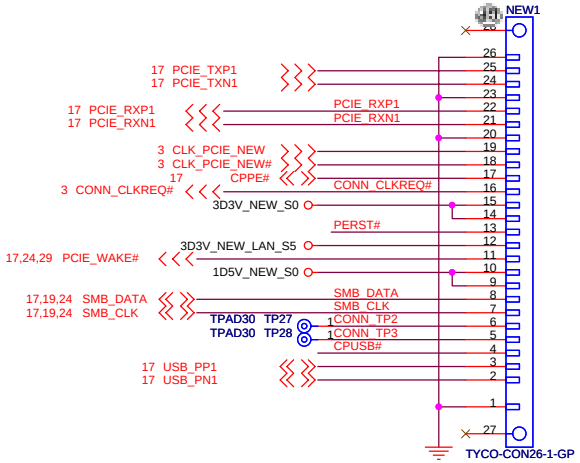
Place them Near to Connector





For Newcard socket





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card
Size: A3
Document Number: Akita
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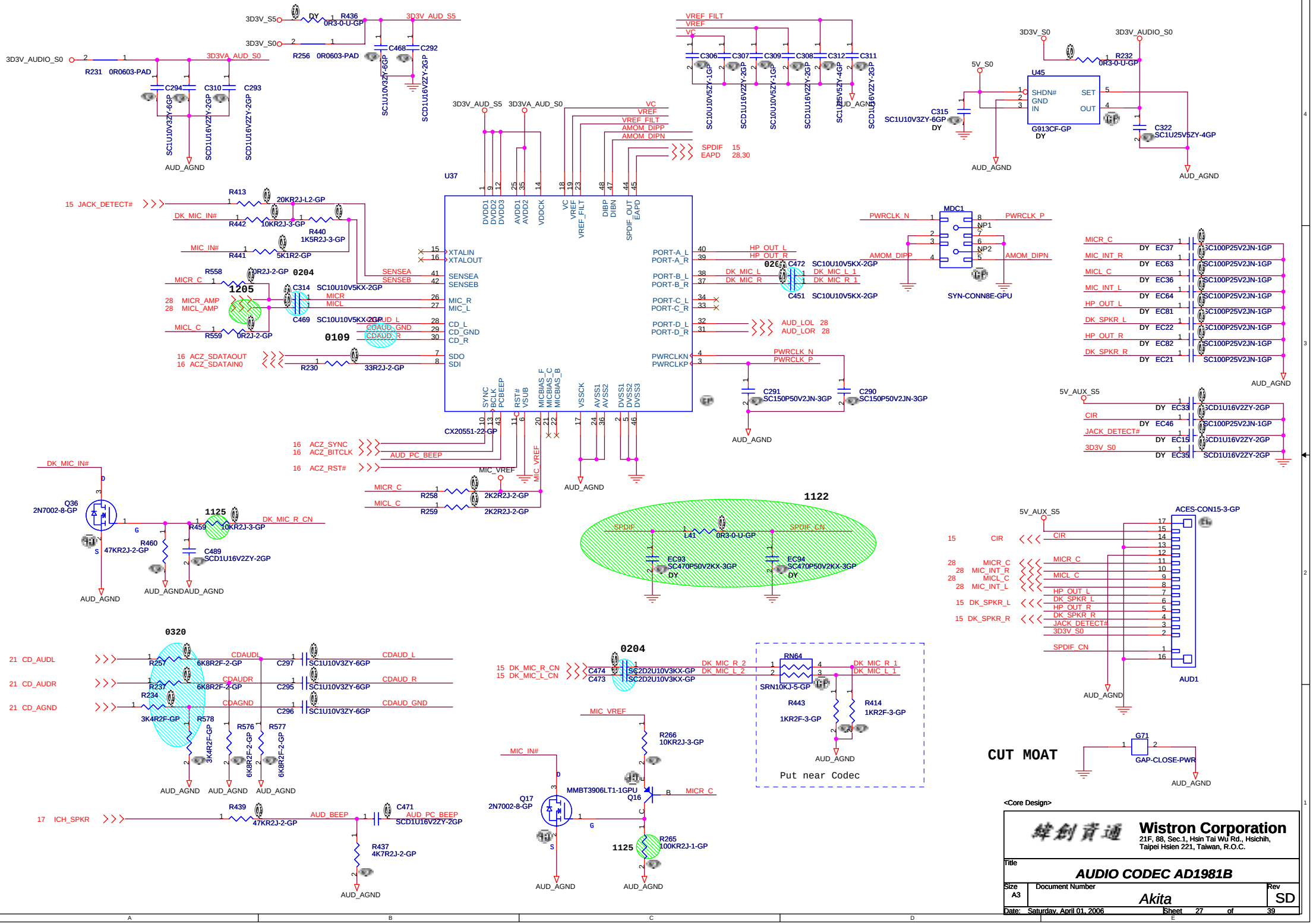
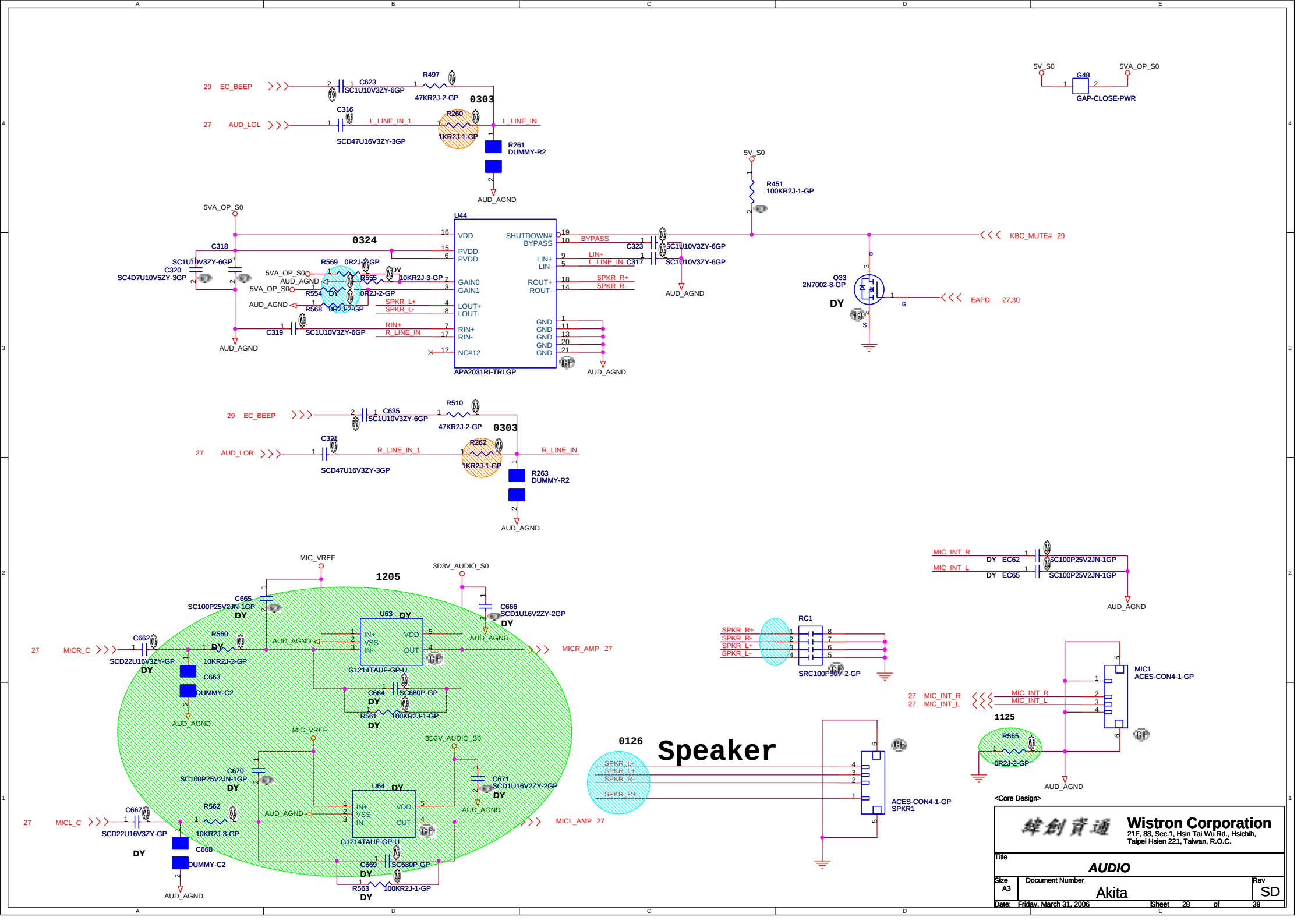
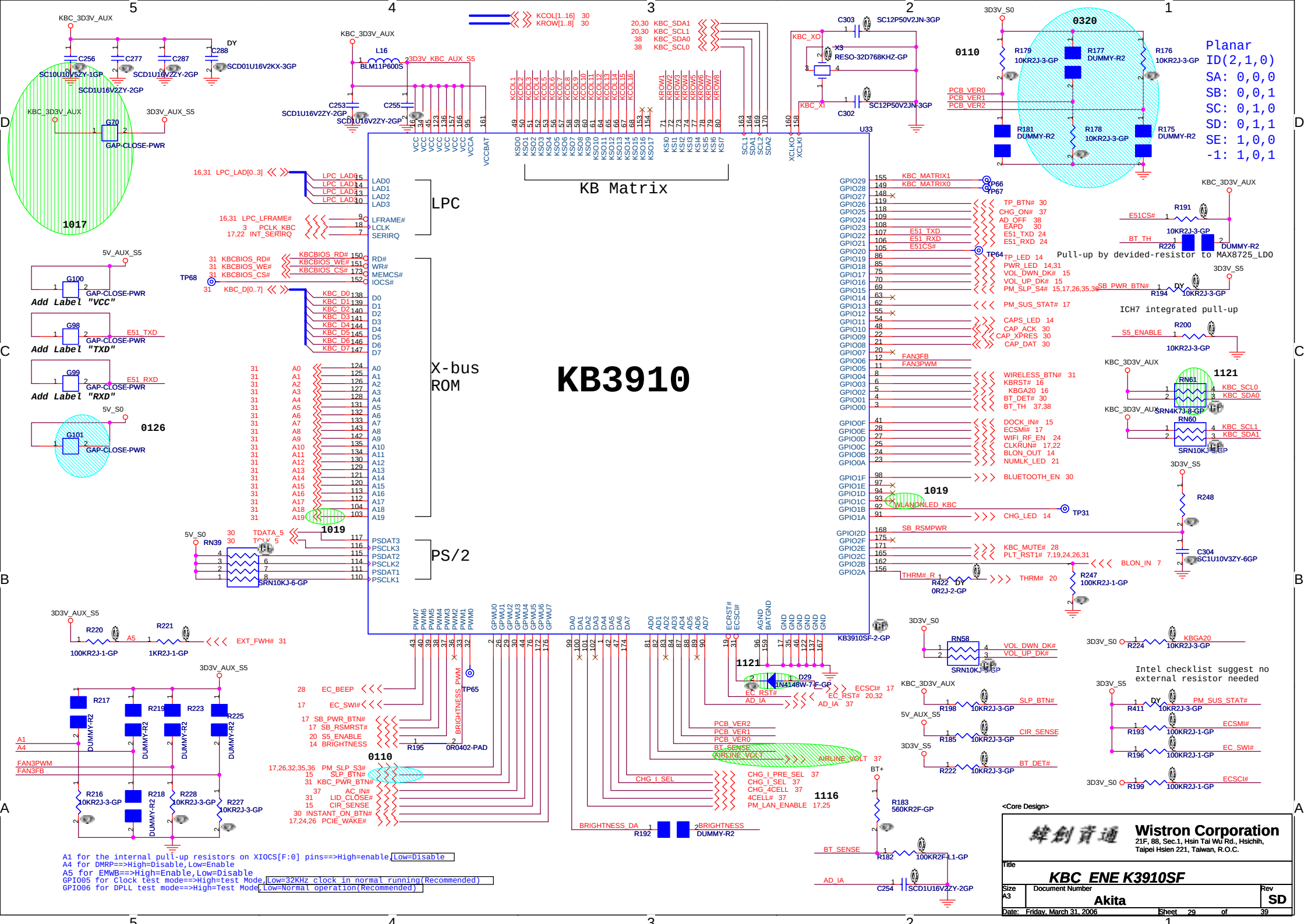
Sheet 26 of 39


3D3V_S5
3D3V_S0
3D3V_AUDIO_S0
3D3VA_AUD_S0
3D3V_AUD_S5
R436 0R3-0-U-GP
R256 0R0603-PAD
R231 0R0603-PAD
C468
C292
C294
C310
C293
SC1U10V3ZY-6GP
SC1U10V2ZY-2GP
SCD1U16V2ZY-2GP
AUD_AGND
VREF_FILT
VREF
VC
C306
C307
C309
C308
C312
C311
SC1U10V5ZY-1GP
SC1U10V5ZY-2GP
SC1U25V5ZY-4GP
5V_S0
U45
SHDN#
GND
IN
SET
OUT
G913CF-GP
DY
R232 0R3-0-U-GP
C315 SC1U10V3ZY-6GP
C322 SC1U25V5ZY-4GP
U37
VC
VREF
VREF_FILT
AMOM_DIPP
AMOM_DIPN
SPDIF 15
EAPD 28,30
DVDD1
DVDD2
DVDD3
AVDD1
AVDD2
VDDCK
VC
VREF
VREF_FILT
DIBP
DIBN
SPDIF_OUT
EAPD
15 JACK_DETECT#
R413 20KR2J-L2-GP
DK_MIC_IN#
R442 10KR2J-3-GP
R440 1K5R2J-3-GP
MIC_IN#
R441 5K1R2-GP
R558 0R2J-2-GP 0204
MICR_C
1205
28 MICR_AMP
28 MICL_AMP
C314 SC10U10V5KX-2GP
C469 SC10U10V5KX-2GP
MICL_C
R559 0R2J-2-GP
0109
16 ACZ_SDATAOUT
16 ACZ_SDATAIN0
R230 33R2J-2-GP
XTALIN
XTALOUT
SENSEA
SENSEB
MIC_R
MIC_L
CD_L
CD_GND
CD_R
SDO
SDI
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-C_L
PORT-C_R
PORT-D_L
PORT-D_R
PWRCLKN
PWRCLKP
HP_OUT_L
HP_OUT_R
DK_MIC_L
DK_MIC_R
AUD_LOL 28
AUD_LOR 28
PWRCLK_N
PWRCLK_P
C291 SC150P50V2JN-3GP
C290 SC150P50V2JN-3GP
0204
C472 SC10U10V5KX-2GP
C451 SC10U10V5KX-2GP
DK_MIC_L_1
DK_MIC_R_1
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONN8E-GPU
SYNC
BCLK
PCBEEP
RST#
VSUB
MICBIAS_F
MICBIAS_C
MICBIAS_B
VSSCK
AVSS1
AVSS2
DVSS1
DVSS2
DVSS3
CX20551-22-GP
16 ACZ_SYNC
16 ACZ_BITCLK
AUD_PC_BEEP
16 ACZ_RST#
MIC_VREF
MIC_CREF
R258 2K2R2J-2-GP
R259 2K2R2J-2-GP
MICR_C
MICL_C
MICR_C DY EC37 SC100P25V2JN-1GP
MIC_INT_R DY EC63 SC100P25V2JN-1GP
MICL_C DY EC36 SC100P25V2JN-1GP
MIC_INT_L DY EC64 SC100P25V2JN-1GP
HP_OUT_L DY EC81 SC100P25V2JN-1GP
DK_SPKR_L DY EC22 SC100P25V2JN-1GP
HP_OUT_R DY EC82 SC100P25V2JN-1GP
DK_SPKR_R DY EC21 SC100P25V2JN-1GP
5V_AUX_S5
CIR DY EC46 SC100P25V2JN-1GP
JACK_DETECT# DY EC15 SCD1U16V2ZY-2GP
3D3V_S0 DY EC35 SCD1U16V2ZY-2GP
DK_MIC_IN#
Q36 2N7002-8-GP
1125
R459 10KR2J-3-GP
DK_MIC_R_CN
R460 47KR2J-2-GP
C489 SCD1U16V2ZY-2GP
1122
SPDIF
SPDIF_CN
L41 0R3-0-U-GP
EC93 SC470P50V2KX-3GP
EC94 SC470P50V2KX-3GP
DY
ACES-CON15-3-GP
AUD1
0320
21 CD_AUDL
21 CD_AUDR
21 CD_AGND
R257 6K8R2F-2-GP
R237 6K8R2F-2-GP
R234 3K4R2F-GP
R578 3K4R2F-GP
R576 6K8R2F-2-GP
R577 6K8R2F-2-GP
CDAUDL
CDAUDR
CDAGND
C297 SC1U10V3ZY-6GP
C295 SC1U10V3ZY-6GP
C296 SC1U10V3ZY-6GP
CDAUD_L
CDAUD_R
CDAUD_GND
0204
15 DK_MIC_R_CN
15 DK_MIC_L_CN
C474 SC2D2U10V3KX-GP
C473 SC2D2U10V3KX-GP
DK_MIC_R_2
DK_MIC_L_2
RN64
SRN10KJ-5-GP
R443 1KR2F-3-GP
R414 1KR2F-3-GP
Put near Codec
MIC_VREF
R266 10KR2J-3-GP
MIC_IN#
Q17 2N7002-8-GP
MMBT3906LT1-1GPU
Q16
MICR_C
1125
R265 100KR2J-1-GP
17 ICH_SPKR
R439 47KR2J-2-GP
AUD_BEEP
C471 SCD1U16V2ZY-2GP
AUD_PC_BEEP
R437 4K7R2J-2-GP
CUT MOAT
G71
GAP-CLOSE-PWR
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC AD1981B
Size A3
Document Number
Akita
Rev SD
Date: Saturday, April 01, 2006
Sheet 27 of 39



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO***	
Size A3	Document Number Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 28 of 39	


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
KB3910SF-2-GP
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
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KBC_ENE K3910SF
Akita
Friday, March 31, 2006

Internal KeyBoard Connector

29 KROW[1..8]
29 KCOL[1..16]

KB1
ACES-CON24-2-GP

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

5V_S5
C396 SCD1U16V2ZY-2GP
C395 SC1U10V3ZY-6GP
R370 10KR2J-3-GP
R369 10KR2J-3-GP
TPAD1
29 TDATA_5
29 TCLK_5
C398 SC33P50V2JN-3GP
C397 SC33P50V2JN-3GP
ACES-CON8-6-GP

CAMERA

5V_S0
ACES-CON5-1GP
C81 SC4D7U10V5ZY-3GP
C80 SCD1U16V2ZY-2GP
USB_4-
USB_4+
CAM1

17 USB_PN4
R87 0R0402-PAD
TR4 L-63UH-GP DY
R88 0R0402-PAD
17 USB_PP4

17 USB_PN5
R269 0R0402-PAD
TR6 L-63UH-GP DY
R264 0R0402-PAD
17 USB_PP5

Blue thumb

BT1
3D3V_BT_S0
USB_5+
USB_5-
31 BT_LED
24 WL_PRIORITY
24 BT_PRIORITY
29 BT_DET#
ACES-CON8-4-GP

BT_PRIORITY
WL_PRIORITY
BT_LED
EC85 SCD1U16V2ZY-2GP DY
EC88 DY
EC87 DY SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
EC38 DY SCD1U16V2ZY-2GP

Close to CN8

5V_S5
C490 SC1U10V3ZY-6GP
U53
SHDN# GND IN SET OUT
G913CF-GP
MAX 150mA
29 BLUETOOTH_EN
C493 SC4D7U10V5ZY-3GP
C492 SCD1U16V2ZY-2GP

3D3V_AUX_S5
D35 BAV99TPT-GP
CAP_ACK
0322
D32 BAV99TPT-GP
CAP_DAT
D33 BAV99TPT-GP
INSTANT_ON_BTN#
D34 BAV99TPT-GP
EAPD#

CAPACITY BUTTON

3D3V_AUX_S5
0119
EC79 SCD1U16V2ZY-2GP
CAP1
29 CAP_XPRES
20,29 KBC_SCL1
20,29 KBC_SDA1
29 CAP_ACK
CAP_DAT
INSTANT_ON_BTN#
R470 DY 0R2J-2-GP
R467 DY 0R2J-2-GP
R468 0R2J-2-GP
0204
R438 DY 0R2J-2-GP
R466 0R2J-2-GP
EAPD#
ACES-CON12-4-GP
5V_S0
DY EC6 SCD1U16V2ZY-2GP
CAP_ACK
CAP_DAT DY EC9 SC100P25V2JN-1GP
INSTANT_ON_BTN# DY EC8 SCD1U16V2ZY-2GP
EAPD# DY EC7 SCD1U16V2ZY-2GP
DY EC12 SCD1U16V2ZY-2GP

3D3V_S0
0119
R197 10KR2J-3-GP
EAPD#
Q11 2N7002-8-GP
27,28 EAPD
EAPD# 15

TOUCH-PAD SWITCH

SW1 SW-TACT-68-GP-T
R180 10KR2J-3-GP
R184 100R2J-2-GP
C242 SC1000P50V3JN-GP DY
TP_BTN# 29

KROW3 KCOL1 KROW6 KROW5
RC6 SRC100P50V-2-GP
for EMI

KROW1 KCOL2 KCOL6 KROW4
RC5 SRC100P50V-2-GP

KCOL9 KCOL8 KCOL5 KCOL3
RC4 SRC100P50V-2-GP

KCOL10 KROW7 KROW8 KROW2
RC7 SRC100P50V-2-GP

for EMI
KCOL16 KCOL11 KCOL12 KCOL15
RC2 SRC100P50V-2-GP

KCOL14 KCOL13 KCOL4 KCOL7
RC3 SRC100P50V-2-GP
for EMI

<Core Design>

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Title: **KeyBoard-CONN**
Size: A3
Document Number: Akita
Rev: SD
Date: Friday, March 31, 2006
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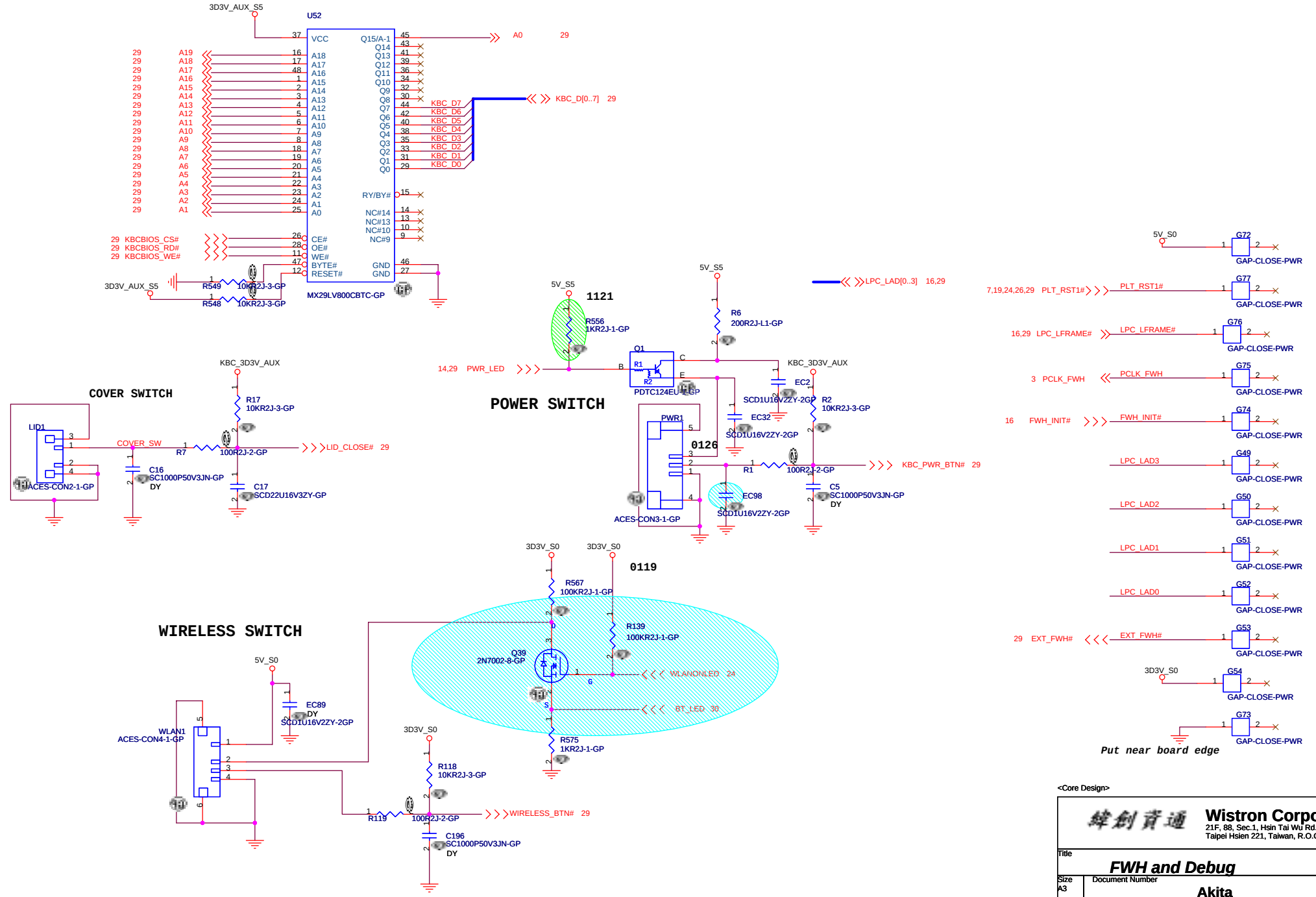

<Core Design>

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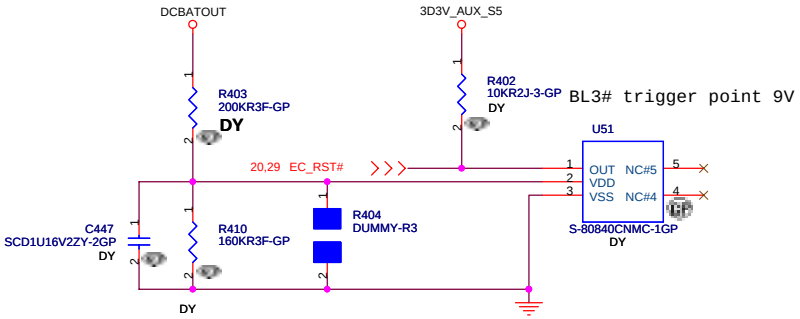
Taipei Hsien 221, Taiwan, R.O.C.

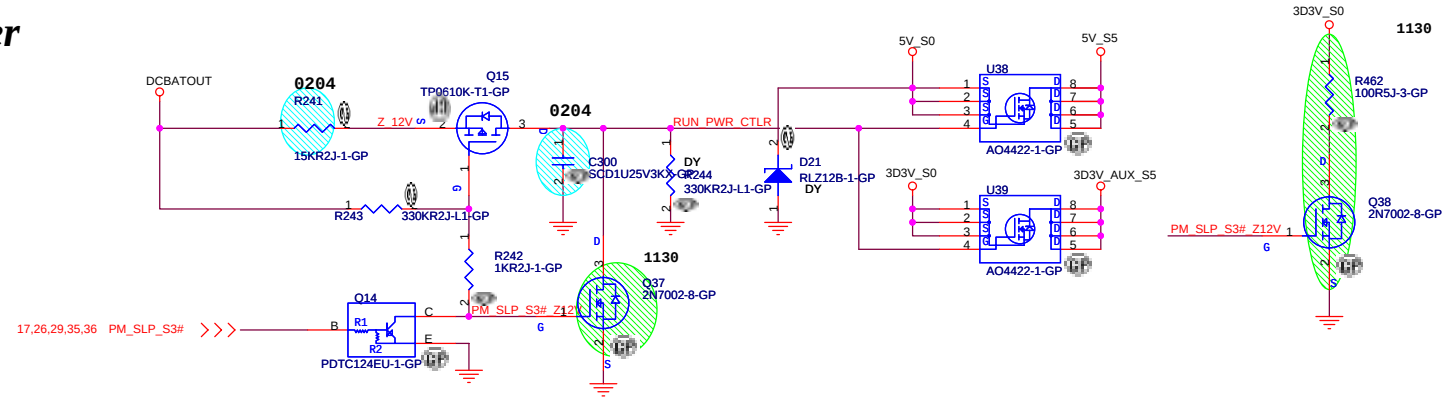
Title: **FWH and Debug**

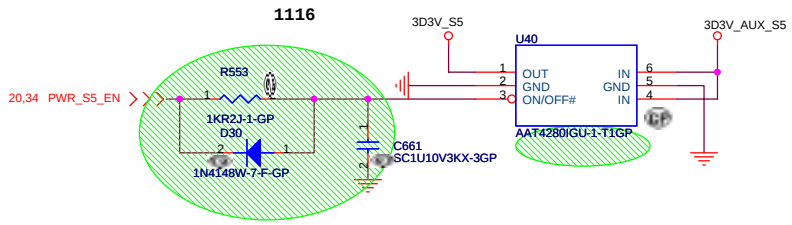
Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 31 of 39



Run Power





<Core Design>

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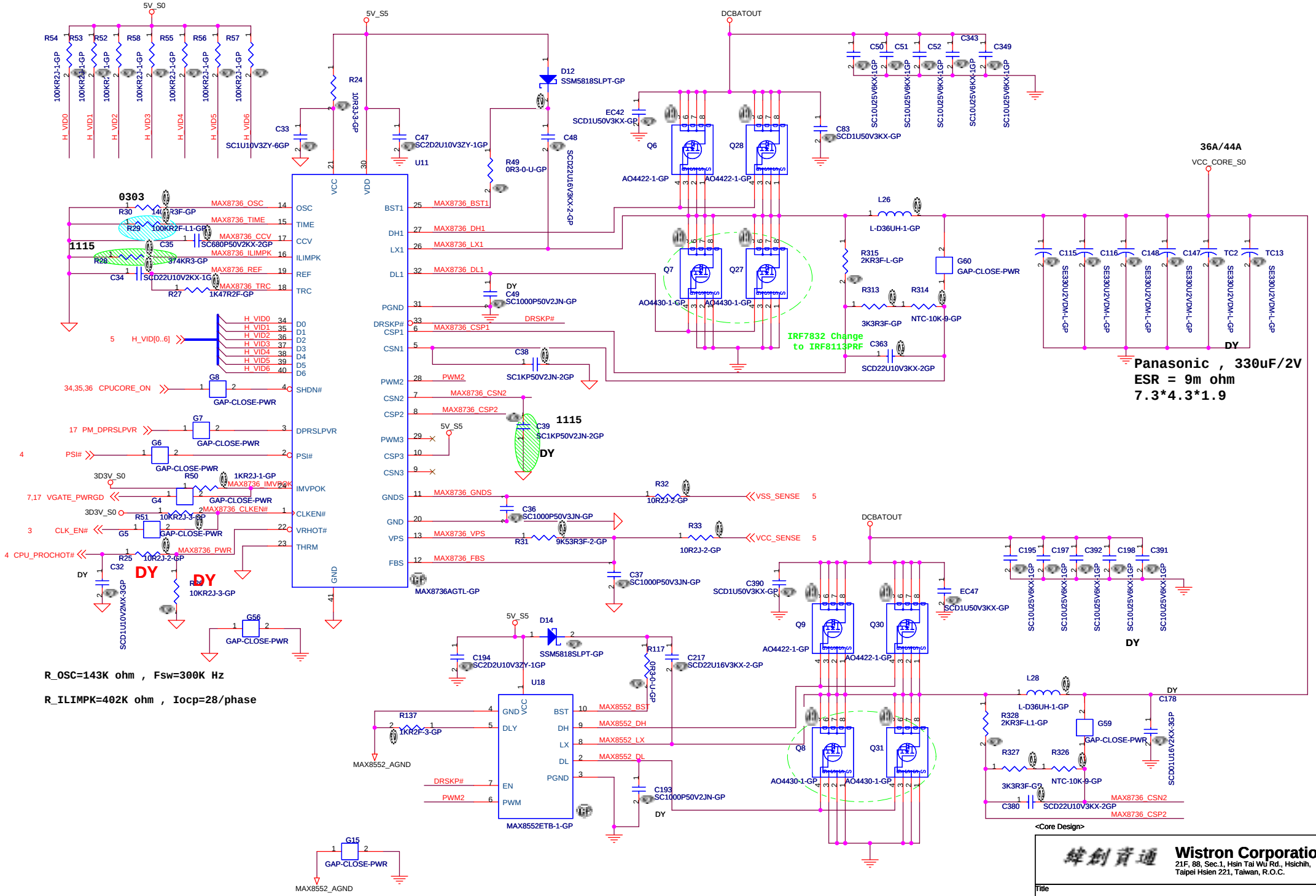
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESETLOGIC***

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 32 of 39



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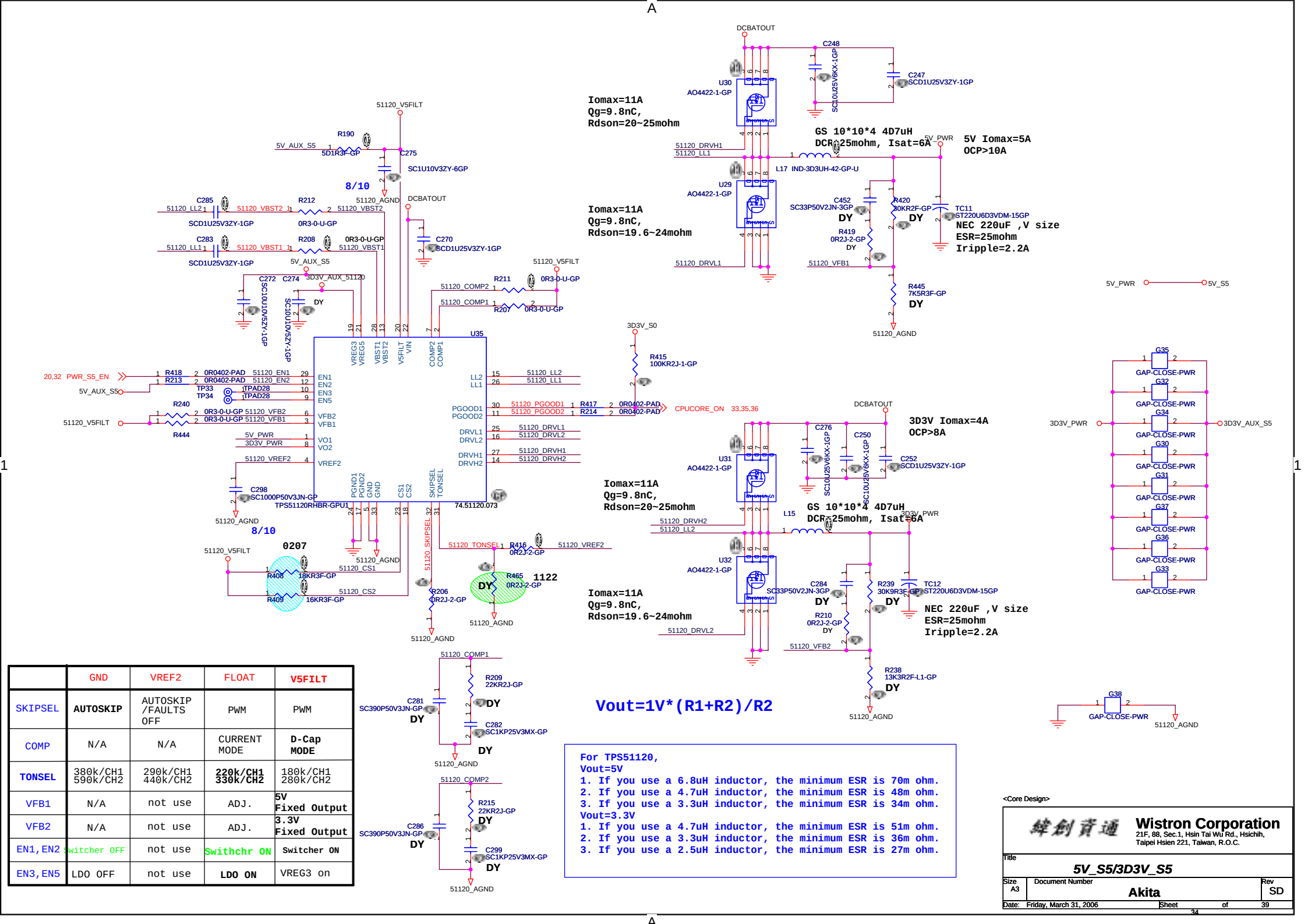
Title: DC-DC VCCCPUCORE

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 33 of 39

<Core Design>



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S5/3D3V_S5

Size: A3 | Document Number: Akita | Rev: SD

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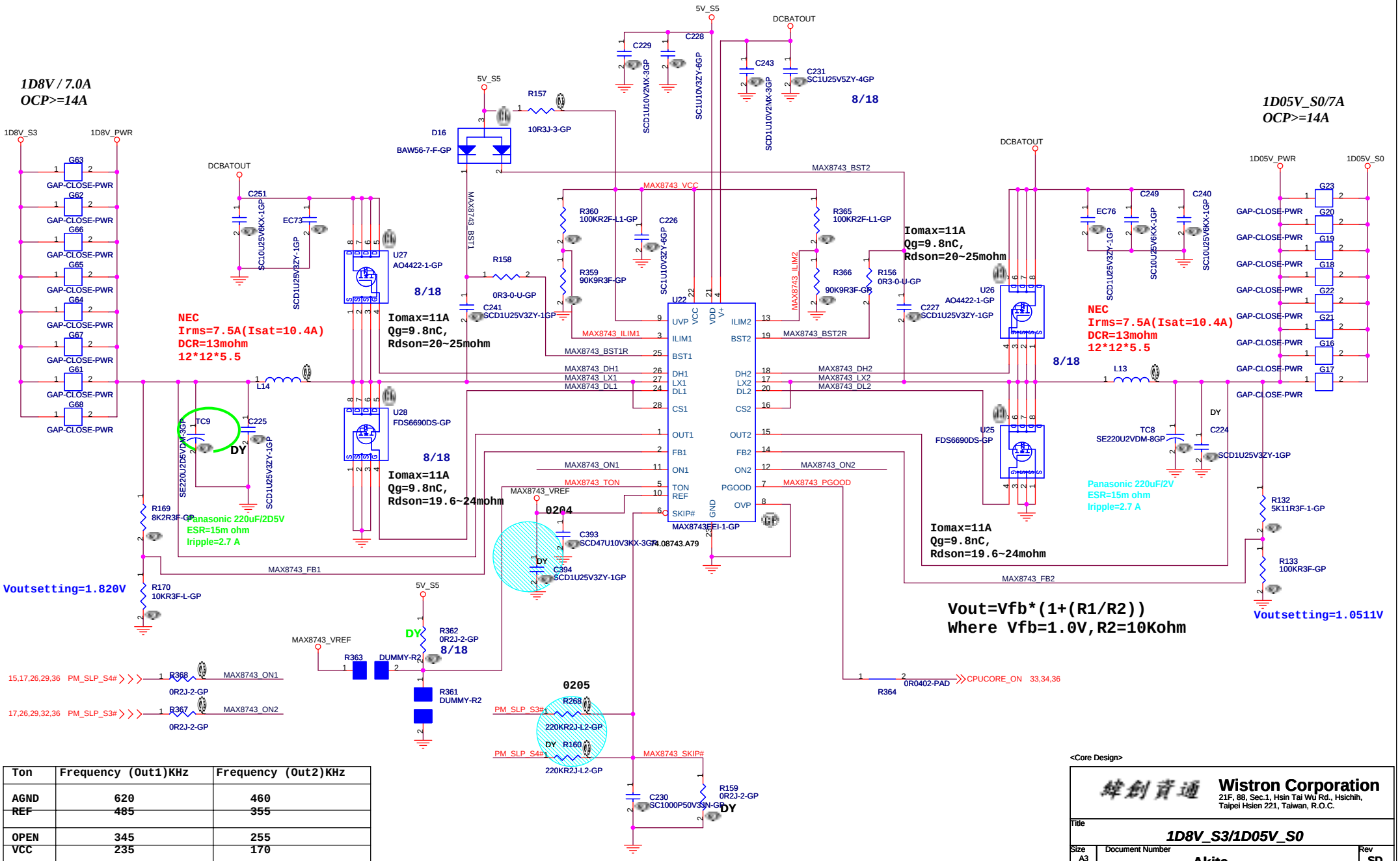
Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/7A
OCP>=14A



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

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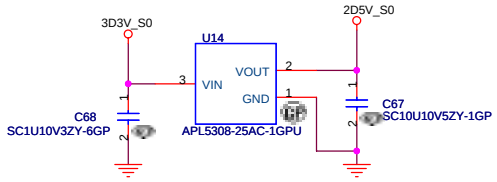
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V_S3/1D05V_S0*

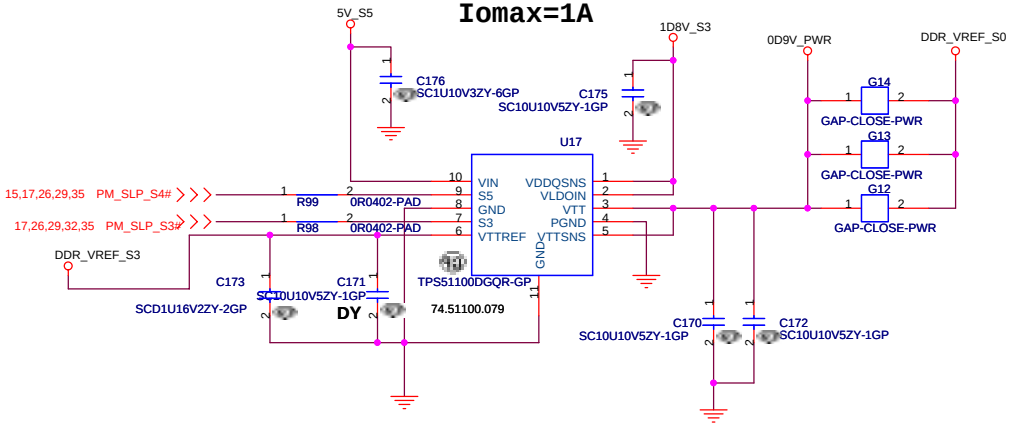
Size: A3 | Document Number: Akita | Rev: SD

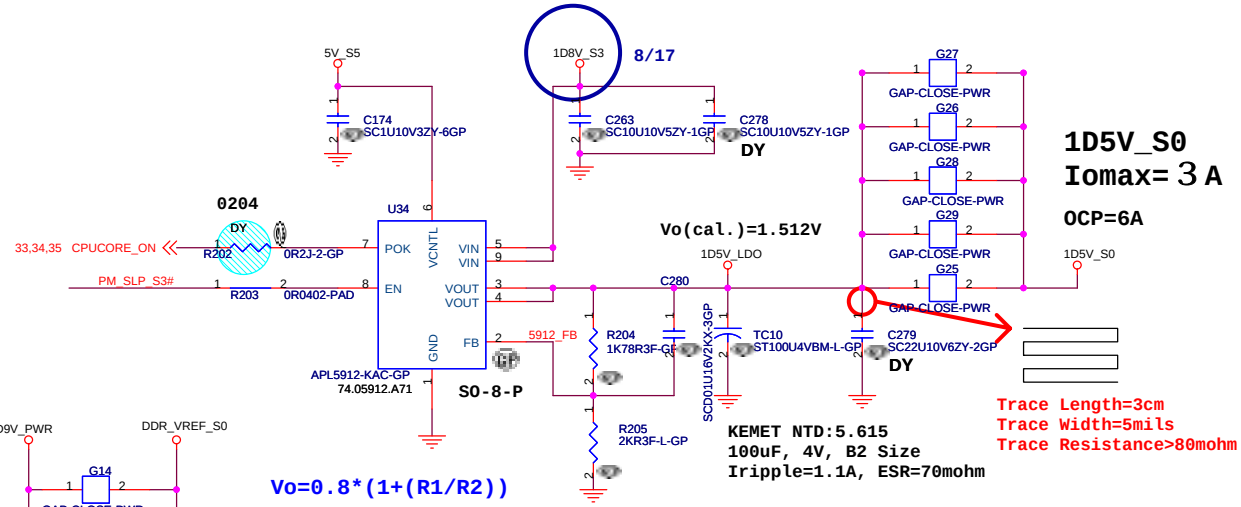
Date: Friday, March 31, 2006 | Sheet 35 of 39

2D5V_S0
Iomax=300mA



0D9V
Iomax=1A



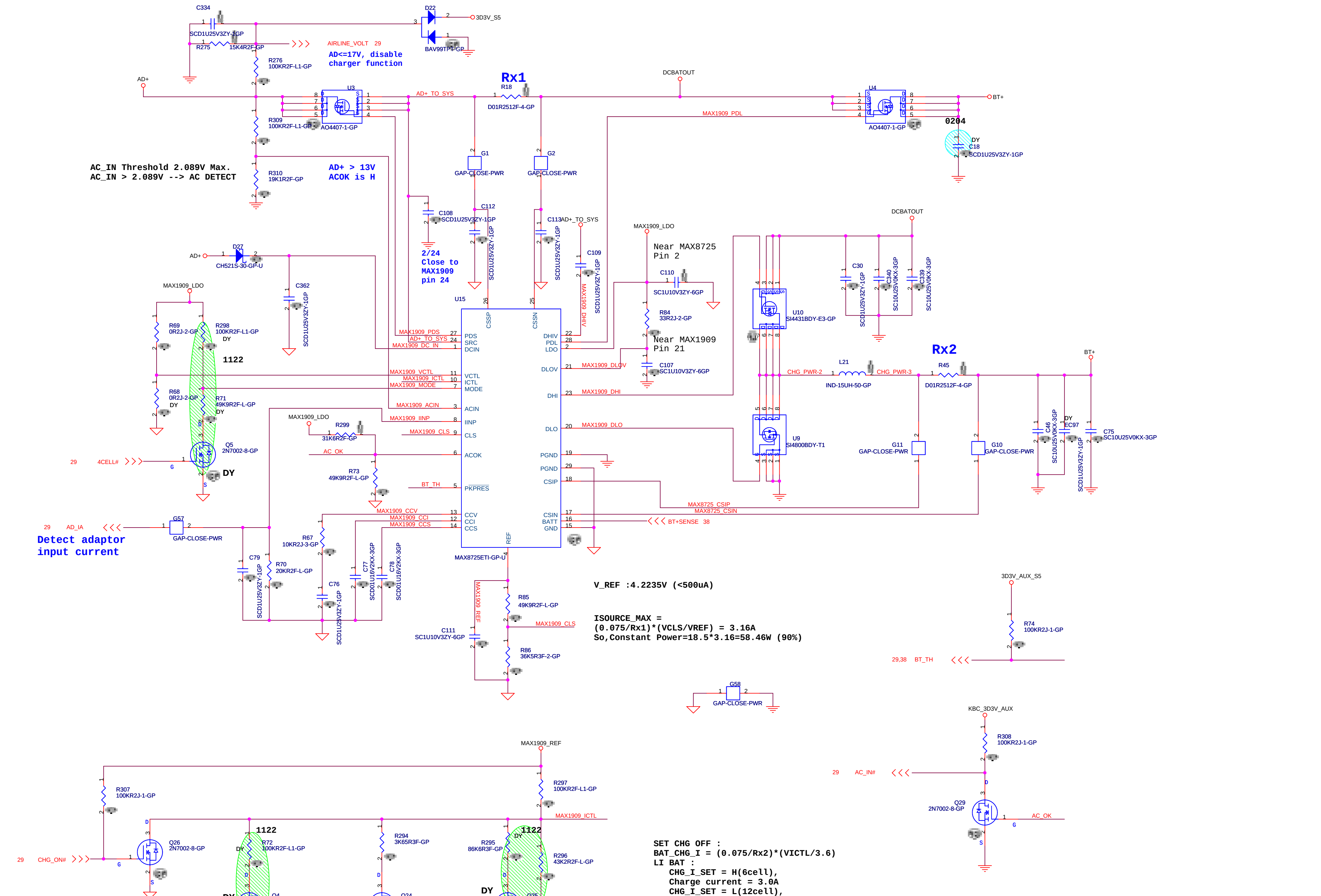


1D5V_S0
Iomax= 3 A
OCP=6A

Vo=0.8*(1+(R1/R2))

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO		
Size: A3	Document Number: Akita	Rev: SD
Date: Friday, March 31, 2006	Sheet 36 of 39	



<Core Design>

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Title: **CHARGER ISL6225**

Size	Document Number	Rev
C	Akita	SD

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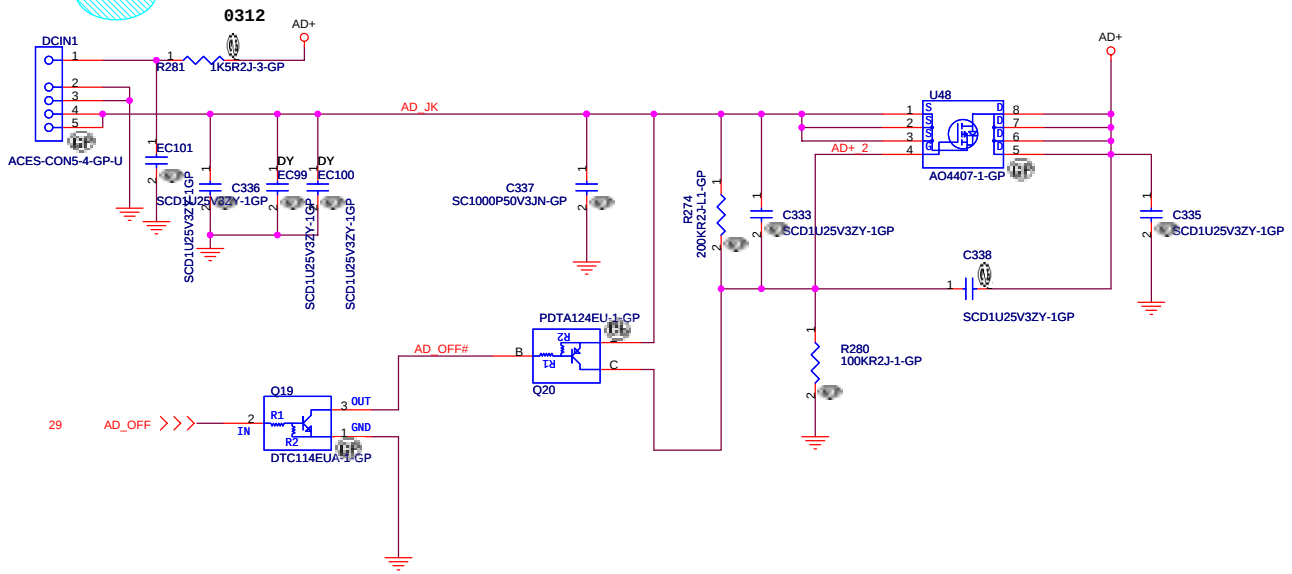
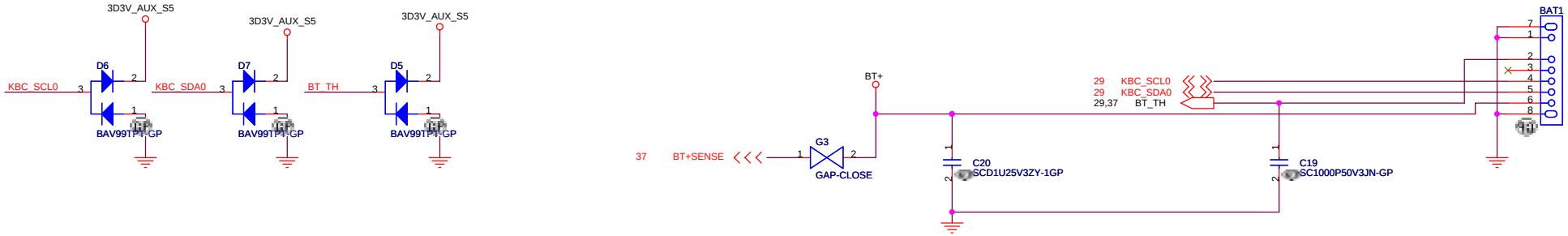
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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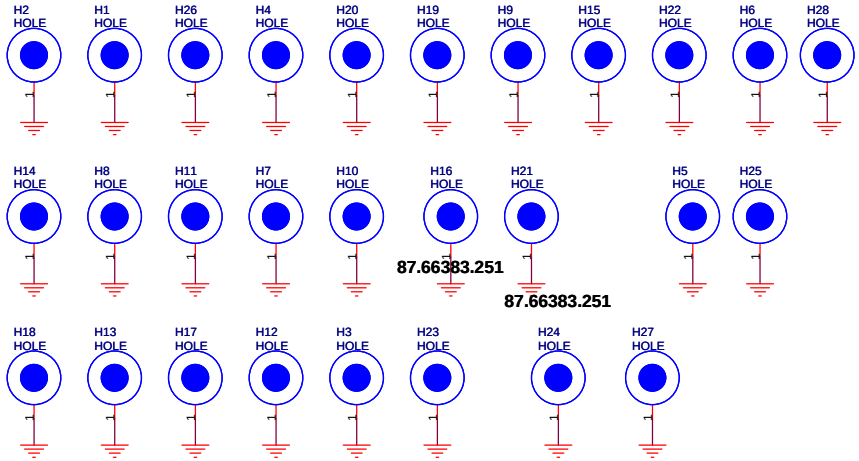
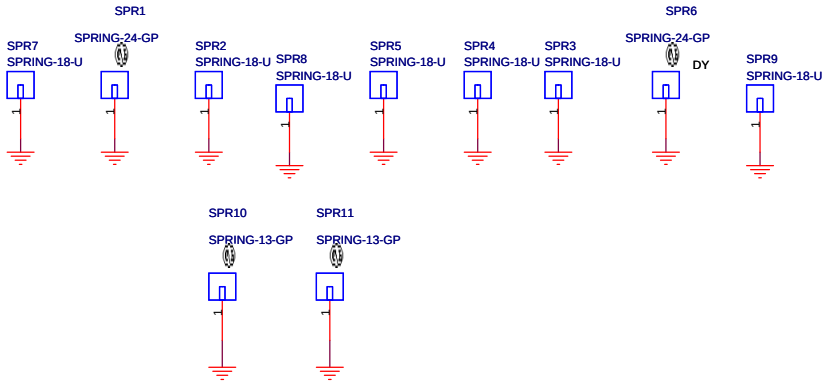
Taipei Hsien 221, Taiwan, R.O.C.

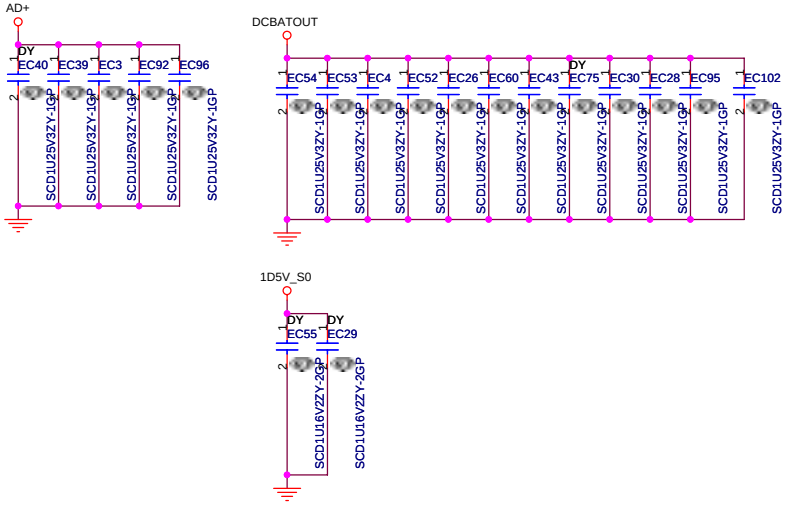
Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	Akita	SD

Date: Saturday, April 01, 2006 Sheet 38 of 39







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC
Size: A3
Document Number: Akita
Rev: SD
Date: Saturday, April 01, 2006
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