

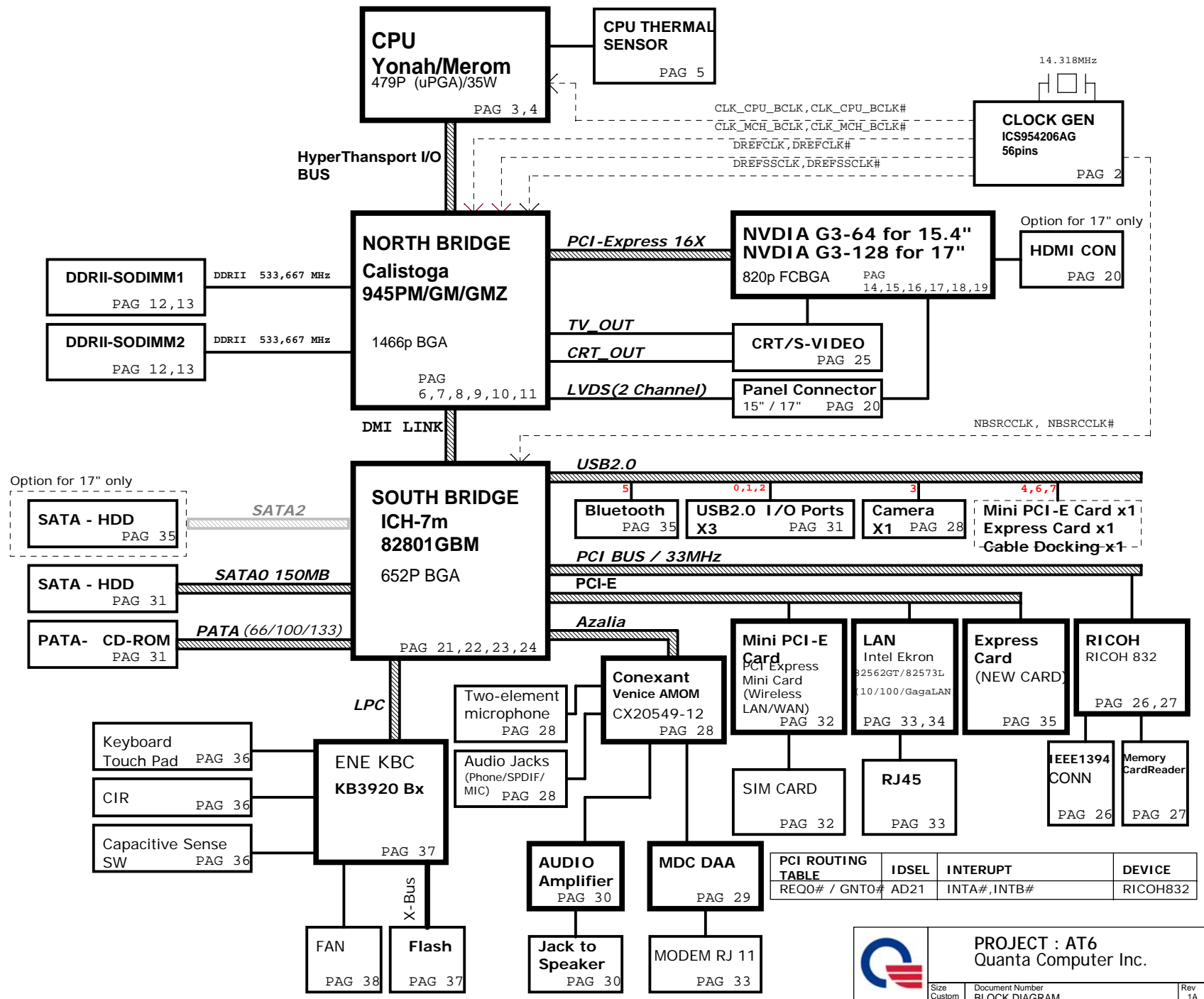
# AT6 BLOCK DIAGRAM

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- Cable Docking**
- TV\_OUT
  - VGA
  - RJ-45
  - CIR/Pwr btn
  - SPDIF Out
  - Stereo MIC
  - Headphone Jack
  - USB Port
  - VOL Cntr
- PAG 38

- SYSTEM CHARGER(MAX8724) PAG 39
- SYSTEM POWER MAX8743A PAG 40
- DDR II SMDR\_VTERM 1.8V/1.8VSUS(MAX8632) PAG 41
- VCCP +1.5V AND GMCH 1.05V(MAX8743) PAG 42
- VGACORE(1.025V)MAX1992 PAG 43
- CPU CORE MAX8771 PAG 44



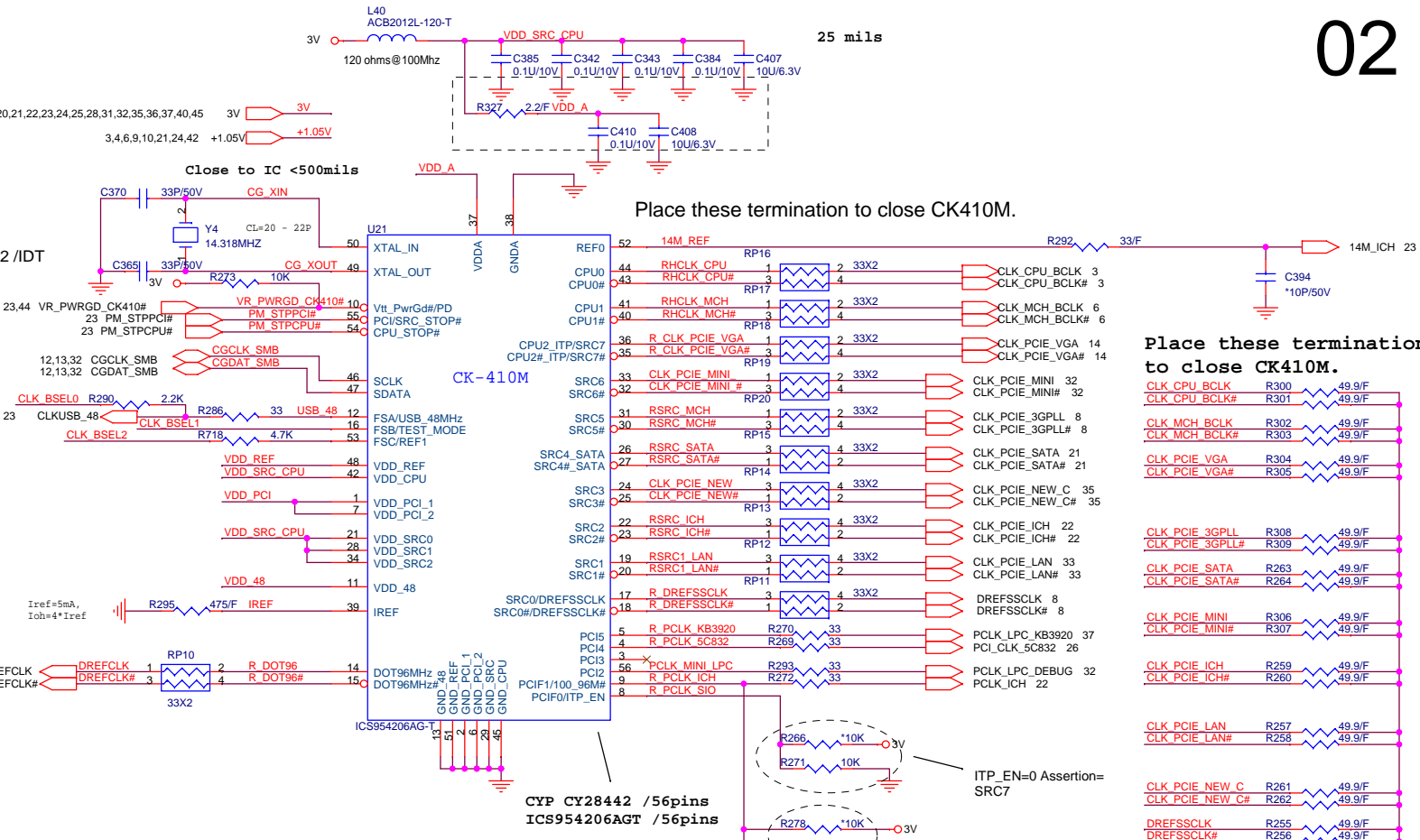
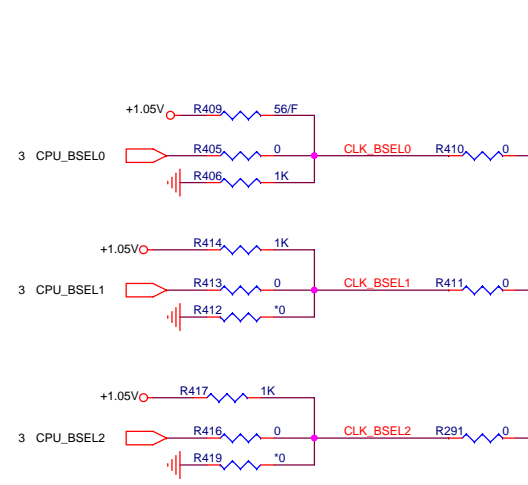
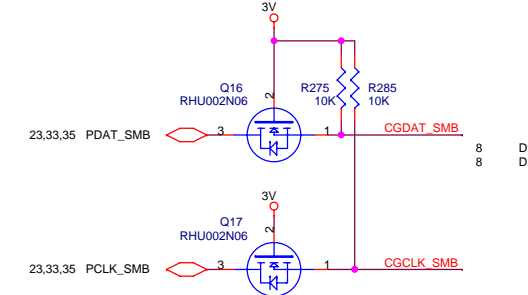
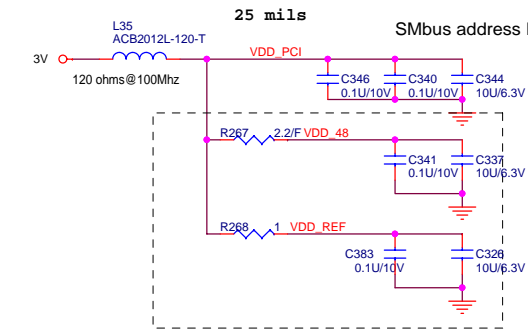
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#, INTB#	RICOH832

**PROJECT : AT6**  
Quanta Computer Inc.

Size Custom	Document Number BLOCK DIAGRAM	Rev 1A
Date: Monday, May 22, 2006		Sheet 1 of 45

NB5/RD1/HW2

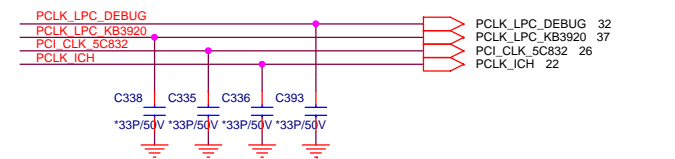
FSC	FSB	FSA	CPU	SRC	PCI	DOT
1	0	1	100	100	33	96
0	0	1	133	100	33	96
0	1	1	166	100	33	96
0	1	0	200	100	33	96
0	0	0	266	100	33	96
1	0	0	333	100	33	96
1	1	0	400	100	33	96
1	1	1	200	100	33	96



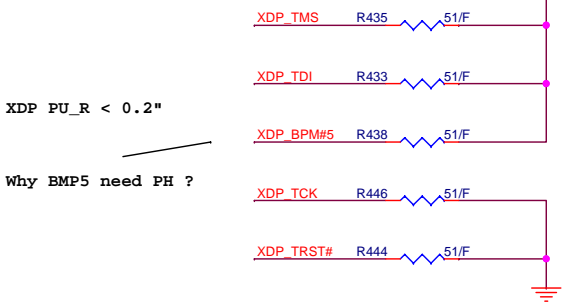
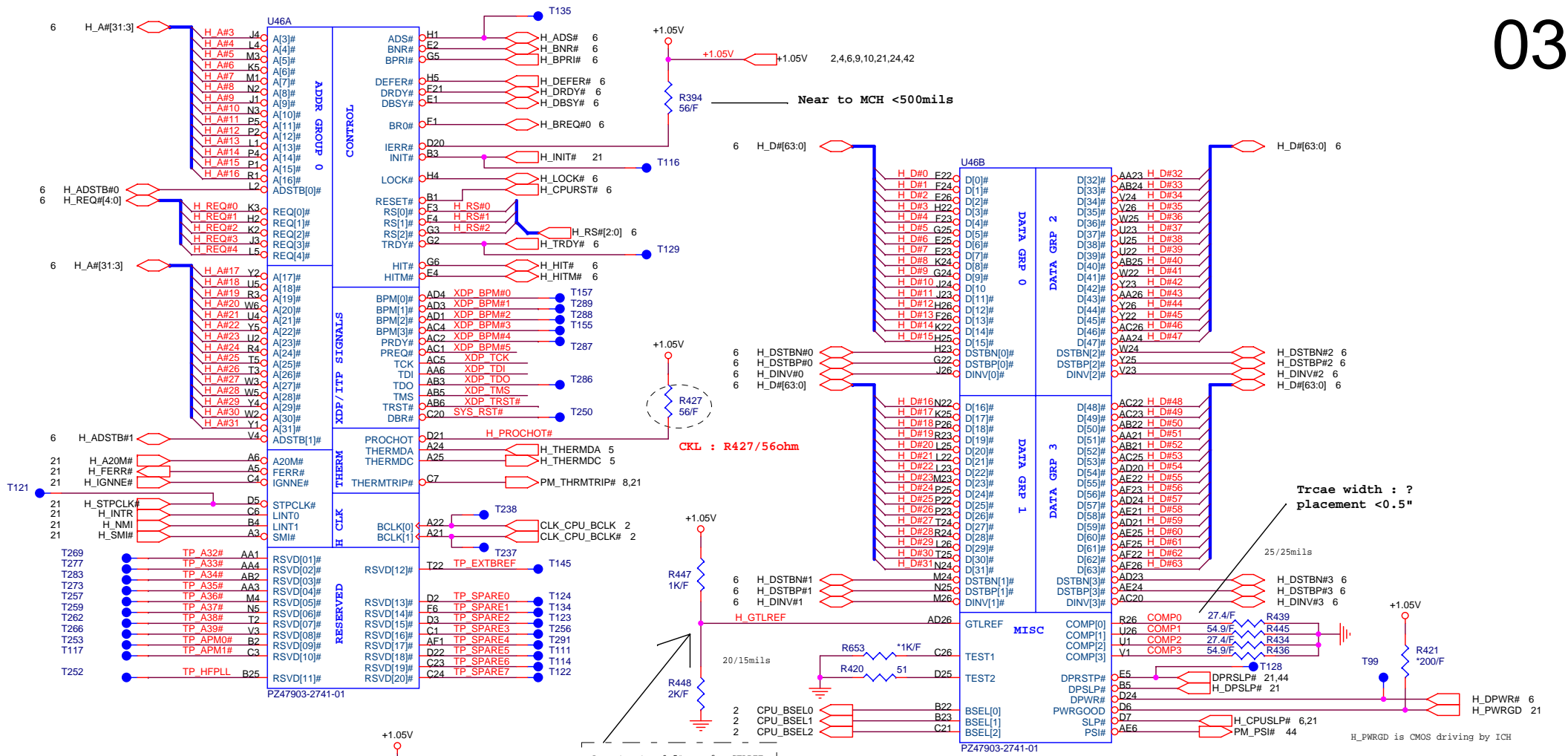
**FSB Frequency Select**

FSB Freq (Mhz)	Configuration
CPU DRIVEN (default)	R405=0
	R406=1K
	R413=0
	R414=1K
	R416=0
	R417=1K
533	R405=NO STUFF
	R409=56 / F
	R413=NO STUFF
	R412=0
	R416=NO STUFF
	R419=0
667	R405=NO STUFF
	R409=56 / F
	R413=NO STUFF
	R414=1K
	R416=NO STUFF
	R419=0


DREFSSCLK Frequency Select.  
"0": 96MHz "1": 100MHz

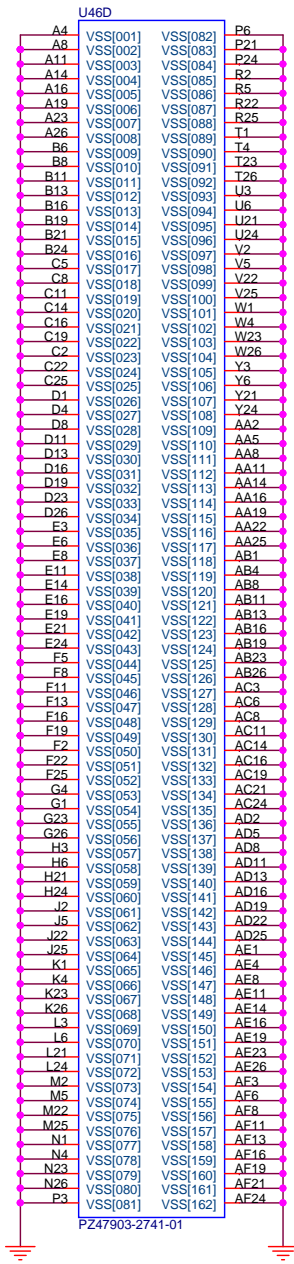
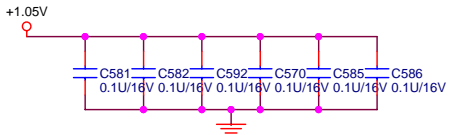
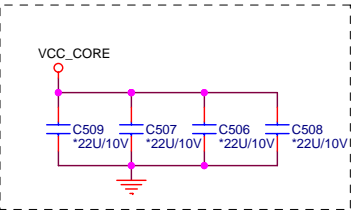
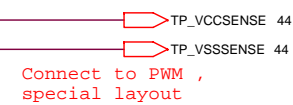
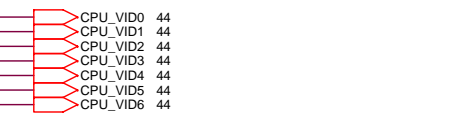
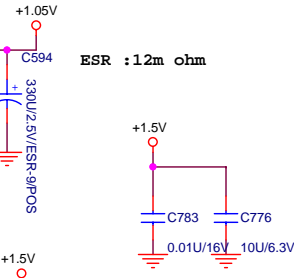
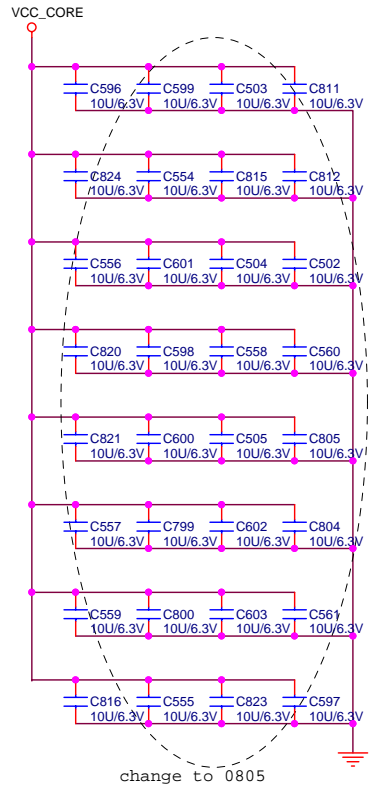
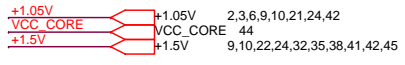
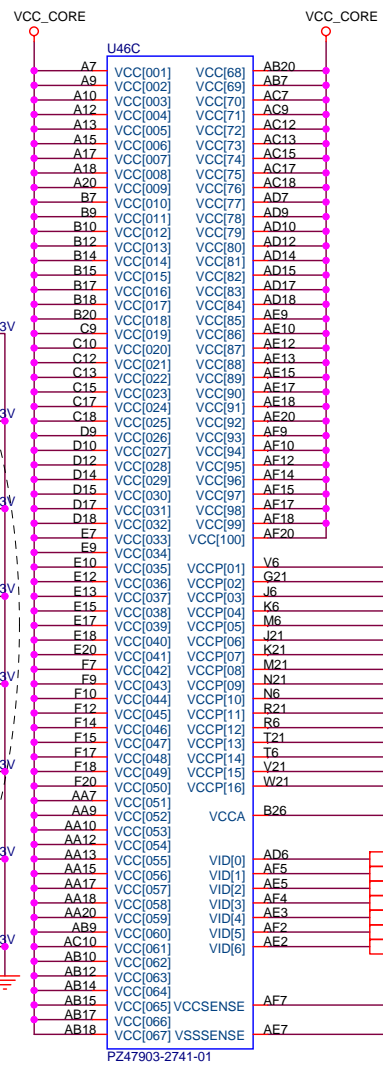


**PROJECT : AT6**  
Quanta Computer Inc.



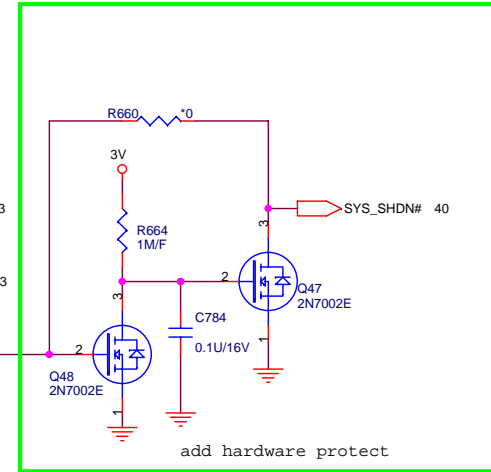
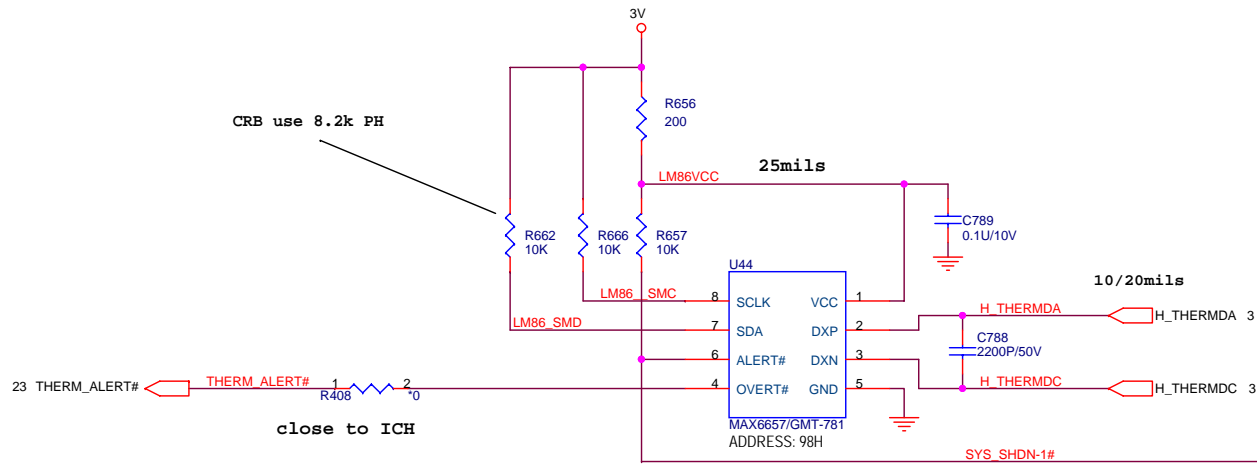
XDP\_TCK PD 27.4/1% ?  
 XDP\_TRST PD 510ohm /5% ?  
 XDP\_TDI PU 150ohm /1.05V  
 XDP\_TMS PU 39.2/1%?  
 XDP\_TDO PU 54.9ohm?  
 For ITP700

 NB5/RD1/HW2	<b>PROJECT : AT6</b> Quanta Computer Inc.		Rev 1A
	Size B	Document Number CPU (1/2)	Date: Monday, May 22, 2006 Sheet 3 of 45

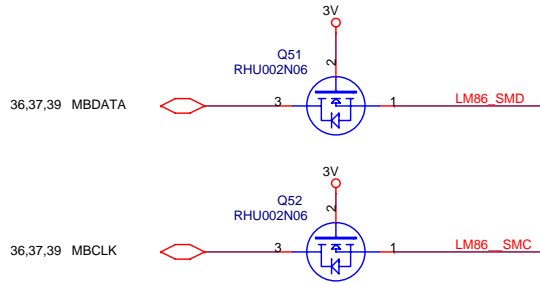


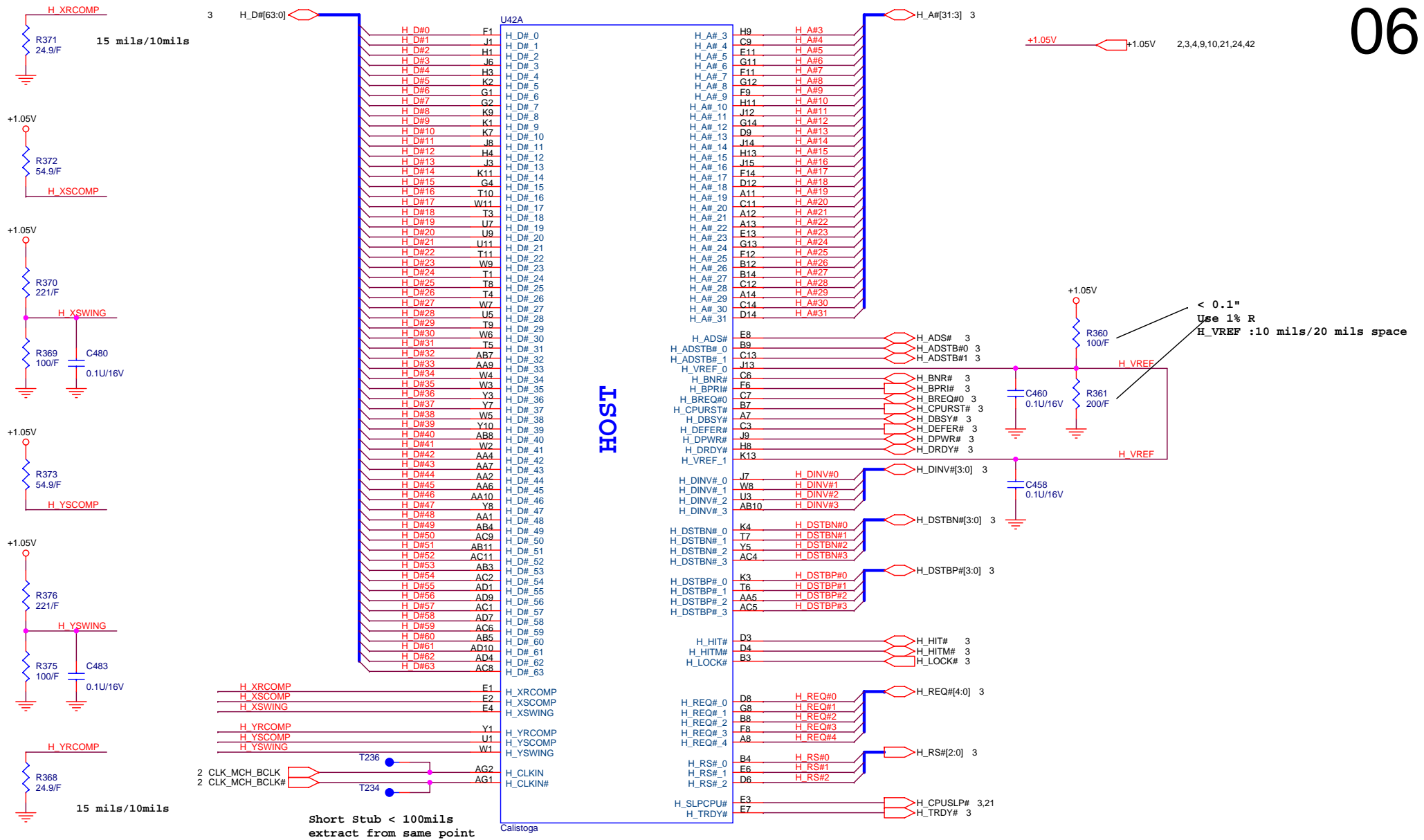
PROJECT : AT6  
 Quanta Computer Inc.


Size B	Document Number CUP (2/2)	Rev 1A
Date: Monday, May 22, 2006		Sheet 4 of 45



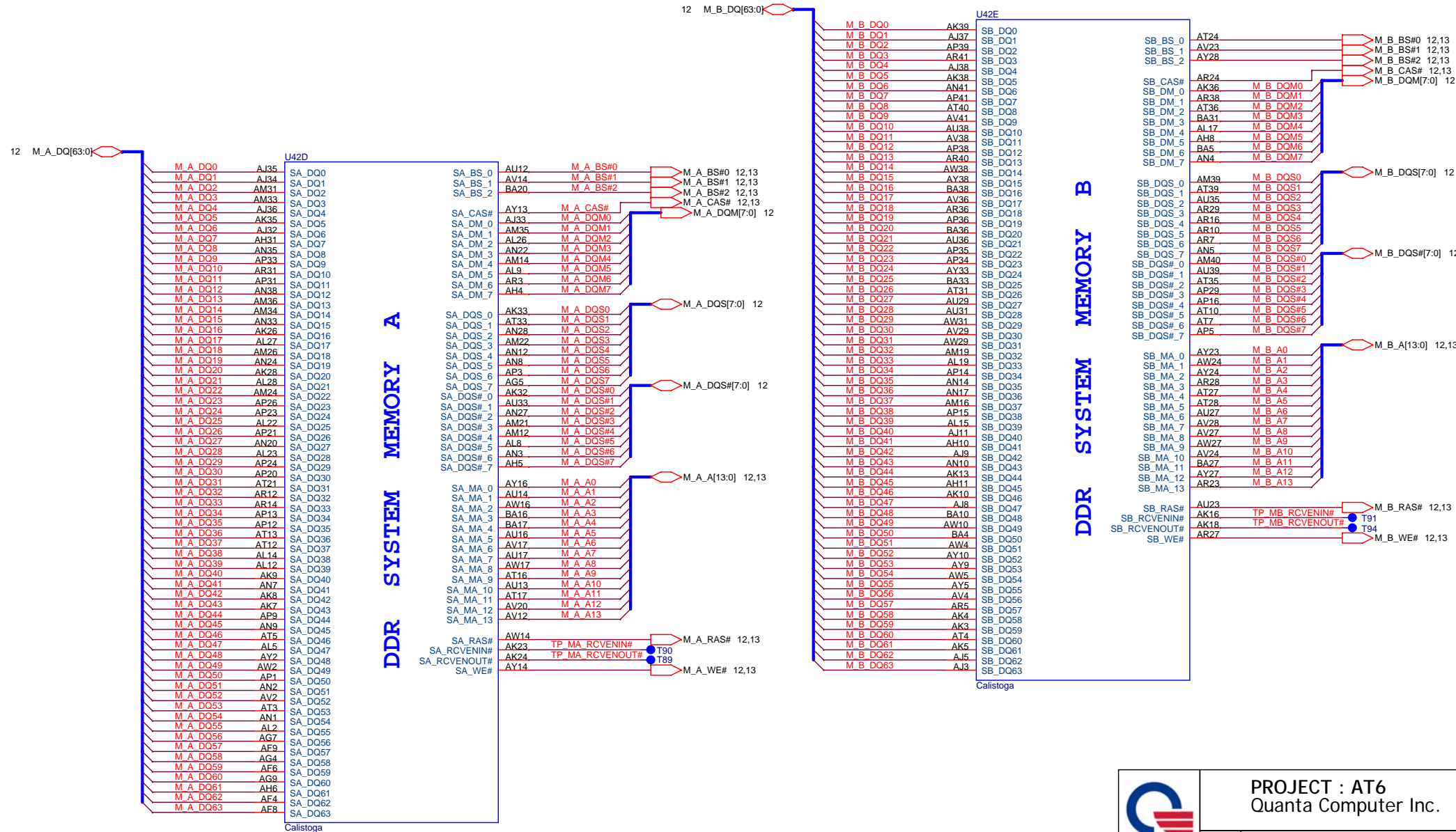
Uninstall R664 , Q47 , Q48 for Intel sighting -> CPU thermal die bug /0506  
 B0 stepping CPU can fix this issue ..



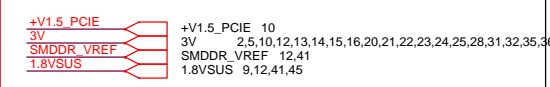
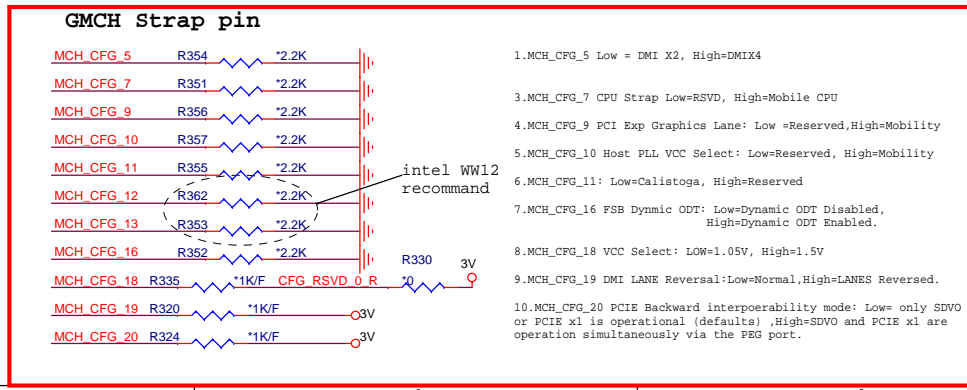
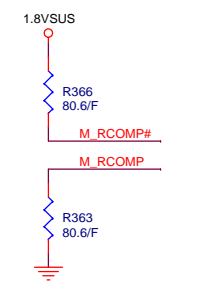
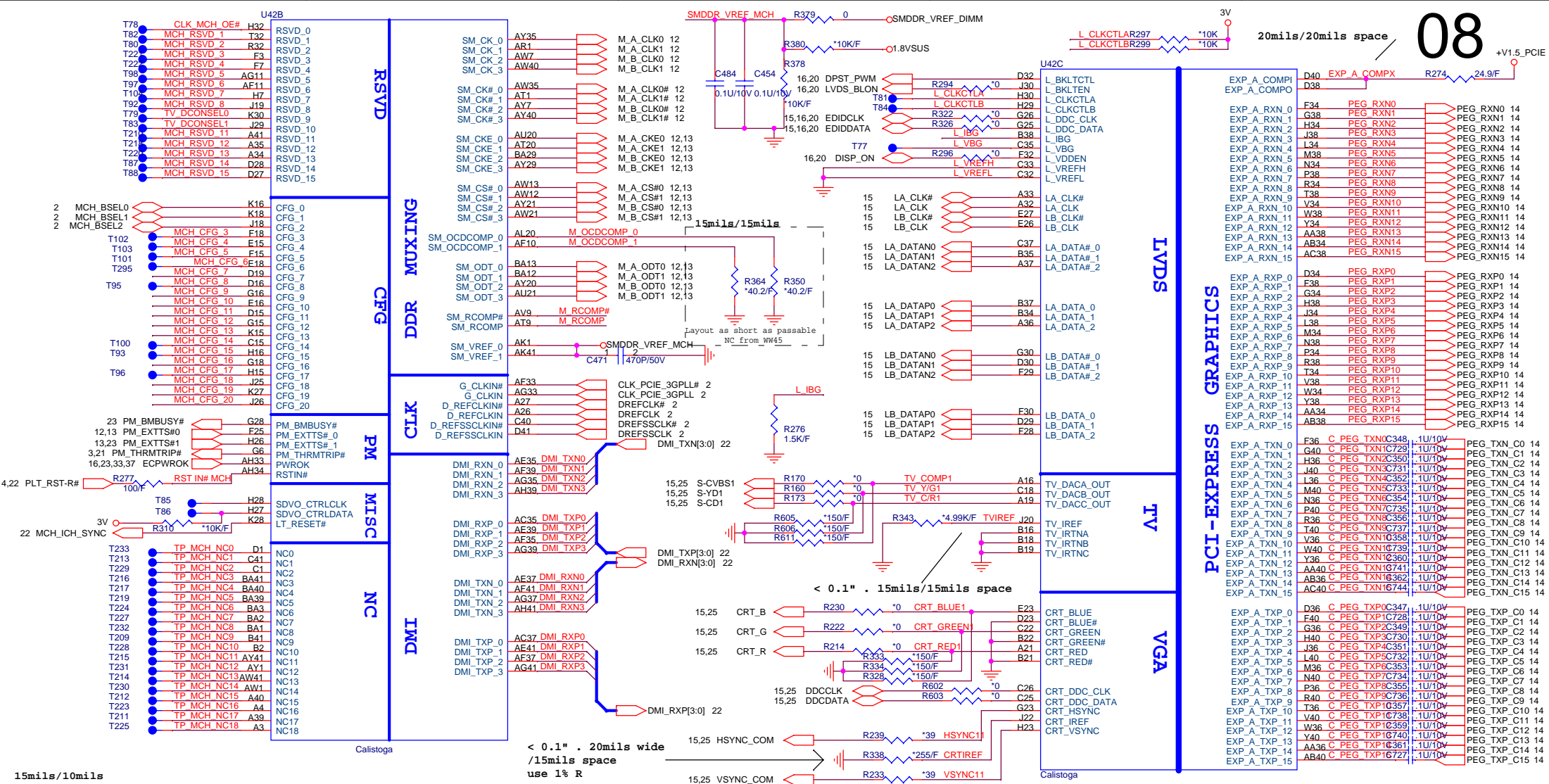


 <b>PROJECT : AT6</b> Quanta Computer Inc.		
Date: Monday, May 22, 2006		Sheet 6 of 45

NB5/RD1/HW2



	<b>PROJECT : AT6</b> Quanta Computer Inc.	
	Size B NB5/RD1/HW2	Document Number GMCH DDR(2/6)
Date: Monday, May 22, 2006		Sheet 7 of 45



## PROJECT : AT6

### Quanta Computer Inc.

Size Custom	Document Number GMCH DMI VIDEO(3/6)	Rev 2A
Date: Monday, May 22, 2006		

08

+V1.5\_PCIE

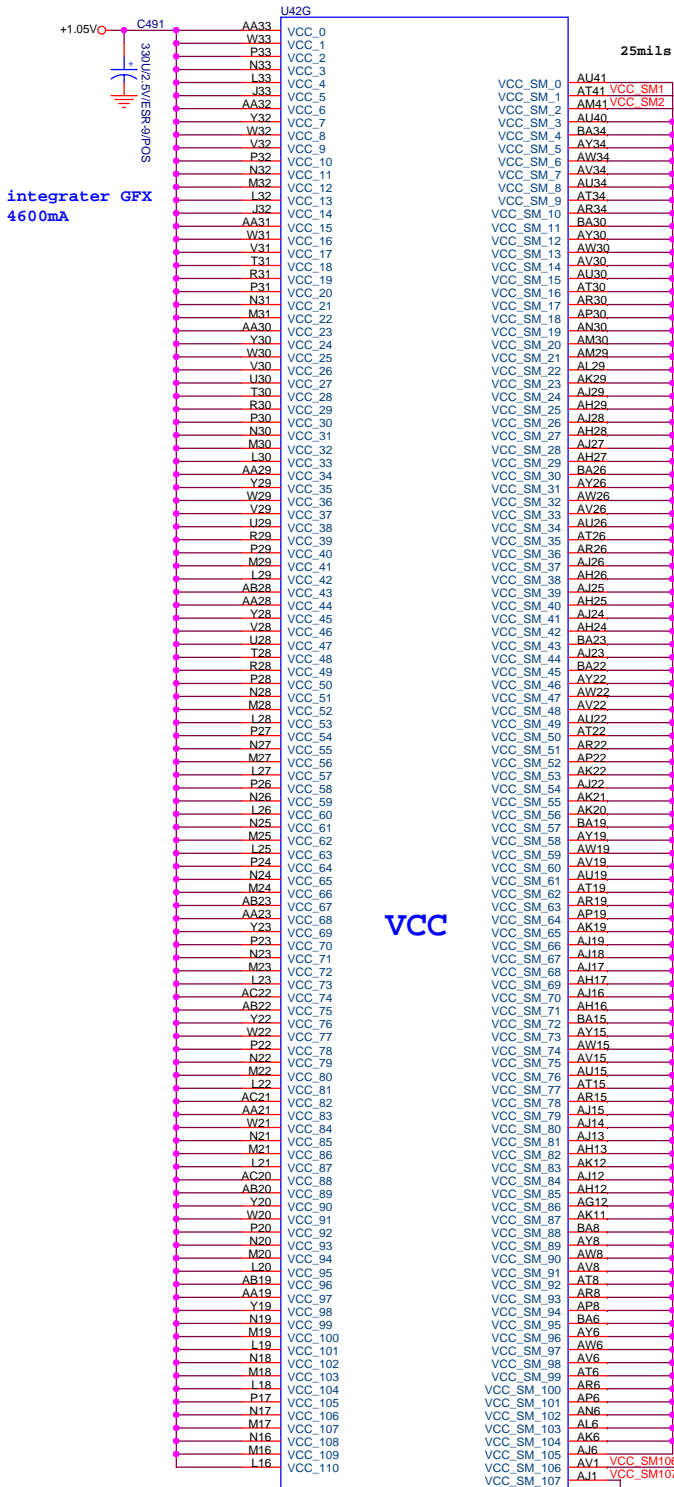
20mils/20mils space

Calistoga

Calistoga

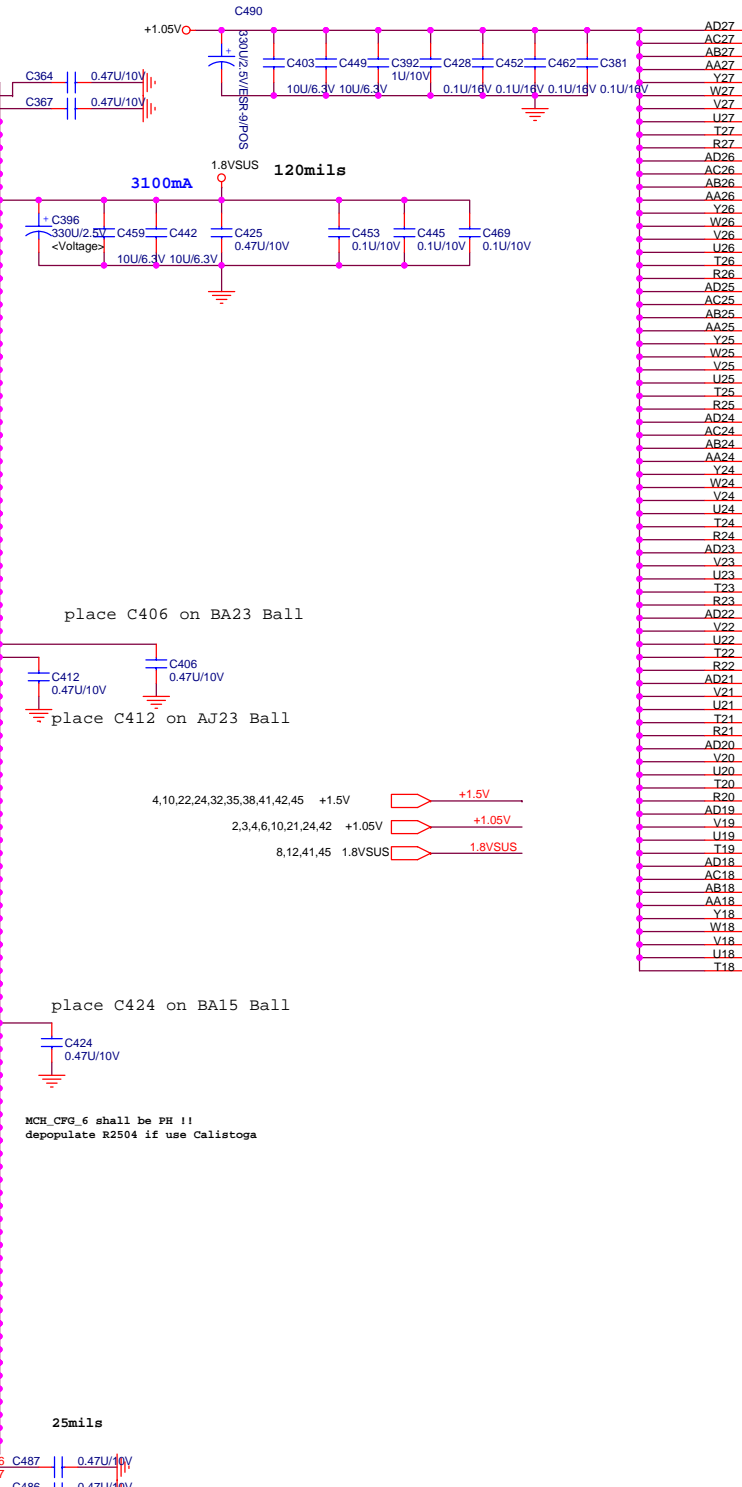


integrater GFX  
4600mA



VCC

Calistoga

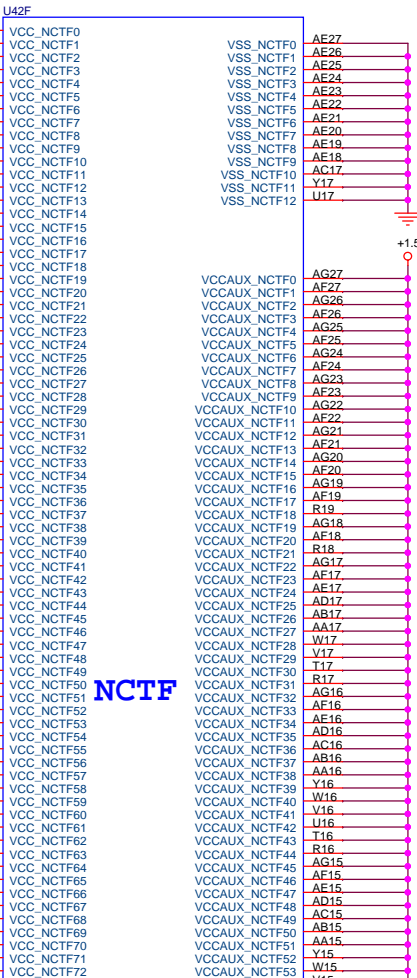


place C406 on BA23 Ball

place C412 on AJ23 Ball

place C424 on BA15 Ball

MCH\_CFG\_6 shall be PH !!  
depopulate R2504 if use Calistoga




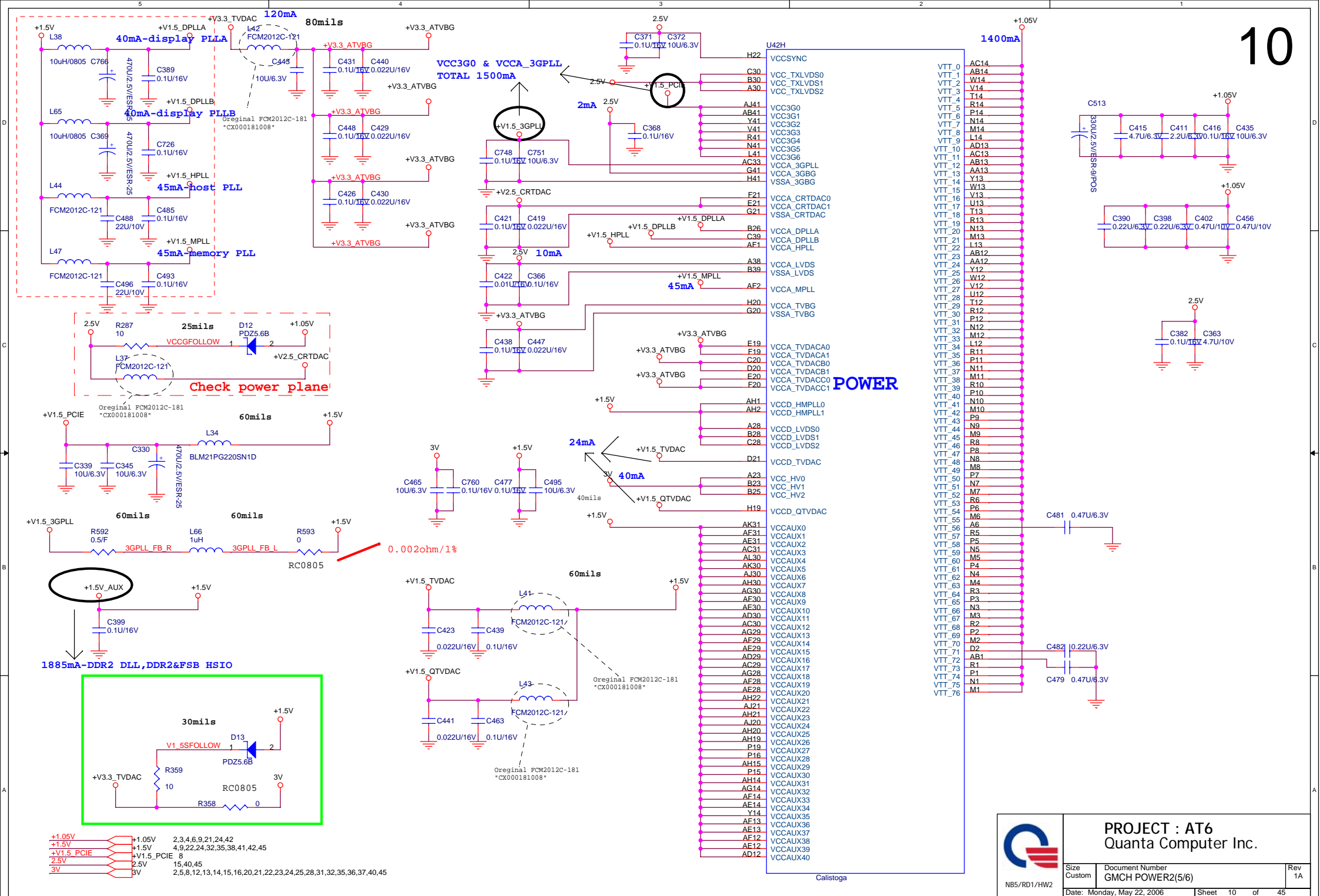
NCTF

Calistoga


09

100mils

		<b>PROJECT : AT6</b> <b>Quanta Computer Inc.</b>	
Size Custom	Document Number GMCH POWER & STRAP(4/6)	Rev 1A	
Date: Monday, May 22, 2006	Sheet 9	of 45	

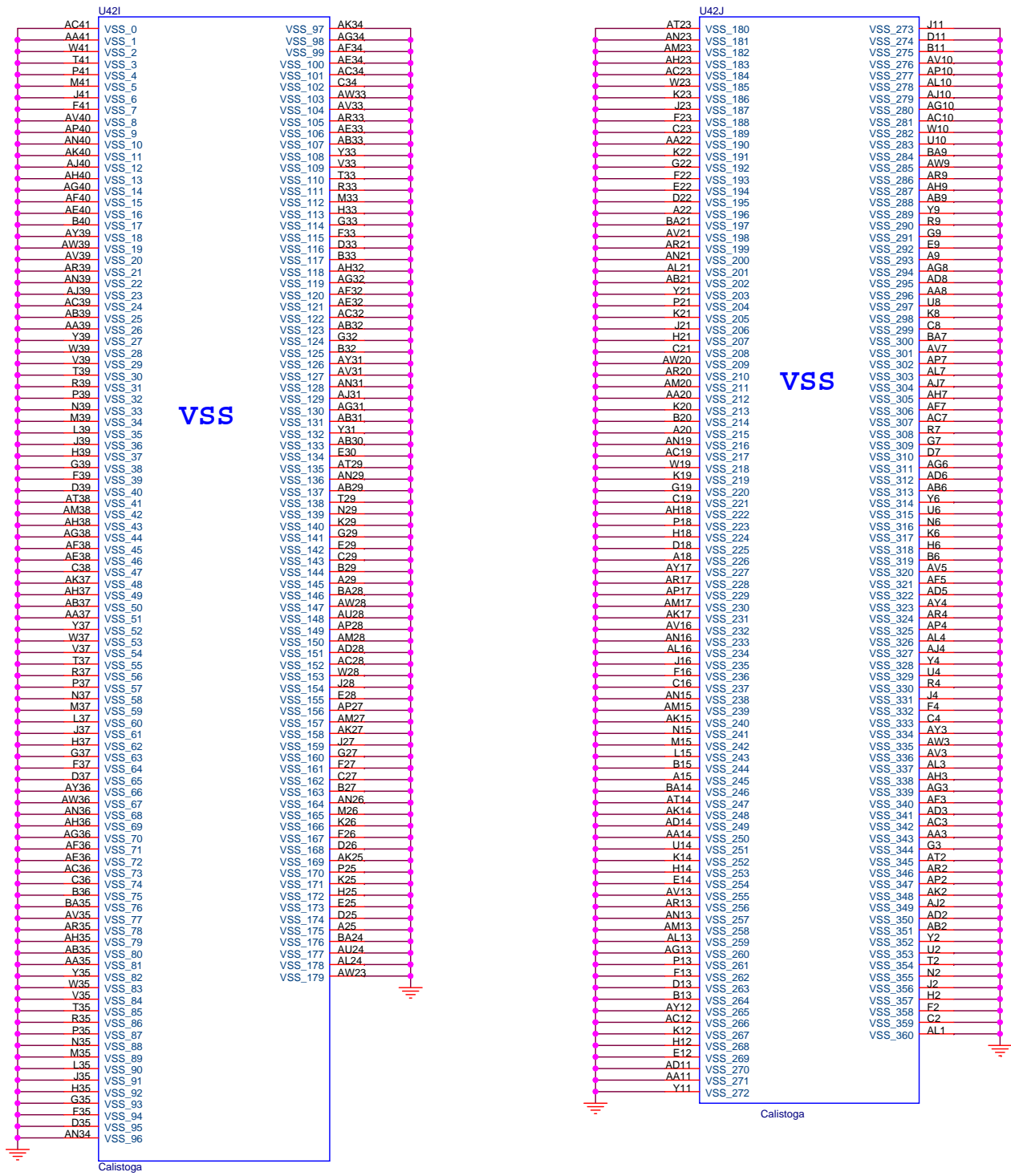


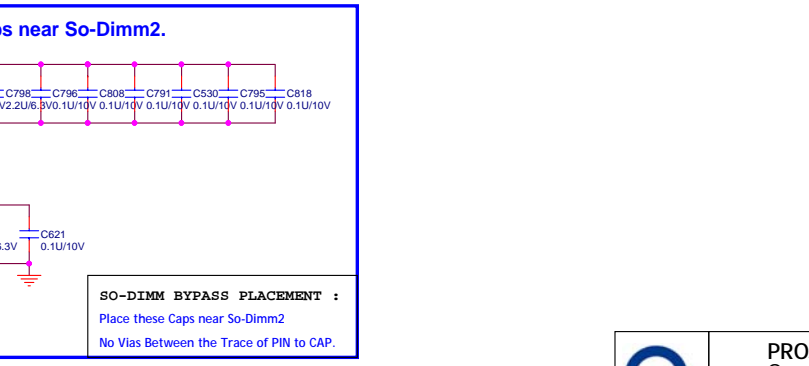
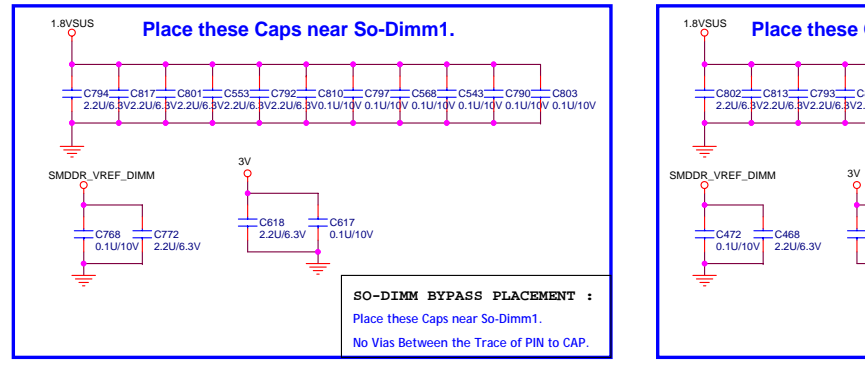
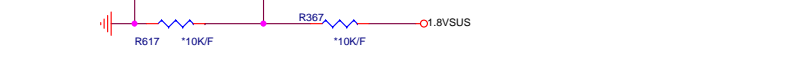
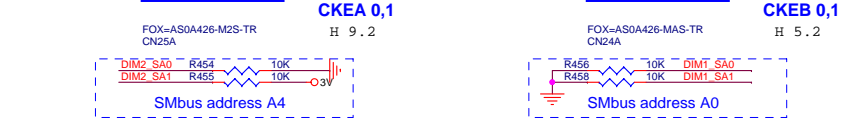
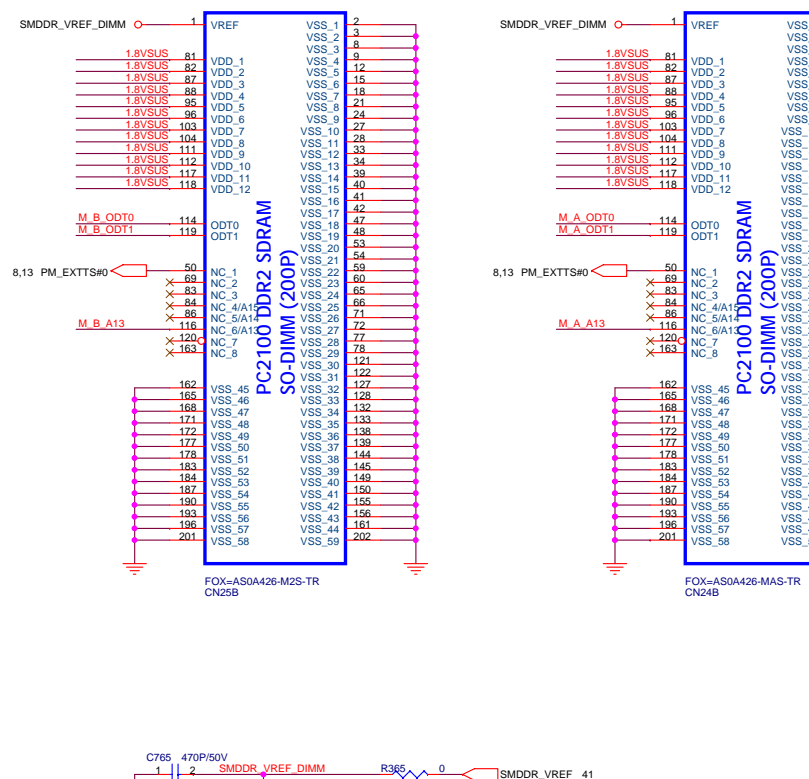
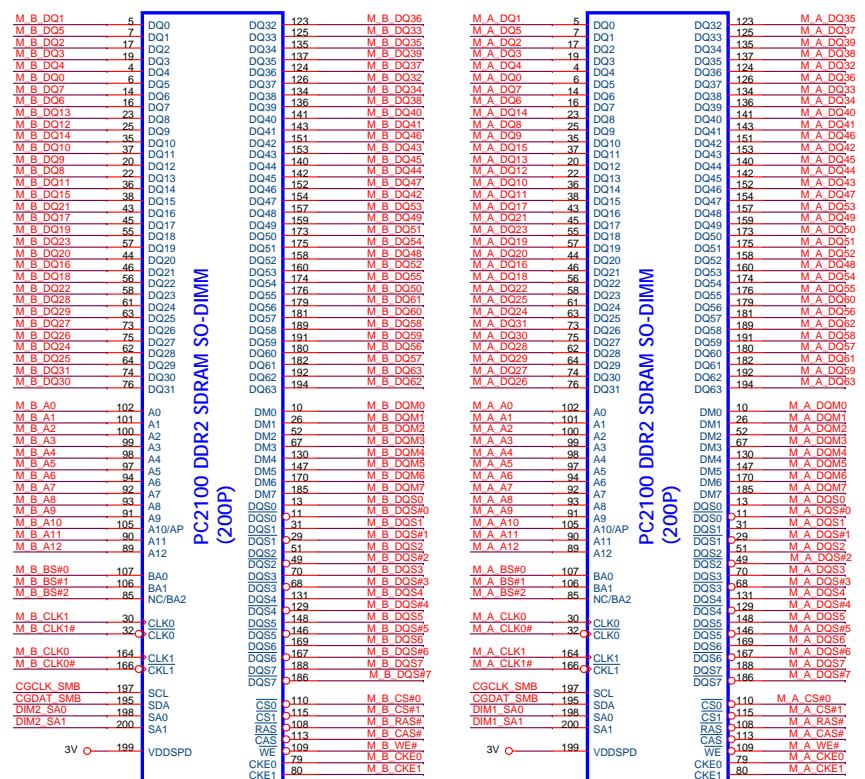
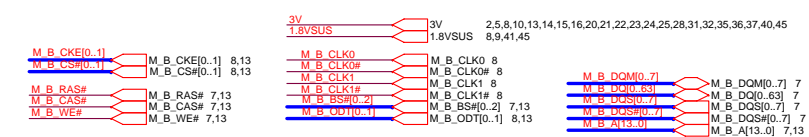
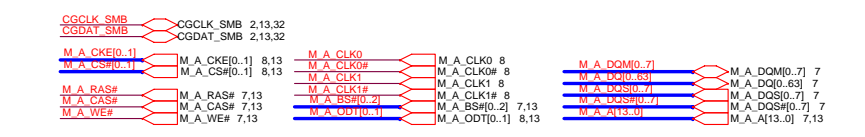
+1.05V	+1.05V	2,3,4,6,9,21,24,42
+1.5V	+1.5V	4,9,22,24,32,35,38,41,42,45
+V1.5_PCIE	+V1.5_PCIE	8
2.5V	2.5V	15,40,45
3V	3V	2,5,8,12,13,14,15,16,20,21,22,23,24,25,28,31,32,35,36,37,40,45



**PROJECT : AT6**  
**Quantas Computer Inc.**

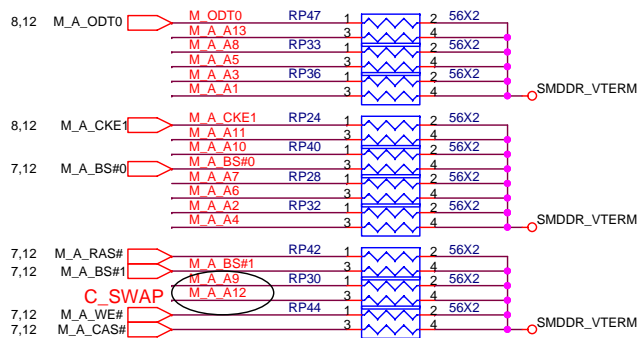
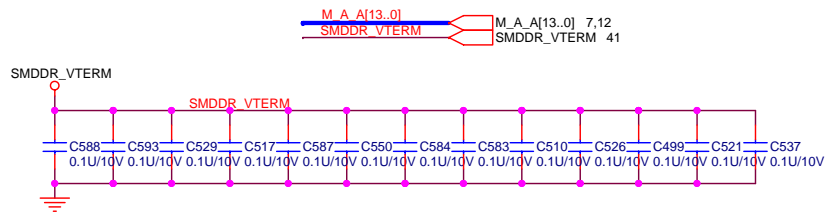
Size Custom	Document Number GMCH POWER2(5/6)	Rev 1A
Date: Monday, May 22, 2006		Sheet 10 of 45



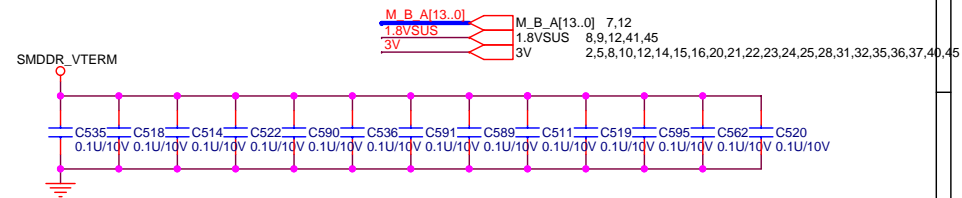


# DDRII DUAL CHANNEL A,B.

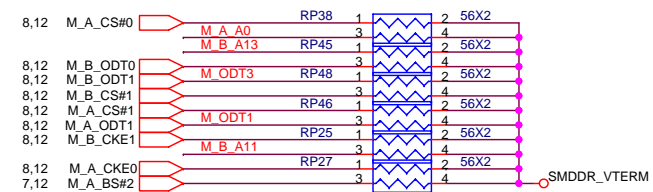
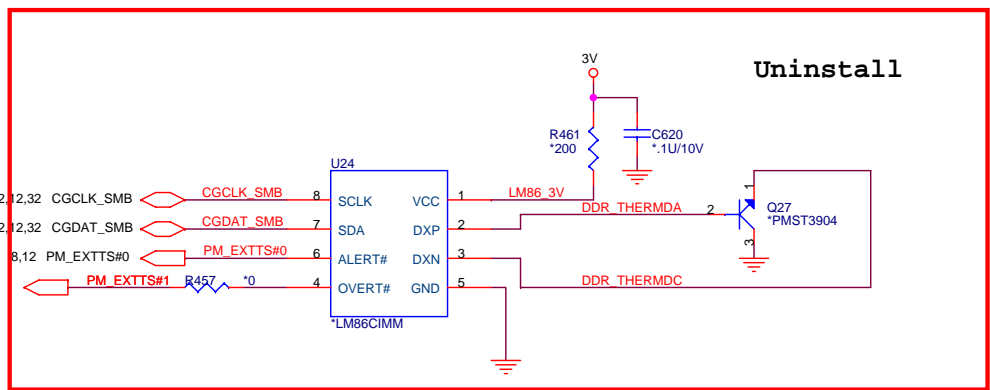
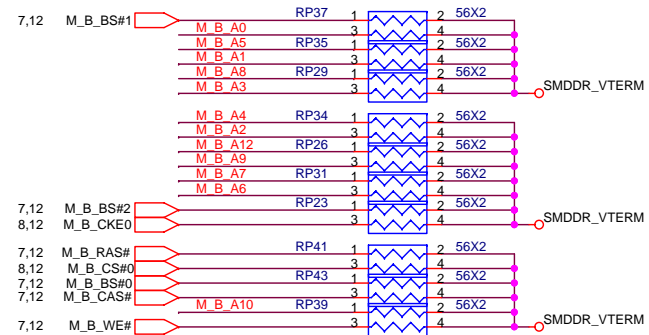
## DDRII A CHANNEL



## DDRII B CHANNEL

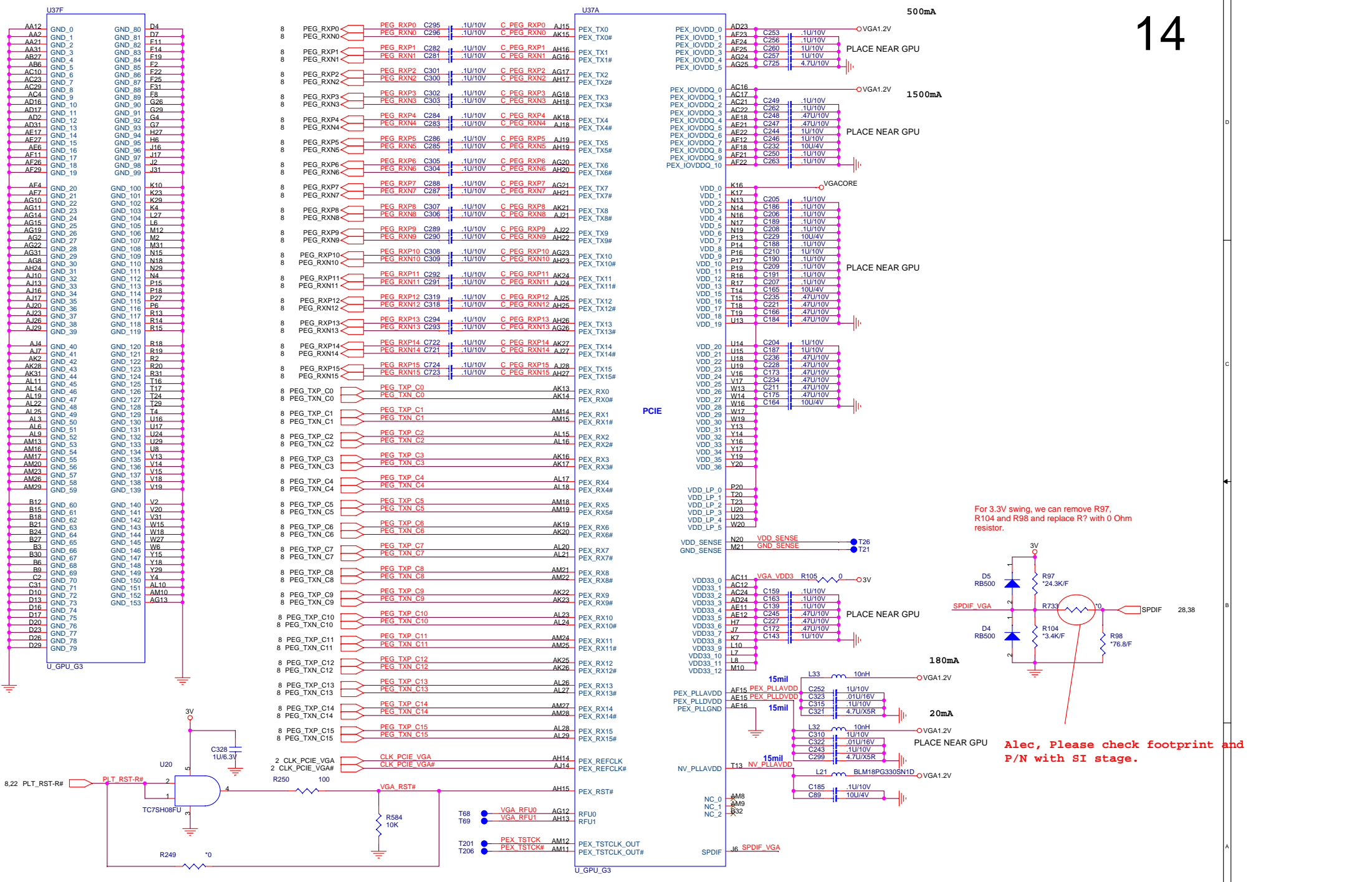


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



**PROJECT : AT6**  
Quanta Computer Inc.

Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Monday, May 22, 2006		
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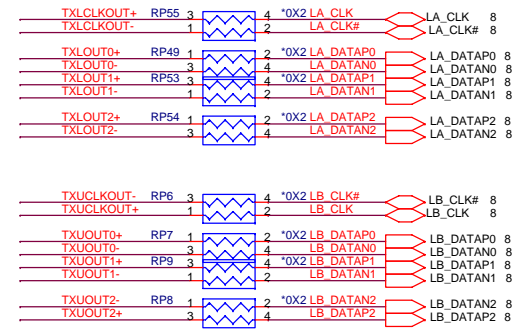
For 3.3V swing, we can remove R97, R104 and R98 and replace R7 with 0 Ohm resistor.

Alec, Please check footprint and P/N with SI stage.

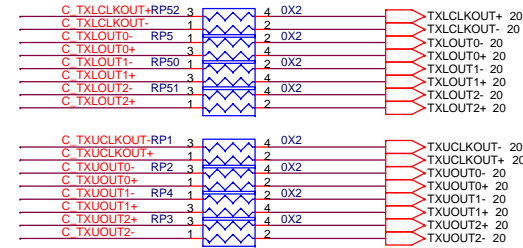


PROJECT : AT6  
Quanta Computer Inc.

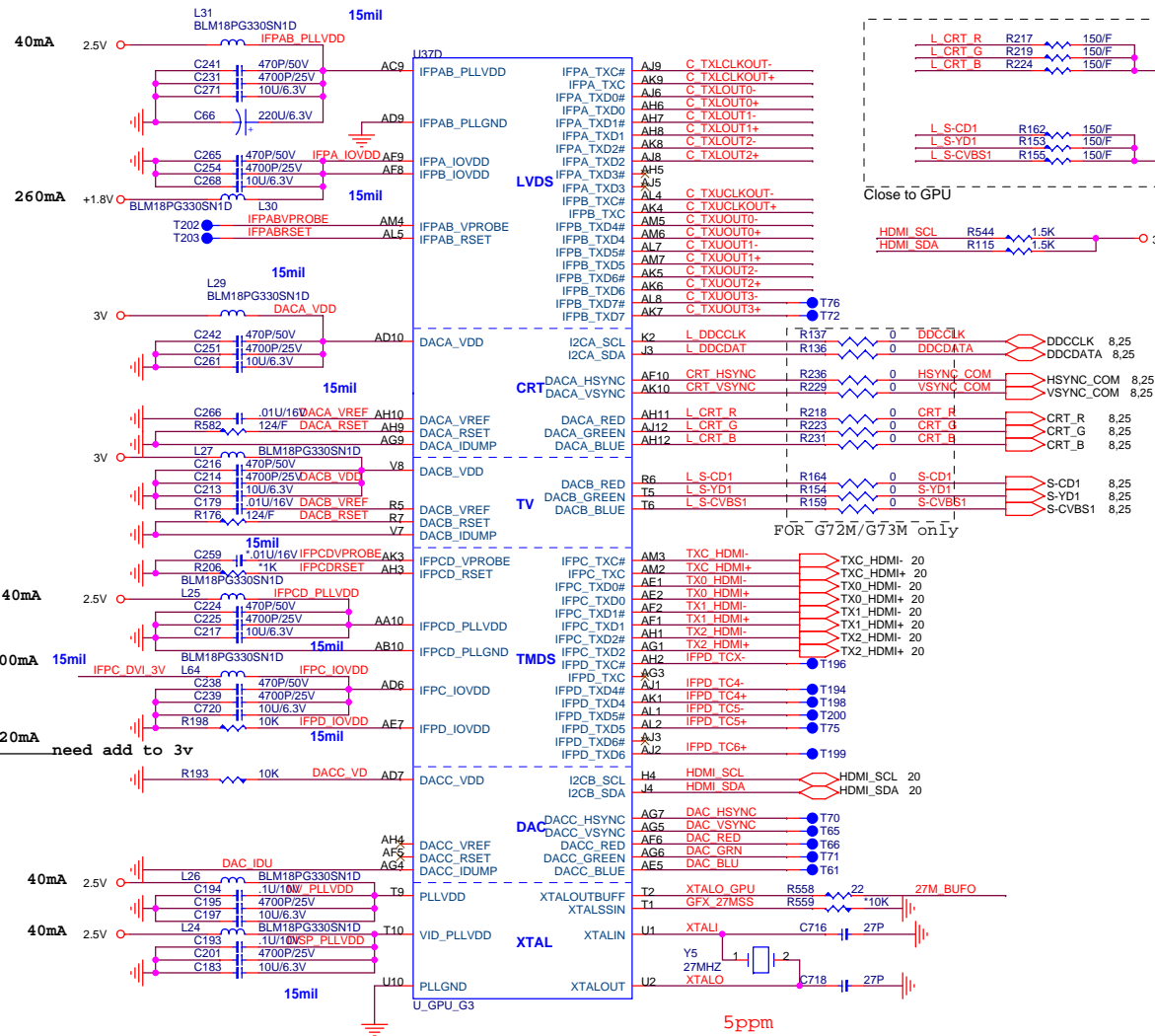
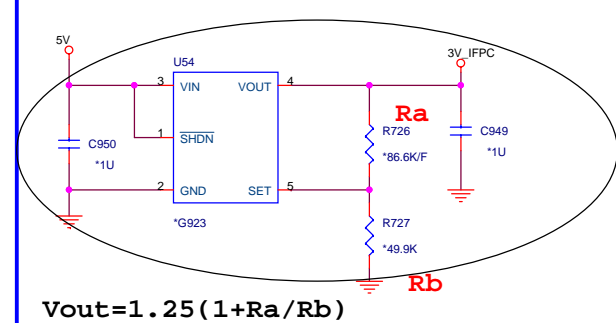
OPTION SIGNAL FROM NB FOR UMA VGA



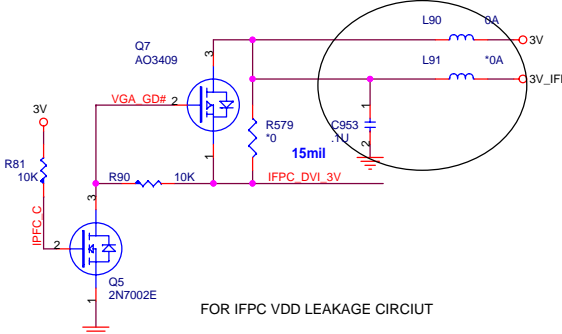
OPTION SIGNAL FROM Nvidia to VGA



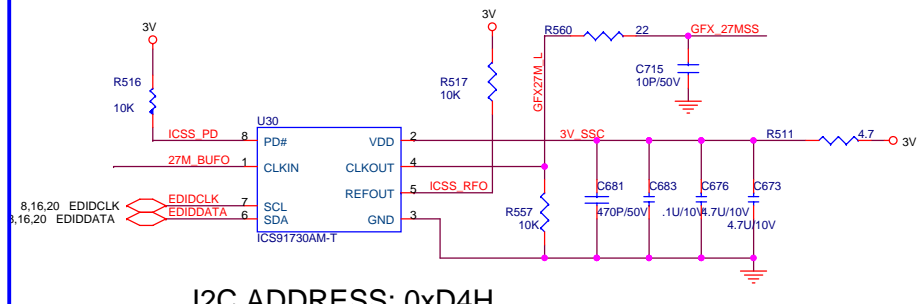
C\_For HDMI Nvidia's PUN issue

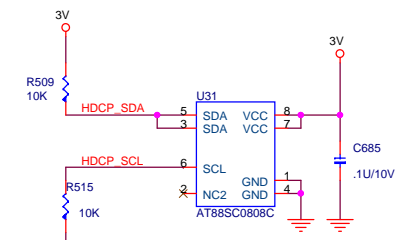
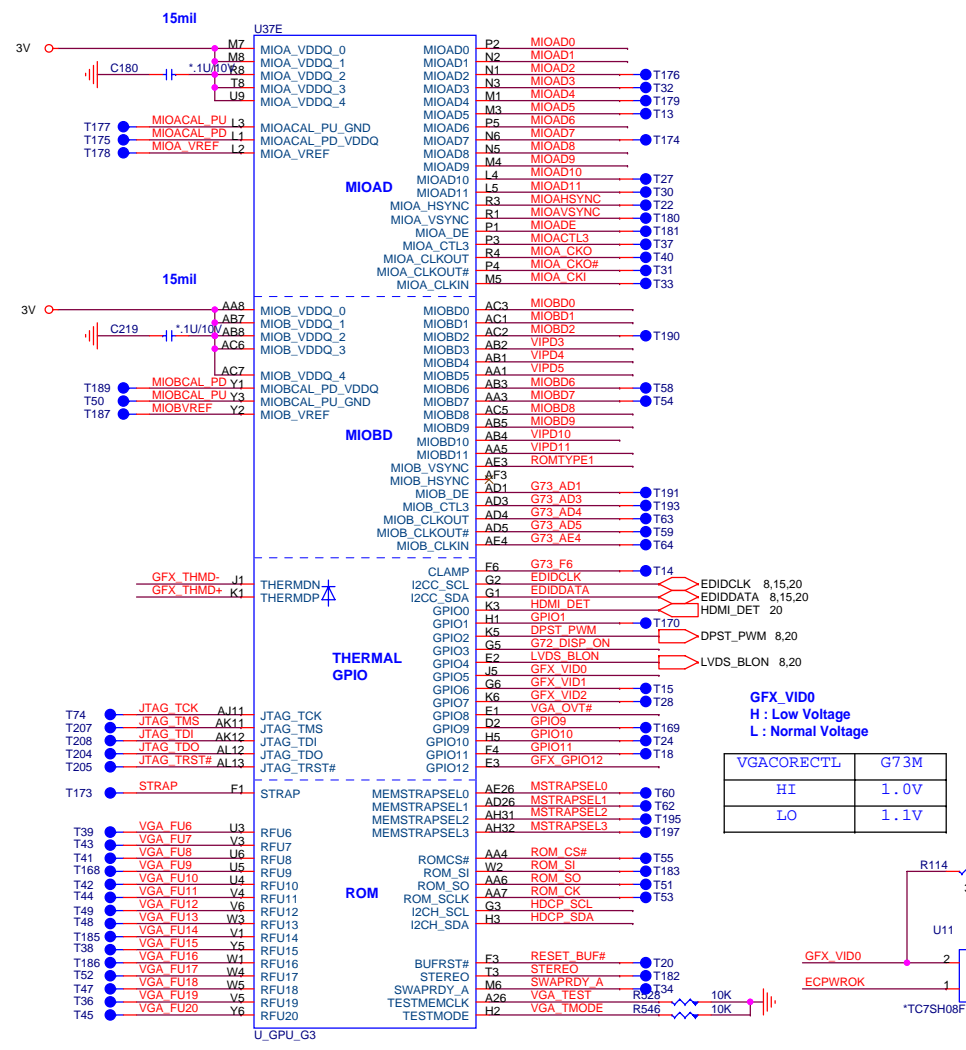


C\_For HDMI Nvidia's PUN issue



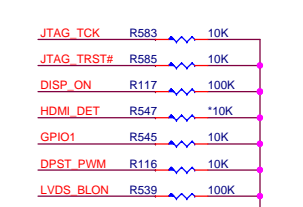
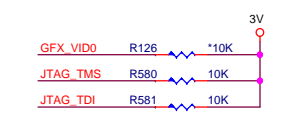
SPREAD SPECTRUM





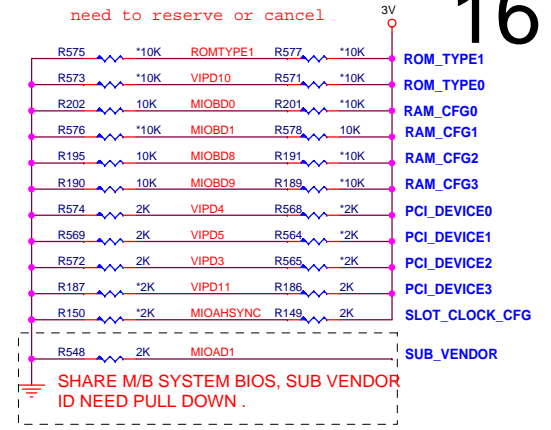
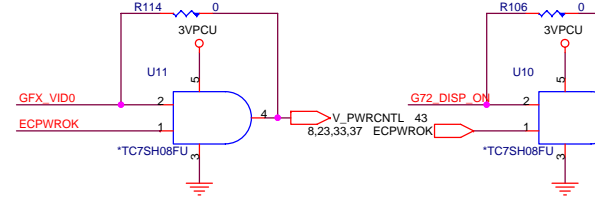
**PCI DEVICE**

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved



**GFX\_VID0**  
H : Low Voltage  
L : Normal Voltage

VGACORECTL	G73M
HI	1.0V
LO	1.1V

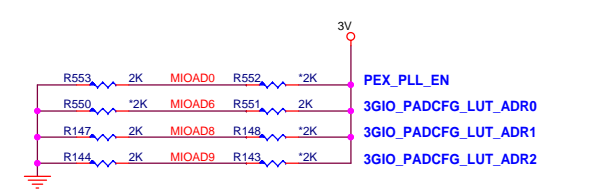
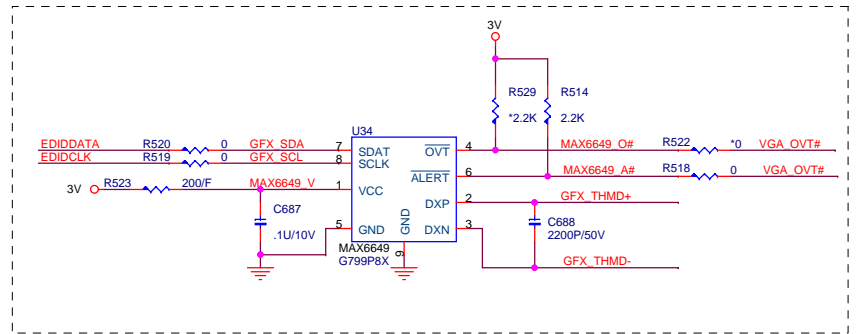
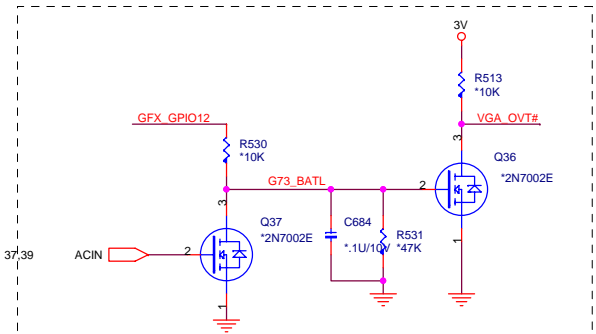


**G72M VRAM Configuration Table**

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

**G73M VRAM Configuration Table**

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



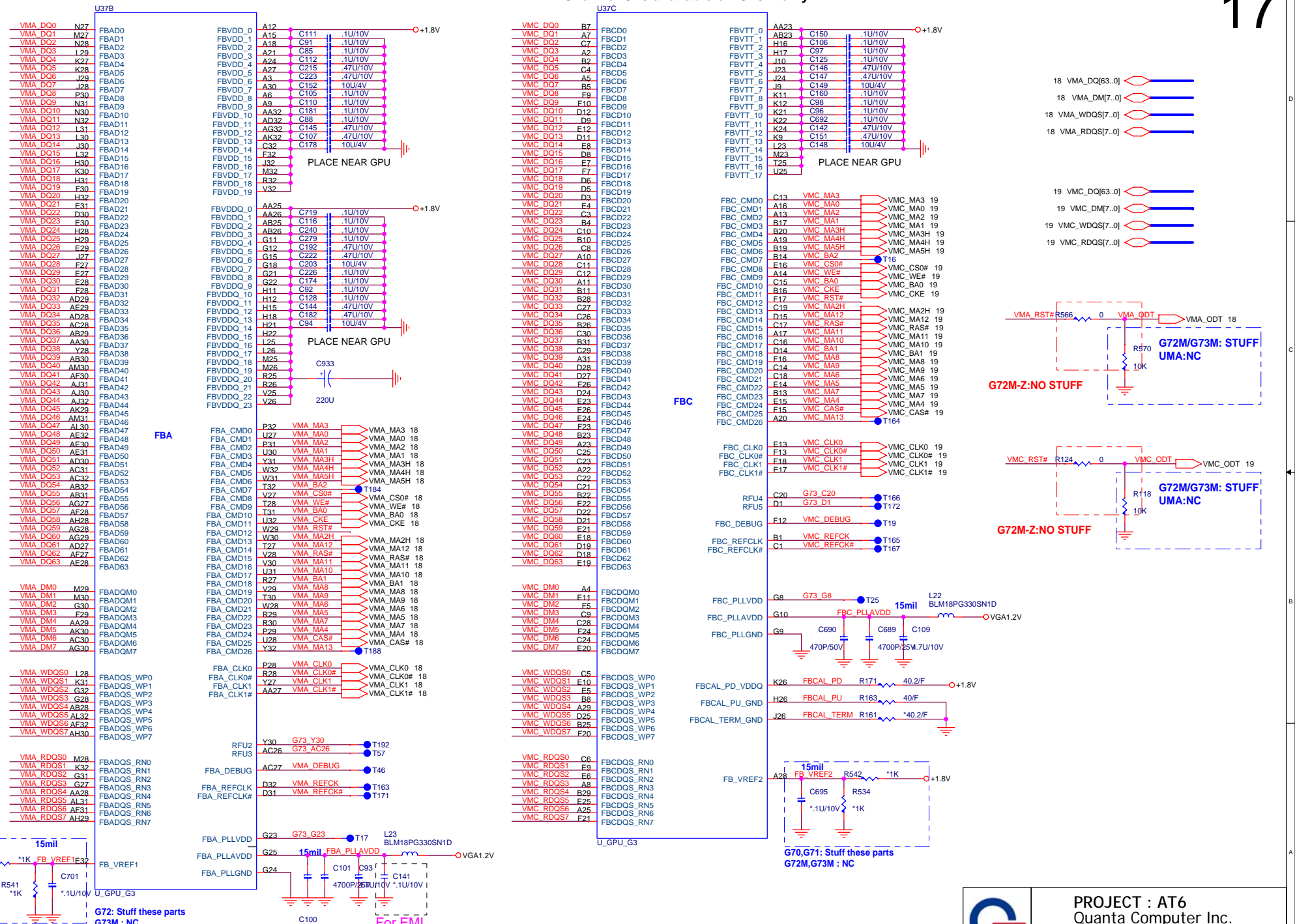
FOR BATTERY MODE FUNCTION  
GFX\_GPIO12=H ENABLE  
GFX\_GPIO12=L DISABLE

**PROJECT : AT6**  
Quanta Computer Inc.

Size Custom	Document Number NVG73M (ROM/GPIO/STRAP)	Rev 2A
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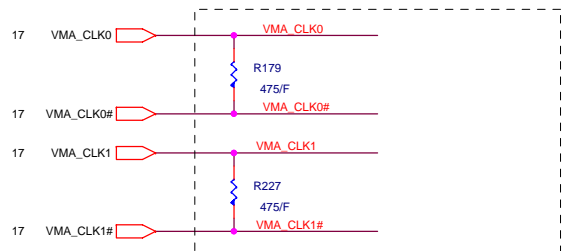
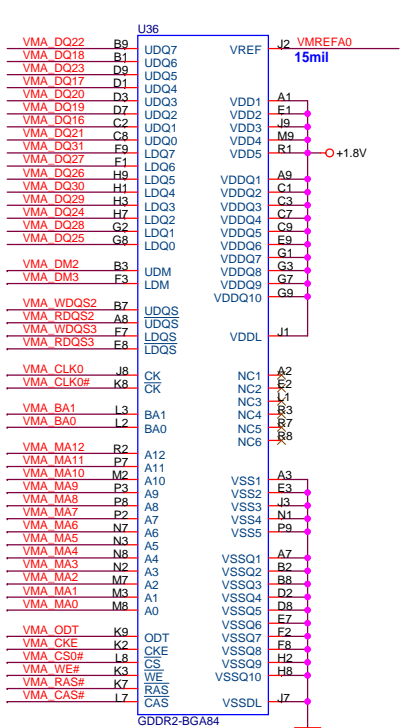
Channel C is available on G73M only



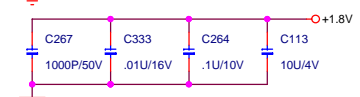
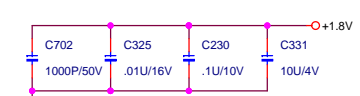
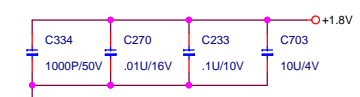
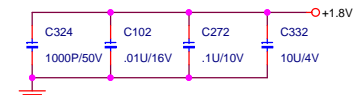
PROJECT : AT6  
Quanta Computer Inc.

Size Custom	Document Number NVG73M (MEM I/F)	Rev 2A
Date: Monday, May 22, 2006 Sheet 17 of 45		

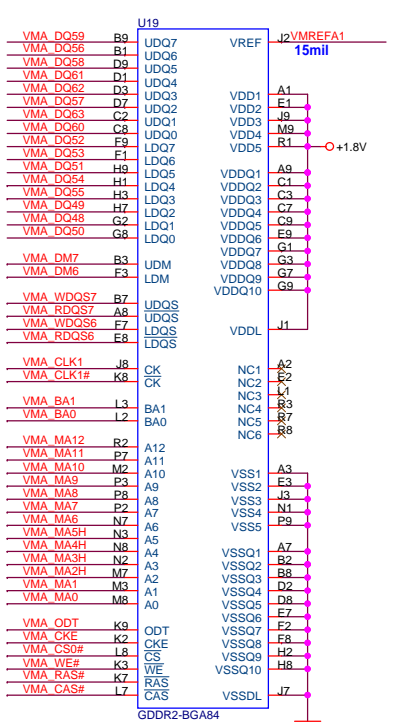
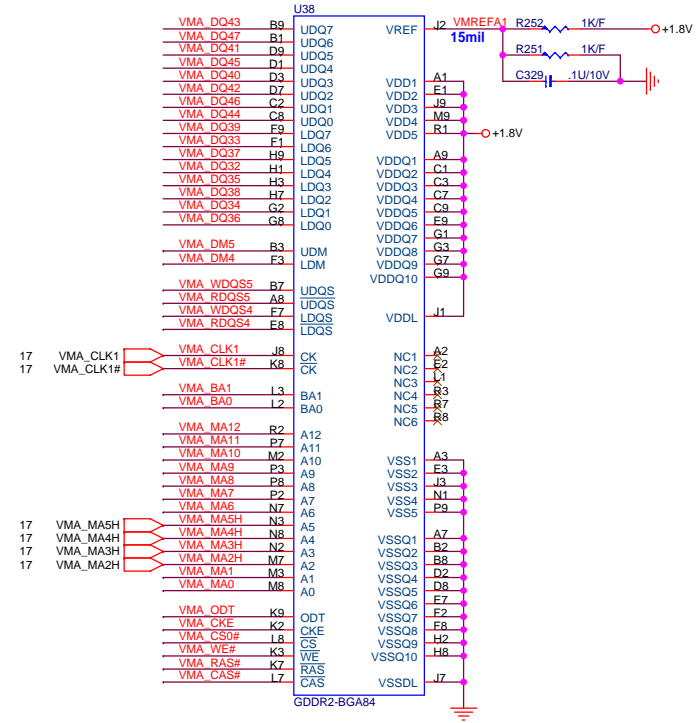
$VREF = FBVDDQ \cdot \frac{R_{bot}}{R_{top} + R_{bot}}$



G72M-Z: NO STUFF  
 G72M: 120 ohm  
 G73M: 480 ohm

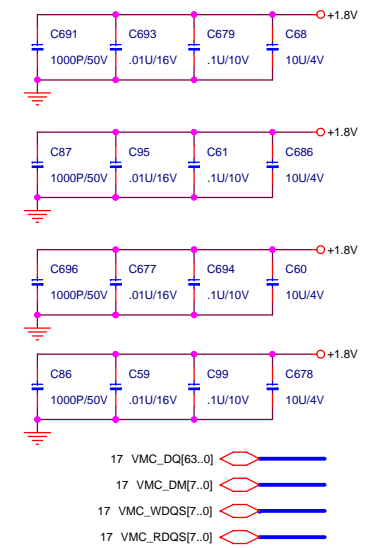
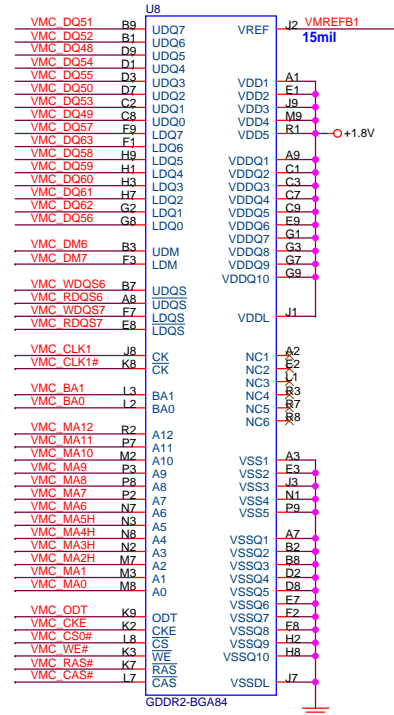
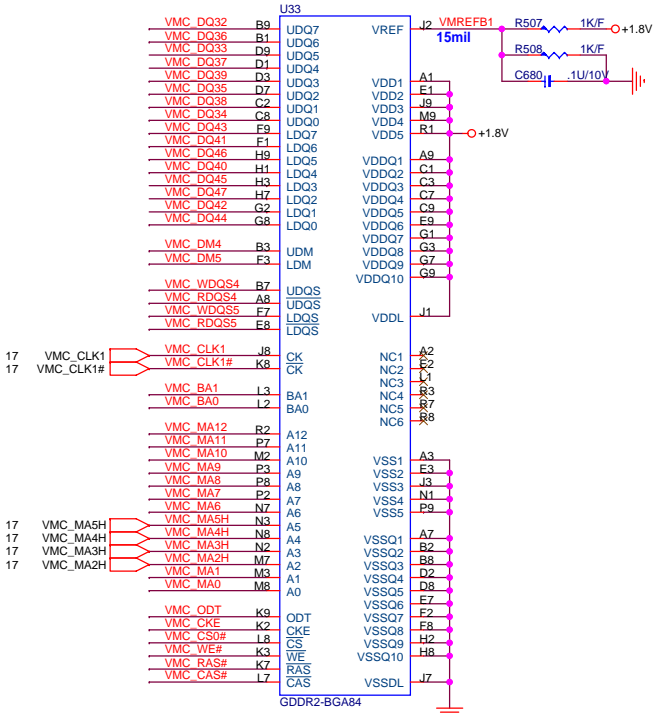
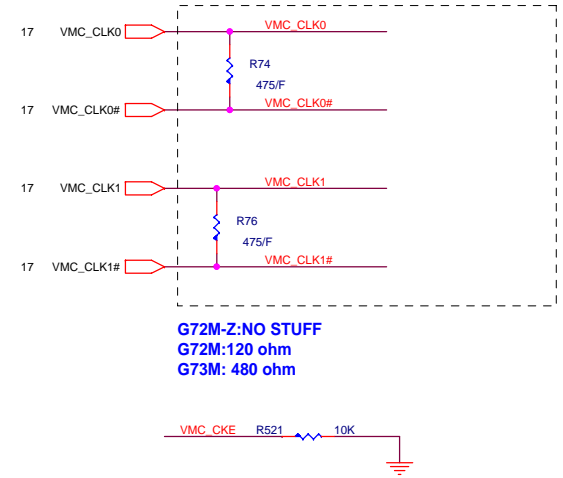
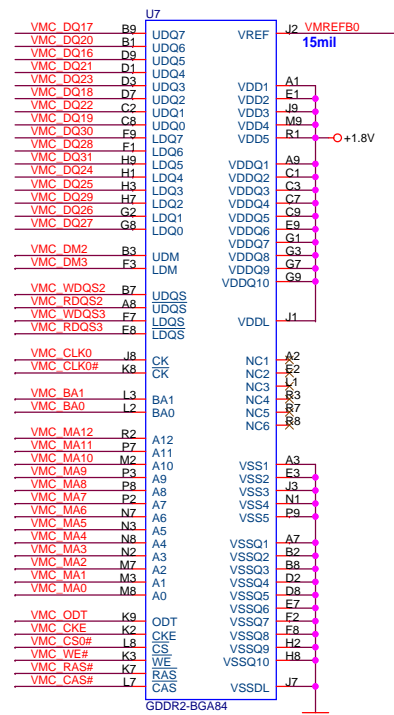
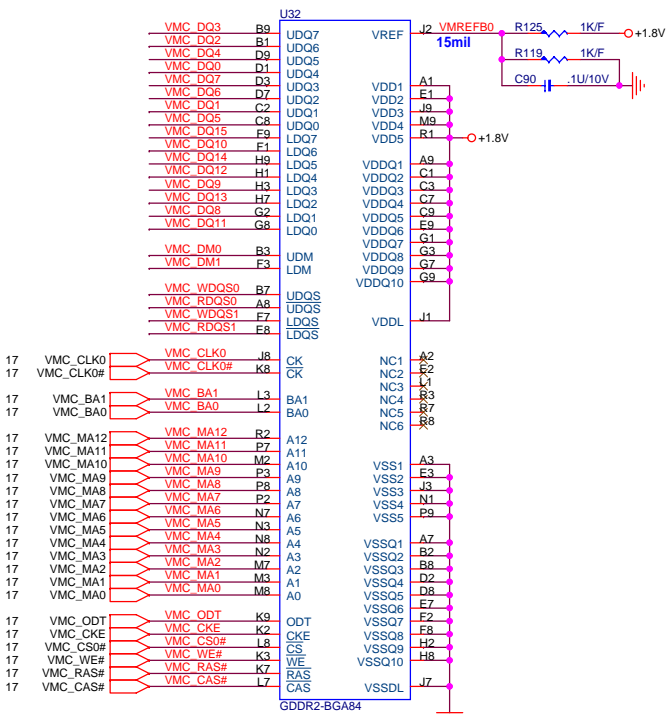


256Mb : AKD5JGAT\*05  
 512Mb : AKD59G-T\*01

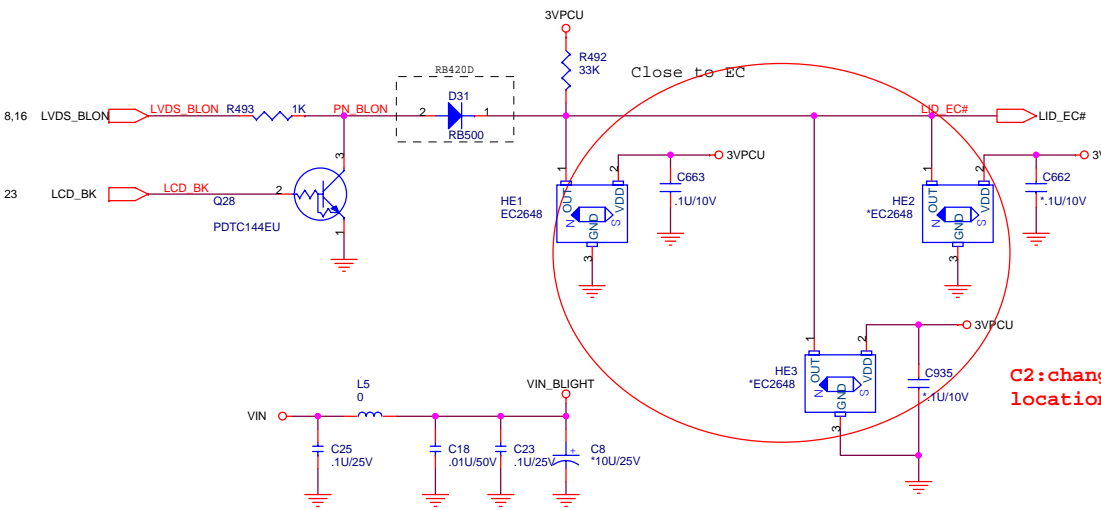
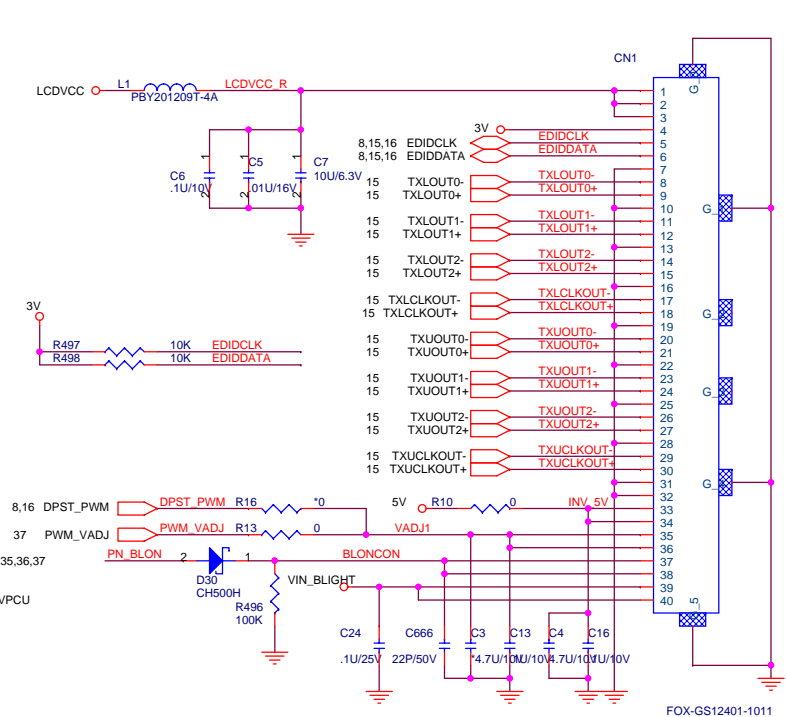
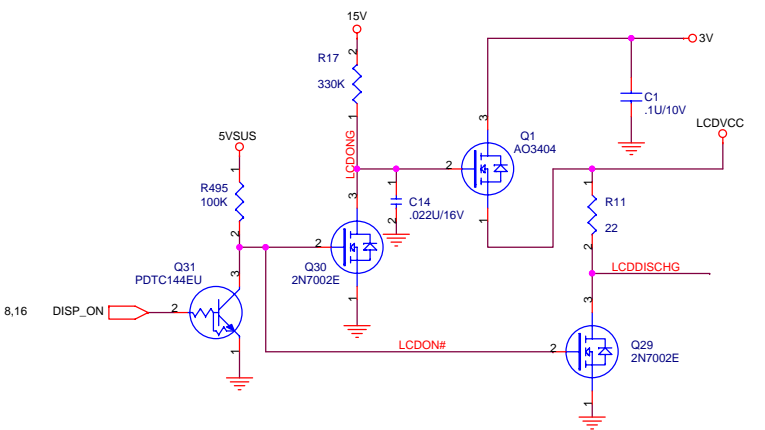


**PROJECT : AT6**  
 Quanta Computer Inc.

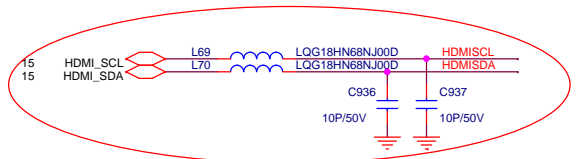
Size Custom Document Number NVG73M VRAN-1(GDDR2 BGA84) Rev 1A  
 Date: Monday, May 22, 2006 Sheet 18 of 45



	PROJECT : AT6 Quanta Computer Inc.	
	Size Custom Date: Monday, May 22, 2006	Document Number NVG73M VREM-2(GDDR2 BGA84)

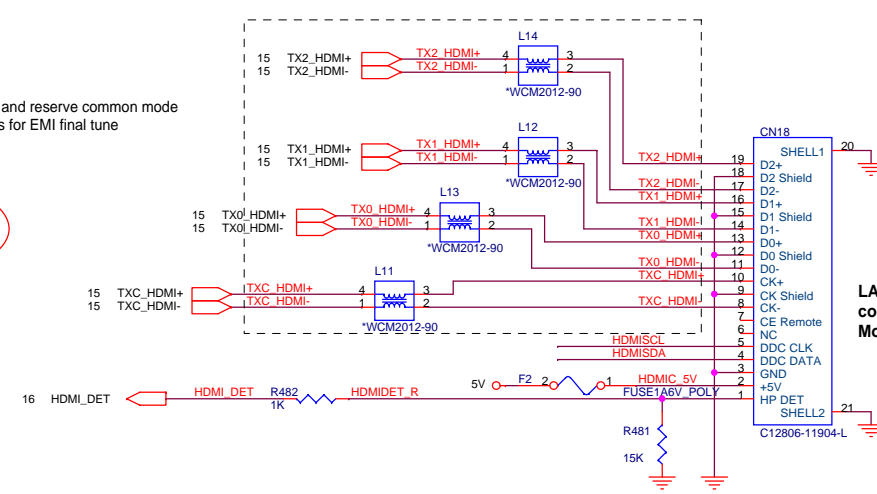


C2:change HE1,HE2 layout location and Add HE3

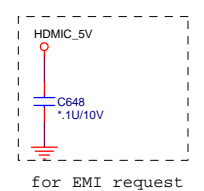


For HDMI Nvidia's PUN issue

C3:Add L69,L70,C936,C937 PUN issue



### HDMI PORT

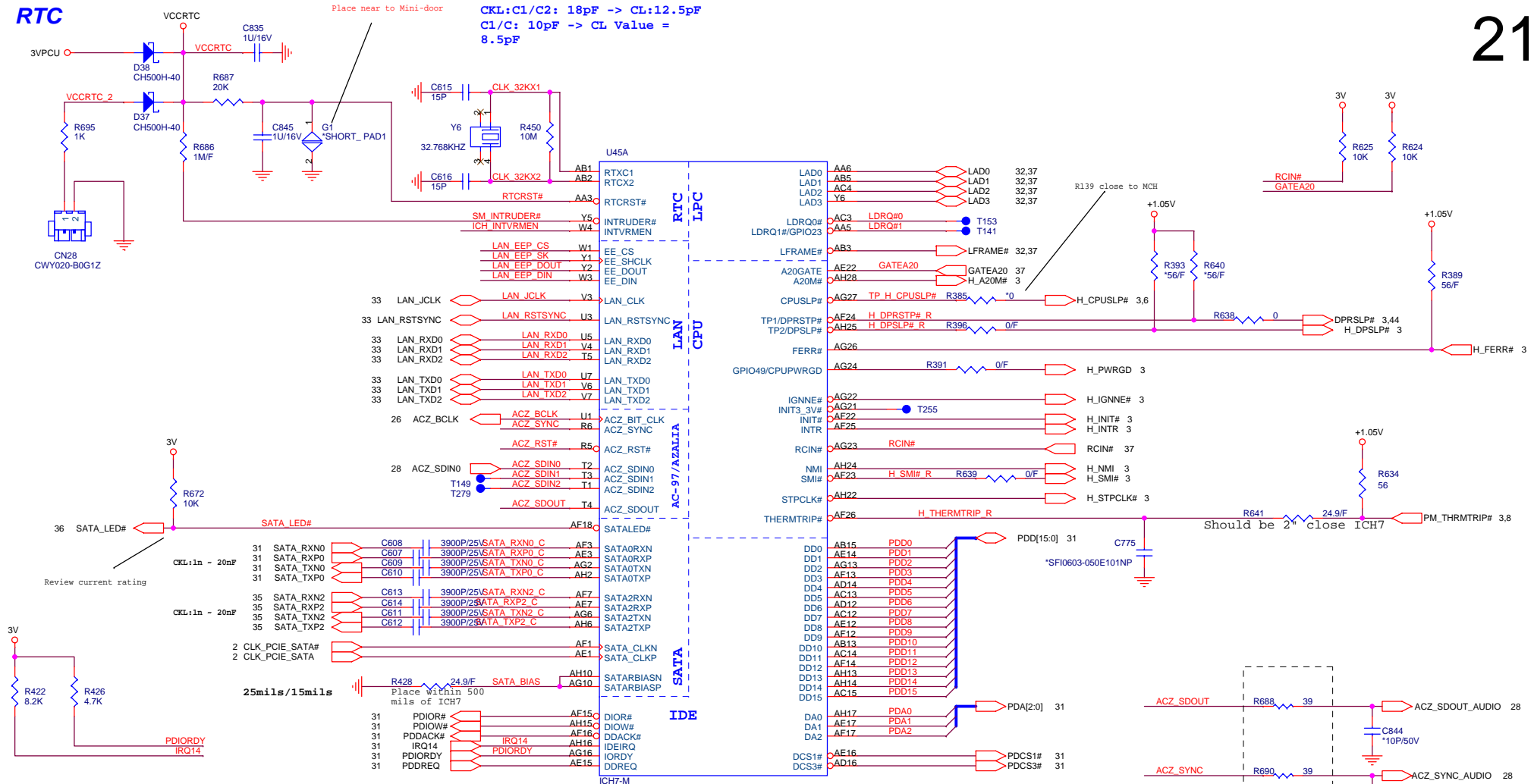


for EMI request

LAYOUT must support connectors from JAE, Molex and Acon.

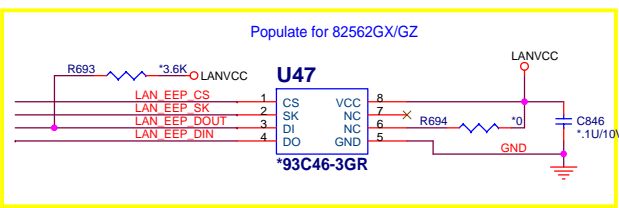
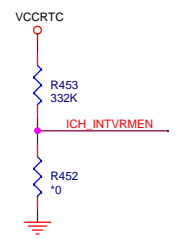
	PROJECT : AT6 Quanta Computer Inc.	
	Size Custom Document Number LCD CONN/HDMI CONN Date: Monday, May 22, 2006	Rev 2A Sheet 20 of 45

CLK: C1/C2: 18pF -> CL: 12.5pF  
 C1/C: 10pF -> CL Value = 8.5pF



**ICH7 internal VR enable strap**

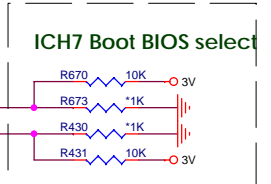
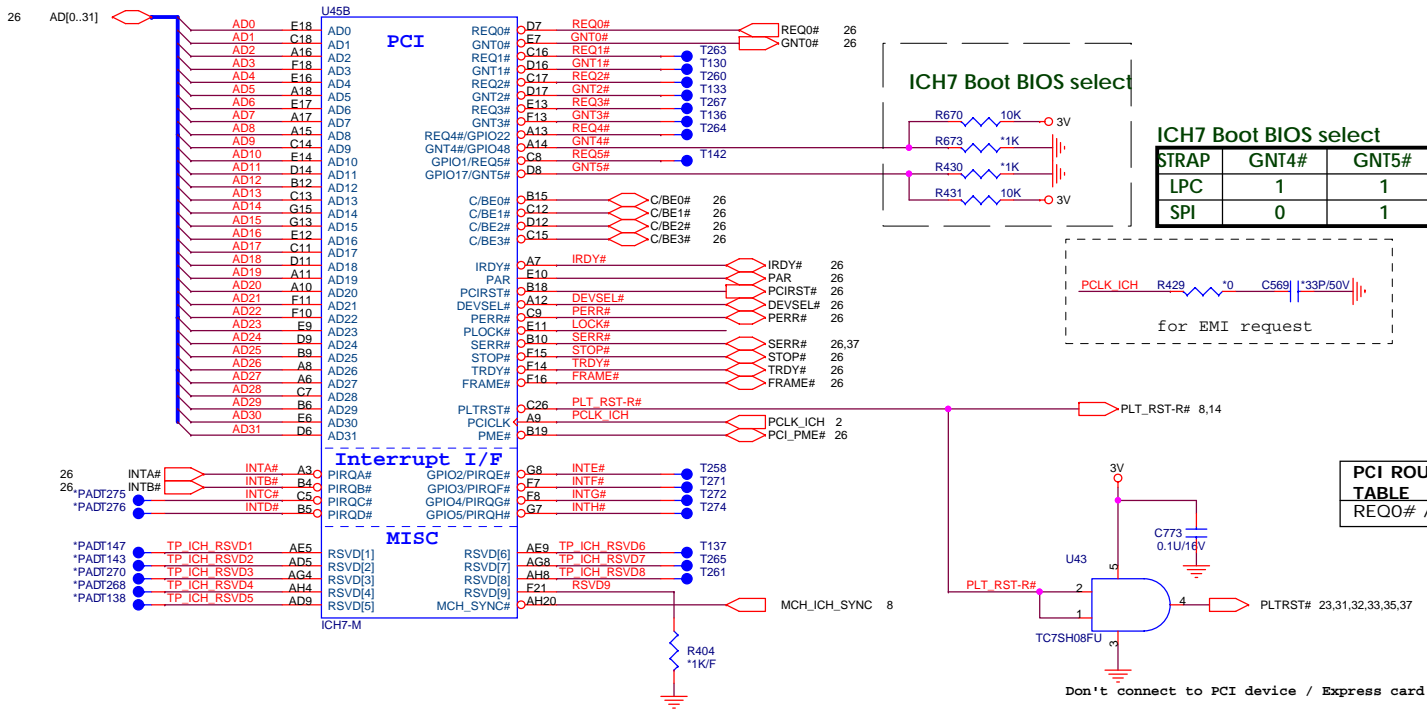
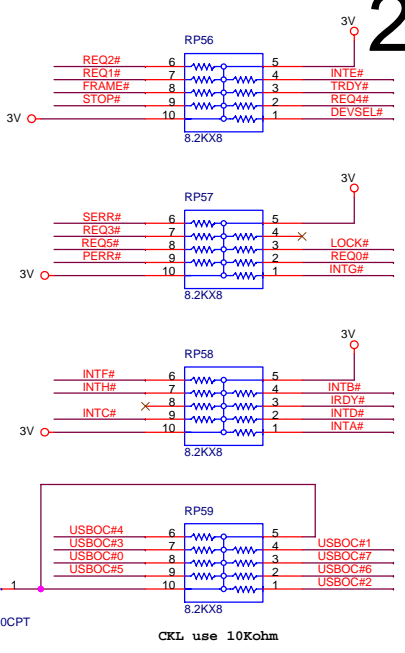
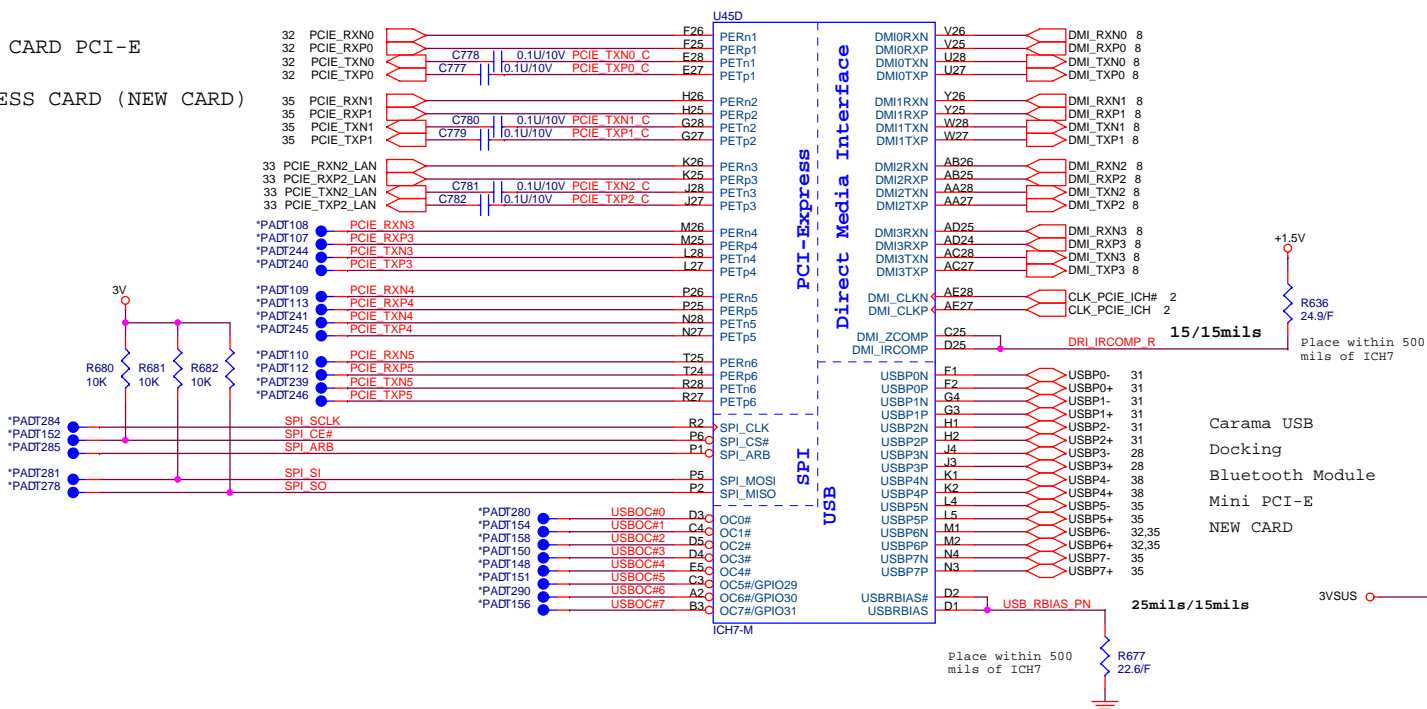
	INTVRMEN
Enable (default)	1
Disable	0



**PROJECT : AT6**  
 Quanta Computer Inc.

MINI CARD PCI-E  
EXPRESS CARD (NEW CARD)

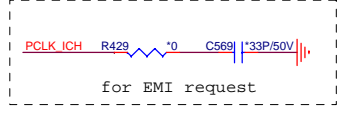
22



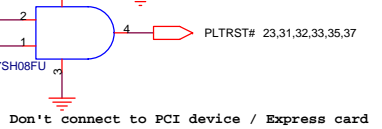
ICH7 Boot BIOS select

STRAP	GNT4#	GNT5#
LPC	1	1
SPI	0	1

(default)



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#, INTB#	RICOH832



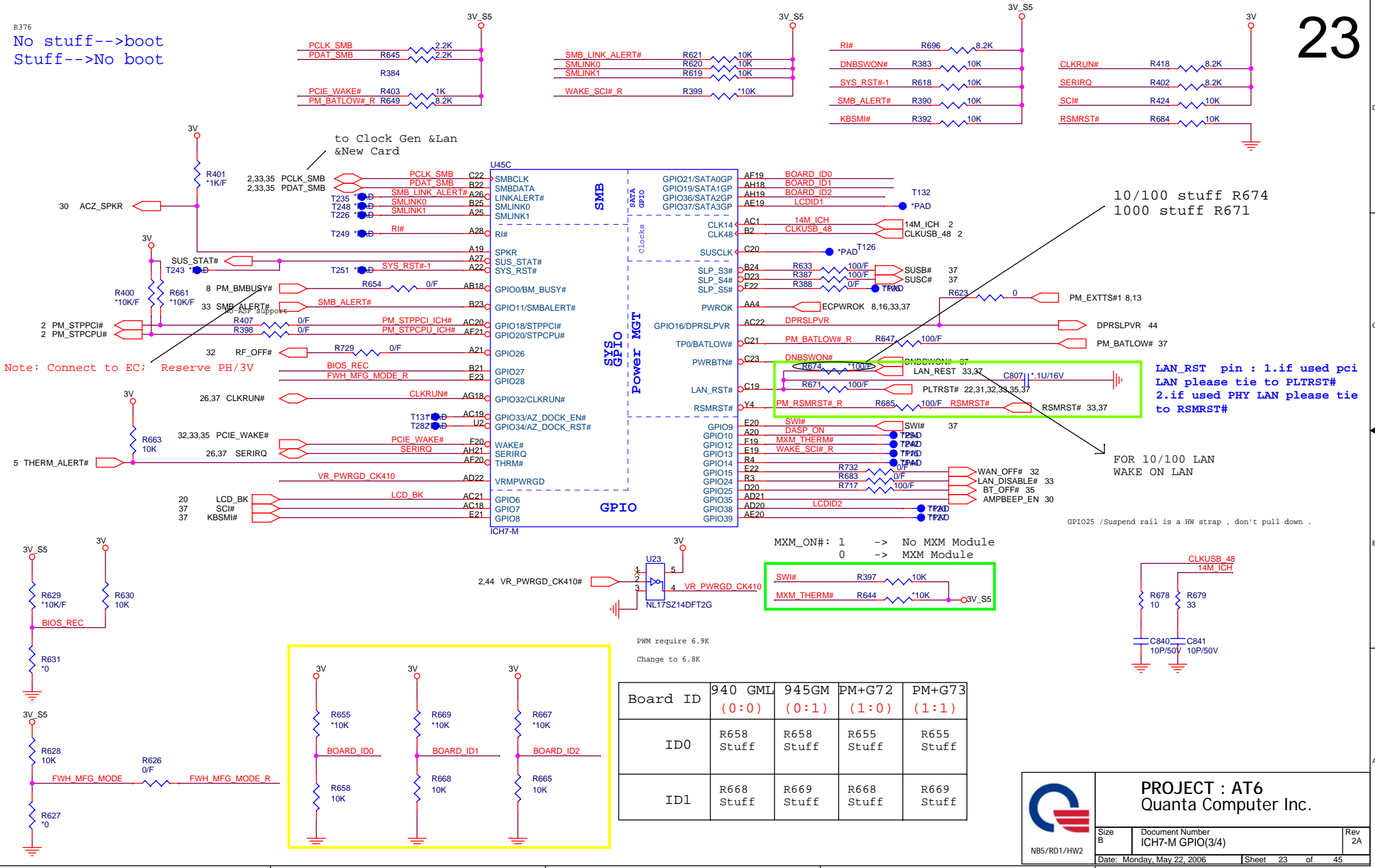
Don't connect to PCI device / Express card

**PROJECT : AT6**  
Quanta Computer Inc.

Size Custom	Document Number ICH7-M M PCI E(2/4)	Rev 1A
Date: Monday, May 22, 2006		Sheet 22 of 45

NBS/RD1/HW2

R376  
 No stuff-->boot  
 Stuff-->No boot



Note: Connect to EC; Reserve PH/3V

10/100 stuff R674  
 1000 stuff R671

LAN\_RST pin : 1.if used pci LAN please tie to PLTRST#  
 2.if used PHY LAN please tie to RSMRST#

FOR 10/100 LAN WAKE ON LAN

GPIO25 /suspend rail is a HW strap , don't pull down .

MXM\_ON#: 1 -> No MXM Module  
 0 -> MXM Module

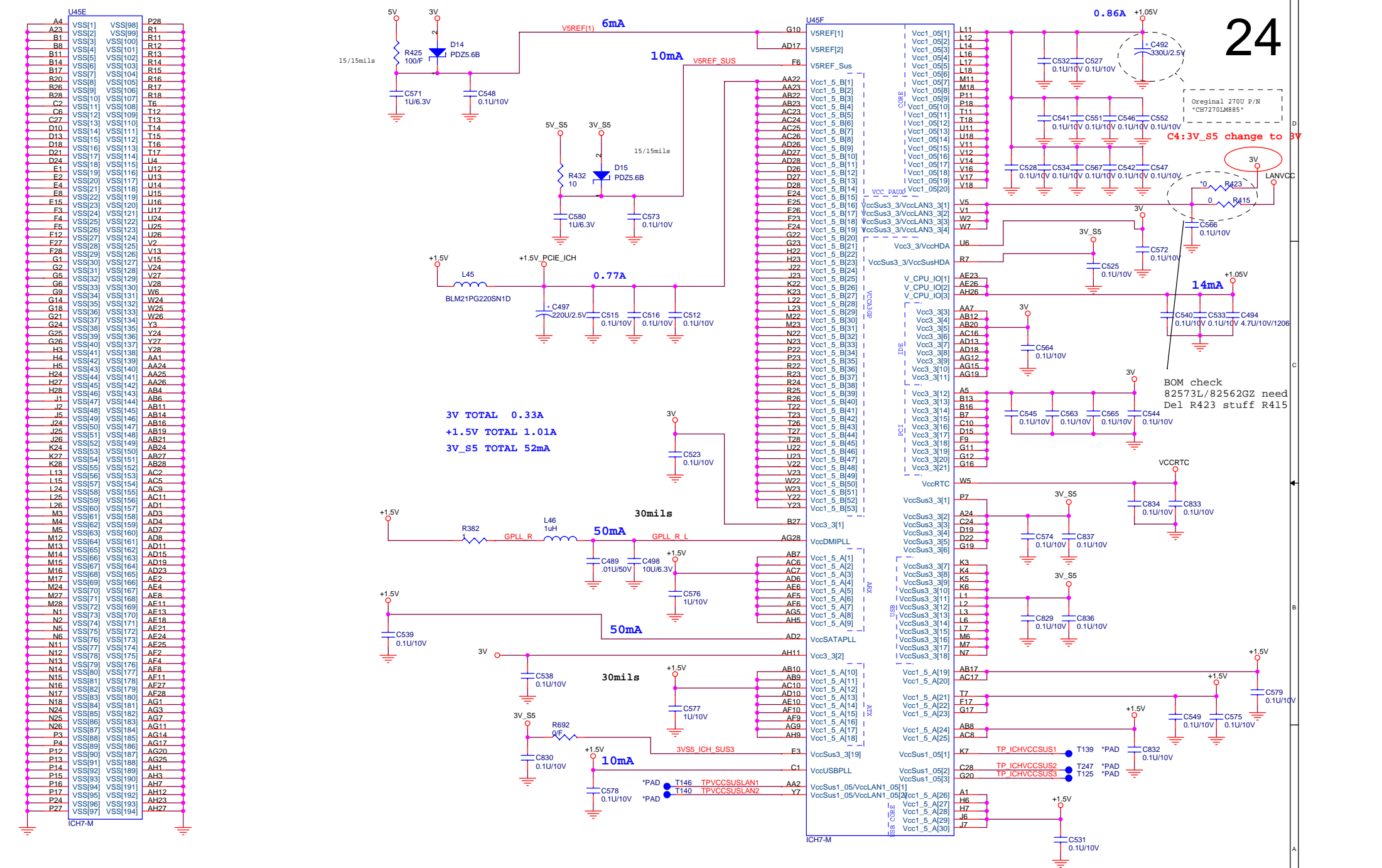
PWM require 6.9K  
 Change to 6.8K


Board ID	940 GML (0:0)	945GM (0:1)	PM+G72 (1:0)	PM+G73 (1:1)
ID0	R658 Stuff	R658 Stuff	R655 Stuff	R655 Stuff
ID1	R668 Stuff	R669 Stuff	R668 Stuff	R669 Stuff

**PROJECT : AT6**  
 Quanta Computer Inc.

Size B	Document Number ICH7-M GPIO(3/4)	Rev 2A
Date: Monday, May 22, 2006		Sheet 23 of 45

NB5/RD1/HW2

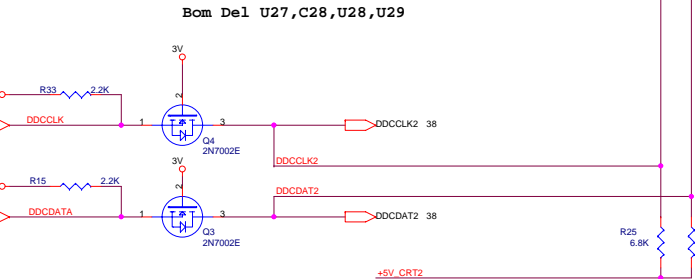
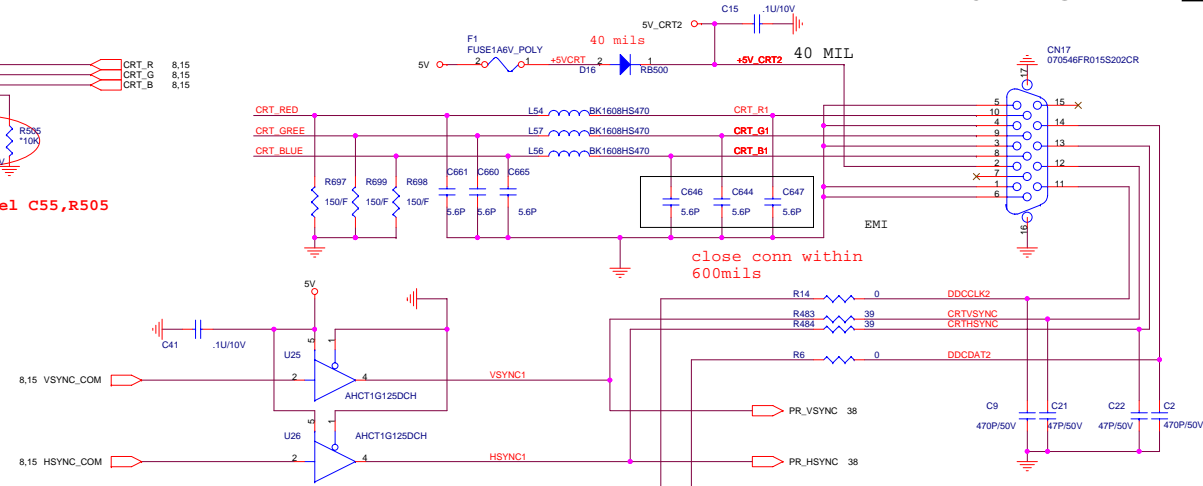
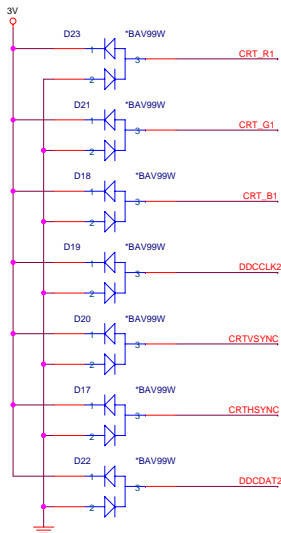
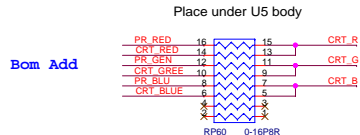
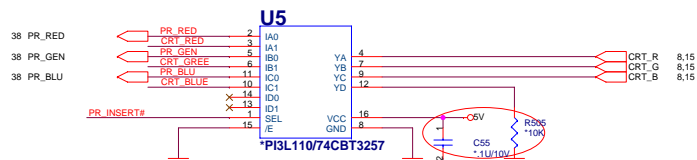


	<b>PROJECT : AT6</b> Quanta Computer Inc.	
	Size Custom Document Number ICH7-M POWER(4/4) Date: Monday, May 22, 2006	Rev 1A Sheet 24 of 45

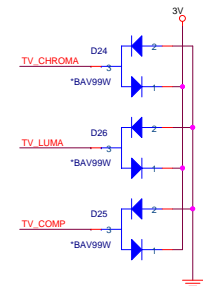
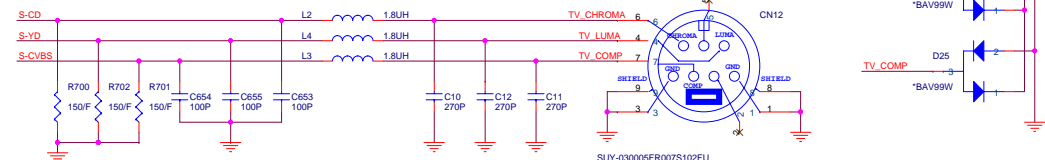
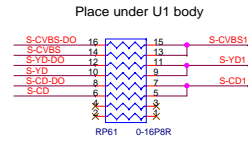
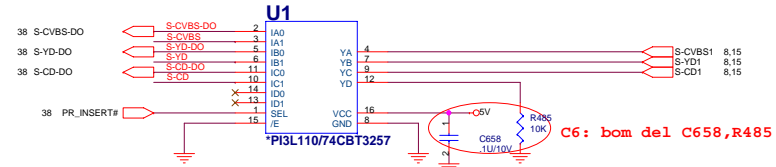


# CRT SWITCH

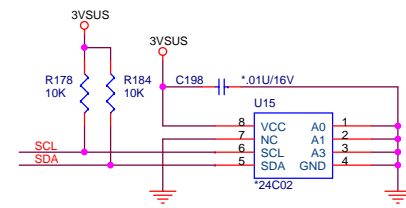
# CRT PORT 25



# TV\_SWITCH



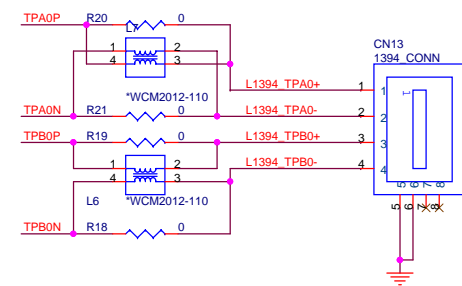
## Serial EEPROM



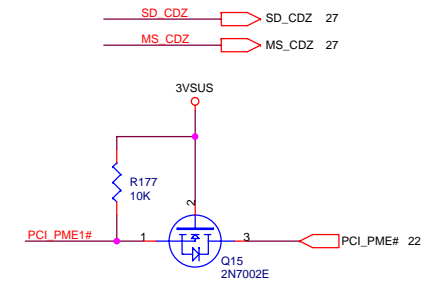
\* NOT Use EEPROM :  
R199 : installed  
R207,U15,C198 : NOT installed

\* Use EEPROM :  
R207,U15,C198 : installed  
R199 : NOT installed

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



\*TPA/TPA#,TPB/TPB# pair trace : As close as possible.  
\*TPA/TPA#,TPB/TPB# pair trace : Same length electrically And layot with shields.  
\*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

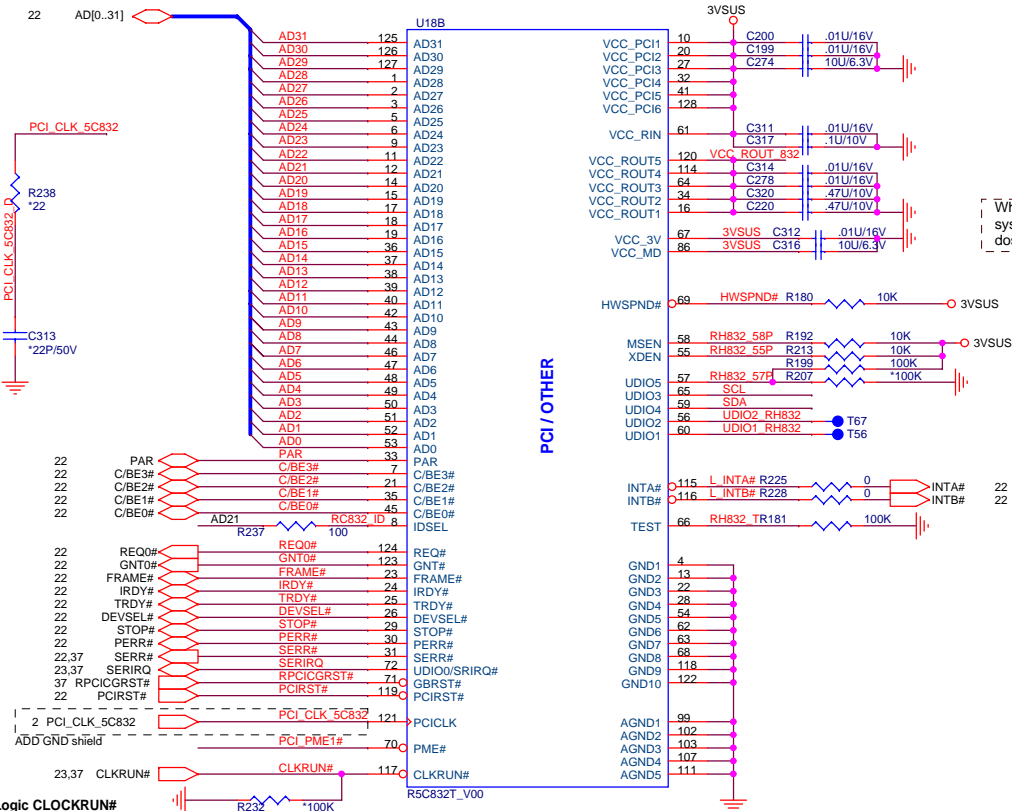


**PROJECT : AT6**  
**Quanta Computer Inc.**

Size Custom	Document Number RICOH832 Controller	Rev 2A
Date: Monday, May 22, 2006		Sheet 26 of 45

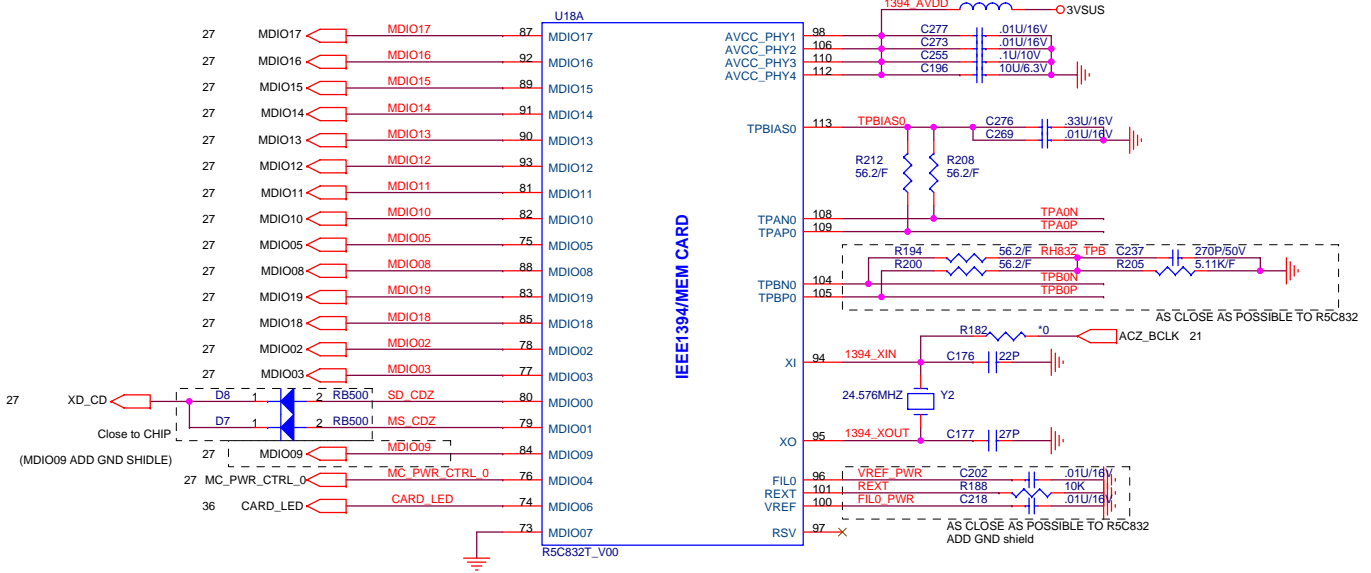
When HWS/PND# is controlled by system, the pull-up resistor(R2) dose not need to apply.

## PCI / OTHER



**CoreLogic CLOCKRUN#**  
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.

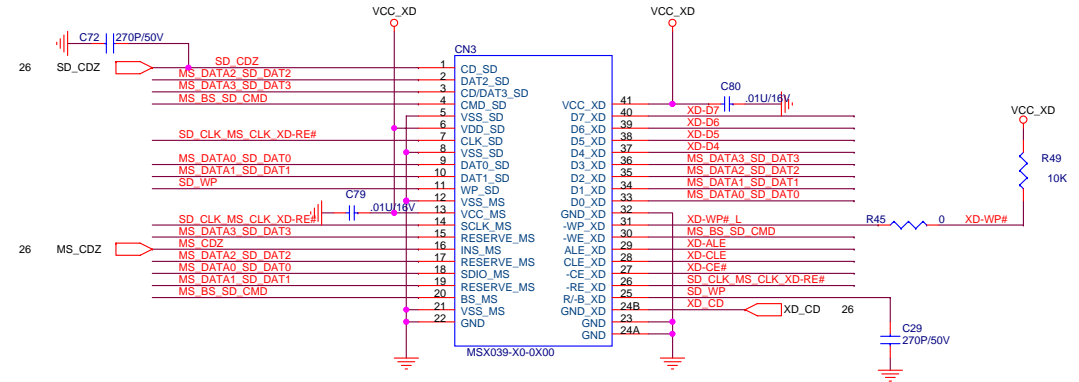
## IEEE1394/MEM CARD



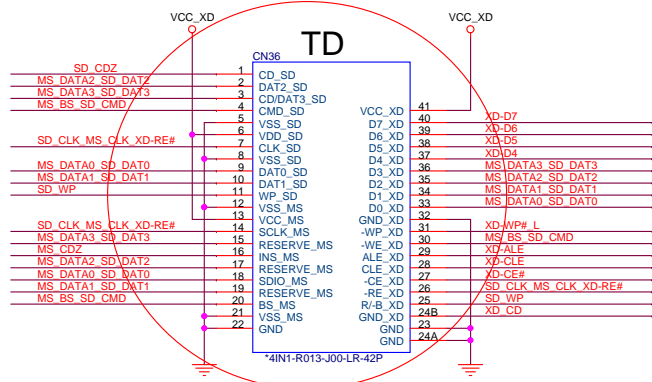
Close to CHIP

AS CLOSE AS POSSIBLE TO R5C832 ADD GND shield

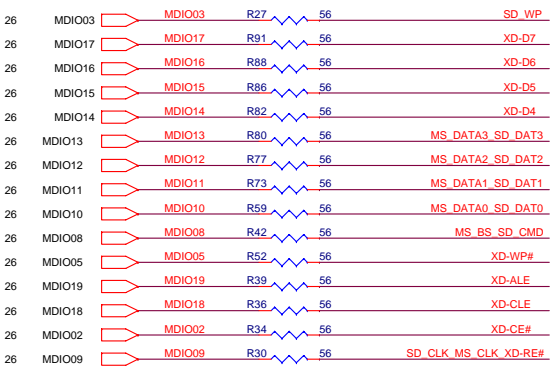
### 4 IN1 CARD READER XD,MMC/SD,MS/MSP



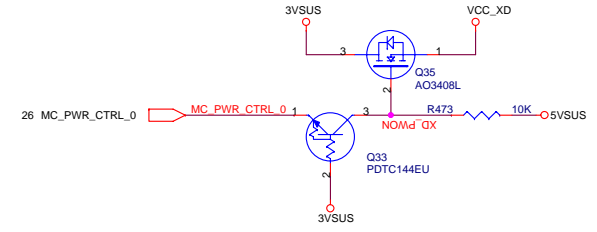
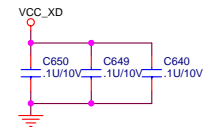
C7: change CN36 footprint



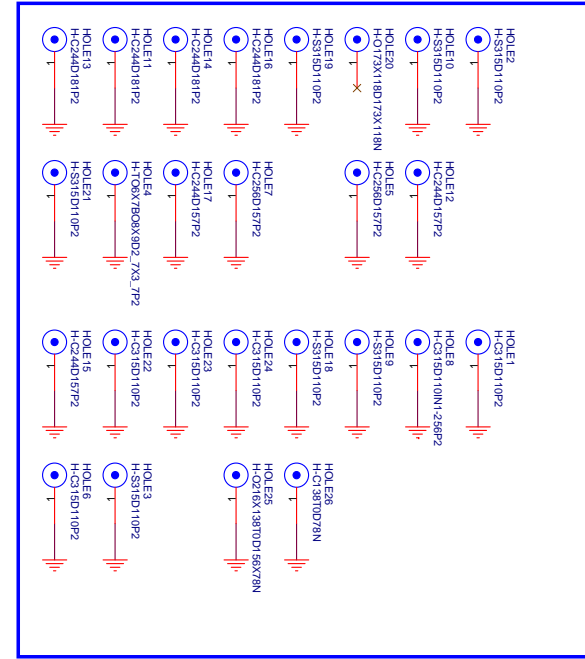
bom create 2'nd source



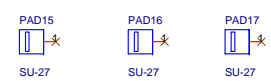
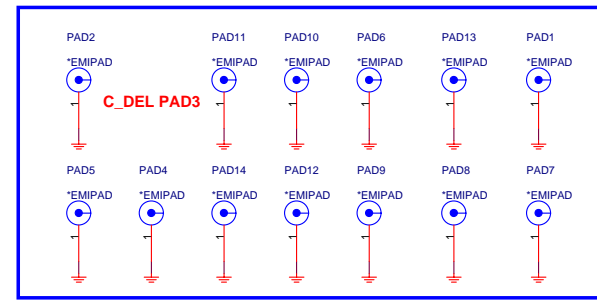
C\_Delete reserve circuit for card reader power.



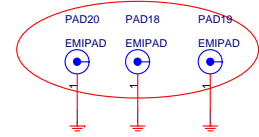
### SCREW HOLE



### EMI PAD



moden cable sprig

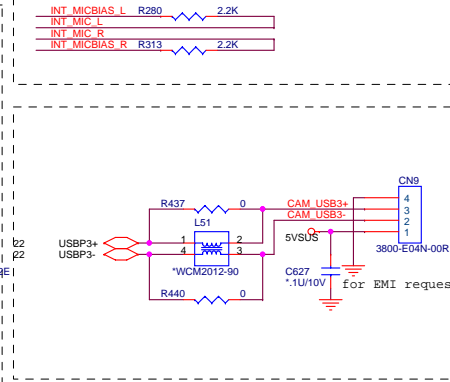
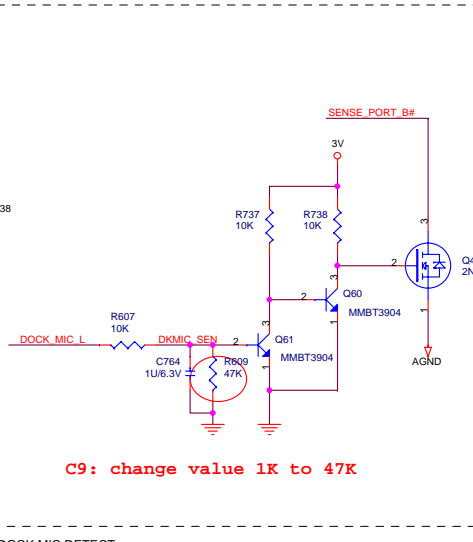
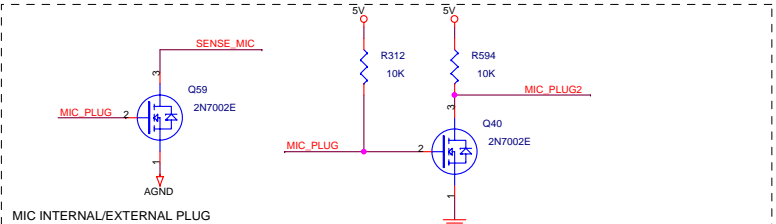
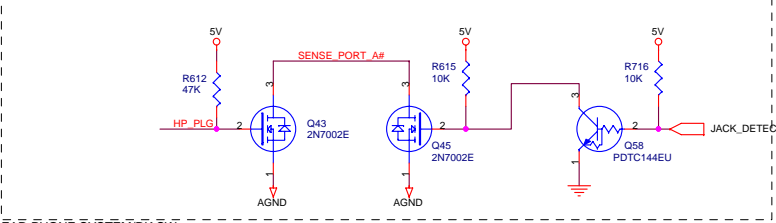
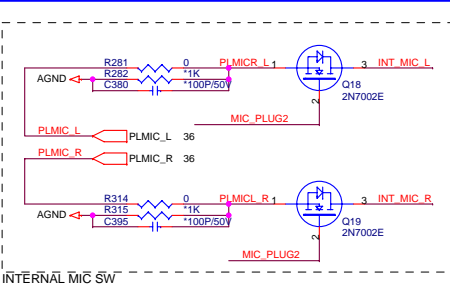
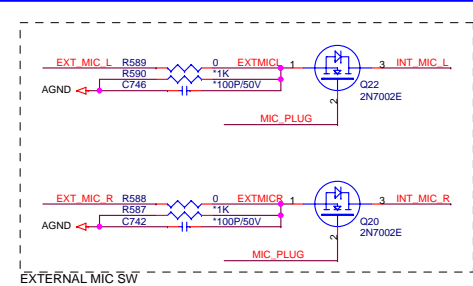
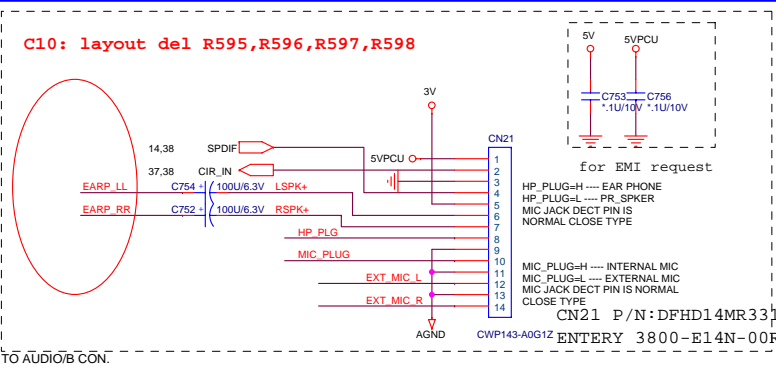
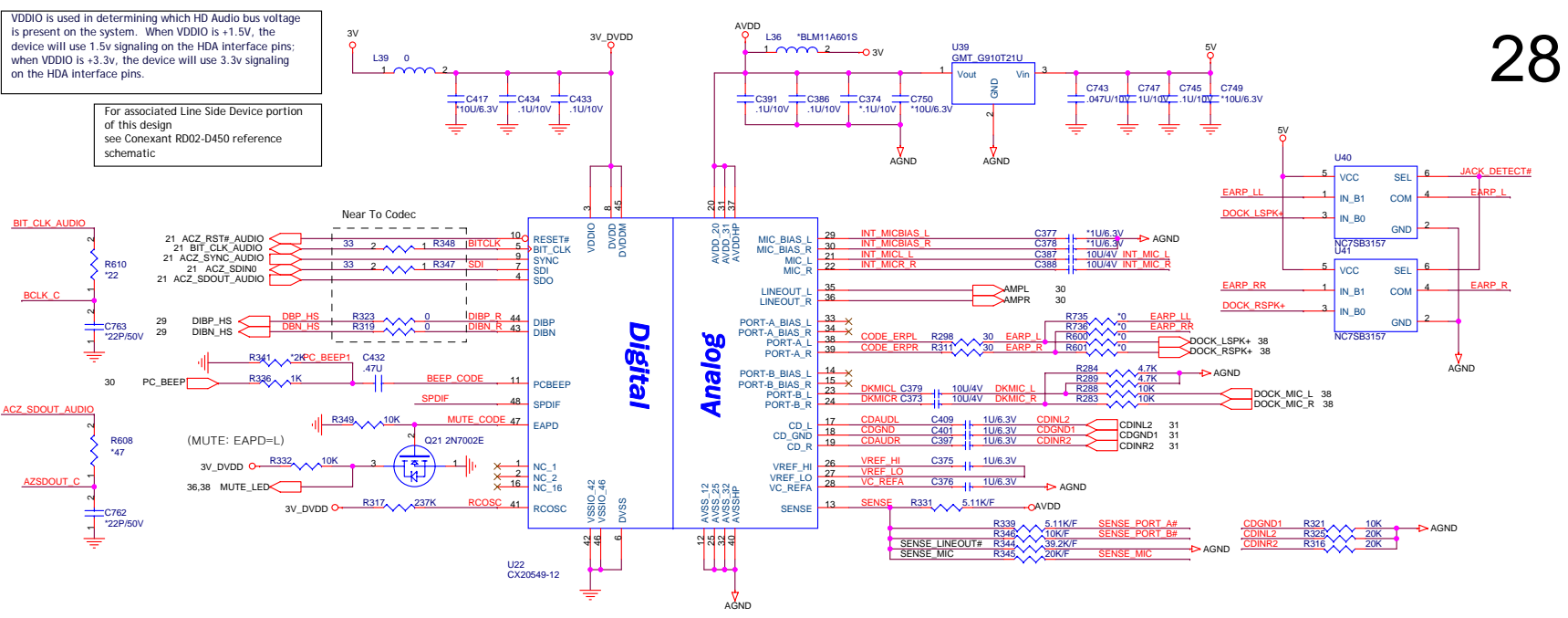


C8: Add lock bluetooths cable sprig

	PROJECT : AT6 Quanta Computer Inc.	
	Size Custom	Document Number CARD READER/HOLE
NBS/RD1/HW2	Date: Monday, May 22, 2006	Rev 1A
	Sheet 27 of 45	

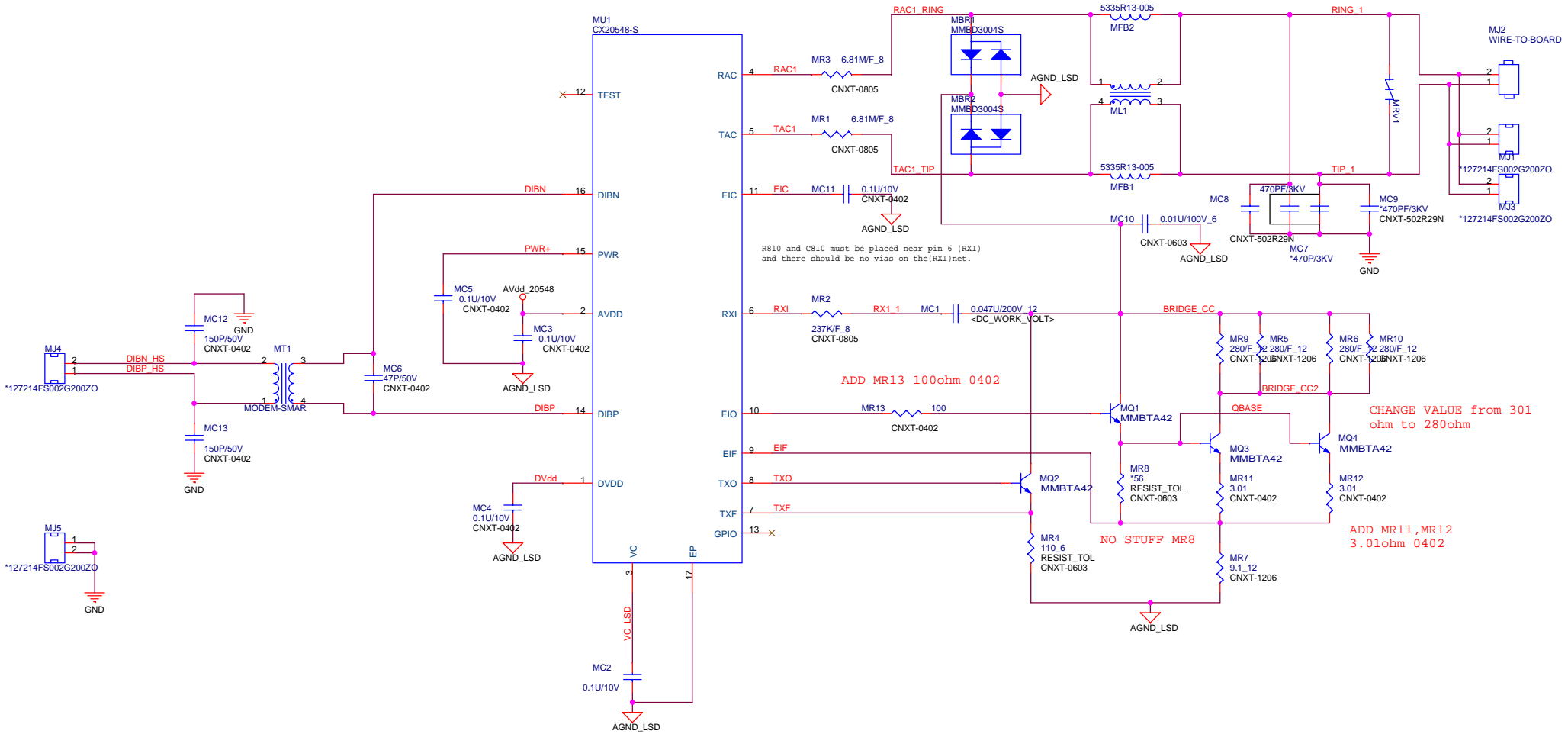
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

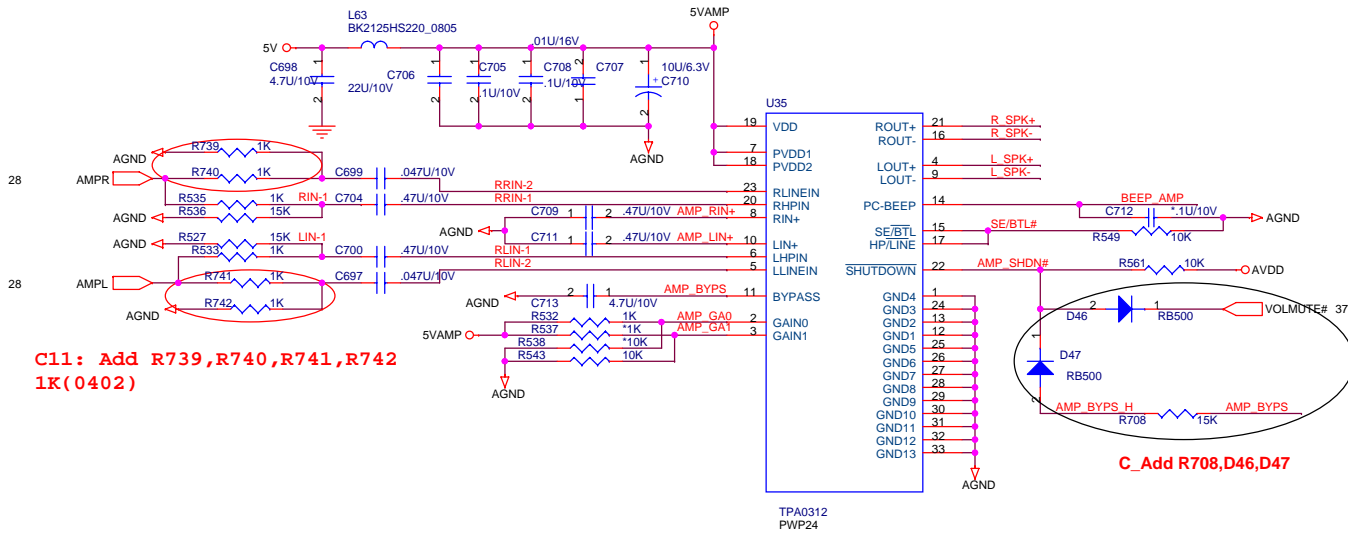


Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

28 DIBN\_HS DIBN\_HS  
 28 DIBP\_HS DIBP\_HS



<p>NB5/RD1/HW2</p>	<p><b>PROJECT : AT6</b>                  Quanta Computer Inc.</p>		
	<p>Size                  Custom</p>	<p>Document Number                  MODEM(DAA)</p>	<p>Rev                  1A</p>
	<p>Date: Monday, May 22, 2006</p>		<p>Sheet 29 of 45</p>

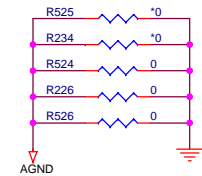


**C11: Add R739,R740,R741,R742 1K(0402)**

**C\_Add R708,D46,D47**

### 0312 Gain Table

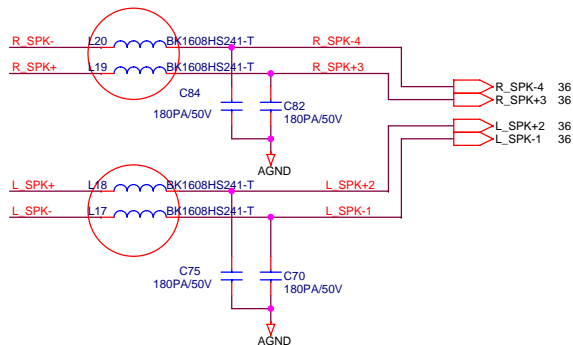
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



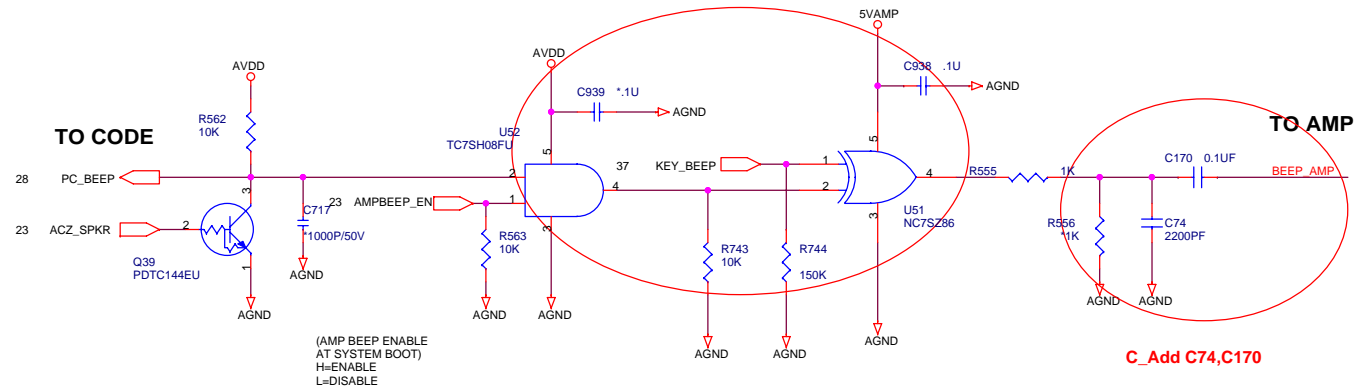
### INT. SPEAKER

### PCSPK BEEP

**C12: change L17,L18,L19,L20 value to 240 Ohm**



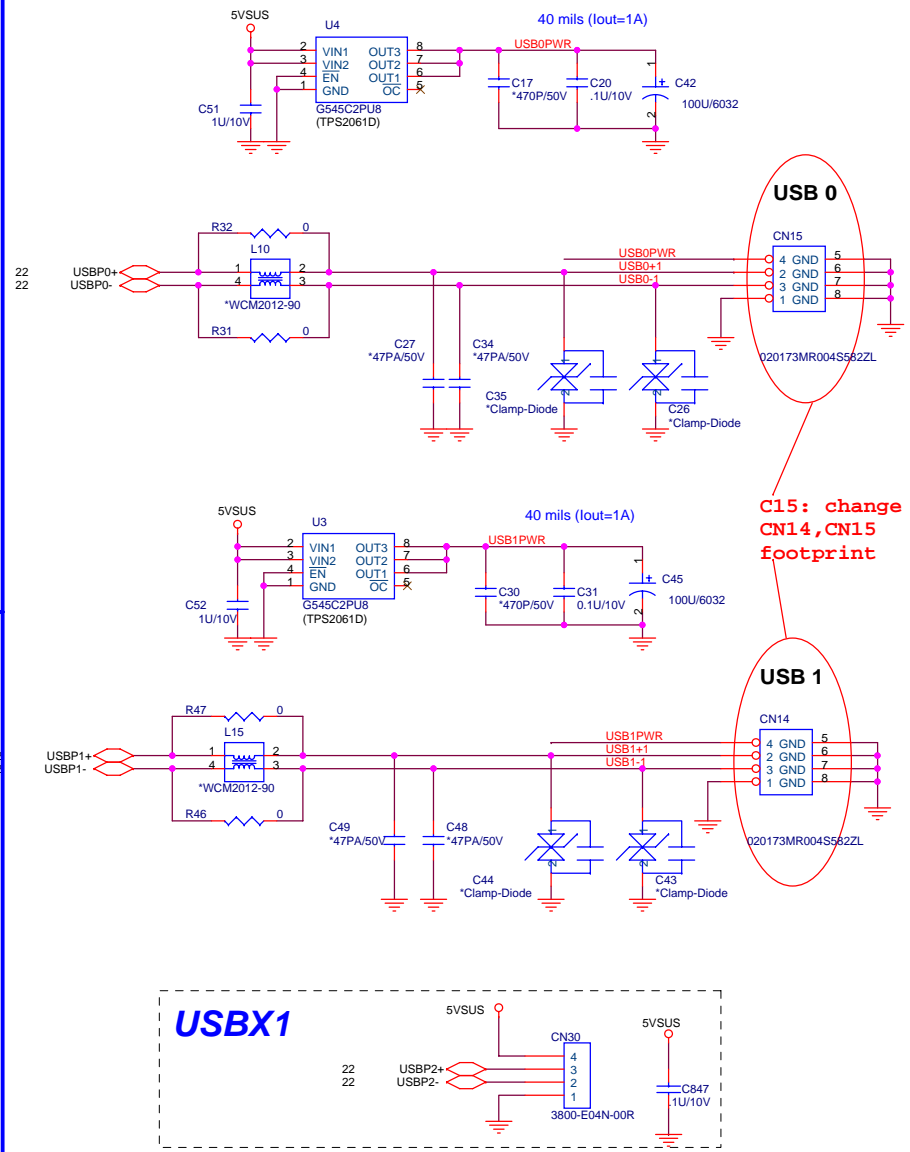
**C13: Del Q57,R715,R554,C714 Add C938,U51,R774,R743,U52,C939,R563**



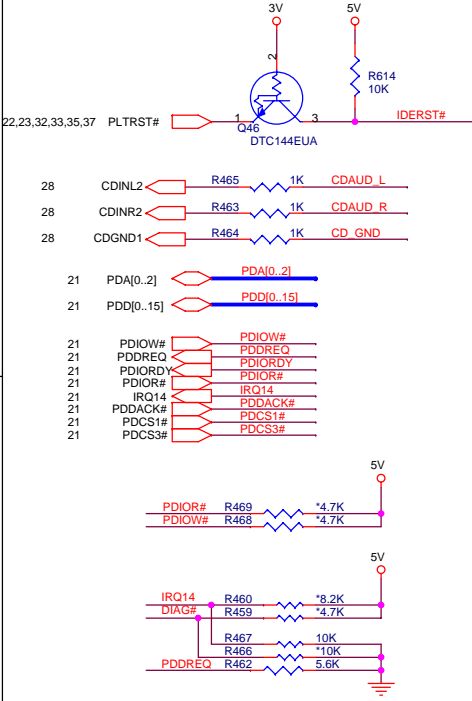
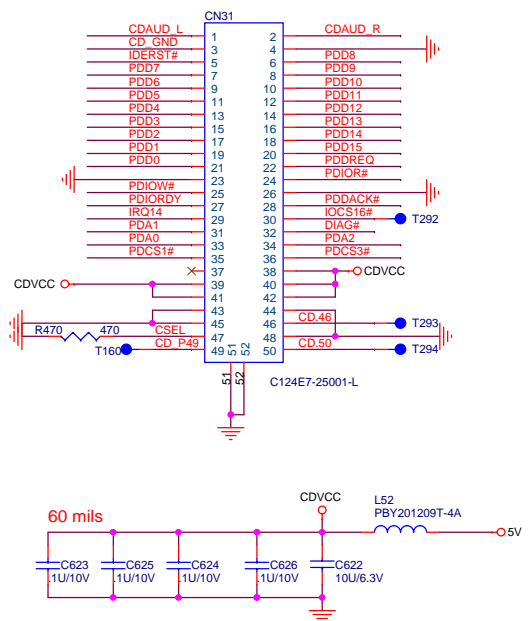
**C\_Add C74,C170**

	PROJECT : AT6	
	Quanta Computer Inc.	
	Size Custom	Document Number JACK/AMP_TAP0312
Date: Monday, May 22, 2006		Sheet 30 of 45

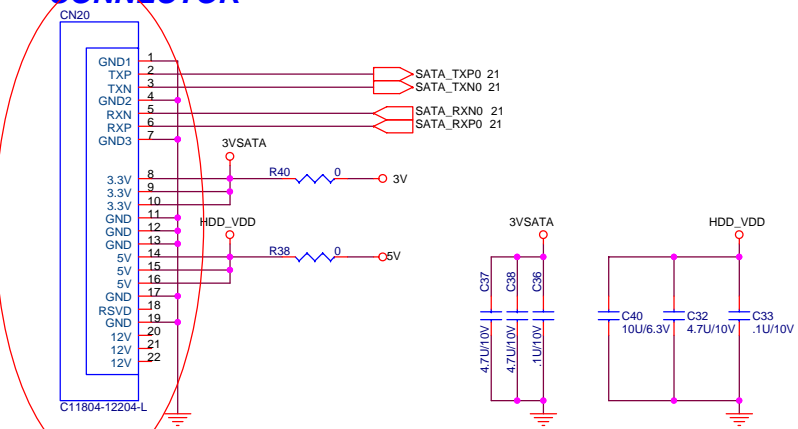
## USBX2



## CD-ROM

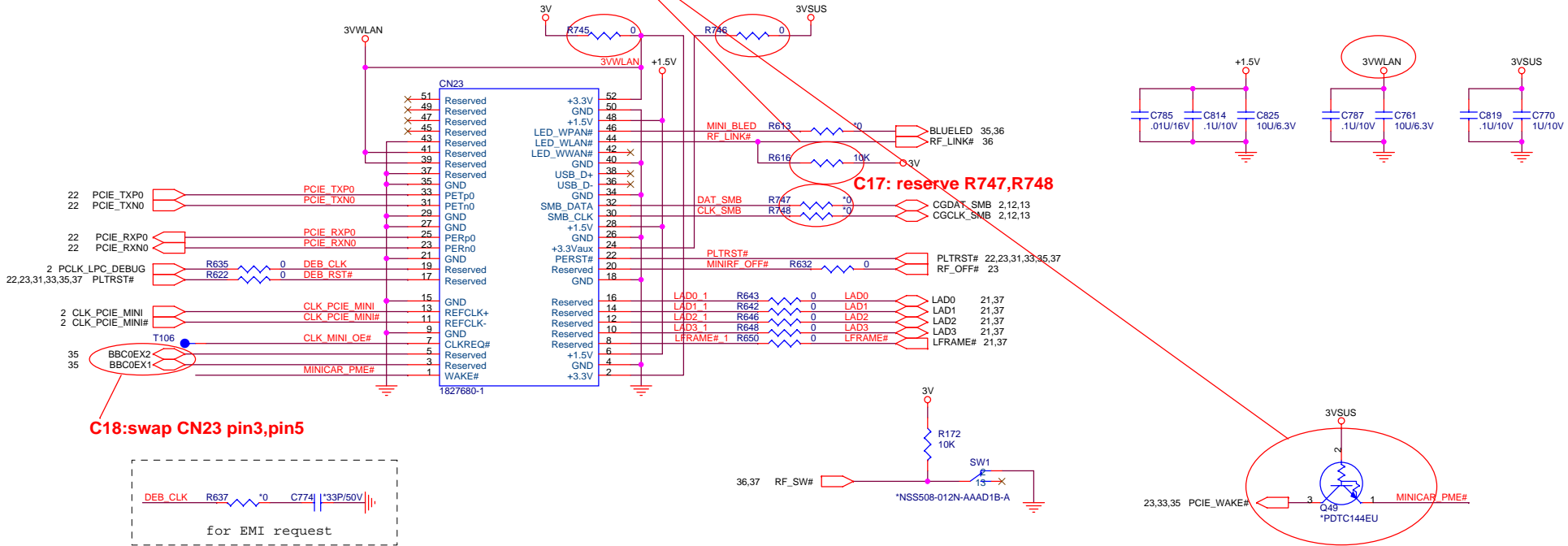


## SATA\_1 CONNECTOR



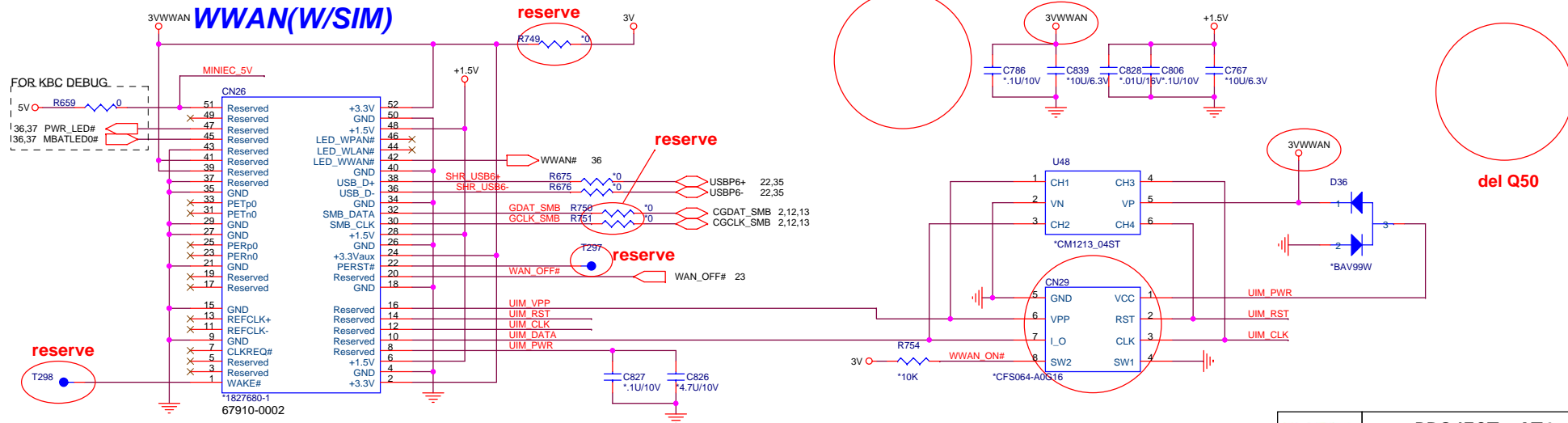
# Mini PCI-E Card 1 WLAN

C16: Add Bom R745(RC1206) R746(RC0603) and R616  
Del Q49



# Mini PCI-E Card 2 WWAN(W/SIM)

del C771,C822

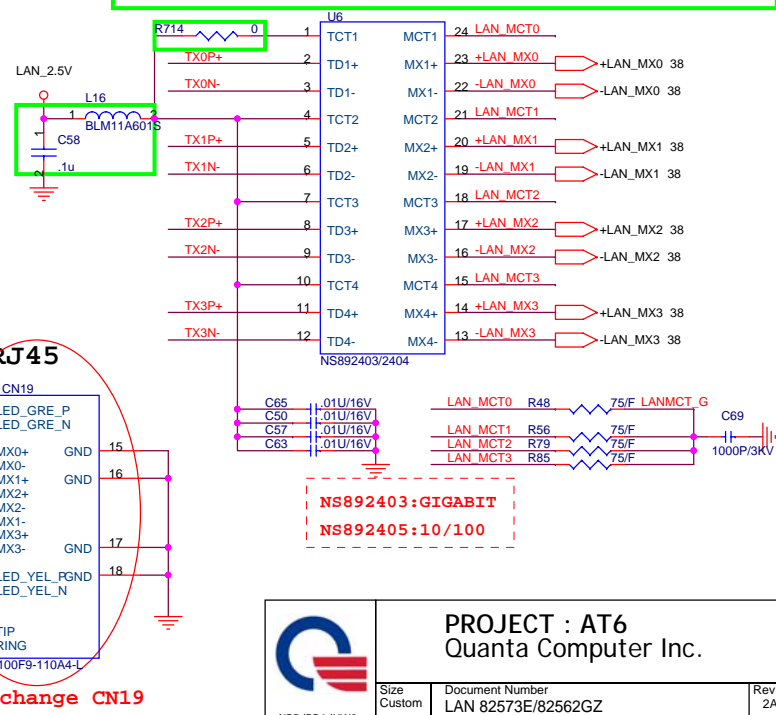
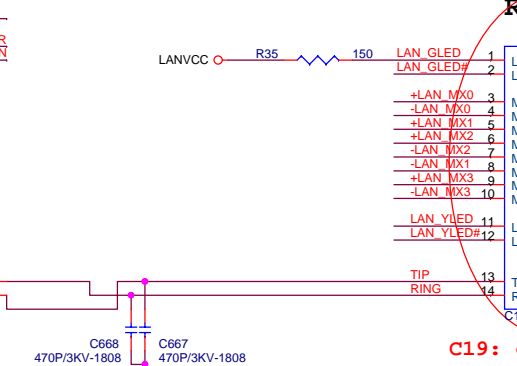
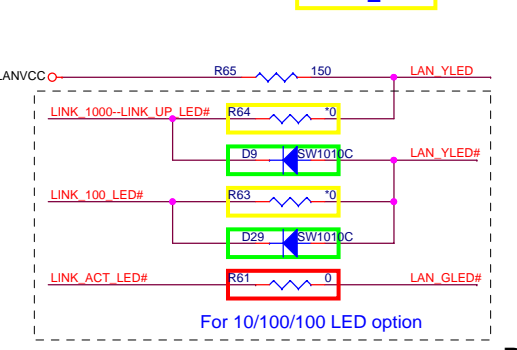
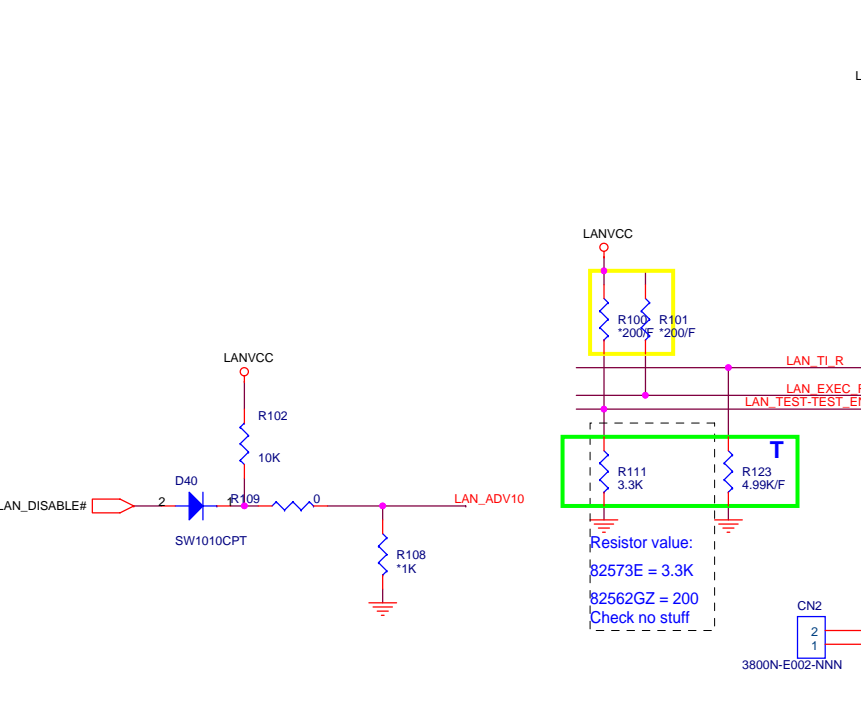
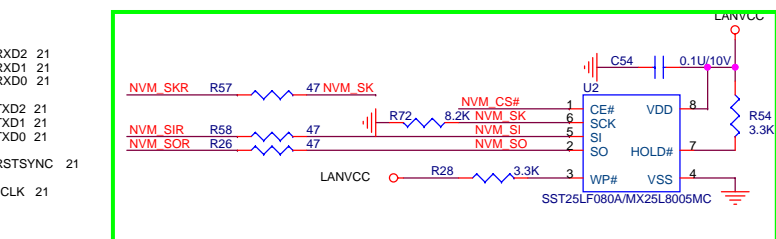
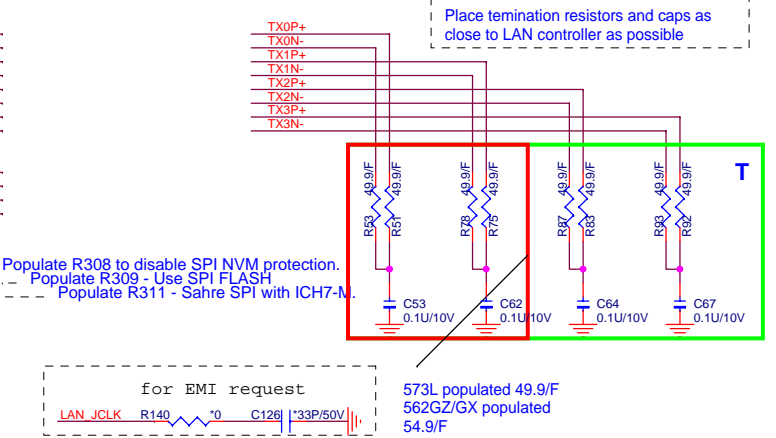
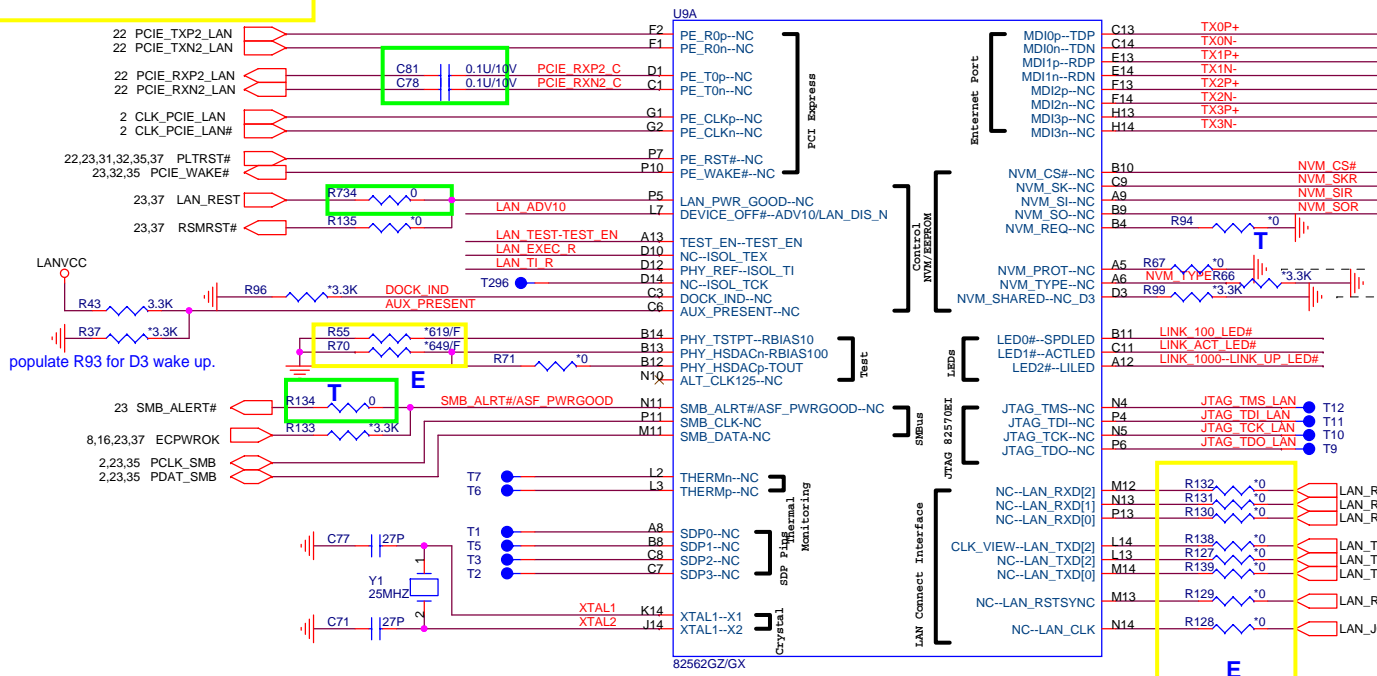


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	Size Custom	Document Number MINI CARD X2
Date: Monday, May 22, 2006		Rev 1A
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T : Stuffed for 82573L(10/100/1000)

E : Stuffed for 82562GZ/GX(10/100)



C19: change CN19 footprint

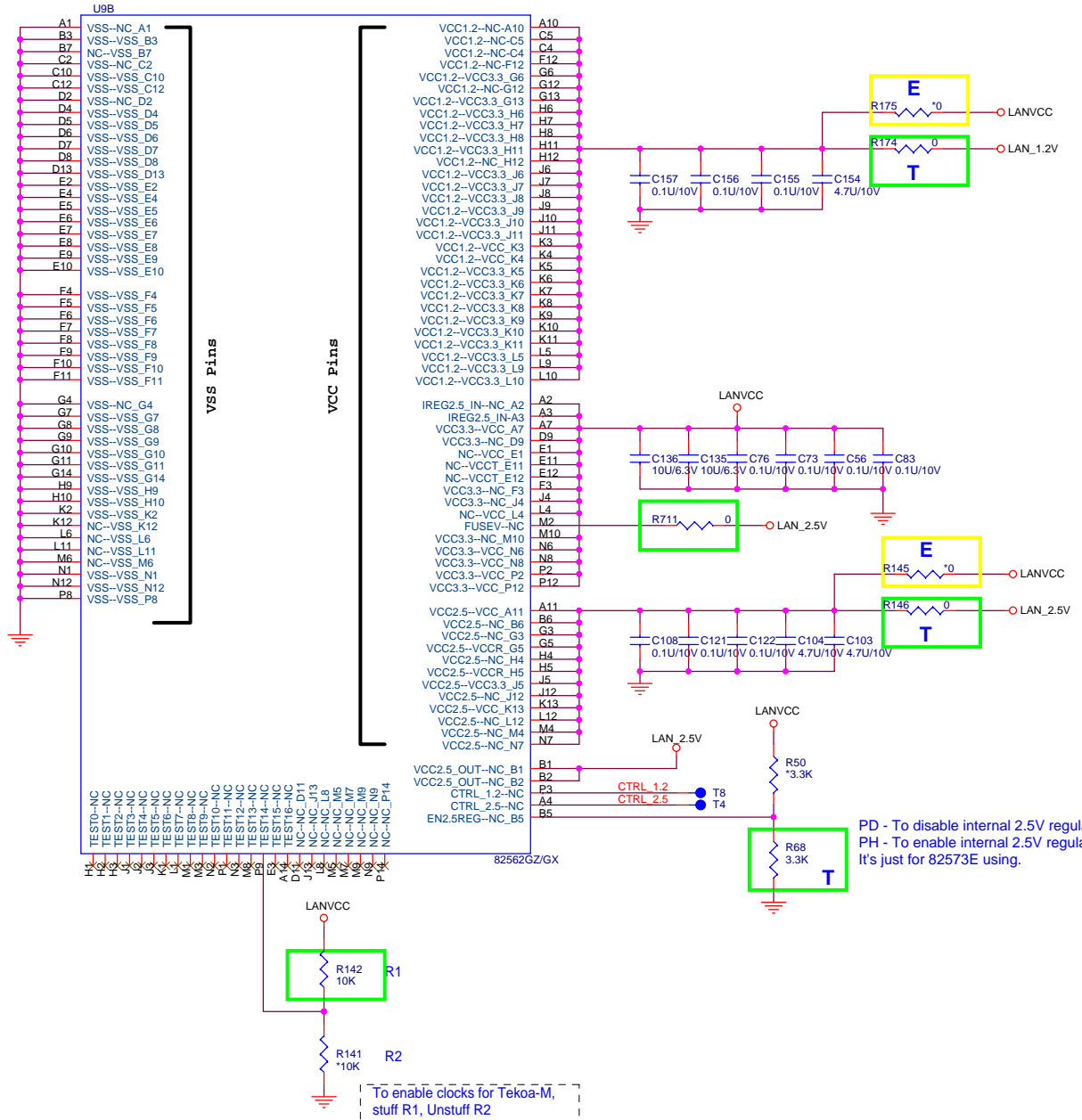
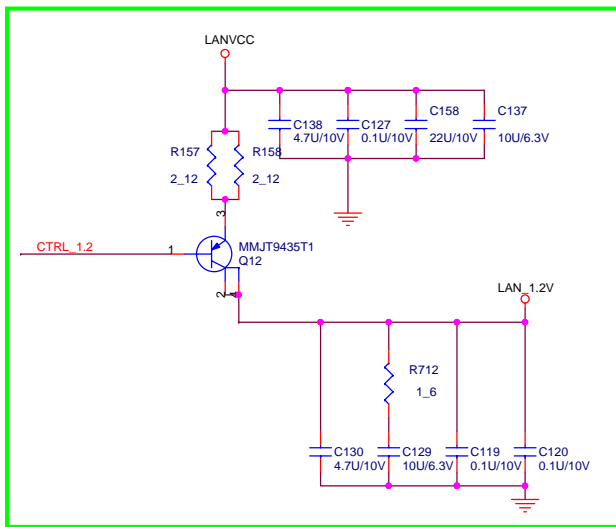
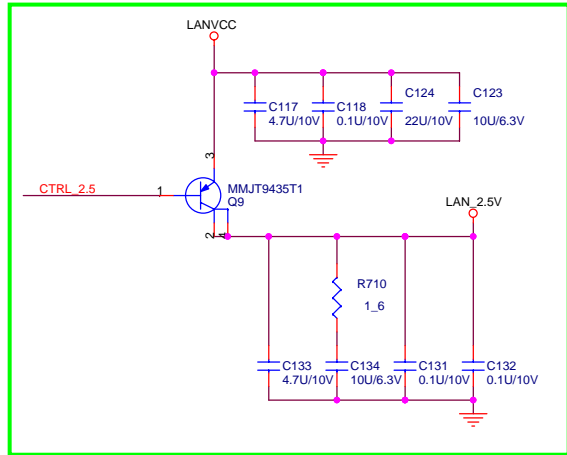
**PROJECT : AT6**  
Quanta Computer Inc.

Size Custom Document Number LAN 82573E/82562GZ Rev 2A

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T : Stuffed for 82573L(10/100/1000)

E : Stuffed for 82856GZ/GX(10/100)

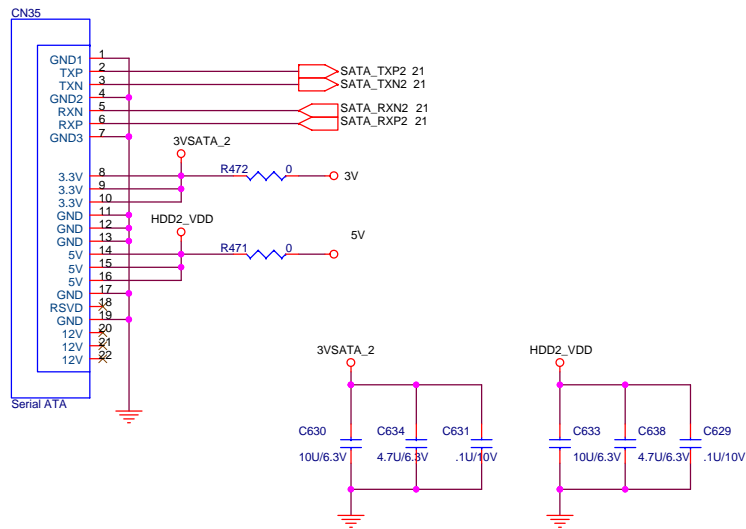


PD - To disable internal 2.5V regulator.  
PH - To enable internal 2.5V regulator.  
It's just for 82573E using.

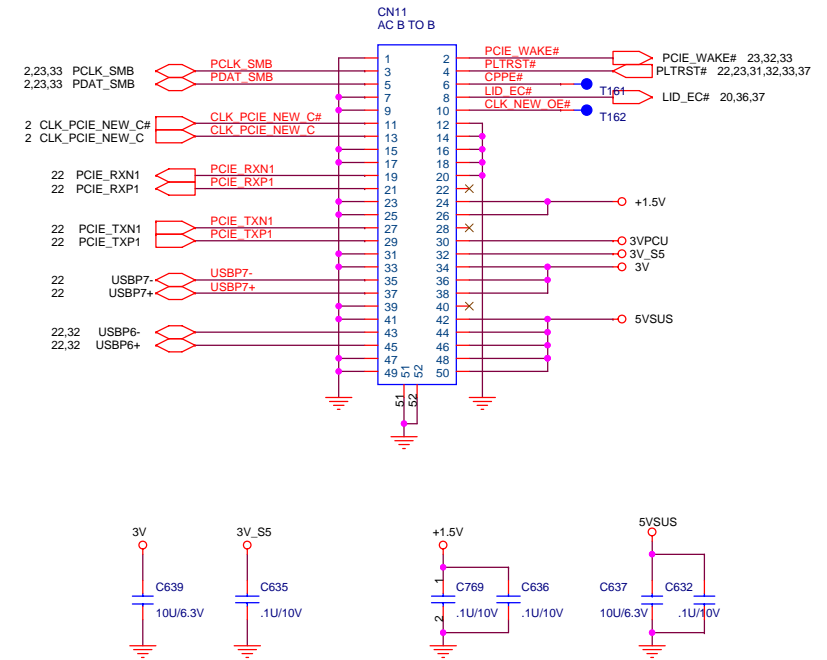
To enable clocks for Tekoa-M,  
stuff R1, Unstuff R2

# SATA\_2 CONNECTOR

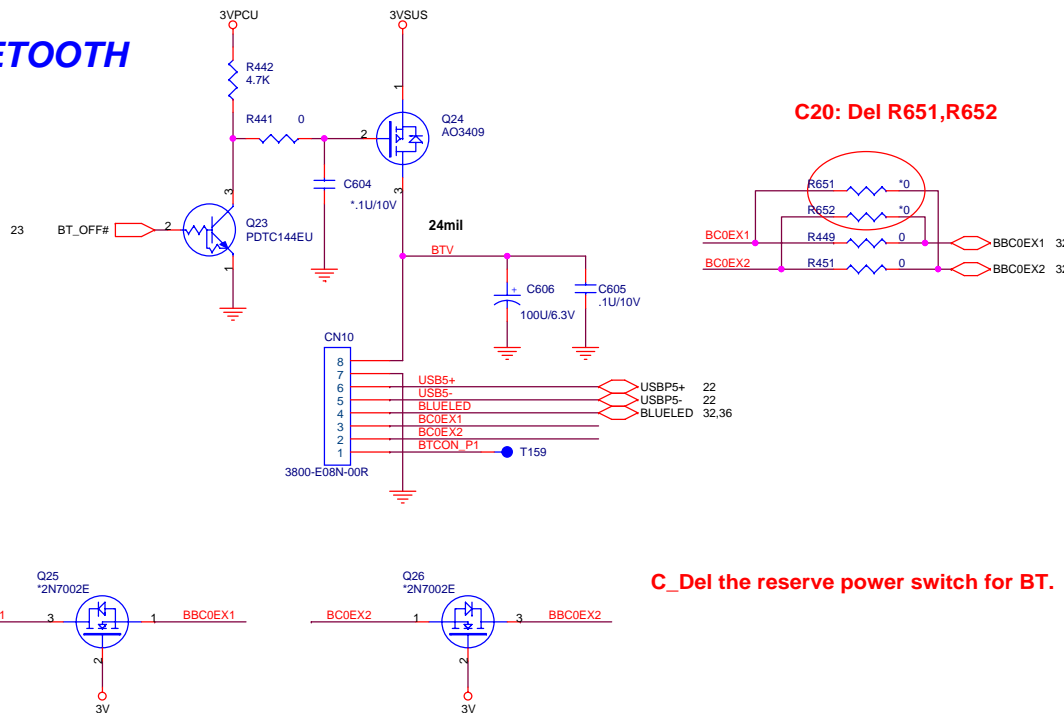
For 17"W Second HDD

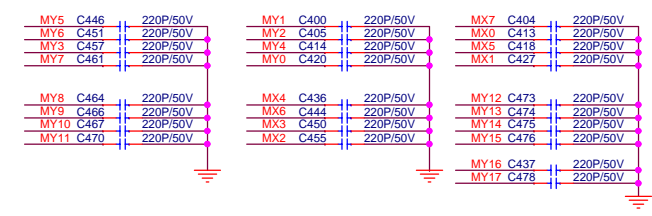
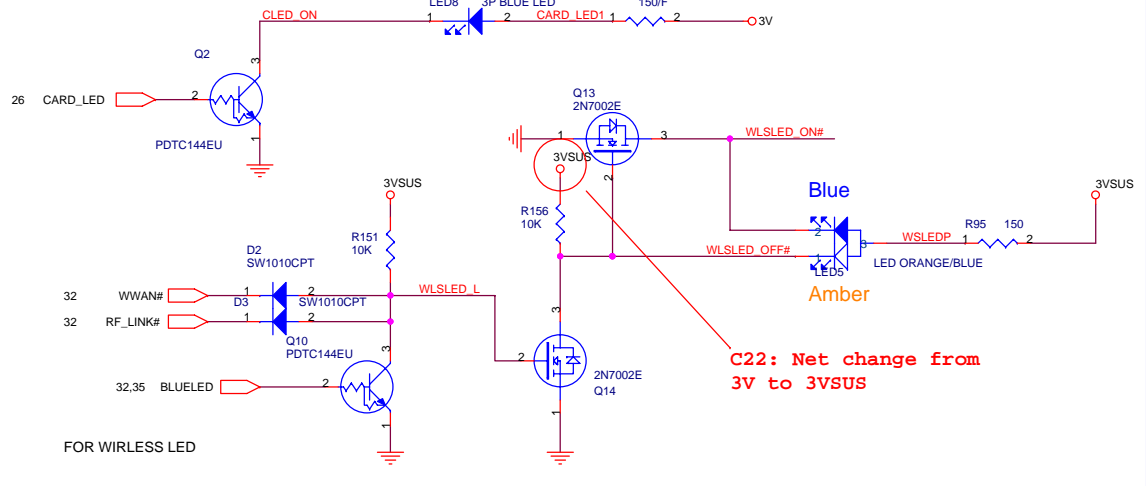
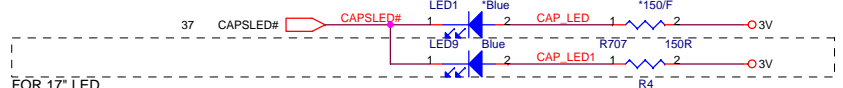
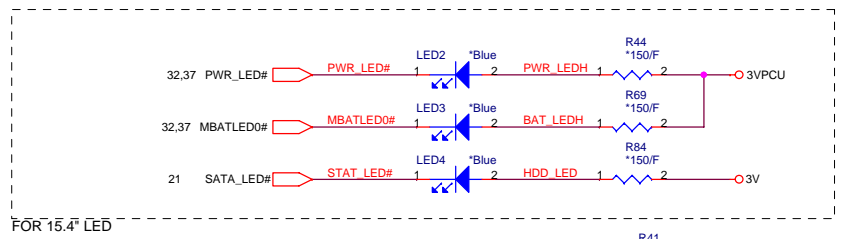
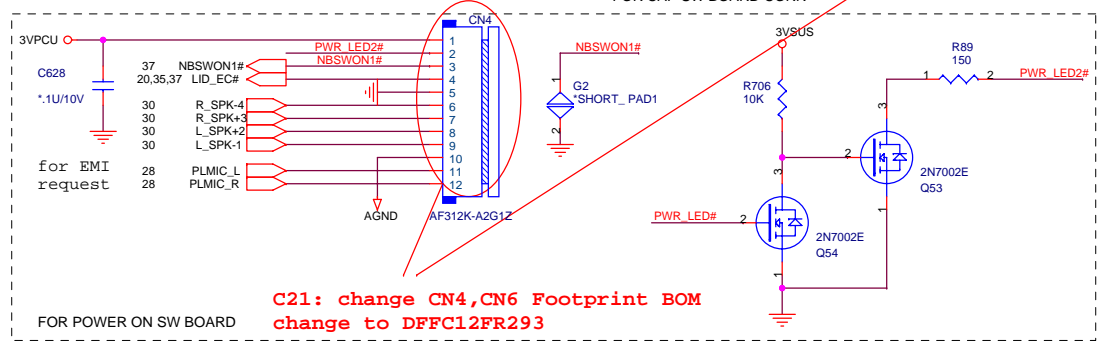
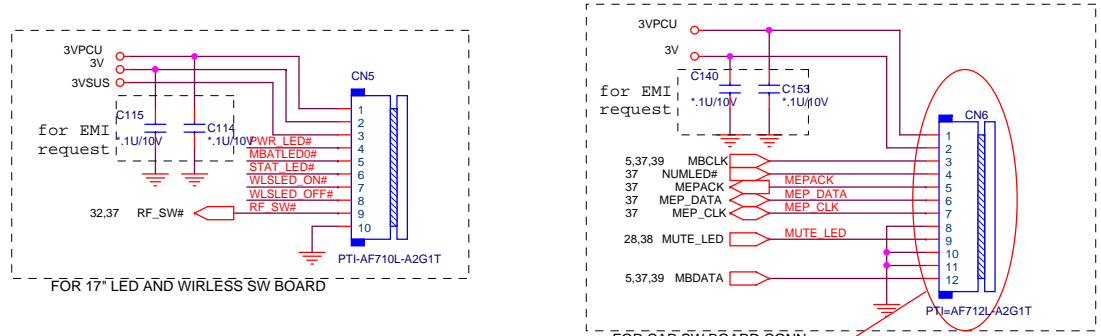


# NEWCARD

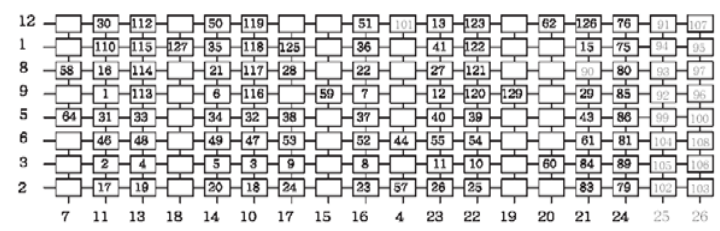
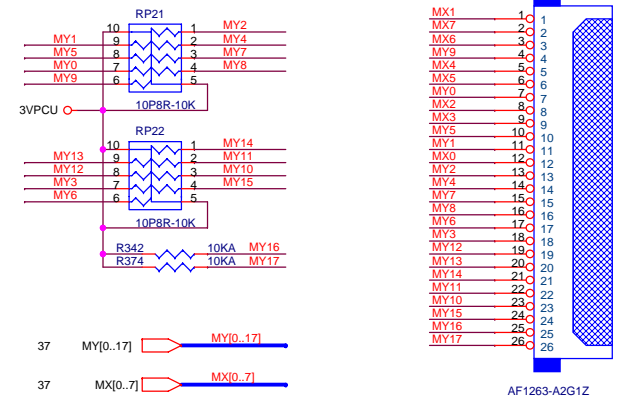


# BLUETOOTH





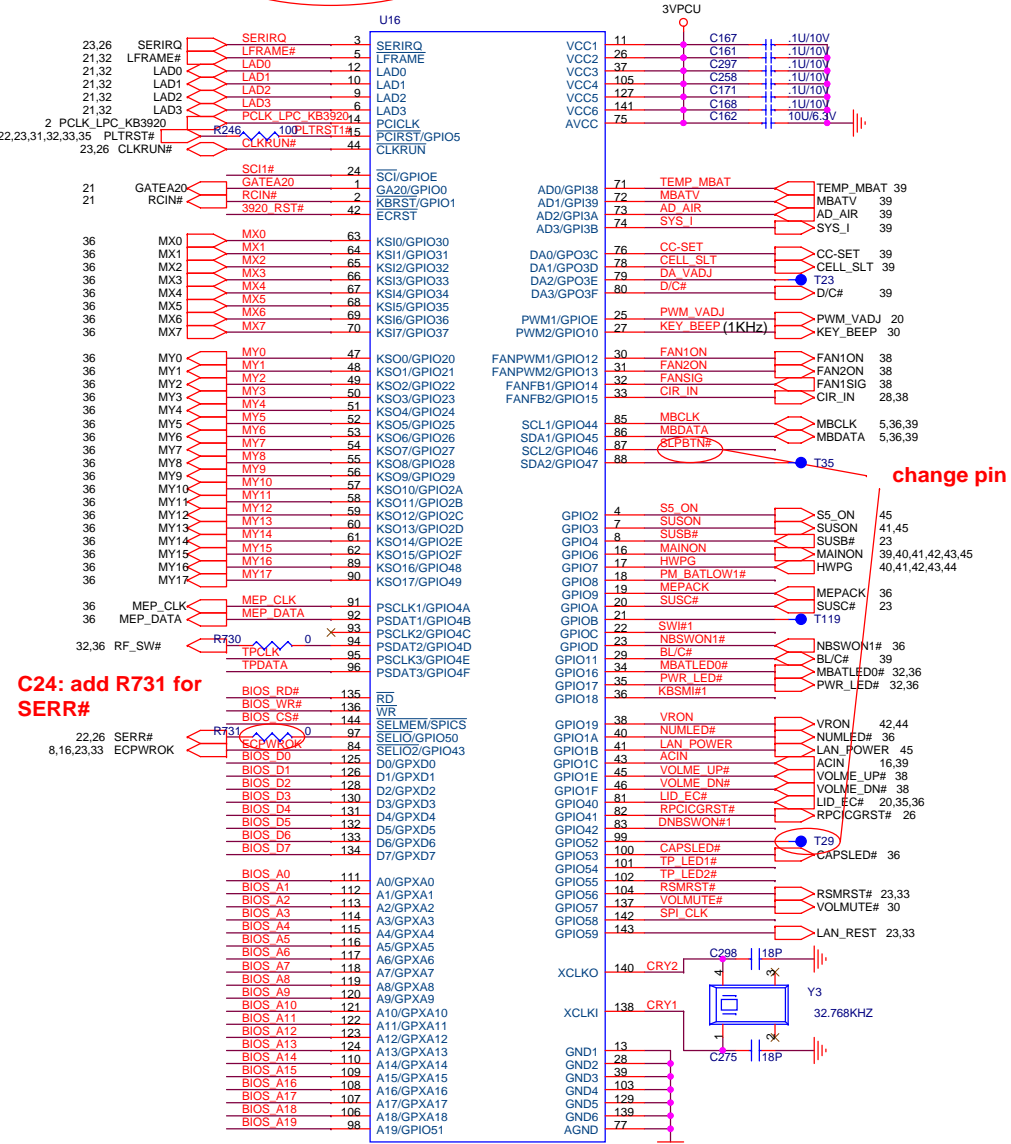
## KEYBOARD PULL-UP



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	Quanta Computer Inc.	
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**C23: SLP\_BTN# change to DNBSWON# Add R753**

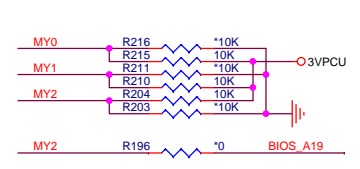


**C24: add R731 for SERR#**

22.26 SERR#  
8.16,23.33 ECPWROK

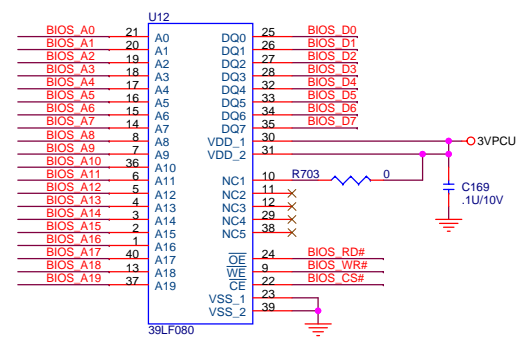
**STRAP PIN**

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 32kHz clock in normal running
MY1	48	TP_PLL: DLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



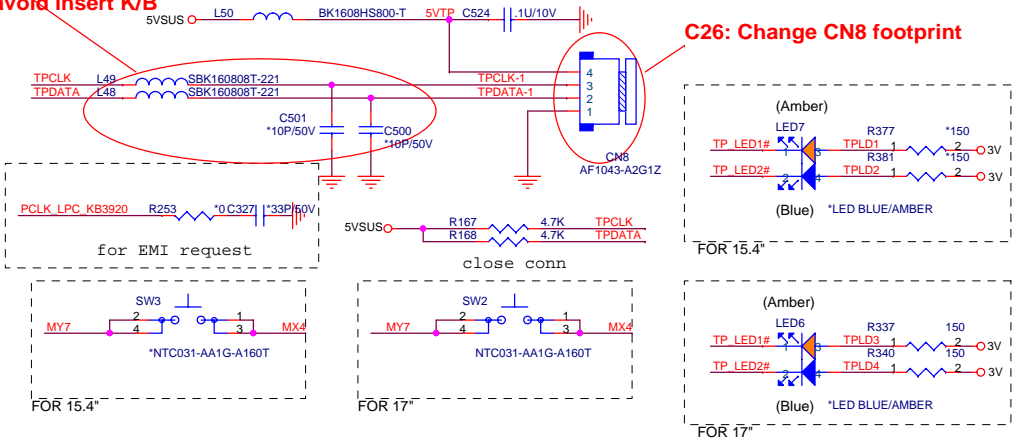
37

**BIOS 1M FLASH ROM**

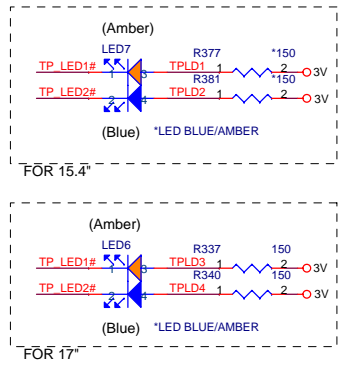


**C25: layout Move L48,L49,C500,C501 in order to avoid insert K/B**

**TOUCH PAD CONNECTOR**



**C26: Change CN8 footprint**

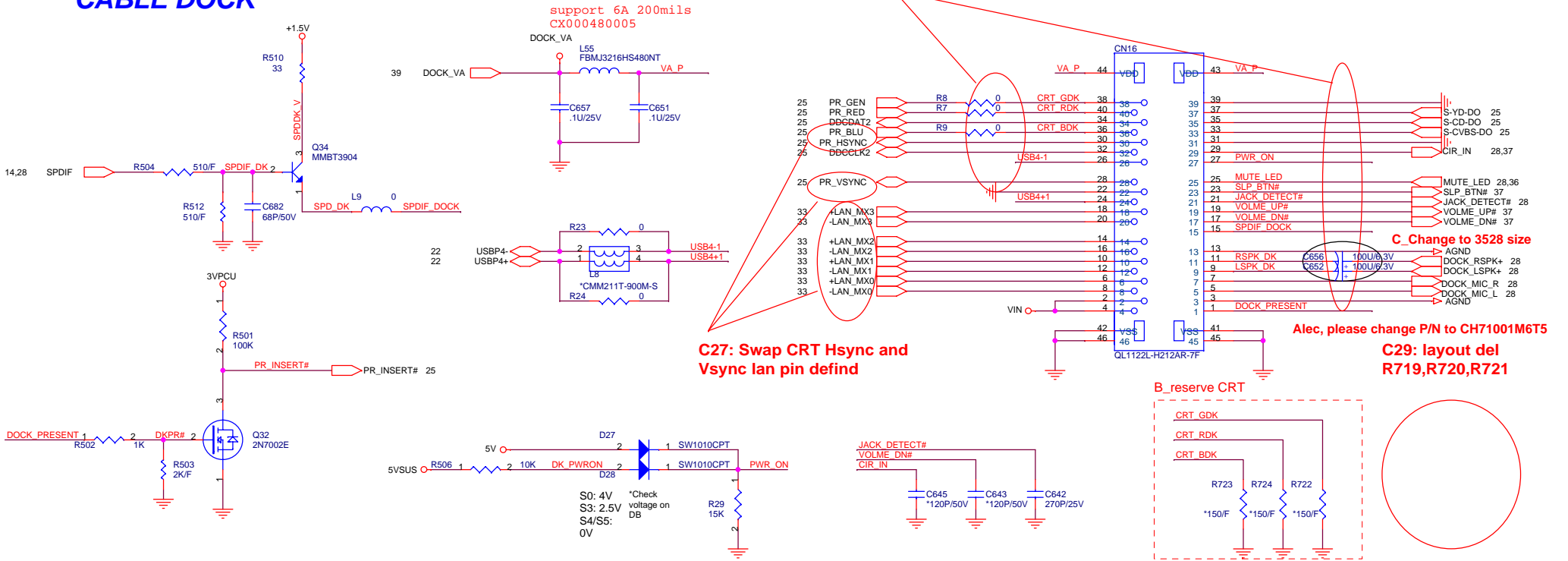


**PROJECT : AT6**  
Quanta Computer Inc.

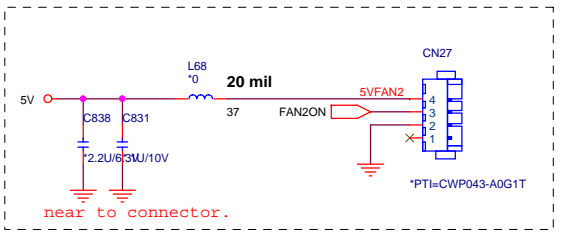
Size Custom	Document Number KB3920/ROM/TP	Rev 2A
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C28: Del R1,R2,R3,R5,R477,R478,R479,R480,R476,R12,R475,R474,R22

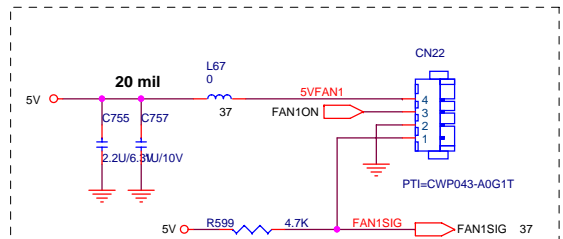
CABLE DOCK



FAN

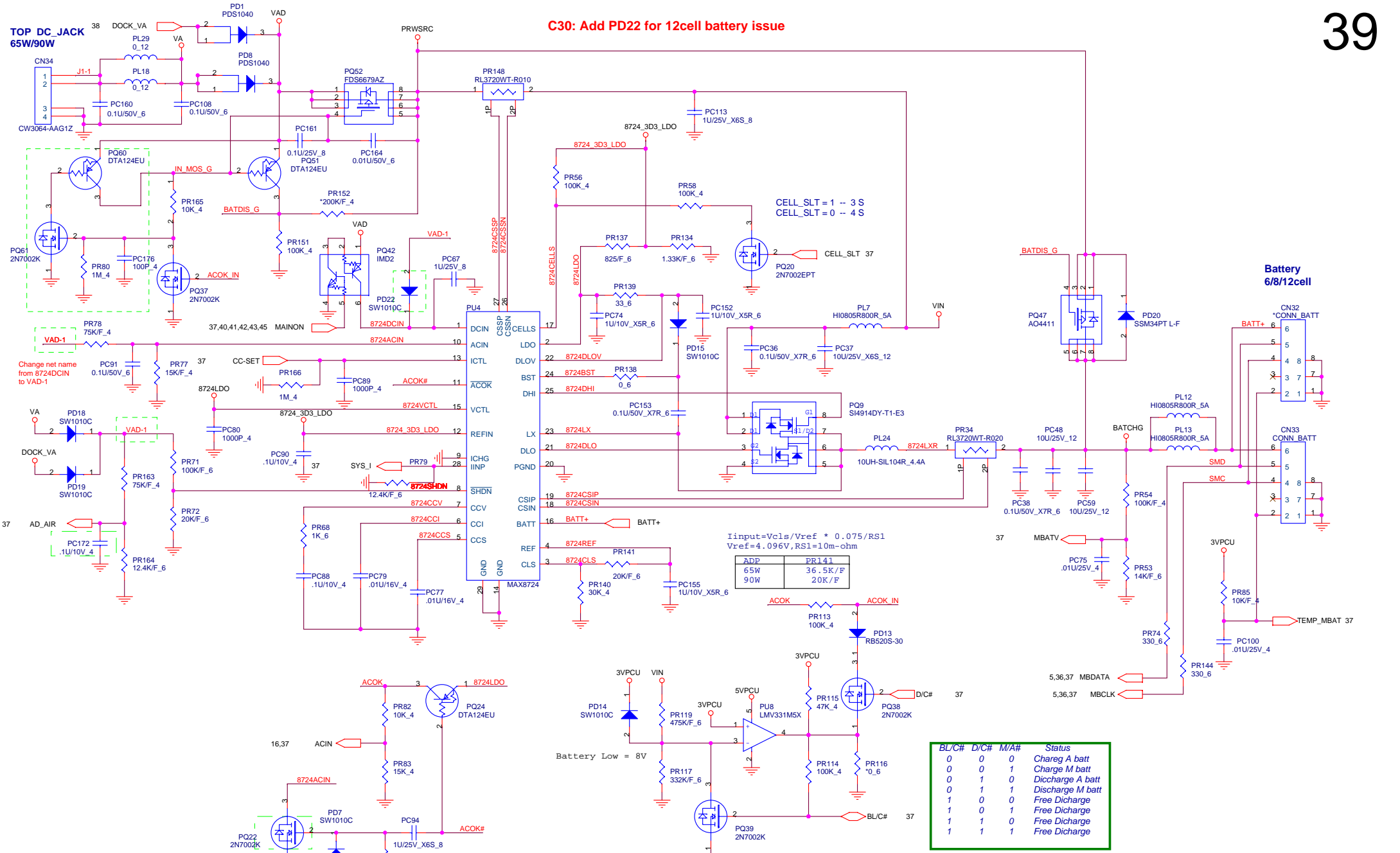


FAN2 PWM CONNECTOR



FAN1 PWM CONNECTOR

C30: Add PD22 for 12cell battery issue



$$I_{input} = V_{cls} / V_{ref} * 0.075 / R_{S1}$$

$$V_{ref} = 4.096V, R_{S1} = 10m\text{-ohm}$$

ADP	PR141
65W	36.5K/F
90W	20K/F

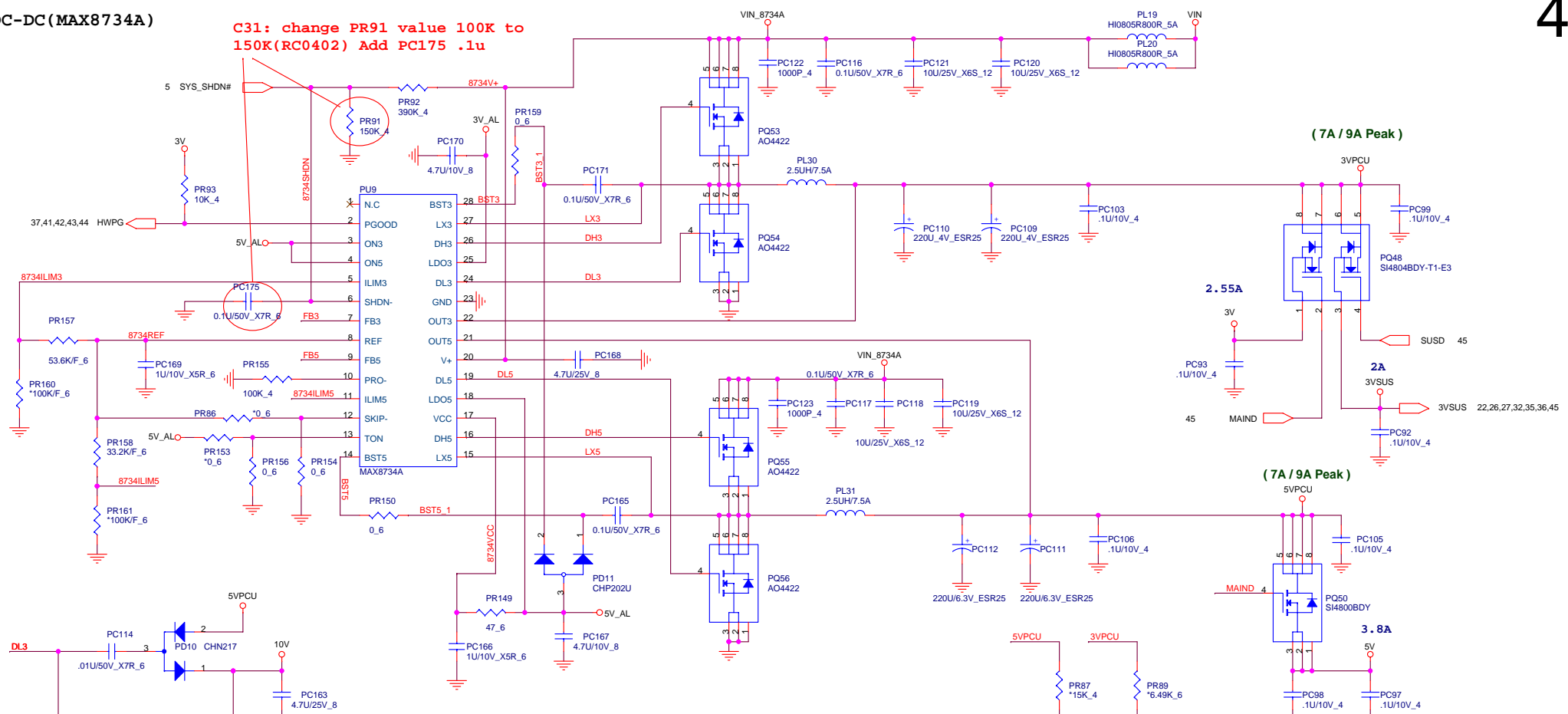
B/LC#	D/C#	M/A#	Status
0	0	0	Charge A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Discharge
1	0	1	Free Discharge
1	1	0	Free Discharge
1	1	1	Free Discharge



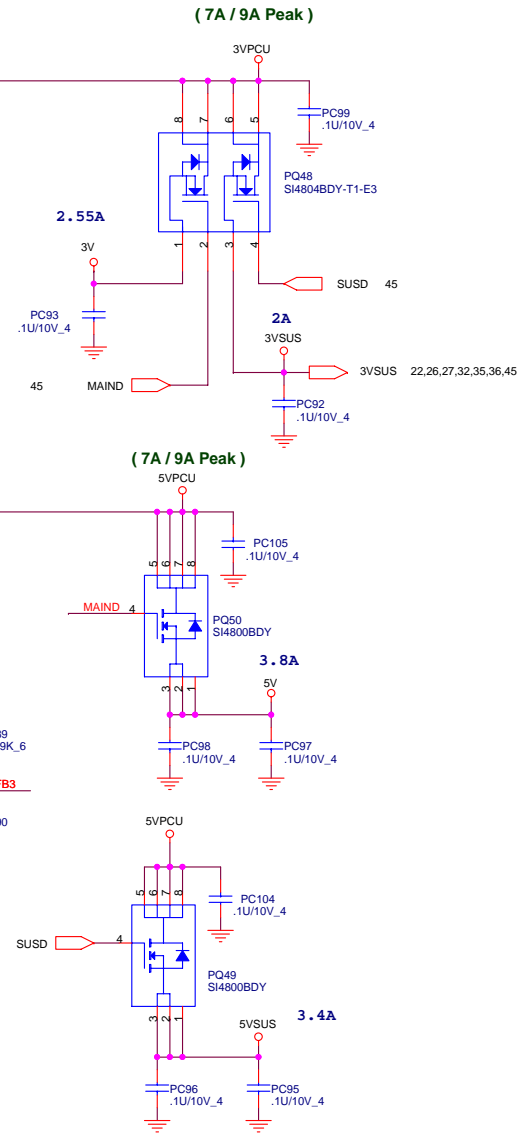
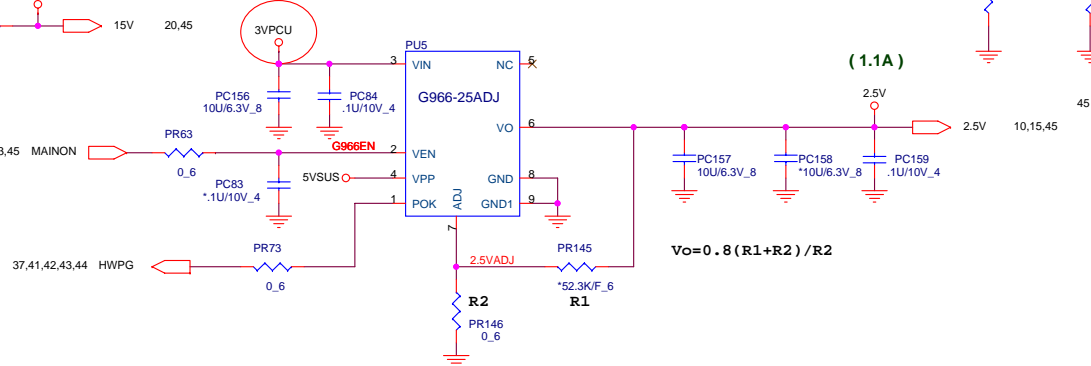
PROJECT : AT6  
Quanta Computer Inc.

DC-DC (MAX8734A)

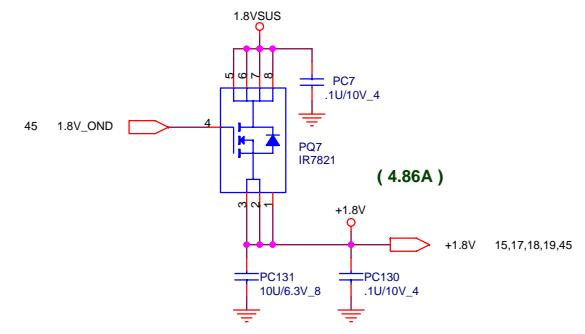
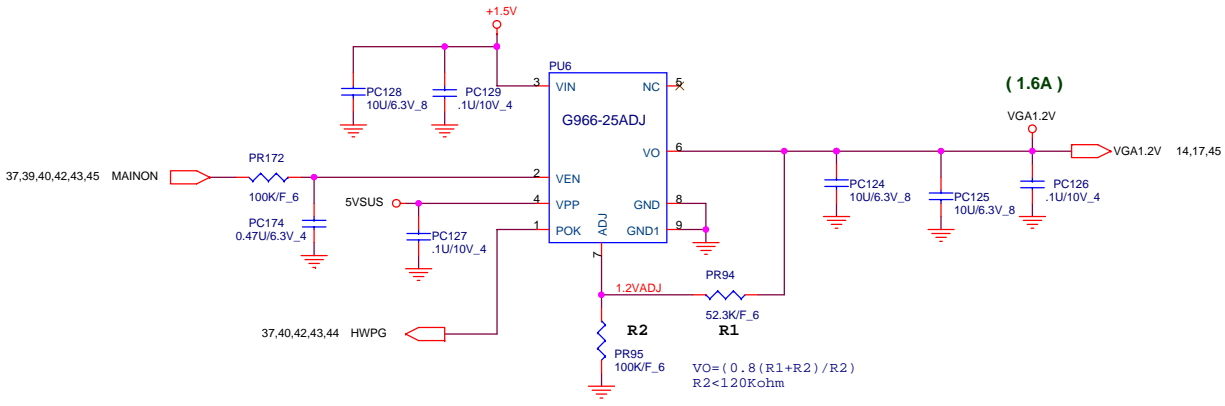
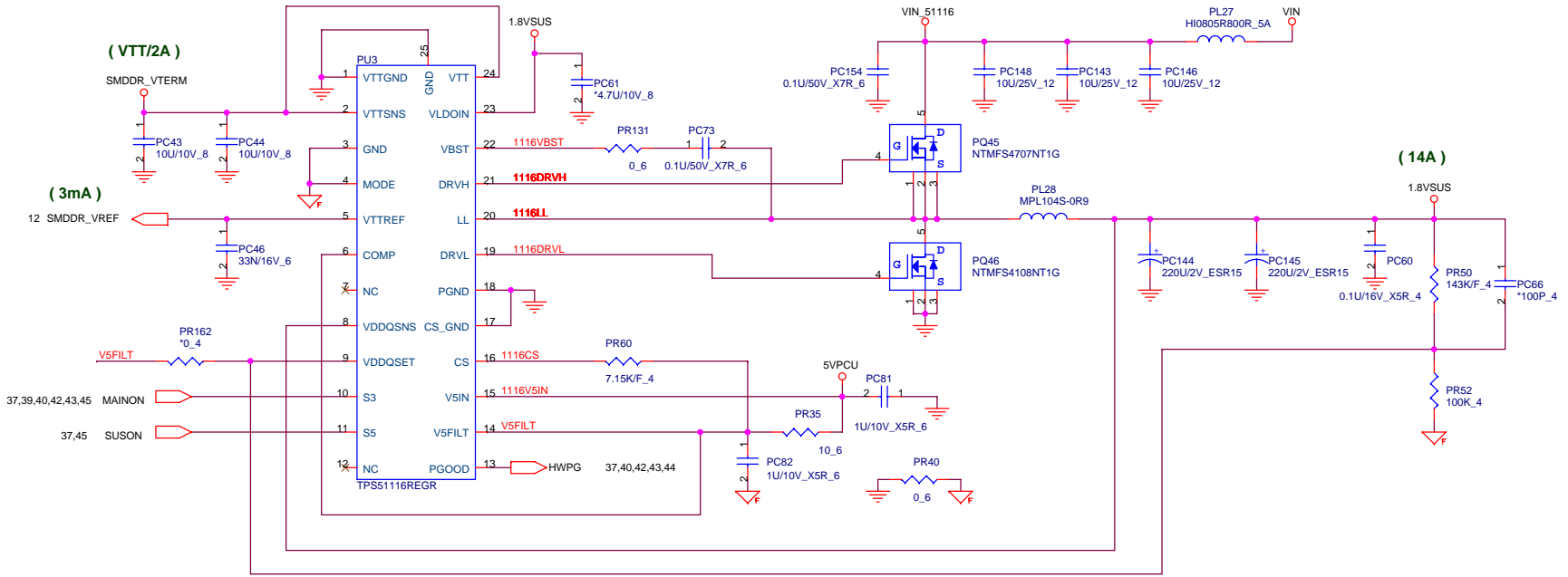
C31: change PR91 value 100K to 150K(RC0402) Add PC175 .1u



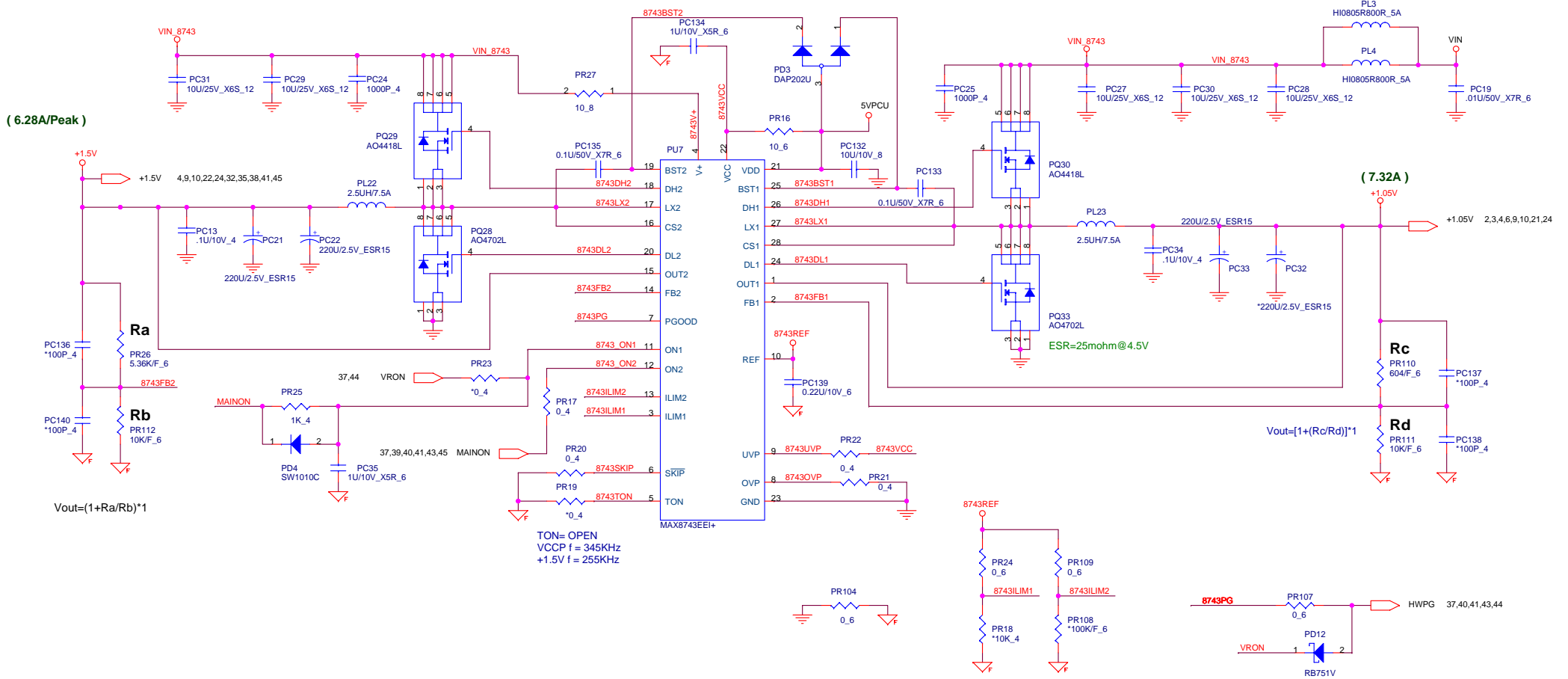
C32: change 2.5V power source from 3VSUS to 3VPCU

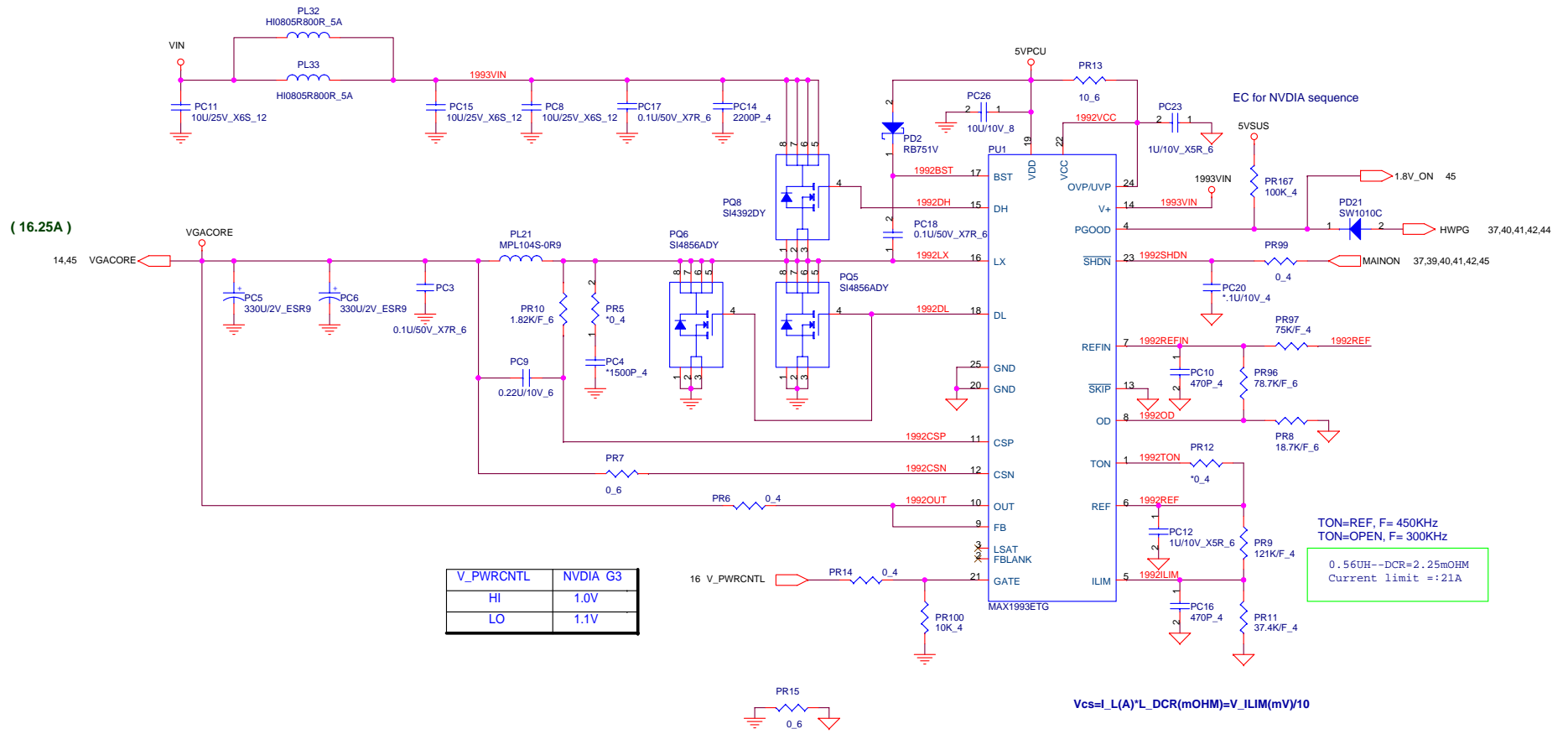


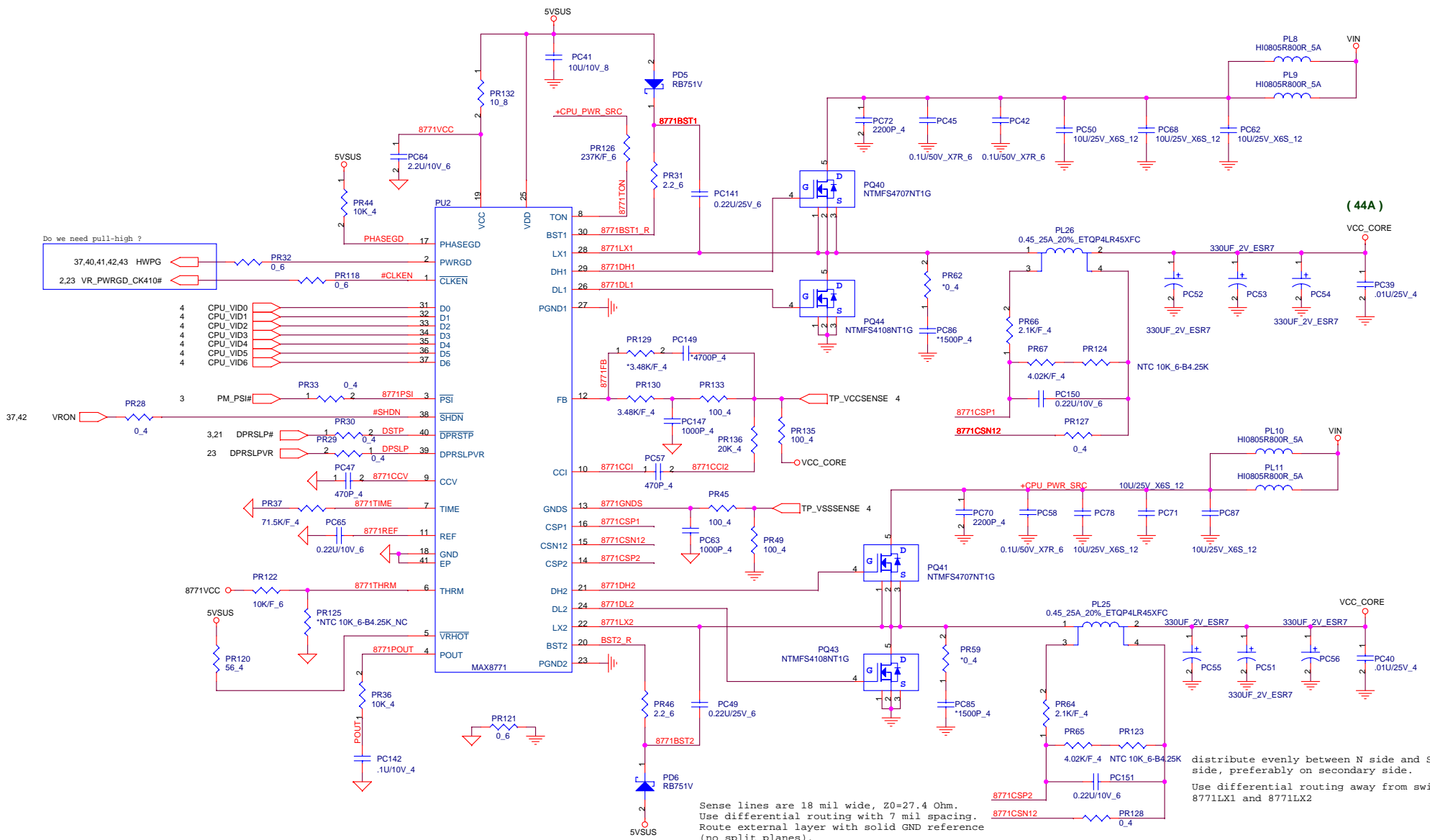




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Quanta Computer Inc.







Do we need pull-high ?


37.40,41,42,43 HWPG

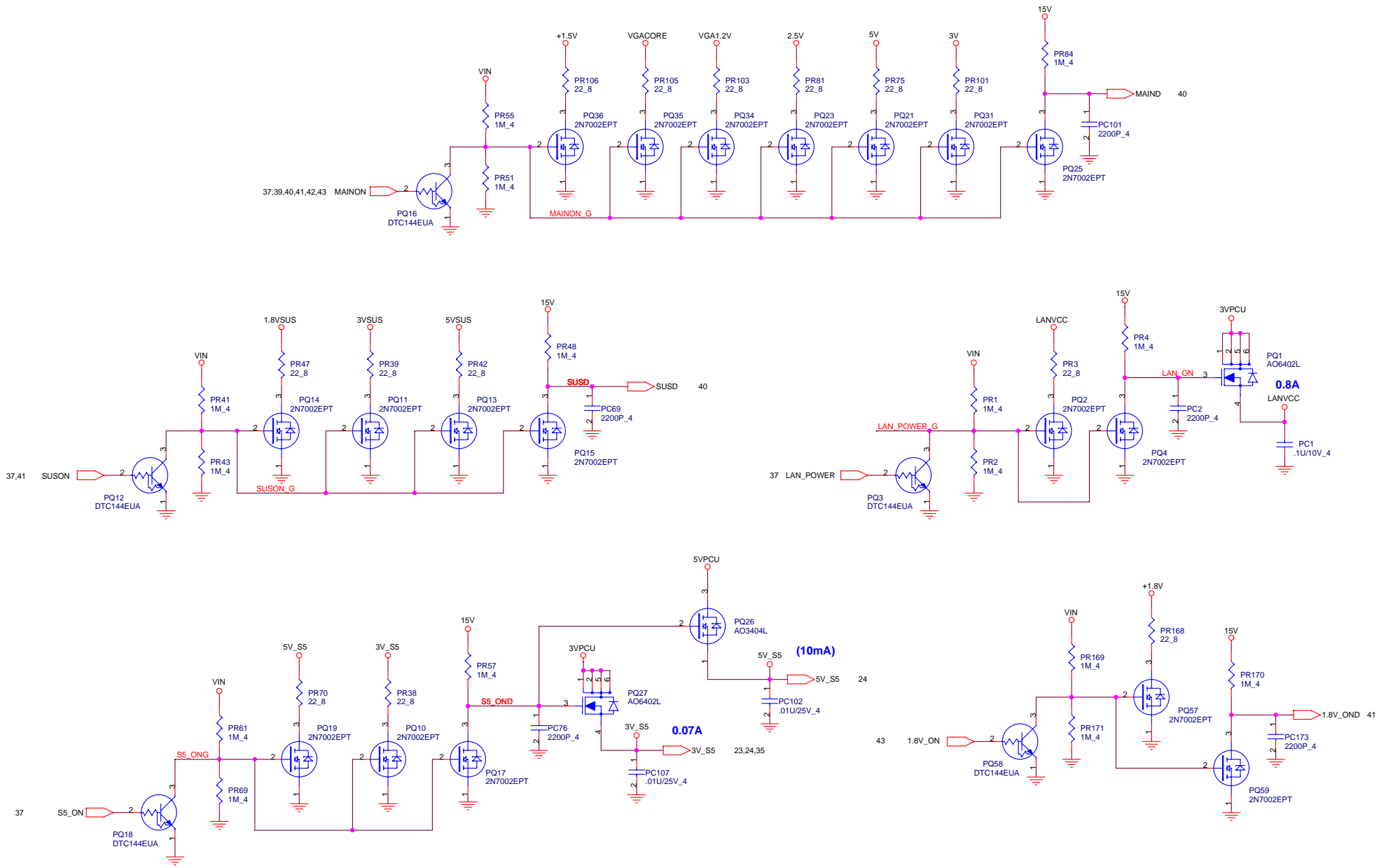
2.23 VR\_PWRGD\_CK410#


Sense lines are 18 mil wide, Z0=27.4 Ohm.  
 Use differential routing with 7 mil spacing.  
 Route external layer with solid GND reference  
 (no split planes).  
 Use 25 mil separation from any other signal.

distribute evenly between N side and S side, preferably on secondary side.  
 Use differential routing away from switch nodes  
 8771LX1 and 8771LX2

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

 NB5/RD1/HW2	<b>PROJECT : AT6</b> Quanta Computer Inc.	
	Size Custom Date: Monday, May 22, 2006	Document Number CPU_CORE(MAX8771)



 NB5/RD1/HW2	<b>PROJECT : AT6</b> Quanta Computer Inc.	
	Size Custom Date: Monday, May 22, 2006	Document Number <b>DISCHARGE</b>