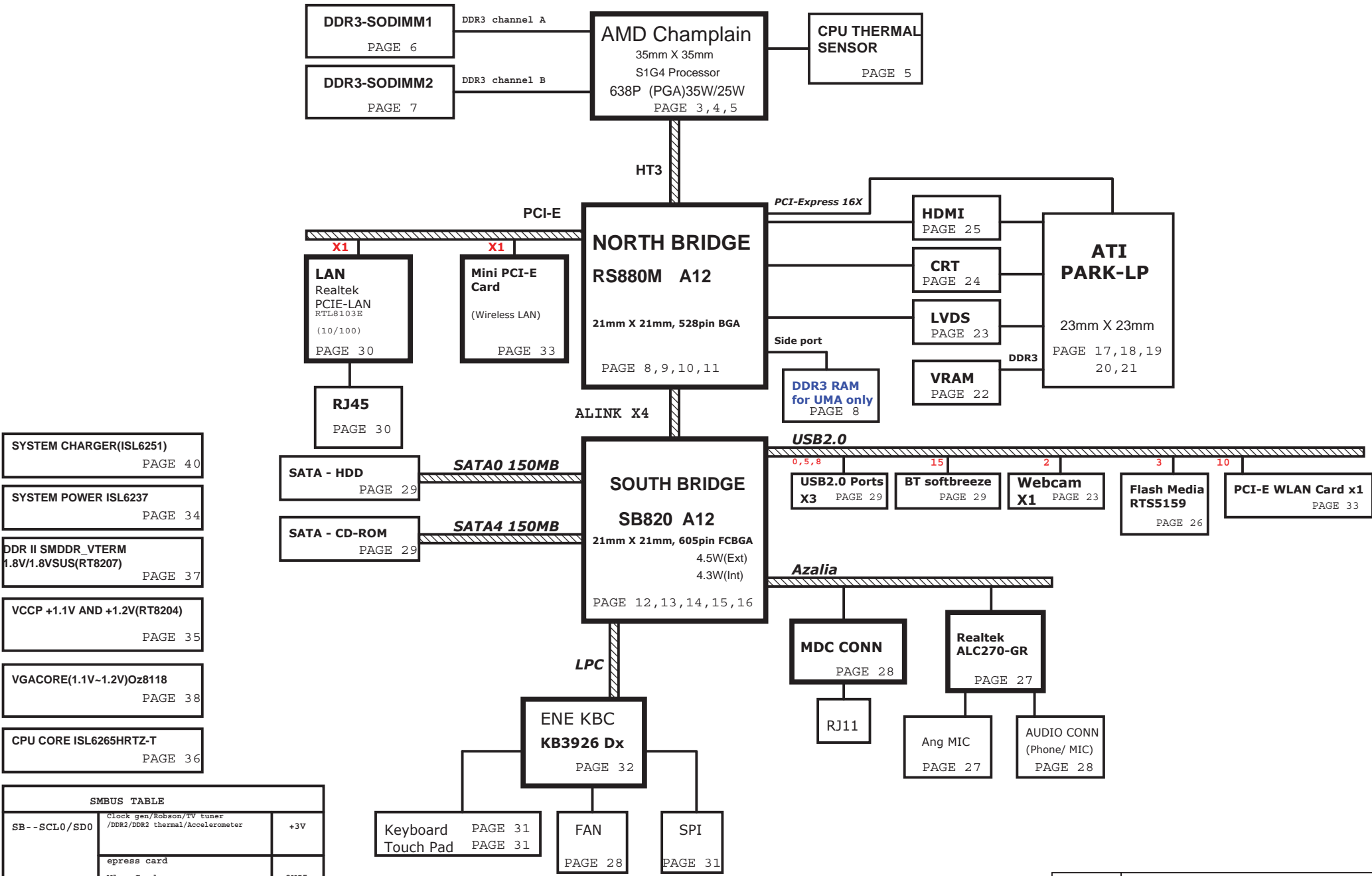


AX2/7 SYSTEM DIAGRAM



01




- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

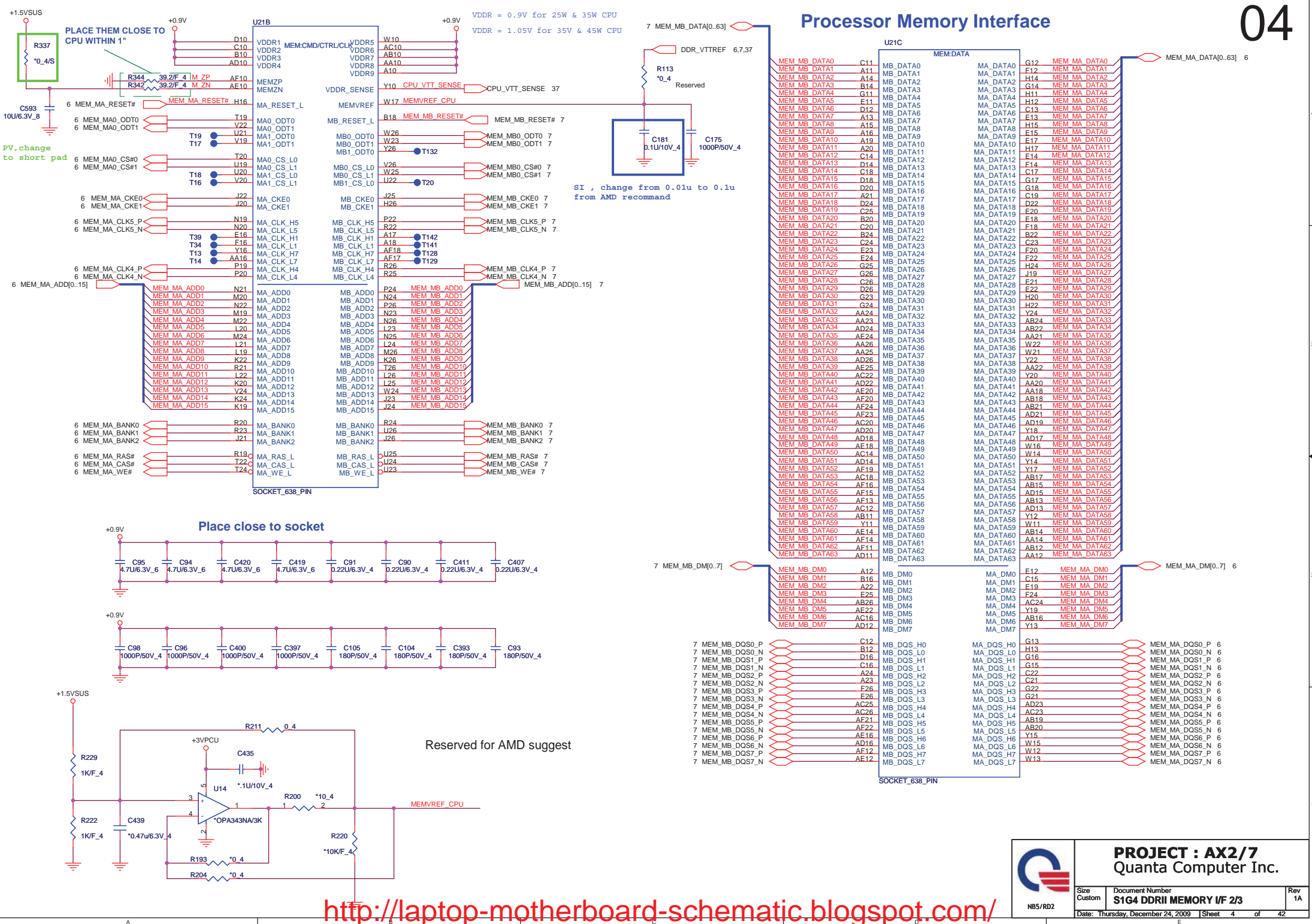
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Thursday, December 24, 2009 Sheet 1 of 42		

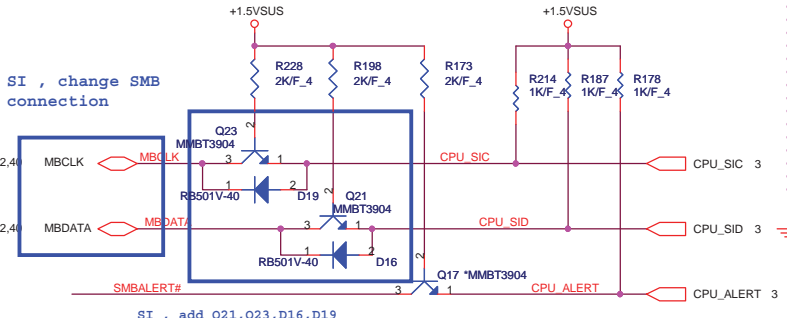
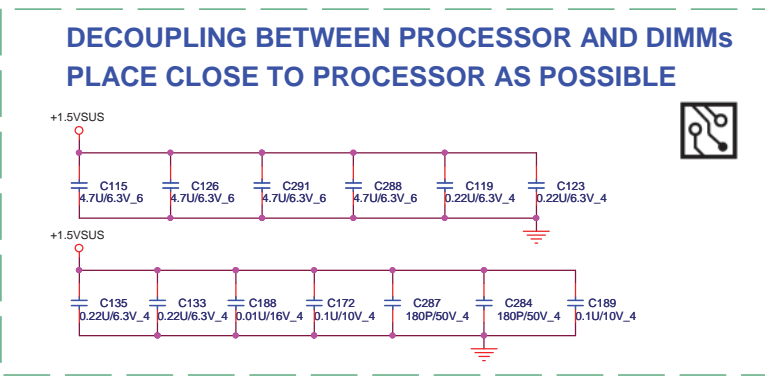
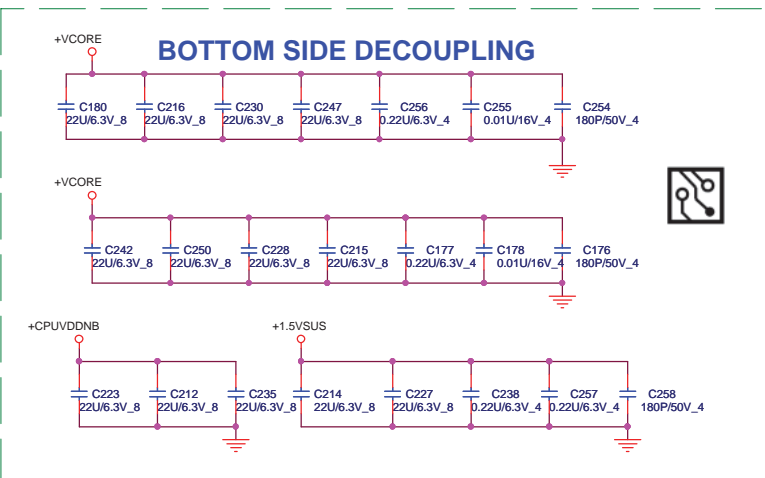
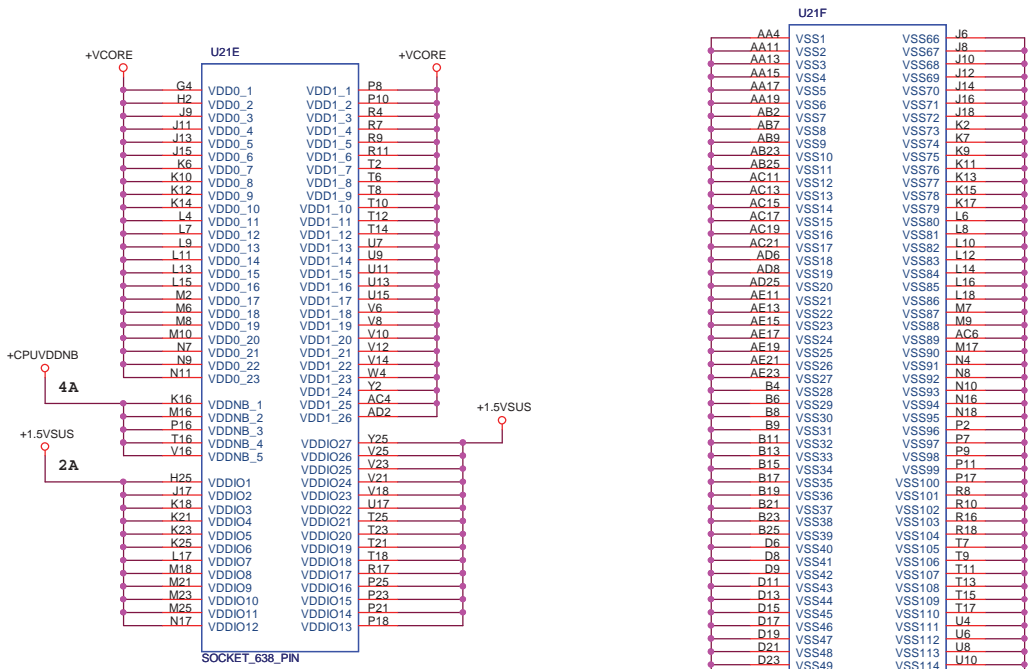
PV,delete all external clock GEN reserve material

 NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom	Document Number Clock Generator
Date: Wednesday, December 23, 2009 Sheet 2 of 42		Rev 1A

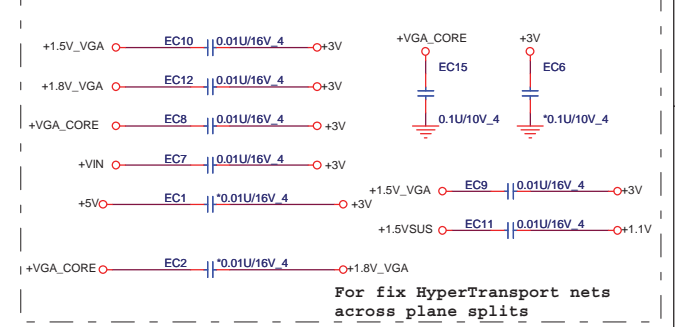
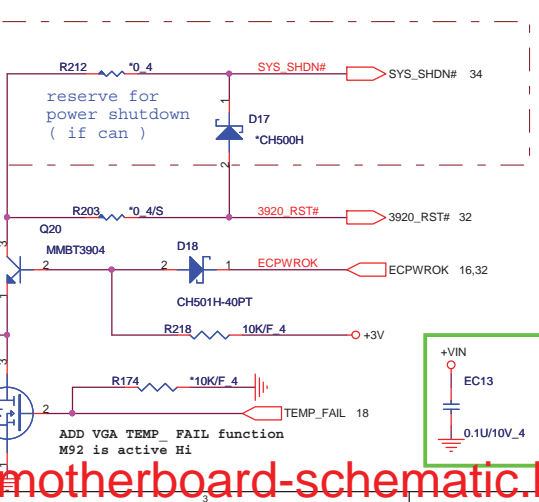
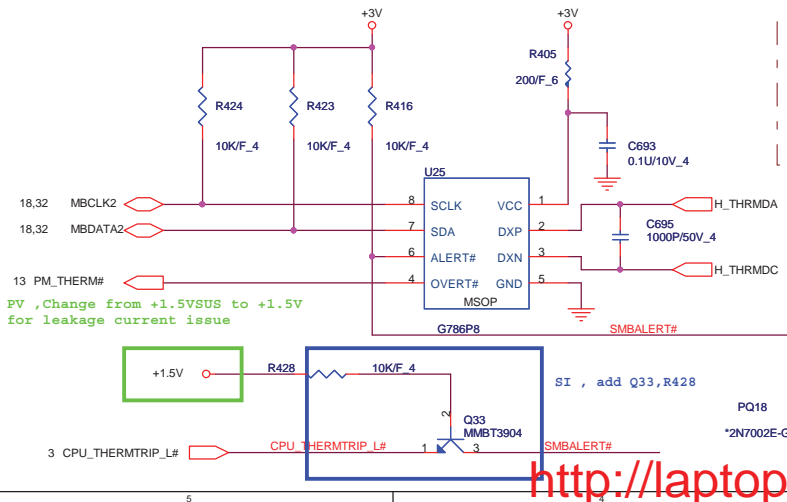


PROJECT : AX2/7
Quanta Computer Inc.

Size: Custom | Document Number: **S1G4 DDRII MEMORY I/F 2/3** | Rev: 1A
 Date: Thursday, December 24, 2009 | Sheet: 4 of 42



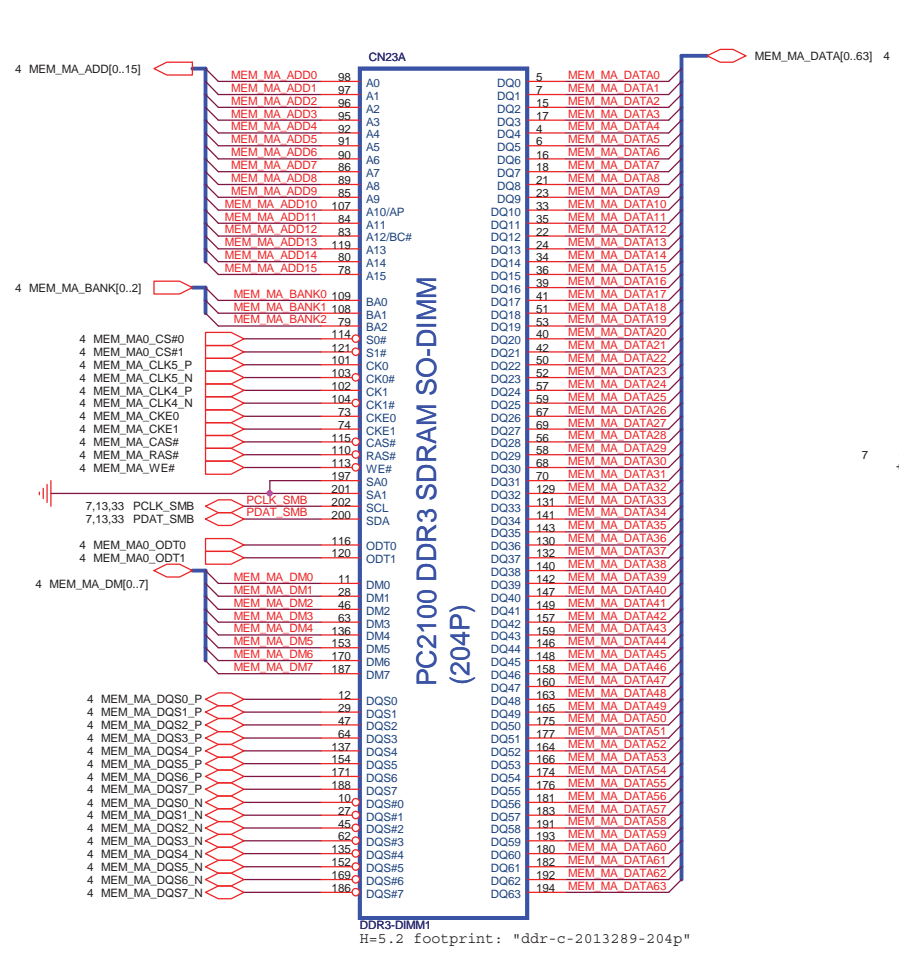
PROCESSOR POWER AND GROUND



PROJECT : AX2/7
Quanta Computer Inc.

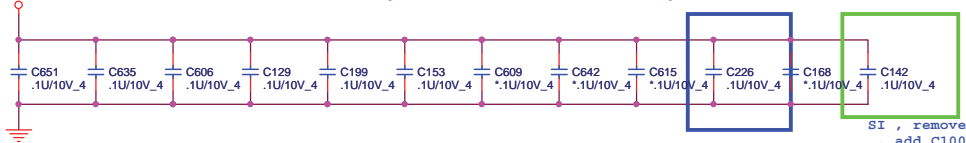
Size Custom Document Number S1G4 PWR & GND 3/3 Rev 1A

Date: Thursday, December 24, 2009 Sheet 5 of 42

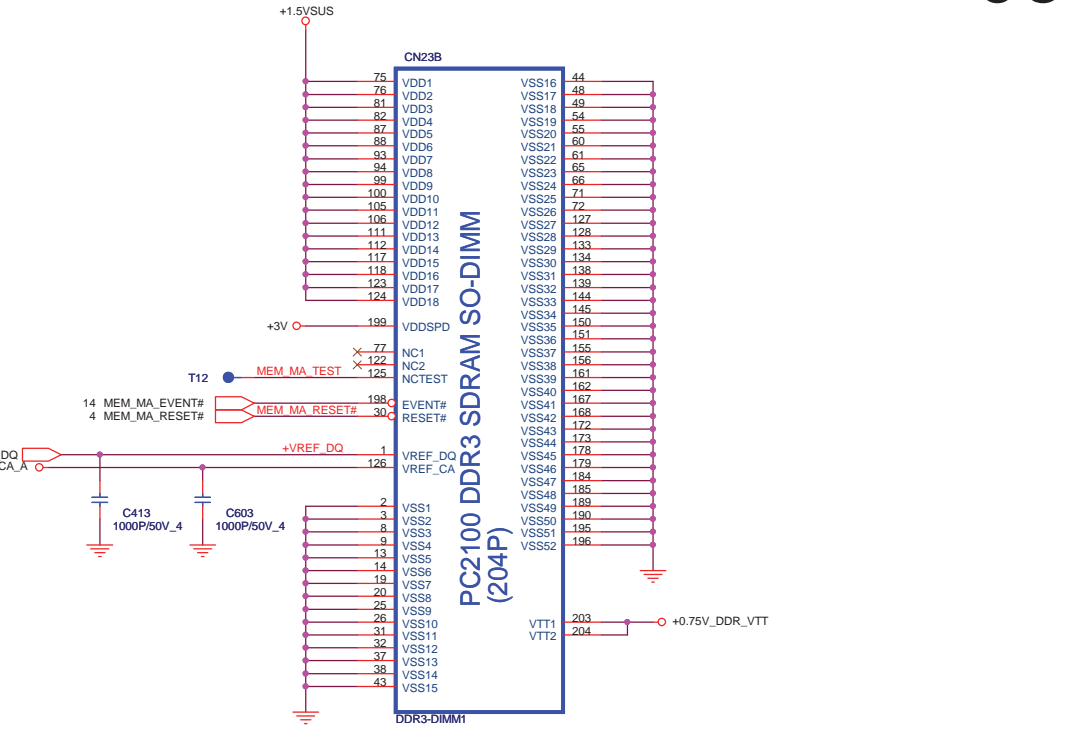
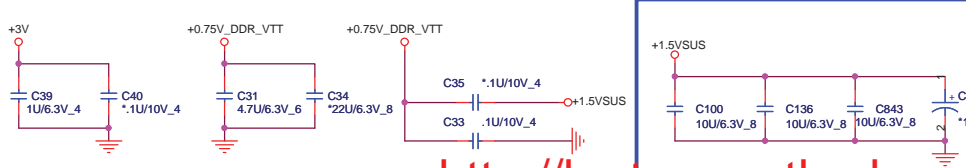


SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

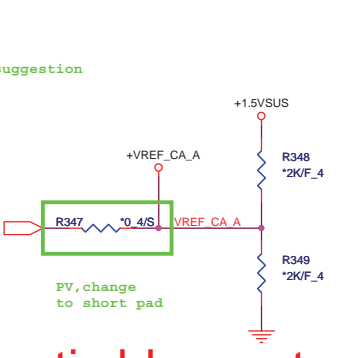
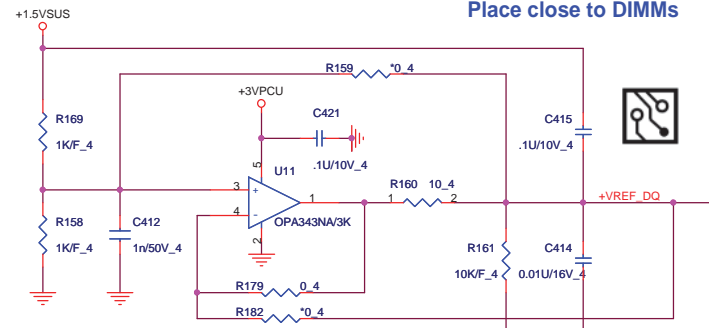
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN) SI , add C226 from EMI suggest



DE-COUPLING FOR DIMM1

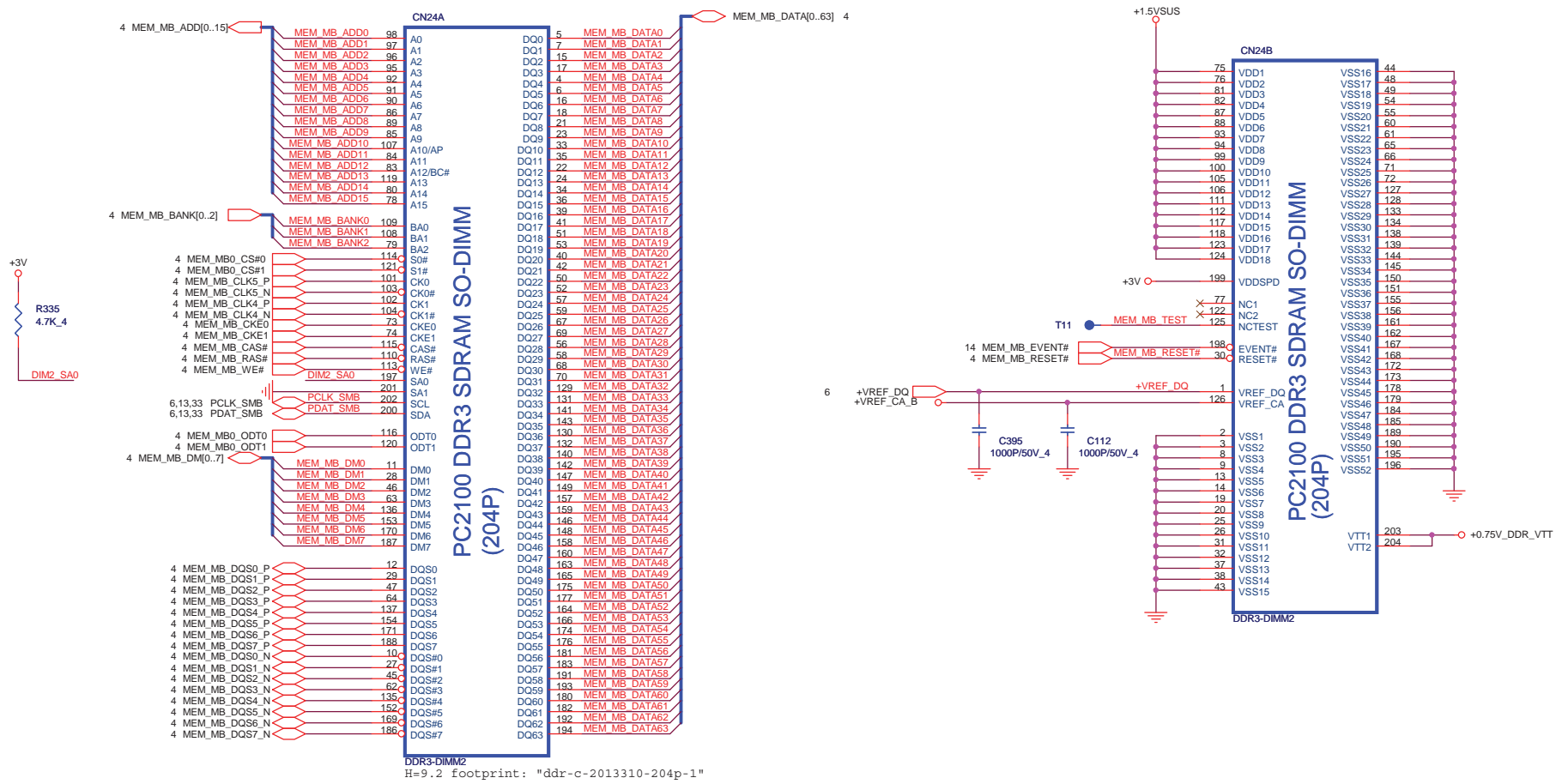


Place close to DIMMs

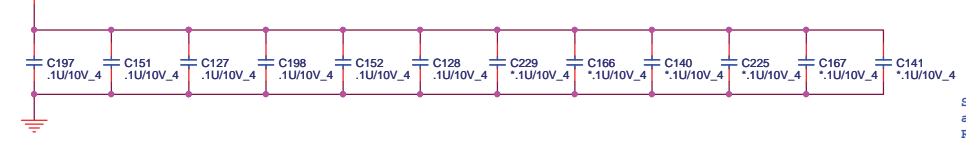


PROJECT : AX2/7
Quanta Computer Inc.

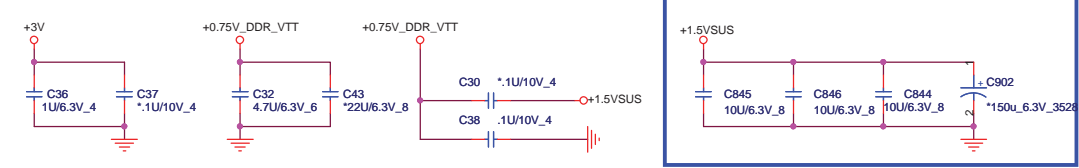
Size Custom Document Number **DDR3 SODIMMS: A/B CHANNEL** Rev 1A
NB5/RD2 Date: Thursday, December 24, 2009 1 Sheet 6 of 42



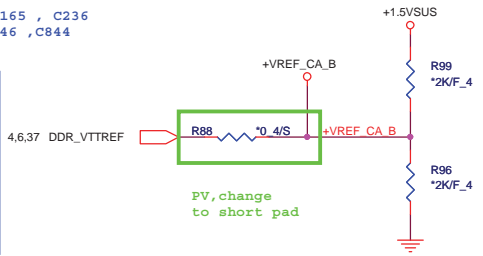
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



DE-COUPLING FOR DIMM2



SI , remove C165 , C236
 add C845 , C846 , C844
 Reserve C902



	PROJECT : AX2/7	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
DDR3 SODIMMS TERMINATIONS		
Date: Thursday, December 24, 2009	Sheet 7	of 42

GFX_RX can remove at next stage for MUXLESS

SI , for routing smooth
GFX_TX 0/1/3/9/10/11

UMA can remove all GFX_TX CAP

SI remove C711,C713,C710,
C712,C708,C709,C703,C704
for MUXLESS

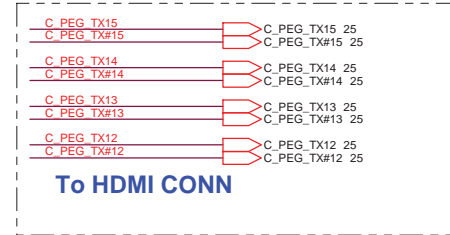
PART 2 OF 6

PCI-E I/F GFX

PEG_RX15	D4	GFX_RX0P	A5	C PEG_TX#15	C711	*0.1U/10V_4	PEG_TX15
PEG_RX#15	C4	GFX_RX0N	B5	C PEG_TX#15	C713	*0.1U/10V_4	PEG_TX#15
PEG_RX#14	A3	GFX_RX1P	A4	C PEG_TX#14	C710	*0.1U/10V_4	PEG_TX14
PEG_RX14	B3	GFX_RX1N	B4	C PEG_TX14	C712	*0.1U/10V_4	PEG_TX#14
PEG_RX13	C2	GFX_RX2P	C3	C PEG_TX13	C708	*0.1U/10V_4	PEG_TX13
PEG_RX#13	C1	GFX_RX2N	B2	C PEG_TX#13	C709	*0.1U/10V_4	PEG_TX#13
PEG_RX12	E5	GFX_RX3P	D1	C PEG_TX12	C703	*0.1U/10V_4	PEG_TX12
PEG_RX#12	E4	GFX_RX3N	D2	C PEG_TX#12	C704	*0.1U/10V_4	PEG_TX#12
PEG_RX11	E5	GFX_RX4P	E2	C PEG_TX11	C698	*0.1U/10V_4	PEG_TX11
PEG_RX#11	G6	GFX_RX4N	E1	C PEG_TX#11	C696	*0.1U/10V_4	PEG_TX#11
PEG_RX10	H5	GFX_RX5P	F4	C PEG_TX10	C691	*0.1U/10V_4	PEG_TX10
PEG_RX#10	H6	GFX_RX5N	F3	C PEG_TX#10	C694	*0.1U/10V_4	PEG_TX#10
PEG_RX9	J6	GFX_RX6P	F1	C PEG_TX9	C690	*0.1U/10V_4	PEG_TX9
PEG_RX#9	J5	GFX_RX6N	F2	C PEG_TX#9	C688	*0.1U/10V_4	PEG_TX#9
PEG_RX8	J5	GFX_RX7P	H4	C PEG_TX8	C686	*0.1U/10V_4	PEG_TX8
PEG_RX#8	J8	GFX_RX7N	H3	C PEG_TX#8	C687	*0.1U/10V_4	PEG_TX#8
PEG_RX7	L5	GFX_RX8P	H1	C PEG_TX7	C685	*0.1U/10V_4	PEG_TX7
PEG_RX#7	L6	GFX_RX8N	H2	C PEG_TX#7	C682	*0.1U/10V_4	PEG_TX#7
PEG_RX6	M6	GFX_RX9P	J2	C PEG_TX6	C679	*0.1U/10V_4	PEG_TX6
PEG_RX#6	M8	GFX_RX9N	J1	C PEG_TX#6	C681	*0.1U/10V_4	PEG_TX#6
PEG_RX5	P7	GFX_RX10P	K4	C PEG_TX5	C675	*0.1U/10V_4	PEG_TX5
PEG_RX#5	M7	GFX_RX10N	K3	C PEG_TX#5	C676	*0.1U/10V_4	PEG_TX#5
PEG_RX4	P5	GFX_RX11P	K1	C PEG_TX4	C677	*0.1U/10V_4	PEG_TX4
PEG_RX#4	M5	GFX_RX11N	K2	C PEG_TX#4	C678	*0.1U/10V_4	PEG_TX#4
PEG_RX3	P8	GFX_RX12P	M4	C PEG_TX3	C670	*0.1U/10V_4	PEG_TX3
PEG_RX#3	P8	GFX_RX12N	M3	C PEG_TX#3	C674	*0.1U/10V_4	PEG_TX#3
PEG_RX2	R6	GFX_RX13P	M1	C PEG_TX2	C669	*0.1U/10V_4	PEG_TX2
PEG_RX#2	R5	GFX_RX13N	M2	C PEG_TX#2	C667	*0.1U/10V_4	PEG_TX#2
PEG_RX1	P4	GFX_RX14P	N2	C PEG_TX1	C662	*0.1U/10V_4	PEG_TX1
PEG_RX0	P3	GFX_RX14N	N1	C PEG_TX#1	C666	*0.1U/10V_4	PEG_TX#1
PEG_RX#0	T3	GFX_RX15P	P1	C PEG_TX0	C656	*0.1U/10V_4	PEG_TX0
		GFX_RX15N	P2	C PEG_TX#0	C658	*0.1U/10V_4	PEG_TX#0

PV,change to reserve for MUXLESS

Close to North Bridge



To HDMI CONN



TO WLAN
TO PCI-E-LAN

PCI-E I/F GPP

PCI-E I/F SB

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

SB_RX0P	AD7	A TX0P C C622	0.1U/10V_4	PCI-E_NB_SB_TX0P	12
SB_RX0N	AE7	A TX0N C C621	0.1U/10V_4	PCI-E_NB_SB_TX0N	12
SB_RX1P	AE6	A TX1P C C623	0.1U/10V_4	PCI-E_NB_SB_TX1P	12
SB_RX1N	AD6	A TX1N C C624	0.1U/10V_4	PCI-E_NB_SB_TX1N	12
SB_RX2P	AC6	A TX2P C C157	0.1U/10V_4	PCI-E_NB_SB_TX2P	12
SB_RX2N	AD5	A TX2N C C158	0.1U/10V_4	PCI-E_NB_SB_TX2N	12
SB_RX3P	AD5	A TX3P C C626	0.1U/10V_4	PCI-E_NB_SB_TX3P	12
SB_RX3N	AE5	A TX3N C C625	0.1U/10V_4	PCI-E_NB_SB_TX3N	12



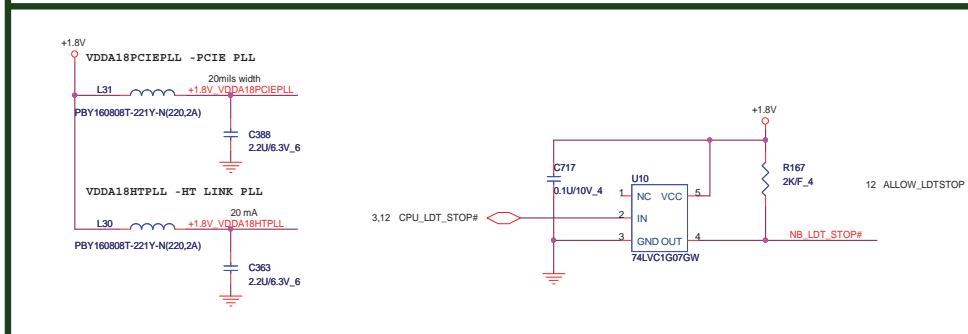
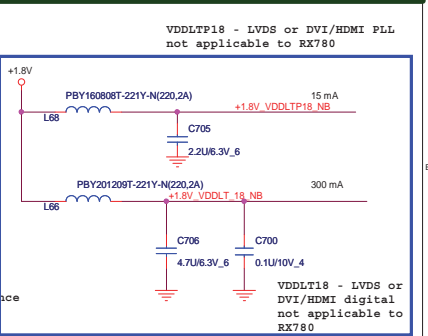
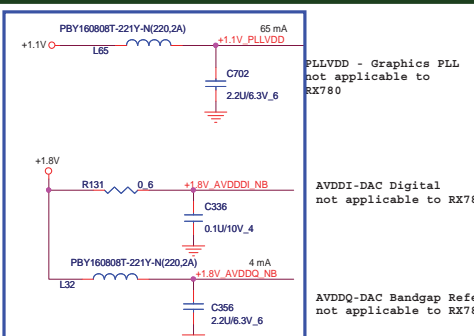
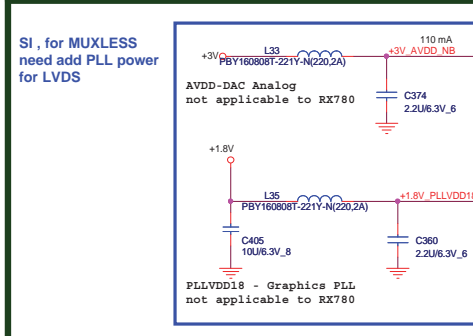
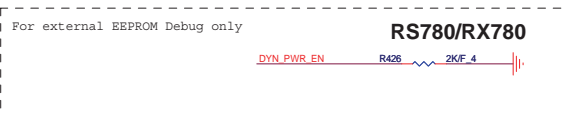
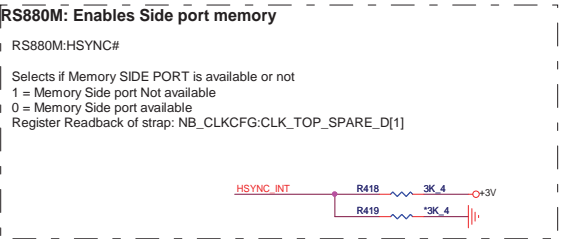
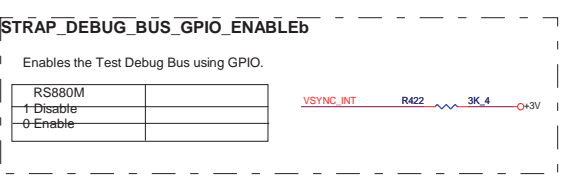
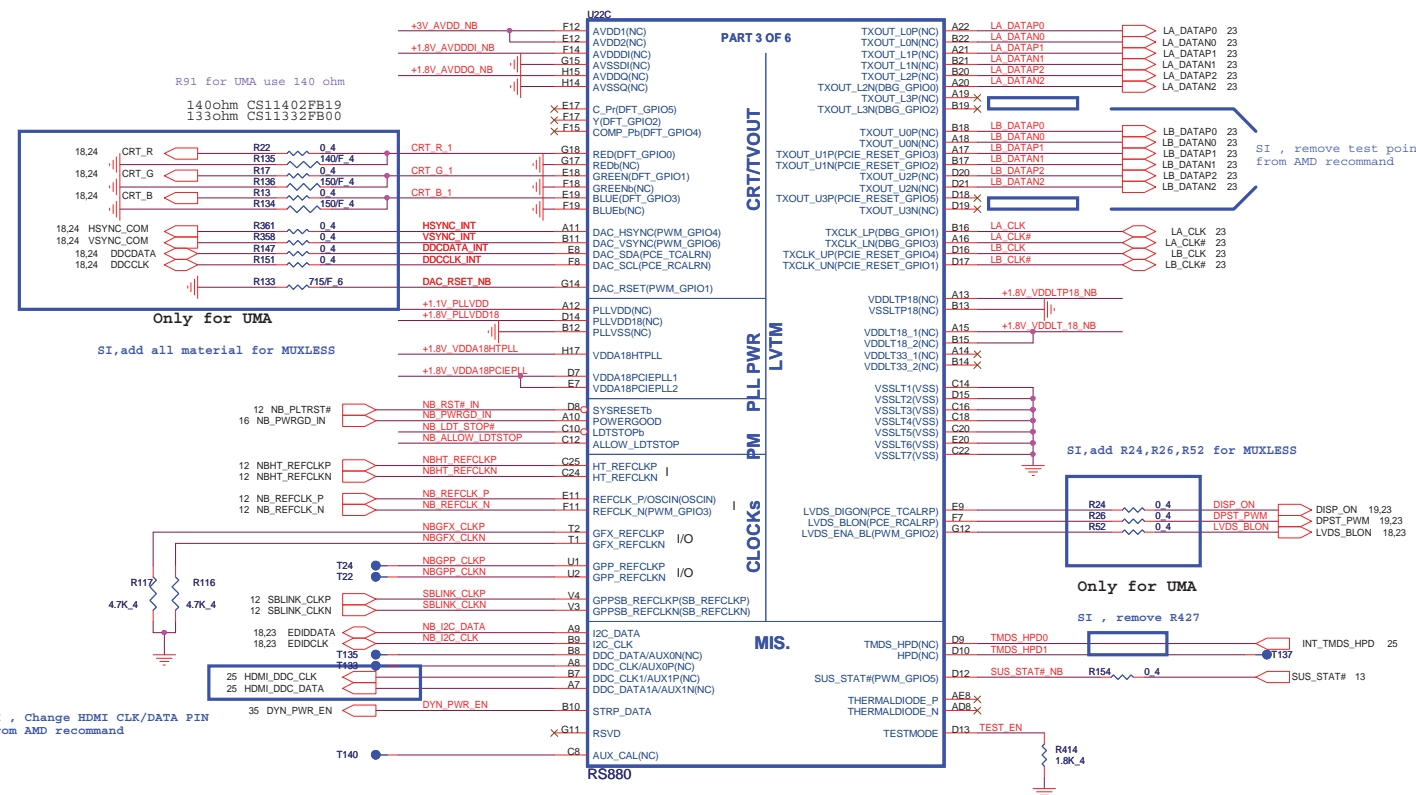
RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

PROJECT : AX2/7
Quanta Computer Inc.

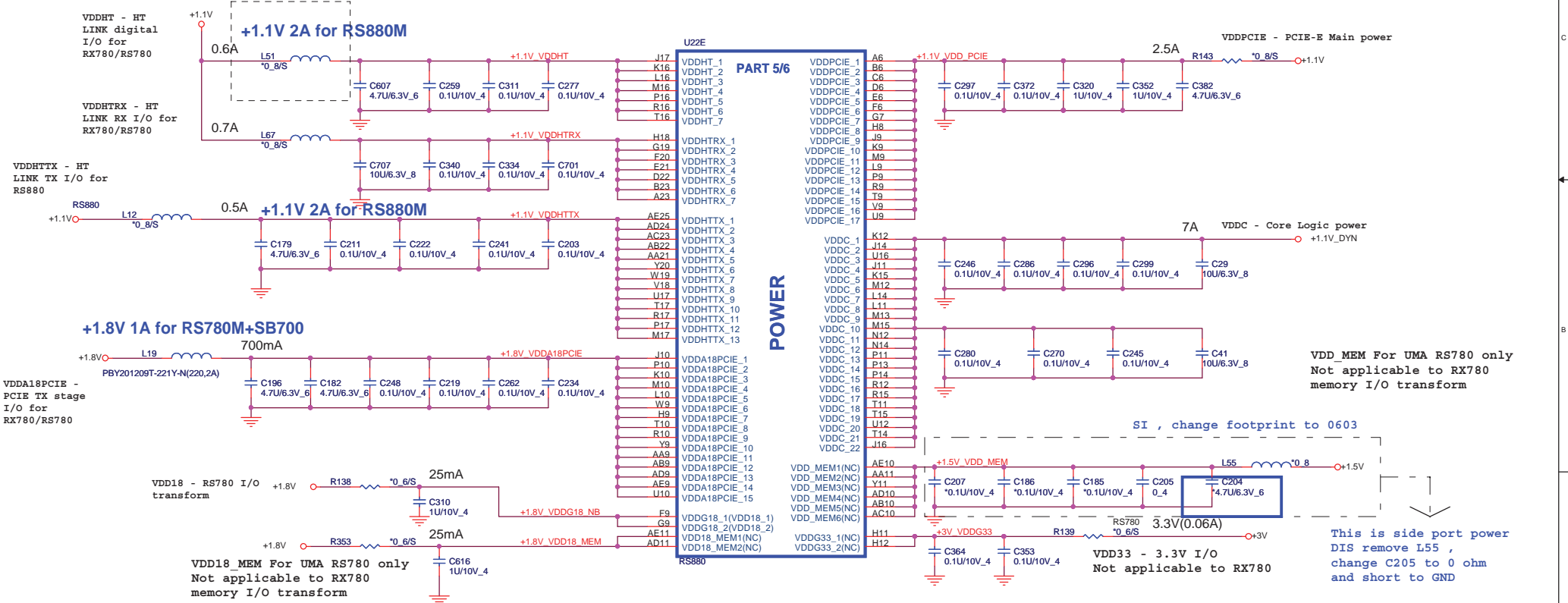
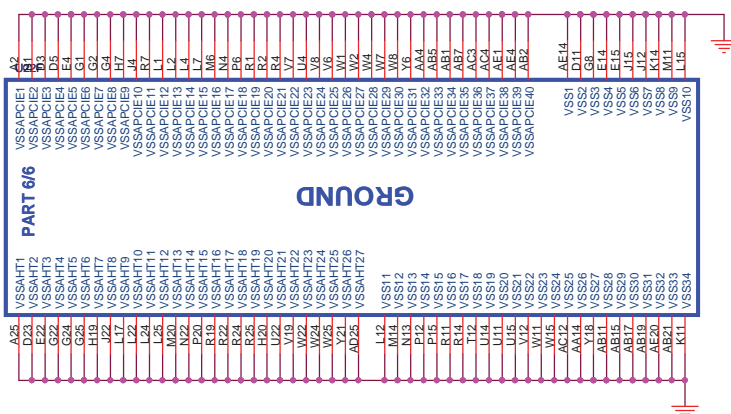
Size Custom Document Number **RS880-PCI-E I/F 2/5** Rev 1A

Date: Thursday, December 24, 2009 | Sheet 9 of 42



RS880M POWER TABLE

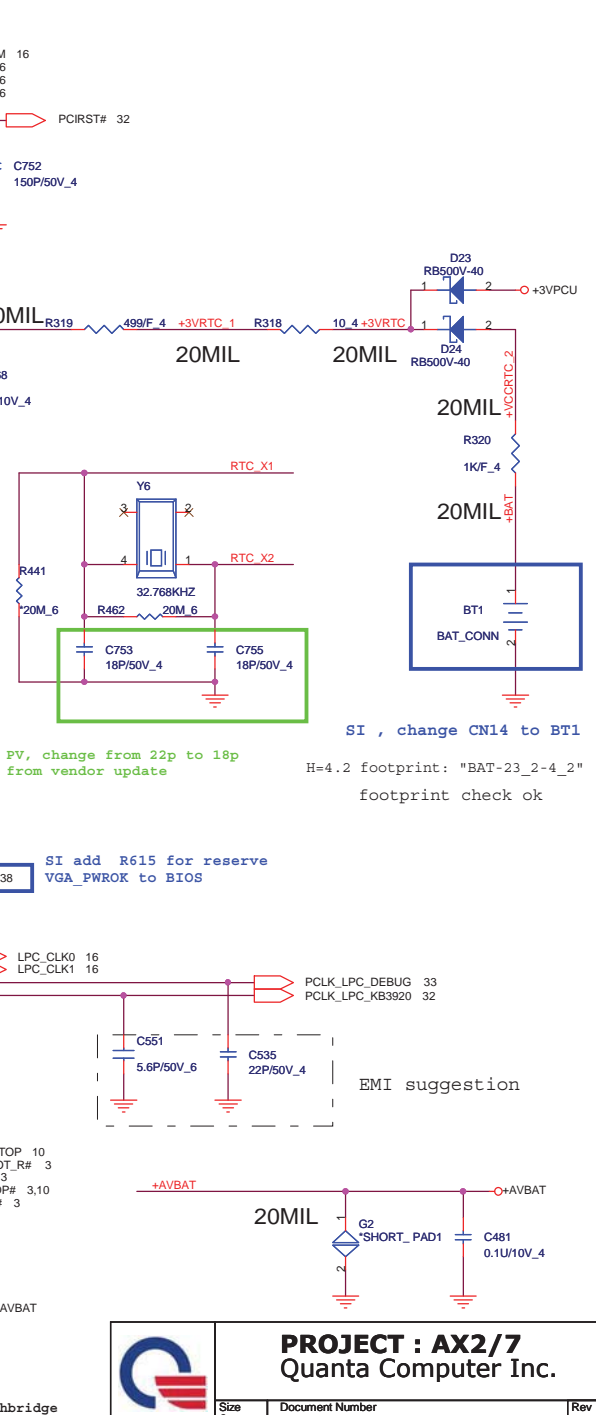
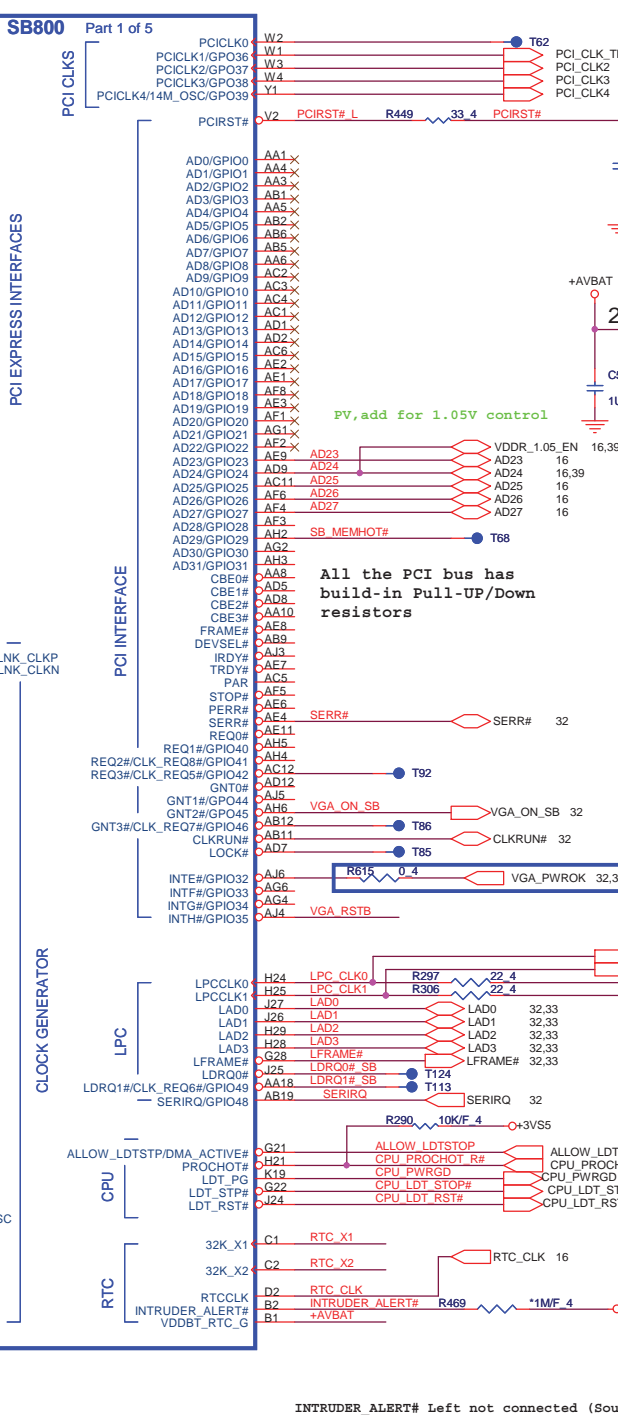
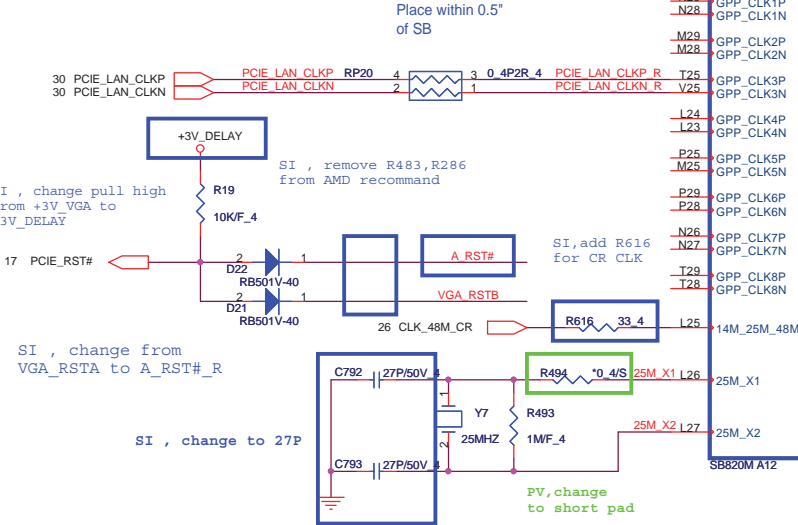
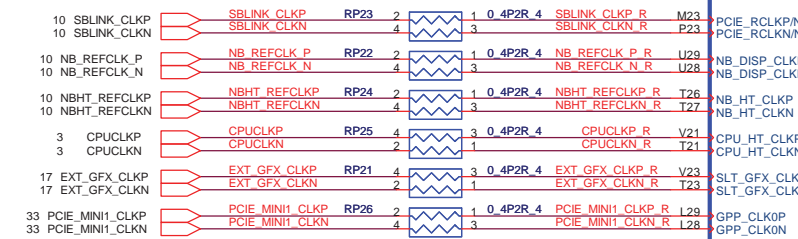
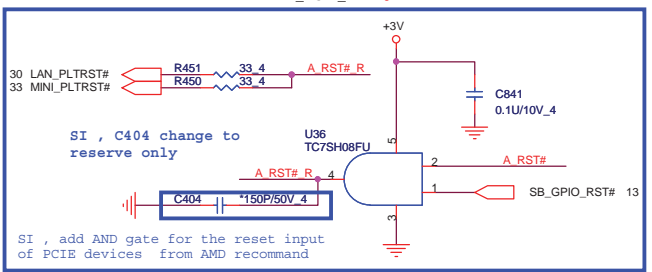
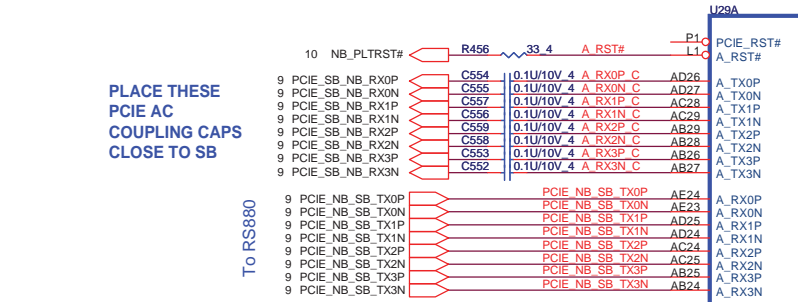
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLTP18	+1.8V
IOPLLVD18	+1.8V	VDDLTP18	+1.8V
		VDDLTP18	NC



PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number RS880-POWER5/5	Rev 1A
Date: Tuesday, December 22, 2009		Sheet 11 of 42

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB



SI, add AND gate for the reset input of PCIE devices from AMD recommend

Place within 0.5" of SB

SI, change pull high from +3V_VGA to +3V_DELAY

SI, change from VGA_RSTA to A_RST#_R

SI, change to 27P

All the PCI bus has build-in Pull-Up/Down resistors

SI add R615 for reserve VGA_PWROK to BIOS

SI, change CN14 to BT1

H=4.2 footprint: "BAT-23_2_4_2" footprint check ok

EMI suggestion

PV, add for 1.05V control

PV, change from 22p to 18p from vendor update

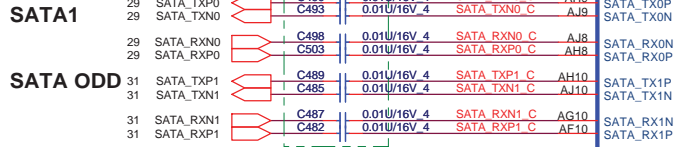
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom | Document Number **SB820-PCIE/PCU/CPU/LPC 1/4** | Rev 1A

Date: Thursday, December 24, 2009 | Sheet 12 of 42

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820



IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SI define side port ID

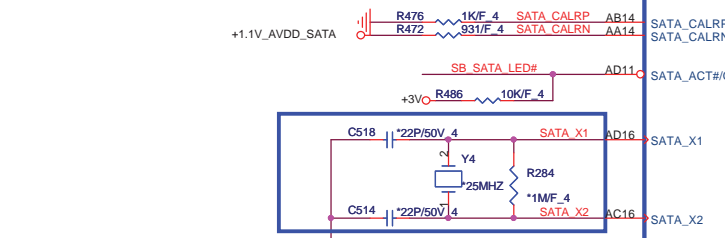
SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

PLVDD SATA--
SATA PLL
POWER

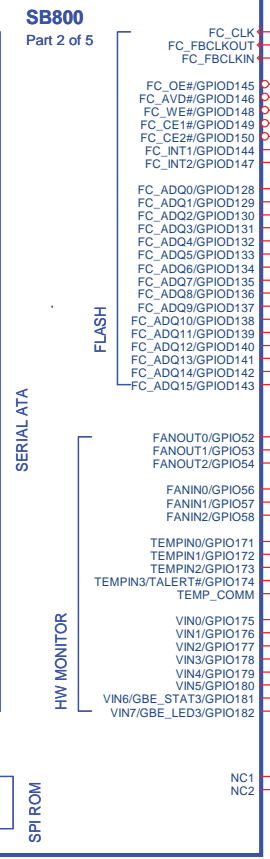
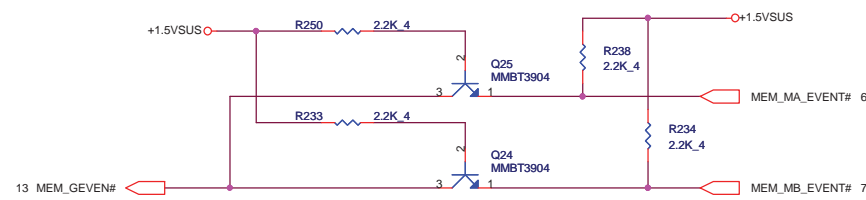
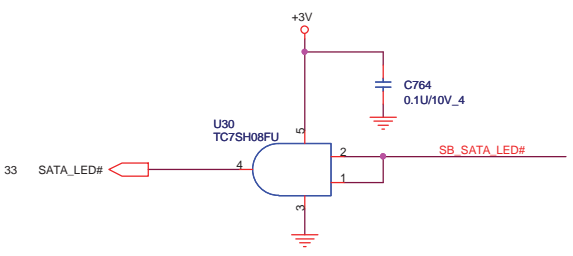
XTLVDD SATA-- SATA
crystal power

PLACE SATA CAL RES VERY CLOSE
TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



SI, change to reserve only

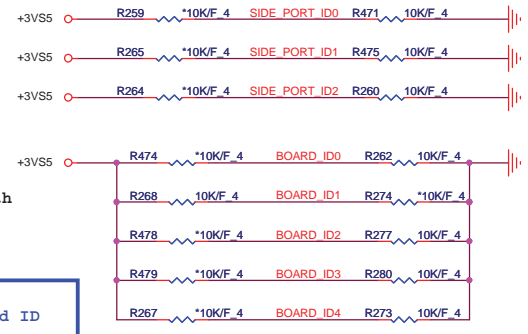


SI, remove test point
from AMD recommend

PV, change
to short pad

For blue tooth
& wireless
merge card

SI define board ID



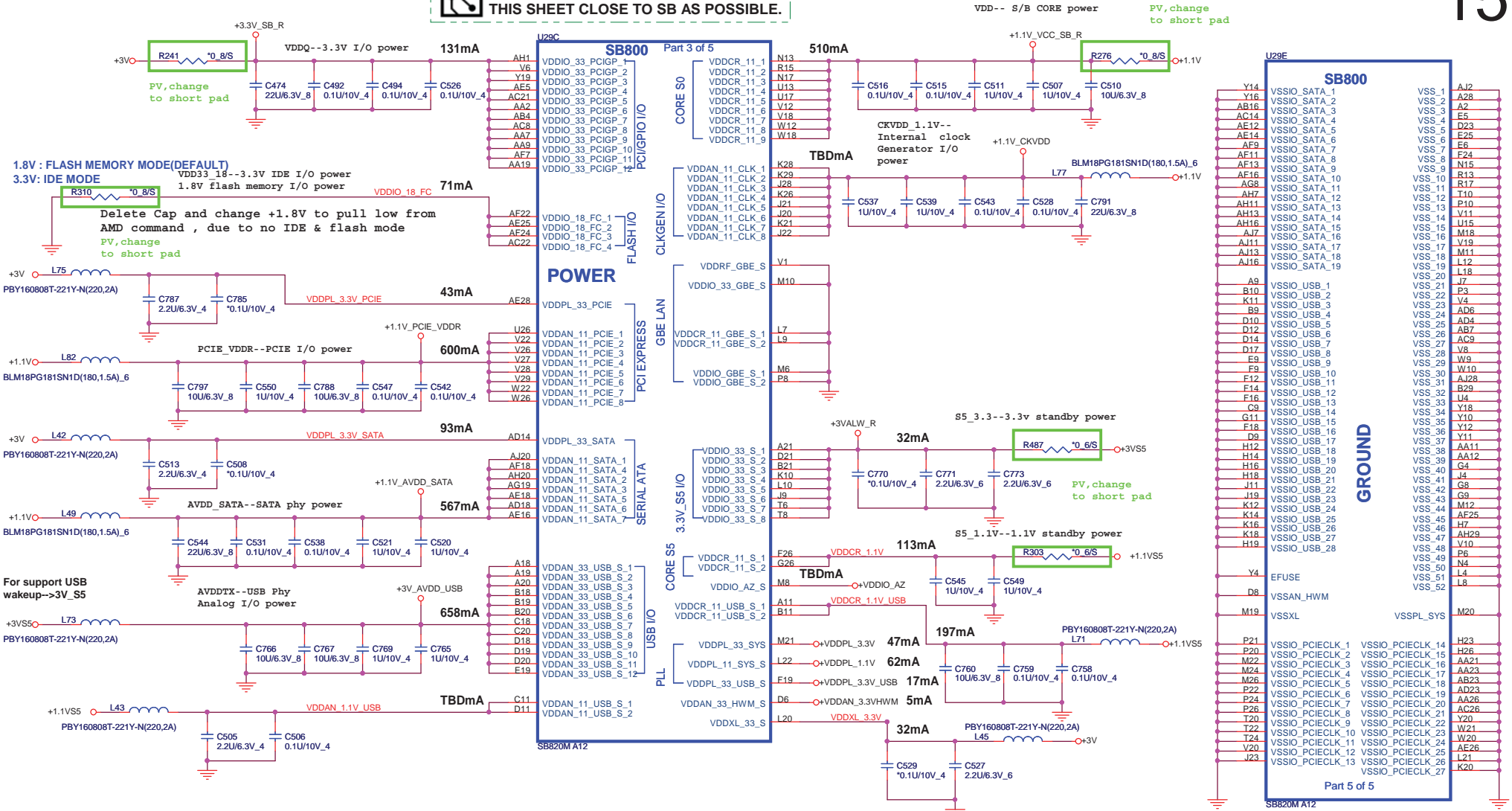
ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF

PV define for M93



PROJECT : AX2/7
Quanta Computer Inc.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
 1.8V flash memory I/O power

Delete Cap and change +1.8V to pull low from AMD command , due to no IDE & flash mode

For support USB wakeup-->3V_S5

To meet SB800 SCL1.02: Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

SI , remove R272 from AMD recommend

SI , remove L48

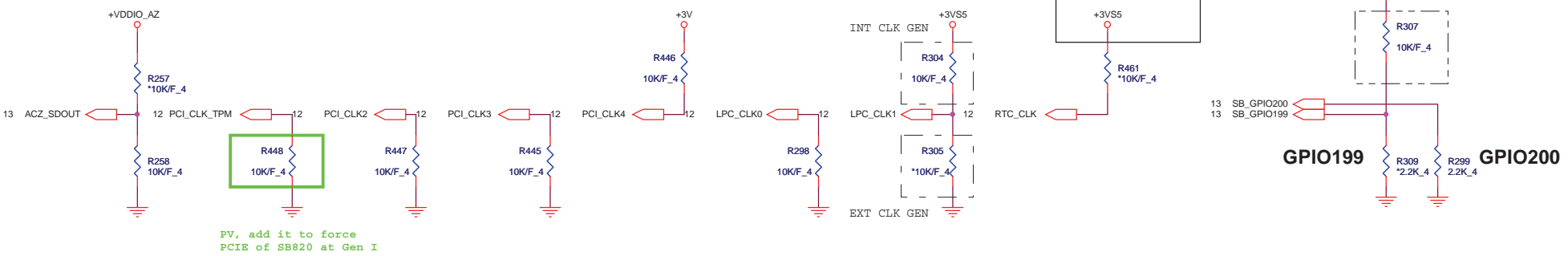


PROJECT : AX2/7
 Quanta Computer Inc.

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



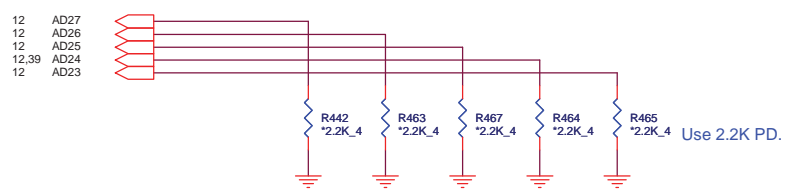
It must ready before RSMRST#

REQUIRED STRAPS

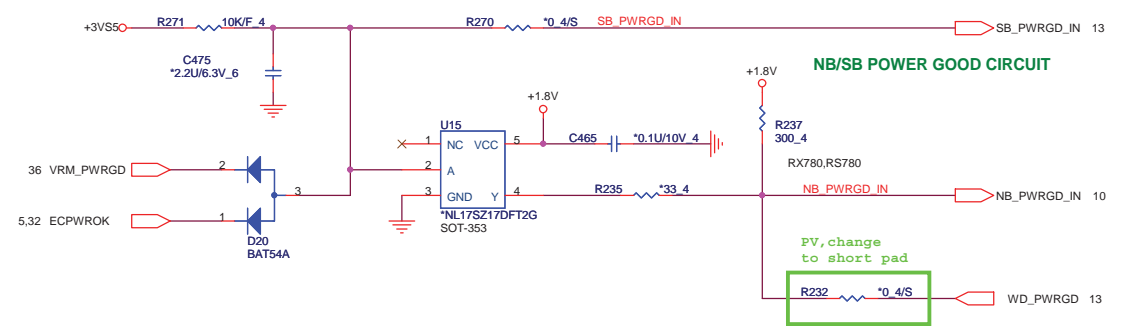
	AZ_SDOOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

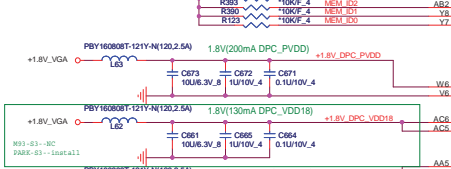
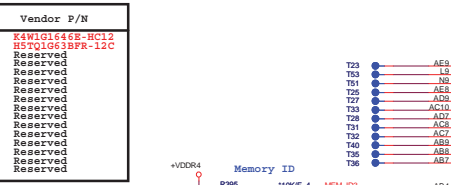
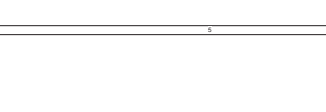
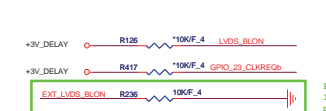
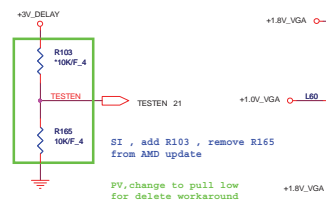
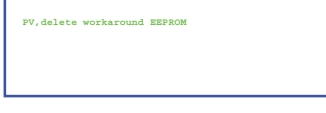
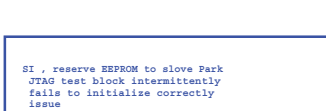
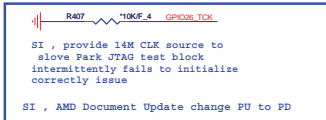
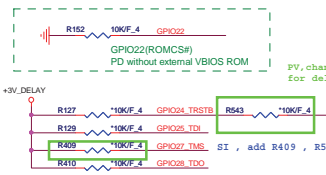
- AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
- ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

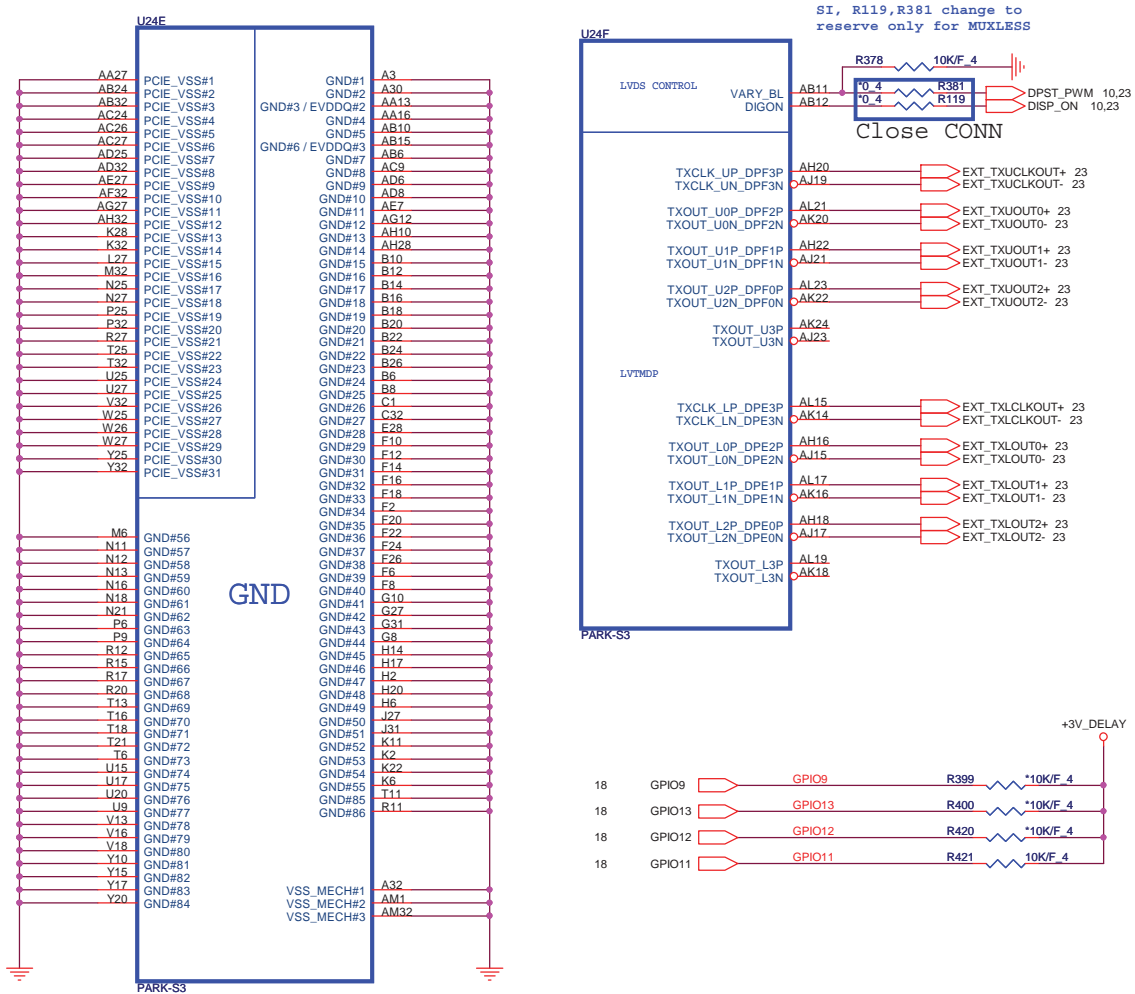
PROJECT : AX2/7
Quanta Computer Inc.

Size: Custom | Document Number: SB820-STRAPS | Rev: 1A
 Date: Thursday, December 24, 2009 | Sheet: 16 of 42

MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	E die	K4WIG1546E-NC12
0001	Bynix	Orion	HF701G638F-11C
0010	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCTRL1	PWRCTRL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V





CONFIGURATION STRAPS

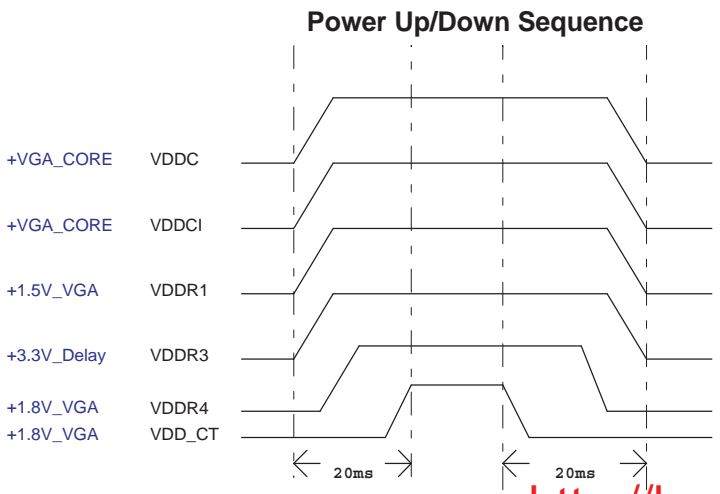
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

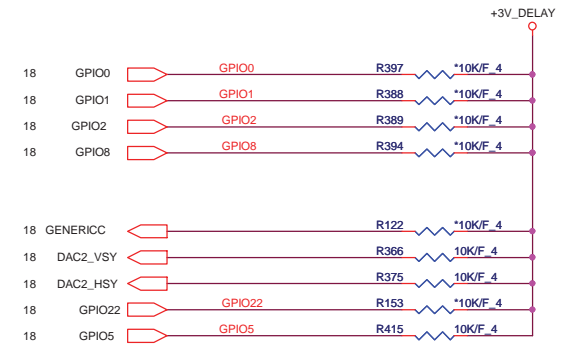
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		



Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

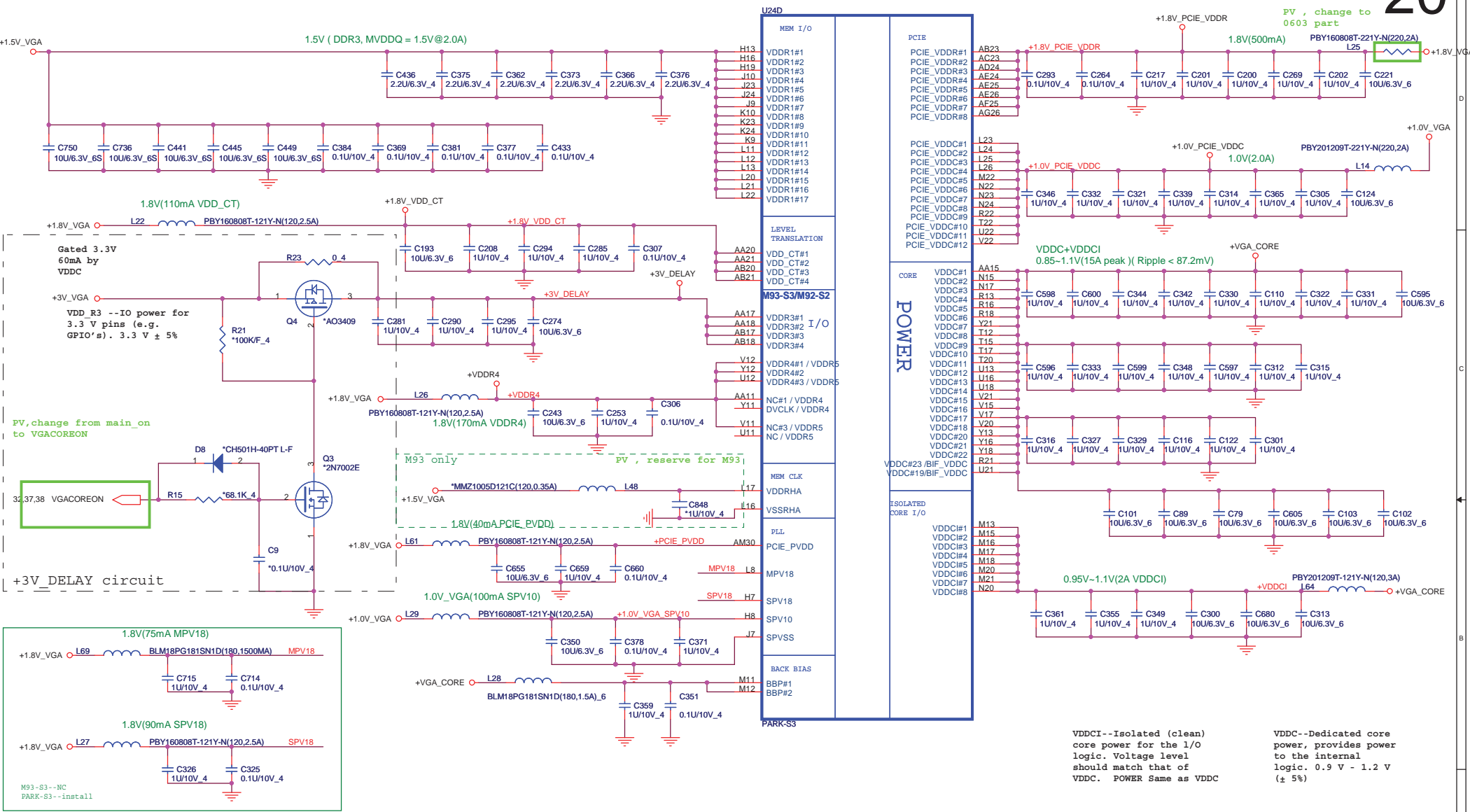


It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

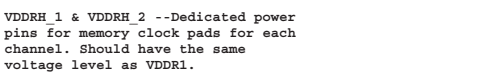
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom | Document Number **PARK_GND / LVDS/ Straps** | Rev 1A

Date: Thursday, December 24, 2009 | Sheet 19 of 42



VDDR1_1 & VDDR2_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.



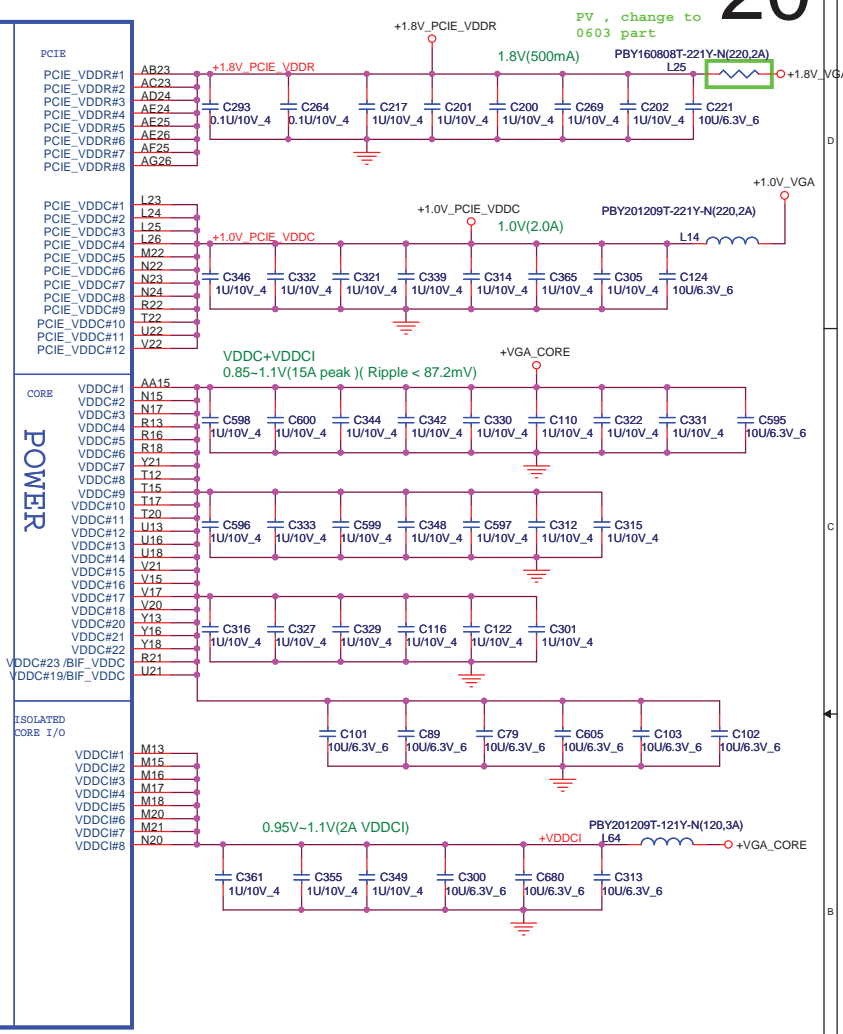
VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

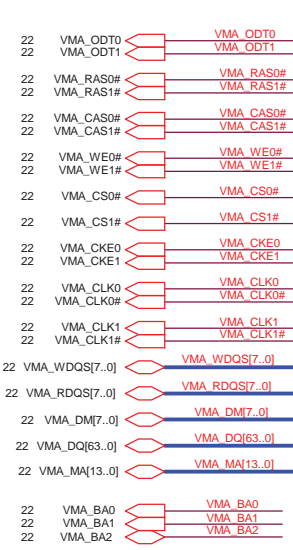
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

MEM I/O	VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17
LEVEL TRANSLATION	VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4 VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4
I/O	VDDR4#1 / VDDR5 VDDR4#2 VDDR4#3 / VDDR5
MEM CLK	VDDRHA VSSRHA
PLL	PCIE_PVDD
MPV18	MPV18
SPV18	SPV18
SPVSS	SPVSS
BACK BIAS	BBP#1 BBP#2
PARK-S3	

POWER

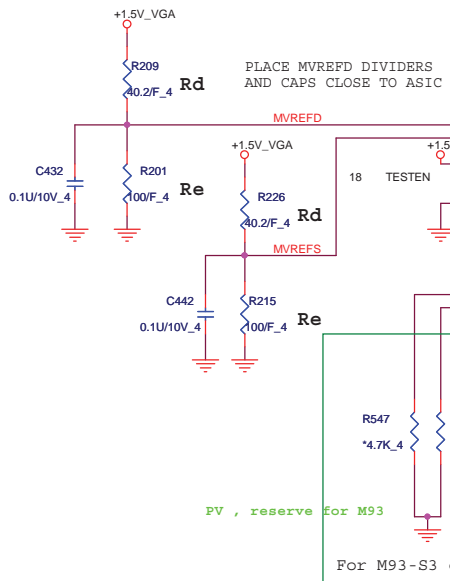


			<p>PROJECT : AX2/7 Quanta Computer Inc.</p>		
Date: Thursday, December 24, 2009			Sheet 20	of 42	

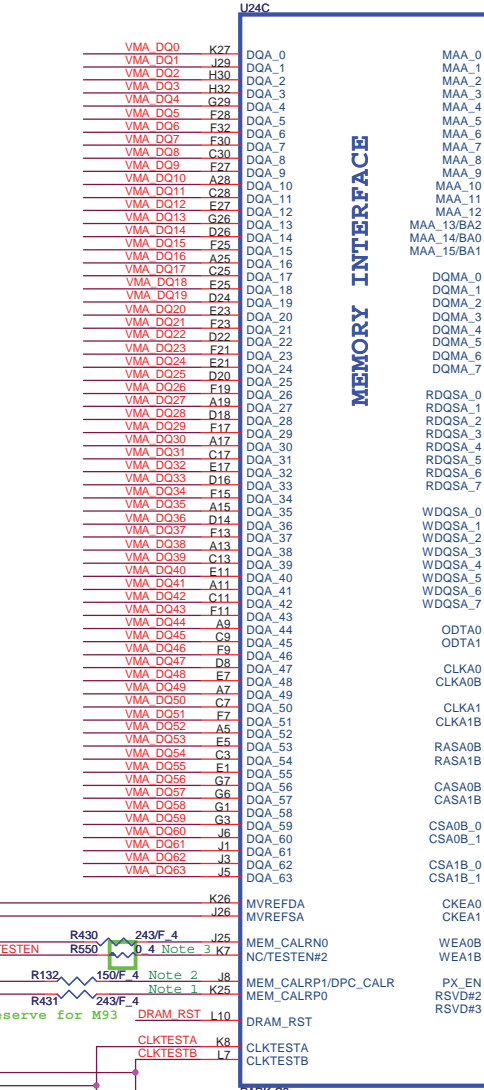


support 1gbt
VRAM (64M X 16)

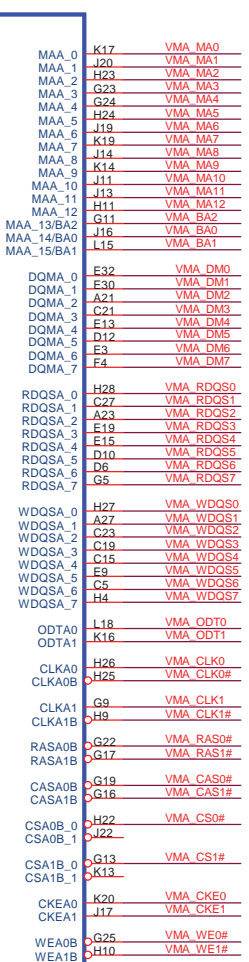
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



PV , reserve for M93
For M93-S3 only

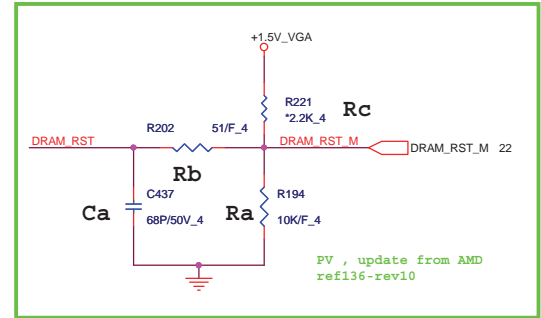


MEMORY INTERFACE

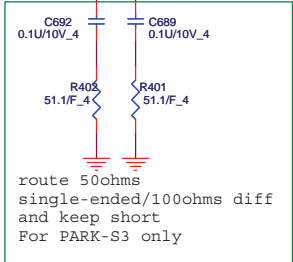


For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.

Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF



PV , update from AMD
ref136-rev10



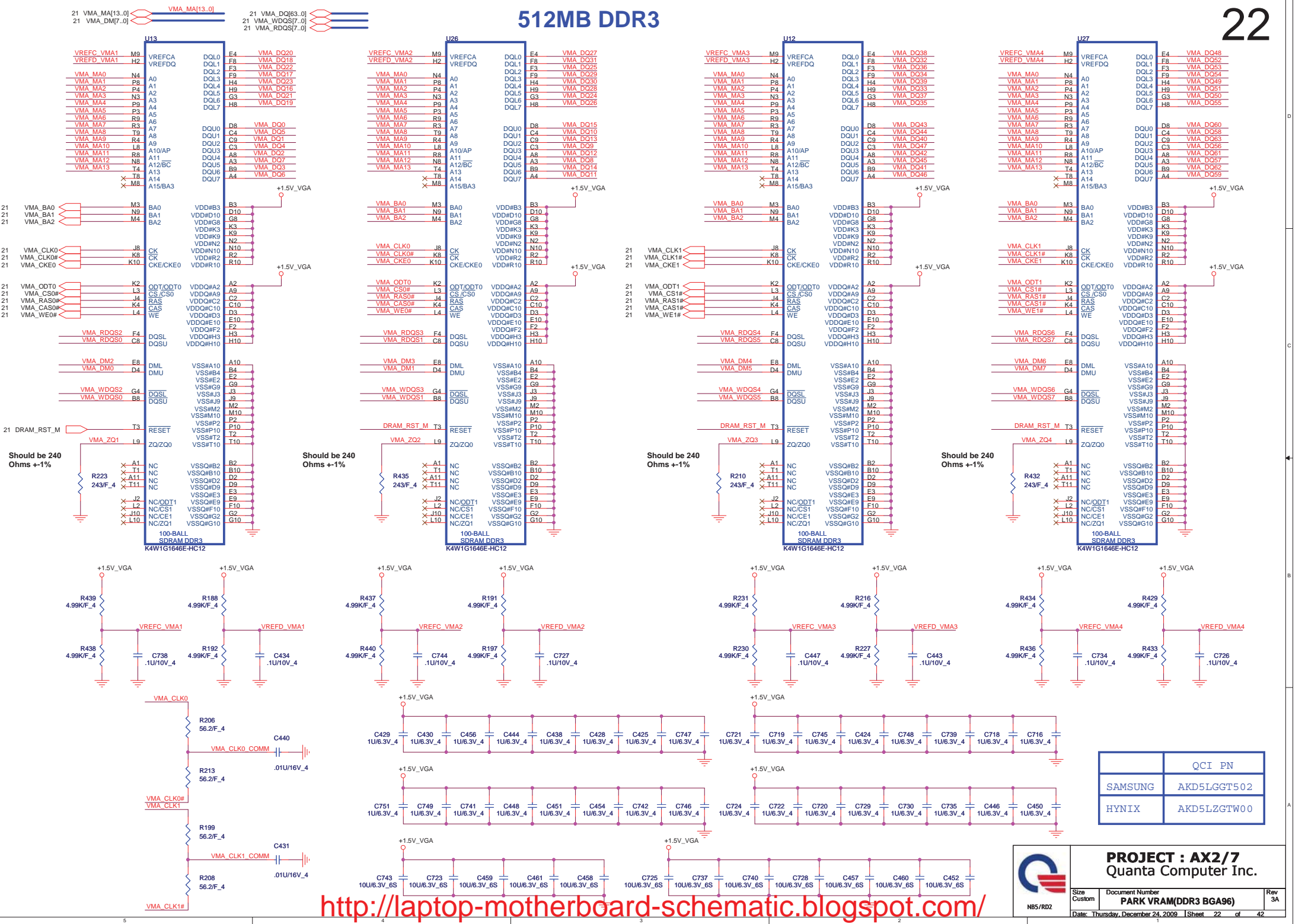
route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3, J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3, J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC MEM_CALR1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number PARK/MEM_Interface	Rev 1A
Date: Thursday, December 24, 2009 Sheet 21 of 42		

512MB DDR3



	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
	PARK VRAM(DDR3 BGA96)	
Date: Thursday, December 24, 2009	Sheet 22	of 42

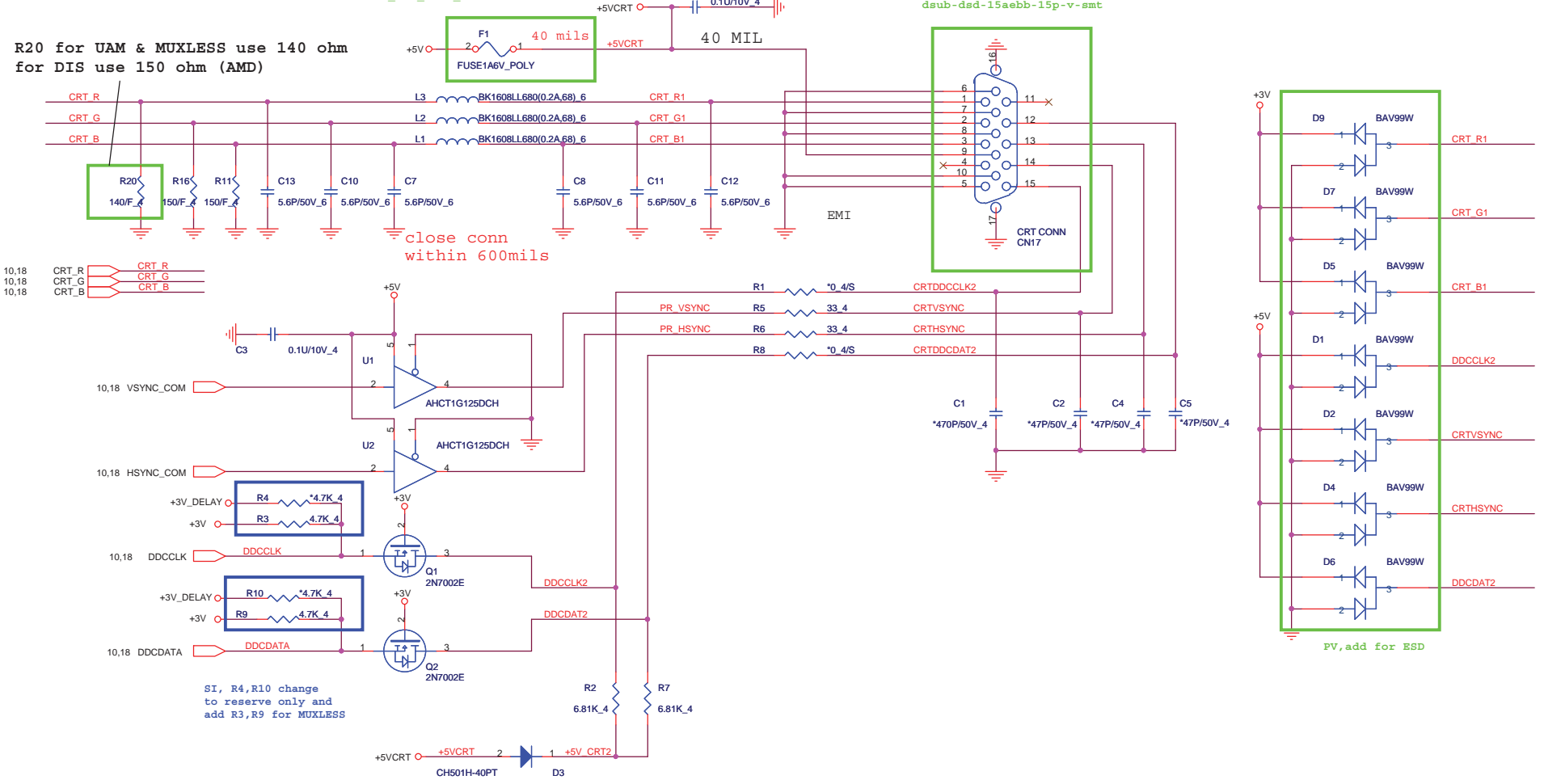
<http://laptop-motherboard-schematic.blogspot.com/>

CRT PORT

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)

PV , change footprint to F3_2X1_65-2_8

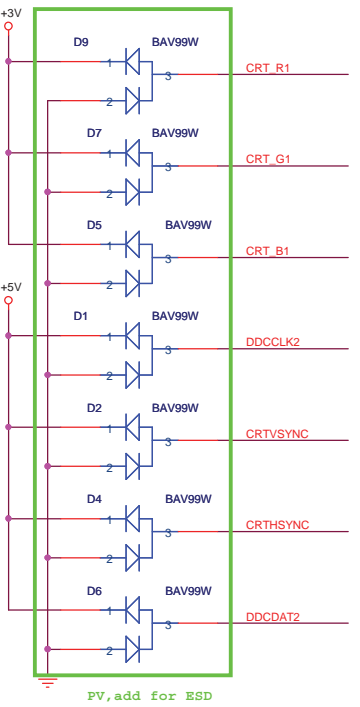
PV , change footprint to dsub-dsd-15aebb-15p-v-smt



close conn within 600mils

- 10,18 CRT_R
- 10,18 CRT_G
- 10,18 CRT_B

SI, R4,R10 change to reserve only and add R3,R9 for MUXLESS

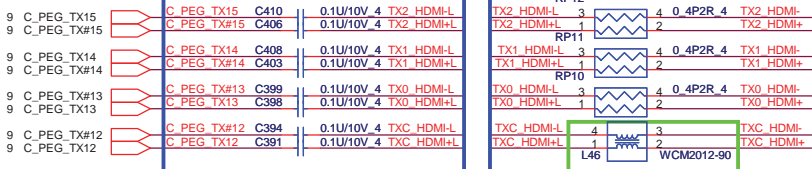


	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom	Document Number CRT
Date: Thursday, December 24, 2009	Sheet 24 of 42	Rev 1A

UMA/DISCRETE select for HDMI

From RS880M

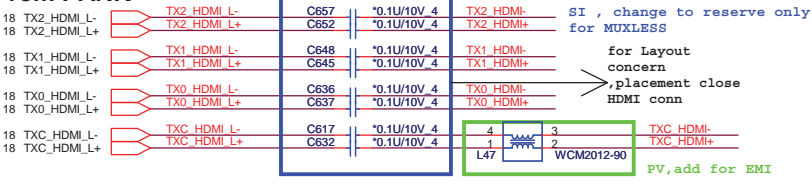
SI, all add for MUXLESS



for Layout concern, placement close north bridge

for Layout concern, placement close HDMI conn

From PARK

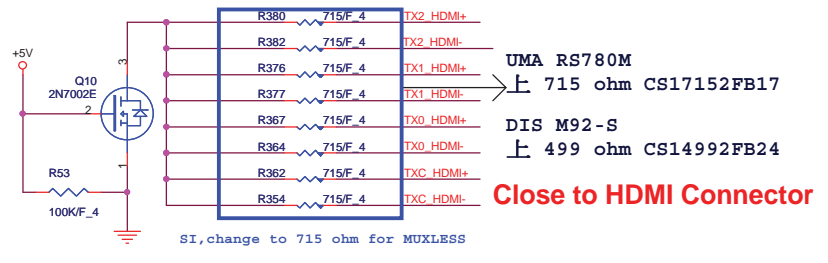


PV, add for EMI

SI, change to reserve only for MUXLESS

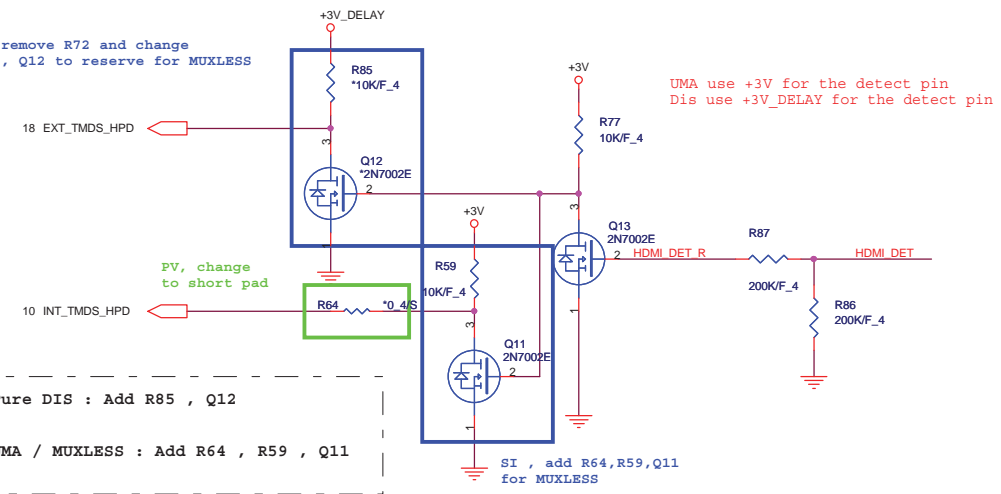
for Layout concern, placement close HDMI conn

PV, add for EMI



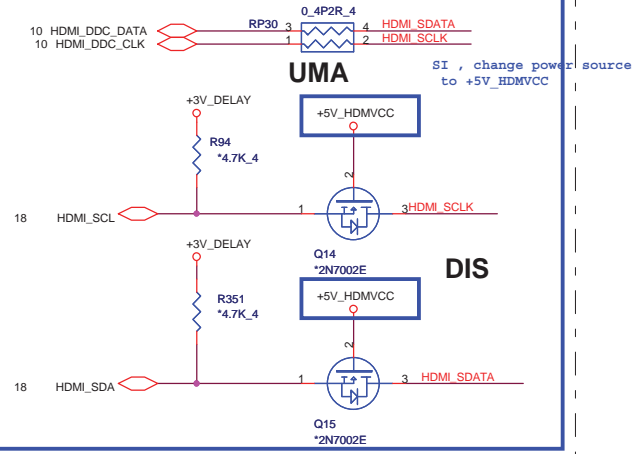
HDMI HPD SENSE

SI, remove R72 and change R85, Q12 to reserve for MUXLESS



UMA AND DISCRETE HDMI I2C SELECT

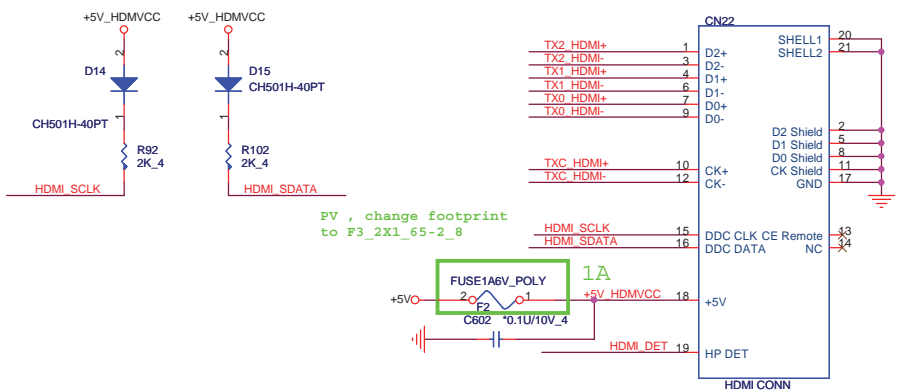
Close to HDMI Connector



UMA DDC4 is 5V tolerance, the MOSFET level shifter no need
Discrete DDC is 3V tolerance, the MOSFET level shifter is need

SI, remove R93, R350. Add RP30
R94, R351, Q14, Q15 change to reserve only for MUXLESS

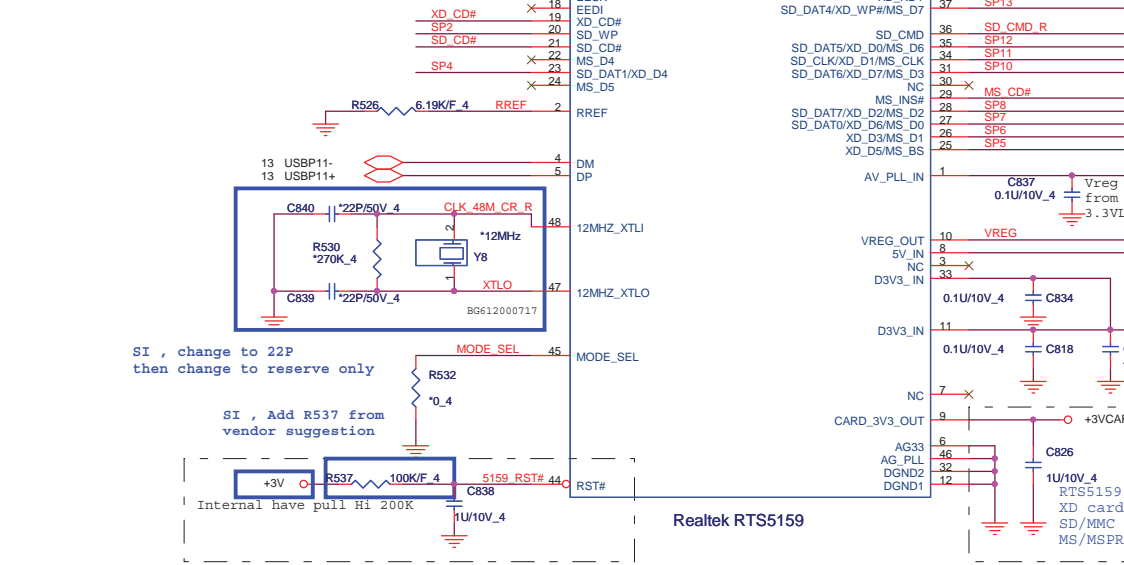
HDMI PORT



PROJECT : AX2/7
Quanta Computer Inc.

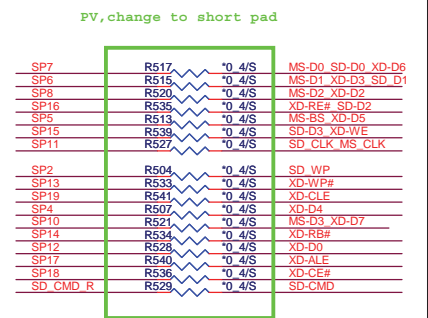
Size Custom	Document Number HDMI	Rev 1A
Date: Thursday, December 24, 2009	Sheet 25	of 42

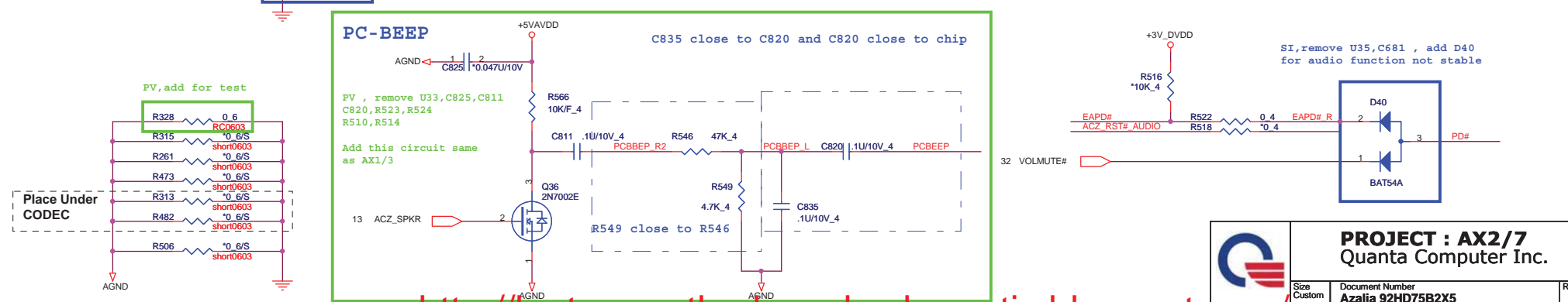
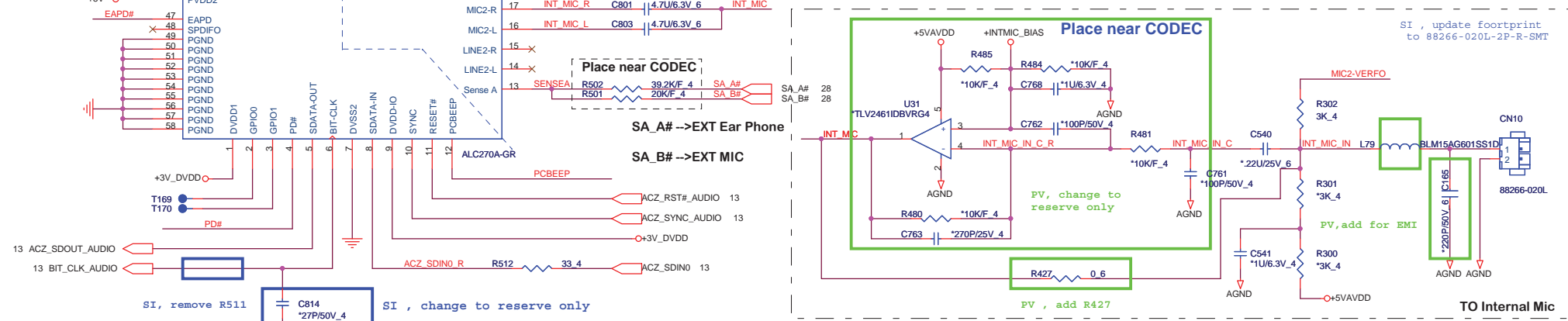
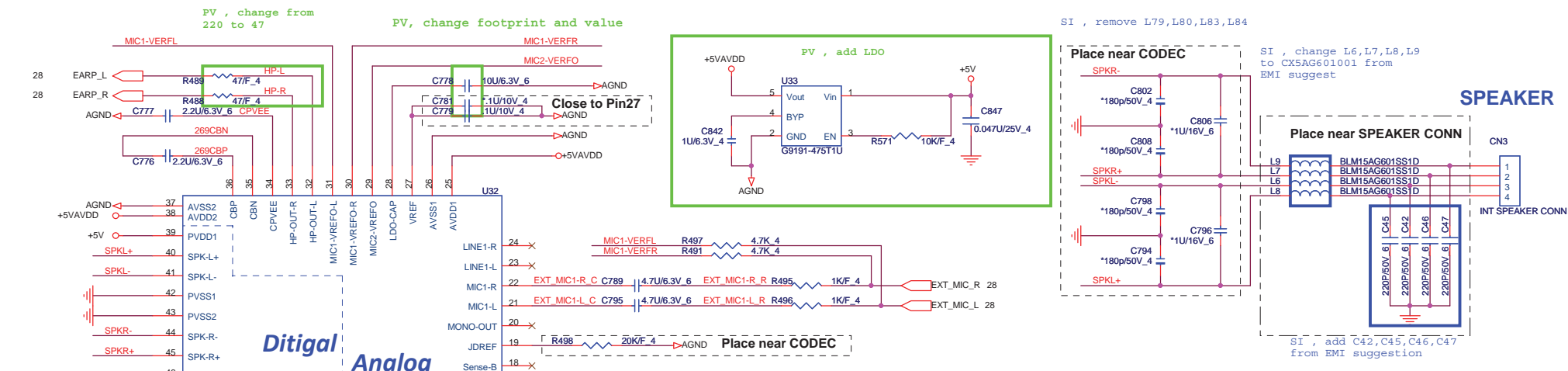
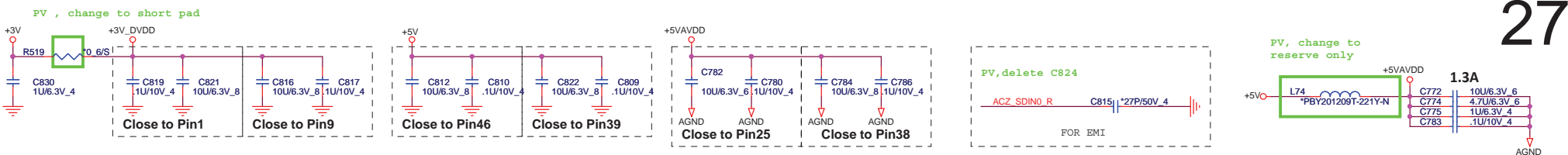
PIN 13	CLK source	Remark
Floating	12M Hz	Xtal
Pull high	48M Hz	Input to RTS5159 pin48



Note:

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5	MS_BS	XD_D5
SP6	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9	MS_INS#	
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D0
SP13	SD_DAT4	XD_WP#
SP14		XD_R/#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE

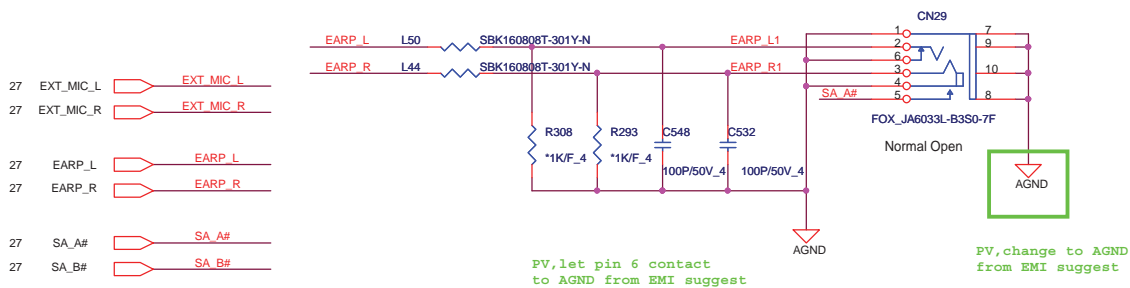




PROJECT : AX2/7
 Quanta Computer Inc.

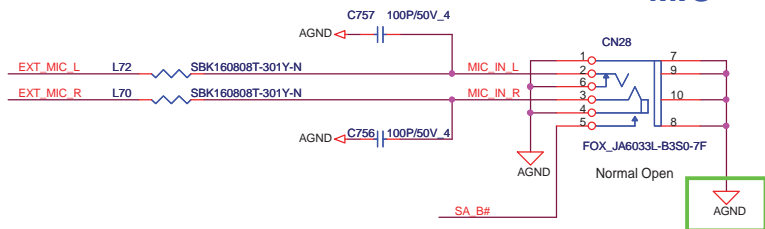
Size Custom	Document Number Azalia 92HD75B2X5	Rev 1A
Date: Thursday, December 24, 2009		Sheet 27 of 42

Line out

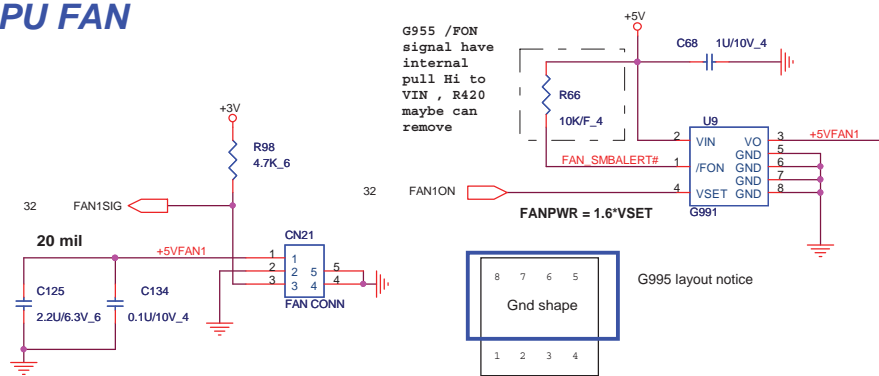


SA_A# -->EXT Ear Phone
SA_B# -->EXT MIC

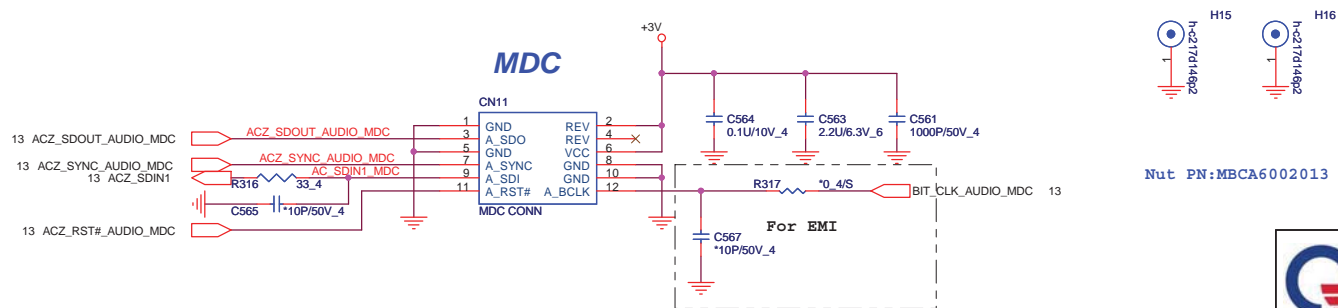
MIC



CPU FAN

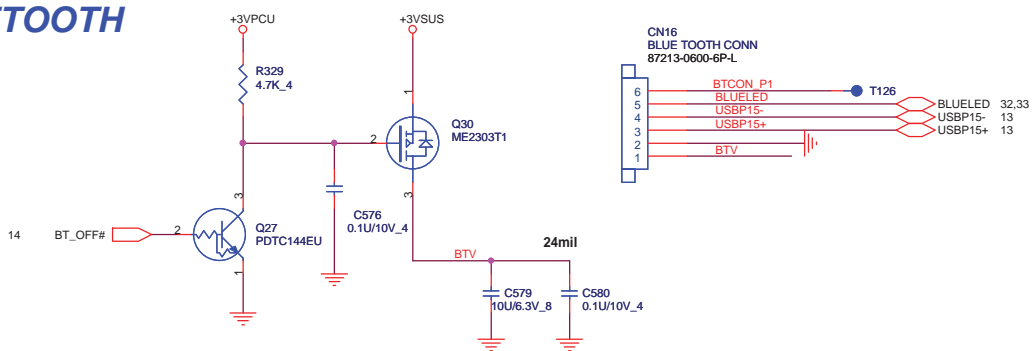


Modem CONN

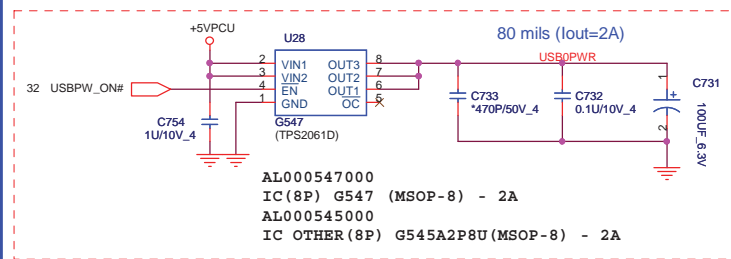


PROJECT : AX2/7 Quanta Computer Inc.		
Size Custom	Document Number AMP_TPA6017/MDC1.5/CPU FAN	Rev 1A
Date: Thursday, December 24, 2009	Sheet 28	of 42

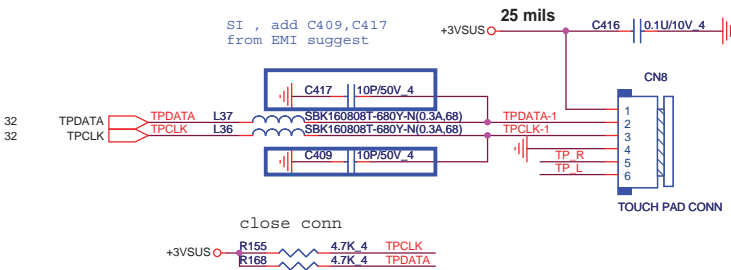
BLUETOOTH



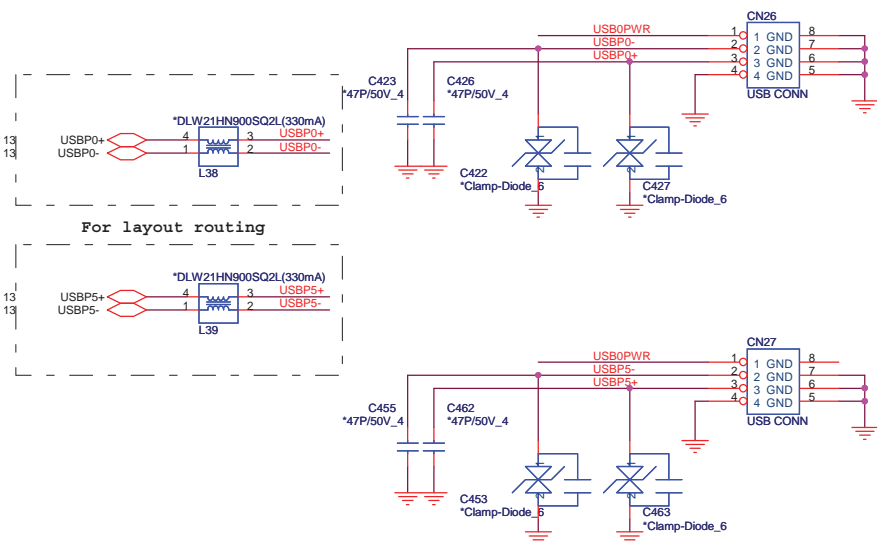
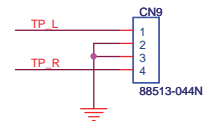
LEFT SIDE USBX2



TOUCH PAD CONN



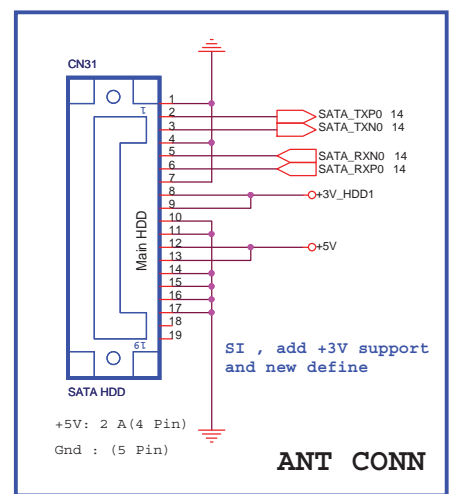
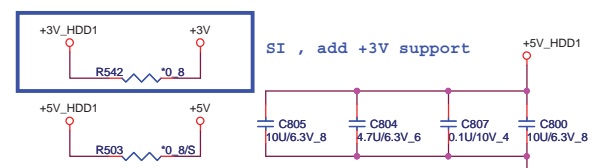
To TOUCH PAD SW board



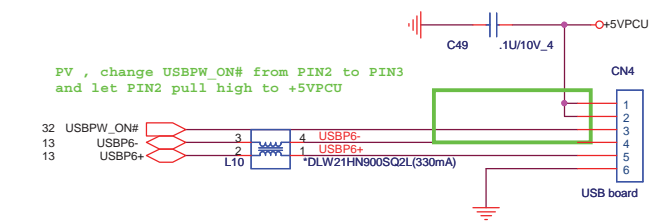
SATA HDD CONNECTOR

SI , update P/N : DFHS13FS019

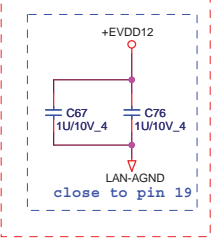
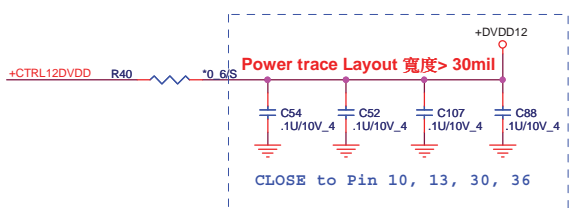
SI , delete CN30 change to ANT CONN



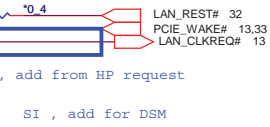
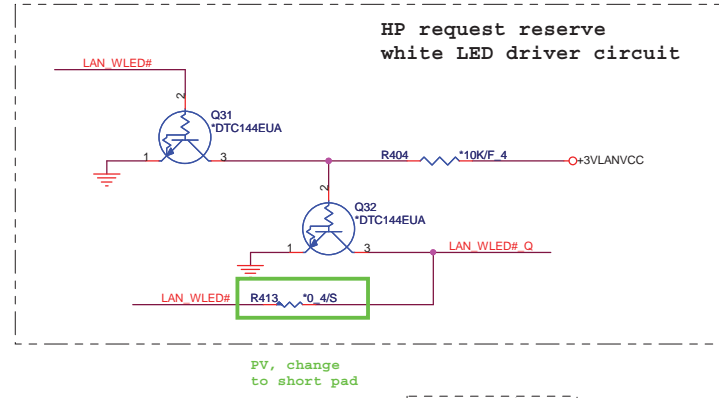
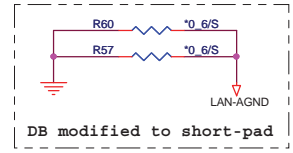
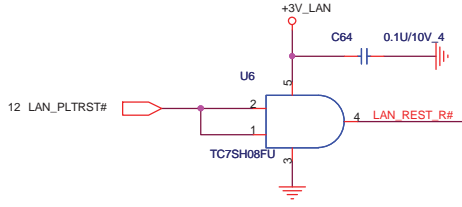
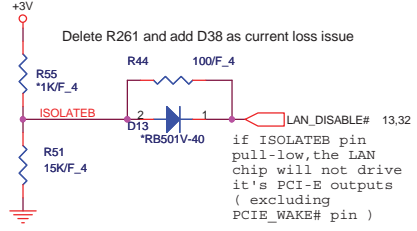
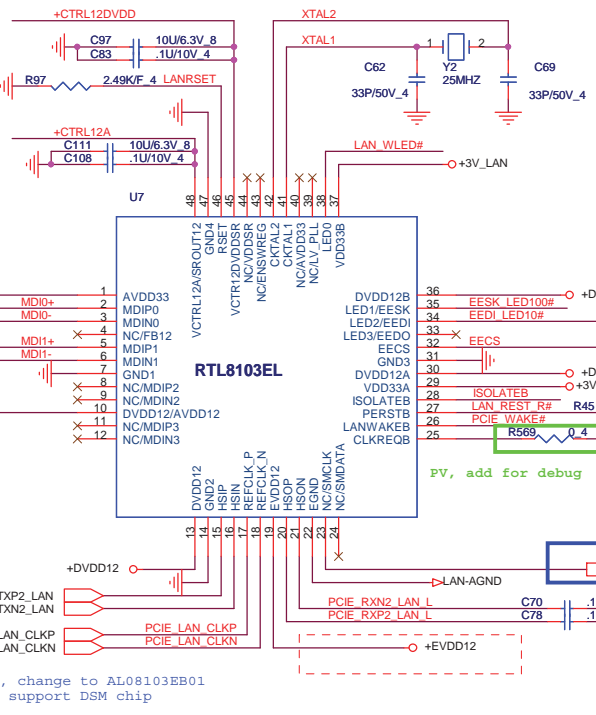
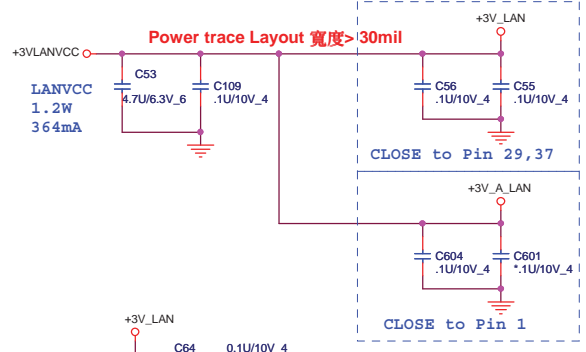
Right SIDE USBX1



			PROJECT : AX2/7	
			Quanta Computer Inc.	
Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A		
Date: Thursday, December 24, 2009		Sheet 29	of 42	



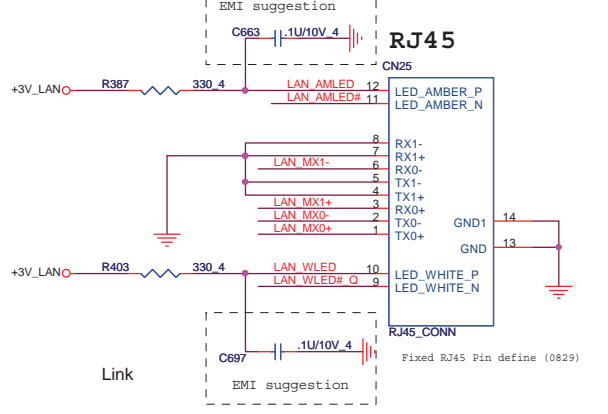
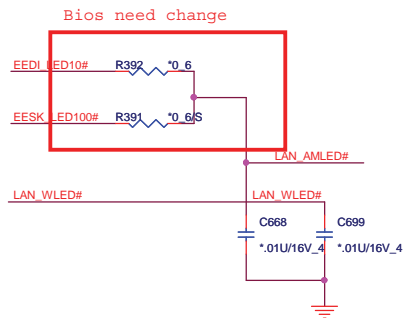
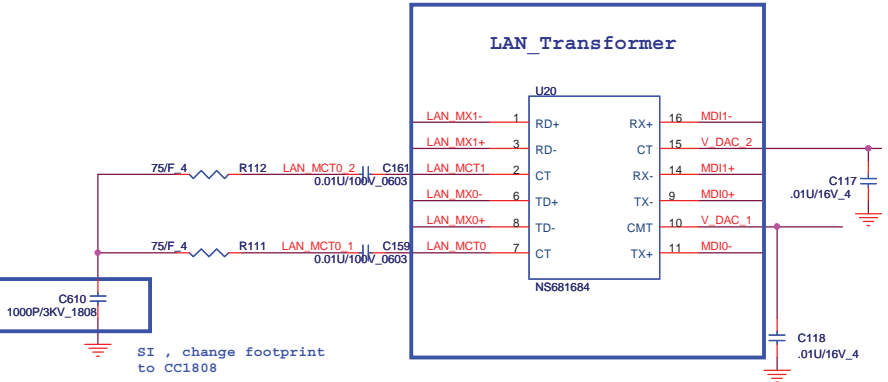
SI , remove EEPROM U5, C48, R42, R50



SI , change to AL08103EB01 for support DSM chip

SI , rotate 180 degree for EMI suggestion

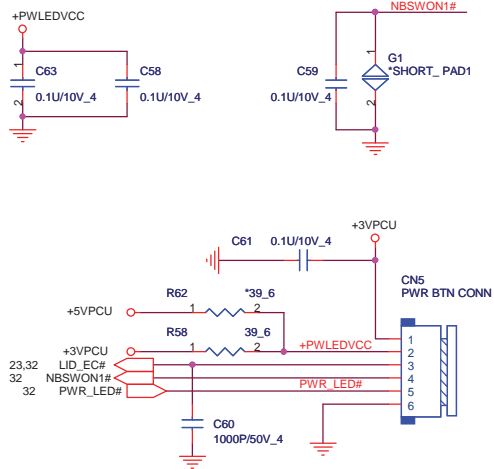
Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx Rs 00 01 10 11
LED1	O	56	35	LED1 LNK100 LNK LNK LNK100
LED2	O	55	34	LED2 LNK10 FULL Rs LNK10
LED3	O	54	33	LED3 NA NA NA NA



PROJECT : AX2/7
 Quanta Computer Inc.

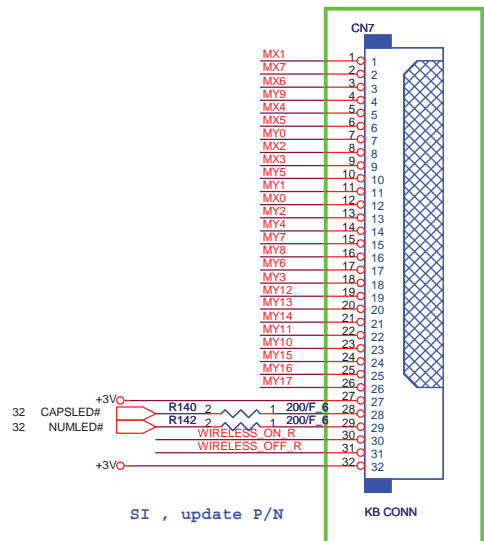
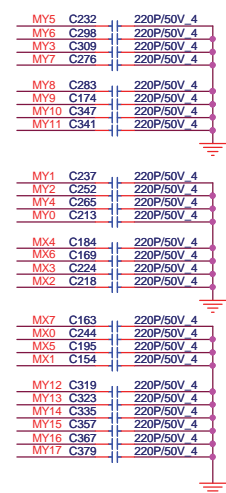
Size Custom	Document Number RTL8102EL/RJ45	Rev 1A
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POWER BUTTON CONNECTOR

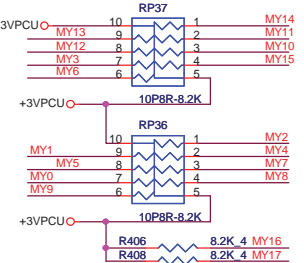


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

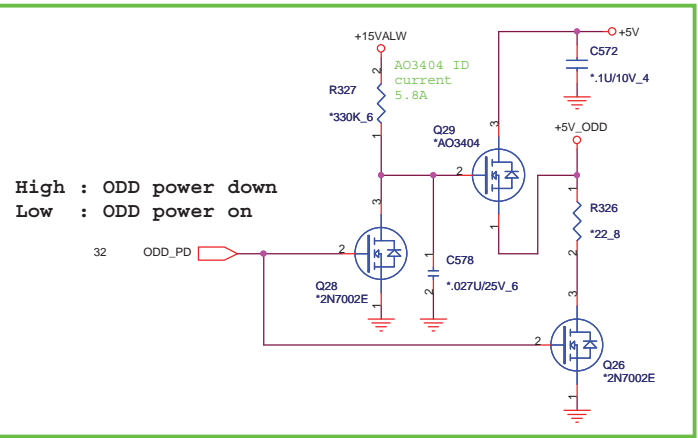
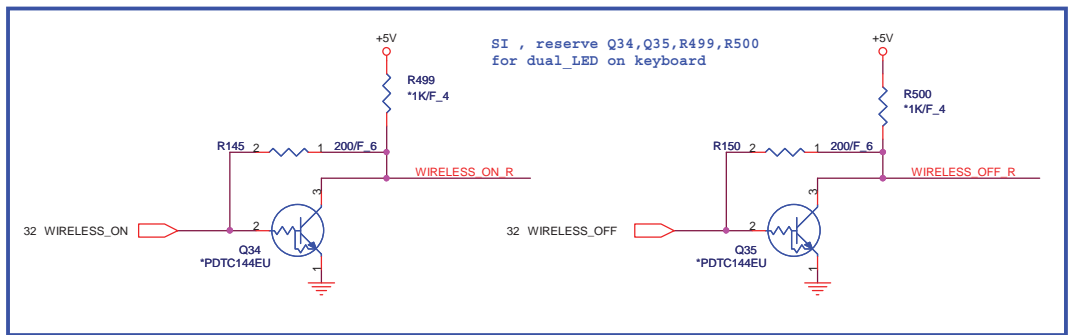
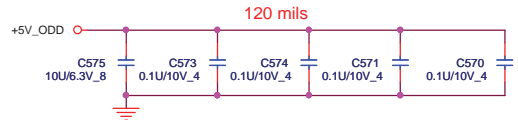
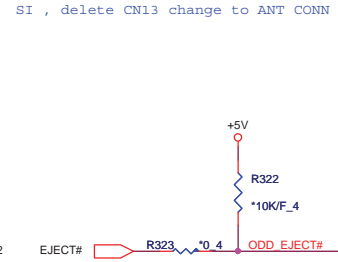
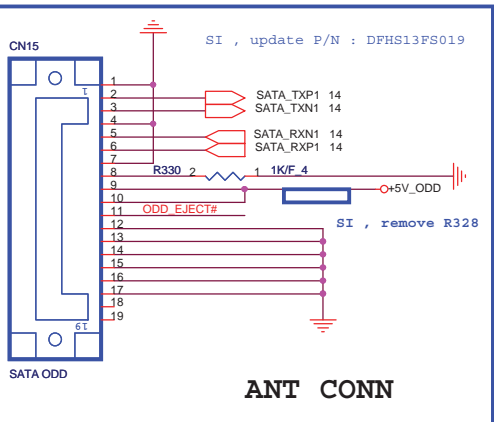
KEYBOARD CONN



KEYBOARD PULL-UP



SATA CD-ROM

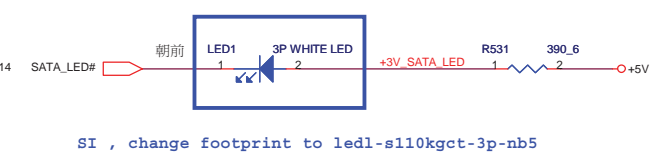
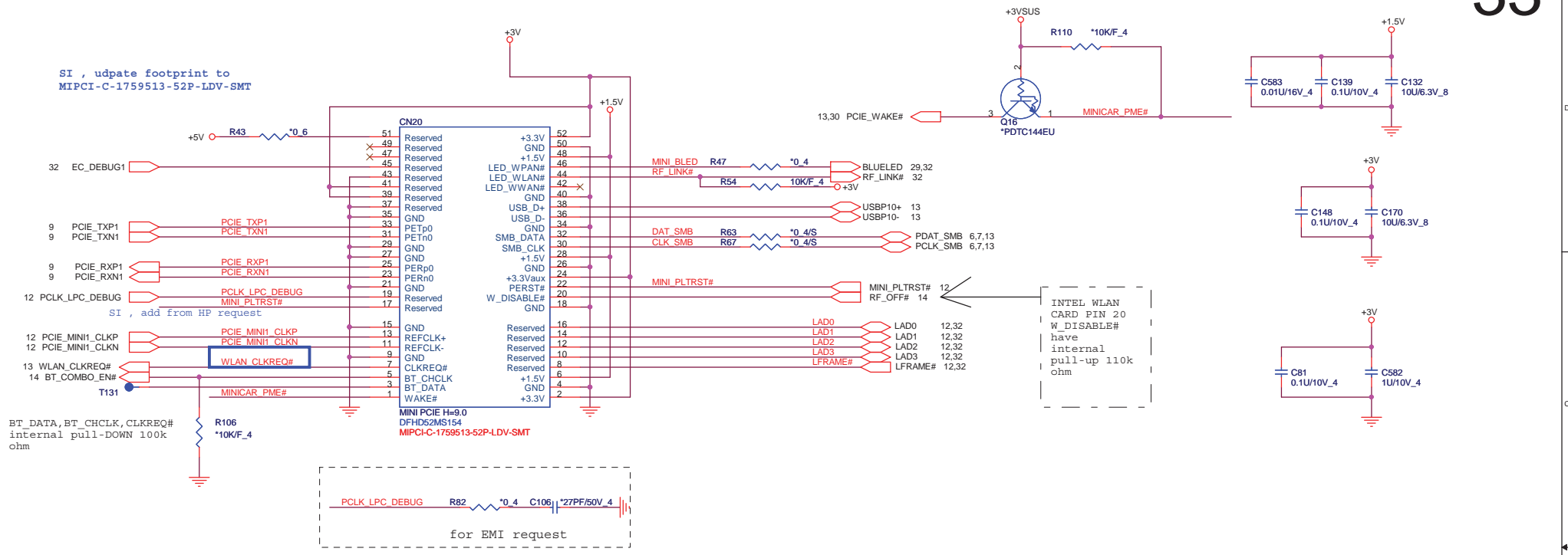


PV, change to reserve only



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Quanta Computer Inc.		
Size Custom	Document Number KEYBOARD_SW_BOARD/ODD	Rev 1A
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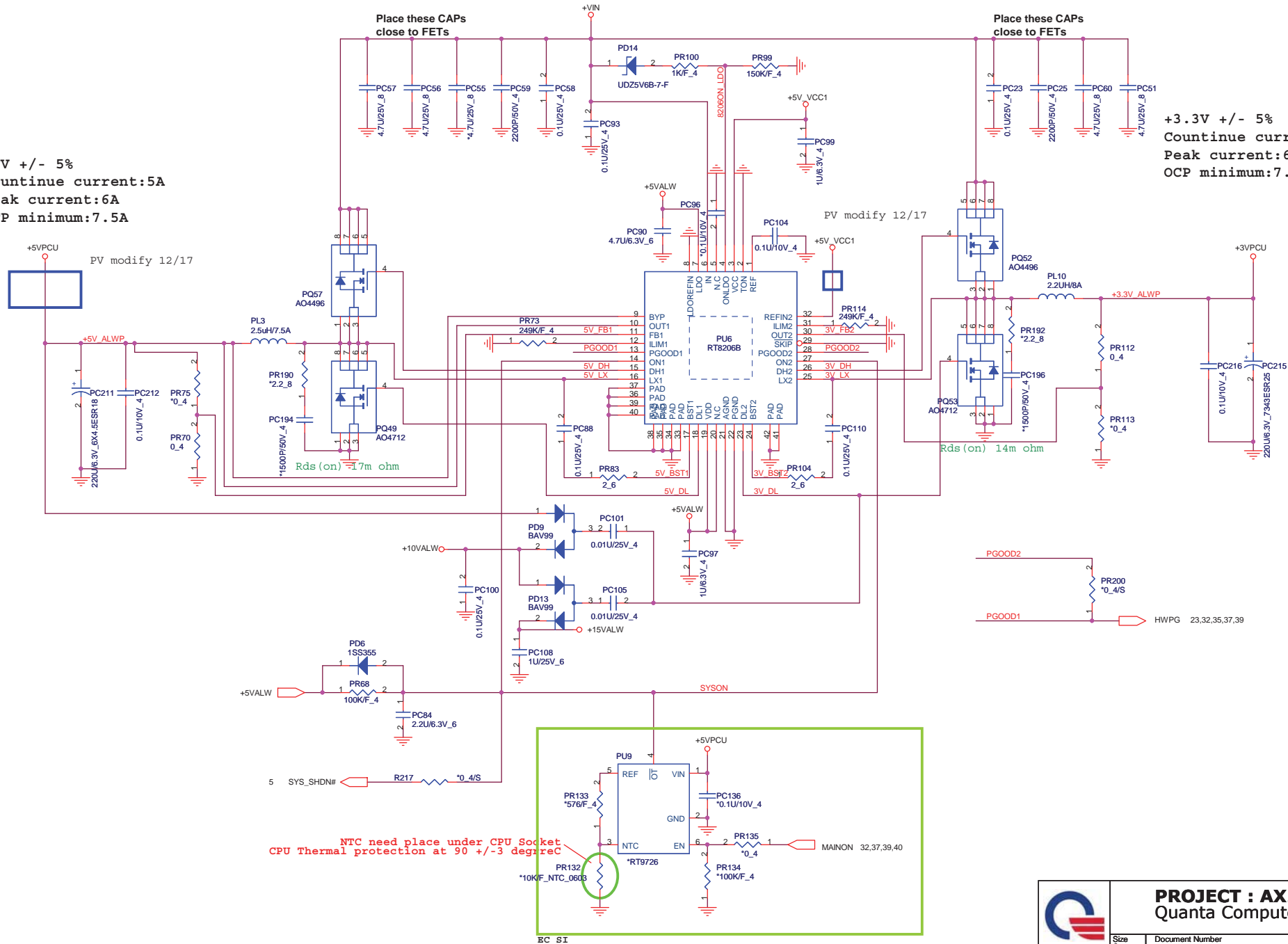
Mini PCI-E Card 1 WLAN



PROJECT : AX2/7 Quanta Computer Inc.		
Size Custom	Document Number Mini CARD/LED	Rev 1A
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+5V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum:7.5A

+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum:7.5A

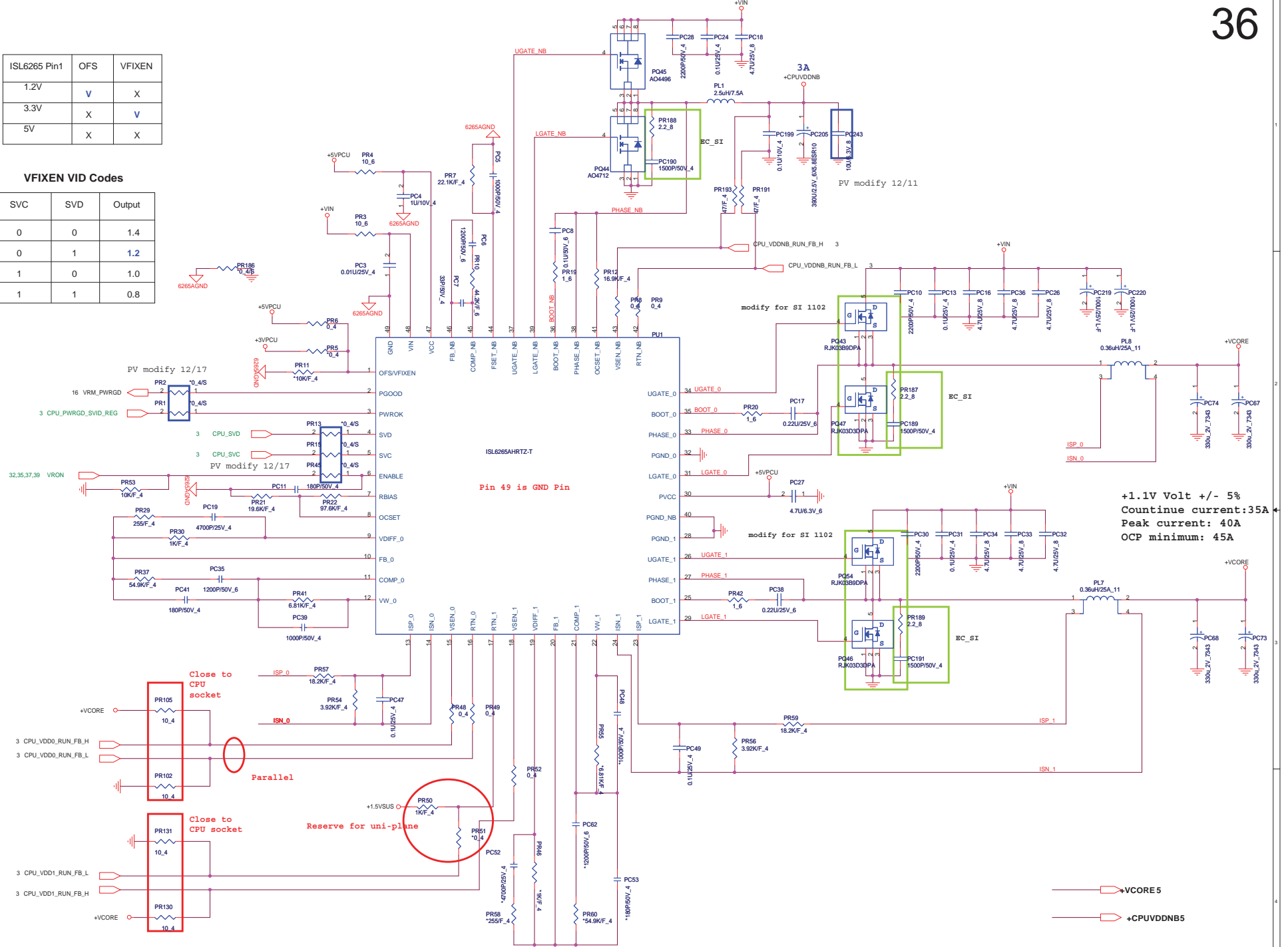


	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom Document Number +5V/+3V (RT8206B) Date: Thursday, December 24, 2009 Sheet 34 of 42	Rev 1A

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

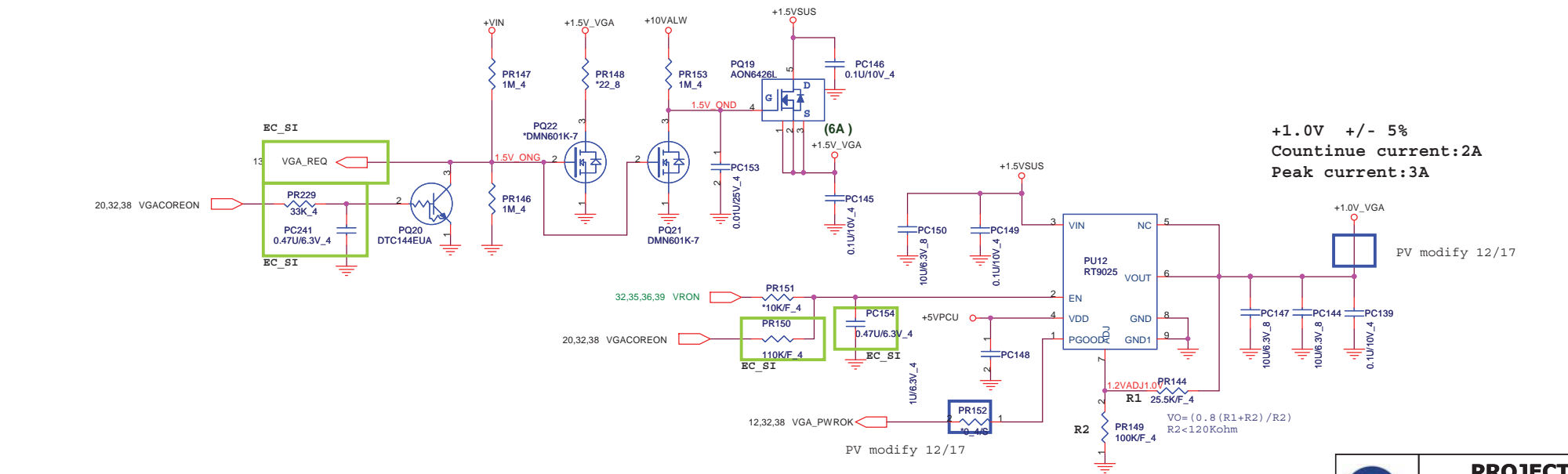
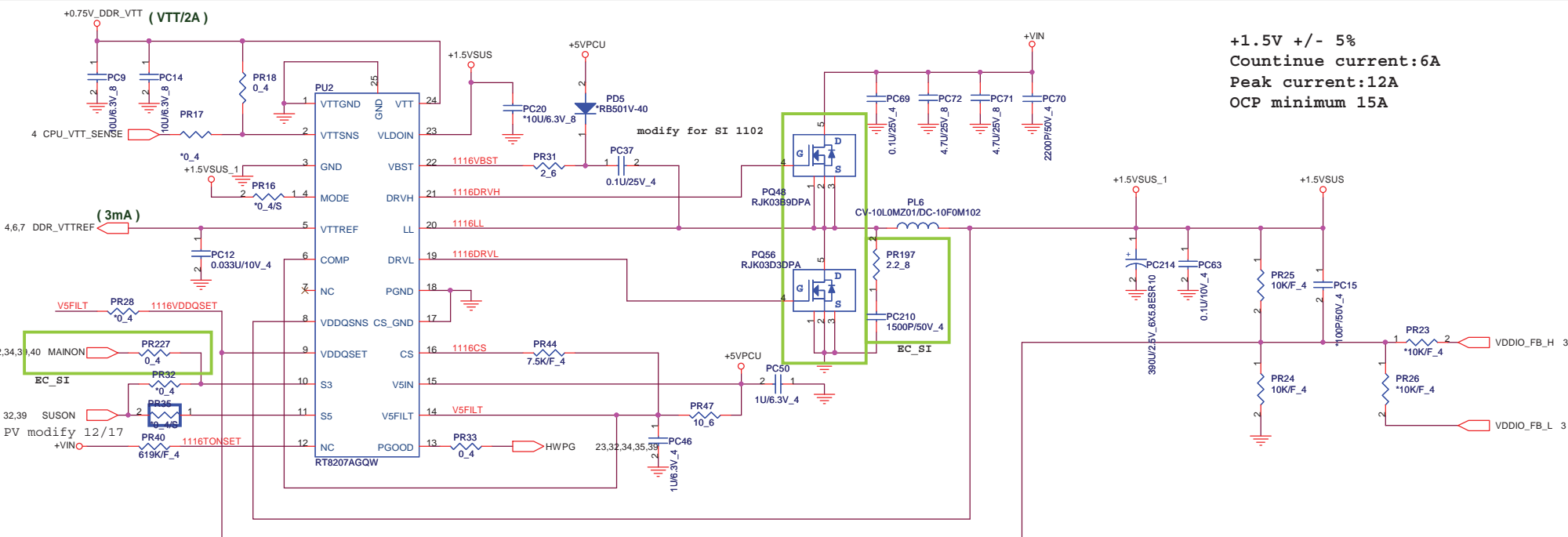
VFIXEN VID Codes


SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



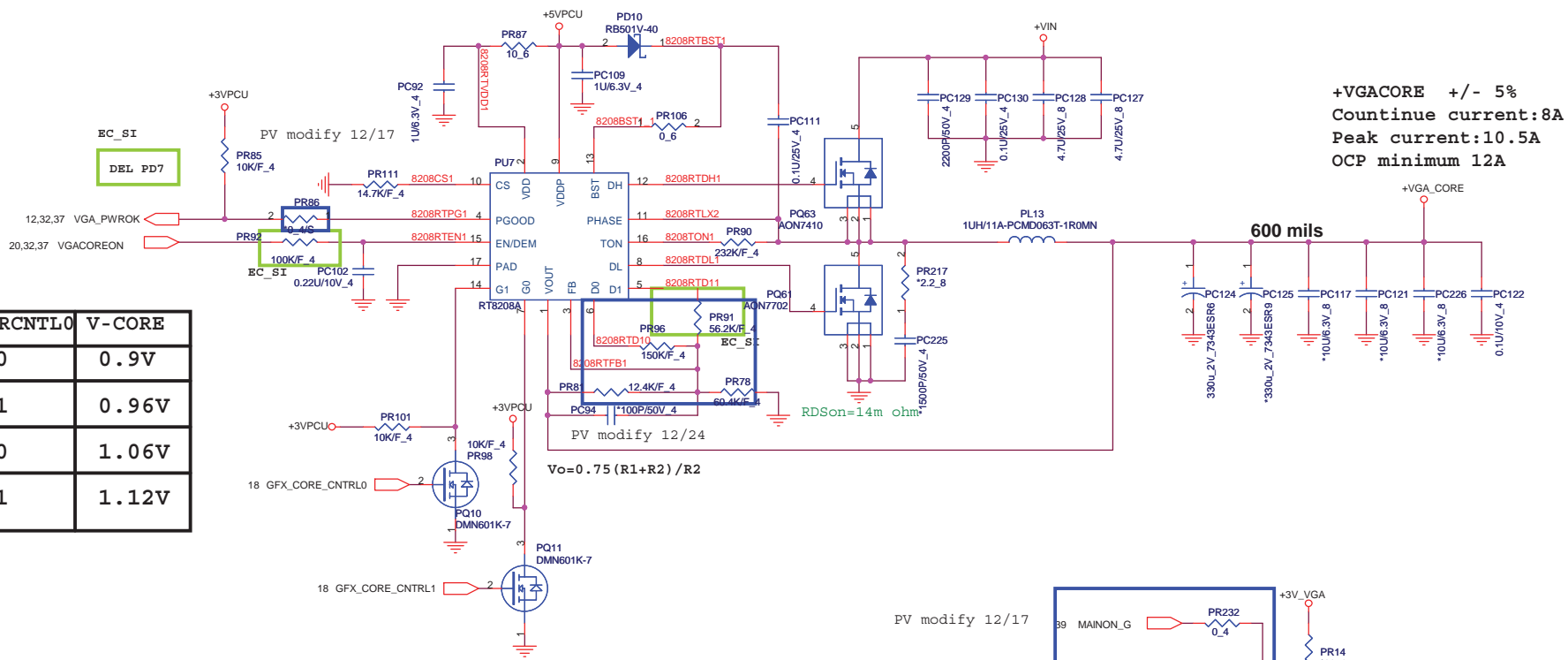
+1.1V Volt +/- 5%
 Continue current: 35A
 Peak current: 40A
 OCP minimum: 45A

	PROJECT : AX2/7 Quanta Computer Inc.	
	Size C Document Number CPU_CORE(ISL6265)	Date: Thursday, December 24, 2009 Sheet 36 of 42



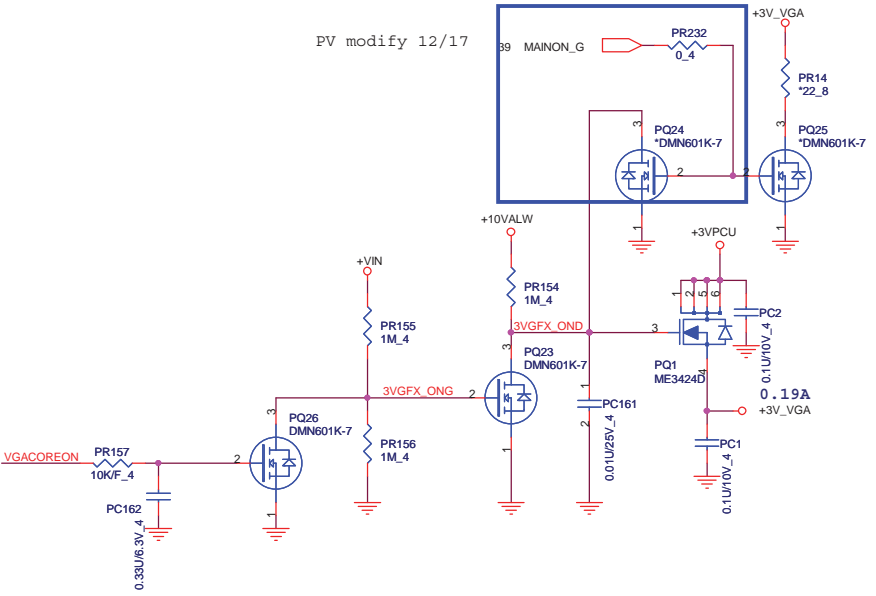
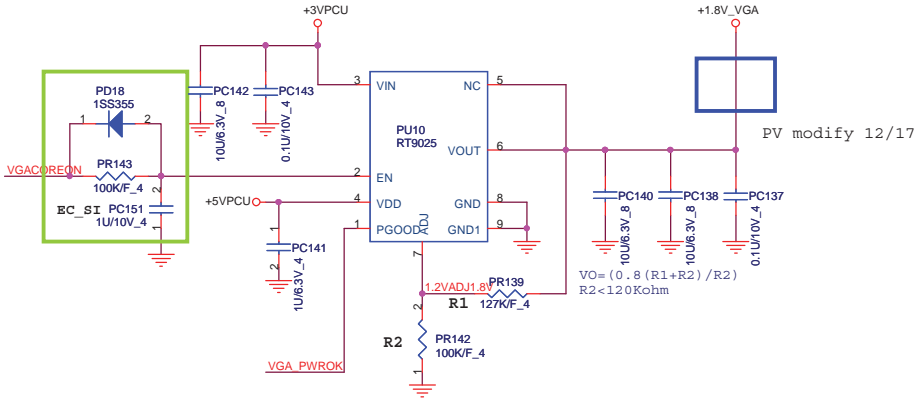
	PROJECT : AX2/7 Quanta Computer Inc. SANTOS INTEL	
	Size NB5/RD2	Document Number DDR3 (RT8207)
Date: Thursday, December 24, 2009 Sheet 37 of 42		

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V



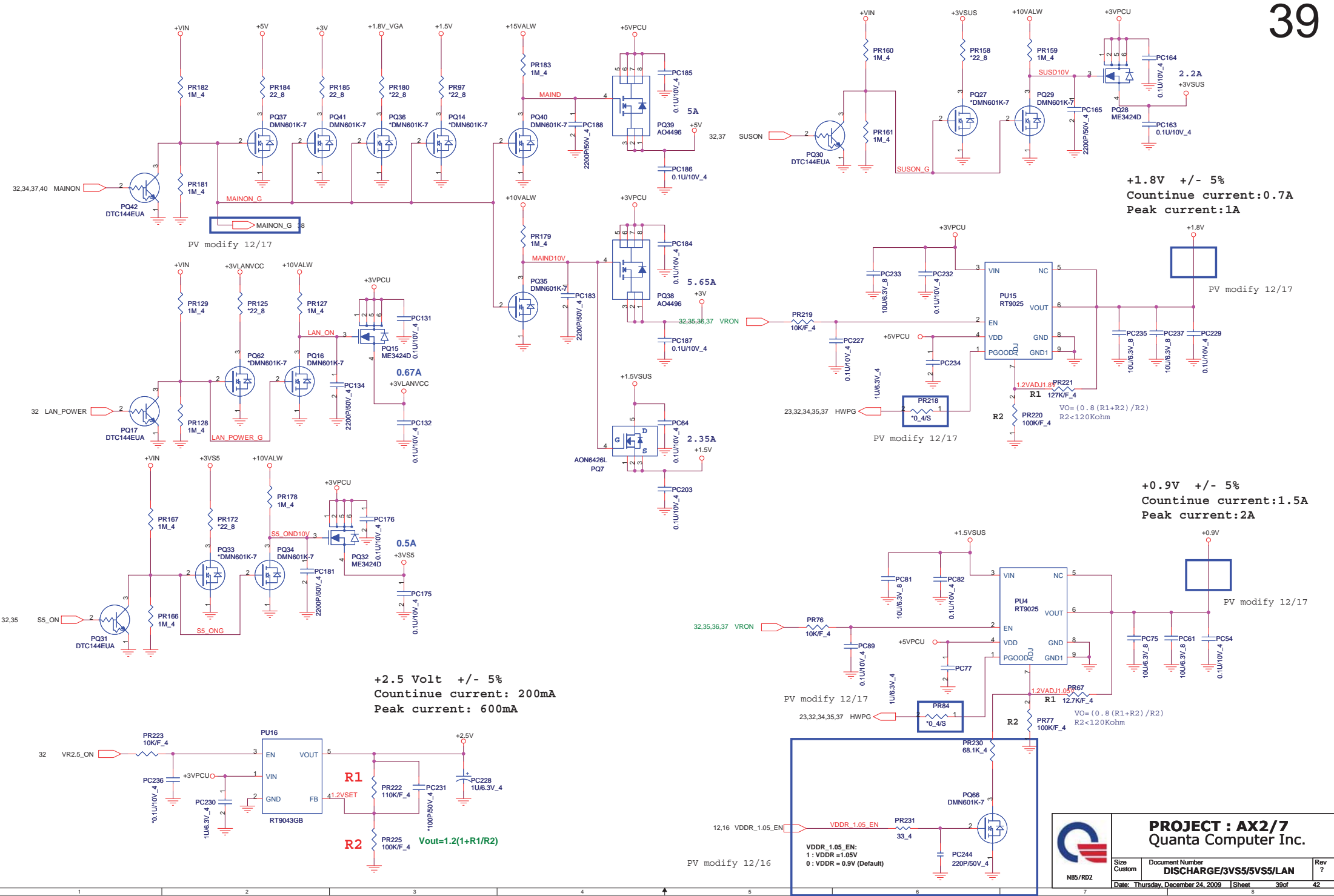
+VGA CORE +/- 5%
Continue current: 8A
Peak current: 10.5A
OCV minimum 12A

+1.8V +/- 5%
Continue current: 1.2A
Peak current: 3A



PROJECT : AX2/7
Quanta Computer Inc.

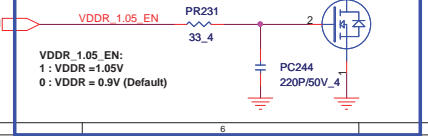
Size Custom	Document Number +VGA CORE (RT8208/1.8V)	Rev 1A
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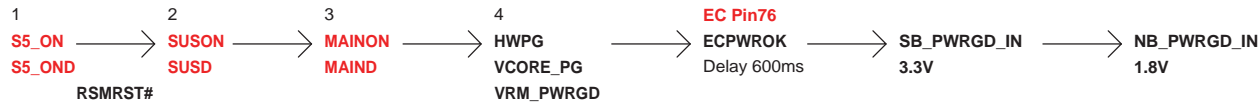
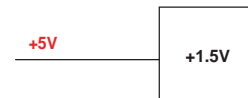
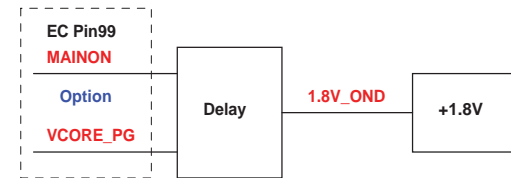
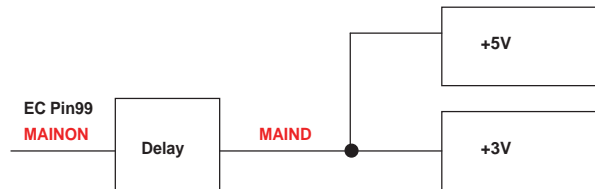
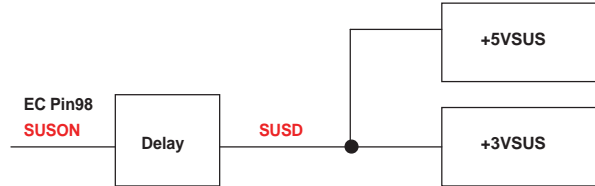
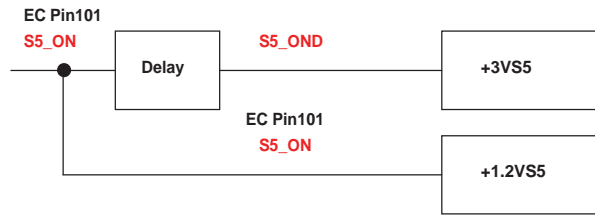
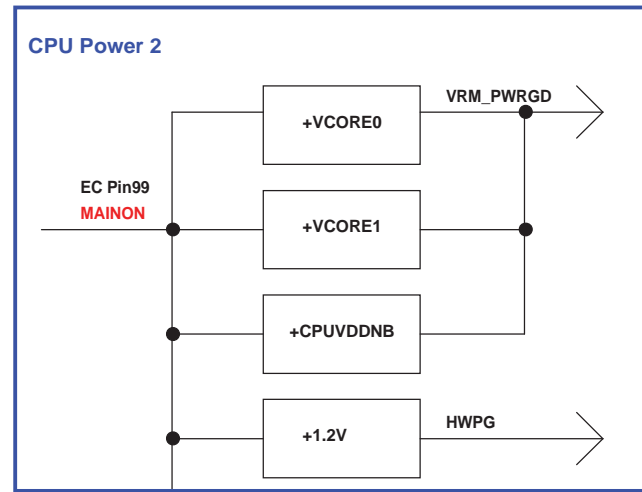
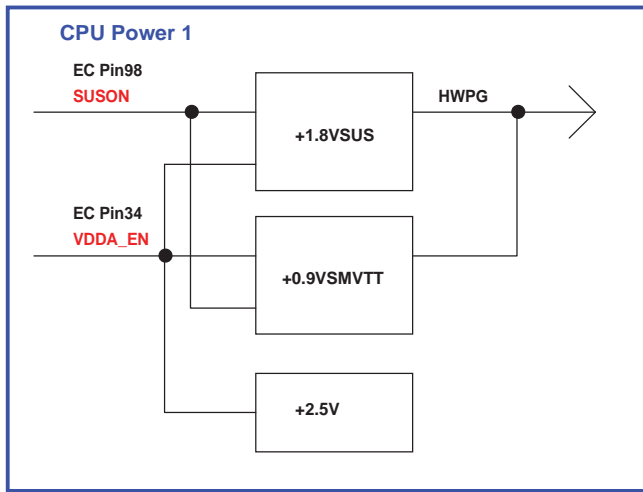
+1.8V +/- 5%
 Countinue current:0.7A
 Peak current:1A

+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

+2.5 Volt +/- 5%
 Countinue current: 200mA
 Peak current: 600mA



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NBS/RD2		Date: Thursday, December 24, 2009	Sheet 39 of 42



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



PROJECT : AX2/7
Quanta Computer Inc.

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