P. Leader	Check by	Design by

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Title: **Index Page**

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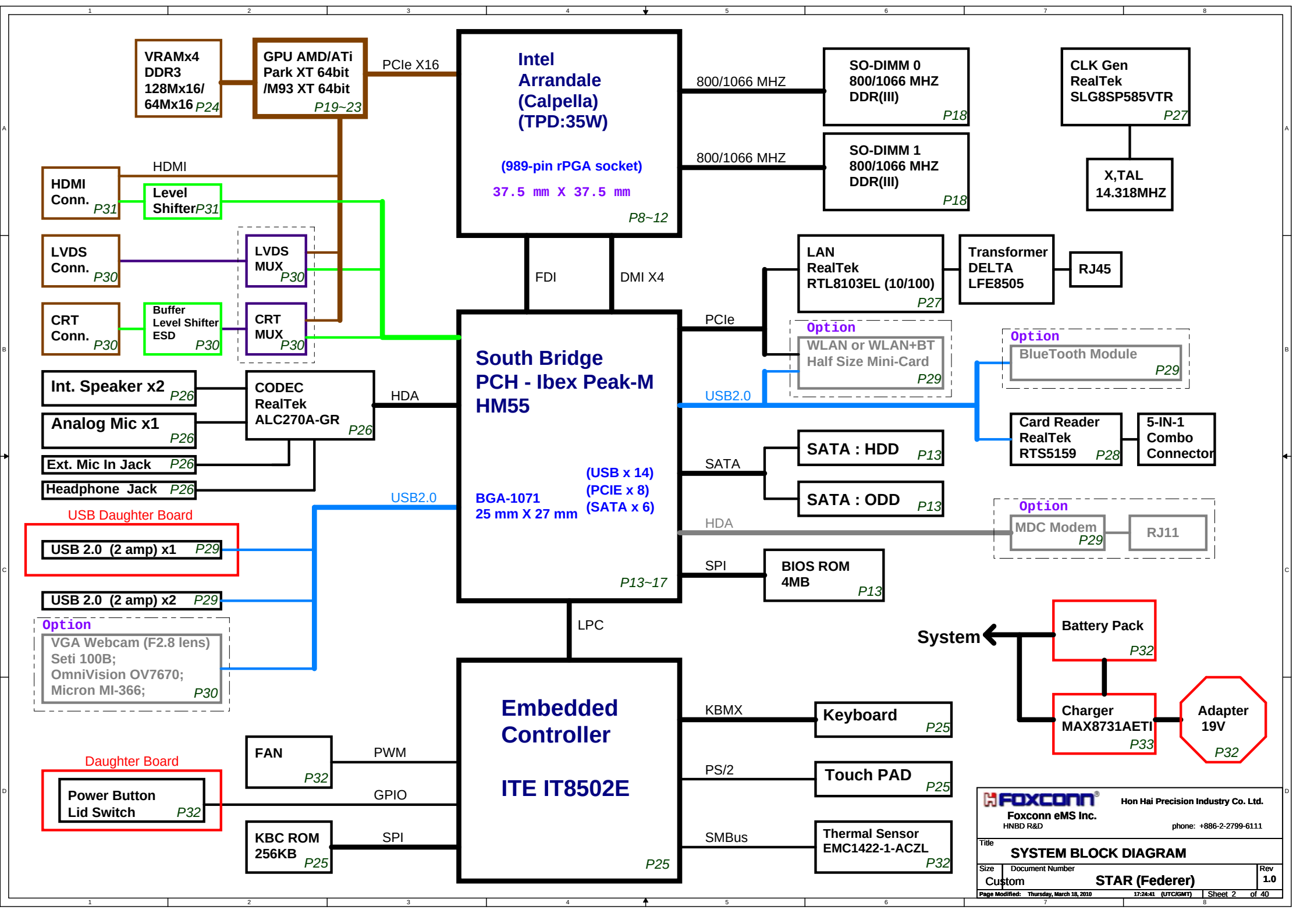
VRAMx4
DDR3
128Mx16/
64Mx16 P24
GPU AMD/ATi
Park XT 64bit
/M93 XT 64bit
P19~23
PCIe X16
Intel
Arrandale
(Calpella)
(TPD:35W)
(989-pin rPGA socket)
37.5 mm X 37.5 mm
P8~12
800/1066 MHZ
SO-DIMM 0
800/1066 MHZ
DDR(III)
P18
800/1066 MHZ
SO-DIMM 1
800/1066 MHZ
DDR(III)
P18
CLK Gen
RealTek
SLG8SP585VTR
P27
X,TAL
14.318MHZ
HDMI
HDMI
Conn. P31
Level
ShifterP31
LVDS
Conn. P30
LVDS
MUX P30
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CRT
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FDI
DMI X4
LAN
RealTek
RTL8103EL (10/100)
P27
Transformer
DELTA
LFE8505
RJ45
Option
WLAN or WLAN+BT
Half Size Mini-Card
P29
Option
BlueTooth Module
P29
South Bridge
PCH - Ibex Peak-M
HM55
BGA-1071
25 mm X 27 mm
(USB x 14)
(PCIE x 8)
(SATA x 6)
P13~17
PCIe
USB2.0
Int. Speaker x2 P26
Analog Mic x1 P26
Ext. Mic In Jack P26
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CODEC
RealTek
ALC270A-GR P26
HDA
Card Reader
RealTek
RTS5159 P28
5-IN-1
Combo
Connector
SATA
SATA : HDD P13
SATA : ODD P13
USB Daughter Board
USB 2.0 (2 amp) x1 P29
USB 2.0 (2 amp) x2 P29
USB2.0
Option
VGA Webcam (F2.8 lens)
Seti 100B;
OmniVision OV7670;
Micron MI-366; P30
Option
MDC Modem P29
RJ11
HDA
SPI
BIOS ROM
4MB
P13
LPC
System
Battery Pack
P32
Charger
MAX8731AETI
P33
Adapter
19V
P32
Embedded
Controller
ITE IT8502E
P25
KBMX
Keyboard
P25
PS/2
Touch PAD
P25
SMBus
Thermal Sensor
EMC1422-1-ACZL
P32
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Power Button
Lid Switch P32
FAN
P32
PWM
GPIO
KBC ROM
256KB
P25
SPI
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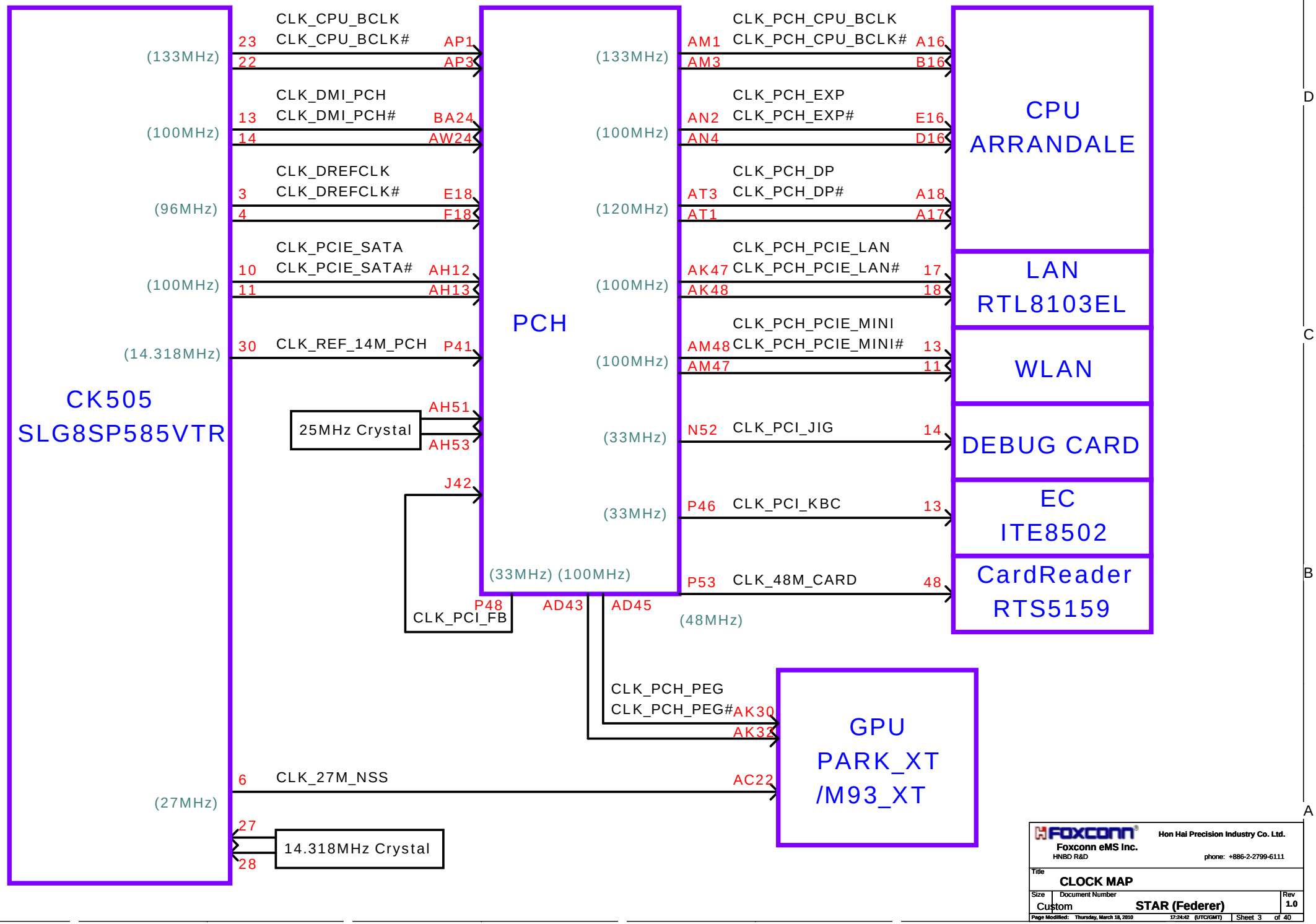

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SCH Page	Change Request Description	Notes
25,33~40	modify the power short pad to "POWER_OPENPAD_1P9X2P4"	SMD performance issue
15	Add RS74,RS77,RS79 for all SG sku	Fix VGA port auto detect function
39	Change PR944 from 1K to 1.5K	Fix power load line test issue
13	Del PCH SPI ROM connector circuitry	Del unnecessary functon parts
25	Del EC SPI ROM connector circuitry	Del unnecessary functon parts
25	Del debug connector	Del unnecessary functon part
25	SKU ID modify to MV phase	MV Phase ID
13	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
25	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
30	VGA connector change part number to halide free type	ROHS issue
29	MDC connector change part number to halide free type	ROHS issue
29	Mini-PCIE connector change part number to halide free type	ROHS issue
30	LVDS connector change part number to halide free type	ROHS issue
13	SATA connector change part number to halide free type	ROHS issue
30	Modify backlight PWM control path	Del unnecessary parts
18	Modify the DDR3 footprint	Co-lay for DDR3 connector
25	Del DI10	Del unnecessary functon parts
25,30	Del RB28 and Add RI54	For 17" keyboard num lock LED
38	add PC775	Add for GPU M93 platform
38	add PC776	Add for VGA wave issue
35	Change VCORE VDD power source from +V5A to +V5S	Modify for V-BOOT
38	Change PR769 pull high power source from +12A to +V5A	Modify for GPU power sequence
29	Modify the HOLE1006 footprint	update footprint
40	modify all VDDCORE circuity	modify VDDCORE circuity
26	modify UA3 pin2 Analogy GND to Digital GND	Analogy GND change to Digital GND
32	add 2 pcs 2N7002 and swap EC_CHAR_LED#_A & EC_AC_LED#_W	Modify LED control and brightness
32	modify HEADER10 pin1 power source from +V5A to +V3.3AL	modify LED control and brightness
33~37	PC547 22uF_X5R_25V to 10uF_X5R_25V*2 PC504 4.7uF_X5R_25V to 10uF_X5R_25V PC813 4.7uF_X5R_25V to 10uF_X5R_25V PC825, PC812 to 10uF_X5R_25V (NI) PC826 to 10uF_X5R_25V (NI) PC824, PC828, PC829 4.7uF_X5R_25V to 10uF_X5R_25V"	modify for acoustic
32	RH1002 change to 1.3Kohm	modify LED control and brightness
27	RL13 change to 2.7Kohm"	modify LED control and brightness
32	ADD QB11	Thermal shutdown
19	ADD RG457,RG458	Add for power leakage issue
35	Del DB14	Thermal shutdown issue

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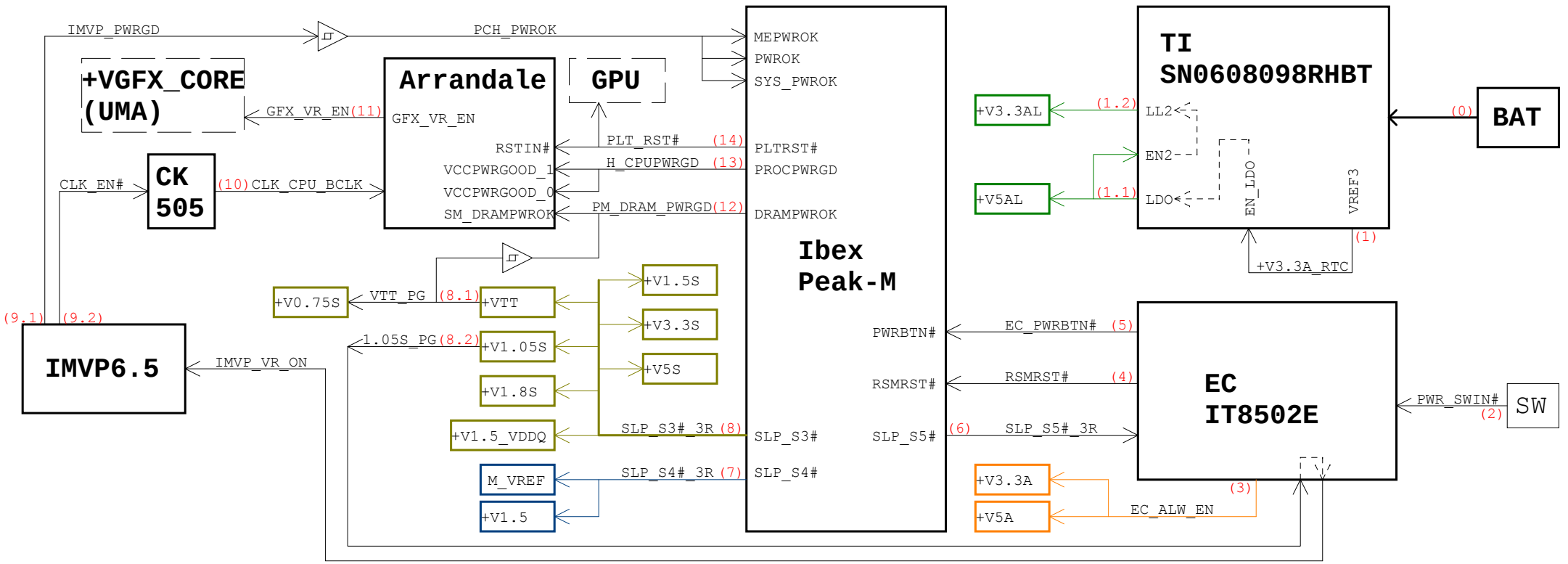

	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

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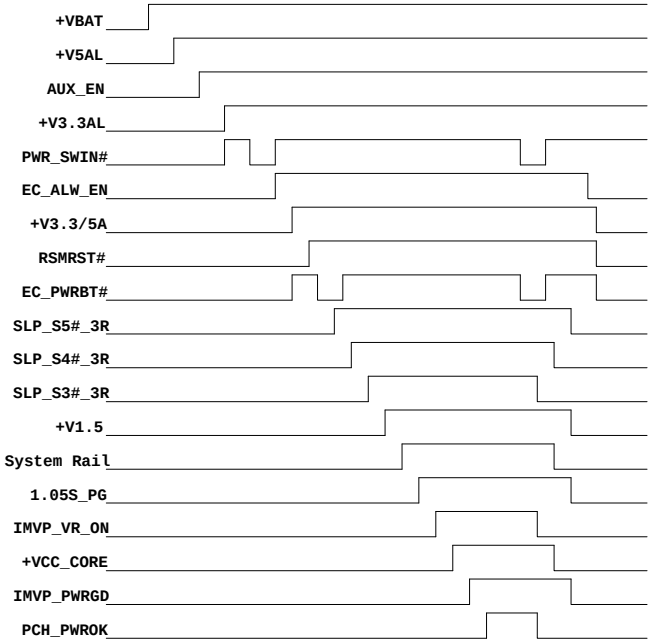
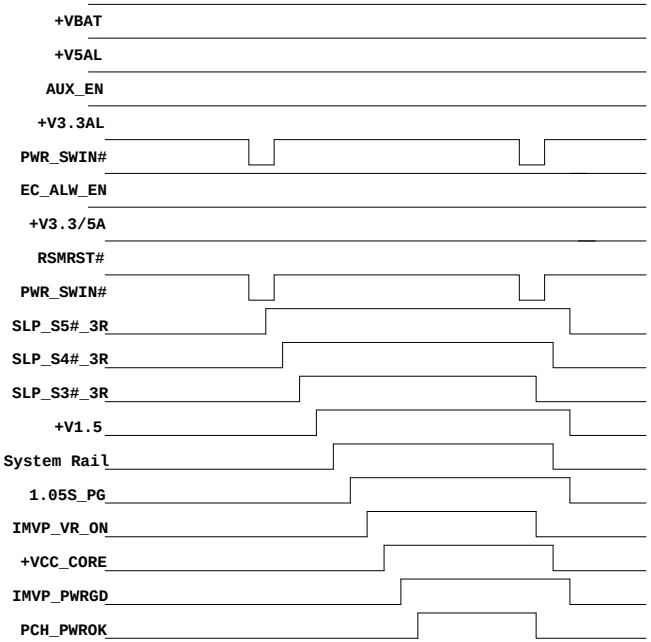
POWER SEQUENCE TIMING

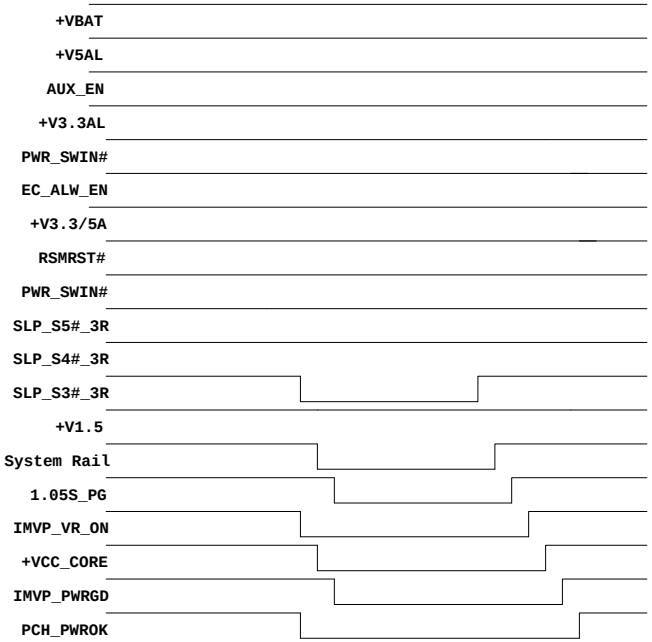
G3(OFF)->S0->S5



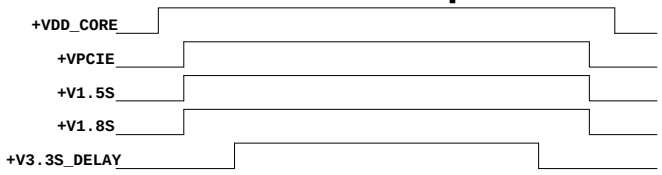
S5->S0->S5



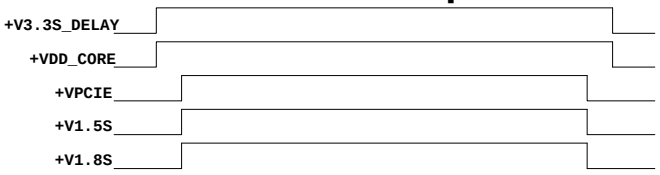
S0->S3->S0



GPU_M93 Sequence



GPU_Park Sequence



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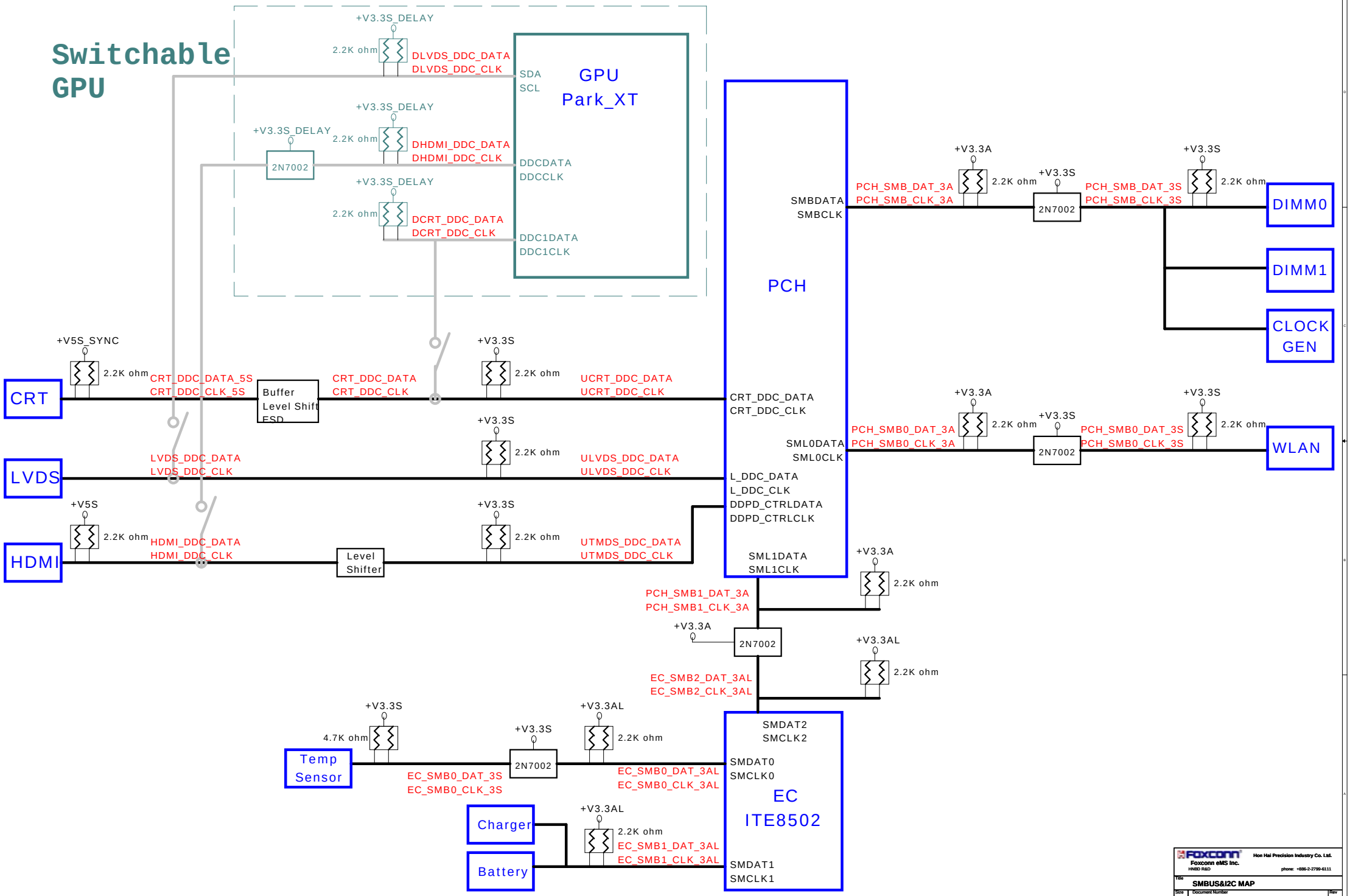
Switchable GPU
GPU Park_XT
SDA
SCL
DDCDATA
DDCCLK
DDC1DATA
DDC1CLK
+V3.3S_DELAY
2.2K ohm
DLVDS_DDC_DATA
DLVDS_DDC_CLK
DHDMI_DDC_DATA
DHDMI_DDC_CLK
DCRT_DDC_DATA
DCRT_DDC_CLK
2N7002
PCH
SMBDATA
SMBCLK
SML0DATA
SML0CLK
SML1DATA
SML1CLK
CRT_DDC_DATA
CRT_DDC_CLK
L_DDC_DATA
L_DDC_CLK
DDPD_CTRLDATA
DDPD_CTRLCLK
+V3.3A
+V3.3S
PCH_SMB_DAT_3A
PCH_SMB_CLK_3A
PCH_SMB_DAT_3S
PCH_SMB_CLK_3S
DIMM0
DIMM1
CLOCK GEN
PCH_SMB0_DAT_3A
PCH_SMB0_CLK_3A
PCH_SMB0_DAT_3S
PCH_SMB0_CLK_3S
WLAN
+V5S_SYNC
CRT
CRT_DDC_DATA_5S
CRT_DDC_CLK_5S
Buffer Level Shift ESD
CRT_DDC_DATA
CRT_DDC_CLK
UCRT_DDC_DATA
UCRT_DDC_CLK
LVDS
LVDS_DDC_DATA
LVDS_DDC_CLK
ULVDS_DDC_DATA
ULVDS_DDC_CLK
+V5S
HDMI
HDMI_DDC_DATA
HDMI_DDC_CLK
Level Shifter
UTMDS_DDC_DATA
UTMDS_DDC_CLK
PCH_SMB1_DAT_3A
PCH_SMB1_CLK_3A
EC_SMB2_DAT_3AL
EC_SMB2_CLK_3AL
+V3.3AL
4.7K ohm
Temp Sensor
EC_SMB0_DAT_3S
EC_SMB0_CLK_3S
EC_SMB0_DAT_3AL
EC_SMB0_CLK_3AL
SMDAT2
SMCLK2
SMDAT0
SMCLK0
EC
ITE8502
Charger
Battery
EC_SMB1_DAT_3AL
EC_SMB1_CLK_3AL
SMDAT1
SMCLK1
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SMBUS&I2C MAP
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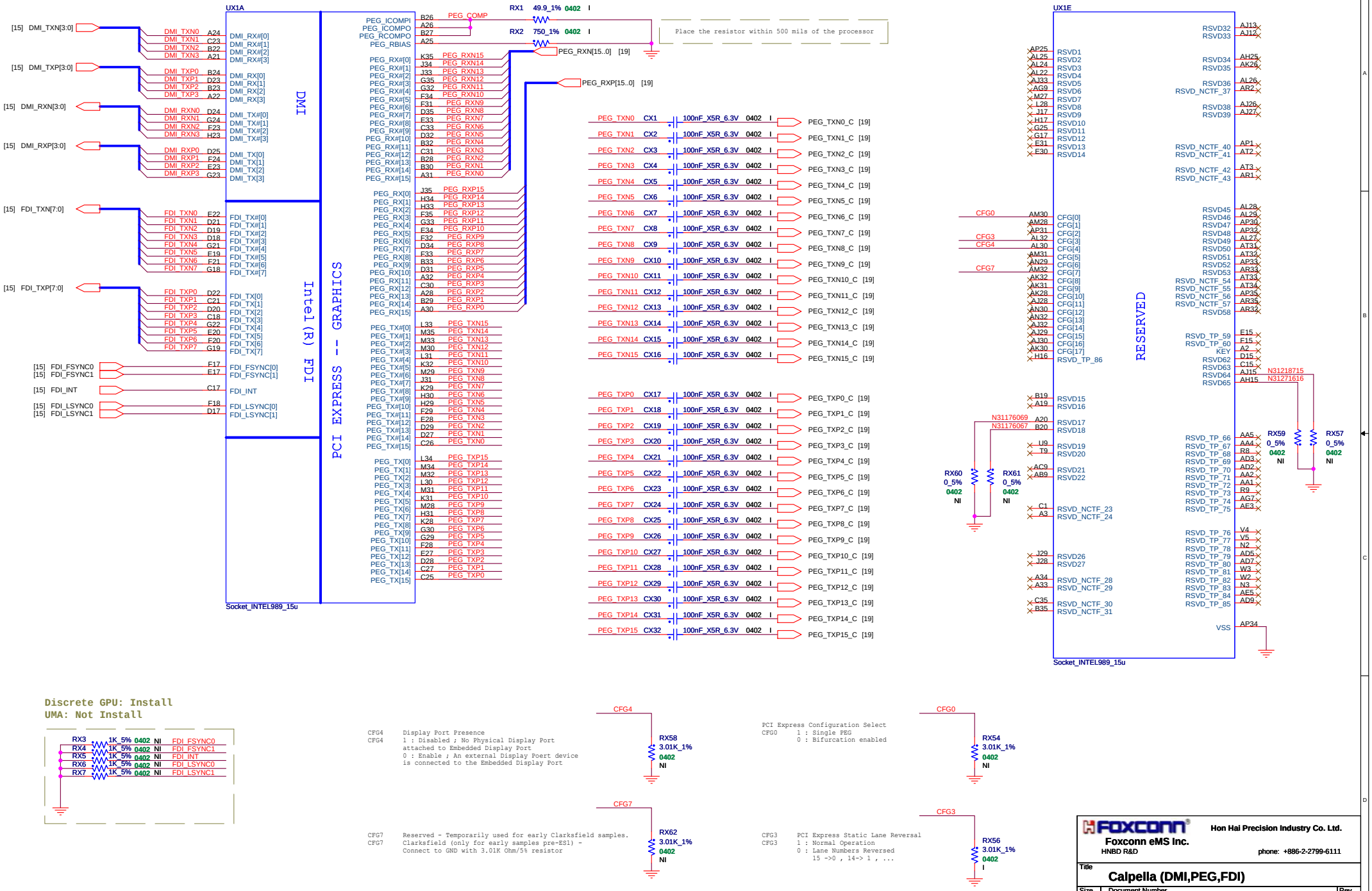
UX1A
DMI
Intel(R) FDI
PCI EXPRESS - GRAPHICS
Socket_INTEL989_15u
RX1 49.9_1% 0402 I
RX2 750_1% 0402 I
Place the resistor within 500 mils of the processor
PEG_RXN[15..0] [19]
PEG_RXP[15..0] [19]
UX1E
RESERVED
Socket_INTEL989_15u
Discrete GPU: Install
UMA: Not Install
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Poert device is connected to the Embedded Display Port
CFG7 Reserved - Temporarily used for early Clarksfield samples.
CFG7 Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enabled
CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 ->0 , 14-> 1 , ...
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Layout Note:
Comp0,2 connect with Zo=27.4 ohm,
make trace length shorter then
0.5".
Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm,
make trace length shorter then
0.5".
Width=5mil(MS)

Place close to chip

RX8 20_1% 0402 COMP3
RX9 20_1% 0402 COMP2
RX10 49.9_1% 0402 COMP1
RX11 49.9_1% 0402 COMP0

UX1B
AT23 COMP3
AT24 COMP2
G16 COMP1
AT26 COMP0
AH24 SKTOCC#
AK14 CATERR#
AT15 PECI
AN26 PROCHOT#
AK15 THERMTRIP#
AP26 RESET_OBS#
AL15 PM_SYNC
AN14 VCCPWRGOOD_1
AN27 VCCPWRGOOD_0
AK13 SM_DRAMPWROK
AM15 VTTPWRGOOD
AM26 TAPPWRGOOD
AL14 RSTIN#

MISC THERMAL PWR MANAGEMENT

Socket_INTEL989_15u

+VTT
RX39 49.9_1% 0402
RX46 68_5% 0402
H_CATERR#
[16] H_PECI
PROCHOT#
[16,32] PM_THRMTRIP#

+V1.5_VDDQ
RX75 1.1K_1% 0402 NI
XDP_RST#_R
RX71 1K_5% 0402
H_CPURST#
[15] H_PM_SYNC
[16] H_CPUPWRGD
RX25 0_5% 0402 CPUPWRGD1
RX26 0_5% 0402 CPUPWRGD0
[15] PM_DRAM_PWRGD
RX28 0_5% 0402 DRAM_PWRGD
VTTPWRGOOD
H_PWRGD_XDP

+V3.3A
CX80 100nF_X5R_6.3V 0402
RX79 1.5K_1% 0402
RX78 750_1% 0402
UX5 74LVC1G17GW
Modify for reduce S3 power consumption on 0908
[32,36,37] VTT_PG
RX77 0_5% 0402
[15,25,32,36,37,38,40] SLP_S3#_3R
RX76 0_5% 0402 NI
[16,19] PLT_RST#
RX30 1.5K_1%
RX31 750_1% 0402

Clarksfield: 1.1V(RX30=1.5K 1%; RX31=750 1%)
Arrandale : 1.05V(RX30=1.5K 1% ; RX31=698 1%)

CLOCKS

BCLK A16
BCLK# B16
BCLK_ITP AR30
BCLK_ITP# AT30
PEG_CLK E16
PEG_CLK# D16
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17

BCLK_ITP_P
BCLK_ITP_N
CLK_PCH_EXP_R
CLK_PCH_EXP#_R
CLK_PCH_DP_R
CLK_PCH_DP#_R

RX12 0_5% 0402
RX13 0_5% 0402
RX14 0_5% 0402 NI
RX15 0_5% 0402
RX16 0_5% 0402
RX17 0_5% 0402 NI

CLK_PCH_CPU_CLK [16]
CLK_PCH_CPU_CLK# [16] (133MHz)
CLK_PCH_EXP [14]
CLK_PCH_EXP# [14]
CLK_PCH_DP [14] (100MHz)
CLK_PCH_DP# [14] (120MHz)

Discrete :RX14,RX17 Not Install and RX15,RX16 0 ohm
UMA: RX14,RX17 0 ohm and RX15,RX16 Not Install

DDR3 MISC

SM_DRAMRST# F6
SM_RCOMP[0] AL1 SM_RCOMP0 RX18 100_1% 0402
SM_RCOMP[1] AM1 SM_RCOMP1 RX21 24.9_1% 0402
SM_RCOMP[2] AN1 SM_RCOMP2 RX22 130_1% 0402
PM_EXT_TS#[0] AN15
PM_EXT_TS#[1] AP15
PM_EXTTS#0
RX19 10K_5% 0402
RX20 10K_5% 0402
PM_EXTTS#1 [18]
RX24 12.4K_1% 0402 NI

DDR3 module w/o this function

+V1.5
RX72 0402 0_5% NI
RX73 1K_5% 0402
QX3 2N7002 SOT23-3
RX74 100K_5% 0402
DDR3_DRAMRST# [18]
PCH_DDR_RST# [16]
CX43 47nF_X7R_16V 0402

JTAG & BPM

PRDY# AT28 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI
TDO AR27 XDP_TDO
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 SB_RST# [15,25]
RX42 0_5% 0402

BPM#[0] AJ22 XDP_OBS0
BPM#[1] AK22 XDP_OBS1
BPM#[2] AK24 XDP_OBS2
BPM#[3] AJ24 XDP_OBS3
BPM#[4] AJ25 XDP_OBS4
BPM#[5] AH22 XDP_OBS5
BPM#[6] AK23 XDP_OBS6
BPM#[7] AH23 XDP_OBS7

TCK 50 PD
TMS 2k~5k PU
TRST 2k~5k PU
TDI 50 PU
TDO unconnect
TDI_M 50 PU
TDO_M unconnect

+VTT
RX32 XDP_TDO
RX33 XDP_TMS
RX34 XDP_TDI
RX35 XDP_PREQ#
RX36 XDP_TCLK
RX37 XDP_TRST#

CON18
XDP_PREQ#
XDP_PRDY#
XDP_OBS0
XDP_OBS1
XDP_OBS2
XDP_OBS3
XDP_OBS4
XDP_OBS5
XDP_OBS6
XDP_OBS7
XDP_TCLK
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD_HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK_HOOK4 ITPCLK#_HOOK5 VCC_OBS_CD RESET#_HOOK6 DBR#_HOOK7 GND15 TDO TRSTn TDI TMS GND17
BCLK_ITP_P
BCLK_ITP_N
XDP_RST#_R
SB_RST#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
BSH-030-01-L-D-A-TR NI

H_CPUPWRGD RX70 1K_5% 0402 H_CPUPWRGD_XDP
[15,25] EC_PWRBTN#
+VTT
H_PWRGD_XDP

+V1.5
RX38 1.1K_1% 0402 NI
DRAM_PWRGD
RX43 3K_1% 0402 NI

+V3.3S
RX45 0_5% 0402 NI
[32,36,37] VTT_PG
[32,36] 1.05S_PG
RX40 0_5% 0402
CX33 100nF_X5R_6.3V 0402
UX2 74LVC1G17GW
RX41 2K_1% 0402
VTTPWRGOOD
RX44 1K_1% 0402

Clarksfield: 1.1V(RX38=1.1K 1%; RX43=3.01K 1%)
Arrandale : 1.05V(RX38=1.1K 1% ; Rx43=2.61K 1%)

Clarksfield: 1.1V(RX41=2K 1%; RX44=1K 1%)
Arrandale : 1.05V(RX41=2K 1% ; R44=931ohm 1%)

[32,35] IMVP_PWRGD
RX29 2M_5% 0402
PCH_PROCHOT# [16,32]
QX1 2N7002 SOT23-3
A0205
QX2
PROCHOT#
PDTC144EU

+V1.5_VDDQ [12,17,27,29,38]
+V3.3S [13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,38,39,40]
+VTT [11,12,16,17,27,35,36,39]
+V1.5 [18,37,38]
+V3.3A [13,14,15,16,17,25,27,29,32,33,37,38]

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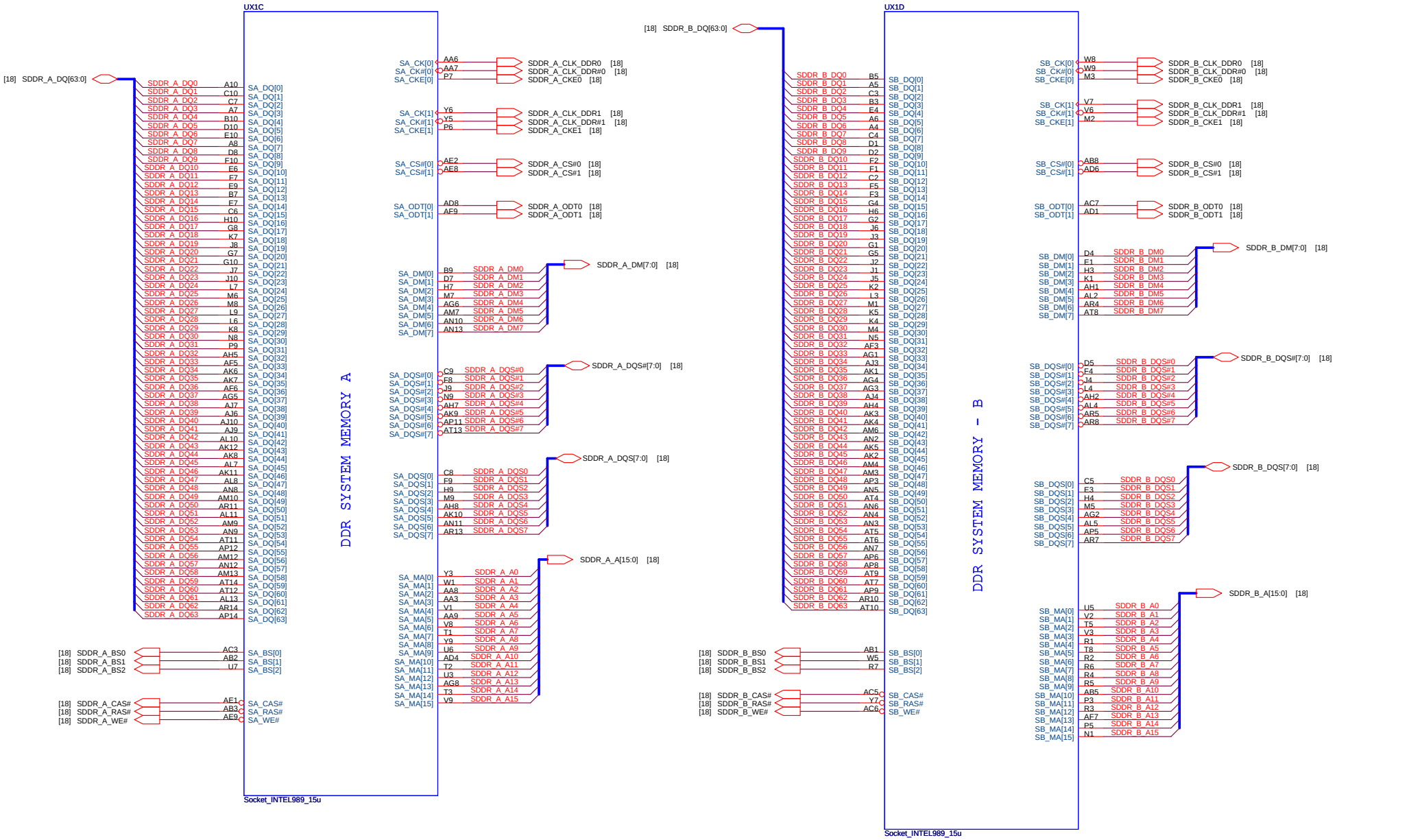
UX1C
DDR SYSTEM MEMORY A
Socket_INTEL989_15u
UX1D
DDR SYSTEM MEMORY - B
Socket_INTEL989_15u
[18] SDDR_A_DQ[63:0]
[18] SDDR_B_DQ[63:0]
SDDR_A_DM[7:0] [18]
SDDR_A_DQS#[7:0] [18]
SDDR_A_DQS[7:0] [18]
SDDR_A_A[15:0] [18]
SDDR_B_DM[7:0] [18]
SDDR_B_DQS#[7:0] [18]
SDDR_B_DQS[7:0] [18]
SDDR_B_A[15:0] [18]
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Title
Calpella (DDR3)
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FOR VCC:
12x 0805 22 µF inside cavity,
7x 0805 10 µF under cavity and 9 x 0805 10 µF
between inductor and socket on top layer

FOR VTT:
7x 0805 22 µF under cavity
8x 0805 10 µF edge caps

52A

+VCC_CORE
CX42 22uF_X5R_6.3V 0805
CX46 22uF_X5R_6.3V 0805
CX47 22uF_X5R_6.3V 0805
CX48 22uF_X5R_6.3V 0805
CX49 22uF_X5R_6.3V 0805
CX50 22uF_X5R_6.3V 0805
CX51 22uF_X5R_6.3V 0805
CX52 22uF_X5R_6.3V 0805
CX53 22uF_X5R_6.3V 0805
CX54 22uF_X5R_6.3V 0805
CX55 22uF_X5R_6.3V 0805
CX56 22uF_X5R_6.3V 0805
CX57 10uF_Y5V_10V 0805
CX58 10uF_Y5V_10V 0805
CX59 10uF_Y5V_10V 0805
CX60 10uF_Y5V_10V 0805
CX61 10uF_Y5V_10V 0805
CX62 10uF_Y5V_10V 0805
CX63 10uF_Y5V_10V 0805
CX64 10uF_Y5V_10V 0805
CX65 10uF_Y5V_10V 0805
CX66 10uF_Y5V_10V 0805
CX67 10uF_Y5V_10V 0805
CX68 10uF_Y5V_10V 0805
CX69 10uF_Y5V_10V 0805
CX70 10uF_Y5V_10V 0805
CX71 33pF_NPO_50V 0402
CX72 10uF_Y5V_10V 0805
CX73 10uF_Y5V_10V 0805
CX74 33pF_NPO_50V 0402

+VTT [9,12,16,17,27,35,36,39]
+VCC_CORE [35]

UX1F
Socket_INTEL989_15u

1.1V RAIL POWER
CPU CORE SUPPLY
CPU VIDS
SENSE LINES

POWER

CX34 10uF_Y5V_10V 0805
CX35 10uF_Y5V_10V 0805
CX36 10uF_Y5V_10V 0805
CX37 10uF_Y5V_10V 0805
CX38 10uF_Y5V_10V 0805
CX39 10uF_Y5V_10V 0805
CX40 10uF_Y5V_10V 0805
CX41 10uF_Y5V_10V 0805
CX44 22uF_X5R_6.3V 0805
CX45 22uF_X5R_6.3V 0805

PSI# [35]
VID0 [35]
VID1 [35]
VID2 [35]
VID3 [35]
VID4 [35]
VID5 [35]
VID6 [35]
PM_DPRSLPVR [35]
TP_P30

Arrandale drives this pin High
Clarksfield drives this pin Low.

IMVP_IMON [35]
RX47 100_1% 0402
RX48 100_1% 0402
VCCSENSE [35]
VSSSENSE [35]
VTT_SENSE [36]
Place close to CPU

UX1H
VSS
Socket_INTEL989_15u

UX1I
VSS
Socket_INTEL989_15u

NCTF
TP_MCP_VSS_NCTF1
TP_MCP_VSS_NCTF2
TP_MCP_VSS_NCTF6
TP_MCP_VSS_NCTF7
TP_P30TP846
TP_P30TP2
TP_P30TP3
TP_P30TP4

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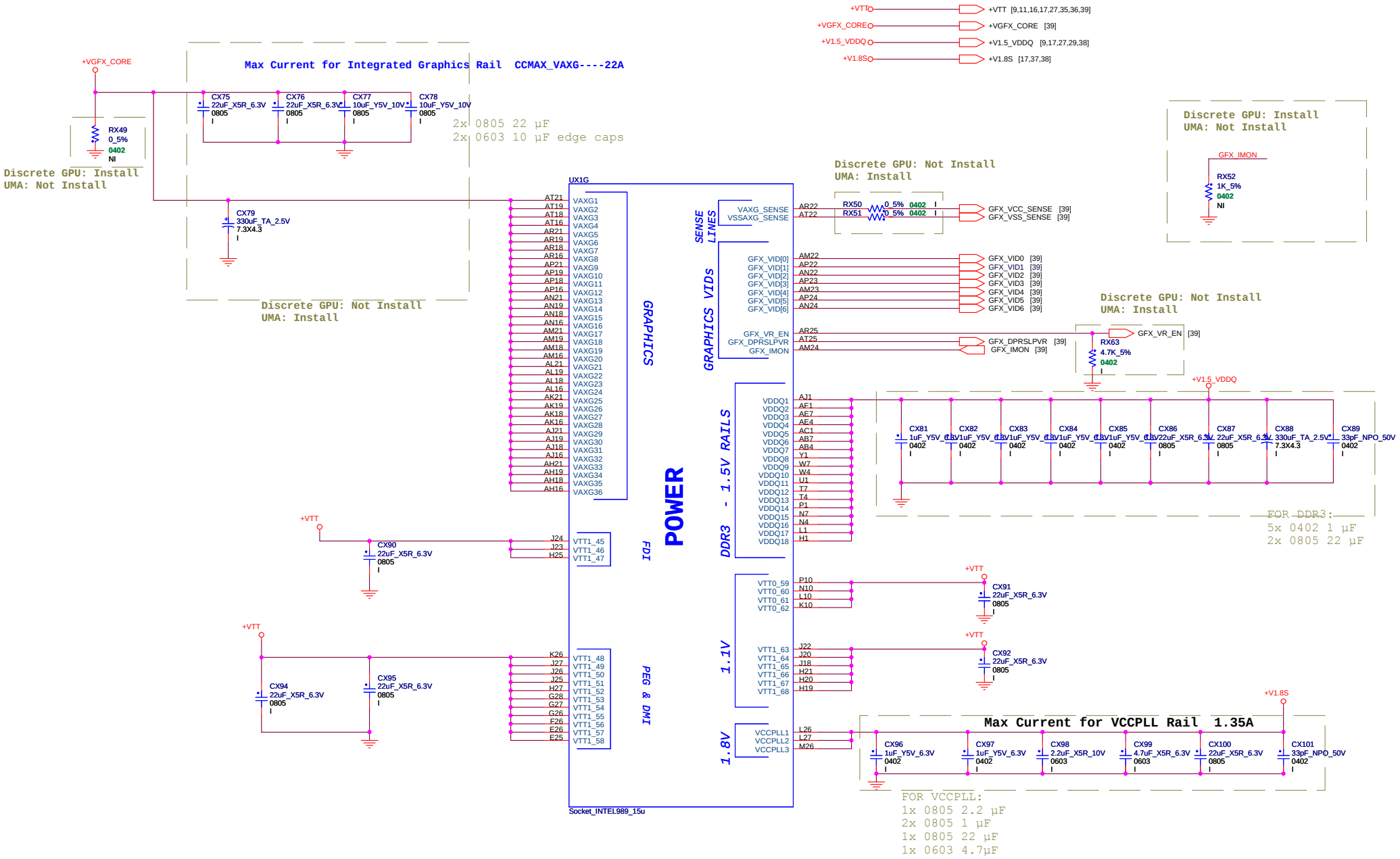

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Title: Calpella (GRAPHICS POWER)

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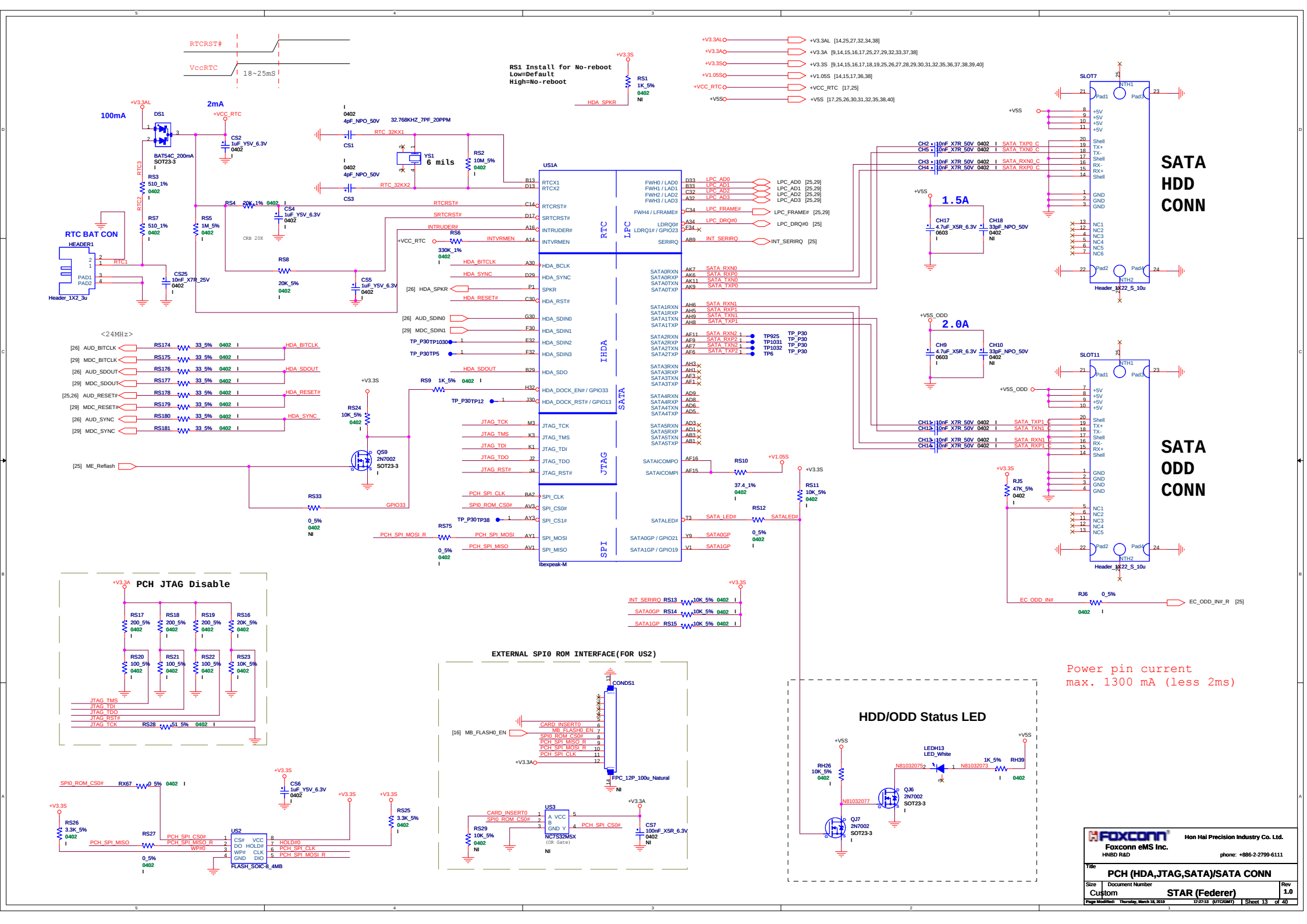

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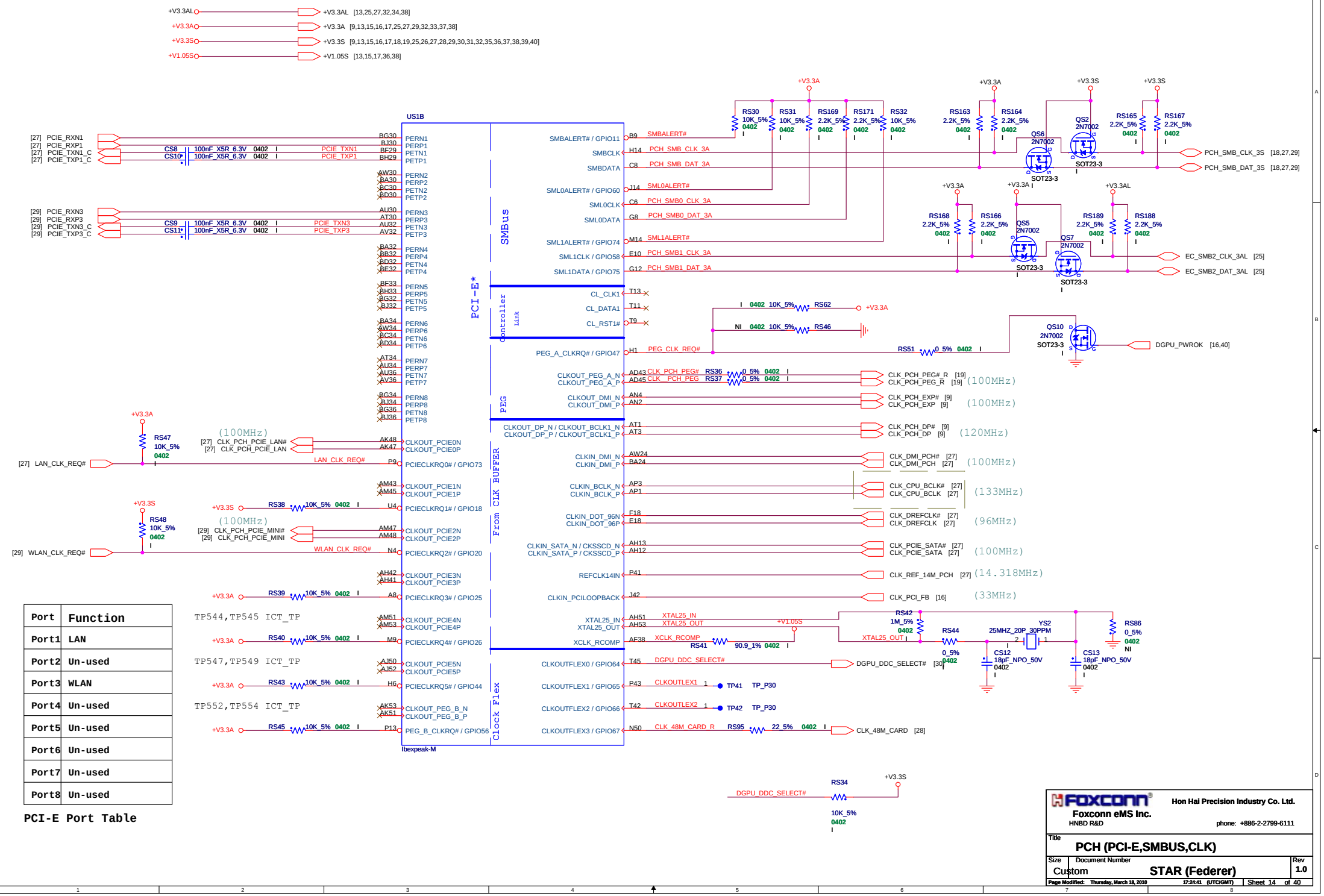

Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

PCI-E Port Table

Company	Hon Hai Precision Industry Co. Ltd.
	Foxconn eMS Inc.
	HNBD R&D
	phone: +886-2-2799-6111
Title	PCH (PCI-E,SMBUS,CLK)
Size	Custom
Document Number	STAR (Federer)
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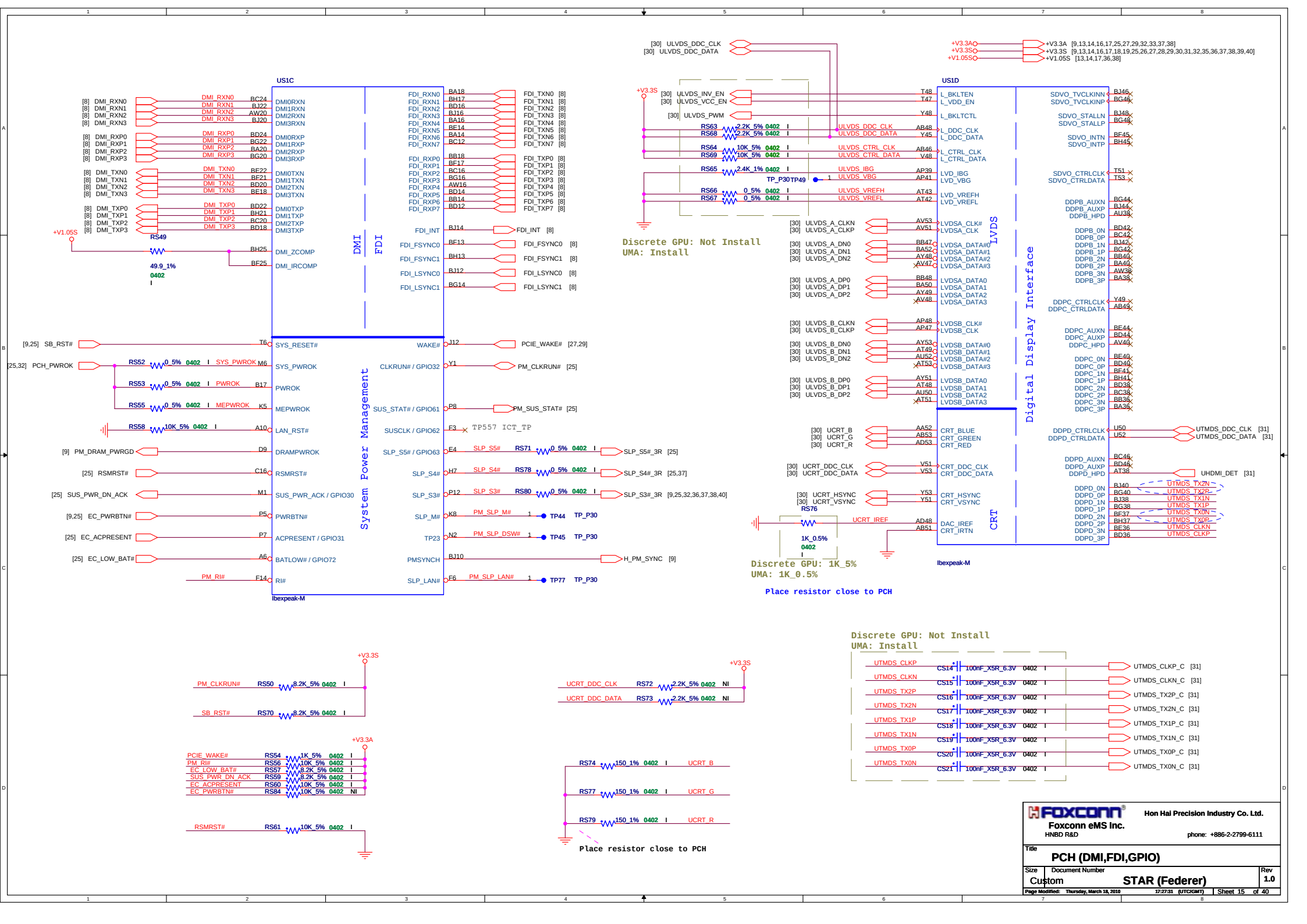
US1C
DMI
FDI
System Power Management
lbexpeak-M
US1D
LVDS
Digital Display Interface
CRT
Discrete GPU: Not Install
UMA: Install
Discrete GPU: 1K_5%
UMA: 1K_0.5%
Place resistor close to PCH
Discrete GPU: Not Install
UMA: Install
Place resistor close to PCH
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PCH (DMI,FDI,GPIO)
Custom
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Rev 1.0
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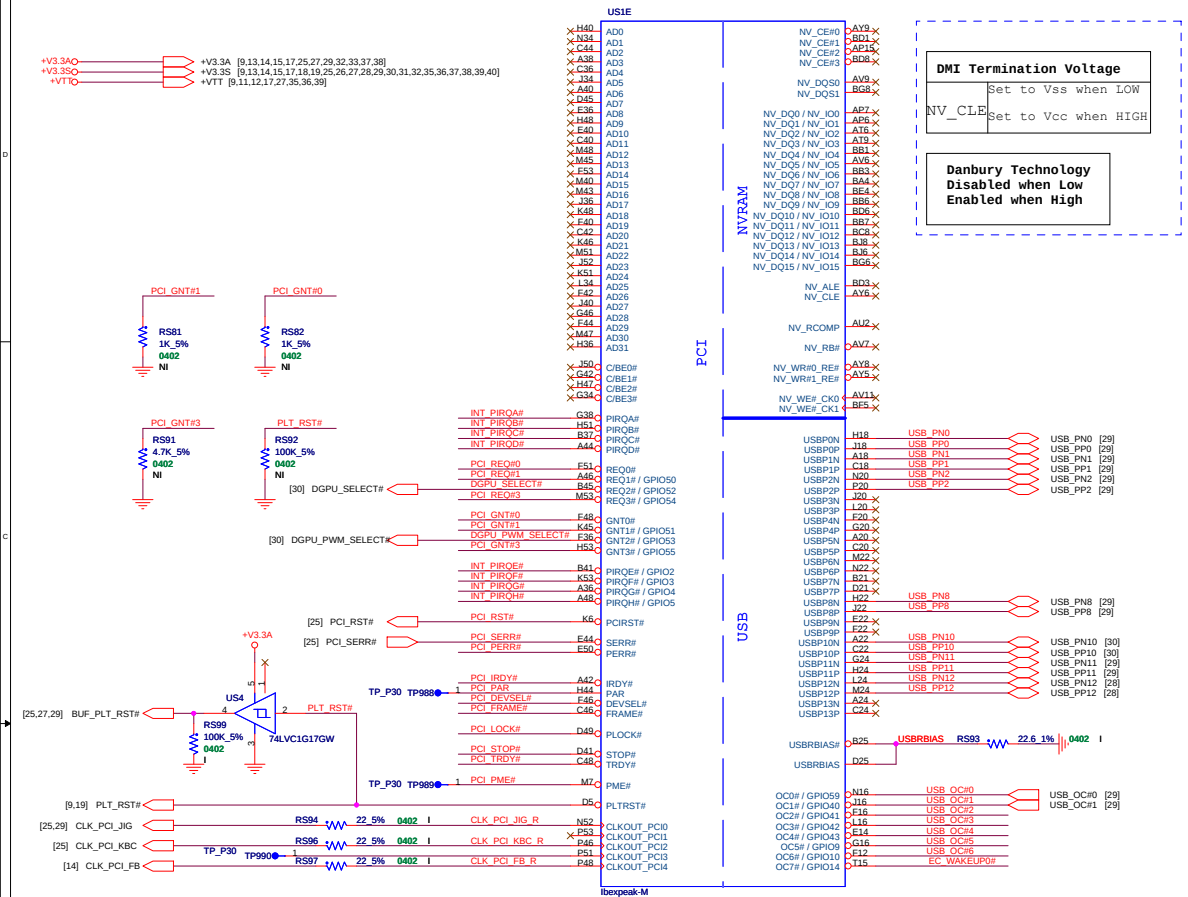
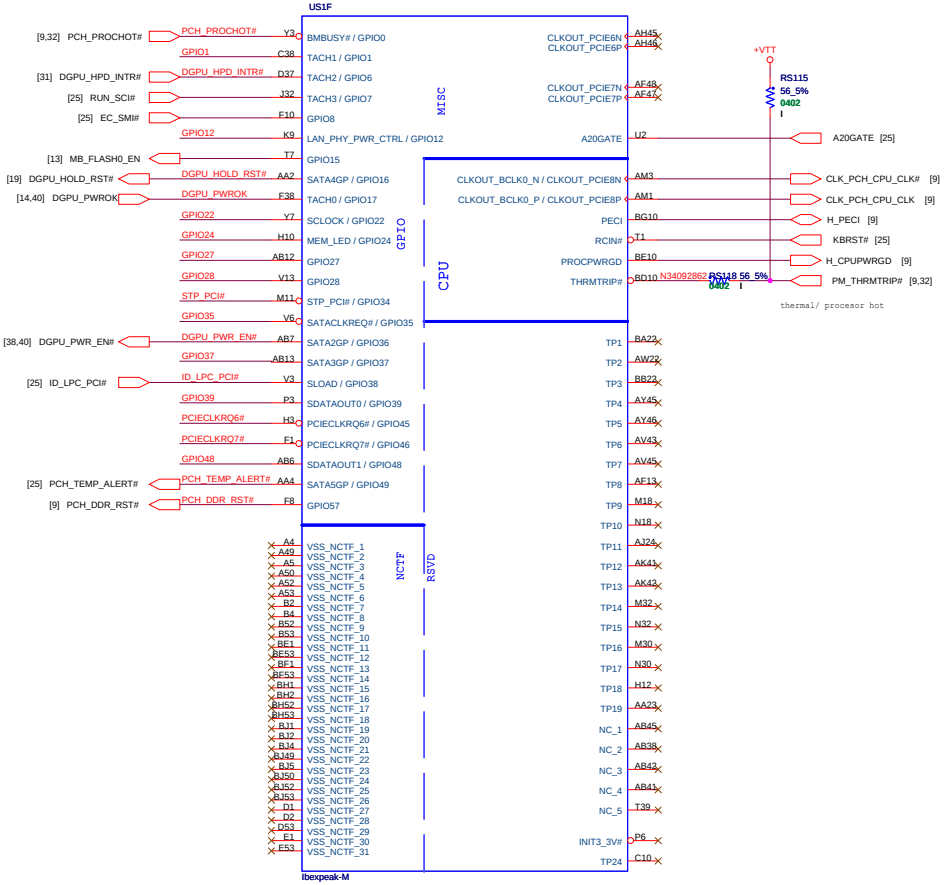
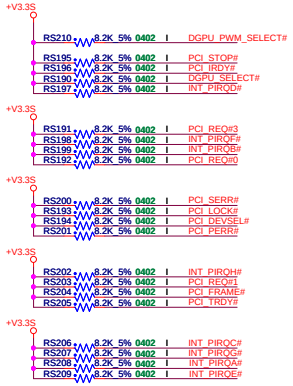
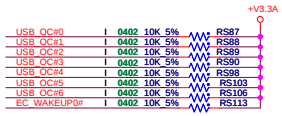
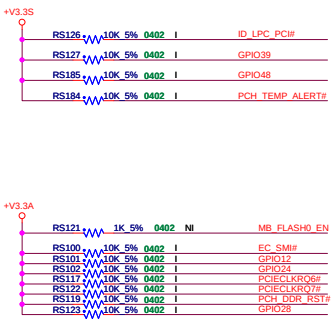


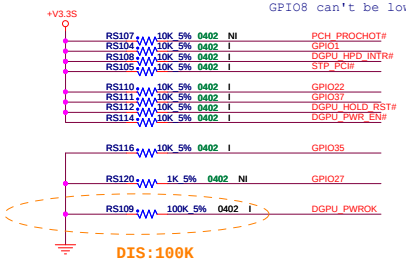




USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8	Bluetooth	
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13		







DVT Ask EC if we need to change GPIO pin.
GPIO8 can't be low.

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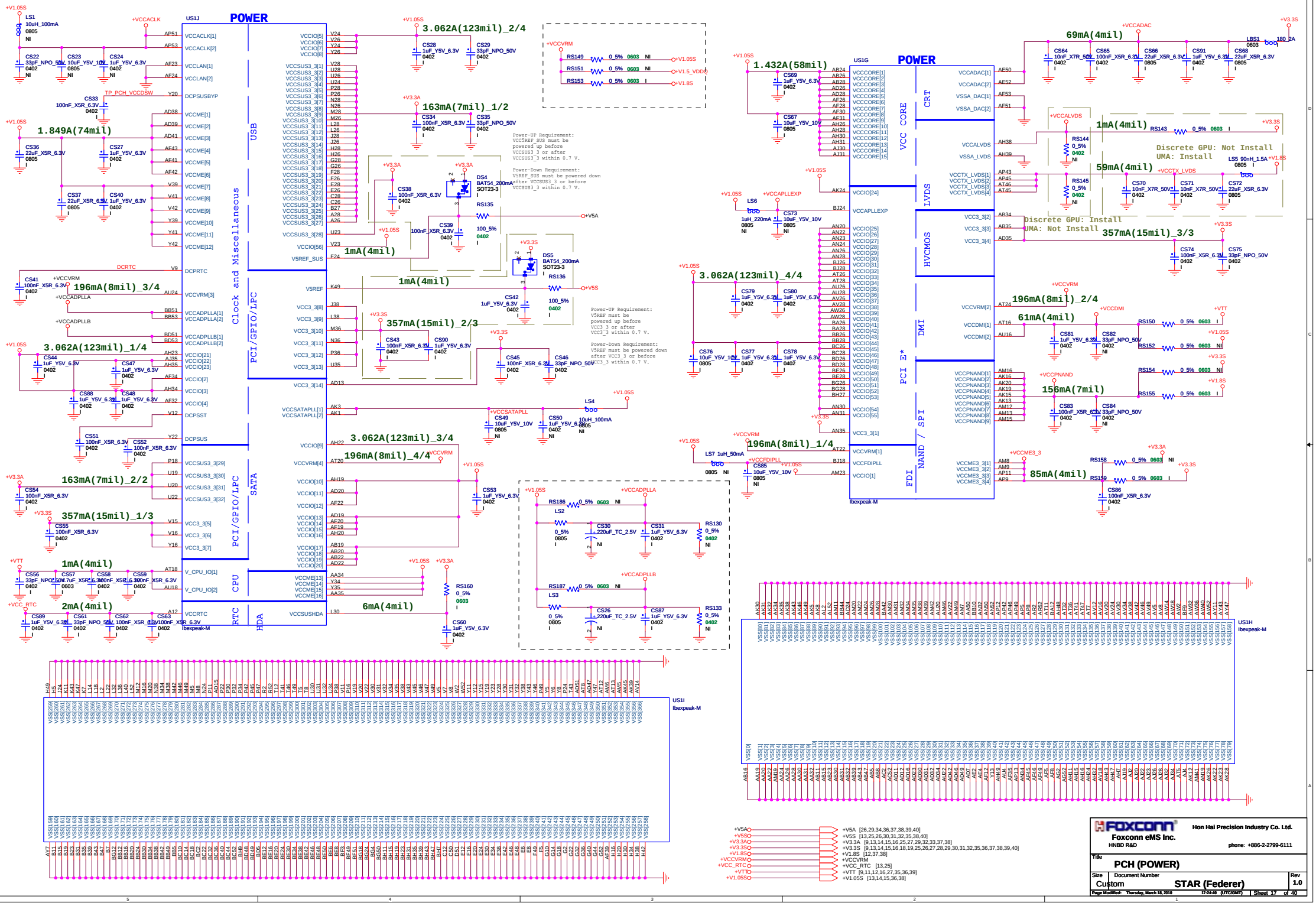

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+V0.75S
+V1.5
+V3.3S
M_VREF

+V0.75S [37,38]
+V1.5 [9,37,38]
+V3.3S [9,13,14,15,16,17,19,25,26,27,28,29,30,31,32,35,36,37,38,39,40]
M_VREF [37]

[10] SDDR_A_A[0..15]
SDDR_A_DQ[0..63] [10]

SLOT2A

SMBus Address: A0H(W)/A1H(R)

[10] SDDR_A_BS0
[10] SDDR_A_BS1
[10] SDDR_A_BS2
[10] SDDR_A_CS#0
[10] SDDR_A_CS#1
[10] SDDR_A_CLK_DDR0
[10] SDDR_A_CLK_DDR#0
[10] SDDR_A_CLK_DDR1
[10] SDDR_A_CLK_DDR#1
[10] SDDR_A_CKE0
[10] SDDR_A_CKE1
[10] SDDR_A_CAS#
[10] SDDR_A_RAS#
[10] SDDR_A_WE#

RM4 10K_5% 0402 SA0_DIM0
RM5 10K_5% 0402 SA1_DIM0

[14,27,29] PCH_SMB_CLK_3S
[14,27,29] PCH_SMB_DAT_3S

[10] SDDR_A_ODT0
[10] SDDR_A_ODT1

[10] SDDR_A_DM[0..7]

[10] SDDR_A_DQS[0..7]

[10] SDDR_A_DQS#[0..7]

DDR3_204P_3u

SLOT3A

[10] SDDR_B_A[0..15]
SDDR_B_DQ[0..63] [10]

[10] SDDR_B_BS0
[10] SDDR_B_BS1
[10] SDDR_B_BS2
[10] SDDR_B_CS#0
[10] SDDR_B_CS#1
[10] SDDR_B_CLK_DDR0
[10] SDDR_B_CLK_DDR#0
[10] SDDR_B_CLK_DDR1
[10] SDDR_B_CLK_DDR#1
[10] SDDR_B_CKE0
[10] SDDR_B_CKE1
[10] SDDR_B_CAS#
[10] SDDR_B_RAS#
[10] SDDR_B_WE#

RM7 10K_5% 0402 SA0_DIM1
RM8 10K_5% 0402 SA1_DIM1

[14,27,29] PCH_SMB_CLK_3S
[14,27,29] PCH_SMB_DAT_3S

[10] SDDR_B_ODT0
[10] SDDR_B_ODT1

[10] SDDR_B_DM[0..7]

[10] SDDR_B_DQS[0..7]

[10] SDDR_B_DQS#[0..7]

DDR3_204P_3u

DIMM_1

DIMM_0

SLOT2B

CM15 330uF_TA_2.5V 7.3X4.3 NI
CM13 22uF_X5R_6.3V 0805 I
CM14 22uF_X5R_6.3V 0805 I
CM16 22uF_X5R_6.3V 0805 I

CM18 33pF_NPO_50V 0402 NI
CM19 100nF_X5R_6.3V 0402 I
CM20 100nF_X5R_6.3V 0402 I
CM21 100nF_X5R_6.3V 0402 I
CM22 100nF_X5R_6.3V 0402 I

CM8 33pF_NPO_50V 0402 NI
CM9 1uF_Y5V_6.3V 0402 I
CM10 1uF_Y5V_6.3V 0402 I
CM11 1uF_Y5V_6.3V 0402 I
CM12 1uF_Y5V_6.3V 0402 I
CM45 10uF_Y5V_10V 0805 I

Place between two SO-DIMM

CM1 2.2uF_X5R_10V 0603 I
CM2 100nF_X5R_6.3V 0402 I

RM3 SDDR_A_DQ_VREF0 0_5% 0402

CM4 2.2uF_X5R_10V 0603 I
CM5 100nF_X5R_6.3V 0402 I
CM6 2.2uF_X5R_10V 0603 I
CM7 100nF_X5R_6.3V 0402 I

[9] PM_EXTTS#1
[9] DDR3_DRAMRST#

CM23 2.2uF_X5R_10V 0603 I
CM24 100nF_X5R_6.3V 0402 I

RM9 SDDR_B_DQ_VREF1 0_5% 0402

CM25 2.2uF_X5R_10V 0603 I
CM26 100nF_X5R_6.3V 0402 I
CM27 2.2uF_X5R_10V 0603 I
CM28 100nF_X5R_6.3V 0402 I

CM36 22uF_X5R_6.3V 0805 I
CM37 22uF_X5R_6.3V 0805 I
CM38 22uF_X5R_6.3V 0805 I
CM35 330uF_TA_2.5V 7.3X4.3 NI

CM40 33pF_NPO_50V 0402 N
CM41 100nF_X5R_6.3V 0402 I
CM42 100nF_X5R_6.3V 0402 I
CM43 100nF_X5R_6.3V 0402 I
CM44 100nF_X5R_6.3V 0402 I

CM30 1uF_Y5V_6.3V 0402 I
CM31 1uF_Y5V_6.3V 0402 I
CM32 1uF_Y5V_6.3V 0402 I
CM33 1uF_Y5V_6.3V 0402 I
CM34 33pF_NPO_50V 0402 NI
CM46 10uF_Y5V_10V 0805 I

Place these Caps near So-DIMM1

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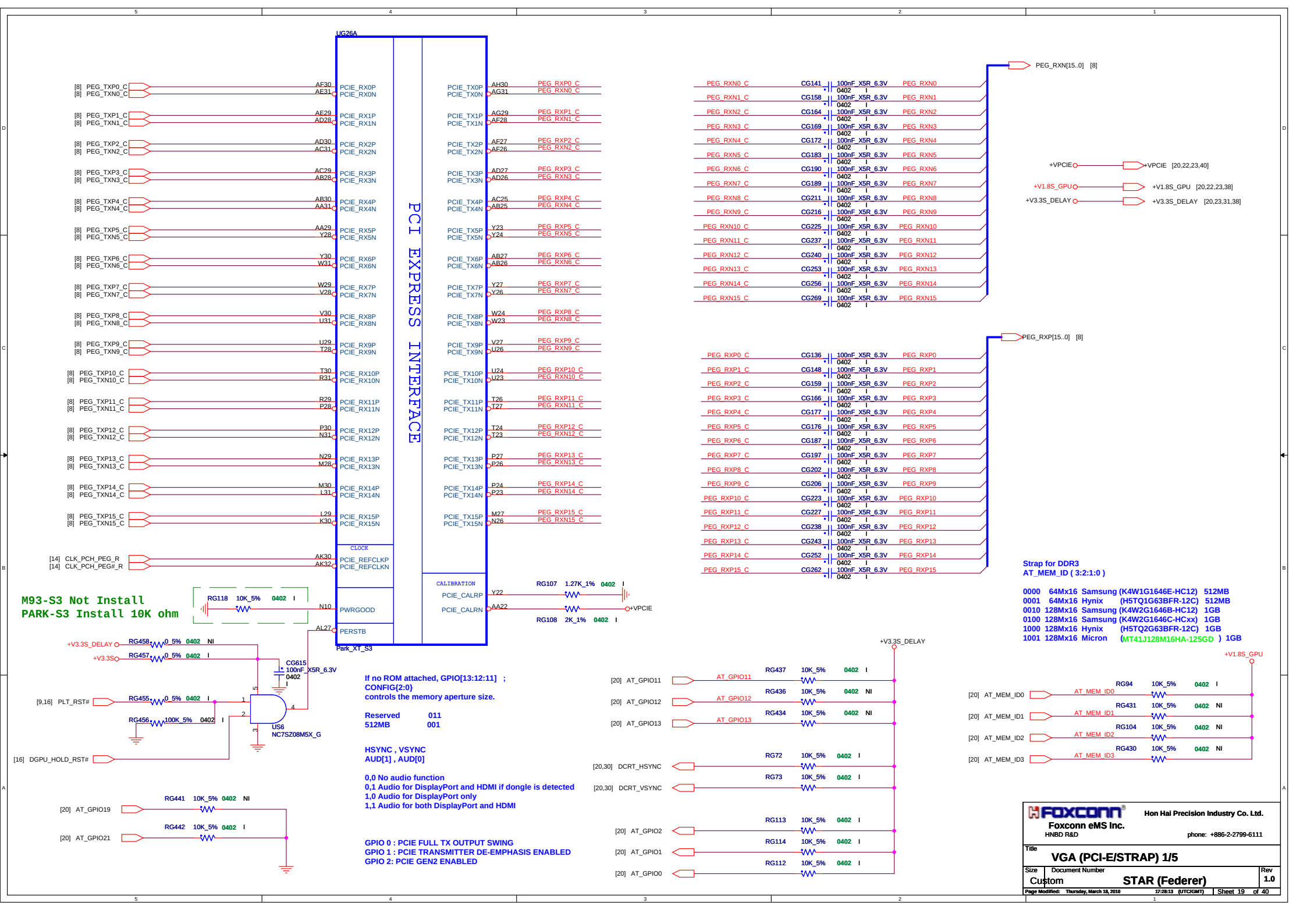
UG26A
PCI EXPRESS INTERFACE
[8] PEG_TXP0_C
[8] PEG_TXN0_C
AF30
AE31
PCIE_RX0P
PCIE_RX0N
PCIE_TX0P
PCIE_TX0N
AH30
AG31
PEG_RXP0_C
PEG_RXN0_C
[8] PEG_TXP1_C
[8] PEG_TXN1_C
AE29
AD28
PCIE_RX1P
PCIE_RX1N
PCIE_TX1P
PCIE_TX1N
AG29
AF28
PEG_RXP1_C
PEG_RXN1_C
[8] PEG_TXP2_C
[8] PEG_TXN2_C
AD30
AC31
PCIE_RX2P
PCIE_RX2N
PCIE_TX2P
PCIE_TX2N
AF27
AF26
PEG_RXP2_C
PEG_RXN2_C
[8] PEG_TXP3_C
[8] PEG_TXN3_C
AC29
AB28
PCIE_RX3P
PCIE_RX3N
PCIE_TX3P
PCIE_TX3N
AD27
AD26
PEG_RXP3_C
PEG_RXN3_C
[8] PEG_TXP4_C
[8] PEG_TXN4_C
AB30
AA31
PCIE_RX4P
PCIE_RX4N
PCIE_TX4P
PCIE_TX4N
AC25
AB25
PEG_RXP4_C
PEG_RXN4_C
[8] PEG_TXP5_C
[8] PEG_TXN5_C
AA29
Y28
PCIE_RX5P
PCIE_RX5N
PCIE_TX5P
PCIE_TX5N
Y23
Y24
PEG_RXP5_C
PEG_RXN5_C
[8] PEG_TXP6_C
[8] PEG_TXN6_C
Y30
W31
PCIE_RX6P
PCIE_RX6N
PCIE_TX6P
PCIE_TX6N
AB27
AB26
PEG_RXP6_C
PEG_RXN6_C
[8] PEG_TXP7_C
[8] PEG_TXN7_C
W29
V28
PCIE_RX7P
PCIE_RX7N
PCIE_TX7P
PCIE_TX7N
Y27
Y26
PEG_RXP7_C
PEG_RXN7_C
[8] PEG_TXP8_C
[8] PEG_TXN8_C
V30
U31
PCIE_RX8P
PCIE_RX8N
PCIE_TX8P
PCIE_TX8N
W24
W23
PEG_RXP8_C
PEG_RXN8_C
[8] PEG_TXP9_C
[8] PEG_TXN9_C
U29
T28
PCIE_RX9P
PCIE_RX9N
PCIE_TX9P
PCIE_TX9N
V27
U26
PEG_RXP9_C
PEG_RXN9_C
[8] PEG_TXP10_C
[8] PEG_TXN10_C
T30
R31
PCIE_RX10P
PCIE_RX10N
PCIE_TX10P
PCIE_TX10N
U24
U23
PEG_RXP10_C
PEG_RXN10_C
[8] PEG_TXP11_C
[8] PEG_TXN11_C
R29
P28
PCIE_RX11P
PCIE_RX11N
PCIE_TX11P
PCIE_TX11N
T26
T27
PEG_RXP11_C
PEG_RXN11_C
[8] PEG_TXP12_C
[8] PEG_TXN12_C
P30
N31
PCIE_RX12P
PCIE_RX12N
PCIE_TX12P
PCIE_TX12N
T24
T23
PEG_RXP12_C
PEG_RXN12_C
[8] PEG_TXP13_C
[8] PEG_TXN13_C
N29
M28
PCIE_RX13P
PCIE_RX13N
PCIE_TX13P
PCIE_TX13N
P27
P26
PEG_RXP13_C
PEG_RXN13_C
[8] PEG_TXP14_C
[8] PEG_TXN14_C
M30
L31
PCIE_RX14P
PCIE_RX14N
PCIE_TX14P
PCIE_TX14N
P24
P23
PEG_RXP14_C
PEG_RXN14_C
[8] PEG_TXP15_C
[8] PEG_TXN15_C
L29
K30
PCIE_RX15P
PCIE_RX15N
PCIE_TX15P
PCIE_TX15N
M27
N26
PEG_RXP15_C
PEG_RXN15_C
CLOCK
[14] CLK_PCH_PEG_R
[14] CLK_PCH_PEG#_R
AK30
AK32
PCIE_REFCLKP
PCIE_REFCLKN
CALIBRATION
PCIE_CALRP
PCIE_CALRN
Y22
AA22
RG107 1.27K_1% 0402
RG108 2K_1% 0402
+VPCIE
PWRGOOD
N10
PERSTB
AL27
Park_XT_S3
PEG_RXN[15..0] [8]
PEG_RXP[15..0] [8]
CG141 100nF_X5R_6.3V 0402
CG158 100nF_X5R_6.3V 0402
CG164 100nF_X5R_6.3V 0402
CG169 100nF_X5R_6.3V 0402
CG172 100nF_X5R_6.3V 0402
CG183 100nF_X5R_6.3V 0402
CG190 100nF_X5R_6.3V 0402
CG189 100nF_X5R_6.3V 0402
CG211 100nF_X5R_6.3V 0402
CG216 100nF_X5R_6.3V 0402
CG225 100nF_X5R_6.3V 0402
CG237 100nF_X5R_6.3V 0402
CG240 100nF_X5R_6.3V 0402
CG253 100nF_X5R_6.3V 0402
CG256 100nF_X5R_6.3V 0402
CG269 100nF_X5R_6.3V 0402
CG136 100nF_X5R_6.3V 0402
CG148 100nF_X5R_6.3V 0402
CG159 100nF_X5R_6.3V 0402
CG166 100nF_X5R_6.3V 0402
CG177 100nF_X5R_6.3V 0402
CG176 100nF_X5R_6.3V 0402
CG187 100nF_X5R_6.3V 0402
CG197 100nF_X5R_6.3V 0402
CG202 100nF_X5R_6.3V 0402
CG206 100nF_X5R_6.3V 0402
CG223 100nF_X5R_6.3V 0402
CG227 100nF_X5R_6.3V 0402
CG238 100nF_X5R_6.3V 0402
CG243 100nF_X5R_6.3V 0402
CG252 100nF_X5R_6.3V 0402
CG262 100nF_X5R_6.3V 0402
+VPCIE
+V1.8S_GPU
+V3.3S_DELAY
+VPCIE [20,22,23,40]
+V1.8S_GPU [20,22,23,38]
+V3.3S_DELAY [20,23,31,38]
M93-S3 Not Install
PARK-S3 Install 10K ohm
RG118 10K_5% 0402
+V3.3S_DELAY
+V3.3S
RG458 0_5% 0402 NI
RG457 0_5% 0402
CG615 100nF_X5R_6.3V 0402
[9,16] PLT_RST#
RG455 0_5% 0402
RG456 100K_5% 0402
US6 NC7SZ08M5X_G
[16] DGPU_HOLD_RST#
RG441 10K_5% 0402 NI
[20] AT_GPIO19
RG442 10K_5% 0402
[20] AT_GPIO21
If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.
Reserved 011
512MB 001
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
+V3.3S_DELAY
[20] AT_GPIO11
[20] AT_GPIO12
[20] AT_GPIO13
RG437 10K_5% 0402
RG436 10K_5% 0402 NI
RG434 10K_5% 0402 NI
[20,30] DCRT_HSYNC
[20,30] DCRT_VSYNC
RG72 10K_5% 0402
RG73 10K_5% 0402
[20] AT_GPIO2
[20] AT_GPIO1
[20] AT_GPIO0
RG113 10K_5% 0402
RG114 10K_5% 0402
RG112 10K_5% 0402
Strap for DDR3
AT_MEM_ID (3:2:1:0)
0000 64Mx16 Samsung (K4W1G1646E-HC12) 512MB
0001 64Mx16 Hynix (H5TQ1G63BFR-12C) 512MB
0010 128Mx16 Samsung (K4W2G1646B-HC12) 1GB
0100 128Mx16 Samsung (K4W2G1646C-HCxx) 1GB
1000 128Mx16 Hynix (H5TQ2G63BFR-12C) 1GB
1001 128Mx16 Micron (MT41J128M16HA-125GD) 1GB
+V1.8S_GPU
[20] AT_MEM_ID0
[20] AT_MEM_ID1
[20] AT_MEM_ID2
[20] AT_MEM_ID3
RG94 10K_5% 0402
RG431 10K_5% 0402 NI
RG104 10K_5% 0402 NI
RG430 10K_5% 0402 NI
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VGA (PCI-E/STRAP) 1/5
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Document Number
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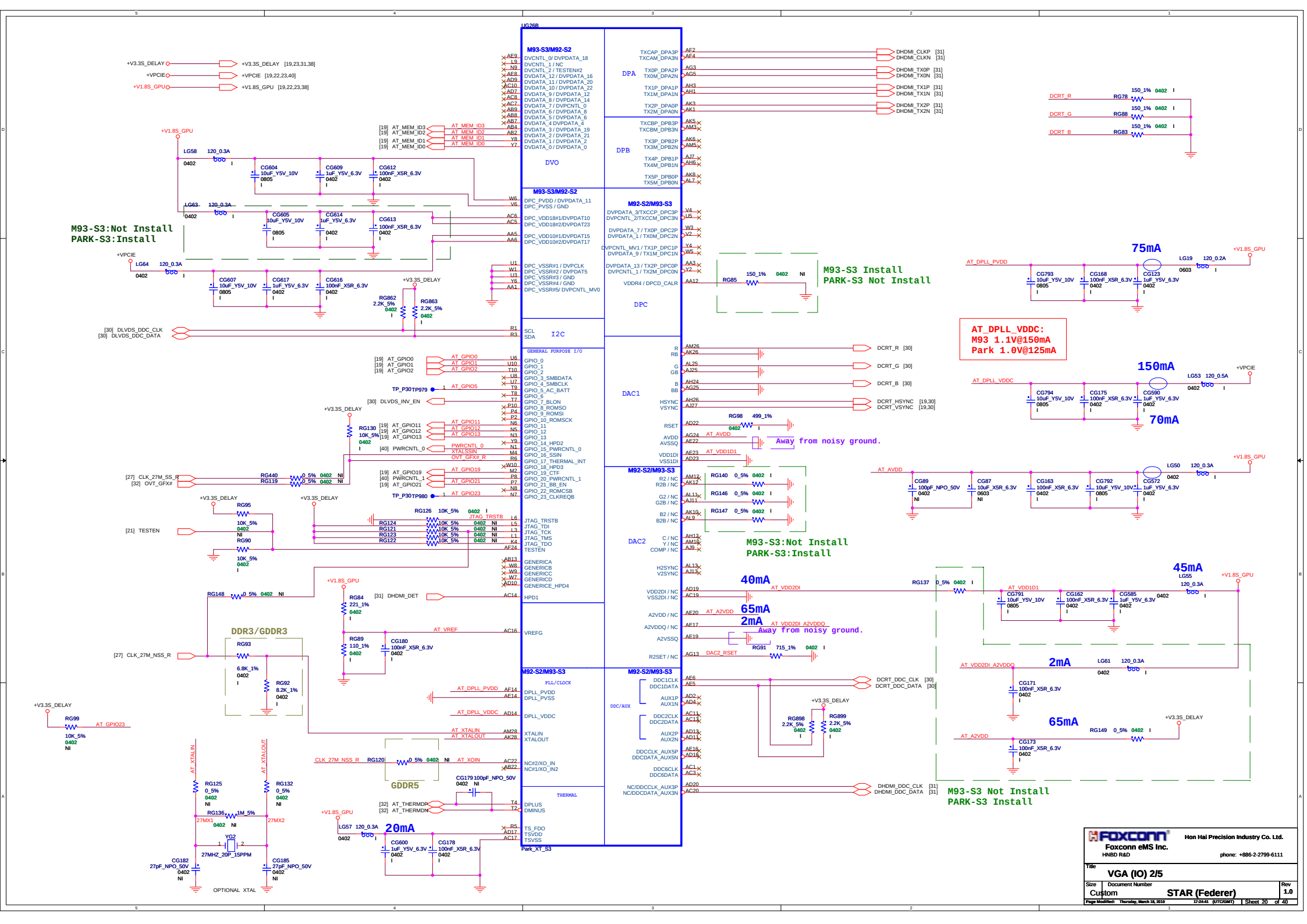
M93-S3:Not Install
PARK-S3:Install
M93-S3 Install
PARK-S3 Not Install
M93-S3:Not Install
PARK-S3:Install
M93-S3 Not Install
PARK-S3 Install
AT_DPLL_VDDC:
M93 1.1V@150mA
Park 1.0V@125mA
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
Away from noisy ground.
DDR3/GDDR3
GDDR5
OPTIONAL XTAL
Park_XT_S3
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Hon Hai Precision Industry Co. Ltd.
HNBD R&D
phone: +886-2-2799-6111
VGA (IO) 2/5
STAR (Federer)
Custom
Rev 1.0
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	M93_XT_S3	Park_XT_S3
RG139	100_1%	40.2_1%
MVREFD	0.75V	1.07V
RG143	100_1%	40.2_1%
MVREFS	0.75V	1.07V

+V1.5S → +V1.5S [23,24,38,40]

UG26F — Park_XT_S3

LVDS CONTROL
VARY_BL AB11 → DLVDS_PWM [30]
DIGON AB12 → DLVDS_VCC_EN [30]

TXCLK_UP_DPF3P / TXCLK_UN_DPF3N	AH20 / AJ19	DLVDS_U_CLKP [30] / DLVDS_U_CLKN [30]
TXOUT_U0P_DPF2P / TXOUT_U0N_DPF2N	AL21 / AK20	DLVDS_U_DP0 [30] / DLVDS_U_DN0 [30]
TXOUT_U1P_DPF1P / TXOUT_U1N_DPF1N	AH22 / AJ21	DLVDS_U_DP1 [30] / DLVDS_U_DN1 [30]
TXOUT_U2P_DPF0P / TXOUT_U2N_DPF0N	AL23 / AK22	DLVDS_U_DP2 [30] / DLVDS_U_DN2 [30]
TXOUT_U3P / TXOUT_U3N	AK24 / AJ23	

LVTMDP

TXCLK_LP_DPE3P / TXCLK_LN_DPE3N	AL15 / AK14	DLVDS_L_CLKP [30] / DLVDS_L_CLKN [30]
TXOUT_L0P_DPE2P / TXOUT_L0N_DPE2N	AH16 / AJ15	DLVDS_L_DP0 [30] / DLVDS_L_DN0 [30]
TXOUT_L1P_DPE1P / TXOUT_L1N_DPE1N	AL17 / AK16	DLVDS_L_DP1 [30] / DLVDS_L_DN1 [30]
TXOUT_L2P_DPE0P / TXOUT_L2N_DPE0N	AH18 / AJ17	DLVDS_L_DP2 [30] / DLVDS_L_DN2 [30]
TXOUT_L3P / TXOUT_L3N	AL19 / AK18	

[24] GDDR_A_DQ[63:0]

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

+V1.5S → RG139 40.2_1% 0402 I → MVREFD
RG135 100_1% 0402 I
CG274 100nF_X5R_6.3V 0402 I

+V1.5S → RG143 40.2_1% 0402 I → MVREFS
RG133 100_1% 0402 I
CG302 100nF_X5R_6.3V 0402 I

CLKTESTA
CLKTESTB
CG273 100nF_X5R_6.3V 0402 NI
CG280 100nF_X5R_6.3V 0402 NI
RG127 51_5% 0402 NI
RG134 51_5% 0402 NI

+V1.5S → RG128 240_1% 0402 I

M93-S3 No Install
PARK-S3 Install

[20] TESTEN → RG188 0_5% 0402 I

+V1.5S → RG145 2.2K_5% 0402 NI

[24] MEM_RST → RG142 680_5% 0402 I

CG781 68pF_NPO_50V 0402 I
RG141 10K_5% 0402 I

	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF

CLKTESTA
CLKTESTB
RG131 4.7K_5% 0402 NI
RG129 4.7K_5% 0402 NI
RG144 240_1% 0402 I
RG138 150_1% 0402 I

M93-S3 Install
PARK-S3 Not Install

M93-S3 Not Install
PARK-S3 Install

M93-S3 Install 240 ohm
PARK-S3 Install 150 ohm

UG26C — Park_XT_S3

MEMORY INTERFACE

DQA_0	K27	GDDR_A_DQ0
DQA_1	J29	GDDR_A_DQ1
DQA_2	H30	GDDR_A_DQ2
DQA_3	H32	GDDR_A_DQ3
DQA_4	G29	GDDR_A_DQ4
DQA_5	F28	GDDR_A_DQ5
DQA_6	F32	GDDR_A_DQ6
DQA_7	F30	GDDR_A_DQ7
DQA_8	C30	GDDR_A_DQ8
DQA_9	F27	GDDR_A_DQ9
DQA_10	A28	GDDR_A_DQ10
DQA_11	C28	GDDR_A_DQ11
DQA_12	E27	GDDR_A_DQ12
DQA_13	G26	GDDR_A_DQ13
DQA_14	D26	GDDR_A_DQ14
DQA_15	F25	GDDR_A_DQ15
DQA_16	A25	GDDR_A_DQ16
DQA_17	C25	GDDR_A_DQ17
DQA_18	E25	GDDR_A_DQ18
DQA_19	D24	GDDR_A_DQ19
DQA_20	F23	GDDR_A_DQ20
DQA_21	F23	GDDR_A_DQ21
DQA_22	D22	GDDR_A_DQ22
DQA_23	F21	GDDR_A_DQ23
DQA_24	E21	GDDR_A_DQ24
DQA_25	D20	GDDR_A_DQ25
DQA_26	F19	GDDR_A_DQ26
DQA_27	A19	GDDR_A_DQ27
DQA_28	D18	GDDR_A_DQ28
DQA_29	F17	GDDR_A_DQ29
DQA_30	A17	GDDR_A_DQ30
DQA_31	C17	GDDR_A_DQ31
DQA_32	E17	GDDR_A_DQ32
DQA_33	D16	GDDR_A_DQ33
DQA_34	F15	GDDR_A_DQ34
DQA_35	A15	GDDR_A_DQ35
DQA_36	D14	GDDR_A_DQ36
DQA_37	F13	GDDR_A_DQ37
DQA_38	A13	GDDR_A_DQ38
DQA_39	C13	GDDR_A_DQ39
DQA_40	E11	GDDR_A_DQ40
DQA_41	A11	GDDR_A_DQ41
DQA_42	C11	GDDR_A_DQ42
DQA_43	F11	GDDR_A_DQ43
DQA_44	A9	GDDR_A_DQ44
DQA_45	C9	GDDR_A_DQ45
DQA_46	F9	GDDR_A_DQ46
DQA_47	D8	GDDR_A_DQ47
DQA_48	E7	GDDR_A_DQ48
DQA_49	A7	GDDR_A_DQ49
DQA_50	C7	GDDR_A_DQ50
DQA_51	F7	GDDR_A_DQ51
DQA_52	A5	GDDR_A_DQ52
DQA_53	E5	GDDR_A_DQ53
DQA_54	C3	GDDR_A_DQ54
DQA_55	F1	GDDR_A_DQ55
DQA_56	G7	GDDR_A_DQ56
DQA_57	G6	GDDR_A_DQ57
DQA_58	G1	GDDR_A_DQ58
DQA_59	G3	GDDR_A_DQ59
DQA_60	J6	GDDR_A_DQ60
DQA_61	J1	GDDR_A_DQ61
DQA_62	J3	GDDR_A_DQ62
DQA_63	J5	GDDR_A_DQ63
MVREFDA	K26	MVREFD
MVREFSA	J26	MVREFS
MEM_CALRN0	J25	
NC/TESTEN#2	K7	
MEM_CALRP1/DPC_CALR	J8	
MEM_CALRP0	K25	
DRAM_RST	L10	
CLKTESTA	K8	CLKTESTA
CLKTESTB	L7	CLKTESTB

MAA_0	K17	GDDR_A_A0
MAA_1	J20	GDDR_A_A1
MAA_2	H23	GDDR_A_A2
MAA_3	G23	GDDR_A_A3
MAA_4	G24	GDDR_A_A4
MAA_5	H24	GDDR_A_A5
MAA_6	J19	GDDR_A_A6
MAA_7	K19	GDDR_A_A7
MAA_8	J14	GDDR_A_A8
MAA_9	K14	GDDR_A_A9
MAA_10	J11	GDDR_A_A10
MAA_11	J13	GDDR_A_A11
MAA_12	H11	GDDR_A_A12
MAA_13/BA2	G11	GDDR_A_BA2 [24]
MAA_14/BA0	J16	GDDR_A_BA0 [24]
MAA_15/BA1	L15	GDDR_A_BA1 [24]
		GDDR_A_A[12:0] [24]
		GDDR_A_DM[7:0] [24]

DQMA_0	E32	GDDR_A_DM0
DQMA_1	E30	GDDR_A_DM1
DQMA_2	A21	GDDR_A_DM2
DQMA_3	C21	GDDR_A_DM3
DQMA_4	E13	GDDR_A_DM4
DQMA_5	D12	GDDR_A_DM5
DQMA_6	E3	GDDR_A_DM6
DQMA_7	F4	GDDR_A_DM7

RDQSA_0	H28	GDDR_A_DQS0 → GDDR_A_DQS0 [24]
RDQSA_1	C27	GDDR_A_DQS1 → GDDR_A_DQS1 [24]
RDQSA_2	A23	GDDR_A_DQS2 → GDDR_A_DQS2 [24]
RDQSA_3	E19	GDDR_A_DQS3 → GDDR_A_DQS3 [24]
RDQSA_4	A17	GDDR_A_DQS4 → GDDR_A_DQS4 [24]
RDQSA_5	D10	GDDR_A_DQS5 → GDDR_A_DQS5 [24]
RDQSA_6	D6	GDDR_A_DQS6 → GDDR_A_DQS6 [24]
RDQSA_7	G5	GDDR_A_DQS7 → GDDR_A_DQS7 [24]
WDQSA_0	H27	GDDR_A_DQS#0 → GDDR_A_DQS#0 [24]
WDQSA_1	A27	GDDR_A_DQS#1 → GDDR_A_DQS#1 [24]
WDQSA_2	C23	GDDR_A_DQS#2 → GDDR_A_DQS#2 [24]
WDQSA_3	C19	GDDR_A_DQS#3 → GDDR_A_DQS#3 [24]
WDQSA_4	C15	GDDR_A_DQS#4 → GDDR_A_DQS#4 [24]
WDQSA_5	E9	GDDR_A_DQS#5 → GDDR_A_DQS#5 [24]
WDQSA_6	C5	GDDR_A_DQS#6 → GDDR_A_DQS#6 [24]
WDQSA_7	H4	GDDR_A_DQS#7 → GDDR_A_DQS#7 [24]

ODTA0	L18	GDDR_A_ODT0 → GDDR_A_ODT0 [24]
ODTA1	K16	GDDR_A_ODT1 → GDDR_A_ODT1 [24]
CLKA0	H26	GDDR_A_CLK0 → GDDR_A_CLK0 [24]
CLKA0B	H25	GDDR_A_CLK#0 → GDDR_A_CLK#0 [24]
CLKA1	G9	GDDR_A_CLK1 → GDDR_A_CLK1 [24]
CLKA1B	H9	GDDR_A_CLK#1 → GDDR_A_CLK#1 [24]
RASA0B	G22	GDDR_A_RAS#0 → GDDR_A_RAS#0 [24]
RASA1B	G17	GDDR_A_RAS#1 → GDDR_A_RAS#1 [24]
CASA0B	G19	GDDR_A_CAS#0 → GDDR_A_CAS#0 [24]
CASA1B	G16	GDDR_A_CAS#1 → GDDR_A_CAS#1 [24]
CSA0B_0	H22	GDDR_A_CS0_0# → GDDR_A_CS0_0# [24]
CSA0B_1	J22	
CSA1B_0	G13	GDDR_A_CS1_0# → GDDR_A_CS1_0# [24]
CSA1B_1	K13	
CKEA0	K20	GDDR_A_CKE0 → GDDR_A_CKE0 [24]
CKEA1	J17	GDDR_A_CKE1 → GDDR_A_CKE1 [24]
WEA0B	G25	GDDR_A_WE#0 → GDDR_A_WE#0 [24]
WEA1B	H10	GDDR_A_WE#1 → GDDR_A_WE#1 [24]
PX_EN	AB16	
RSVD#2	G14	
RSVD#3	G20	GDDR_A_A13_R → RG187 0_5% 0402 I → GDDR_A_A13 [24]

M93-S3 No Install
PARK-S3 Install

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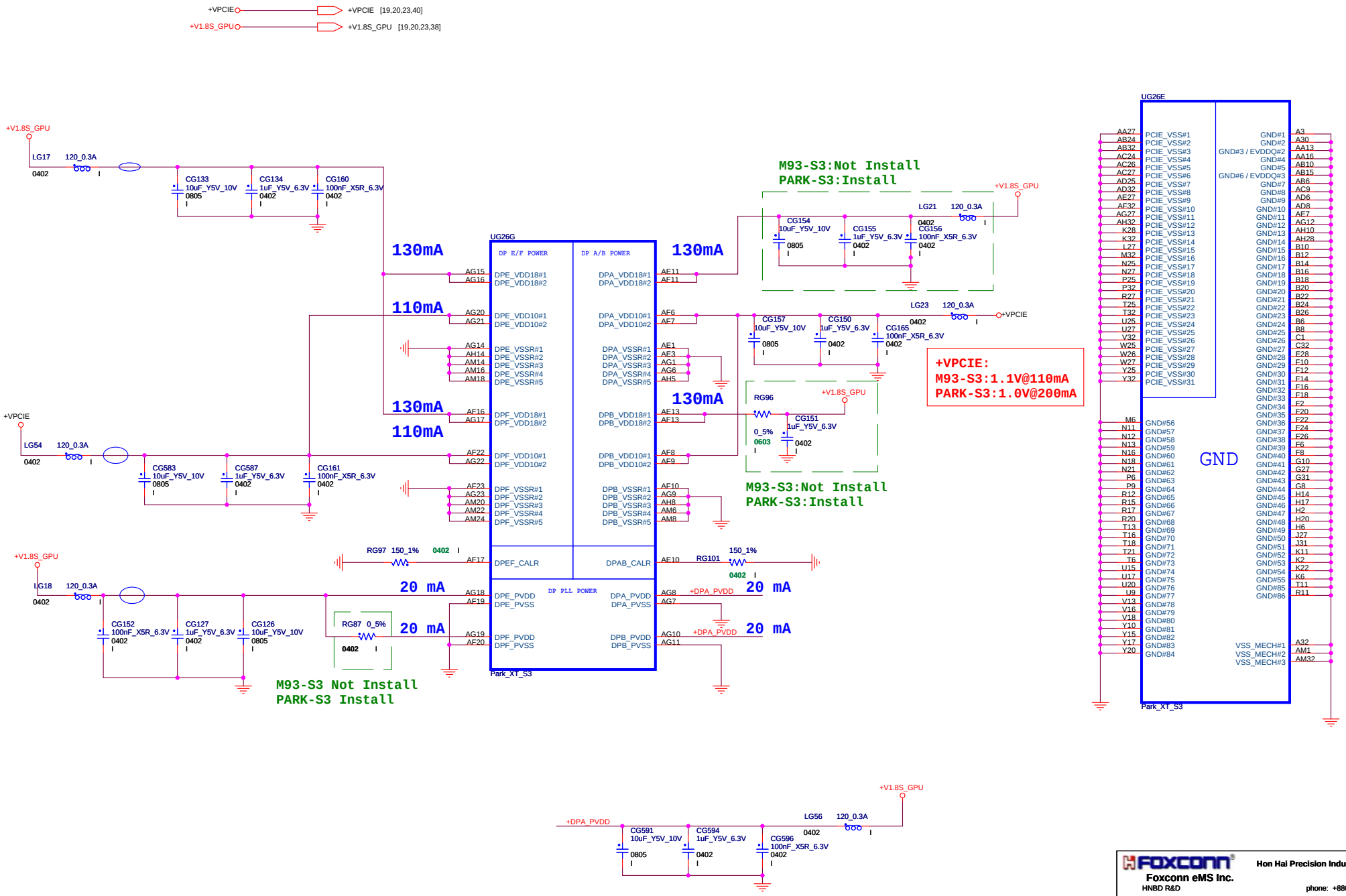

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Title: VGA (POWER) 4/5

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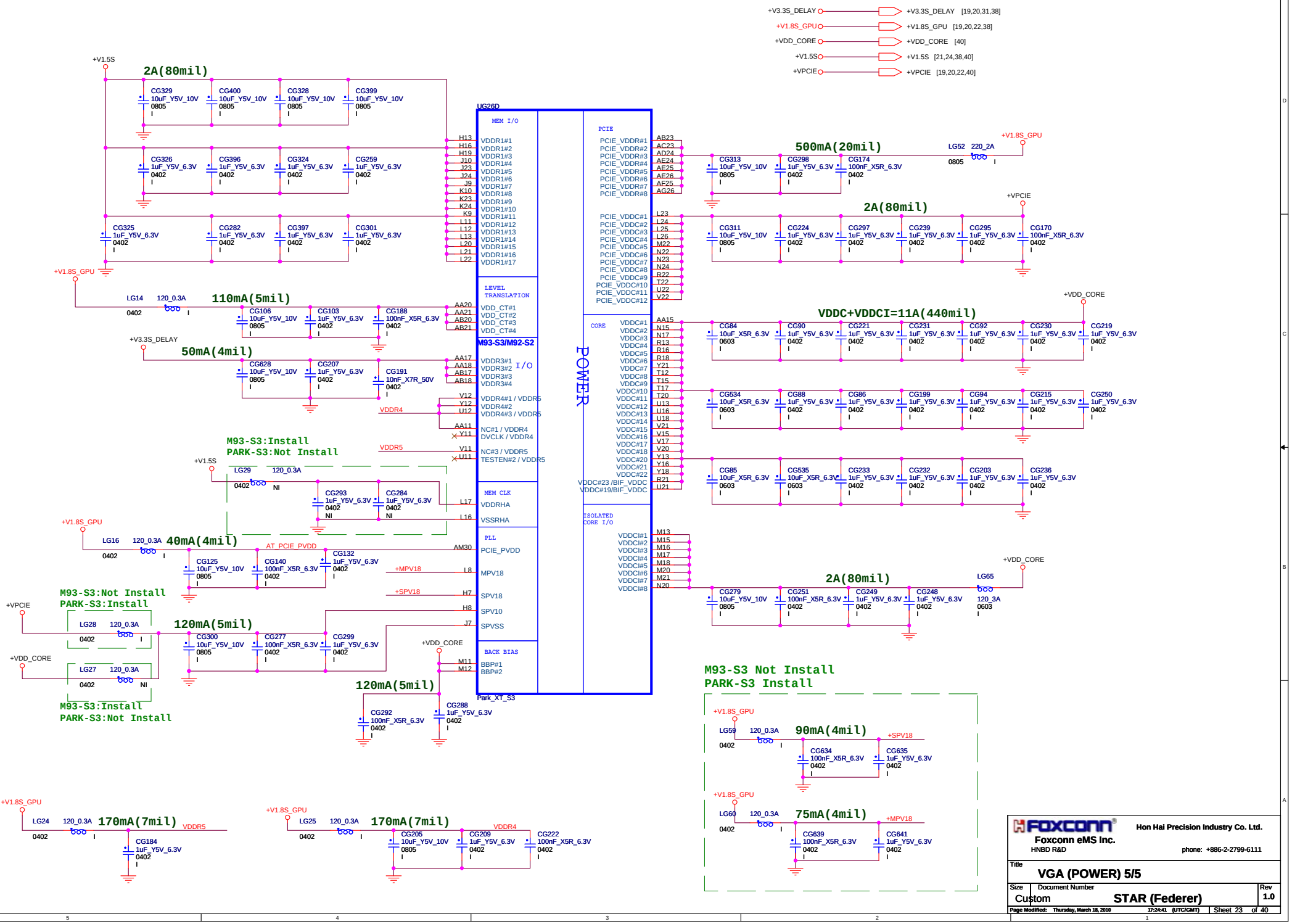
+V3.3S_DELAY +V3.3S_DELAY [19,20,31,38]
+V1.8S_GPU +V1.8S_GPU [19,20,22,38]
+VDD_CORE +VDD_CORE [40]
+V1.5S +V1.5S [21,24,38,40]
+VPCIE +VPCIE [19,20,22,40]
UG26D
MEM I/O
PCIE
LEVEL TRANSLATION
M93-S3/M92-S2 I/O
MEM CLK
PLL
BACK BIAS
CORE
ISOLATED CORE I/O
POWER
Park_XT_S3
2A(80mil)
110mA(5mil)
50mA(4mil)
40mA(4mil)
120mA(5mil)
500mA(20mil)
VDDC+VDDCI=11A(440mil)
M93-S3:Install
PARK-S3:Not Install
M93-S3:Not Install
PARK-S3:Install
M93-S3:Install
PARK-S3:Not Install
M93-S3 Not Install
PARK-S3 Install
90mA(4mil)
75mA(4mil)
170mA(7mil)
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VGA (POWER) 5/5
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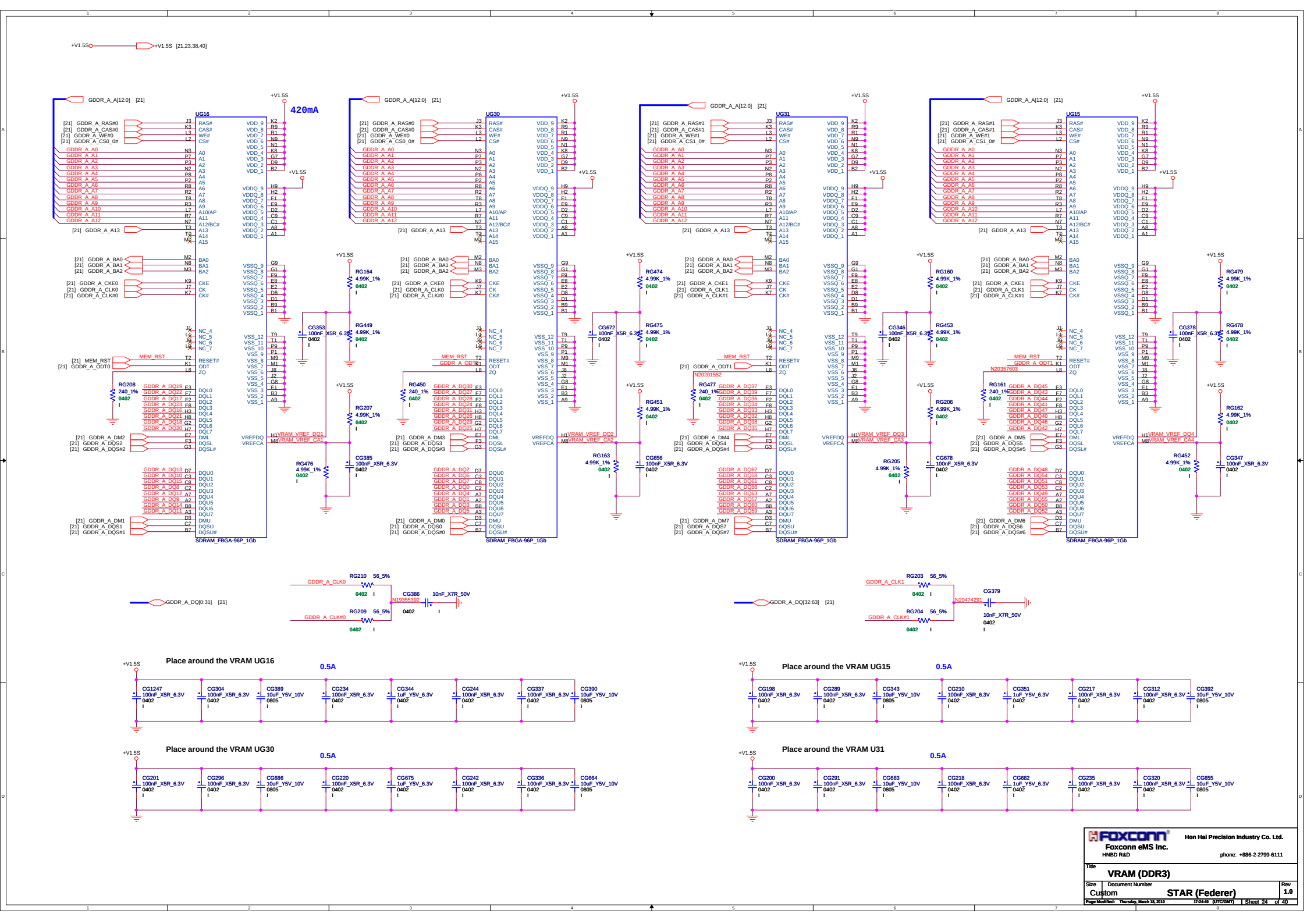
+V1.5S [21,23,38,40]
UG16
UG30
UG31
UG15
420mA
SDRAM_FBGA-96P_1Gb
Place around the VRAM UG16
Place around the VRAM UG15
Place around the VRAM UG30
Place around the VRAM UG31
0.5A
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VRAM (DDR3)
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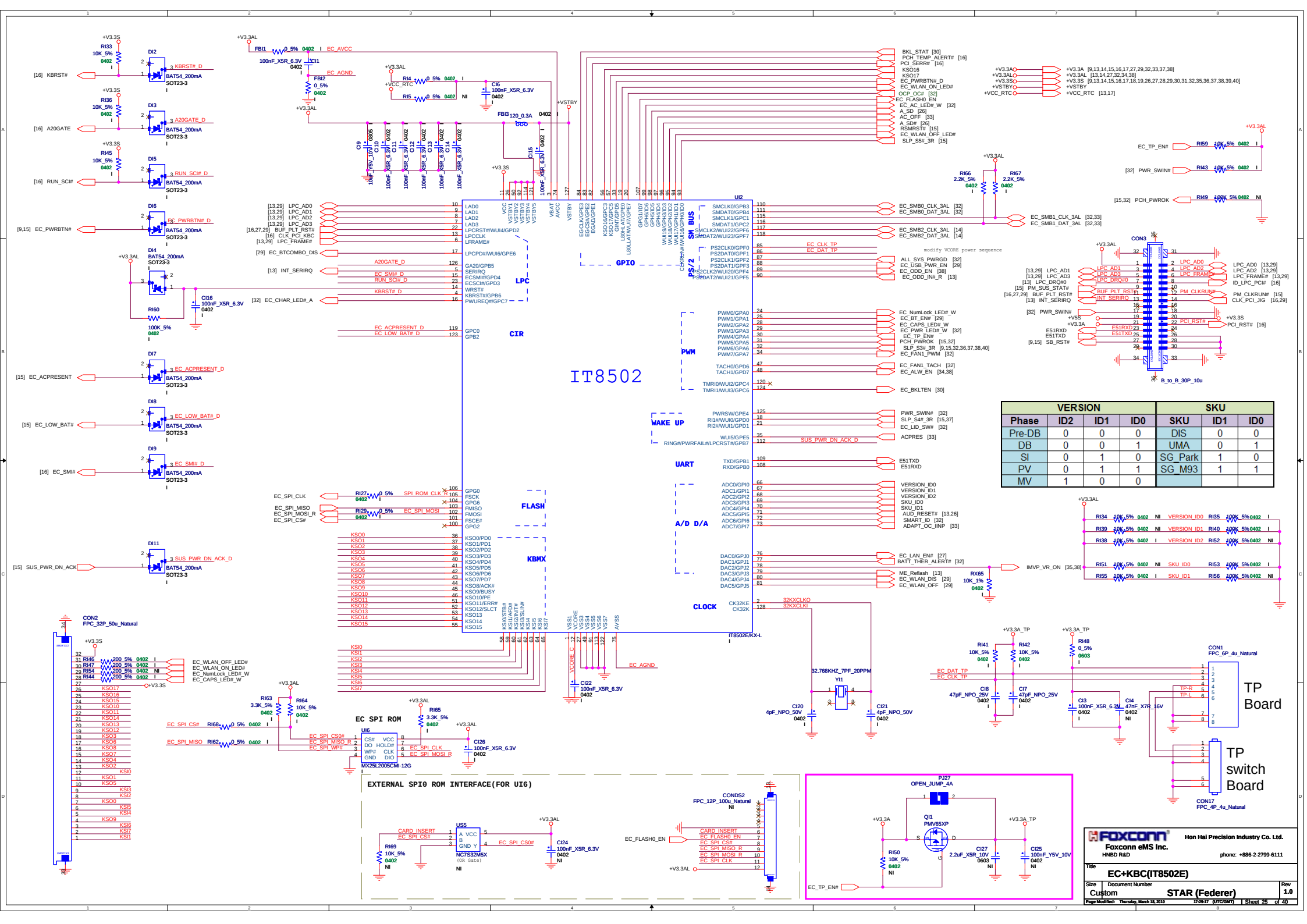
IT8502
LPC
CIR
PWM
GPIO
SM BUS
PS/2
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
EC SPI ROM
EXTERNAL SPI0 ROM INTERFACE(FOR UI6)
IT8502E/XX-L
TP Board
TP switch Board
VERSION
SKU
Phase
ID2
ID1
ID0
Pre-DB
DB
SI
PV
MV
SKU
DIS
UMA
SG_Park
SG_M93
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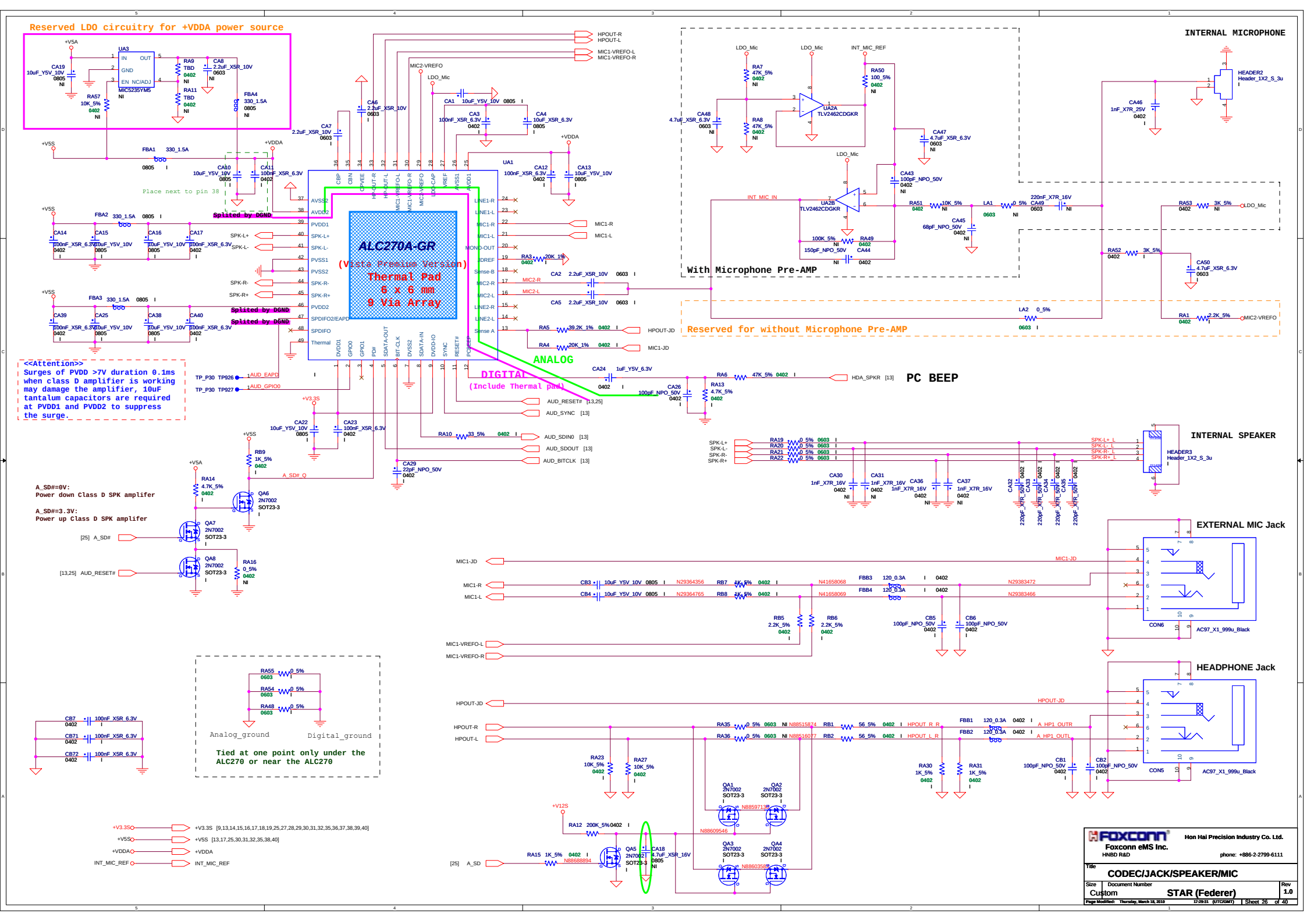
Reserved LDO circuitry for +VDDA power source
ALC270A-GR
(Vista Premium Version)
Thermal Pad
6 x 6 mm
9 Via Array
ANALOG
DIGITAL
(Include Thermal pad)
INTERNAL MICROPHONE
With Microphone Pre-AMP
Reserved for without Microphone Pre-AMP
PC BEEP
INTERNAL SPEAKER
EXTERNAL MIC Jack
HEADPHONE Jack
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.
A_SD#=0V:
Power down Class D SPK amplifer
A_SD#=3.3V:
Power up Class D SPK amplifer
Analog_ground
Digital_ground
Tied at one point only under the ALC270 or near the ALC270
Splited by DGND
Place next to pin 38
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Hon Hai Precision Industry Co. Ltd.
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CODEC/JACK/SPEAKER/MIC
Custom
STAR (Federer)
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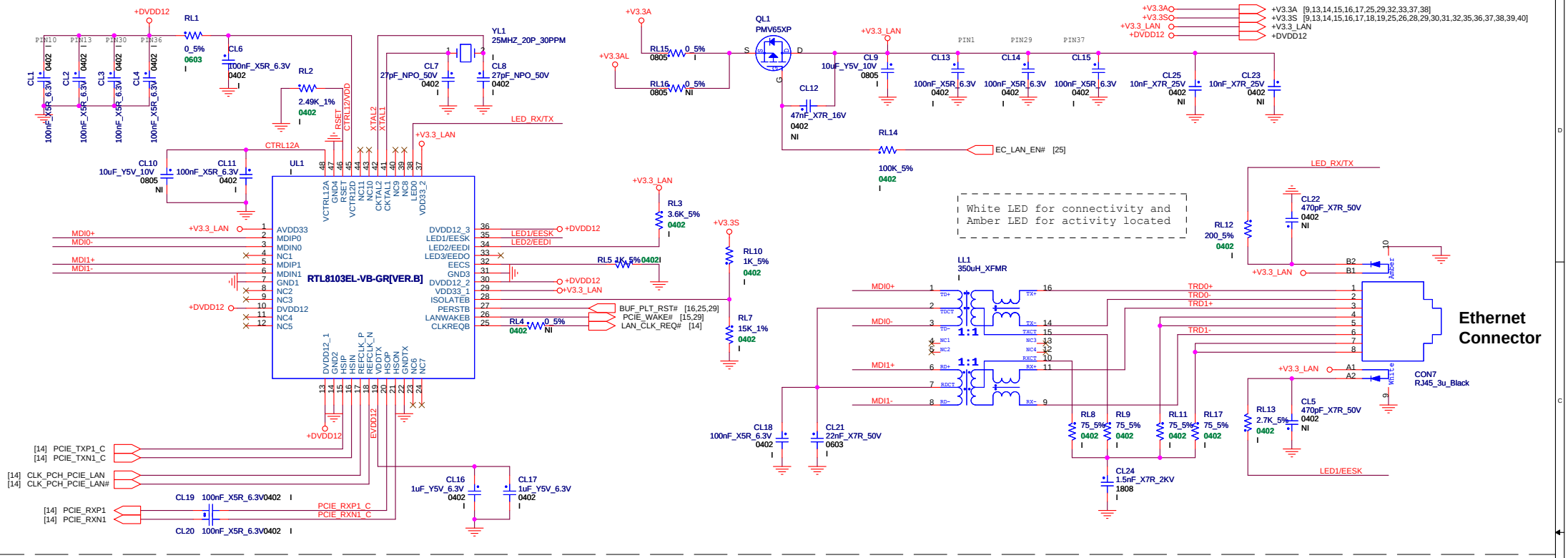

FSP Table

FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

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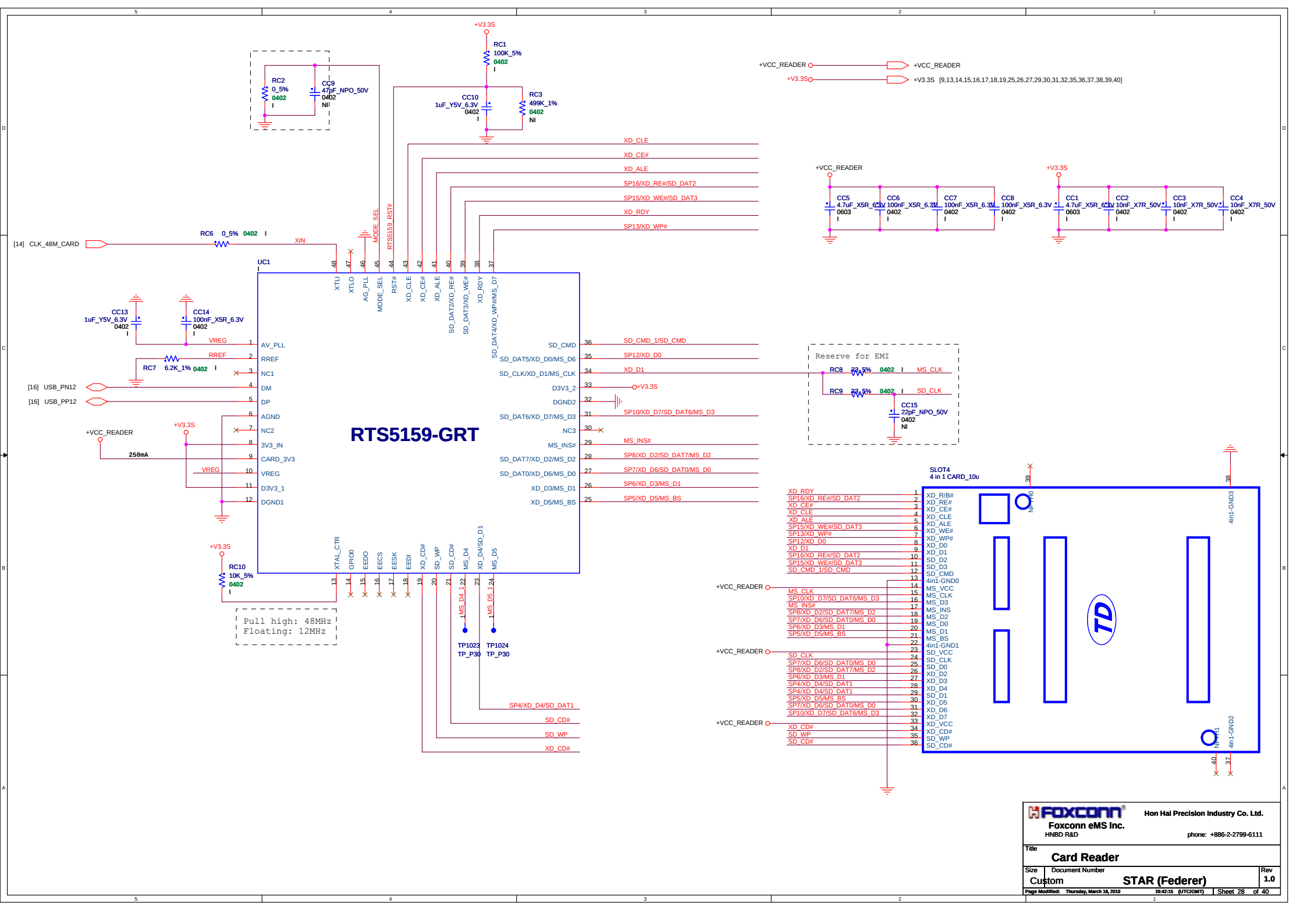
RTS5159-GRT
UC1
RC1 100K_5% 0402 I
RC2 0_5% 0402 I
CC9 47pF_NPO_50V 0402 NI
CC10 1uF_Y5V_6.3V 0402 I
RC3 499K_1% 0402 NI
RC6 0_5% 0402 I
RC7 6.2K_1% 0402 I
RC10 10K_5% 0402 I
CC13 1uF_Y5V_6.3V 0402 I
CC14 100nF_X5R_6.3V 0402 I
CC5 4.7uF_X5R_6.3V 0603 I
CC6 100nF_X5R_6.3V 0402 I
CC7 100nF_X5R_6.3V 0402 I
CC8 100nF_X5R_6.3V 0402 I
CC1 4.7uF_X5R_6.3V 0603 I
CC2 10nF_X7R_50V 0402 I
CC3 10nF_X7R_50V 0402 I
CC4 10nF_X7R_50V 0402 I
CC15 22pF_NPO_50V 0402 NI
RC8 33_5% 0402 I
RC9 33_5% 0402 I
Reserve for EMI
SLOT4
4 in 1 CARD_10u
TP1023 TP_P30
TP1024 TP_P30
Pull high: 48MHz
Floating: 12MHz
250mA
+V3.3S
+VCC_READER
[14] CLK_48M_CARD
[16] USB_PN12
[16] USB_PP12
XIN
VREG
RREF
MODE_SEL
RTS5159_RST#
XD_CLE
XD_CE#
XD_ALE
SP16/XD_RE#/SD_DAT2
SP15/XD_WE#/SD_DAT3
XD_RDY
SP13/XD_WP#
SD_CMD_1/SD_CMD
SP12/XD_D0
XD_D1
SP10/XD_D7/SD_DAT6/MS_D3
MS_INS#
SP8/XD_D2/SD_DAT7/MS_D2
SP7/XD_D6/SD_DAT0/MS_D0
SP6/XD_D3/MS_D1
SP5/XD_D5/MS_BS
SP4/XD_D4/SD_DAT1
SD_CD#
SD_WP
XD_CD#
MS_CLK
SD_CLK
4in1-GND3
4in1-GND2
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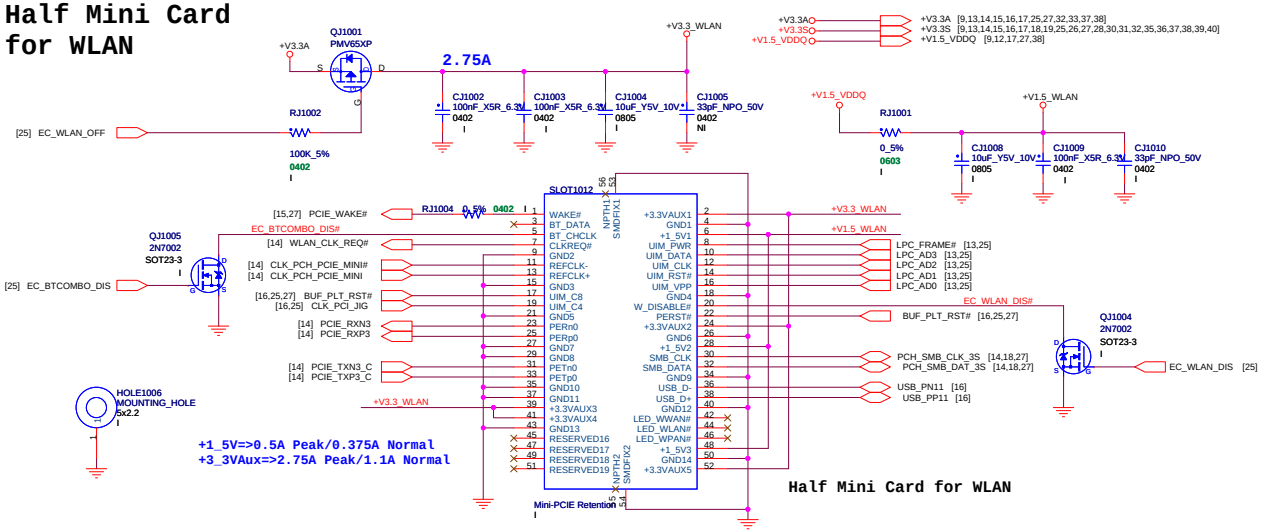
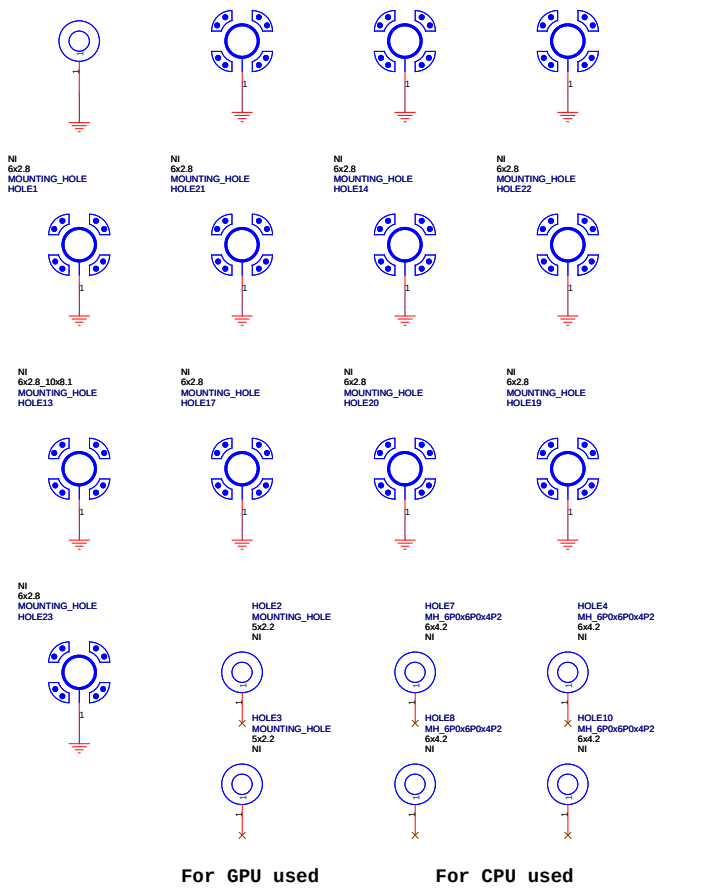
Half Mini Card for WLAN



Half Mini Card for WLAN

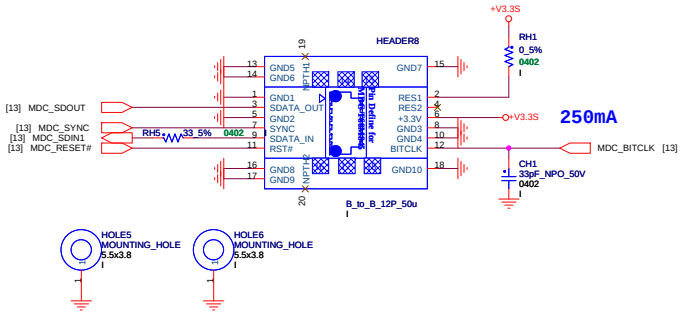
MOUNTING HOLE



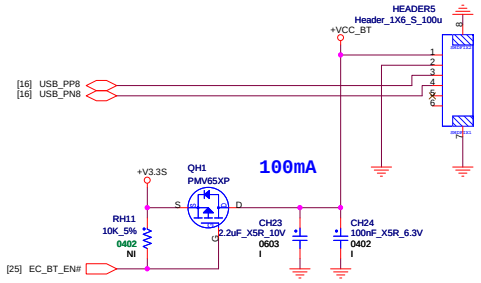
For GPU used

For CPU used

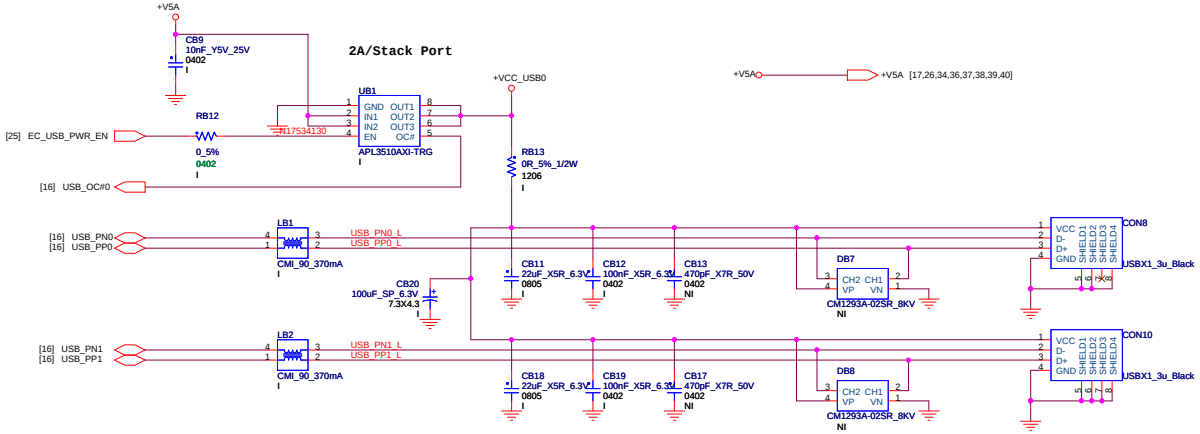
MDC CONN.



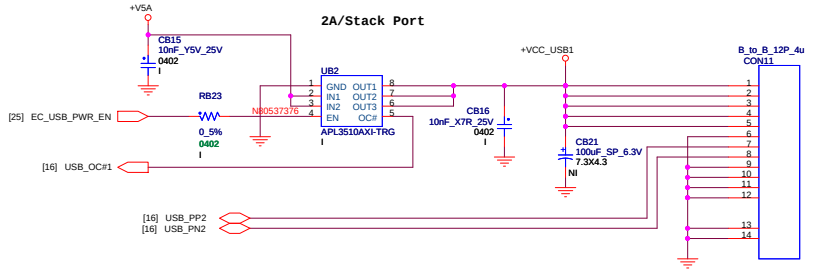
Bluetooth CONN.



USBX2 CONN.



USBX1 CONN.



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Title: WLAN/BT/MDC/USB/MOUNTING HOLE

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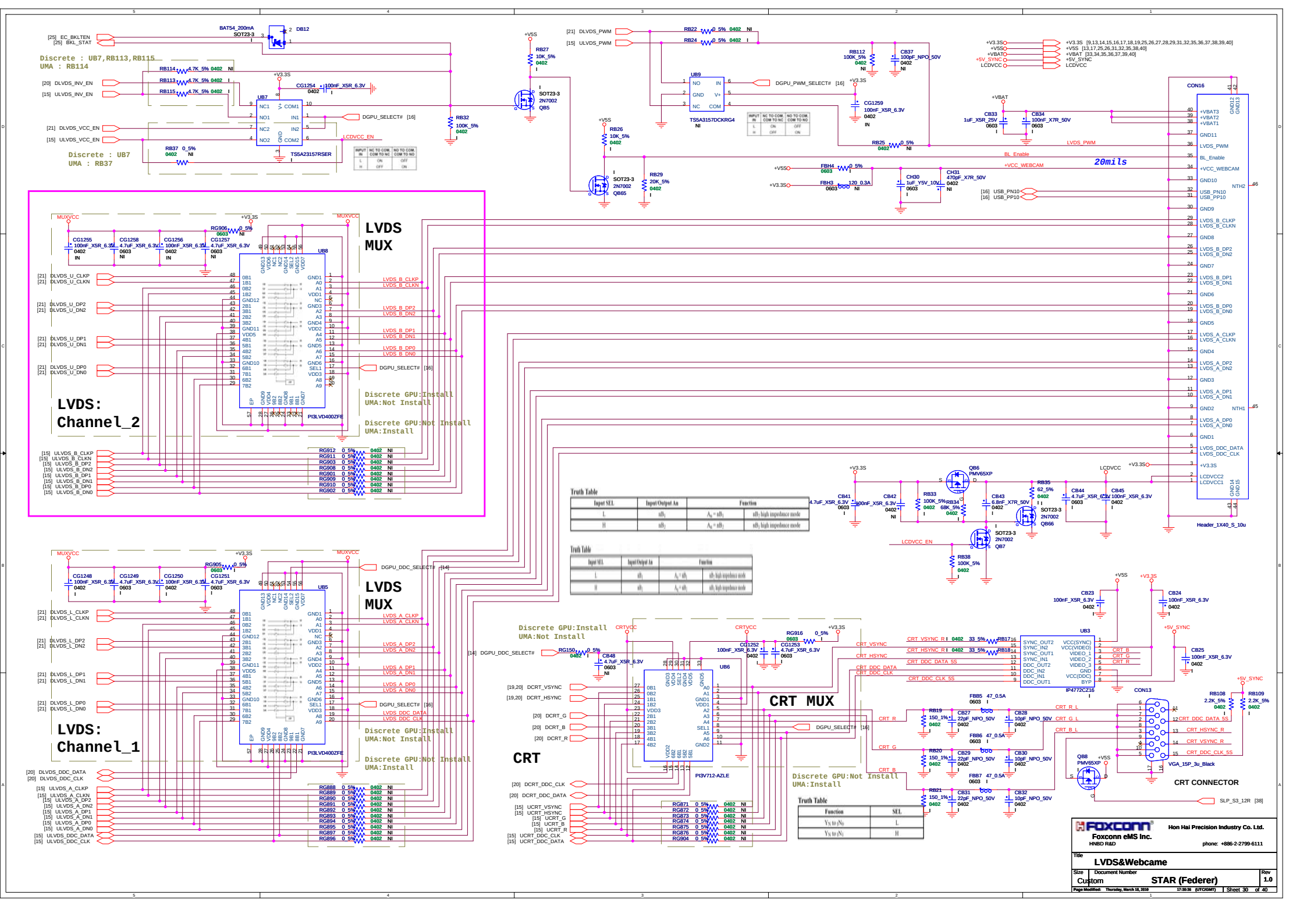
LVDS MUX
LVDS: Channel_2
LVDS MUX
LVDS: Channel_1
CRT MUX
CRT
CRT CONNECTOR
Discrete : UB7,RB113,RB115
UMA : RB114
Discrete : UB7
UMA : RB37
Discrete GPU:Install
UMA:Not Install
Discrete GPU:Not Install
UMA:Install
20mils
Truth Table
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LVDS&Webcame
Custom
STAR (Federer)
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Discrete GPU: Install
UMA: Not Install

+V5S
DB13 BAT54_200mA SOT23-3
CB75 10nF_X7R_25V 0402 NI
CB76 10nF_X7R_25V 0402 NI
+V3.3S_DELAY
RB41 2.2K_5% 0402
RB42 2.2K_5% 0402
RB43 2.2K_5% 0402
RB44 2.2K_5% 0402
[20] DHDMI_DDC_DATA
[20] DHDMI_DDC_CLK
HDMI_DDC_DATA
HDMI_DDC_CLK
QB67 2N7002 SOT23-3
QB9 2N7002 SOT23-3
[16] DGPU_HPD_INTR#
QB10 2N7002 SOT23-3
QB2 MMBT3904_G SOT23-3
HDMI_DET_5_R
RB45 200K_1% 0402
HDMI_DET_5
[20] DHDMI_DET
RB83 0_5% 0402
RB39 10K_5% 0402

+V5S [13,17,25,26,30,32,35,38,40]
+V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,32,35,36,37,38,39,40]
+V3.3S_DELAY [19,20,23,38]
+V5S_HDMI
+V3.3S_HDMI

RB51 0_5% 0603 NI
LB6 90Ohm@100MHz
RB55 0_5% 0603 NI
RB52 0_5% 0603 NI
LB5 90Ohm@100MHz
RB54 0_5% 0603 NI
RB47 0_5% 0603 NI
LB3 90Ohm@100MHz
RB48 0_5% 0603 NI
RB49 0_5% 0603 NI
LB4 90Ohm@100MHz
RB50 0_5% 0603 NI
HDMI_CLKN
HDMI_CLKP
HDMI_TX1N
HDMI_TX1P
HDMI_TX2P
HDMI_TX2N
HDMI_TX0P
HDMI_TX0N
HDMI_TX2P_L
HDMI_TX2N_L
HDMI_TX0P_L
HDMI_TX0N_L
HDMI_CEC
HDMI_DDC_CLK
HDMI_DET_5
TP1025 TP_P30
DB22 PESD24VS1UL SOD882-2
CB74 180pF_NPO_50V 0402 NI

CON15
Data2+ Data2- TMDS Data1 Shield
Data0+ Data0- TMDS Clock Shield
CEC SCL DDC/CEC Ground Hot Plug Detect PTH1
TMDS Data2 Shield Data1+ Data1-
TMDS Data0 Shield TMDS Clock+ TMDS Clock-
Reserved SDA +5V Power PTH2
HDMI_R_19P_999u_Black

HDMI_TX1P_L
HDMI_TX1N_L
HDMI_CLKP_L
HDMI_CLKN_L
HDMI_DDC_DATA
CB58 180pF_NPO_50V 0402 NI
CB57 100nF_X5R_6.3V 0402
DB15 B340A-13-F_3A SOD123-2

HDMI spec:
+5V:4.7V min ,
55mA max.

[20] DHDMI_TX2P
[20] DHDMI_TX2N
CB63 0402 100nF_X5R_6.3V
CB64 0402 100nF_X5R_6.3V
[20] DHDMI_TX1P
[20] DHDMI_TX1N
CB65 0402 100nF_X5R_6.3V
CB66 0402 100nF_X5R_6.3V
[20] DHDMI_TX0P
[20] DHDMI_TX0N
CB67 0402 100nF_X5R_6.3V
CB68 0402 100nF_X5R_6.3V
[20] DHDMI_CLKP
[20] DHDMI_CLKN
CB69 0402 100nF_X5R_6.3V
CB70 0402 100nF_X5R_6.3V

RB84 499_1% 0402
RB85 499_1% 0402
RB88 499_1% 0402
RB89 499_1% 0402
RB92 499_1% 0402
RB93 499_1% 0402
RB97 499_1% 0402
RB98 499_1% 0402
CB35 22pF_NPO_50V 0402
QB63 2N7002 SOT23-3
RB100 100K_5% 0402

Discrete GPU:Not Install
UMA:Install

+V3.3S
FBB9 0_5% 0603 NI
+V3.3S_HDMI
CB52 10nF_X7R_25V 0402 NI
CB53 10nF_X7R_25V 0402 NI
CB54 100nF_X5R_6.3V 0402 NI
CB55 100nF_X5R_6.3V 0402 NI
CB51 10uF_Y5V_10V 0805 NI
CB46 100nF_X5R_6.3V 0402 NI
CB47 100nF_X5R_6.3V 0402 NI
CB50 100nF_X7R_25V 0402 NI
CB56 100nF_X5R_6.3V 0402 NI
RB53 2.2K_5% 0402 NI
HDMI_DET_5
HDMI_DDC_DATA
HDMI_DDC_CLK
OE#
RB46 10K_5% 0402 NI
QB64 2N7002 SOT23-3 NI
HDMI_DET_5_R

UB4
GND_8 NC_4 NC_3 VDD_6 DDC_EN GND_7 HPD_SINK SCL_SINK SDA_SINK GND_6 VDD_5 OE#
GND_9 IN_D1- IN_D1+ VDD_7 IN_D2- IN_D2+ GND_10 IN_D3- IN_D3+ VDD_8 IN_D4- IN_D4+ GND_11
GND_5 OUT_D1- OUT_D1+ VDD_4 OUT_D2- OUT_D2+ GND_4 OUT_D3- OUT_D3+ VDD_3 OUT_D4- OUT_D4+
GND_1 VDD_1 NC_0 NC_1 GND_2 REXT HPD_SOURCE SDA_SOURCE SCL_SOURCE NC_2 VDD_2 GND_3
PTN3360BBS

[15] UTMDS_TX2P_C
[15] UTMDS_TX2N_C
[15] UTMDS_TX1P_C
[15] UTMDS_TX1N_C
[15] UTMDS_TX0P_C
[15] UTMDS_TX0N_C
[15] UTMDS_CLKP_C
[15] UTMDS_CLKN_C
UHDMI_TX2P RB56 0_5% 0402 NI HDMI_TX2P
UHDMI_TX2N RB57 0_5% 0402 NI HDMI_TX2N
UHDMI_TX1P RB58 0_5% 0402 NI HDMI_TX1P
UHDMI_TX1N RB59 0_5% 0402 NI HDMI_TX1N
UHDMI_TX0P RB60 0_5% 0402 NI HDMI_TX0P
UHDMI_TX0N RB61 0_5% 0402 NI HDMI_TX0N
UHDMI_CLKP RB62 0_5% 0402 NI HDMI_CLKP
UHDMI_CLKN RB63 0_5% 0402 NI HDMI_CLKN

[15] UHDMI_DET
RB106 100K_5% 0402 NI
RB73 2.2K_5% 0402 NI
RB71 2.2K_5% 0402 NI
RB77 10K_1% 0402 NI
[15] UTMDS_DDC_DATA
[15] UTMDS_DDC_CLK

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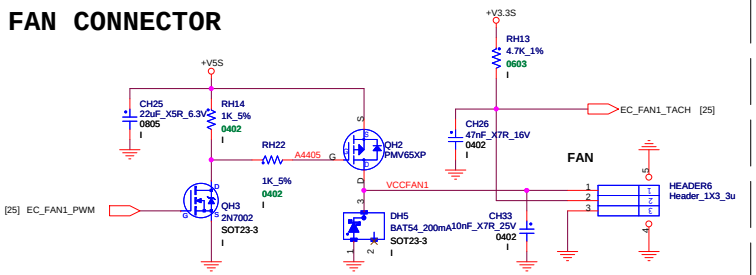
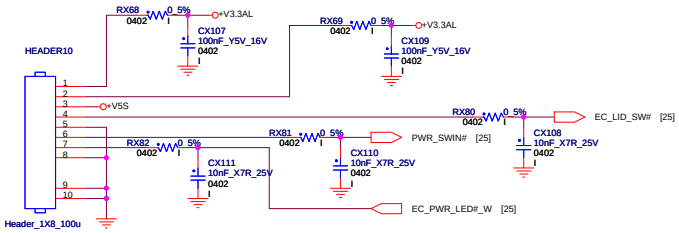
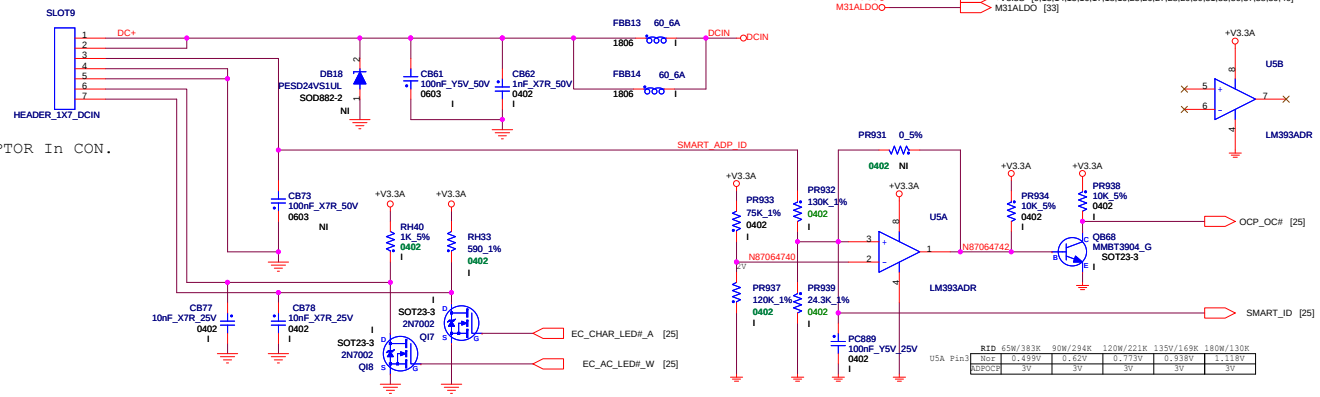
FAN CONNECTOR



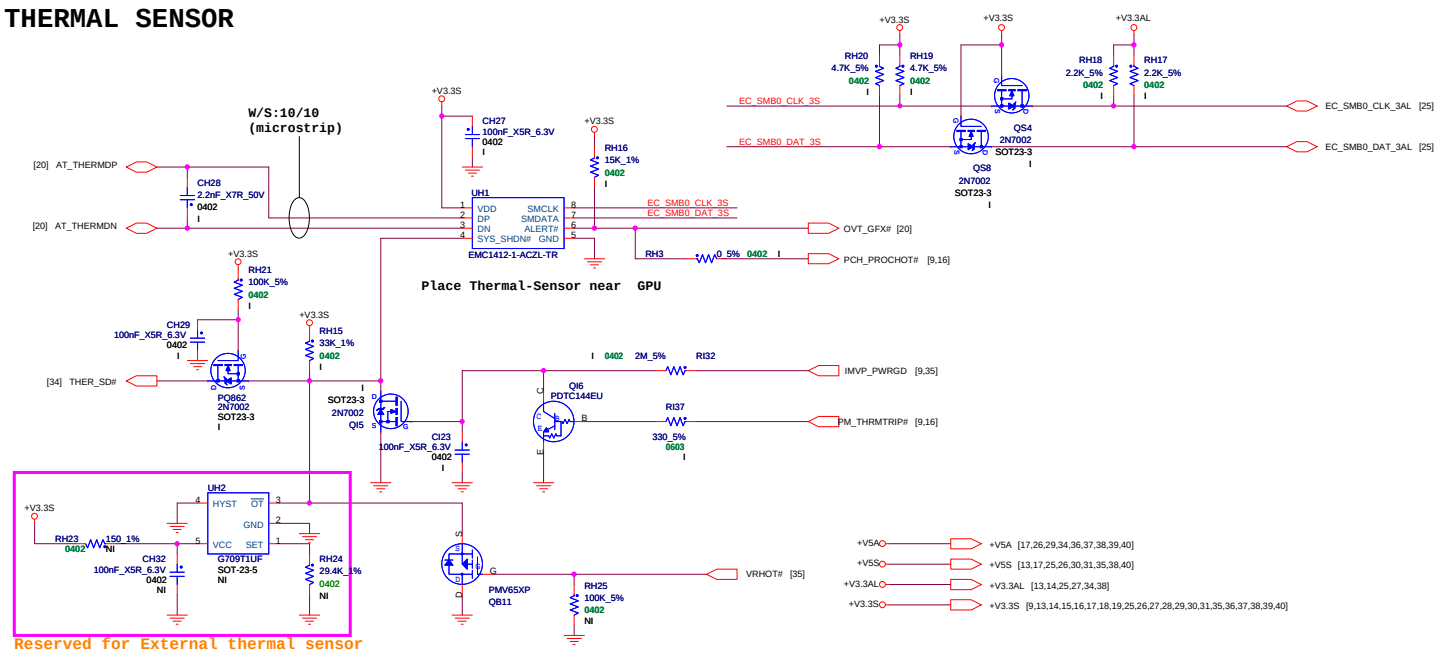
POWER BUTTON BOARD CONNECTOR



DC_JACK Wire to Board Connector

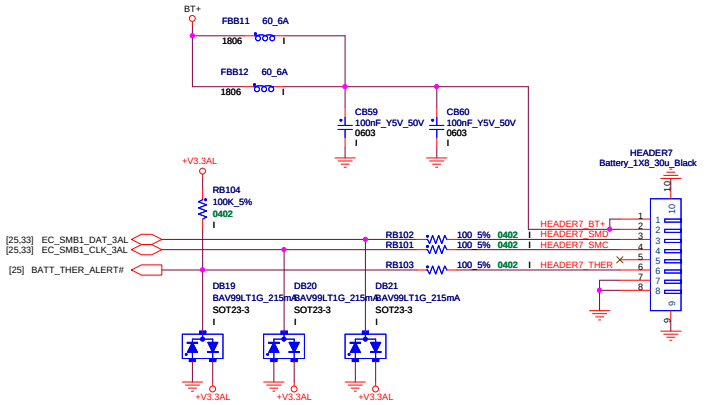


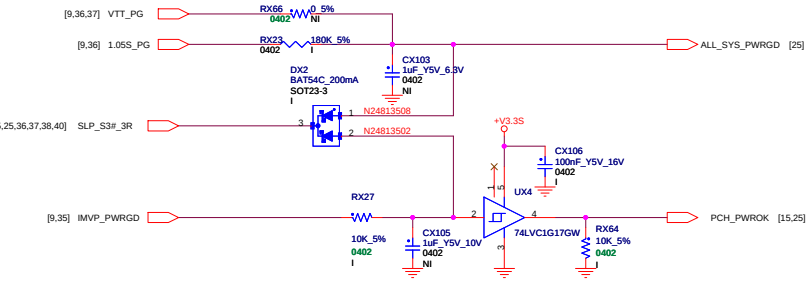
THERMAL SENSOR



Reserved for External thermal sensor

BATTERY CONNECTOR





Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin.
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

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Title: DCIN/Battery/OCP/FAN

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Custom	STAR (Federer)	1.0

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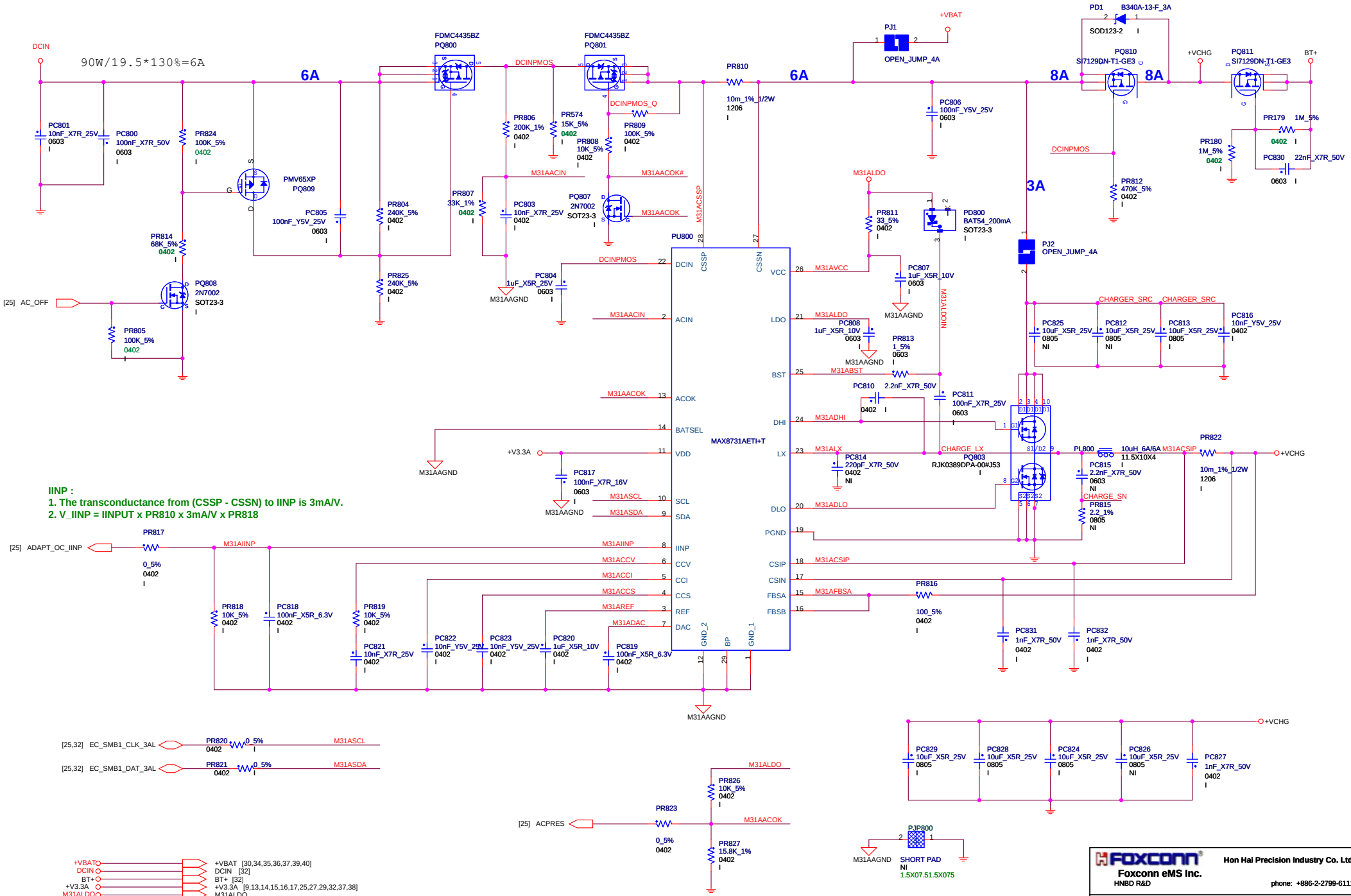
DCIN
90W/19.5*130%=6A
6A
FDMC4435BZ
PQ800
FDMC4435BZ
PQ801
DCINPMOS
PR810
10m_1%_1/2W
1206
6A
PJ1
OPEN_JUMP_4A
+VBAT
PD1
B340A-13-F_3A
SOD123-2
8A
PQ810
SI7129DN-T1-GE3
8A
+VCHG
PQ811
SI7129DN-T1-GE3
BT+
PC801
10nF_X7R_25V
0603
PC800
100nF_X7R_50V
0603
PR824
100K_5%
0402
PMV65XP
PQ809
PR806
200K_1%
0402
PR574
15K_5%
0402
PR808
10K_5%
0402
DCINPMOS_Q
PR809
100K_5%
0402
PC806
100nF_Y5V_25V
0603
DCINPMOS
PR812
470K_5%
0402
PR179
1M_5%
0402
PR180
1M_5%
0402
PC830
22nF_X7R_50V
0603
PR807
33K_1%
0402
M31AACIN
M31AACOK#
PQ807
2N7002
SOT23-3
M31AACOK
PC803
10nF_X7R_25V
0402
PC805
100nF_Y5V_25V
0603
PR804
240K_5%
0402
PR825
240K_5%
0402
M31ALDO
PR811
33_5%
0402
PD800
BAT54_200mA
SOT23-3
3A
PJ2
OPEN_JUMP_4A
PR814
68K_5%
0402
PQ808
2N7002
SOT23-3
[25] AC_OFF
PR805
100K_5%
0402
PC804
1uF_X5R_25V
0603
M31AAGND
PU800
MAX8731AETI+T
M31ACSSP
M31ACSSN
DCIN
CSSP
CSSN
VCC
M31AVCC
PC807
1uF_X5R_10V
0603
M31AAGND
M31ALDOIN
CHARGER_SRC
CHARGER_SRC
PC825
10uF_X5R_25V
0805
NI
PC812
10uF_X5R_25V
0805
NI
PC813
10uF_X5R_25V
0805
PC816
10nF_Y5V_25V
0402
ACIN
LDO
M31ALDO
PC808
1uF_X5R_10V
0603
M31AAGND
PR813
1_5%
0603
BST
M31ABST
PC810
2.2nF_X7R_50V
0402
PC811
100nF_X7R_25V
0603
ACOK
M31AACOK
DHI
M31ADHI
BATSEL
+V3.3A
PC817
100nF_X7R_16V
0603
M31AAGND
VDD
LX
M31ALX
PC814
220pF_X7R_50V
0402
NI
CHARGE_LX
PQ803
RJK0389DPA-00#J53
PL800
10uH_6A/6A
11.5X10X4
M31ACSIP
PR822
10m_1%_1/2W
1206
+VCHG
PC815
2.2nF_X7R_50V
0603
NI
CHARGE_SN
PR815
2.2_1%
0805
NI
SCL
M31ASCL
SDA
M31ASDA
DLO
M31ADLO
PGND
CSIP
M31ACSIP
CSIN
FBSA
M31AFBSA
FBSB
PR816
100_5%
0402
PC831
1nF_X7R_50V
0402
PC832
1nF_X7R_50V
0402
IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x PR810 x 3mA/V x PR818
[25] ADAPT_OC_IINP
PR817
0_5%
0402
M31AIINP
IINP
CCV
M31ACCV
CCI
M31ACCI
CCS
M31ACCS
REF
M31AREF
DAC
M31ADAC
PR818
10K_5%
0402
PC818
100nF_X5R_6.3V
0402
PR819
10K_5%
0402
PC821
10nF_X7R_25V
0402
PC822
10nF_Y5V_25V
0402
PC823
10nF_Y5V_25V
0402
PC820
1uF_X5R_10V
0402
PC819
100nF_X5R_6.3V
0402
GND_2
BP
GND_1
M31AAGND
[25,32] EC_SMB1_CLK_3AL
PR820
0_5%
0402
M31ASCL
[25,32] EC_SMB1_DAT_3AL
PR821
0_5%
0402
M31ASDA
M31ALDO
PR826
10K_5%
0402
[25] ACPRES
PR823
0_5%
0402
M31AACOK
PR827
15.8K_1%
0402
PC829
10uF_X5R_25V
0805
PC828
10uF_X5R_25V
0805
PC824
10uF_X5R_25V
0805
PC826
10uF_X5R_25V
0805
NI
PC827
1nF_X7R_50V
0402
+VCHG
PJP800
SHORT PAD
NI
1.5X07.51.5X075
M31AAGND
+VBAT
DCIN
BT+
+V3.3A
M31ALDO
+VBAT [30,34,35,36,37,39,40]
DCIN [32]
BT+ [32]
+V3.3A [9,13,14,15,16,17,25,27,29,32,37,38]
M31ALDO
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Title
PWR_Charger
Size
Custom
Document Number
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Rev
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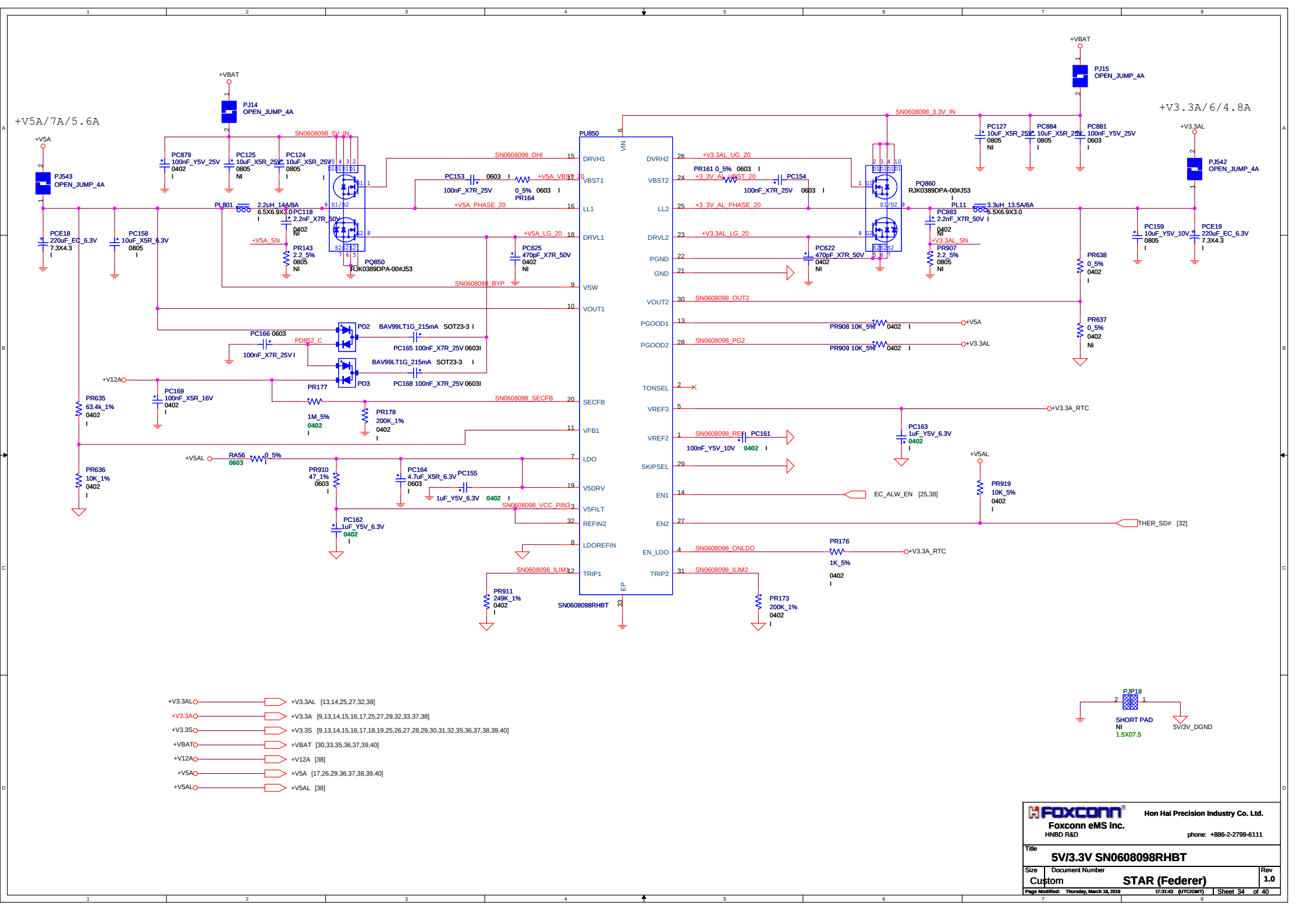
Sheet 33 of 40



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Title: 5V/3.3V SN0608098RHBT

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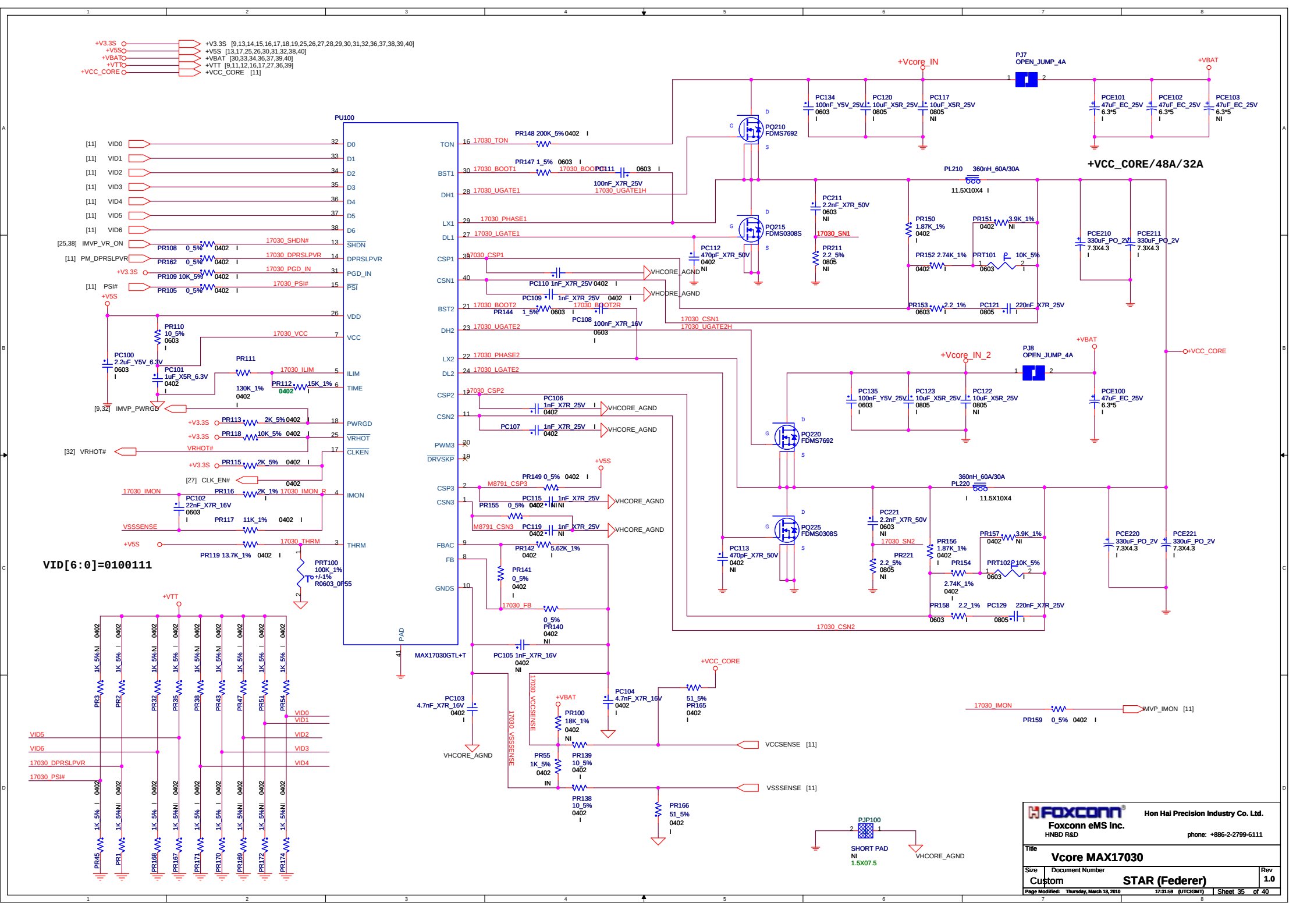
+V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,36,37,38,39,40]
+V5S [13,17,25,26,30,31,32,38,40]
+VBAT [30,33,34,36,37,39,40]
+VTT [9,11,12,16,17,27,36,39]
+VCC_CORE [11]
PU100
MAX17030GTL+T
VID[6:0]=0100111
+Vcore_IN
+Vcore_IN_2
+VCC_CORE/48A/32A
PJ7 OPEN_JUMP_4A
PJ8 OPEN_JUMP_4A
PJP100 SHORT PAD NI 1.5X07.5
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phone: +886-2-2799-6111
Title
Vcore MAX17030
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Document Number STAR (Federer)
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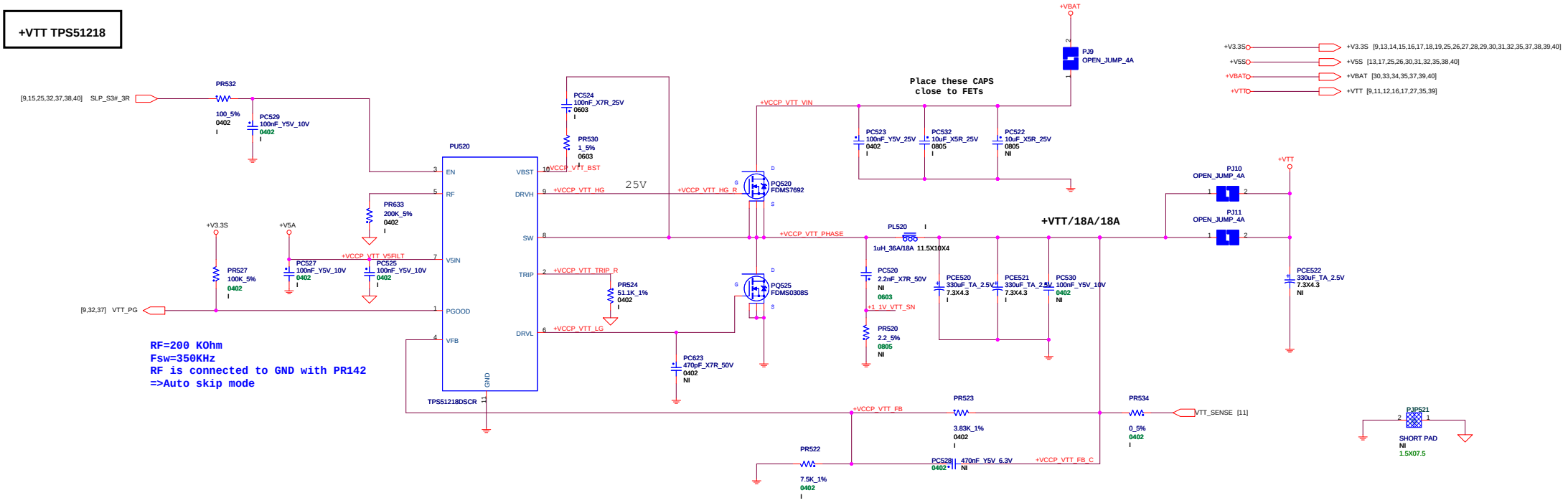
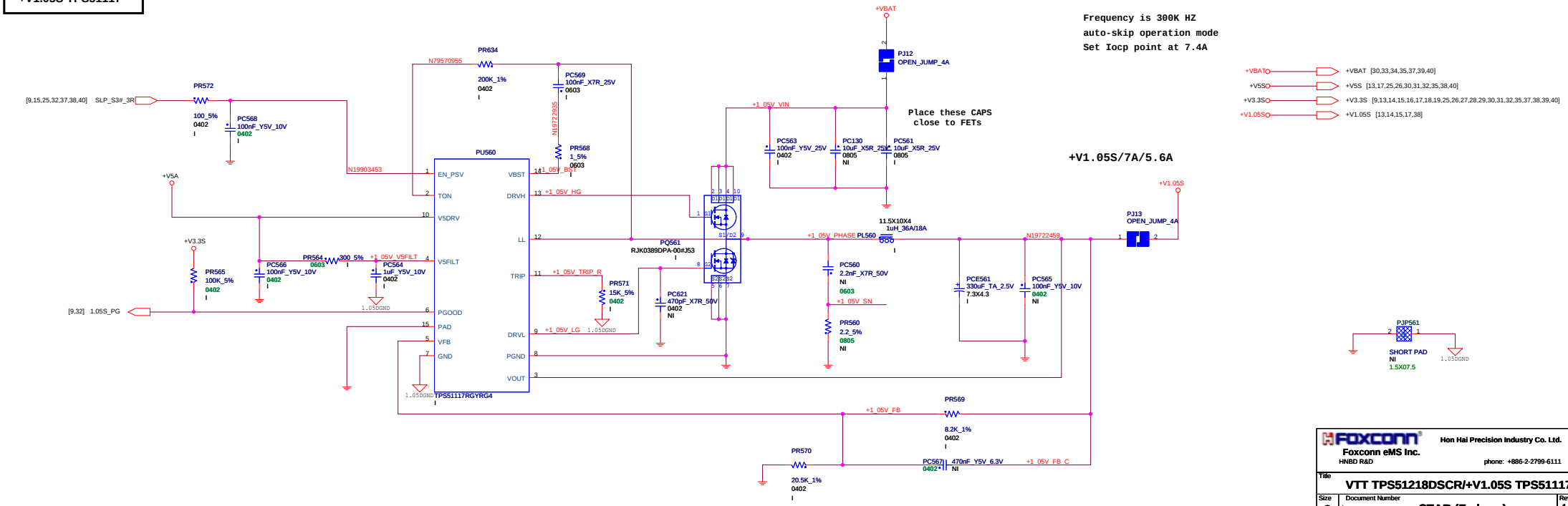
+VTT TPS51218



+V1.05S TPS51117



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Title	VTT TPS51218DSCR/+V1.05S TPS51117
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Frequency is 400K HZ
D-CAP Mode
Set Iocp point at 12A

PR505 Fsw=400kHz
PU500
249K_1%
0402
[15,25] SLP_S4#_3R
+V5A
EN_PSV
TON
V5DRV
V5FILT
PGOOD
PAD
VFB
GND
VBST
DRVH
LL
TRIP
DRVL
PGND
VOUT
TPS51117RGYRG4
PR503 4.7_5% 0402
PC507 100nF_Y5V_10V 0402
PC505 1uF_Y5V_10V 0603
+V3.3A
PR801 47K_5% 0402
PR501 1_5% 0603
+1_5V_DUAL_BST
+1_5V_DUAL_UG_20
+1_5V_DUAL_PHASE_20
+1_5V_DUAL_DRVL_20
OCP
PR573 13K_1% 0402
PC510 100nF_X7R_25V 0603
PC624 470pF_X7R_50V 0402 NI
PQ500 RJK0389DPA-00#J53
PL500 L=1.0uH 1uH_36A/18A 11.5X10X4
PC500 2.2nF_X7R_50V NI 0603
PR500 2.2_5% 0805 NI
+1_5V_DUAL_SN
+1_5V_DUAL_VIN
PC501 2.2uF_X7R_25V 0805
PC131 10uF_X5R_25V 0805 NI
PC502 10uF_X5R_25V 0805
PJ16 OPEN_JUMP_4A
+VBAT
PC509 100nF_Y5V_25V 0402
+V1.5
PJ18 OPEN_JUMP_4A
+V1.5/10A/8A
PC513 100nF_Y5V_10V 0402 NI
PCE501 330uF_TA_2.5V 7.3X4.3
PJP501 SHORT PAD NI 1.5X07.51.5X075
DDRPGND
+VBAT [30,33,34,35,36,39,40]
+V5A [17,26,29,34,36,38,39,40]
+V3.3A [9,13,14,15,16,17,25,27,29,32,33,38]
+V1.5 [9,18,38]
+1_5V_DUAL_SENSE
PR502 75K_1% 0402
PR504 75K_1% 0402
PC503 100pF_NPO_50V 0402 NI
Vout=(1+Rtop/Rbot)*0.75V

Design Current Should be 3A

PJ550 OPEN_JUMP_4A
+VBAT
+V1.8S_VIN
PC547 10uF_X5R_25V 0805
PC554 10uF_X5R_25V 0805
PU541
VIN
VCC
BST
SW
PG
AAM
EN/SYNC
FB
GND
THM
NB634EL-C285-LF-Z
+V5_BAK3
PC552 100nF_X7R_25V 0603
+V1.8S_BST_20
PR506 15_1% 0603
PC549 100nF_X7R_25V 0603
+V1.8S_SW_20
PL541 2.2uH_14A/8A 6.5X6.9X3.0
+V1.8S
PC548 100nF_Y5V_10V 0402 NI
PC550 22uF_X5R_6.3V 0805
PC546 22uF_X5R_6.3V 0805
PR546 10K_5% 0402
+V3.3S
+V1.8S_PG
PR540 130K_1% 0402
+V1.8S_AAM
PR541 10K_1% 0402
[9,15,25,32,36,38,40] SLP_S3#_3R
PR547 0_5% 0603
+V1.8S_EN_R
+V1.8S_FB
PR543 36K_1% 0402
PR555 8.06K_1% 0402
+V1.8S_SENSE_R
PR548 10K_1% 0402
PR544 0_5% 0402
PC551 100pF_NPO_50V 0402
+V1.8S_SENSE
PJP20 SHORT PAD NI 1.5X07.51.5X075
1.8=0.8*(1+R1/R2)

+V0.75S/1A/0.8A
PU501
+V1.5
+V0.75S
PJ17 OPEN_JUMP_4A
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
VIN
S5
GND
S3
VTTREF
PAD
G2997F6U
PC504 10uF_X5R_25V 0805
PC506 10uF_X5R_6.3V 0805
PC515 10uF_X5R_6.3V 0805
+V5A
PC511 1uF_Y5V_10V 0603
PR511 0_5% 0402
SLP_S4#_3R [15,25]
PC508 100nF_X7R_25V 0603
PR566 100K_5% 0402
VTT_PG [9,32,36]
PR512 0_5% 0402 NI
SLP_S3#_3R [9,15,25,32,36,38,40]
M_VREF
PC512 100nF_X7R_25V 0603 NI
PC514 1uF_Y5V_10V 0603
M_VREF [18]
+V0.75S [18,38]

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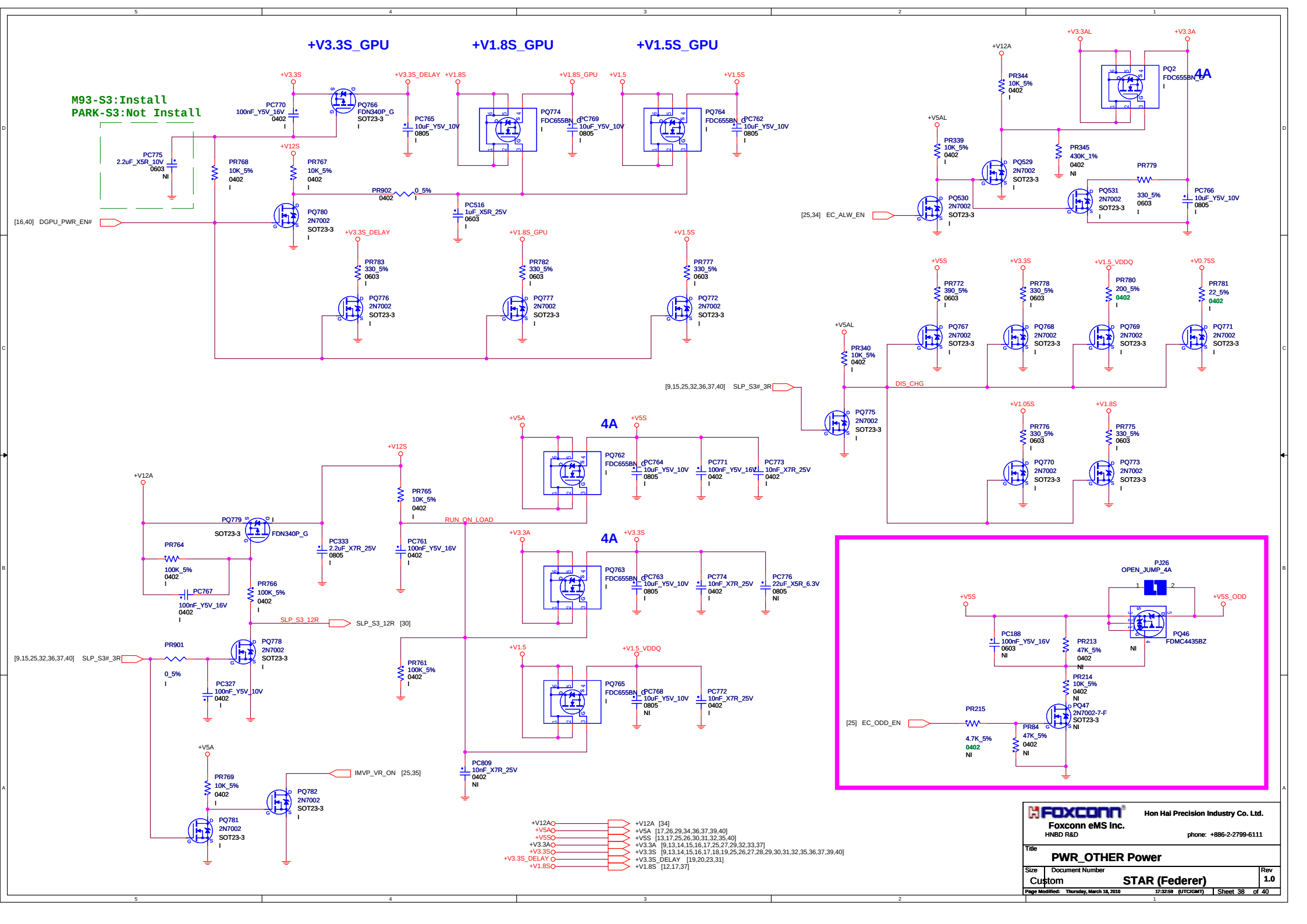
+V3.3S_GPU
+V1.8S_GPU
+V1.5S_GPU
M93-S3:Install
PARK-S3:Not Install
4A
[16,40] DGPU_PWR_EN#
[25,34] EC_ALW_EN
[9,15,25,32,36,37,40] SLP_S3#_3R
DIS_CHG
RUN_ON_LOAD
SLP_S3_12R
SLP_S3_12R [30]
IMVP_VR_ON [25,35]
[25] EC_ODD_EN
PJ26
OPEN_JUMP_4A
+V12A [34]
+V5A [17,26,29,34,36,37,39,40]
+V5S [13,17,25,26,30,31,32,35,40]
+V3.3A [9,13,14,15,16,17,25,27,29,32,33,37]
+V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,39,40]
+V3.3S_DELAY [19,20,23,31]
+V1.8S [12,17,37]
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PWR_OTHER Power
Custom
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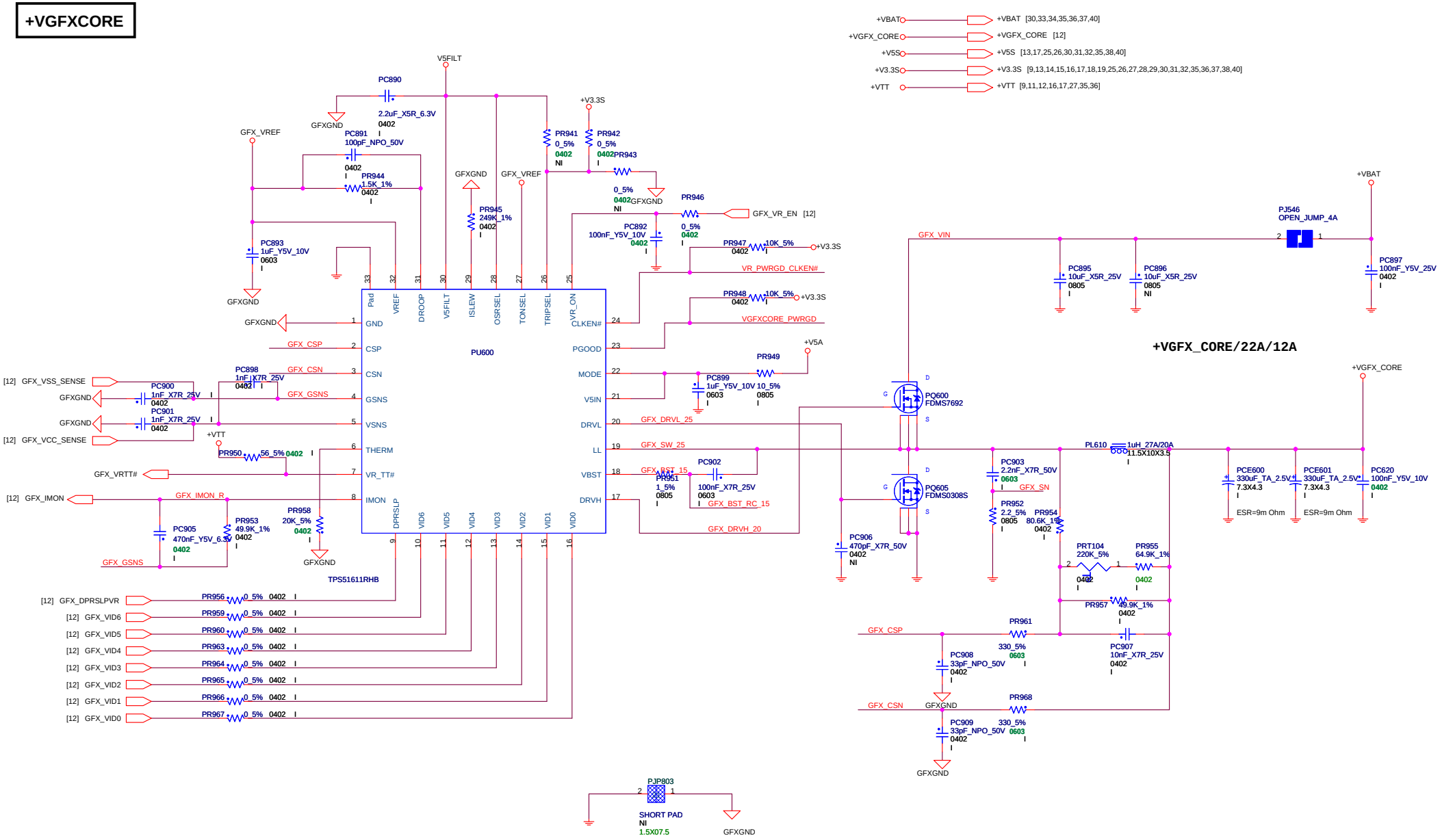
+VGFXCORE



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Title: **CPU VREG & Decoupling**

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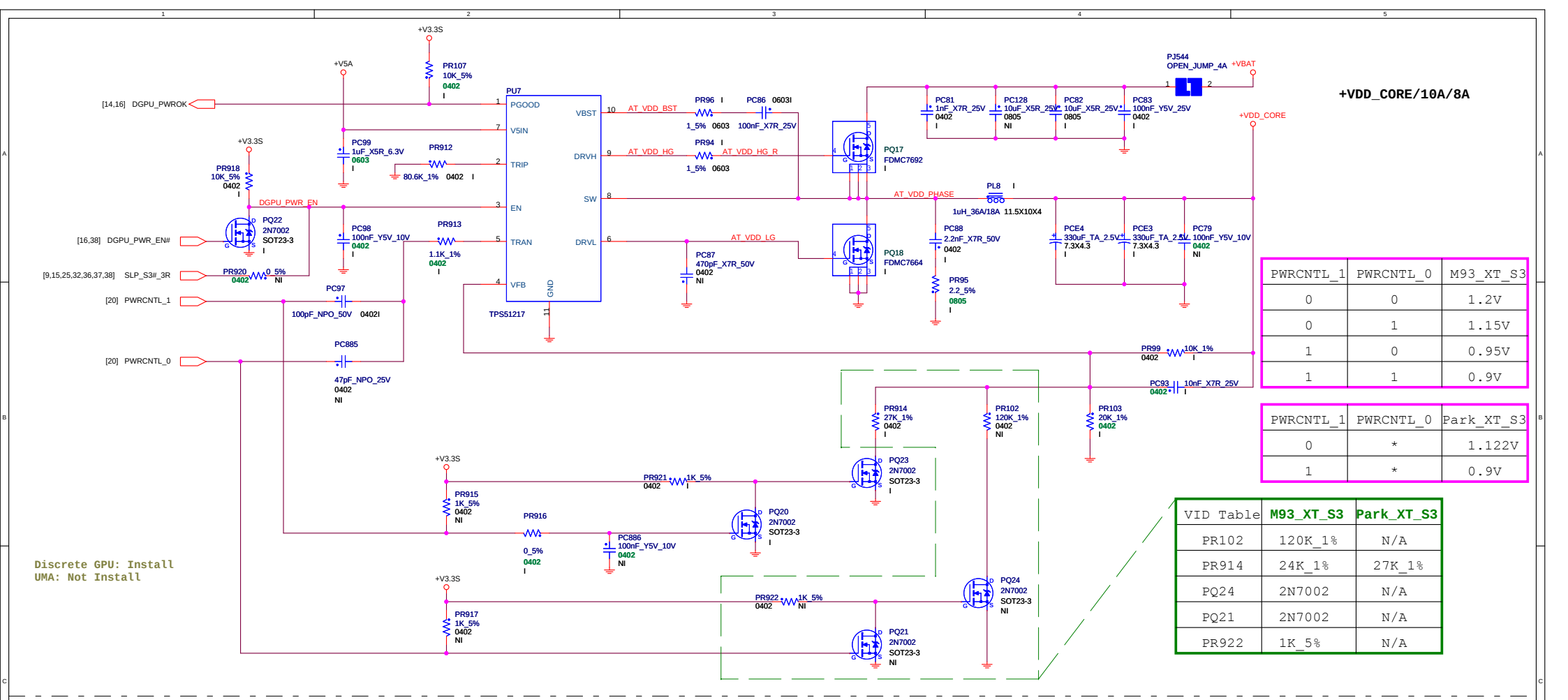

PWRCNTL_1	PWRCNTL_0	M93_XT_S3
0	0	1.2V
0	1	1.15V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	PWRCNTL_0	Park_XT_S3
0	*	1.122V
1	*	0.9V

VID Table	M93_XT_S3	Park_XT_S3
PR102	120K_1%	N/A
PR914	24K_1%	27K_1%
PQ24	2N7002	N/A
PQ21	2N7002	N/A
PR922	1K_5%	N/A

Discrete GPU: Install
UMA: Not Install

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