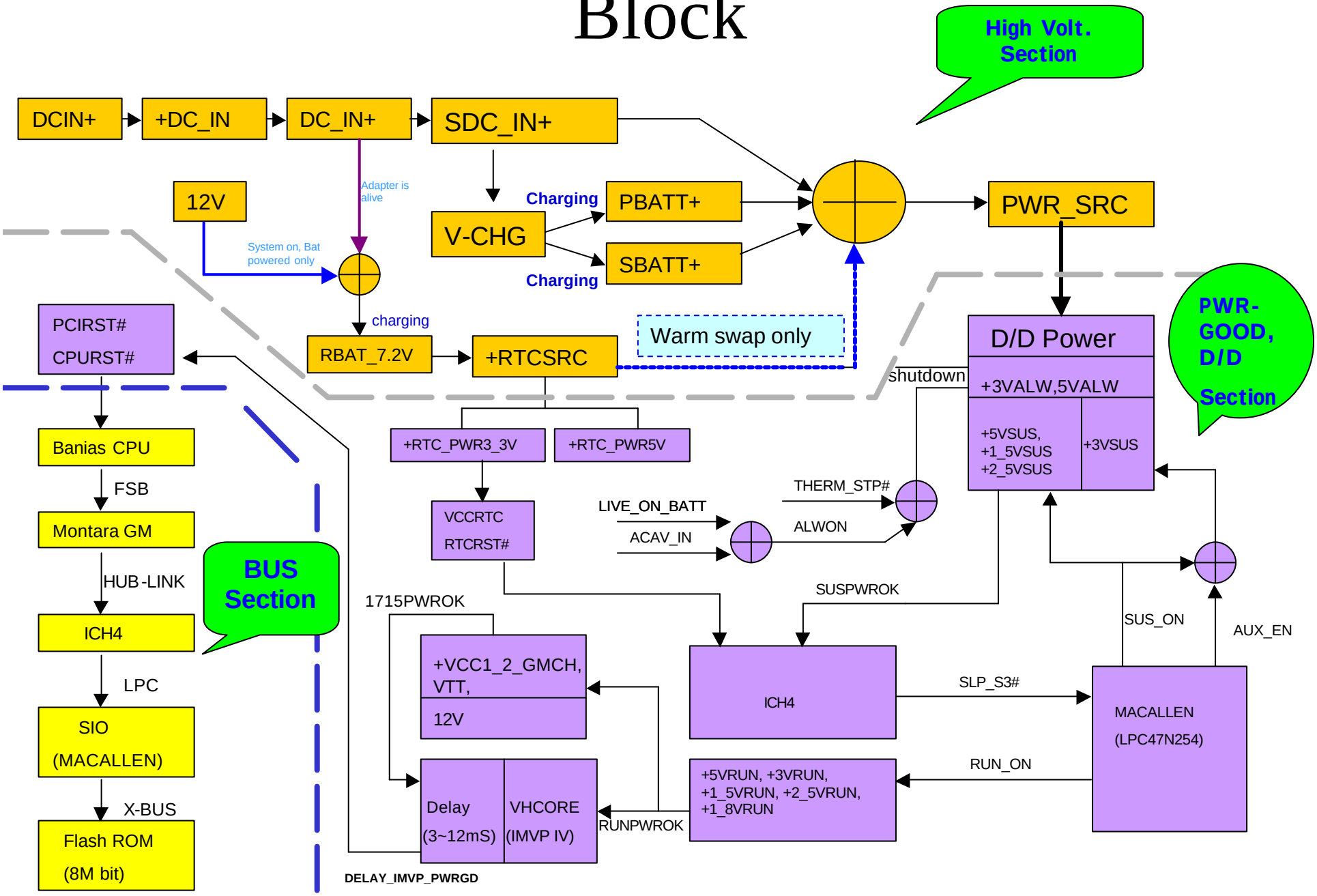
JM3 Power-up Sequence

1. *To know JM3 Power-Up Sequence.*
2. *More easy to find out the root-cause if system Lock-Up of No-Power.*
3. *To realize each step before BIOS is working.*
4. *Summarized preliminary Power-Up sequence diagram.*
5. *Power-up sequence after POWER_SW# in the Nutshell.*

Block


High Volt. Section
DCIN+
+DC_IN
DC_IN+
SDC_IN+
12V
Adapter is alive
System on, Bat powered only
Charging
PBATT+
V-CHG
SBATT+
Charging
PWR_SRC
charging
RBAT_7.2V
+RTCSRC
Warm swap only
PCIRST#
CPURST#
D/D Power
+3VALW,5VALW
+5VSUS, +1_5VSUS +2_5VSUS
+3VSUS
shutdown
PWR-GOOD, D/D Section
Banias CPU
FSB
Montara GM
HUB-LINK
ICH4
LPC
SIO (MACALLEN)
X-BUS
Flash ROM (8M bit)
BUS Section
+RTC_PWR3_3V
+RTC_PWR5V
VCCRTC
RTCRST#
LIVE_ON_BATT
ACAV_IN
THERM_STP#
ALWON
1715PWROK
+VCC1_2_GMCH, VTT,
12V
SUSPWROK
SUS_ON
AUX_EN
ICH4
SLP_S3#
MACALLEN (LPC47N254)
RUN_ON
+5VRUN, +3VRUN, +1_5VRUN, +2_5VRUN, +1_8VRUN
Delay (3~12mS)
VHCORE (IMVP IV)
RUNPWROK
DELAY_IMVP_PWRGD

Binchuan:

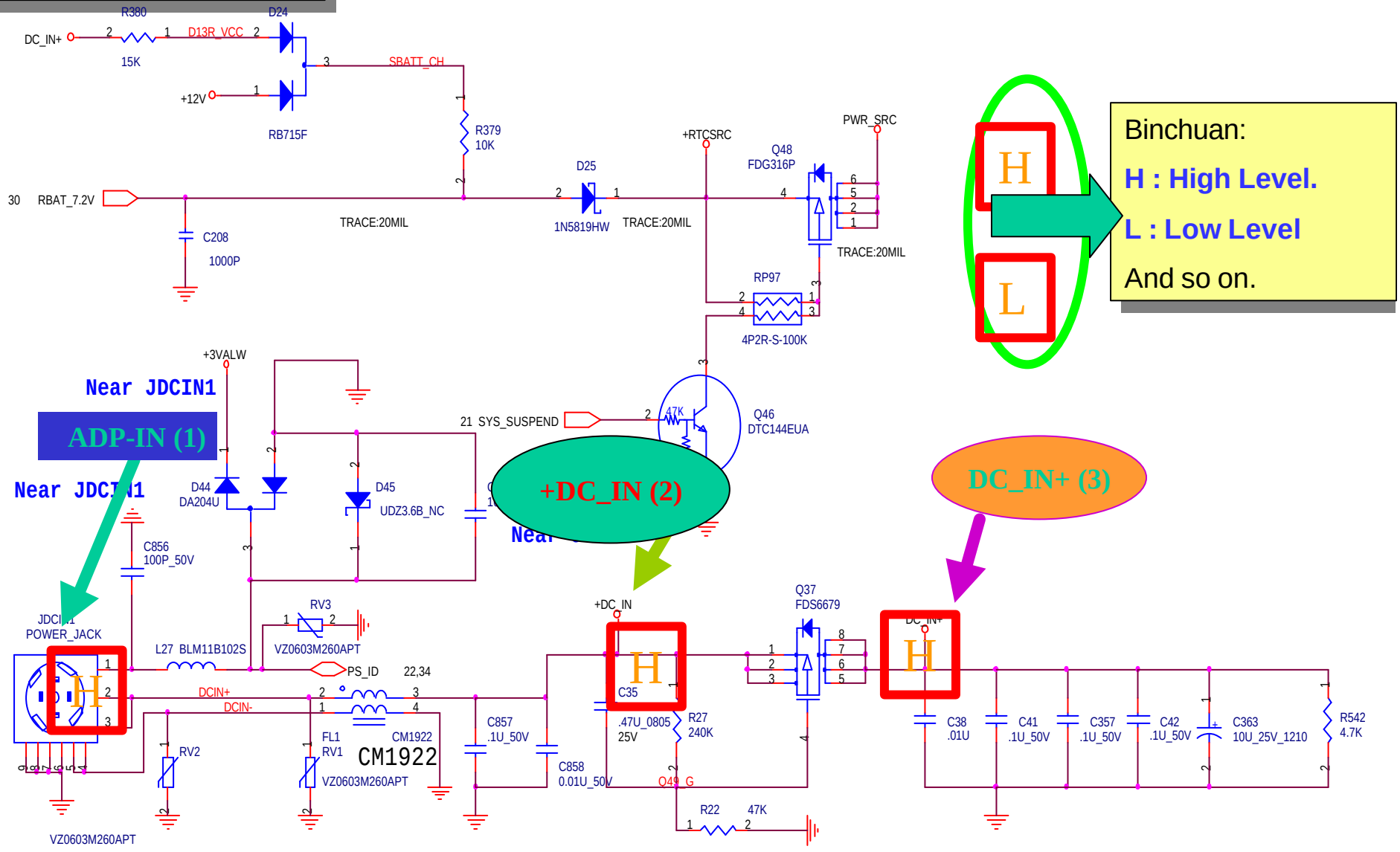
(1).ADP-IN

(2).+DC_IN

(3).DC_IN+

Schematic page 29

ADAPTER-IN(P29)



Binchuan:

H : High Level.

L : Low Level

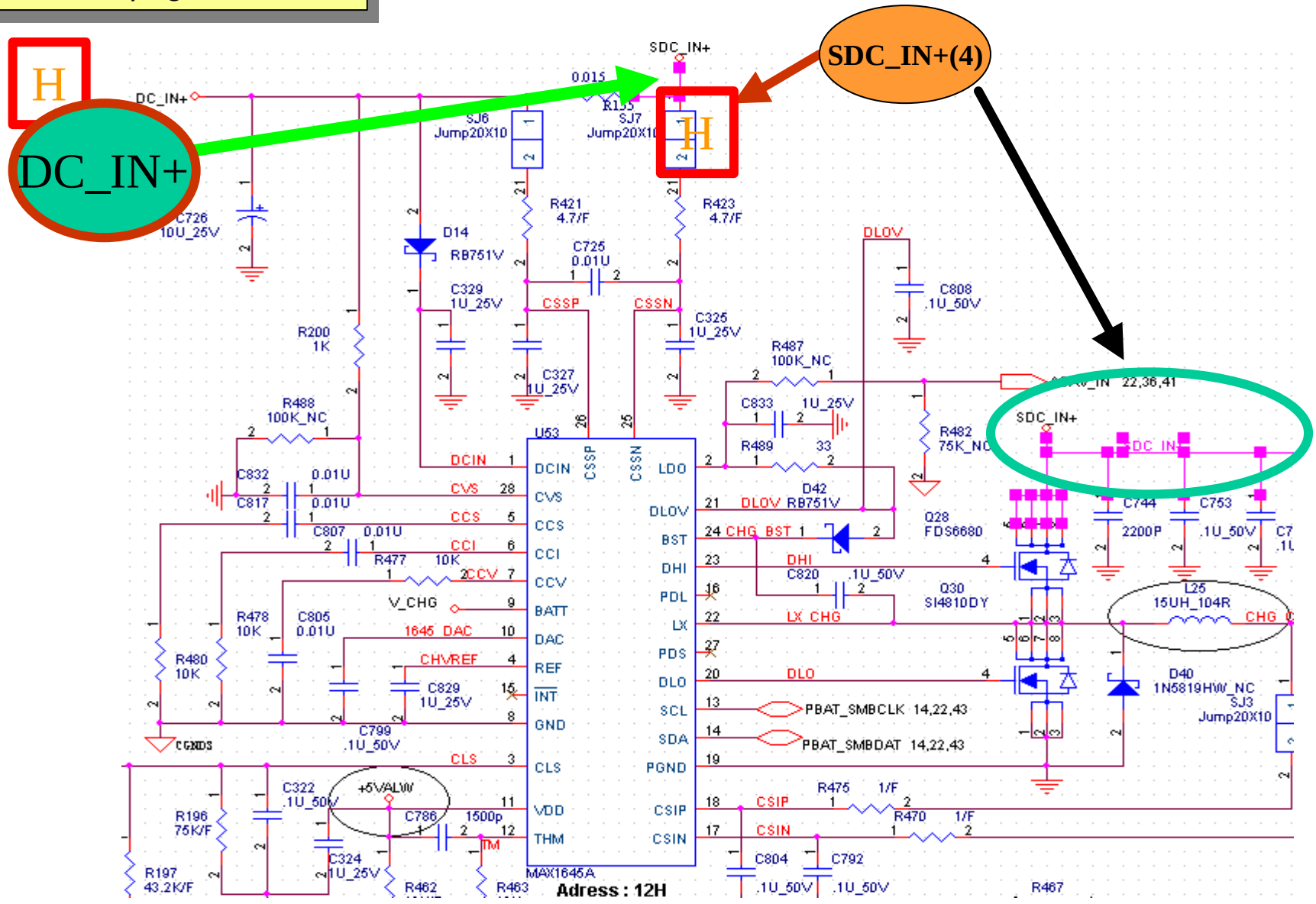
And so on.

Binchuan:

(4). DC_IN+ to SDC_IN+

Schematic page 37

SDC_IN+(P31)

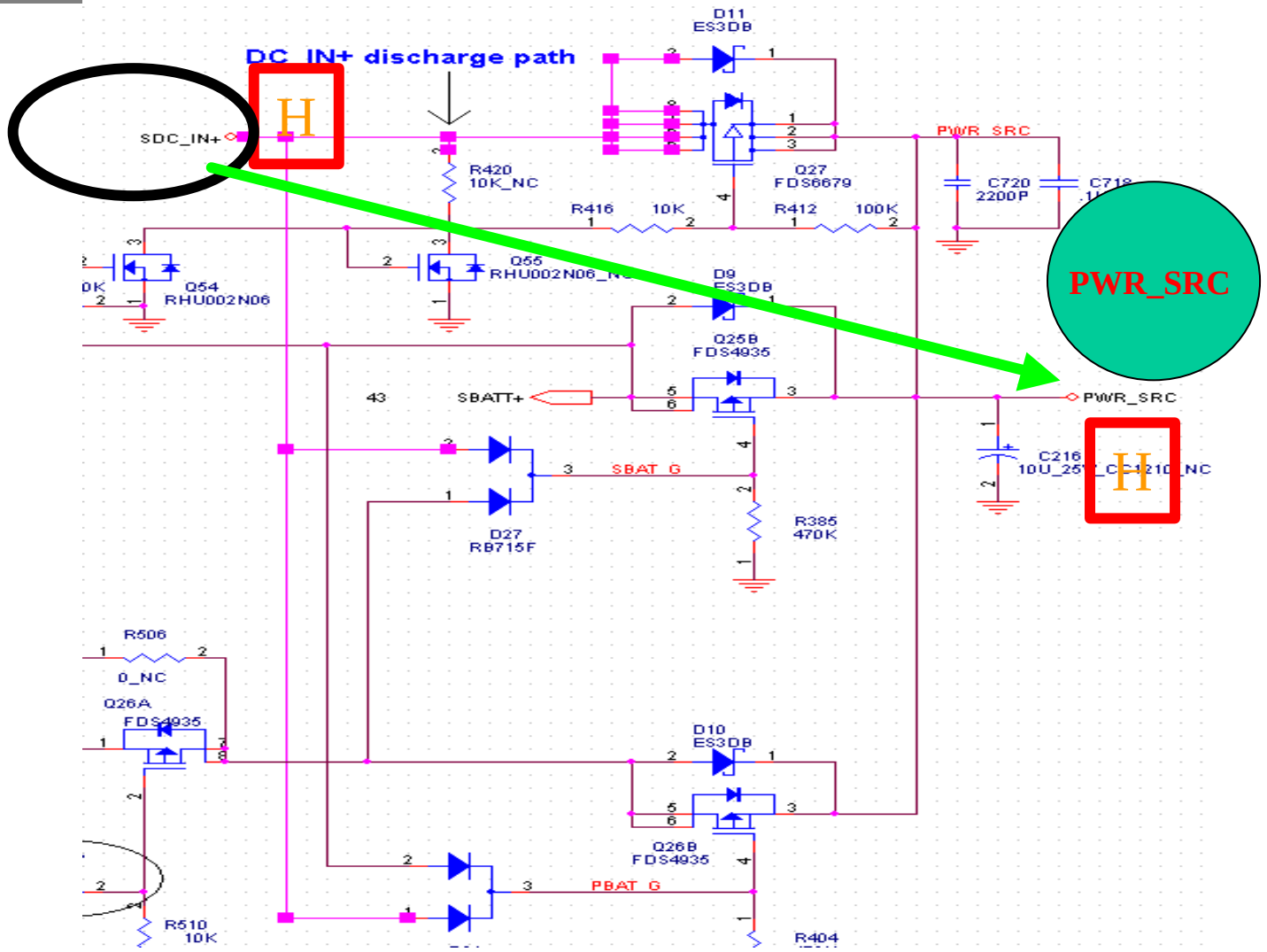


Binchuan:

(5). SDC_IN+ to PWR_SRC

Schematic page 36

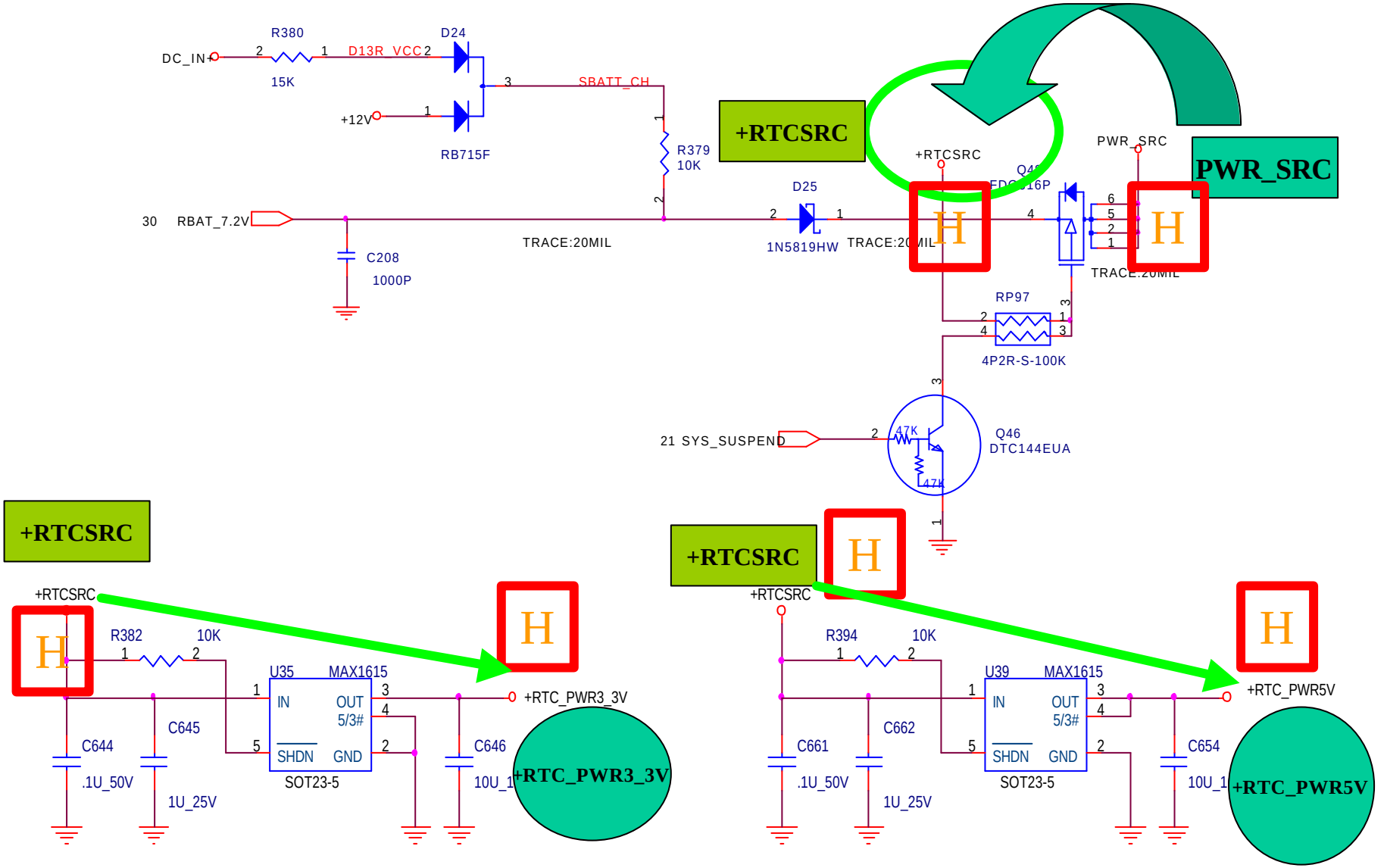
PWR_SRC(P36)



Binchuan:

+RTCSRC supply +RTC_PWR5V and +RTC_PWR3_3V

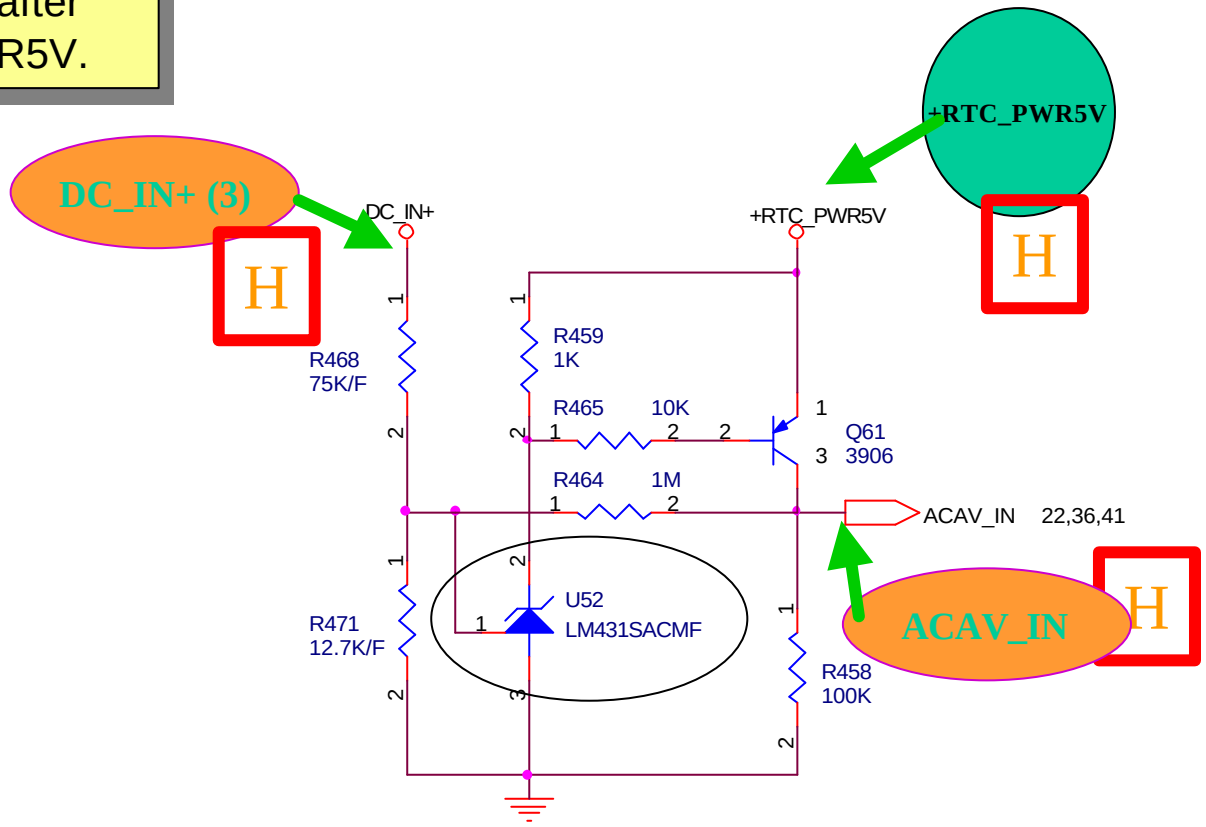
+RTCSRC(P41,43)



Binchuan:

ACAV_IN will be generated after +RTC_PWR5V.

ACAV_IN(P37)



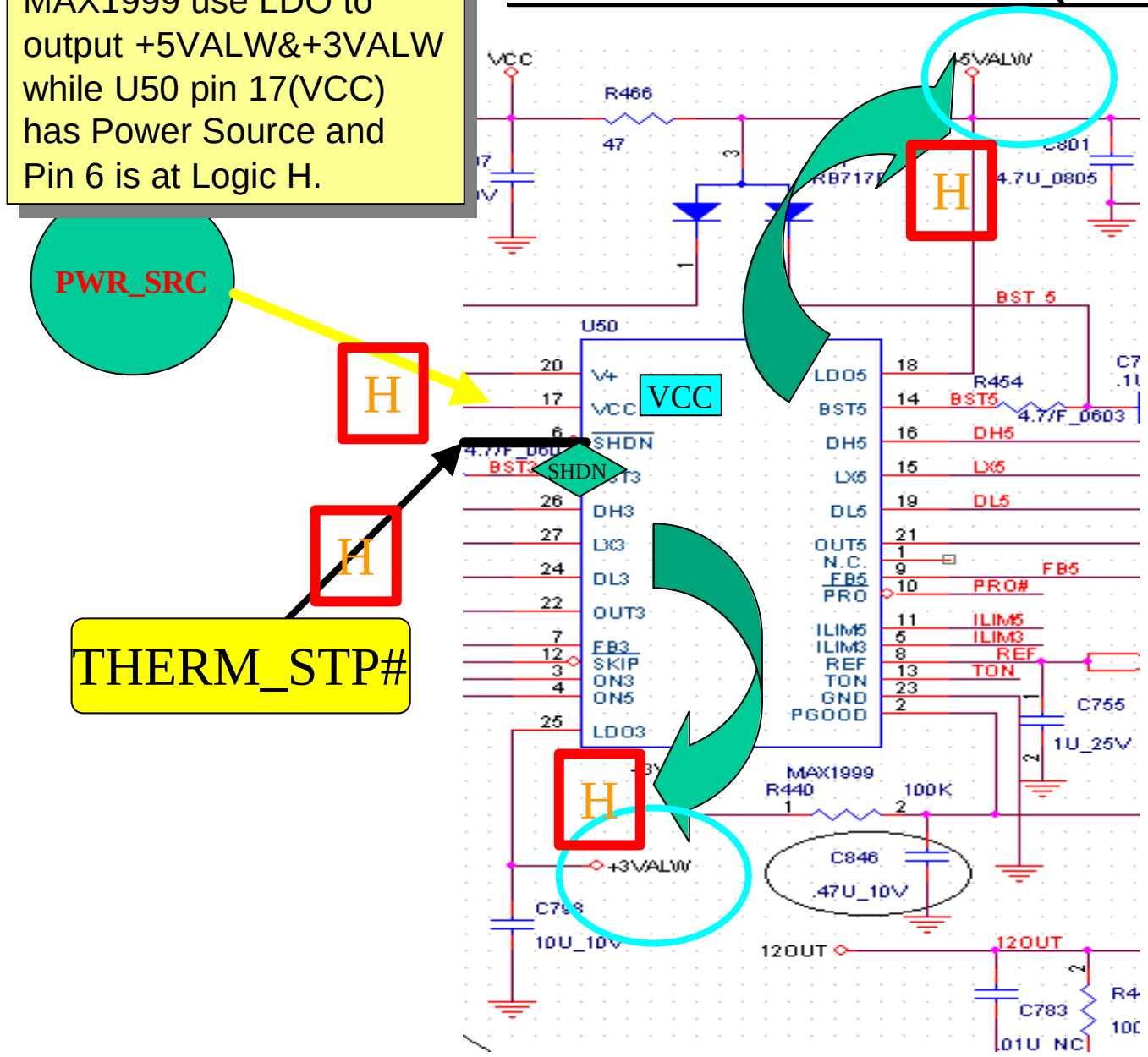
Binchuan:

ACAV_IN generate to notice SIO about Adaptor(Present).

+3VALW&+5VALW(P41)

Binchuan:

MAX1999 use LDO to output +5VALW&+3VALW while U50 pin 17(VCC) has Power Source and Pin 6 is at Logic H.



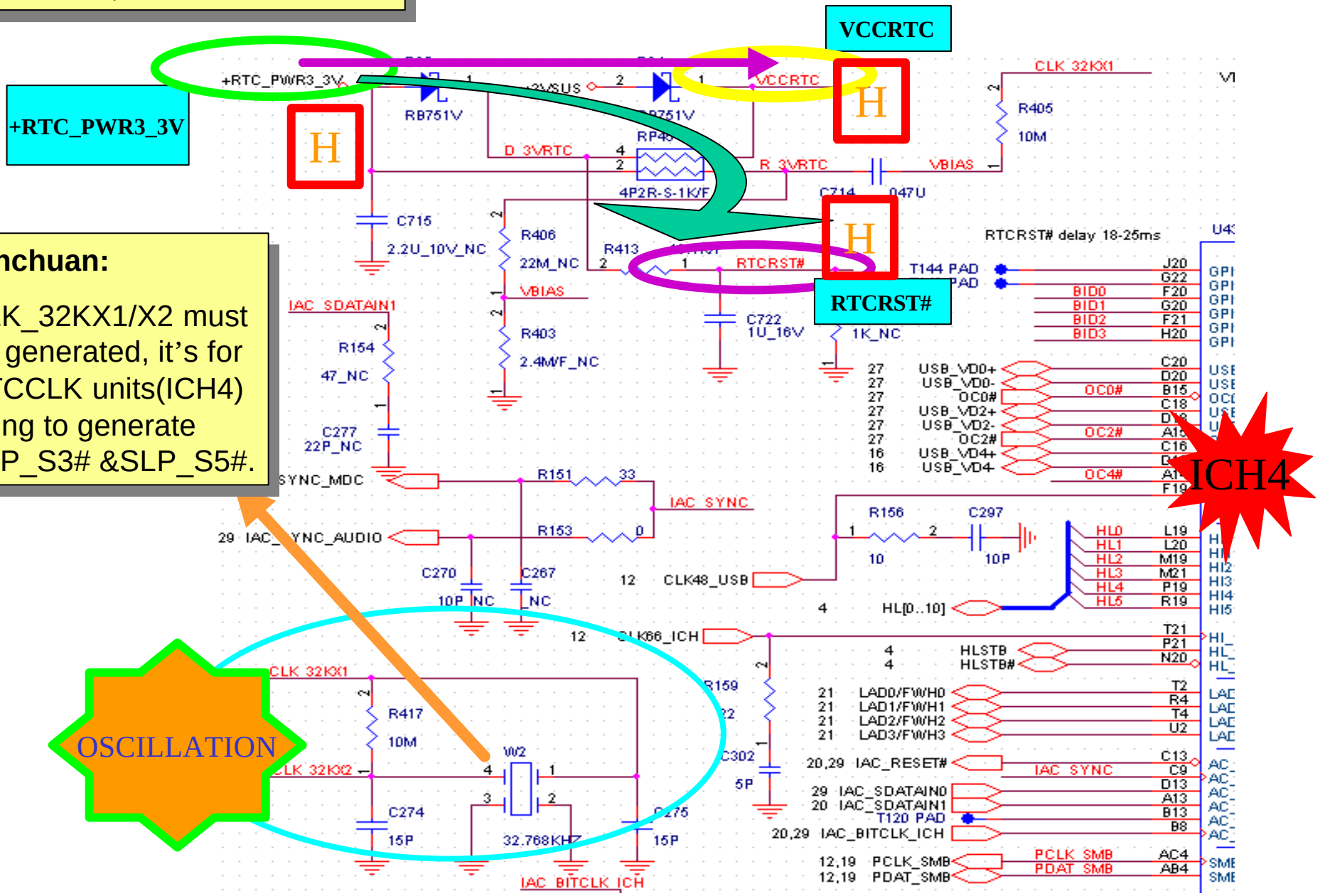
Binchuan:

(6).As soon as +RTC_PWR3_3V on, then RTCRST# will be from Low ✍High.
(Reset CMOS)

RTCRST#(P9)

Binchuan:

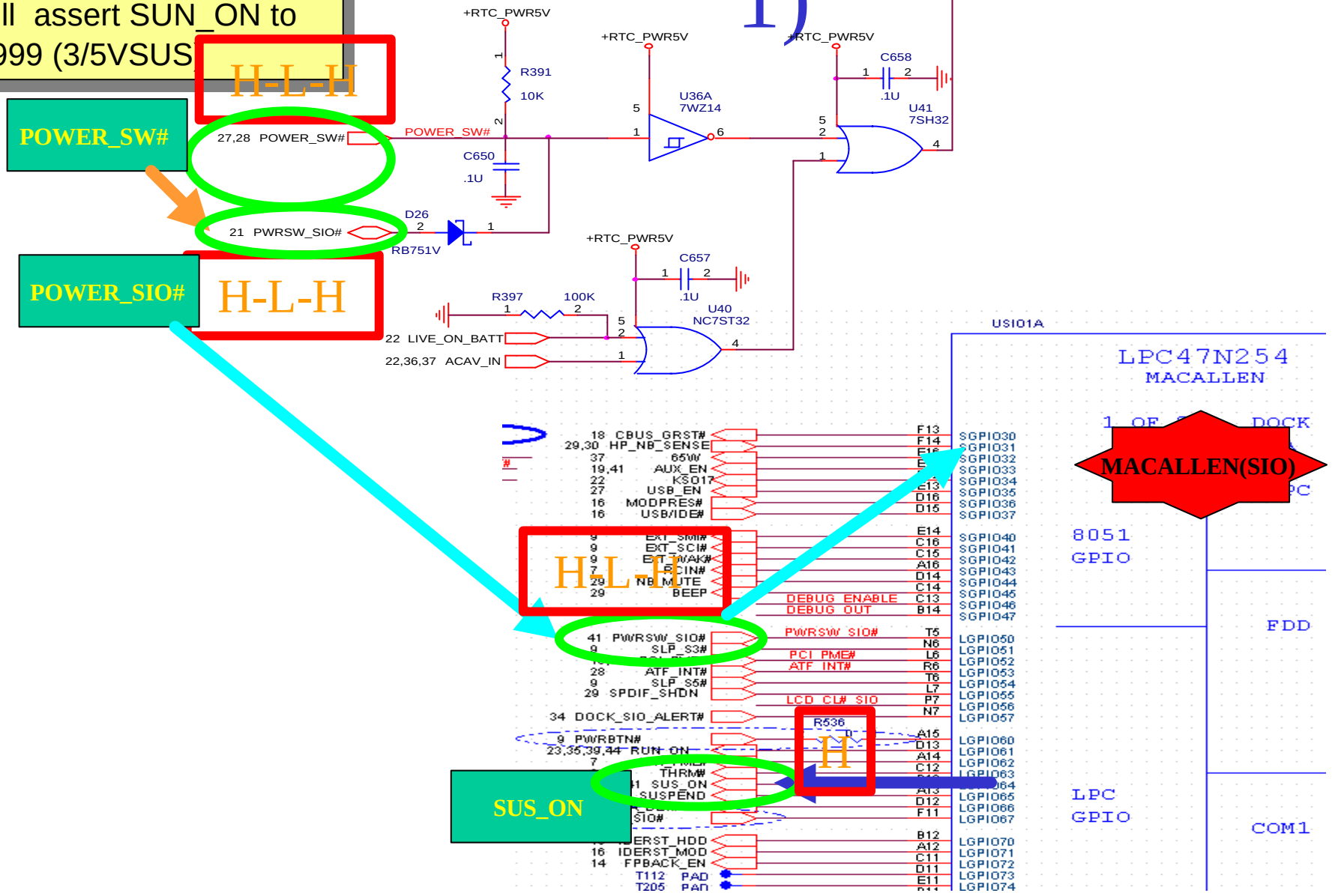
CLK_32KX1/X2 must be generated, it's for RTCCLK units(ICH4) using to generate SLP_S3# &SLP_S5#.



Binchuan:

(A).POWER_SW# generate the POWER_SIO#, and If MACALLEN(SIO) is alive then it'll assert SUN_ON to MAX1999 (3/5VSUS

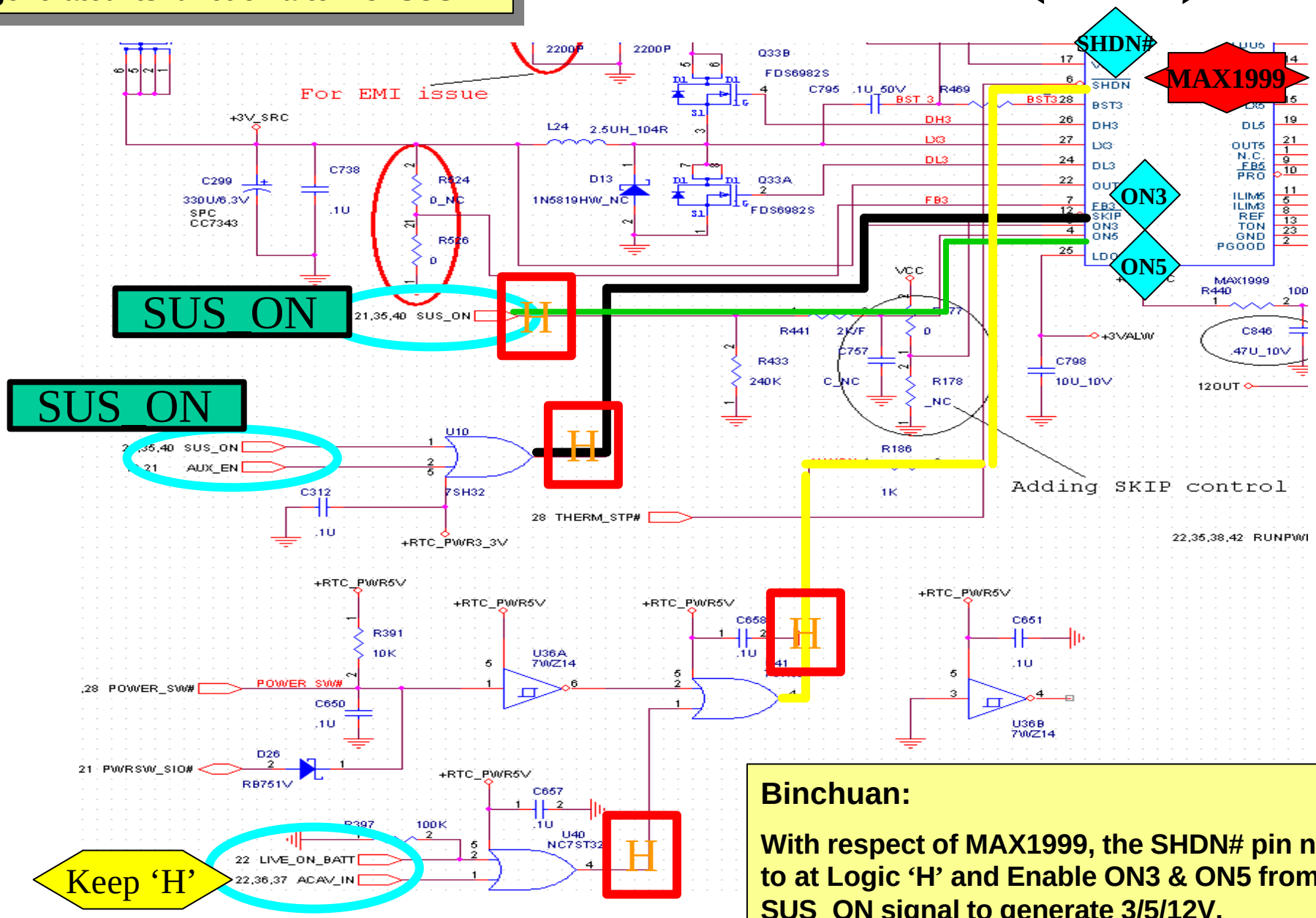
POWER_SW#(P41,P21)



Binchuan:

THERM_STP# is OD and will be generated its function after +3VSUS.

MAX1999(P41)



Binchuan:

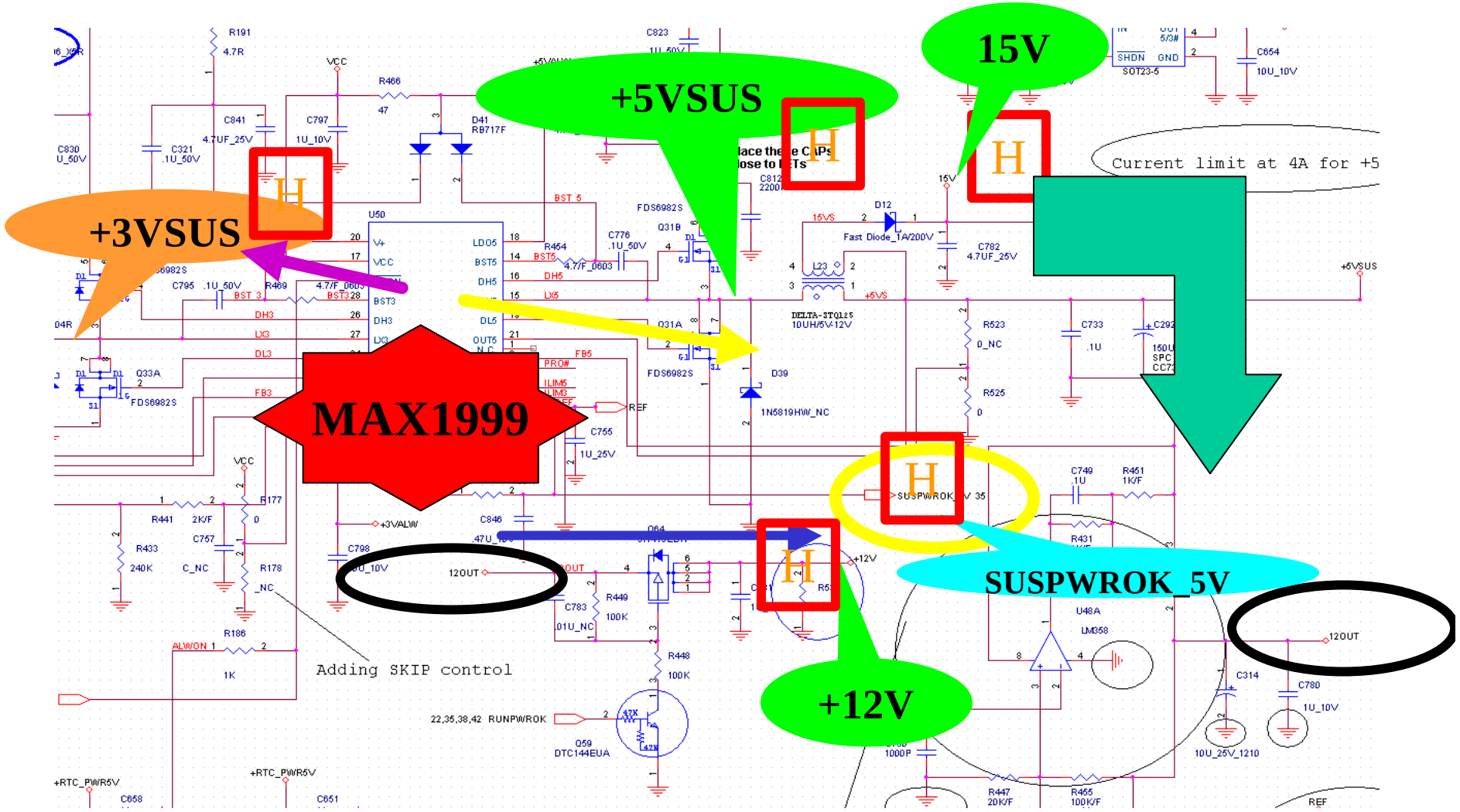
With respect of MAX1999, the SHDN# pin need to at Logic 'H' and Enable ON3 & ON5 from SUS_ON signal to generate 3/5/12V.

Binchuan:

SUS_ON turn on +3/5VSUS power.

While MAX1999 stable then it generate SUSPWROK_5V.

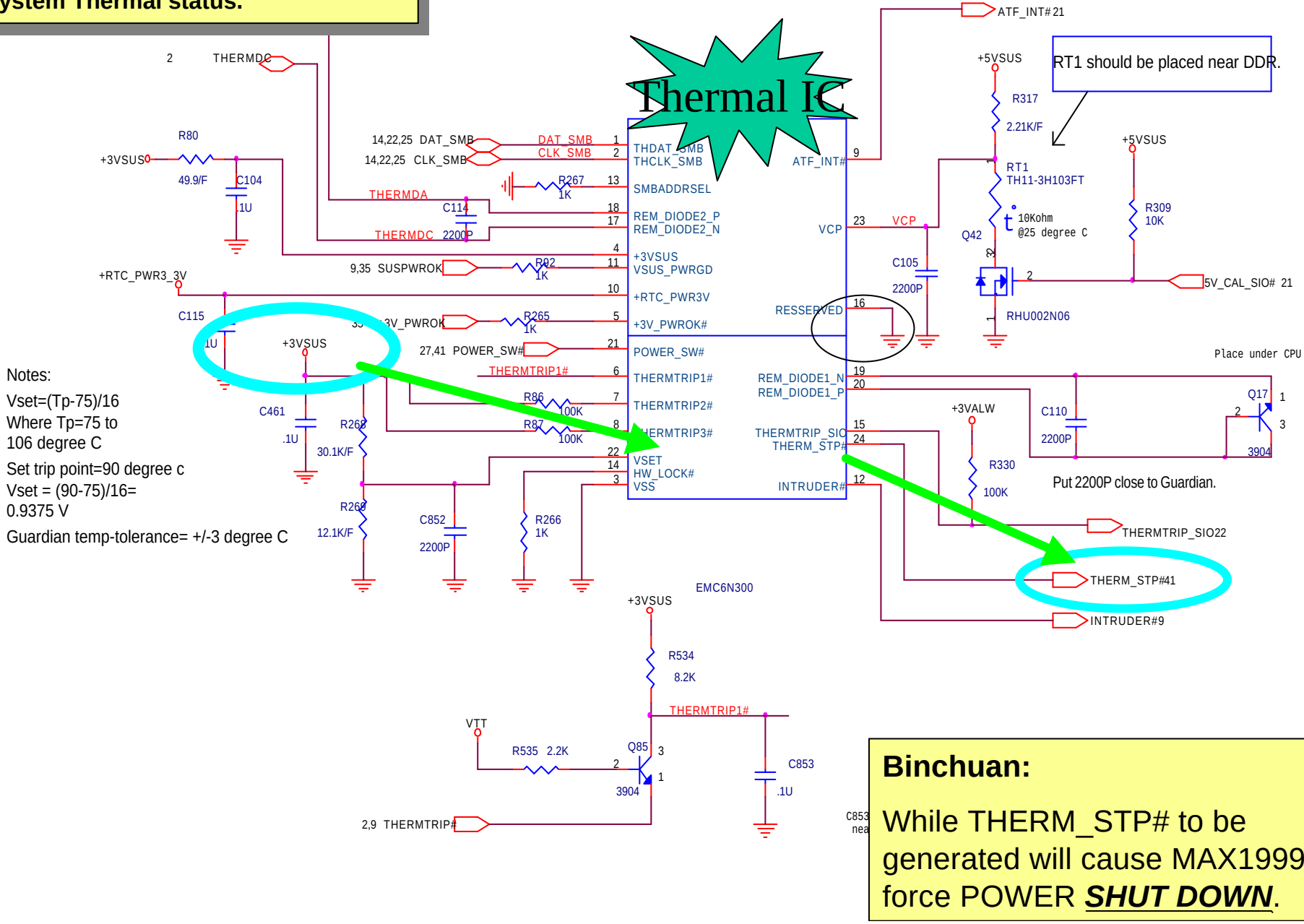
3/5/12V(P41)



Binchuan:

+3VSUS✍ THERM_STP# at Logic 'H'. Guardian Thermal IC control currently System Thermal status.

THERM_STP#(P28)



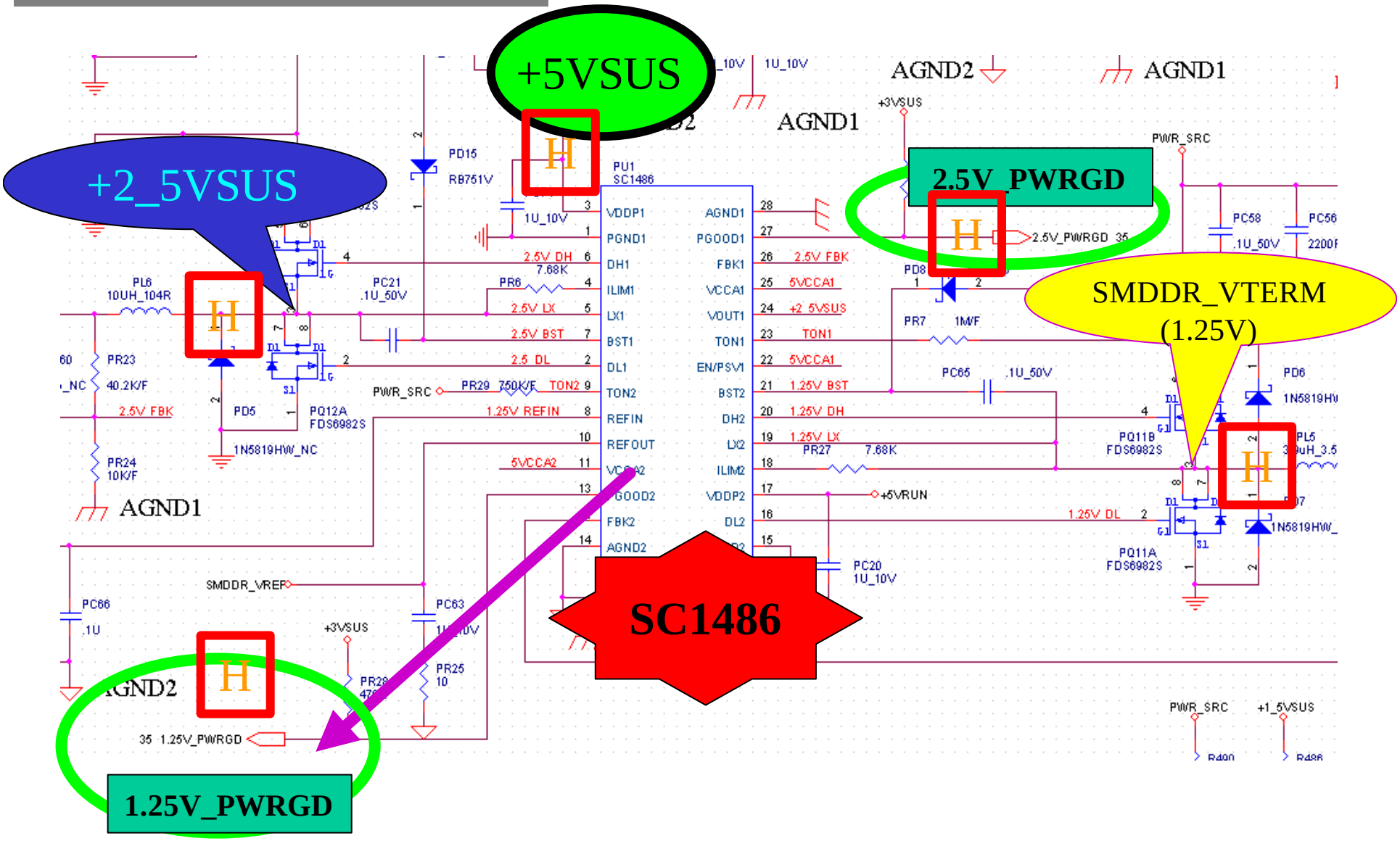
Binchuan:

While THERM_STP# to be generated will cause MAX1999 force POWER ***SHUT DOWN***.

Binchuan:

When +5VSUS supply SC1486 then it'll generate +2_5VSUS,SMDDR_VTERM and 1.25V_PWRGD & 2.5V_PWRGD.

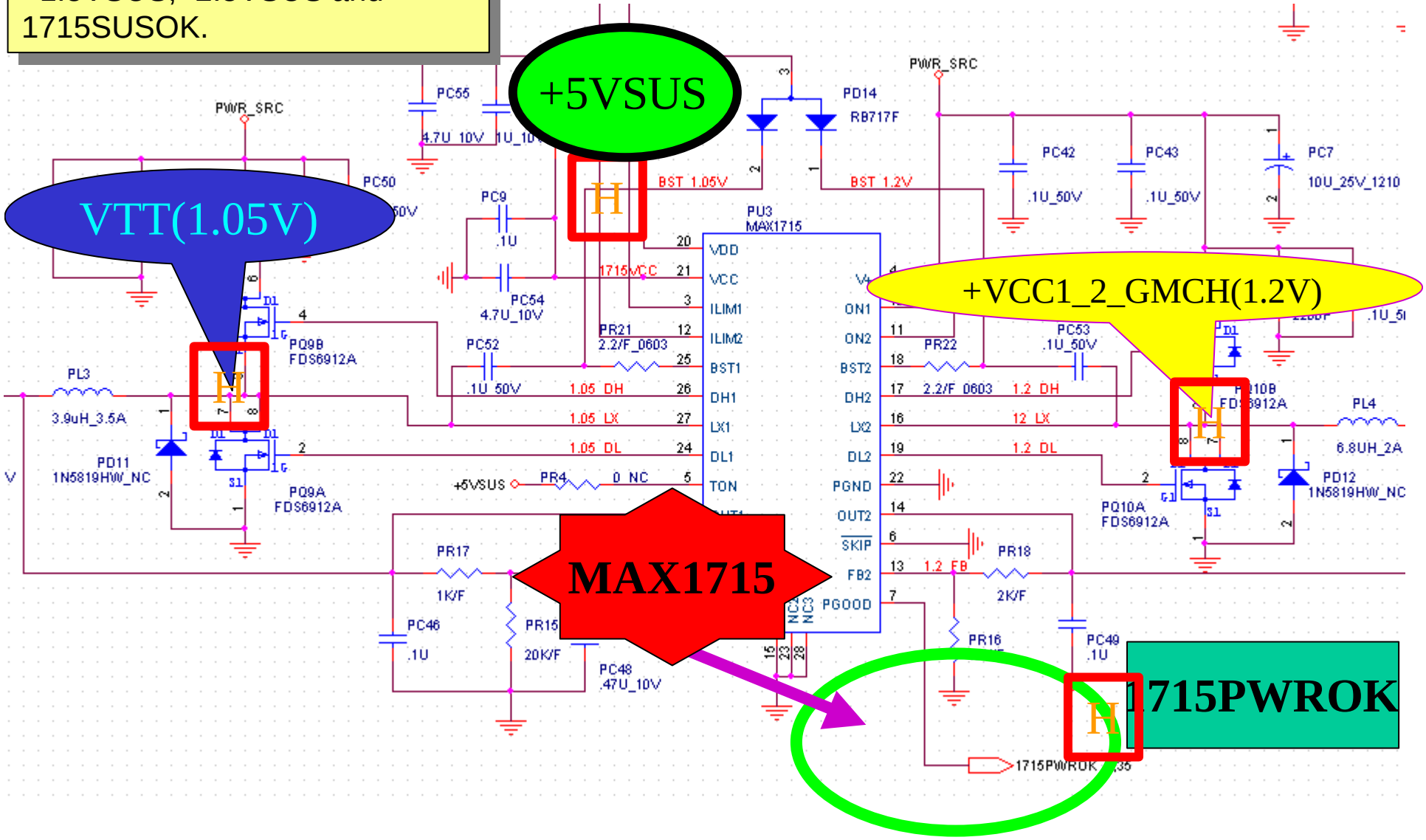
1.25V_PWRGD(P40)



Binchuan:

(C). When +5VSUS supply MAX1715 then it'll generate +1.5VSUS,+2.5VSUS and 1715SUSOK.

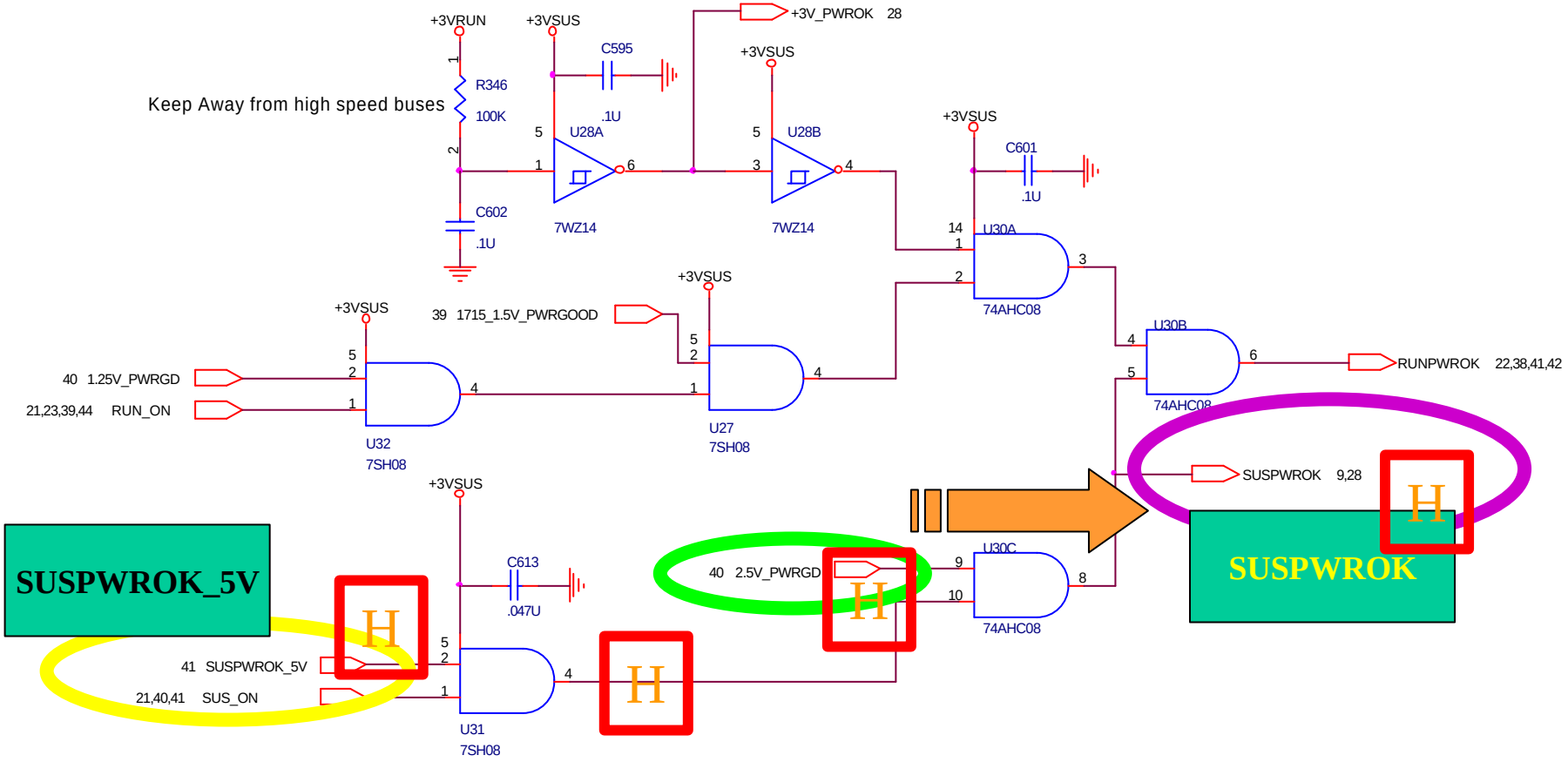
1715PWROK(P42)



Binchuan:

SUSPWROK_5V as +3/5VSUS is ok. Then it will connect with AND-Gate with SUS_ON then AND with 2.5V_PWRGD to produce SUSPWROK.

SUSPWROK(P35)

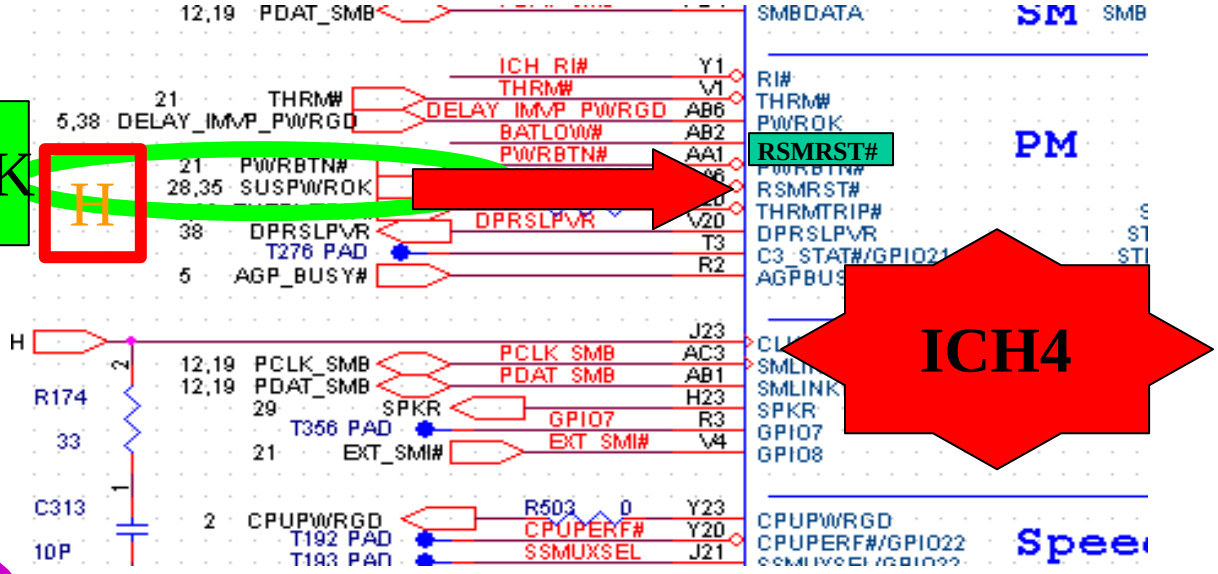


Binchuan:

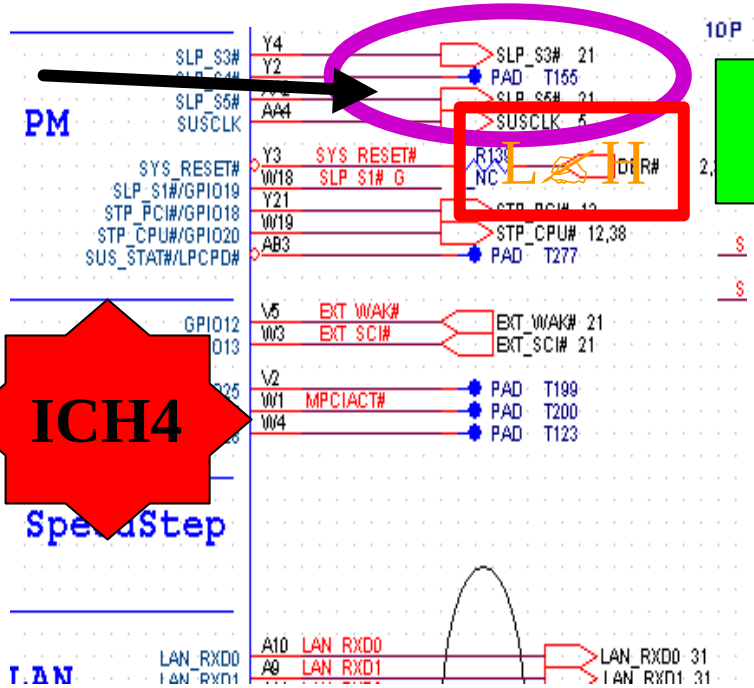
RTCRST# inactive to SUSCLK running,SLP_S3#,SLP_S5# inactive.

SLP_S3#,SLP_S5#(P09)

SUSPWROK H



SLP_S3#
SLP_S5#



Binchuan:

RSMRST# used for resetting the resume power plane logic.

Binchuan:

Inactive SLP_S3# signal detected by MACALLEN(SIO).

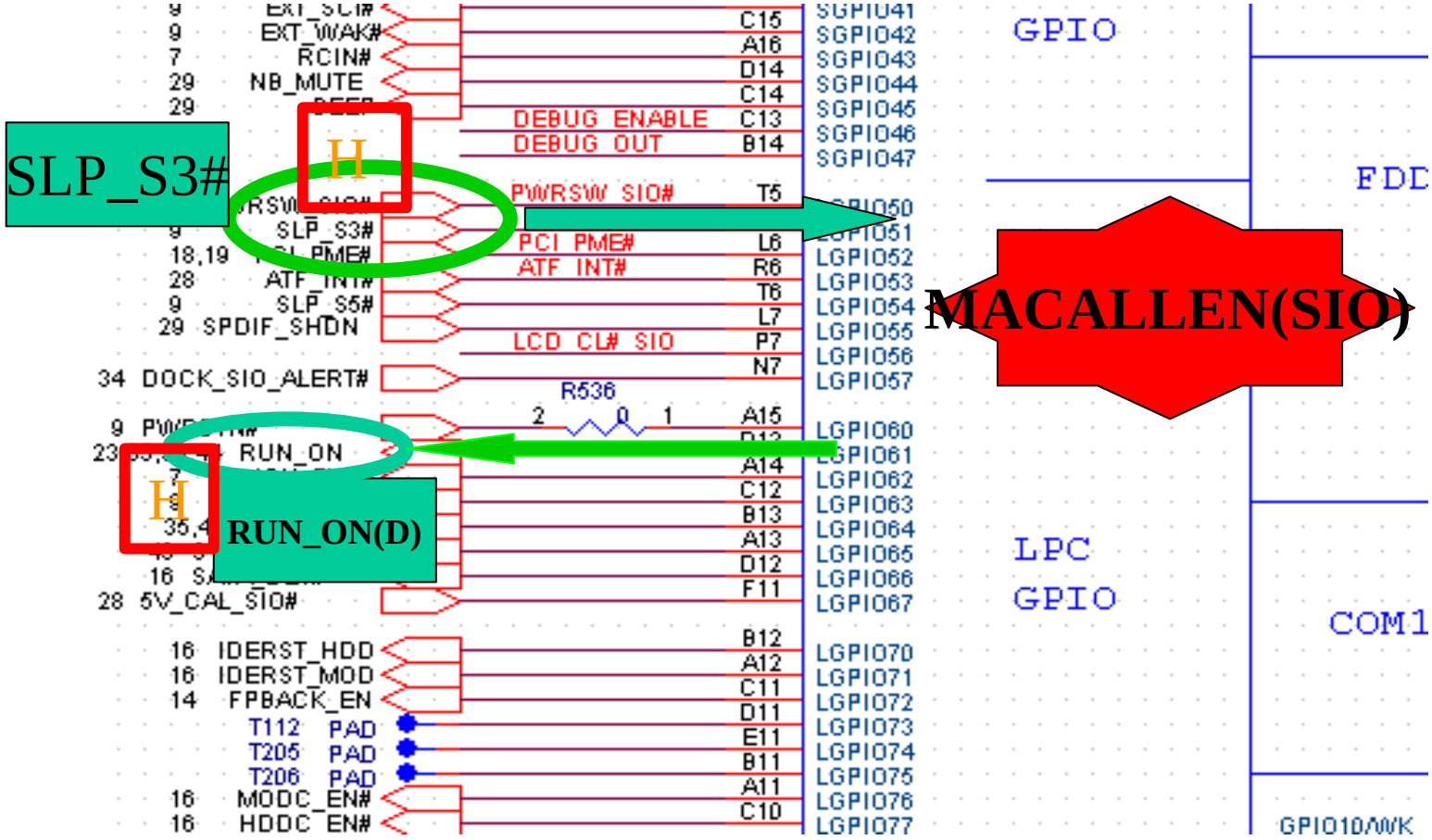
Logical Level **L** ✍ **H**.

Binchuan:

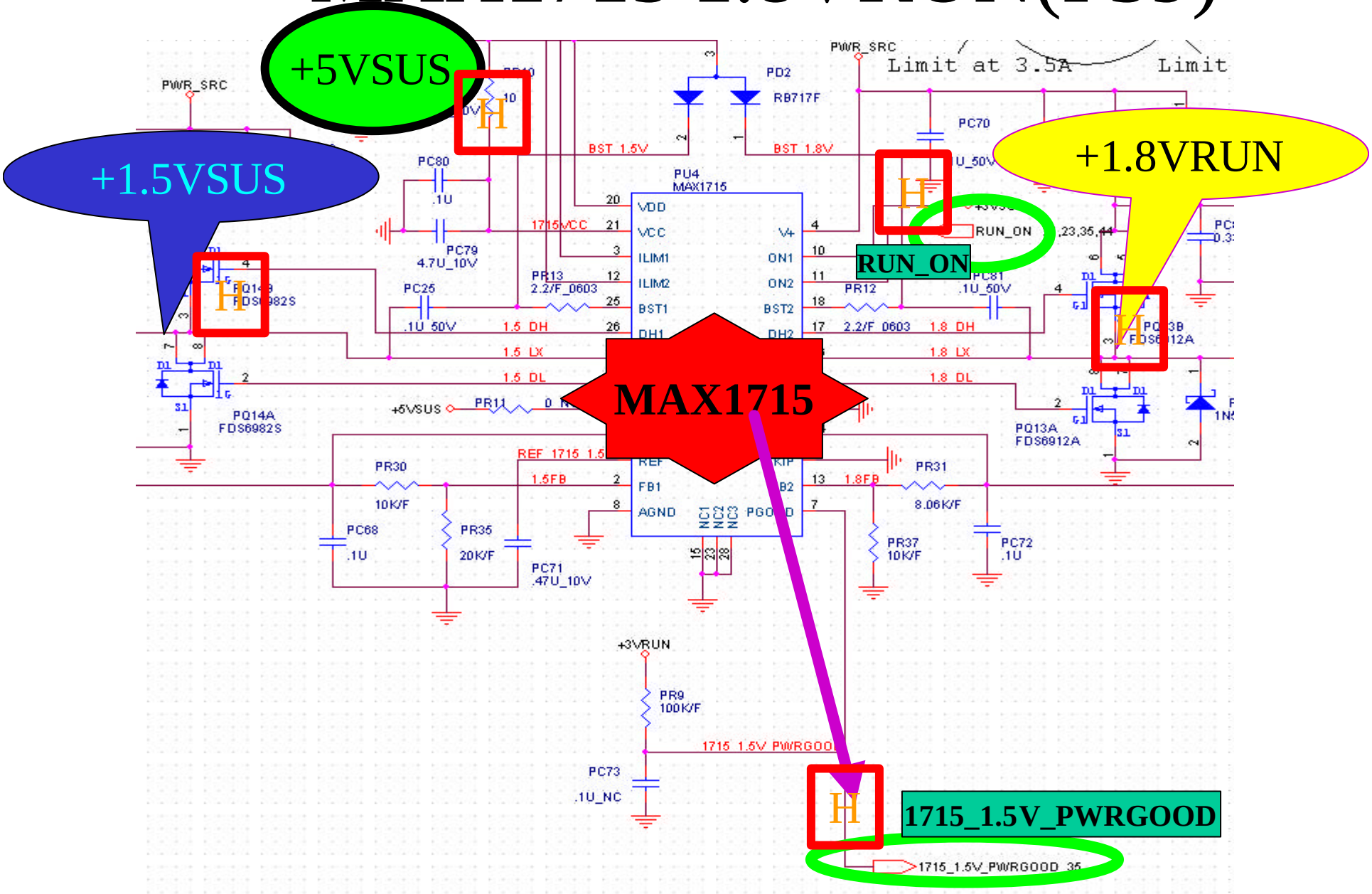
(D). SLP_S3# generate RUN_ON to turn on RUN Power plane.

P.S.: MACALLEN(SIO) ignore the SLP_S5# signal

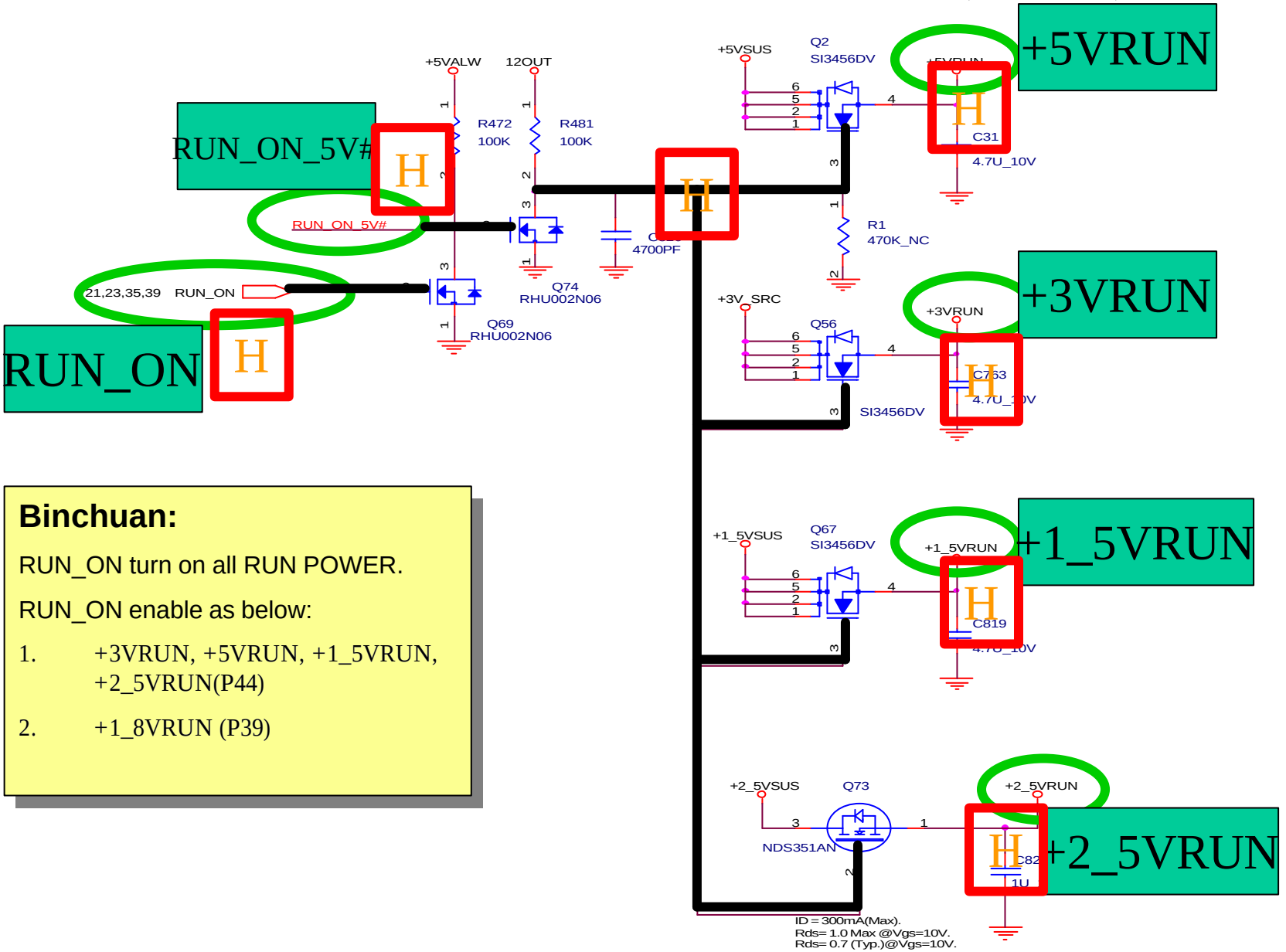
RUN_ON(P21)



MAX1715 1.8VRUN(P39)



RUN POWER(P44)



Binchuan:

RUN_ON turn on all RUN POWER.

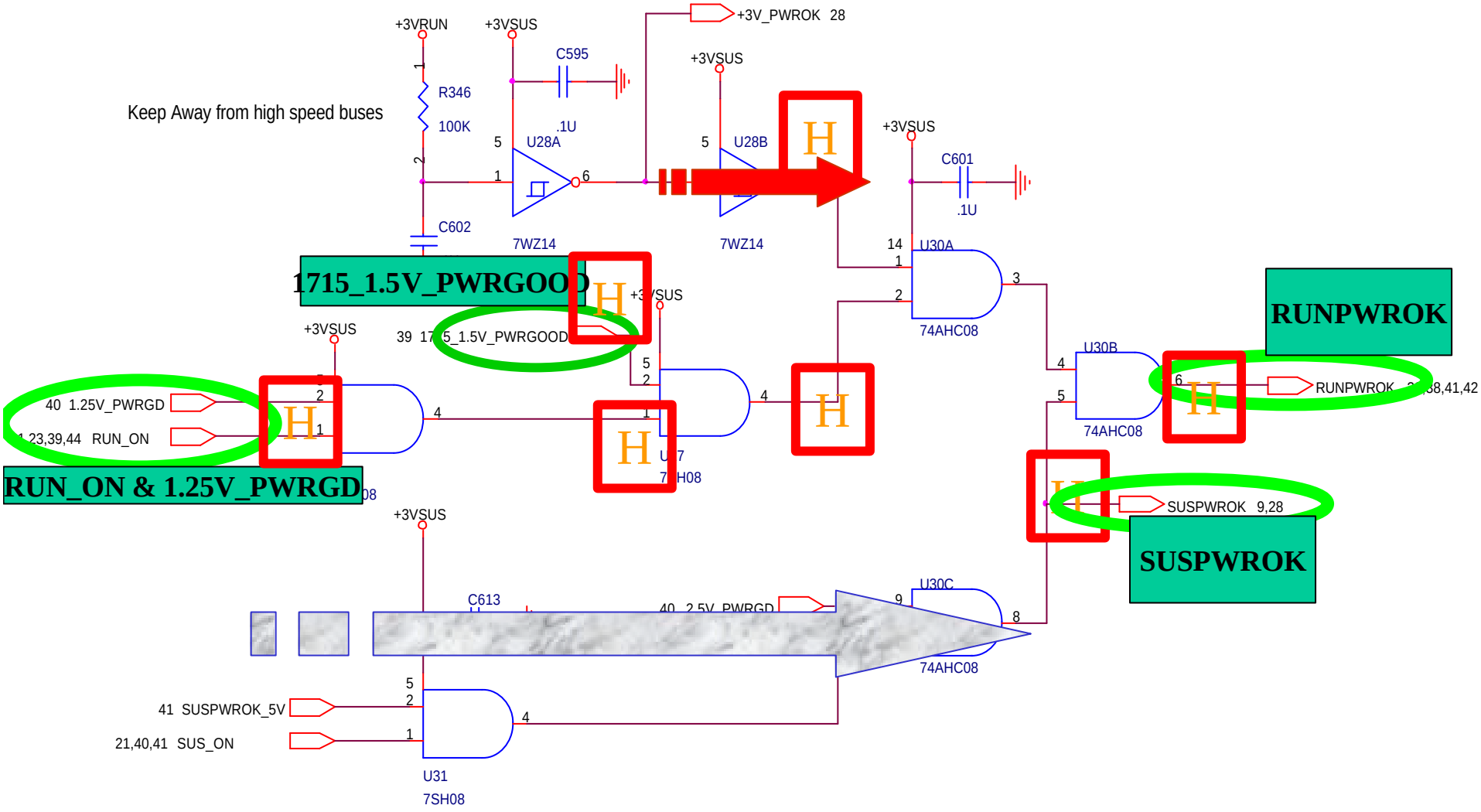
RUN_ON enable as below:

1. +3VRUN, +5VRUN, +1_5VRUN, +2_5VRUN(P44)
2. +1_8VRUN (P39)

Binchuan:

RUNPWROK turns on CPU VCORE POWER.

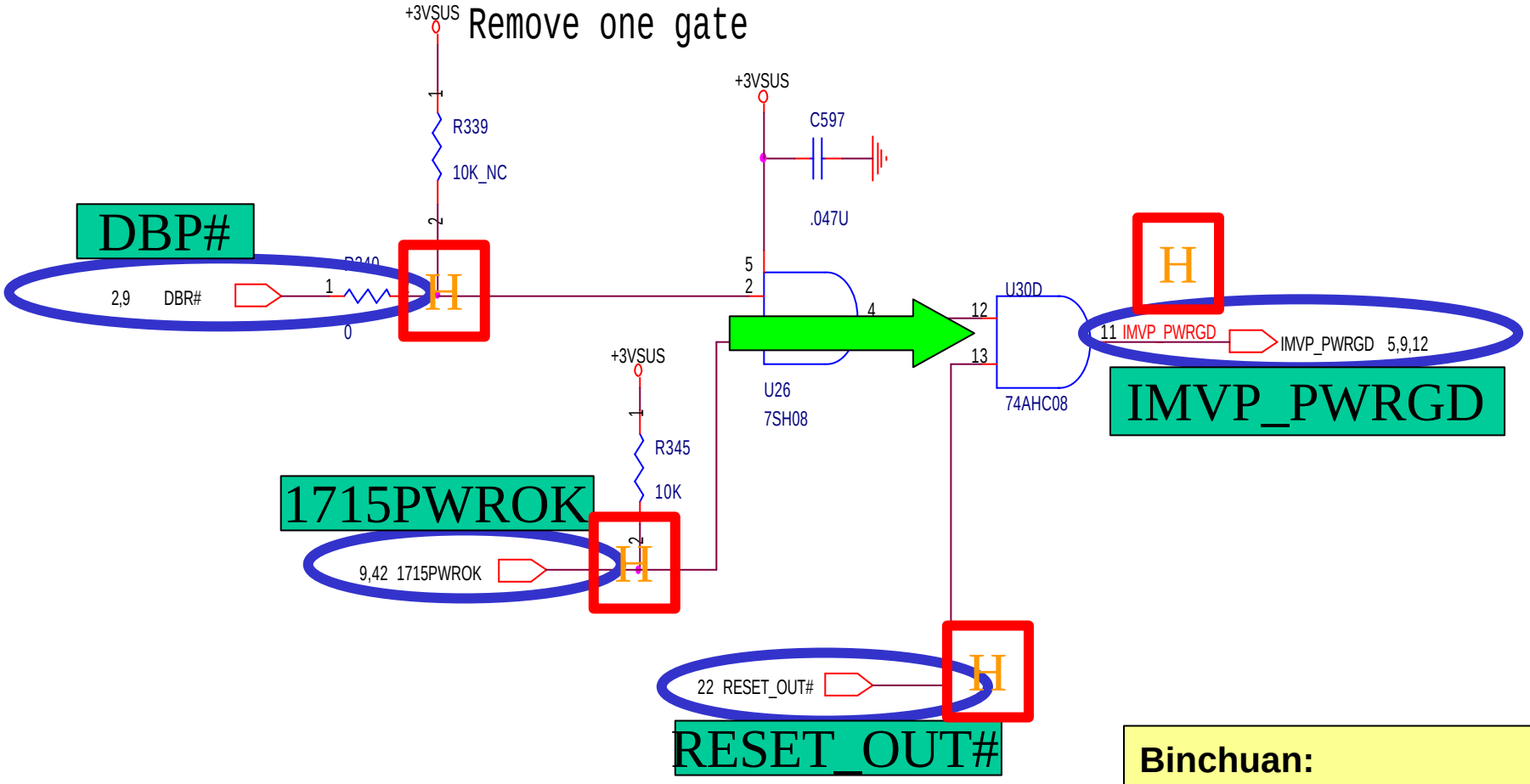
RUNPWROK(P35)



Binchuan:

DBR#(Date Bus Reset) is used only in processor systems where no debug port is implemented on system board. (Can be drive as system reset.)

IMVP_PWRGD(P35)



Binchuan:

RESET_OUT# comes from MACALLEN(SIO).

VTT_PWRGD#(P12)

Binchuan:

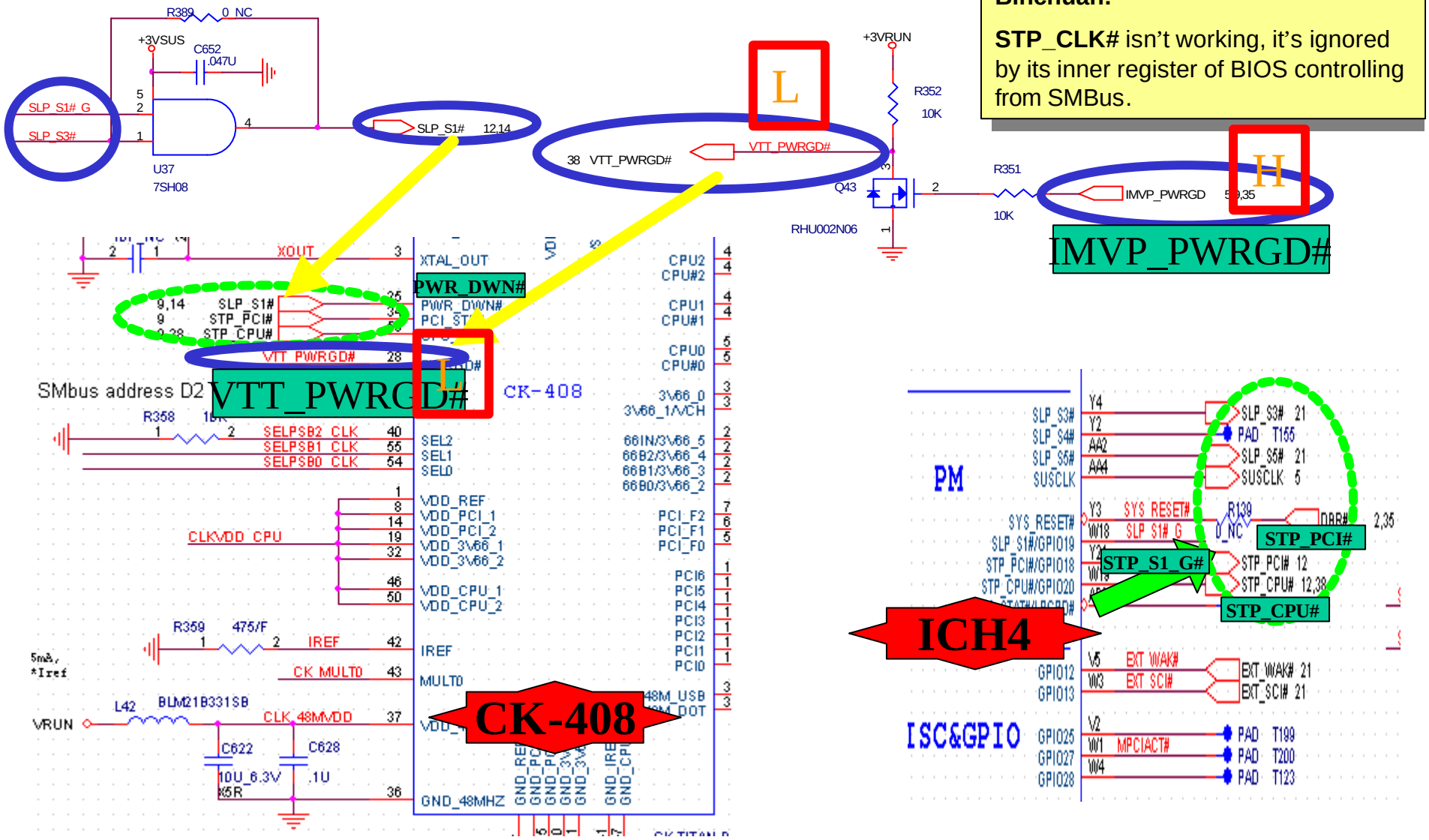
SLP_S3# & SLP_S1_G# inactive generate **SLP_S1#** inactive, so it causes **CK-408** active.

Binchuan:

Then VTT_PWRGD# causes **CK-408** pin-28 active to transmit All system clocks.**(STP_PCI#,STP_CPU#** can let system stop its Clock .)

Binchuan:

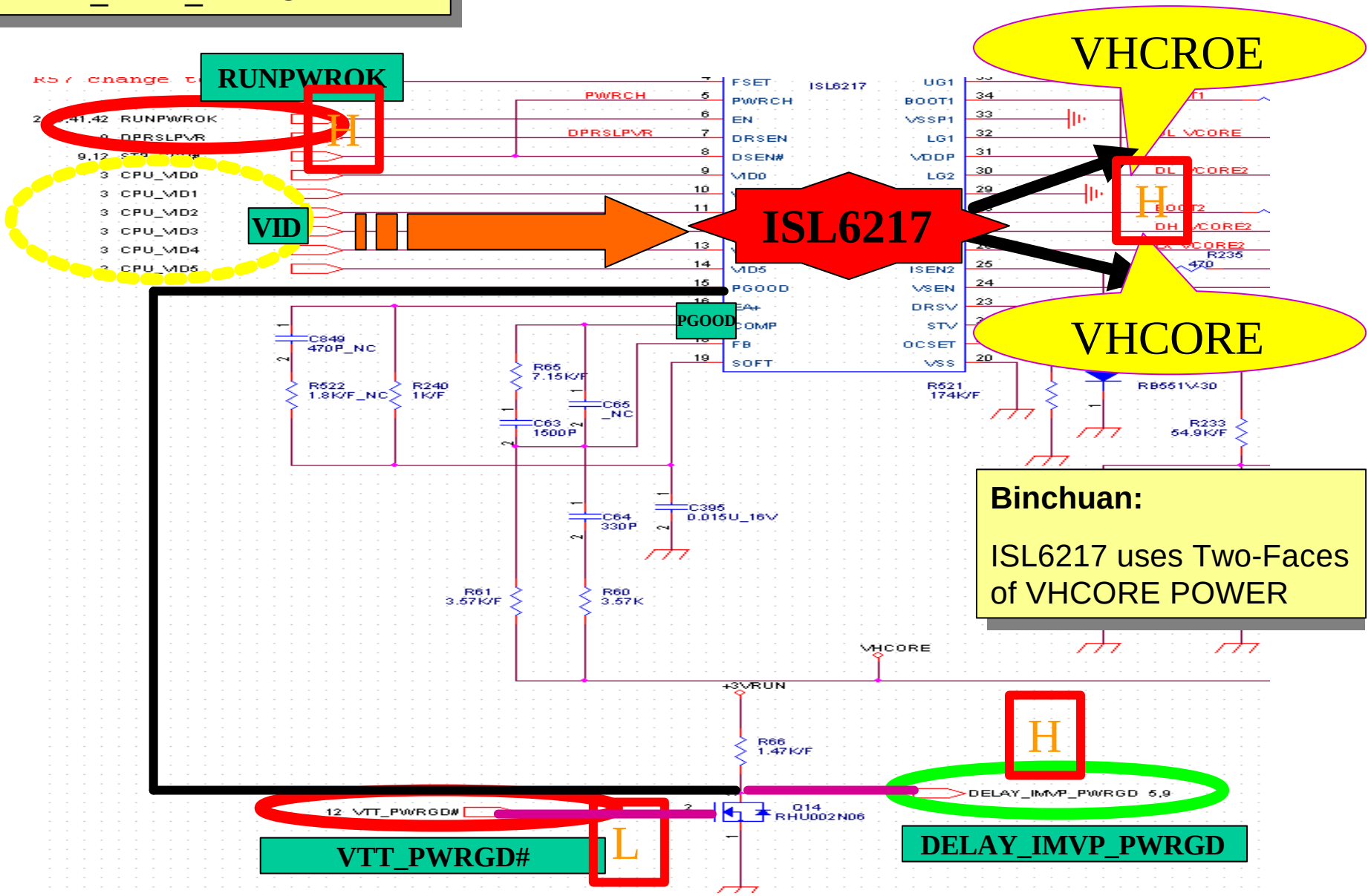
STP_CLK# isn't working, it's ignored by its inner register of BIOS controlling from SMBus.



Binchuan:

RUNPWROK ✍ VHCORE ✍ DELAY_IMVP_PWRGD.

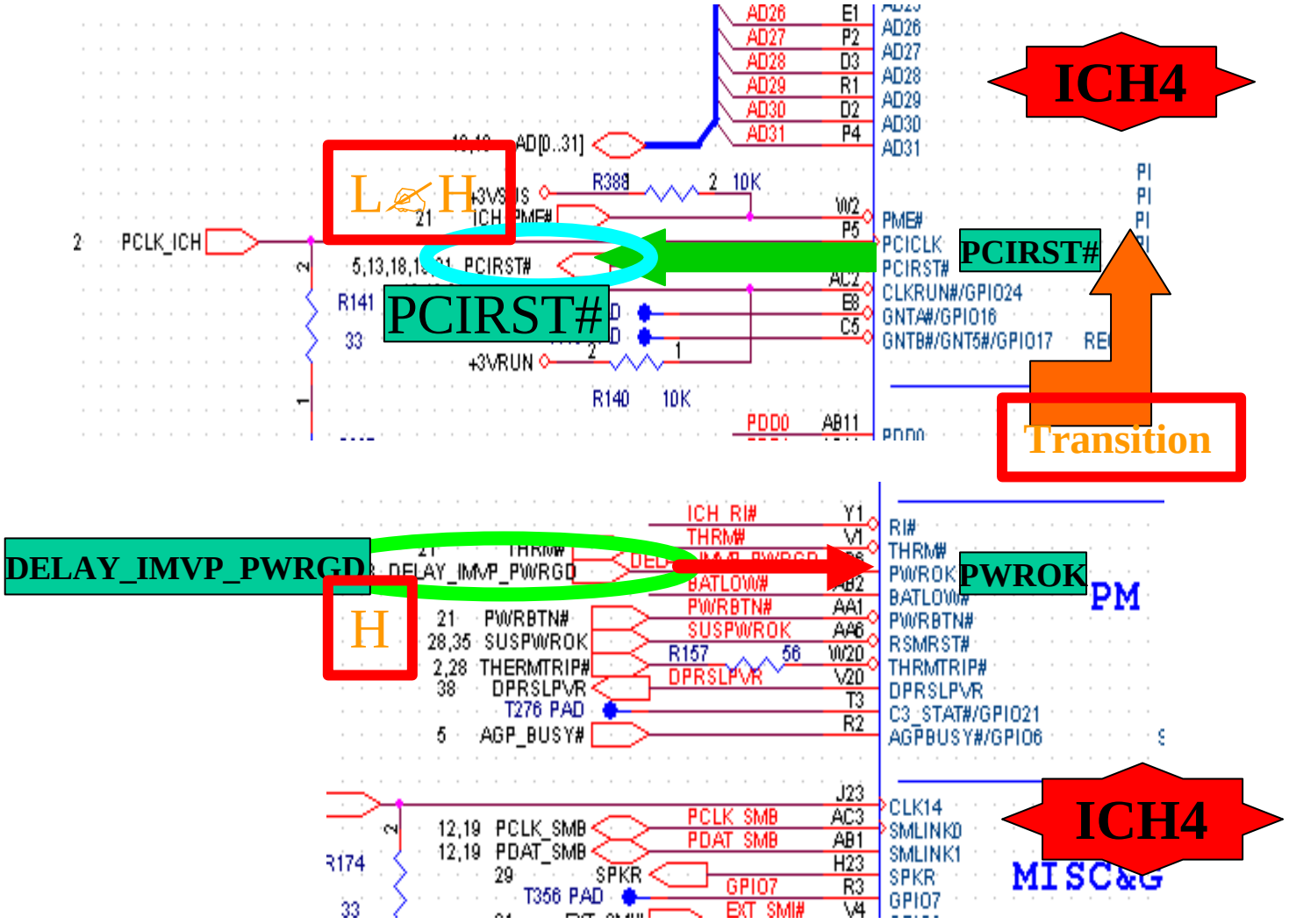
VHCORE, DELAY_IMVP_PWRGD(P38)



Binchuan:

(H). DELAY_IMVP_PWRGD access into ICH4 will generate PCIRST#(Low✍High) **L✍H**

PCIRST#(P7,9)



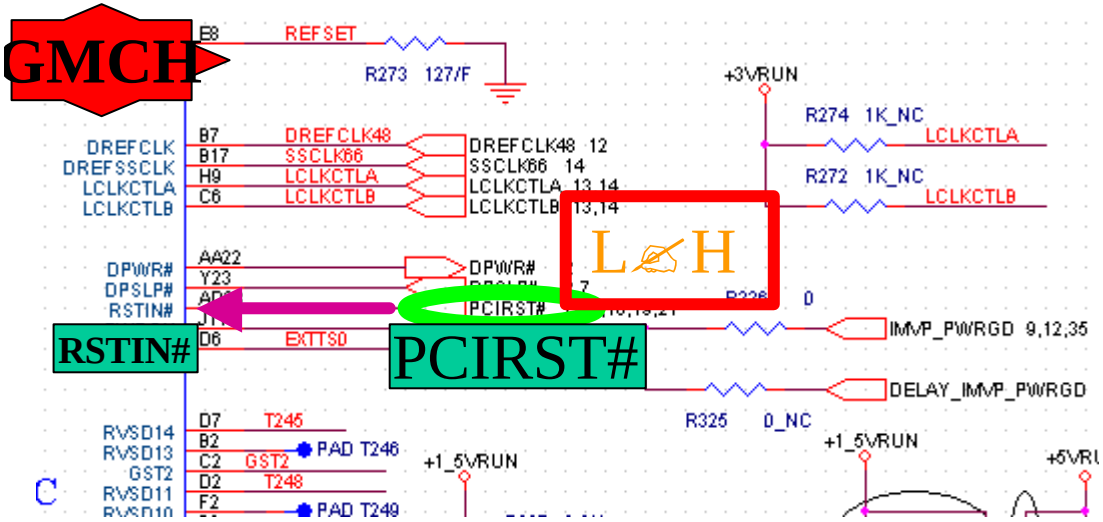
Binchuan:

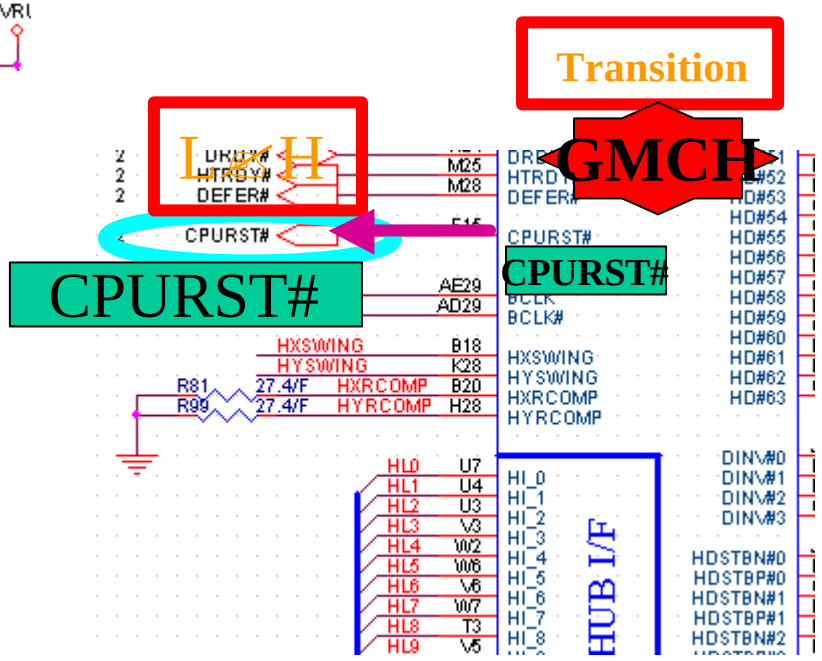
(I). PCIRST# access into GMCH to generate CPURST#.

CPURST#(P4,5)

Binchuan:

PCIRST# inactive will occur CPURST# inactive.

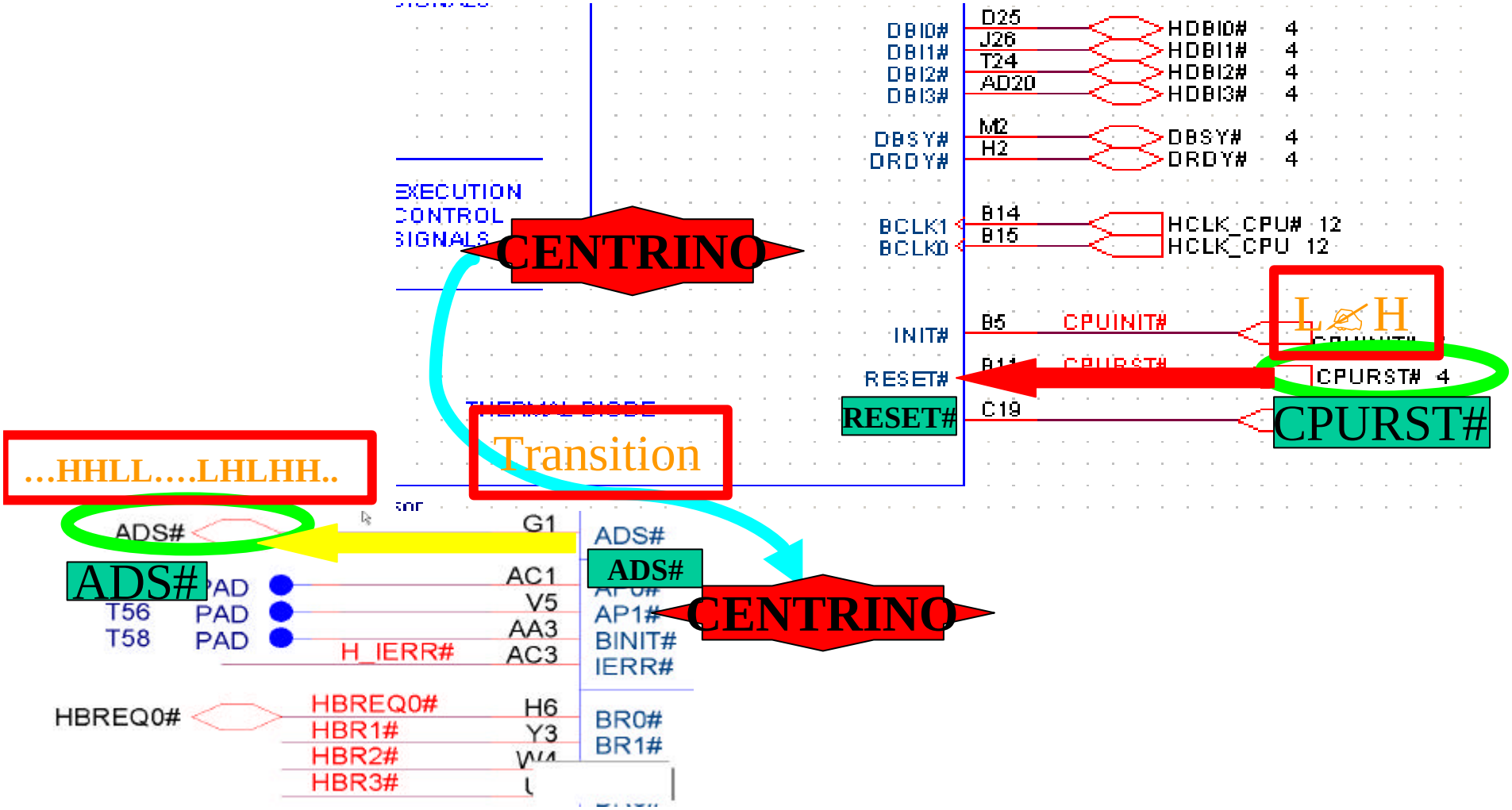




Binchuan:

After CPURST# inactive, and all other **necessary signals are all to be initiated from ICH-4 to CPU** that have correct configuration.

ADS#, Miscellanea(P2)

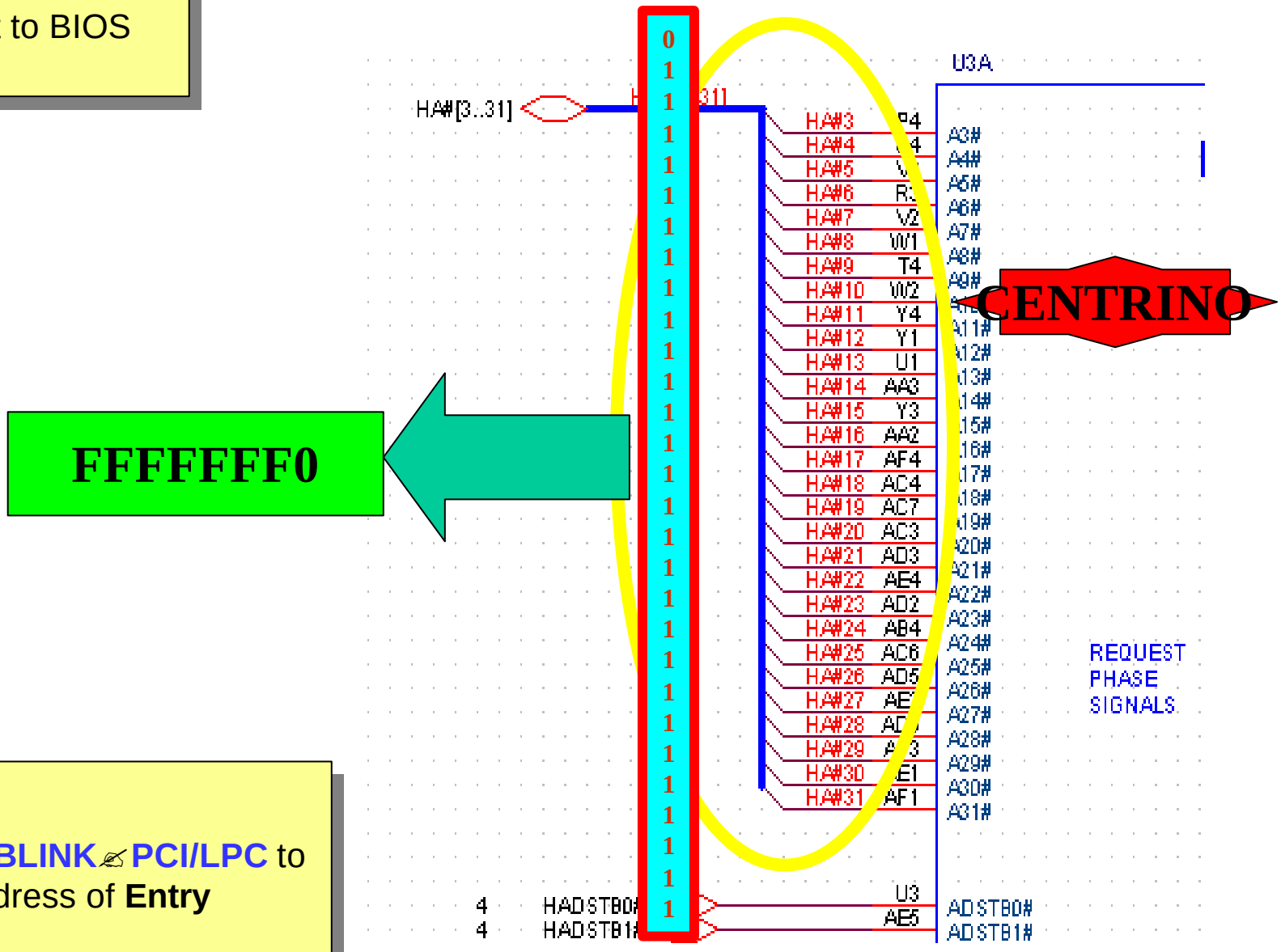


Binchuan:

The Inner A0#~A2# value is 000.

FFFFFFF0 point to BIOS Entry-Point.

The address of Entry-Point(P2)



Binchuan:

AGTL+ ✍ HUBLINK✍PCI/LPC to point BIOS address of **Entry address.**

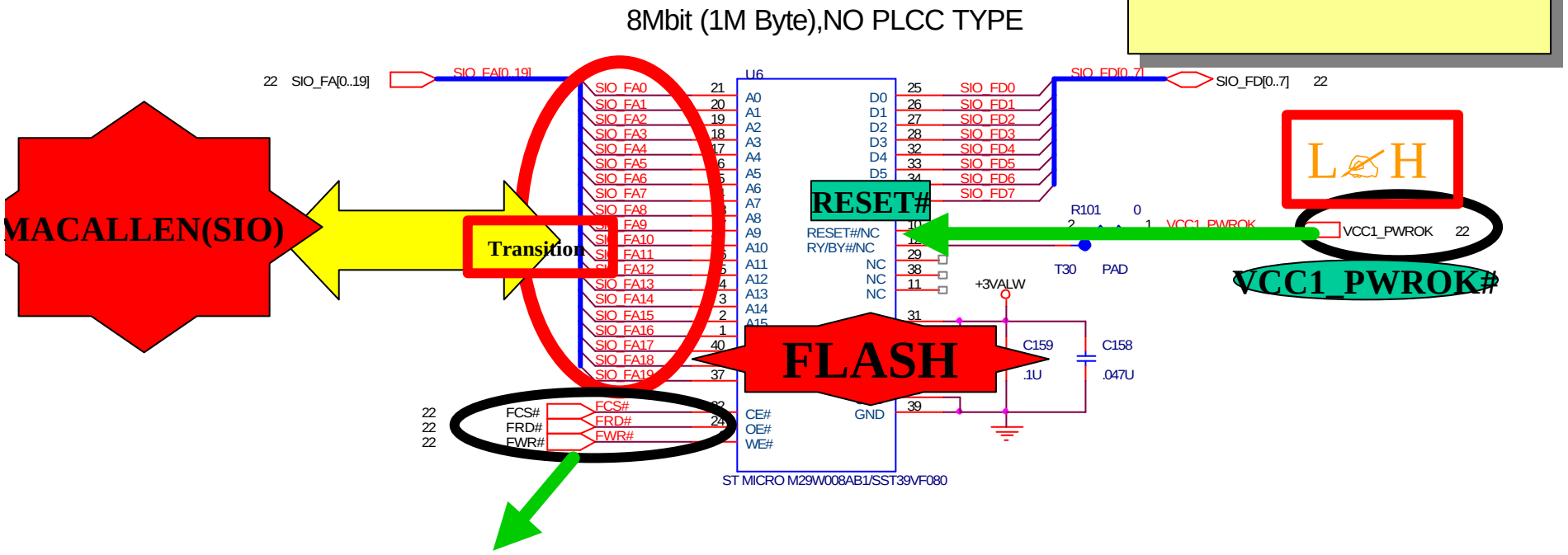
Binchuan:

FLASH need VCC1_PWROK# to reset, and FLASH Control Signal from MACALLEN(SIO).

Remainder action of Power on(P25)

Binchuan:

VCC1_PWROK# inactive while +3VALW assert.



Binchuan:

FLASH Control signals.

Binchuan:

FLASH connect with MACALLEN(SIO) by

X-BUS. And SIO has some translated instructions to do its interpretation/ translation.

Summary Sequence (1)

Test Purpose:	To record the timing sequence for the power rails.
Overview of Procedure:	Measure the timing of the power rails. The definition of these timing variables is given in the power sequencing document attached below this table.

Timing Variable	Time	Comments
T1	280us	Delay time form DC_IN+ to +RTCSRC
T2	-200us	Delay time form +RTCSRC to +RTC_PWR5V
T3	-184us	Delay time form +RTC_PWR5V to +RTC_PWR3_3V
T4	170us	Delay time form +RTC_PWR3_3V to +3VALW
T5	-80us	Delay time form +3VALW to +5VALW
T6	580us	Delay time form +5VALW to POWER_SIO#
T7	-454.2ms	Delay time form POWER_SIO# to SUS_ON
T8	-3.744us	Delay time form SUS_ON to AUXEN
T9	520us	Delay time form AUXEN to +3V_LAN
T10	-80us	Delay time form +3V_LAN to 12OUT
T11	30us	Delay time form 12OUT to +5VSUS
T12	10us	Delay time form +5VSUS to +3V_SRC
T13	46.8ms	Delay time form +3V_SRC to SUSPWROK_5V
T14	-46ms	Delay time form SUSPWROK_5V to +1.5VSUS
T15	-880us	Delay time form +1.5VSUS to 3VSUS_ON
T16	-80us	Delay time form 3VSUS_ON to +3VSUS
T17	860us	Delay time form +3VSUS to +2.5VSUS
T18	780us	Delay time form +2.5VSUS to SMDDR_VREF
T19	420us	Delay time form SMDDR_VREF to 2.5V_PWRGD
T20	157ms	Delay time form 2.5V_PWRGD to LAN_PWROK

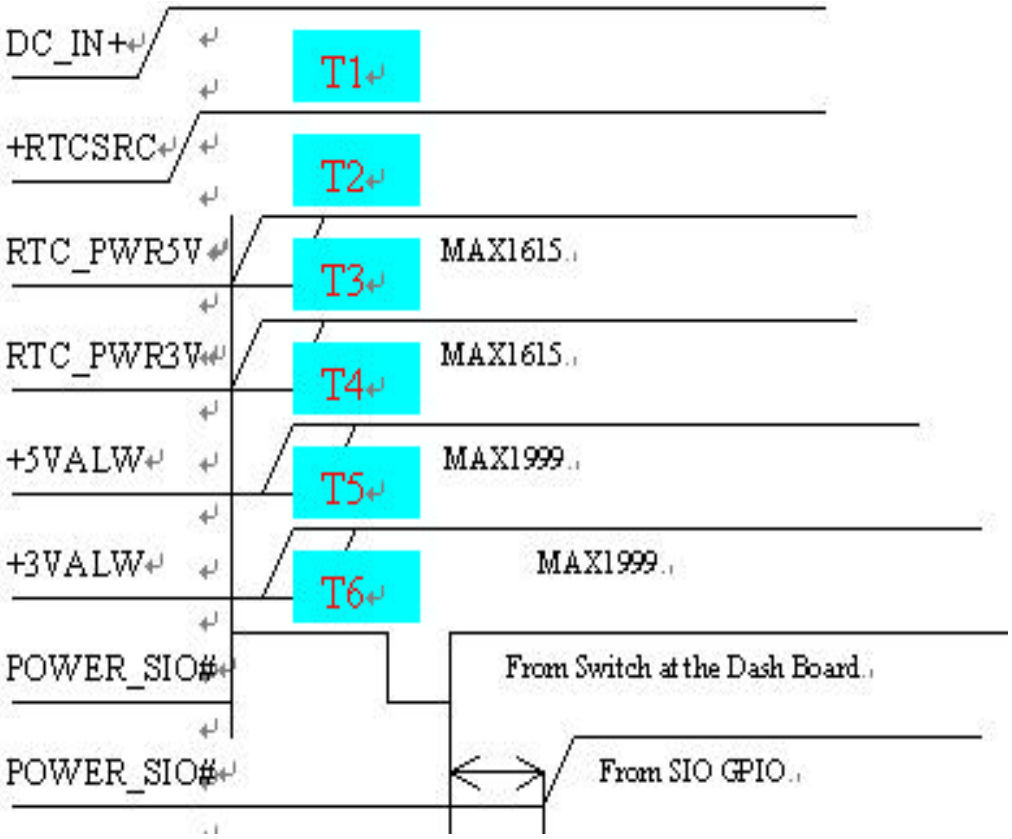
Summary Sequence (2)

T21	-127ms	Delay time form LAN_PEROK to SUSPWROK
T22	98ms	Delay time form SUSPWROK to RUN_ON
T23	290us	Delay time form RUN_ON to +2_5VRUN
T24	30us	Delay time form +2.5VRUN to +3VRUN
T25	-57us	Delay time form +3VRUN to +1.5VRUN
T26	110us	Delay time form +1.5VRUN to +5VRUN
T27	256us	Delay time form +5VRUN to SMDDR_VTERM
T28	1.372ms	Delay time form SMDDR_VTERM to 1.25V_PWRGD
T29	-1.728ms	Delay time form 1.25V_PWRGD to +1.8VRUN
T30	194us	Delay time form +1.8VRUN to 1715_1.5V_PWRGOOD
T31	8.86ms	Delay time form 1715_1.5V_PWRGOOD to RUNPWROK
T32	15.12us	Delay time form RUNPWROK to +12V
T33	940us	Delay time form +12V to +VCC1_2V_MCH
T34	-70us	Delay time form +VCC1_2V_MCH to CPU VTT
T35	410us	Delay time form CPU VTT to 1715PWROK
T36	9.79ms	Delay time form 1715PWROK to VCORE_PWRGOOD_D

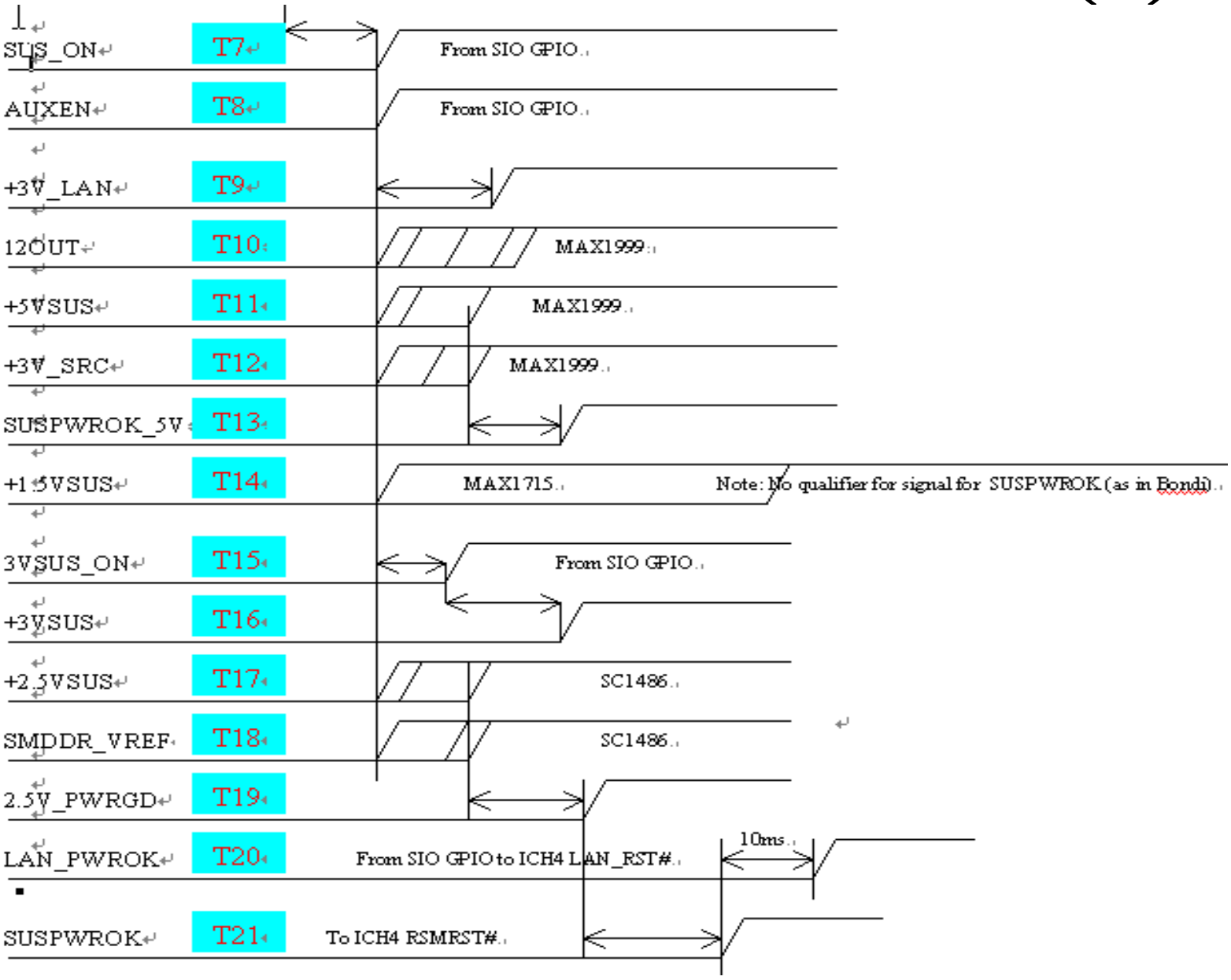
Summary Sequence (3)

T37	9.2ms	Delay time form VCORE_PWRGOOD_D to DBR# and RESET_OUT#
T38	-10us	Delay time form DBR# and RESET_OUT# to IMVP_PWRGD
T39	-29.26ms	Delay time form IMVP_PWRGD to VTT_PWRGD#
T40	9.16ms	Delay time form VTT_PWRGD# to VHCORE
T41	28.88ms	Delay time form CPU VCC CPRE to DELAY_IMVP_PWRGD
T42	-7.16ms	Delay time form DELAY_IMVP_PWRGD to CK408 OUT PUT
T43	8.32ms	Delay time form CK408 OUT PUT to PCIRST#
T44	900us	Delay time form PCIRST# to CPURST#
T45	-28.86ms	Delay time form CPURST# to CPU VID
Section Owner:		
Section Tester:		
Time To Complete:		
Date Finished:	Dec/05/2002	

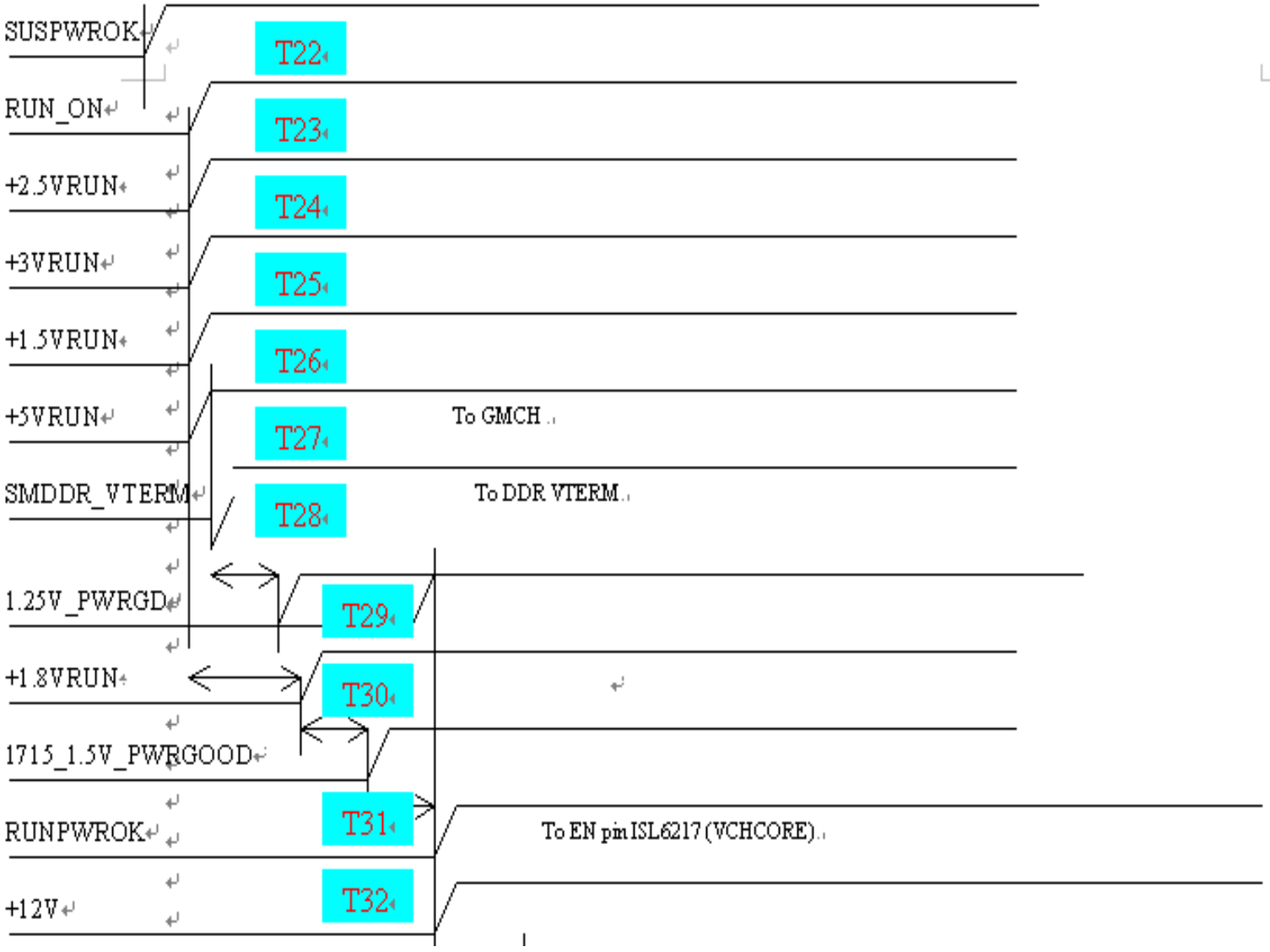
The Procedure of Power-UP(1)



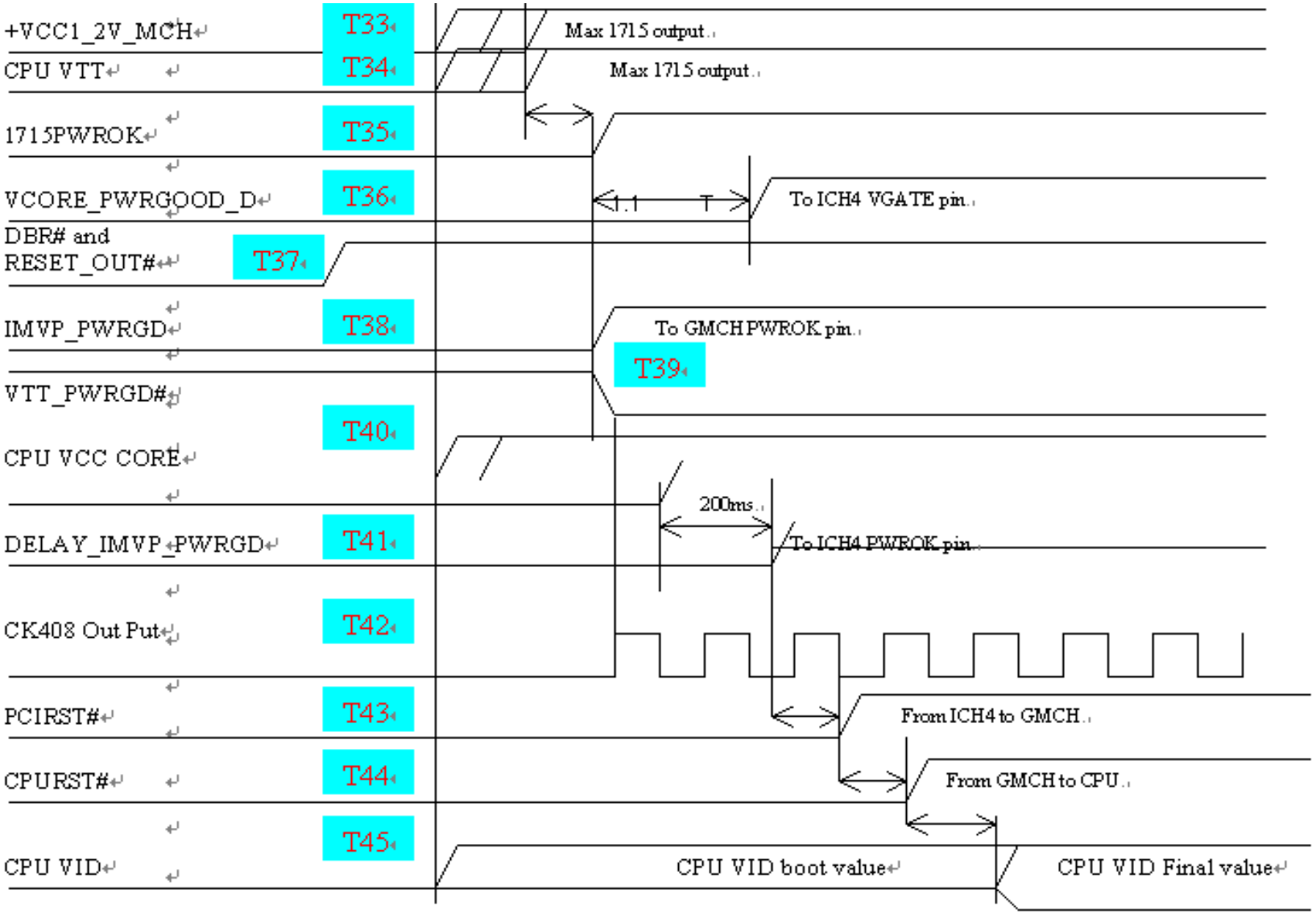
The Procedure of Power-UP(2)



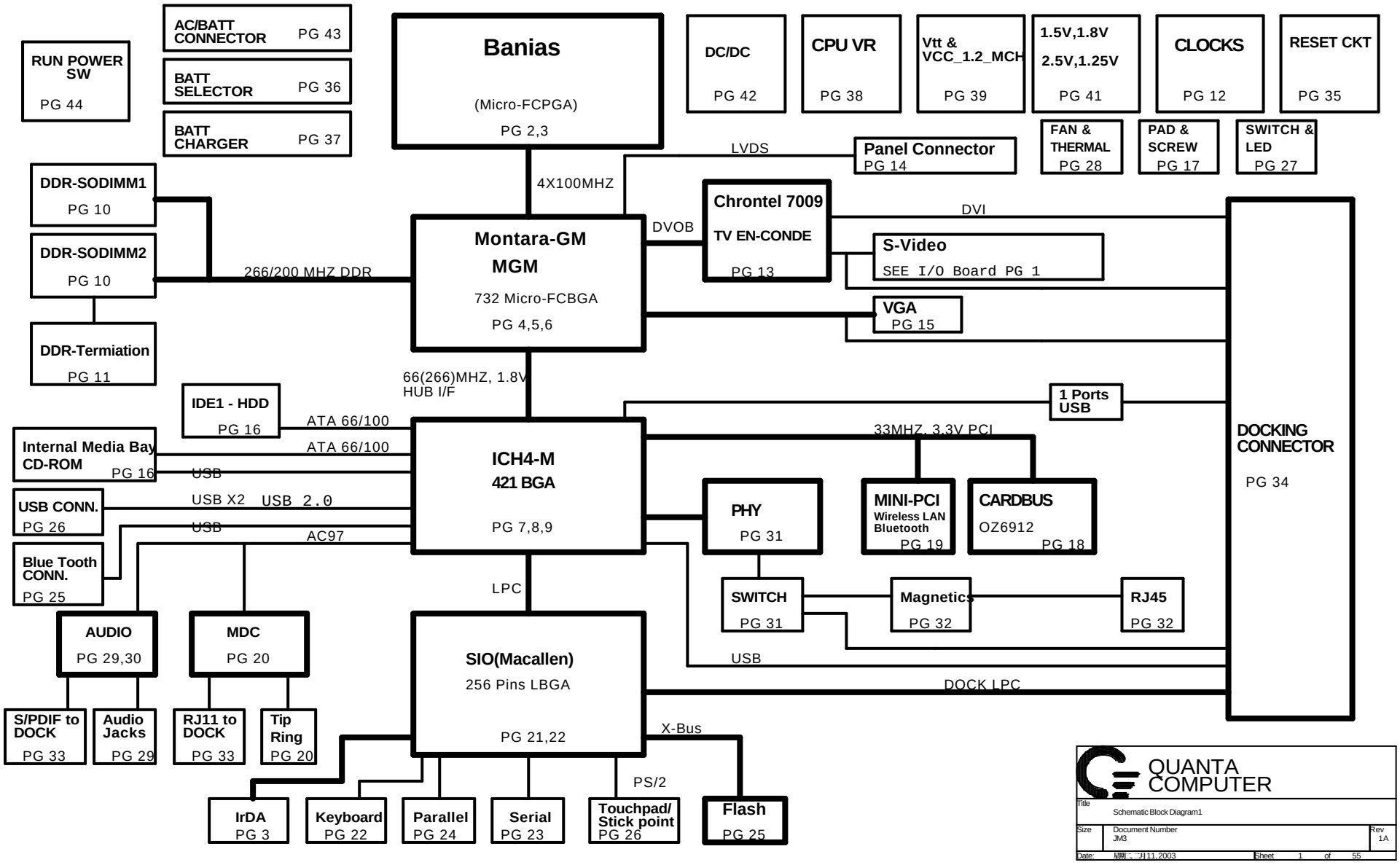
The Procedure of Power-UP(3)



The Procedure of Power-UP(4)



Appendix.
DAYTONA



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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