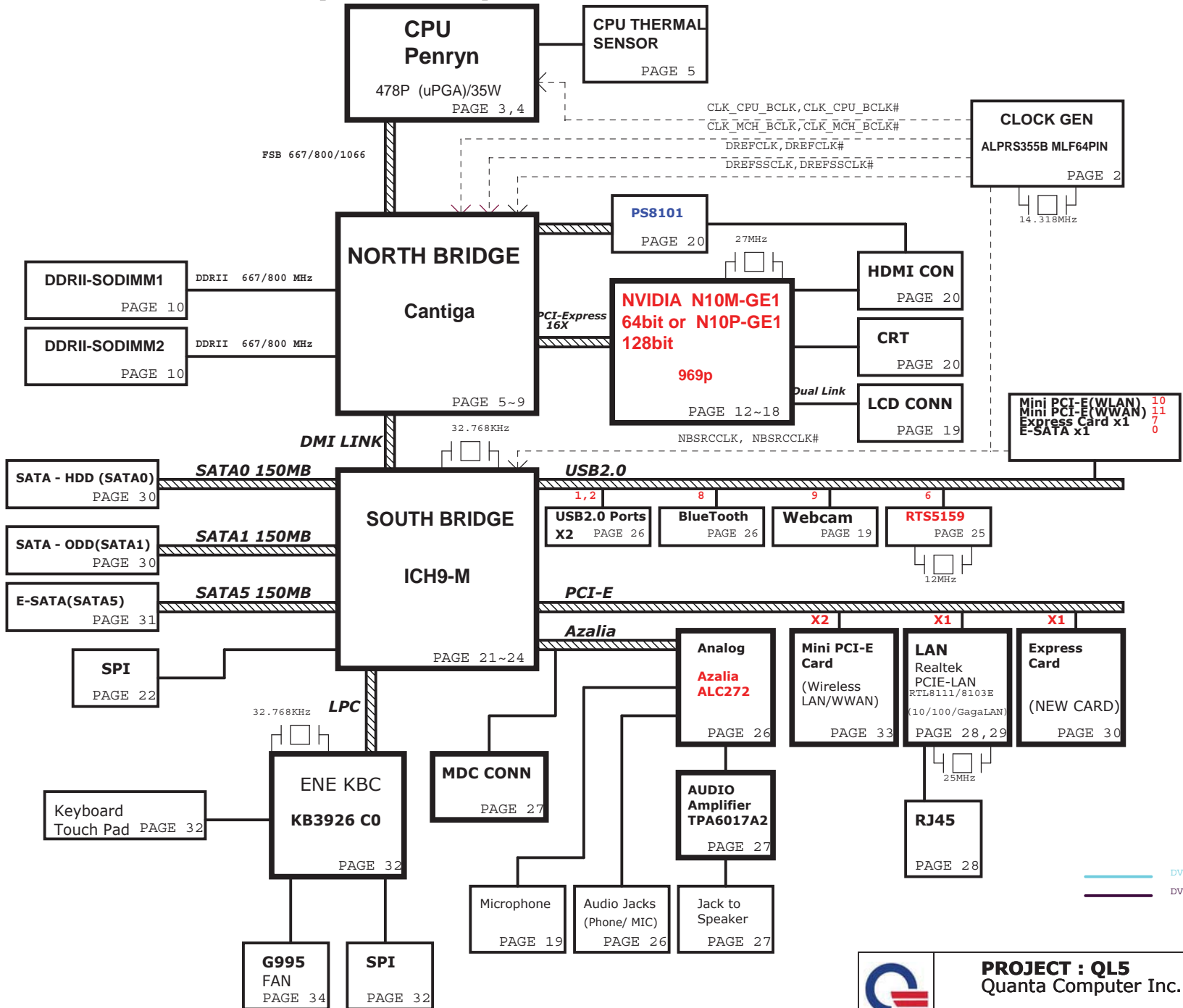


**PCB STACK UP**  
8L

<http://hobi-elektronika.net>  
**QL5(15.6W) BLOCK DIAGRAM**

01

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SGND1
- LAYER 5 : SVCC
- LAYER 6 : IN2
- LAYER 7 : SGND2
- LAYER 8 : BOT

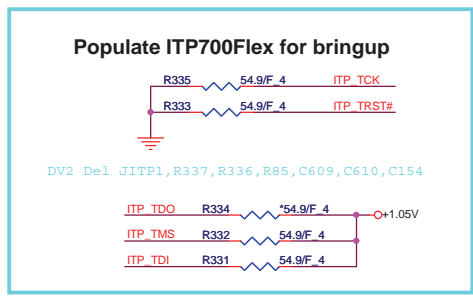
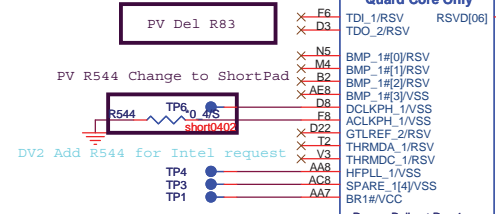
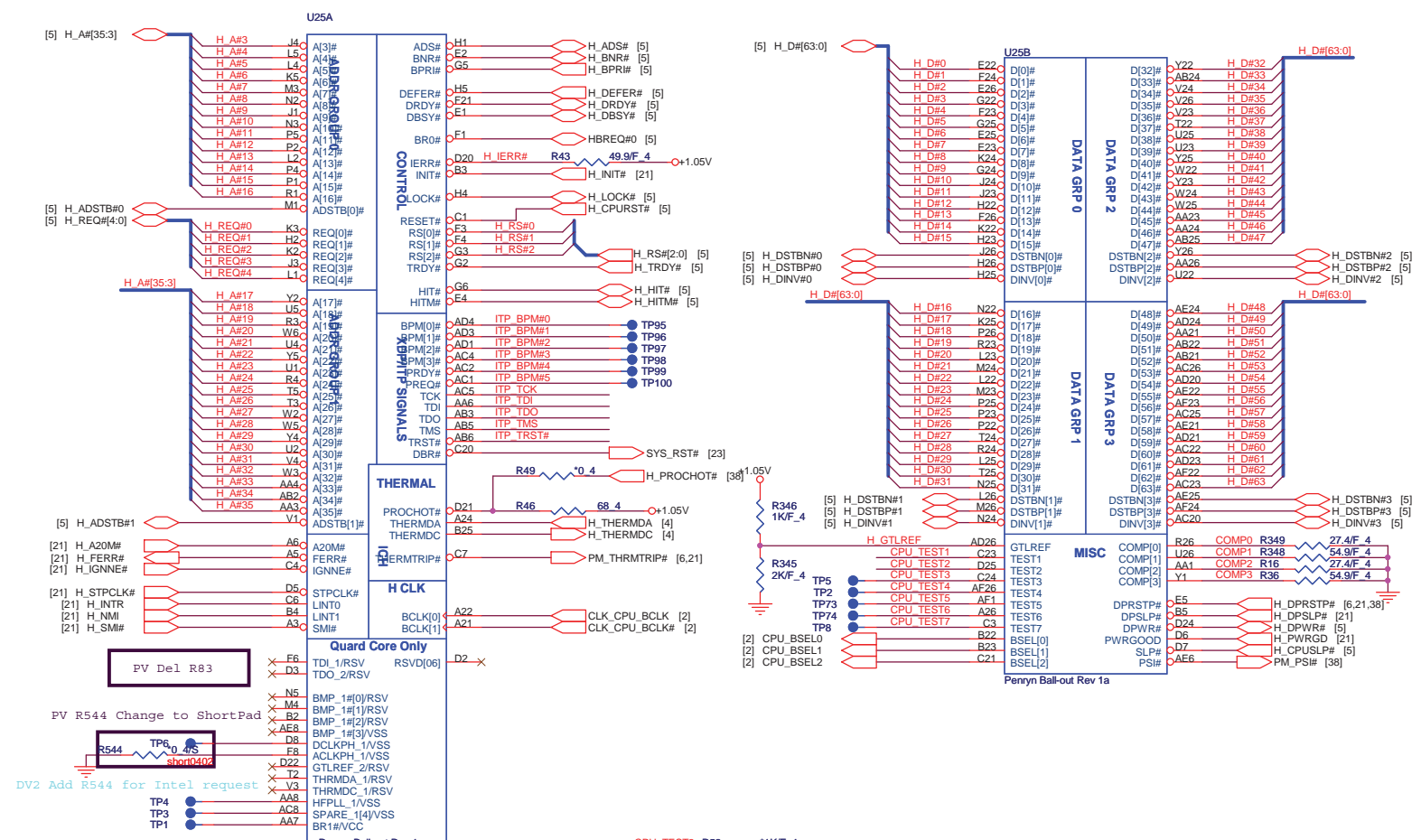


- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 35
- SYSTEM POWER ISL6237IRZ-T PAGE 36
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 37
- CPU CORE ISL6266A PAGE 38
- VGACORE(1.025V)Oz8118 PAGE 39
- DDR II SMDR\_VTERM 1.8V/1.8VSUS(TPSS51116REGR) PAGE 40

	<b>PROJECT : QL5</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number	
Date: Tuesday, March 17, 2009		Sheet 1 of 41	

DV2  
DV3





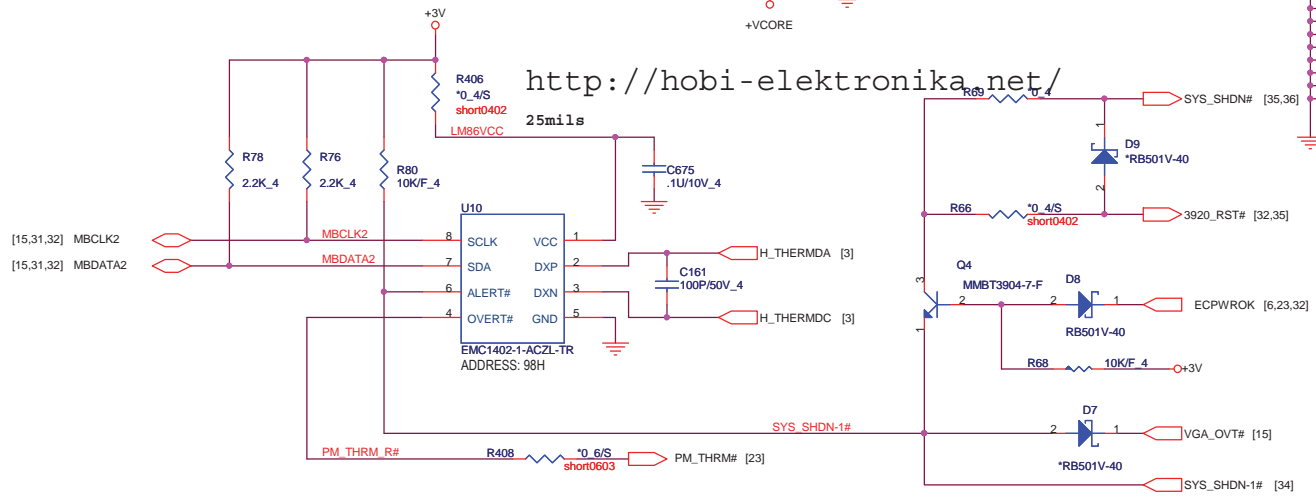
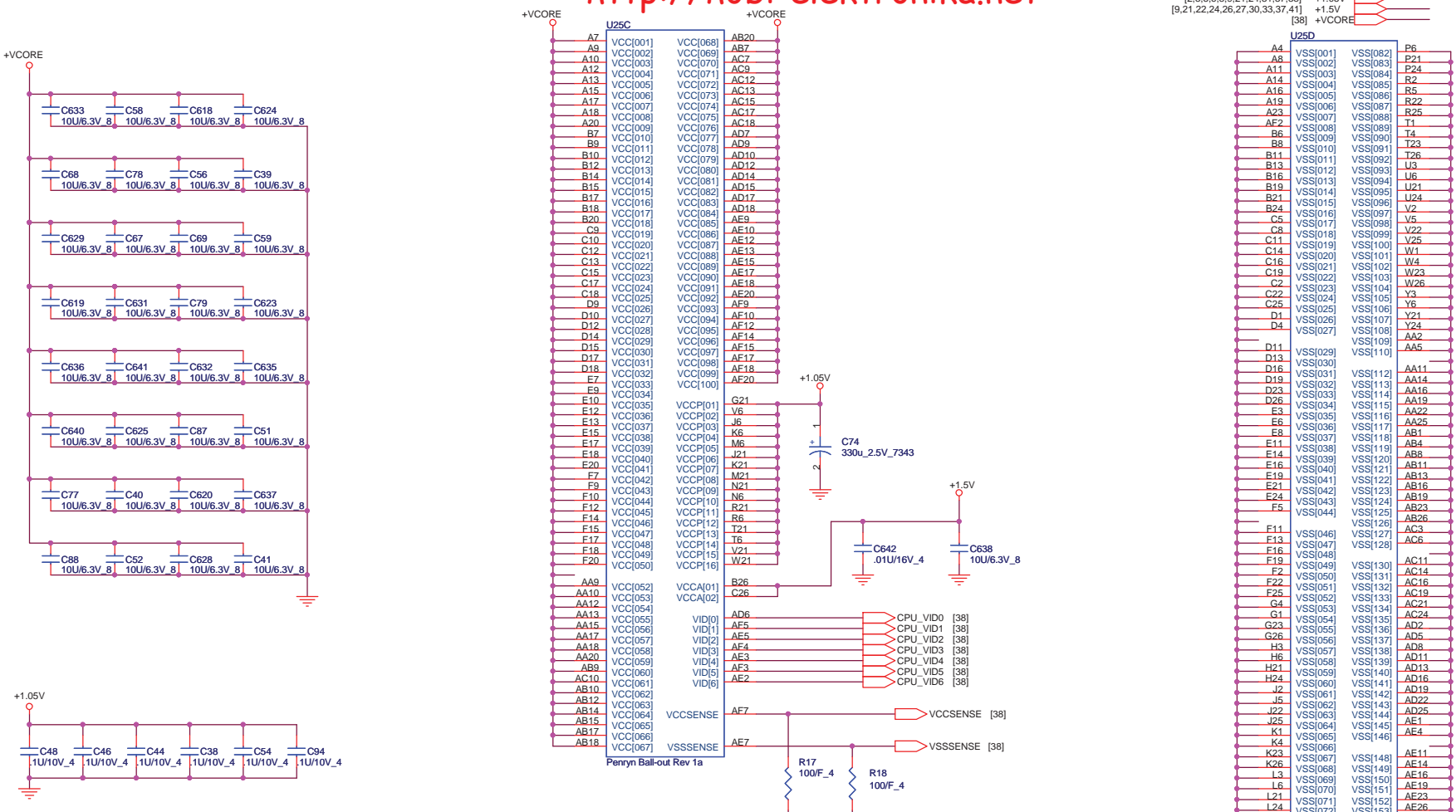
DV2 Del JITP1, R337, R336, R85, C609, C610, C154

**PROJECT : QL5**  
Quanta Computer Inc.

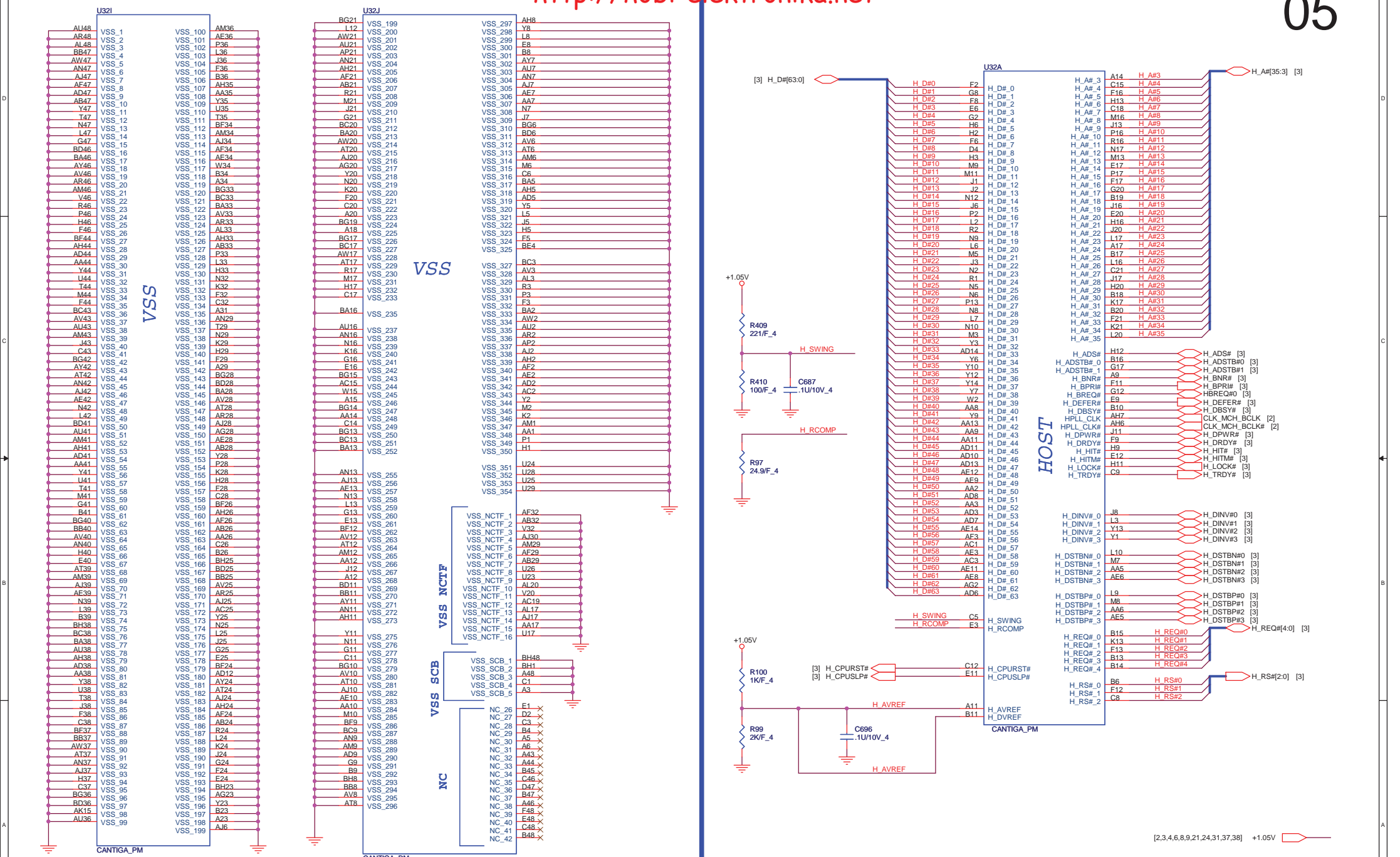
**NB5**

Size Custom Document Number Penryn 1/2 Rev 1A

Date: Tuesday, March 17, 2009 Sheet 3 of 41



**PROJECT : QL5**  
 Quanta Computer Inc.



**PROJECT : QL5**  
**Quanta Computer Inc.**

**NB5**

Size Custom Document Number Cantiga Host & VSS 1/5 Rev 1A

Date: Tuesday, March 17, 2009 Sheet 5 of 41

MCH\_CFG\_5 DMi2 selection
Low: DMi2
High: DMi4 (Default)
MCH\_CFG\_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH\_CFG\_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)
MCH\_CFG\_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved
MCH\_CFG\_6 ITPM Host Interface

Low: ITPM Host Interface enabled
High: ITPM Host Interface disabled (Default)
MCH\_CFG\_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH\_CFG\_10 PCIe Lookback Enable
Low: Enabled
High: Disabled (Default)
MCH\_CFG\_12/13 XOR/ALLZ/CLOCK Un-gating

MCH\_CFG\_13 MCH\_CFG\_12 Configuration
0 0 Reserved
0 0 XOR Mode enabled
0 1 All-Z Mode enabled
1 1 Normal operation (Default)

ME\_JTAG\_TCK
ME\_JTAG\_TDI
ME\_JTAG\_TDO
ME\_JTAG\_TMS

MCH\_BSEL0
MCH\_BSEL1
MCH\_CFG\_3
MCH\_CFG\_4
MCH\_CFG\_5
MCH\_CFG\_6
MCH\_CFG\_7
MCH\_CFG\_8
MCH\_CFG\_9
MCH\_CFG\_10
MCH\_CFG\_11
MCH\_CFG\_12
MCH\_CFG\_13
MCH\_CFG\_14
MCH\_CFG\_15
MCH\_CFG\_16
MCH\_CFG\_17
MCH\_CFG\_18
MCH\_CFG\_19
MCH\_CFG\_20

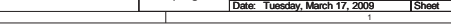
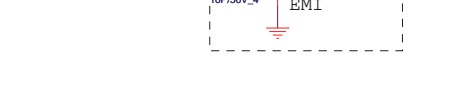
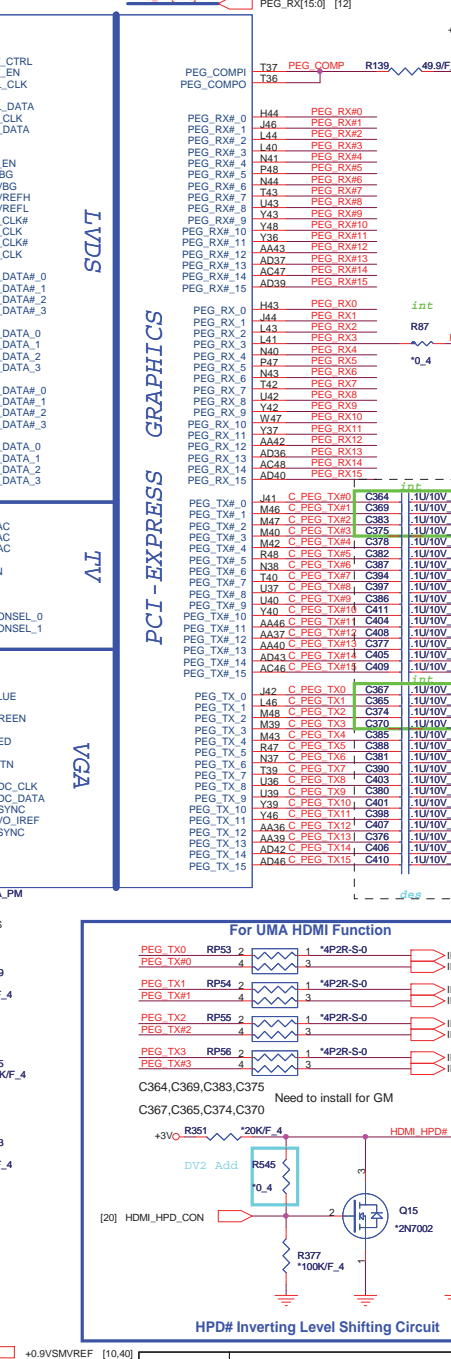
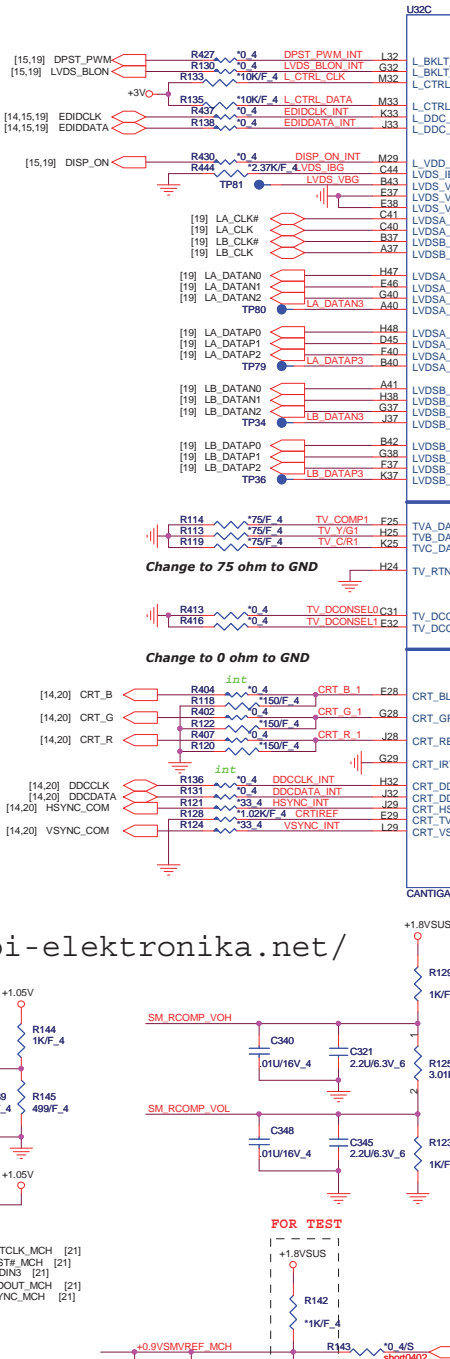
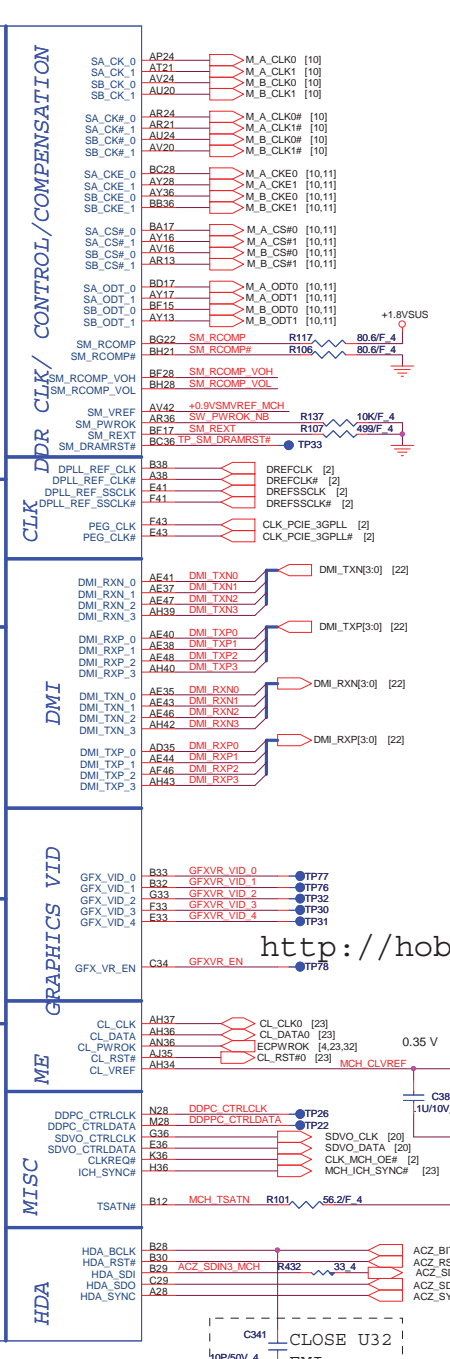
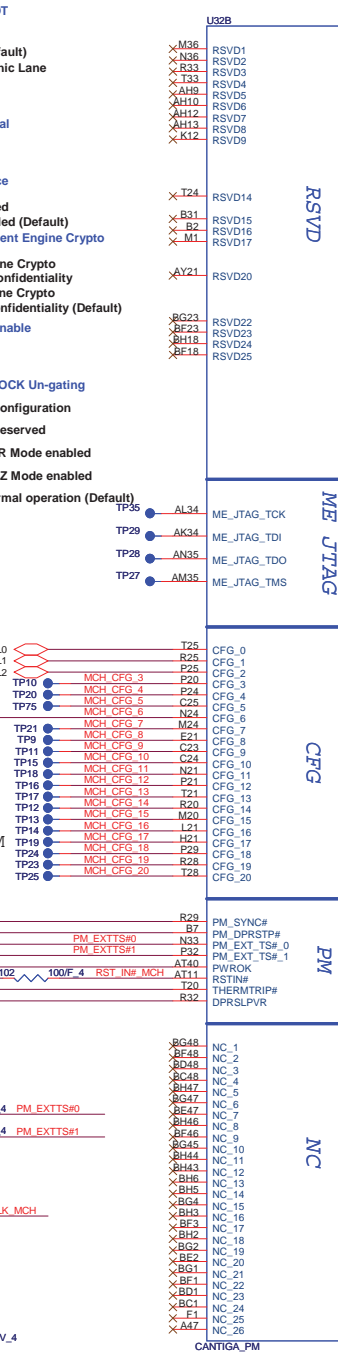
PM\_SYNC#
H\_DPRSTP#
PM\_EXTTSS#0
PM\_EXTTSS#1
PM\_EXTTSS#2
PM\_EXTTSS#3
PM\_EXTTSS#4
PM\_EXTTSS#5
PM\_EXTTSS#6
PM\_EXTTSS#7
PM\_EXTTSS#8
PM\_EXTTSS#9
PM\_EXTTSS#10
PM\_EXTTSS#11
PM\_EXTTSS#12
PM\_EXTTSS#13
PM\_EXTTSS#14
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PM\_EXTTSS#17
PM\_EXTTSS#18
PM\_EXTTSS#19
PM\_EXTTSS#20

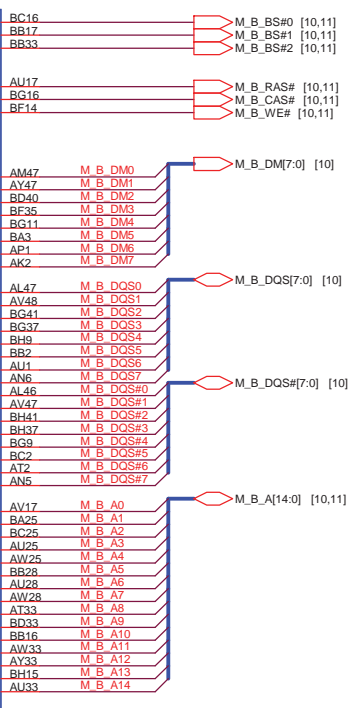
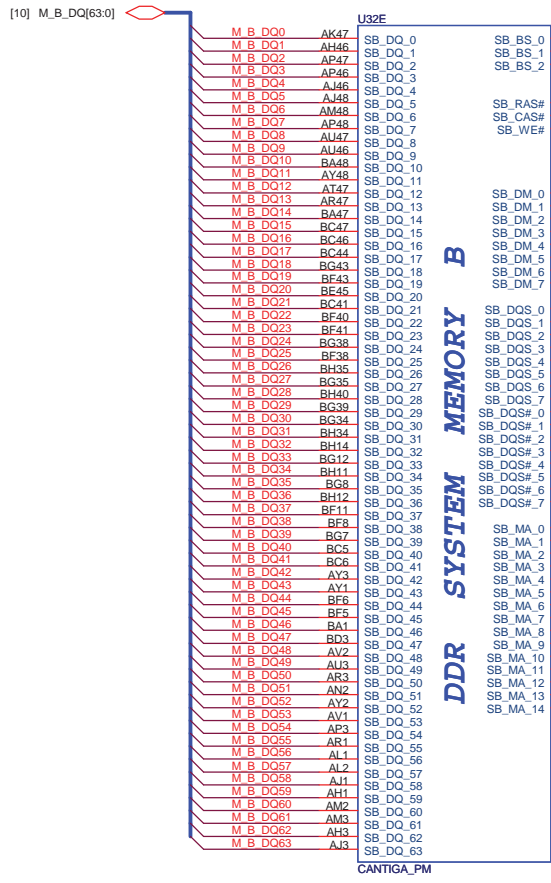
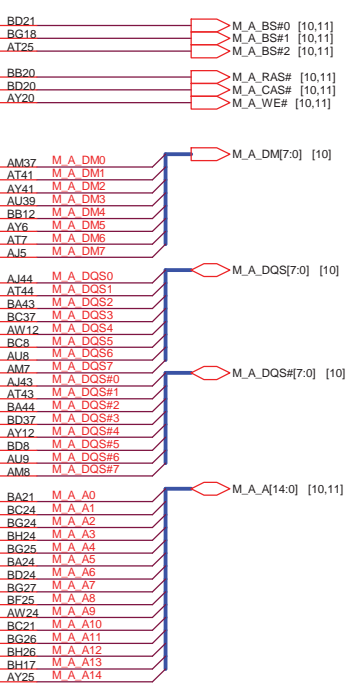
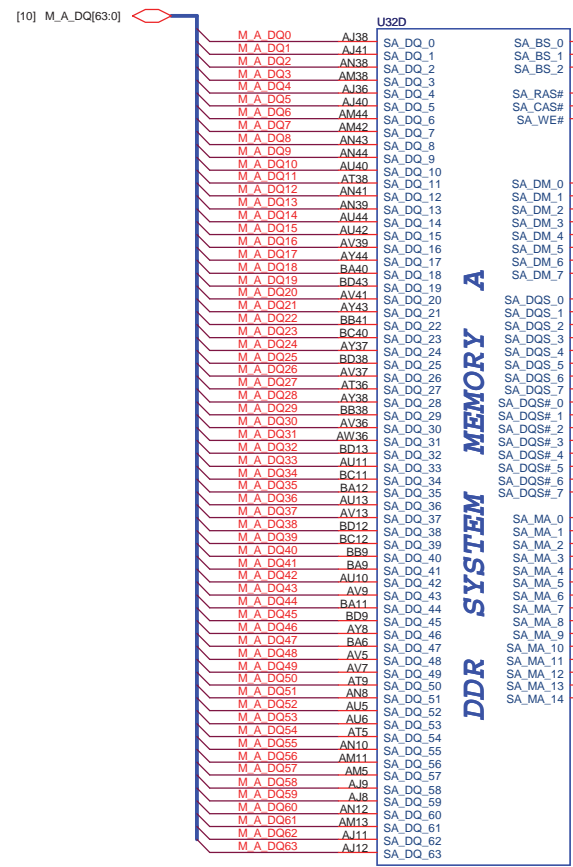
NC.1
NC.2
NC.3
NC.4
NC.5
NC.6
NC.7
NC.8
NC.9
NC.10
NC.11
NC.12
NC.13
NC.14
NC.15
NC.16
NC.17
NC.18
NC.19
NC.20
NC.21
NC.22
NC.23
NC.24
NC.25
NC.26

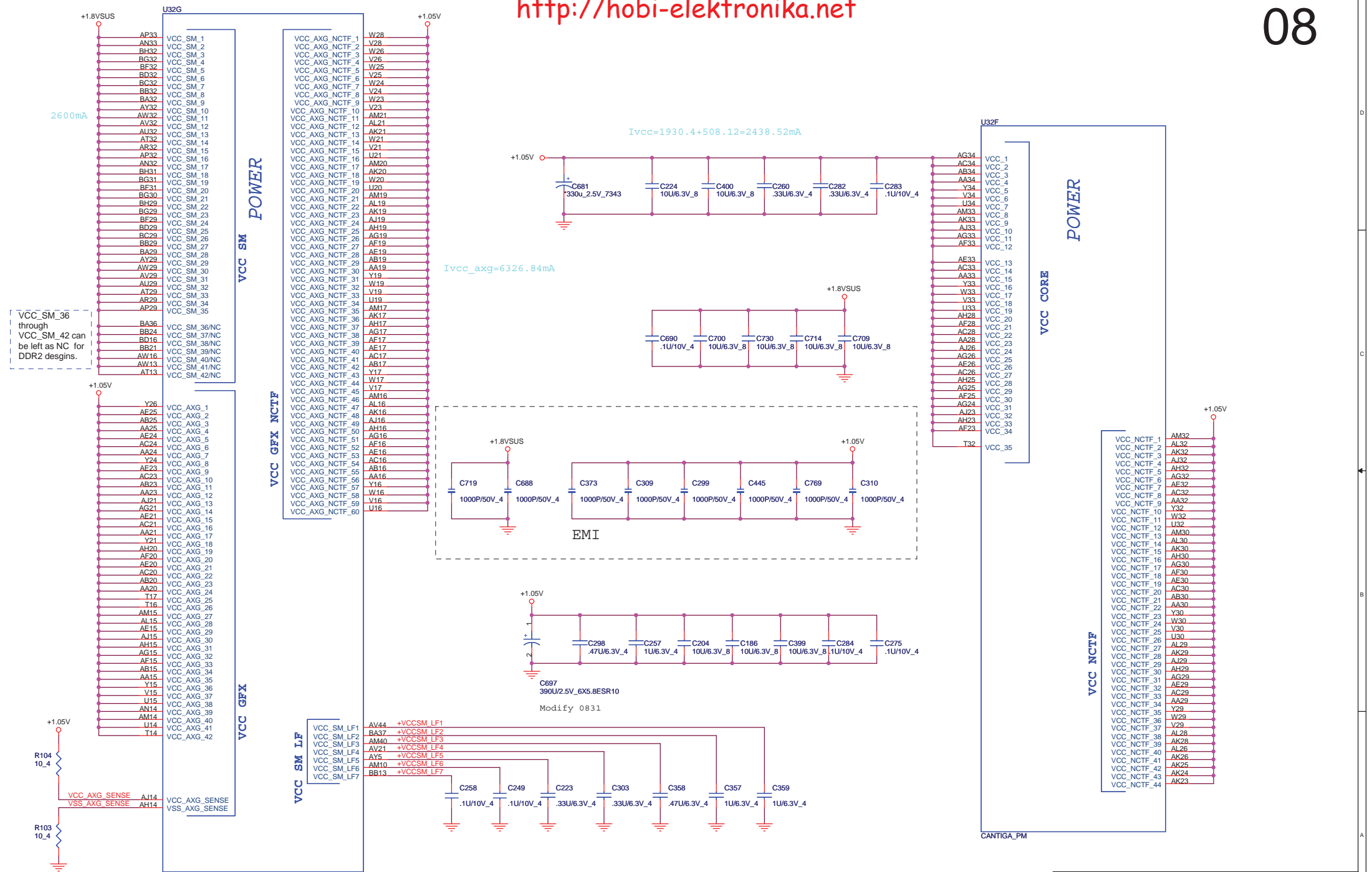
HDA\_BCLK
HDA\_RST#
HDA\_SDI
HDA\_SDO
HDA\_SYNC

CANTIGA\_PM
ACZ\_BITCLK\_MCH
ACZ\_RST#\_MCH
ACZ\_SDI#\_MCH
ACZ\_SDO#\_MCH
ACZ\_SYNC\_MCH

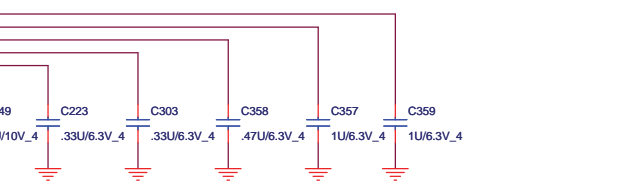
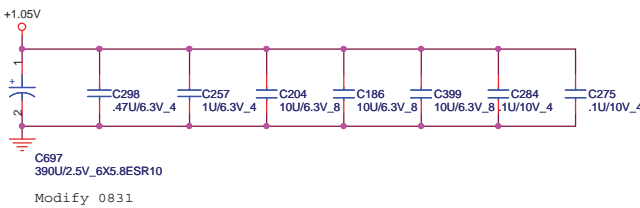
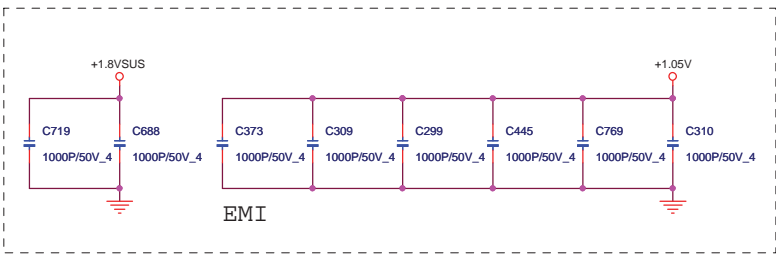
CANTIGA\_PM







VCC\_SM\_36 through VCC\_SM\_42 can be left as NC for DDR2 designs.



**PROJECT : QL5**  
Quanta Computer Inc.

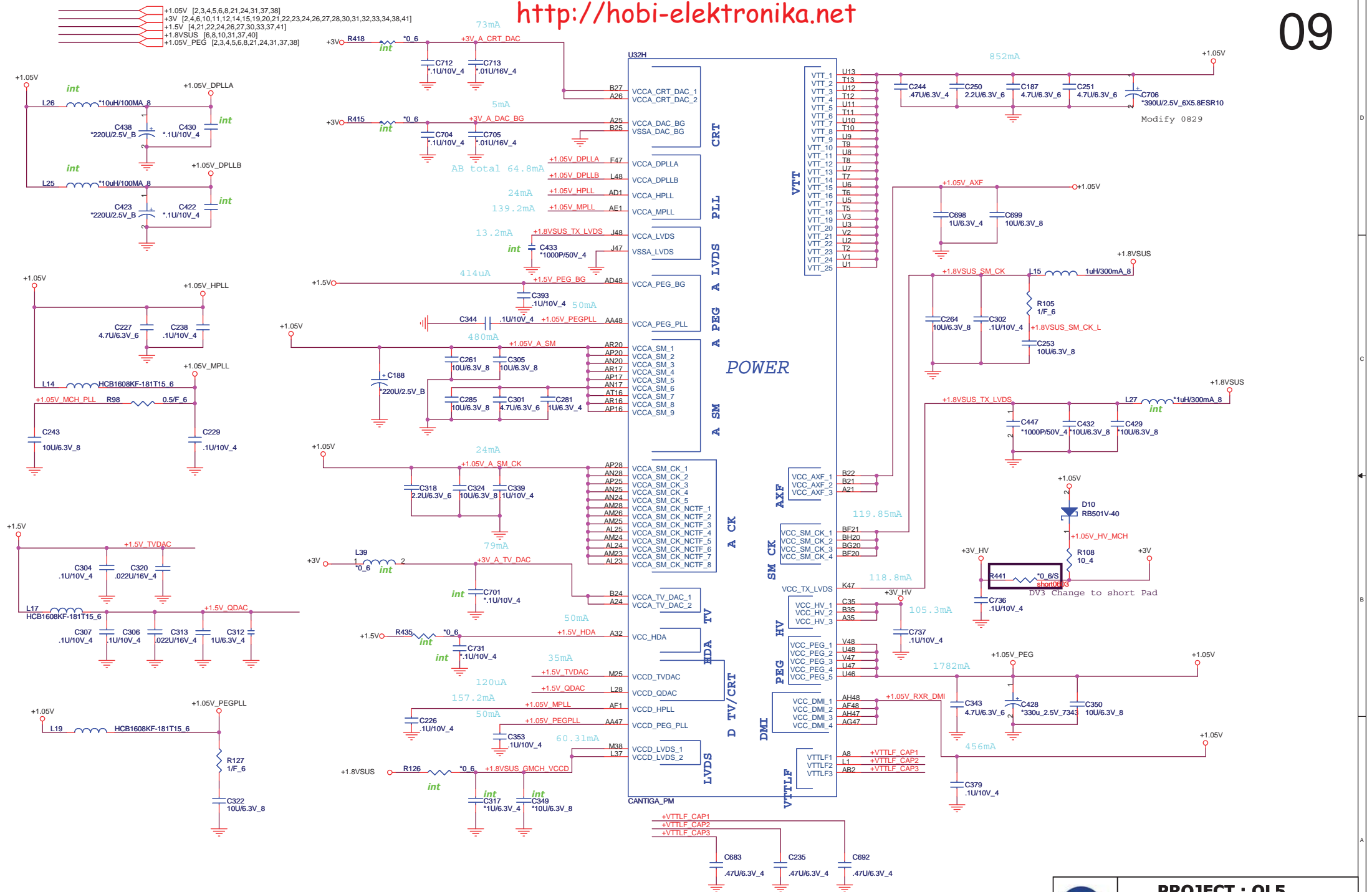
**NB5** Custom Document Number **Cantiga Vcc 4/5** Rev 1A

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[6,9,10,31,37,40] +1.8VSUS  
[2,3,4,5,6,9,21,24,31,37,38] +1.05V

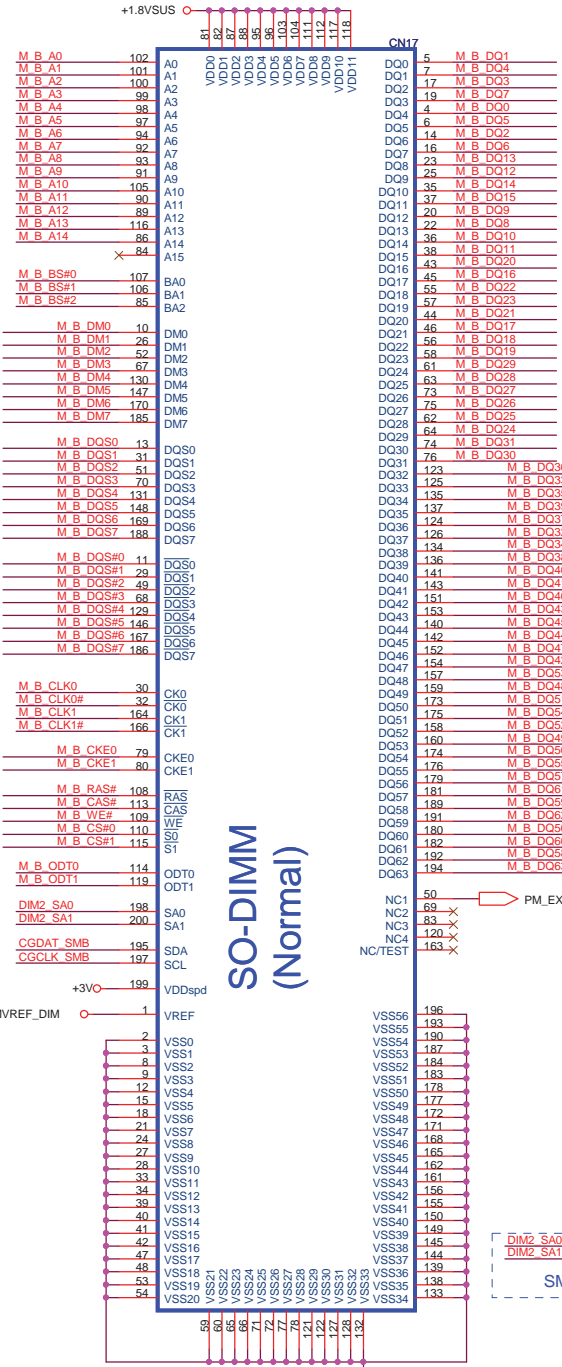






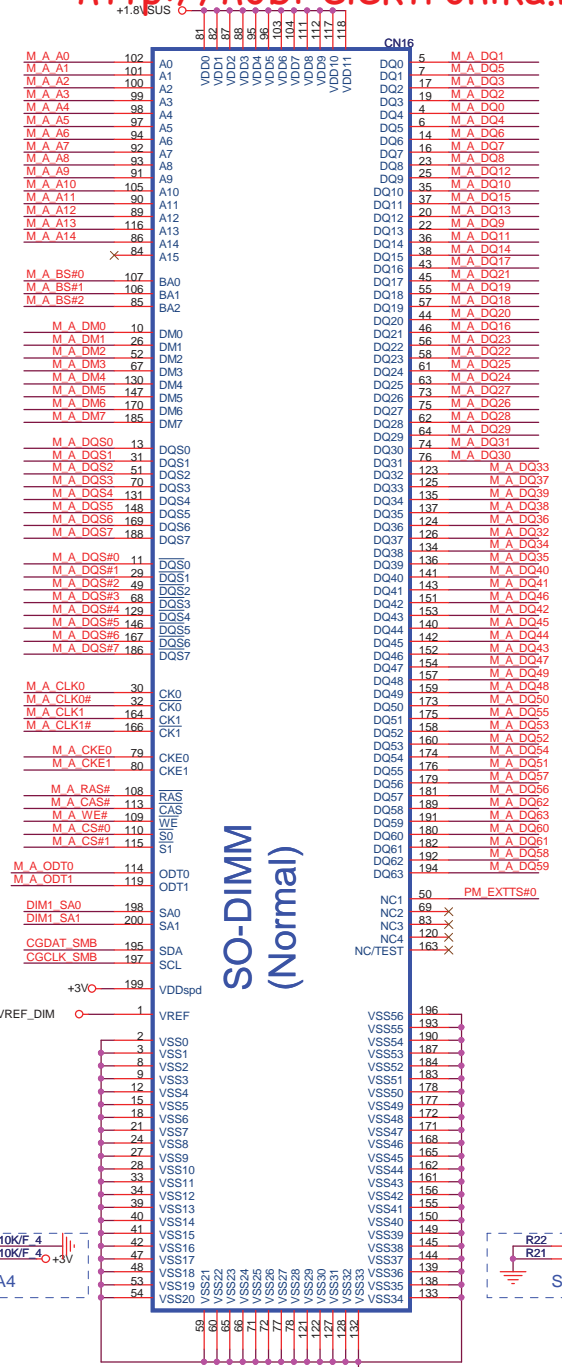
**PROJECT : QL5**  
Quanta Computer Inc.

Size Custom	Document Number <b>Cantiga Power 5/5</b>	Rev 1A
Date: Tuesday, March 17, 2009 Sheet 9 of 41		



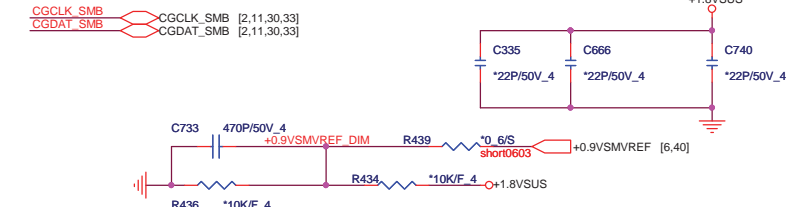
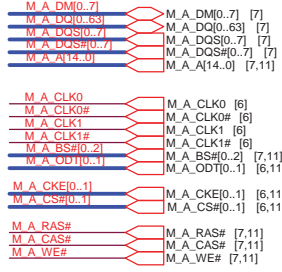
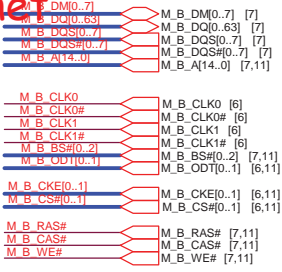
SO-DIMM (Normal)

H 9.2

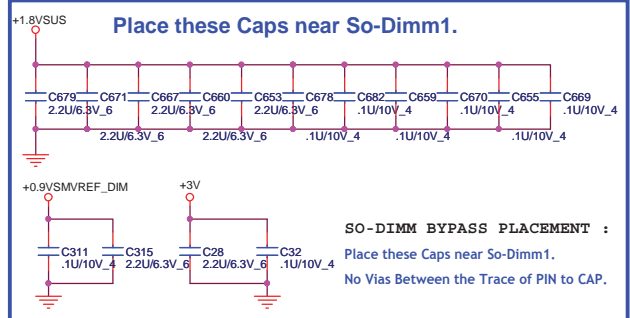


SO-DIMM (Normal)

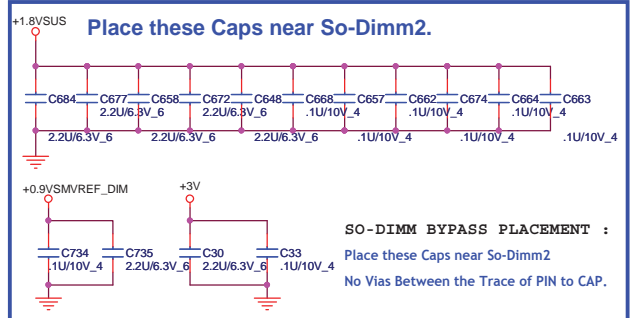
H 5.2



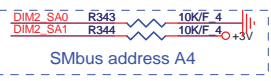
http://hobi-elektronika.net/



SO-DIMM BYPASS PLACEMENT : Place these Caps near So-Dimm1. No Vias Between the Trace of PIN to CAP.



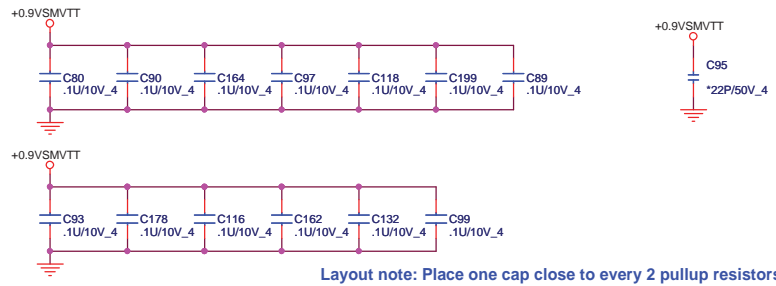
SO-DIMM BYPASS PLACEMENT : Place these Caps near So-Dimm2. No Vias Between the Trace of PIN to CAP.



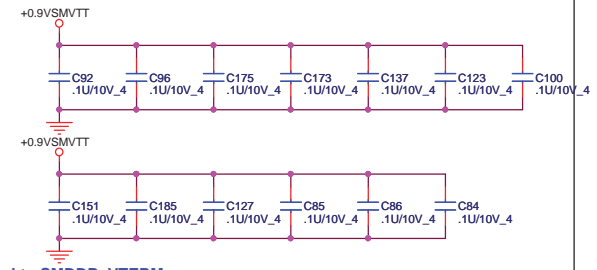
PROJECT : QL5 Quanta Computer Inc.

# DDRII DUAL CHANNEL A, B.

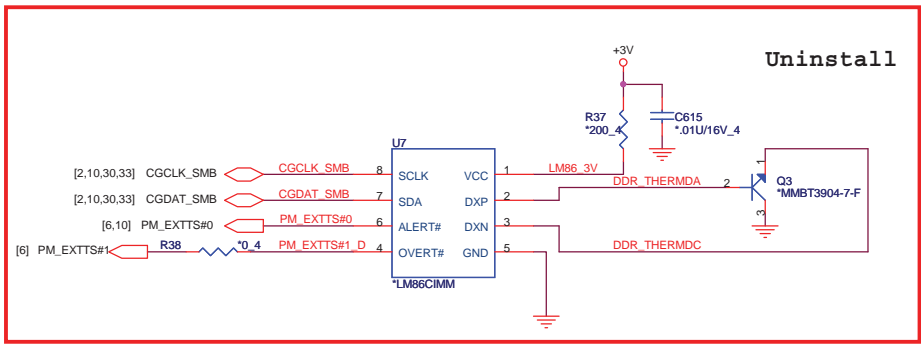
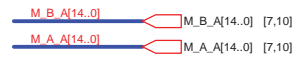
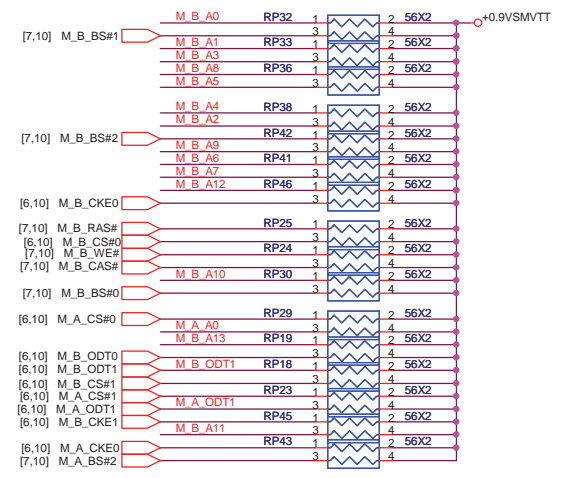
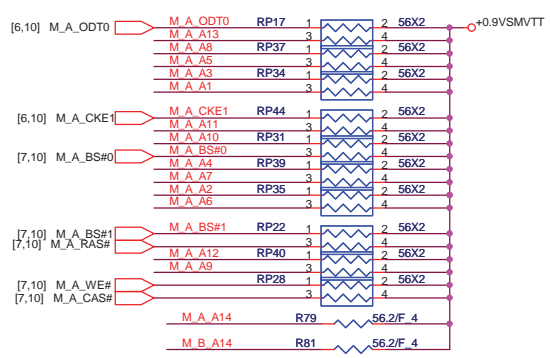
## DDRII A CHANNEL



## DDRII B CHANNEL

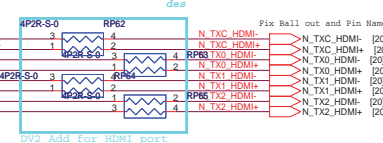
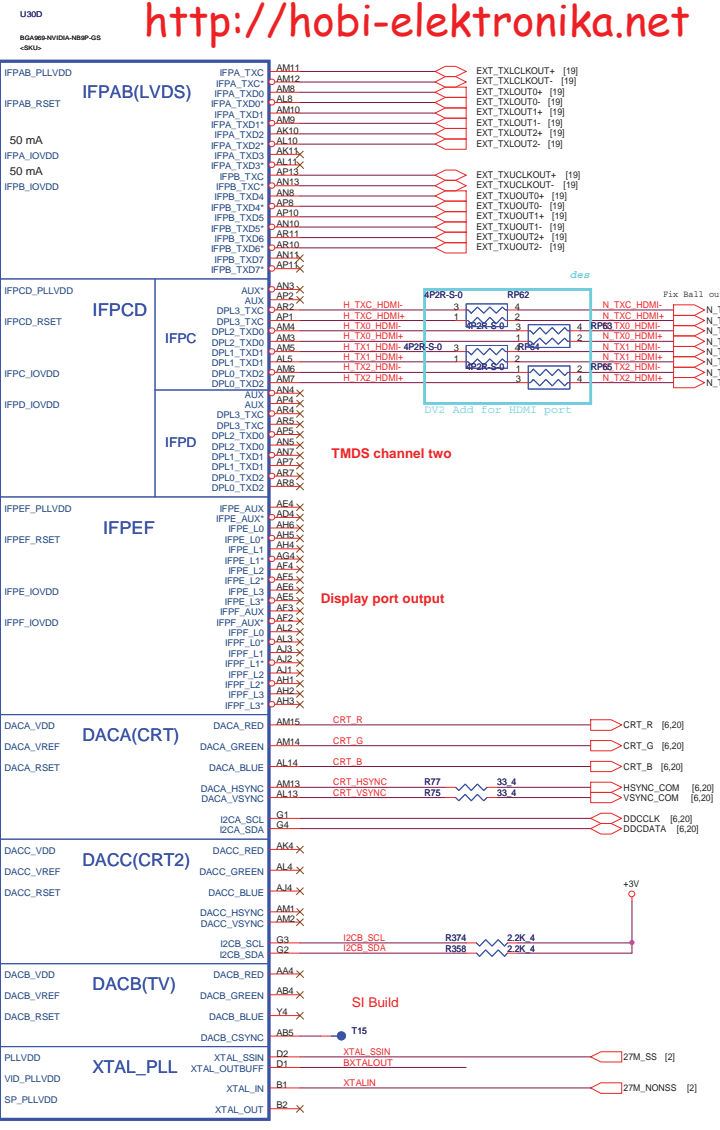
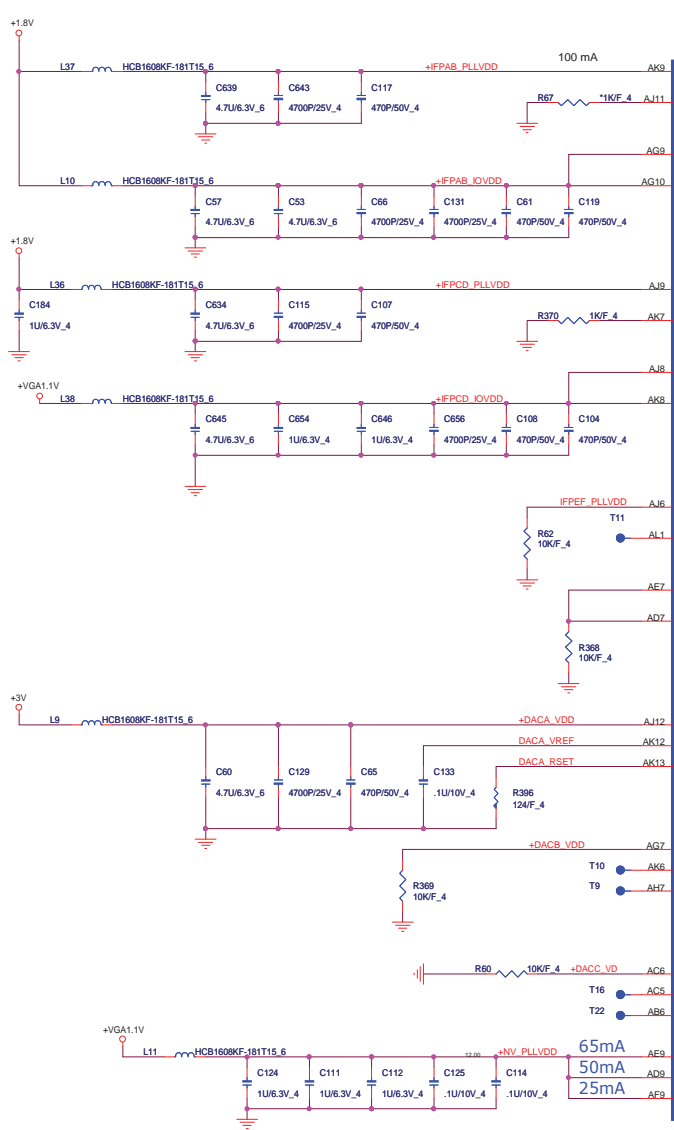


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR\_VTERM





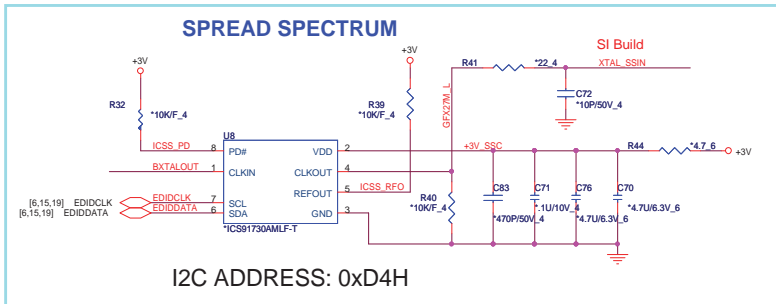
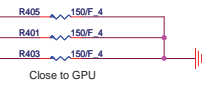




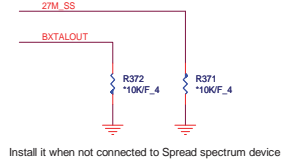
TMDs channel two

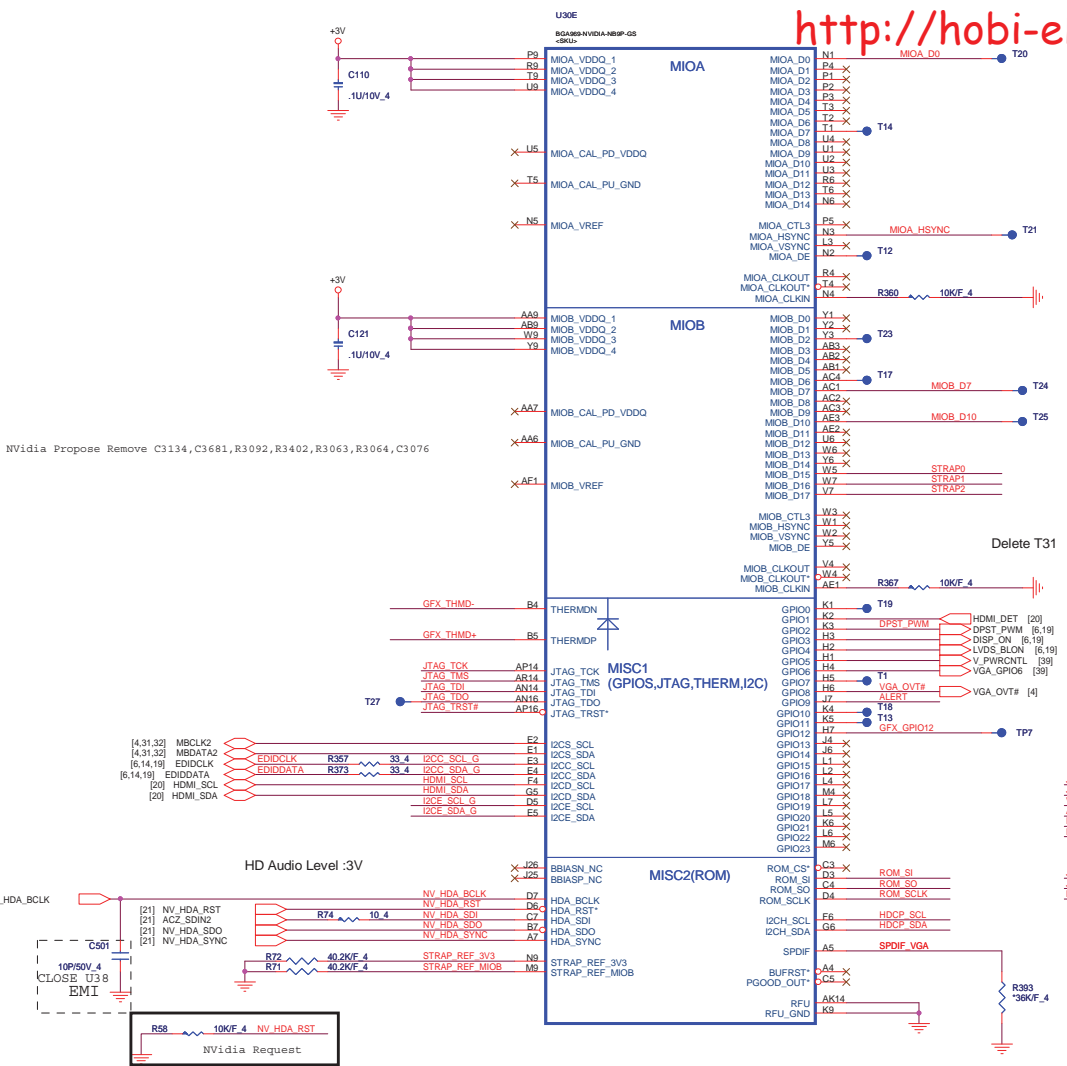
Display port output

SI Build



STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT\_SS IS NOT USED





### N10P-GE1 (G96) Straps N10M-GE1 (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	FB_VDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

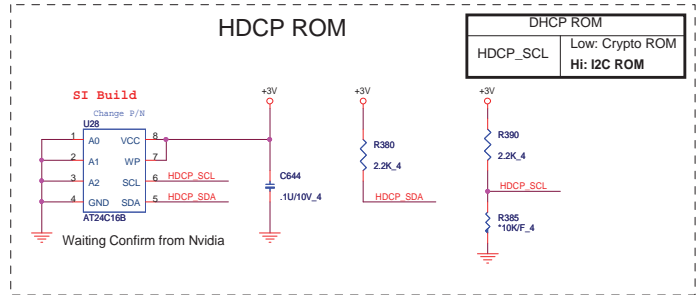
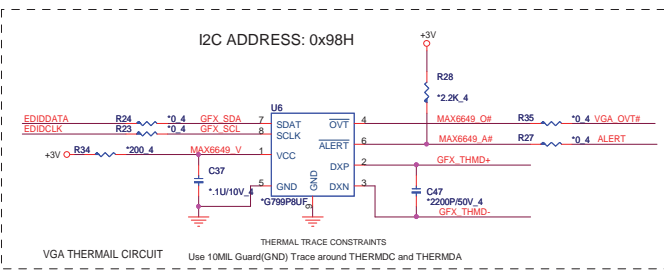
SEE Datasheet for details on G10x Straps!

PV	Hynix	Samsung	Qimonda
R381	CS25102FB02 5K	CS31002FB26 10K	CS31502FB24 15K
		N10M-GE1	N10P-GE1
		R361 25K	R362 15K
		R384 15K	R383 15K

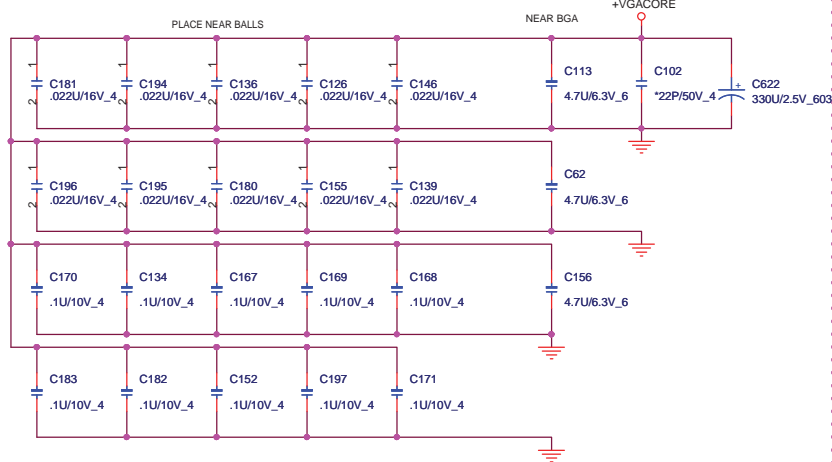
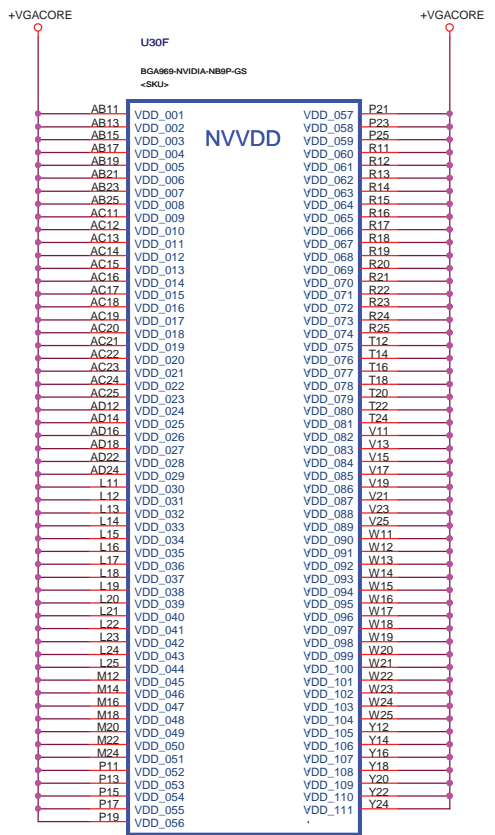
#### Logical Strap Bit Mapping

PU-VDD		PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

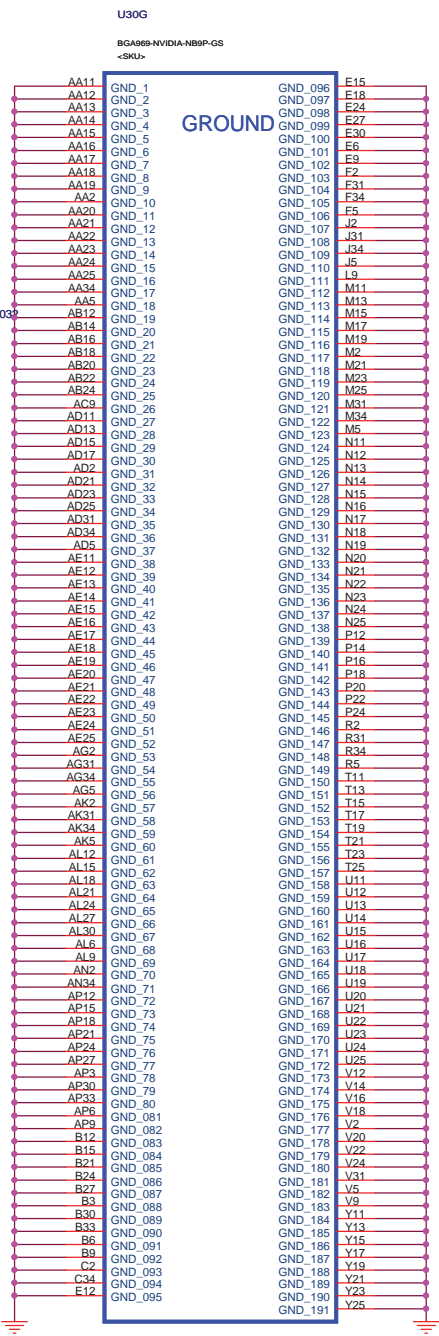
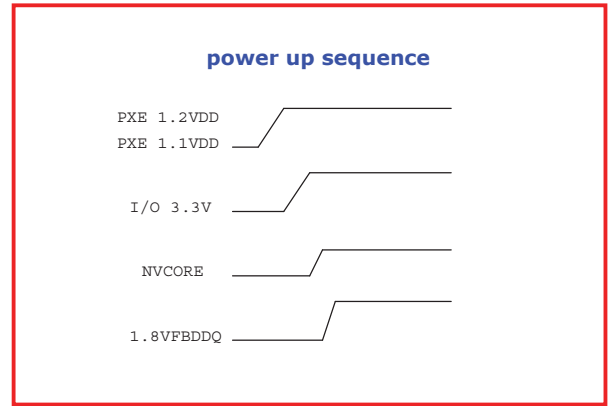
N10M-GE1			N10P-GE1		
RAM_CFG[3:0]	Config	Definitions	RAM_CFG[3:0]	Config	Definitions
64Mx16	DDR2	Hynix	0000	64Mx16	DDR2
64Mx16	DDR2	Samsung	0001	64Mx16	DDR2
64Mx16	DDR2	Qimonda	0010	64Mx16	DDR2



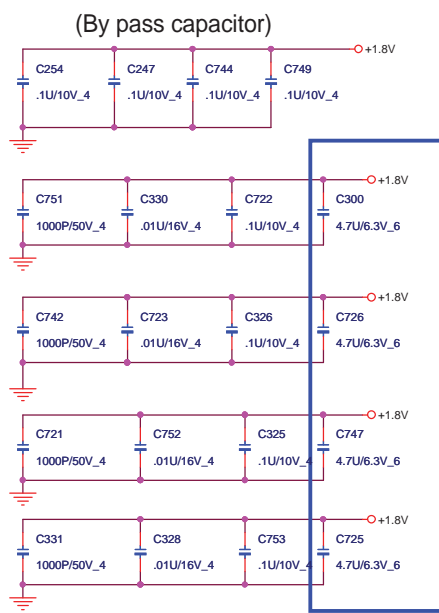
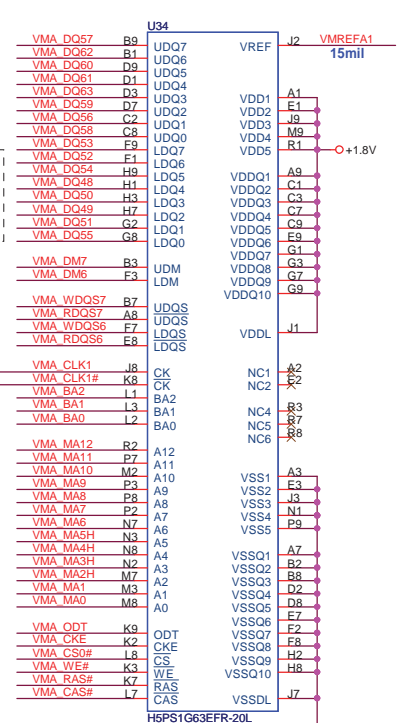
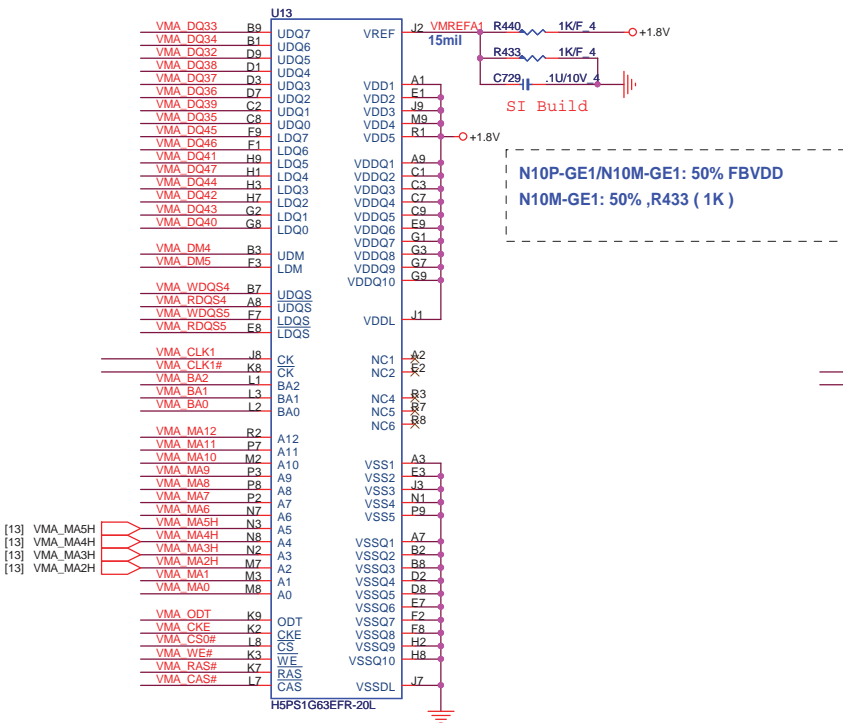
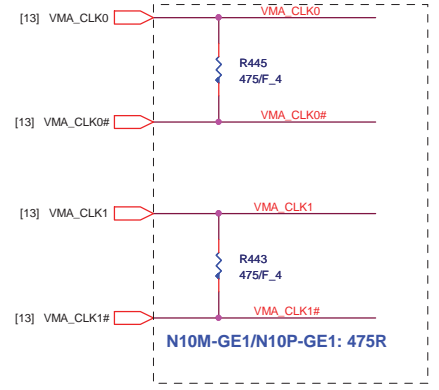
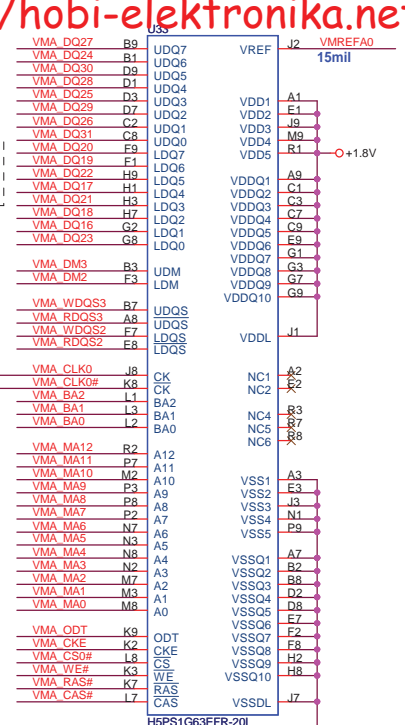
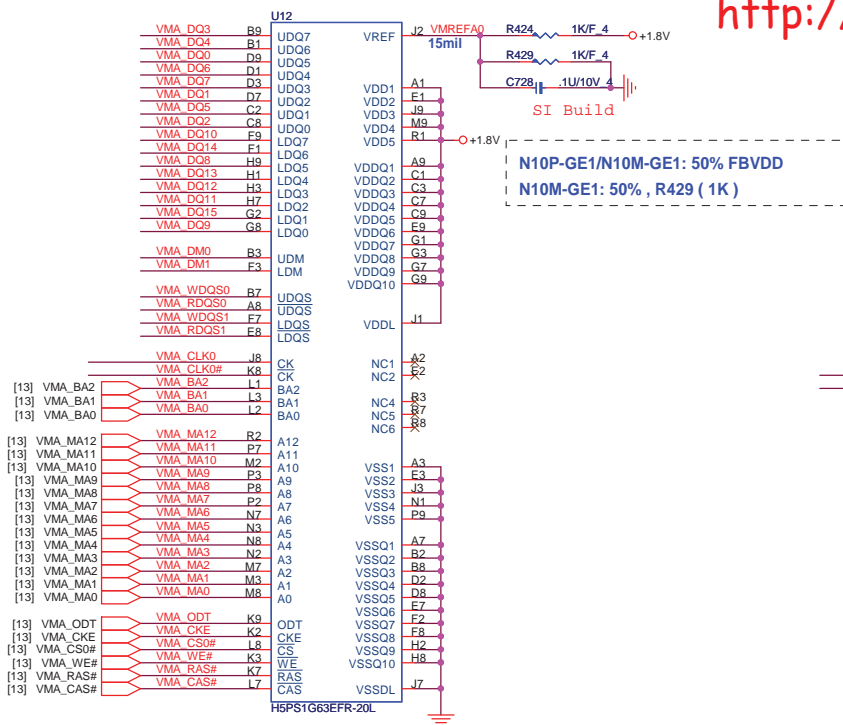
# NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uF x3 and 0.22x10 uF instead of 0.1uF x10





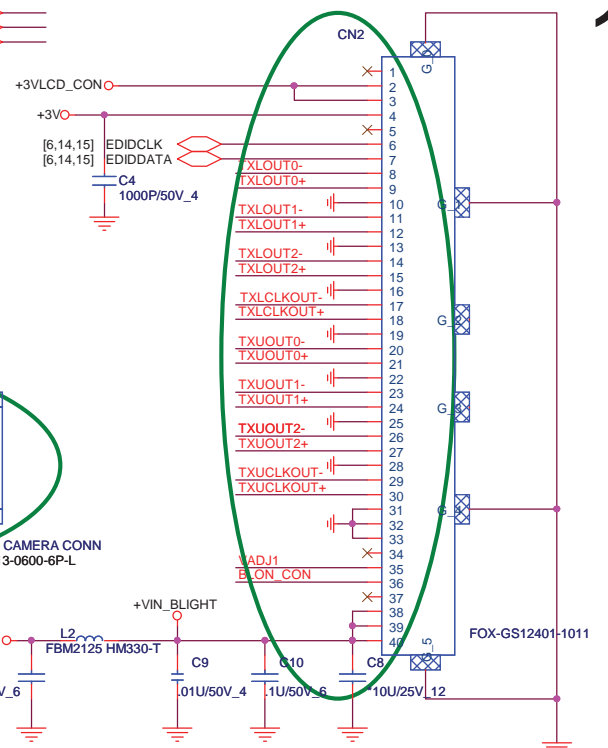
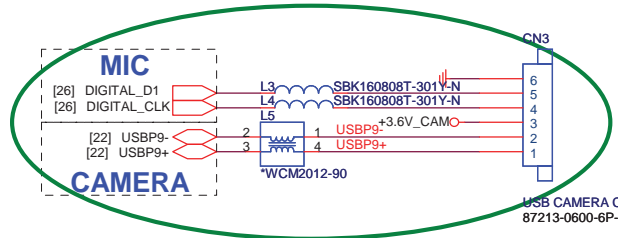
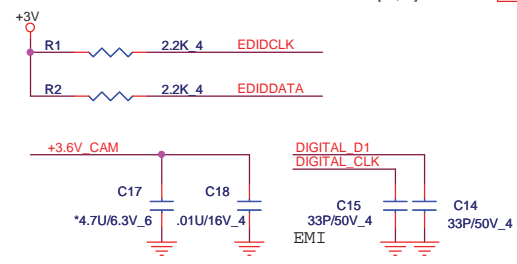
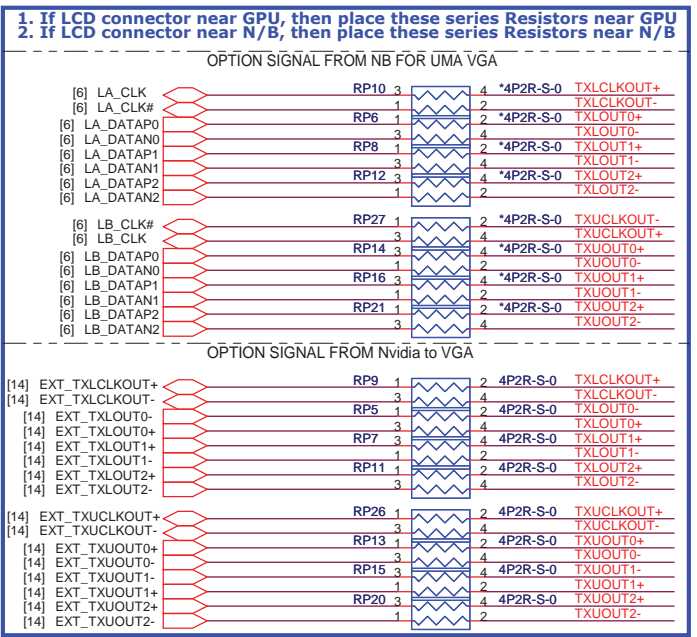


**PROJECT : QL5**  
**Quanta Computer Inc.**

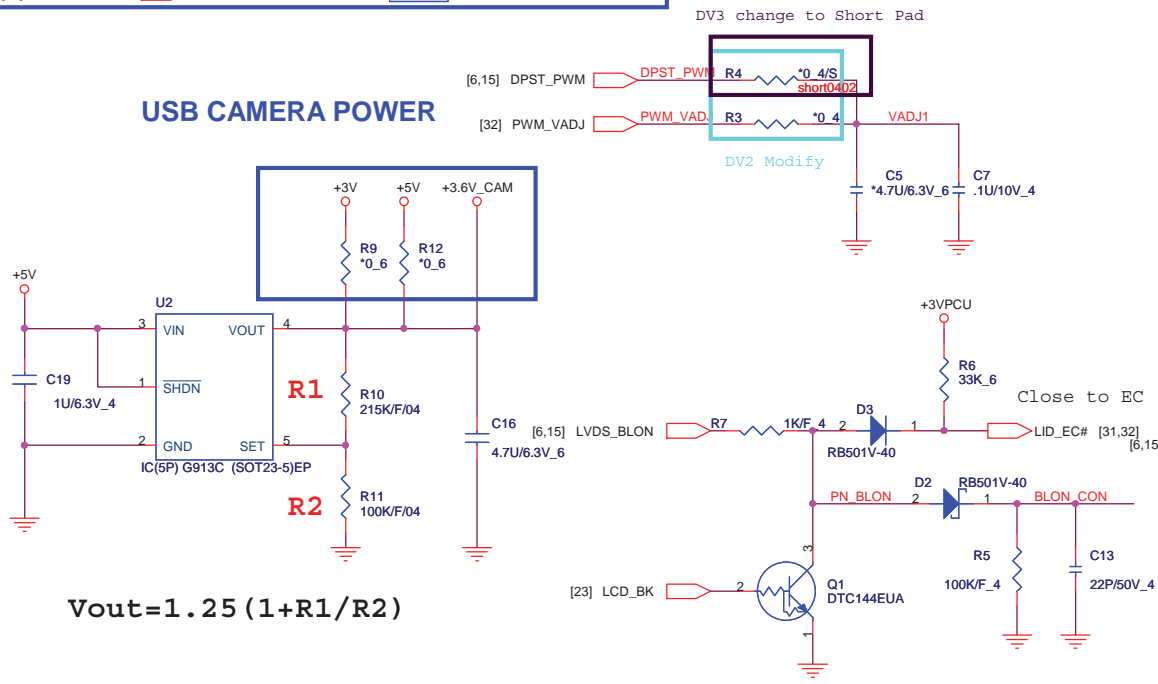
NB5

Size Custom	Document Number <b>NV10X VRAM-1(GDDR2 BGA84)</b>	Rev 1A
Date: Tuesday, March 17, 2009	Sheet 17 of 41	

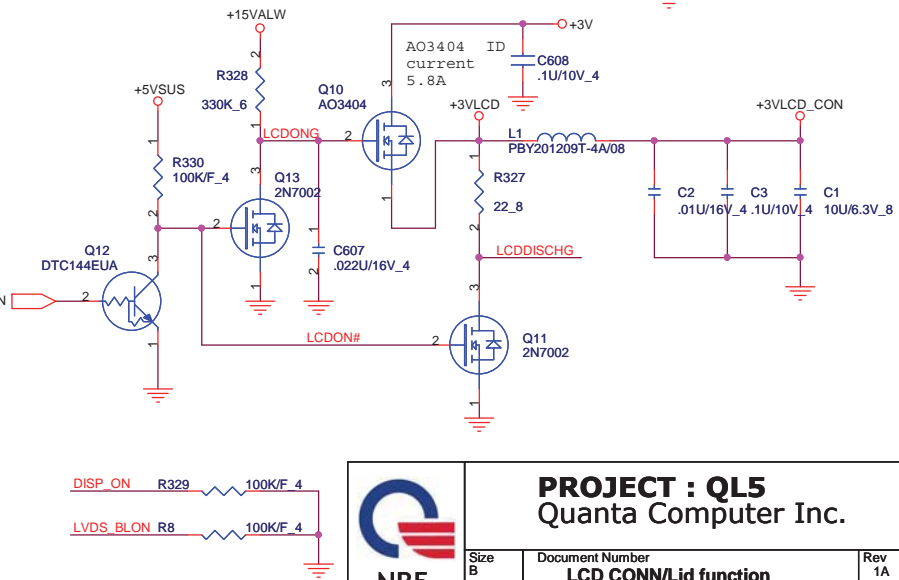




**USB CAMERA POWER**



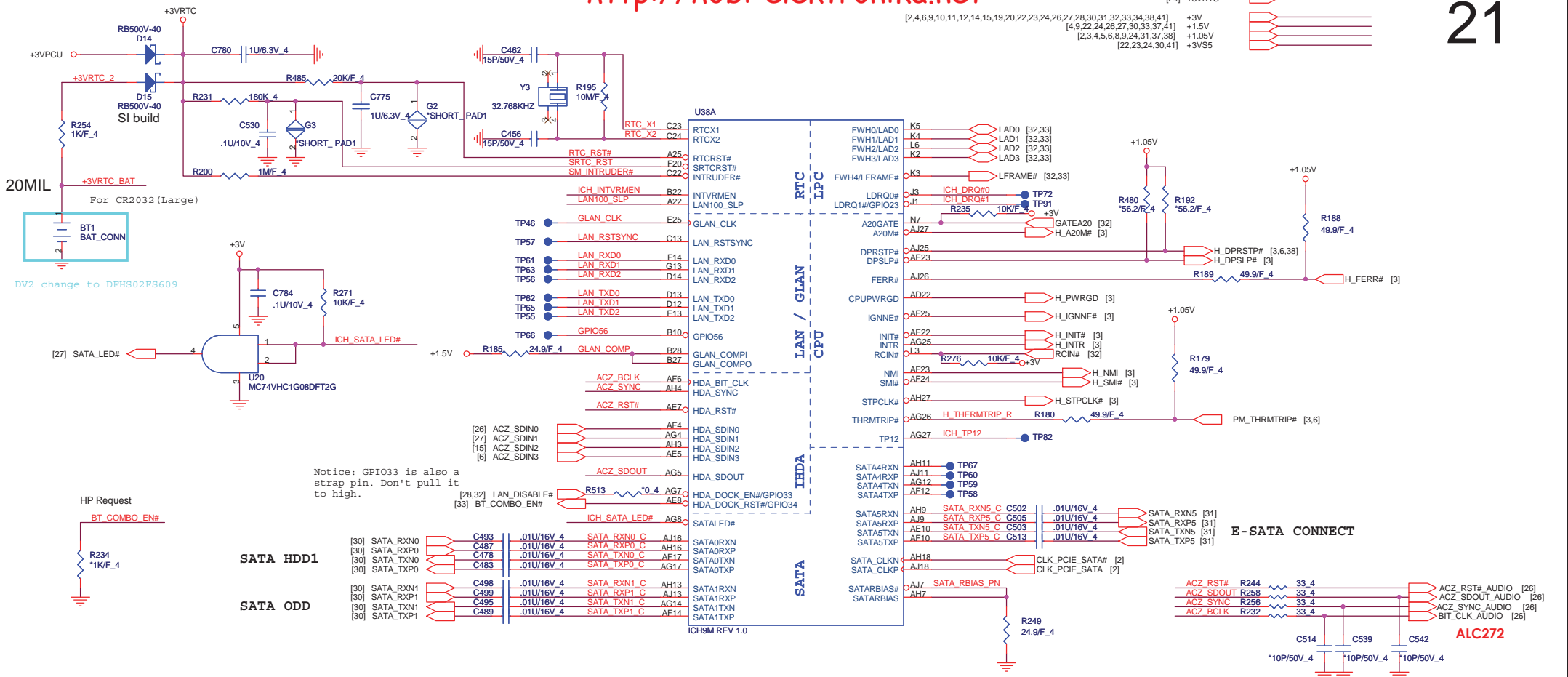
$V_{out} = 1.25 (1 + R1/R2)$



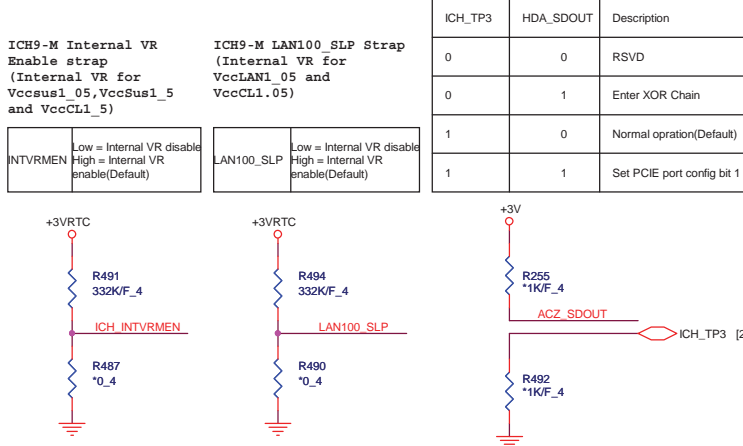
**PROJECT : QL5**  
Quanta Computer Inc.

Size B	Document Number <b>LCD CONN/Lid function</b>	Rev 1A
Date: Tuesday, March 17, 2009 Sheet 19 of 41		





**SB Strap**



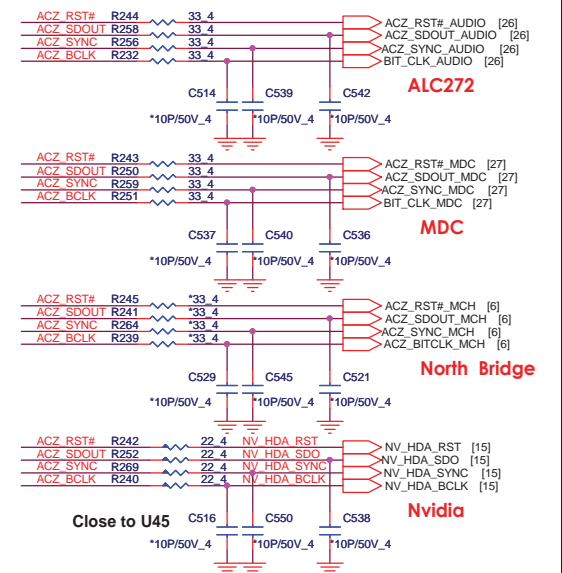
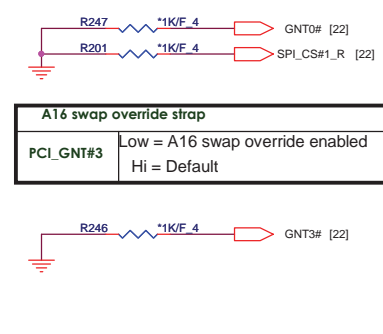
**XOR Chain Entrance Strap**

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

**ICH9 Boot BIOS select**

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

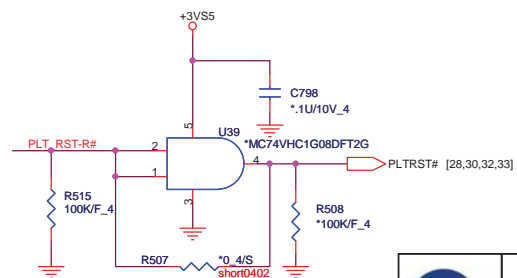
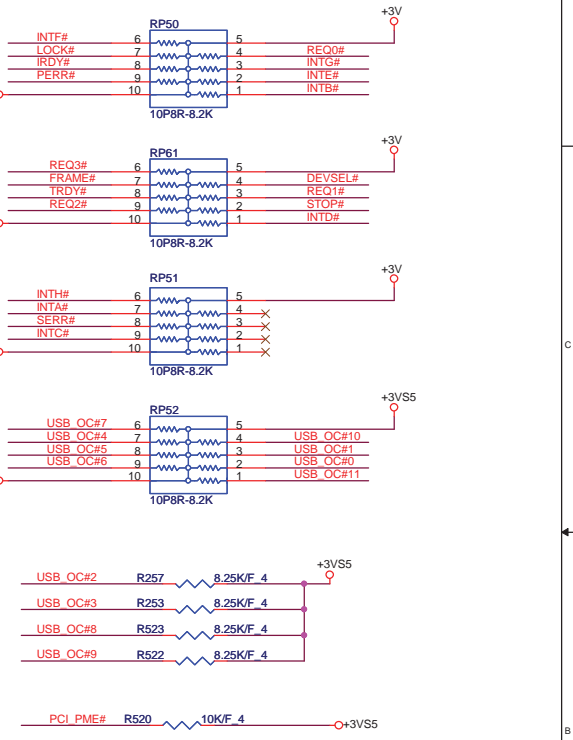
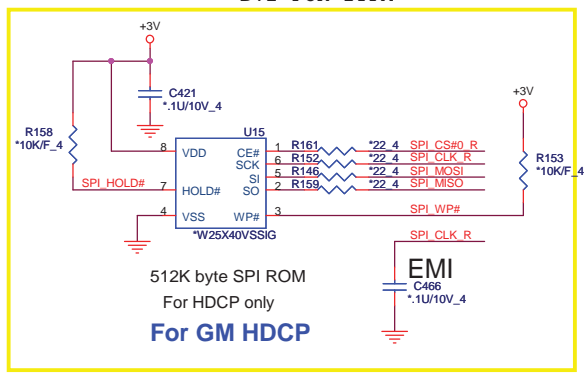
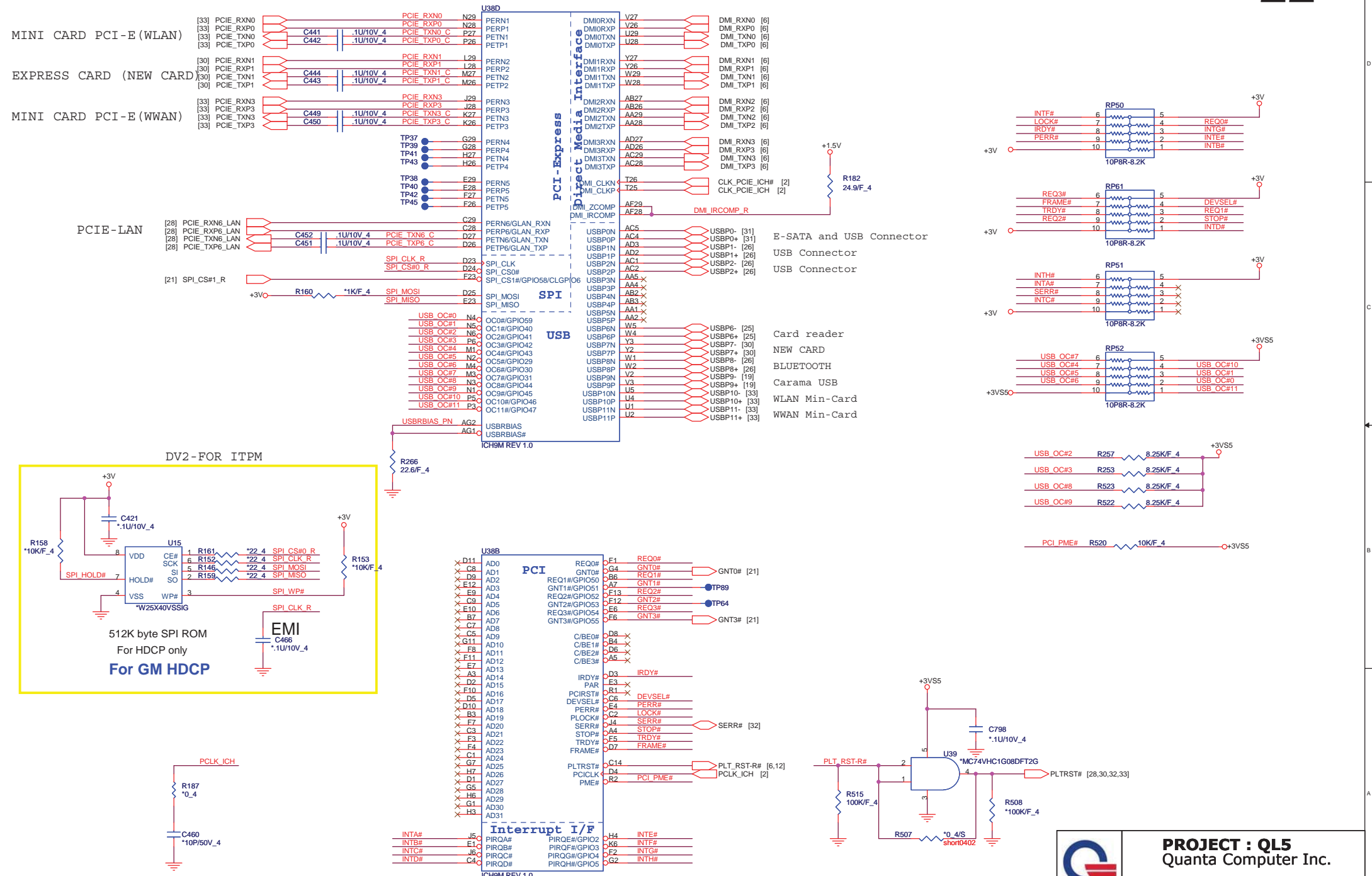


**PROJECT : QL5**  
Quanta Computer Inc.

**NB5**

Size Custom Document Number ICH9-M Host 1/4 Rev 1A

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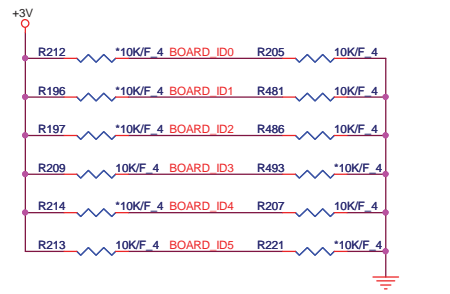
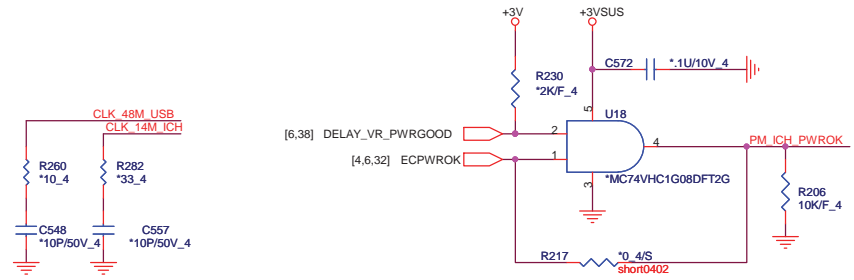
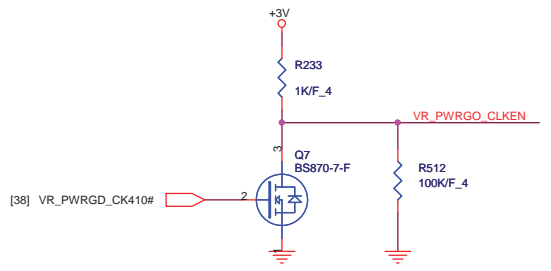
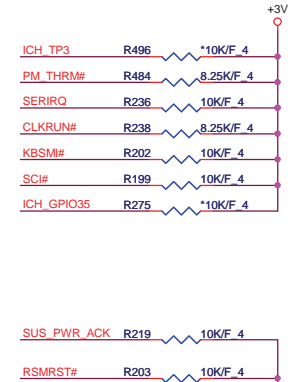
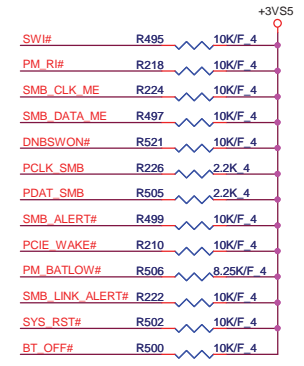
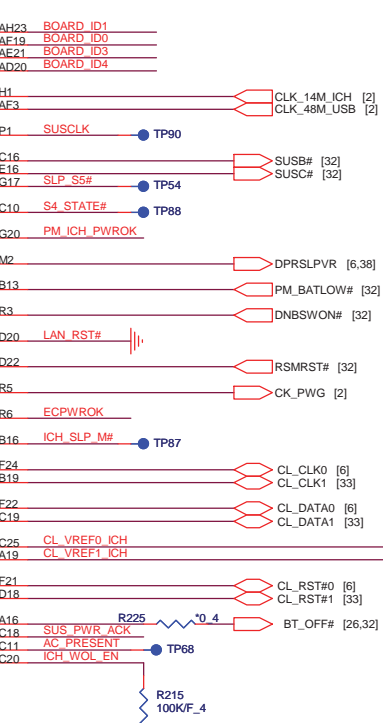
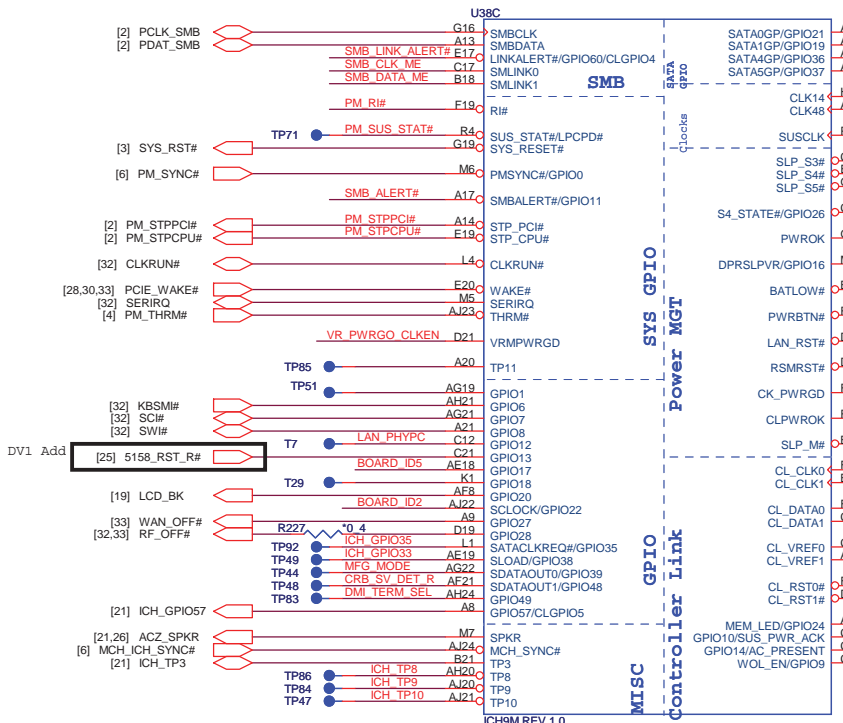
**PROJECT : QL5**  
Quanta Computer Inc.

NB5

Size Custom Document Number ICH9-M PCIE 2/4 Rev 1A

Date: Tuesday, March 17, 2009 Sheet 22 of 41

[4,9,21,22,24,26,27,30,33,37,41] +1.5V  
 [2,4,6,9,10,11,12,14,15,19,20,21,22,24,26,27,28,30,31,32,33,34,38,41] +3V  
 [21,22,24,30,41] +3VS5  
 [25,26,33,37,39,41] +3VSUS

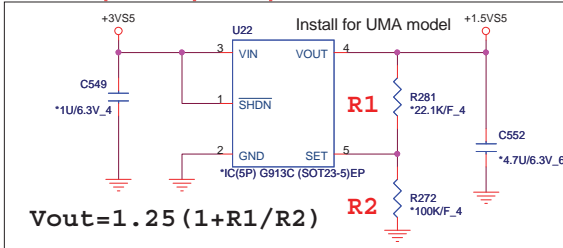
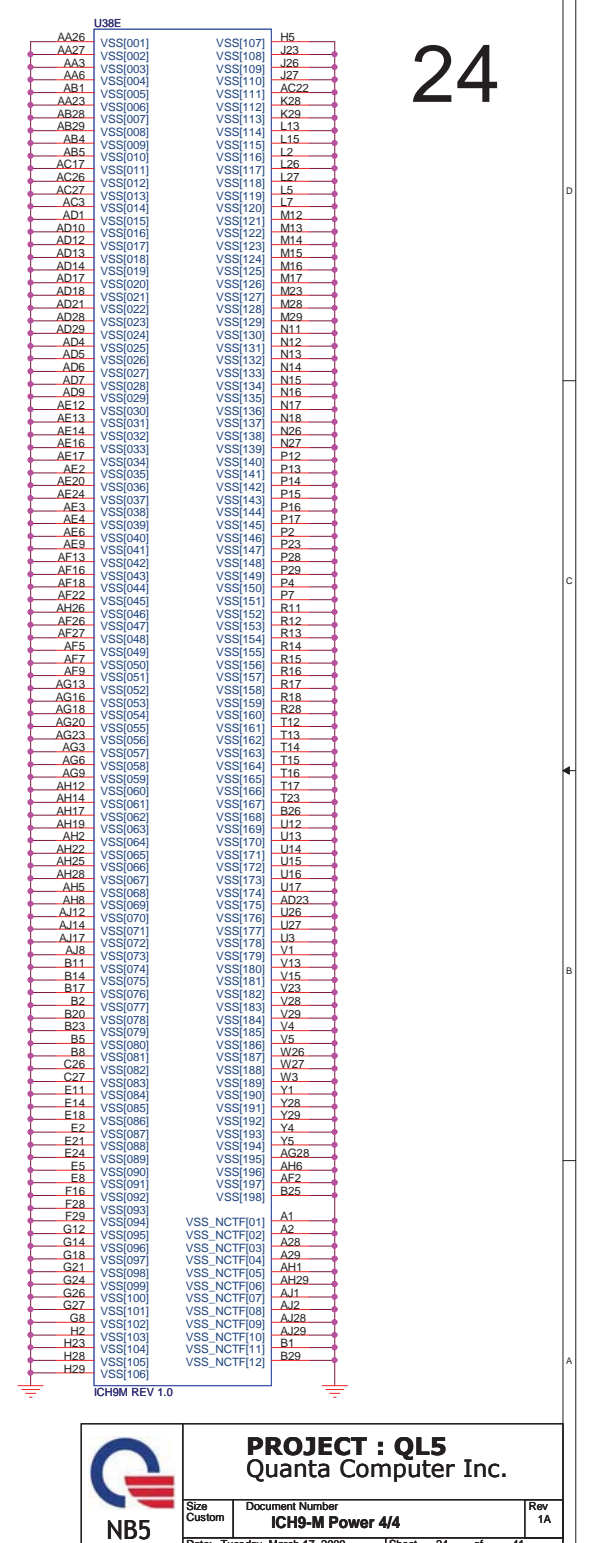
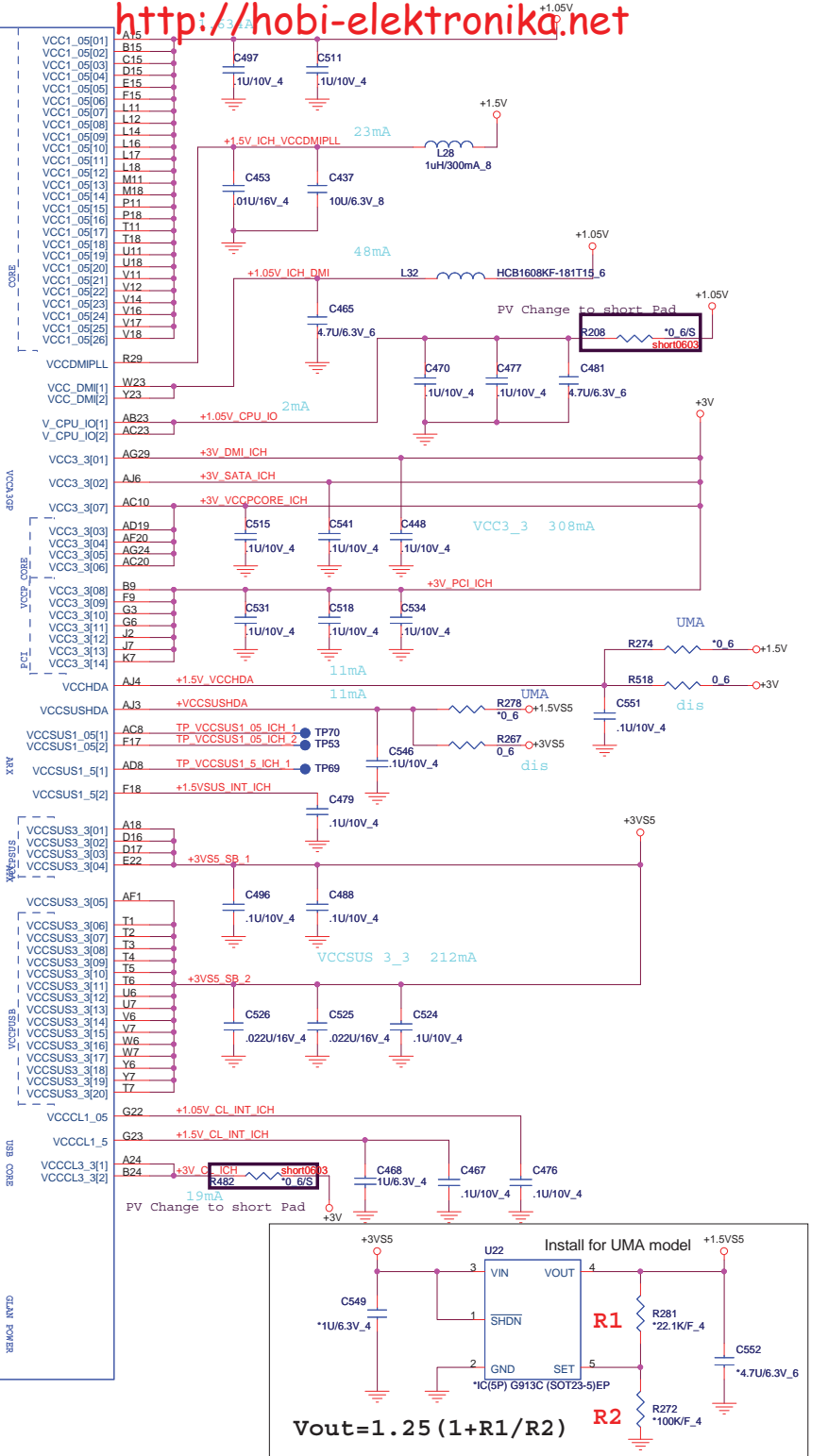
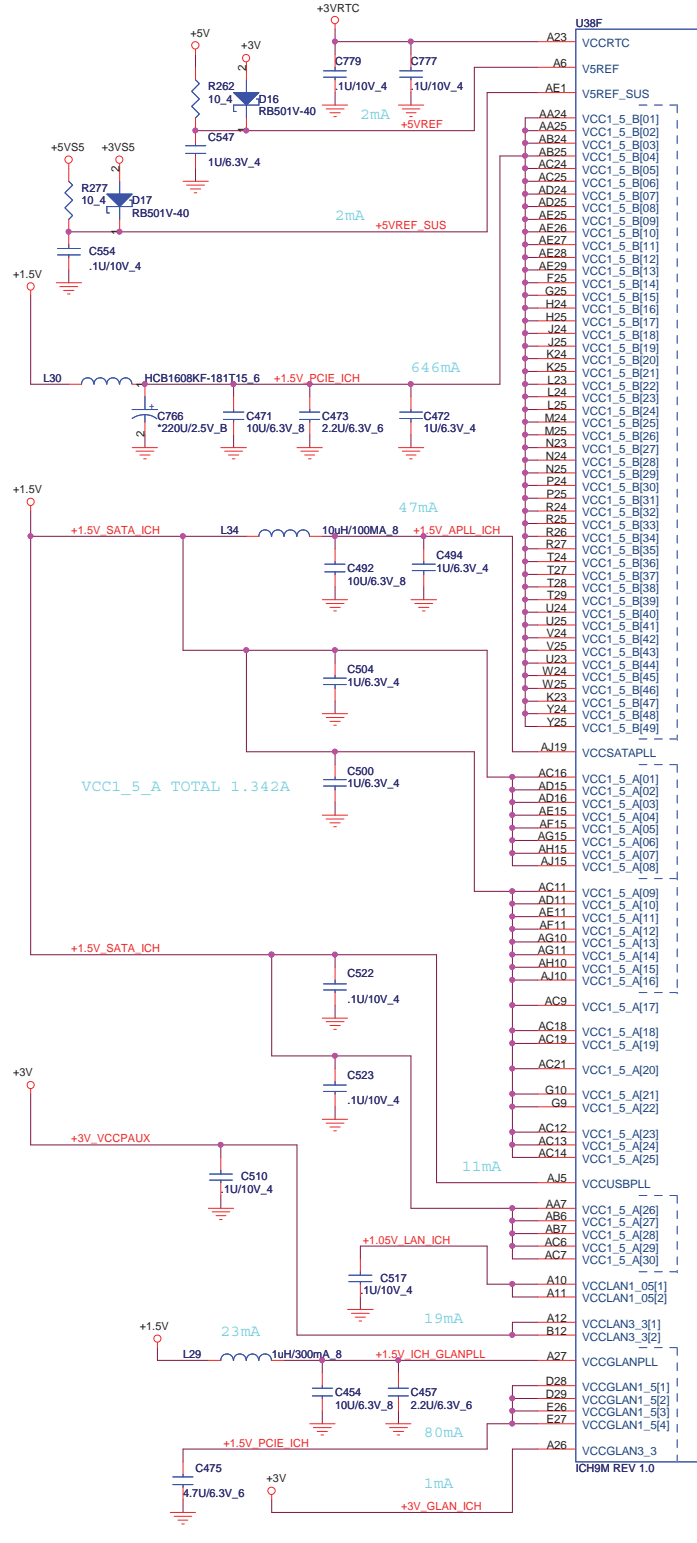


System Board ID  
 PV change system board ID set

		ID 5	ID 4	ID 3	ID 2	ID 1	ID 0
QL5	GL40	1	0	1	0	0	0
QL5	GM45	1	0	1	0	0	0
QL5	N10M	1	0	1	1	0	0
QL5	N10P	1	0	1	0	0	0

**PROJECT : QL5**  
 Quanta Computer Inc.

Size Custom Document Number ICH9-M GPIO 3/4 Rev 1A  
 Date: Tuesday, March 17, 2009 Sheet 23 of 41



**PROJECT : QL5**  
Quanta Computer Inc.

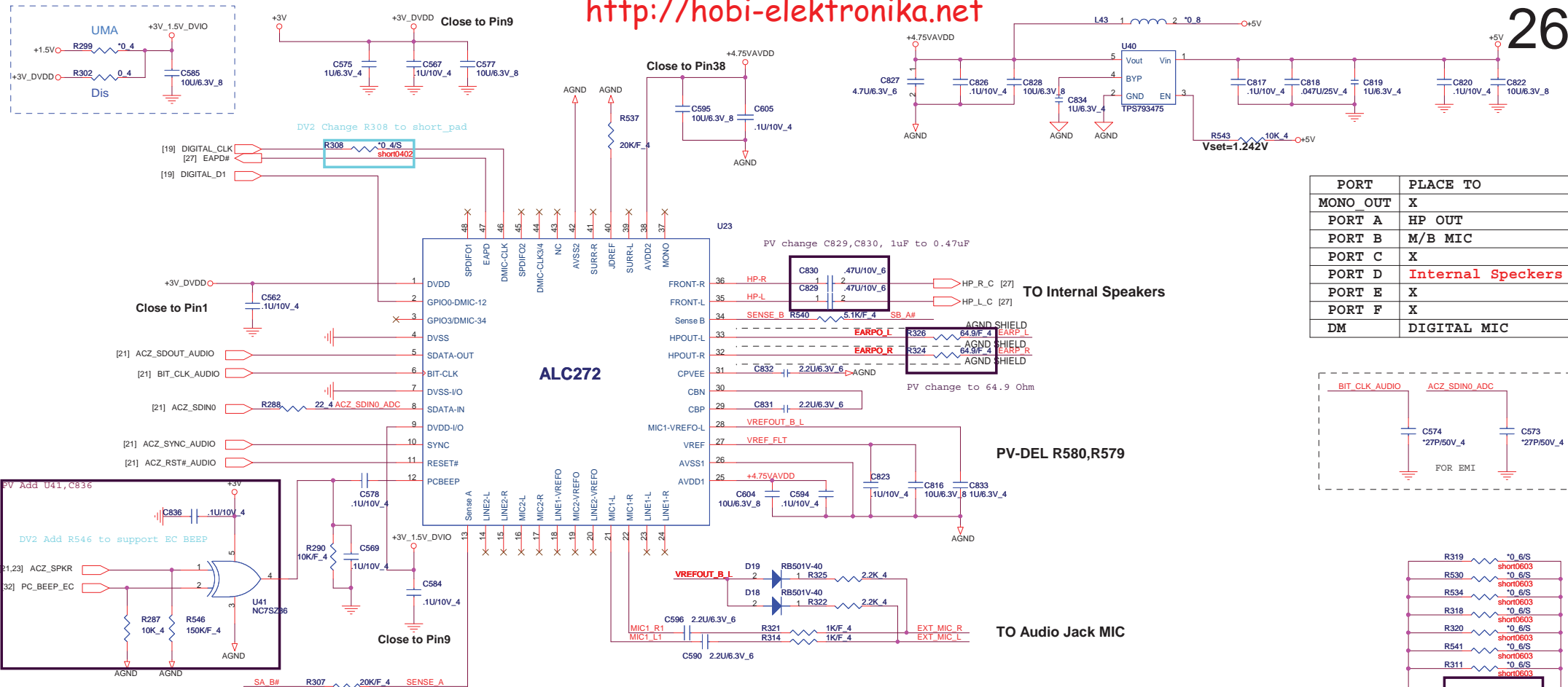
**NB5**

Size Custom Document Number ICH9-M Power 4/4 Rev 1A

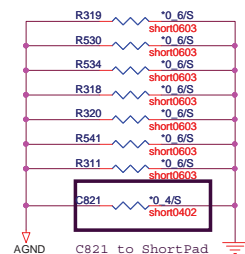
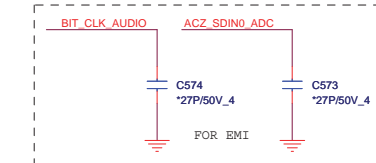
Date: Tuesday, March 17, 2009 Sheet 24 of 41



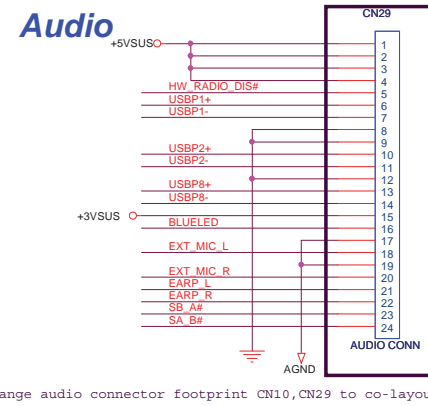
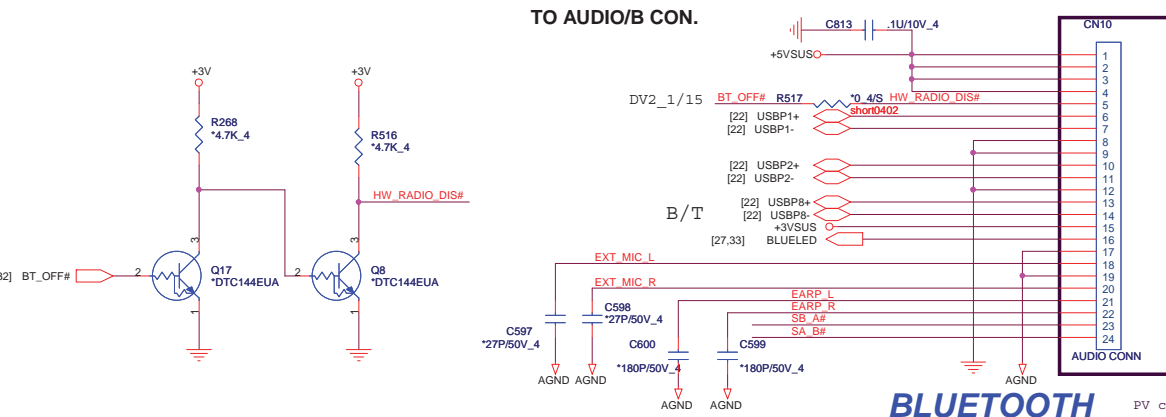




PORT	PLACE TO
MONO OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speakers
PORT E	X
PORT F	X
DM	DIGITAL MIC

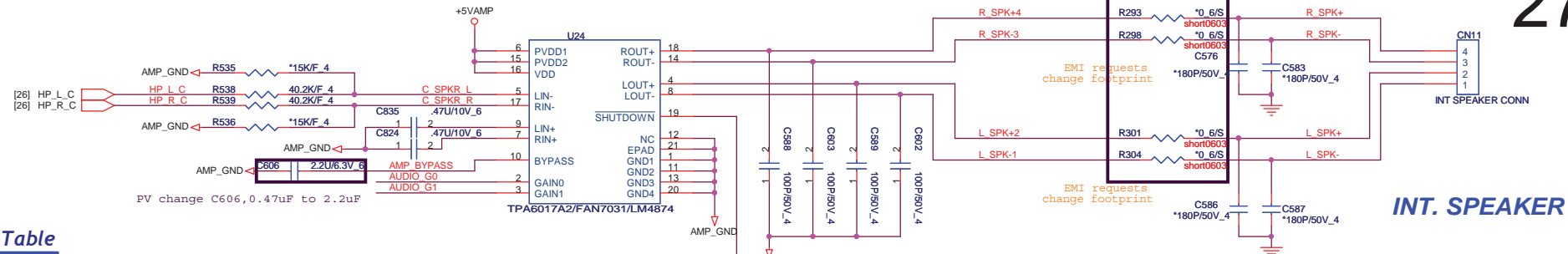


TO AUDIO/B CON.



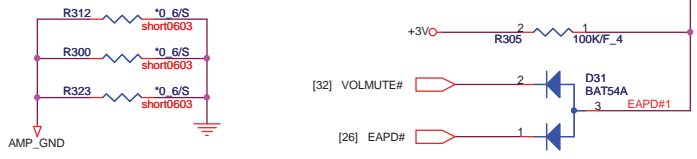
SB\_A# -->EXT HP  
 SA\_B# -->EXT MIC  
 Audio JACK: Normal Open

# AUDIO AMPLIFIER



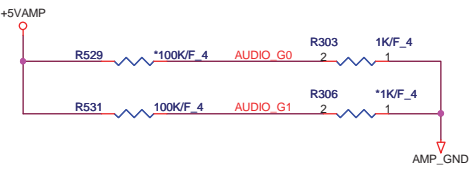
## 6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

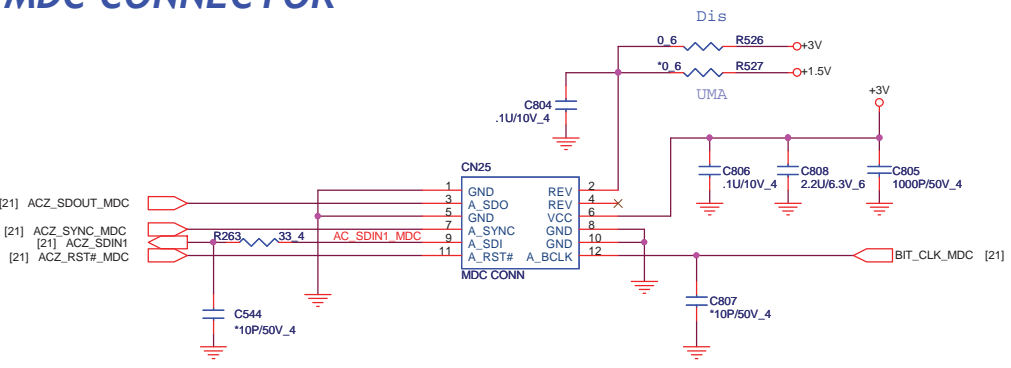


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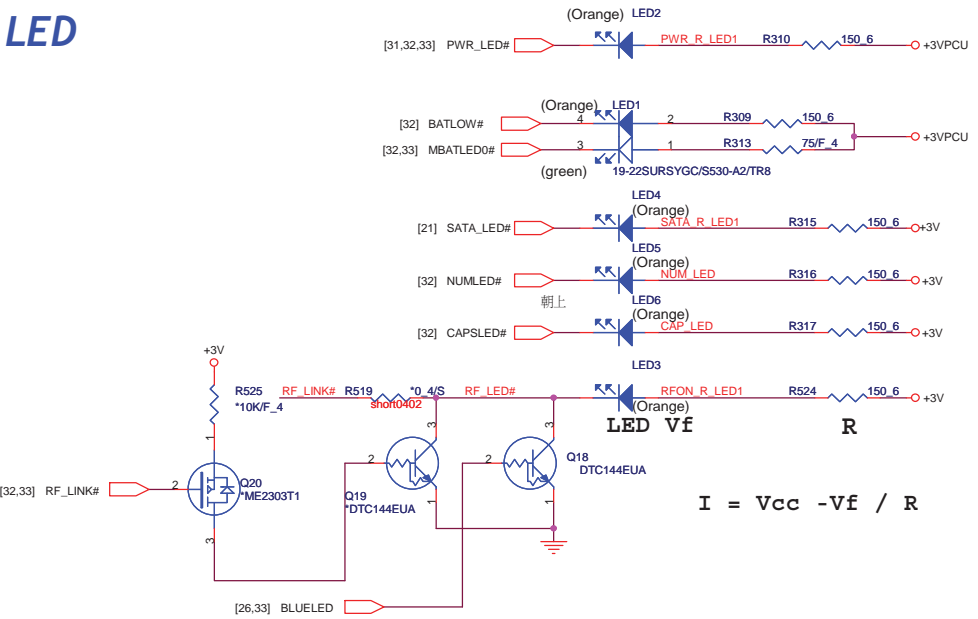
AL001431K04  
AL6017A2K12  
APA2031 ,AL002031K00



# MDC CONNECTOR



# LED



$$I = \frac{V_{cc} - V_f}{R}$$



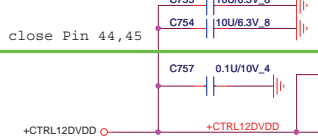
**PROJECT : QL5**  
Quanta Computer Inc.

Size Custom	Document Number <b>AMP_TPA6017/Accelerometer</b>	Rev 1A
Date: Tuesday, March 17, 2009	Sheet 27	of 41

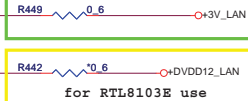
T : Stuffed for RTL8111DL(10/100/1000)

E : Stuffed for 8103EL(10/100)

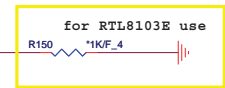
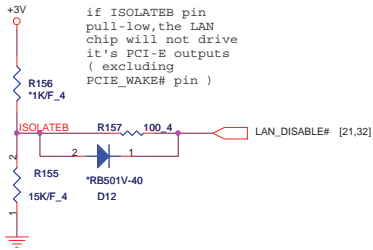
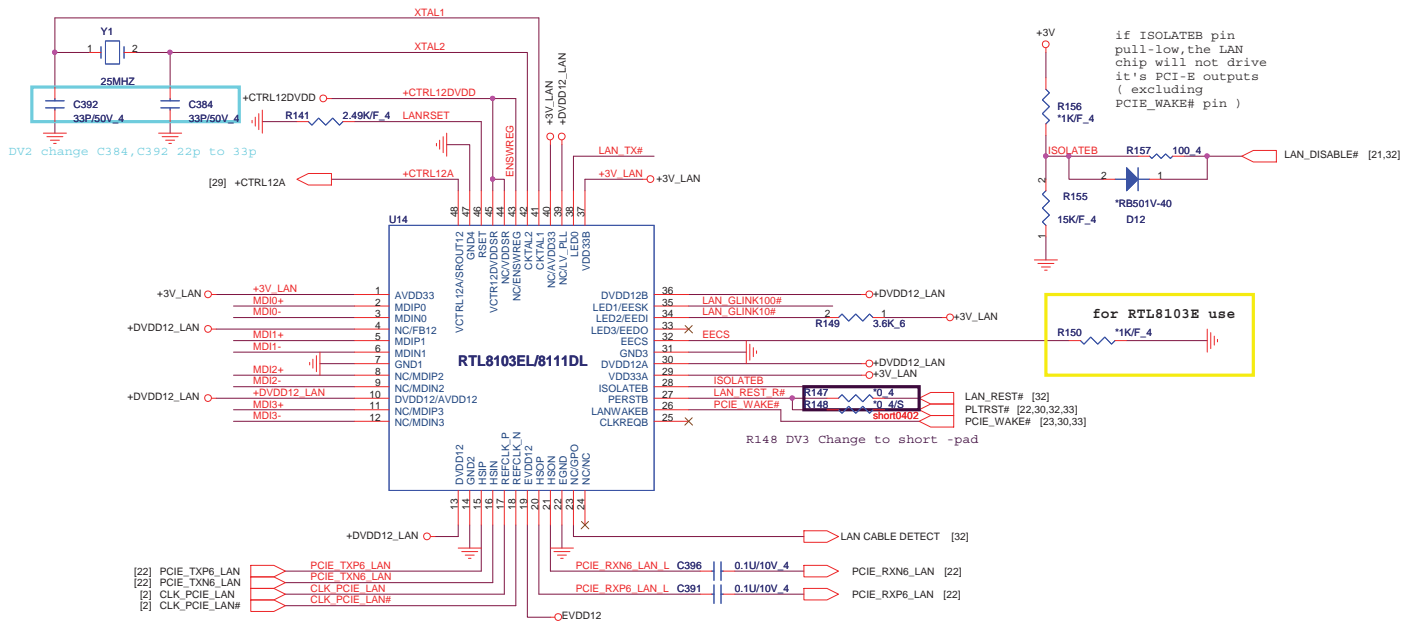
for RTL8111DL use



for RTL8111DL use

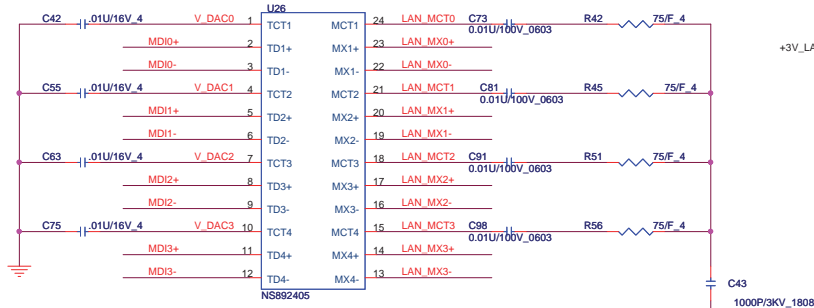
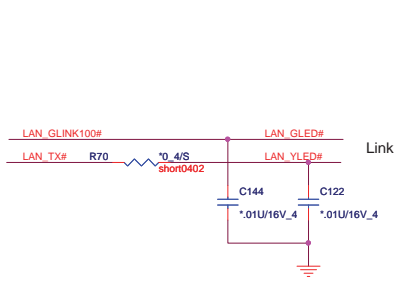


Remove R3571, R3573
R3571 and R3573 are used in RTL8111DL, remove R3573 if switching regulator is enable, Remove R3571 external power is used.



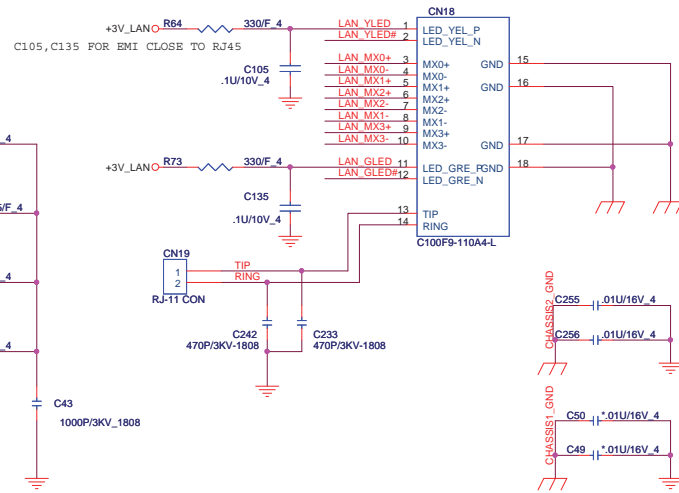
AL08111DB00 RTL8111DL-GR
AL08103EB00 RTL8103EL-GR

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NS892402: GIGABIT DB0AT9LAN05
NS892405: 10/100 DB0ZB1LAN04

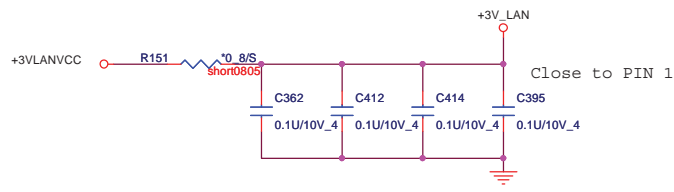
RJ45



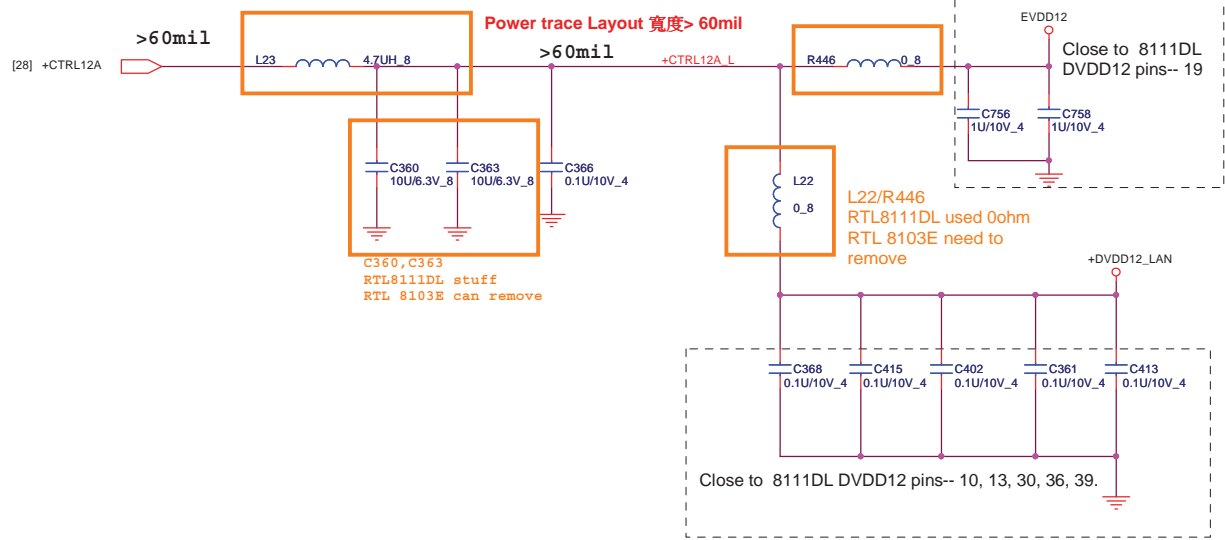
PROJECT : QL5
Quanta Computer Inc.
NB5
Document Number: RTL8111DL/8103EL/RJ45
Date: Tuesday, March 17, 2009
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T : Stuffed for RTL8111C(10/100/1000)

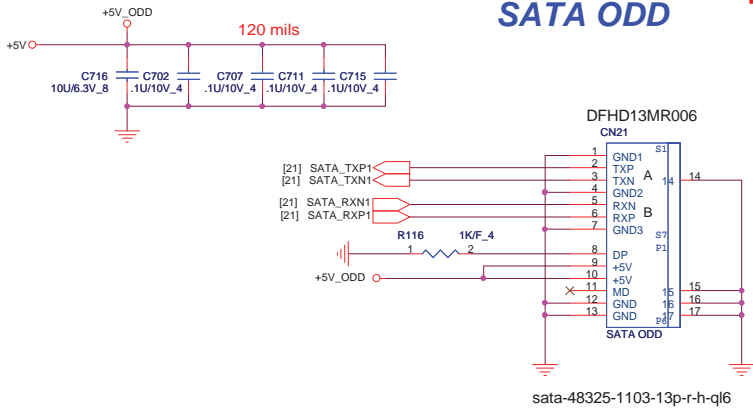
E : Stuffed for 8102E(10/100)



L23  
 RTL8111DL (Gaga lan) use 4.7uH  
 power choke A>600mA tolerance  
 ±15%  
 RTL8103E stuff 0ohm

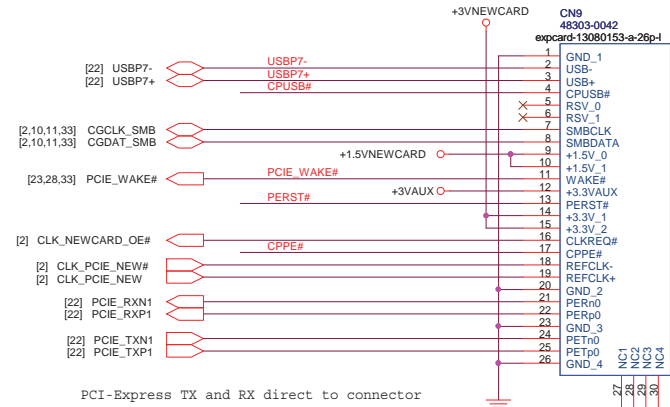


### SATA ODD

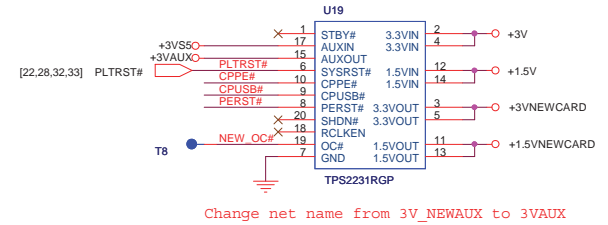


### NEWCARD

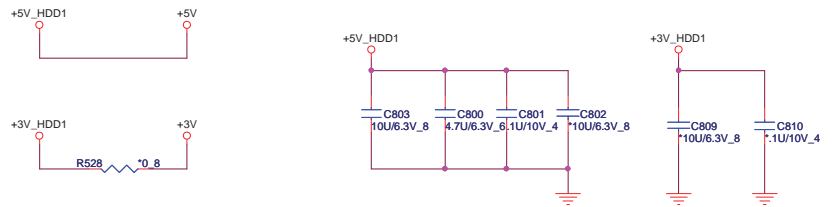
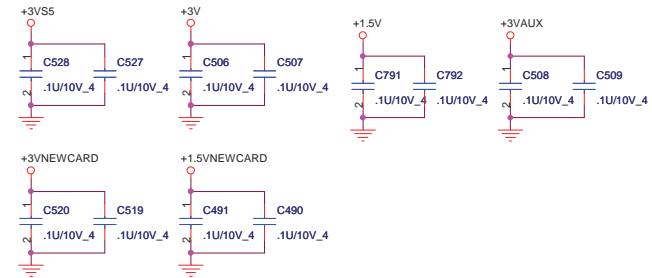
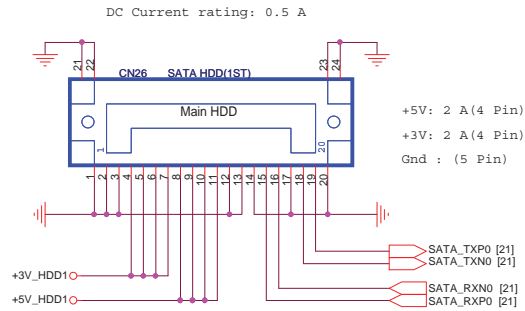
### NEWCARD (PCIEXPRESS\*1 + USB\*1)



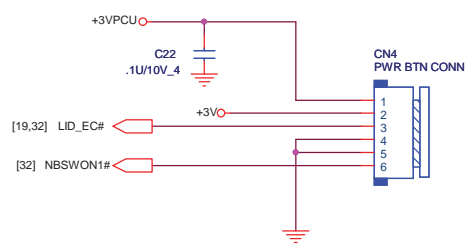
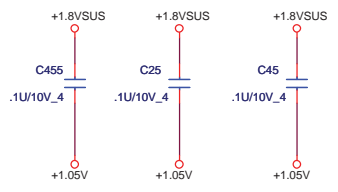
Change CN15#31,32 as ME request for Hole pad  
 expcard-48303-0042-26p-1-qt6 as ME modify Pad size (pin31,32)  
 Move CN15#29,30 Pin as ME request (Molex confirm drawing)



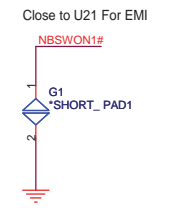
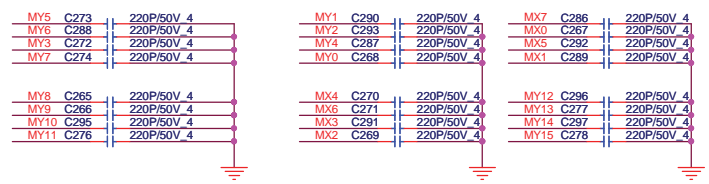
### SATA\_1 CONNECTOR



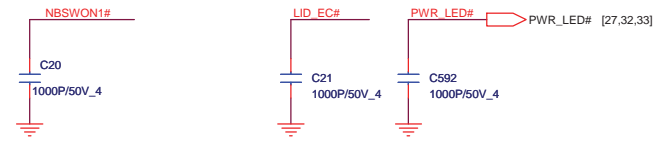
	<b>PROJECT : QL5</b>	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
	<b>ODD/HDD/NEW CARD</b>	
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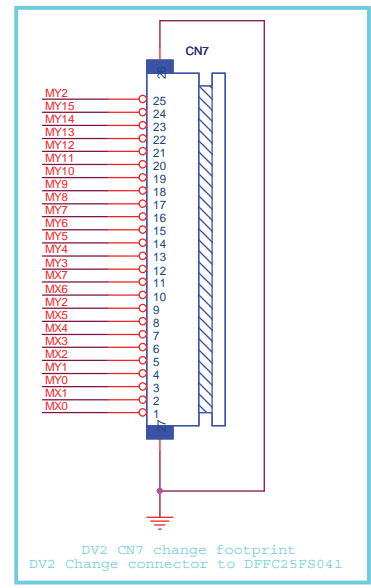
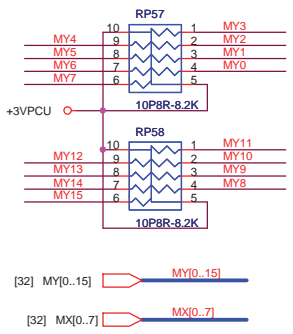
1. +3VPCU(LIDSWITCH PWR)
2. +3V
3. LIDSWITCH
4. GND
5. GND
6. POWERON#
7. NC
8. NC



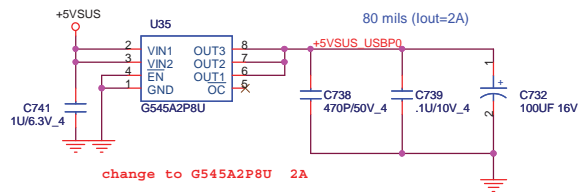
**POWER BOTTON CONNECT**



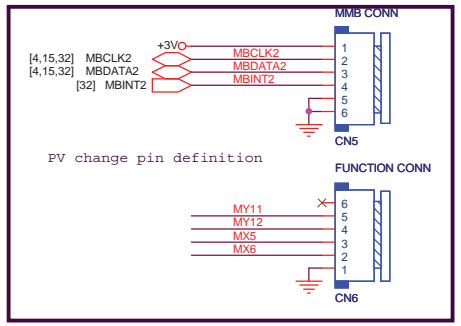
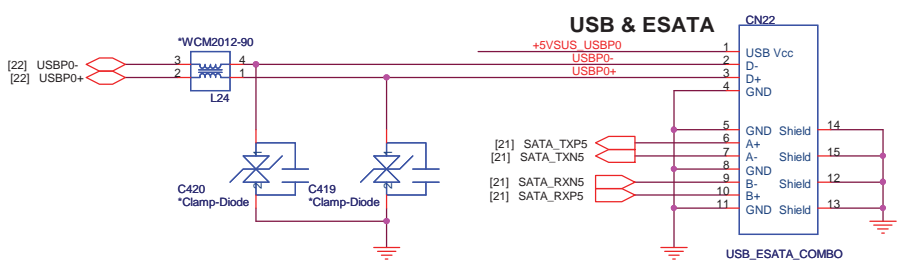
**KEYBOARD PULL-UP**



**E-SATA/USB COMBO**

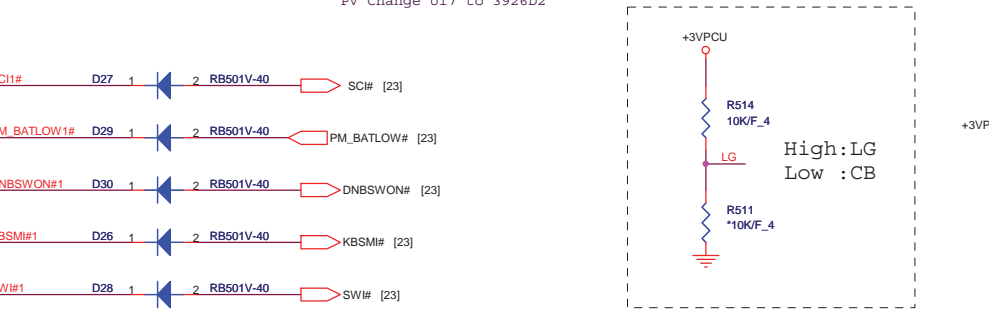
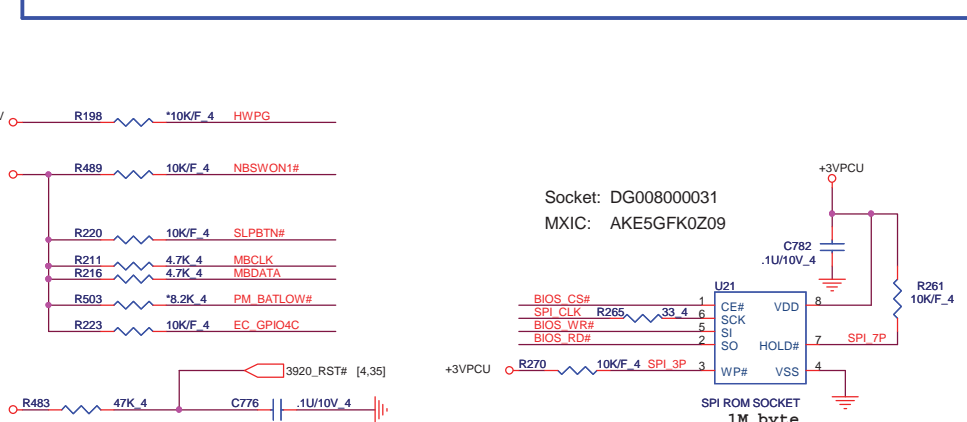
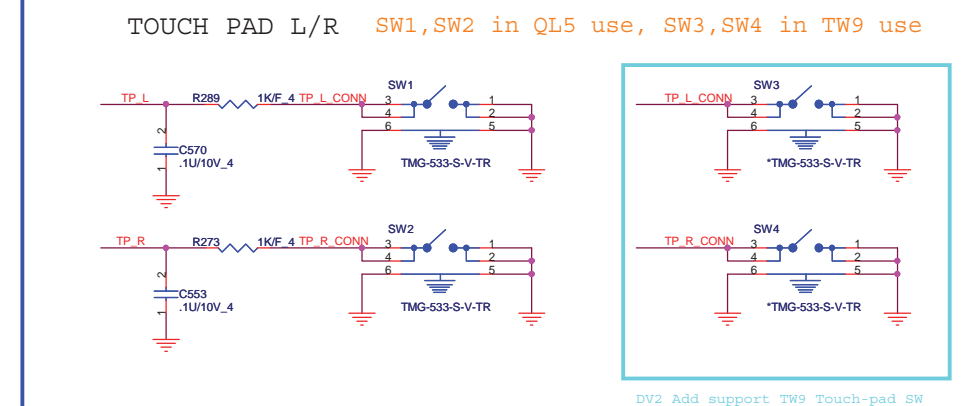
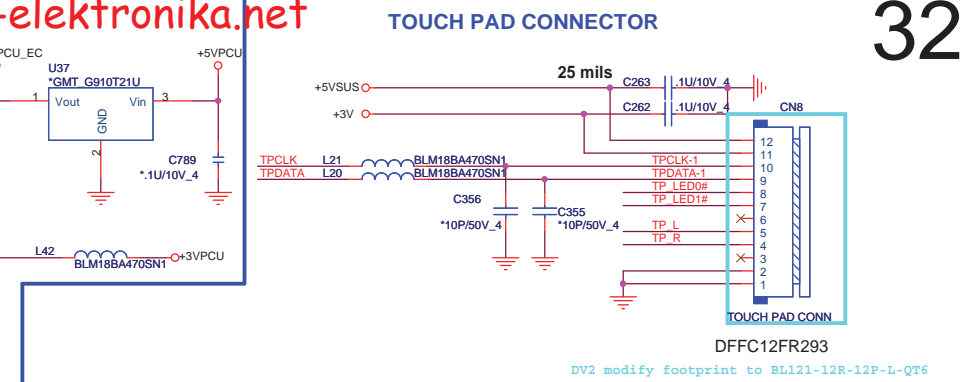
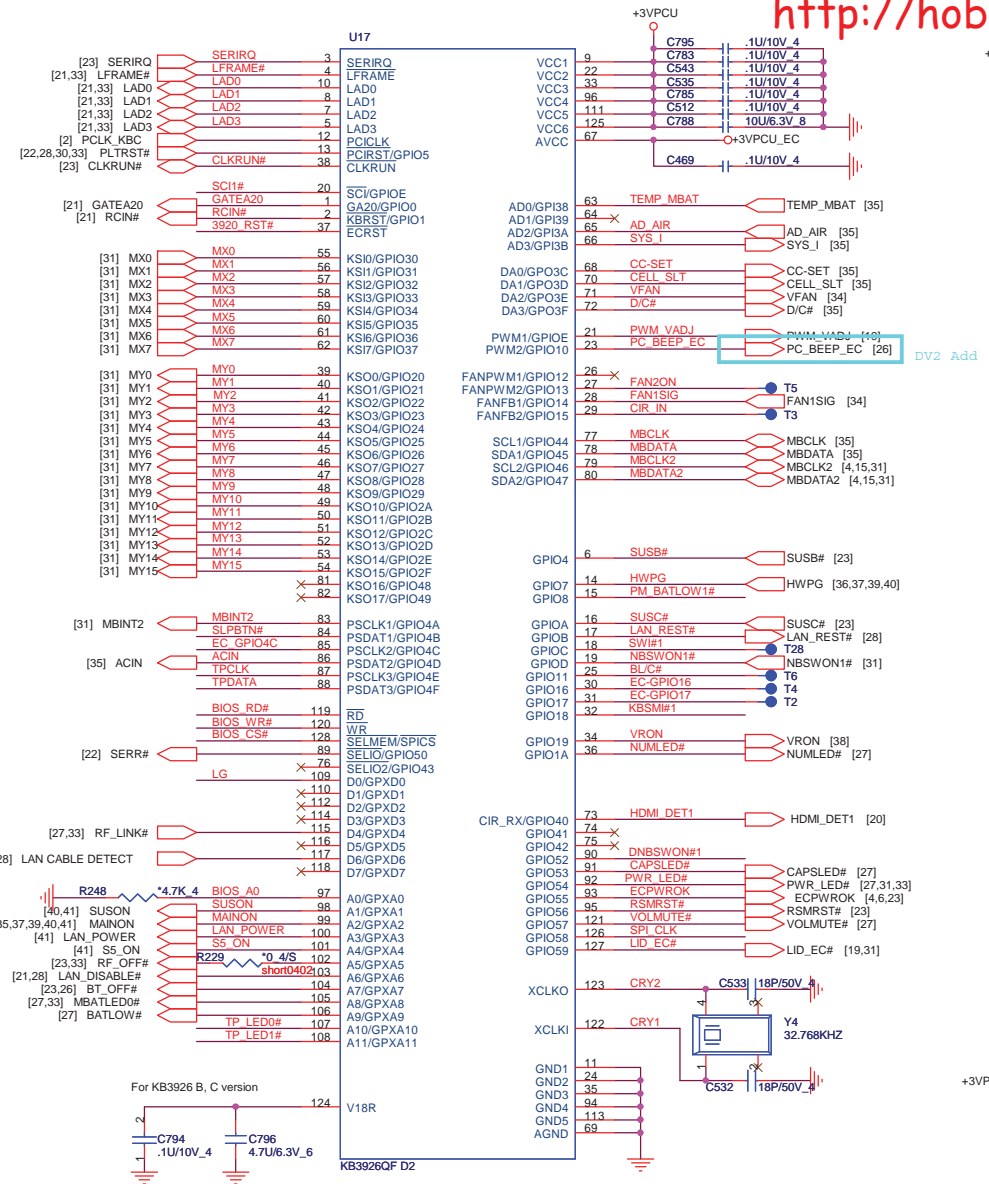


change to G545A2P8U 2A



**PROJECT : QL5**  
Quanta Computer Inc.

Size Custom	Document Number <b>KB/CAP/POWER CONN</b>	Rev 1A
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**PROJECT : QL5**  
Quanta Computer Inc.

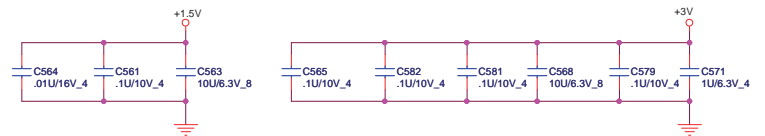
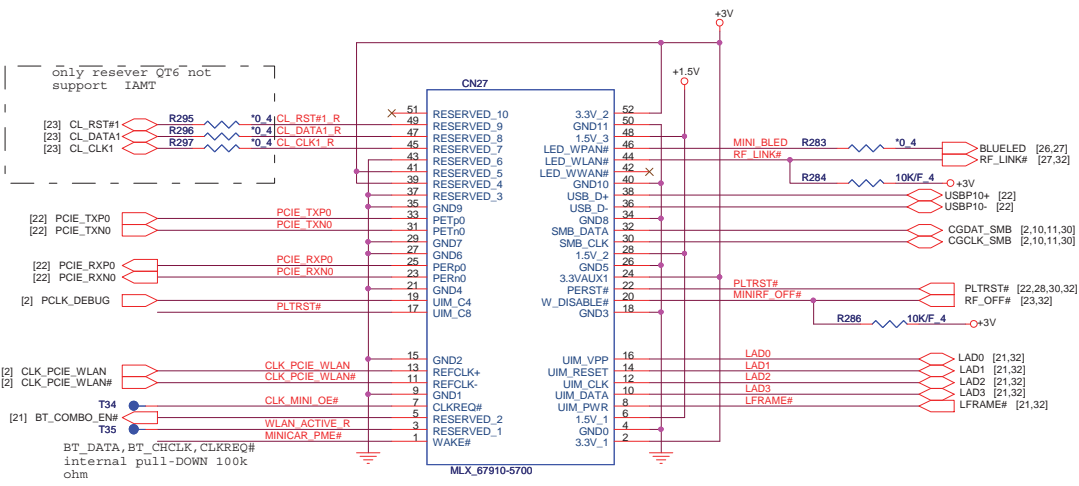
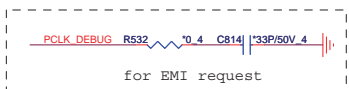
**NB5**

Size Custom | Document Number: KB3926/ROM/TP | Rev 1A

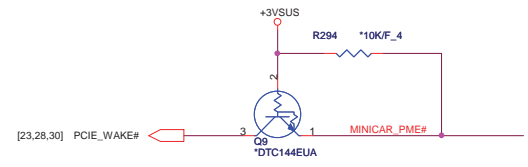
Date: Tuesday, March 17, 2009 | Sheet 32 of 41



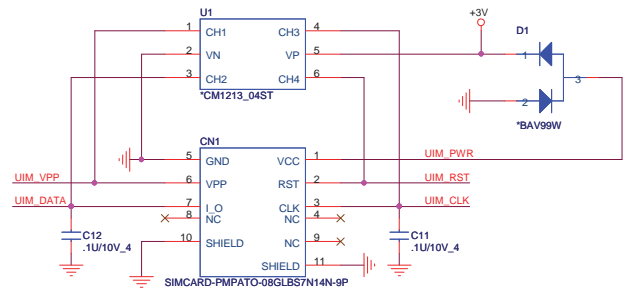
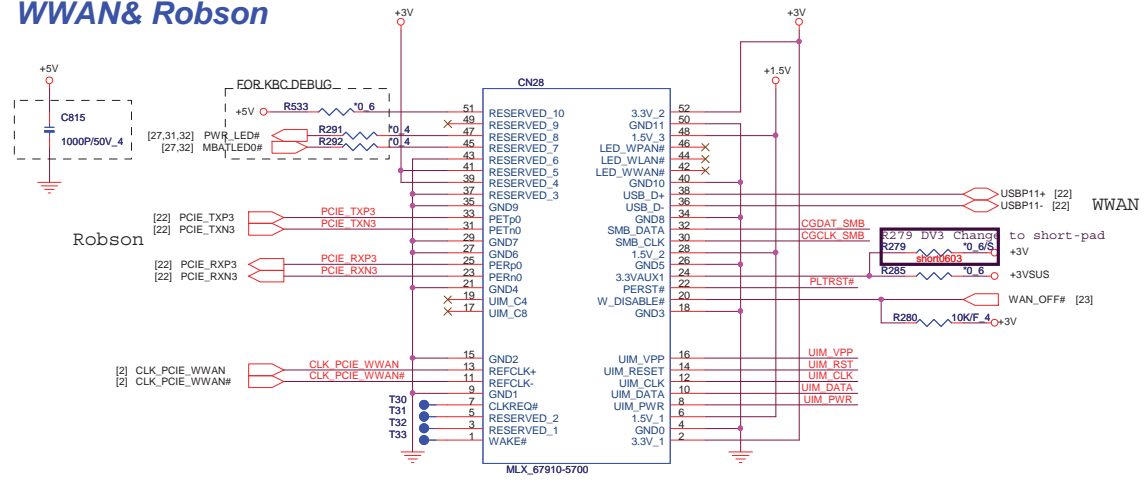
# Mini PCI-E Card 1 WLAN



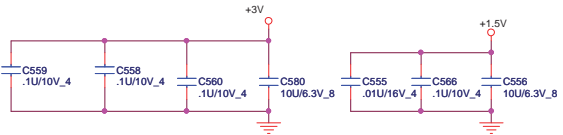
INTEL WLAN CARD PIN 20 W\_DISABLE# have internal pull-up 110k ohm



# Mini PCI-E Card 2 WWAN& Robson

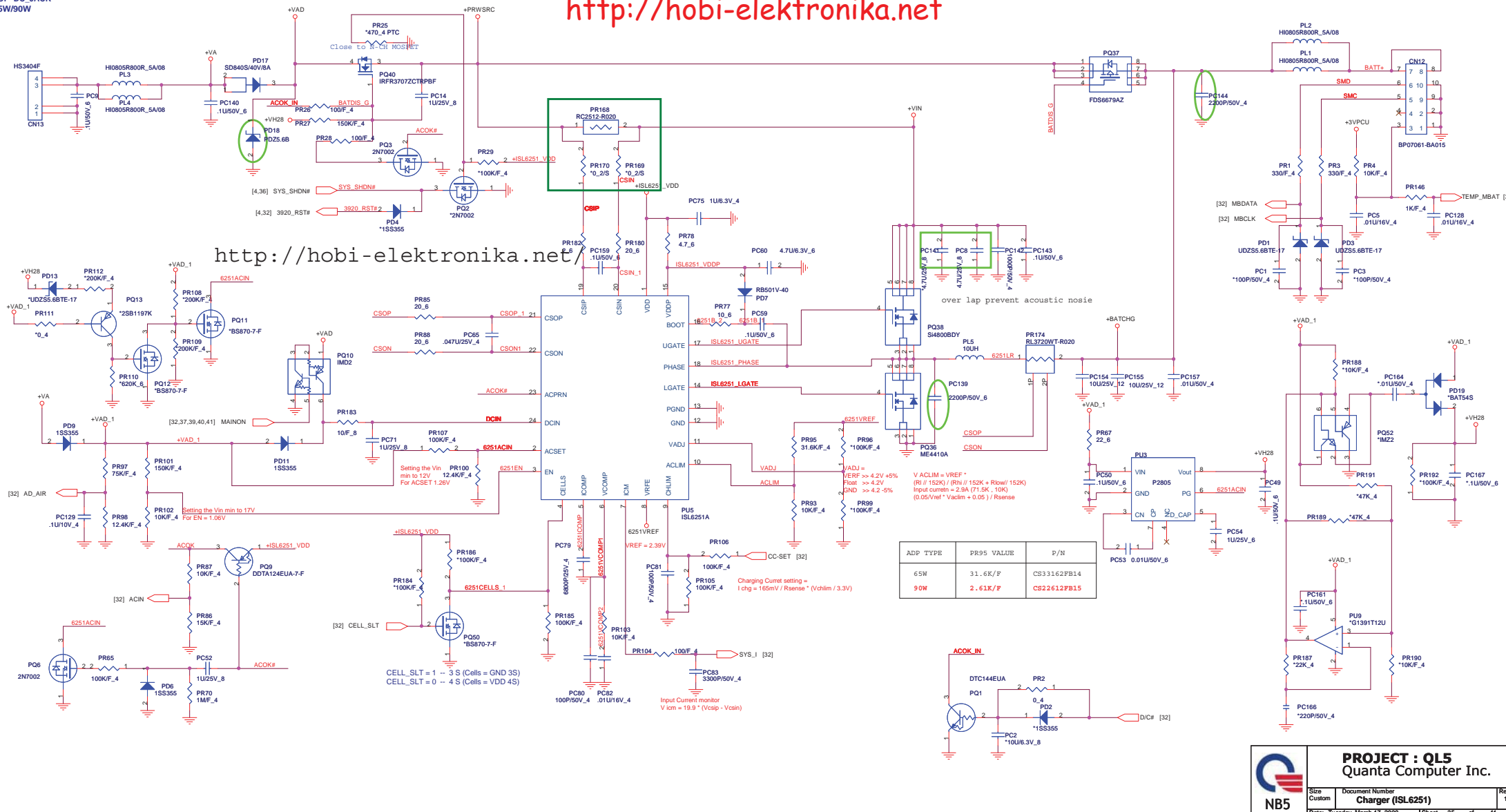


Add shielding connect to GND



	<b>PROJECT : QL5</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	MINI PCIE CONN X2	
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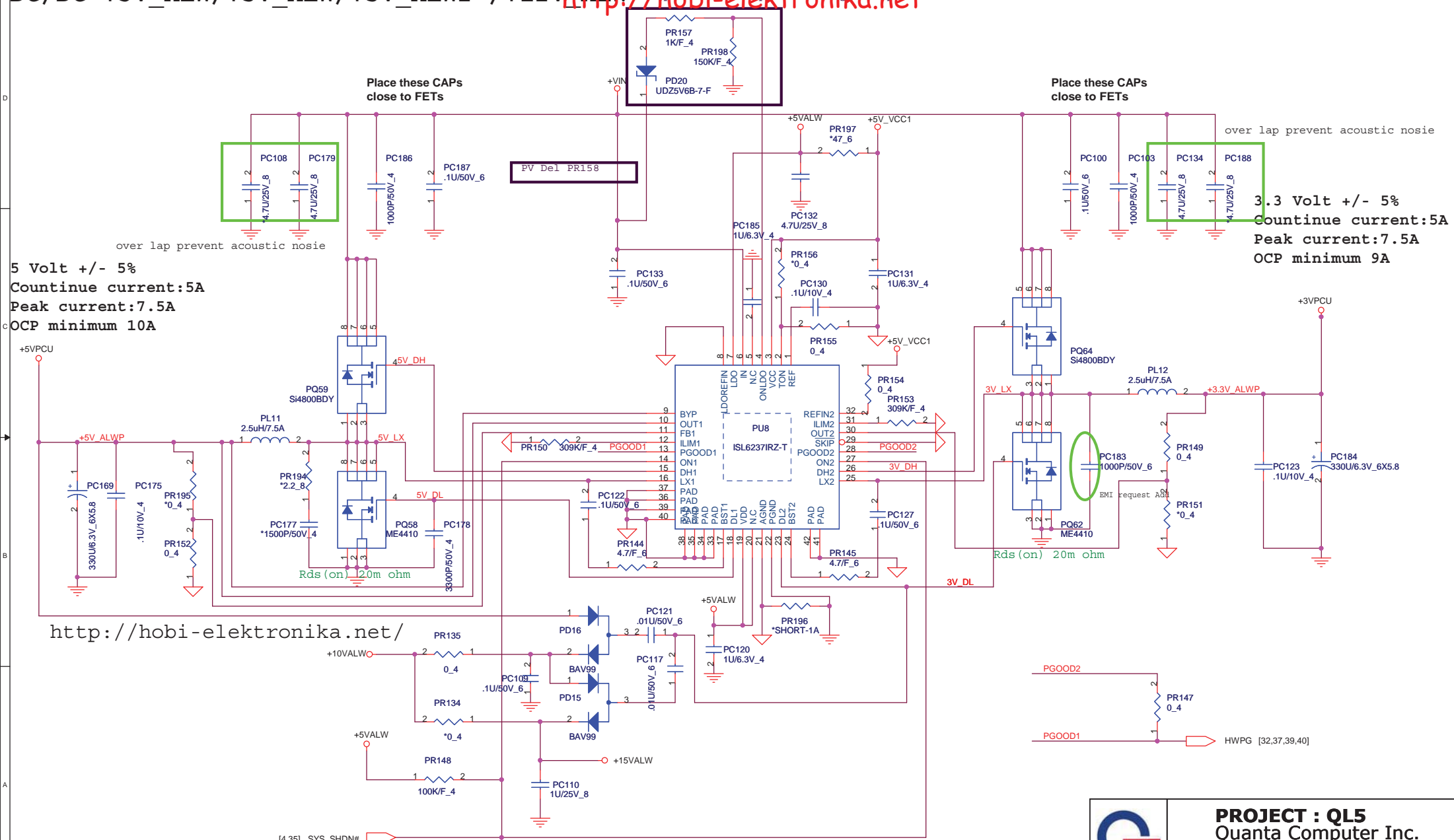


ADP TYPE	PR95 VALUE	F/N
65W	31.6K/F	CS33162FB14
90W	2.61K/F	CS22612FB15

**PROJECT : QL5**  
**Quanta Computer Inc.**

Size: Custom    Document Number: **Charger (ISL6251)**    Rev: 1A

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5 Volt +/- 5%  
 Countinue current:5A  
 Peak current:7.5A  
 OCP minimum 10A

3.3 Volt +/- 5%  
 Countinue current:5A  
 Peak current:7.5A  
 OCP minimum 9A

<http://hobi-elektronika.net/>

[4.35] SYS\_SHDN#



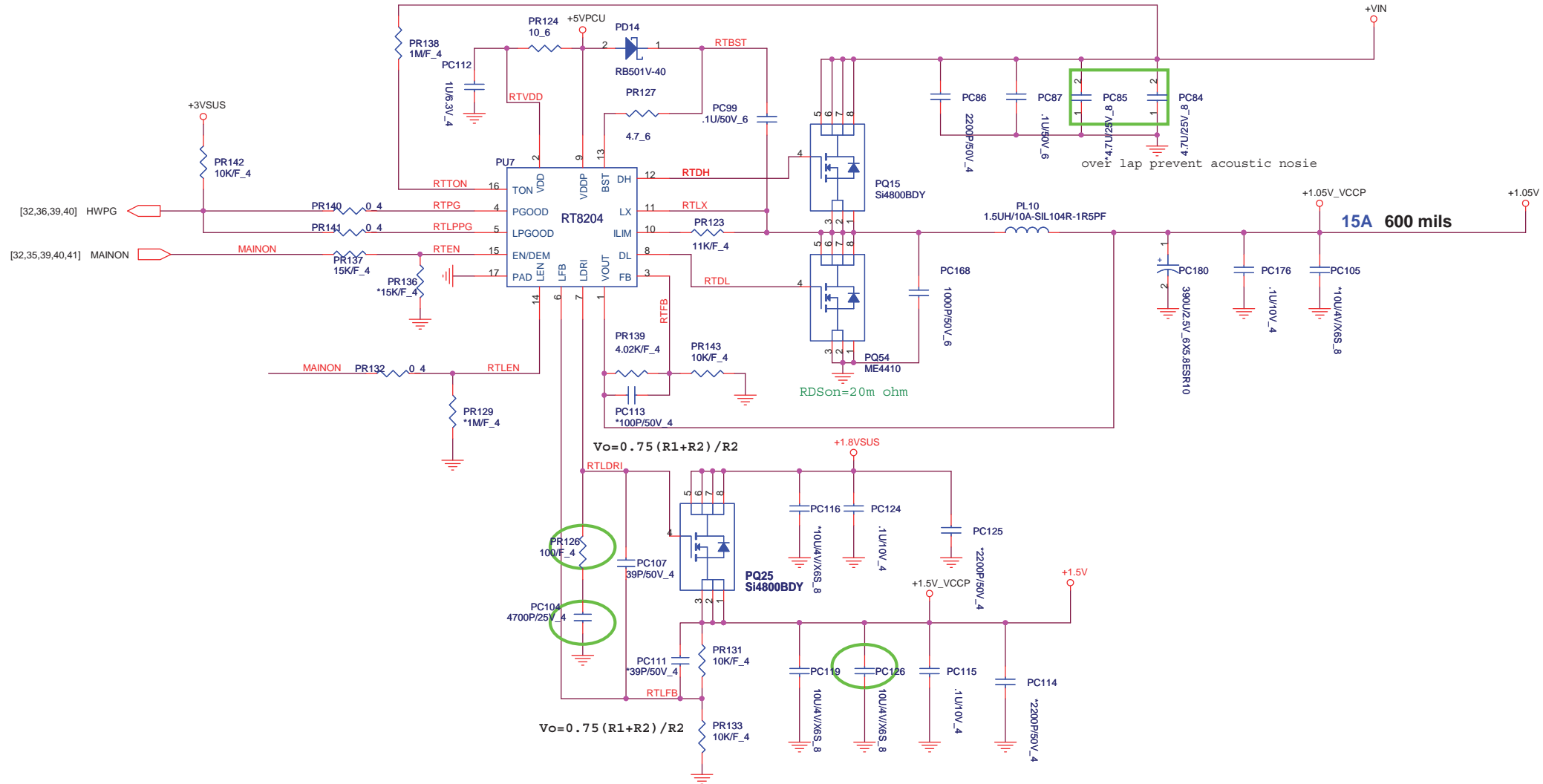
**PROJECT : QL5**  
 Quanta Computer Inc.

Size B	Document Number <b>+5V/+3V (ISL6237)</b>	Rev 1A
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# VCCP1.05V & +1.5V

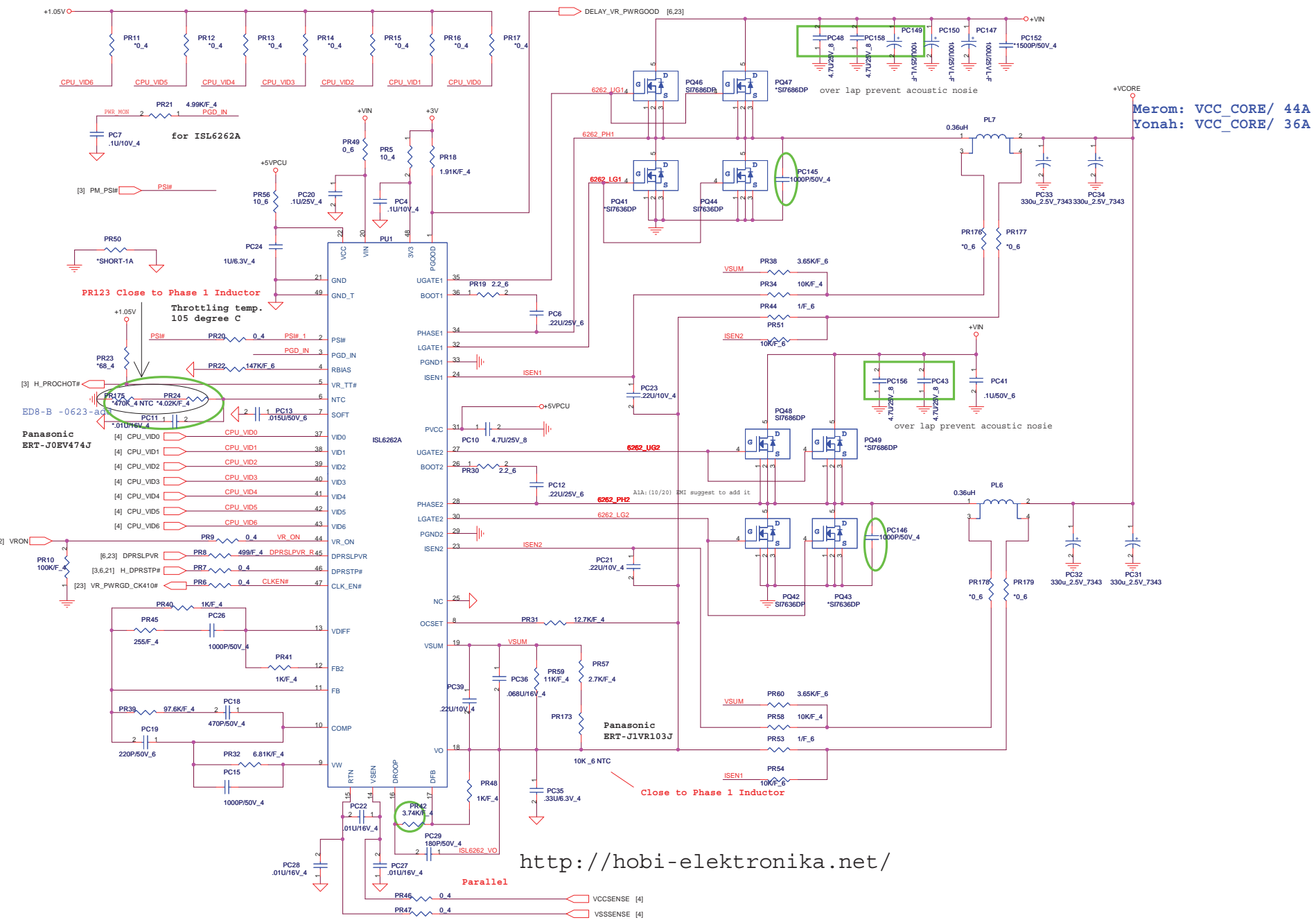
<http://hobi-elektronika.net>

+1.05V Volt +/- 5%  
 Countinue current 6A  
 Peak current:8A  
 OCP minimum 12A




<http://hobi-elektronika.net/>

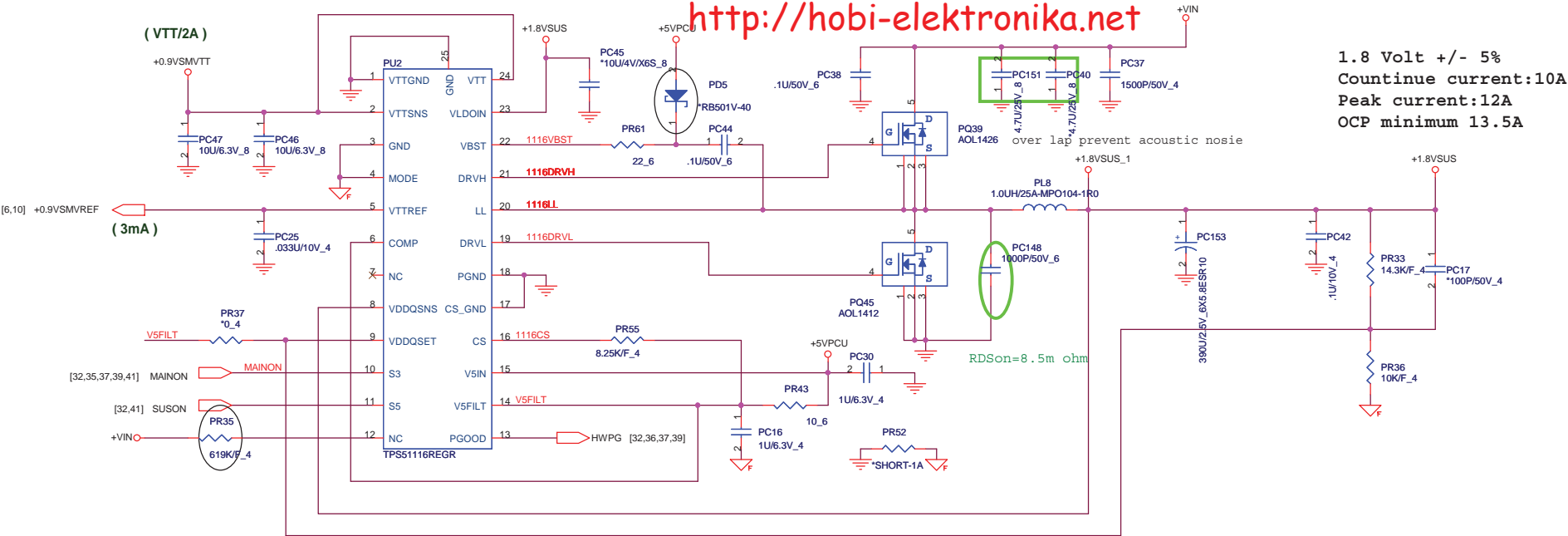
	<b>PROJECT : QL5</b> Quanta Computer Inc.	
	Size B	Document Number <b>+1.05V/+1.5V (RT8204)</b>
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Merom: VCC\_CORE/ 44A  
 Yonah: VCC\_CORE/ 36A

	<b>PROJECT : QL5</b>	
	Quanta Computer Inc.	
	Size: Custom Document Number: CPU Core ( ISL6266A ) Date: Tuesday, March 17, 2009	Rev: 1A Sheet: 38 of 41





**For Discrete Only**

1.1 Volt +/- 5%  
 Countinue current:2A  
 Peak current:3A

