

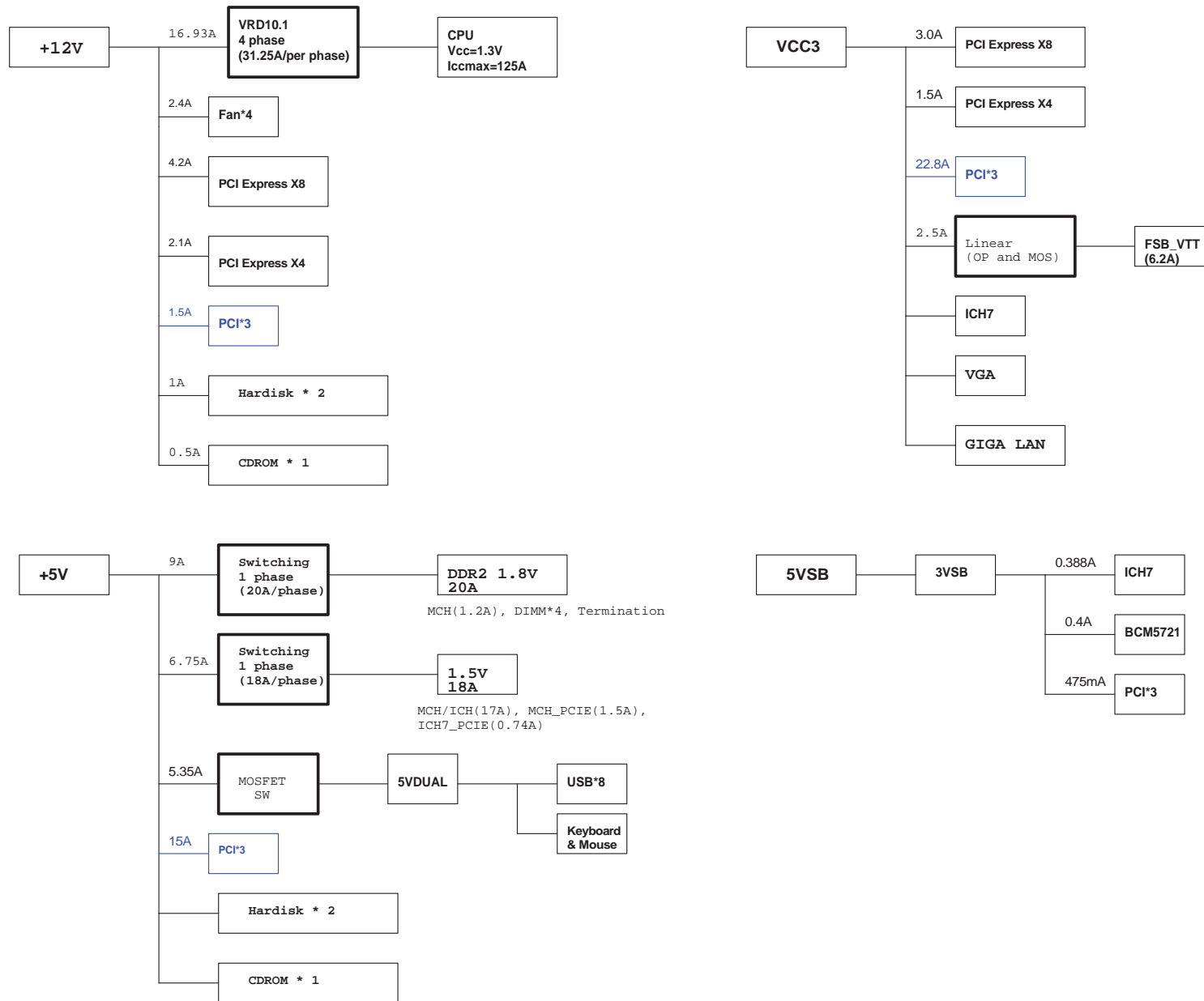


MS-9618 REV 1A

Mukilteo + ICH7 Schematics

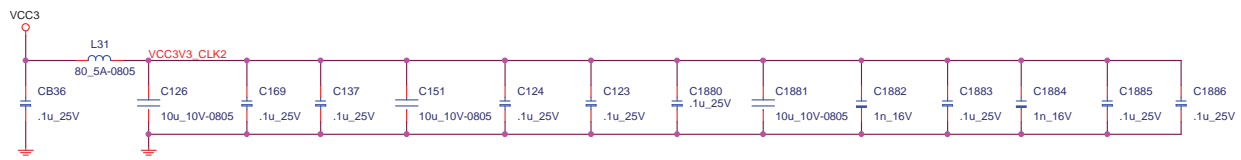
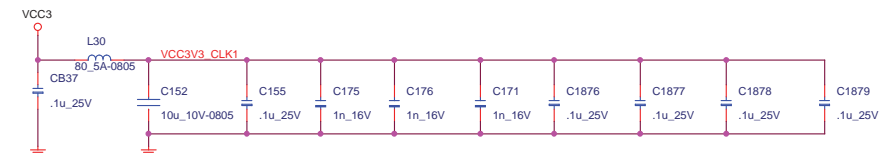
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MS-91XX POWER DELIEVERY DIAGRAM



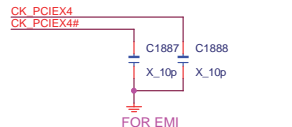
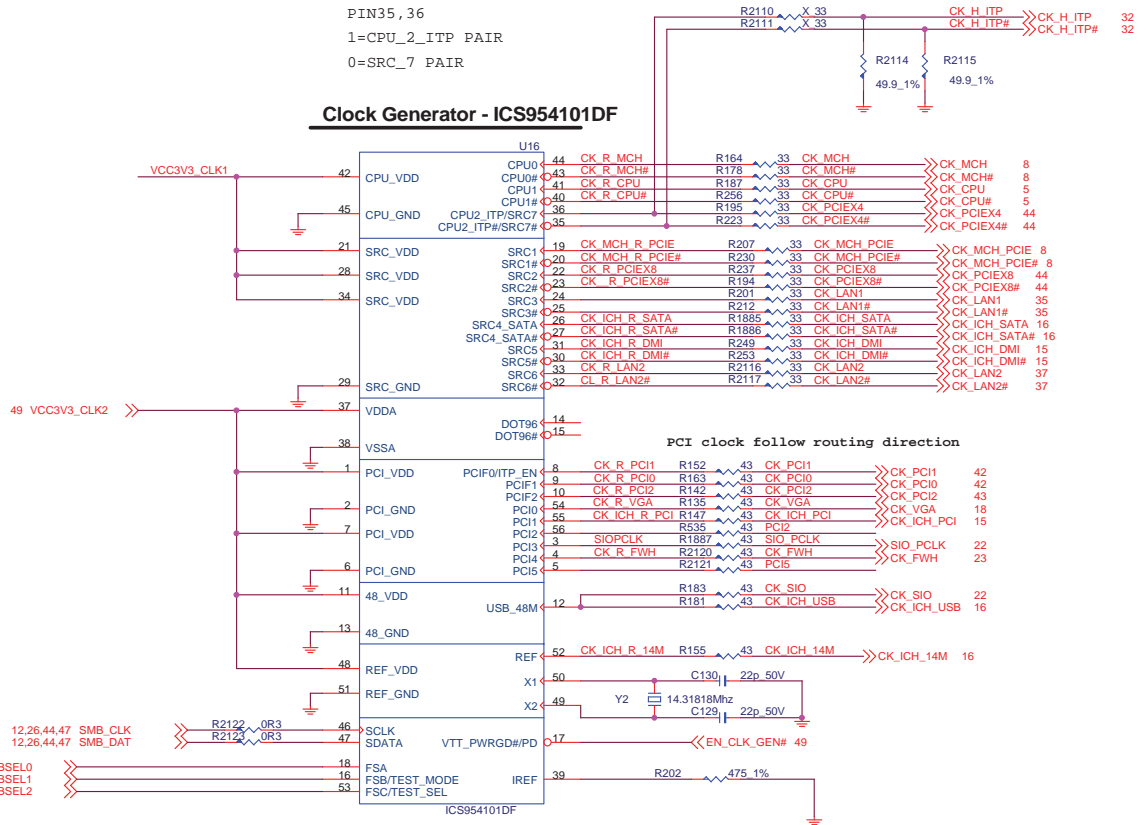
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Title	Power Delivery Block Diagram	
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PIN35, 36
 1=CPU_2_ITP PAIR
 0=SRC_7 PAIR

Clock Generator - ICS954101DF



CK CPU	R1883	49.9 1%
CK CPU#	R222	49.9 1%
CK MCH	R1884	49.9 1%
CK MCH#	R208	49.9 1%
CK PCIE#	R200	49.9 1%
CK PCIE4	R196	49.9 1%
CK MCH PCIE	R165	49.9 1%
CK MCH PCIE#	R178	49.9 1%
CK PCIE#	R188	49.9 1%
CK PCIE#	R238	49.9 1%
CK LAN1	R255	49.9 1%
CK LAN1#	R225	49.9 1%
CK ICH SATA	R213	49.9 1%
CK ICH SATA#	R248	49.9 1%
CK ICH DMI	R193	49.9 1%
CK ICH DMI#	R254	49.9 1%
CK LAN2	R217	49.9 1%
CK LAN2#	R218	49.9 1%

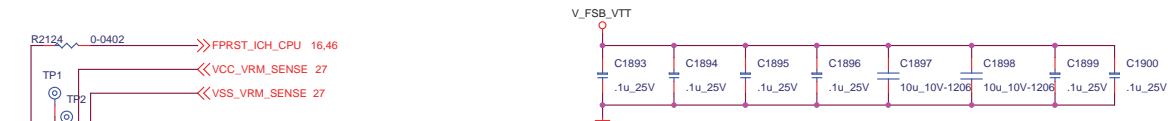
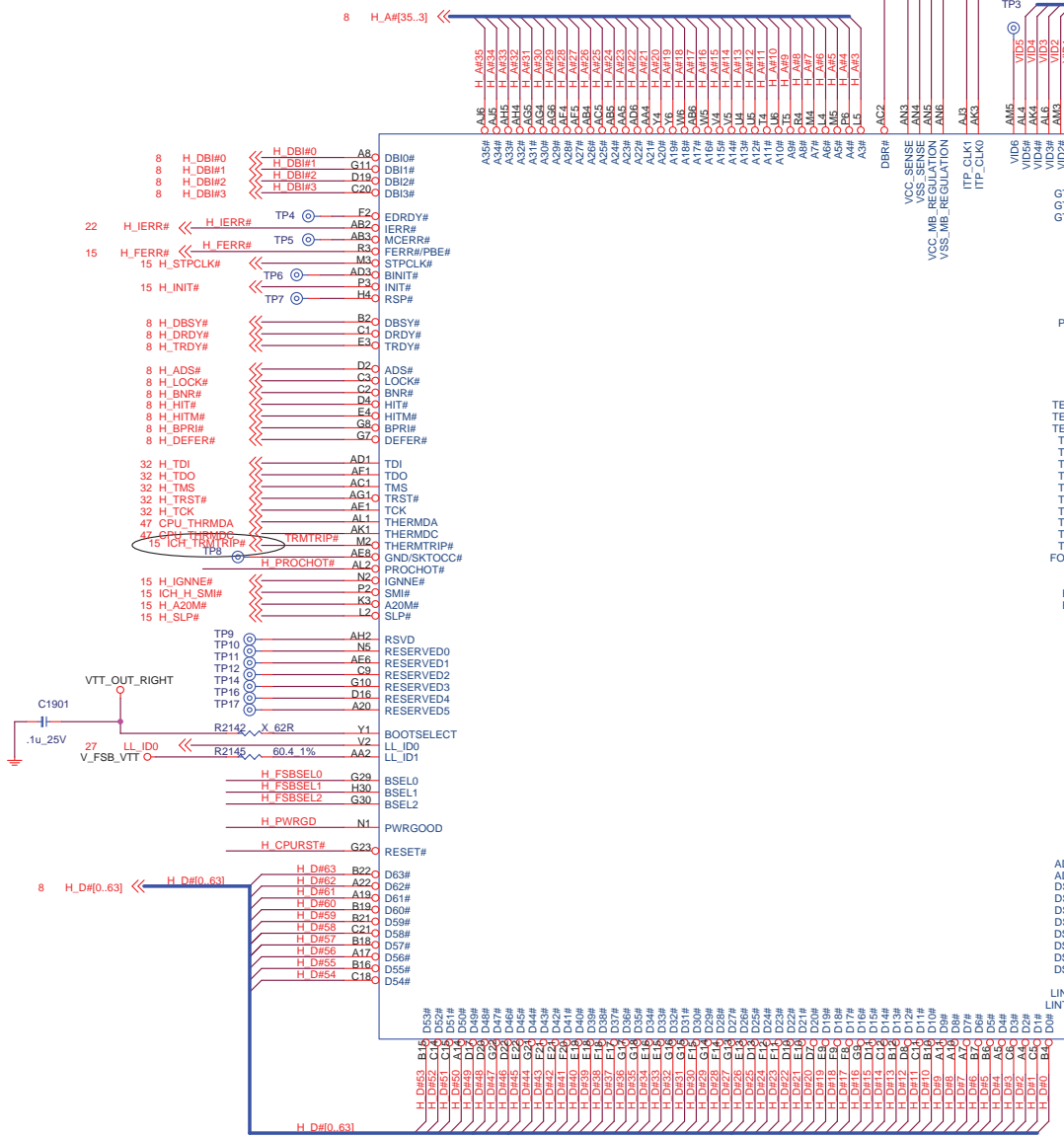
CK PCI	C134	10p
CK PCIO	C140	10p
CK PCI2	C125	10p
CK VGA	C162	10p
CK ICH PCI	C128	10p
PCI2	C1625	10p
CK FW#	C150	10p
CK ICH USB	C1889	10p
CK SIO	C1890	10p
CK ICH 14M	C1891	10p
PCI5	C1892	10p
SIO_PCLK	C2355	10p

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Size	Document Number	MS-9618	
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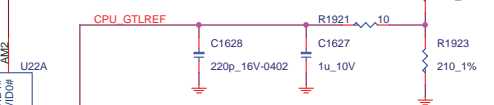
CPU SIGNAL BLOCK



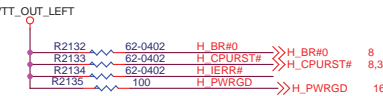
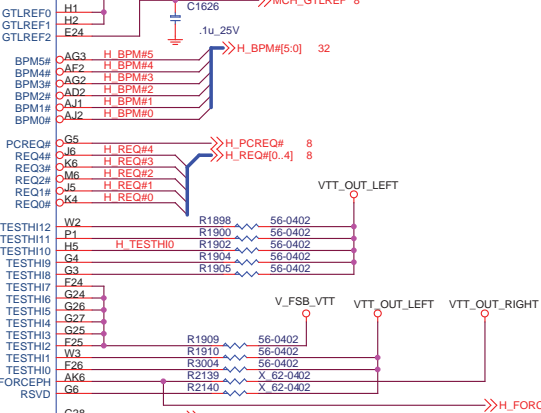
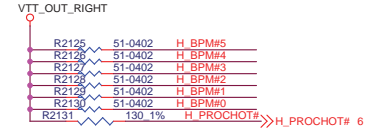
FSB FREQUENCY TABLE

H_FSBSEL0	H_FSBSEL1	H_FSBSEL2	FREQUENCY
L	H	L	200MHz
L	L	L	266MHz

GTREF VOLTAGE SHOULD BE 0.628*VTT = 0.75V

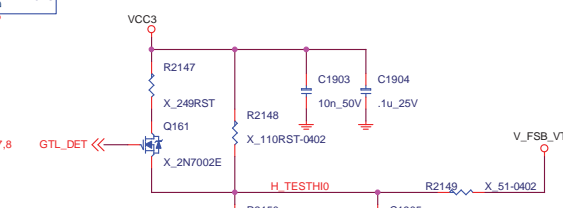
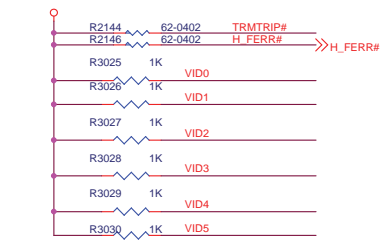


PLACE BPM TERMINATION NEAR CPU



Asynchronous

R336, R337 place at ICH7 end of routing

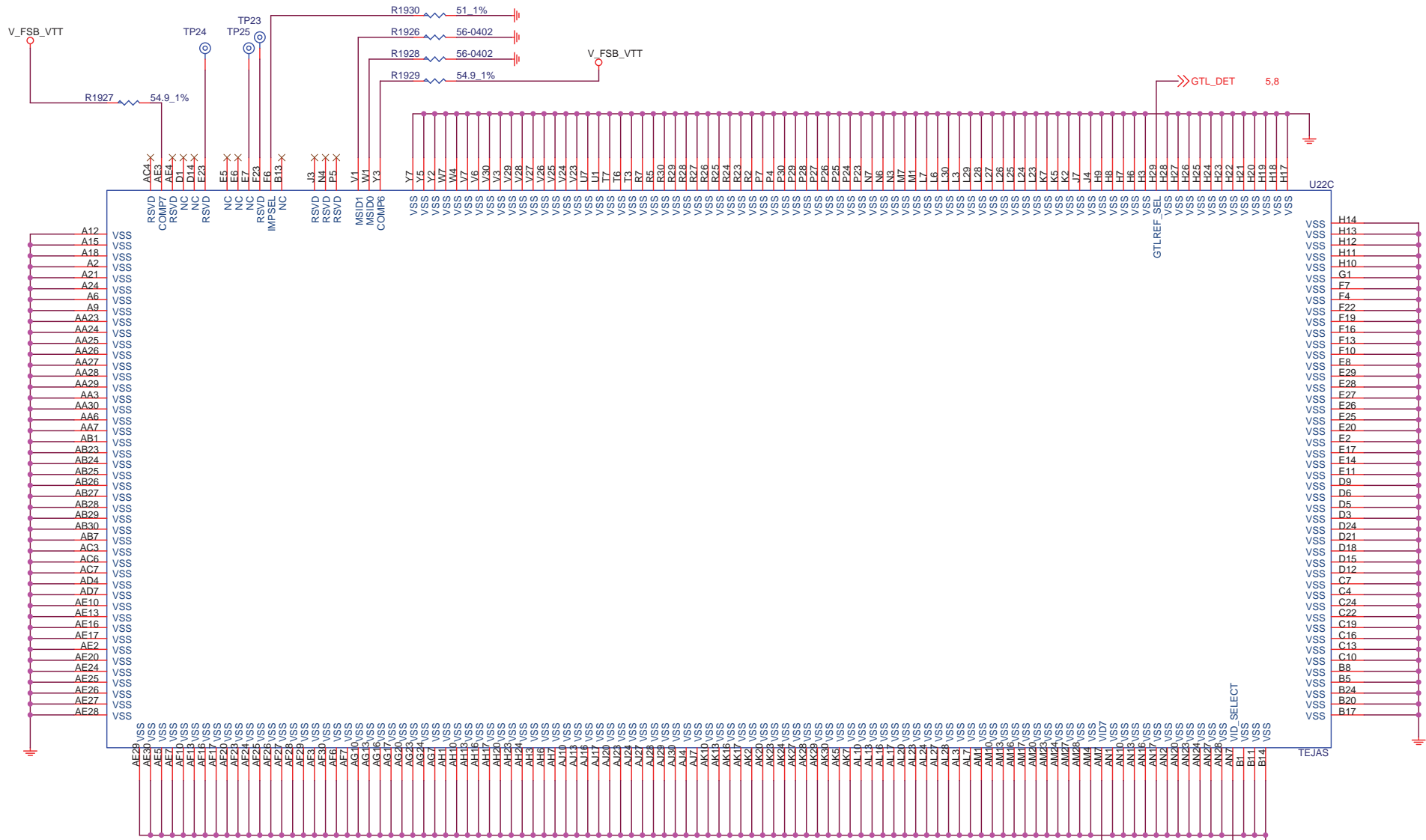


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Title: **Intel LGA775 Signal Block**

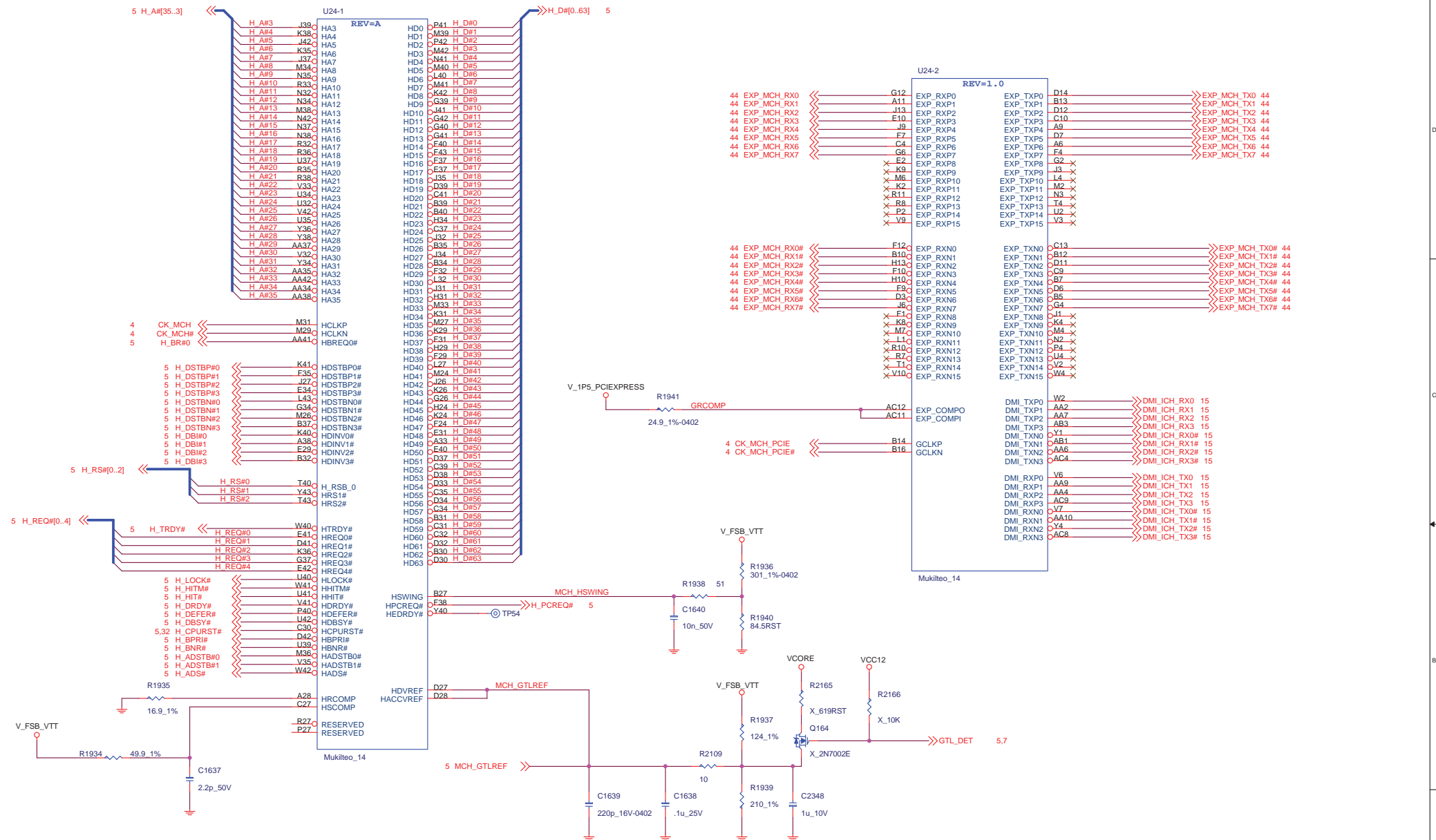
Size: Document Number
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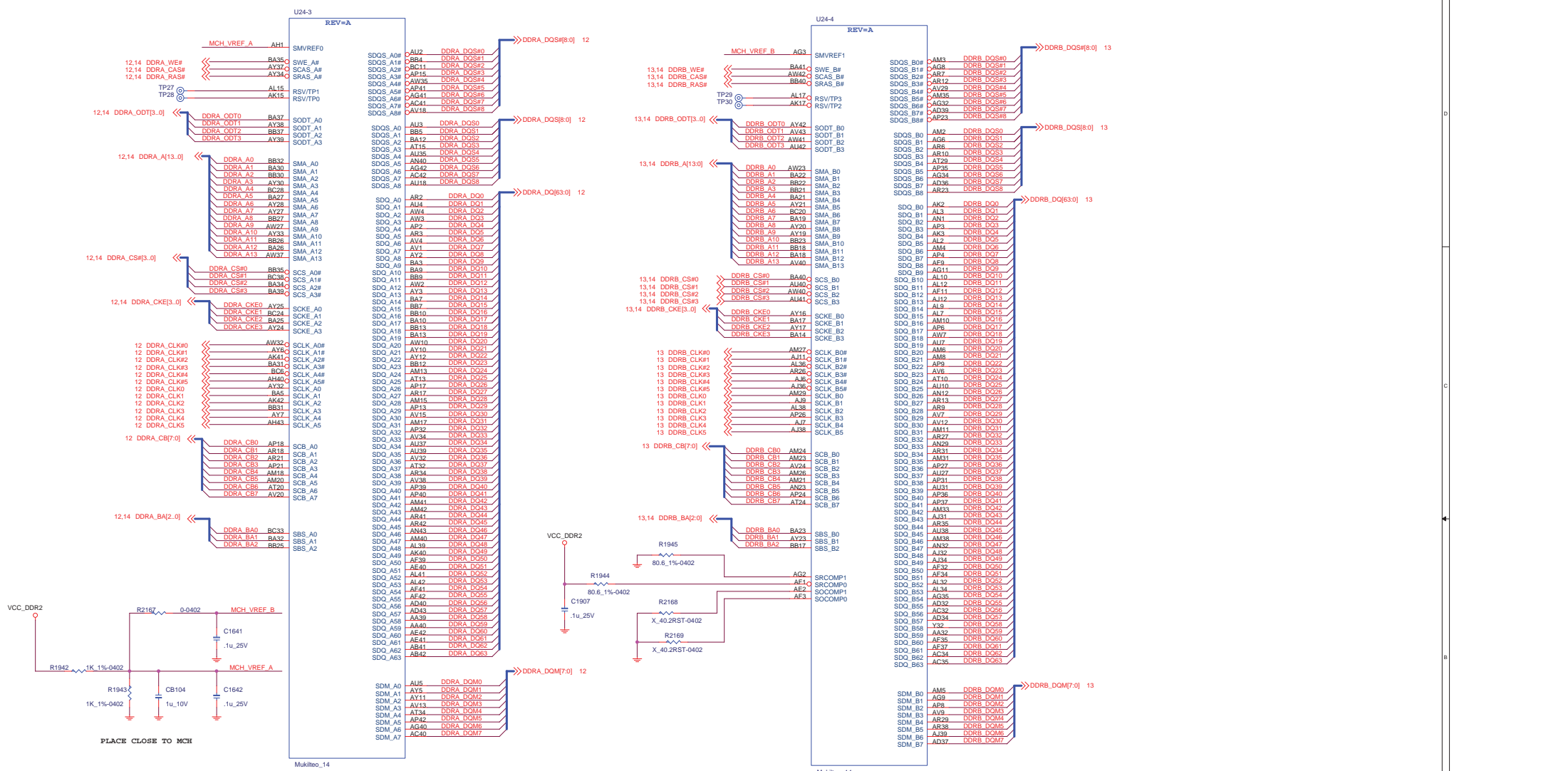
Title Intel LGA775 GND		
Size Custom	Document Number MS-9618	Rev 1A
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Title Glenwood CPU/PCI Signal		
Size Custom	Document Number MS-9618	Rev 1A
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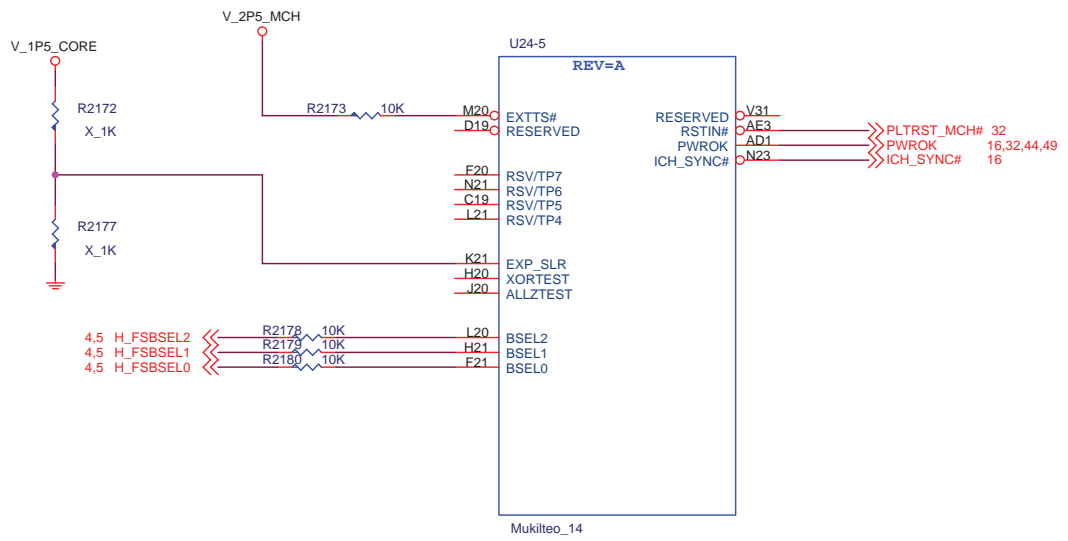


Mukilteo_14

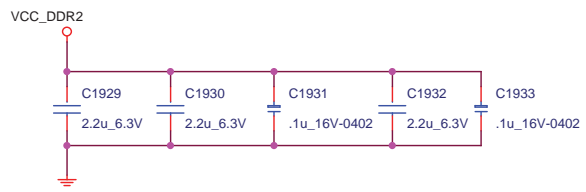
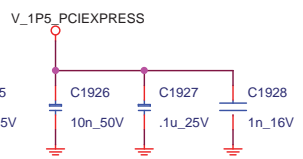
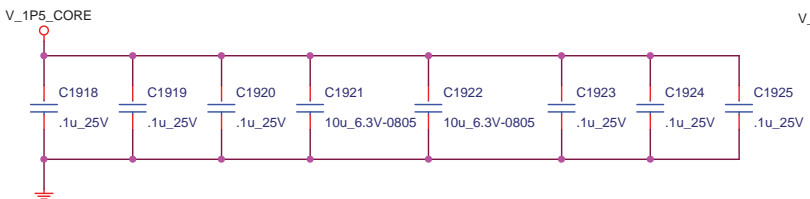
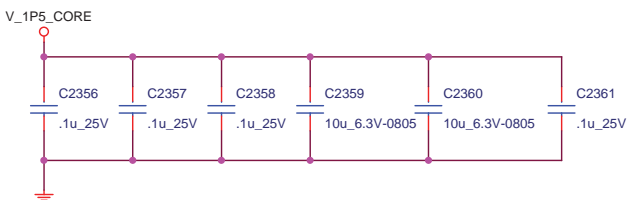
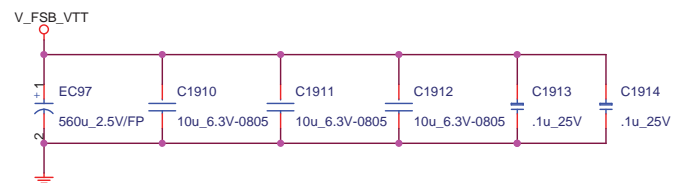
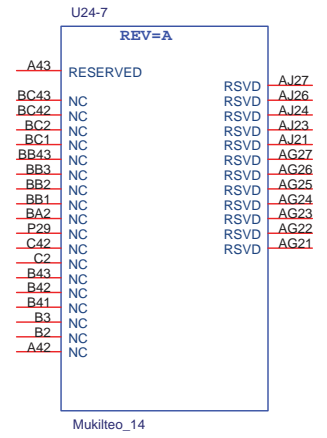
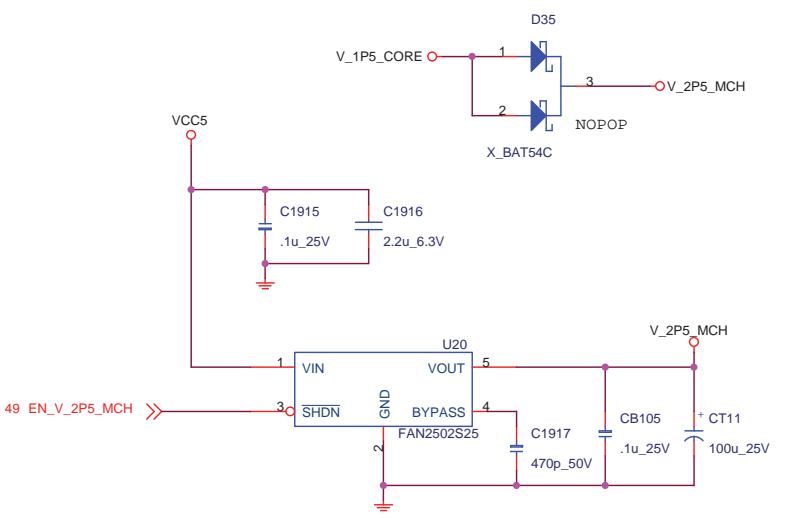
Mukilteo_14

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Title		Glenwood Memory Signal
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2.5V DAC Voltage Supplier



BSEL	TABLE		
2	1	0	PSB FREQUENCY
0	0	0	267 MHZ (800)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)

EXP Mode	
R315	Normal Operation
R325	Reverse Mode

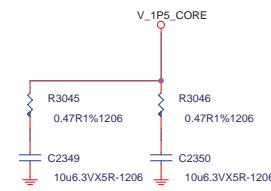
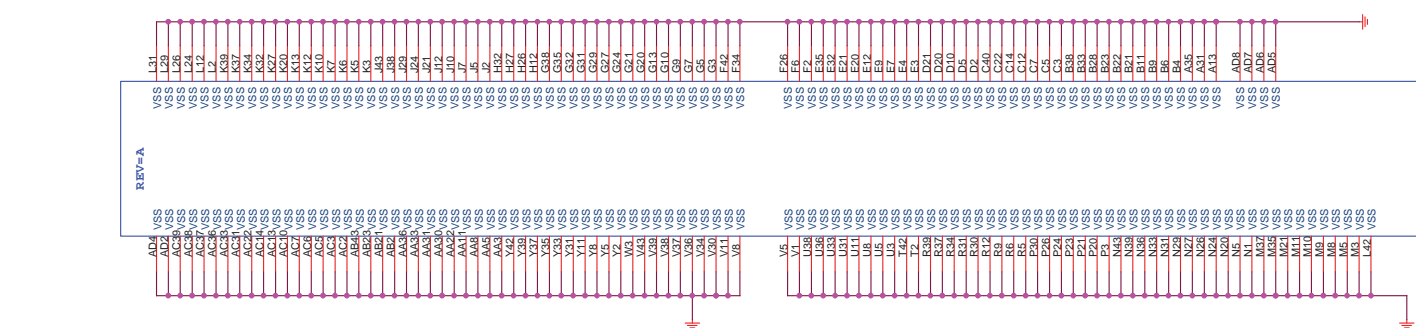
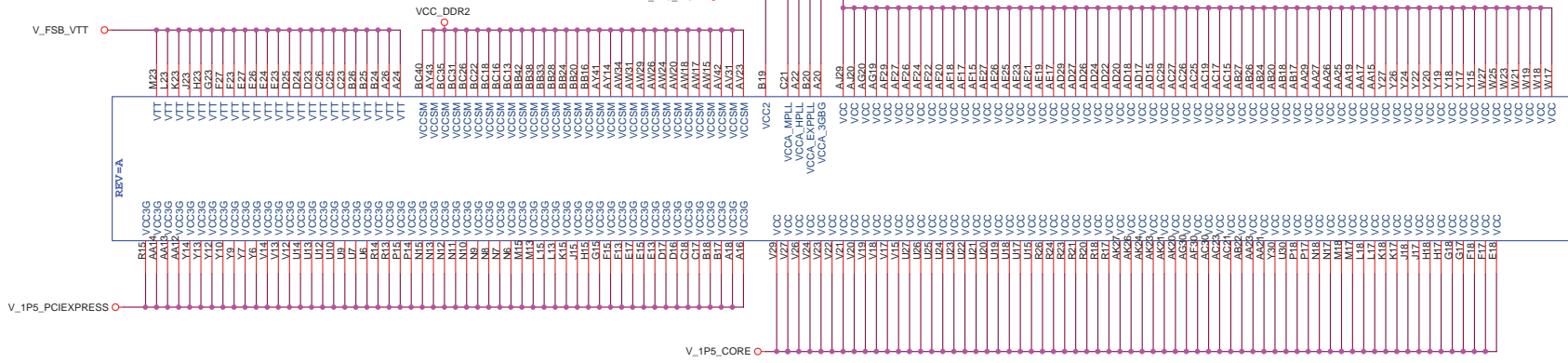
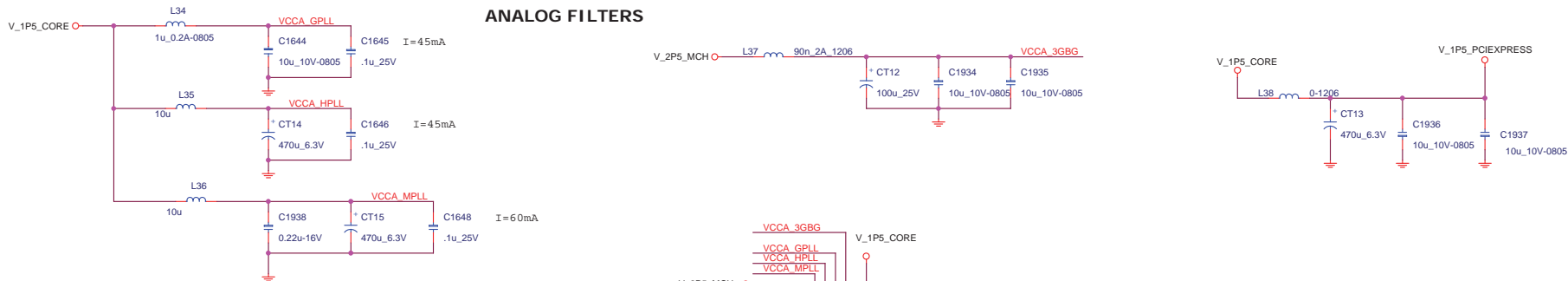
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Title: **Glenwood Misc/Power Signal**

Size: Custom
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ANALOG FILTERS



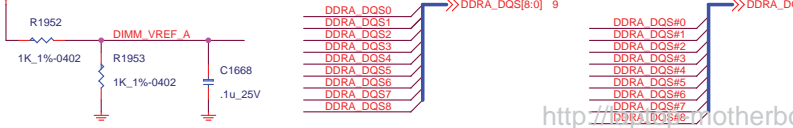
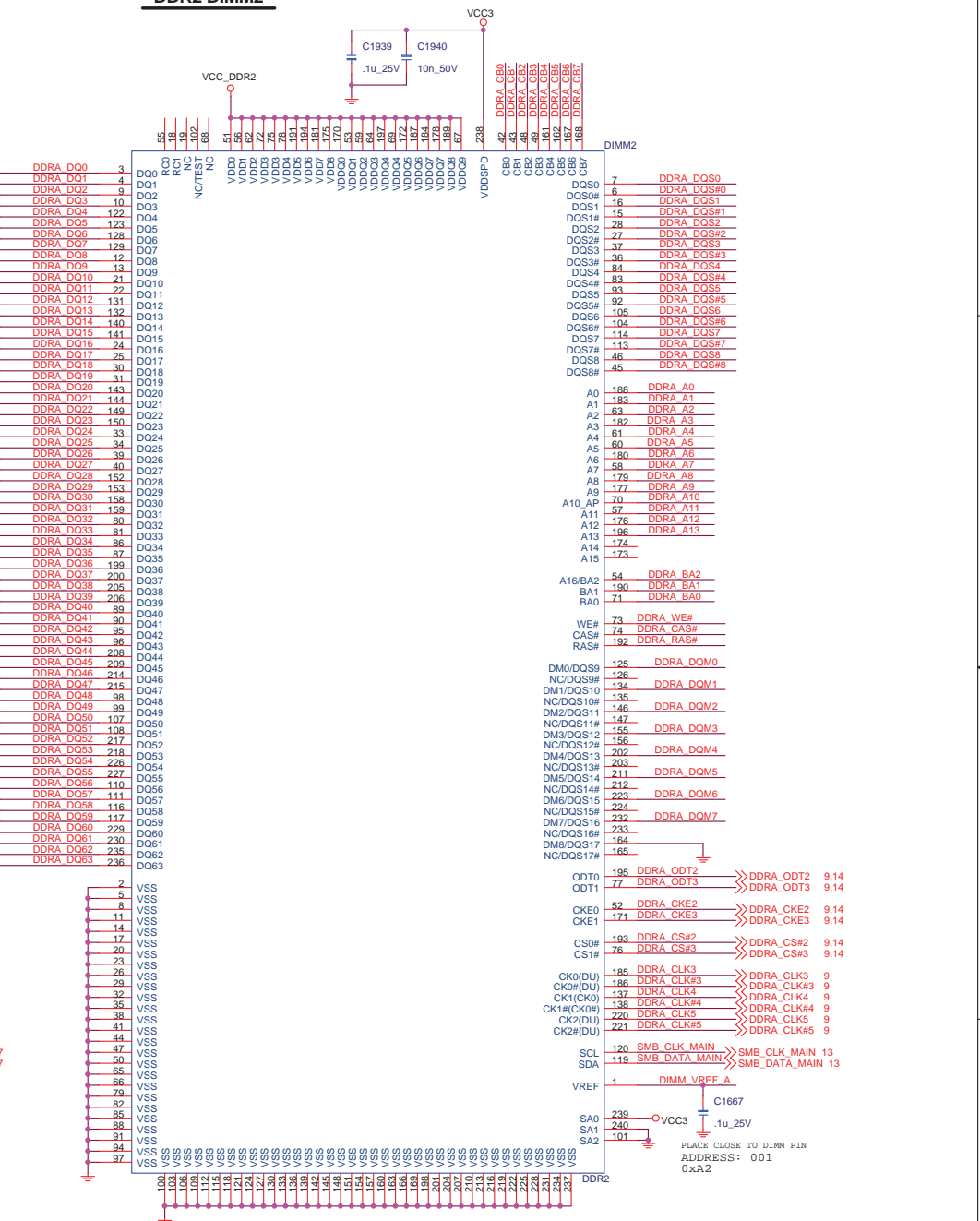
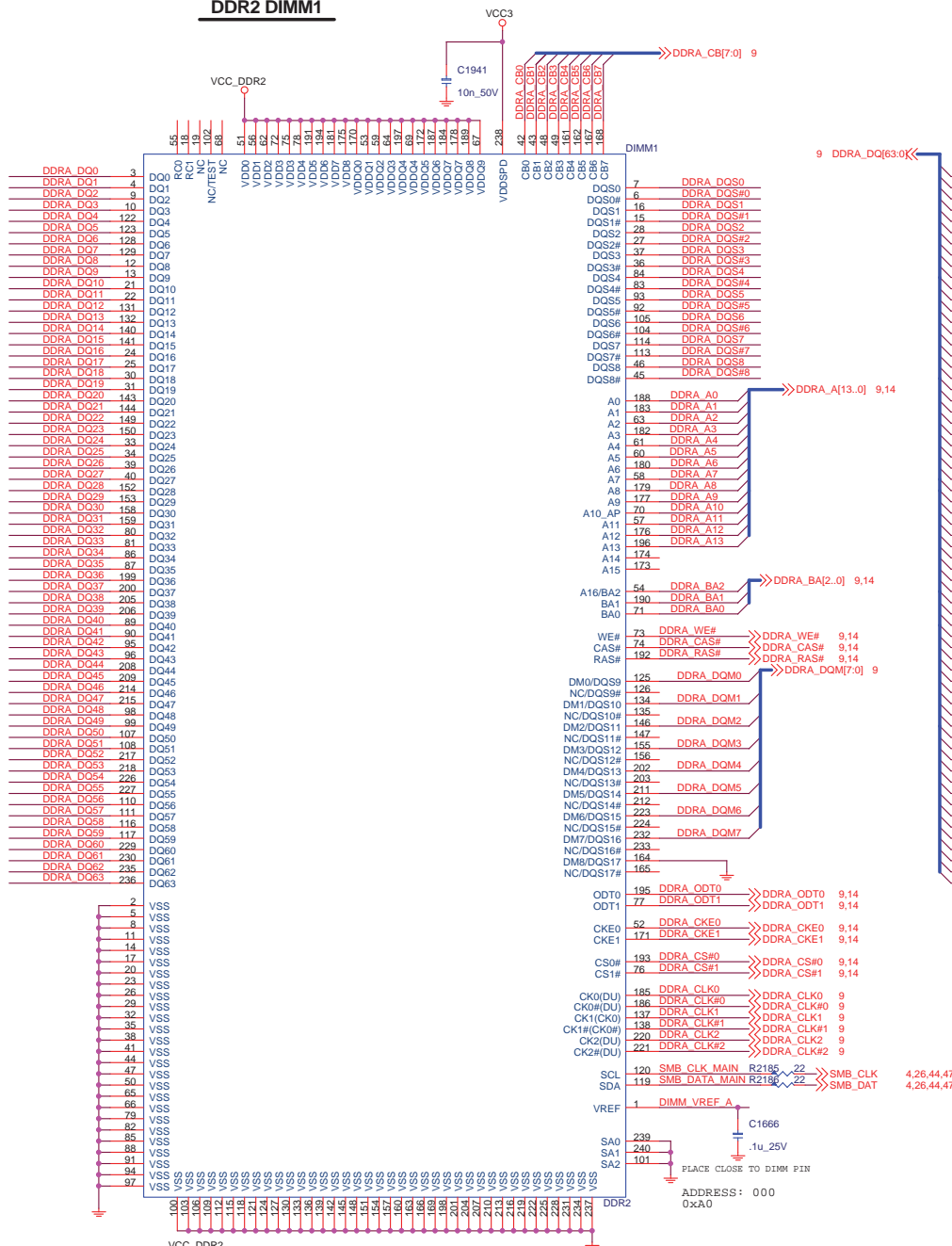
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Glenwood Power/Gnd		
Title		
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DDR2 DIMM1

DDR2 DIMM2



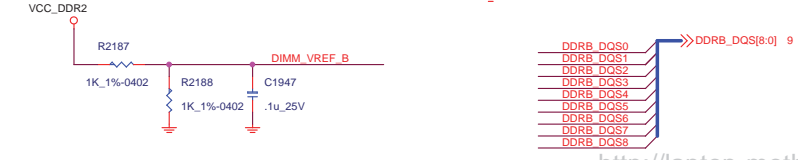
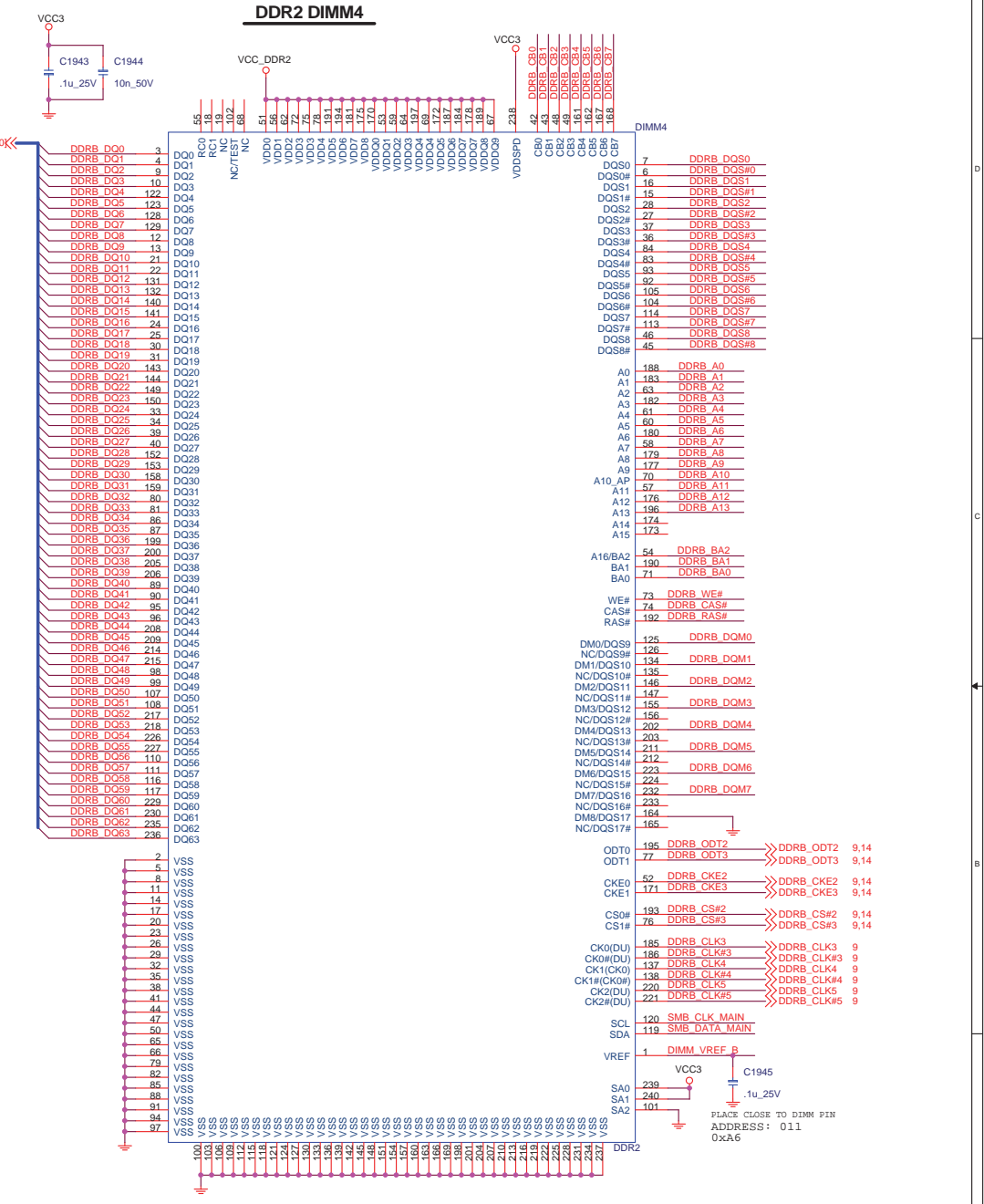
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Title: **DDR II DIMM 1/2**

Size: Document Number
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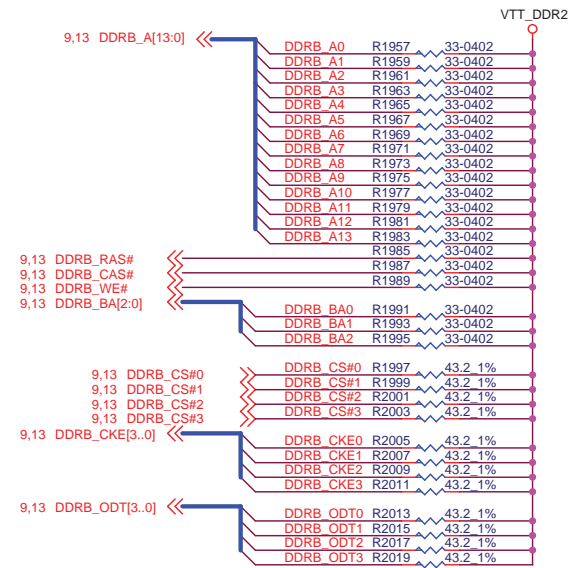
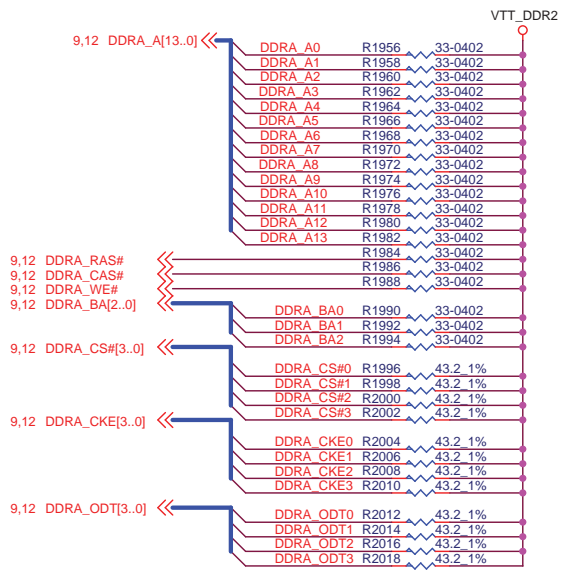
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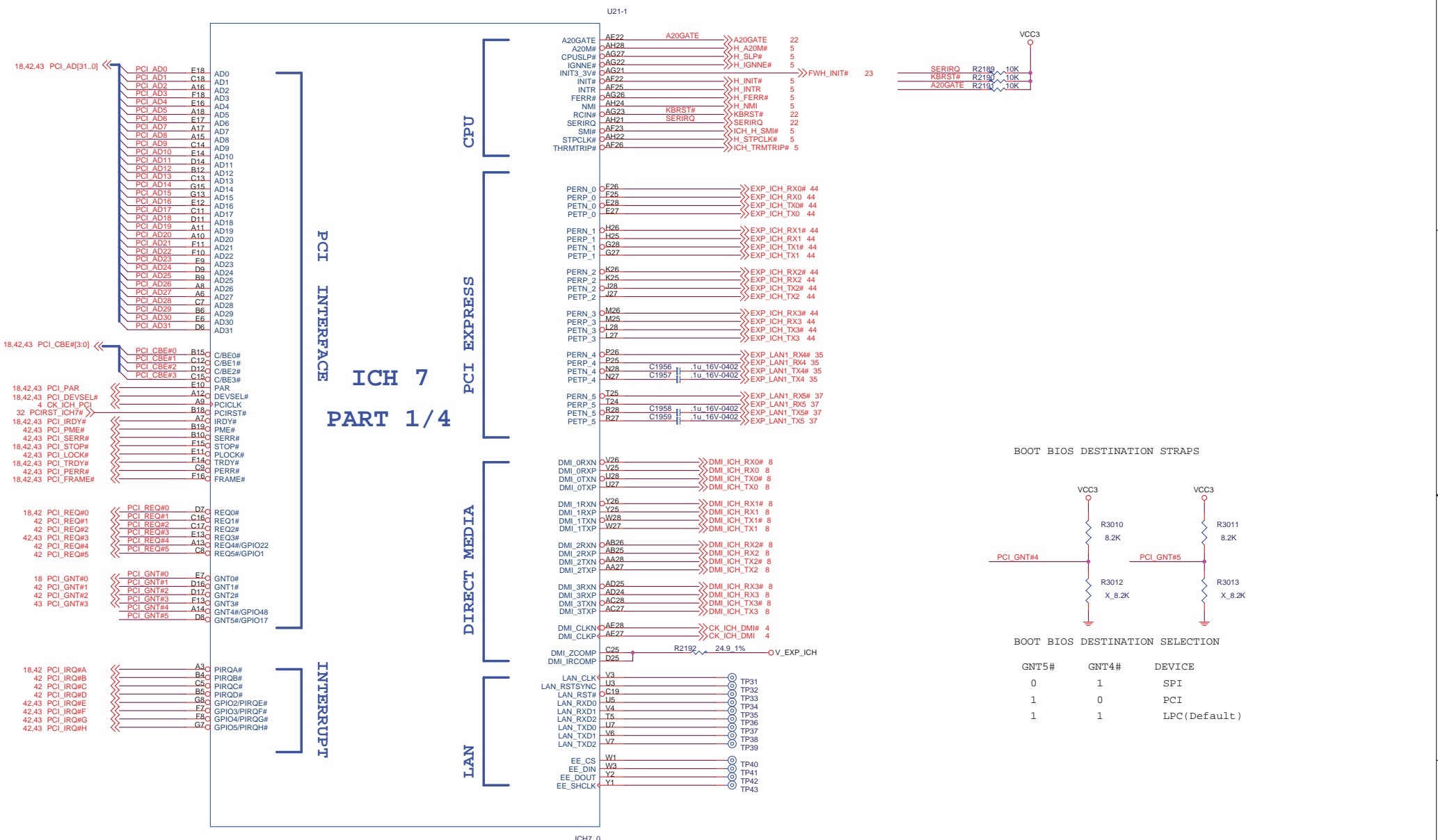
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Size	Document Number	Rev
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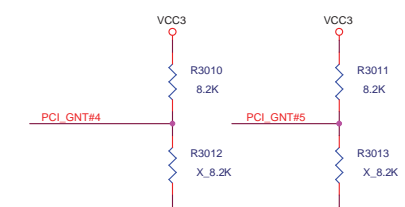
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Title DDR2 Termination		
Size B	Document Number MS-9618	Rev 1A
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**ICH 7
PART 1/4**

BOOT BIOS DESTINATION STRAPS

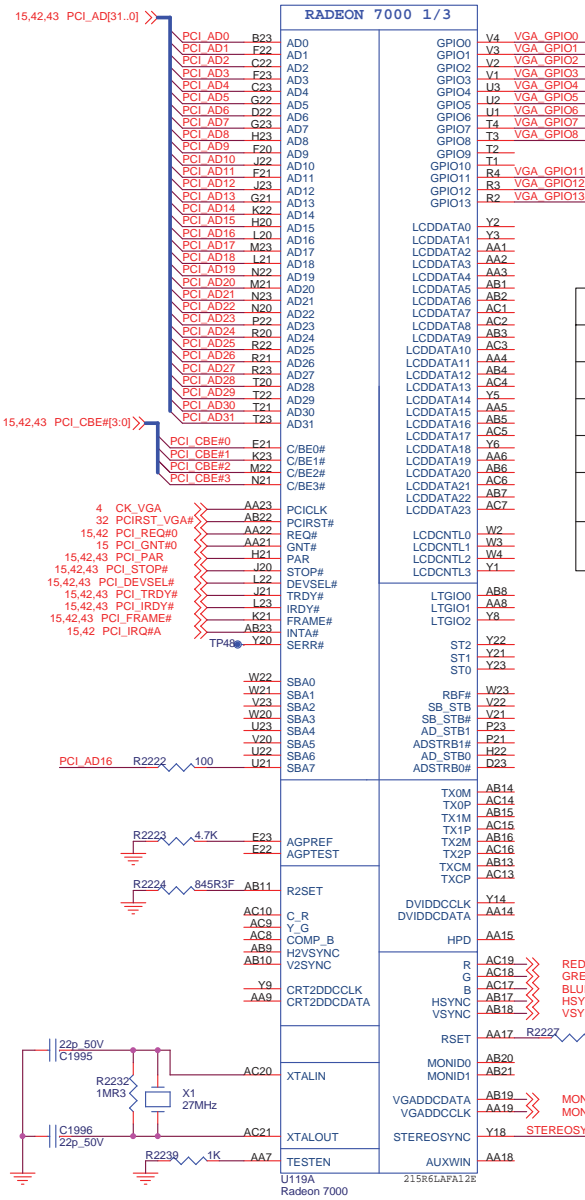
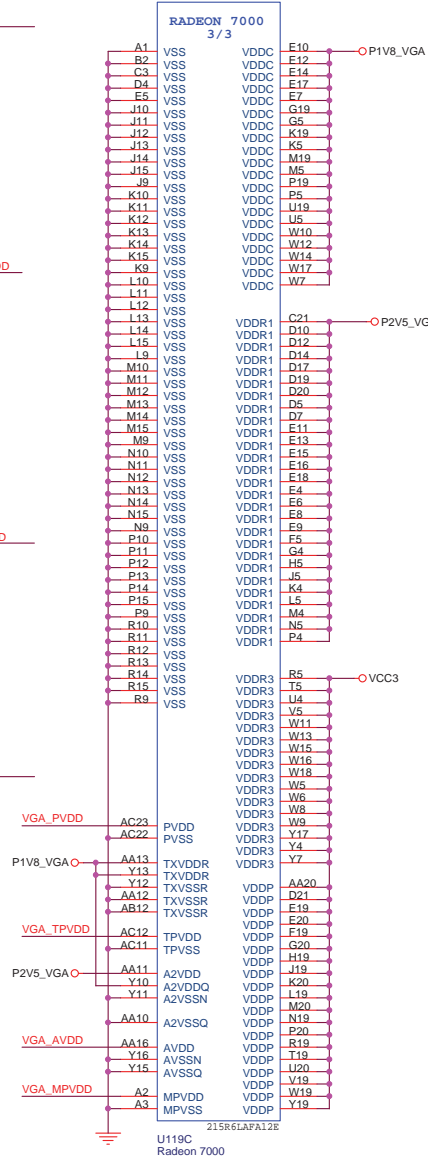
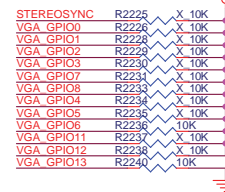
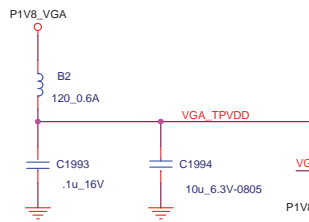
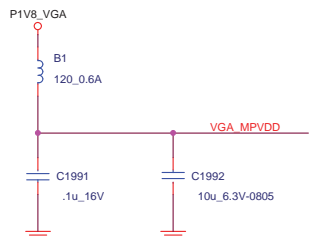
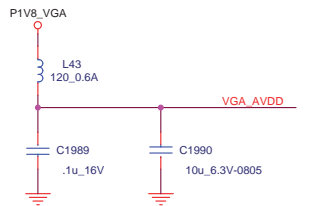
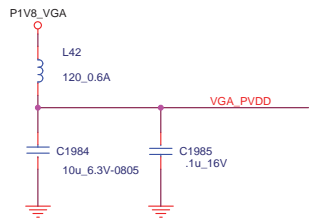


BOOT BIOS DESTINATION SELECTION

GNT5#	GNT4#	DEVICE
0	1	SPI
1	0	PCI
1	1	LPC(Default)

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Title		ICH7-PCI,DMI,CPU,IRQ	
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STEREOSYNC	ENINTB	0 - Enable interrupt (Default) (Internal Pull-Down)
GPIO[1..0]	AGPFBKEW	00 - refclk slightly earlier than feedback (Default) (Internal Pull-Down)
GPIO[3..2]	X1CLK_SKEW	00 - 0 tap delay (Default) (Internal Pull-Down)
GPIO7	VGA_DISABLE	0 - Enabled (Default) (Internal Pull-Down)
GPIO8	ID_DISABLE	0 - Normal Operation (Default) (Internal Pull-Down)
GPIO[6..4]	BUSCFG	100 - PCI 66MHz / 3.3V / REF Clk (Internal Pull-Down / GPIO13 Internal Pull-Up)
GPIO[13..11]	ROMIDCFG	000 - No ROM (Video BIOS integrated into system BIOS) (Internal Pull-Down / GPIO13 Internal Pull-Up)

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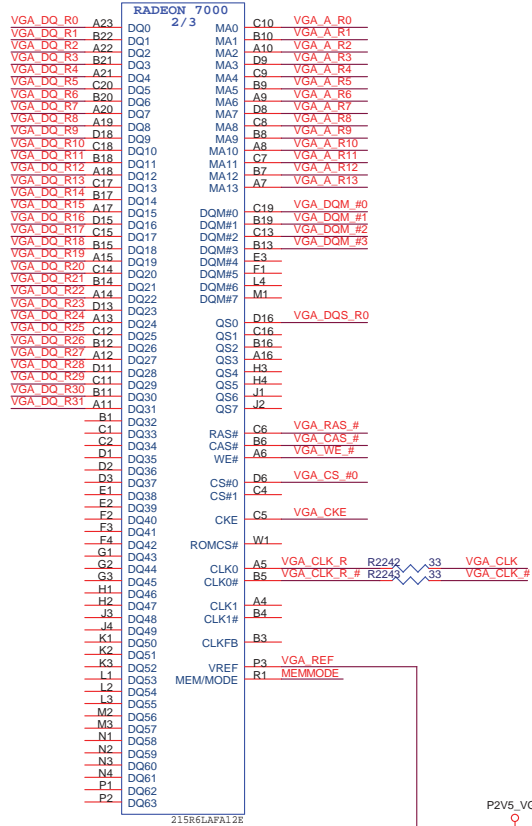
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Size: Document Number
 Custom: **MS-9618**

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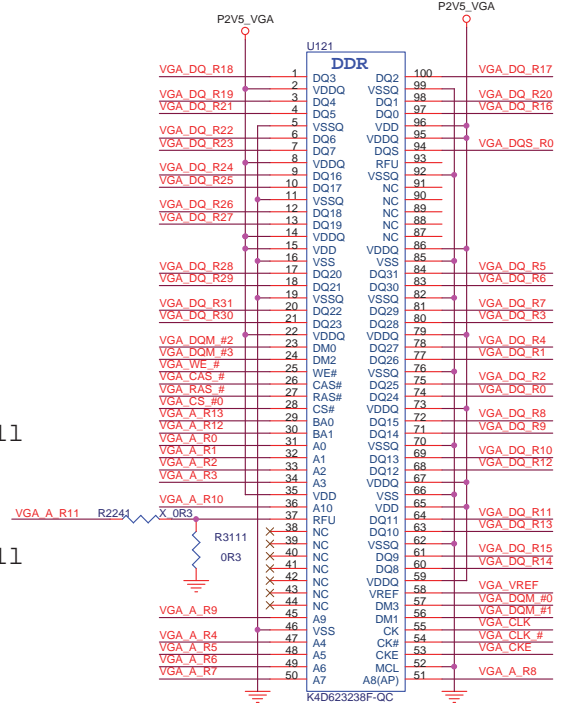
DDR

2X32

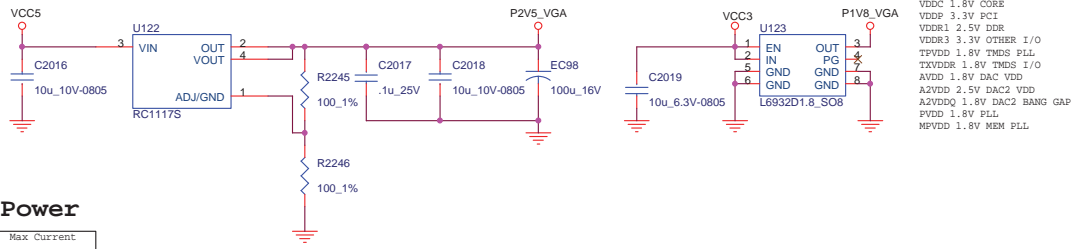


2M*32 R2241 Install
R3111 Uninstall

1M*32 R3111 Install
R2241 Uninstall



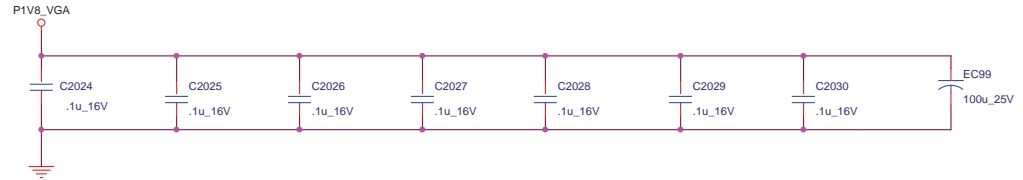
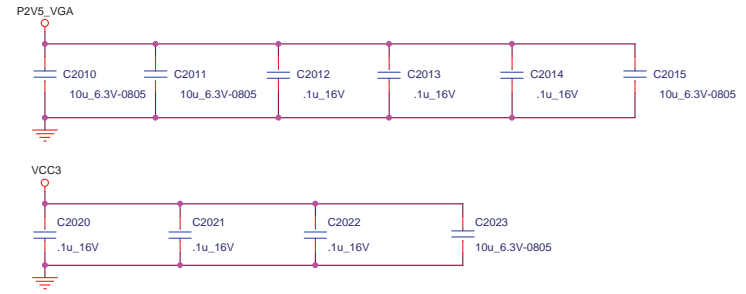
VGA 2.5V Regulator



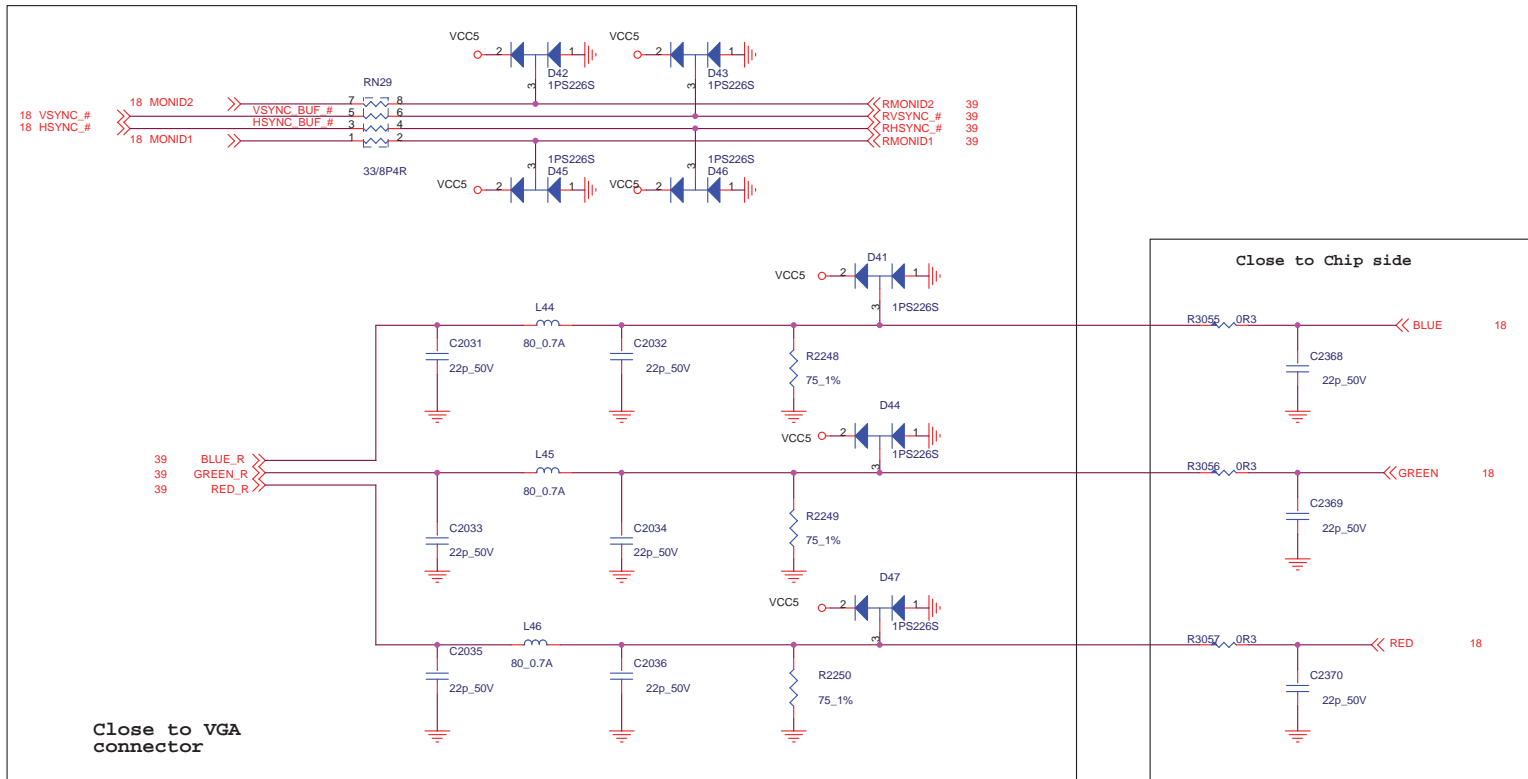
VGA Power

Voltage	Max Current
1.8V	1245mA
2.5V	940mA
3.3V	90mA

VDC 1.8V CORE
 VDDP 3.3V PCI
 VDDR1 2.5V DDR
 VDDR3 3.3V OTHER I/O
 TPVDD 1.8V TMS PLL
 TXVDDR 1.8V TMS I/O
 AVDD 1.8V DAC VDD
 AZVDD 2.5V DAC2 VDD
 AZVDDQ 1.8V DAC2 BANG GAP
 PVDD 1.8V PLL
 MPVDD 1.8V MEM PLL



Video Connector



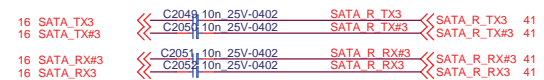
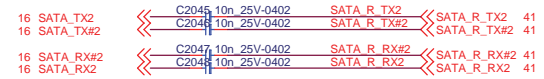
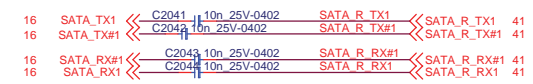
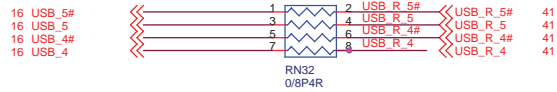
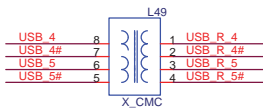
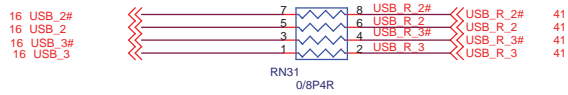
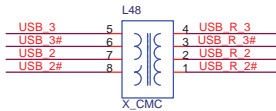
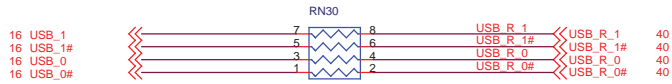
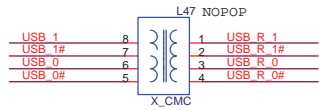
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Title: **VGA_III**

Size: Custom
 Document Number: **MS-9618**

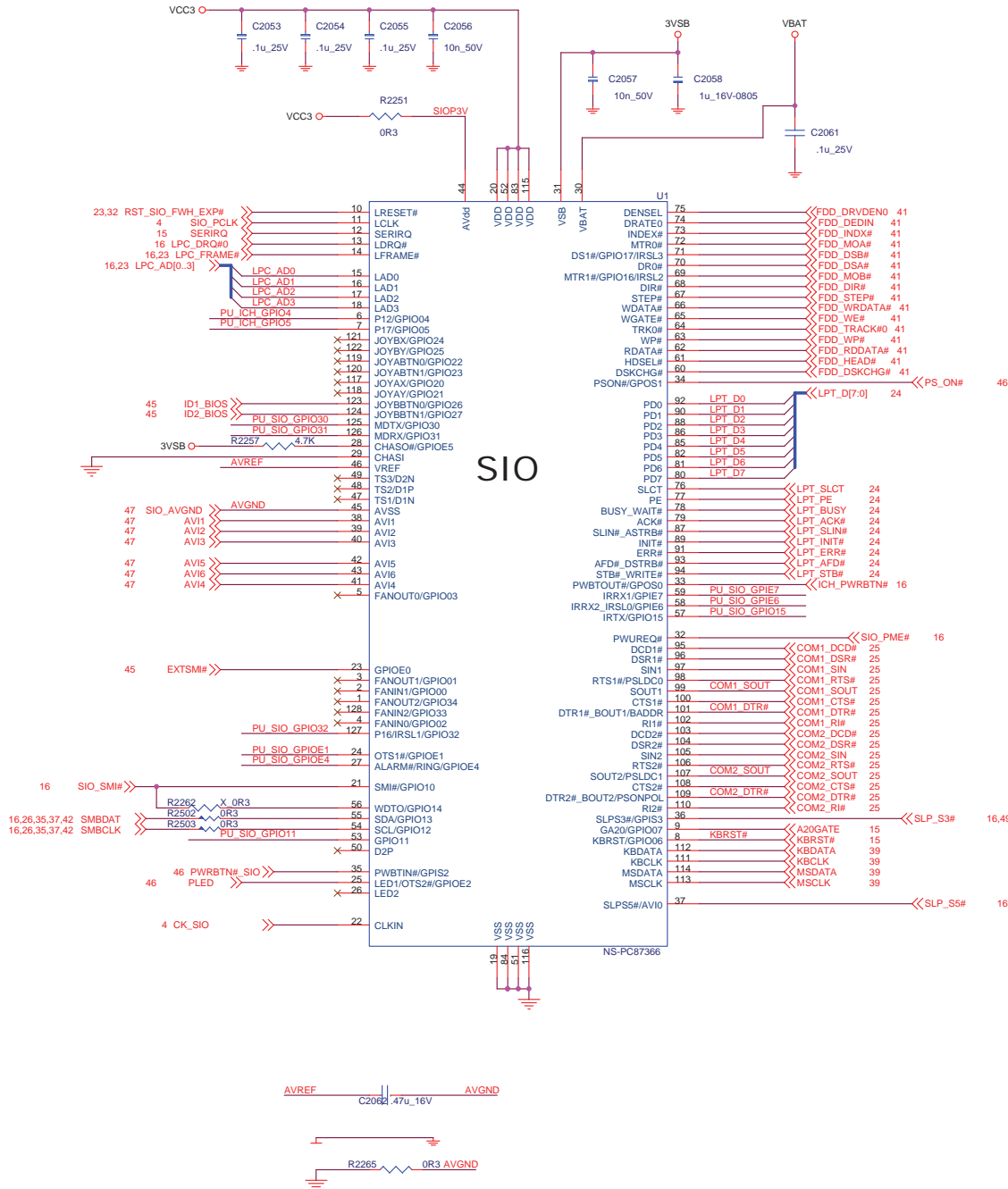
Date: Tuesday, February 01, 2005 Sheet 20 of 51

SerialATA Connector Block

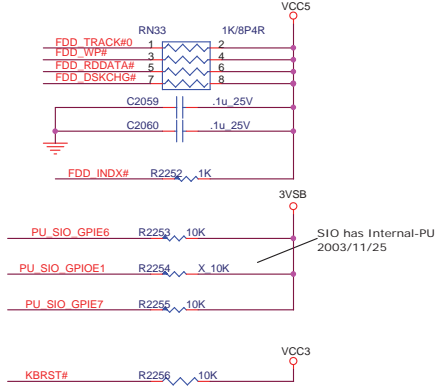


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Title USB2.0/SATA Serial R and C		
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LPC SIO

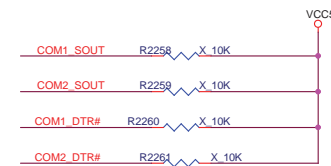


Super IO Pull-Up Resistors

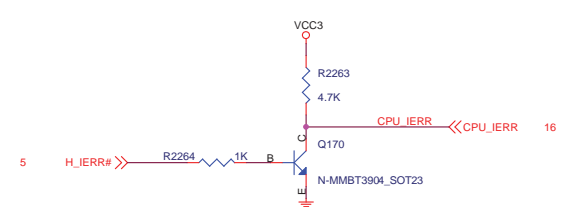


SOUT1	L: PIN 33-35, 37 ,power control function
---	H: PIN 33-35, 37 as GPIO
SOUT2	
DTR1_N	L: BADDR=2E H: BADDR=4E
DTR2_N	L: LOW PWR-ON H: HIGH PWR-ON

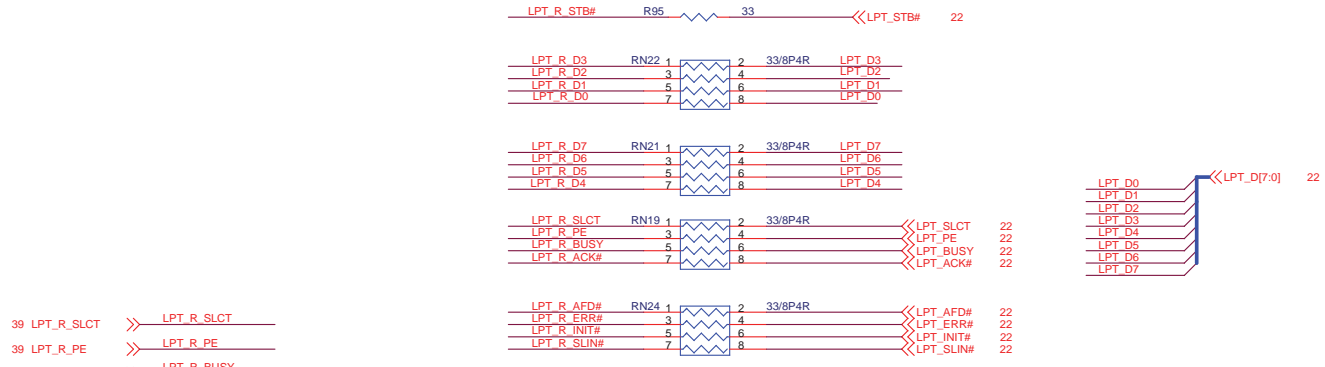
SIO STRAPPING RESISTORS



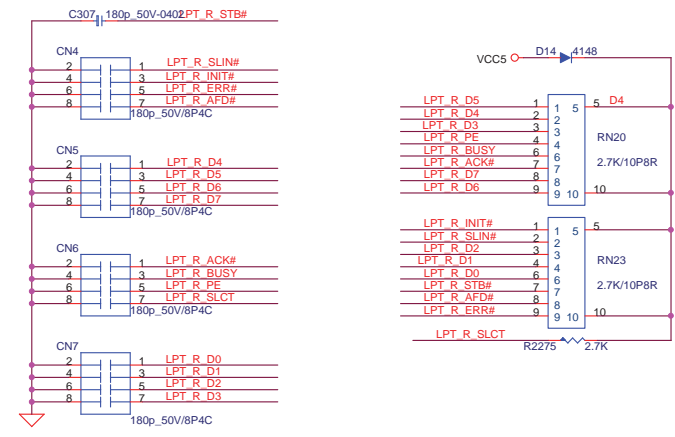
CPU IERR



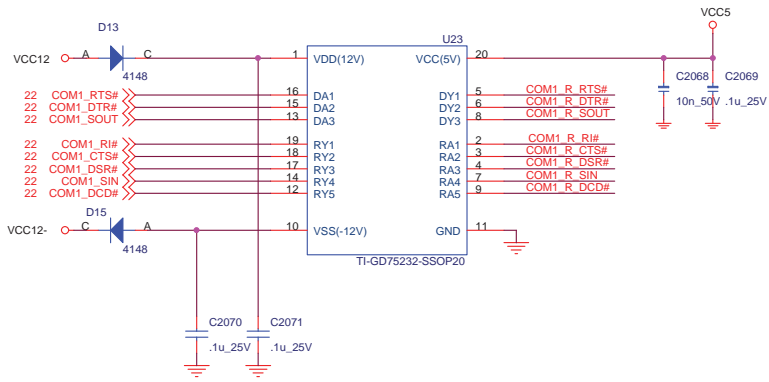
PARALLAL PORT



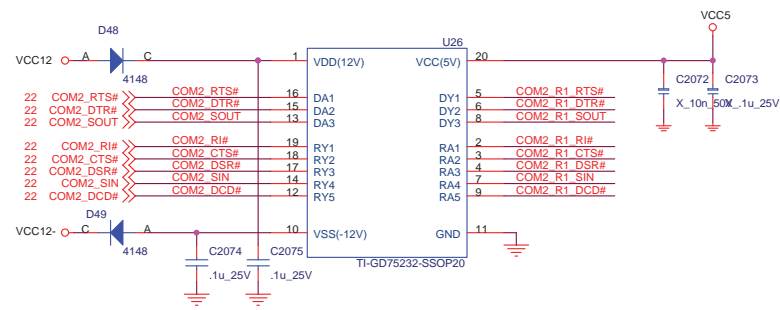
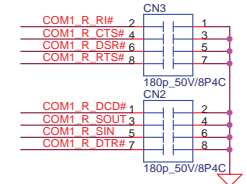
- 39 LPT_R_SLCT >> LPT_R_SLCT
- 39 LPT_R_PE >> LPT_R_PE
- 39 LPT_R_BUSY >> LPT_R_BUSY
- 39 LPT_R_ACK# >> LPT_R_ACK#
- 39 LPT_R_D7 >> LPT_R_D7
- 39 LPT_R_D6 >> LPT_R_D6
- 39 LPT_R_D5 >> LPT_R_D5
- 39 LPT_R_D4 >> LPT_R_D4
- 39 LPT_R_D3 >> LPT_R_D3
- 39 LPT_R_SLIN# >> LPT_R_SLIN#
- 39 LPT_R_D2 >> LPT_R_D2
- 39 LPT_R_INIT# >> LPT_R_INIT#
- 39 LPT_R_D1 >> LPT_R_D1
- 39 LPT_R_ERR# >> LPT_R_ERR#
- 39 LPT_R_D0 >> LPT_R_D0
- 39 LPT_R_AFD# >> LPT_R_AFD#
- 39 LPT_R_STB# >> LPT_R_STB#



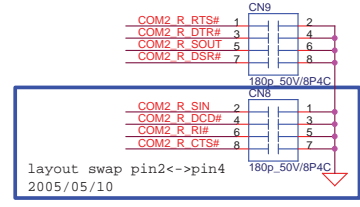
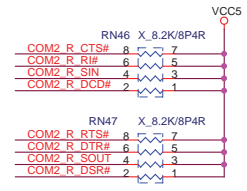
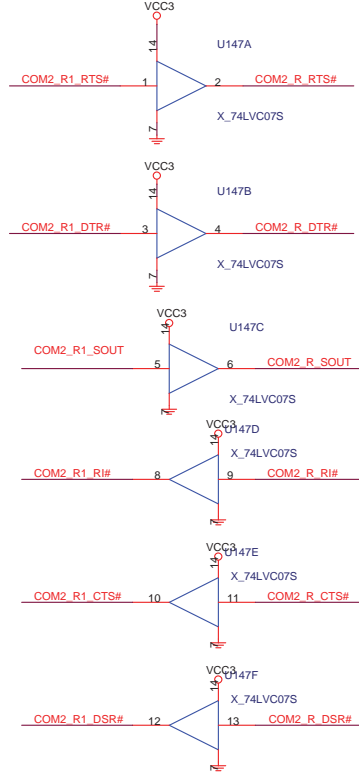
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Title Parallel Serial R and C		
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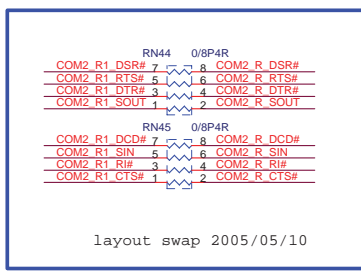
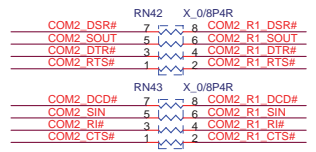
- 39 COM1_R_DCD# << COM1_R_DCD#
- 39 COM1_R_DSR# << COM1_R_DSR#
- 39 COM1_R_SIN << COM1_R_SIN
- 39 COM1_R_RTS# << COM1_R_RTS#
- 39 COM1_R_SOUT << COM1_R_SOUT
- 39 COM1_R_CTS# << COM1_R_CTS#
- 39 COM1_R_DTR# << COM1_R_DTR#
- 39 COM1_R_RI# << COM1_R_RI#



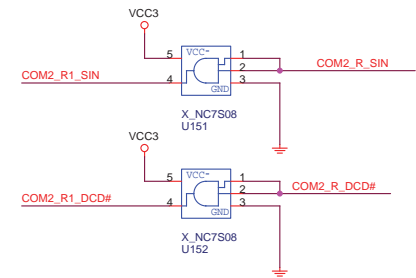
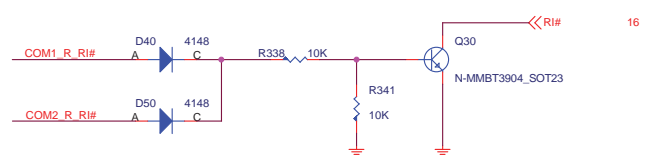
- 39 COM2_R1_DCD# << COM2_R1_DCD#
- 39 COM2_R1_DSR# << COM2_R1_DSR#
- 39 COM2_R1_SIN << COM2_R1_SIN
- 39 COM2_R1_RTS# << COM2_R1_RTS#
- 39 COM2_R1_SOUT << COM2_R1_SOUT
- 39 COM2_R1_CTS# << COM2_R1_CTS#
- 39 COM2_R1_DTR# << COM2_R1_DTR#
- 39 COM2_R1_RI# << COM2_R1_RI#



- COM2_R_DCD# << COM2_R_DCD# 45
- COM2_R_DSR# << COM2_R_DSR# 45
- COM2_R_SIN << COM2_R_SIN 45
- COM2_R_RTS# << COM2_R_RTS# 45
- COM2_R_SOUT << COM2_R_SOUT 45
- COM2_R_CTS# << COM2_R_CTS# 45
- COM2_R_DTR# << COM2_R_DTR# 45
- COM2_R_RI# << COM2_R_RI# 45



WAKE UP ON RING

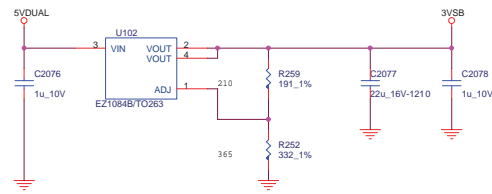
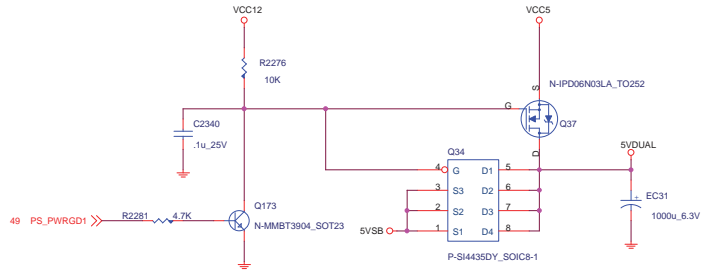
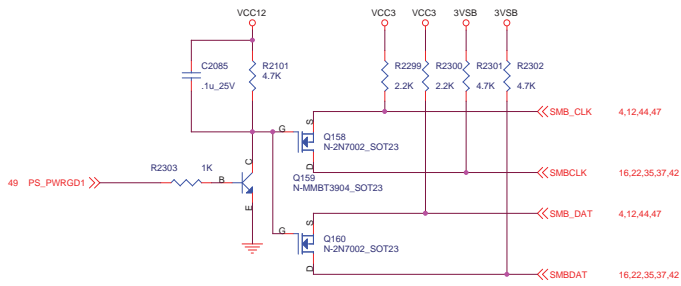


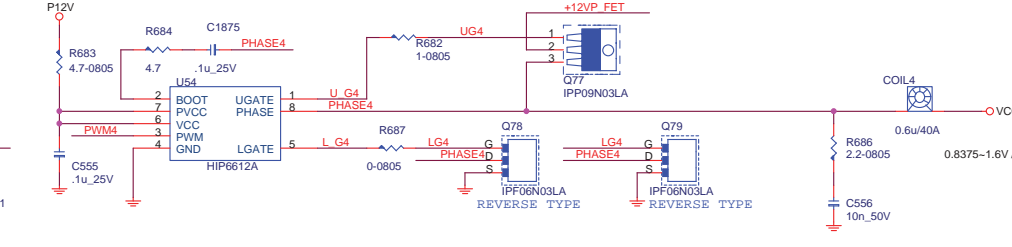
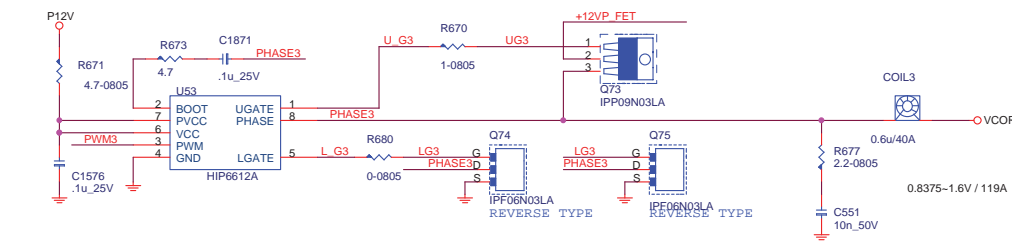
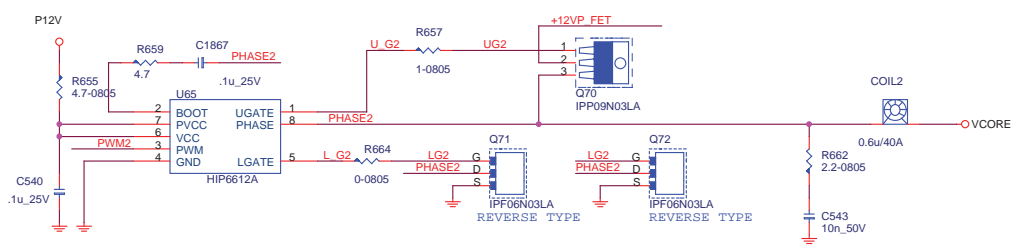
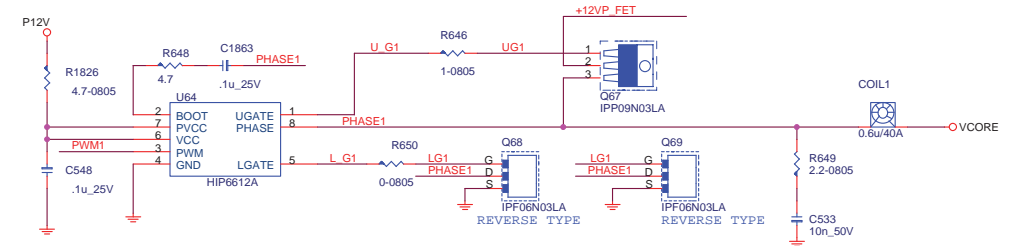
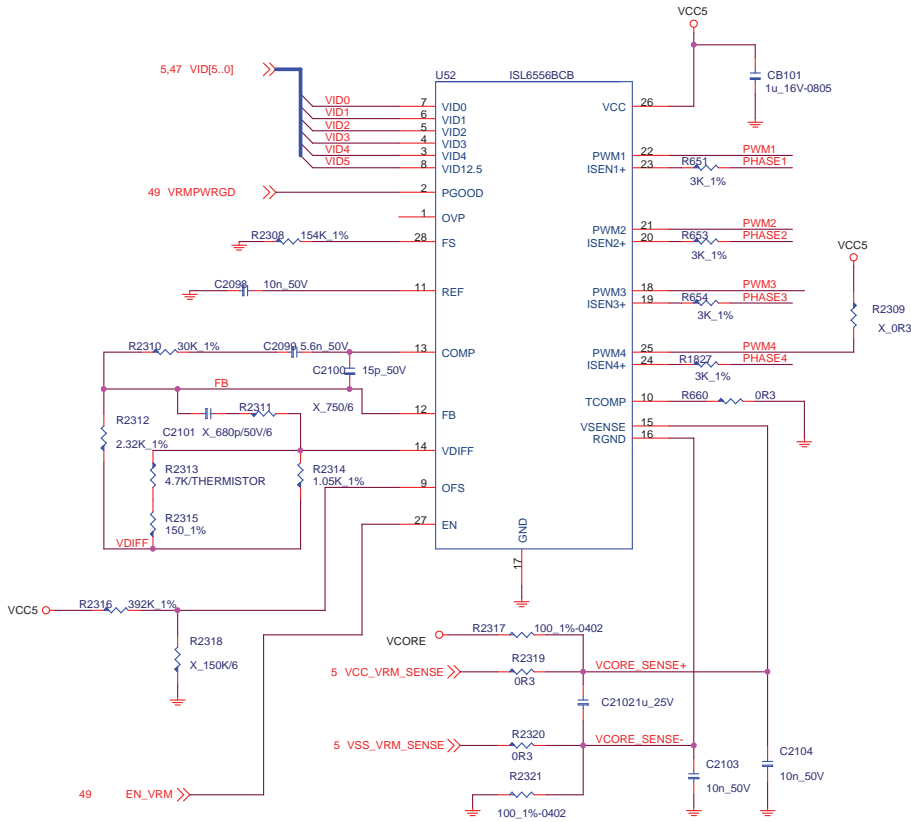
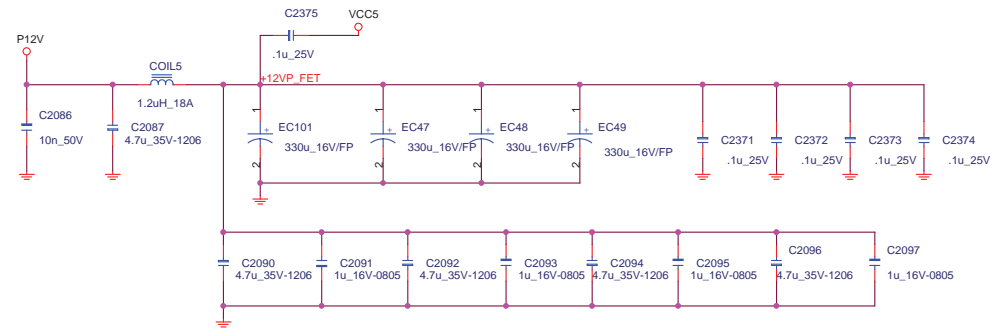
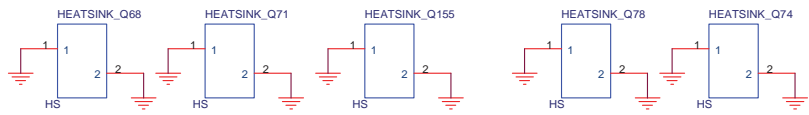
Reserved for 5V COM port device

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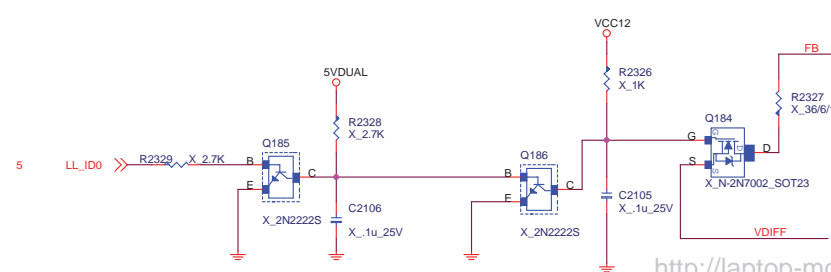
Title COM PORT		
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5V Dual Power Switching





CHECK THIS! CONNECT TO BULK CAPACITOR

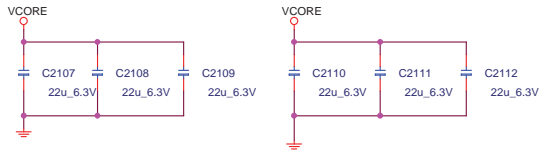


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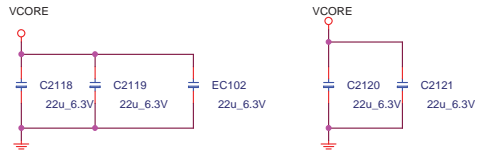
Micro-Star Int'l Co., Ltd.
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Title VRM - ISL6556B		
Size Custom	Document Number MS-9618	Rev 1A
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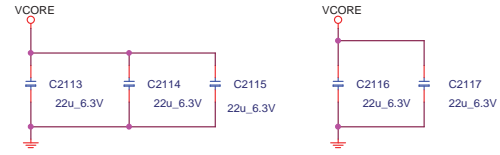
CPU DECOUPLING CAPACITORS



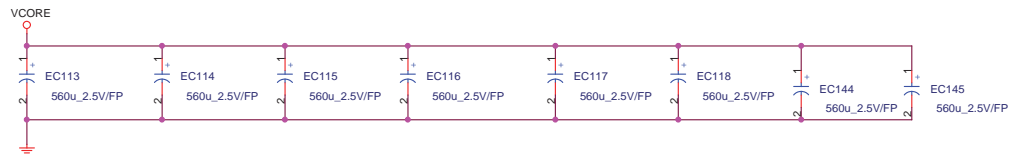
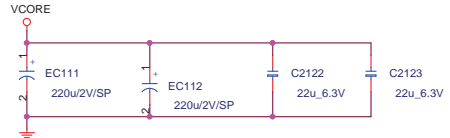
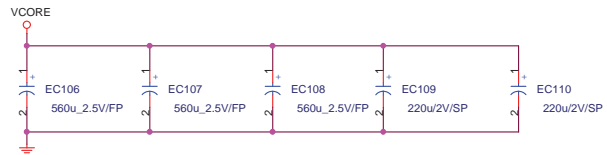
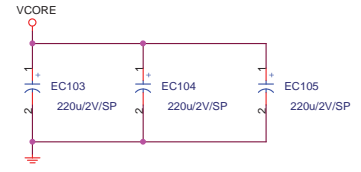
Place these caps within socket cavity



Place these caps within north side of processor

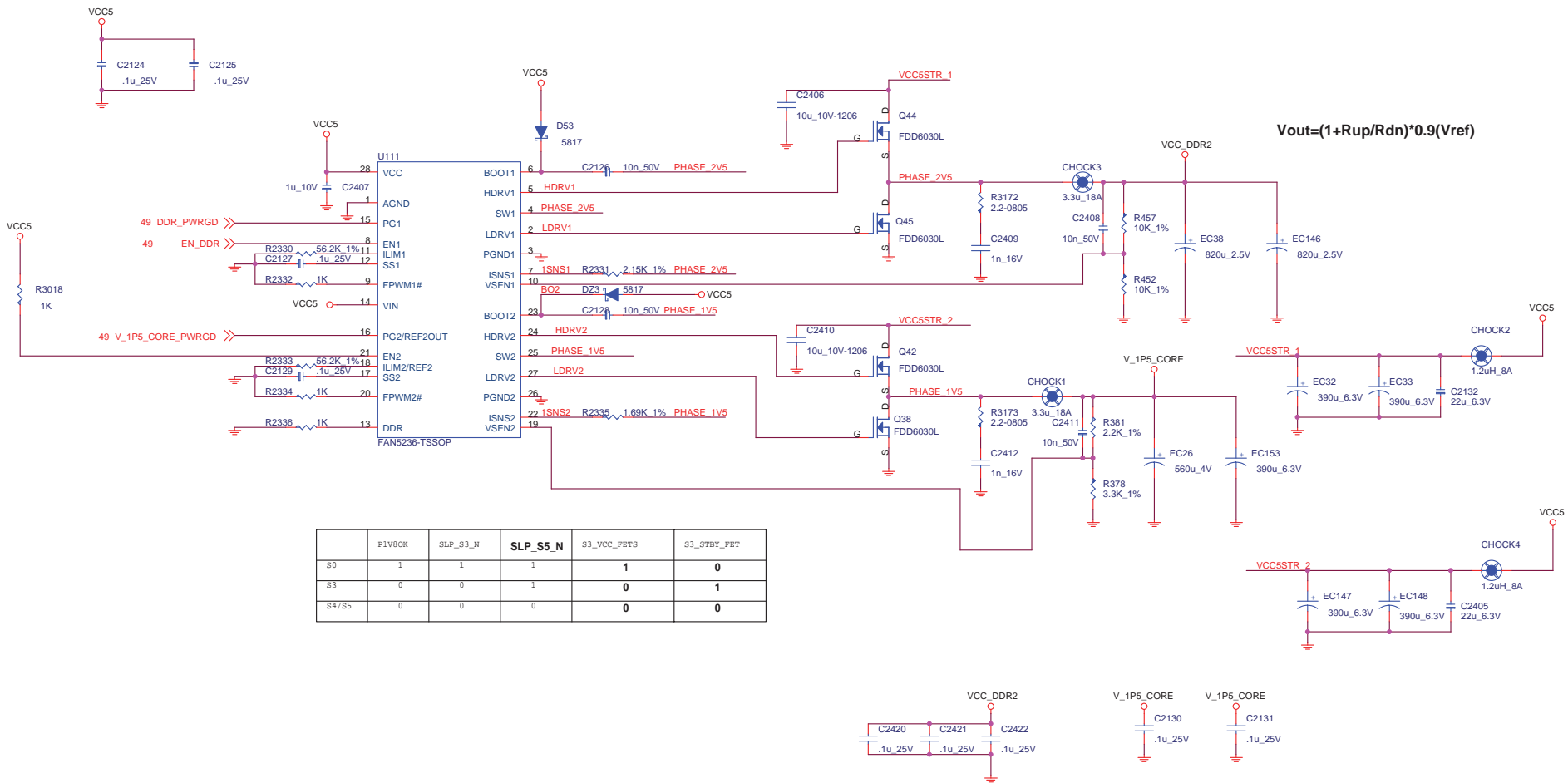


Place these caps within south side of processor



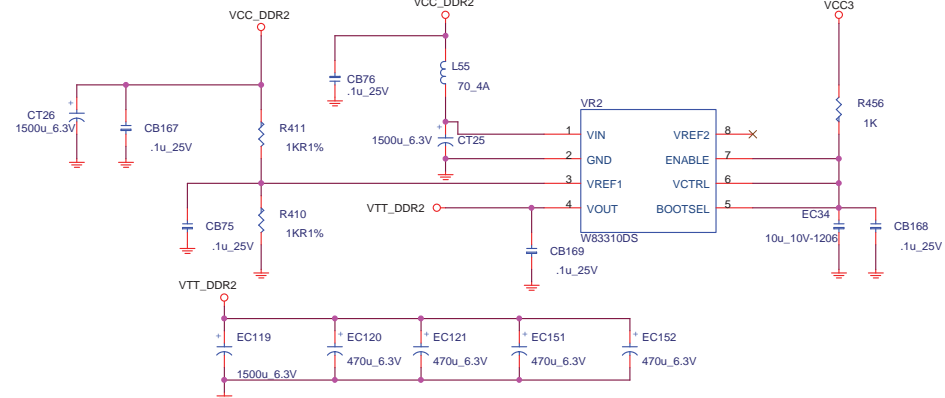
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VRM Decoupling		
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	P1V8OK	SLP_S3_N	SLP_S5_N	S3_VCC_FFTS	S3_STBY_FFT
S0	1	1	1	1	0
S3	0	0	1	0	1
S4/S5	0	0	0	0	0

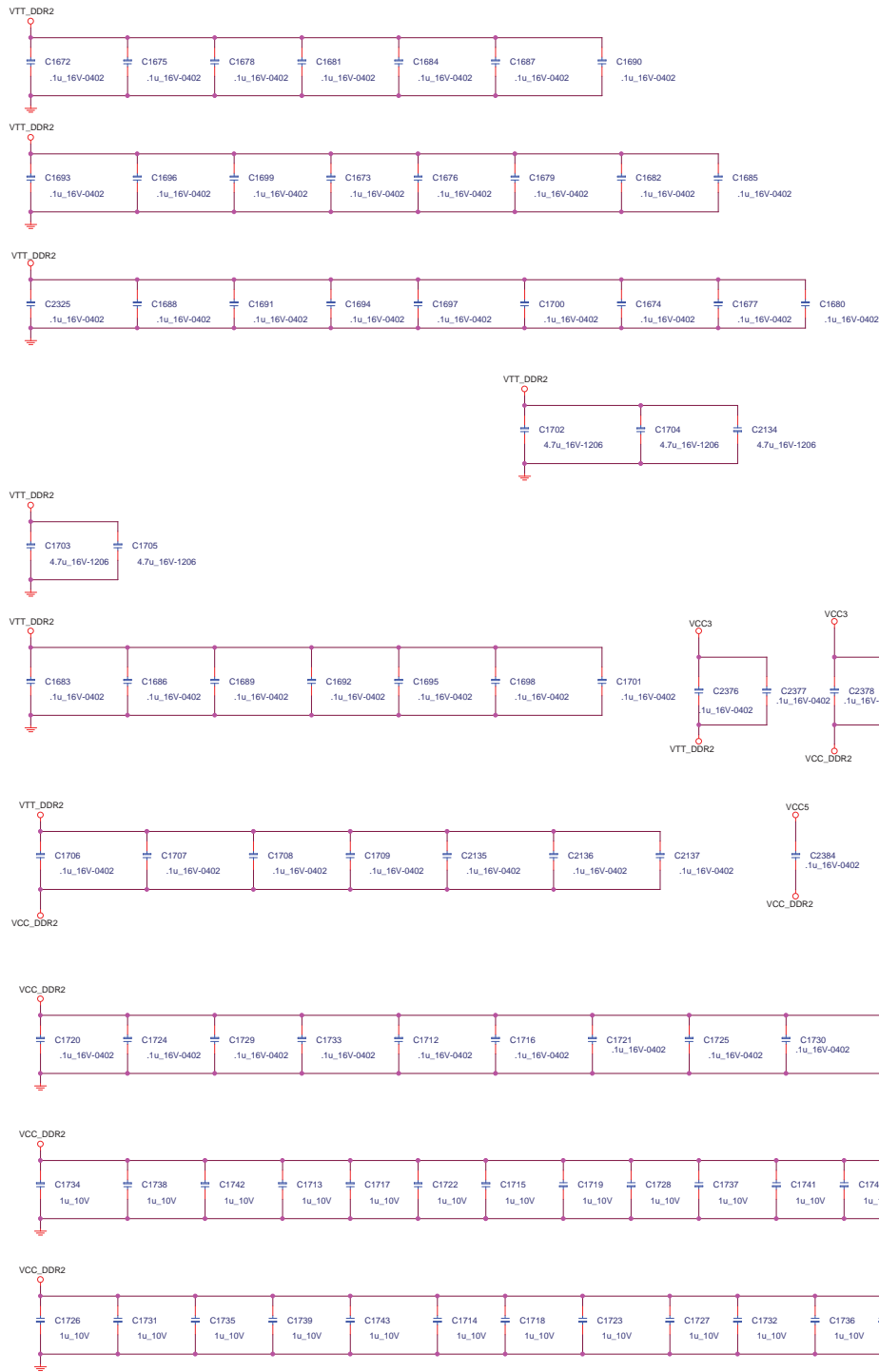
VTT_DDR2 Voltage Supplier



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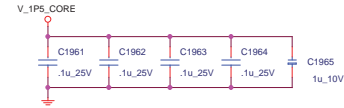
Title: **DDR2 Power**

Size: Custom
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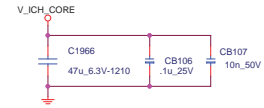


ICH Decoupling

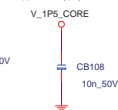
Decoupling Requirements for ICH7, USB, SATA



Decoupling Requirements for ICH7 CORE



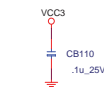
Decoupling Requirements for USBPLL (C1)



Decoupling Requirements for USB2.0



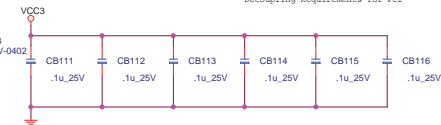
Decoupling Requirements for IDE



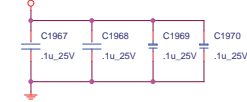
Decoupling Requirements for AUDIO, SATA, PCI EXPRESS



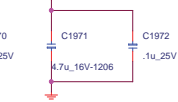
Decoupling Requirements for PCI



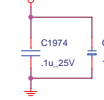
3VSB



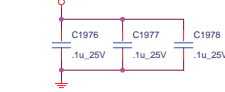
V_FSB_VTT

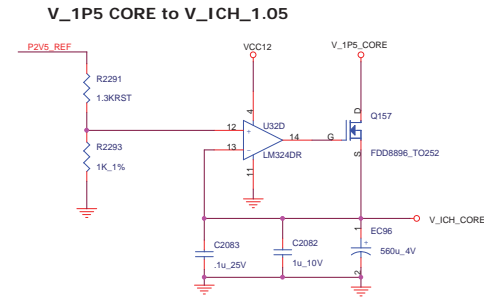
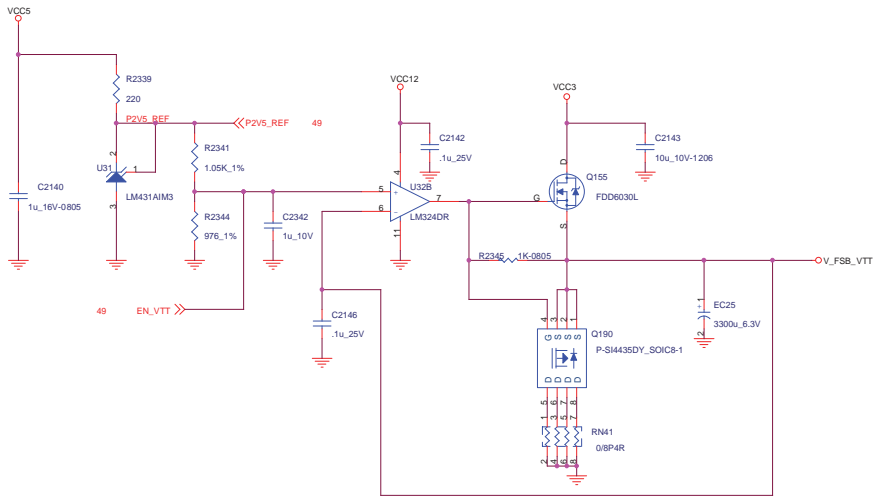


VBAT



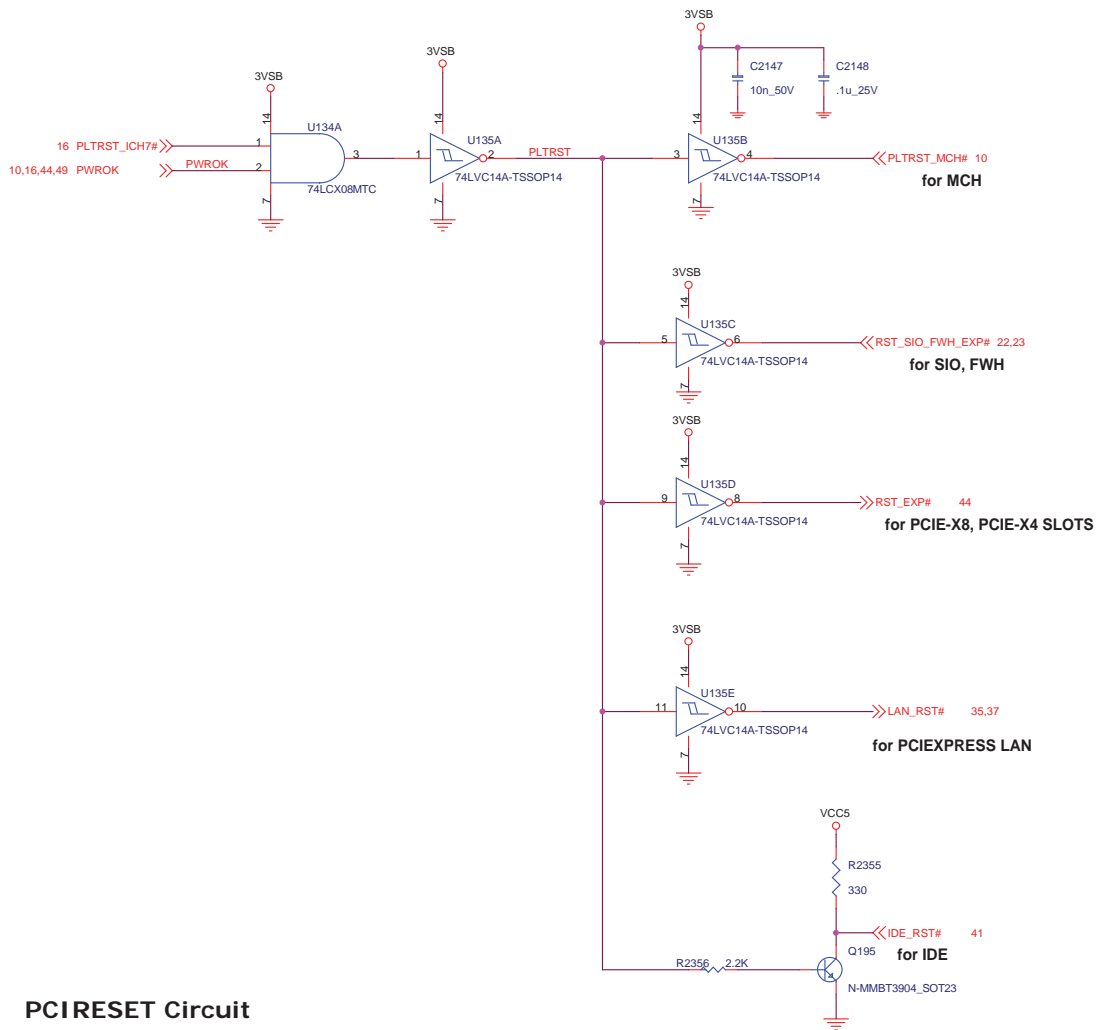
V_EXP_ICH



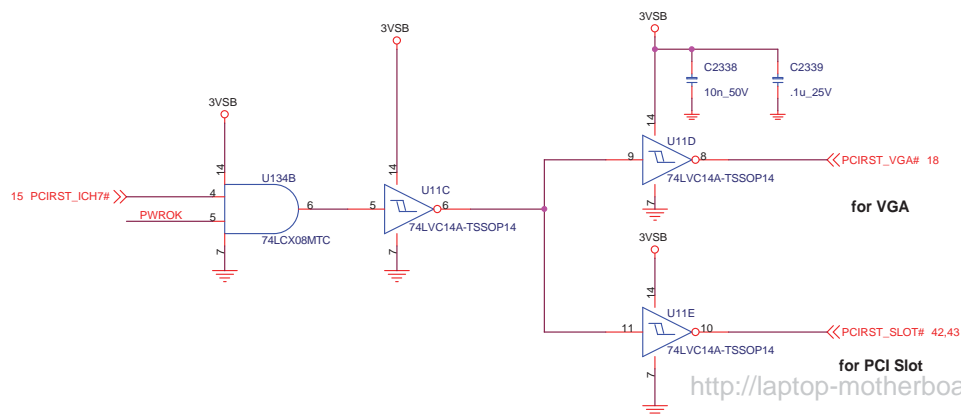


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Title		
V_FSB_VTT		
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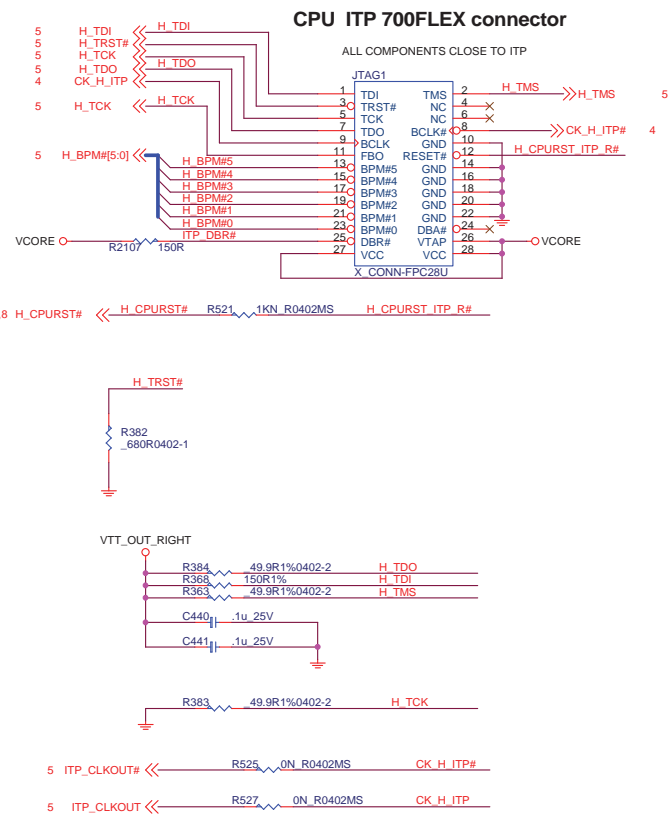
PLTRESET Circuit



PCIRESET Circuit



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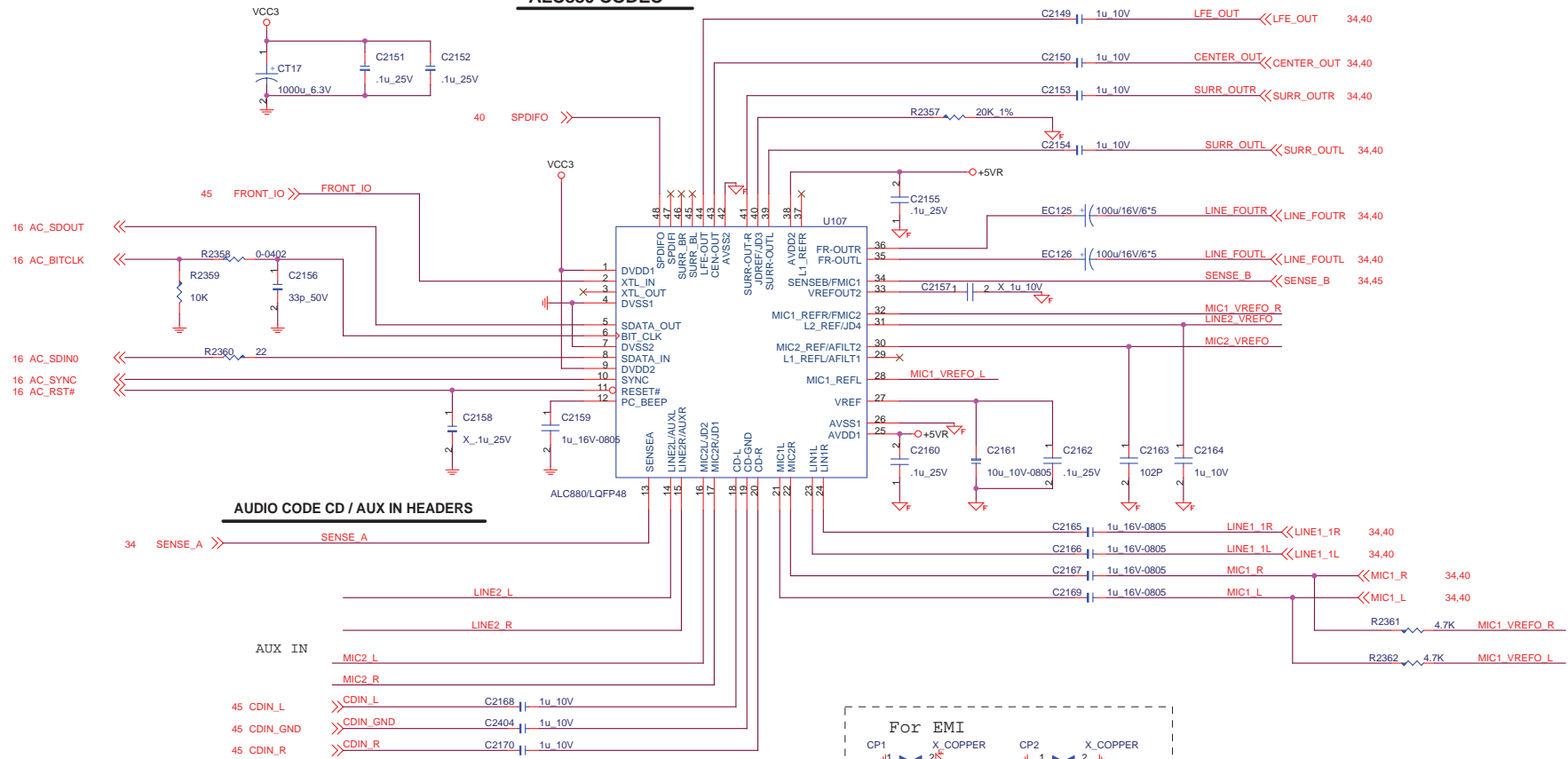


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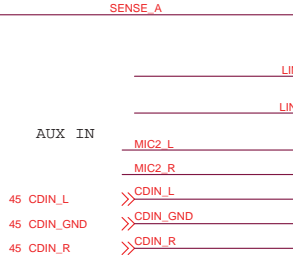
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Title		PCI Reset
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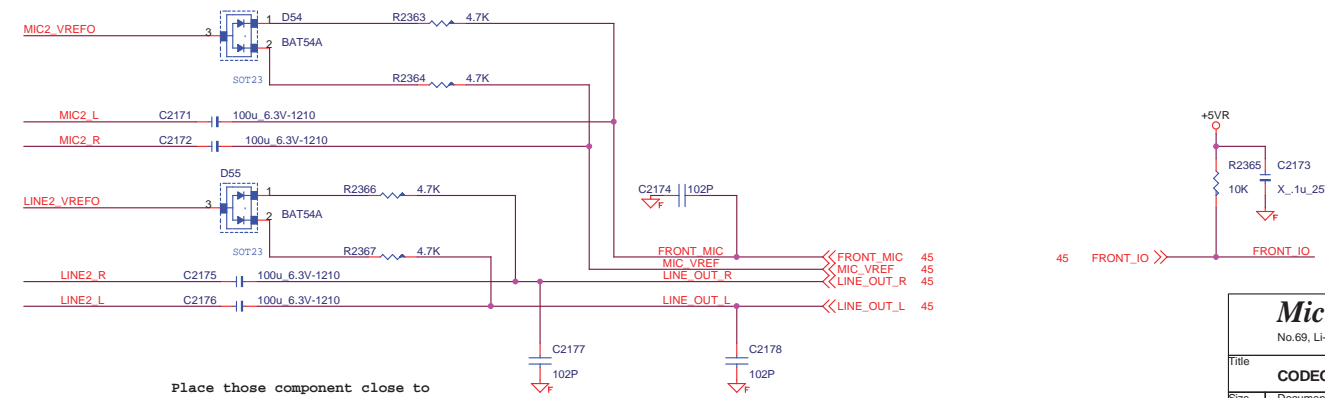
ALC880 CODEC



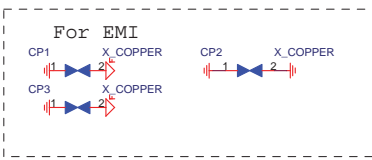
AUDIO CODE CD / AUX IN HEADERS



Speaker Out Decoupling



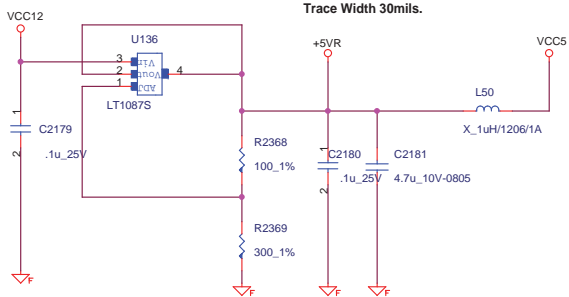
Place those component close to audio connector.



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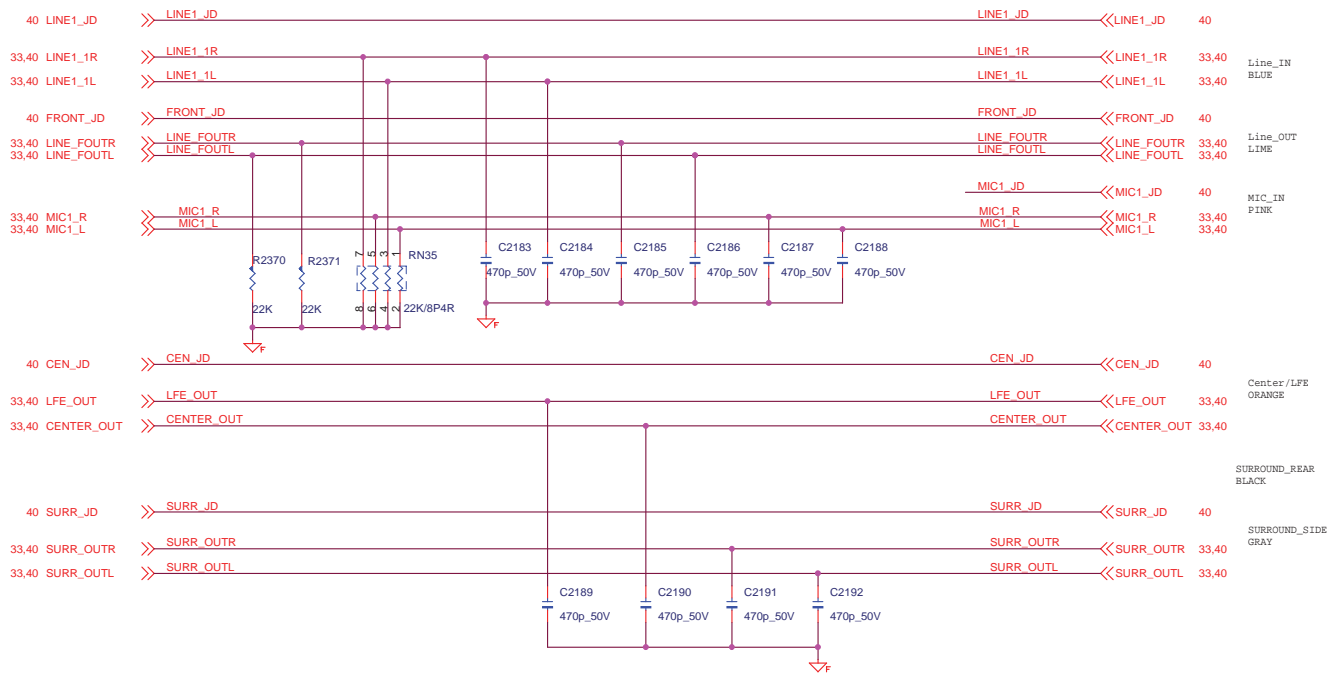
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No.69, Li-De St., Jung-He City, Taipei Hsien, Taiwan. http://www.msi.com.tw		
Title CODEC(ALC880_I)		
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AUDIO CODE REGULATORS

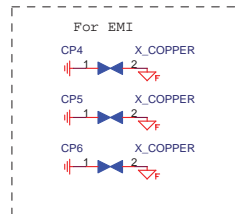
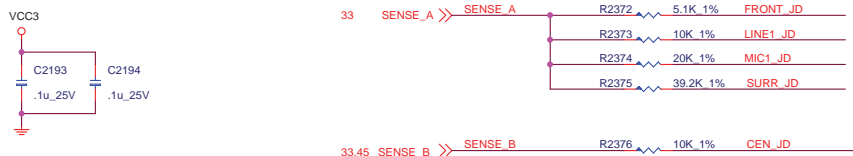


Rear audio jack

ALC880 JACK

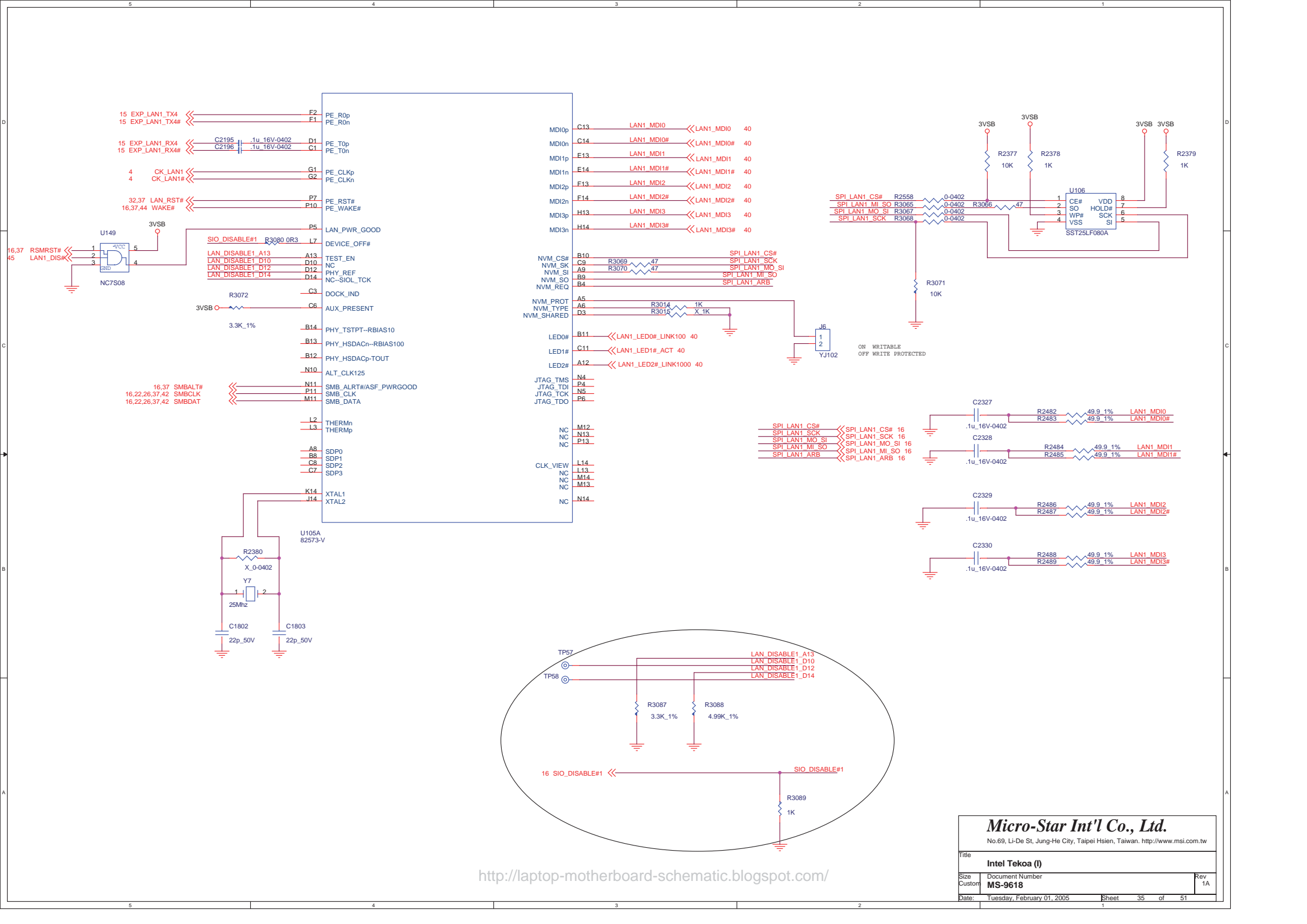


ALC880 JACK DETECT



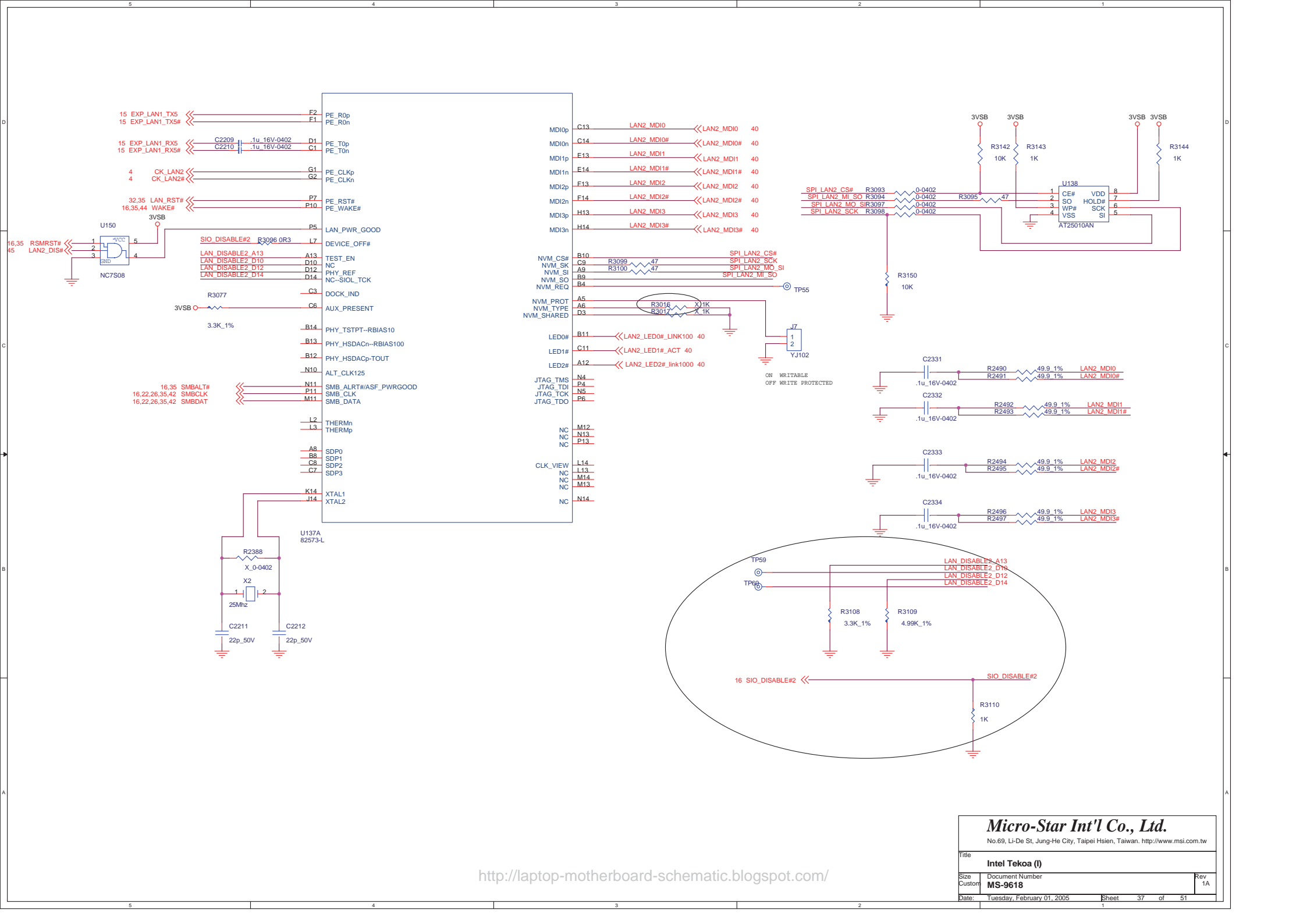
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Title		CODEC(ALC880)_ (II)	
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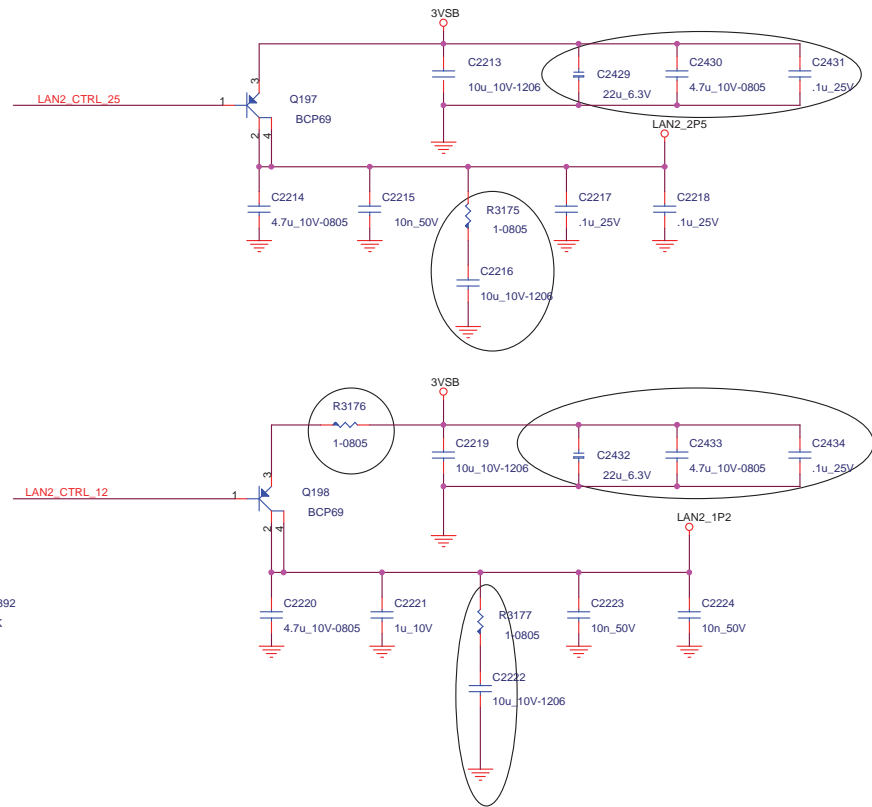
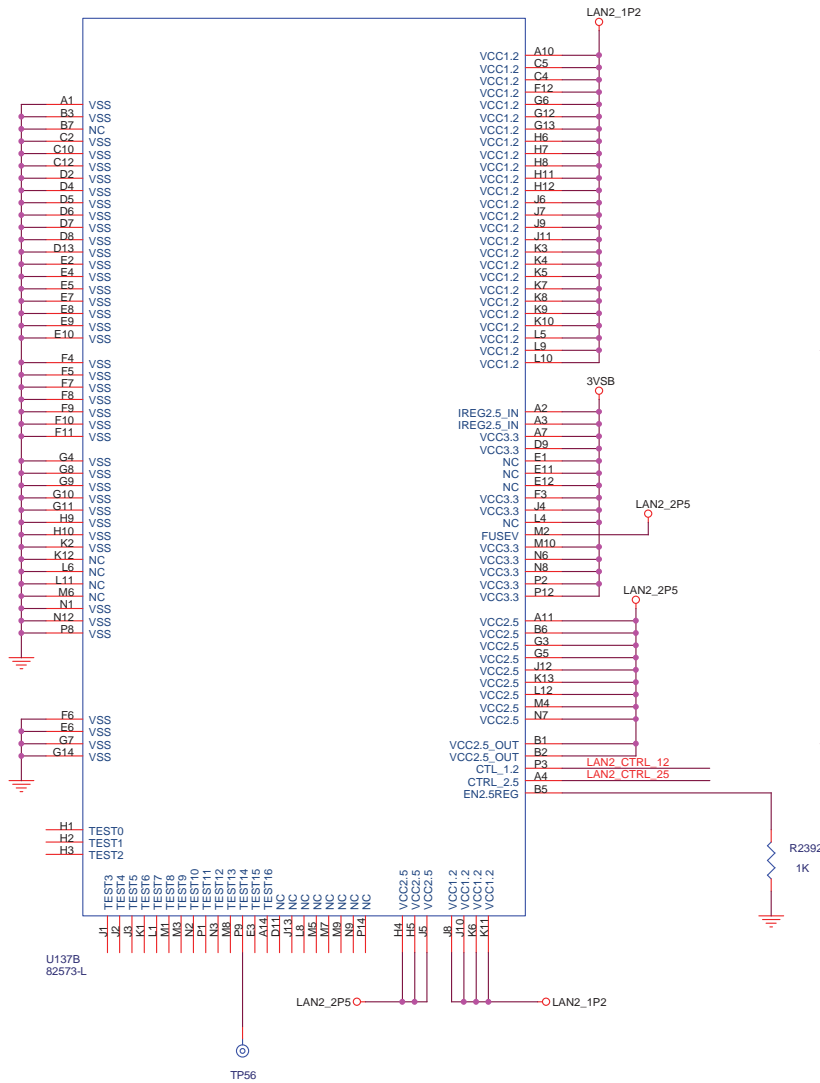


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Title		Intel Tekoa (I)
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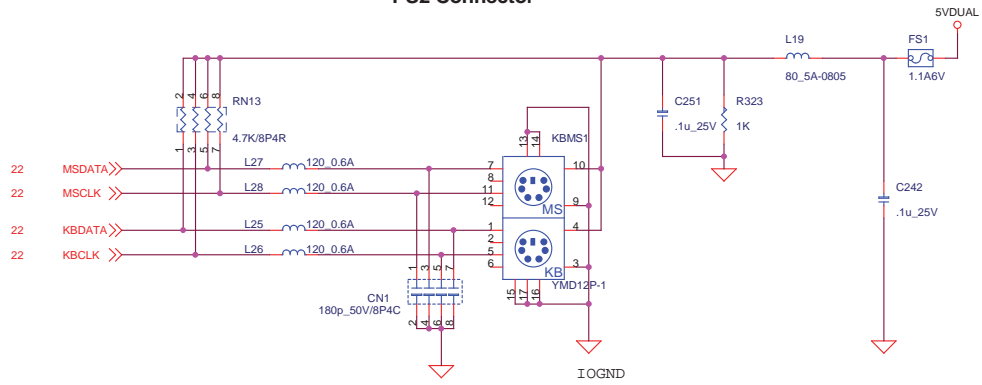
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Title: Intel Tekoa (I)	
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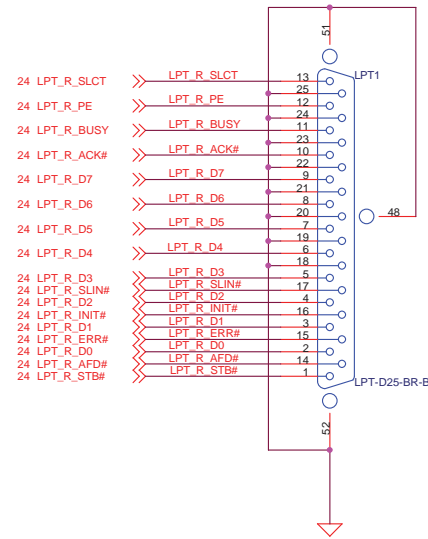
<http://laptop-motherboard-schematic.blogspot.com/>

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Title		
Intek Tekoa (II)		
Size	Document Number	
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		Rev 1A

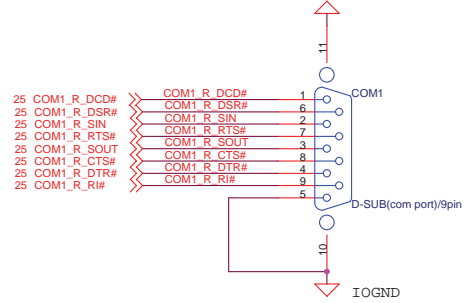
PS2 Connector



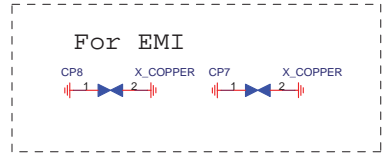
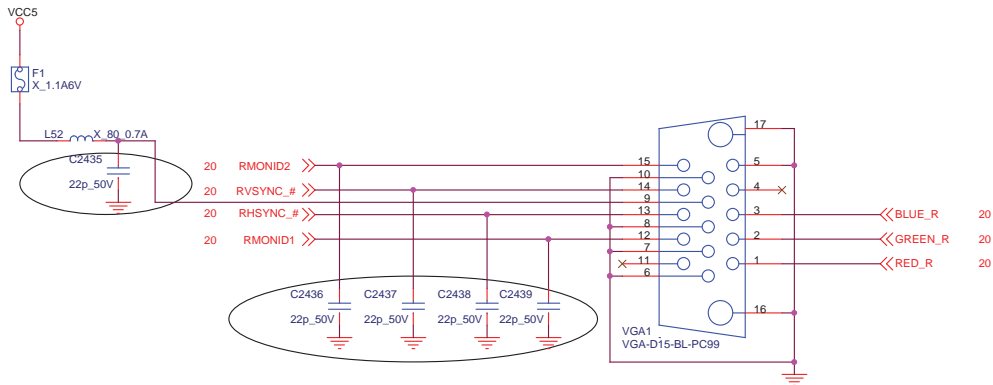
PARALLEL PORT



COM PORT

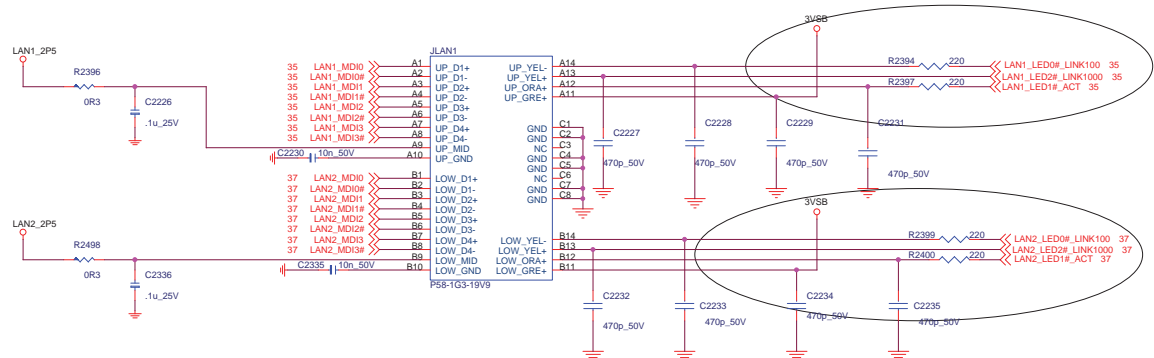
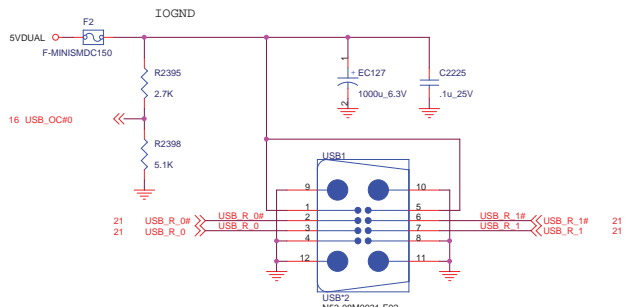


VGA PORT

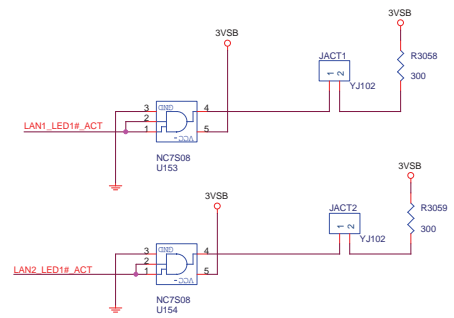
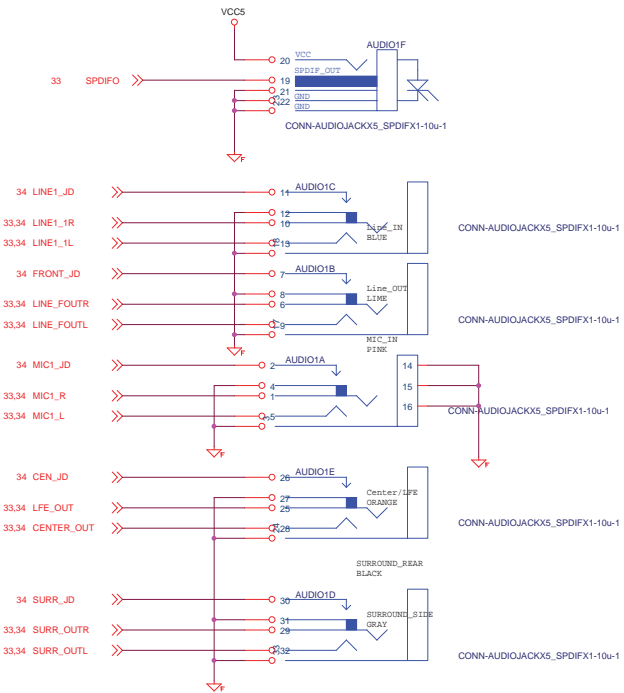


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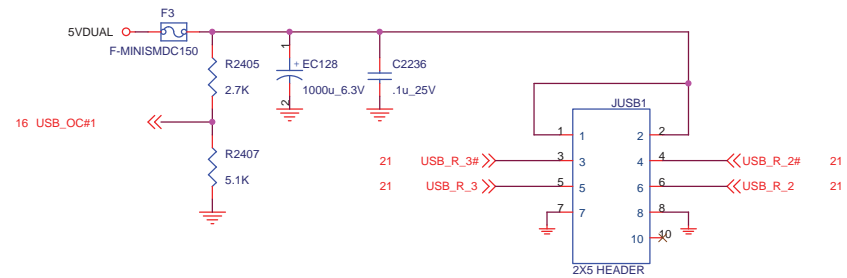
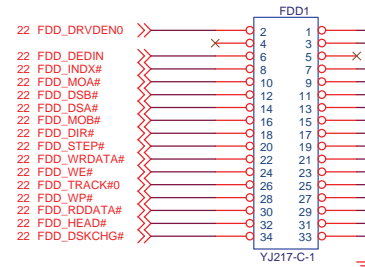
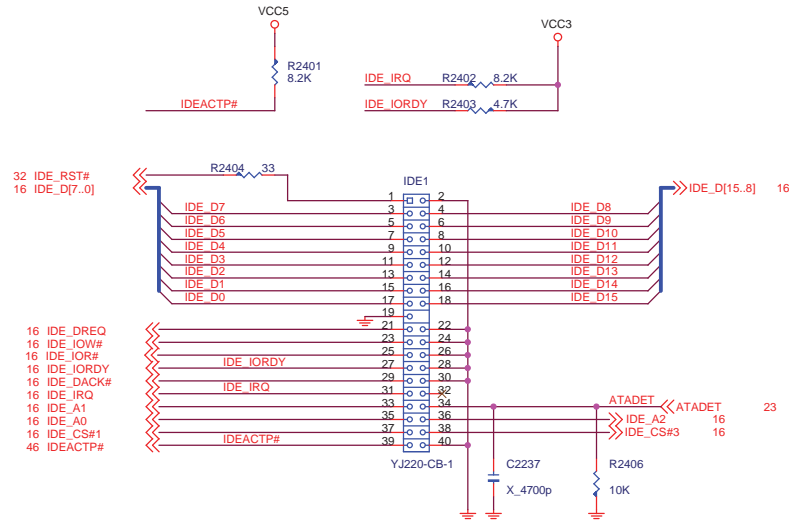
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PS2/COM/VGA/PARALLEL Conn		
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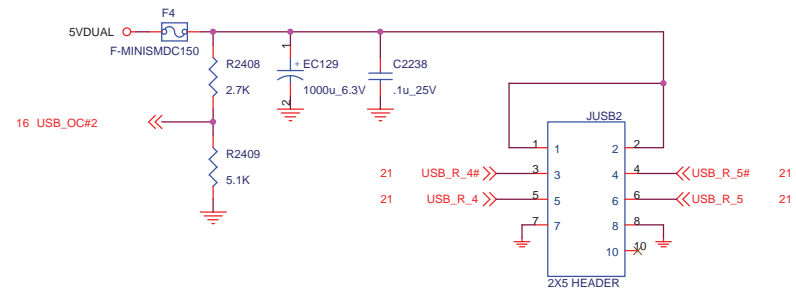
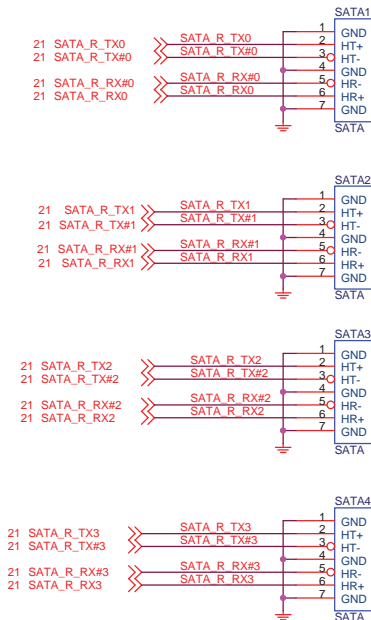
ALC880 JACK



IDE Connector

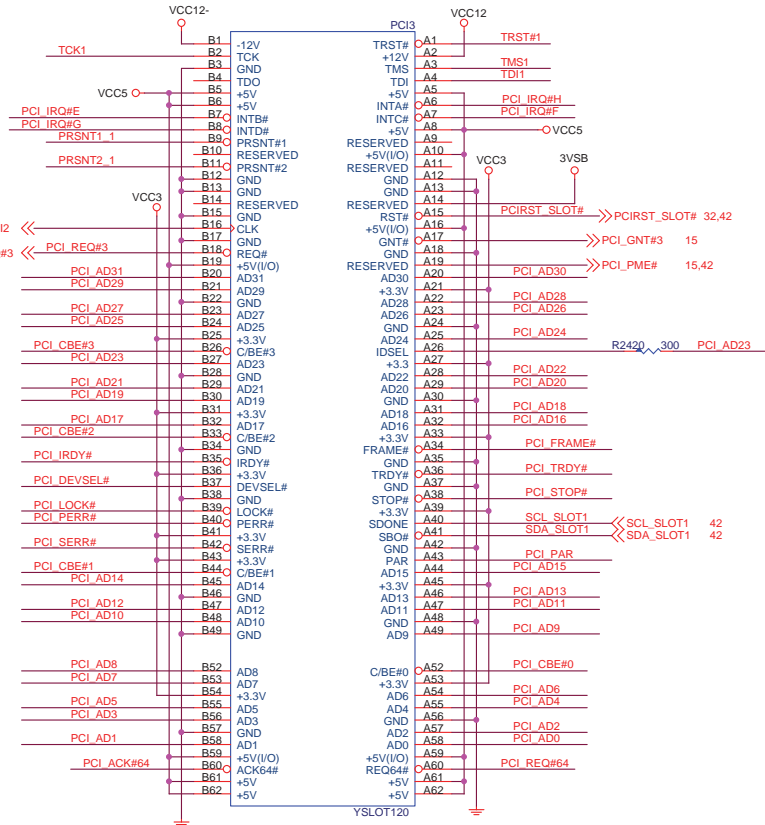


SATA Connector

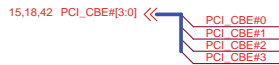
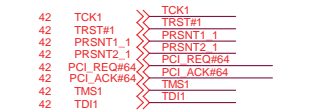
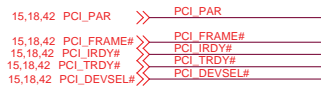


PIRQE#INTDINTCINTB
 PIRQF#INTAINTDINTC
 PIRQG#INTBINTAINTD
 PIRQH#INTCINTBINTA
 IDSELAD21AD22AD23

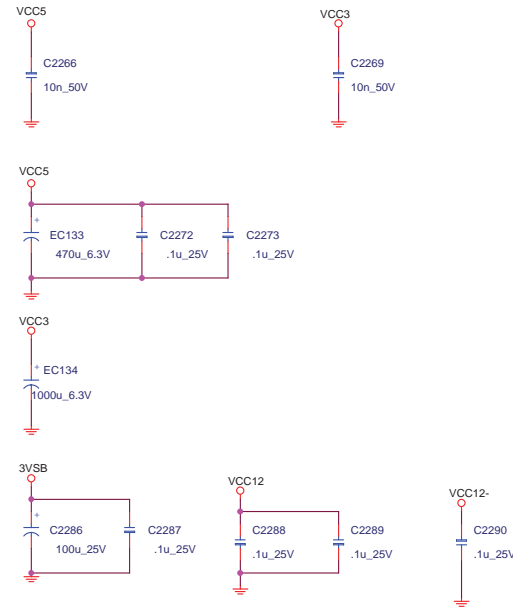
PCI SLOT 3



IDSEL = AD23



PCI SLOT DECOUPLING CAPACITORS



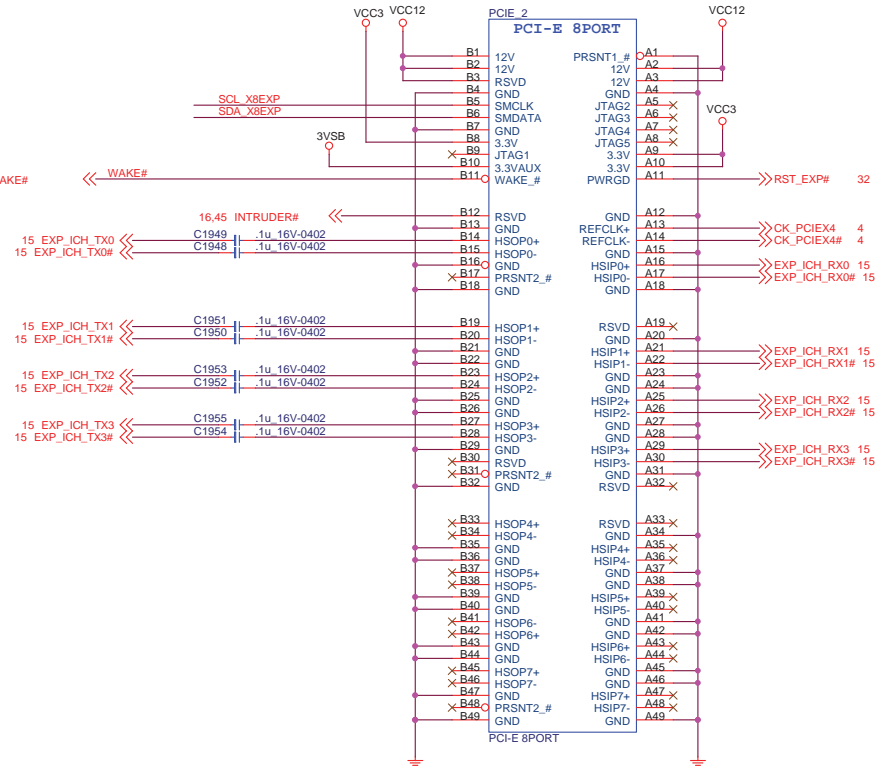
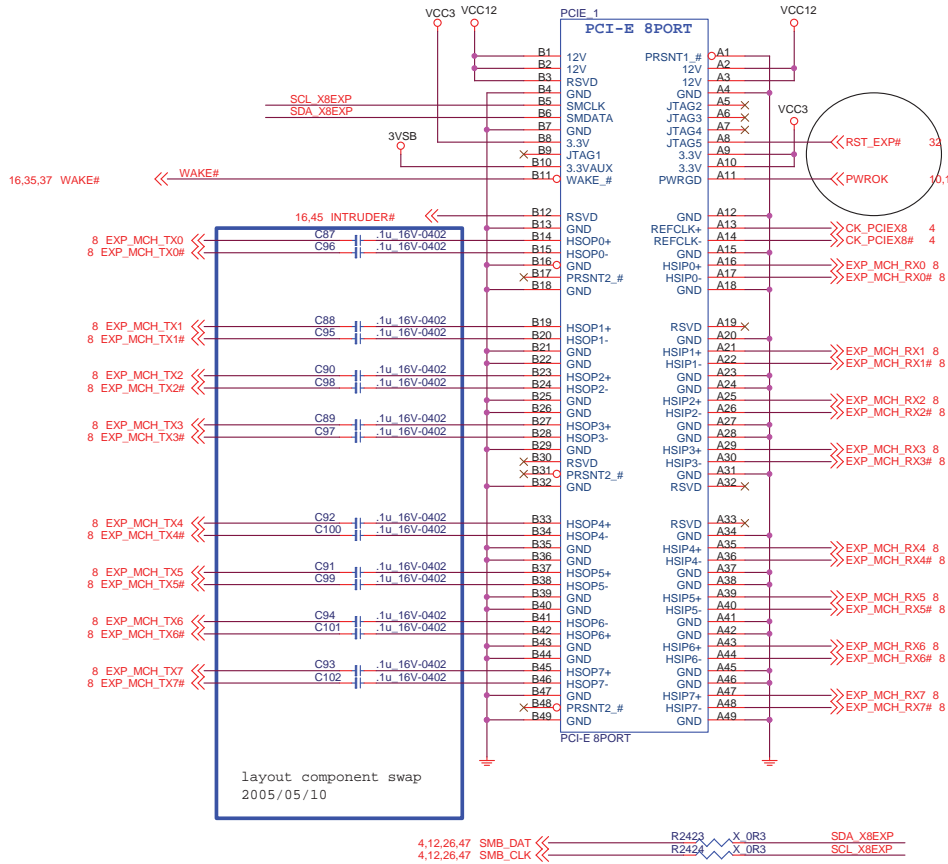
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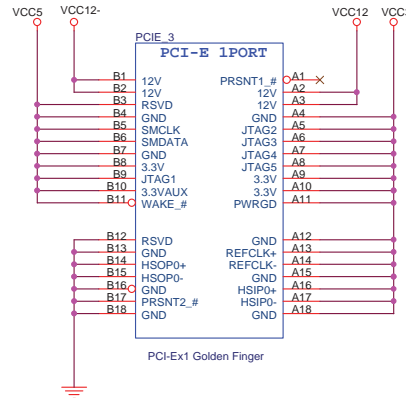
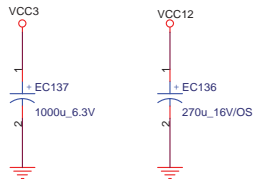
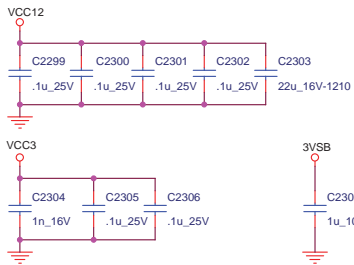
Title PCI 3		
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PCI-EXPRESS x 8

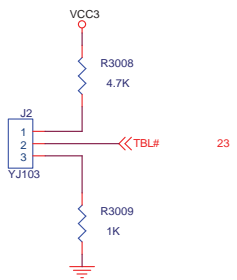
PCI-EXPRESS x 4



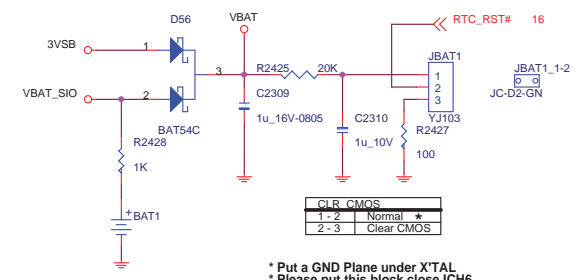
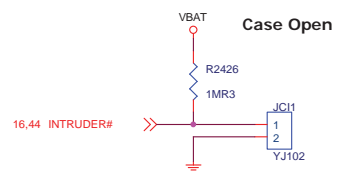
layout component swap
2005/05/10



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Title PCI EXPRESS x8 and x4		
Size Custom	Document Number MS-9618	Rev 1A
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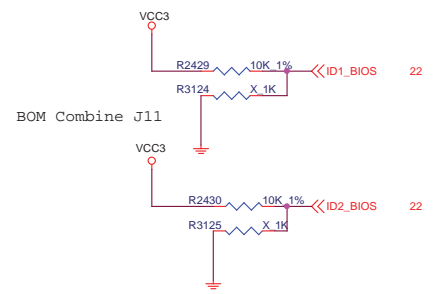
1-2 LOCKED
2-3 UNLOCKED (Default)



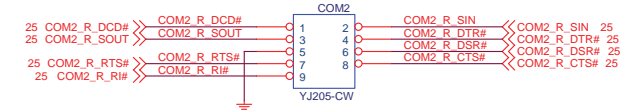
CLR CMOS	
1-2	Normal *
2-3	Clear CMOS

* Put a GND Plane under X'TAL
* Please put this block close ICH6

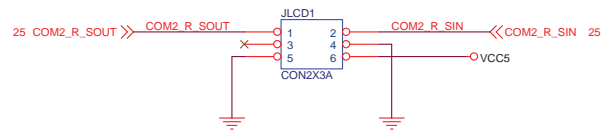
ID FOR BIOS



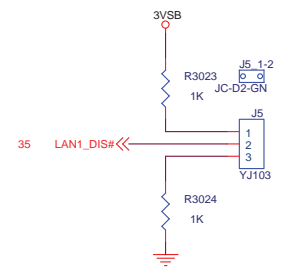
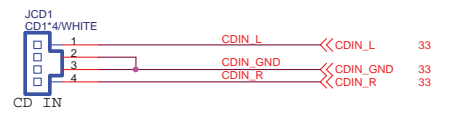
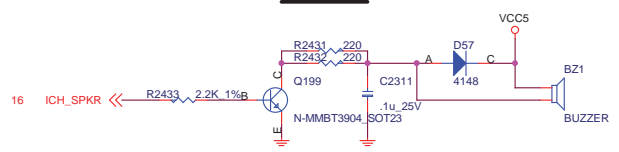
COM PORT B



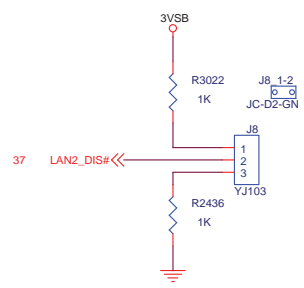
JLCD1



BUZZER

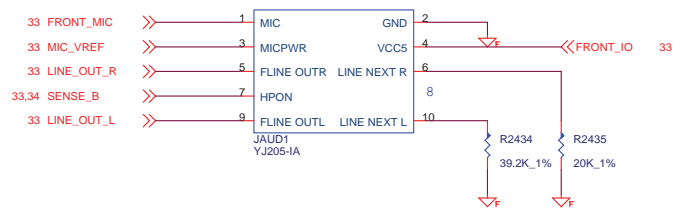


Lan Enable/Disable	
Disable	2-3
Enable	1-2



Lan Enable/Disable	
Disable	2-3
Enable	1-2

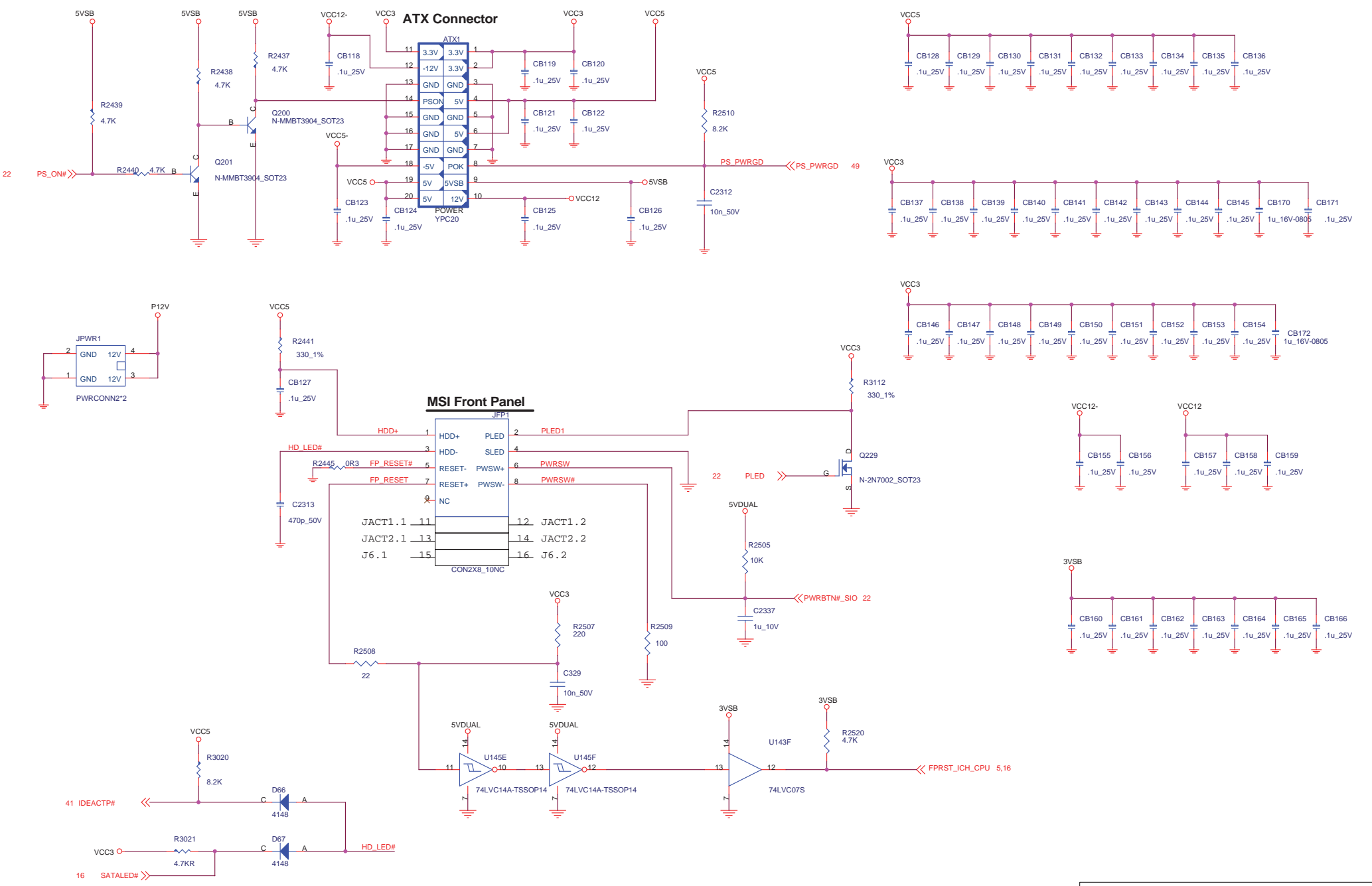
Azalia Front Audio Connector



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Title: **MISC PIN header**

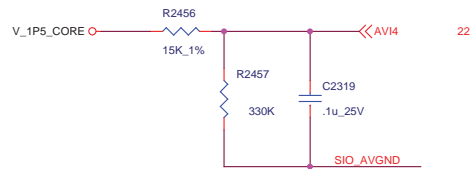
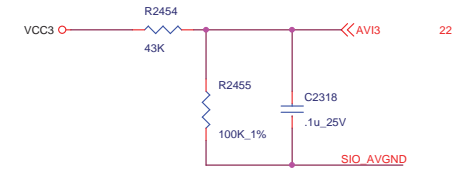
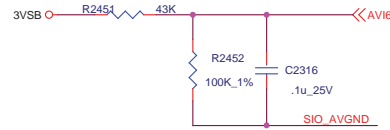
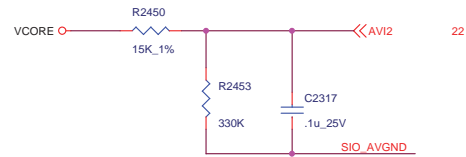
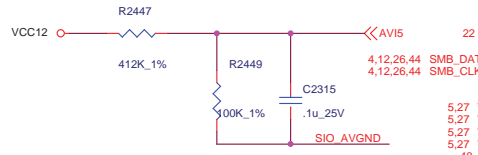
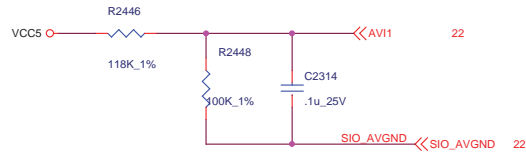
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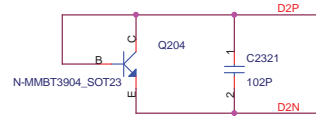
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Title		
ATX PWR/Font panel		
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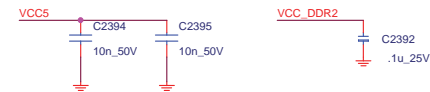
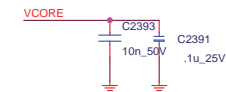
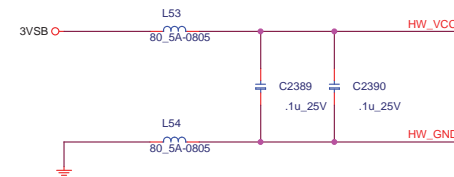
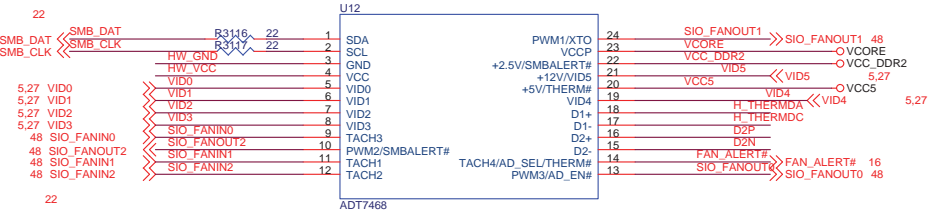
SIO Hardware Monitor (VCC5, VCORE, VCC3, VCC12, V_1P5_CORE, 3VSB)
System Temperatur * 2



SYSTEM TEMPERATURE



Put Between PCI Slots

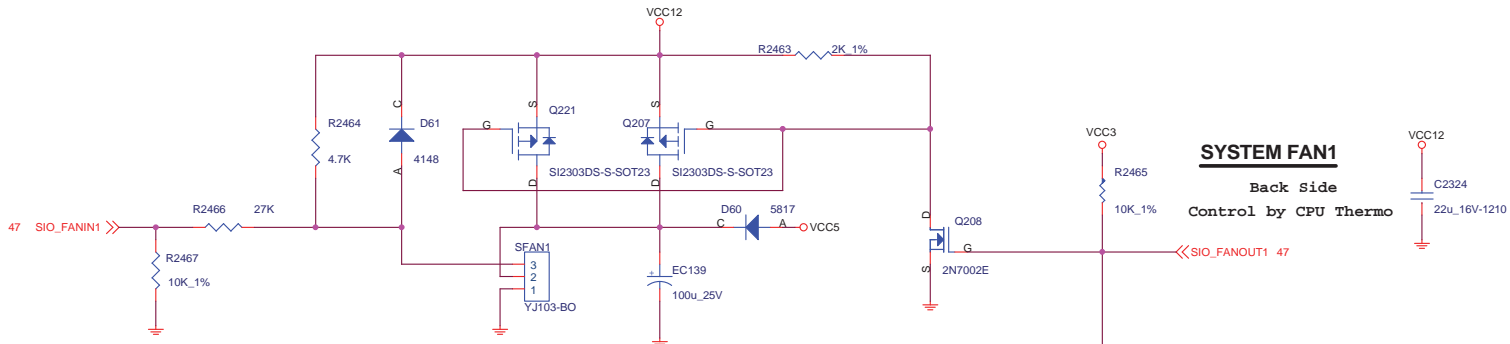
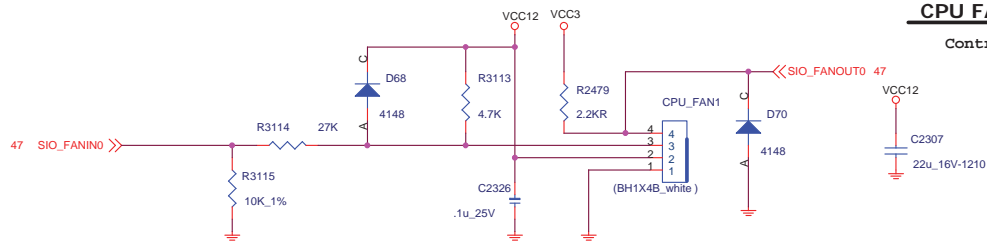


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Title: SIO HW		
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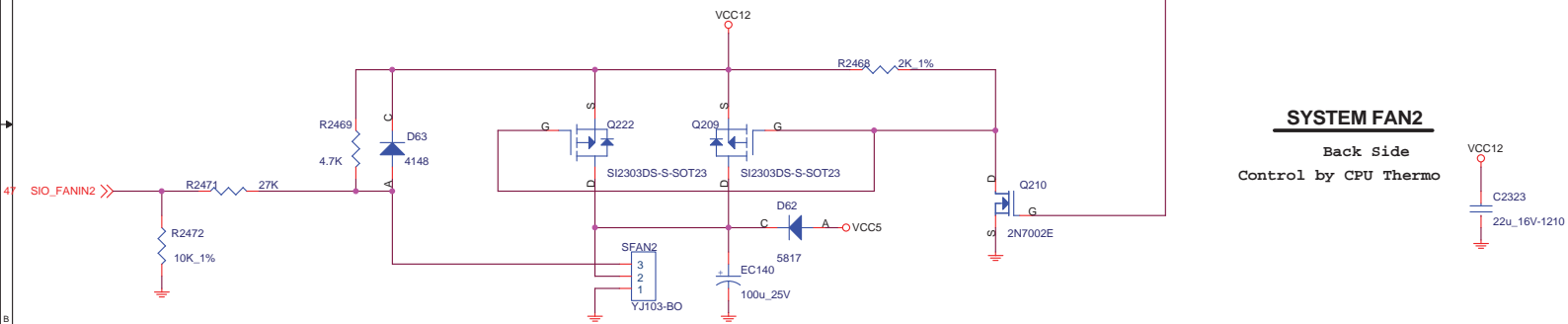
CPU FAN

Control by CPU Thermo



SYSTEM FAN1

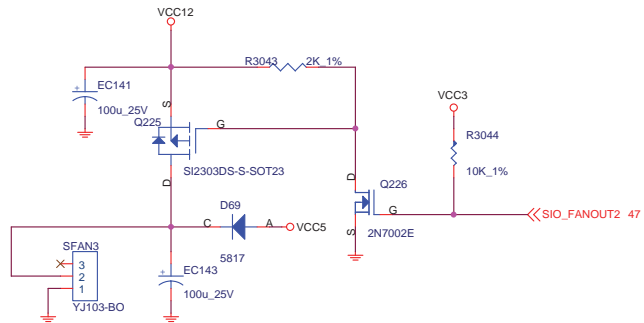
Back Side
Control by CPU Thermo



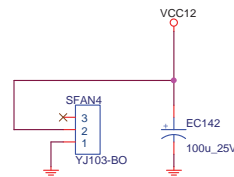
SYSTEM FAN2
Back Side
Control by CPU Thermo

SYSTEM FAN3

Front Side
Control by System Thermo



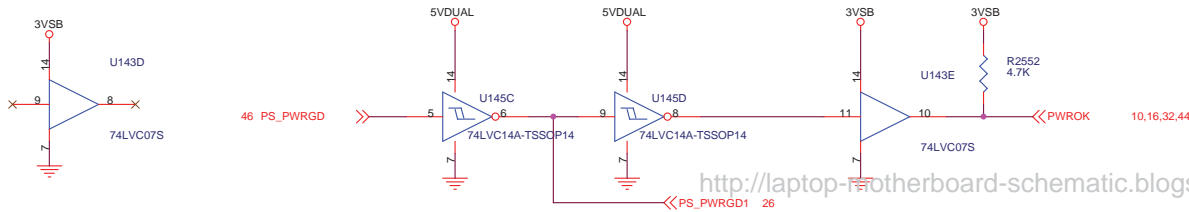
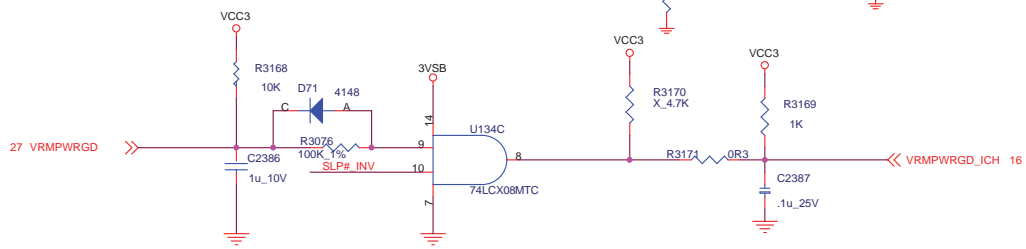
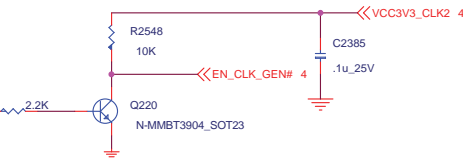
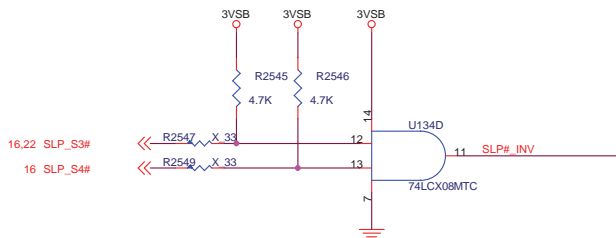
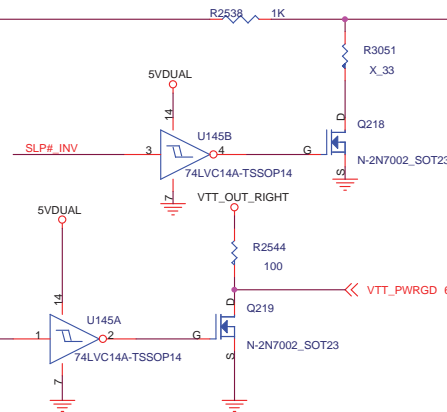
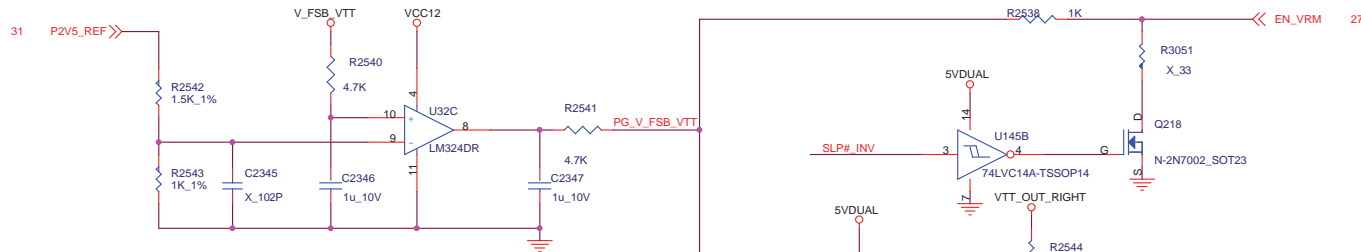
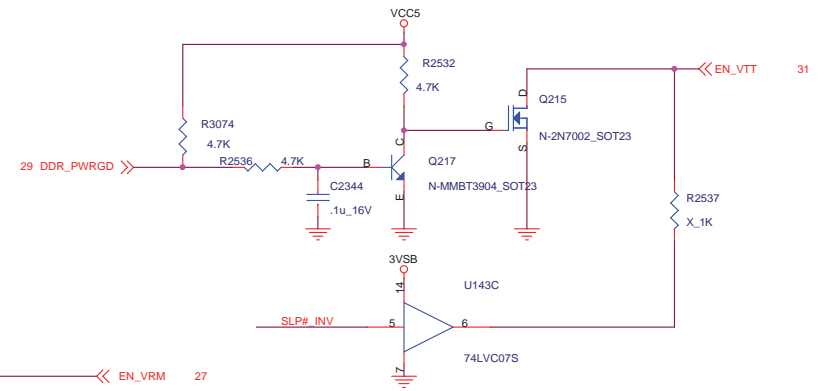
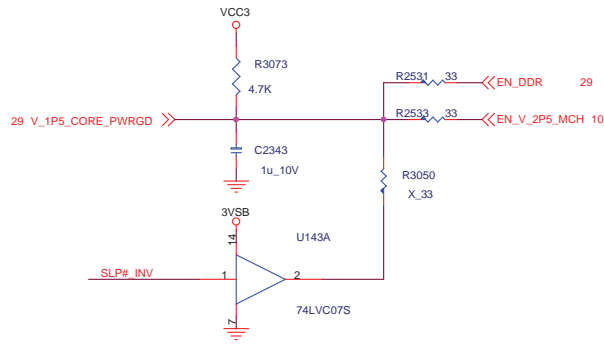
For NB Chipset



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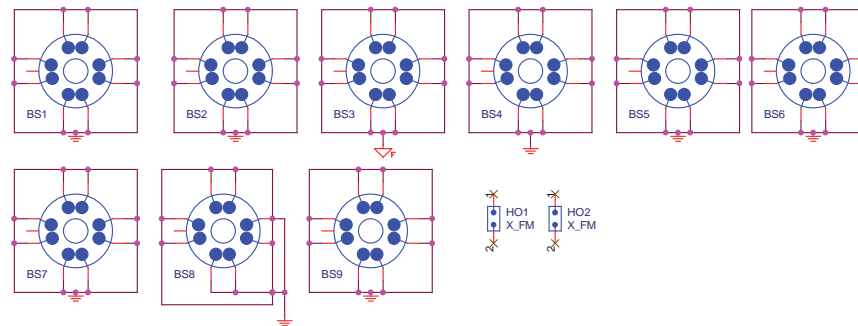
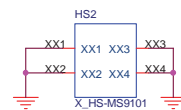
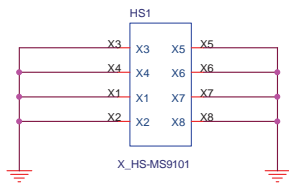
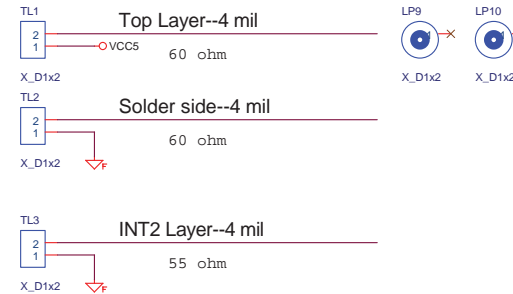
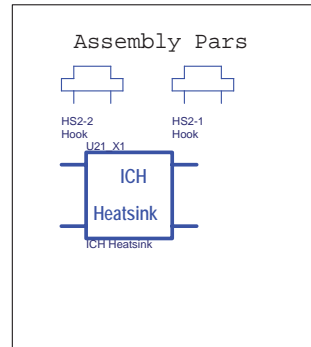
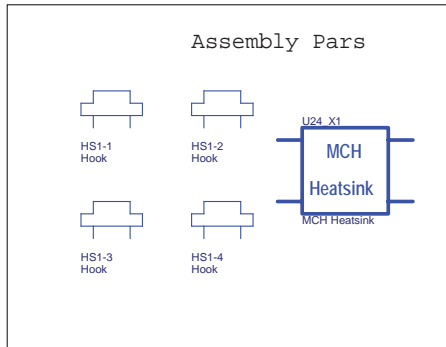
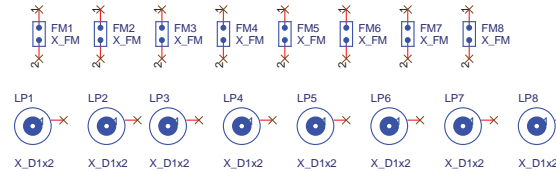
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FAN		
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Title Layout Components		
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