MS-9620-0A

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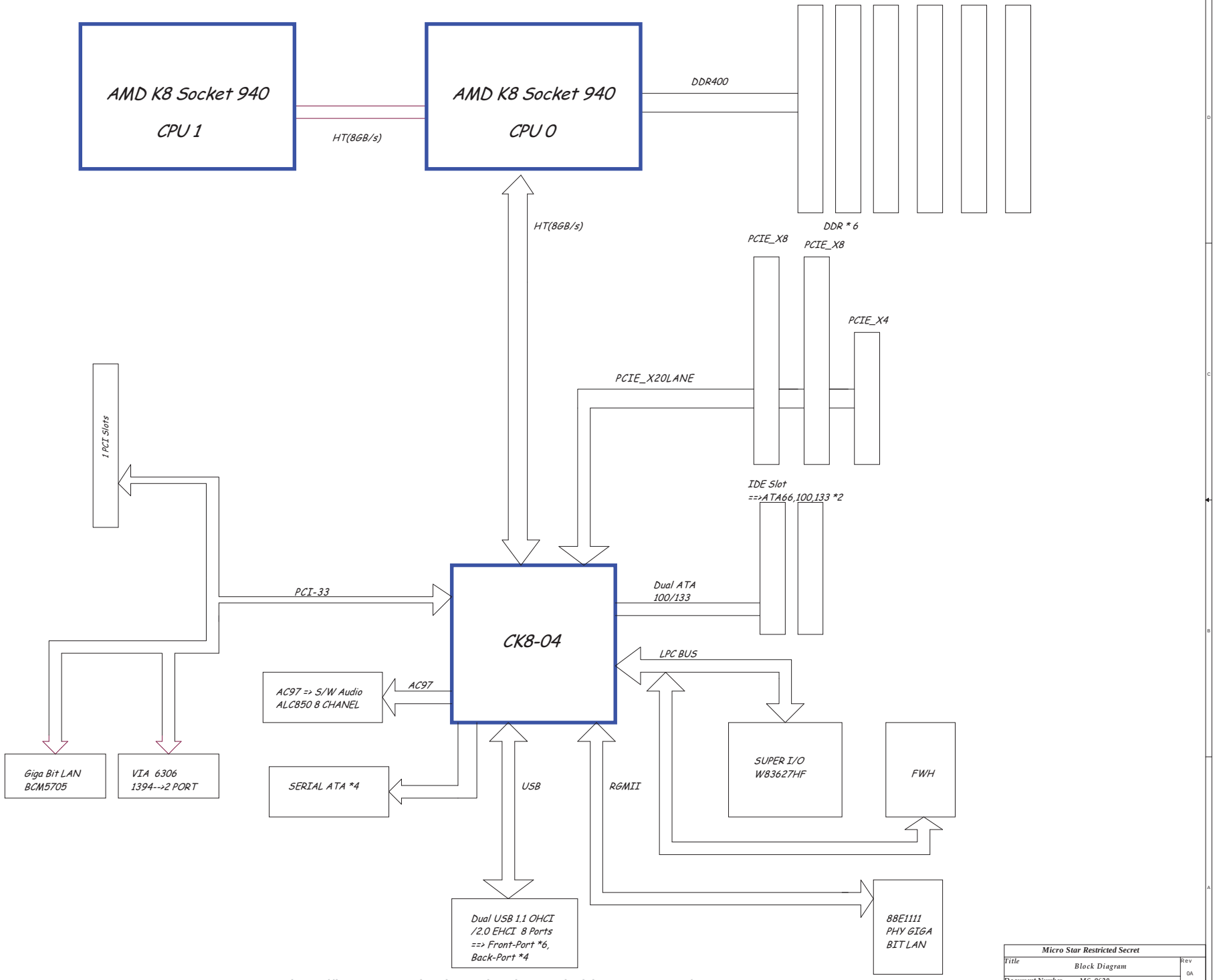
Block Diagram



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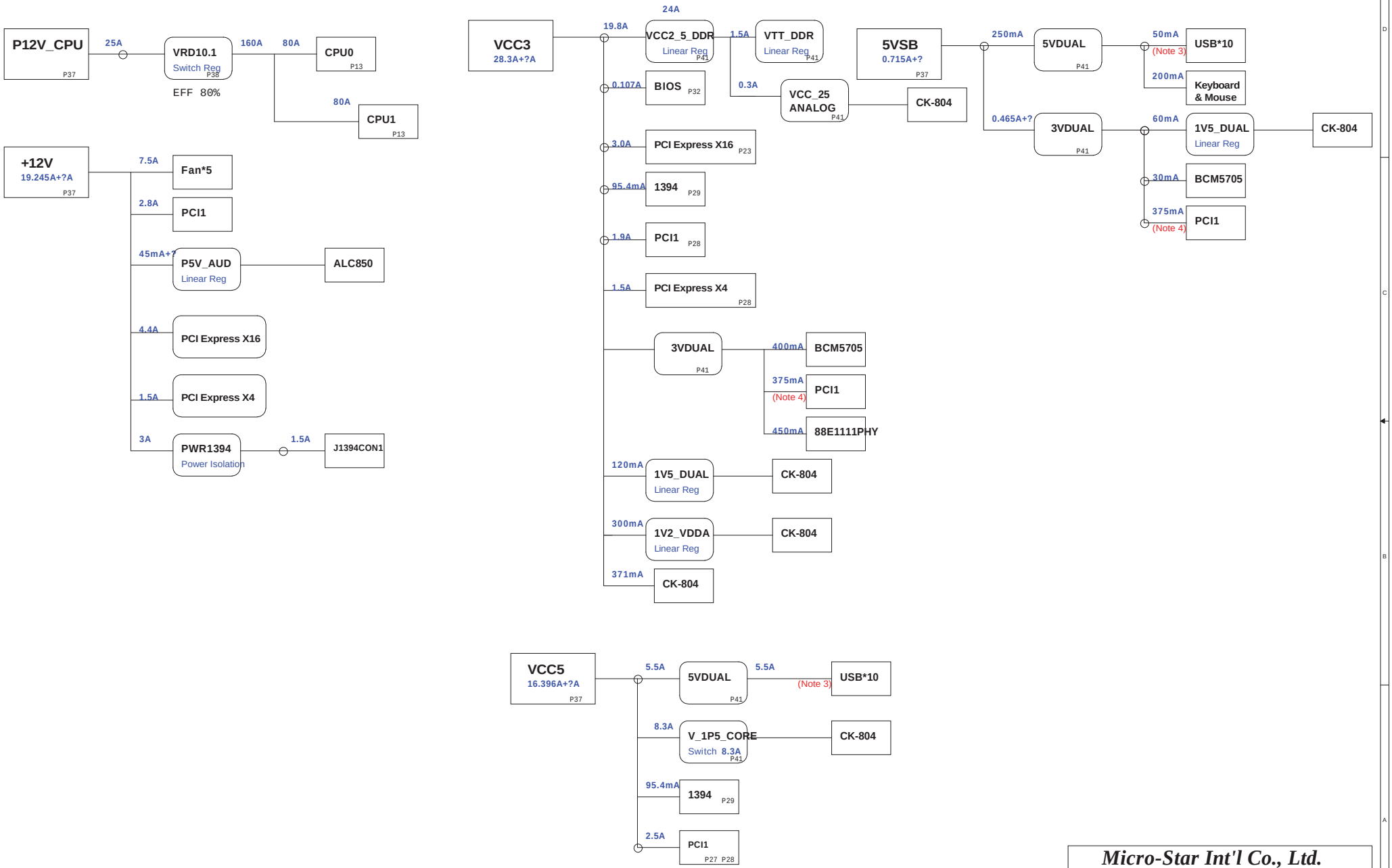
MS-9620 POWER DELIEVERY DIAGRAM



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Title	Power Delivery Block Diagram	
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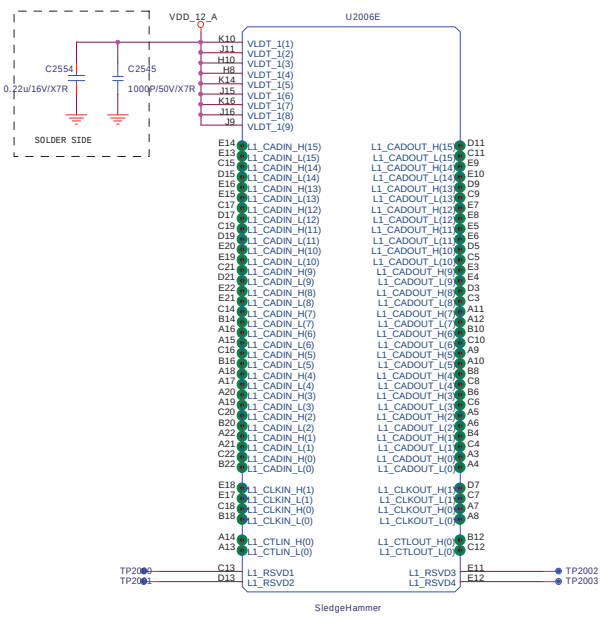
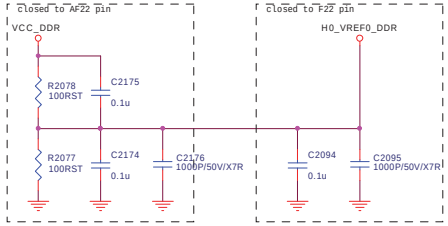
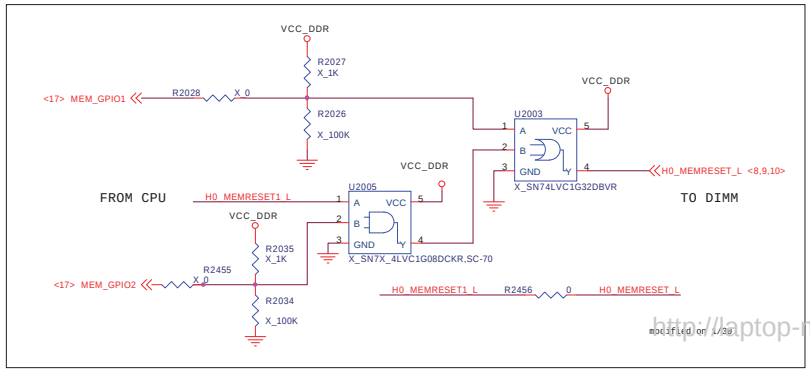
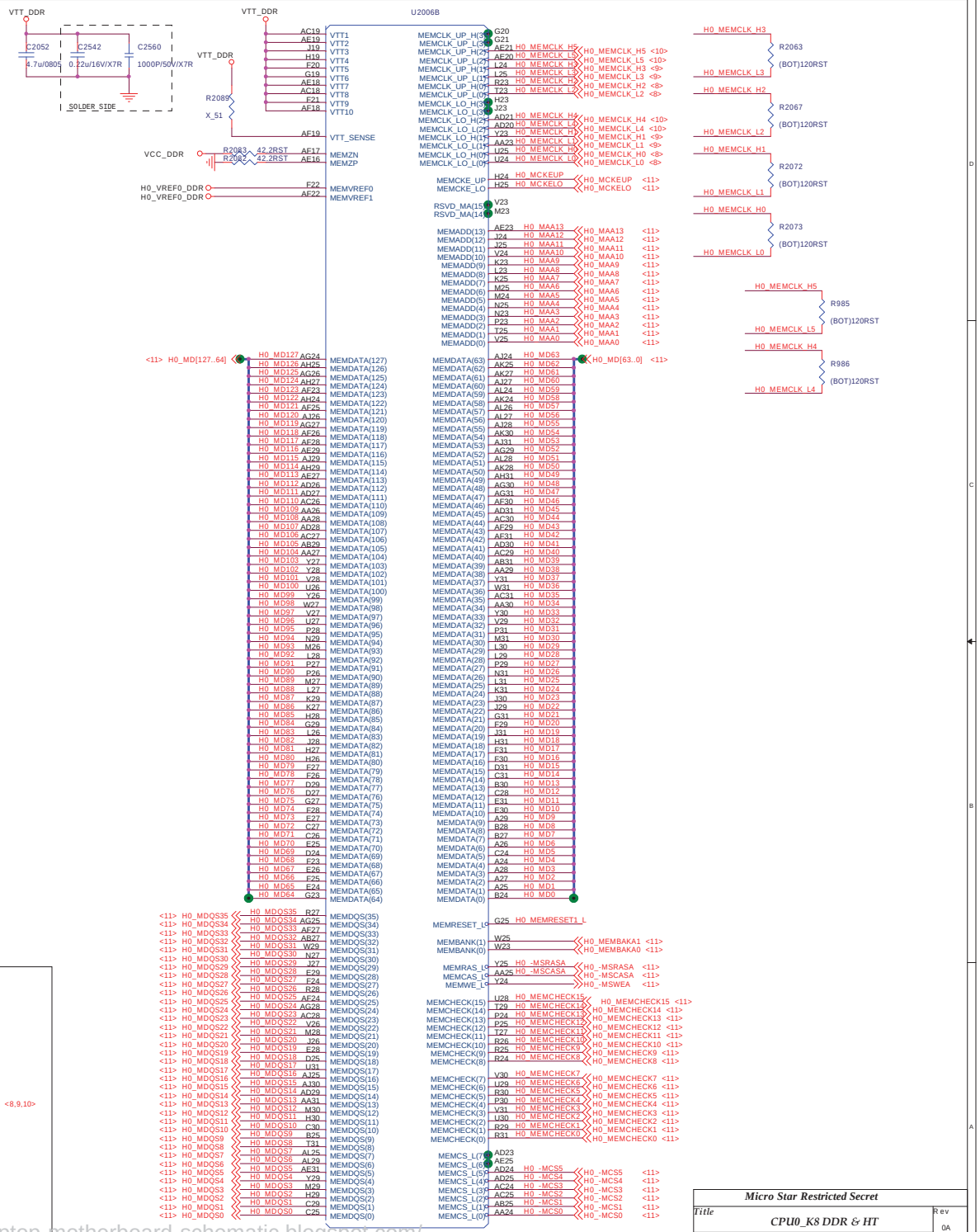
HT0 is for SH0 & Golem connection









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Rev	0A
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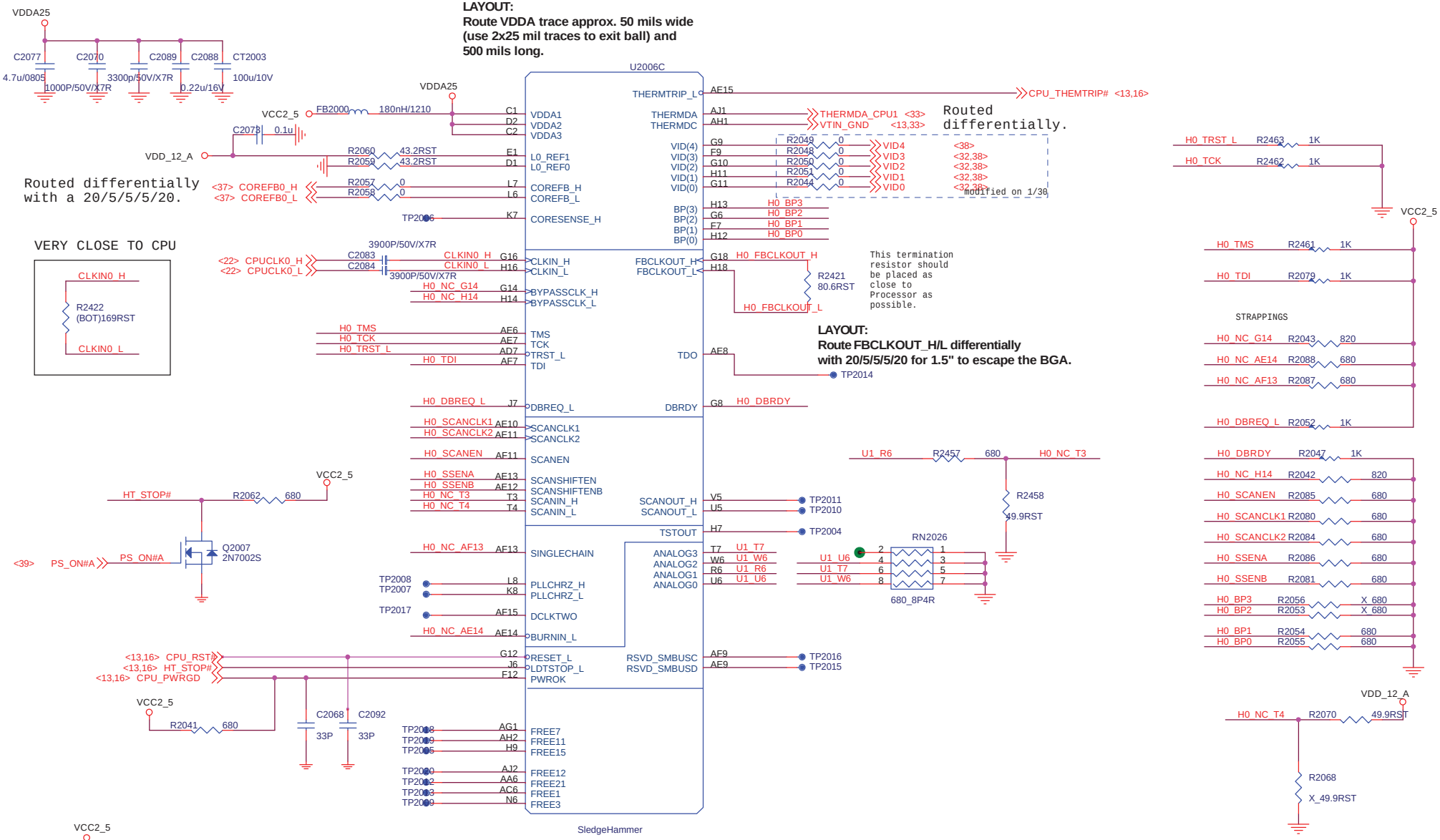

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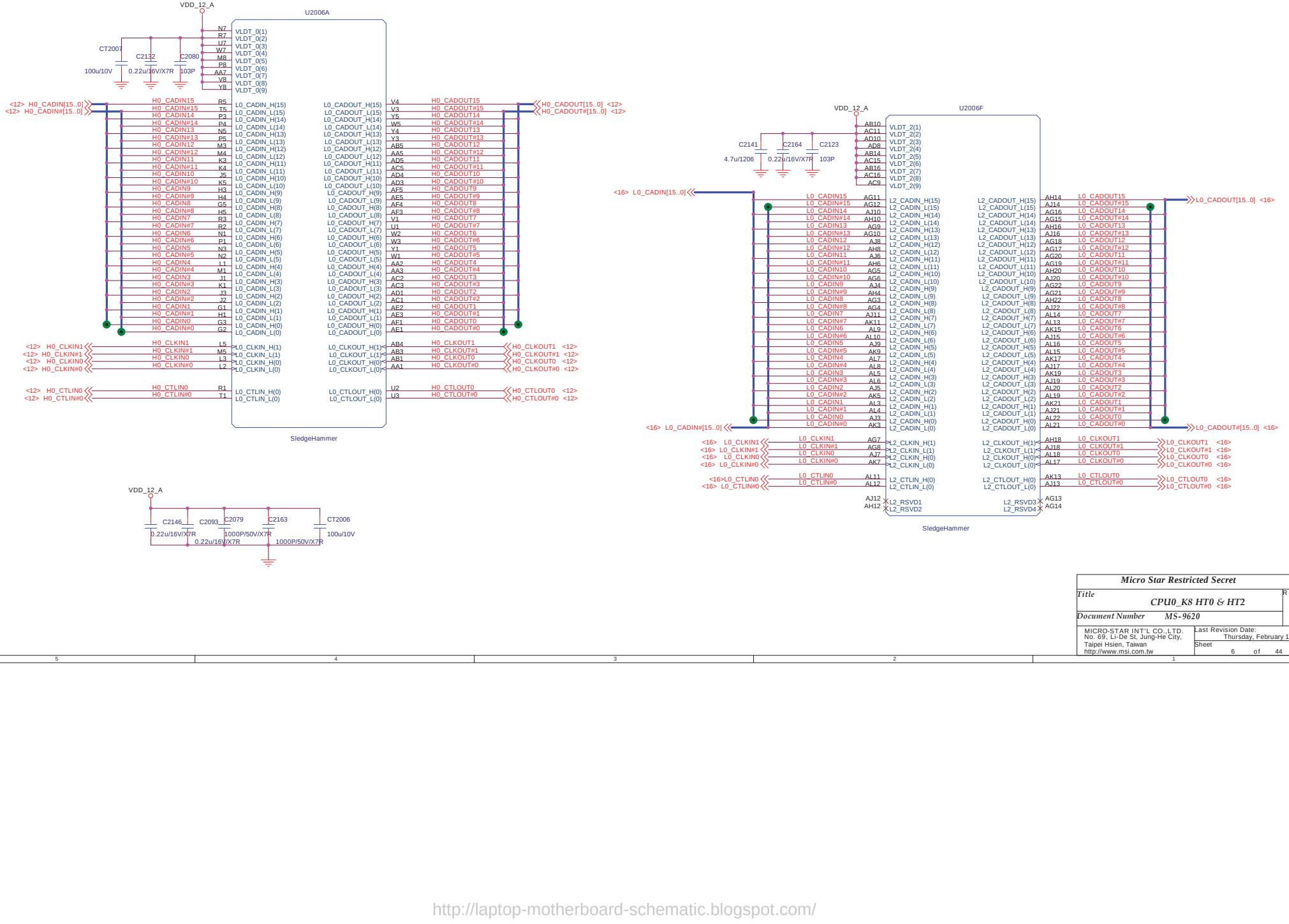

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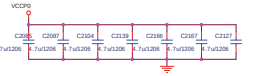
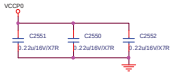
LAYOUT: Place solder side of processor.

LAYOUT: Place clolse to socket.

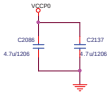


BULK / Decoupling

Place on CPU Solder side

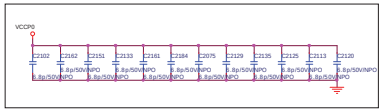


Buck-decoupling Mid-Freq. decoupling Cap. (7 * 4.7uF / 1206 X7R)

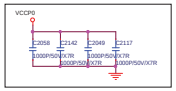


EMI

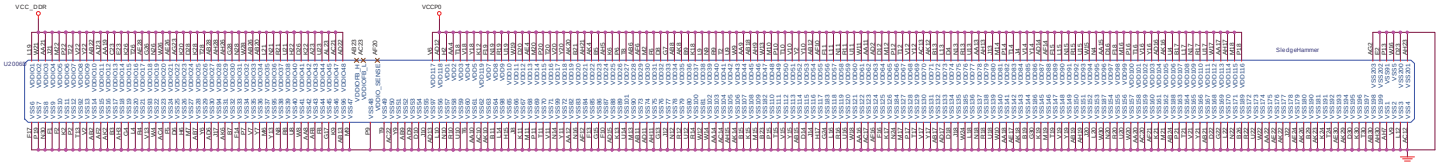
LAYOUT:
Place 1 capacitor every 1-1.5" along VDD_CORE perimiter.



LAYOUT:
Place 1000pF capacitors between VRM & CPU.



Buck-decoupling Mid-Freq. decoupling Cap. (7 * 4.7uF / 1206 X7R)



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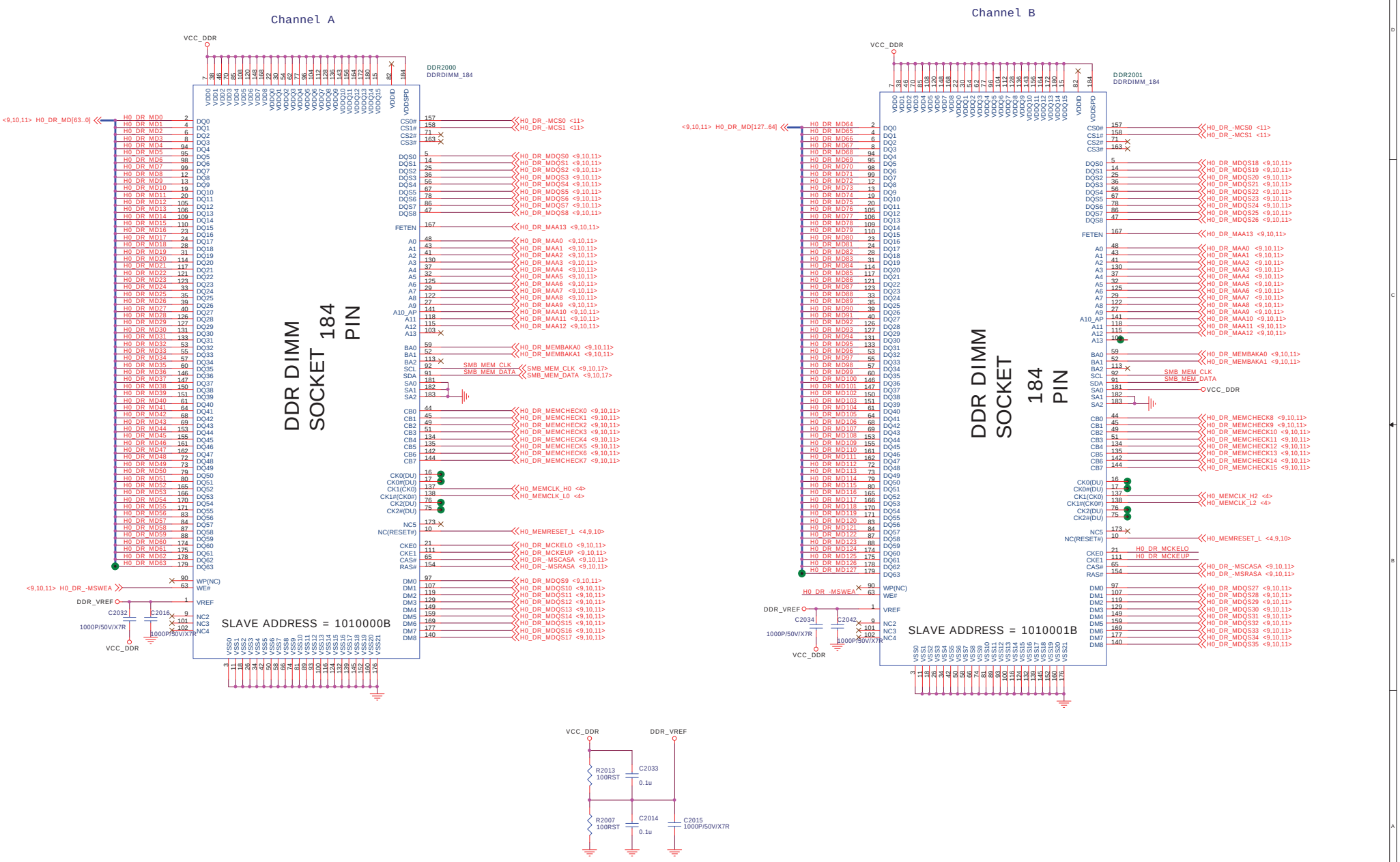
Registered DDR333 SDRAM Sockets



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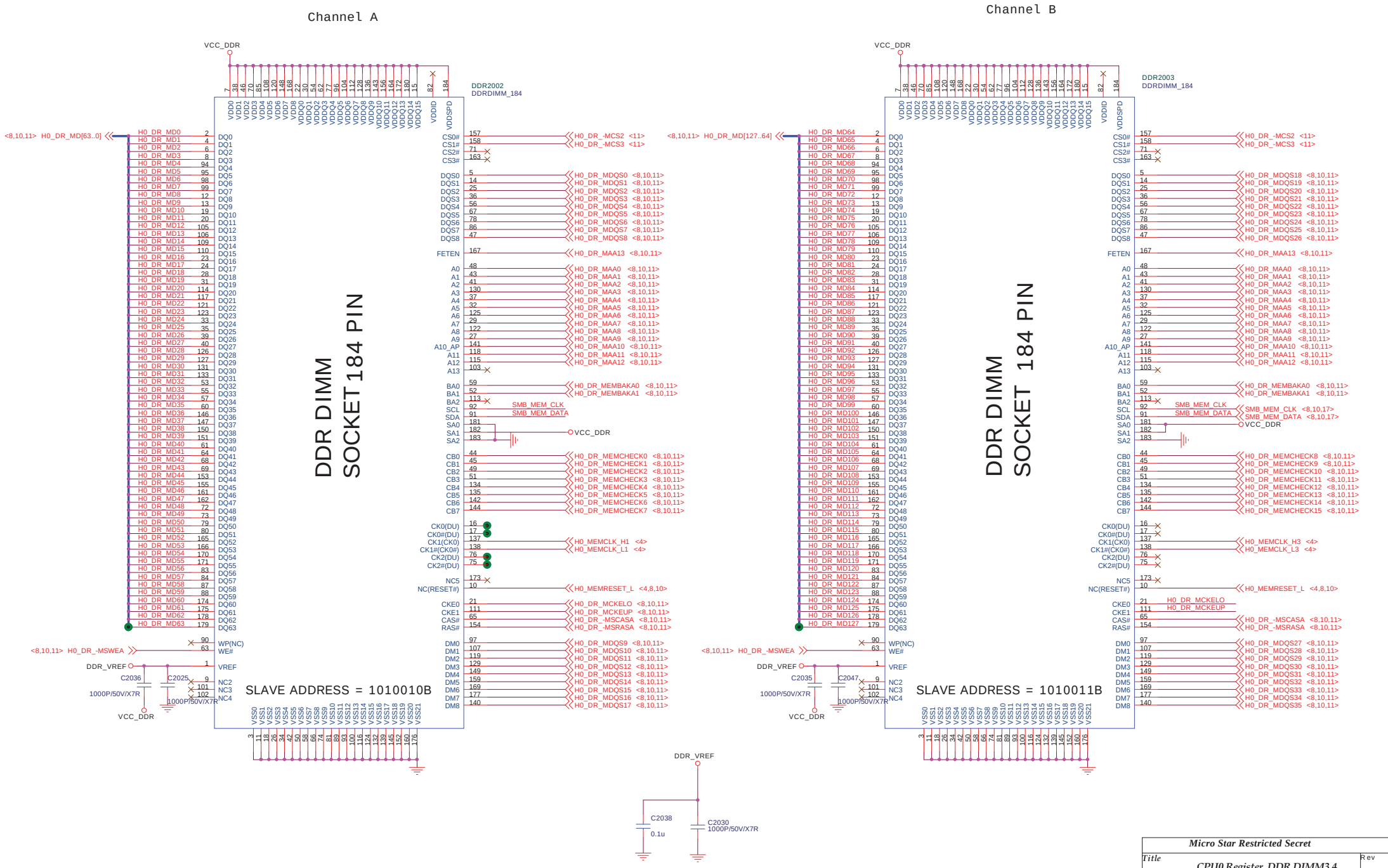
Registered DDR333 SDRAM Sockets



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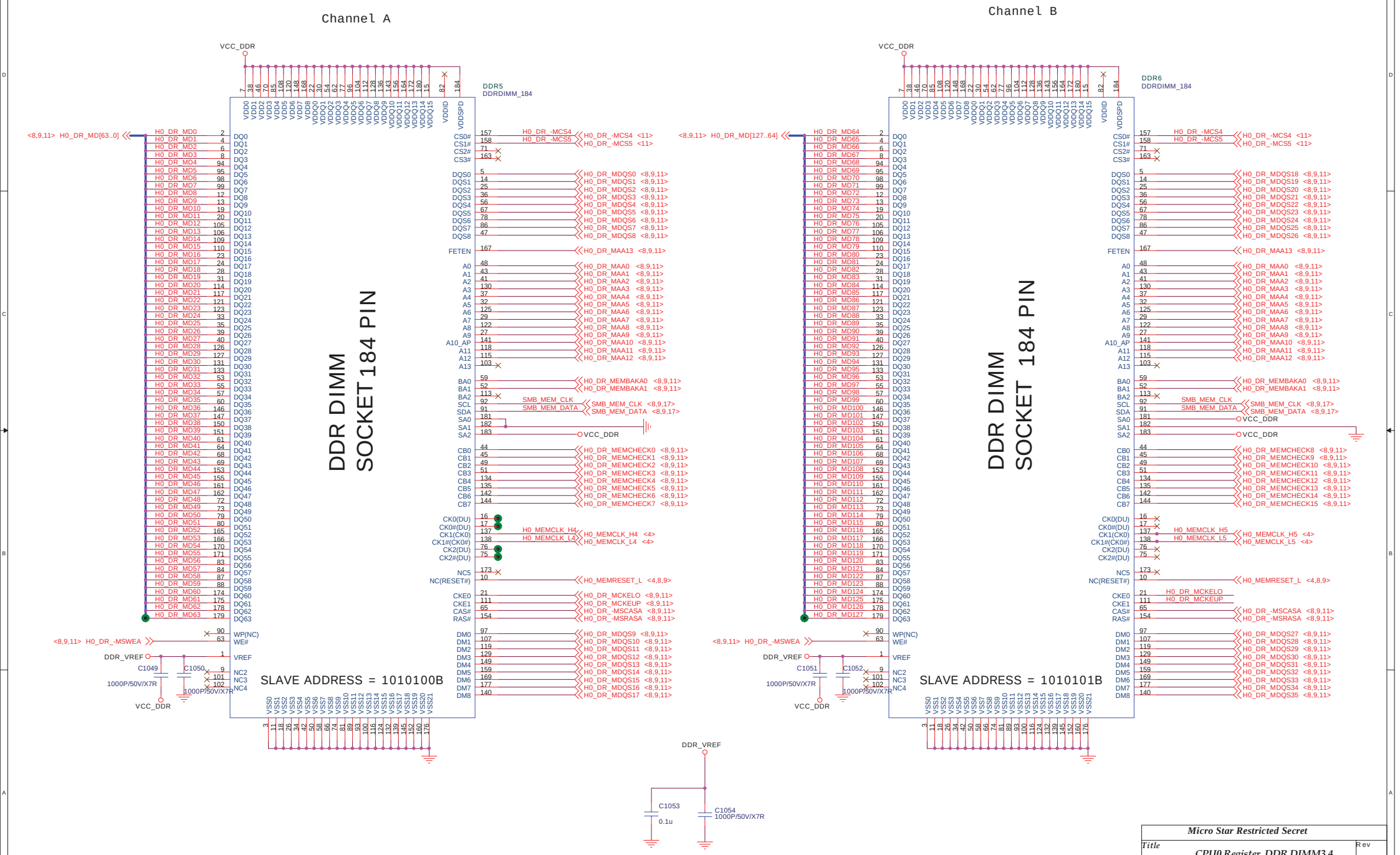
Registered DDR333 SDRAM Sockets



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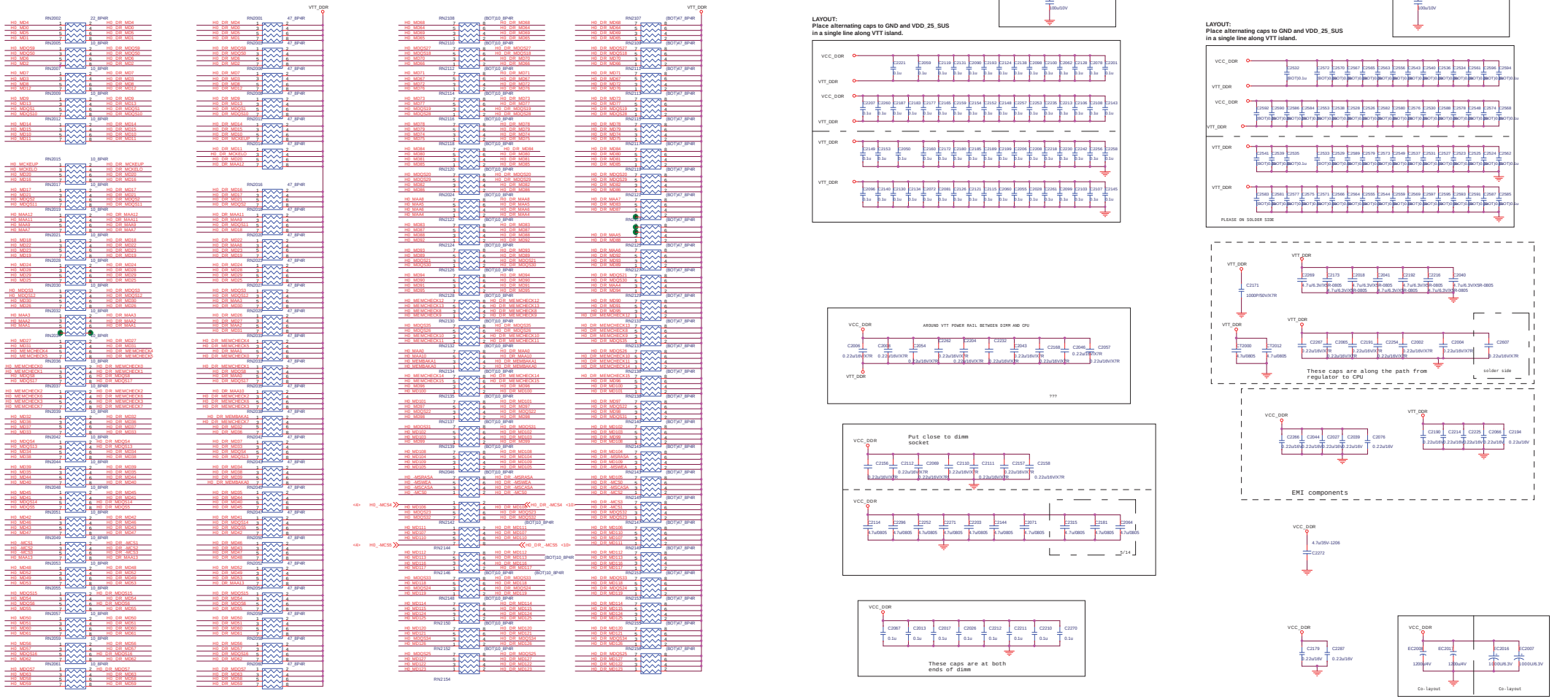
DDR Terminations



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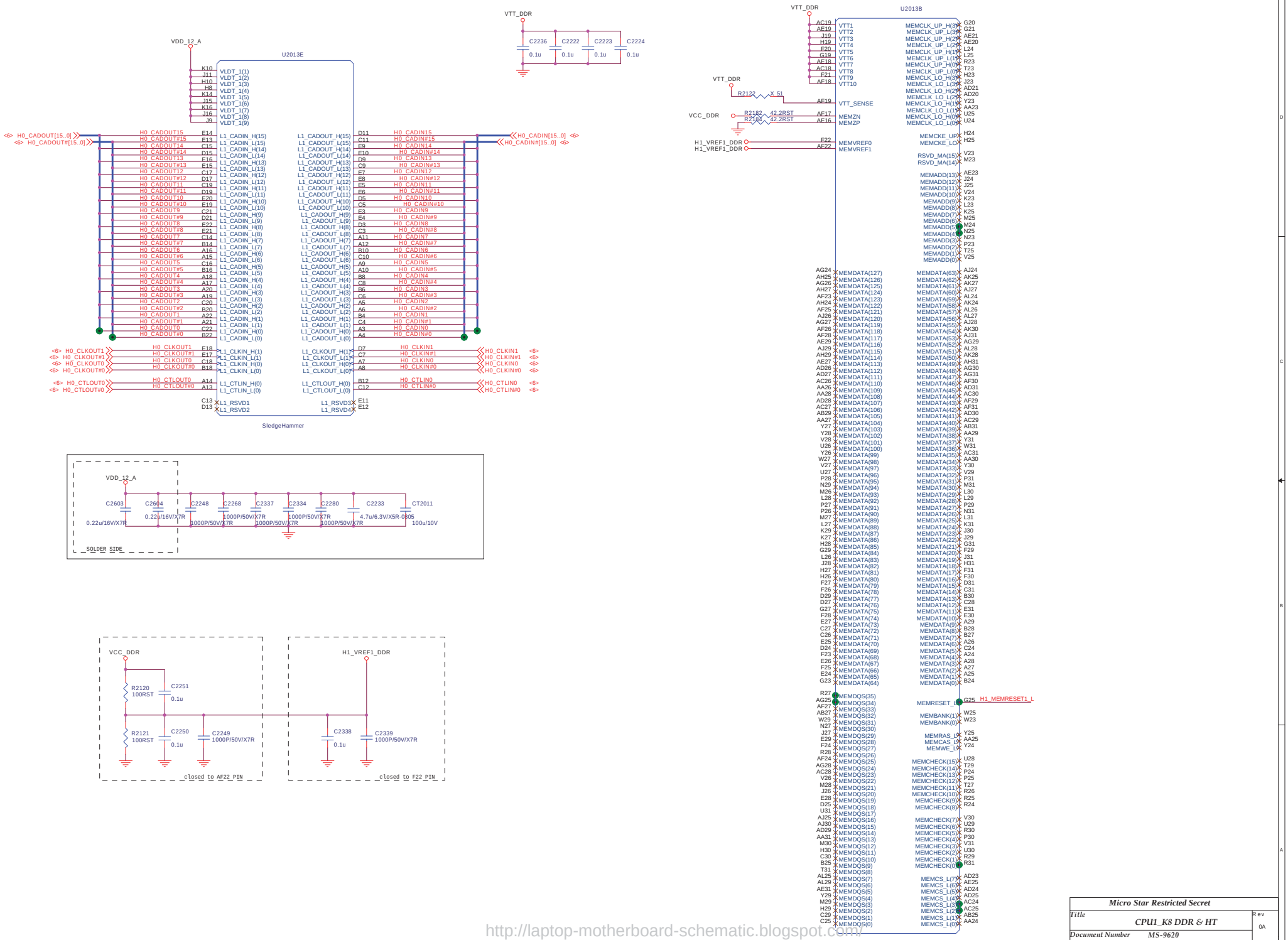

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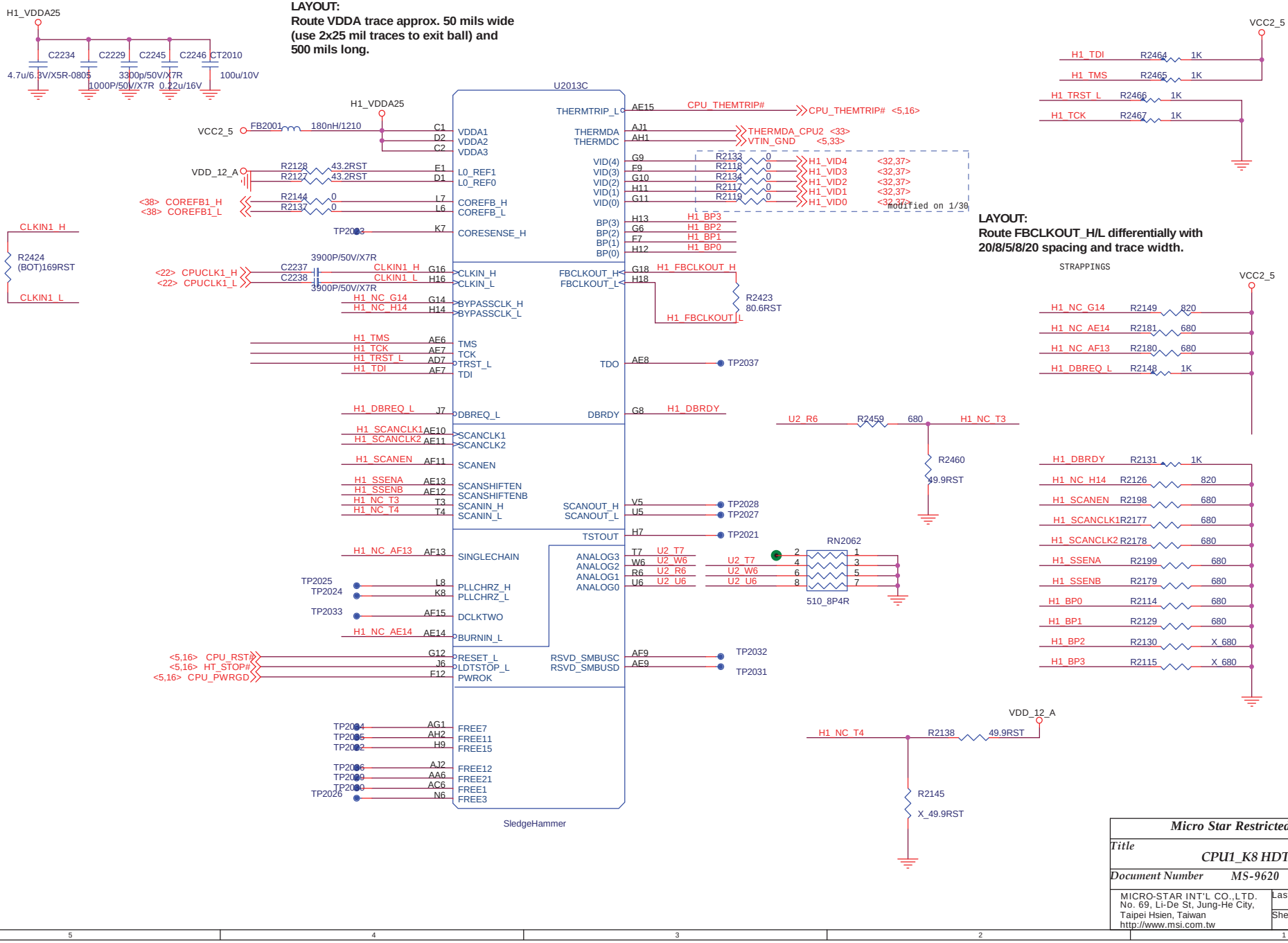

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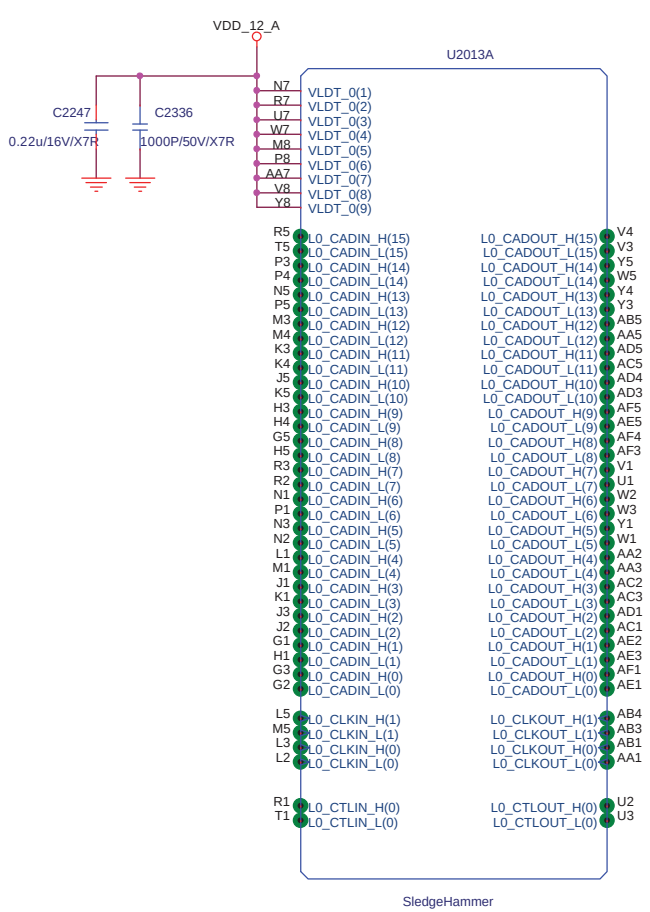

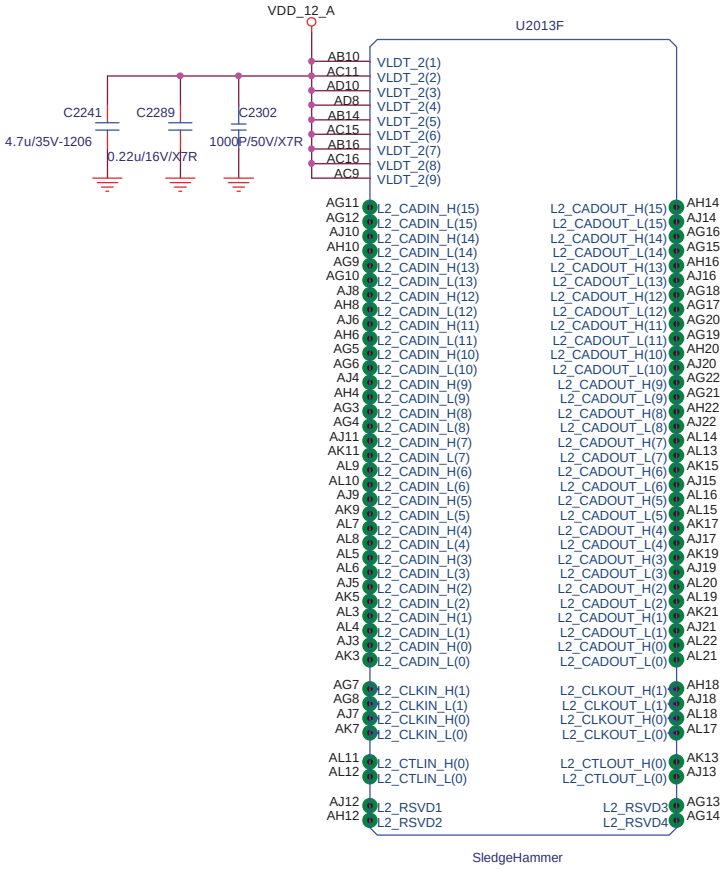

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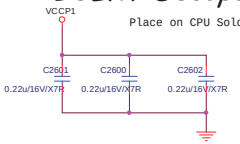
CPU

Place on inside of CPU Cavity (10 * 0.22uF/0603
X7R high-freq decoupling Cap.)

LAYOUT: Place inside of processor.

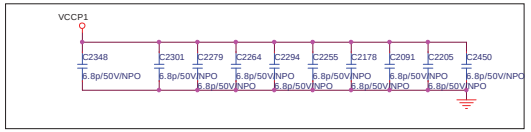
BULK / Decoupling

Place on CPU Solder side

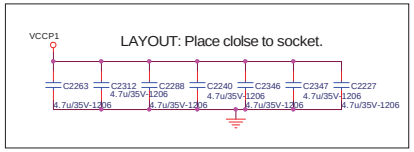


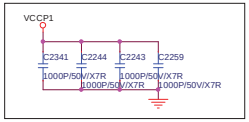
EMI

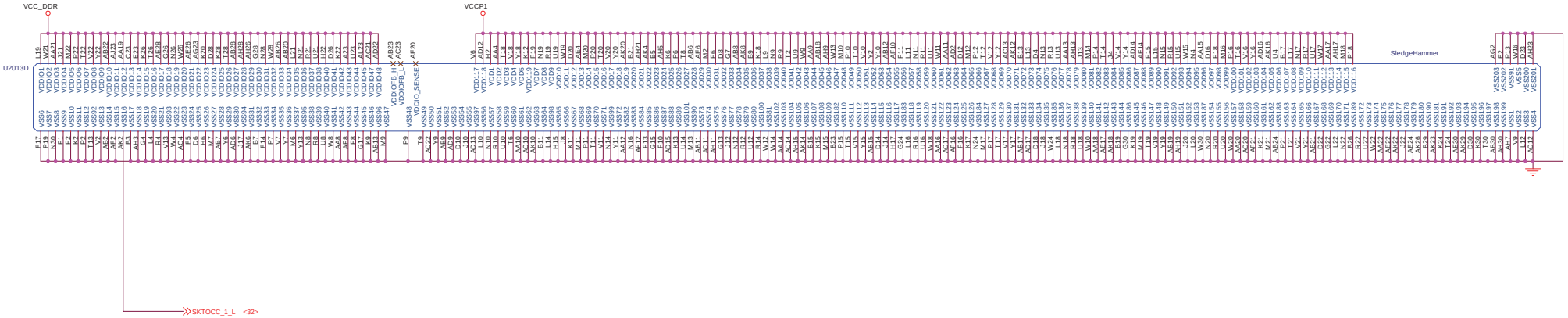
LAYOUT:
Place 1 capacitor every 1-1.5" along VDD_CORE perimiter.



LAYOUT: Place clolse to socket.







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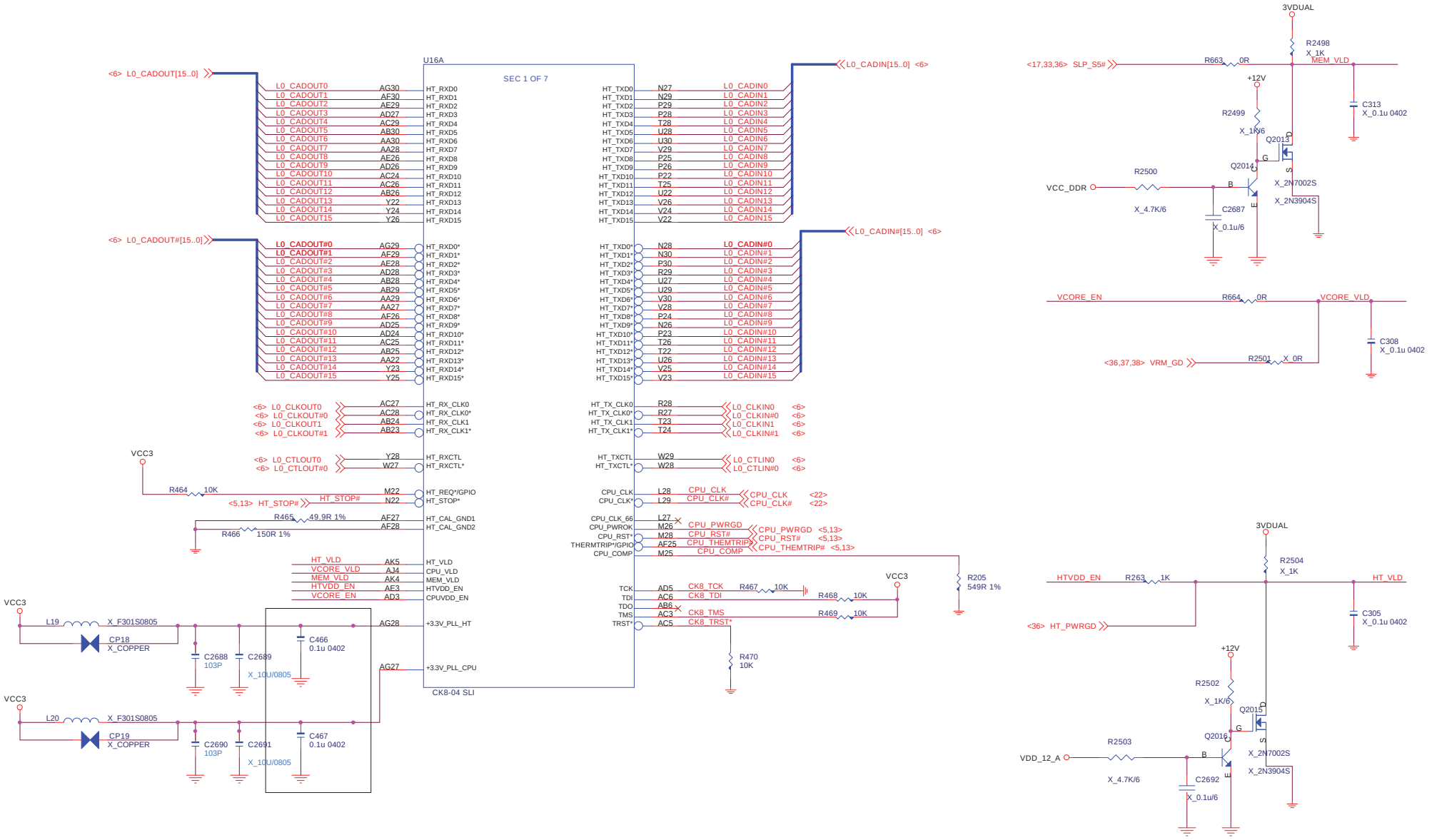

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3VDUAL
R174 1.5K 1%
High:Use PHY
Low: No use PHY
MII_MDIO
R617 X_4.7K
<29> RGMII_TX[3..0]
RN104
RGMII_TX0 RGMII_TX1 RGMII_TX2 RGMII_TX3
RGMIITX0 RGMIITX1 RGMIITX2 RGMIITX3
22R-8P4R
PLACE NEAR CK8-04
MII_COL
R2468 10K
MII_CRS
R2469 10K
U16E
SEC 5 OF 7
CK804
3VDUAL
R180 2.4K 1%
R181 1.47K 1%
C226 0.1u 0402
<29> RGMII_TXCLK
<29> RGMII_TXCTL
<29> RGMII_RX[3..0]
R498 22
R499 22
RGMIITXCLK
RGMIITXCTL
RGMII_RX0
RGMII_RX1
RGMII_RX2
RGMII_RX3
<29> RGMII_RXCLK
<29> RGMII_RXCTL
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RGMII_RXCLK
RGMII_RXCTL
MII_MDC
MII_VREF
MII_COL
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MII_MDIO
MII_CRS
<29> RGMII_PWDN#
R500 0R
RGMIIPWDN#
<29> RGMII_25M
R195 X_22
RGMIITX0 H28 G/MII_TXD0
RGMIITX1 J27 G/MII_TXD1
RGMIITX2 J28 G/MII_TXD2
RGMIITX3 J29 G/MII_TXD3
RGMIITXCLK H26 G/MII_TXCLK
RGMIITXCTL J26 G_TXCTL/MII_TXEN
RGMII_RX0 G29 G/MII_RXD0
RGMII_RX1 E30 G/MII_RXD1
RGMII_RX2 F29 G/MII_RXD2
RGMII_RX3 F28 G/MII_RXD3
RGMII_RXCLK H27 G/MII_RXCLK
RGMII_RXCTL G28 G_RXCTL/MII_RXDV
MII_MDC K24 G/MII_MDC
MII_VREF E29 MII_VREF
MII_COL K29 MII_RXER/GPIO
MII_COL K26 MII_COL
MII_MDIO J30 G/MII_MDIO
MII_CRS K27 MII_CRS
RGMIIPWDN# K25 MII_PWRDWN/GPIO
K28 MII_INTR/GPIO
BUF_25MHZ M24
VCC3
R283 10K
R287 X_10K
R501 10K
R282 X_10K
R284 10K
R502 X_10K
<31> AC97CLK
R268 22
AC_BITCLK
AC_SDOUT
<31> AC_SDIN0
AC_RST#
AC_SYNC
Y6 AC97_CLK
AA5 AC_BITCLK
Y8 AC_SDATA_OUT/GPIO
Y7 AC_SDATA_IN0/SYS_PERR*
AB8 AC_SDATA_IN1/SYS_SERR*
Y5 AC_RESET*
AA9 AC_SYNC/GPIO
C310 X_10P
R278 10K
R503 10K
R504 X_10K
R507 X_10K
R508 10K
SPDIF_OUT
SPDIF1
AB7 SPDIF0/GPIO
AC7 SPDIF1/GPIO
AC_RST*
0=MII
1=RGMII*
AC_SYNC
0=Normal operation*
1=Slave mode
AC_SDOUT
0=DISABLE_TERM(100ohm PCIE _REF)
1=ENABLE_TERM*
DEFAULT=*
SPDIF0
(SIO CLK)
1=24MHz*
0=14.318MHz
SPDIF1
(REF CLK)
1=EXTERNAL*
0=INTERNAL
<25> GPO_SLI
<4> MEM_GPIO1
<4> MEM_GPIO2
<33> BIOS_WP#
<29> LAN_RST#
AG8 GPIO_1
AB2 GPIO_2/CPU_SLP*
AB3 GPIO_3/CPU_CLKRUN*
AC2 GPIO_4/SUS_STAT*
AB1 GPIO_5/SYS_ERR*
3VDUAL
R509 10K
R288 10K
<21> RTC_RST-
AE6 LID*/GPIO
AF6 SLP_DEEP*
AD6 V3P3_DEEP
AH6 LLB*
AE2 RTC_RST*
VCC3
R2506 10K
MEM_GPIO1
L26 X_F301S0805
CP25 X_COPPER
C498 0.1u 0402
C2699 103P
C2700 X_10U/0805
AH1 +3.3V_PLL_USB
CK8-04 SLI
USB_0 P2
USB_0* P3
USB_1 P8
USB_1* P9
USB_2 R2
USB_2* R3
USB_3 T3
USB_3* R4
USB_4 U3
USB_4* U4
USB_5 U1
USB_5* U2
USB_6 T5
USB_6* T6
USB_7 T7
USB_7* T8
USB_8 U5
USB_8* V6
USB_9 V7
USB_9* V8
USB0+ USB0- USB1+ USB1- USB2+ USB2- USB3+ USB3- USB4+ USB4- USB5+ USB5- USB6+ USB6- USB7+ USB7- USB8+ USB8- USB9+ USB9-
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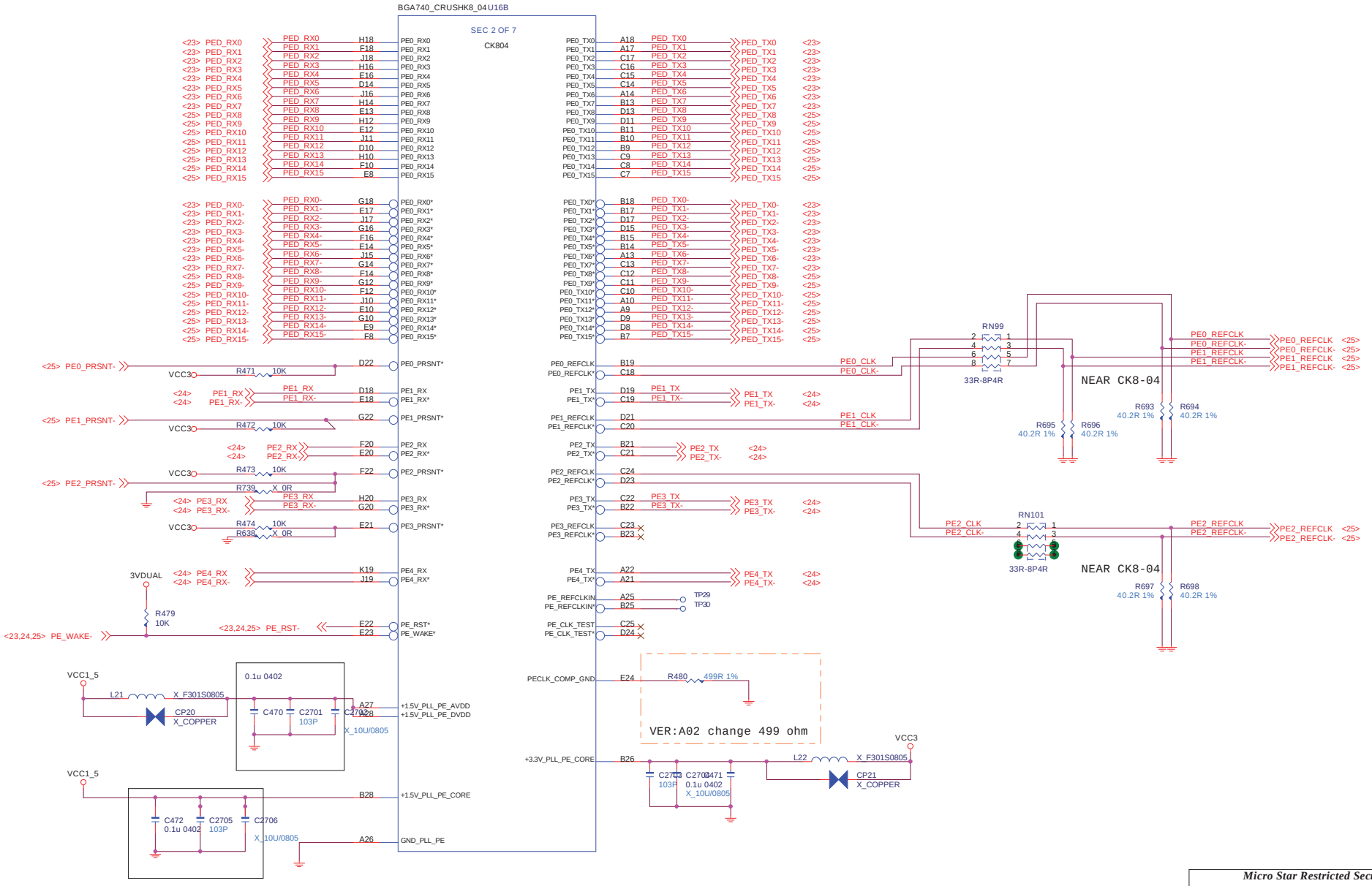
USB_OC0* V4
USB_OC1*/GPIO V5
USB_OC2*/GPIO V3
USB_OC3*/GPIO V2
USB_OC4*/GPIO AA4
USB_RBIAS V9
USB_OC#1 USB_OC#3 USB_OC#5 USB_OC#7 USB_OC#9
R273 732R 1%
+3.3V_PLL_DUAL A29
C2697 103P
C2698 102P
C300 X_10U/0805
L25 X_F301S0805
CP24 X_COPPER
3VDUAL
A20GATE/GPIO AG7
INTRUDER* AK3
EXT_SMI*/GPIO AH5
RI*/GPIO AJ3
SPKR AF3
PWRBTN* AJ2
SIO_PME*/GPIO AJ5
KBRDRSTIN*/GPIO AF2
SMB_CLK0/GPIO Y3
SMB_DATA0/GPIO W4
SMB_CLK1/GPIO W2
SMB_DATA1/GPIO W3
+3.3V_VBAT AH4
BUF_SIO_CLK AF1
SUSCLK/GPIO AG5
THERM*/GPIO AD4
RSTBTN* AJ6
SLP_S5* AJ7
SLP_S3* AH7
PWRGD_SB AG3
PWRGD AC4
FANRPM/GPIO AA3
FANCTL0/GPIO AA2
FANCTL1/GPIO AB4
TEST AE5
A20GATE INTRUDER# EXTSMI# RI# SPKR PWRBTN# SIO_PME# KBRST# SMB_MEM_CLK SMB_MEM_DATA SMBCLK SMBDATA VBAT THERM# FP_RST# SLP_S5# SLP_S3# RSMRST# ATX_PWR_OK
<33> <39> <8,9,10> <22,23,24,25,27,33,36>
R266 1M
VBAT
R269 22 SIO_24M
C312 X_10P
R259 X_22 SUSCLK
C302 X_10P
R281 1K
Giga-Lan not use, pulldown below
R621 X_10K MII_VREF
RN580
RGMIITXCLK RGMII_RXCTL RGMII_RXCLK MII_MDC
X_10K-8P4R
RN581
RGMII_RX1 RGMII_RX3 RGMII_RX2 RGMII_RX0
X_10K-8P4R
3VDUAL
D44 BAV99W_SOT323
D45 BAV99W_SOT323
RN84
SMB_MEM_DATA SMBCLK SMBDATA SMB_MEM_CLK
VCC_DDR 3VDUAL
2.7K-8P4R
EXTSMI# R618 4.7K 3VDUAL
THRM# R619 4.7K VCC3
SLP_S5# R639 X_10K
SLP_S3# R640 X_10K
SIO_PME# R641 10K
RI# R642 10K
3VDUAL
RN80 RN85 RN86 RN79 RN103
USB1+ USB1- USB0+ USB0-
USB2+ USB2- USB3- USB3+
USB7- USB7+ USB6- USB6+
USB5+ USB5- USB4+ USB4-
USB9+ USB9- USB8+ USB8-
15K-8P4R
SPEAKER STRAOS
ROM TABLE SELECT
0=USER
1=SAFE (DEFAULT)
VCC3
R510 1K
SPKR
R511 X_1K
Micro Star Restricted Secret
Title
NVIDIA CrushK8-04 Part 5
Rev 0A
Document Number MS-9620
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Tuesday, February 15, 2005
Sheet 17 of 44
http://laptop-motherboard-schematic.blogspot.com/



Micro Star Restricted Secret	
Title: NVIDIA CrushK8-04 Part 2	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
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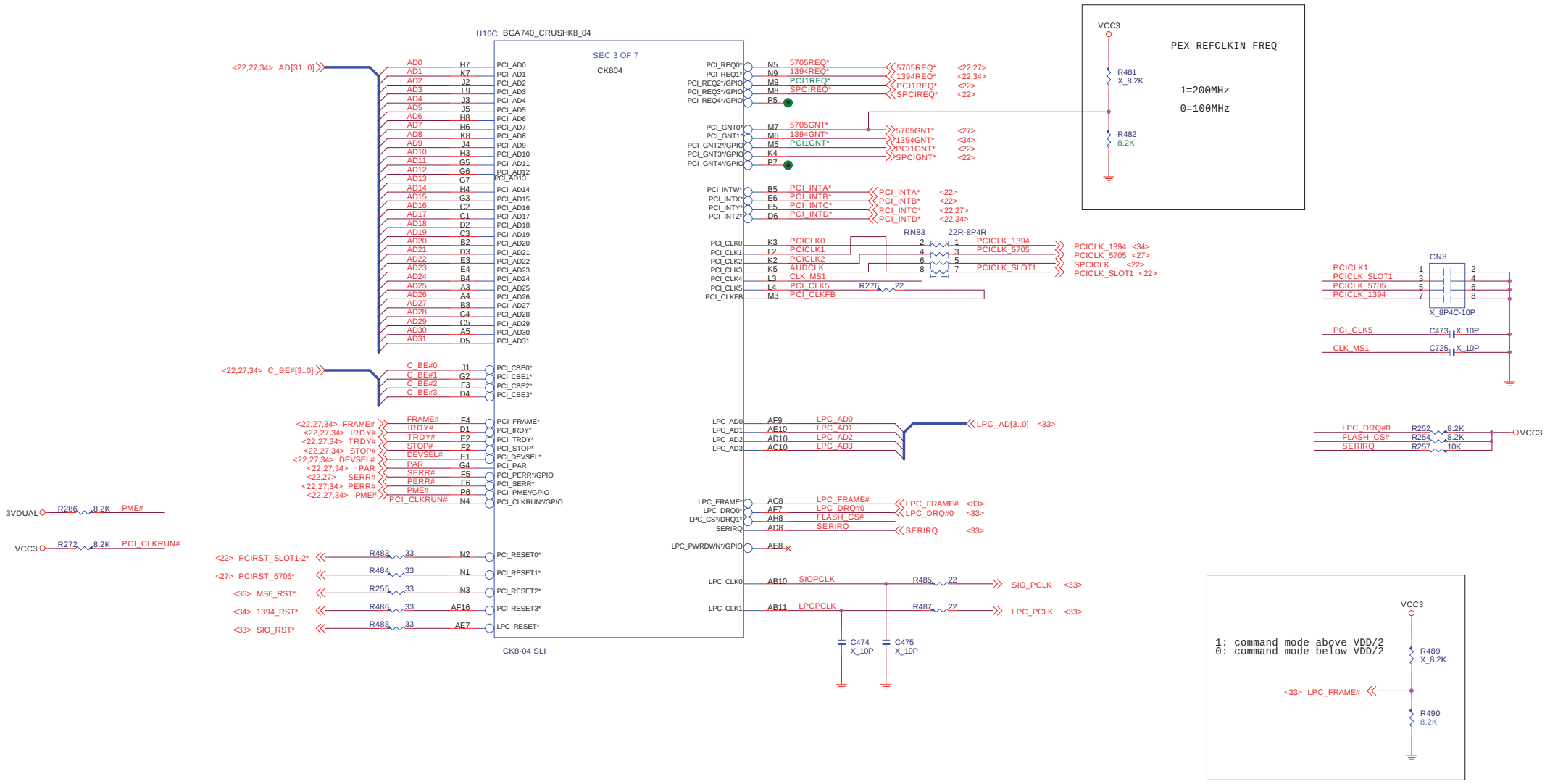
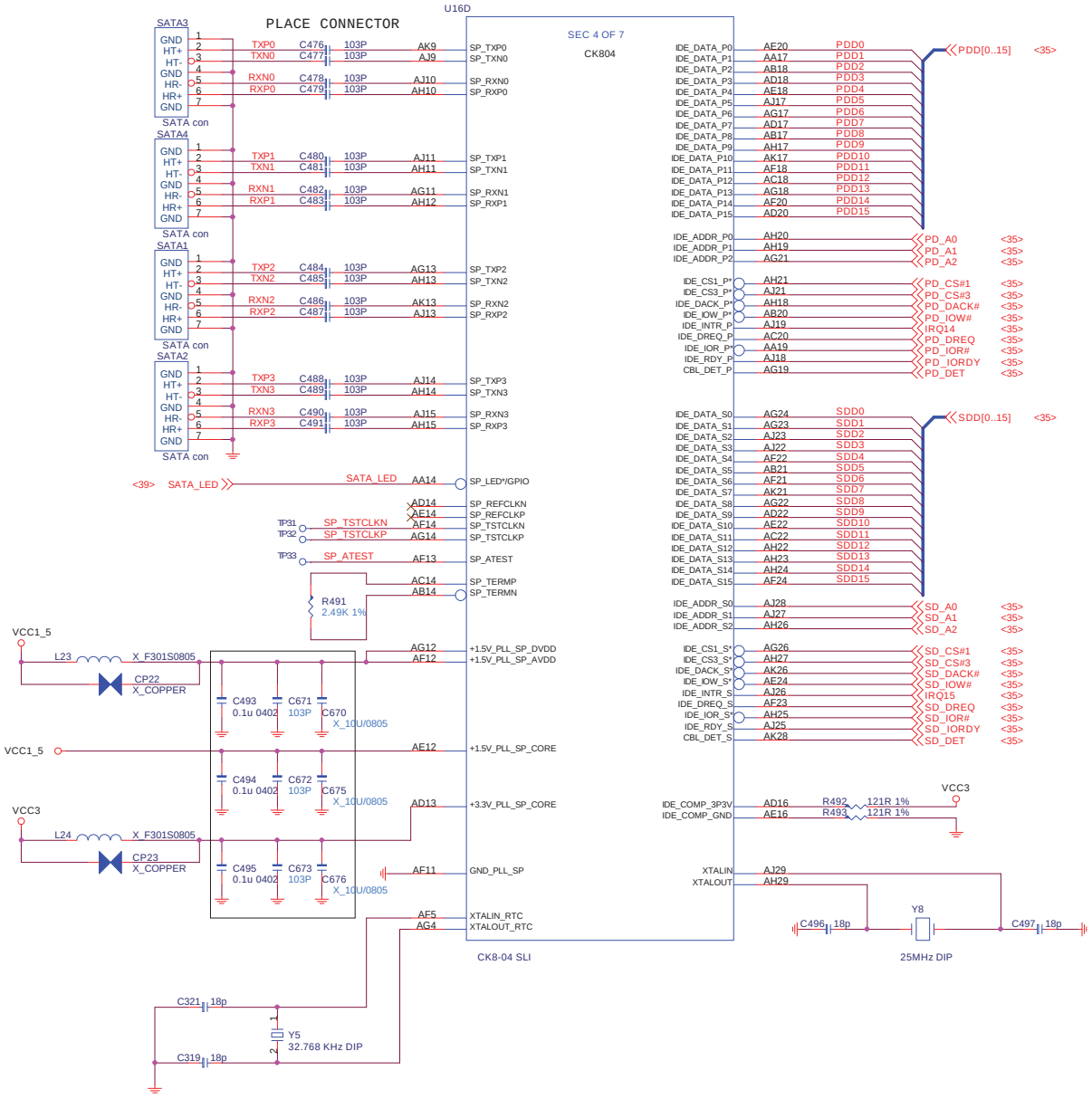


http://laptop-motherboard-schematic.blogspot.com/



Micro Star Restricted Secret

Title	NVIDIA CrushK8-04 Part 4
Rev	0A
Document Number	MS-9620
Last Revision Date:	Tuesday, February 15, 2005
Sheet	20 of 44

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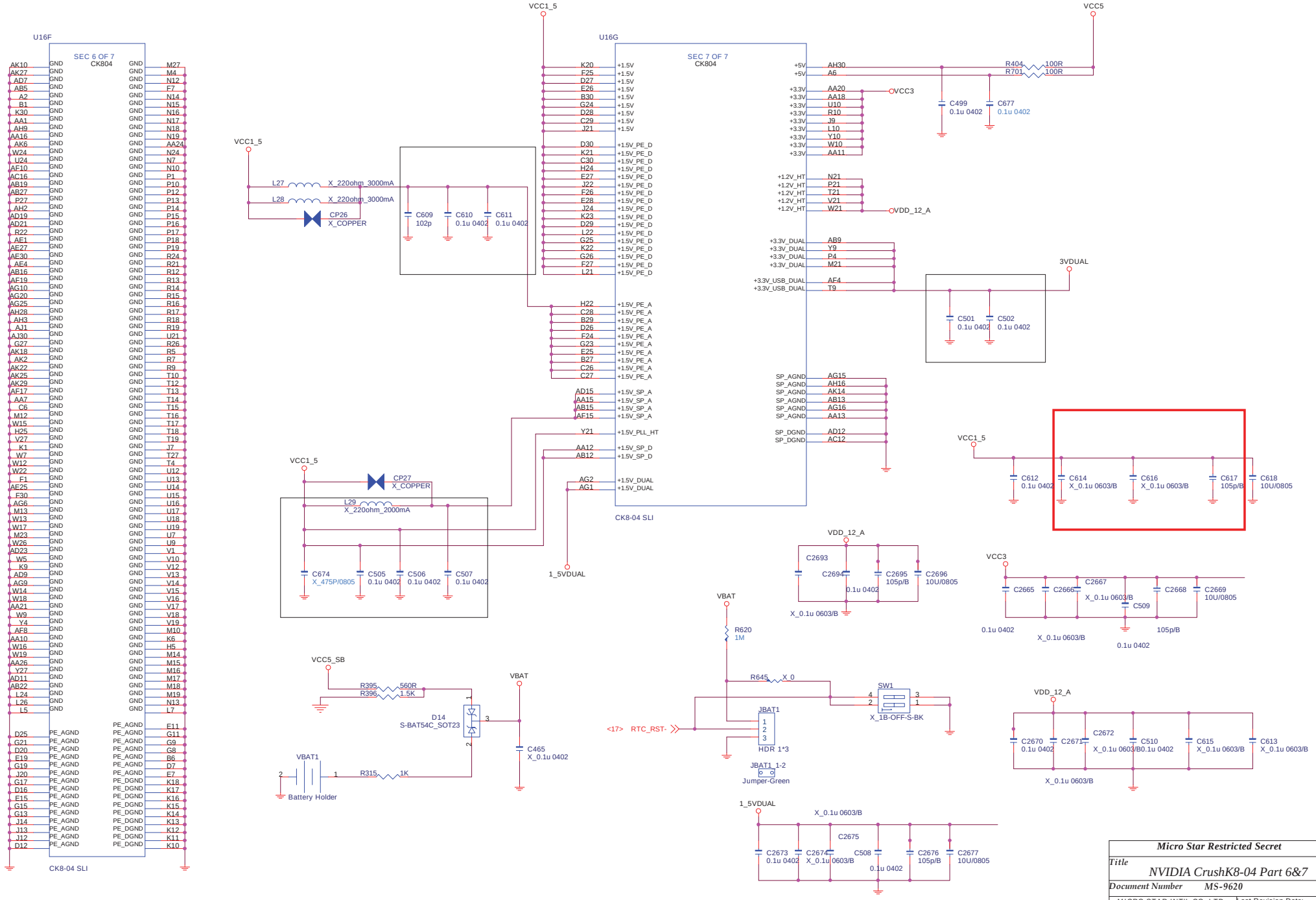

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Micro Star Restricted Secret	
Title: NVIDIA CrushK8-04 Part 6&7	Rev: 0A
Document Number: MS-9620	
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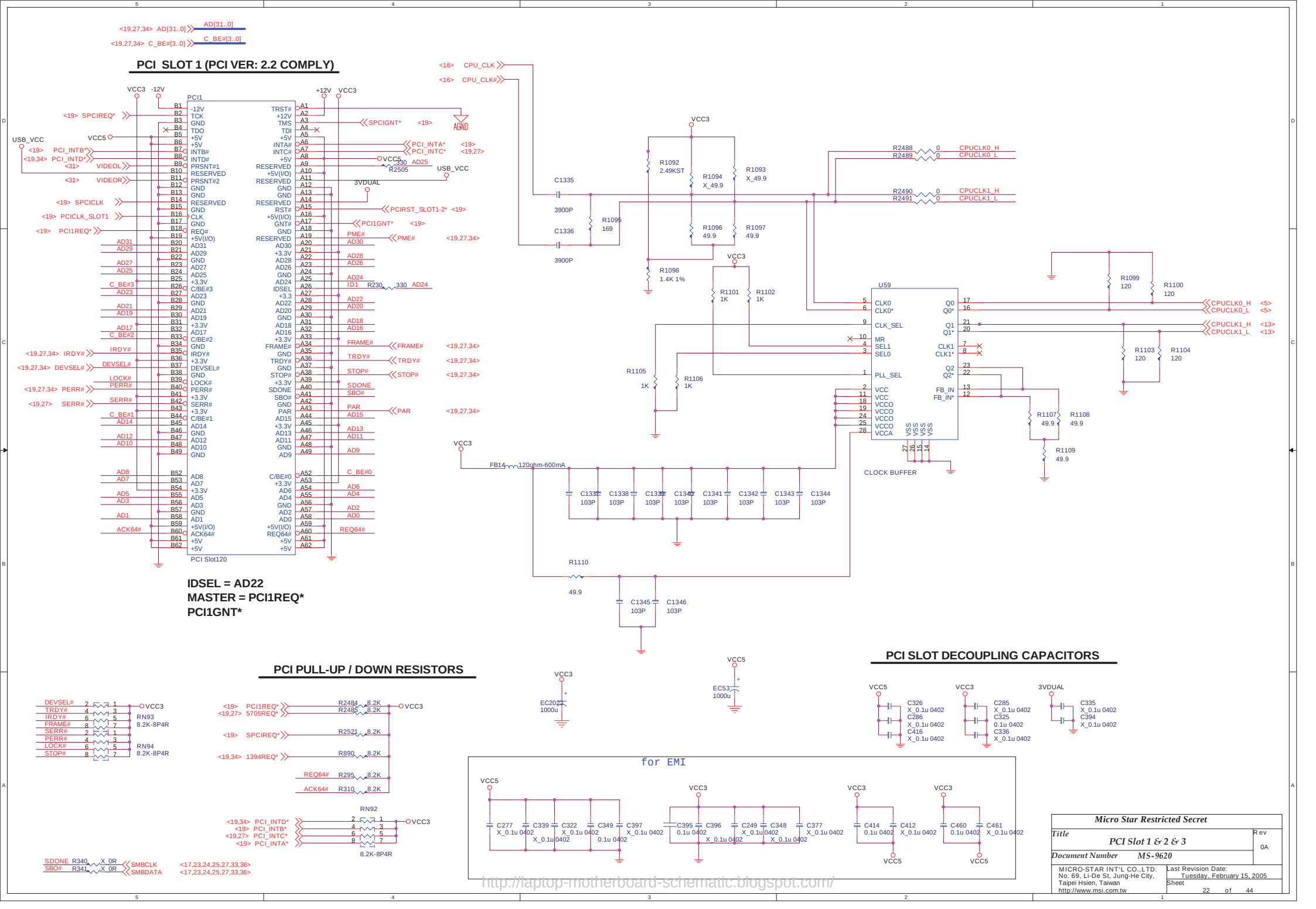
	Sheet 21 of 44


PCI SLOT 1 (PCI VER: 2.2 COMPLY)
IDSEL = AD22
MASTER = PCI1REQ*
PCI1GNT*
PCI PULL-UP / DOWN RESISTORS
PCI SLOT DECOUPLING CAPACITORS
for EMI
CLOCK BUFFER
PCI Slot120
Micro Star Restricted Secret
Title
PCI Slot 1 & 2 & 3
Rev
0A
Document Number
MS-9620
MICRO-STAR INT'L CO., LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
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Tuesday, February 15, 2005
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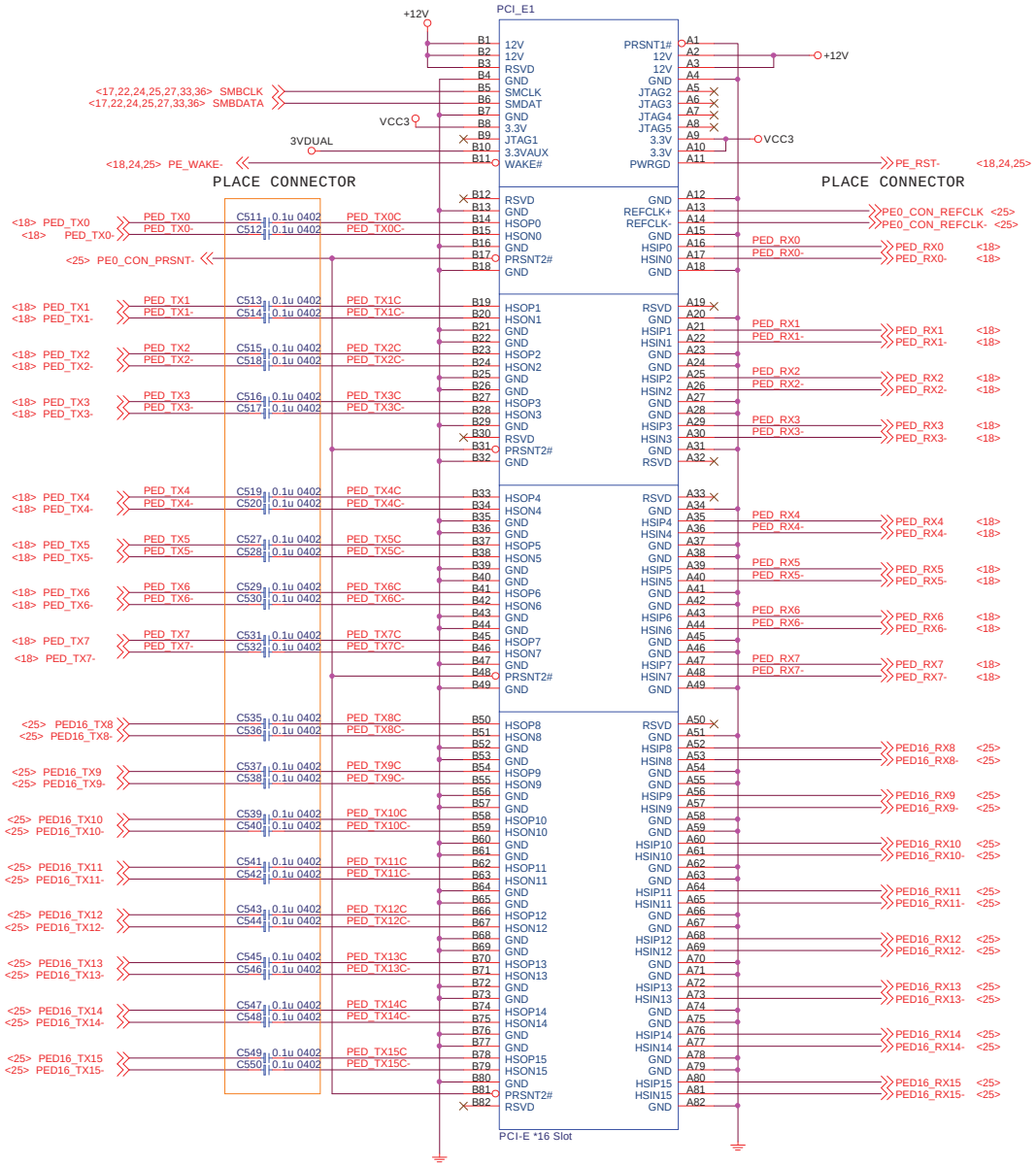
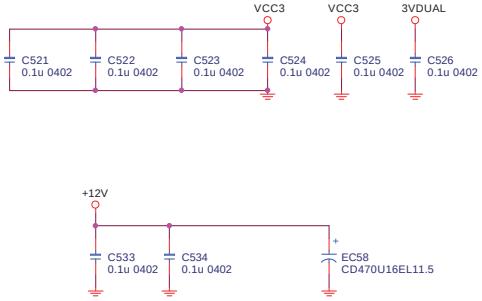
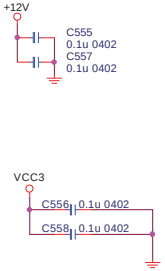
PCI-E *16







Micro Star Restricted Secret	
Title: PCI EXPRESS X16 POARTA	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
	Sheet 23 of 44

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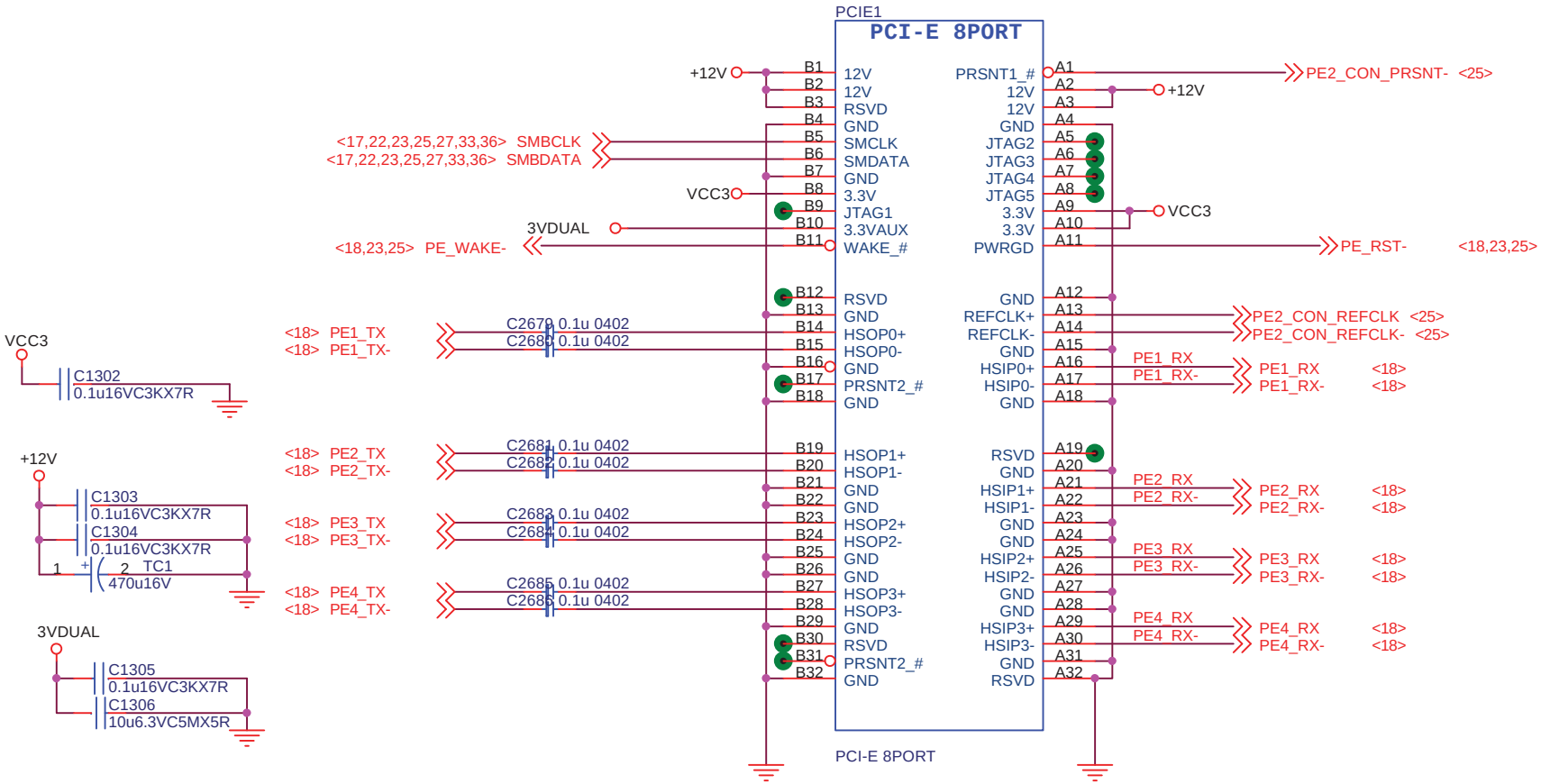
PCI-E *4



25 W limit
+3.3V 3A
+12V 2.1A
+3.3VDUAL 375mA

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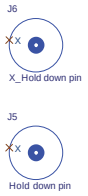
Title: PCI-E SLOT		
Size: A4	Document Number: MS-9620	Rev: 0A
Date: Tuesday, February 15, 2005	Sheet 24 of 44	

PCI-E *8



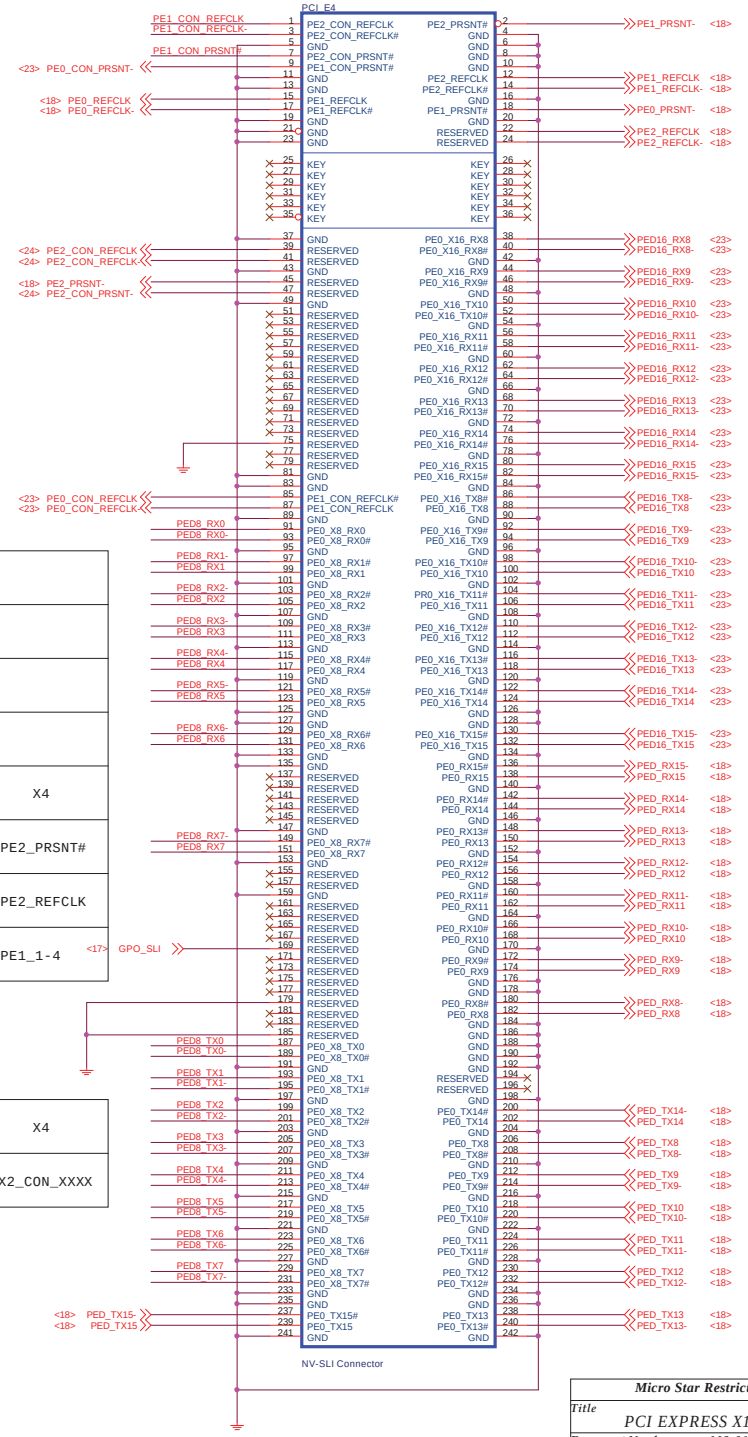
From CK8-04 Pro

	X16	X4	
PRSNT#	PE0_PRSNT#	PE1_PRSNT#	
REFCLK	PE0_REFCLK	PE1_REFCLK	
LANE TX/RX	PE0_0-15	PE1_1-4	
	X8	X8	X4
PRSNT#	PE1_PRSNT#	PE0_PRSNT#	PE2_PRSNT#
REFCLK	PE1_REFCLK	PE0_REFCLK	PE2_REFCLK
LANE TX/RX	PE0_0-7	PE0_8-15	PE1_1-4

Connect to PCIE Slot

	X16	X8	X4
Naming	XX0_CON_XXXX	XX1_CON_XXXX	XX2_CON_XXXX

NV-SLI Connector



Normal Mode = Low
SLI Mode = High

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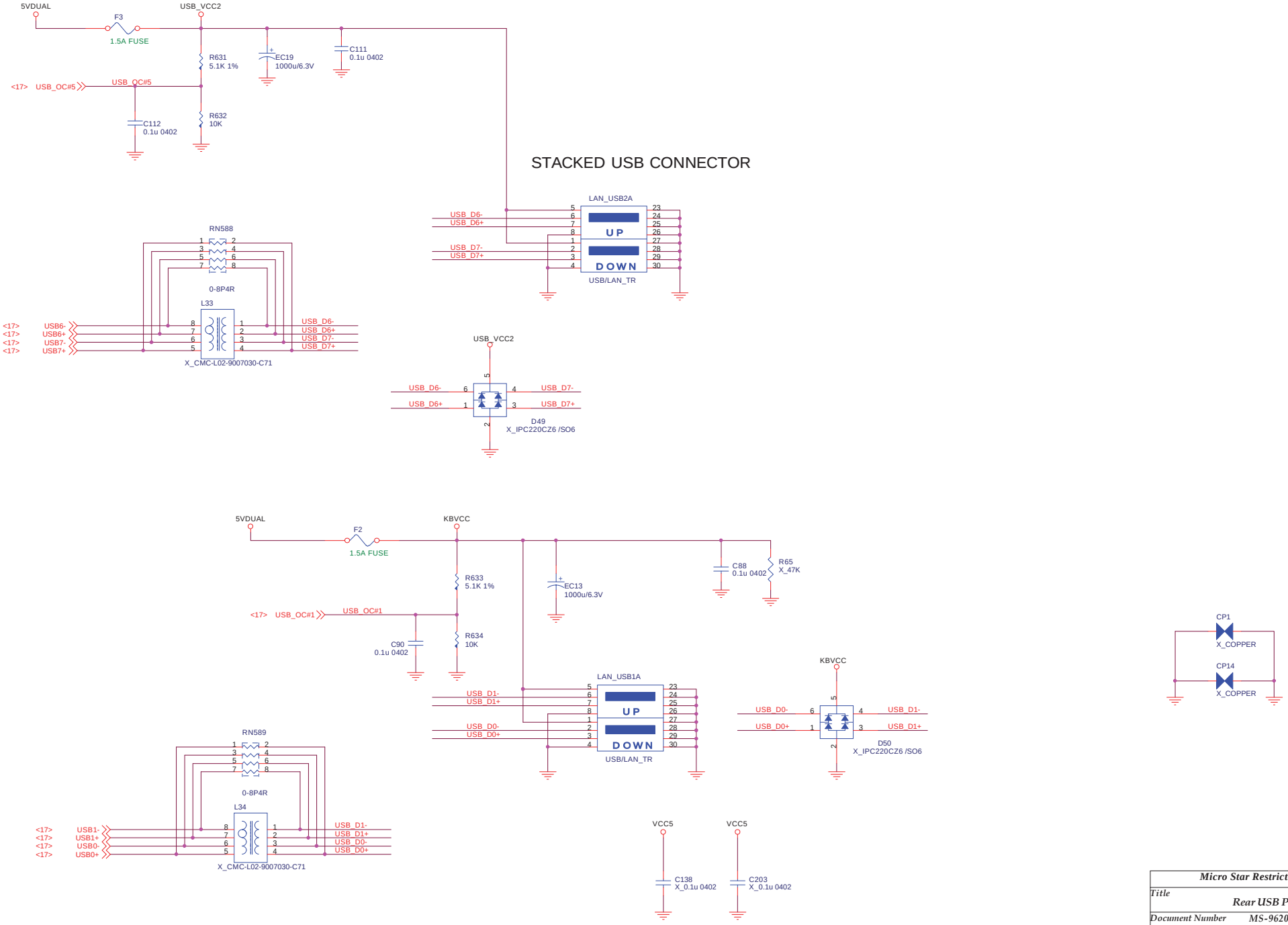
Micro Star Restricted Secret		
Title	*PCI EXPRESS X1 POART*	Rev 0A
Document Number	*MS-9620*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005	Sheet 25 of 44

REAR USB PORT



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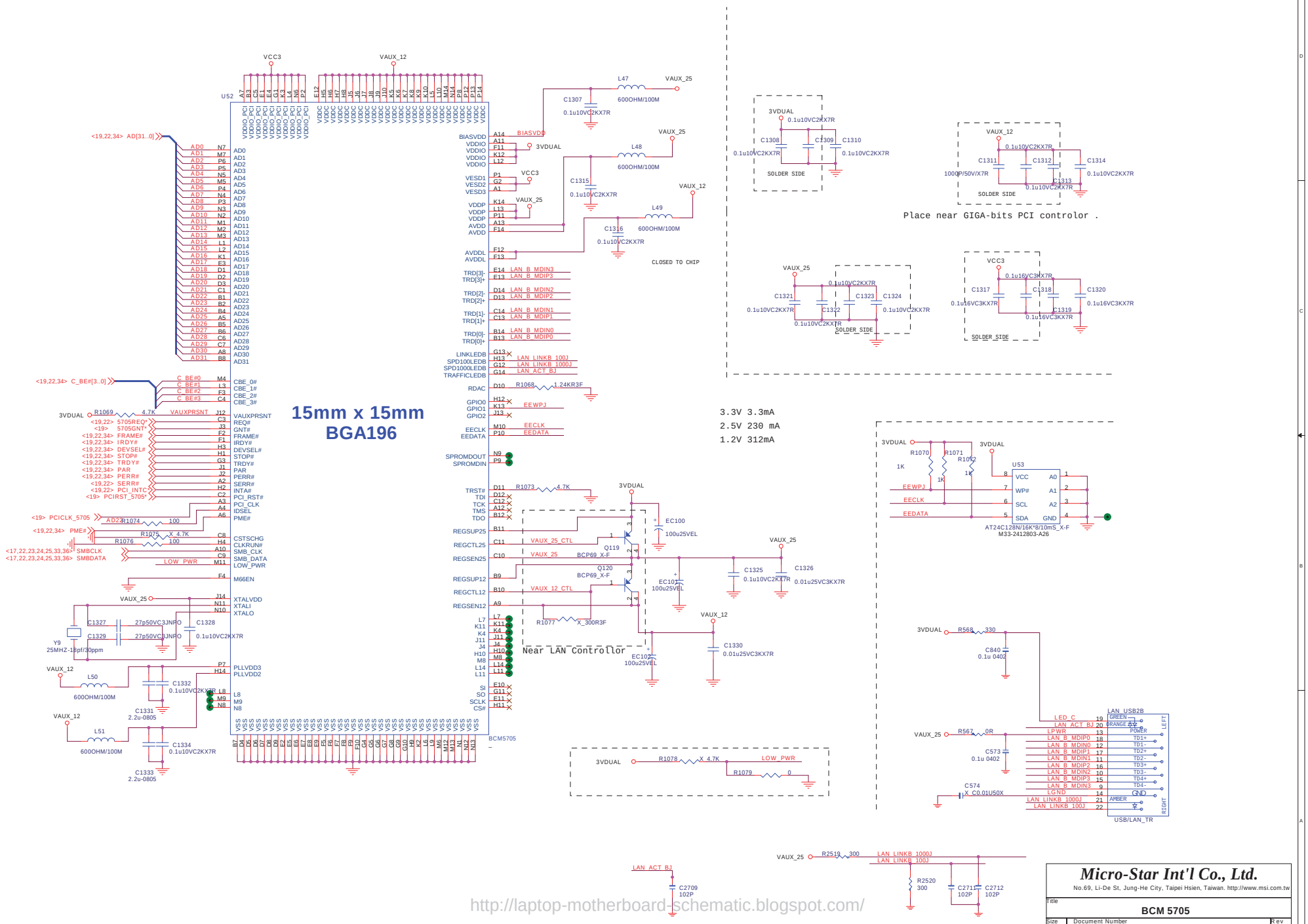
Micro Star Restricted Secret	
Title	*Rear USB Port*
	Rev 0A
Document Number	*MS-9620*
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
	Sheet 26 of 44



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Micro-Star Int'l Co., Ltd.

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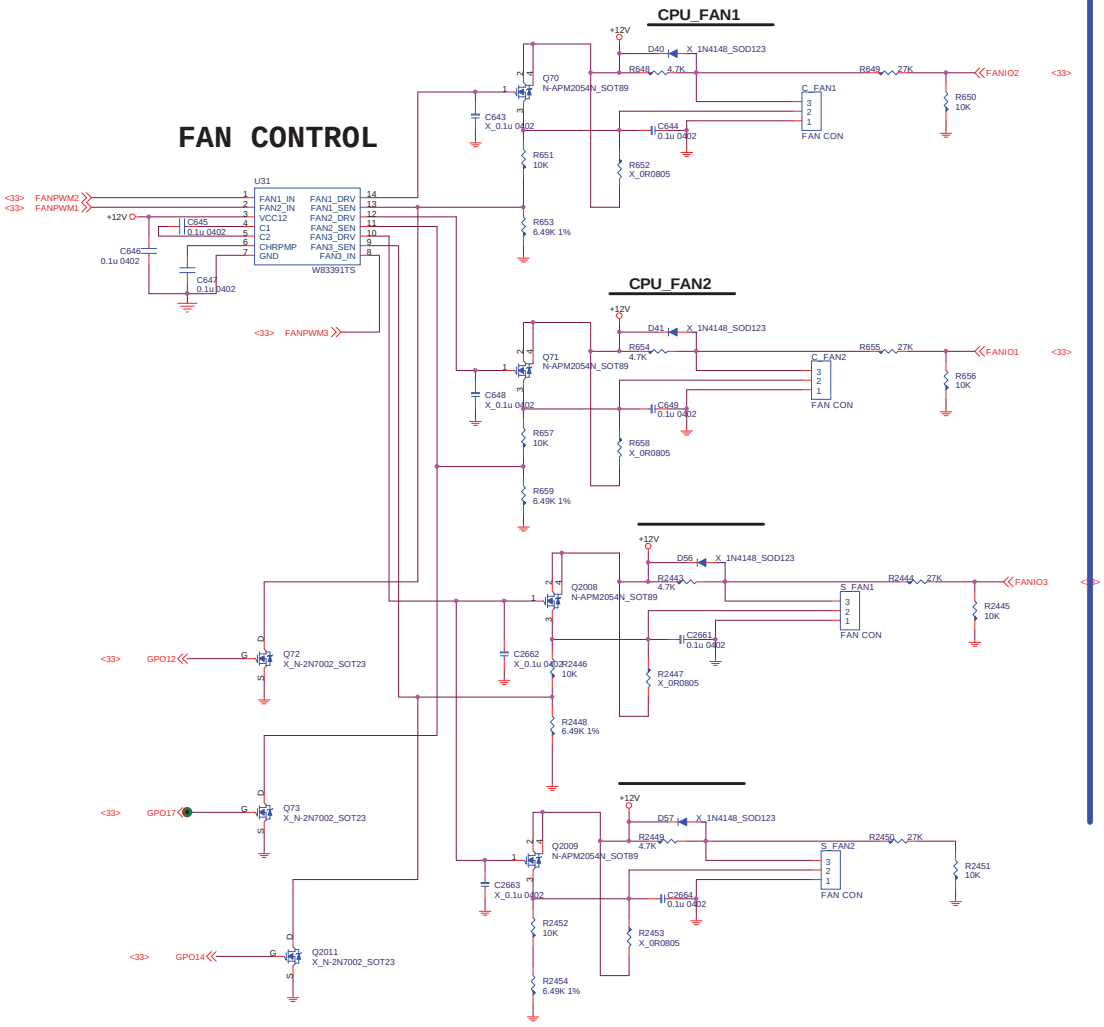
Title	BCM 5705	
Size C	Document Number MS-9620	Rev 0A
Date: Tuesday, February 15, 2005	Sheet 27 of 44	



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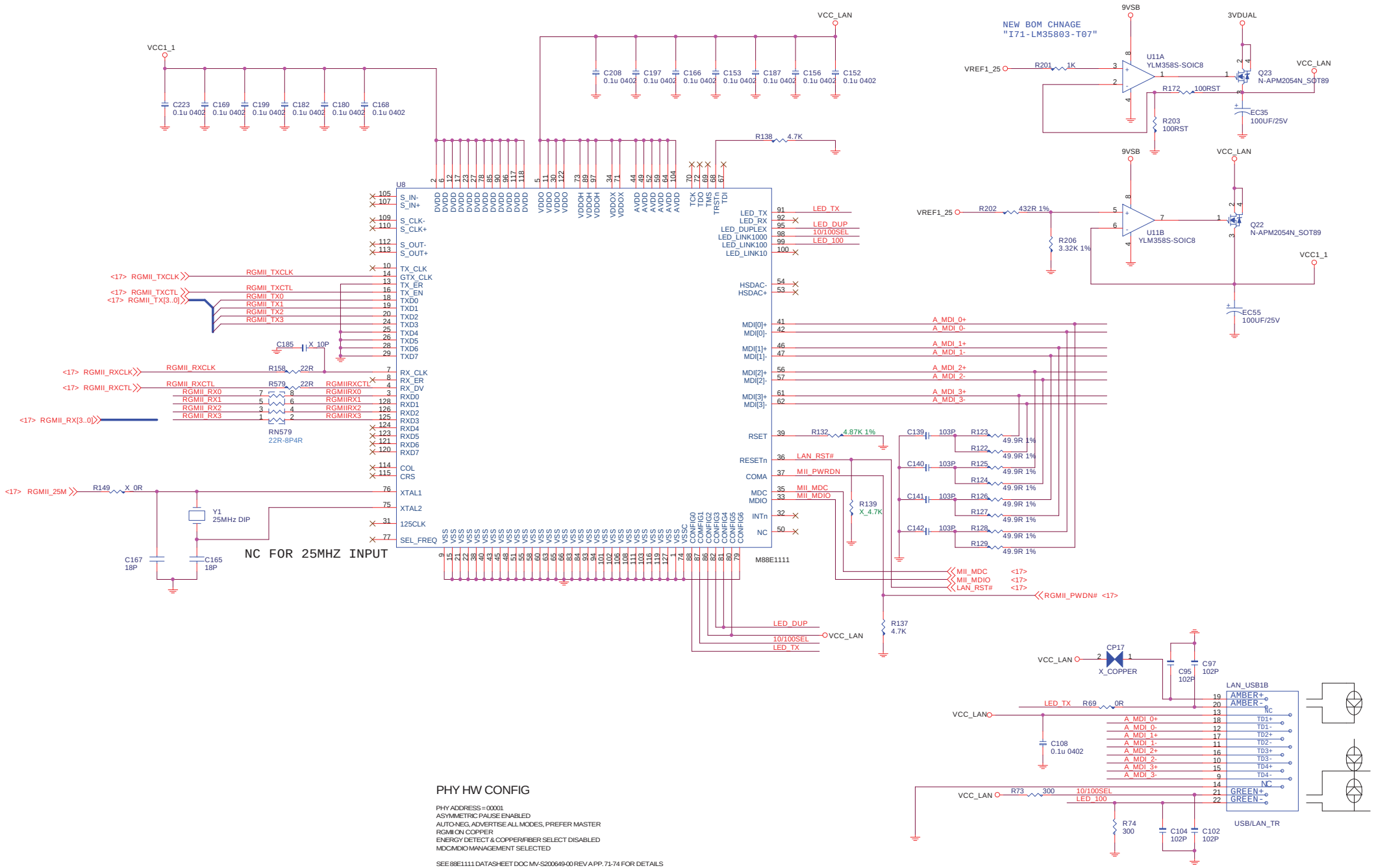
NEW BOM CHNAGE
"I71-LM35803-T07"
U8
M88E1111
NC FOR 25MHZ INPUT
PHY HW CONFIG
PHY ADDRESS = 00001
ASYMMETRIC PAUSE ENABLED
AUTO-NEG, ADVERTISE ALL MODES, PREFER MASTER
RGMII ON COPPER
ENERGY DETECT & COPPER/FIBER SELECT DISABLED
MDC/MDIO MANAGEMENT SELECTED
SEE 88E1111 DATASHEET DOC MV-S200649-00 REV A PP. 71-74 FOR DETAILS
Micro Star Restricted Secret
88E1111CAA LAN
MS-9620
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
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Tuesday, February 15, 2005
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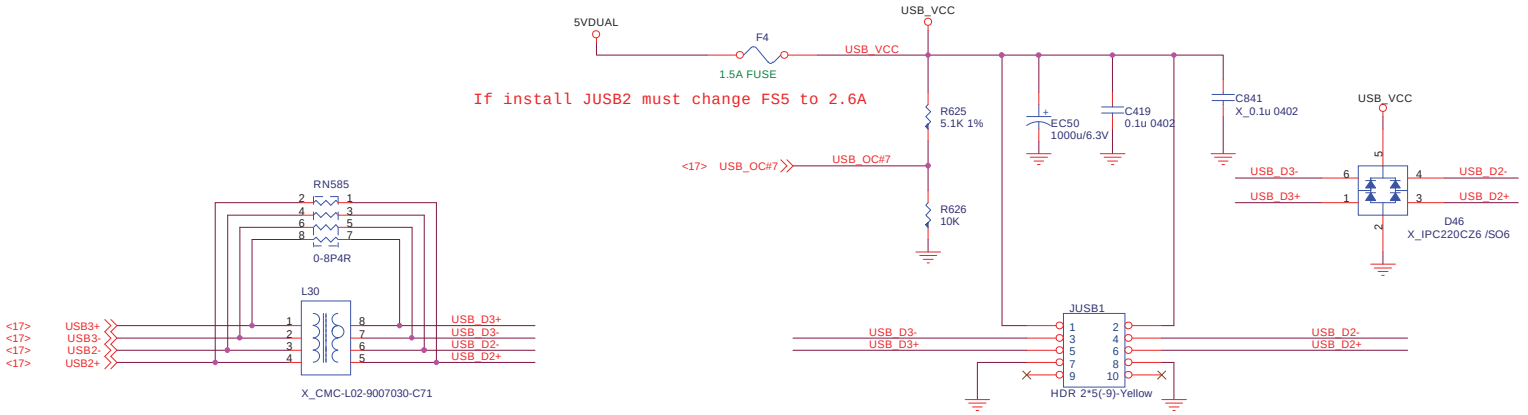
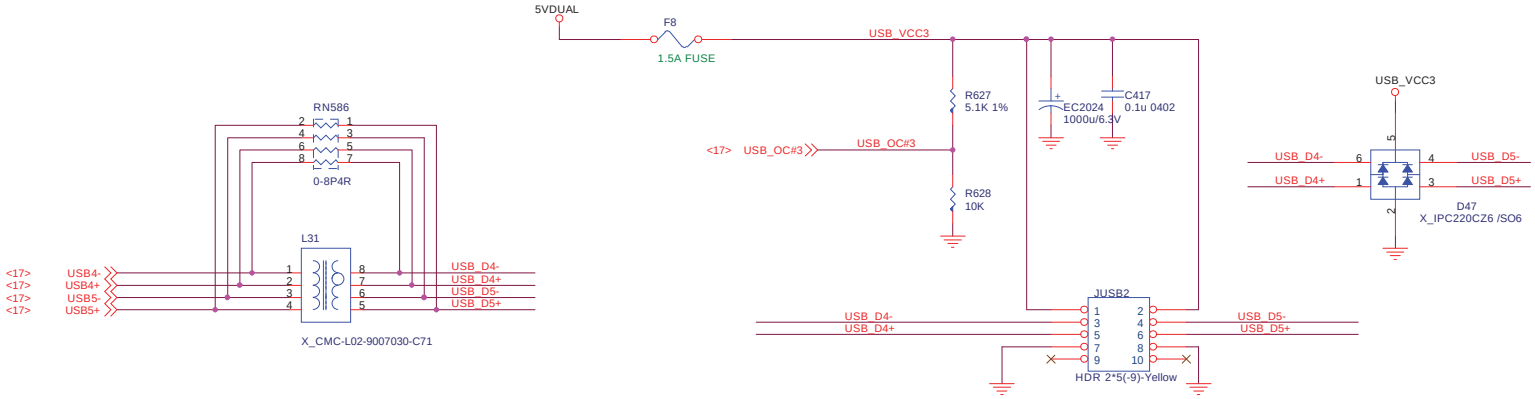
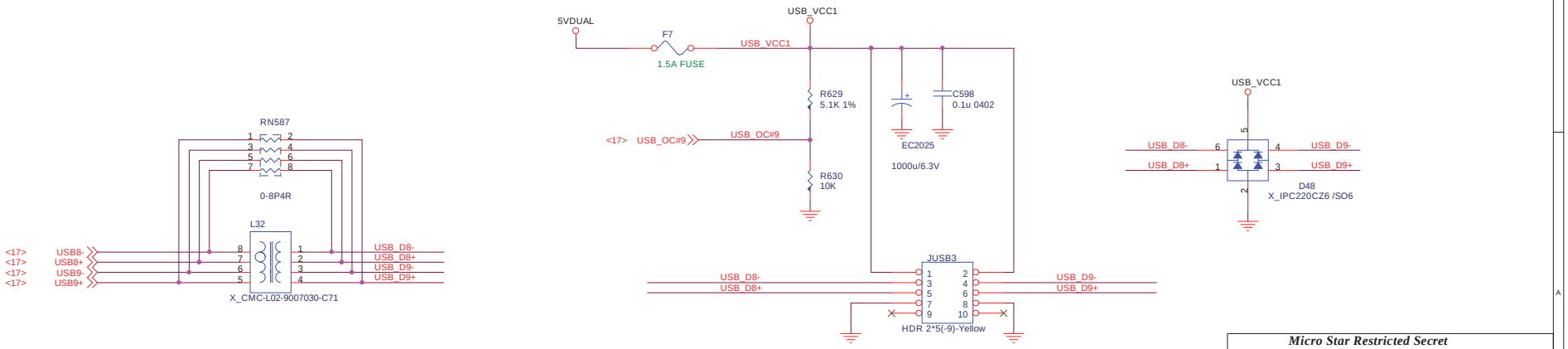
FRONT USB PORT



USB 2.0 PIN HEADER
(Yellow)



USB 2.0 PIN HEADER
(Yellow)



USB 2.0 PIN HEADER
(Yellow)

*** USB Trace width : 7.5 mils**
*** USB Trace Spacing : 20 mils**
*** Differential USB Signlas Trace, Spacing : 7.5 mils**

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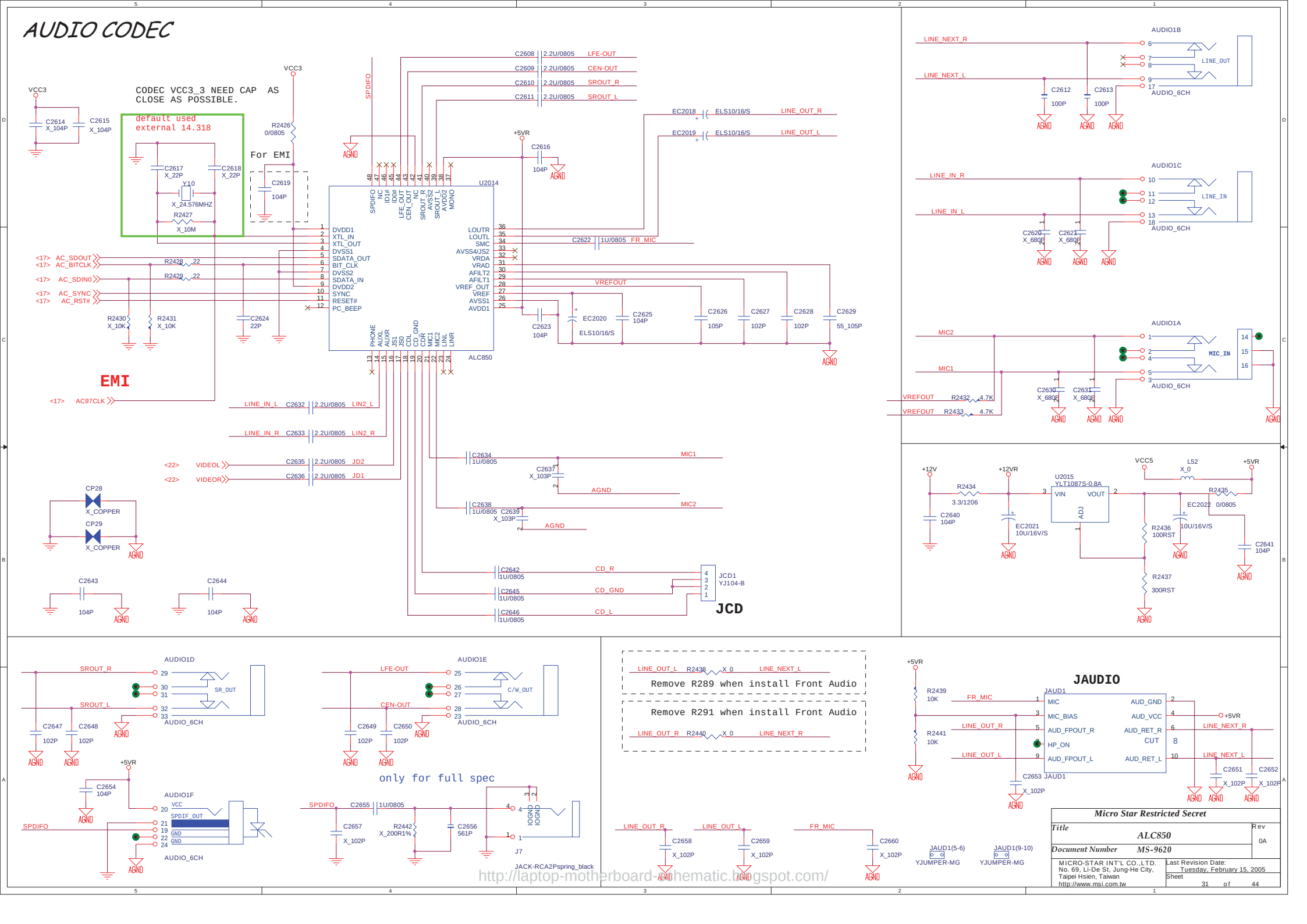
Micro Star Restricted Secret	
Title: Front USB Port	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
	Sheet 30 of 44

AUDIO CODEC



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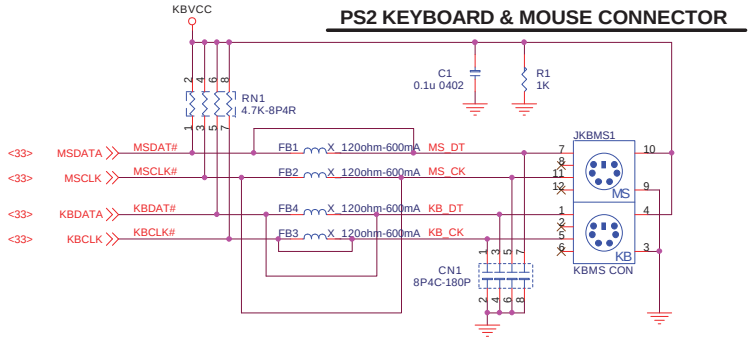
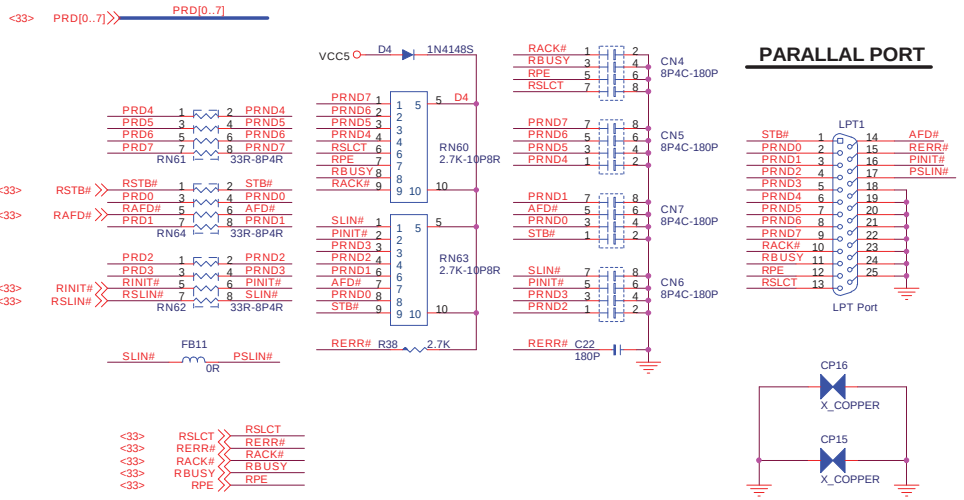
KB/MS/LPT/COM Port/FAN

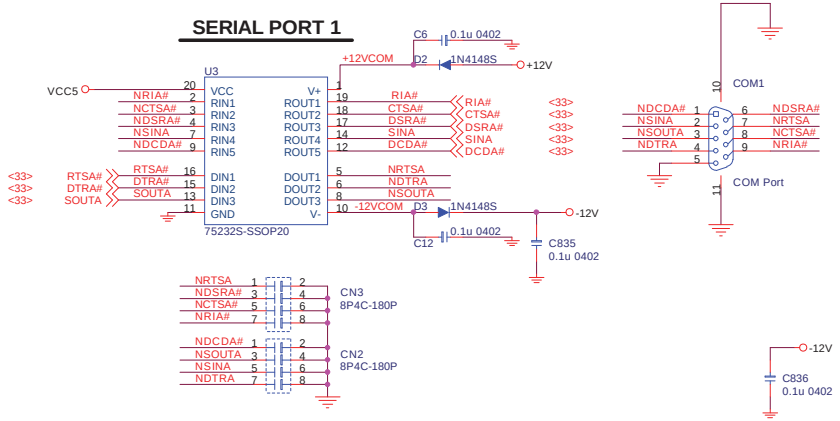
PS2 KEYBOARD & MOUSE CONNECTOR

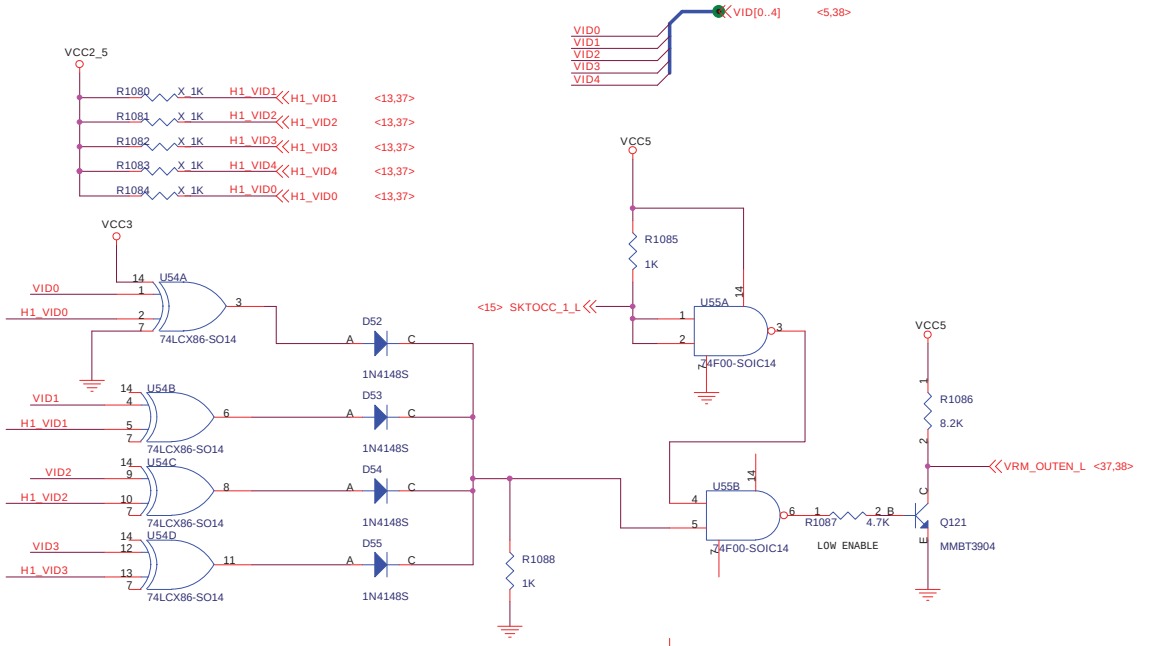


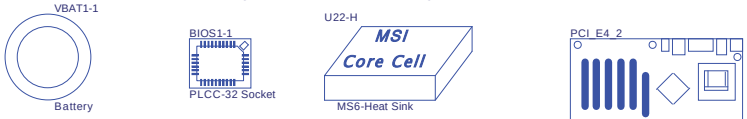
PARALLAL PORT

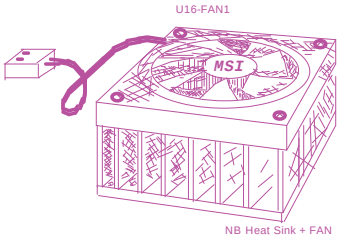


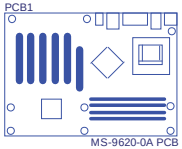
SERIAL PORT 1

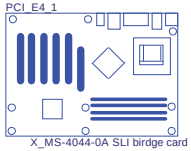












Micro Star Restricted Secret	
Title: KB/MS/LPT/COM Port/FAN	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
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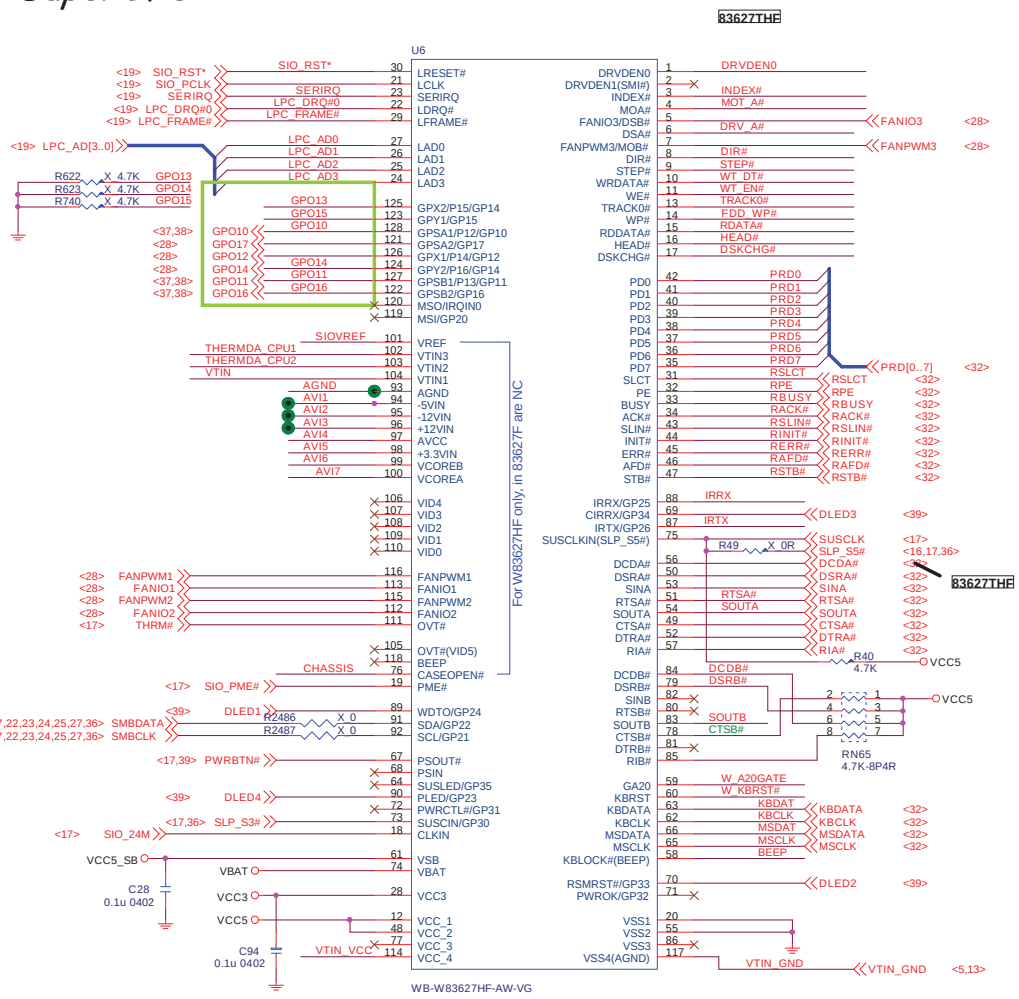
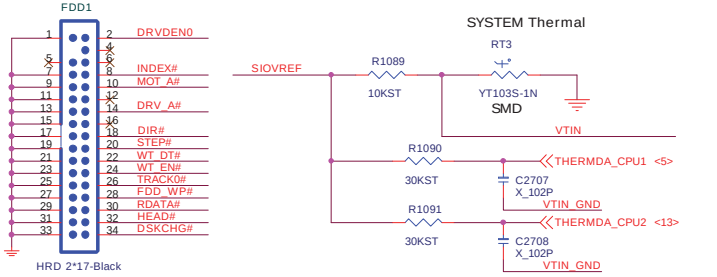
Super I/O

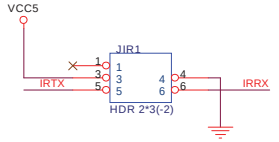
LPC SUPER I/O W83627F/HF/THF



FLOPPY CONNECTOR

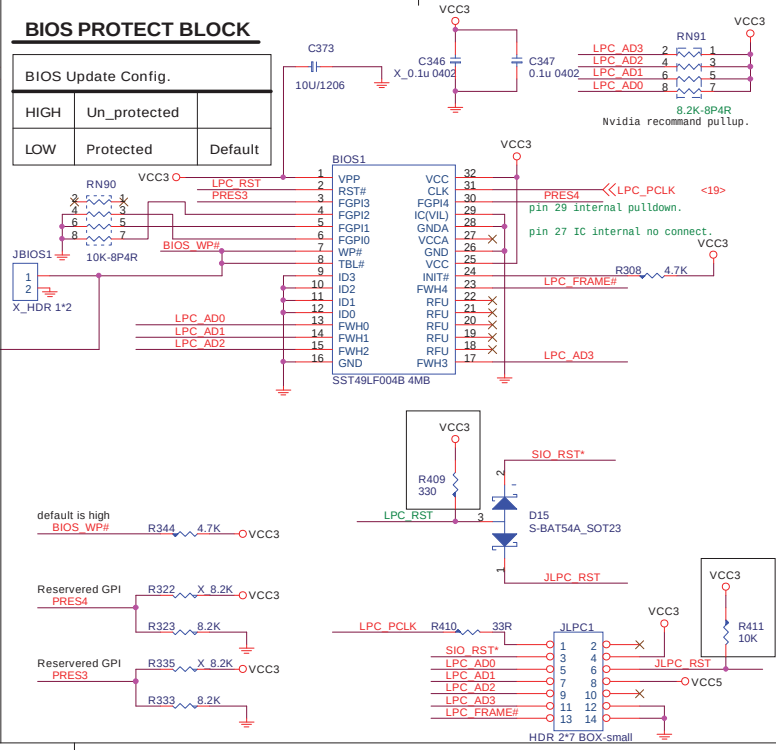


Intel Front IR Header



BIOS PROTECT BLOCK

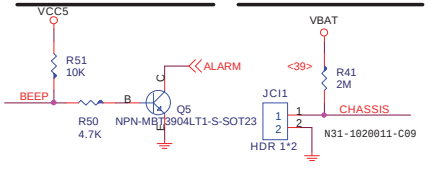
BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default



LPC I/O STRAPPING RESISTOR

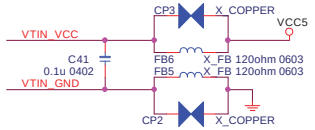
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

SPEAKER BLOCK



Chasiss Intrusion

Thermal Resistor



NOTE: LOCATE CLOSE STATUS PANEL

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Micro Star Restricted Secret	
Title: W627THF LPC I/O / FWH	Rev: 0A
Document Number: MS-9620	
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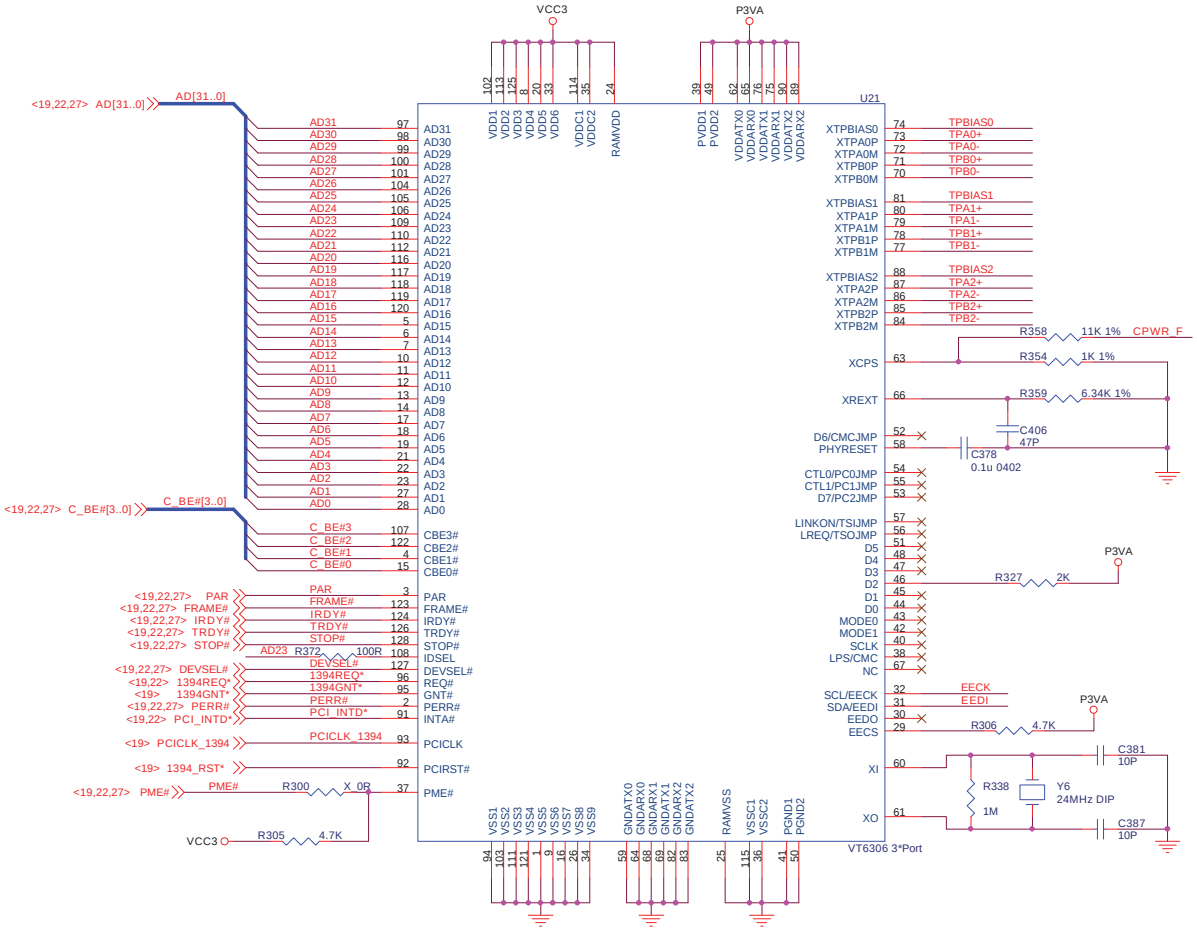
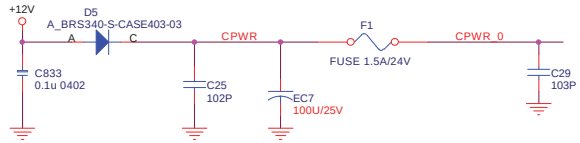
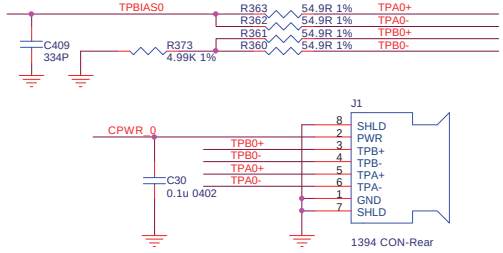
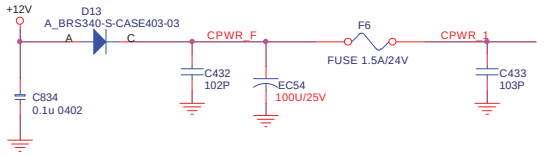
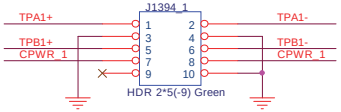
1394a OHCI Link Layer Controller

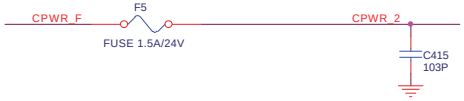


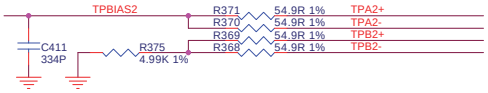


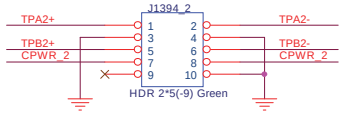




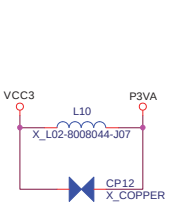


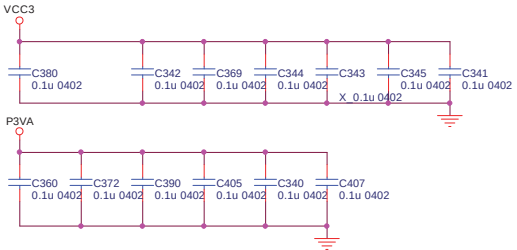


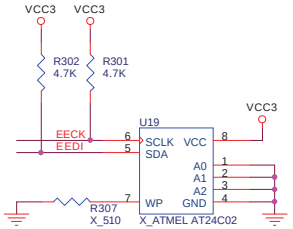




For Intel 1394 pinheader







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Micro Star Restricted Secret	
Title: *1394a Link Layer Controller*	Rev: 0A
Document Number: *MS-9620*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
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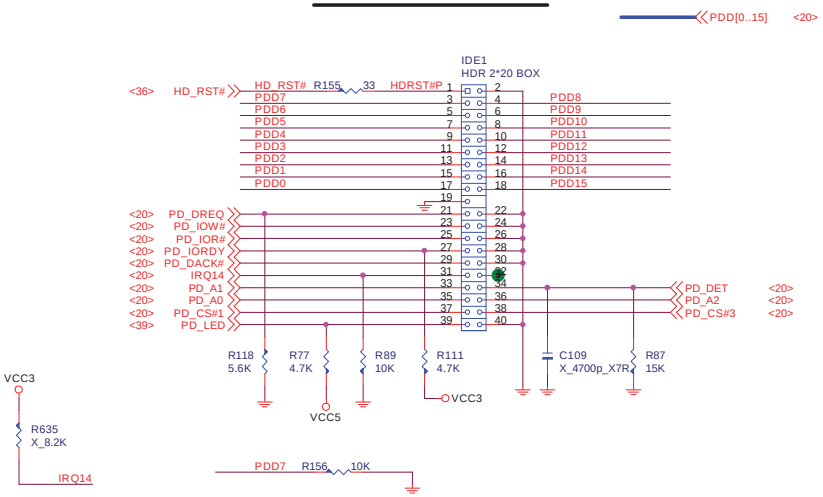
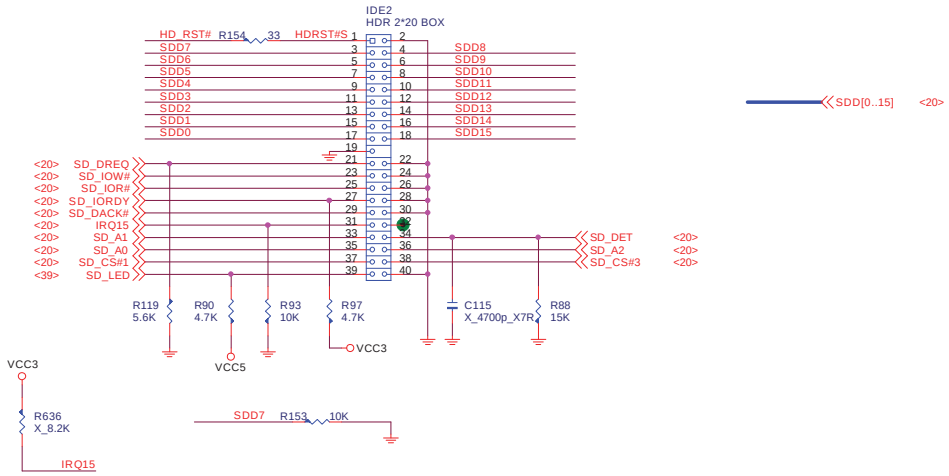
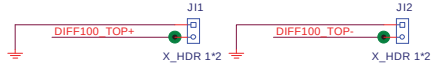
ATA 33/66/100 Connector

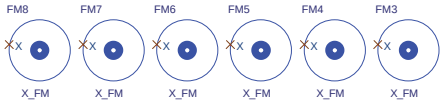
PRIMARY IDE BLOCK



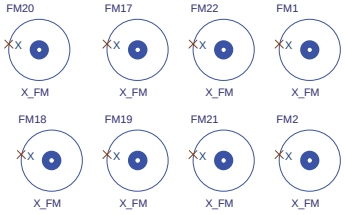
SECONDARY IDE BLOCK



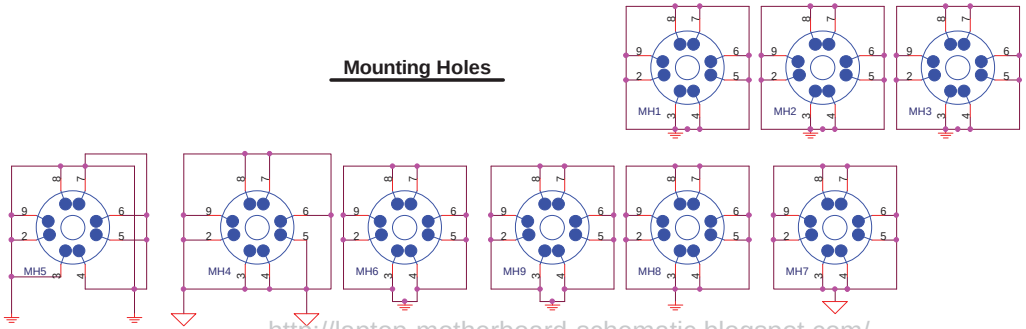




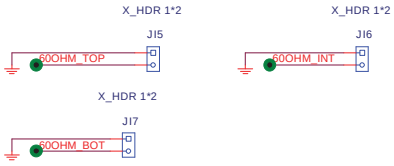
Optics Orientation Holes



Mounting Holes



Simulation



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Micro Star Restricted Secret	
Title: ATA 33/66/100 Connector	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
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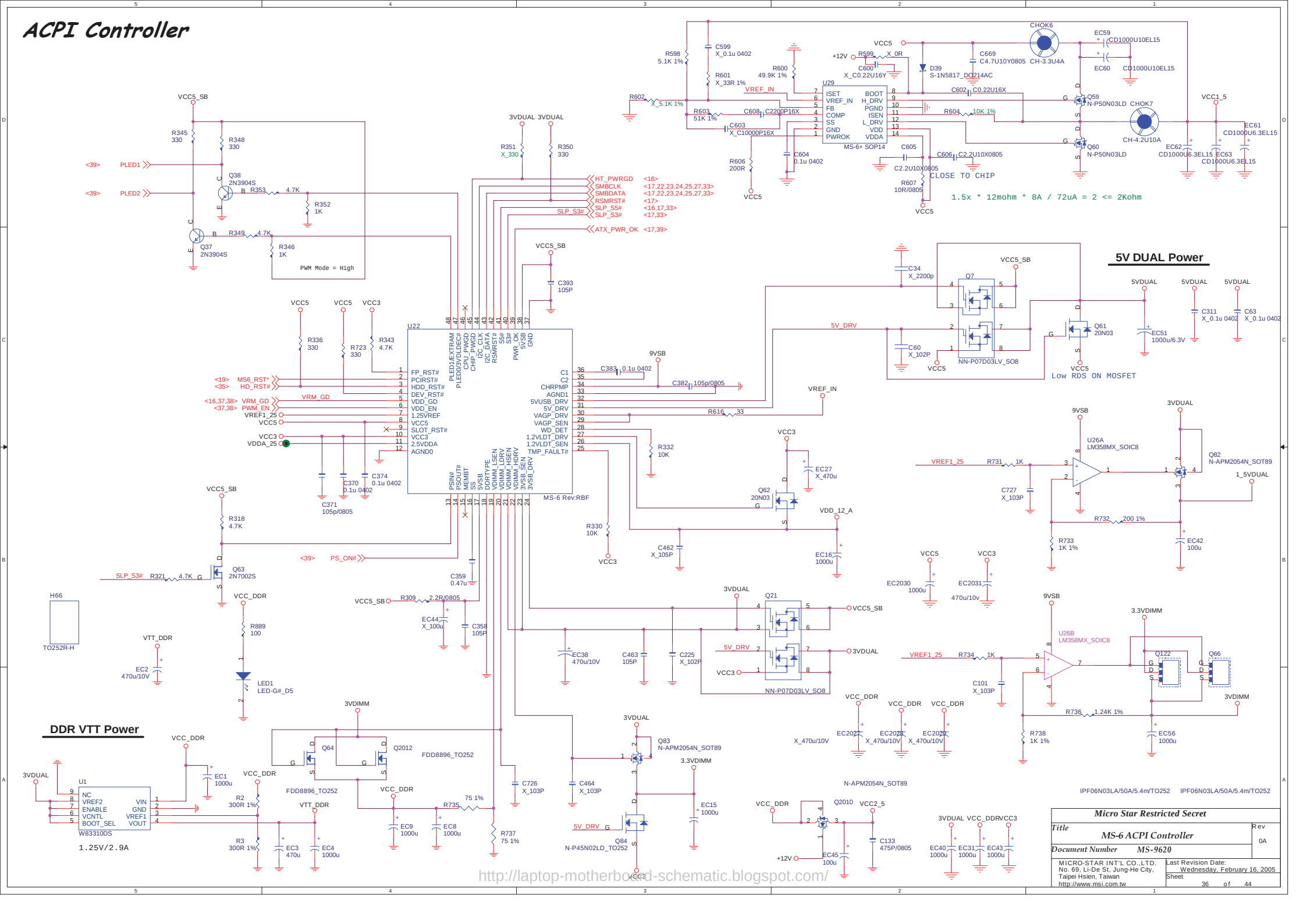
ACPI Controller



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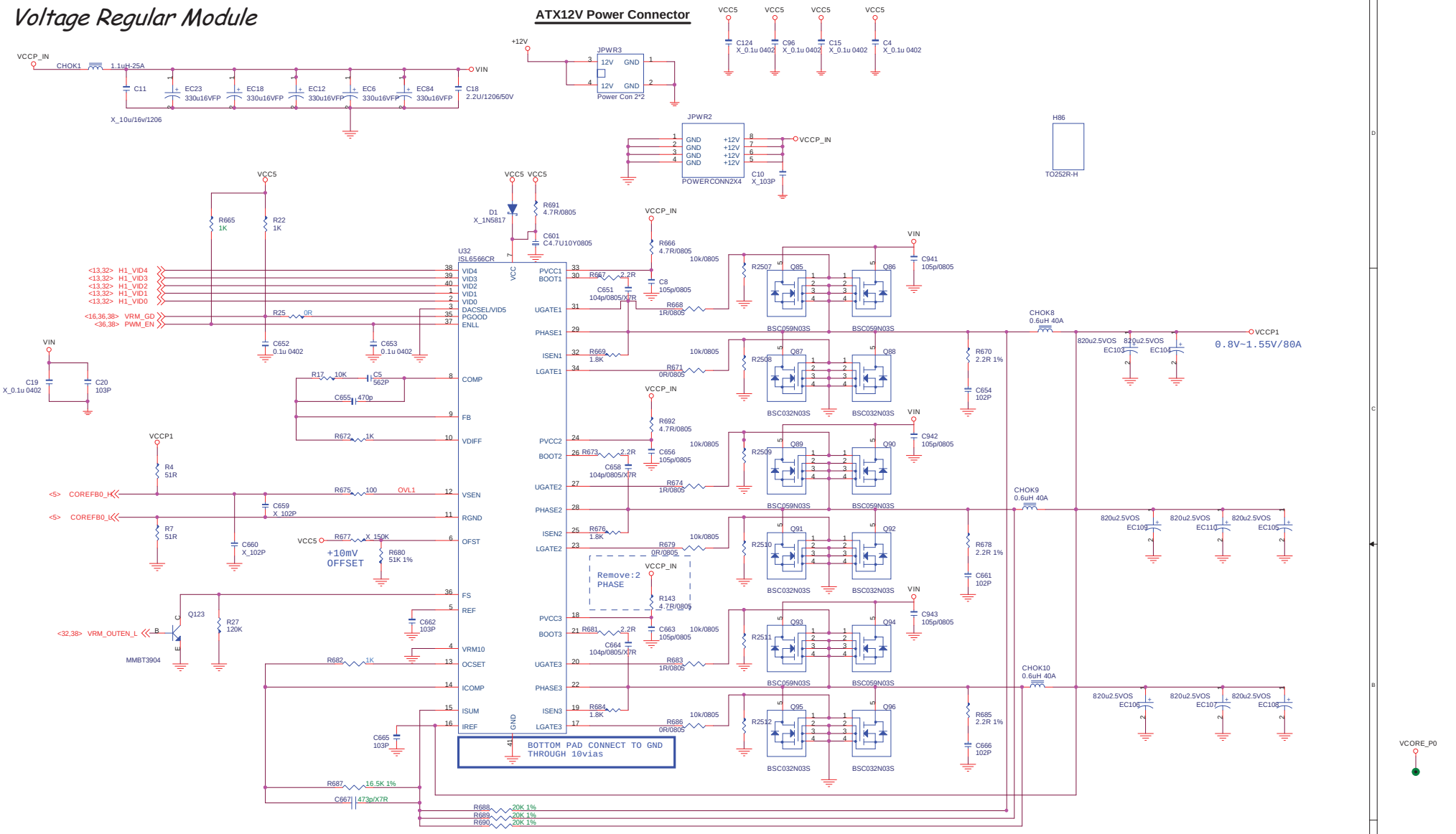
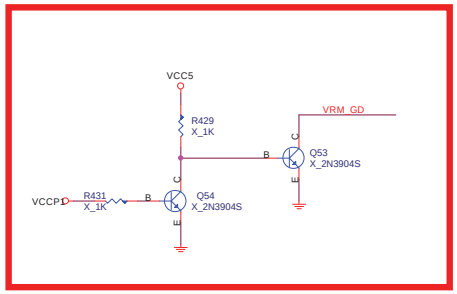
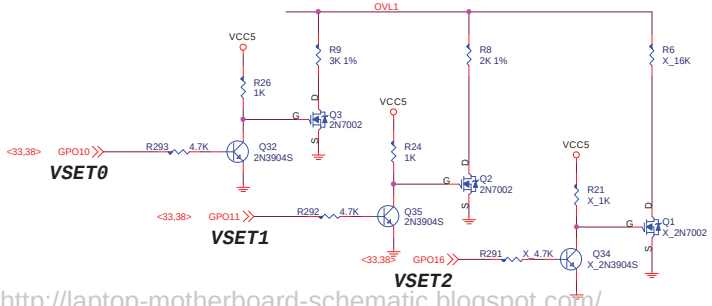
Voltage Regular Module

ATX12V Power Connector







VCORE_P0

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Title: K8 VRM ISL6559CB	Rev: 0A
Document Number: MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005
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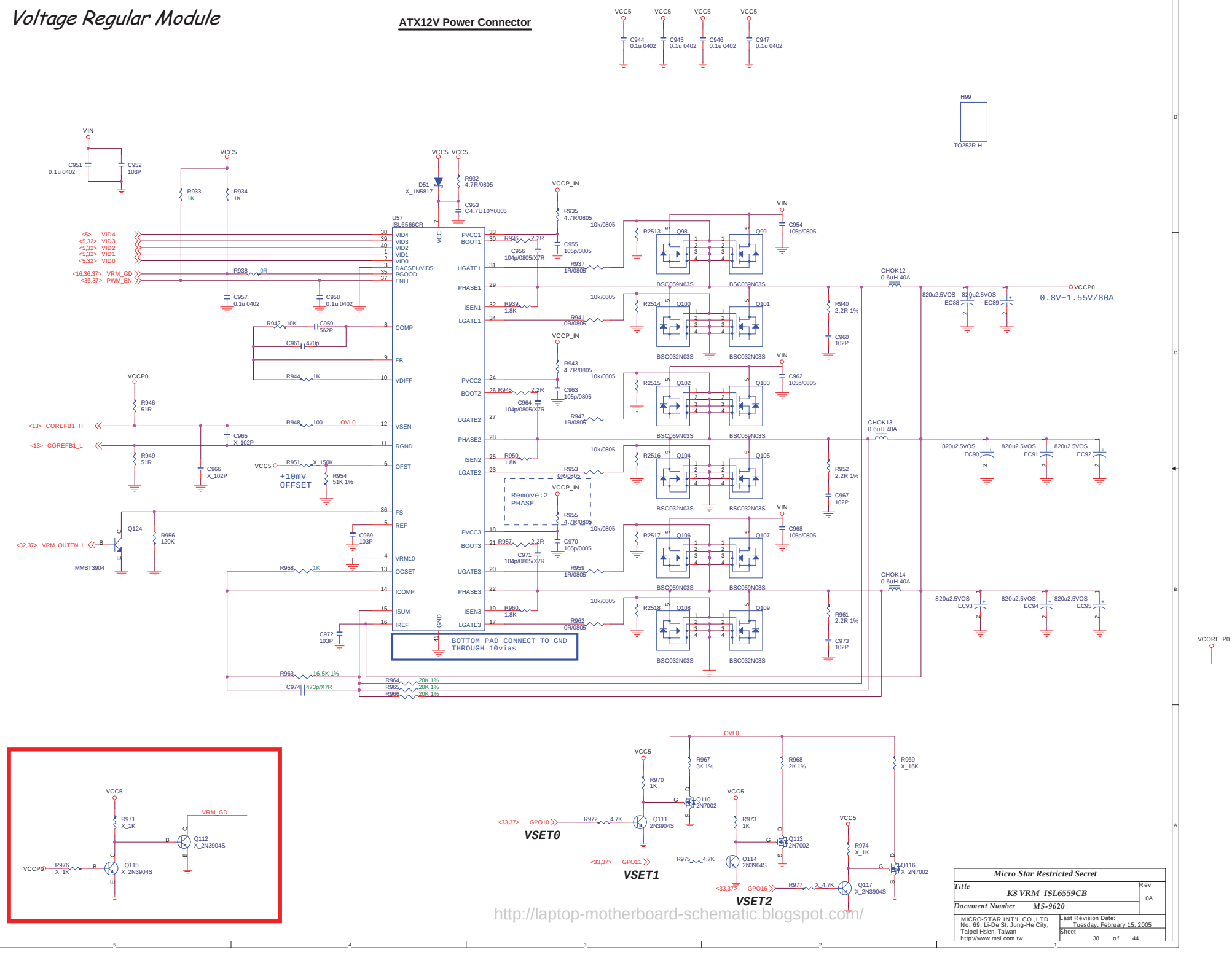
Voltage Regular Module

ATX12V Power Connector



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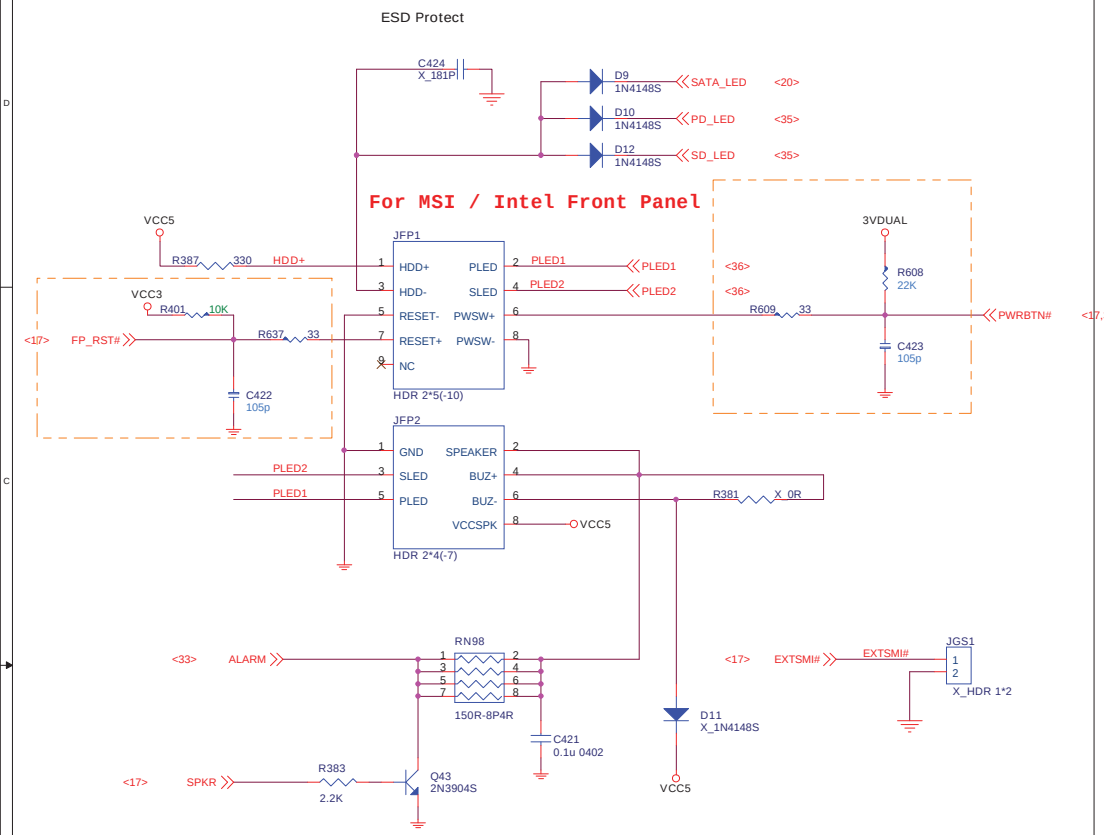
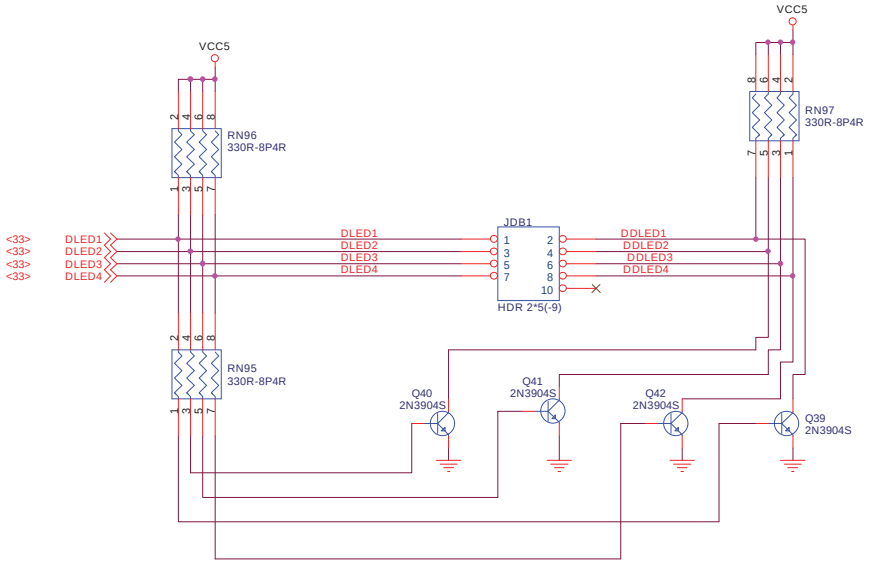
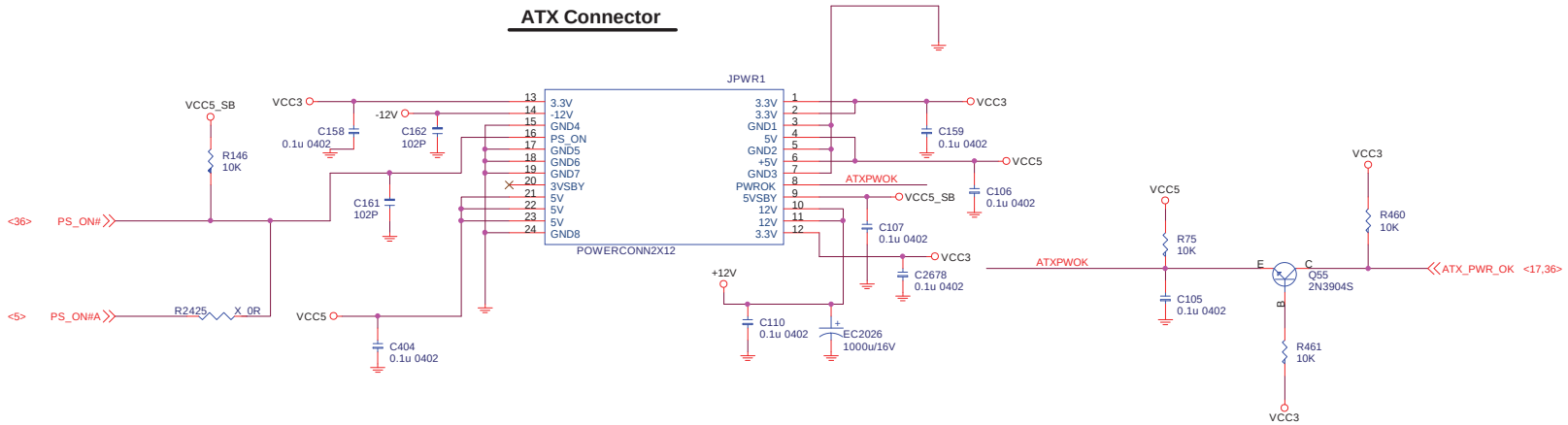
Micro Star Restricted Secret		
Title	K8 VRM ISL6559CB	Rev 0A
Document Number	MS-9620	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, February 15, 2005	Sheet 38 of 44

ATX connector / Front Panel







Micro Star Restricted Secret	
Title: ATX connector / Front Panel	Rev: 0A
Document Number: MS-9620	
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	Sheet 39 of 44

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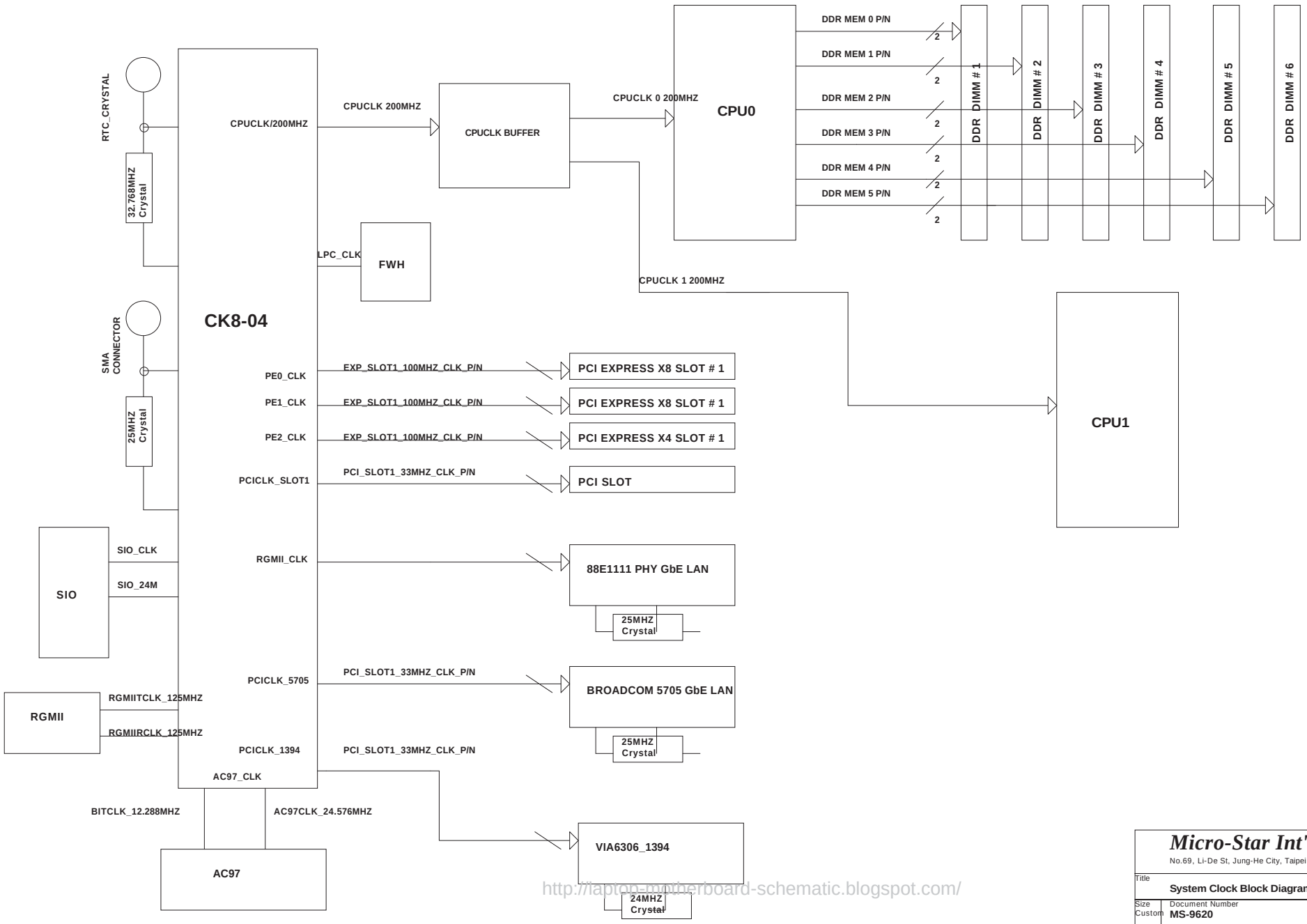
MS-9620 CLOCK BLOCK DIAGRAM



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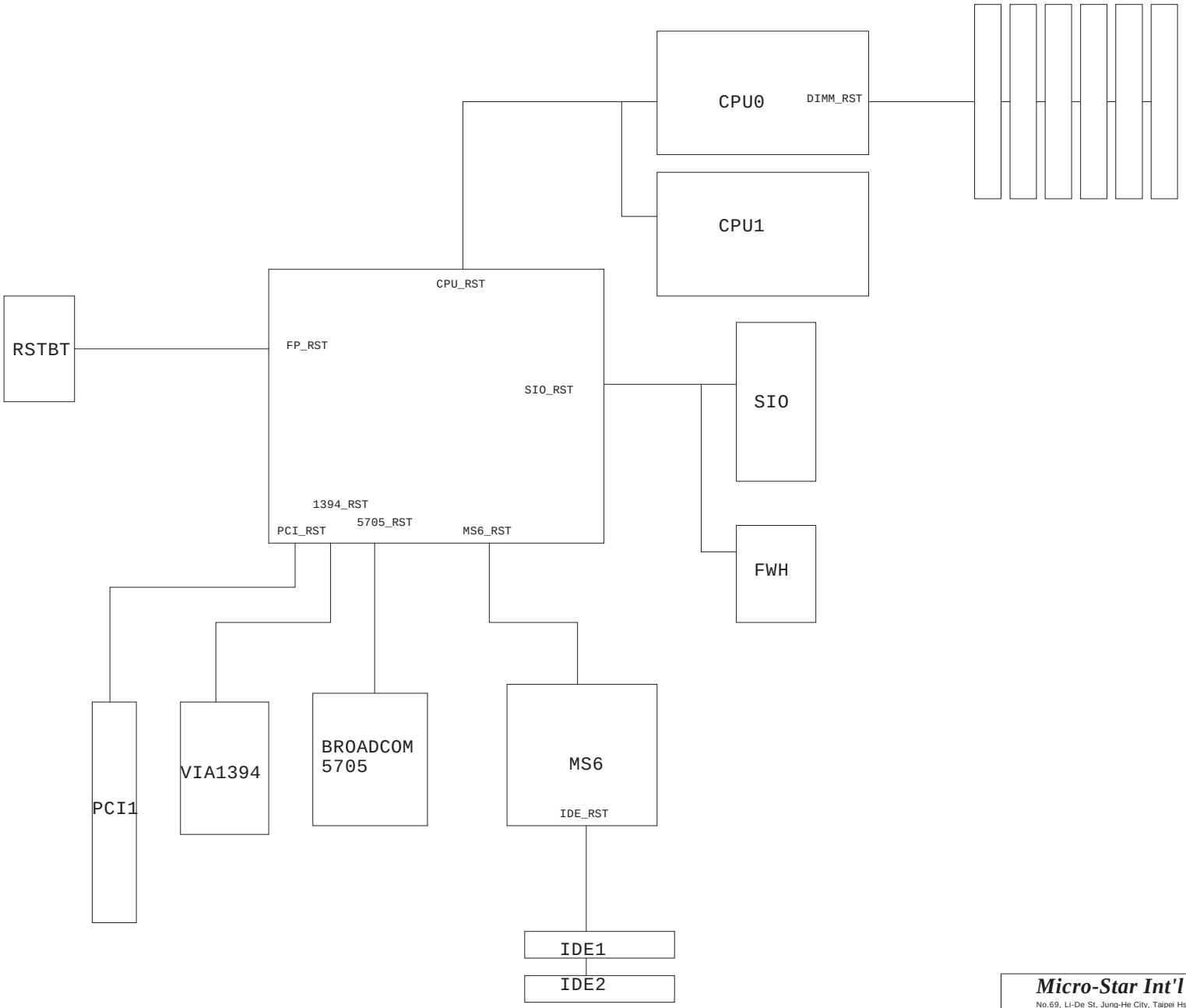
Title: System Clock Block Diagram

Size: Custom | Document Number: MS-9620 | Rev: 0A

Date: Tuesday, January 25, 2005 | Sheet 40 of 44

MS-9620 SYSTEM RESET & POWER ON SEQUENCINGBLOCK DIAGRAM



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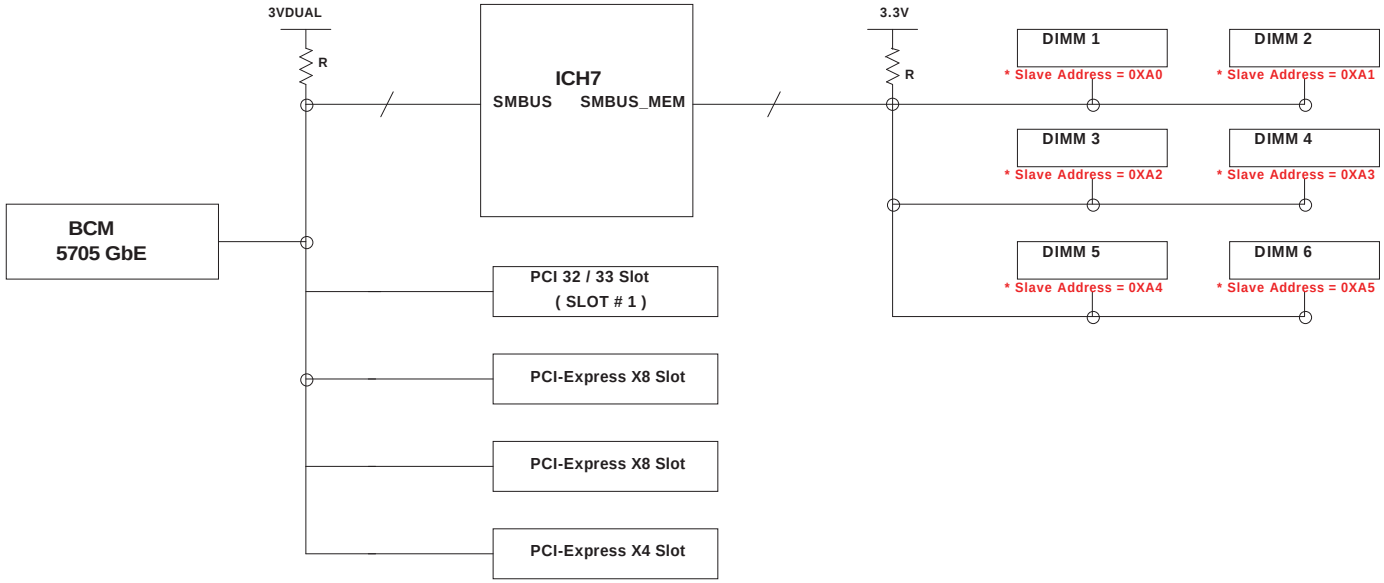
Title: **ABR Block Diagram**

Size: Custom | Document Number: **MS-9620** | Rev: 0A

Date: Tuesday, January 25, 2005 | Sheet 41 of 44

MS-9162 SMBus Block Diagram



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Title: System SMBus Block Diagram

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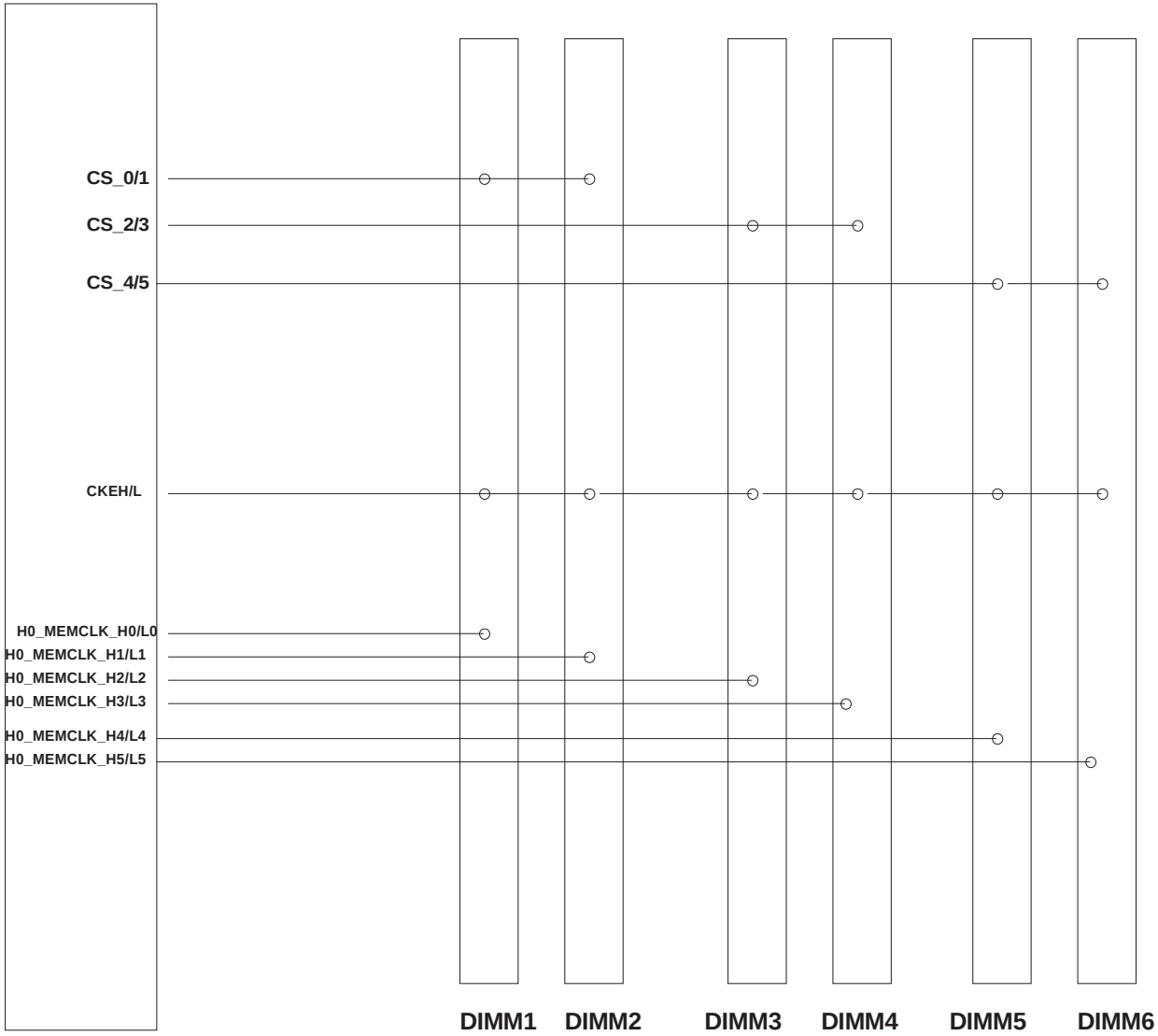
Date: Tuesday, January 25, 2005 | Sheet 42 of 44

MS-9620 DDR Routing Block Diagram



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No.69, Li-De St, Jung-He City, Taipei Hsien, Taiwan. http://www.msi.com.tw		
Title: DDRII Routing Block Diagram		
Size: Custom	Document Number: MS-9620	Rev: 0A
Date: Tuesday, January 25, 2005	Sheet 43 of 44	

General SPEC

Vcore Adjust

VSET2	VSET1	VSET0	Voltage
1	0	0	1.65V
1	0	1	1.6V
1	1	0	1.55V
1	1	1	1.5V

SIO WB 83627

GPIO Pin	Type	Function
GPO10	O	VSET0
GPO11	O	VSET1
GPO16	O	VSET1

CK_804

GPIO Pin	Type	Function
GPI 1	I	MEM_GPIO1
GPI 2	I	MEM_GPIO2
GPI 3	I	BIOS_WP#
GPI 4	I	LAN_RST#
GPI 7	I	GPO_SLI

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	REQ&GNT
5705 GIGALAN	INTC#	AD22	PCICLK1	0
VIA6306 1394	INTD#	AD23	PCICLK0	1
PCI1	INT A#B#C#D	AD24	PCICLK3	2
MSI BLUETOOTH		AD25	PCICLK2	3

** GPIO18 will toggle at 1Hz frequency.*

Title	GENERAL SPEC		
Size B	Document Number MS-9620		Rev 0A
Date: Friday, January 28, 2005		Sheet 44 of 44	

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