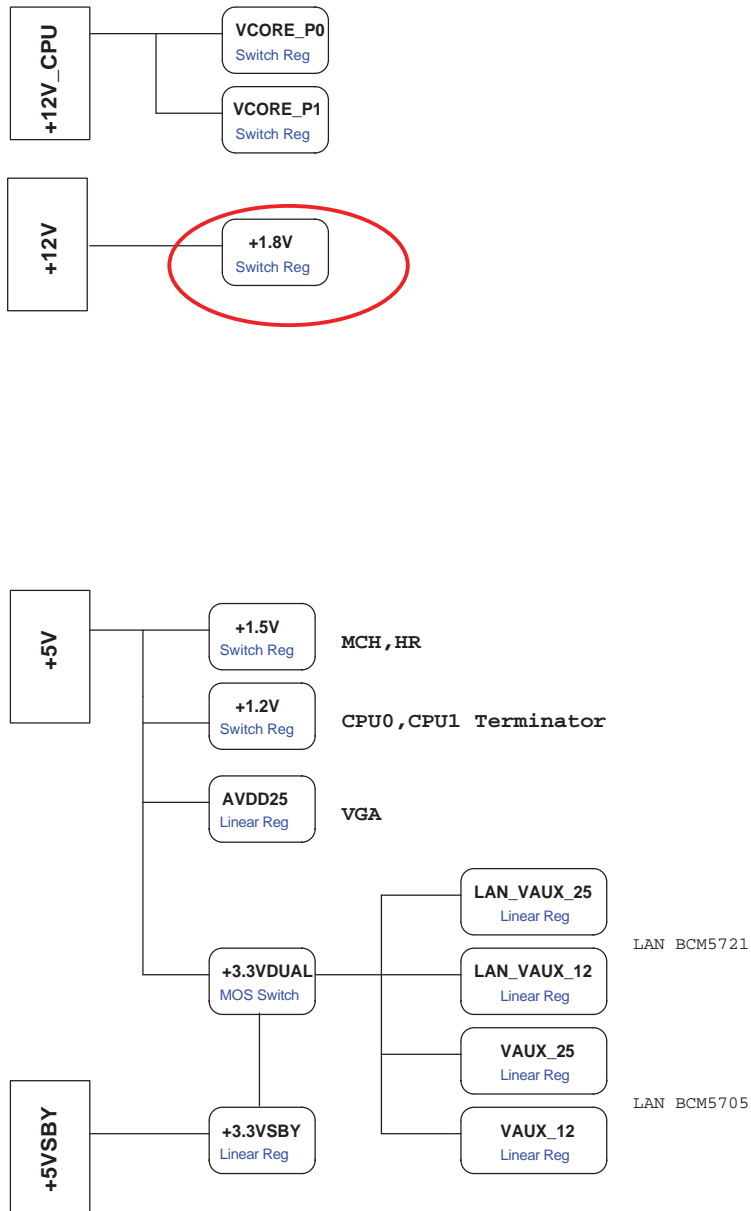
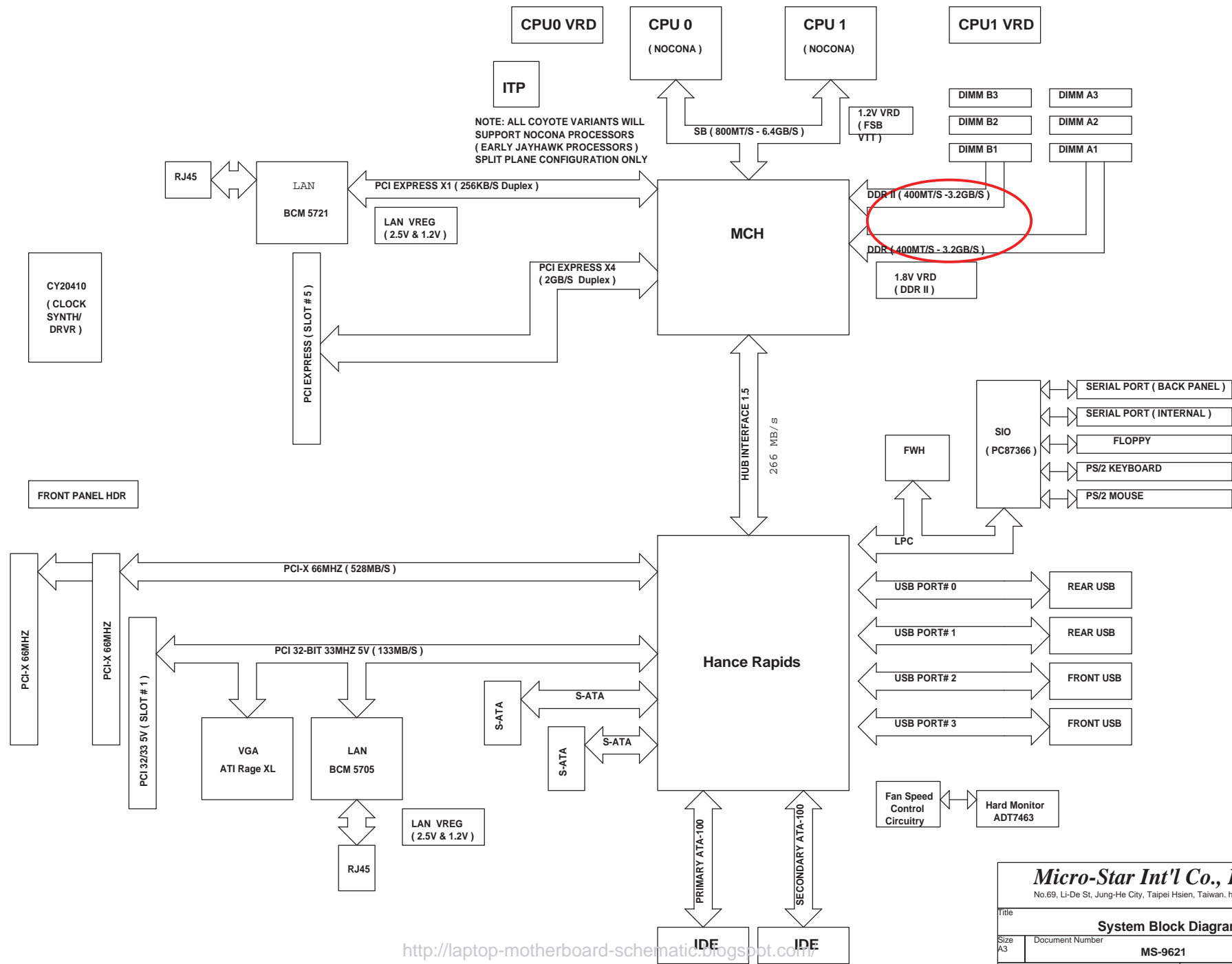


MS-9621 POWER BLOCK DIAGRAM



- * 01 Power Block Diagram
- * 02 System Block Diagram
- * 03 Clock Block Diagram
- 04 GPIO setting & SMBus address
- 05 CPU0 Power
- 06 CPU1 Power
- * 07 DDR Power 1.8V
- * 08 MP_VTT & 1.5V
- 09 System Power
- 10 Clock
- 11 CPU0 Signal
- 12 CPU0 Power and GND
- 13 CPU1 Signal
- 14 CPU1 Power and GND
- 15 ITP Port
- * 16 MCH A
- * 17 MCH B
- * 18 MCH C
- * 19 DDRII DIMM A1
- * 20 DDRII DIMM A2
- * 21 DDRII DIMM A3
- * 22 DDRII DIMM B1
- * 23 DDRII DIMM B2
- * 24 DDRII DIMM B3
- 25 PCI-E SLOT
- 26 BCM 5721
- 27 BCM 5705
- 28 HR A
- * 29 HR B
- 30 HR C
- 31 PCI-X SLOT 1,2
- 32 SCSI A
- 33 SCSI B
- 34 SCSI C
- 35 PCI32
- 36 VGA A
- 37 VGA B
- 38 IDE, SATA, FWH BIOS
- * 39 SIO
- 40 PRINTER PORT & COM & PS2
- 41 HM
- 42 FAN Connector
- 43 System logic
- * 44 Layout Component

MS-9621 SYSTEM BLOCK DIAGRAM

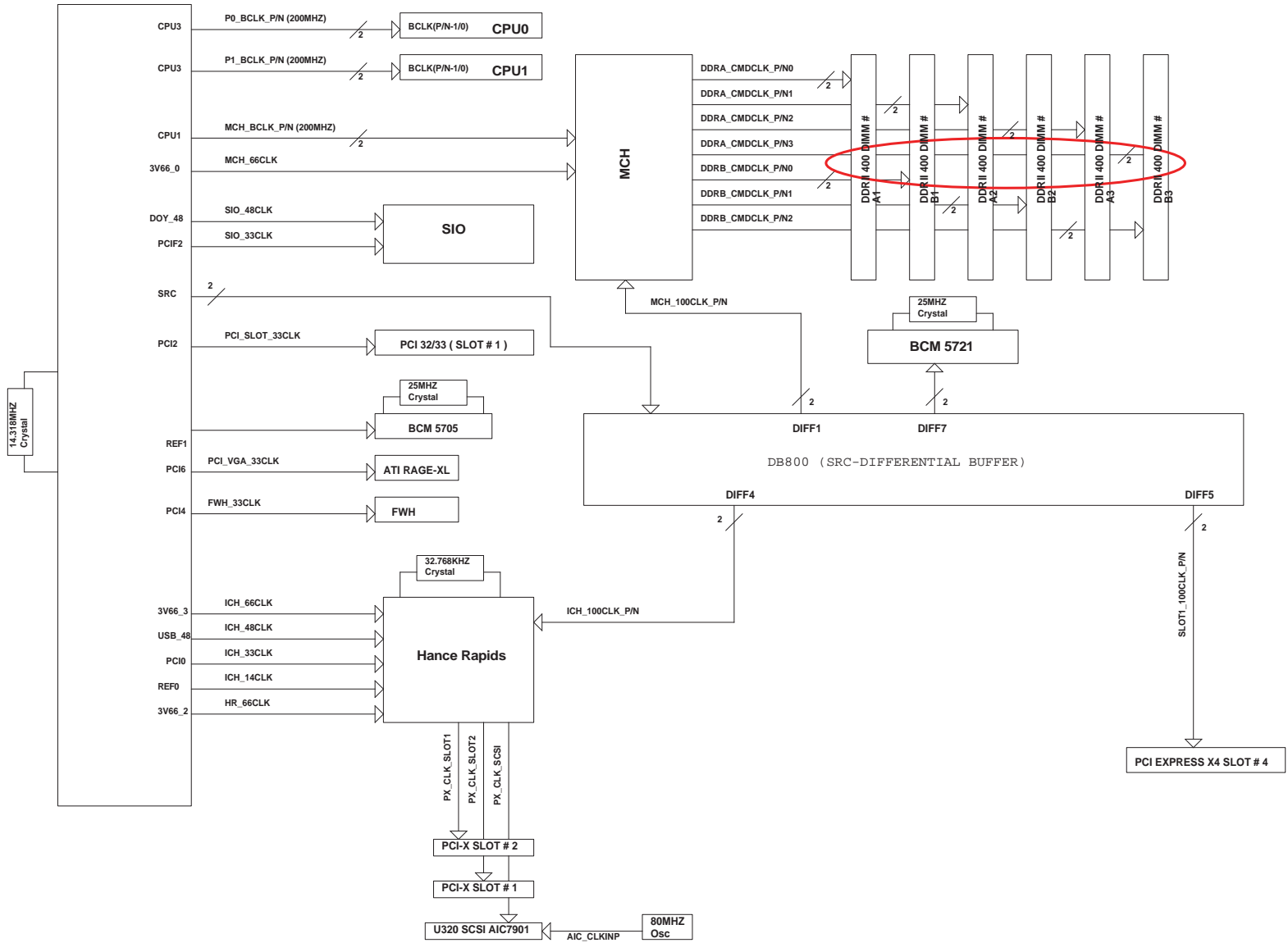


<http://laptop-motherboard-schematic.blogspot.com/>

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Title		
System Block Diagram		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 2 of 44

MS-9621 CLOCK BLOCK DIAGRAM

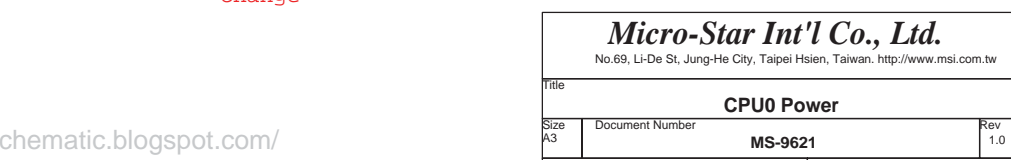
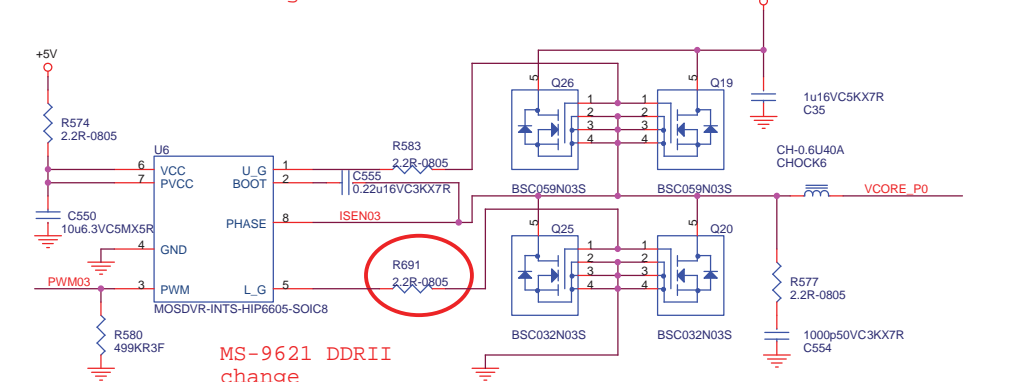
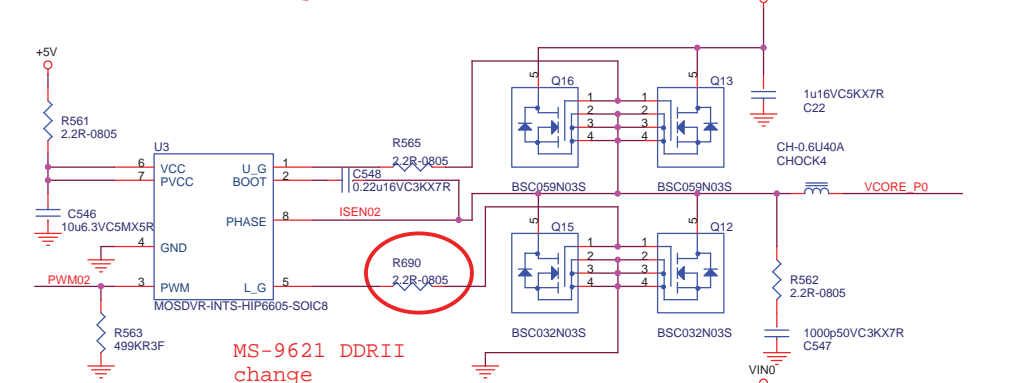
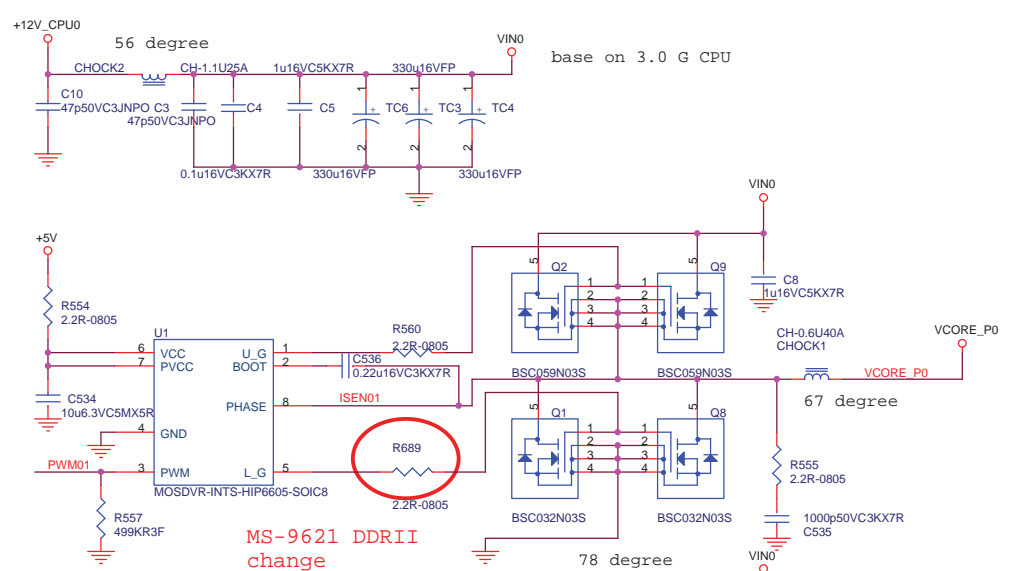
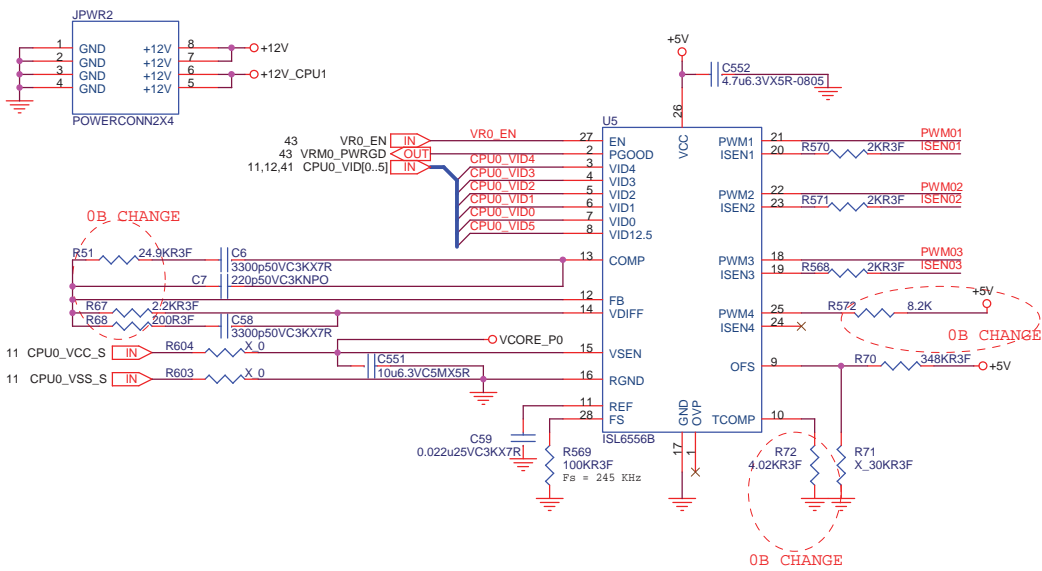


GPIO Pin	Type	Function	Power well
GPIO0	I	PX_REQJ2	Main
GPIO1	I	NC	Main
GPIO2	I	SIO_SMI_N	Main
GPIO3	I	MCH_GPEJ	Main
GPIO4	I	MCH_PMEJ	Main
GPIO5	I	DUMP_SW	Main
GPIO6	I	HMI_ALERTJ	Main
GPIO7	I	HMO_ALERTJ	Main
GPIO8	I	PX_PMEJ	Resume
GPIO11	I	SMBALERT_N	Resume
GPIO12	I	WAKE_N	Resume
GPIO13	I	PCIE_SIO_WAKEJ	Resume
GPIO16	O	PX_GNTJ2	Main
GPIO17	O	NC	Main
GPIO18	O	NC	Main
GPIO19	O	NC	Main
GPIO20	O	SCSI_ENABLE	Main
GPIO21	O	NC	Main
GPIO22	O	SATALED	Main
GPIO23	O	NC	Main
GPIO24	I/O	SYS_LED	Resume
GPIO25	I/O	PLLSEL0	Resume
GPIO27	I/O	PLLSEL1	Resume
GPIO28	I/O	LAN_ENABLE	Resume
GPIO32	I/O	NC	Main
GPIO33	I/O	PX_IRQJ0	Main
GPIO34	I/O	PX_IRQJ1	Main
GPIO35	I/O	PX_IRQJ2	Main
GPIO36	I/O	PX_IRQJ3	Main
GPIO37	I/O	NC	Main
GPIO38	I/O	NC	Main
GPIO39	I/O	BIOS_WPJ	Main
GPIO40	I/O	CONFIG1	Main
GPIO41	I/O	CONFIG0	Main
GPIO42	I/O	CPU1_IERR	Main
GPIO43	I/O	CPU0_IERR	Main
GPIO56	O	NC	Resume
GPIO57	O	NC	Resume

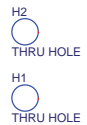
GPIO Pin	Type	Function	Power Well
GPIO00	I/O	NC	Main
GPIO01	I/O	NC	Main
GPIO02	I/O	NC	Main
GPIO03	I/O	NC	Main
GPIO04	I/O	NC	Main
GPIO05	I/O	NC	Main
GPIO06	I/O	KRRSTJ	Main
GPIO07	I/O	CPU_A20GATE	Main
GPIO10	I/O	SIO_SMI_N	Main
GPIO11	I/O	NC	Main
GPIO12	I/O	NC	Main
GPIO13	I/O	NC	Main
GPIO15	I/O	NC	Main
GPIO16	I/O	MTR1J	Main
GPIO17	I/O	DR1J	Main
GPIO20	I/O	NC	Main
GPIO21	I/O	NC	Main
GPIO22	I/O	NC	Main
GPIO23	I/O	NC	Main
GPIO24	I/O	CPU0_FORCEPRJ	Main
GPIO25	I/O	CPU1_FORCEPRJ	Main
GPIO26	I/O	NC	Main
GPIO27	I/O	NC	Main
GPIO30	I/O	NC	Main
GPIO31	I/O	NC	Main
GPIO32	I/O	NC	Main
GPIO33	I/O	NC	Main
GPIO34	I/O	NC	Main
GPIOE0	I/O	COLD_WOL_EN	Standby
GPIOE1	I/O	NC	Standby
GPIOE2	I/O	PLED	Standby
GPIOE3	I/O	IPMB_ALT2	Standby
GPIOE4	I/O	IPMB_ALT1	Standby
GPIOE5	I/O	NC	Standby
GPIE6	I	NC	Standby
GPIE7	I	NC	Standby
GPOS0	O	PWBTOUTJ	Standby
GPOS1	O	PSONJ	Standby
GPIS2	I	PWBTIN	Standby
GPIS3	I	SLPS3J	Standby

Device	Address	CLOCK
DIMM1	0xA0	DDR_A_CMDCLK_P0/N0
DIMM2	0xA8	DDR_B_CMDCLK_P0/N0
DIMM3	0xA2	DDR_A_CMDCLK_P1/N1
DIMM4	0xAA	DDR_B_CMDCLK_P1/N1
DIMM5	0xA4	DDR_A_CMDCLK_P2/N2
DIMM6	0xAC	DDR_B_CMDCLK_P2/N2

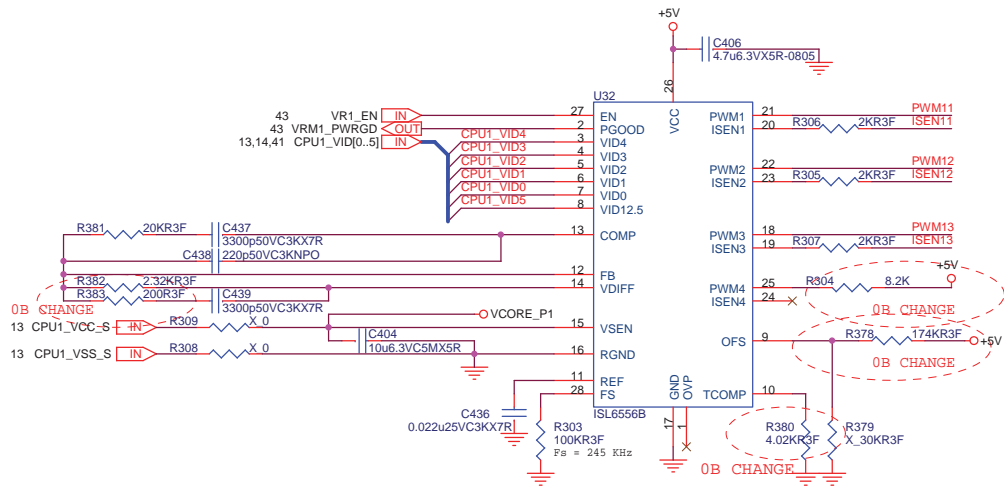
DEVICE	INT	REQ#/GNT#	IDSEL	CLOCK
PCI 1	PIRQ#A	REQ#0/GNT#0	AD20	PCI0
	PIRQ#B			
	PIRQ#C			
	PIRQ#D			
VGA	PIRQ#C	REQ#1/GNT#1	AD21	PCI6
	LAN	REQ#2/GNT#2	AD22	PCIF2
PCIX1	PXIRQ#0	PXREQ#0/PXGNT#0	PXAD17	FXPCLK00
	PXIRQ#1			
	PXIRQ#2			
	PXIRQ#3			
PCIX2	PXIRQ#1	PXREQ#1/PXGNT#1	PXAD18	FXPCLK01
	PXIRQ#2			
	PXIRQ#3			
	PXIRQ#0			
SCSI	PXIRQ#2	PXREQ#2/PXGNT#2	PXAD19	FXPCLK02



VID=1.35V
 I_{max}=92 A
 I_{ripple current} = 92*0.17=15.64 A

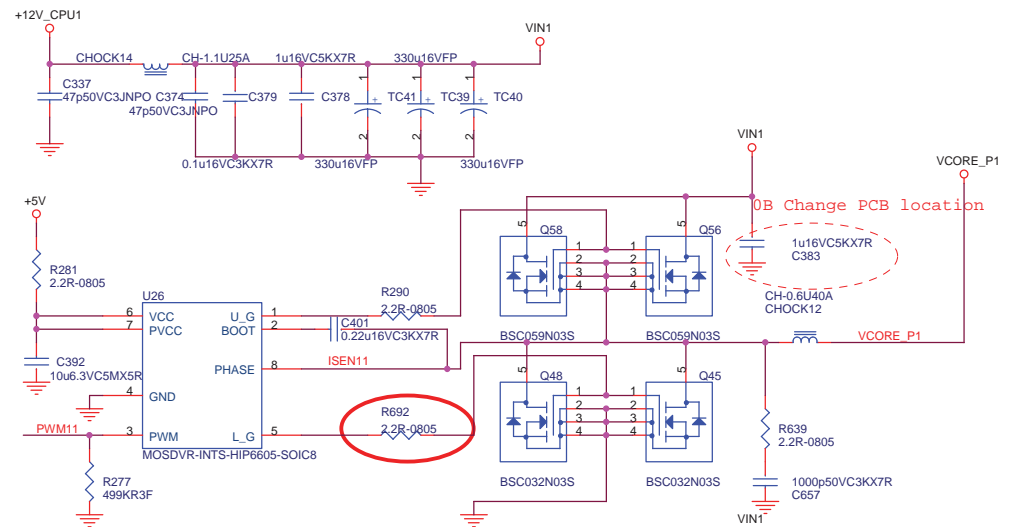


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Title CPU0 Power		
Size A3	Document Number MS-9621	Rev 1.0
Date: Friday, March 25, 2005	Sheet 5	of 44

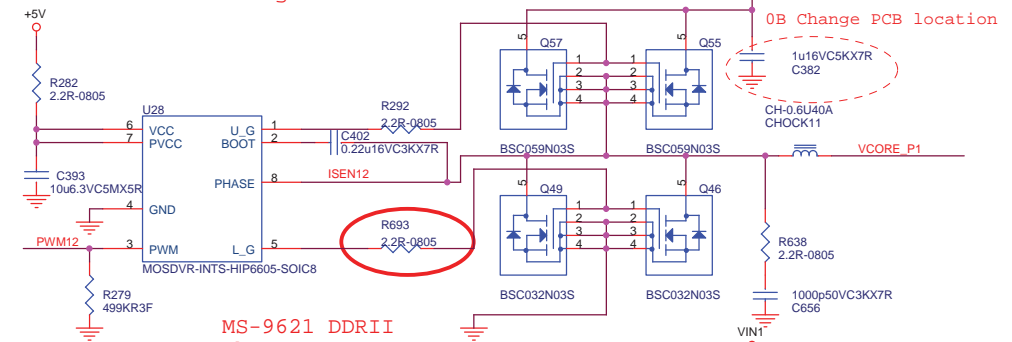


H4
THRU HOLE

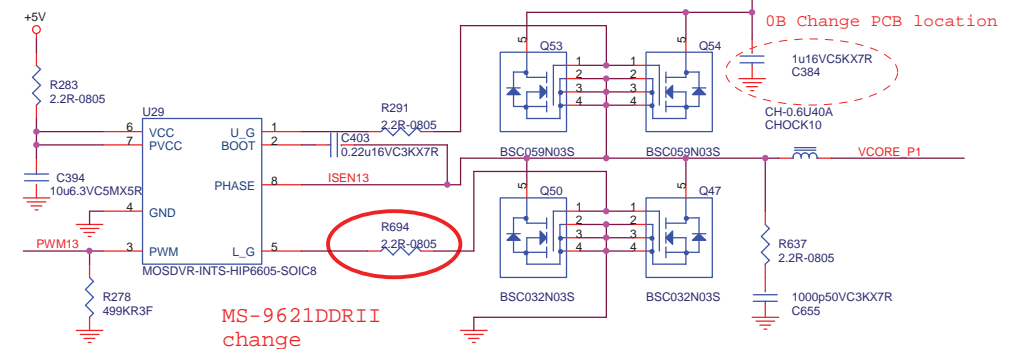
H3
THRU HOLE



MS-9621 DDRII
change

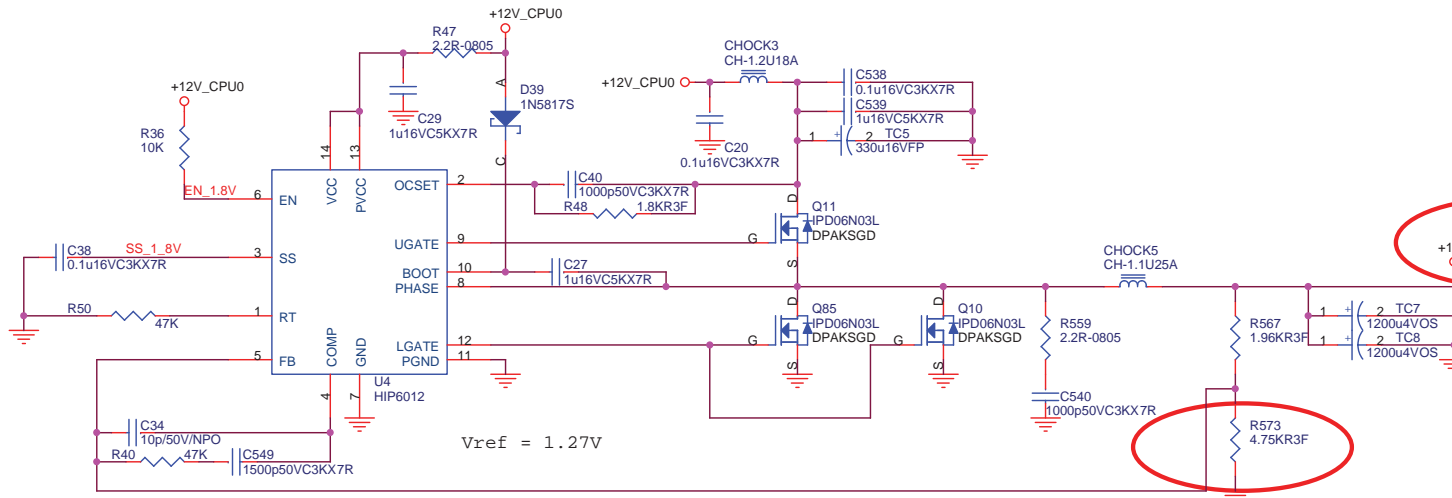


MS-9621 DDRII
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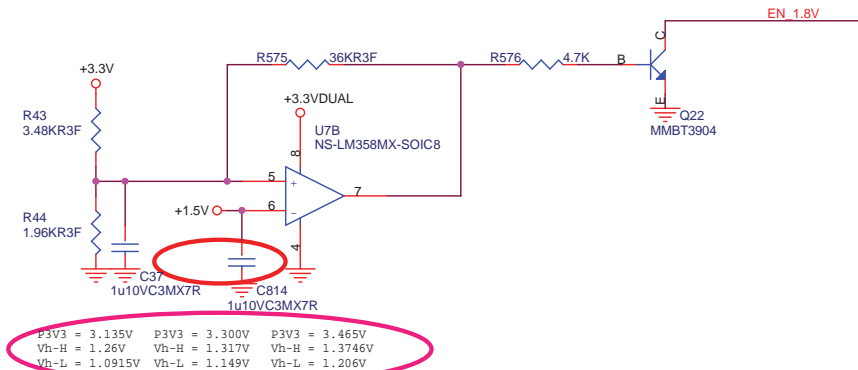
MS-9621 DDRII
change

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Title		
CPU1 Power		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 6 of 44



MCH 8.8 A
 1Gb 9 device 0.495 A/device
 ACTIVE 22.2 Watt/DIMM
 STANDBY 5.1 Watt/DIMM
 Total Power
 =22.2+22.2+5.1*4
 =64.4 Watt
 Current=27.96 A
 Aripple=25*0.5=12.5A

MS-9621 change R573 from 2K to 4.75K ohm



COST:3.7068

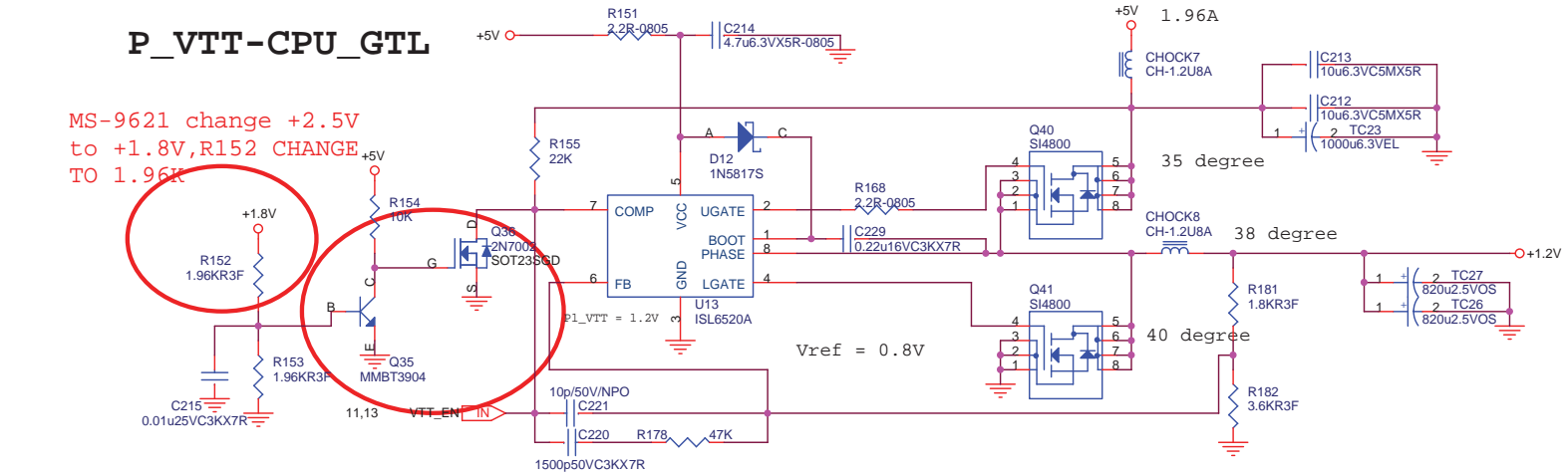
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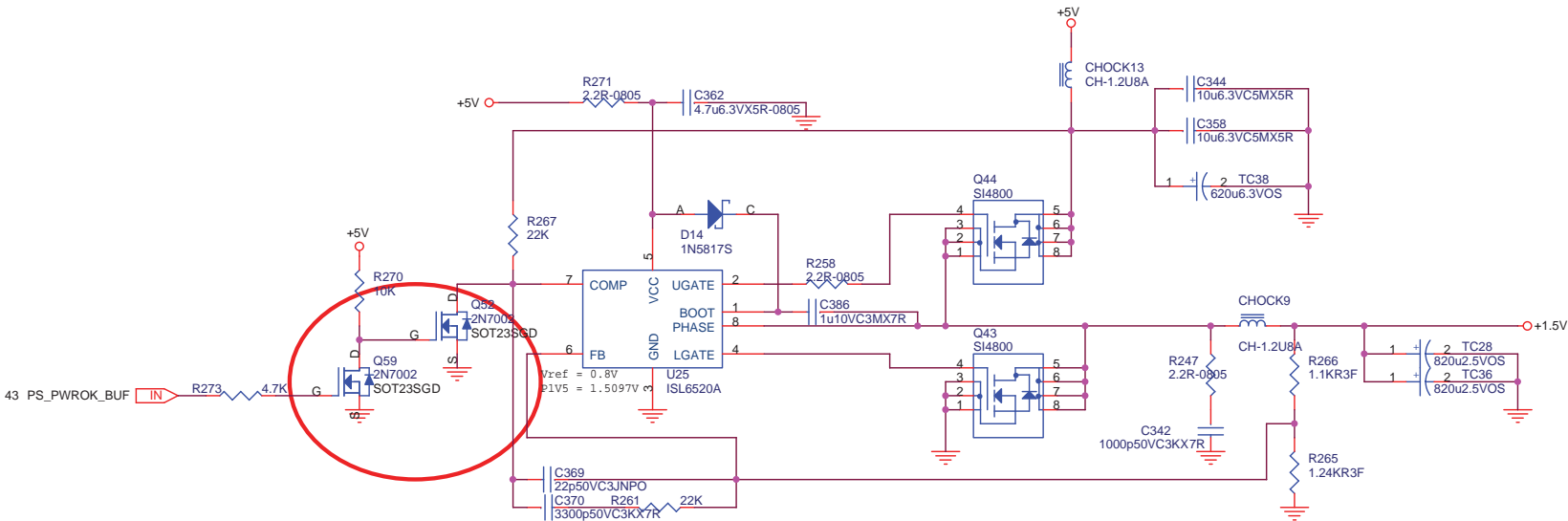
Title		
DDR Power 1.8V		
Size B	Document Number	Rev 1.0
MS-9621		
Date:	Friday, March 25, 2005	Sheet 7 of 44

P_VTT-CPU_GTL

MS-9621 change +2.5V
to +1.8V, R152 CHANGE
TO 1.96K



+1.2V MAX 6A
+1.2V TYPE 3.5A
Static Voltage 1.2 V+/-2%
Transient Voltage 1.2 V+/-5%

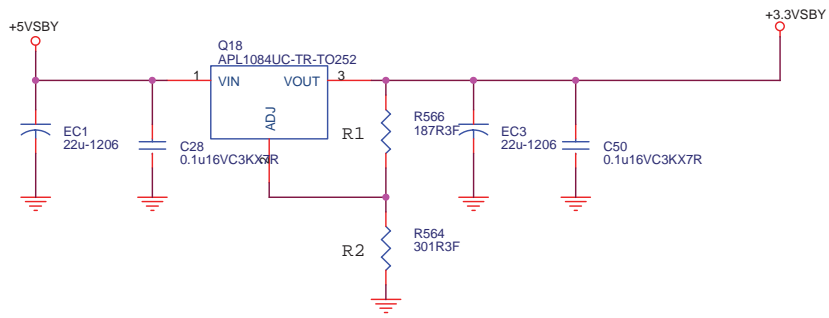


1.5V 6.1 A
Transient Voltage 1.5 V+/-5%

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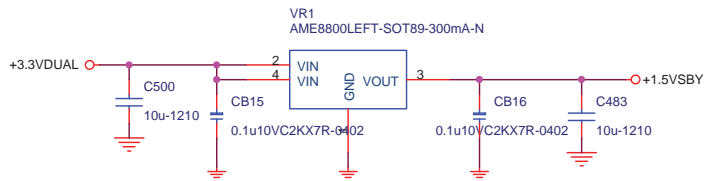
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MP_VTT & 1.5V		
Size B	Document Number	Rev 1.0
MS-9621		
Date:	Friday, March 25, 2005	Sheet 8 of 44

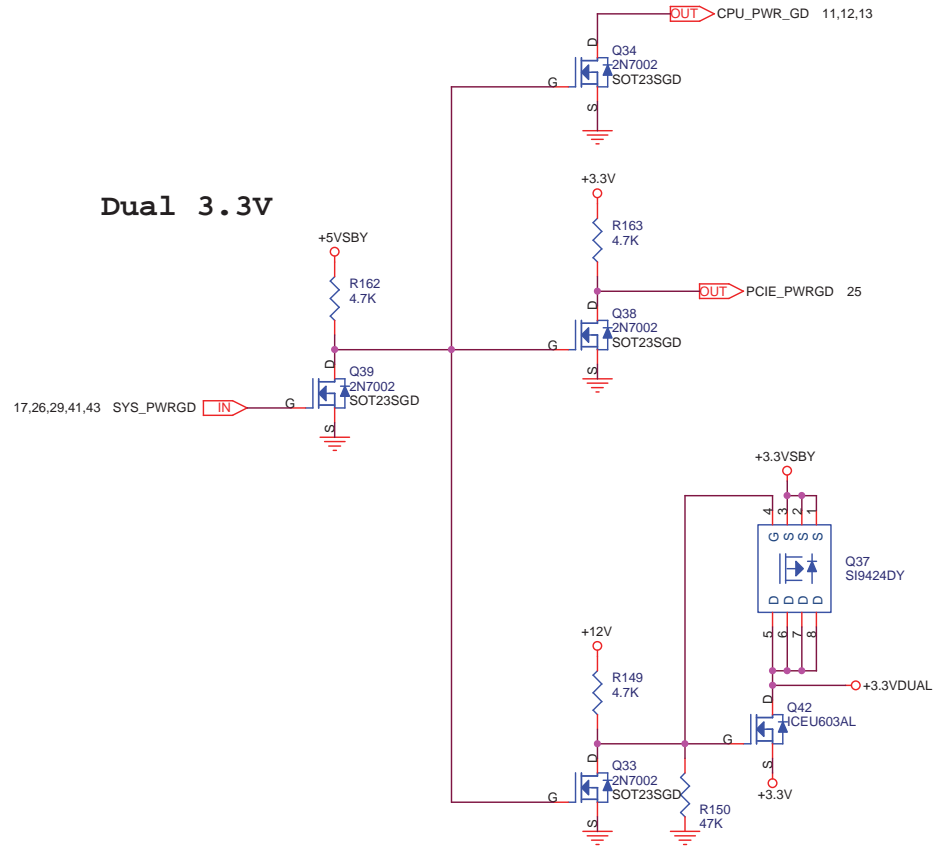


$$V_{out} = 1.25 * (1 + R2 / R1)$$

+1.5V SBY 75mA



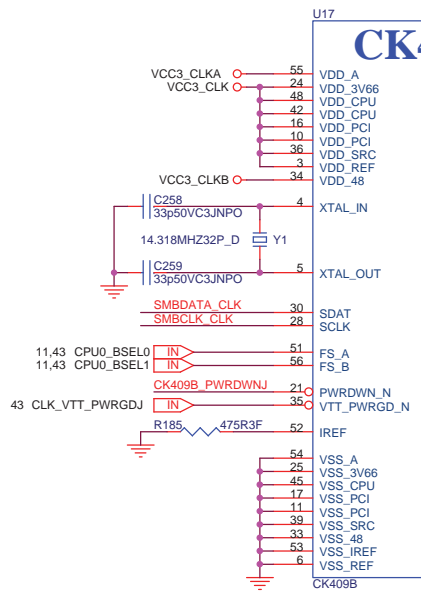
Dual 3.3V



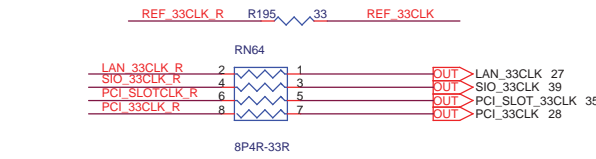
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Title		
System Power		
Size	Document Number	Rev
B	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 9 of 44

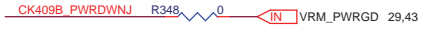
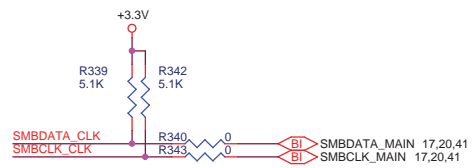
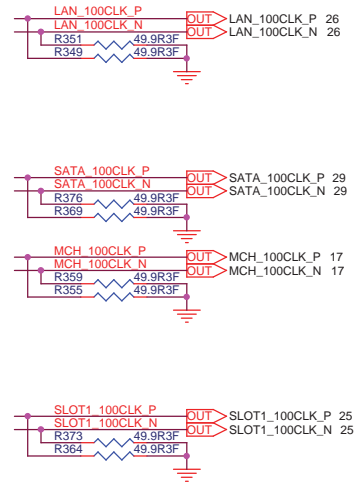
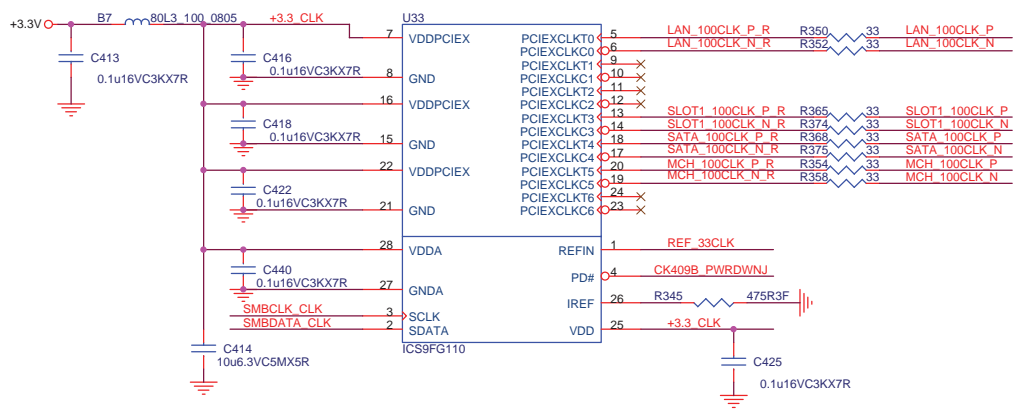
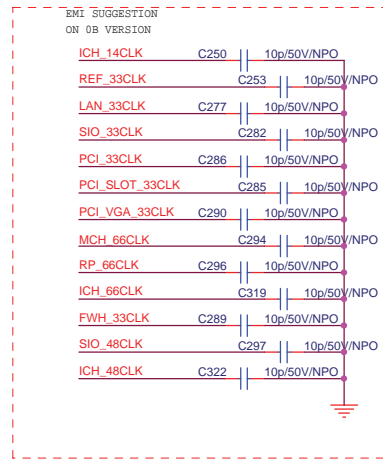
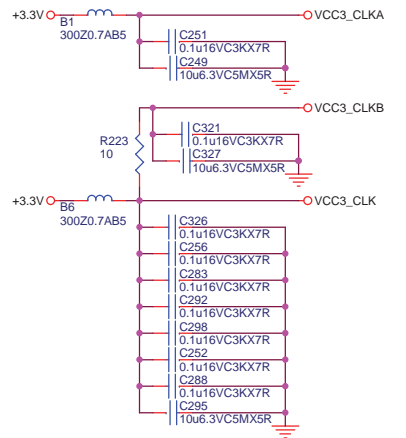


ICS 932S208



Power => CK409B

F_SEL1	F_SEL0	FREQ.
0	0	100 Mhz
0	1	133 Mhz
1	0	200 Mhz
1	1	166 Mhz

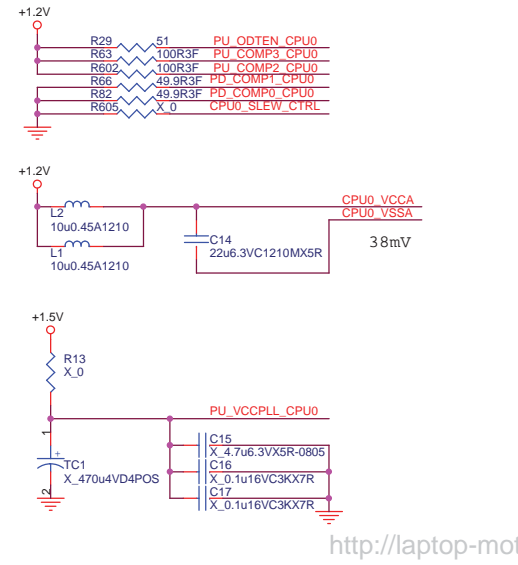
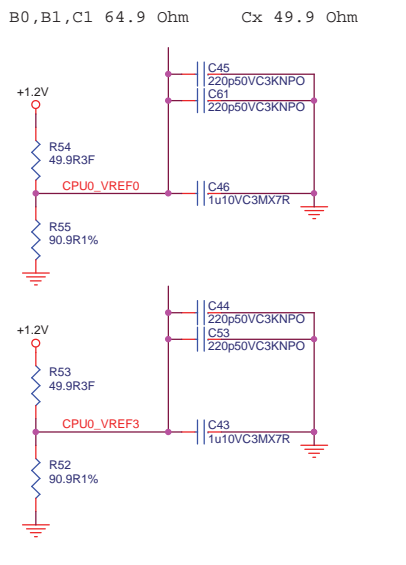
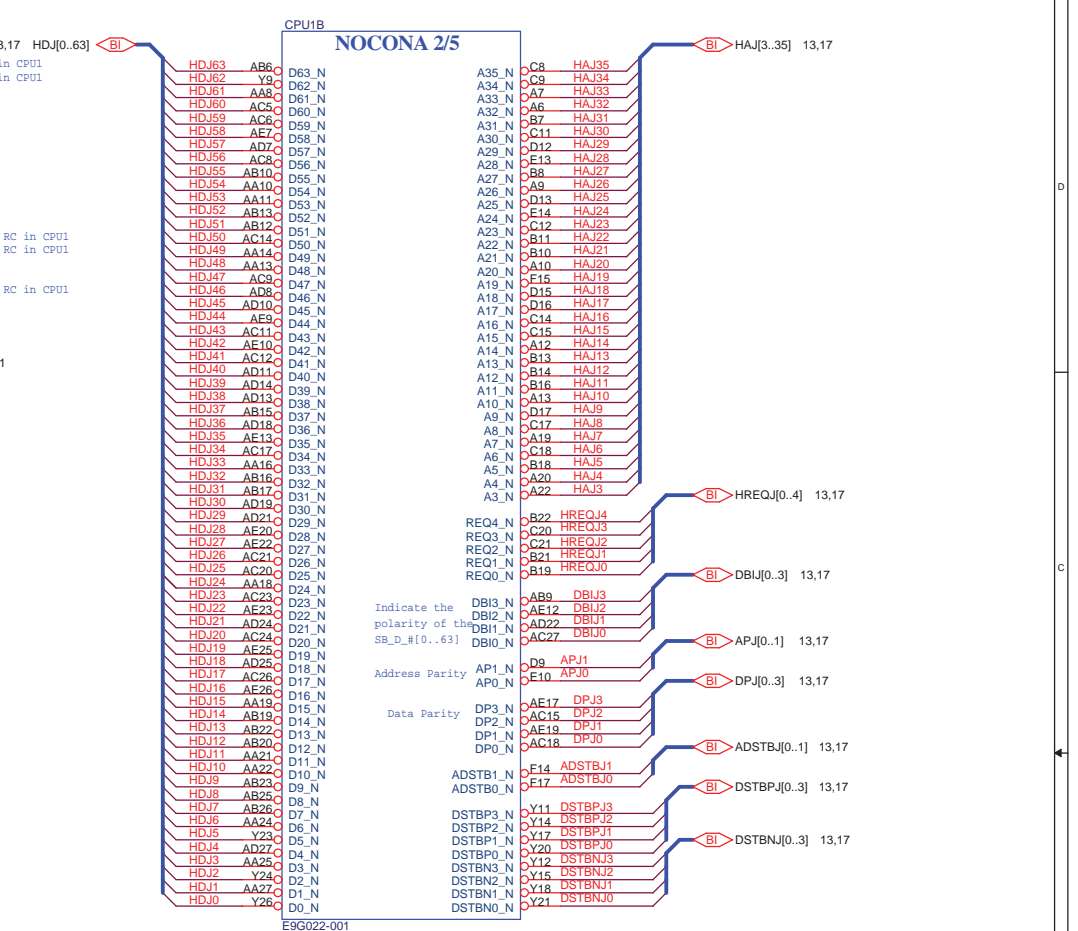
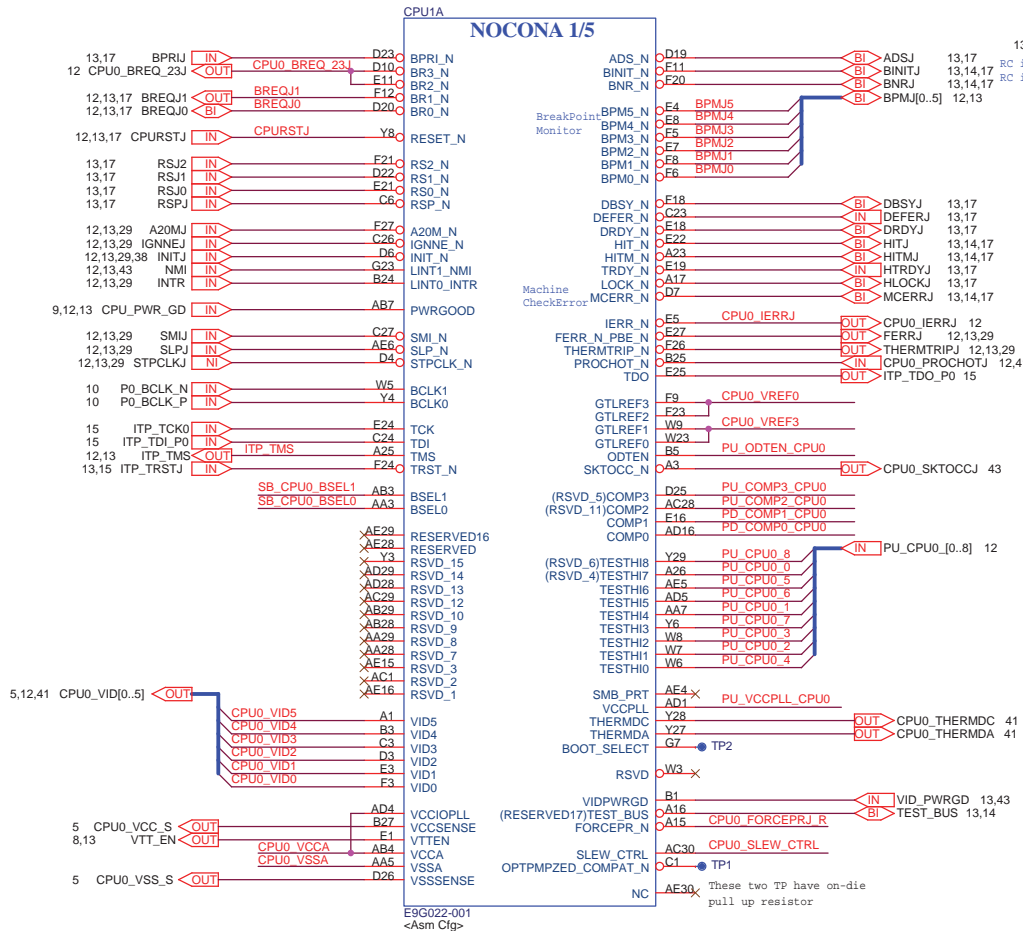


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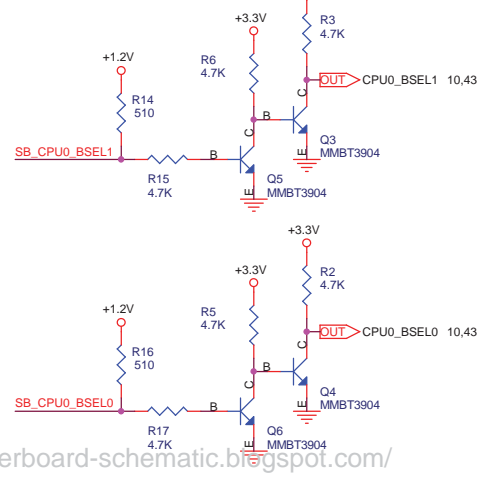
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Size A3	Document Number MS-9621	Rev 1.0
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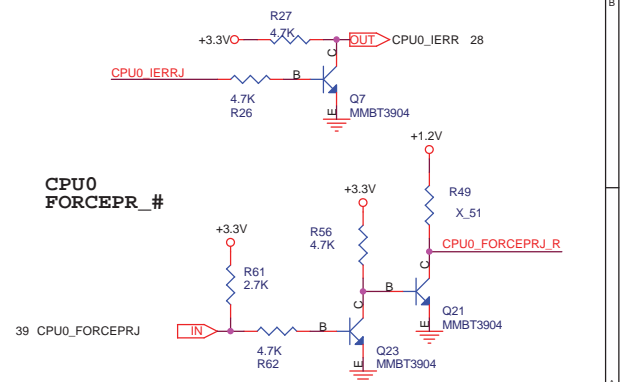
Date: Friday, March 25, 2005 Sheet 10 of 44



Frequency Select



CPU0_FORCEPRJ_#

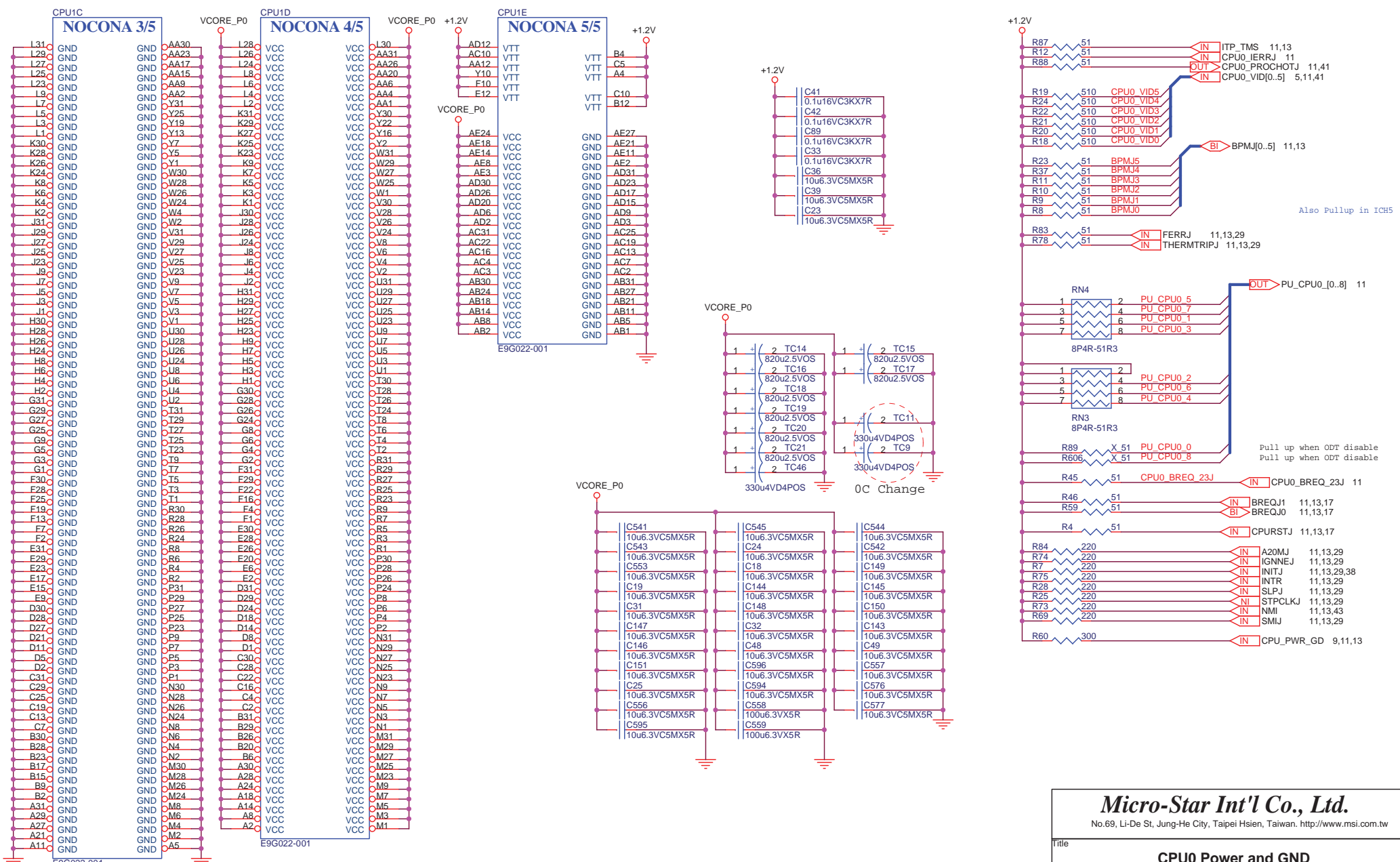


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Title: **CPU0 Signal**

Size A3 Document Number **MS-9621** Rev 1.0

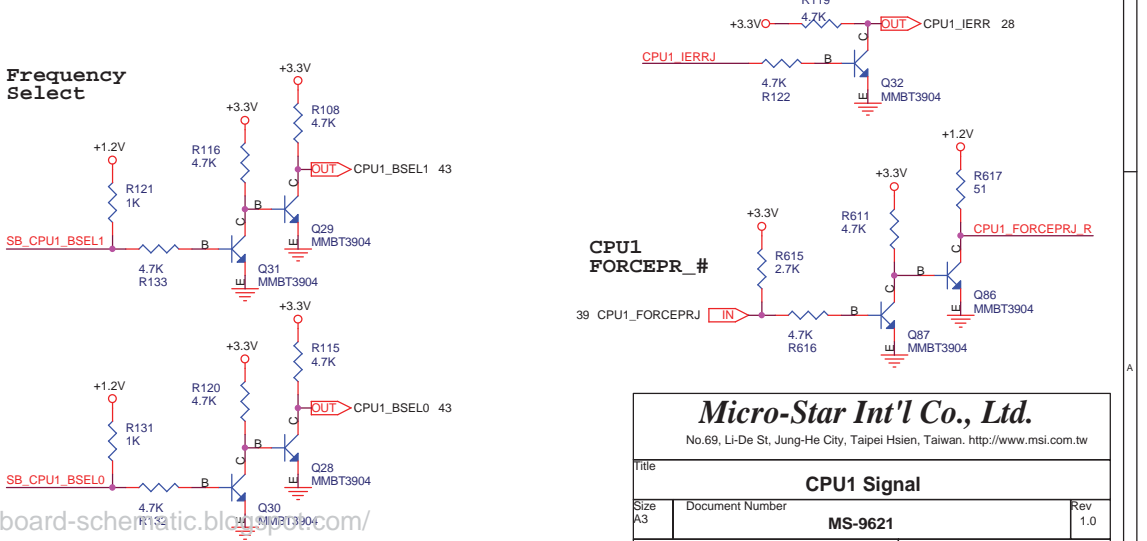
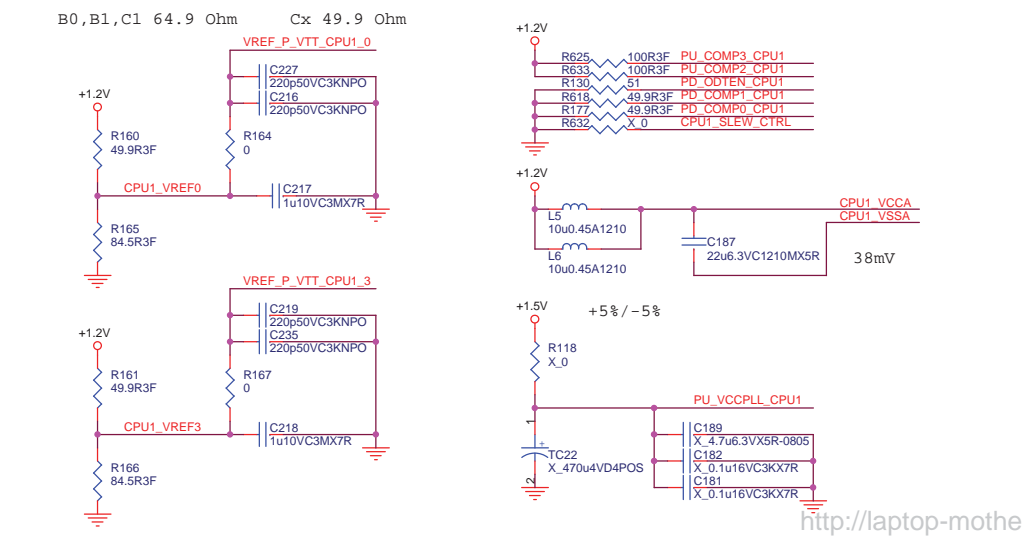
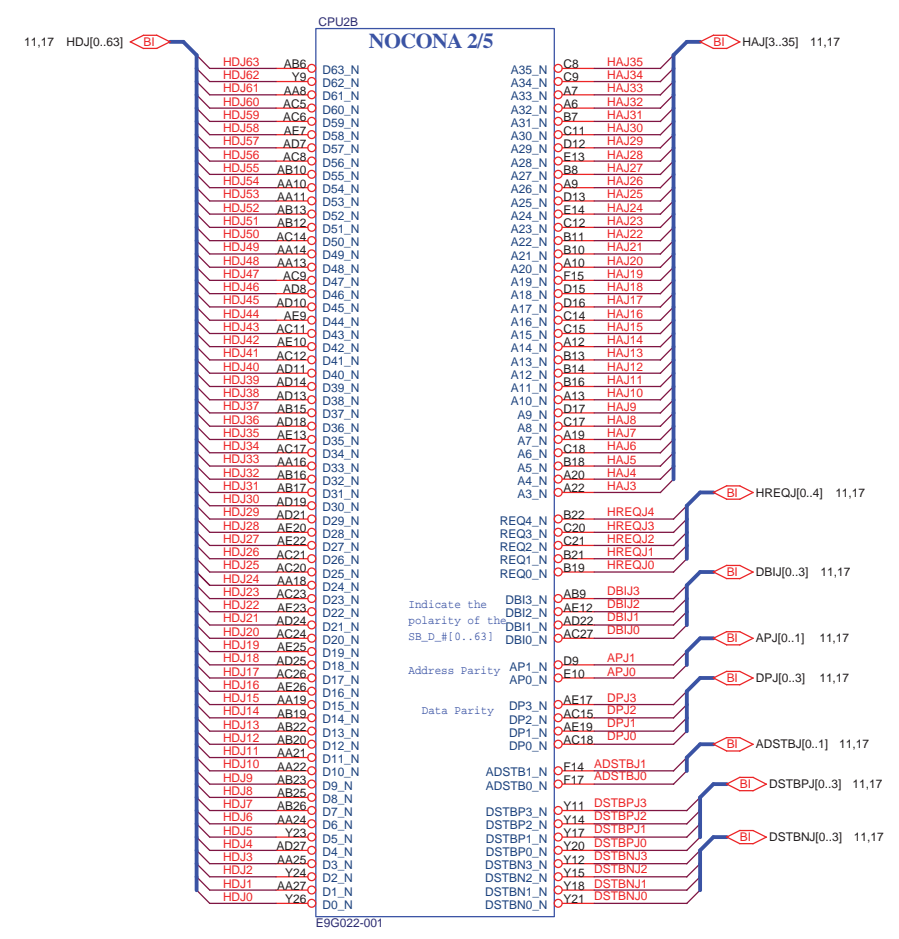
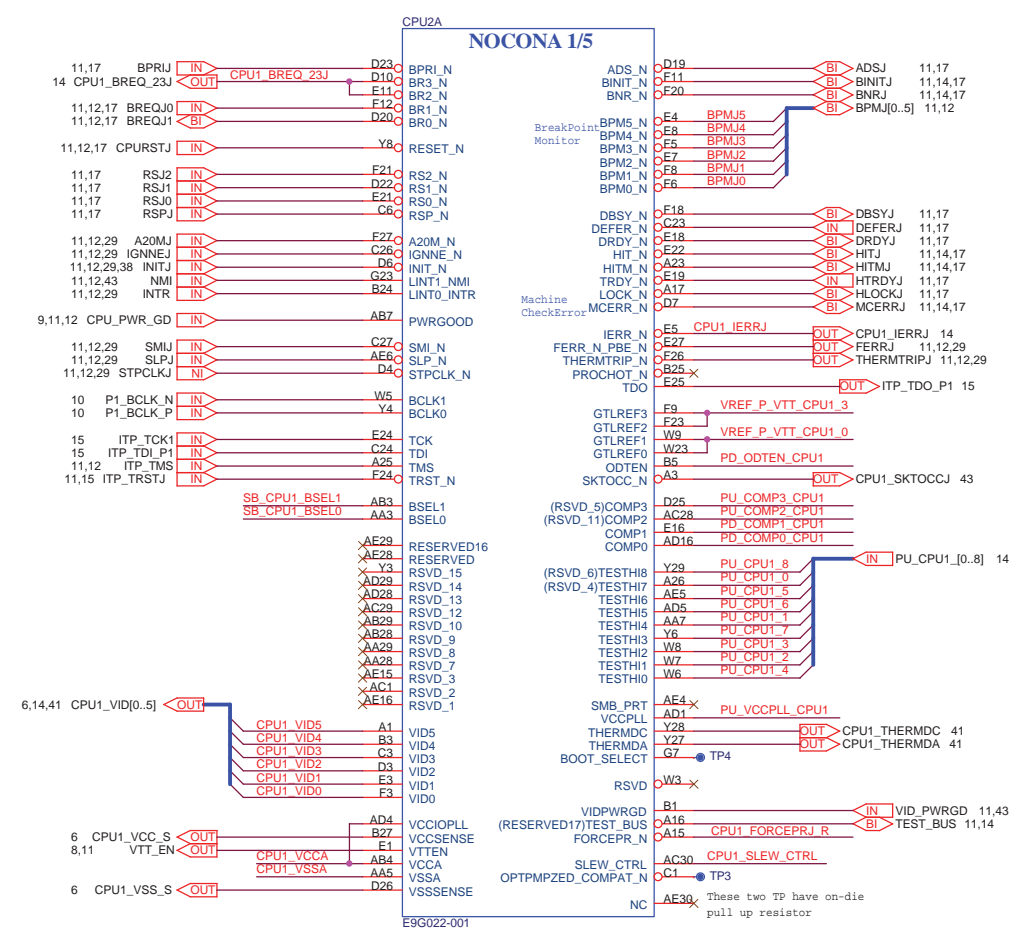
Date: Friday, March 25, 2005 Sheet 11 of 44



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Title: **CPU0 Power and GND**

Size B	Document Number MS-9621	Rev 1.0
Date: Friday, March 25, 2005	Sheet 12 of 44	

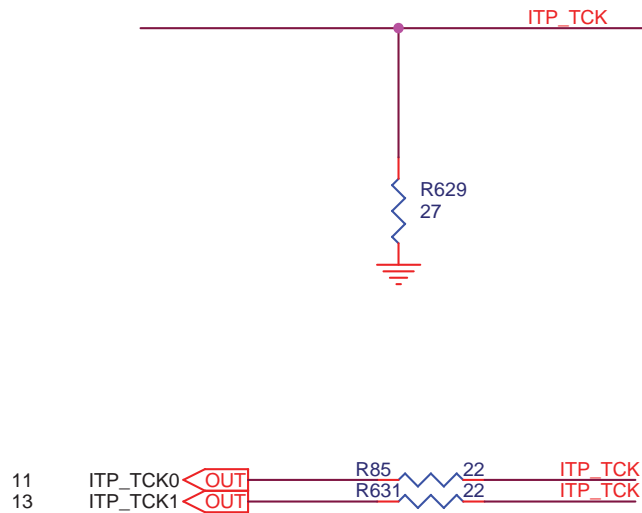
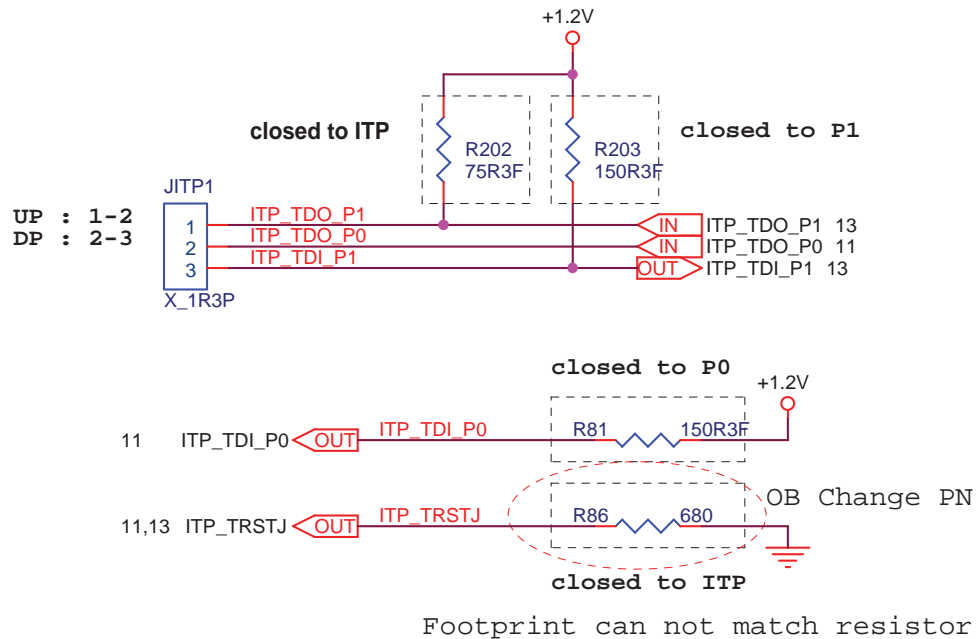


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Title		
CPU1 Signal		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 13 of 44

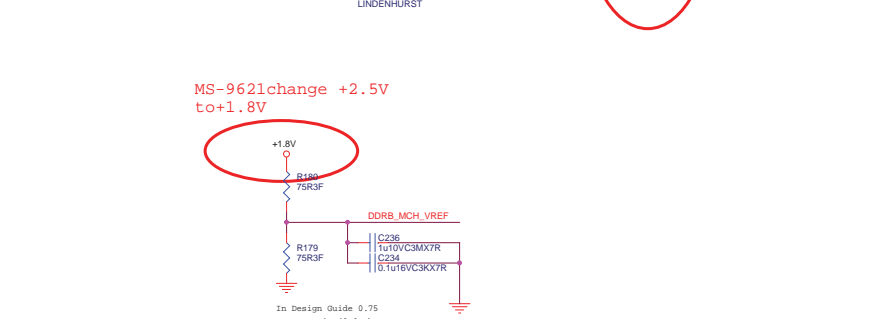
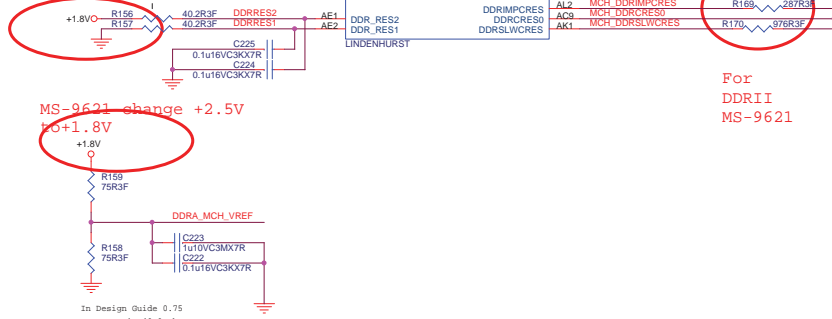
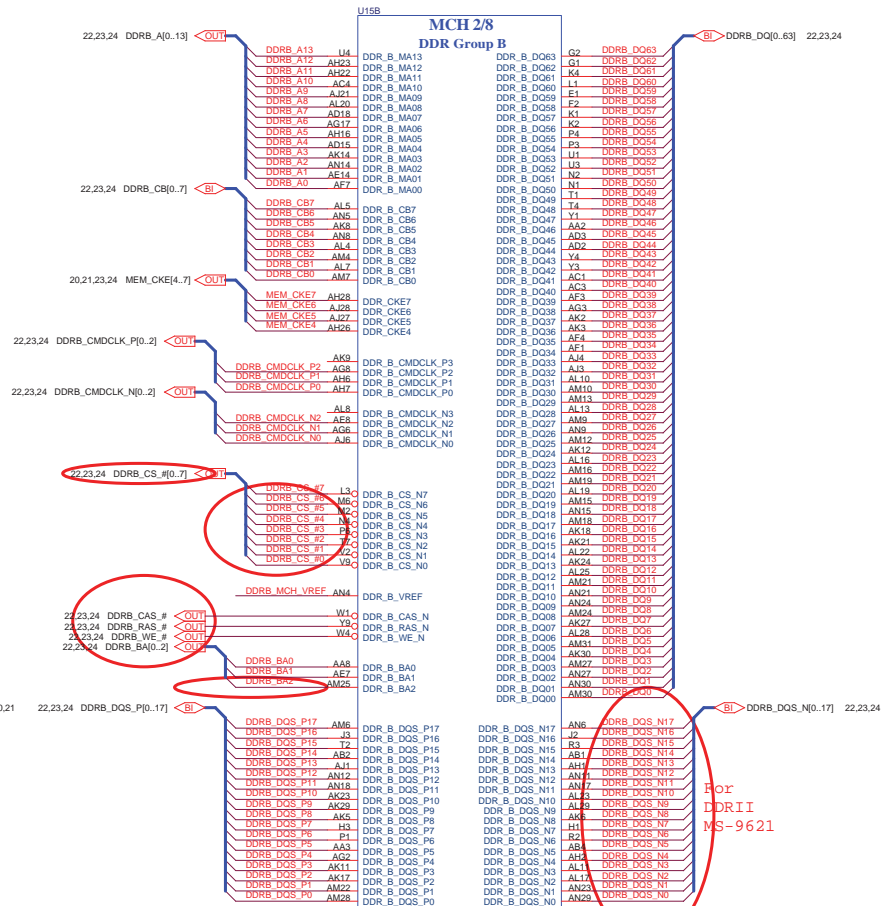
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Place R130 at the place where the HCPURST# signal starts to branch



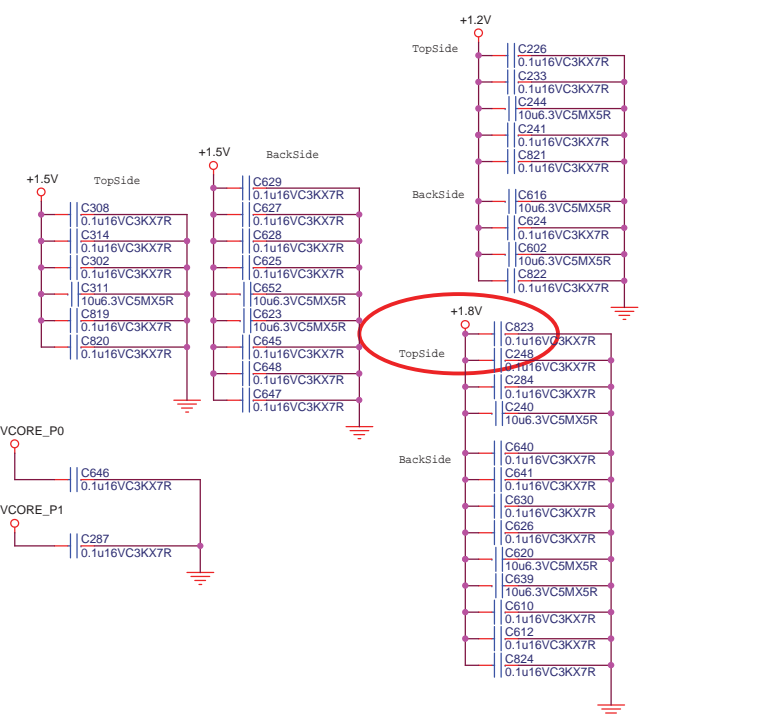
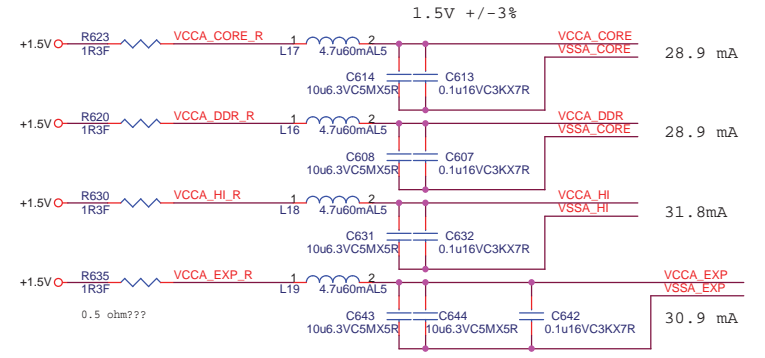
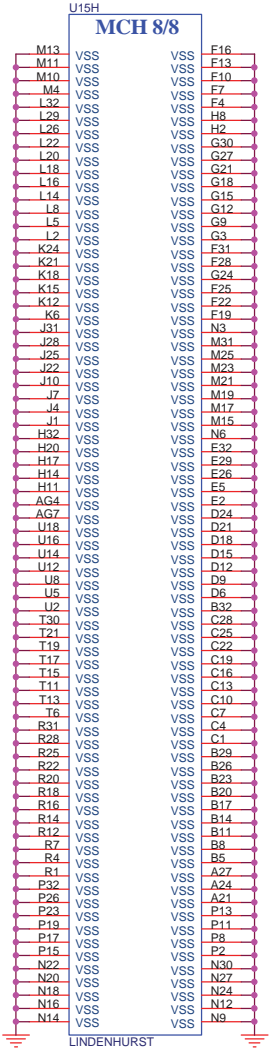
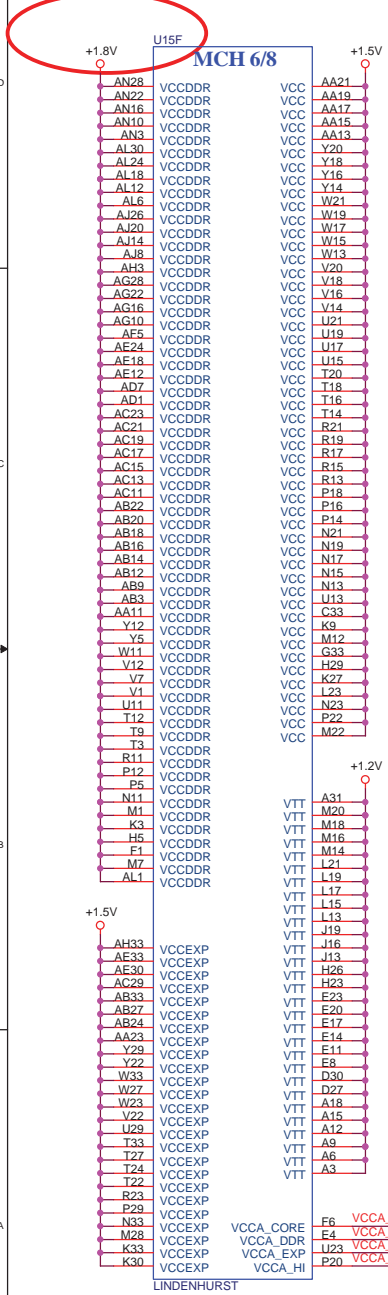
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Size A	Document Number	Rev 1.0
	MS-9621	
Date: Friday, March 25, 2005	Sheet 15 of 44	1



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Title	MCH A	
Size	Document Number	Rev
C	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 16 of 44



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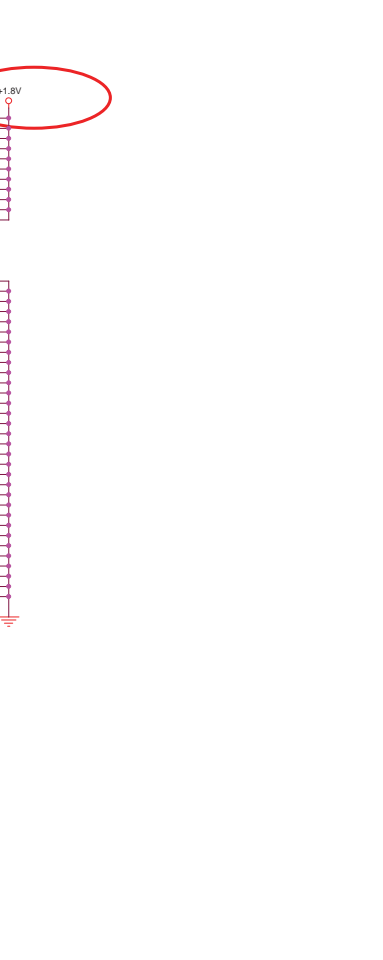
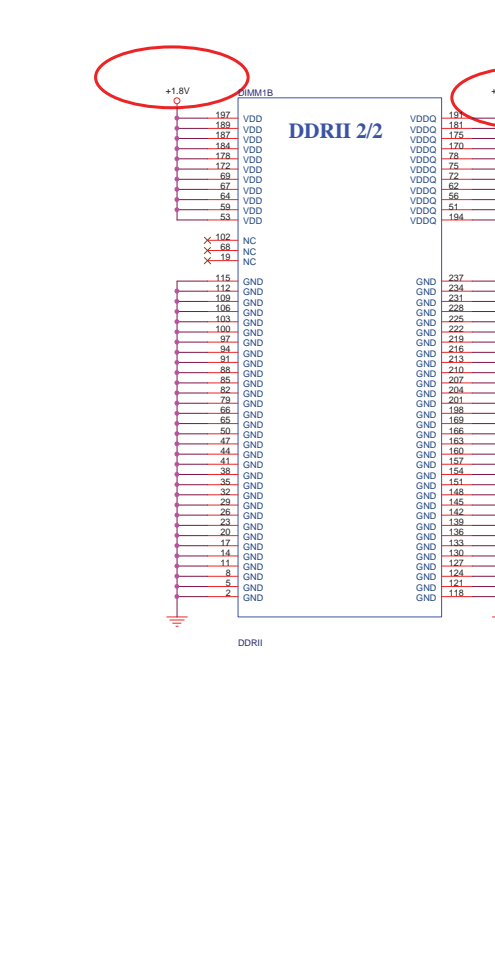
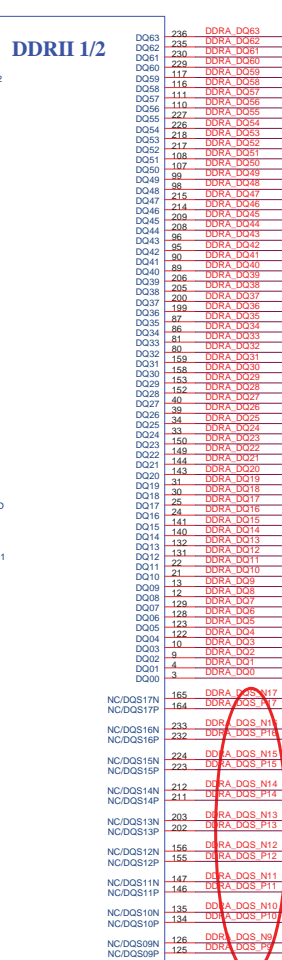
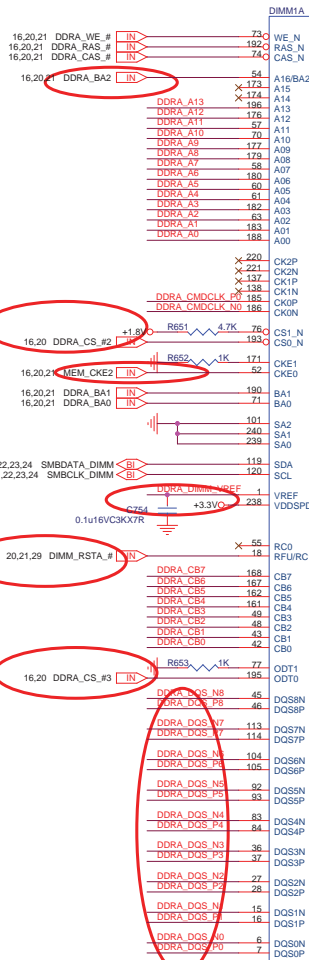
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Date: Friday, March 25, 2005 | Sheet: 18 of 44

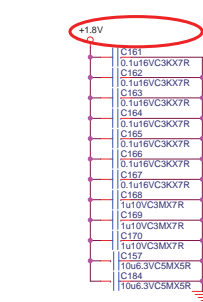
DIMM A1

SMBUS ADDR: 0XA0

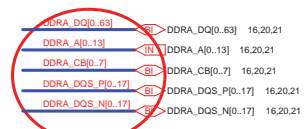
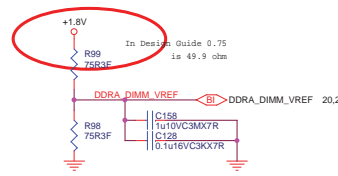
1010 000 0



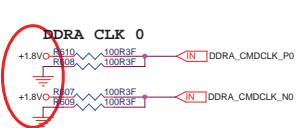
MS-9621 change
+2.5V to +1.8V



MS-9621 change
+2.5V to +1.8V



MS-9621 change
+2.5V to +1.8V



DIMM A1 CKE0,1 -> MEM_CKE2,X

DIMM A1 CS_#0,1 -> DDR_A_CS_#2,X

DIMM A1 ODT_#0,1 -> DDR_A_ODT_#3,X

MS-9621 change +1.25V_A to +1.8V

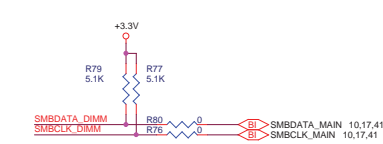
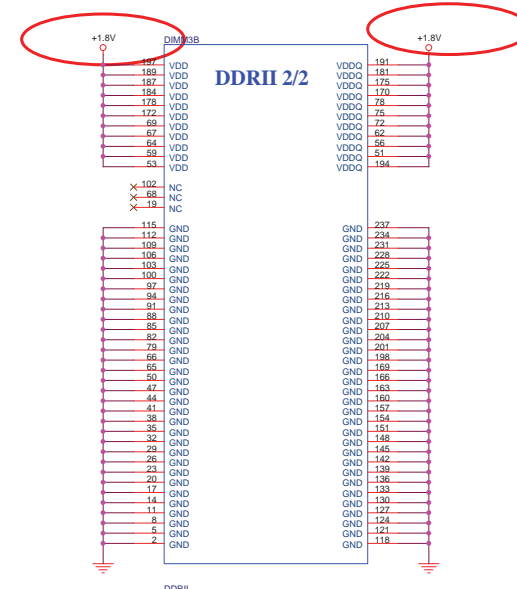
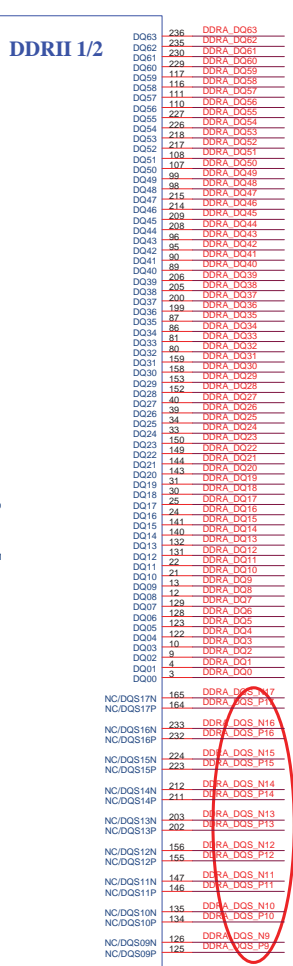
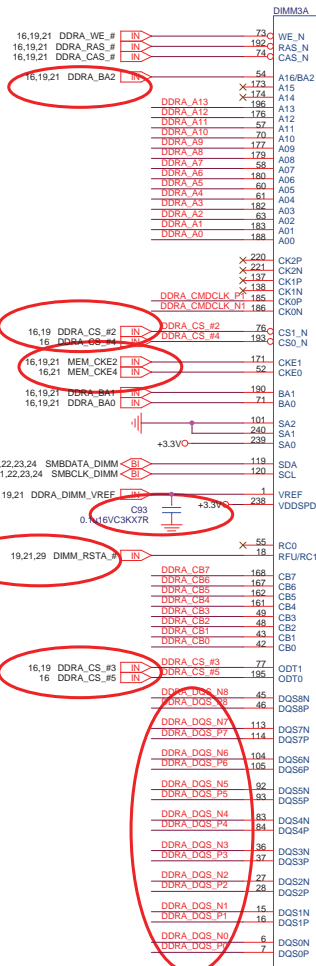


Title		DDR II-DIMM A1
Size	Document Number	MS-9621
Date	Friday, March 25, 2005	Sheet 19 of 44

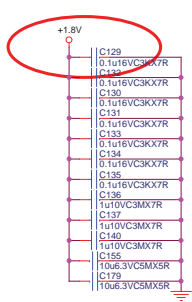
DIMM A2

SMBUS ADDR: 0XA2

1010 001 0

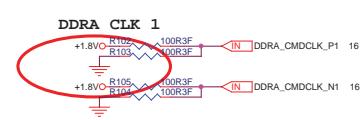


MS-9621 change+2.5V to +1.8V



- DDR_A_DQ[0..63] <-> DDR_A_DQ[0..63] 16,19,21
- DDR_A_A[0..13] <-> IN DDR_A_A[0..13] 16,19,21
- DDR_A_CB[0..7] <-> IN DDR_A_CB[0..7] 16,19,21
- DDR_A_DQS_P[0..17] <-> IN DDR_A_DQS_P[0..17] 16,19,21
- DDR_A_DQS_N[0..17] <-> IN DDR_A_DQS_N[0..17] 16,19,21

MS-9621 change+2.5V to +1.8V



DIMM A2 CKE0,1 -> MEM_CKE4,2

DIMM A2 CS_#0,1 -> DDRA_CS_#4,2
DIMM A2 ODT0,1 -> DDRA_CS_#5,3



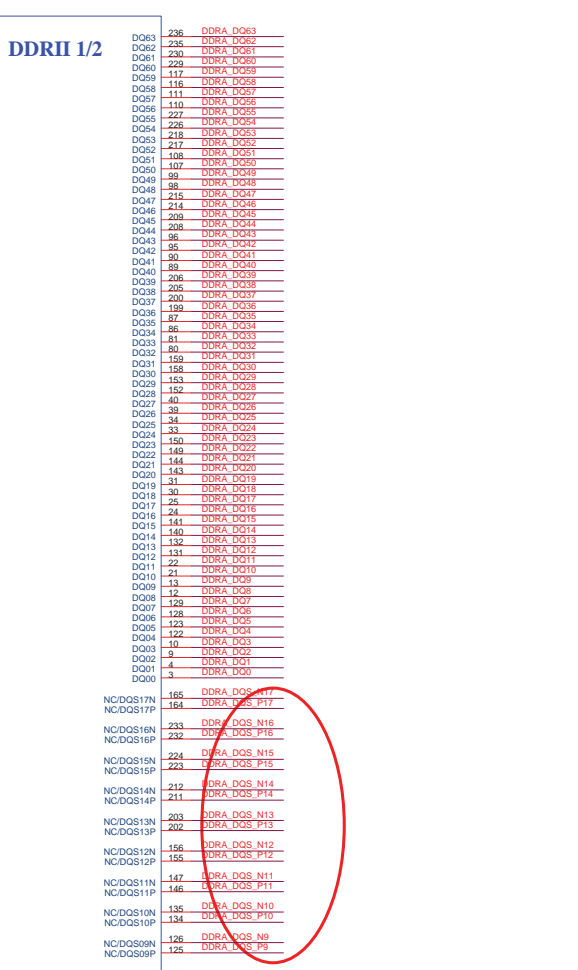
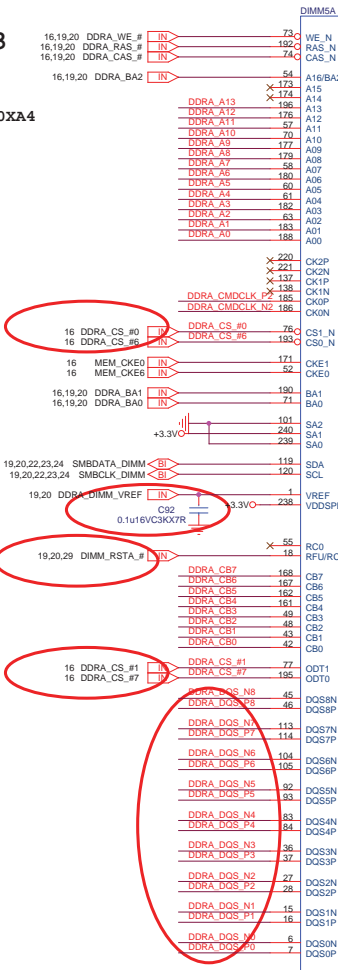
File	DDR II-DIMM A2	
Size	Document Number	Rev
	MS-9621	
Date:	Friday, March 25, 2005	Sheet 20 of 44

DIMM A3

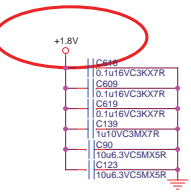
SMBUS ADDR: 0XA4

1010 010 0

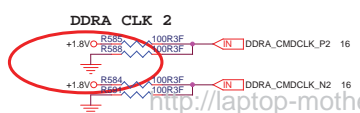
DDR II 1/2



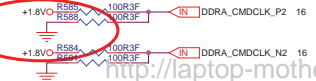
MS-9621 change
+2.5V to +1.8V



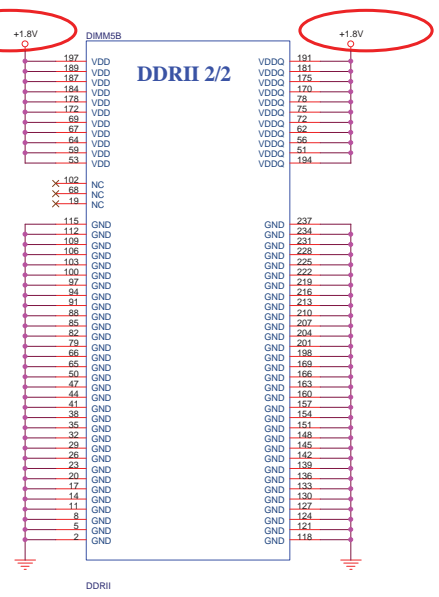
MS-9152 change
+2.5V to +1.8V



DDR A CLK 2



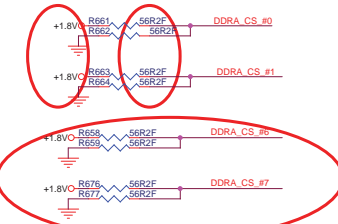
DDR II 2/2



DIMM A3 CKE0,1 -> MEM_CKE6,0

DIMM A3CS_#0,1 -> DDR_A_CS_#6,0

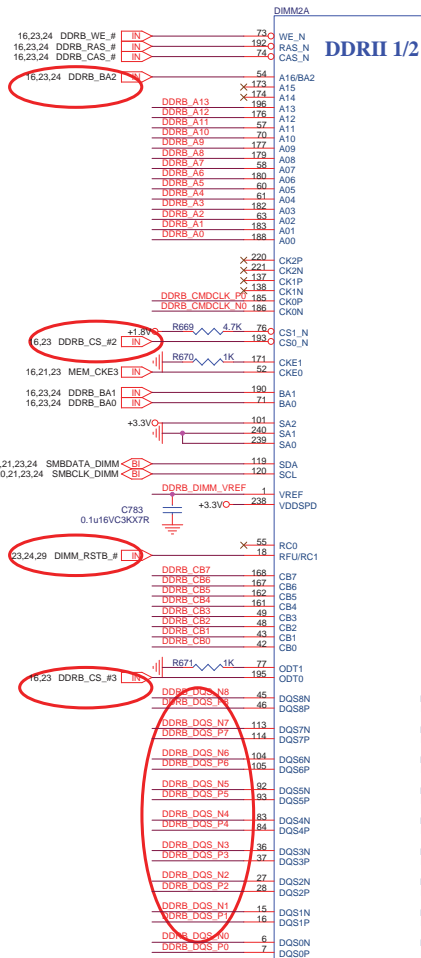
DIMM A3 ODT0,1 -> DDR_A_CS_#7,1



MS-9621 DDR-II A
channel
terminator

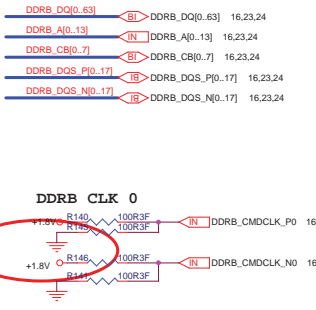
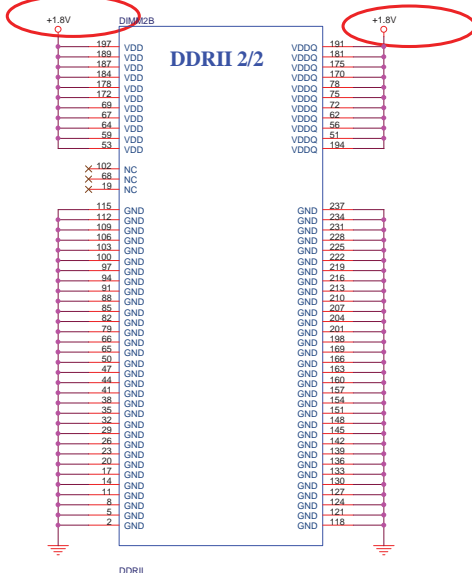
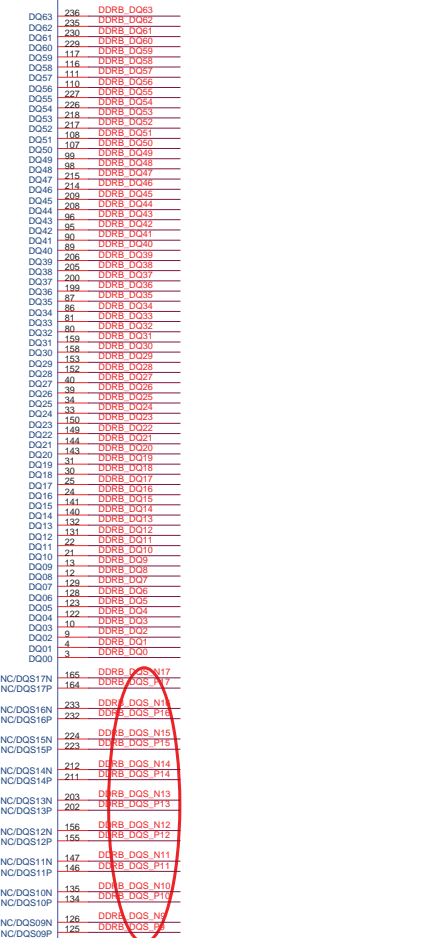
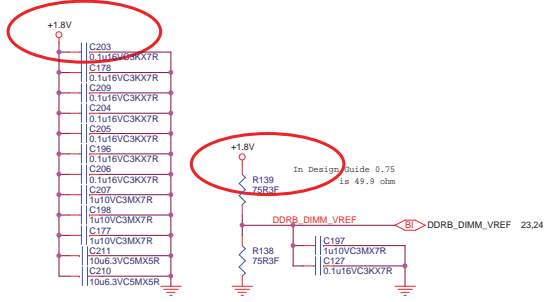
Title		
DDR II-DIMM A3		
Size	Document Number	Rev
	MS-9621	
Date	Friday, March 25, 2005	Sheet 21 of 44

DIMM B1
 SMBUS ADDR: 0XA8
 1010 100 0



DDR II

MS-9621change
 +2.5V to
 +1.8V



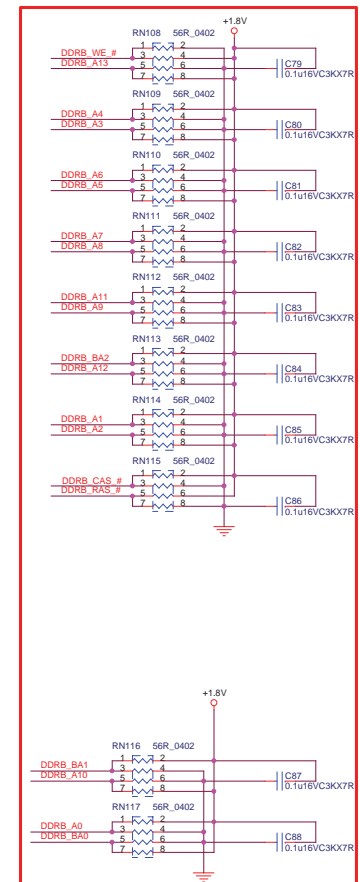
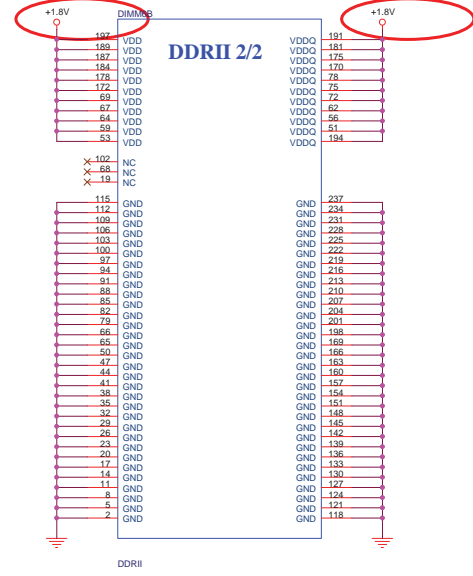
DIMM B1 CKE0,1 -> MEM_CKE3,X
 DIMM B1 CS_#0,1 -> DDRB_CS_#2,X
 DIMM B1 ODT0,1 -> DDRB_CS_#3,X



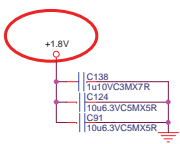
File	DDR II-DIMM B1	
Size	Document Number	Rev
	MS-9621	
Date:	Friday, March 25, 2005	Sheet 22 of 44

DIMM B3

SMBUS ADDR: 0XAC
1010 110 0

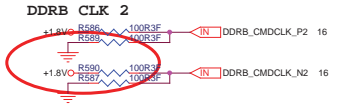


MS-9621 change +2.5V to +1.8V

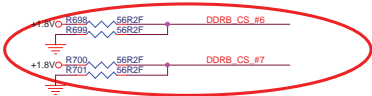
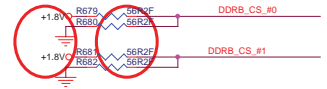


- DDR_B DQ[0..63] <BI> DDRB_DQ[0..63] 16,22,23
- DDR_B A[0..13] <IN> DDRB_A[0..13] 16,22,23
- DDR_B CB[0..7] <BI> DDRB_CB[0..7] 16,22,23
- DDR_B DQS_P[0..17] <BI> DDRB_DQS_P[0..17] 16,22,23
- DDR_B DQS_N[0..17] <BI> DDRB_DQS_N[0..17] 16,22,23

MS-9152 change +2.5V to +1.8V

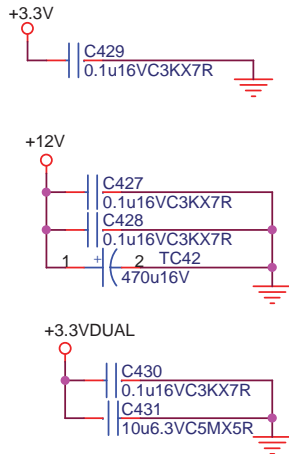
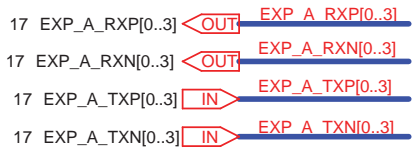


- DIMM B3 CKE0,1 -> MEM_CKE7,1
- DIMM B3 CS_#0,1 -> DDRB_CS_#6,0
- DIMM B3 ODT0,1 -> DDRB_CS_#7,1

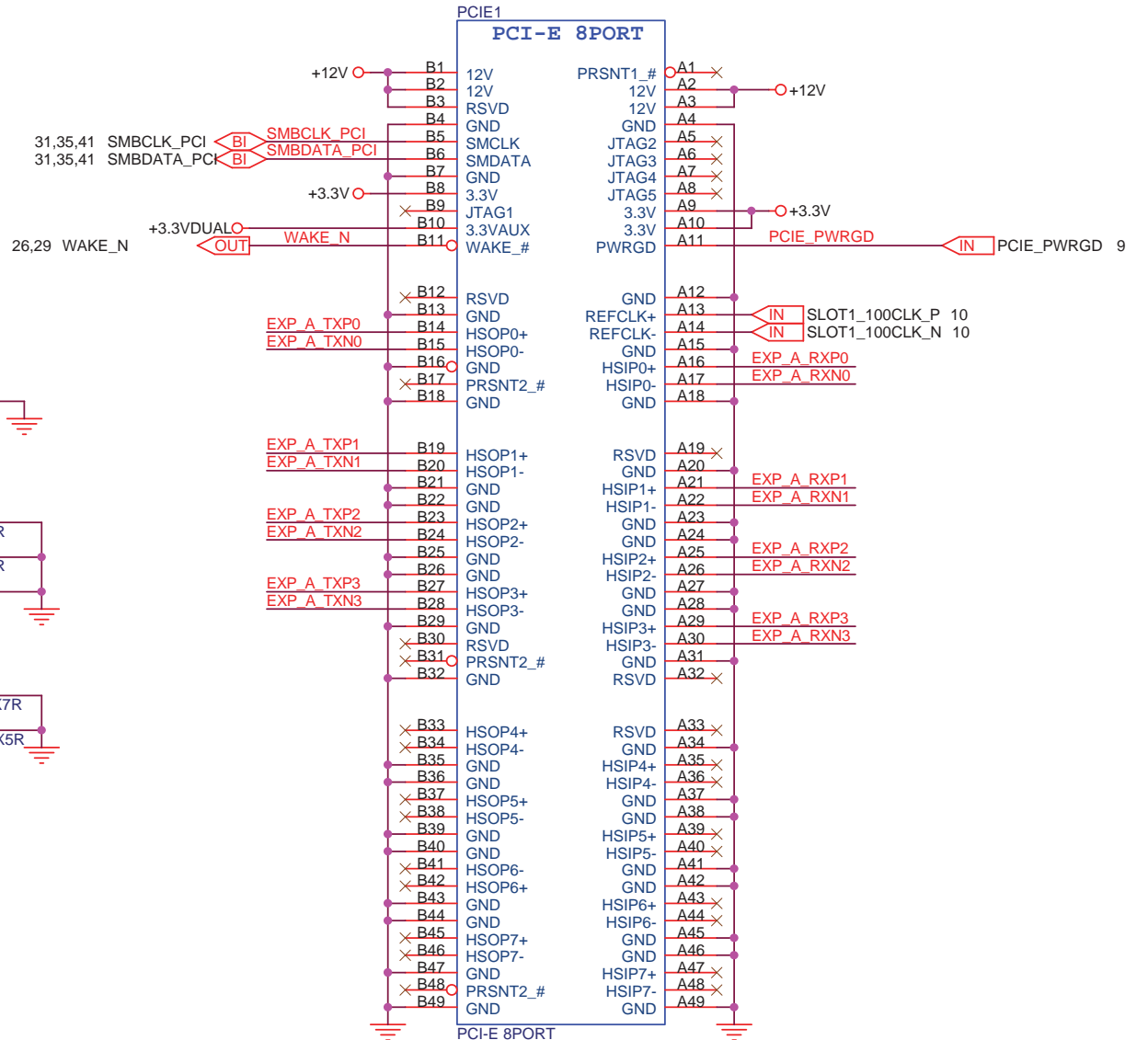


MSB		DDR II-DIMM B3	
Size	Document Number	MS-9621	
Date	Friday, March 25, 2005	Sheet	24 of 44

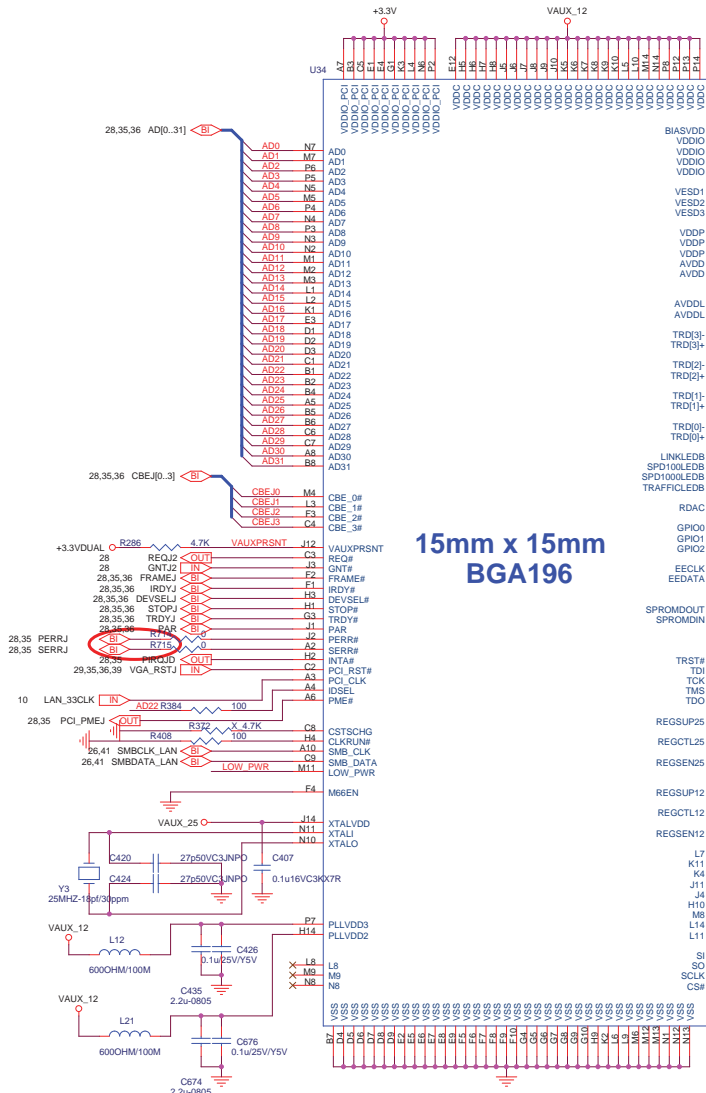
PCI-E *4



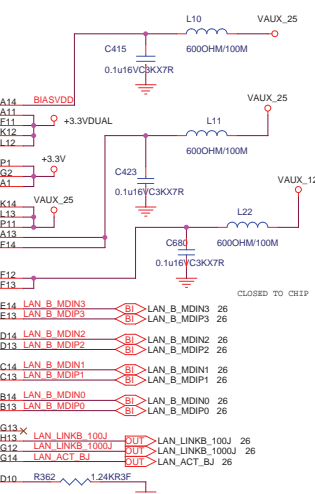
25 W limit
 +3.3V 3A
 +12V 2.1A
 +3.3VDUAL 375mA



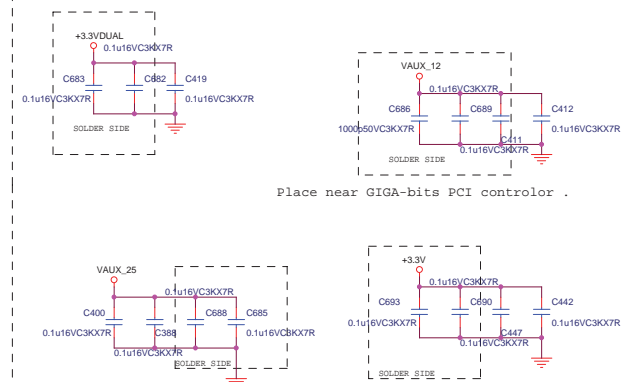
Micro-Star Int'l Co., Ltd.		
No.69, Li-De St, Jung-He City, Taipei Hsien, Taiwan. http://www.msi.com.tw		
PCI-E SLOT		
Title		
Size A4	Document Number	Rev
	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 25 of 44



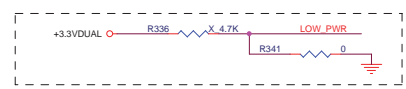
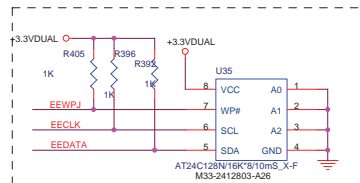
**15mm x 15mm
BGA196**



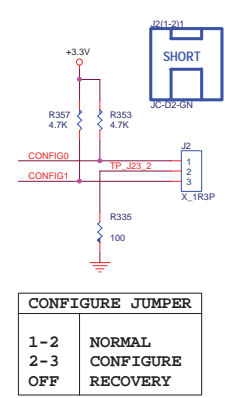
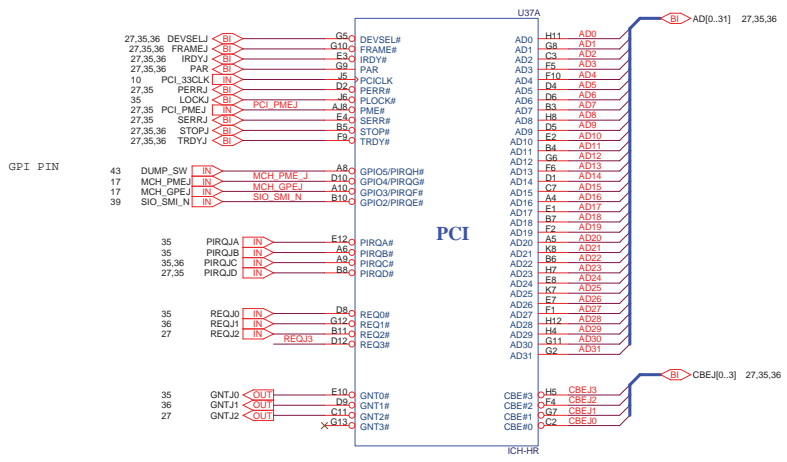
3.3V 3.3mA
2.5V 230 mA
1.2V 312mA



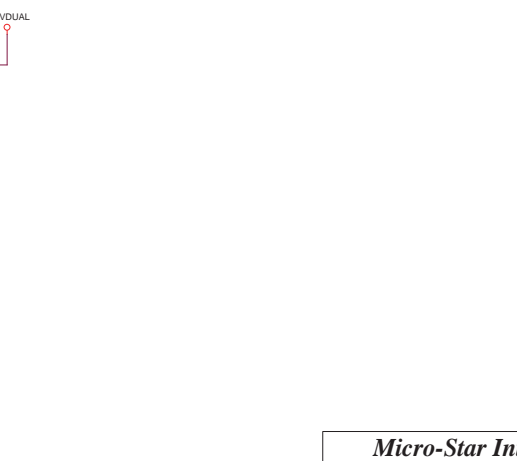
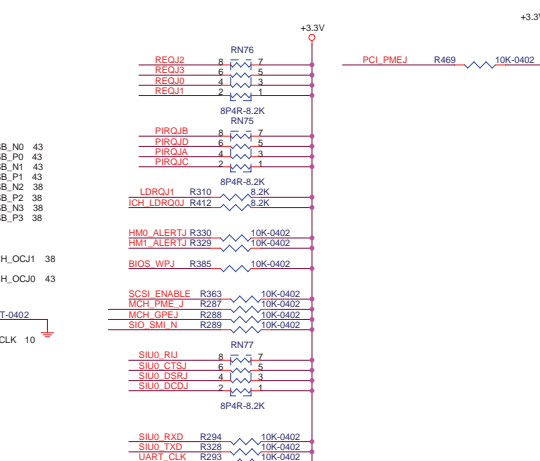
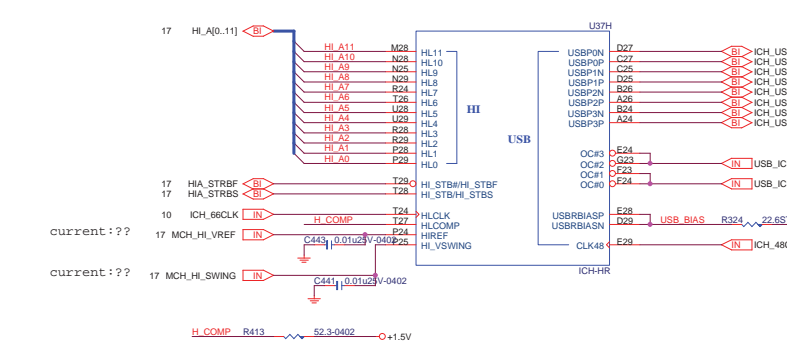
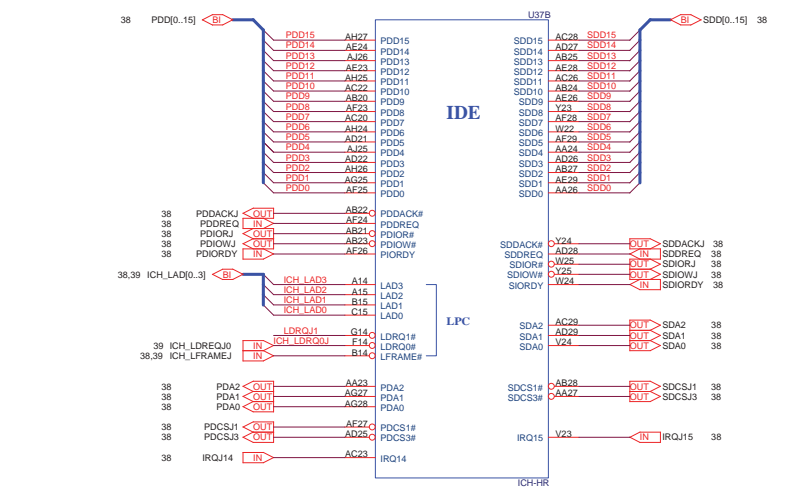
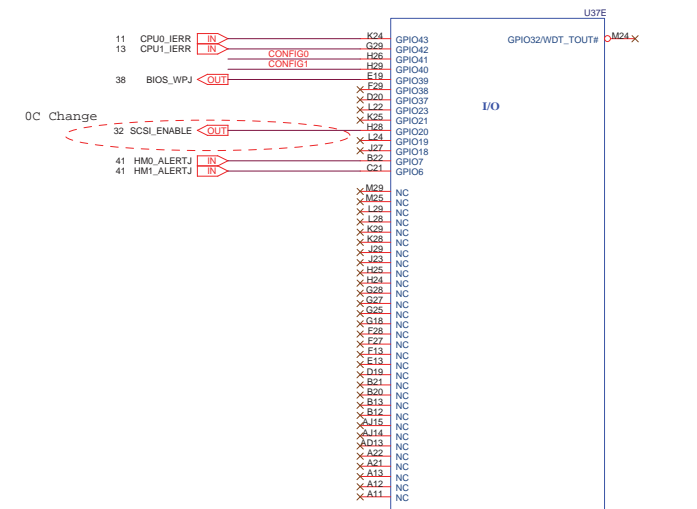
Place near GIGA-bits PCI controller .



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Title	BCM 5705	
Size	Document Number	Rev
C	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 27 of 44



CONFIGURE JUMPER	
1-2	NORMAL
2-3	CONFIGURE
OFF	RECOVERY



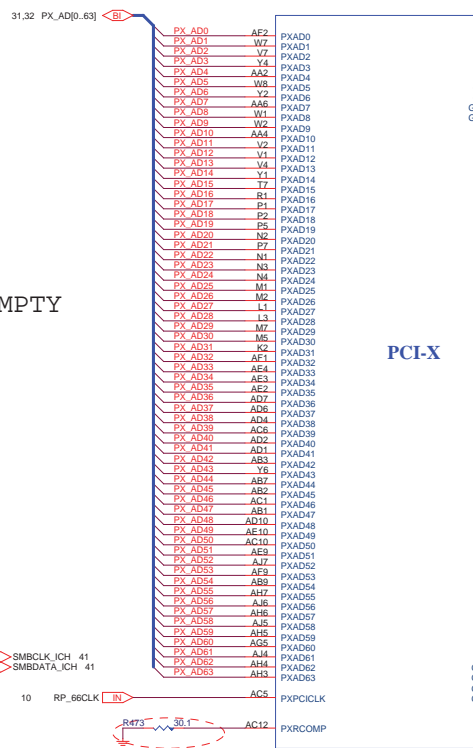
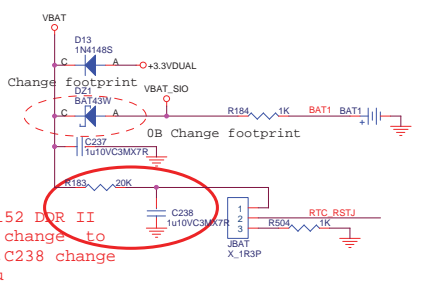
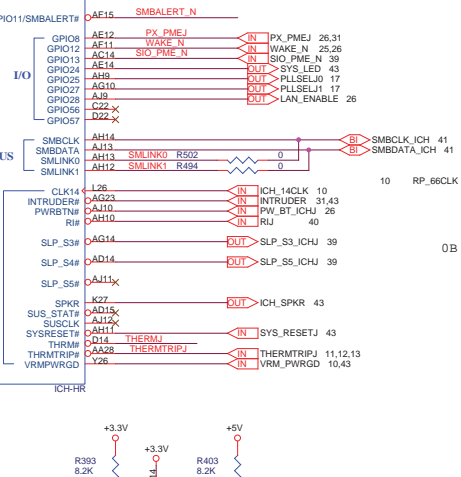
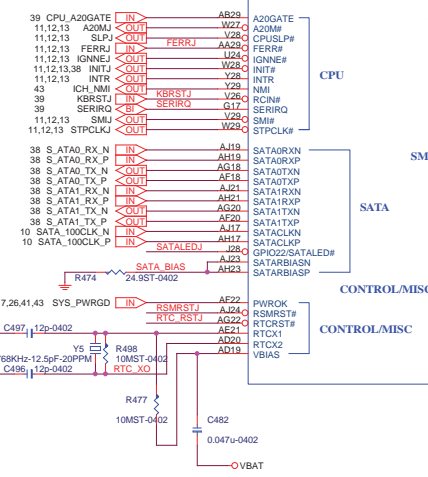
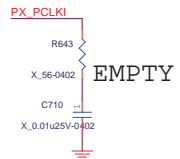
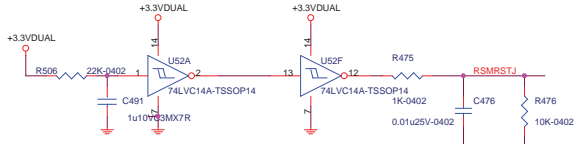
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Title: **HR A**

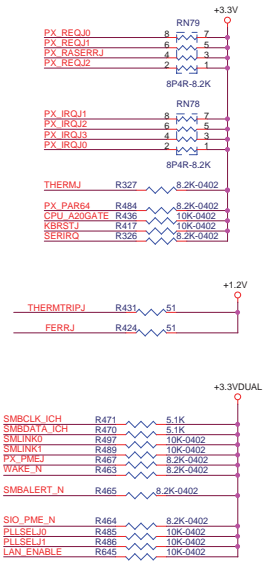
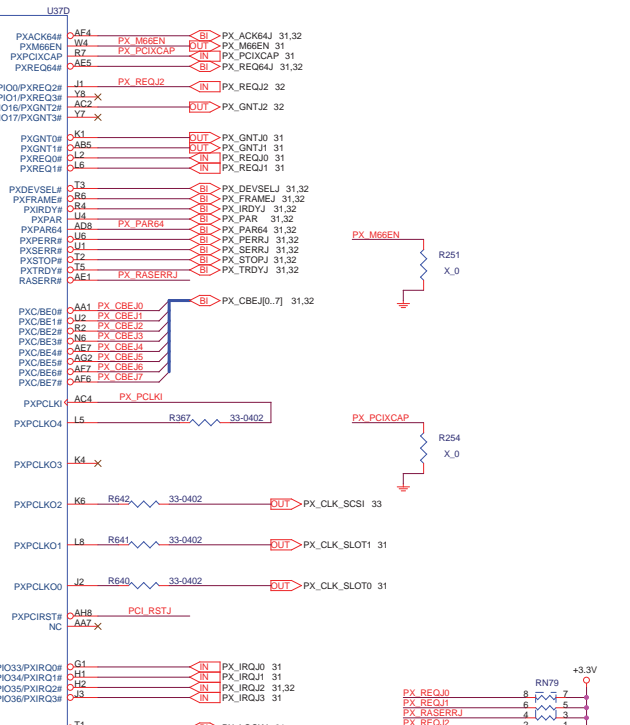
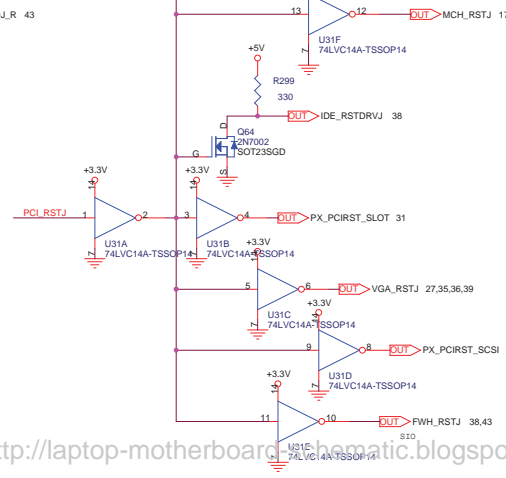
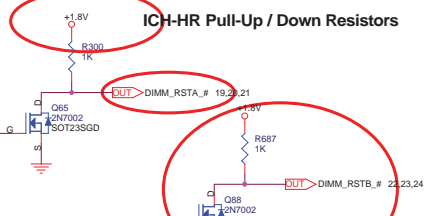
Size: Document Number **MS-9621** Rev: 1.0

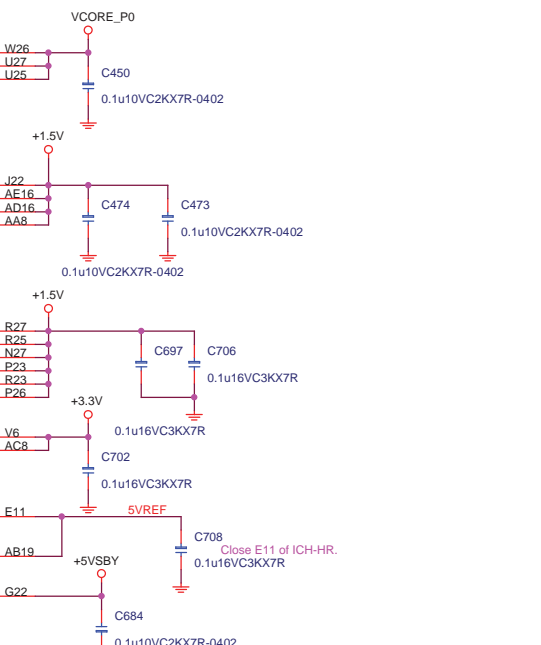
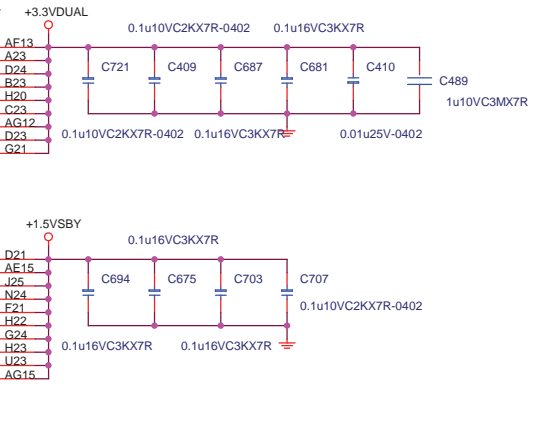
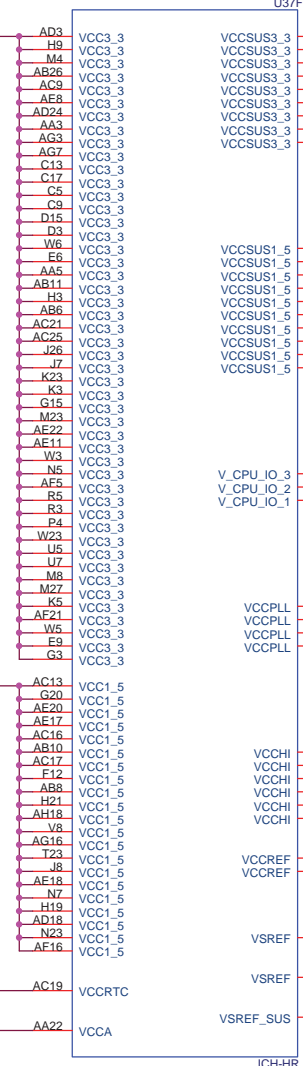
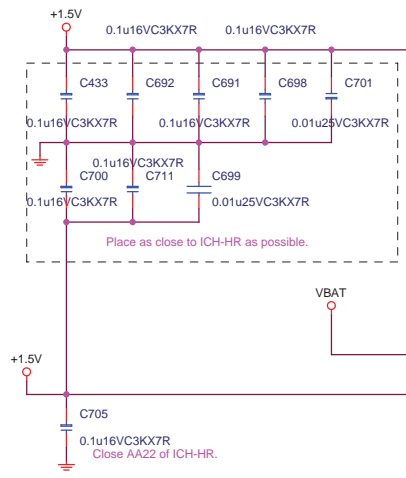
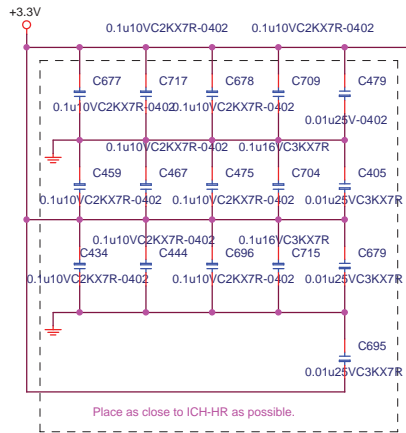
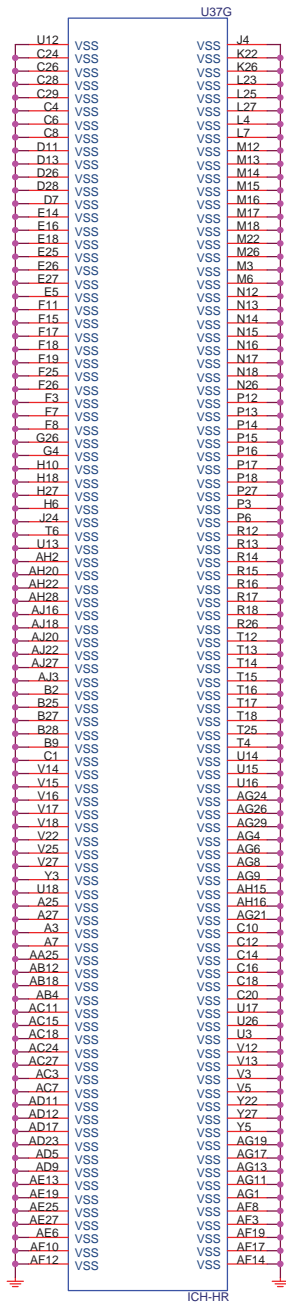
Date: Friday, March 25, 2005 Sheet: 28 of 44

Resume Reset Circuitry
Using a 22msec delay

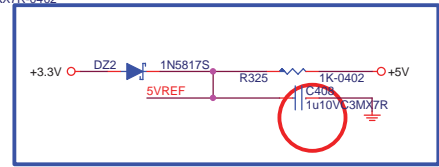


0B Change footprint & PN
MS-9621 DDR II change P2V5 to +1.8V, R300 change to 1K

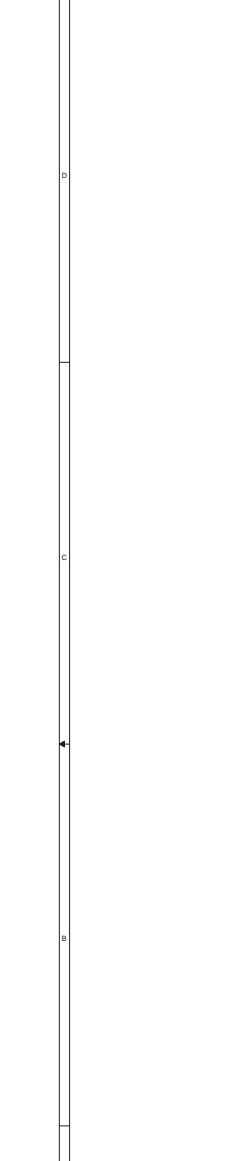
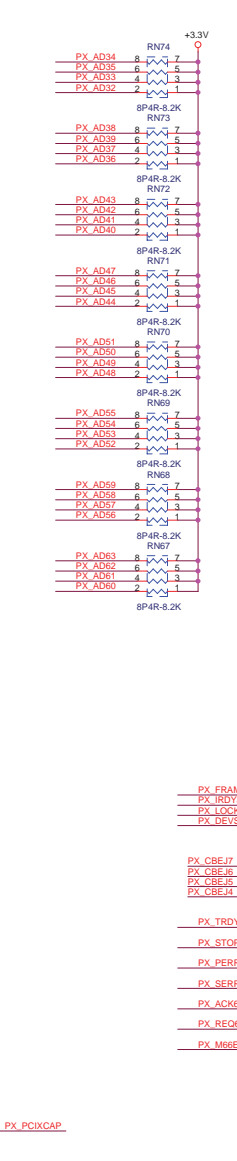
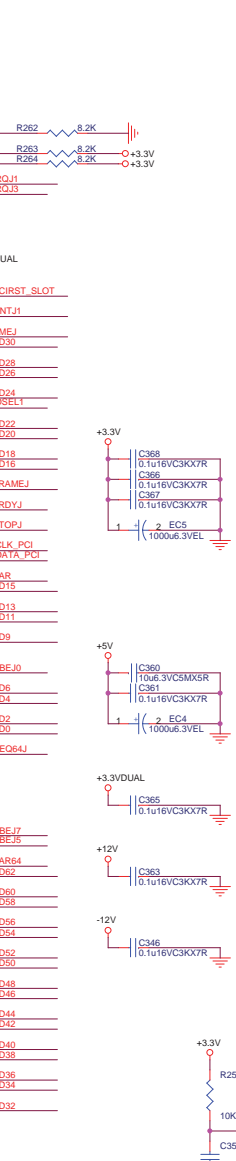
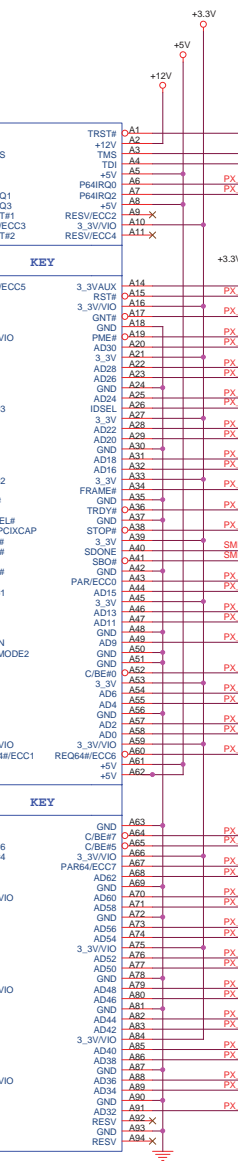
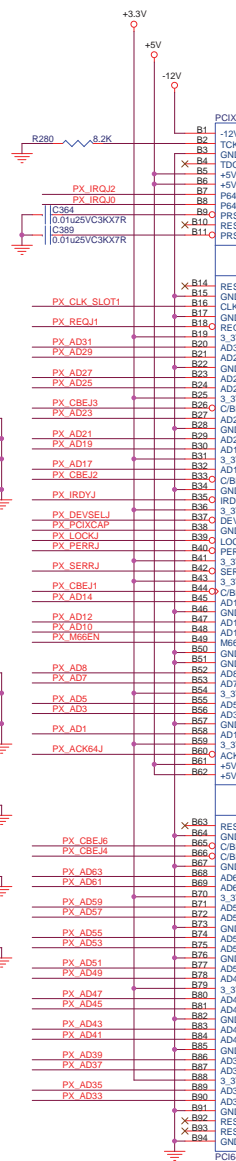
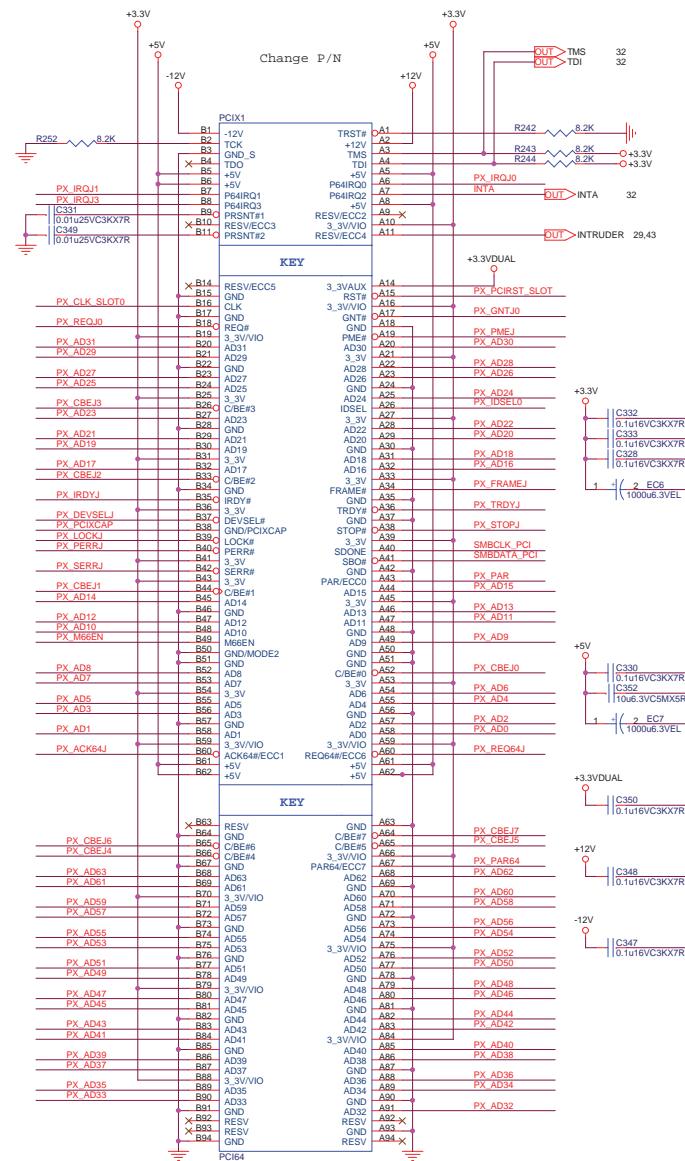




+1.5V 732 mA (CORE) + 99 mA (VCCHI)
 +1.5VSBY S0 75mA S3 15.6 mA
 +3.3V 528 mA
 +3.3VDUAL S0 142 mA S1 2.3 mA



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Title			
HR C			
Size	Document Number	Rev	
A3	MS-9621	1.0	
Date:	Friday, March 25, 2005	Sheet	30 of 44



29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT0	IN	PX_CLK_SLOT0
29 PX_PCIRST_SLOT	IN	PX_PCIRST_SLOT
29 PX_REQ0	IN	PX_REQ0
29 PX_GNTJ0	IN	PX_GNTJ0
PX_AD17	R237	100
PX_AD17	R237	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT1	IN	PX_CLK_SLOT1
29 PX_REQ1	IN	PX_REQ1
29 PX_GNTJ1	IN	PX_GNTJ1
PX_AD18	R236	100
PX_AD18	R236	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT1	IN	PX_CLK_SLOT1
29 PX_REQ1	IN	PX_REQ1
29 PX_GNTJ1	IN	PX_GNTJ1
PX_AD18	R236	100
PX_AD18	R236	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT1	IN	PX_CLK_SLOT1
29 PX_REQ1	IN	PX_REQ1
29 PX_GNTJ1	IN	PX_GNTJ1
PX_AD18	R236	100
PX_AD18	R236	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT1	IN	PX_CLK_SLOT1
29 PX_REQ1	IN	PX_REQ1
29 PX_GNTJ1	IN	PX_GNTJ1
PX_AD18	R236	100
PX_AD18	R236	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

29.32 PX_IRQ[0..3]	OUT	PX_IRQ[0..3]
29 PX_CLK_SLOT1	IN	PX_CLK_SLOT1
29 PX_REQ1	IN	PX_REQ1
29 PX_GNTJ1	IN	PX_GNTJ1
PX_AD18	R236	100
PX_AD18	R236	100
29.32 PX_AD[0..63]	BI	PX_AD[0..63]
29.32 PX_CBE[0..7]	BI	PX_CBE[0..7]
29.32 PX_ACK64J	BI	PX_ACK64J
29.32 PX_REQ64J	BI	PX_REQ64J
29.32 PX_PARB4	BI	PX_PARB4
29.32 PX_PAR	BI	PX_PAR
29.32 PX_STOPJ	BI	PX_STOPJ
29.32 PX_PERRJ	BI	PX_PERRJ
29.32 PX_SERRJ	BI	PX_SERRJ
29.32 PX_IRDYJ	BI	PX_IRDYJ
29.32 PX_TRDYJ	BI	PX_TRDYJ
29.32 PX_FRAMEJ	BI	PX_FRAMEJ
29.32 PX_DEVSELJ	BI	PX_DEVSELJ
29.32 PX_LOCKJ	BI	PX_LOCKJ
29.32 PX_PCI0CAP	OUT	PX_PCI0CAP
29.32 PX_M66EN	IN	PX_M66EN
26.35.41 SMBCLK_PCI	BI	SMBCLK_PCI
26.35.41 SMBDATA_PCI	BI	SMBDATA_PCI
26.29 PX_PMEJ	OUT	PX_PMEJ

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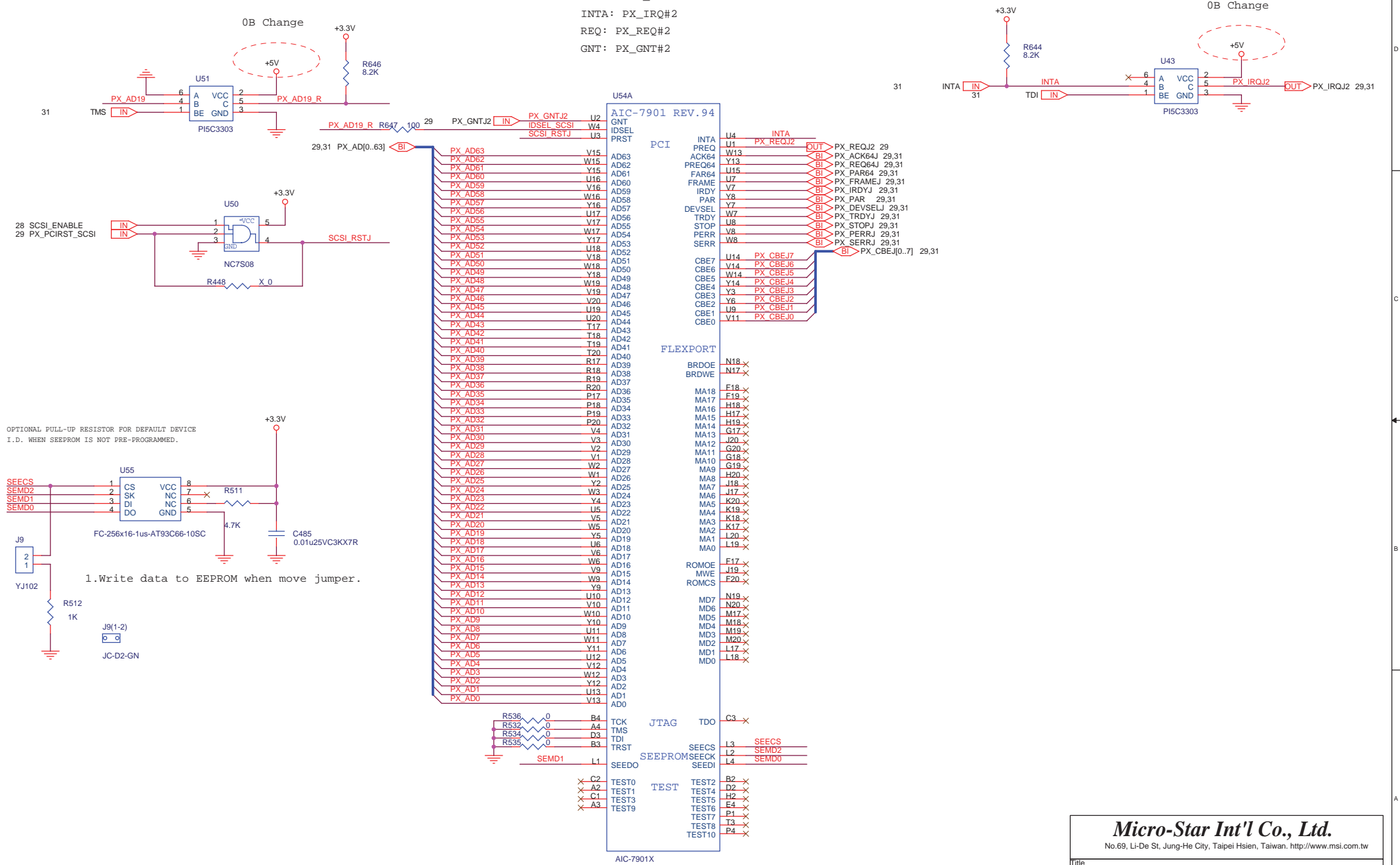
Title: **PCI-X SLOT 1,2**

Size: Document Number **MS-9621** Rev: 1.0

Date: Friday, March 25, 2005 Sheet: 31 of 44

PCIX-66 Interface

IDSEL: PX_AD19
 INTA: PX_IRQ#2
 REQ: PX_REQ#2
 GNT: PX_GNT#2



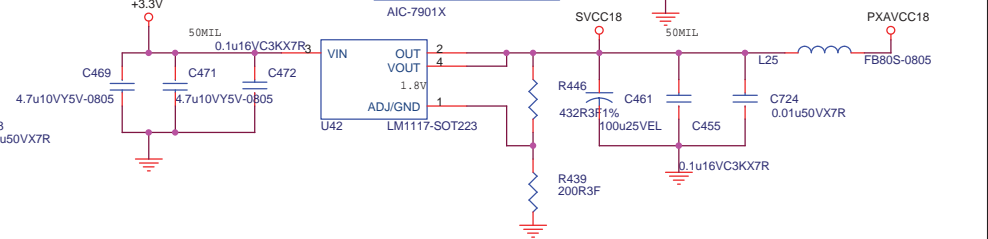
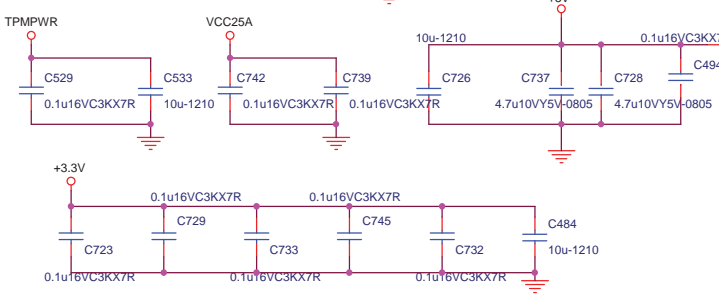
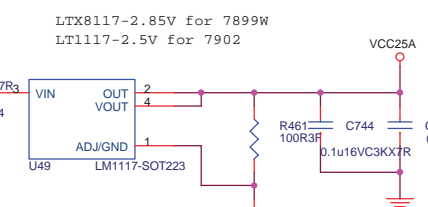
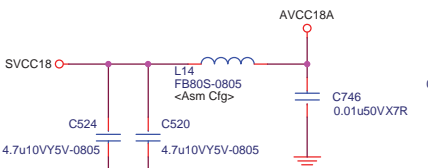
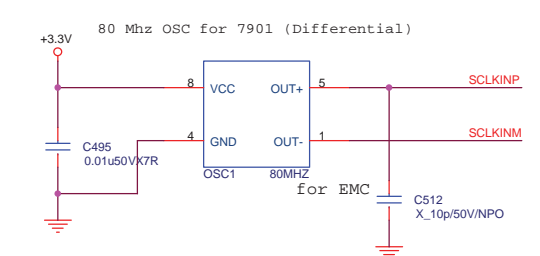
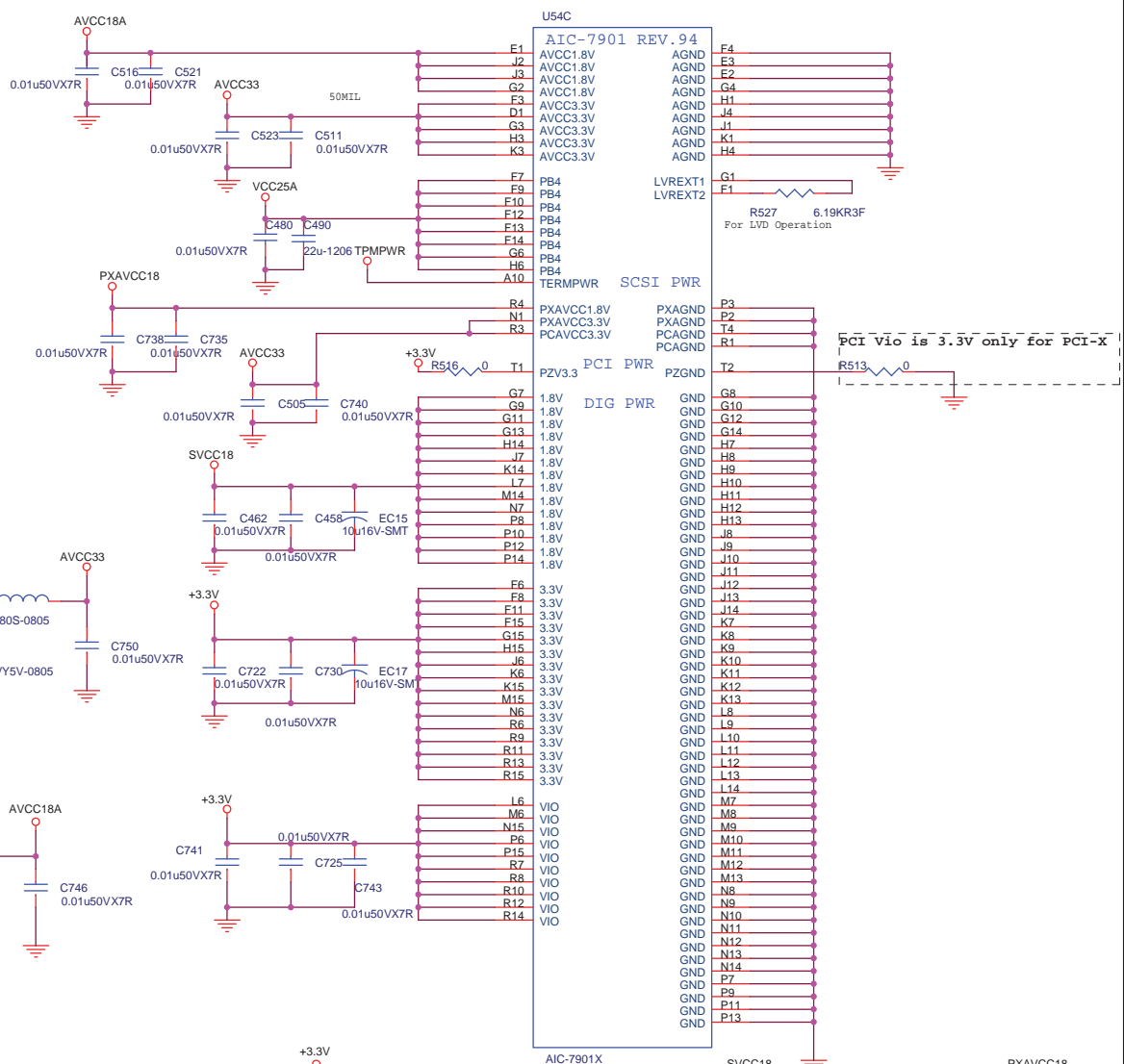
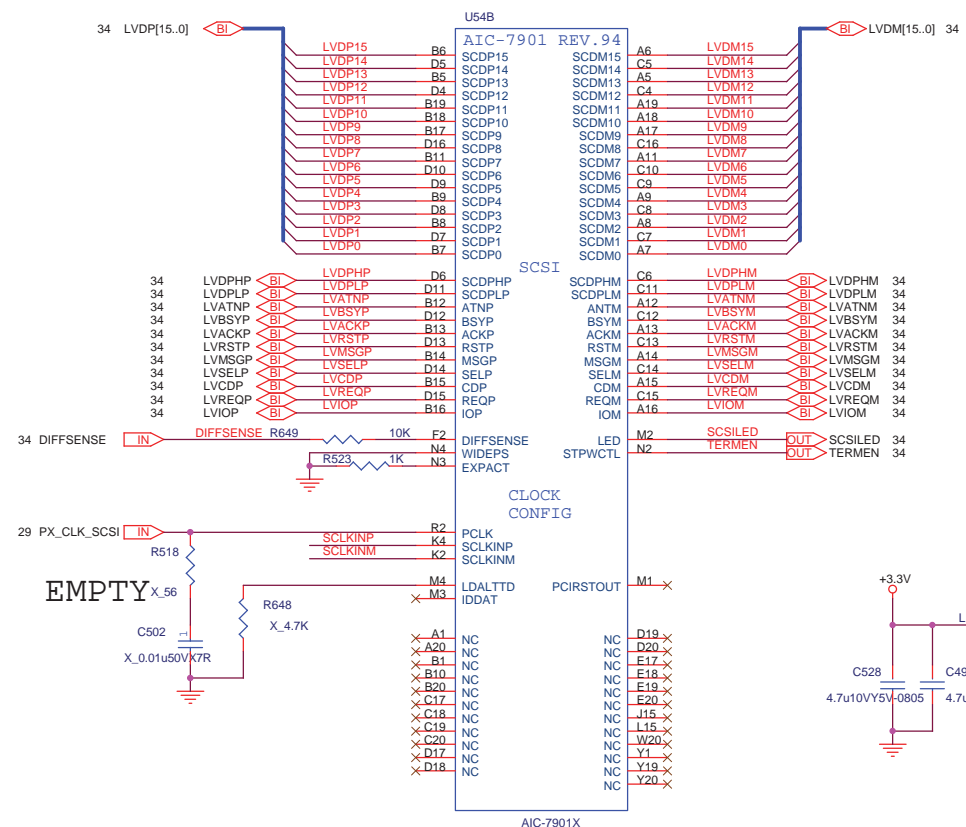
OPTIONAL PULL-UP RESISTOR FOR DEFAULT DEVICE
 I.D. WHEN SEEPROM IS NOT PRE-PROGRAMMED.

1. Write data to EEPROM when move jumper.

<http://laptop-motherboard-schematic.blogspot.com/>

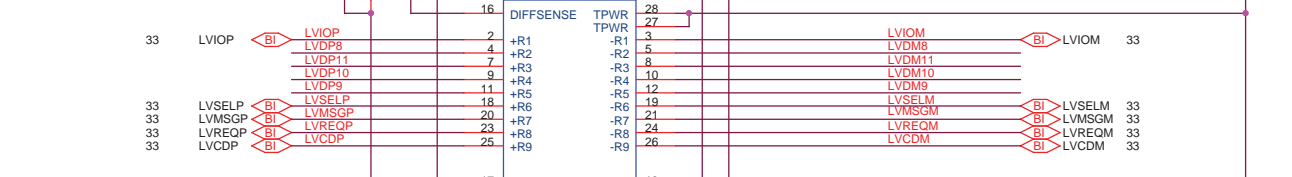
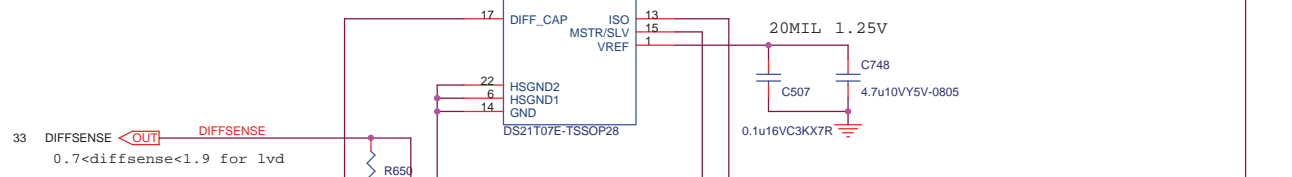
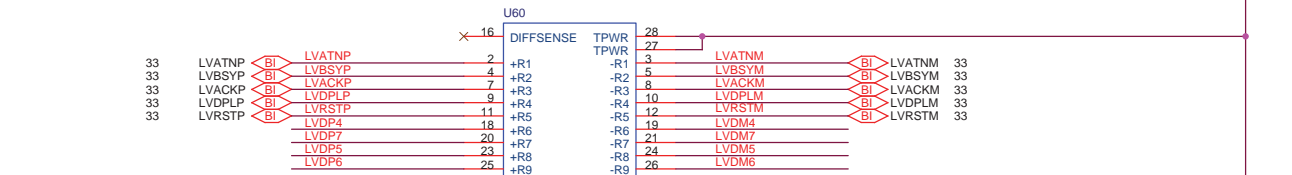
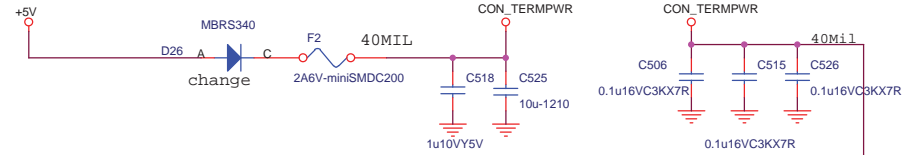
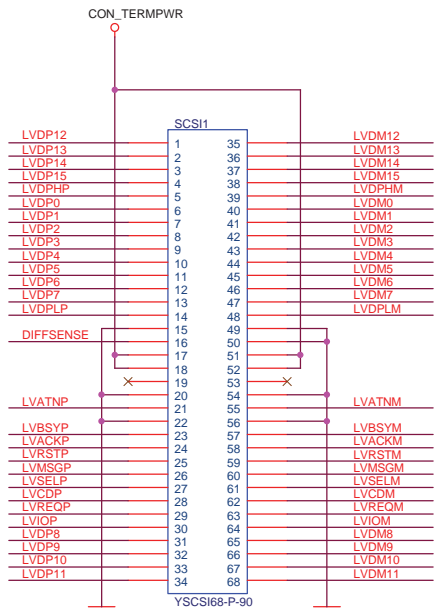
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Title		
SCSI A		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 32 of 44

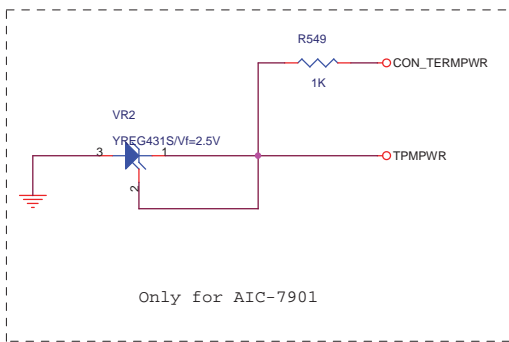
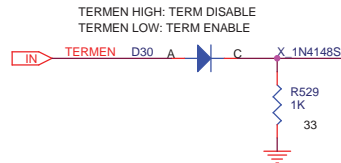
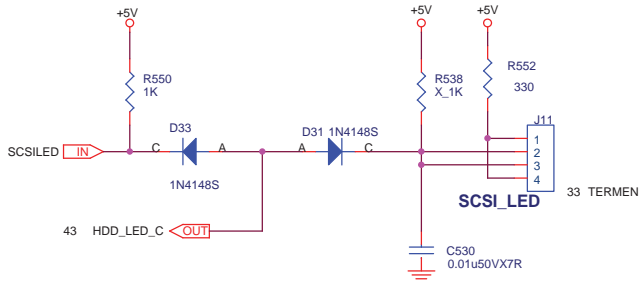


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Title		
SCSI B		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 33 of 44

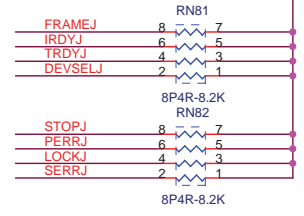
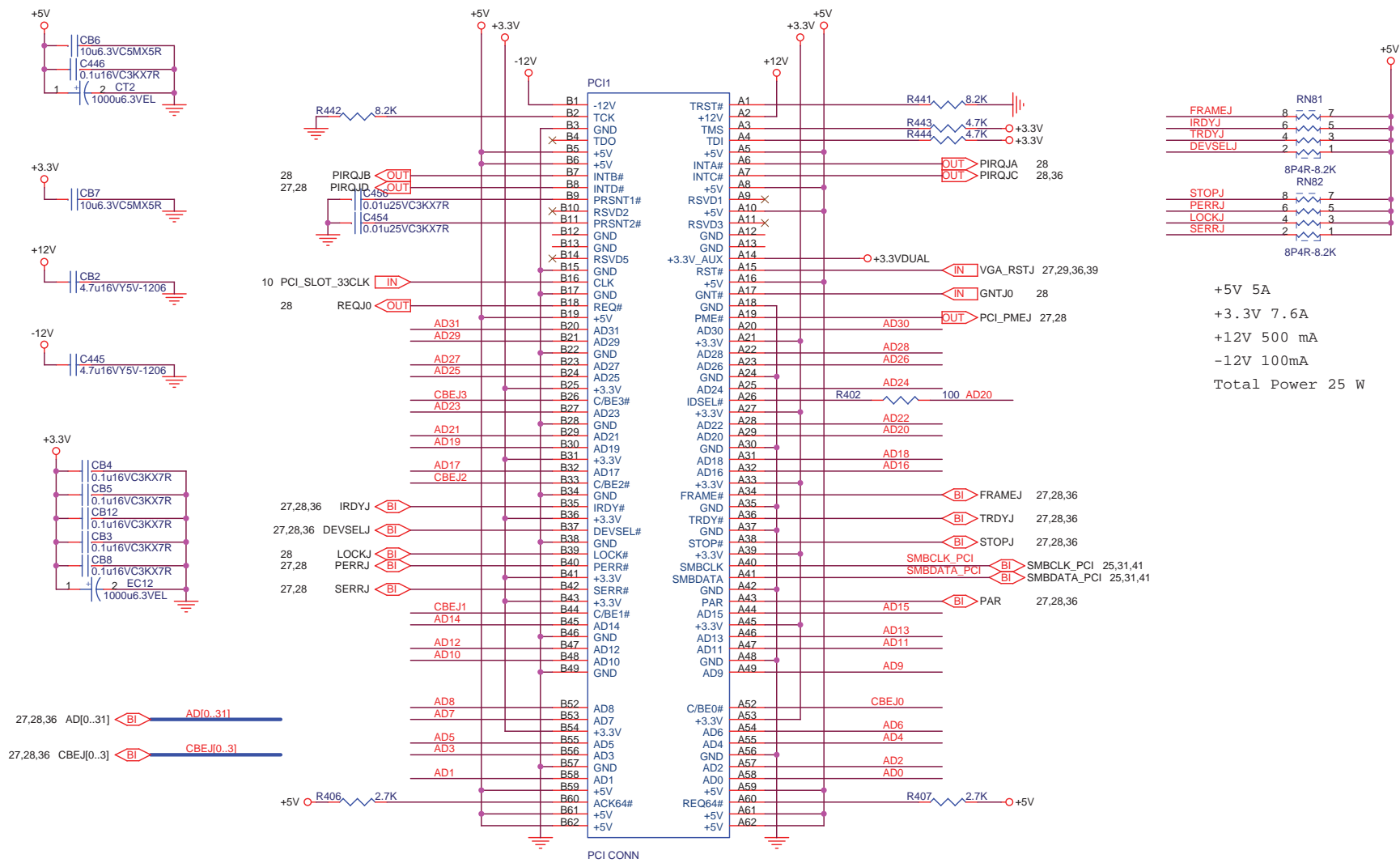


SCSI 1x4 LED Header

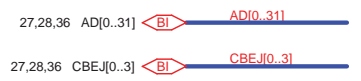


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Title		
SCSI C		
Size	Document Number	Rev
A3	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 34 of 44



+5V 5A
 +3.3V 7.6A
 +12V 500 mA
 -12V 100mA
 Total Power 25 W

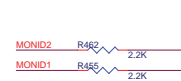
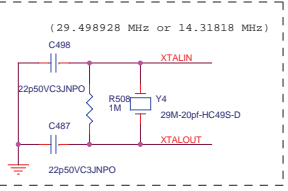
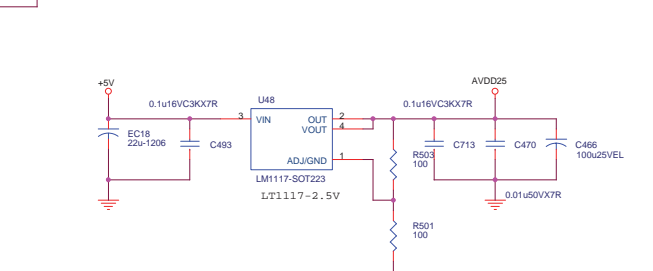
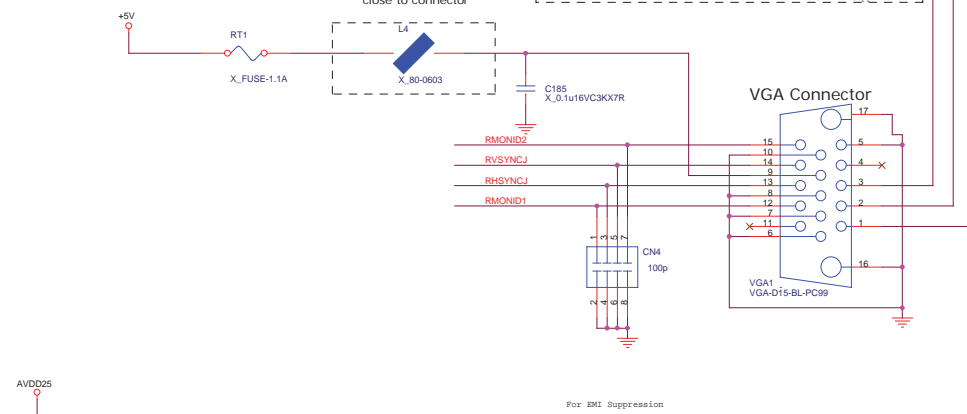
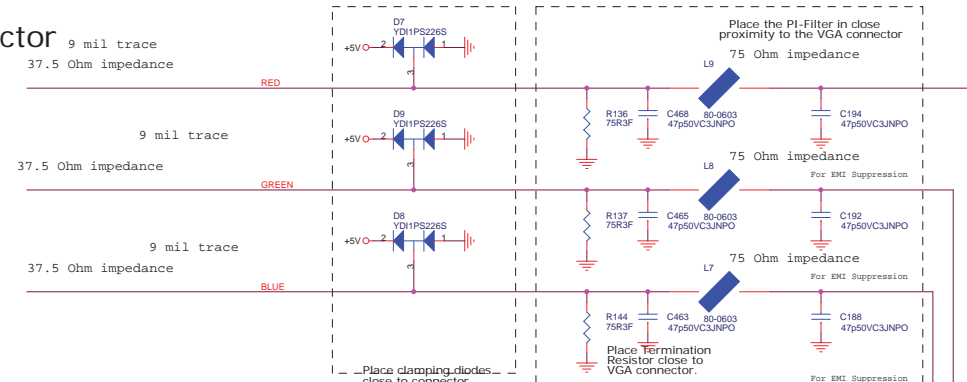
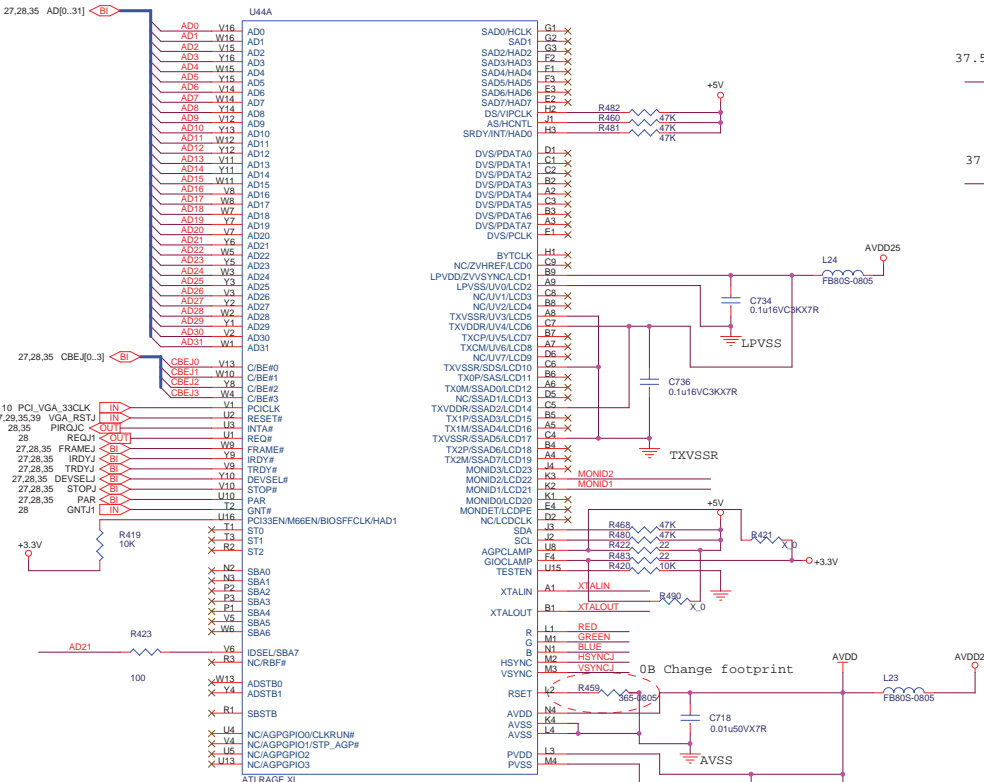


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Title		
PCI 32 SLOT		
Size	Document Number	Rev
B	MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet 35 of 44

VGA
 IDSEL: AD21
 INT: PIRQD
 REQ: REQ1
 GNT: GNT1

Video Connector

9 mil trace
 37.5 Ohm impedance



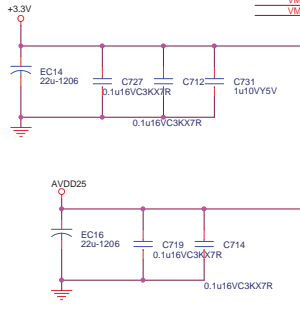
<http://laptop-motherboard-schematic.blogspot.com/>

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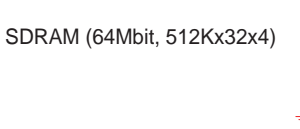
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Size: Document Number **MS-9621** Rev: 1.0

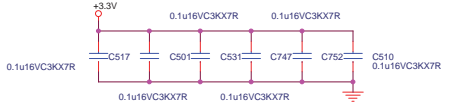
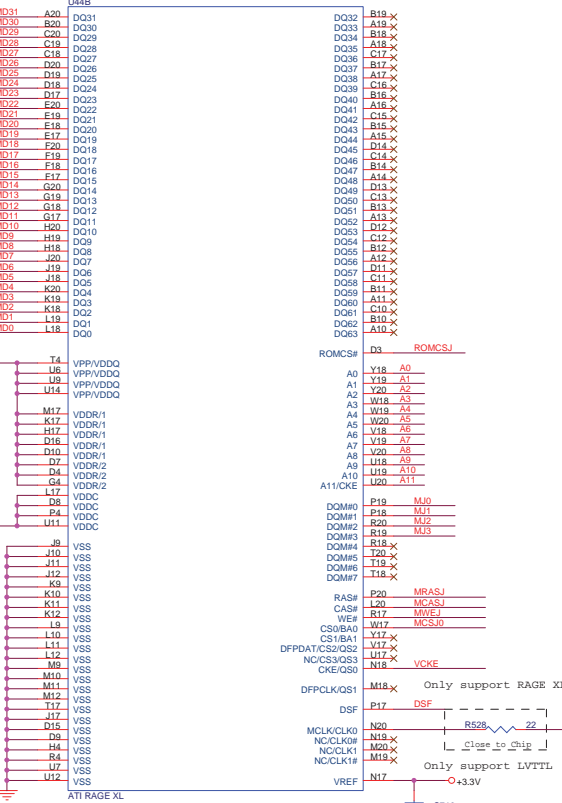
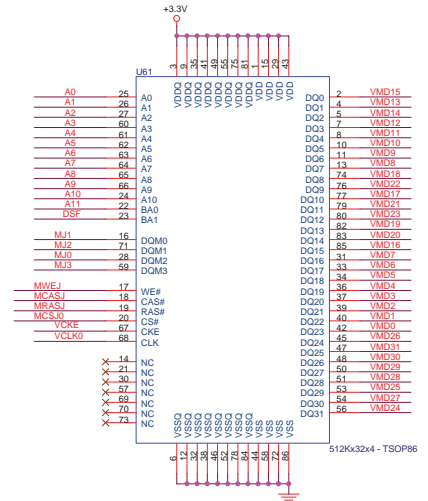
Date: Friday, March 25, 2005 Sheet: 36 of 44



Current provided by VDDC is 600 mA



8MBytes SDRAM (64Mbit, 512Kx32x4)



VMA8	
INT Enable	Open
INT Disable	Close

INTERRUPT always enable

Read BIOS straps	Close
Don't Read BIOS	Open

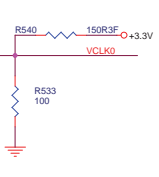
VMA7	
VGA Enable	Open
VGA Disable	Close

VGA always enable

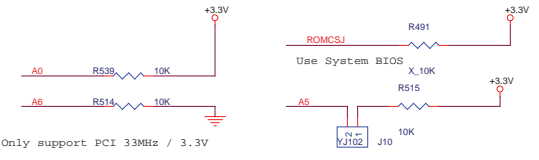
VDDR	I/O power for Memory & multimedia
VDDP	Power for PCI or AGP Interface
VDDC	Graphic controller power
AVDD	Analog DAC Power - 2.5 V
PVDD	Phase Lock Loop Power - 2.5 V

	VMA0	VMA6	PCI33MHz
	Bus Clock Select	Bus Type	PCI33MHz
PCI 33MHz / 3.3V	1	0	1
PCI 33MHz / 5V	1	1	1
PCI 66MHz	0	1	0
AGP 1/2X	0	0	0
AGP Test Mode	1	Don't care	0

Close to Chip



STRAPPING RESISTORS



Only support PCI 33MHz / 3.3V

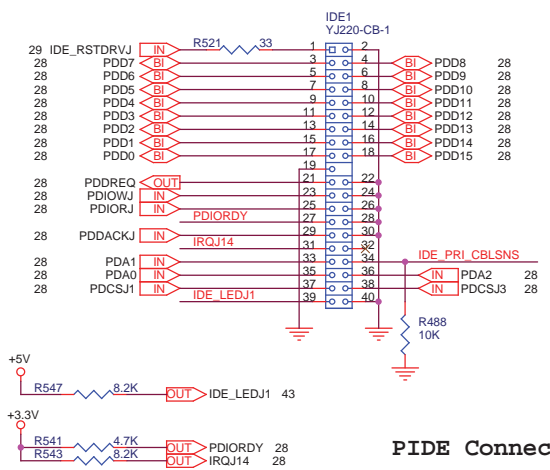
VMA5	
IDSEL Enable	Open
IDSEL Disable	Close

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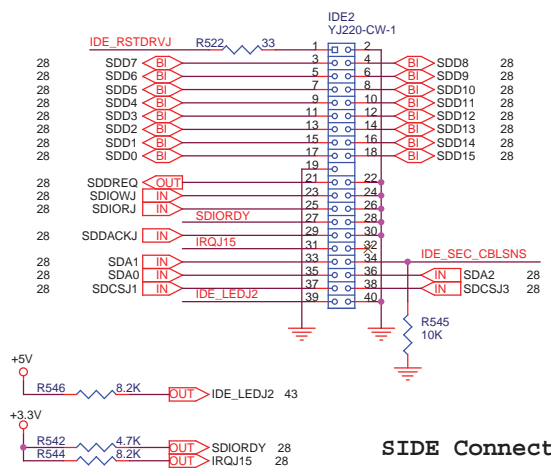
Title: **VGA B**

Size	Document Number	Rev
C	MS-9621	1.0

Date: Friday, March 25, 2005 Sheet 37 of 44

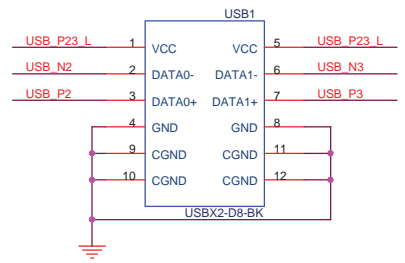
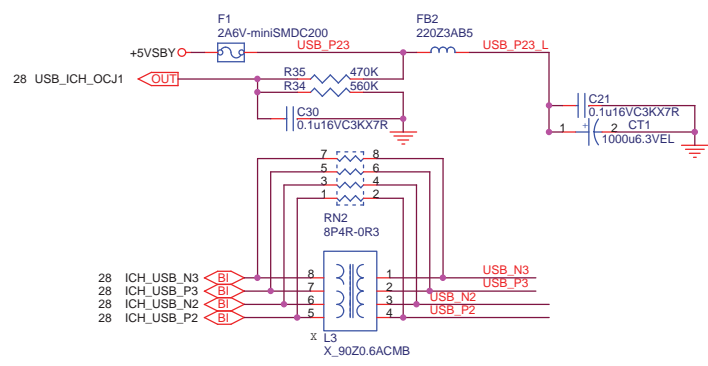
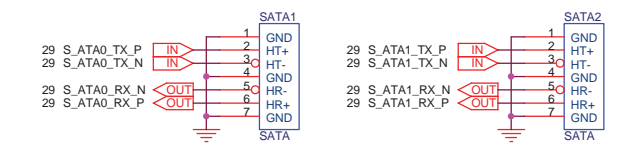


PIDE Connector

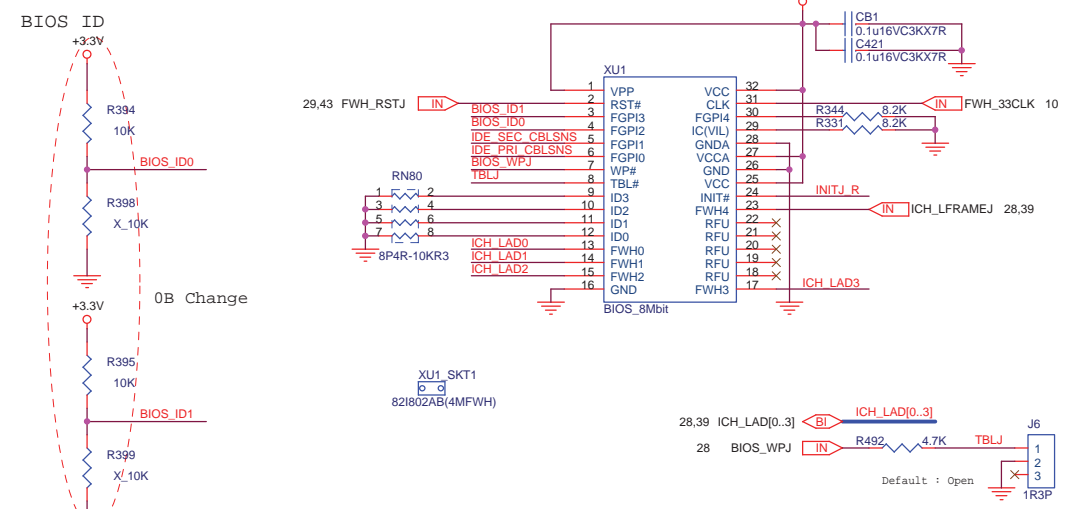


SIDE Connector

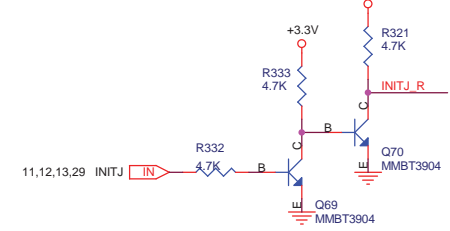
SATA



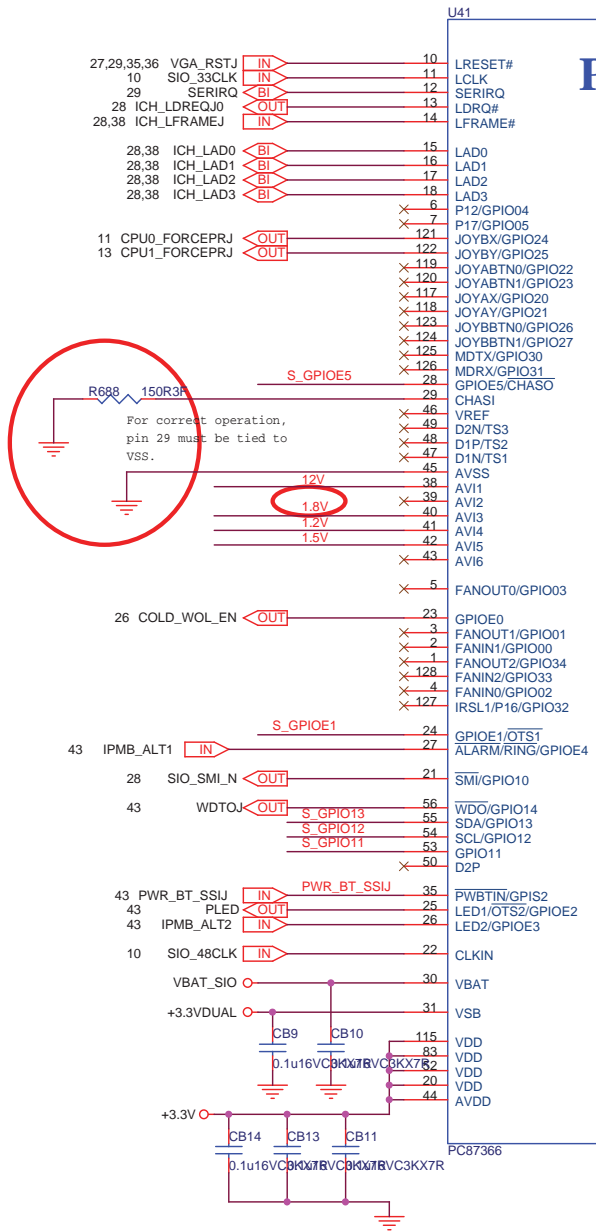
FWH



Voltage Trans

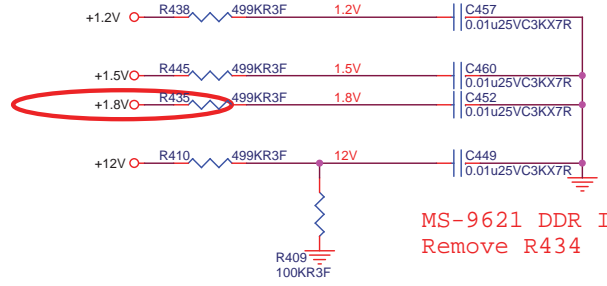
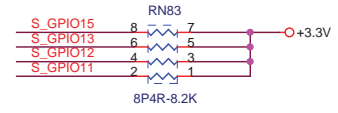
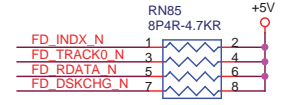
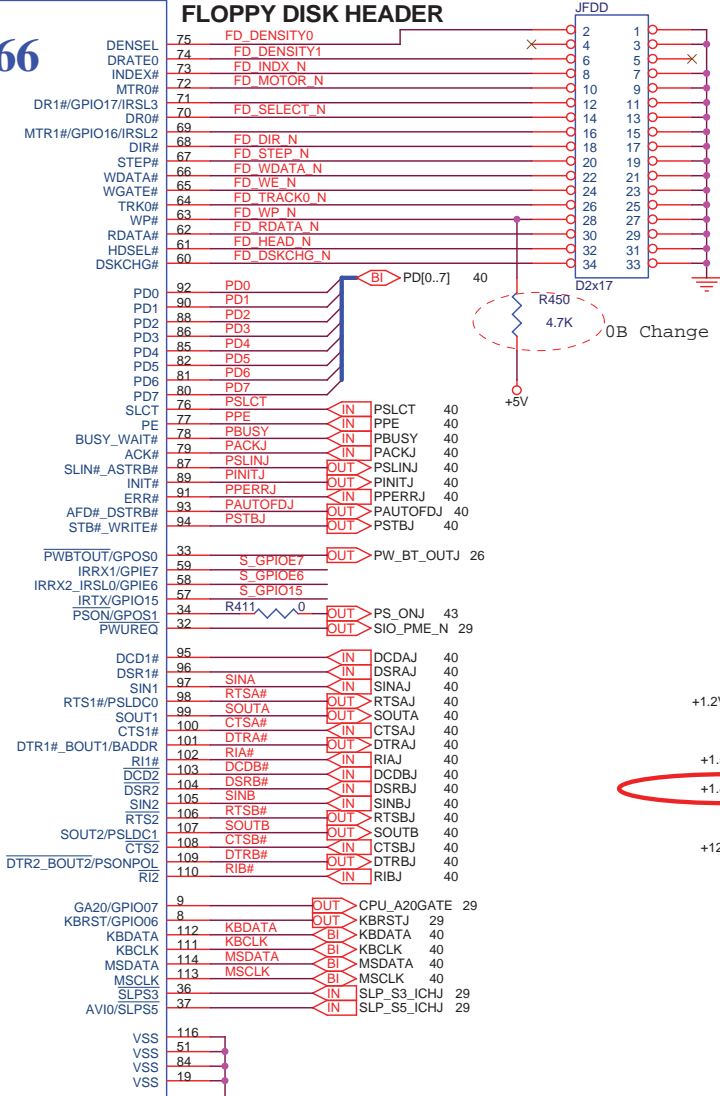


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Title IDE,SATA,FWH BIOS		
Size A3	Document Number MS-9621	Rev 1.0
Date: Friday, March 25, 2005	Sheet 38	of 44



PC87366

FLOPPY DISK HEADER



MS-9621 DDR II
 Remove R434

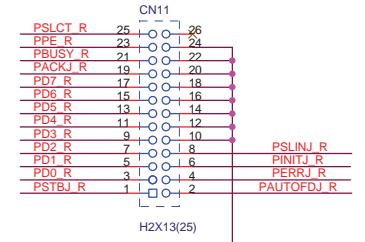
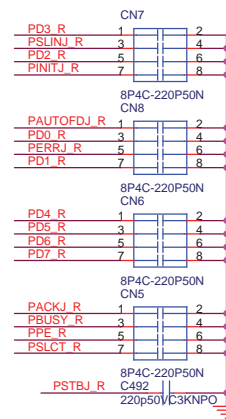
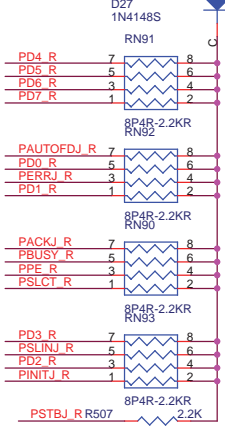
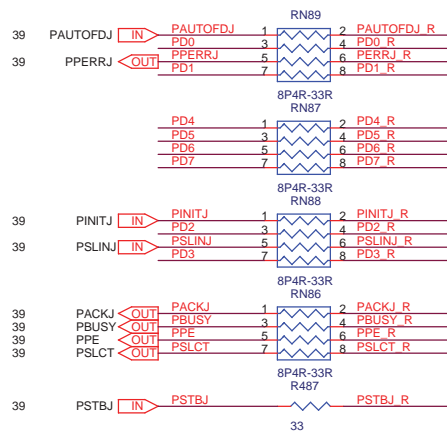
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Title: **SIO**

Size B: Document Number **MS-9621** Rev 1.0

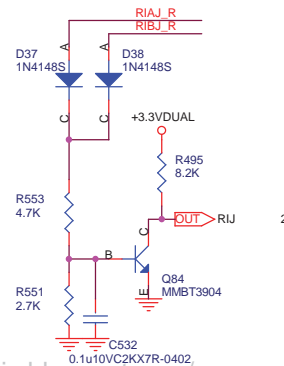
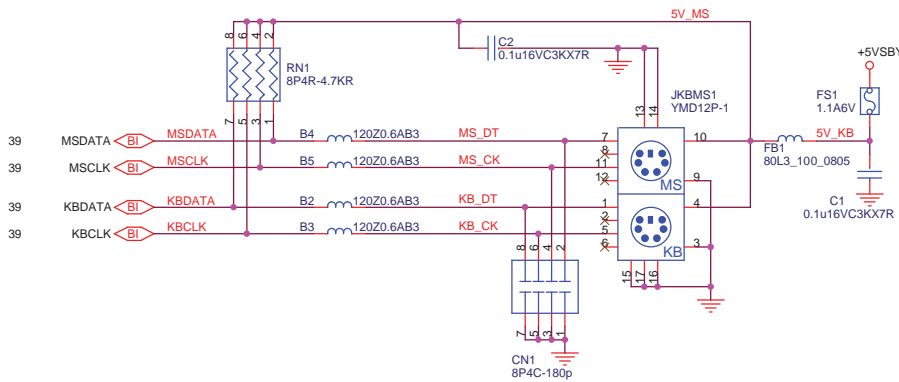
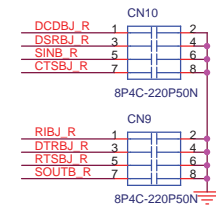
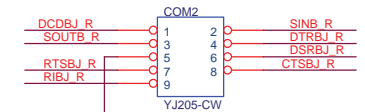
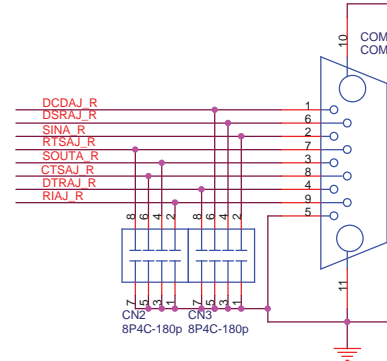
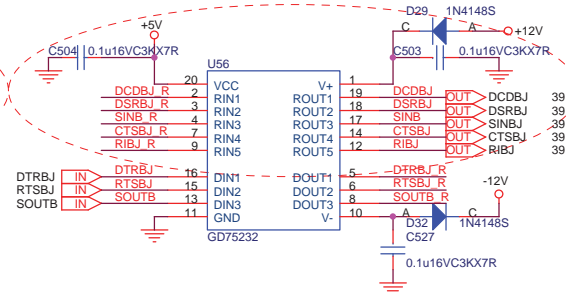
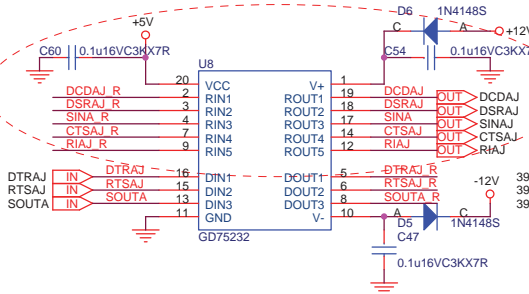
Date: Friday, March 25, 2005 Sheet 39 of 44

39 PD[0..7] BI PD[0..7]



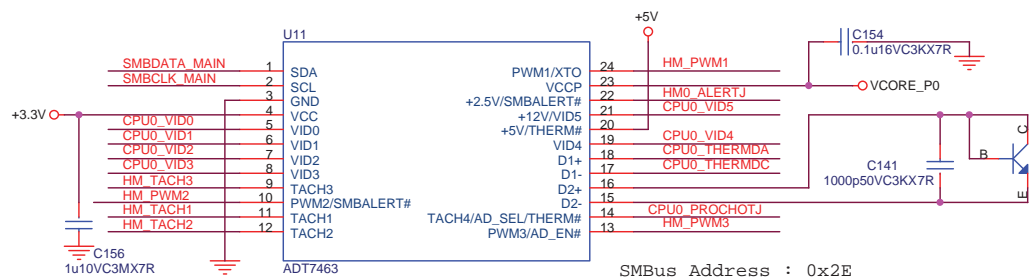
0B Change

0B Change

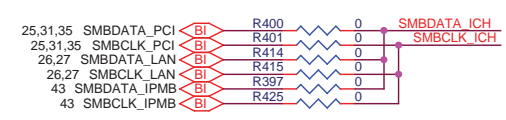
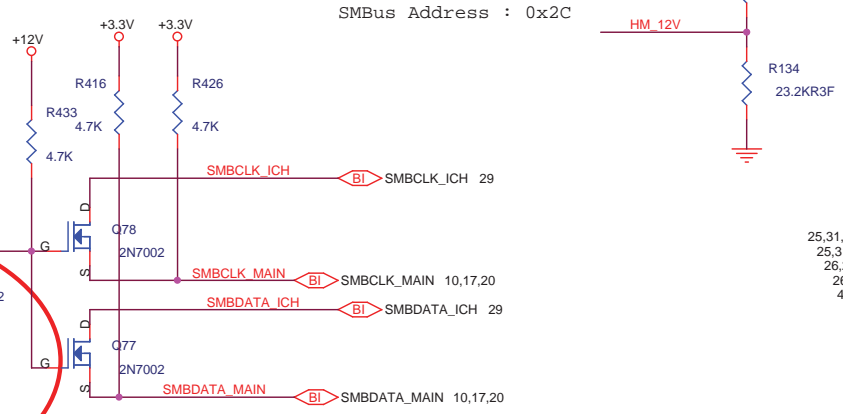
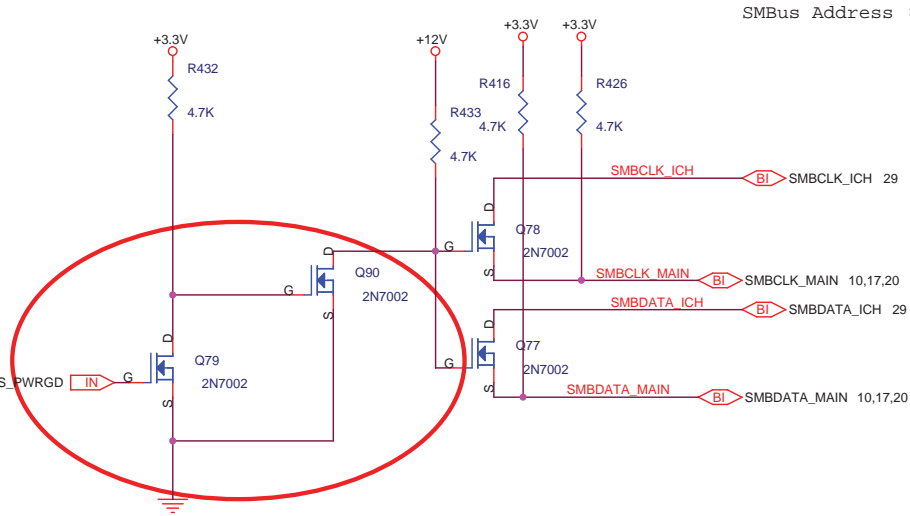
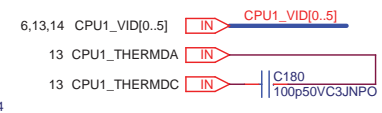
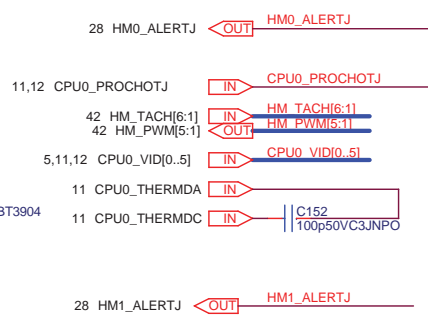
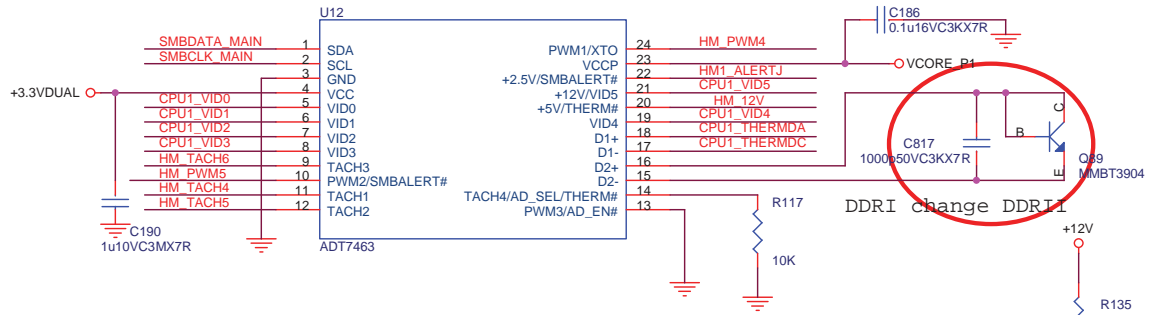


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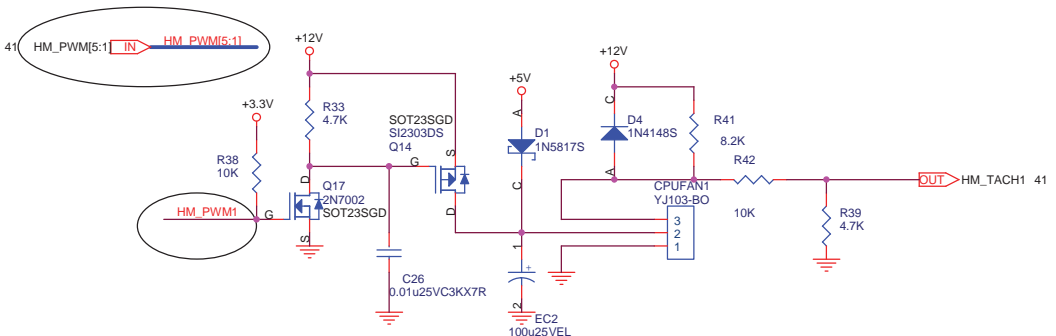
Title		PRINTER PORT & COM & PS2	
Size	Document Number	MS-9621	Rev
A3			1.0
Date:	Friday, March 25, 2005	Sheet	40 of 44



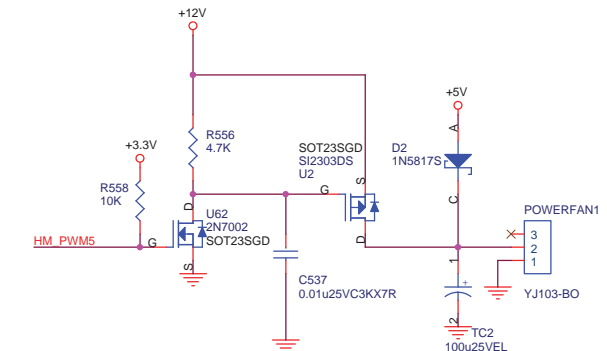
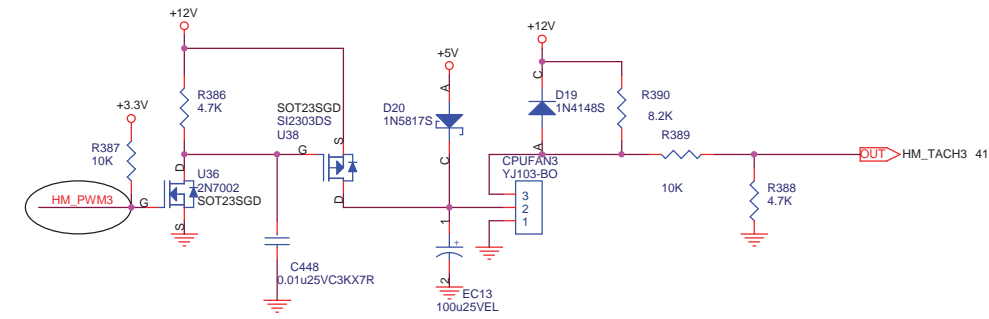
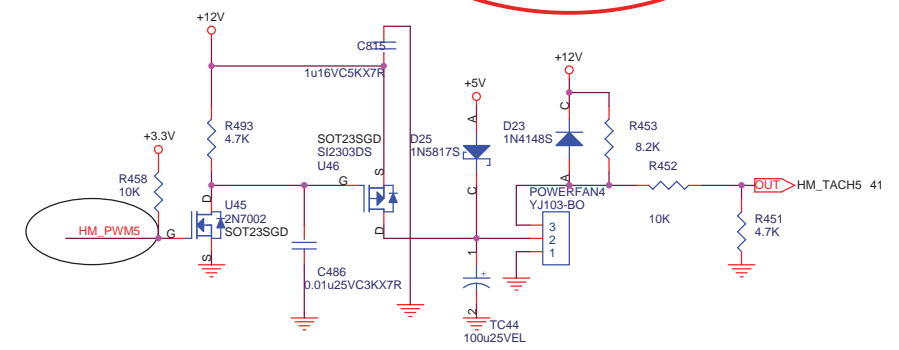
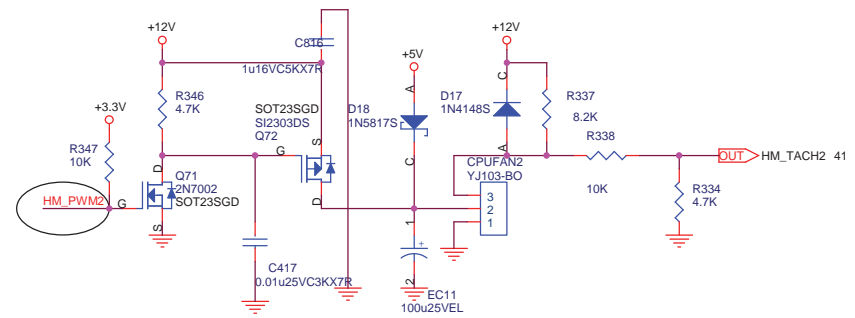
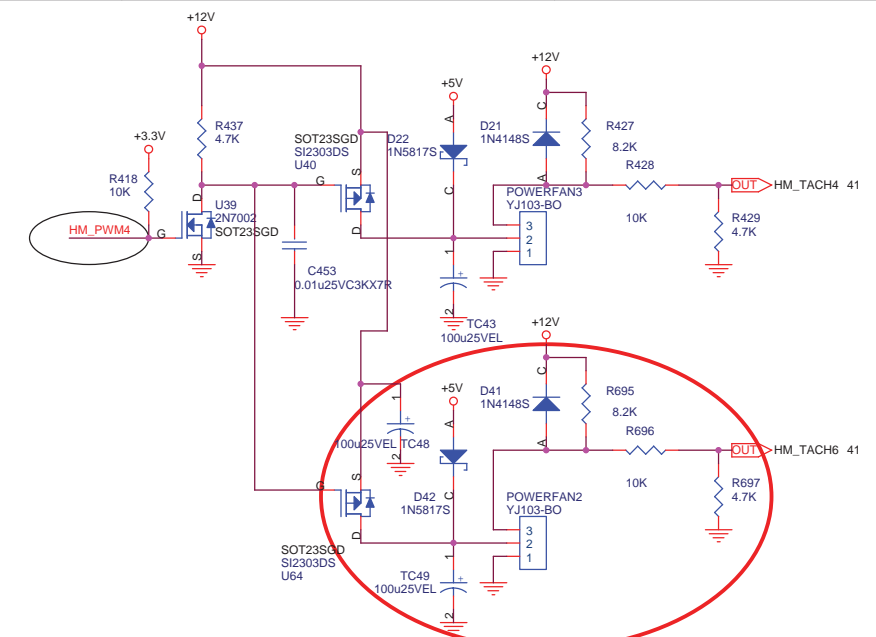
When a temperature exceed its THERM limit, All Fan will turn on 100%



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Title HM		
Size B	Document Number MS-9621	Rev 1.0
Date: Friday, March 25, 2005	Sheet 41	of 44



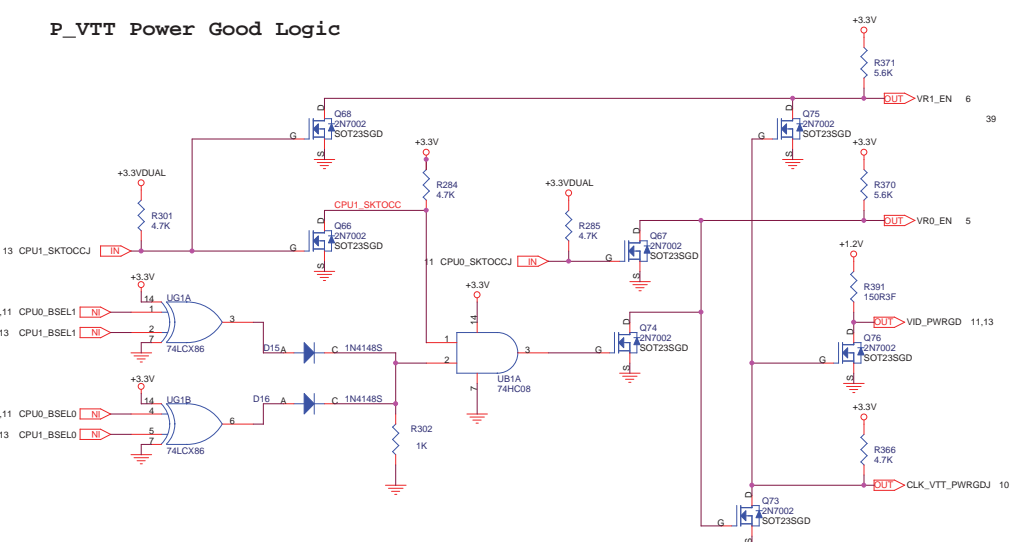
Gate voltage increase slowly
 --> Channel turn on slowly Drain voltage do not droop instantly



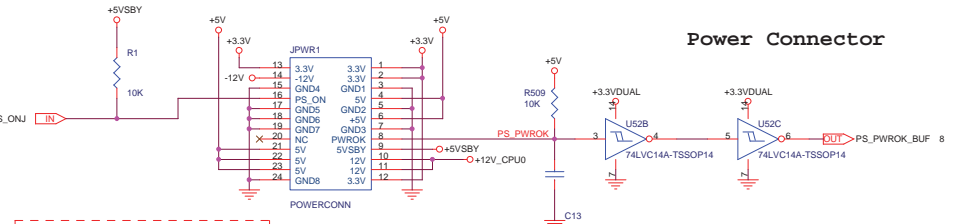
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Title			
FAN Connector Circuit			
Size	Document Number	Rev	
A3		MS-9621	1.0
Date:	Friday, March 25, 2005	Sheet	42 of 44

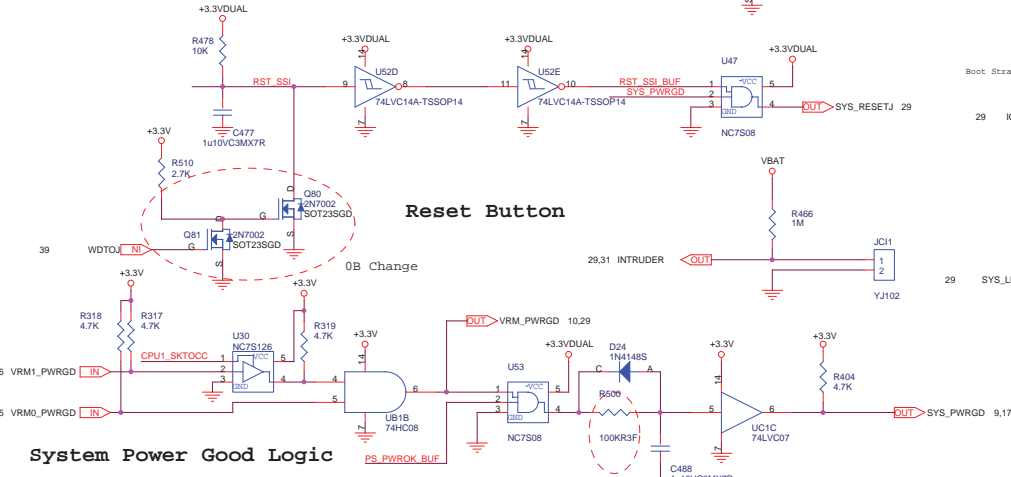
P_VTT Power Good Logic



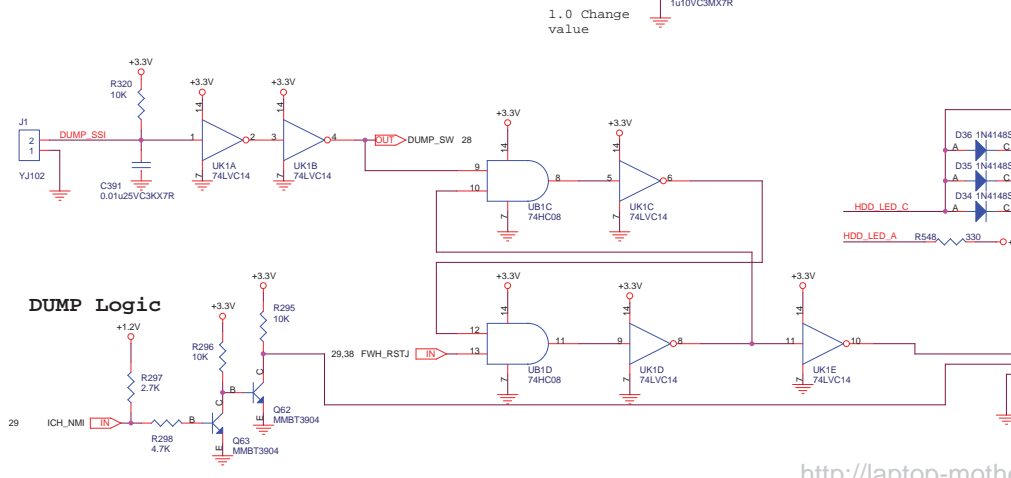
Power Connector



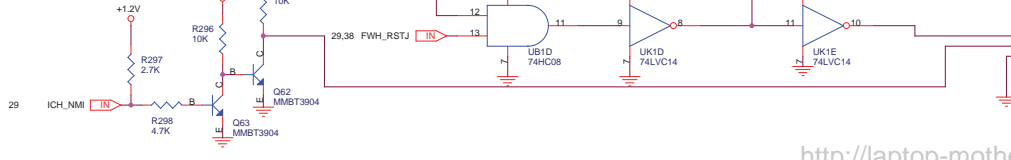
Reset Button



System Power Good Logic



DUMP Logic



Boot Strap : Disable ICH
TOD timer

29 ICH_SPKR IN

29 SYS_LED IN

29.31 INTRUDER OUT

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

29 SYS_LED IN

29 J102

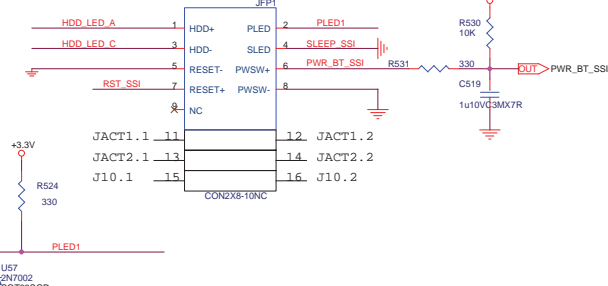
29 SYS_LED IN

29 J102

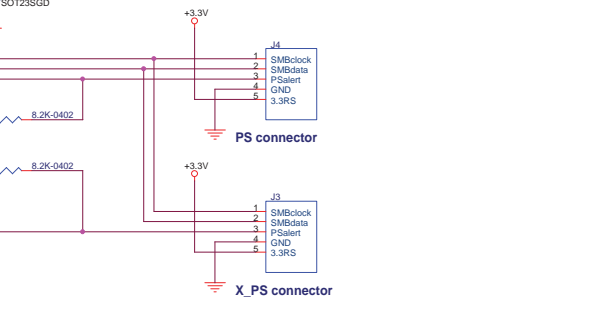
29 SYS_LED IN

29 J102

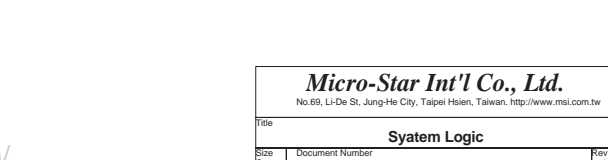
MSI Front Panel

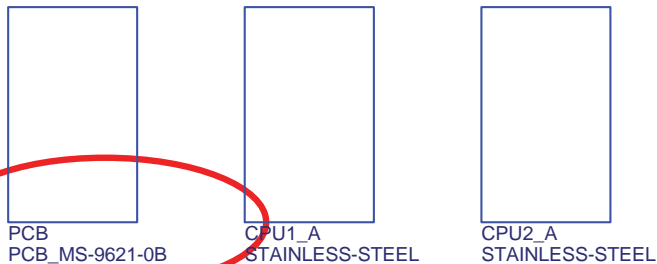
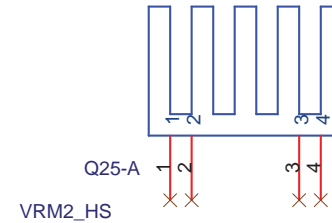
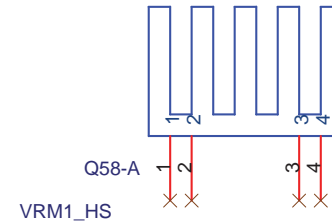
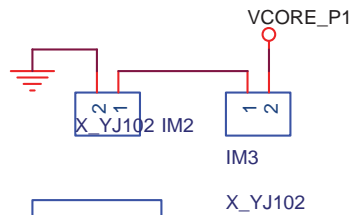
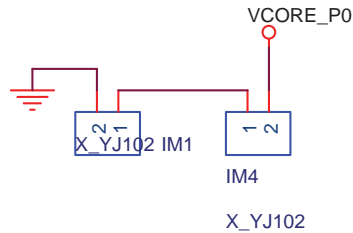
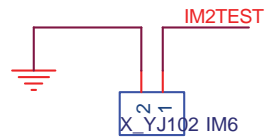
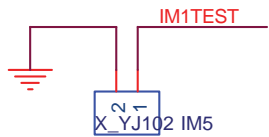
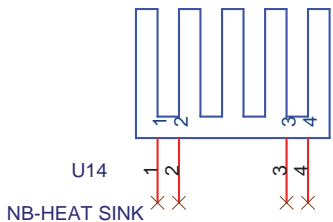
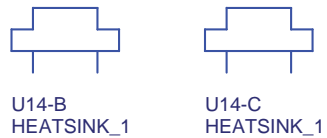
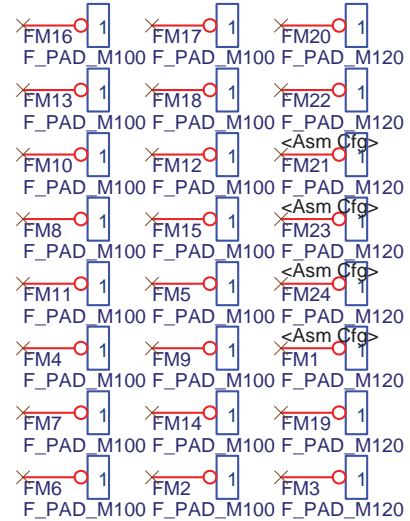
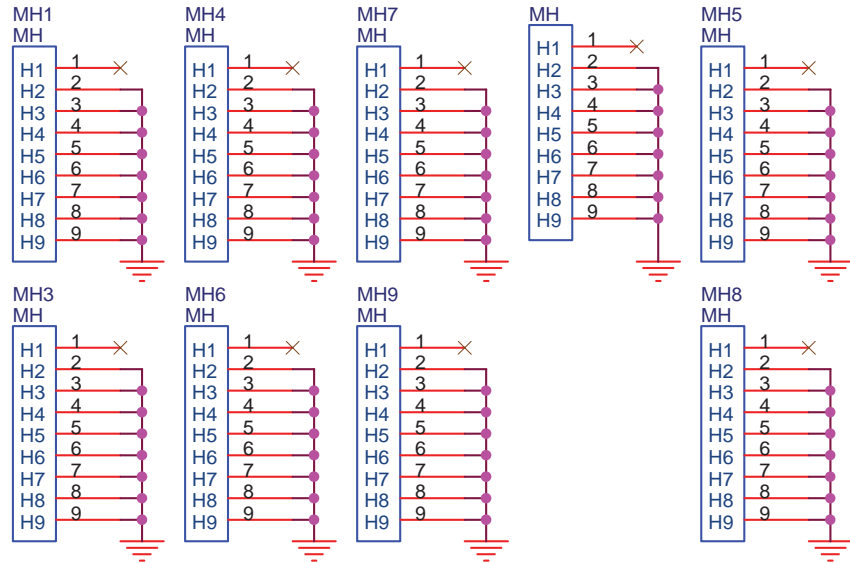


PS connector



X_PS connector





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Title: **Layout Component**

Size A	Document Number MS-9621	Rev 2.0
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Date: Friday, March 25, 2005