

Cover Sheet	1
Block Diagram	2
Intel Dothan CPU - Host	3
Intel Dothan CPU - Power & GND	4-5
Intel Alviso - Host & Memory Signals	6-8
Intel Alviso - Power & GND	9-10
Intel ICH6 - PCI & DMI & CPU & IRQ	11
Intel ICH6 - LPC & ATA & USB & GPIO & POWER	12-13
Clock -ICS954310& FWH	14
LPC I/O - W83627DHF	15
LAN1-Intel 82573L	16
LAN2-Intel 82573L/82562GZ	17
DDR2 DIMM 1 & 2	18
DDR2 Termination Resistors	19
PCI -Express x1 2Port	20
PCI -Express x8 1Port	21
PCI Slot	22
AC'97 Codec-ALC662 & ALC888	23
NMISwitch/PCIRST/JUMPER	24
SATA&IDEConnectors/TPM	25
USB CONNECTORS	26
ATX ,Front Panel&VGA Conn	27
System Power	28
CPU Power	29
FAN Connectors	30
POST LED/Status LED	31
GPIO SETTING	32

MS-9623(ROHS)

Version 1.2
07/31/2007

CPU:

Intel Pentium-M Processor/Celeron-M Processor

System Chipset:

Intel 915GME - GMCH (North Bridge)

Intel ICH6M(South Bridge)

On Board Chipset:

Clock Generator - ICS954310

LAN1 -- Intel 82573

LAN2 -- Intel 82573L/82562GZ

LPC Super I/O -- W83627DHF

BIOS -- FWH EEPROM

Main Memory:

DDR2 * 2 (Max 2GB)

Expansion Slots:


PCI EXPRESS X1 SLOT * 2

PCI EXPRESS X8 SLOT * 1

PCI2.3 SLOT * 2

Manual Part	33
System Clock Block Diagram	34
Power Delivery Block Diagram	35
Power on sequence	36
Board Map	37
History	38

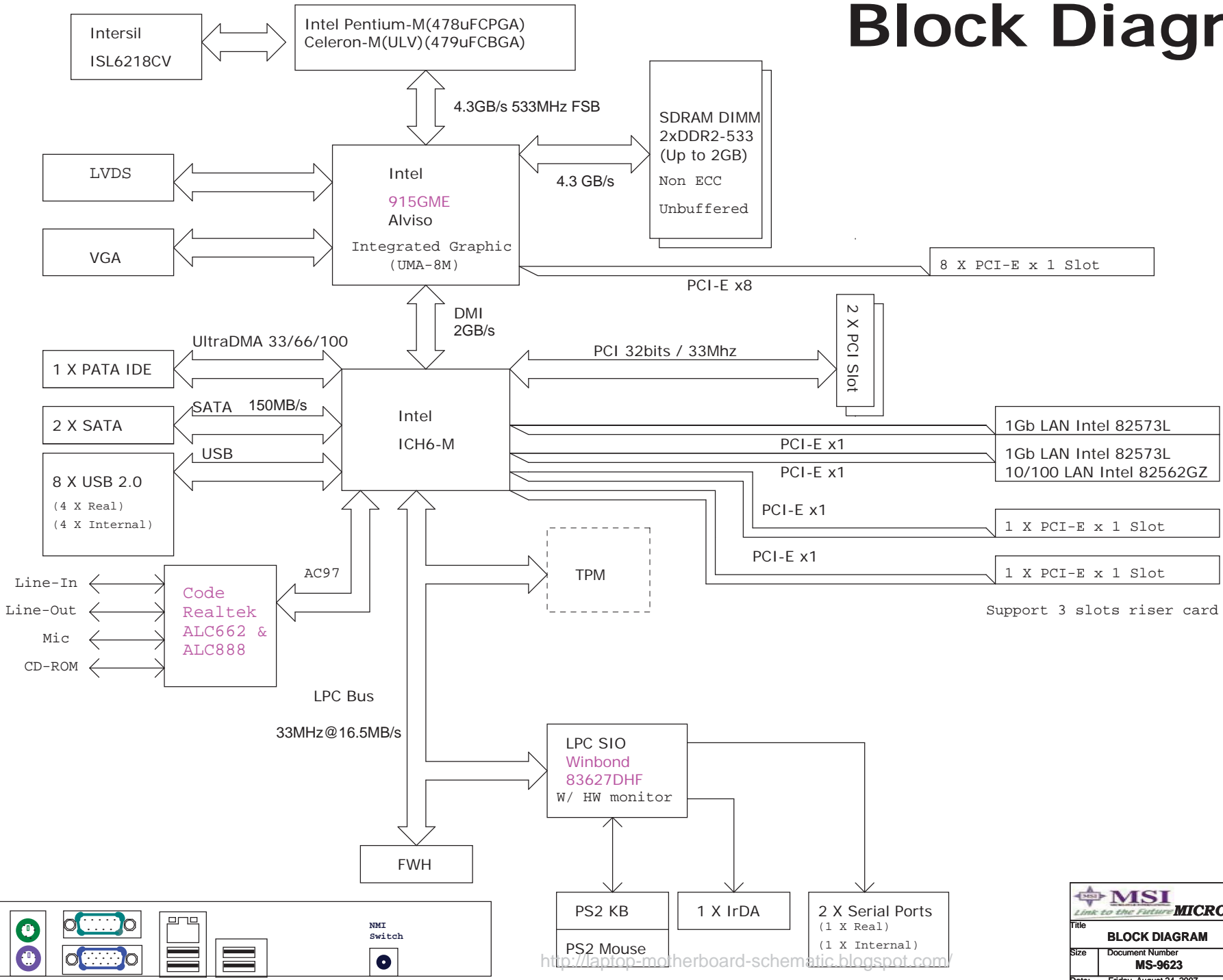
HW:MIA.CHENG #8871

 **MSI**
Link to the Future
MICRO-START INT'L CO.,LTD.


Title: **COVER SHEET**

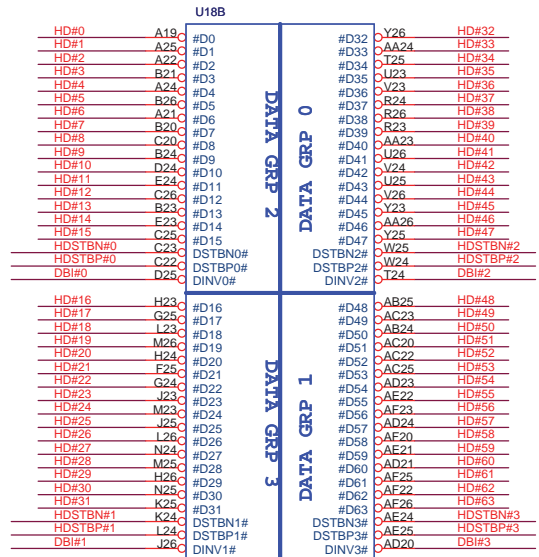
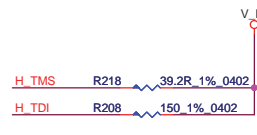
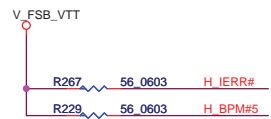
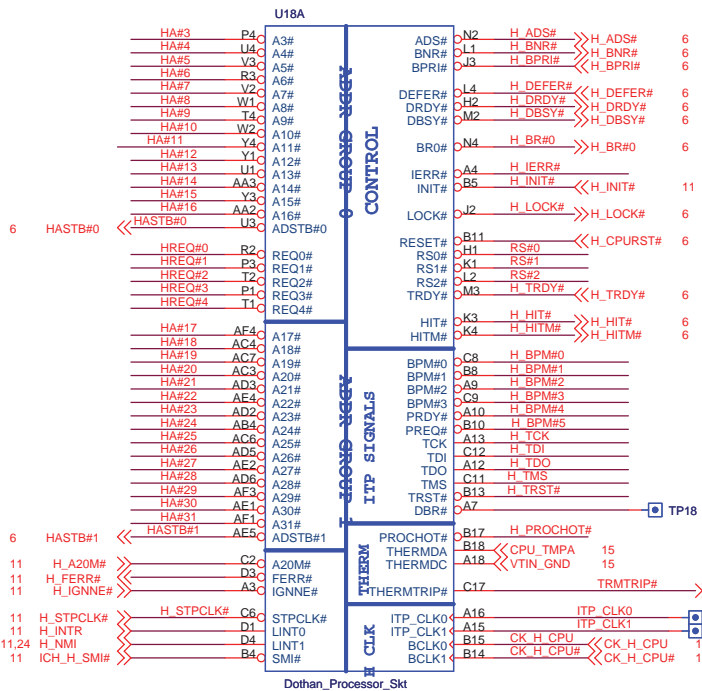
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 1 of 38

Block Diagram

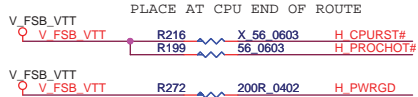
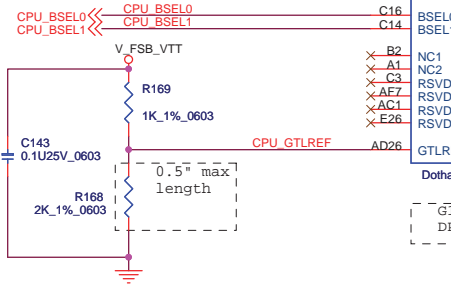


<http://laptop-motherboard-schematic.blogspot.com/>

 MICRO-START INT'L CO.,LTD.		
Title: BLOCK DIAGRAM		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 2 of 38



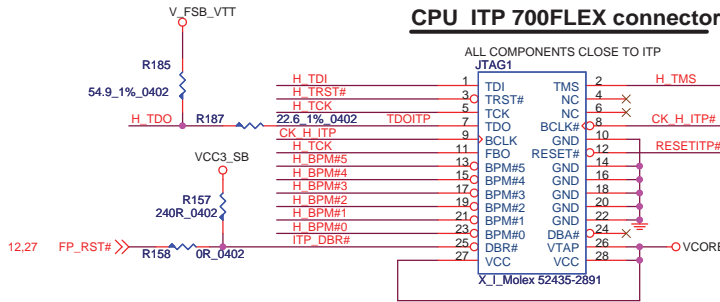
0.5" max length
 25 MIL AWAY FROM HIGH SPEED SIGNAL



Celeron:A09-1020105-I06
 Dothan:N12-4790010-L06



CPU ITP 700FLEX connector



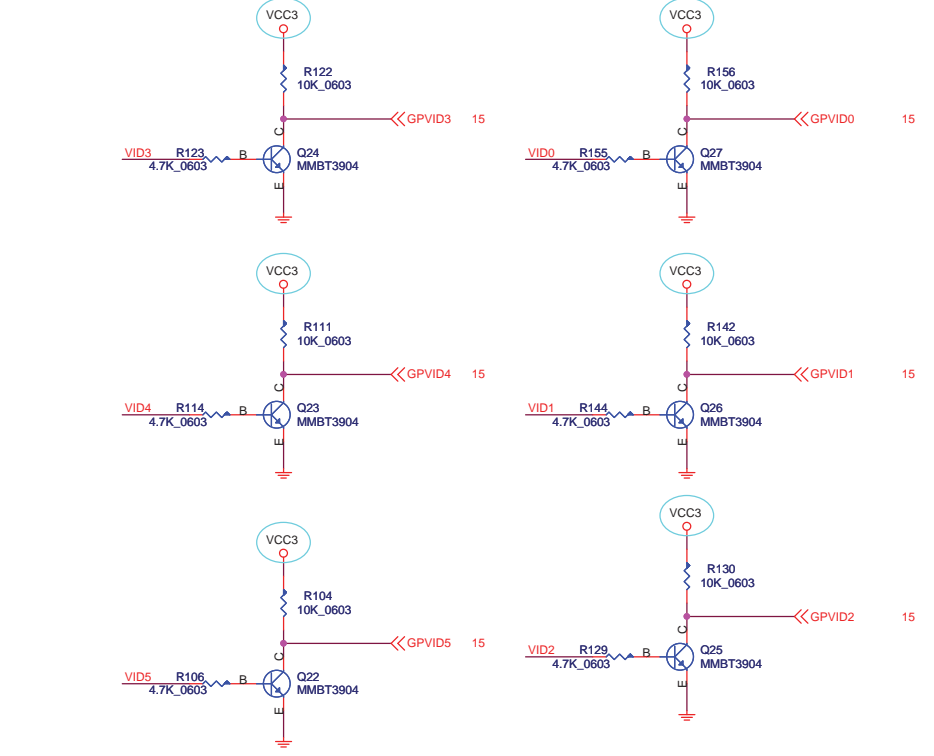
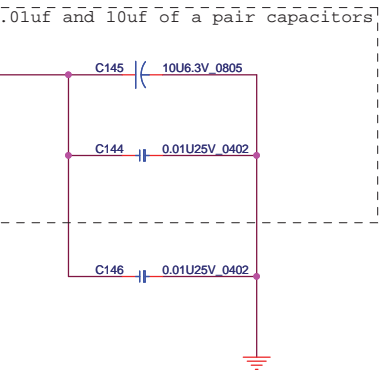
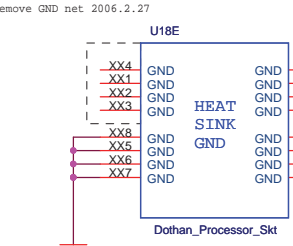
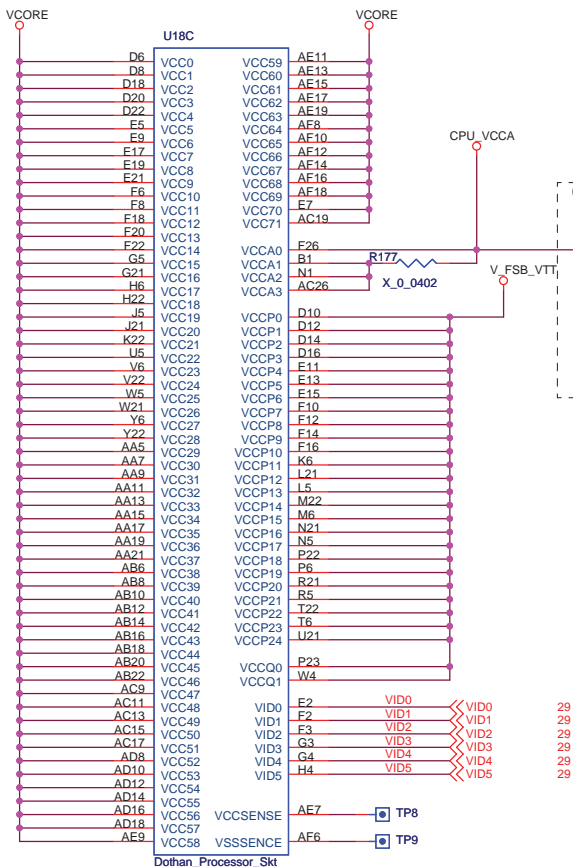
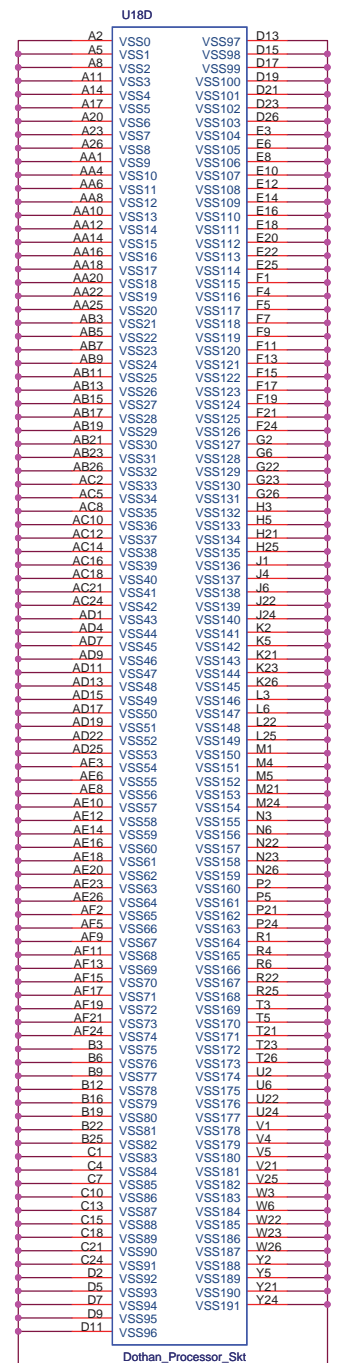
BSEL1	BSEL0	FREQ
L	H	100 MHz
L	L	133 MHz
H	L	REV
H	H	REV

MSI
 Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **Dothan (Host Bus)**

Size: Document Number **MS-9623** Rev **1.2**

Date: Friday, August 24, 2007 Sheet 3 of 38



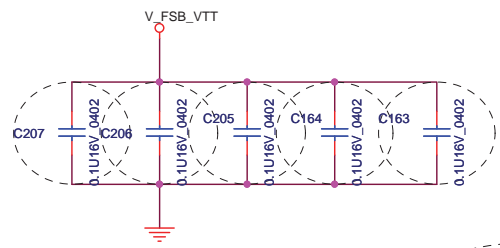
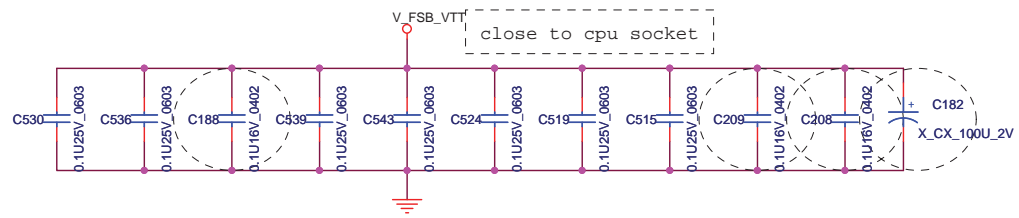
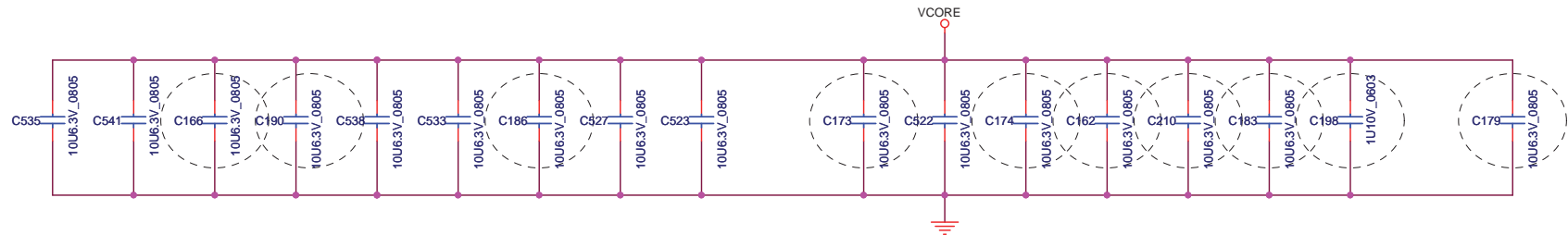
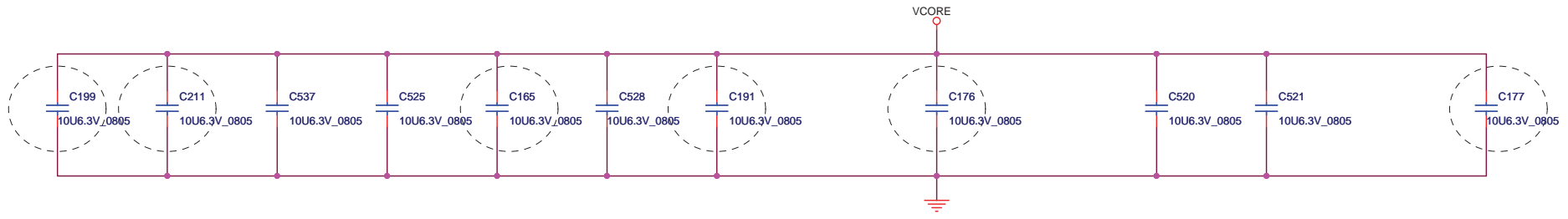
Remove GND net: 2006.2.27

<http://laptop-motherboard-schematic.blogspot.com/>

MSI
Link to the Future
MICRO-START INT'L CO., LTD.

Title: **Dothan (Power/GND)/ITP**

Size	Document Number MS-9623	Rev 1.2
Date:	Friday, August 24, 2007	Sheet 4 of 38

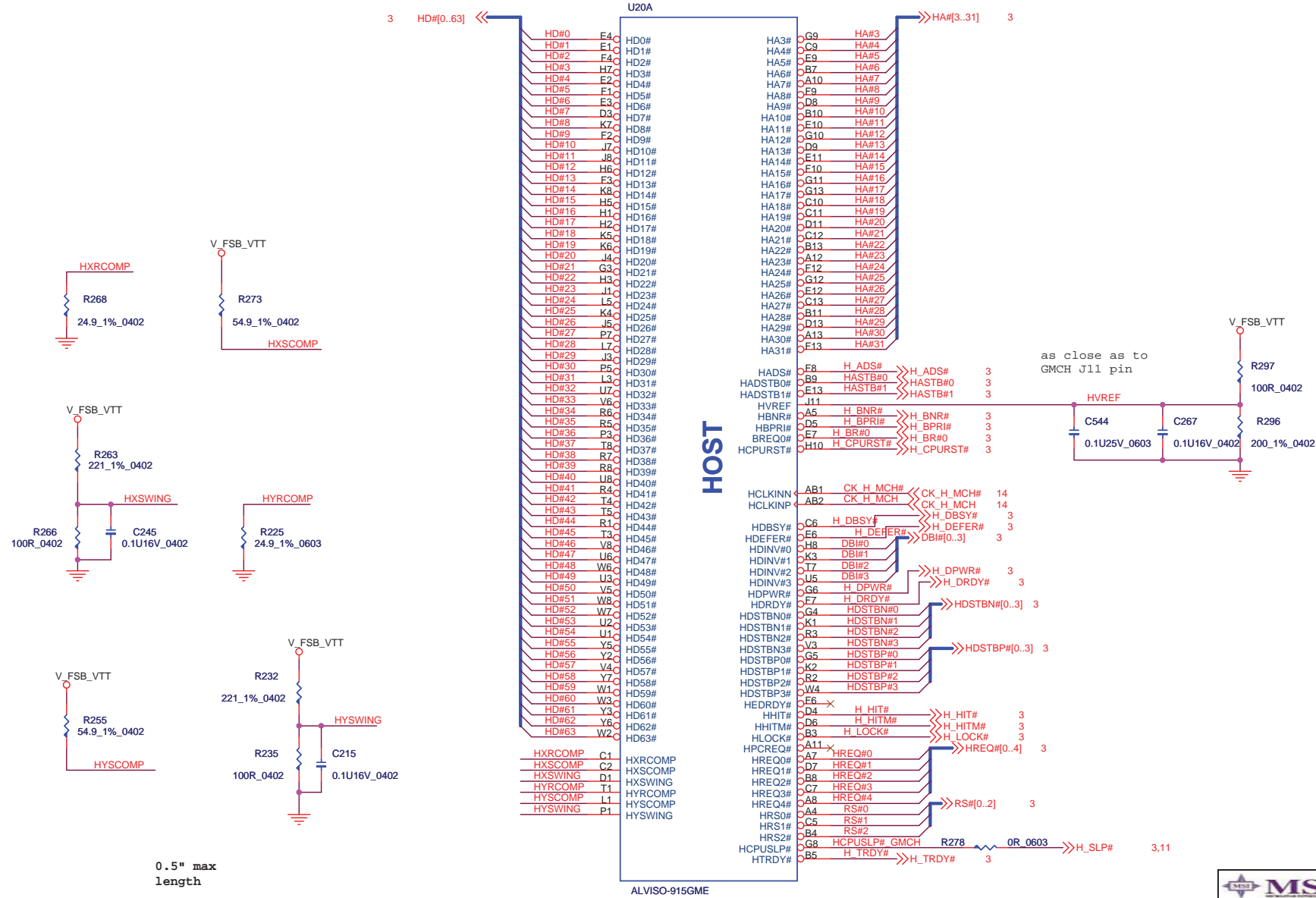


Without on
Celeron-M

MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **Dothan (By Pass)**

Size	Document Number MS-9623	Rev 1.2
Date:	Friday, August 24, 2007	Sheet 5 of 38

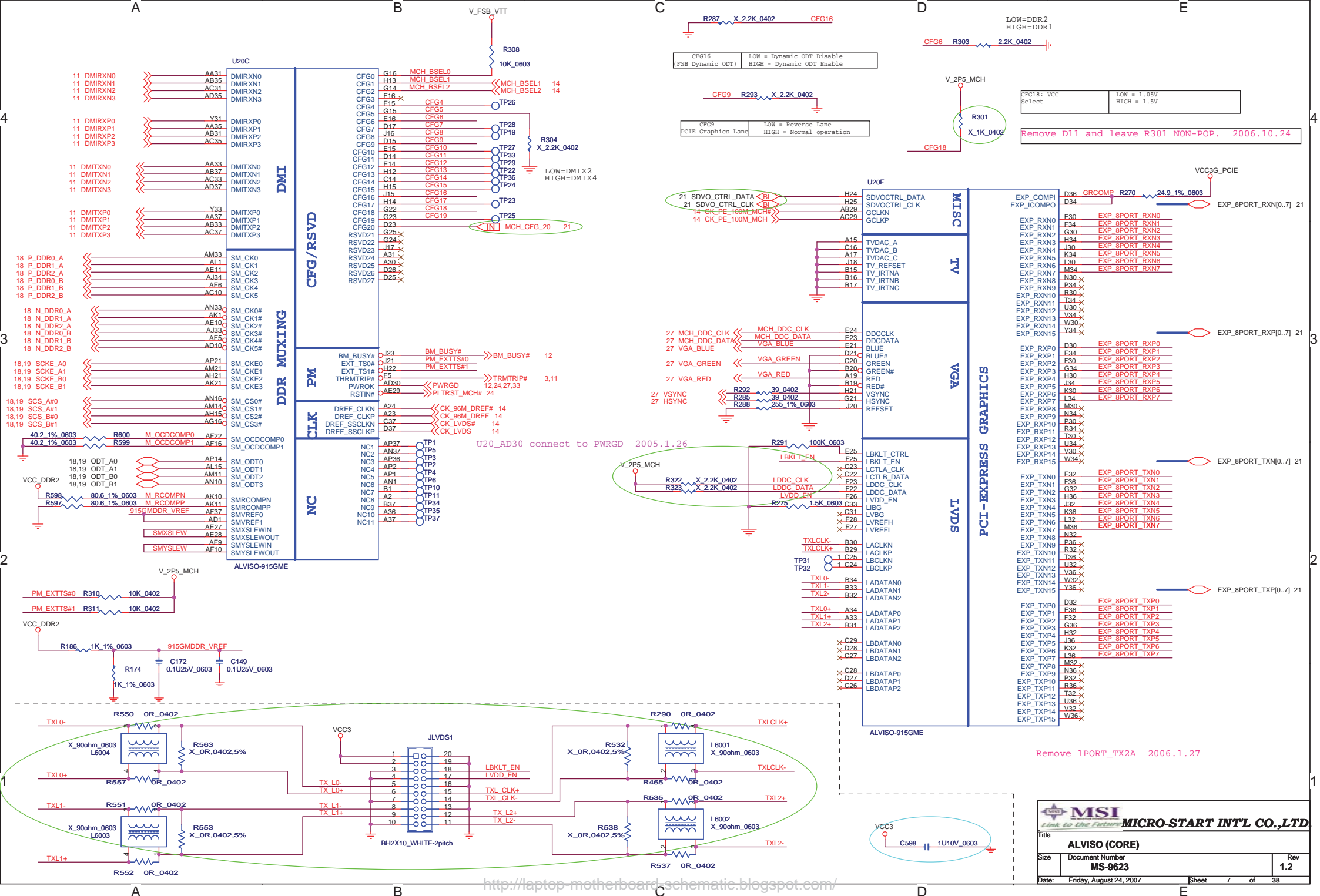


0.5" max length

MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **ALVISO (HOST)**

Size	Document Number MS-9623	Rev 1.2
Date:	Friday, August 24, 2007	Sheet 6 of 38



CFG16 LOW = Dynamic ODT Disable
 [FSB Dynamic ODT] HIGH = Dynamic ODT Enable

CFG9 LOW = Reverse Lane
 [PCI Express Lane] HIGH = Normal operation

LOW=DDR2
 HIGH=DDR1

CFG18: VCC Select LOW = 1.05V HIGH = 1.5V

Remove D11 and leave R301 NON-POP. 2006.10.24

VCC3G_PCIE

U20 AD30 connect to PWRGD 2005.1.26

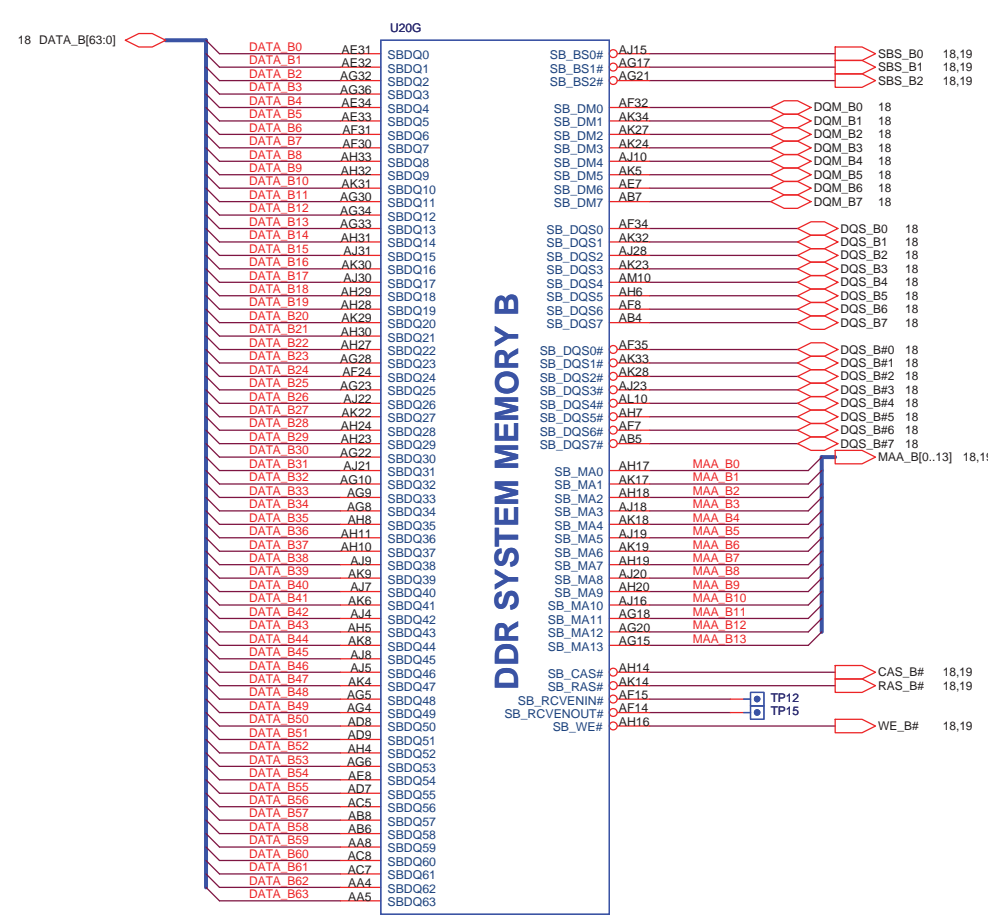
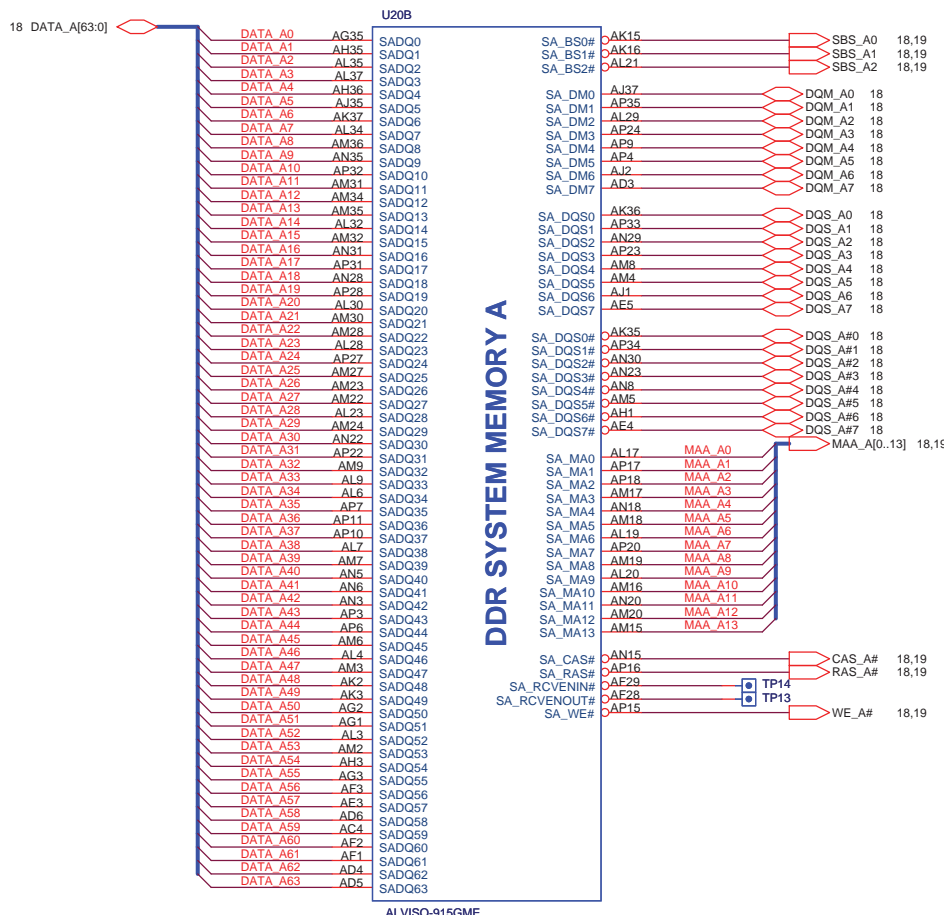
Remove 1PORT_TX2A 2006.1.27

MSI
 Link to the Future
MICRO-START INT'L CO.,LTD

Title: **ALVISO (CORE)**

Size: Document Number **MS-9623** Rev **1.2**

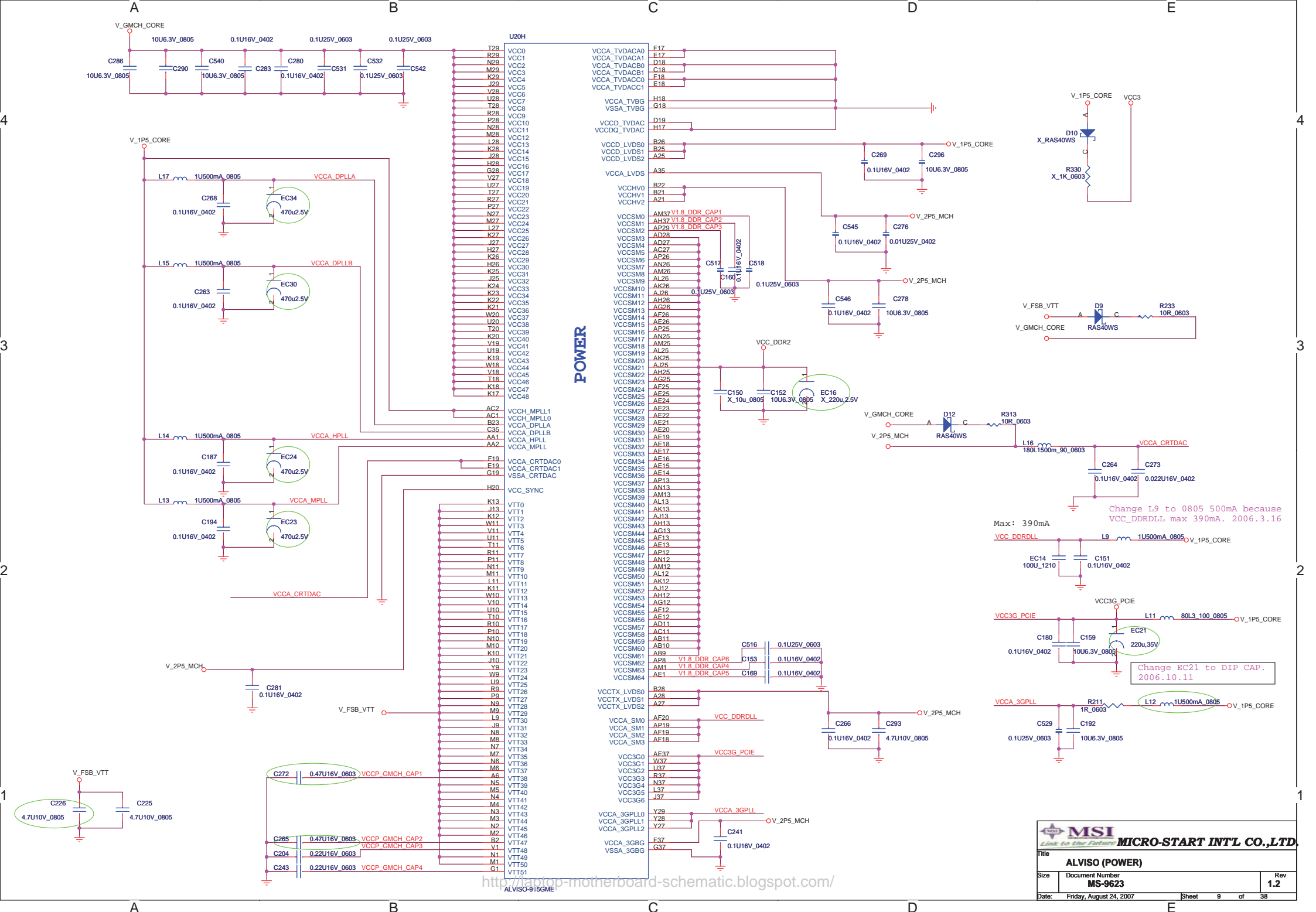
Date: Friday, August 24, 2007 Sheet 7 of 38



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

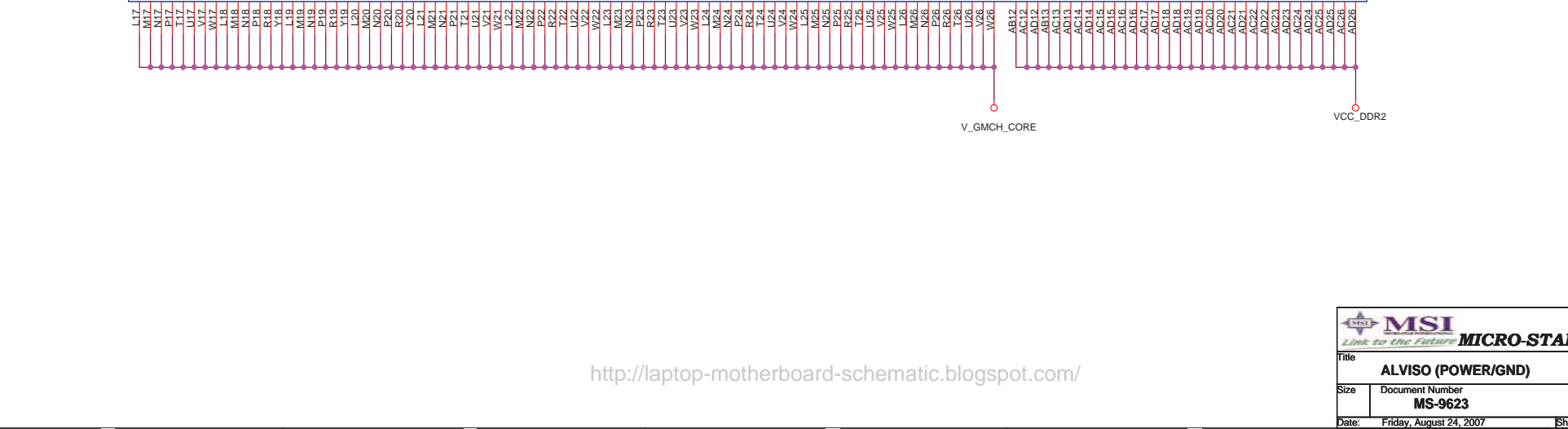
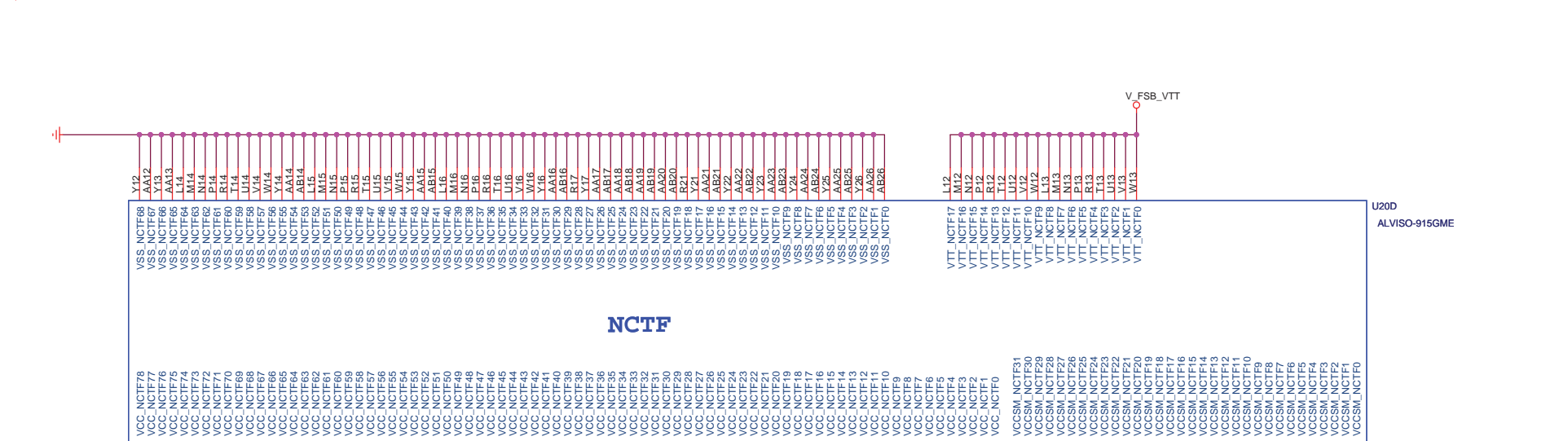
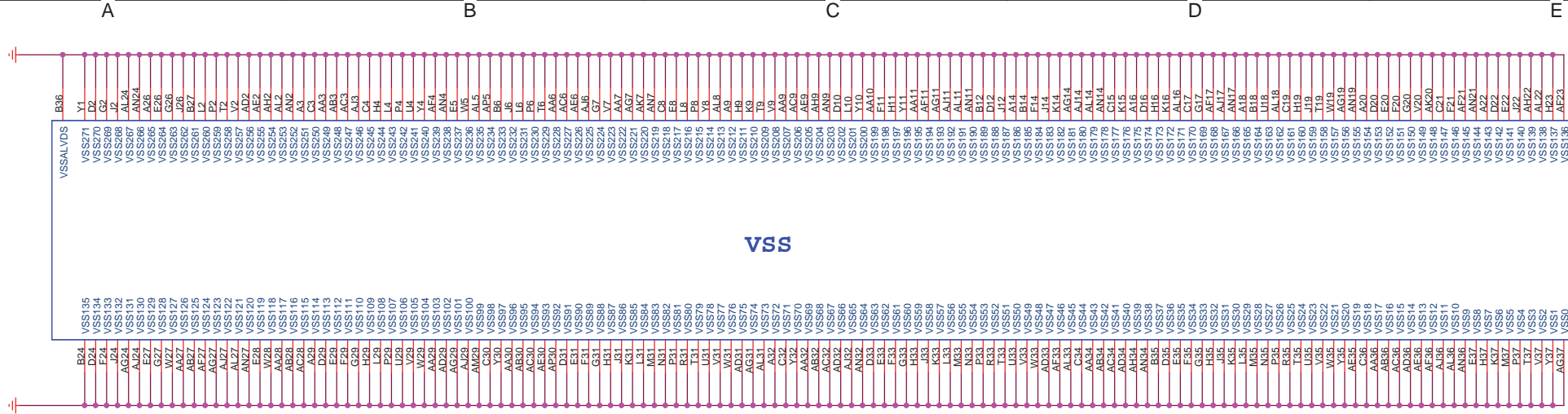
Title: **ALVISO (MEMORY)**

Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 8 of 38




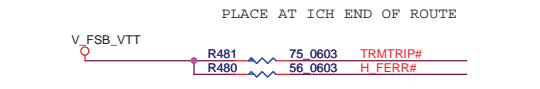
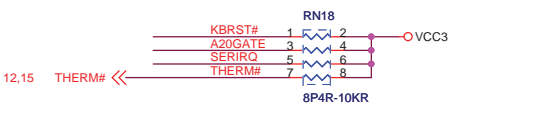
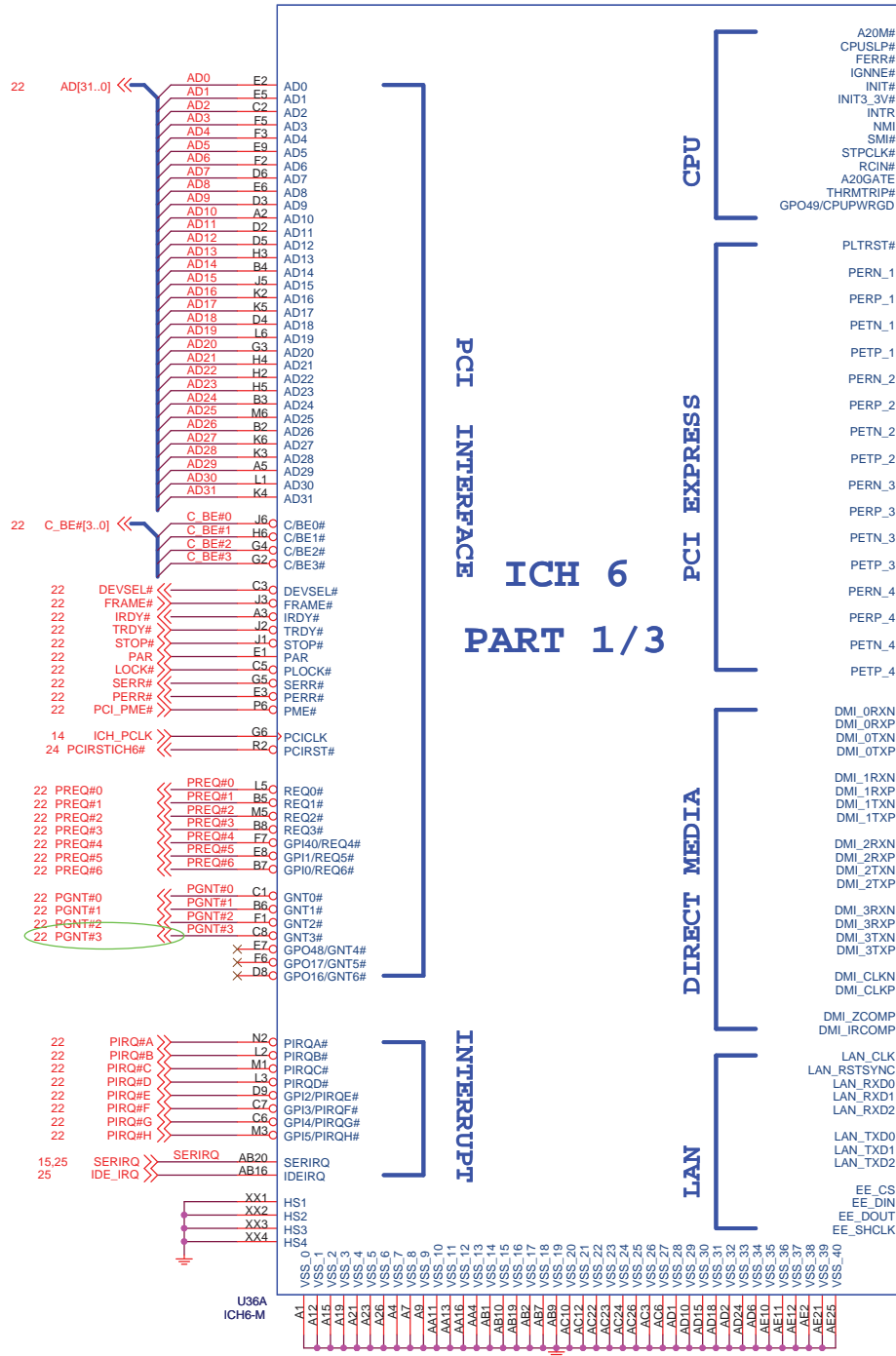
<http://antip-motherboard-schematic.blogspot.com/>

MSI Link to the Future		
MICRO-START INTL CO., LTD.		
ALVISO (POWER)		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 9 of 38

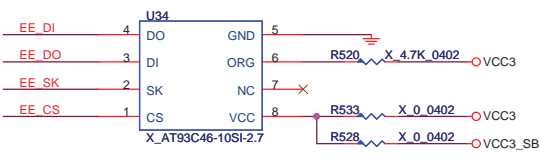


<http://laptop-motherboard-schematic.blogspot.com/>

 MICRO-START INT'L CO.,LTD.		
Title		
ALVISO (POWER/GND)		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 10 of 38



DMI Interface
Trace width 5 mils & 7 mils space.
GMCH breakout space 5 mils, length < 250 mils
Length matching < 5 mils
Trace length 2" to 11"



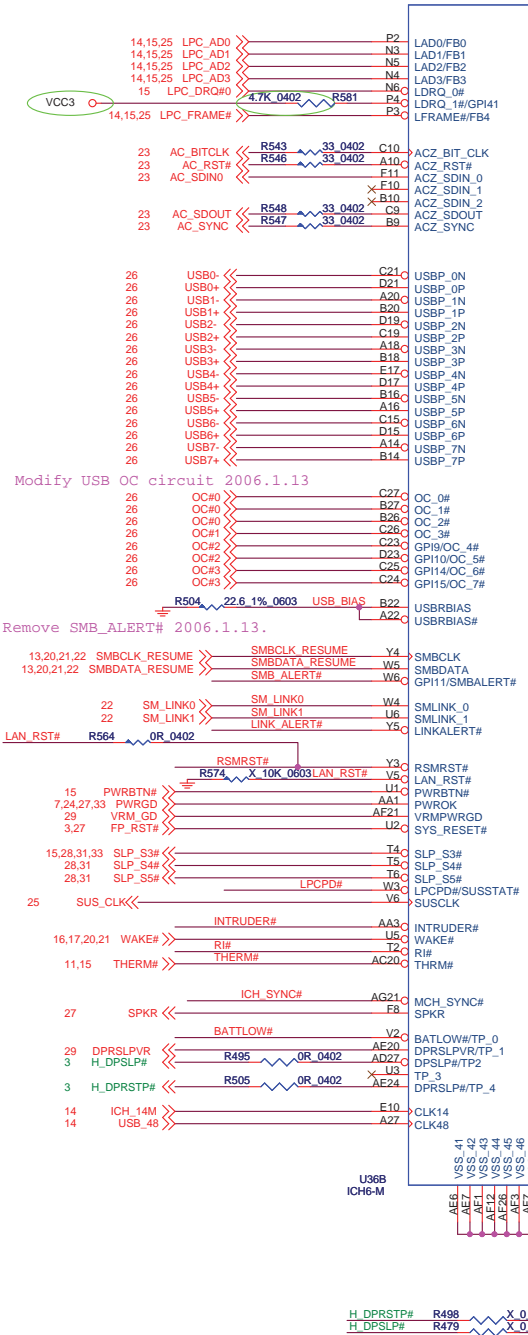
MSI
Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: **Intel ICH6M - PCI & DMI & CPU & IRQ**

Size	Document Number	Rev
	MS-9623	1.2

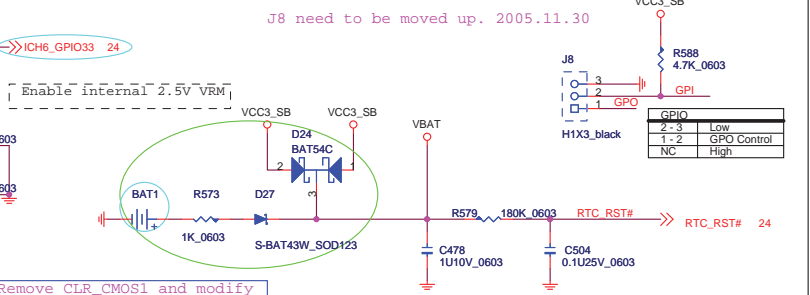
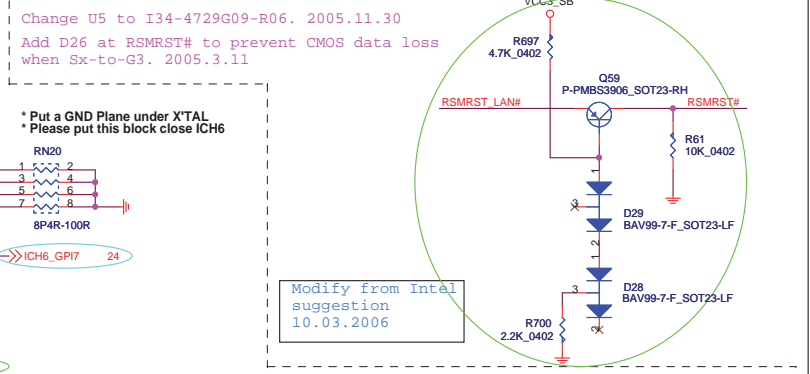
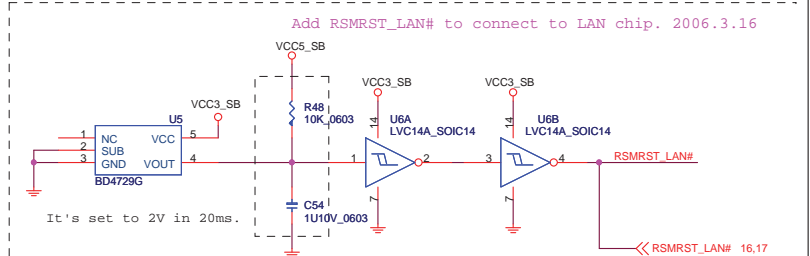
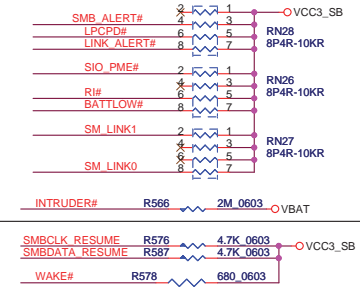
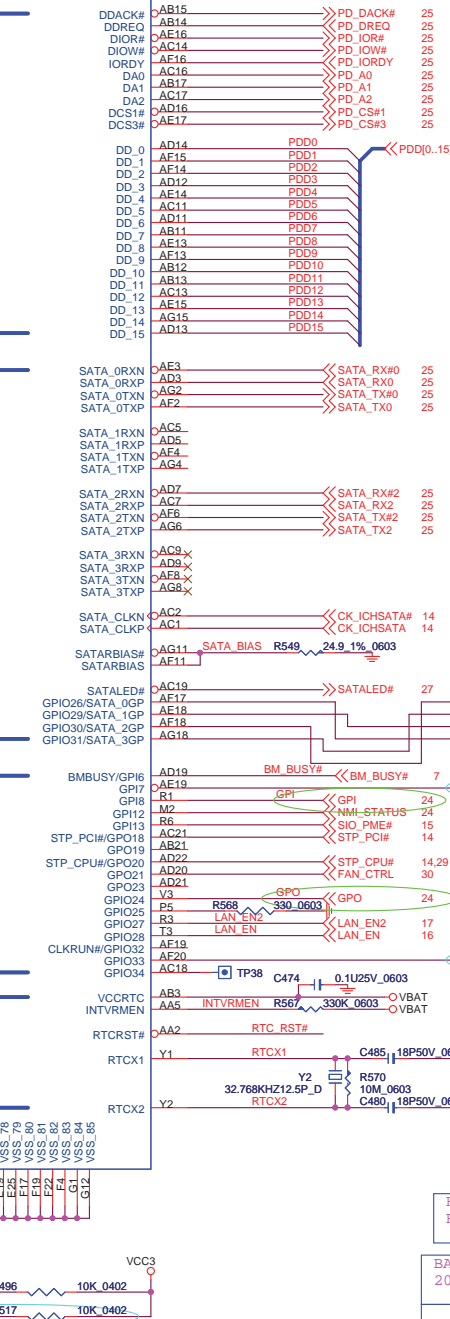
Date: Friday, August 24, 2007 Sheet 11 of 38

Remove SMB_ALERT# from RN28 pin4 2005.11.30
Remove R565 2005.1.26
Connect SMB_ALERT# from RN28 pin4 2006.3.11



ICH 6 PART 2/3

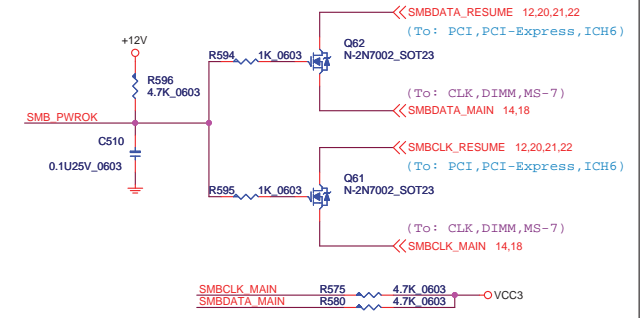
LPC
AC-LINK
USB
SM BUS
POWER MGMT
MISC
P-ATA
S-ATA
GPIO
RTC



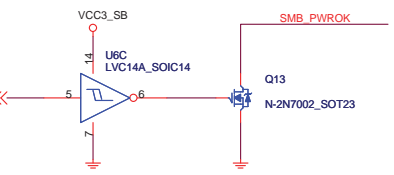
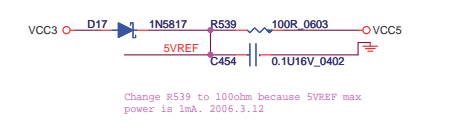
Remove CLR_CMOS1 and modify RTC_RST# circuit 2005.11.30
BAT1 change from CR2032 to CR2450. 2006.09.29
BAT54C x1=> BAT54Cx1 + BAT43x1 10.01.2006

MICRO-START INT'L CO.,LTD.		
Intel ICH6M - LPC & ATA & USB & GPIO		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 12 of 38

SM BUS ISOLATION



5VREF Sequencing Circuit



**ICH 6
PART 3/3**

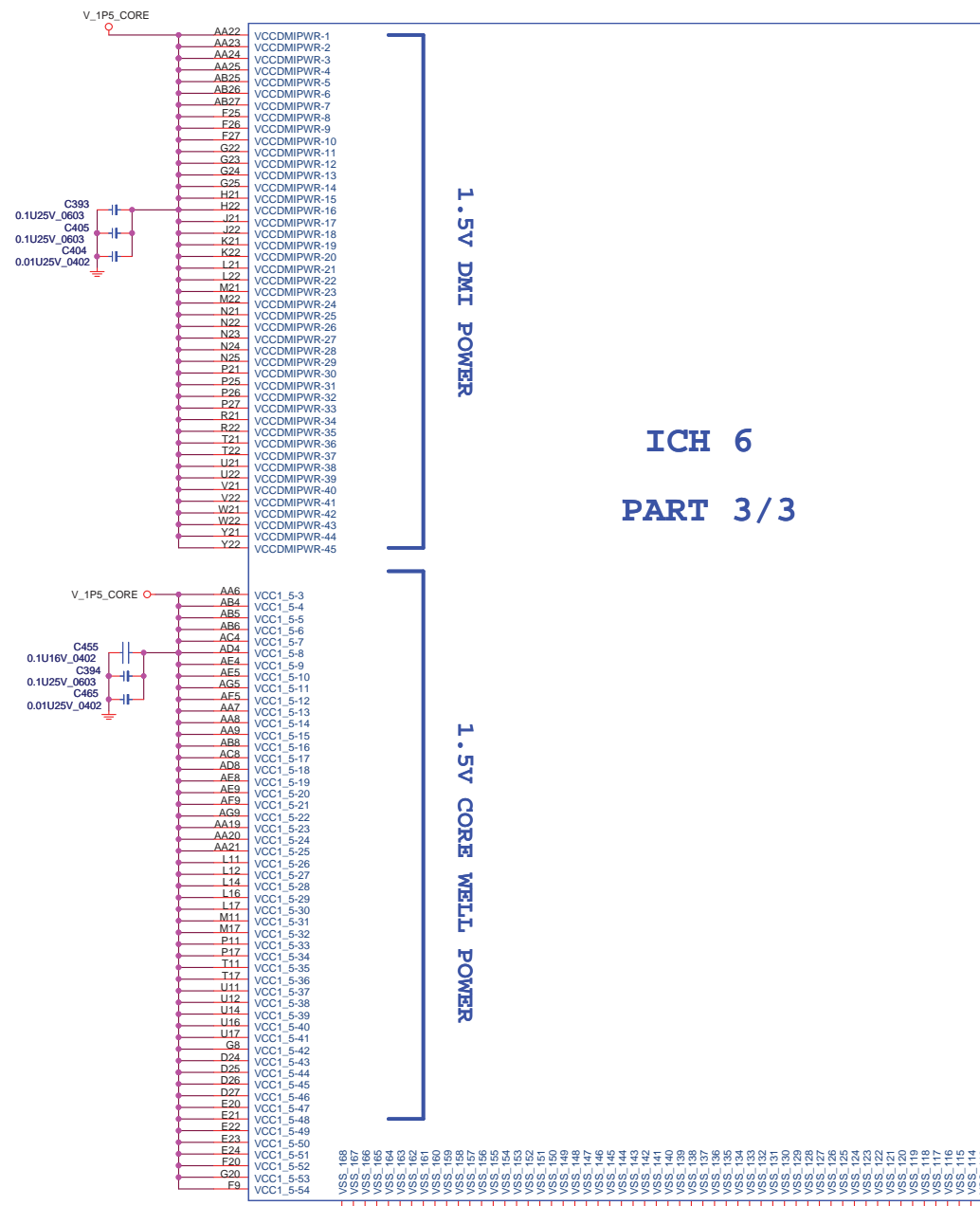
1.5V DMI POWER

1.5V CORE WELL POWER

S0 POWER

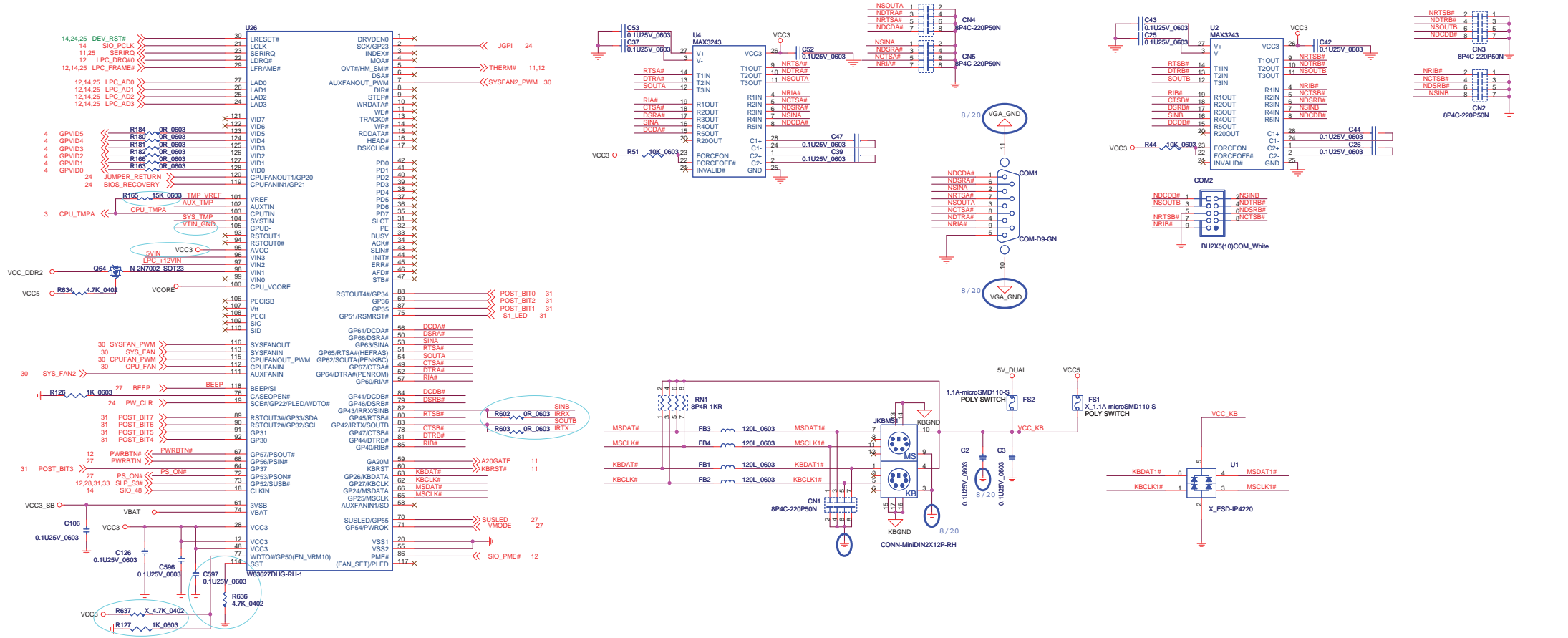
MISC

S5 POWER

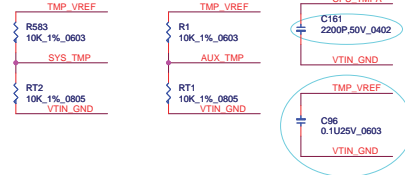
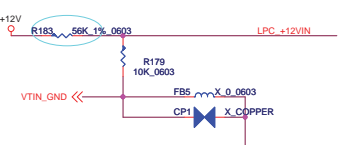
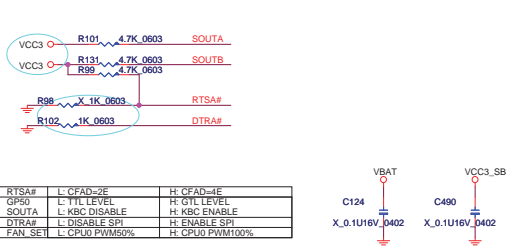


U36C ICH6-M

MSI <i>Link to the Future</i>		
MICRO-START INT'L CO.,LTD.		
Title Intel ICH6M - POWER		
Size	Document Number MS-9623	Rev 1.2
Date:	Friday, August 24, 2007	Sheet 13 of 38



LPC I/O STRAPPING RESISTOR



IR HEADER

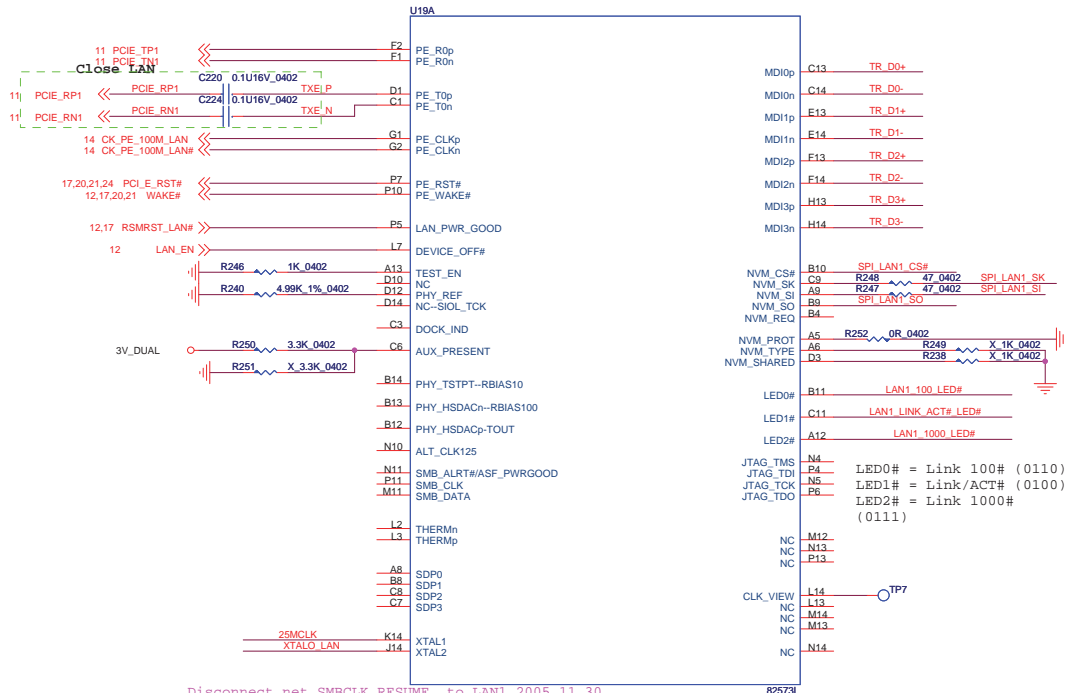


RTSA#	L: CFAD-<E	H: CFAD-<E
GP50	L: IYL LEVEL	H: OYL LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRAF	L: DISABLE SPI	H: ENABLE SPI
FAN_SET	L: CPU0 PWM50%	H: CPU0 PWM100%

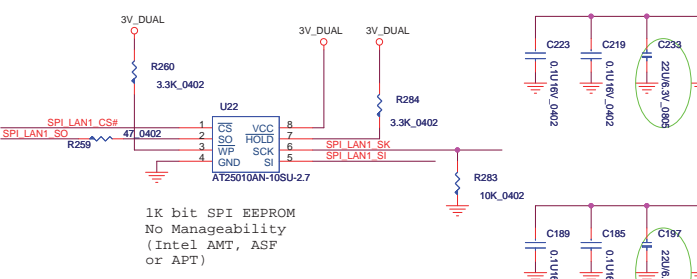
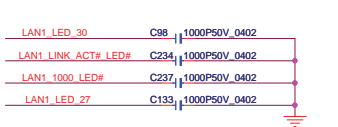
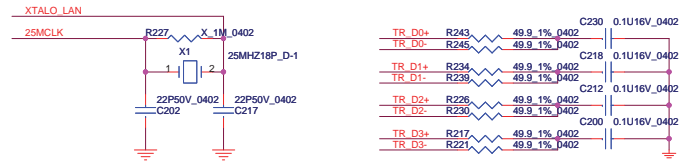
MSI MICRO-START INTL CO.,LTD.

File: **LPC SUPER I/O & CONNECTORS**

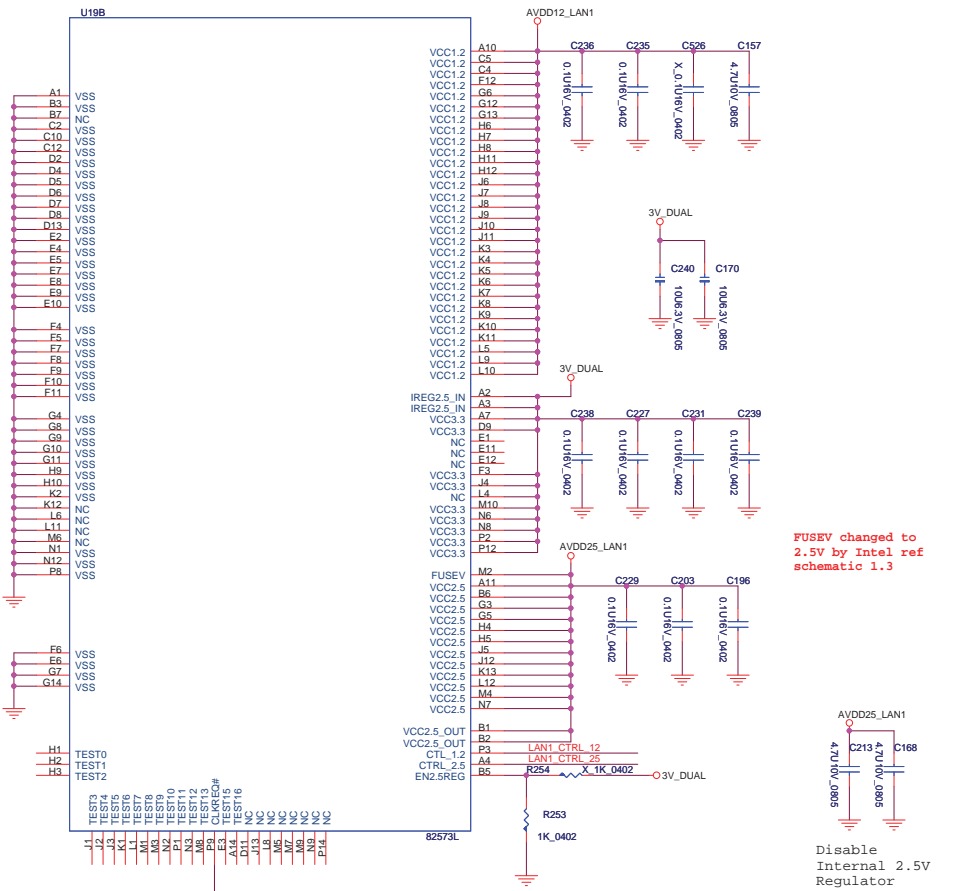
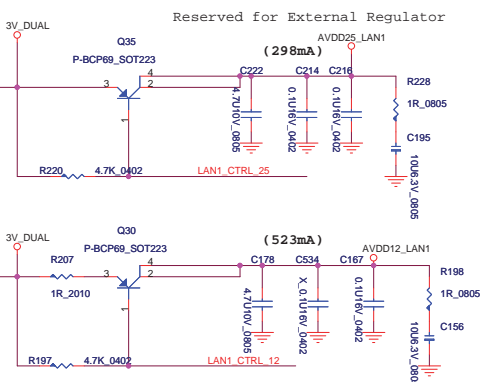
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 15 of 38



Disconnect net SMBCLK_RESUMD to LAN1_2005.11.30
 Disconnect net SMBDATA_RESUME to LAN1_2005.11.30
 Disconnect net SMB_ALERT# to LAN1_2005.11.30



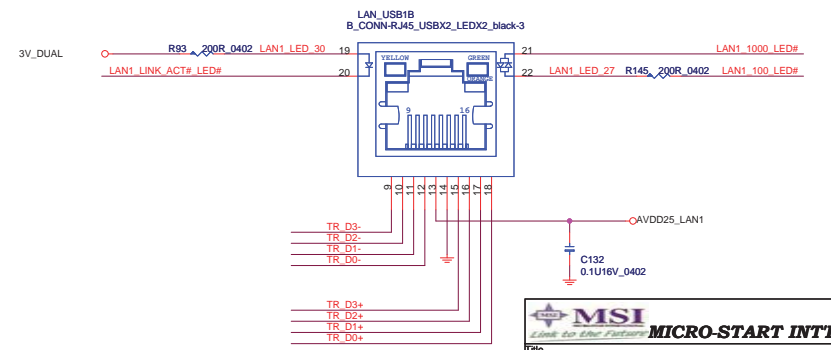
1K bit SPI EEPROM
 No Manageability
 (Intel AMT, ASF
 or APT)



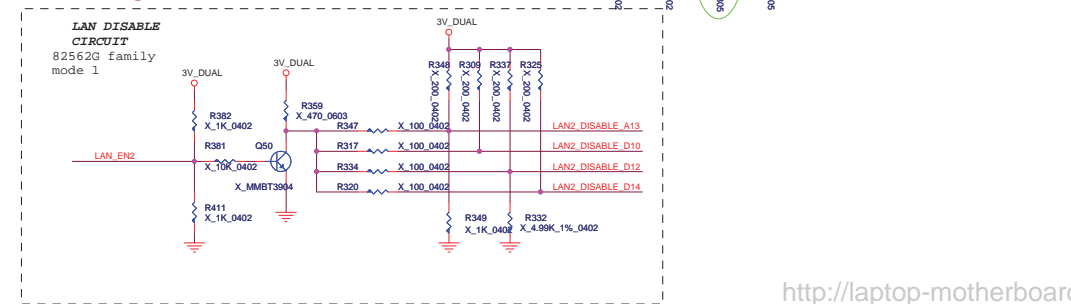
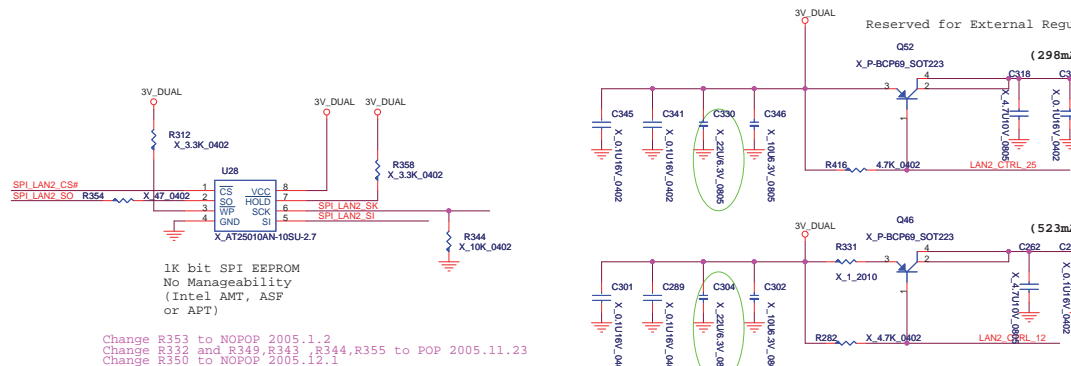
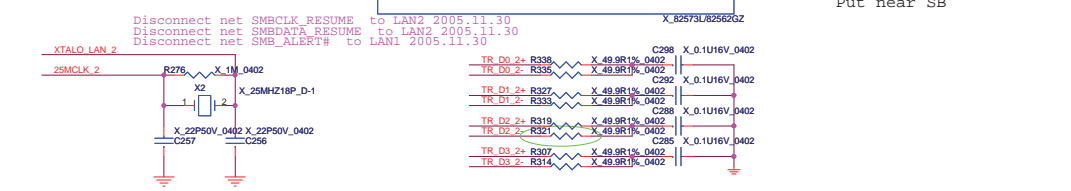
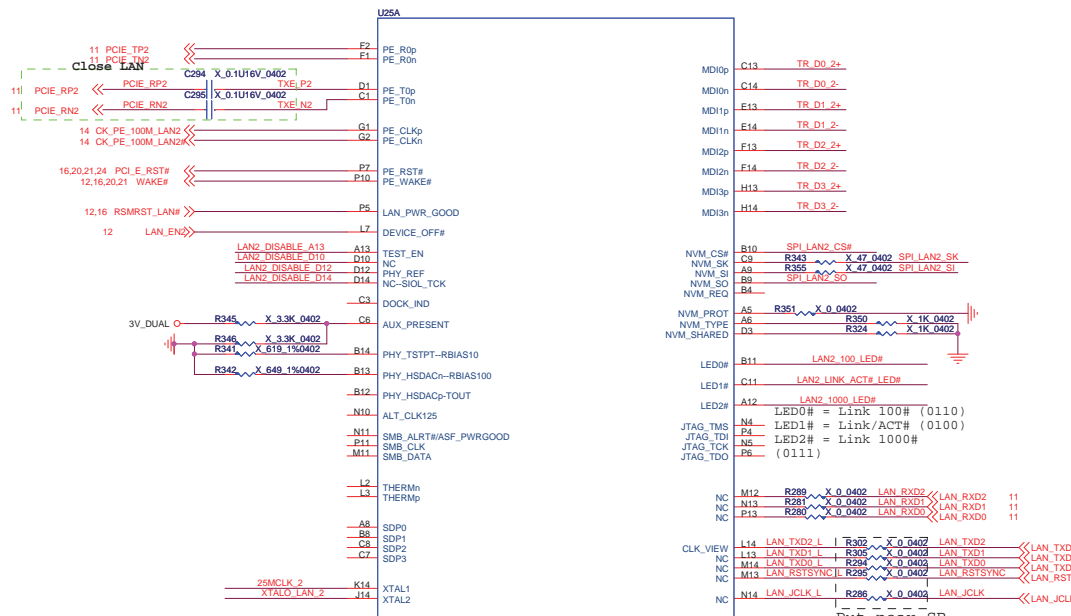
FUSEV changed to 2.5V by Intel ref schematic 1.3

Disable Internal 2.5V Regulator

LAN CONNECTOR



Title		
LAN1 - INTEL 82573L		
Size	Document Number	Rev
	MS-9623	1.1
Date: Friday, August 24, 2007		Sheet 16 of 38

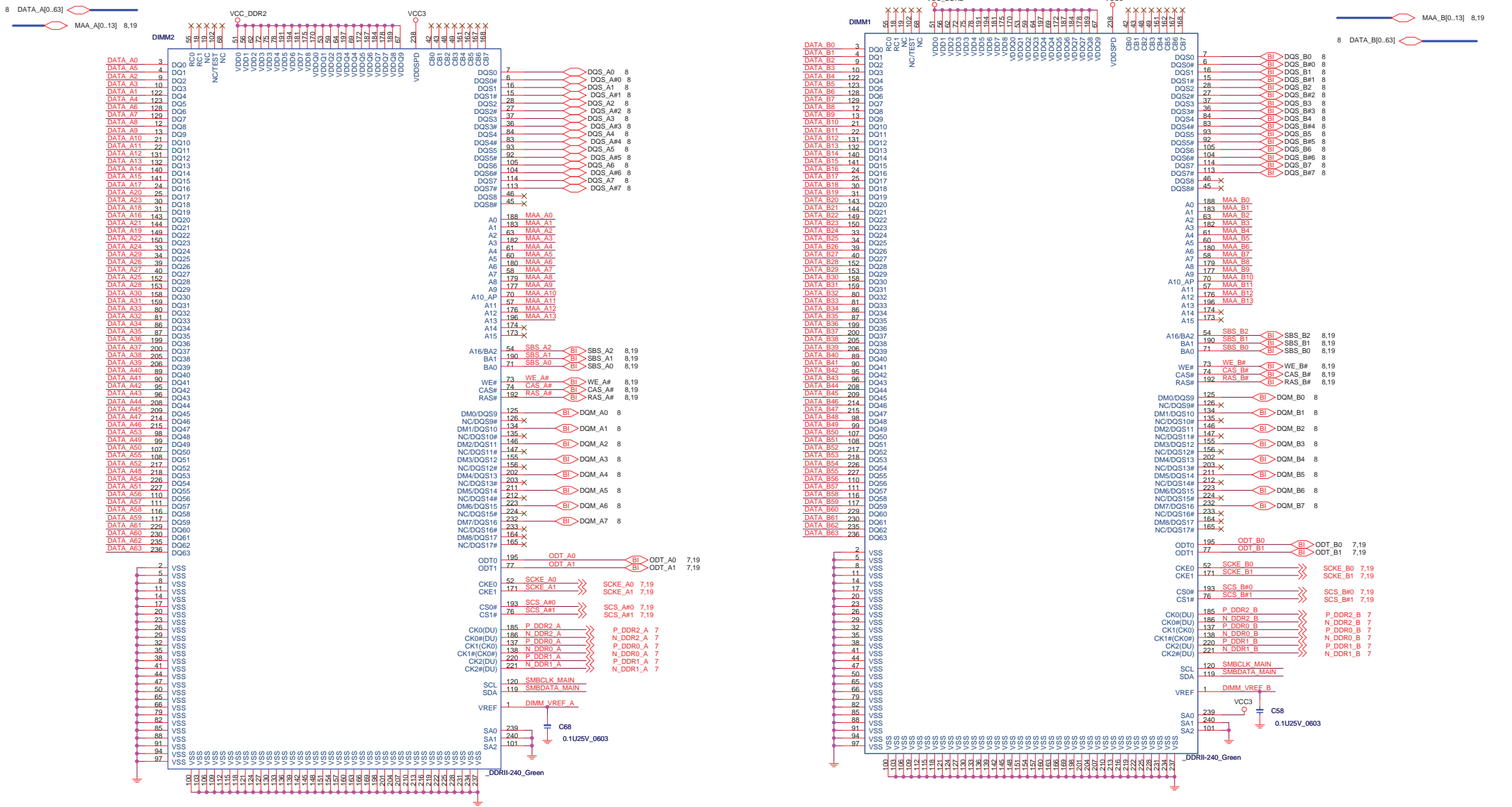


<http://laptop-motherboard-schematic.blogspot.com/>

MSI
Link to Our Factory

MICRO-START INTL CO.,LTD.

File: LAN2 - INTEL 82573L		
Size	Document Number	Rev
	MS-9623	1.1
Date:	Friday, August 24, 2007	Sheet 17 of 38

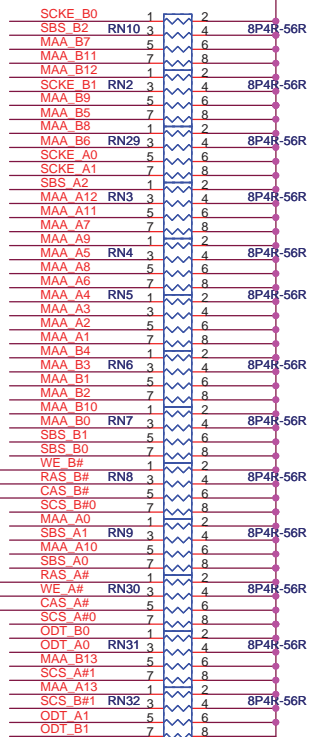
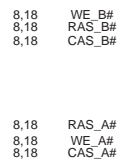
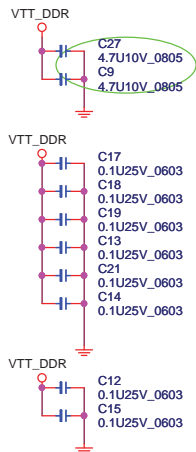
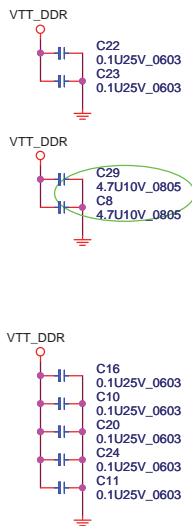


MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

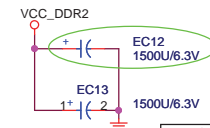
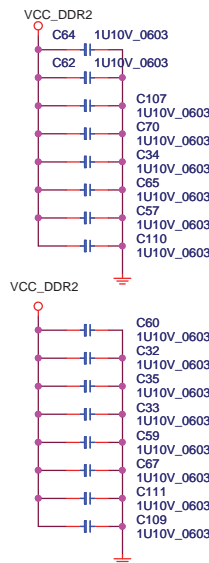
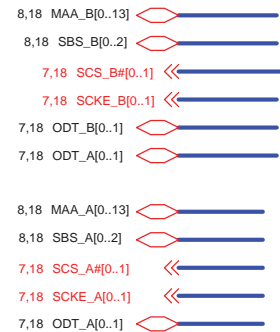
Title: **DDR2 DIMM 1 & 2**

Size	Document Number	Rev
	MS-9623	1.1

Date: Friday, August 24, 2007 Sheet 18 of 38



Change all resistors to RN. Remove R18~R35 and Add RN29~RN32. 2006.3.11



EC13 to C94-1520641-P01 2005.11.23
EC12 to C94-1520641-P01 2006.10.11.

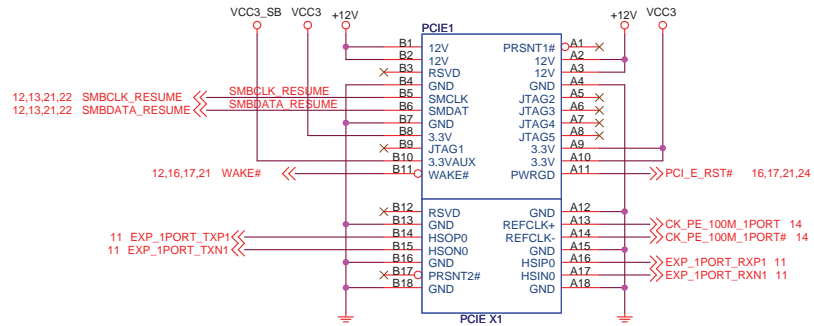
EC1 to C94-1520641-P01 2005.11.23

MSI
Link to the Future **MICRO-START INT'L CO.,LTD.**

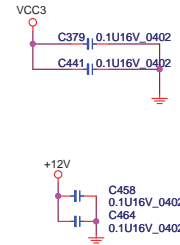
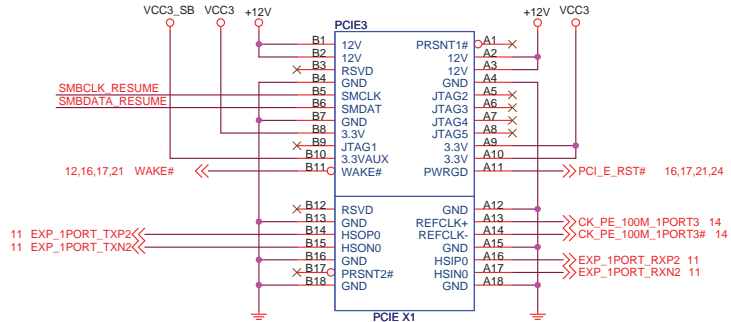
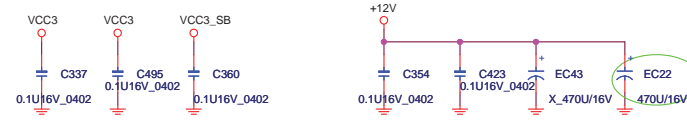
Title: **DDR2 TERMINATION & VTT DECOUPLING**


Size	Document Number	Rev
	MS-9623	1.1
Date:	Friday, August 24, 2007	Sheet 19 of 38

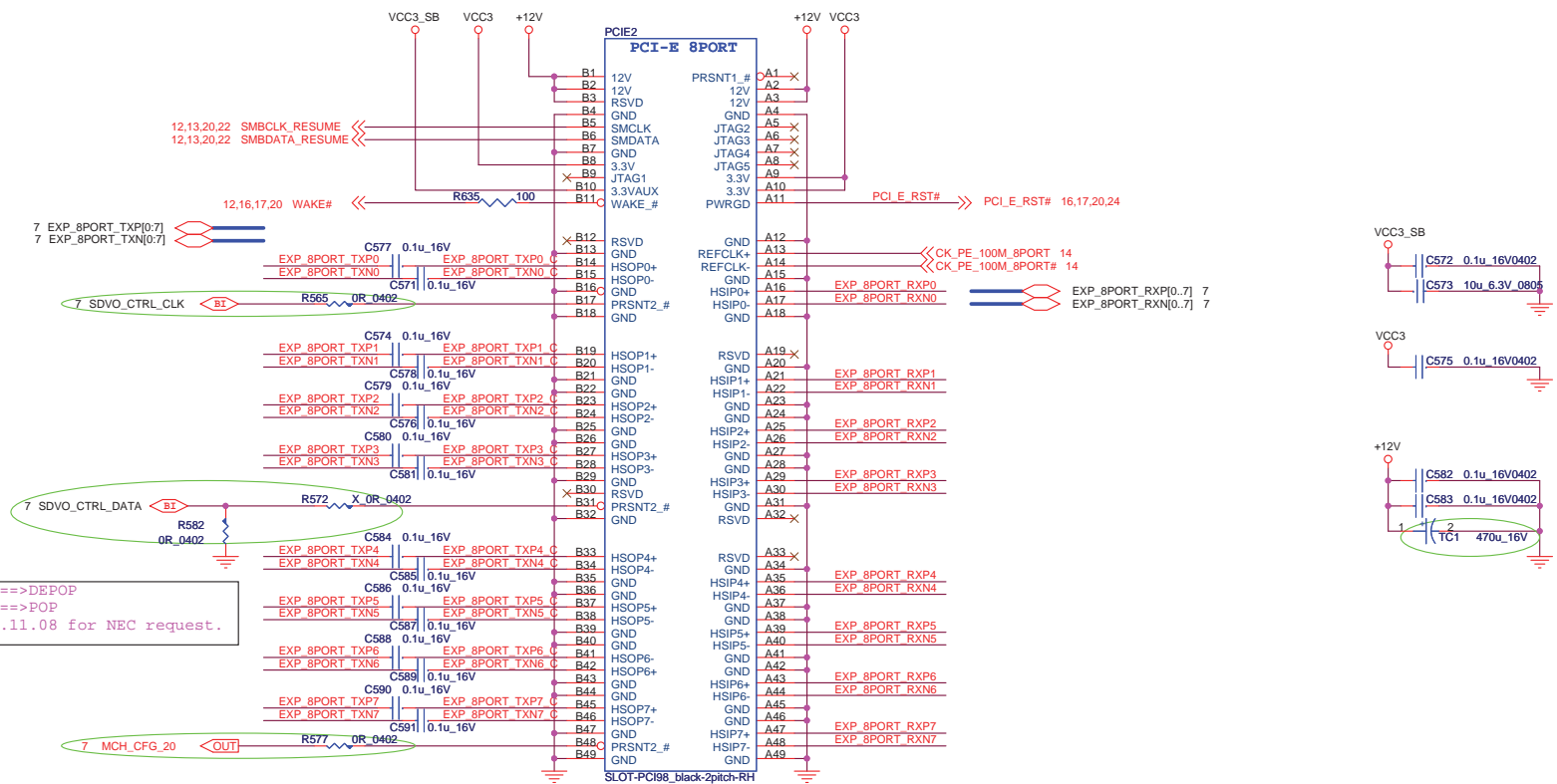
PCI EXPRESS 1-PORT




Remove PCIE2 and PCIE switch 2006.1.27
Remove PCIE_RM1 and PCIE_RM2 2006.1.27



 MSI <i>Link to the Future</i>		
MICRO-START INT'L CO.,LTD.		
Title PCI EXPRESS X1 Slot		
Size	Document Number MS-9623	Rev 1.1
Date:	Friday, August 24, 2007	Sheet 20 of 38

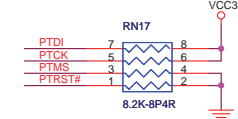
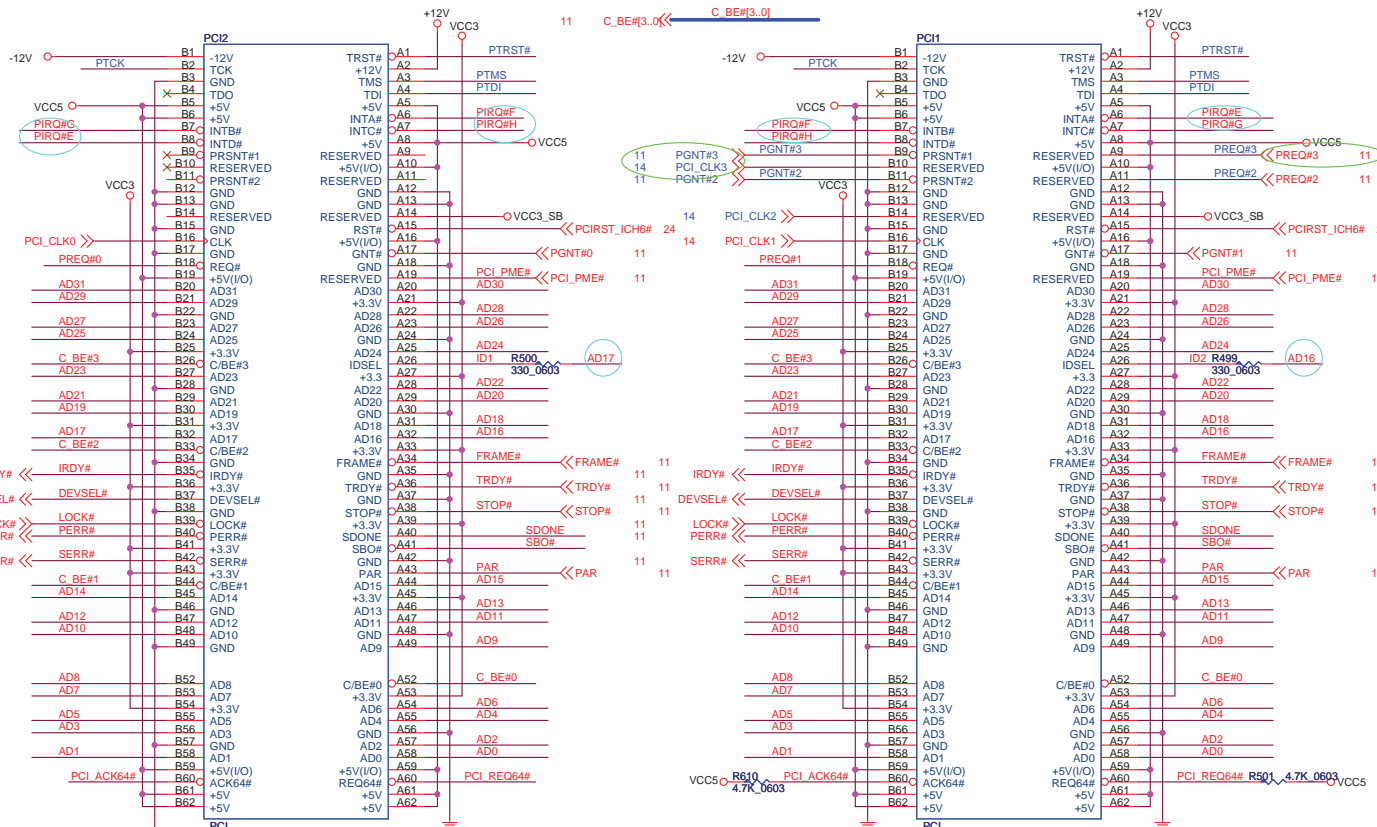


PCI-E * 8

 MICRO-START INT'L CO.,LTD		
Title		
PCI EXPRESS X8 Solt		
Size	Document Number	Rev
	MS-9623	1.1
Date:	Friday, August 24, 2007	Sheet 21 of 38

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

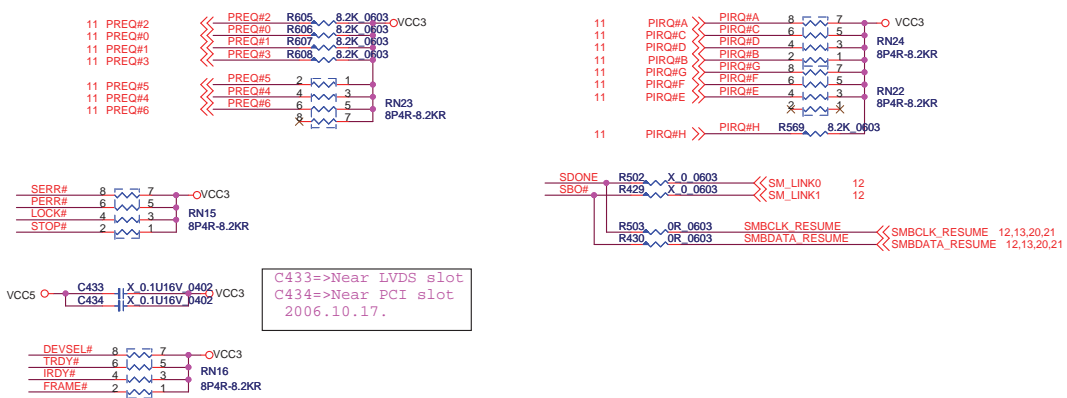


IDSEL = AD17
MASTER = PREQ#0
PIRQ#E

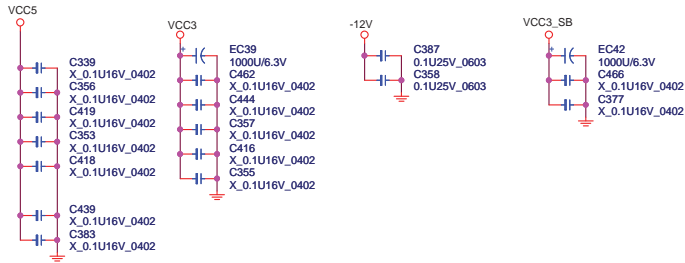
Change PCI_ACK64# to pull high 2006.1.13.
 Add PCI1 Riser3. 2006.10.

IDSEL = AD16
MASTER = PREQ#1
PIRQ#F

PCI PULL-UP / DOWN RESISTORS



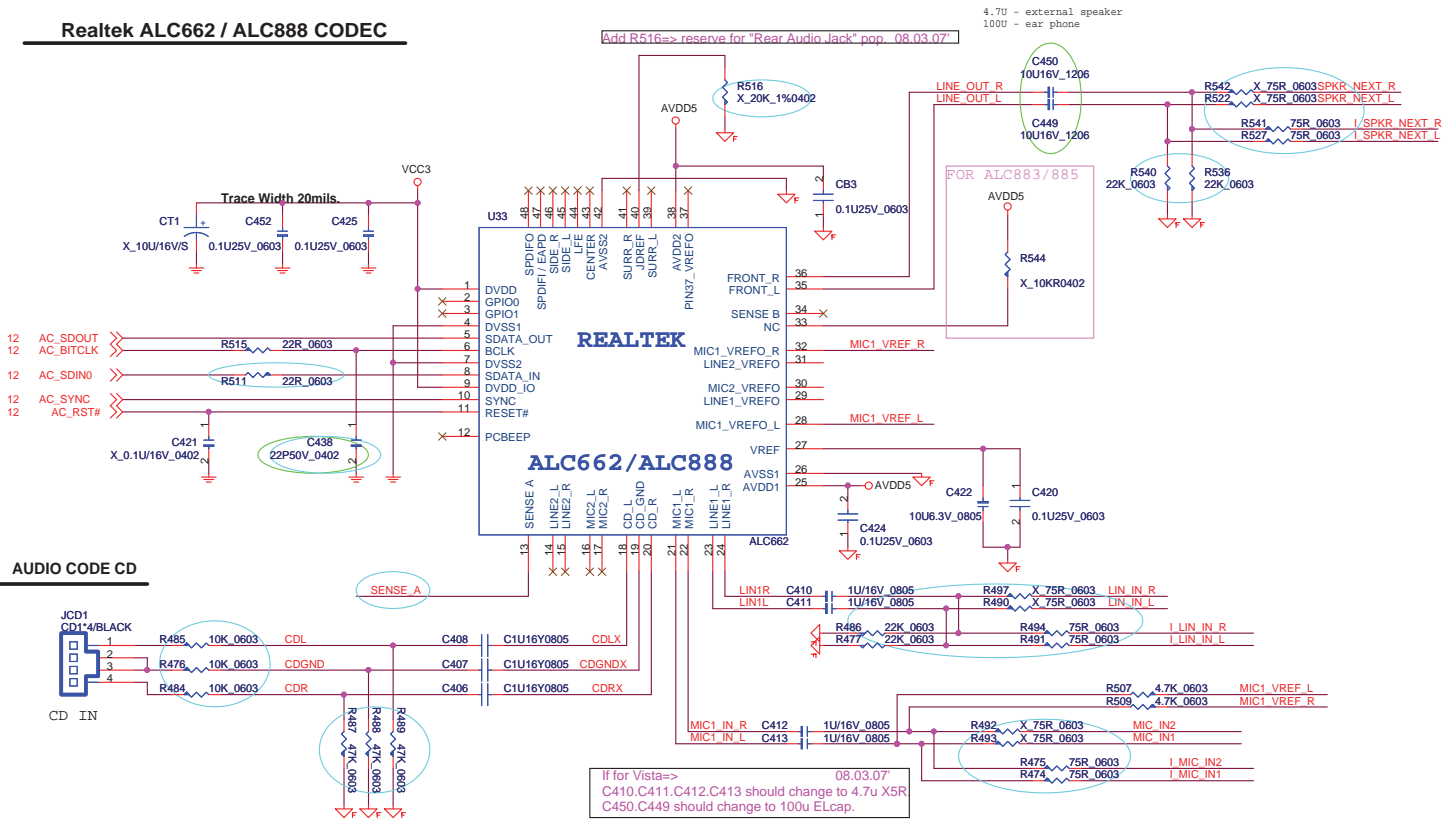
PCI SLOT DECOUPLING CAPACITORS



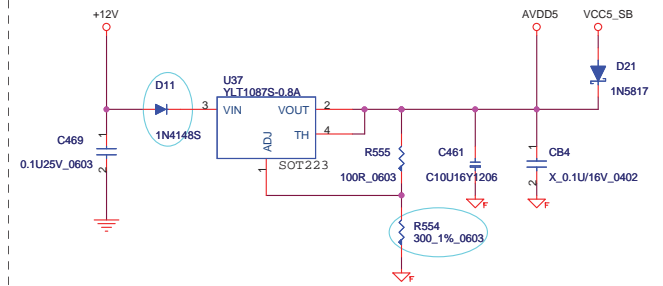
C433=>Near LVDS slot
 C434=>Near PCI slot
 2006.10.17.

MSI <i>Link to the Future</i>		
MICRO-START INT'L CO.,LTD.		
PCI 1 & 2 Slots		
Size	Document Number	Rev
	MS-9623	1.1
Date:	Friday, August 24, 2007	Sheet 22 of 38

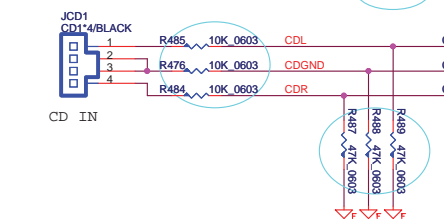
Realtek ALC662 / ALC888 CODEC



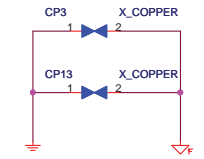
AUDIO CODE REGULATORS



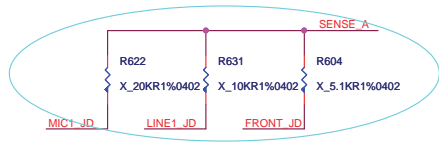
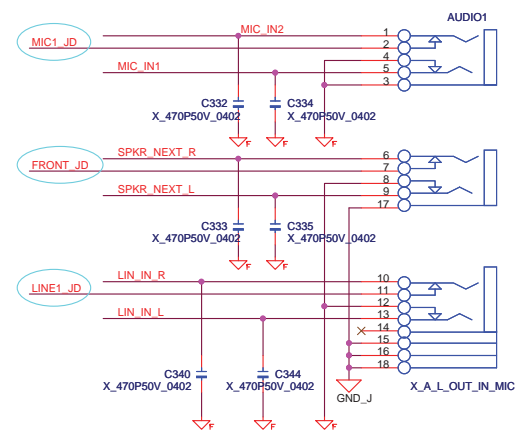
AUDIO CODE CD



EMI Solution

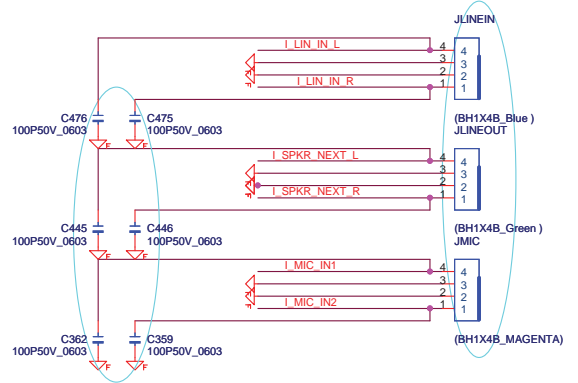


Rear Audio Jack (NOPOP)



Reserve for "Rear Audio Jack" pop. 08.03.07

FOR Intel INTERNAL HEADER



Change three White pin headers to different colors. (Blue, Green and Magenta) 08.21.07

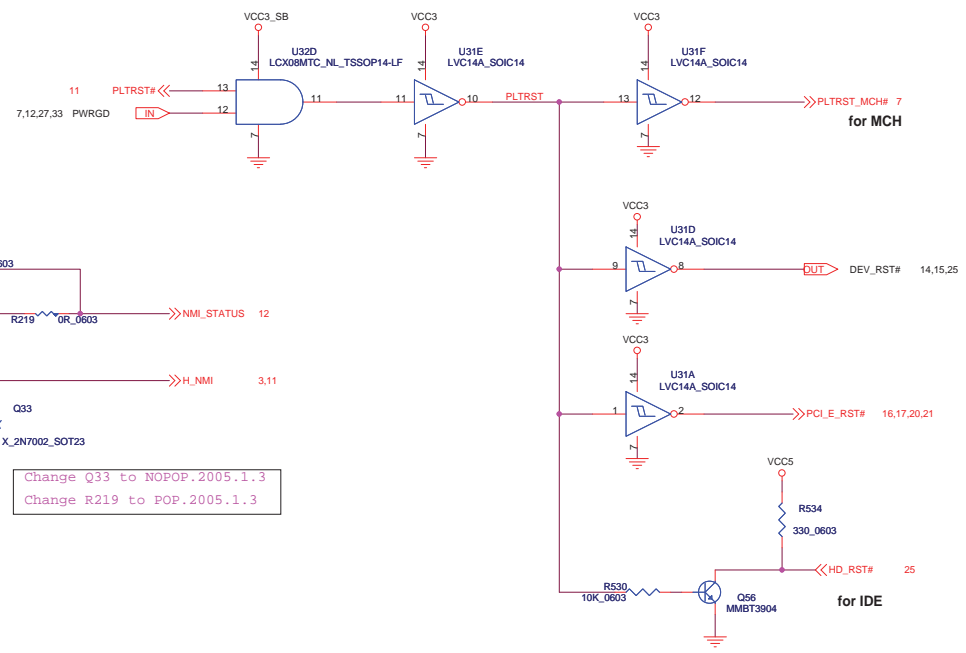
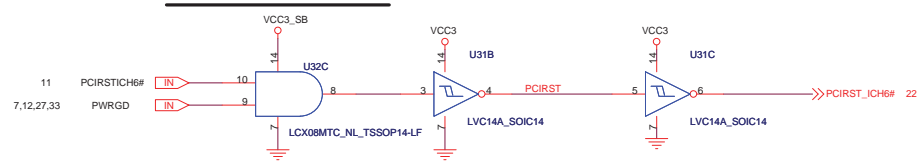
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **Codec-ALC662/ALC888**

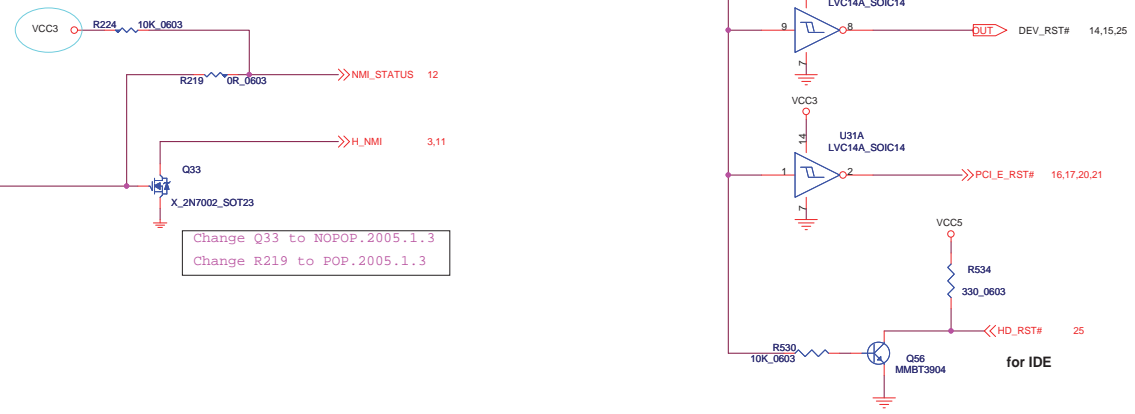
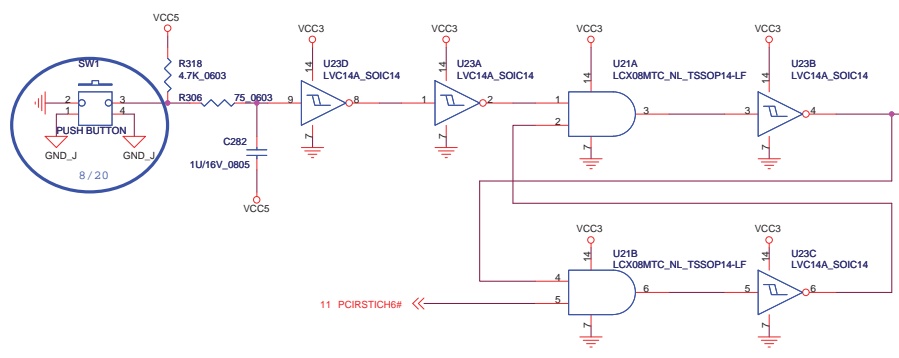
Size: Document Number **MS-9623** Rev **1.2**

Date: Friday, August 24, 2007 Sheet 23 of 38

PCI RESET Circuit



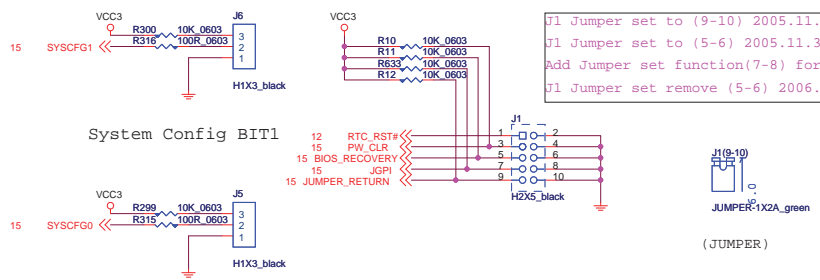
NMI Switch Circuit



Change Q33 to NOPOP.2005.1.3
Change R219 to POP.2005.1.3

JUMPER

Add Jumper function 2005.9.16

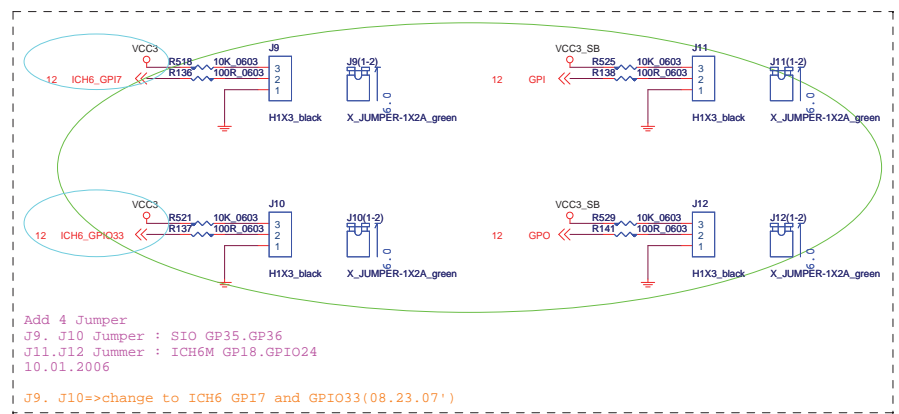


J1 Jumper set to (9-10) 2005.11.30
J1 Jumper set to (5-6) 2005.11.30
Add Jumper set function(7-8) for SIO_GP45 2006.1.27
J1 Jumper set remove (5-6) 2006.3.31

System Config BIT1

System Config BIT0

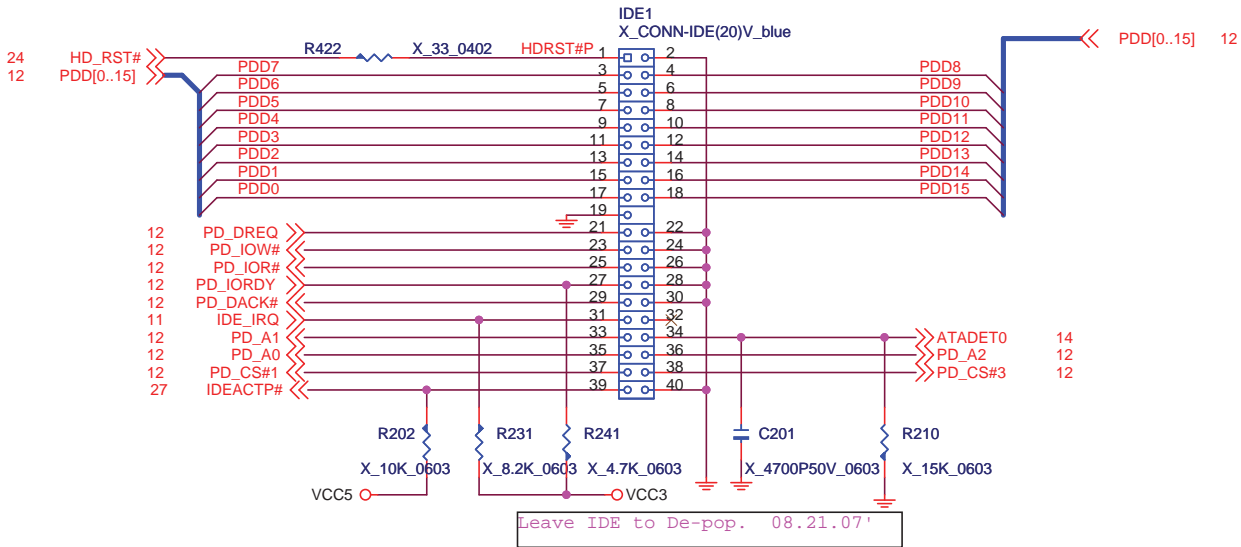
Jumper:1-2:CMOS-CLR
Jumper:3-4:PASSWORD_CLR
Jumper:5-6:BIOS-RECOVERY
Jumper:9-10:Jumper-Return-Check



Add 4 Jumper
J9, J10 Jumper : SIO GP35,GP36
J11,J12 Jumper : ICH6M GP18,GPIO24
10.01.2006
J9, J10->change to ICH6 GPIO7 and GPIO33(08.23.07')

MSI <i>Leading the Industry</i>		
MICRO-START INT'L CO.,LTD.		
Title: PCI Reset & NMI Switch & Jumper		
Size:	Document Number:	Rev:
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 24 of 38

ATA 33/66/100 IDE Connectors

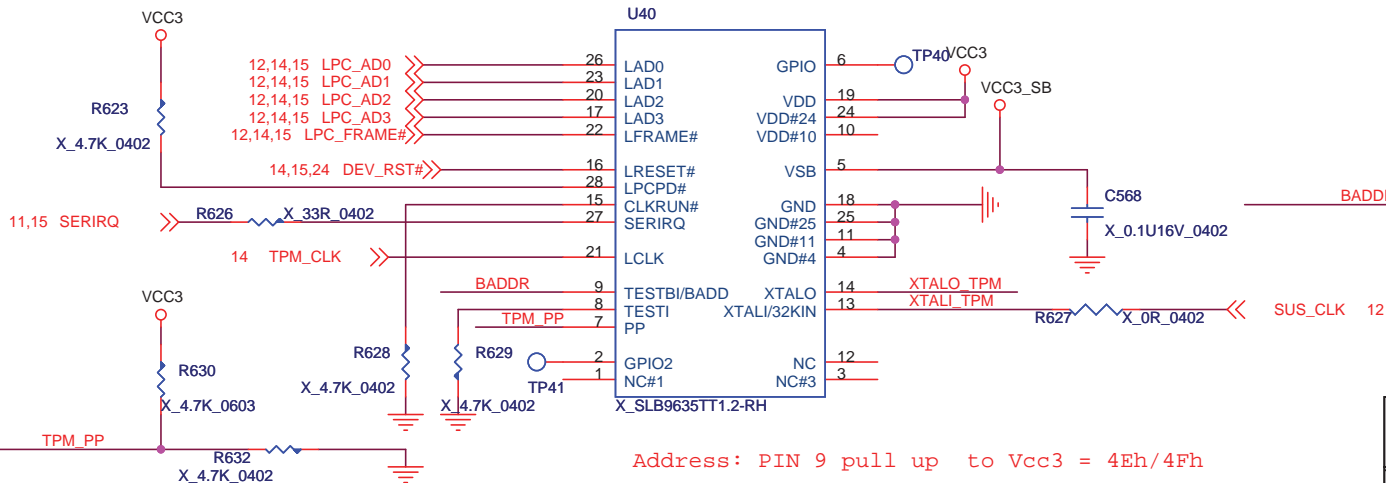
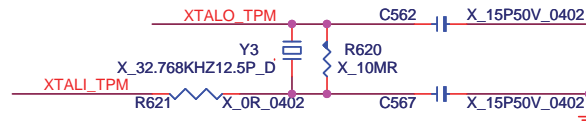
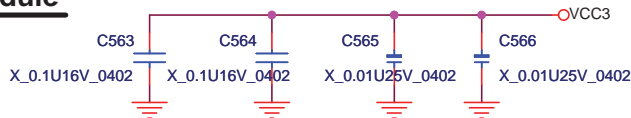


TPM Module

NOPOP

Update to TPM1.2 2006.1.25

TPM Module



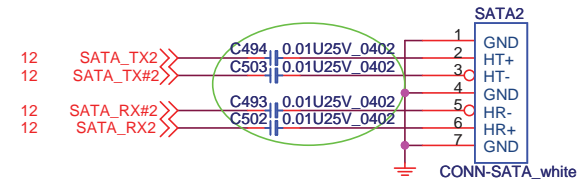
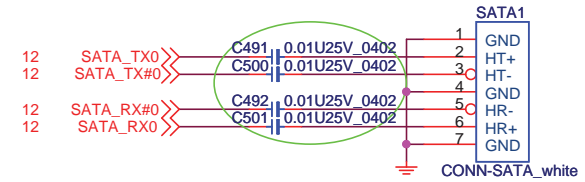
Address: PIN 9 pull up to Vcc3 = 4Eh/4Fh

Address: PIN 9 pull down to GND = 2Eh/2Fh

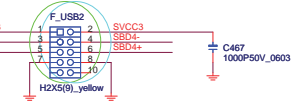
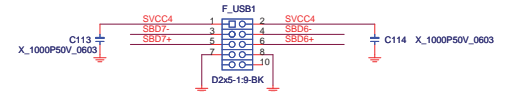
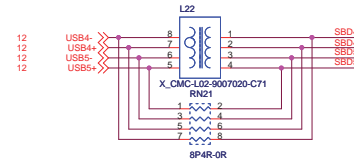
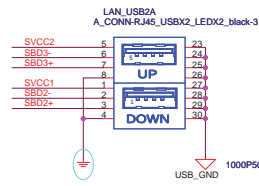
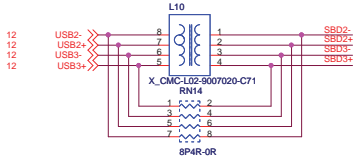
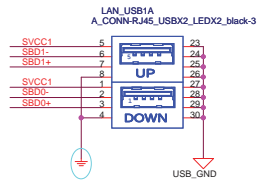
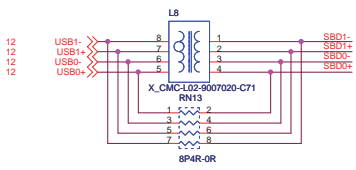
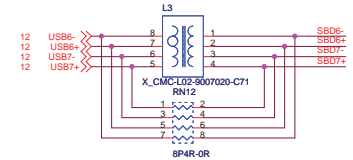
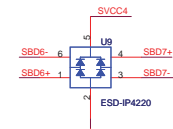
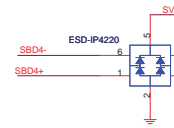
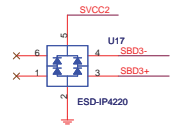
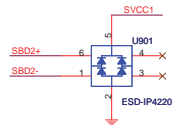
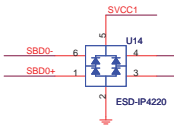
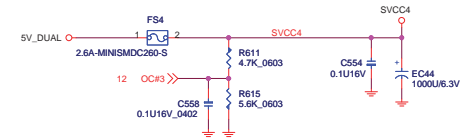
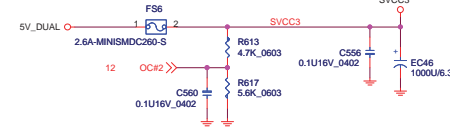
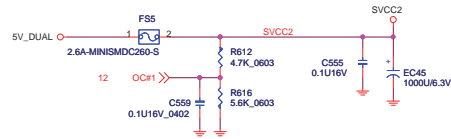
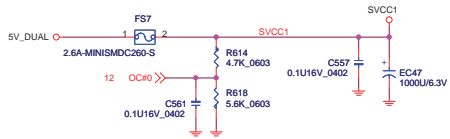
Modify TPM schematic for vender suggestion 2006.1.27

<http://laptop-motherboard-schematic.blogspot.com/>

SERIAL ATA CONNECTOR BLOCK



MSI <small>MICRO-STAR INTERNATIONAL</small> <i>Link to the Future</i>		
MICRO-STAR INT'L CO.,LTD.		
Title IDE & SATA Connectors/TPM		
Size	Document Number MS-9623	Rev 1.2
Date:	Friday, August 24, 2007	Sheet 25 of 38



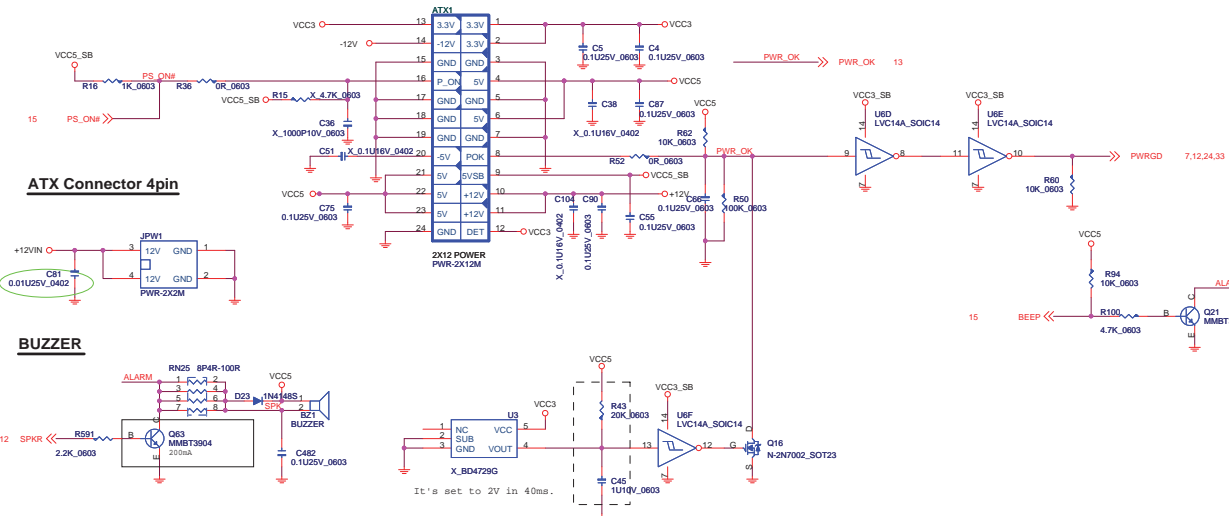
Change connector color to yellow with housing.
10.01.2006
Change from smaller to standard size housing.
07.27.2007

MSI
MICRO-START INT'L CO.,LTD.

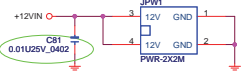
File: **USB Connectors**

Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 26 of 38

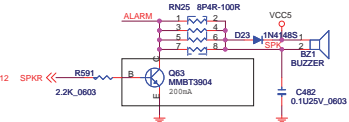
ATX Connector 24pin



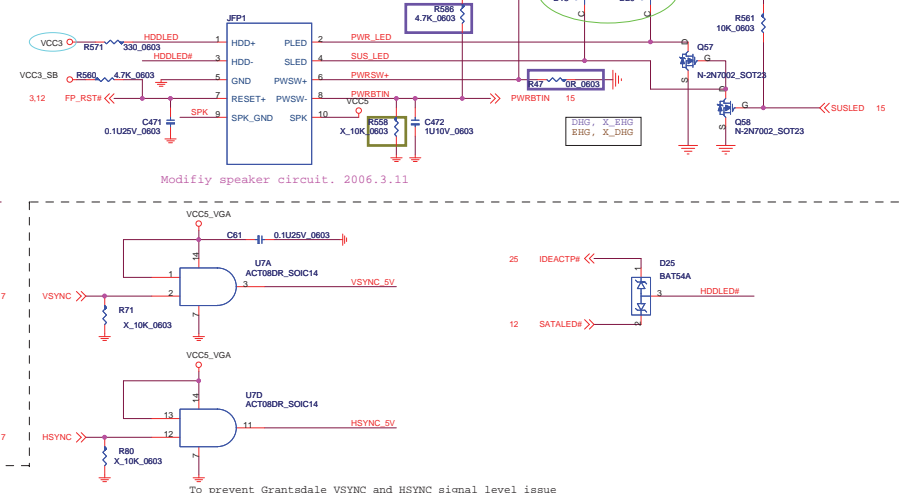
ATX Connector 4pin



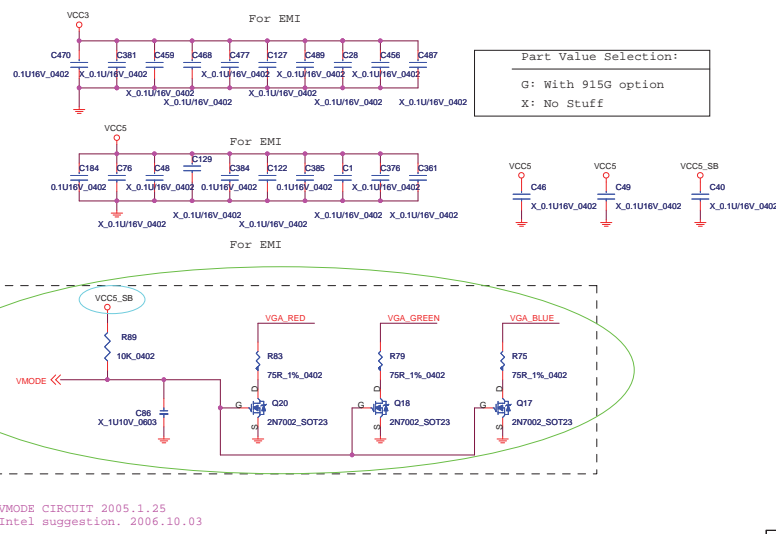
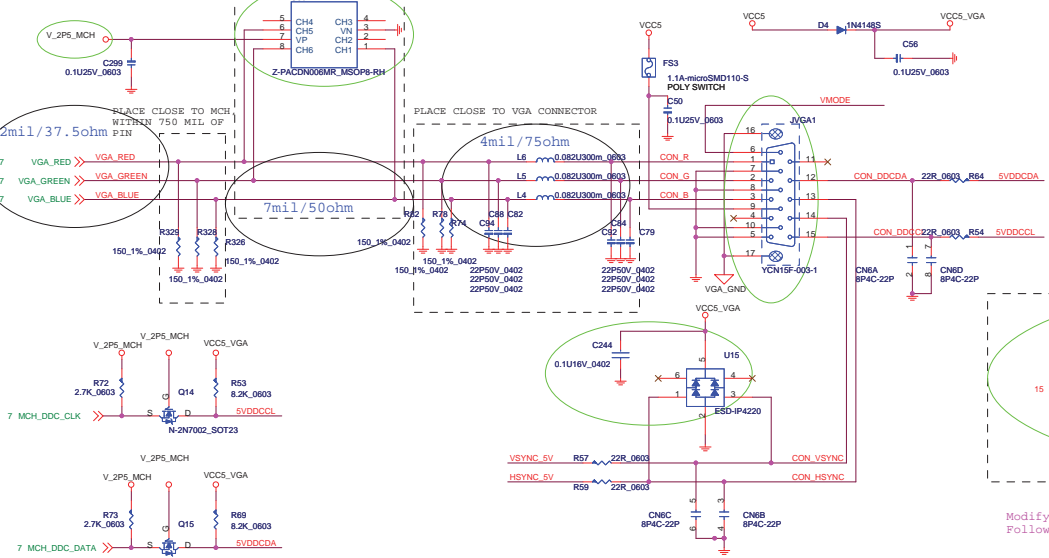
BUZZER



Intel Front Panel



VGA Connector



Change 1PS226 x2 to PACDN006NR (U35) x1 and change diode power to "V_1P5_VORE" 2006.10.23

Need to change bigger JVGA footprint 2005.11.30

Change COM port to VGA(bottom)+COM(top) 2006.3.7

Change 1PS226 x2 to IP4220 x1(U15) and add one 0.1u cap at power pin. 2006.10.23

Modify VMODE CIRCUIT 2005.1.25
Follow Intel suggestion. 2006.10.03

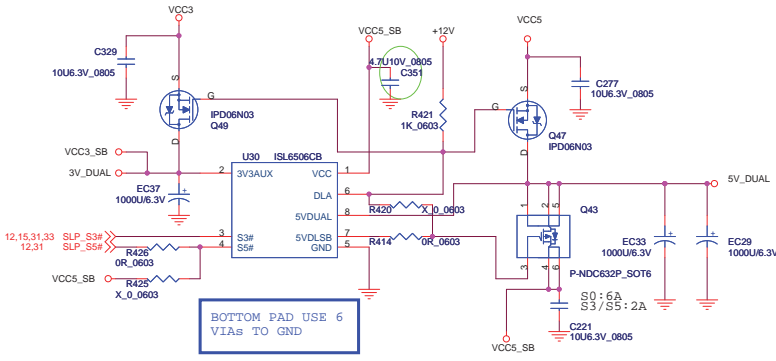
MSI
Micro-Start Int'l Co., Ltd.

File: **ATX Connector & Front Panel & VGA Connector**

Size	Document Number	Rev
	MS-9623	1.2

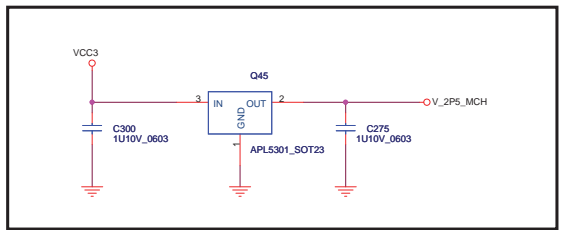
Date: Friday, August 24, 2007 Sheet 27 of 38

5V_DUAL



BOTTOM PAD USE 6 VIAS TO GND

5V_DUAL ALWAYS ON:R942-NC,R941-0,R940-0,R945-NC
5V_DUAL DISABLE IN S5:R942-0,R941-NC,R940-NC,R945-0

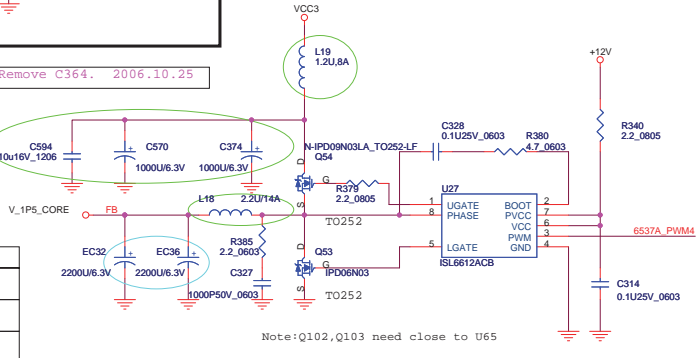


Remove C364. 2006.10.25

V_1P5_CORE

1.5V/14A

Change C364 and C374 to 220UF_16V 2006.2.28
Change C364 and C374 to 1000u X3 +10u MLCC. 2006.10.09
Remove J7, R378, Q51, R97 (1.5V or 1.05V choosing jumper and circuit) 2006.10.24
Change EC32 and EC36 from C94-10206A1-P01 to C94-2220661-P01. 2007.08.06



SYSTEM POWER

BOM change R92 to 0603 2005.11.17
R81 change from 8.2K to 20K. 2007.08.06.
R86 change from 1k to 0ohm. 2007.08.06.
R89 change to NON-POP. 2007.08.06.
Add one Schokey Diode on output 2007.08.06

V_GMCH_CORE

1.05V or 1.5V

V_FSB_VTT

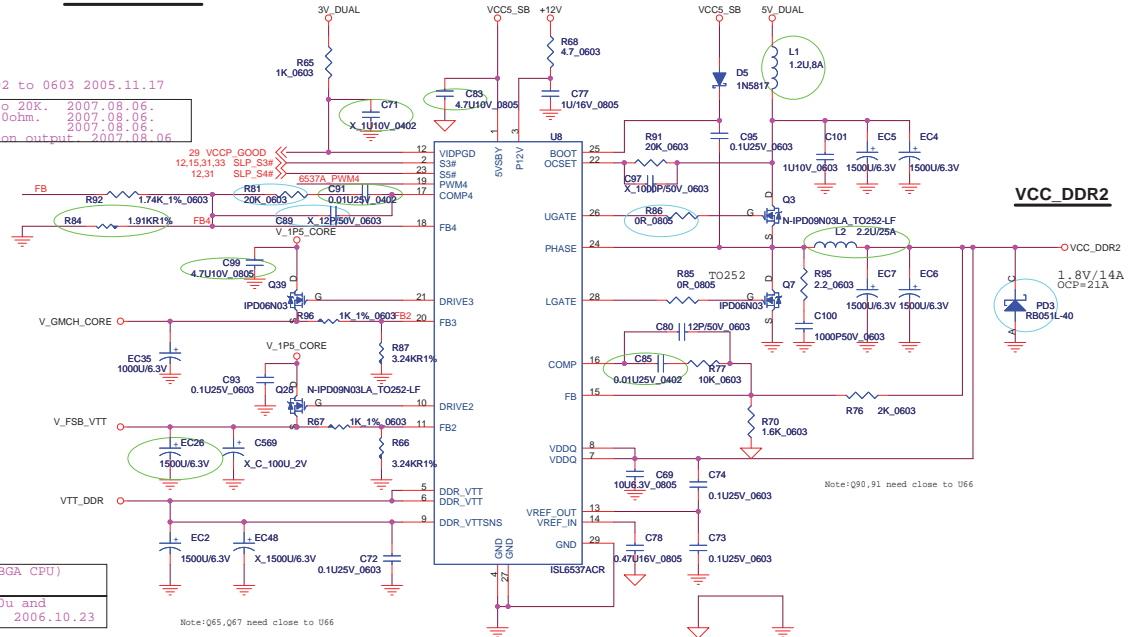
1.05V

VTT_DDR

0.9V/2A

Add C569 if C128 nopop (for BGA CPU) 2006.2.27
Change EC26 from 100u to 1500u and leave C569 and C182 NON-POP. 2006.10.23

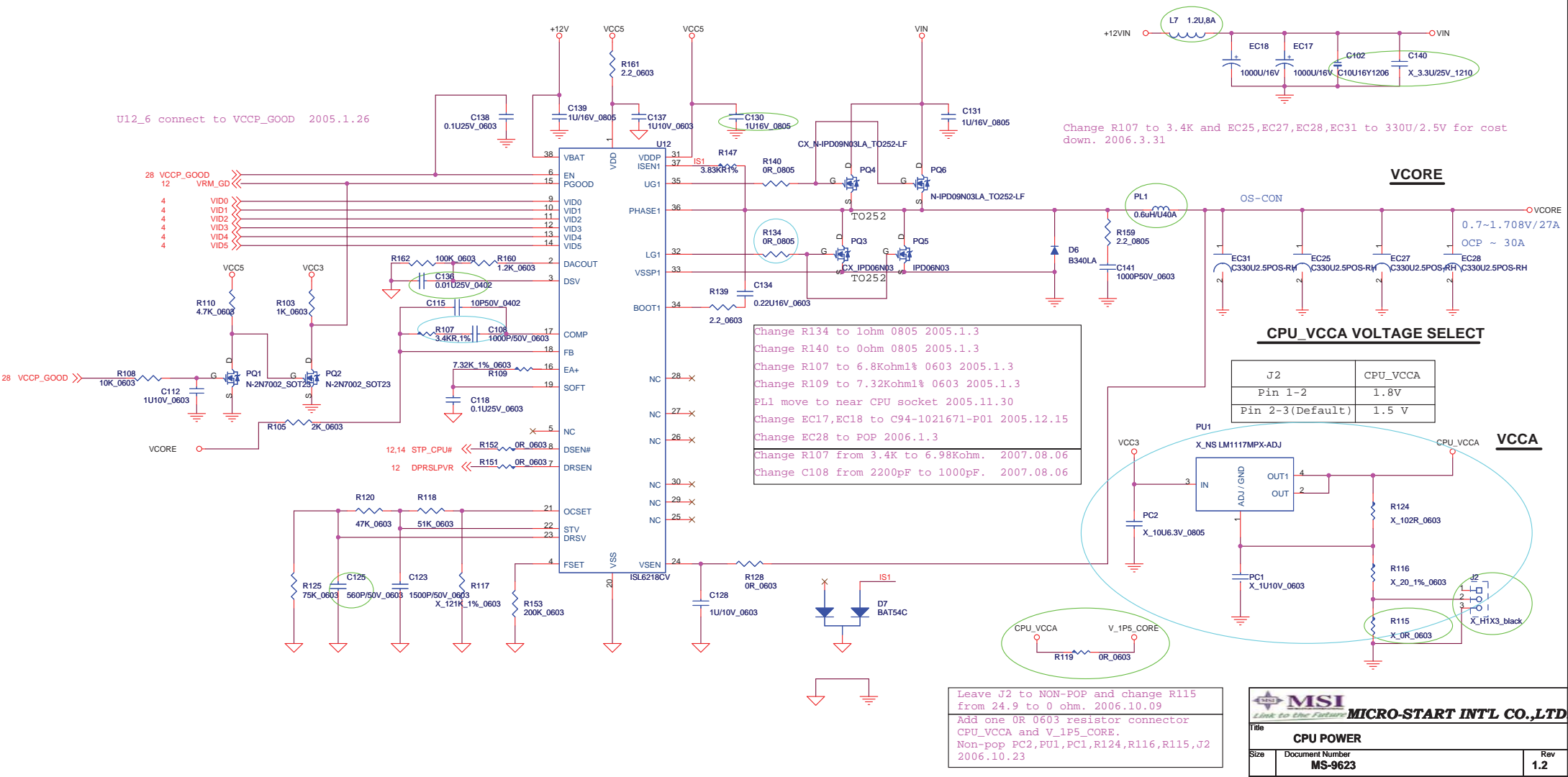
Note:Q65,Q67 need close to U66



VCC_DDR2

1.8V/1.4A
OCF=21A

MSI <small>Link to the Future</small>		
MICRO-START INT'L CO.,LTD.		
SYSTEM POWER		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 28 of 38



MSI
 Link to the Future **MICRO-START INT'L CO.,LTD.**

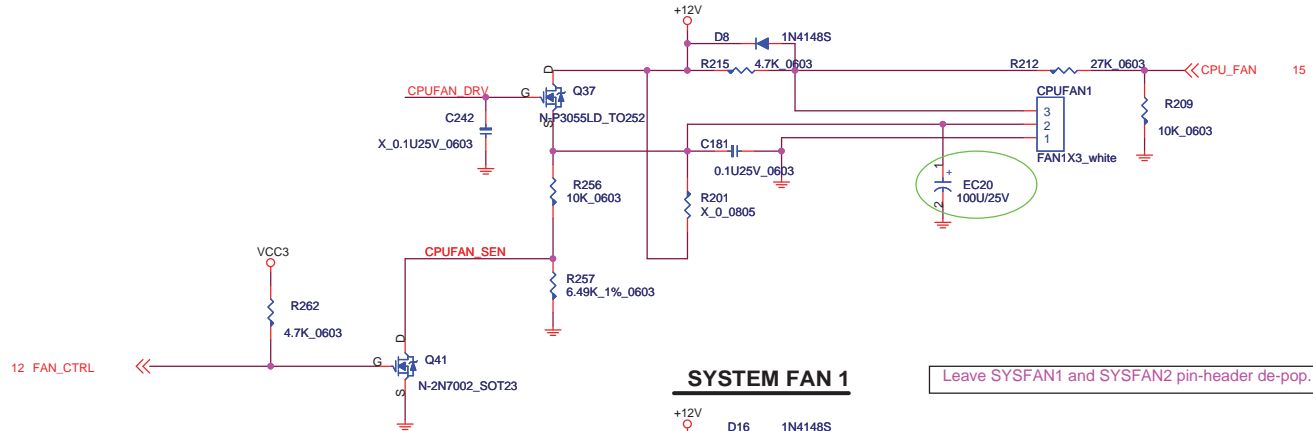
CPU POWER

Size	Document Number	Rev
	MS-9623	1.2

Date: Friday, August 24, 2007 Sheet 29 of 38

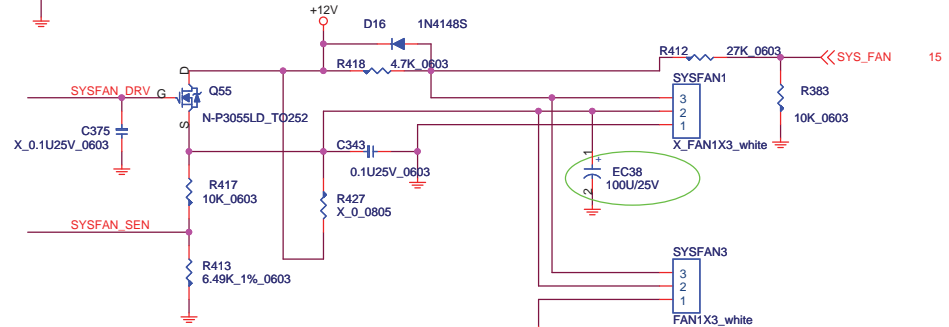
FAN CONTROL

CPU FAN



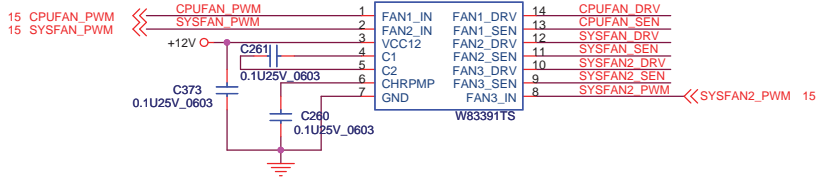
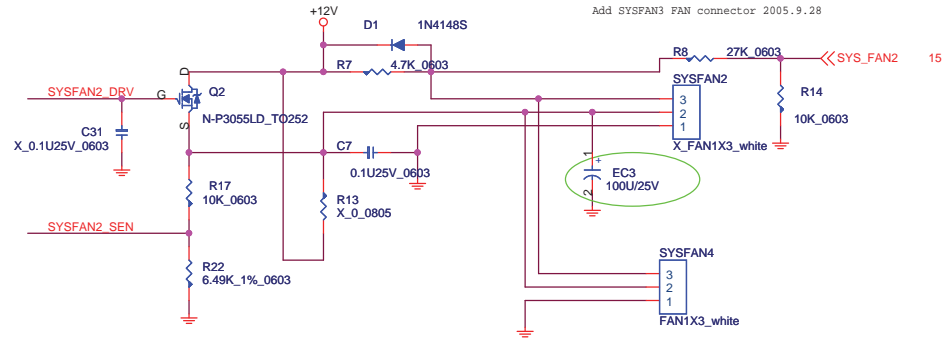
SYSTEM FAN 1

Leave SYSFAN1 and SYSFAN2 pin-header de-pop. 08.10.07'

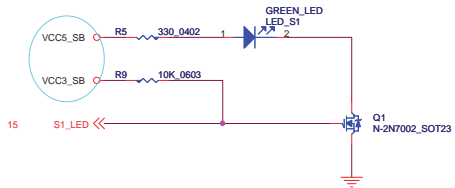


SYSTEM FAN 2

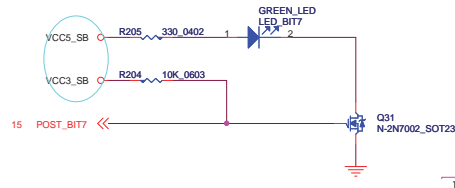
Add SYSFAN3 FAN connector 2005.9.28



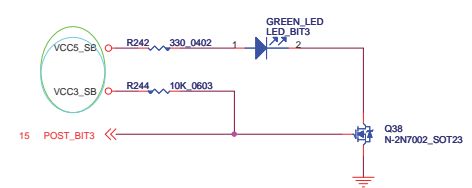
S1 Status LED



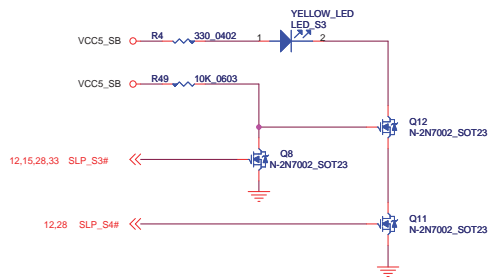
POST Status LED MSB BIT7



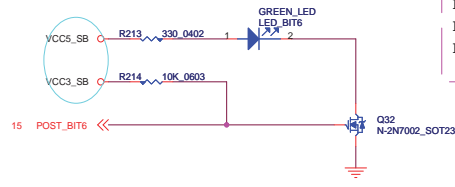
POST Status LED MSB BIT3



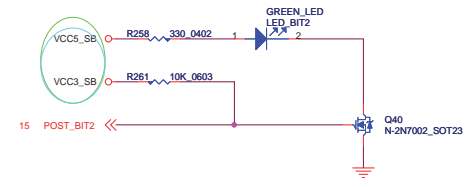
S3 Status LED



POST Status LED MSB BIT6

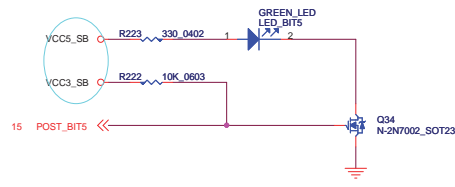


POST Status LED MSB BIT2

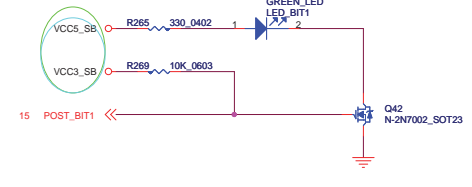


BIT0-W83627DHG-PIN88 (GP34)
 BIT1-W83627DHG-PIN87 (GP35)
 BIT2-W83627DHG-PIN69 (GP36)
 BIT3-W83627DHG-PIN64 (GP37)
 BIT4-W83627DHG-PIN92 (GP30)
 BIT5-W83627DHG-PIN91 (GP31)
 BIT6-W83627DHG-PIN90 (GP32)
 BIT7-W83627DHG-PIN89 (GP33)
 07.27.07'

POST Status LED MSB BIT5

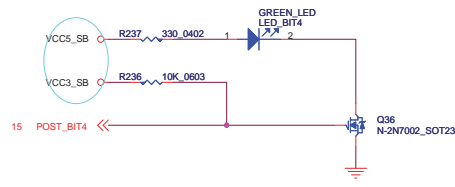


POST Status LED MSB BIT1

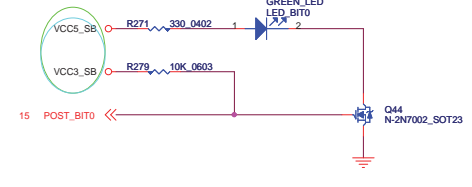


Remove "S4 Status LED circuit".
 2006.11.10. For NEG request.

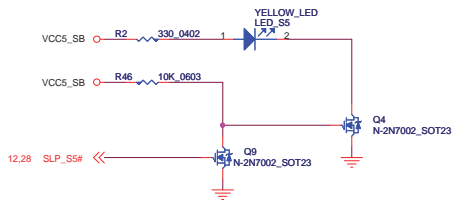
POST Status LED MSB BIT4



POST Status LED MSB BIT0



S5 Status LED



GPIO

SIO GPIO	GPIO	PIN	FUNCTION	I/O/NC	POWER	NOTE	
SIO GPIO	GP10	PIN128	CPU VID0	O	VCC5		
	GP11	PIN127	CPU VID1	O	VCC5		
	GP12	PIN126	CPU VID2	O	VCC5		
	GP13	PIN125	CPU VID3	O	VCC5		
	GP14	PIN124	CPU VID4	O	VCC5		
	GP15	PIN123	CPU VID5	O	VCC5		
	GP20	PIN120	JUMPER RETURN	I	VCC5		
	GP21	PIN119	BIOS RECOVERY	I	VCC5		
	GP22	PIN118	PASSWORK CLEAR	I	VCC5		
	GP23	PIN96	S1 STATUS LED	O	VCC5		
	GP50	PIN110	STATUS LED BIT0	O	VCC5		
	GP51	PIN109	STATUS LED BIT1	O	VCC5		
	GP52	PIN108	STATUS LED BIT2	O	VCC5		
	GP53	PIN107	STATUS LED BIT3	O	VCC5		
	GP30	PIN92	STATUS LED BIT4	O	VCC5_SB		
	GP31	PIN91	STATUS LED BIT5	O	VCC5_SB		
	GP32	PIN90	STATUS LED BIT6	O	VCC5_SB		
	GP33	PIN89	STATUS LED BIT7	O	VCC5_SB		
	GP35	PIN86	N/A	O	VCC5_SB		
	GP43	PIN71	N/A	O	VCC5_SB		
	GP44	PIN70	N/A	O	VCC5_SB		
	GP45	PIN69	N/A	O	VCC5_SB		
	GP24	PIN95	System Config BIT0	O	VCC5		
	GP25	PIN94	System Config BIT1	O	VCC5		
	GP47	PIN67	PSOUT	O	VCC5_SB		
	GP46	PIN68	PSIN	I	VCC5_SB		
	GP37	PIN64	SUSLED	O	VCC5_SB		
	GP42	PIN72	PSON	I	VCC5_SB		
	GP41	PIN73	SLP_S3	I	VCC5_SB		
	GP34	PIN88	IRRXX	I	VCC5_SB		
	ICH6-M GPIO	GPI[0]	B7	PCI_REQ[6]#	I	VCC5	
		GPI[1]	E8	PCI_REQ[5]#	I	VCC5	
		GPI[40]	F7	PCI_REQ[4]#	I	VCC5	
		GPI[2]	D9	PIRQE#	I	VCC3	
		GPI[3]	C7	PIRQF#	I	VCC3	
		GPI[4]	C6	PIRQG#	I	VCC3	
		GPI[5]	M3	PIRQH#	I	VCC3	
		GPI[6]	AD19	Bus Master Busy	I	VCC3	
		GPI[8]	R1	GPI	I	VCC3	
		GPIO[24]V3		GPO	O	VCC3_SB	
GPI[9]		C23	USB OCP PORT4	I	VCC3_SB		
GPI[10]		D23	USB OCP PORT5	I	VCC3_SB		
GPI[14]		C25	USB OCP PORT6	I	VCC3_SB		
GPI[15]		C24	USB OCP PORT7	I	VCC3_SB		
GPI[11]		W6	SBM_ALERT#	I	VCC3_SB		
GPI[12]		M2	NMI SWITCH STATUS	I	VCC3		
GPI[13]		R6	SIO_PME#	I	VCC3_SB		
GPO[19]		AB21	BIOS_WP#	O	VCC3		
GPO[21]		AD20	FAN_CTR	O	VCC3		
GPO[23]		AD21	RTC_RST1#	O	VCC3		
GPI[26]		AF17	SATA[0]GP	I	VCC3		
GPI[29]		AE18	SATA[1]GP(Desktop)	I	VCC3		
GPI[30]		AF18	SATA[2]GP	I	VCC3		
GPI[31]		AG18	SATA[3]GP(Desktop)	I	VCC3		
GPO[28]	T3	LAN1 Enable	O	VCC3_SB			
GPO[27]	R3	LAN2 Enable	O	VCC3_SB			
GPIO[49]	AG25	H_PWRGD	OD	V_CPU_IO			

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	ATADET0
FPGI[1]	5	Main	3.3	pull-high
FPGI[2]	4	Main	3.3	pull-high
FPGI[3]	3	Main	3.3	pull-high
FPGI[4]	30	Main	3.3	pull-high

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/#GNT#	IDSEL	CLOCK
PCI Slot 1	PIROE PIROF PIROG PIROH	PCI_REQ#0 PCI_GNT#0	AD16	PCICLK0
PCI Slot 2	PIROF PIROG PIROH PIROE	PCI_REQ#1 PCI_GNT#1	AD17	PCICLK1
Riser Card (PCI Slot 1)		PCI_REQ#2 PCI_GNT#2		PCICLK2
Riser Card (PCI Slot 1)		PCI_REQ#3 PCI_GNT#3		PCICLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM2	(000)	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM1	(001)	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

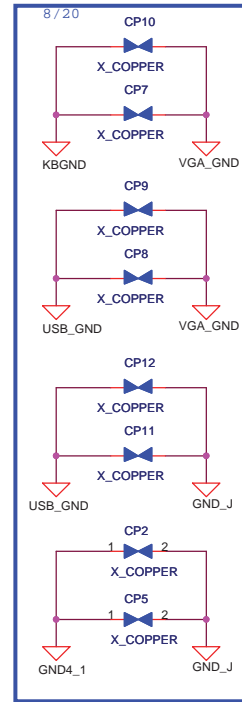
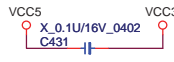
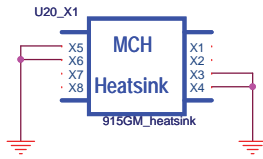
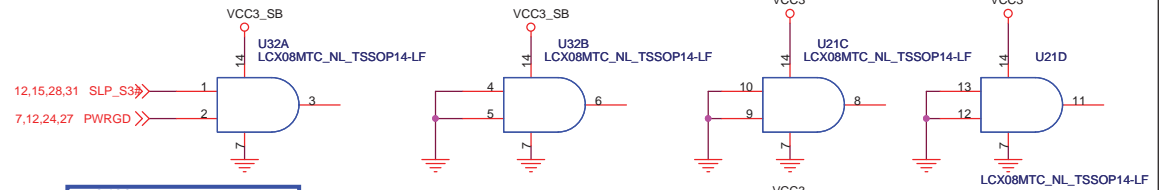
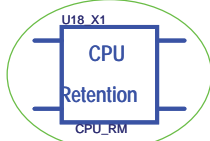
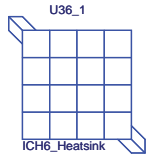
PCI Reset

DEVICE	Device
PLTRST# (ICH6-M)	PCIRST BUFFER
PCIRST_ICH6# (ICH6-M)	PCI Slot1 PCI Slot2
PCI_E_RST# (PCIRST BUF)	LAN1 Controller PCIE-1Slot PCIE-3Slot
PLTRST_MCH# (PCIRST BUF)	915GM(GMCH)
HD_RST# (PCIRST BUF)	IDE1
DEV_RST# (PCIRST BUF)	Super IO TPM Firmware Hub

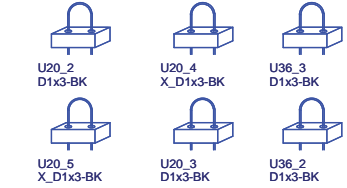
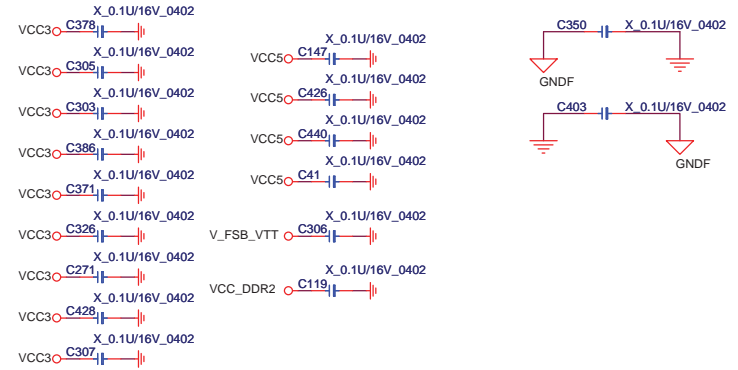
MANUAL PART

Change U36_X1 to E31-0401472-K08.2005.1.3
 Change U18_X1 to E91-0000082-L06.2005.1.3
 Change BIOS1_1 to POP. 2005.11.30
 Change U36_X1 back to E31-0401470-K08. 2005.3.14
 Change U36_X1 to E31-0401470-K08. 2005.5.10

Change BAT1_1 FROM CR2032 TO CR2450.
 10.01.2006

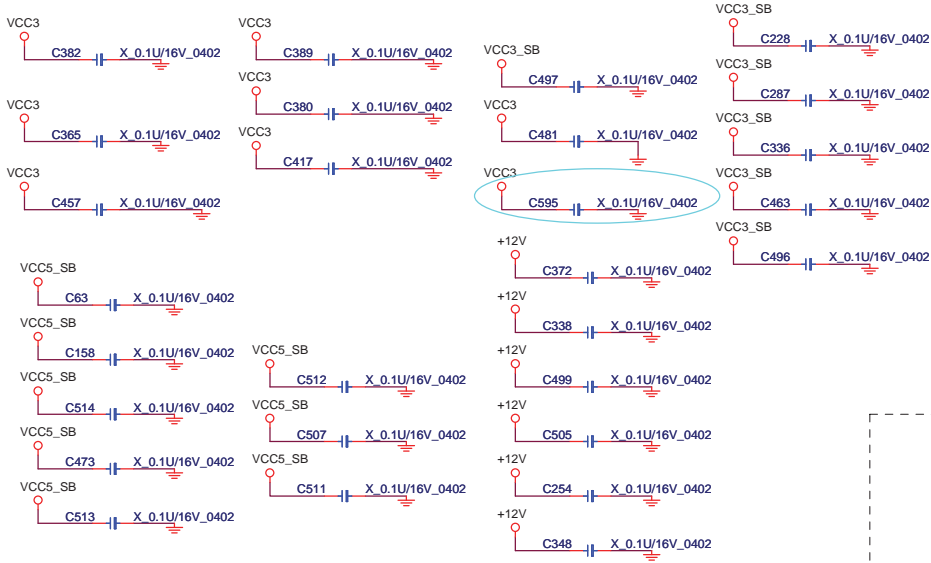


FOR EMI

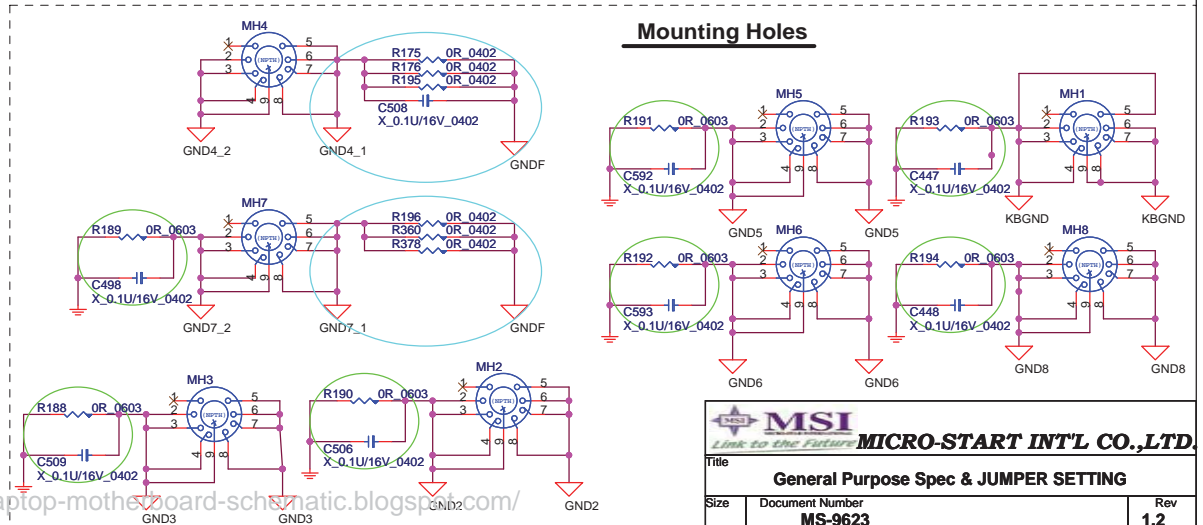


Change to N31-1031091-F02. 2005.5.10

FOR EMI



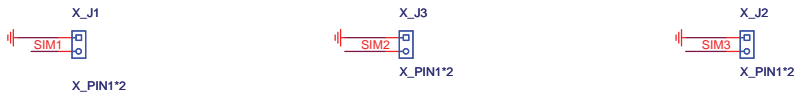
Mounting Holes



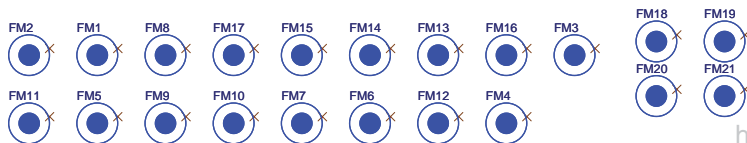
Layer1/5mil/55ohm

Layer6/5mil/55ohm

Layer4/4mil/55ohm



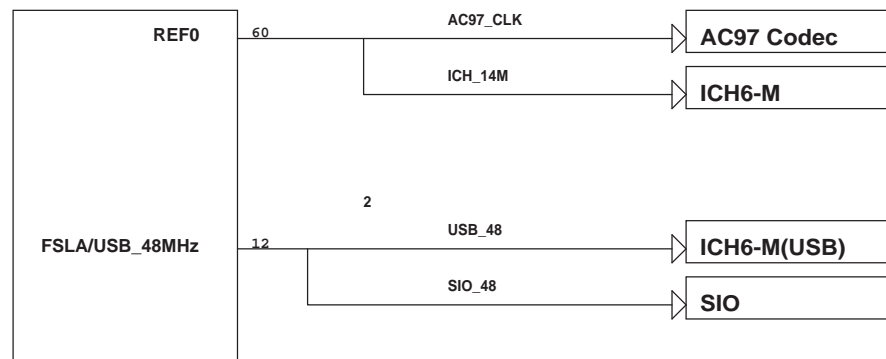
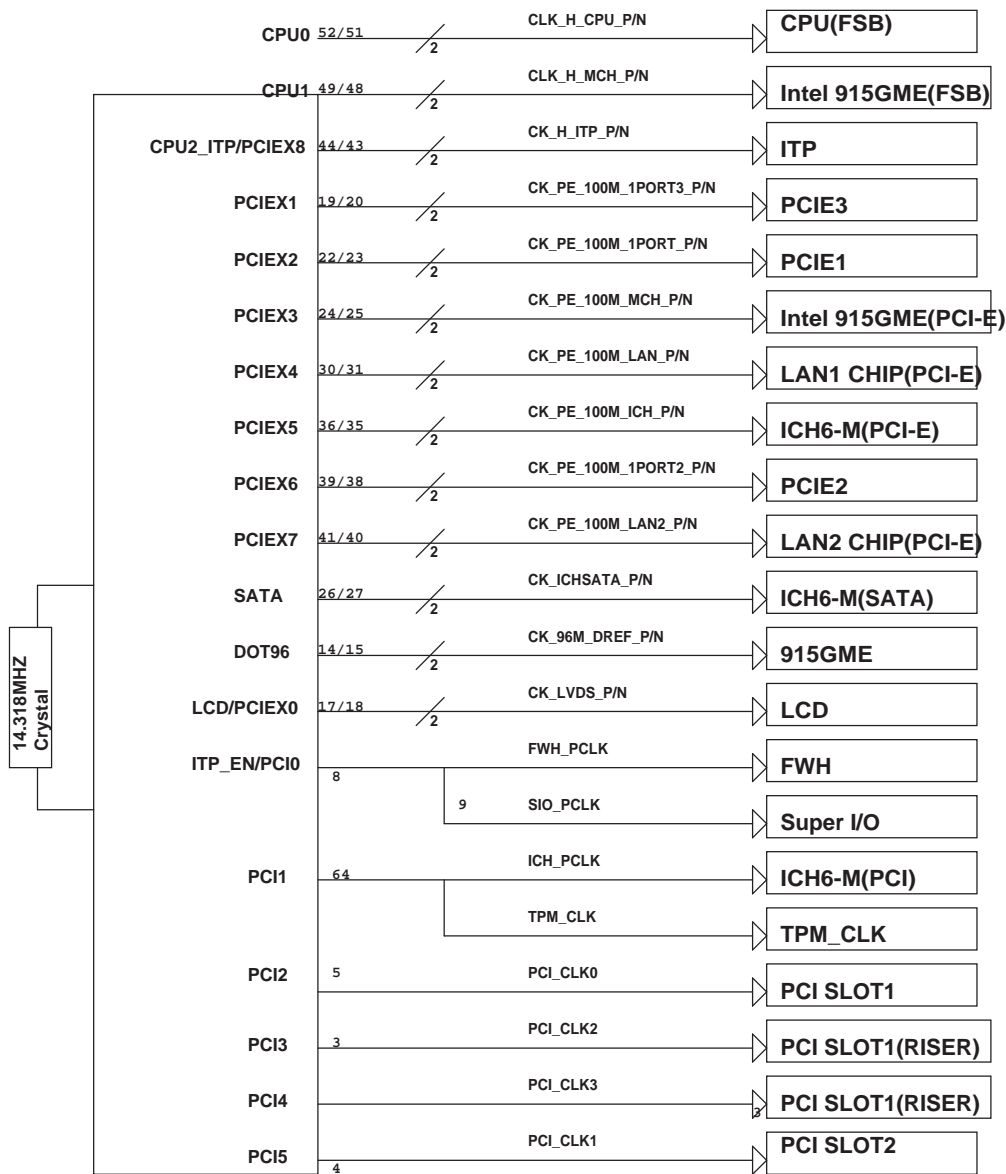
Optical Fiducial Marks



Title		
General Purpose Spec & JUMPER SETTING		
Size	Document Number	Rev
	MS-9623	1.2
Date:	Friday, August 24, 2007	Sheet 33 of 38

FX CLOCK BLOCK DIAGRAM

Clock Gen(ICS954310BGLF)

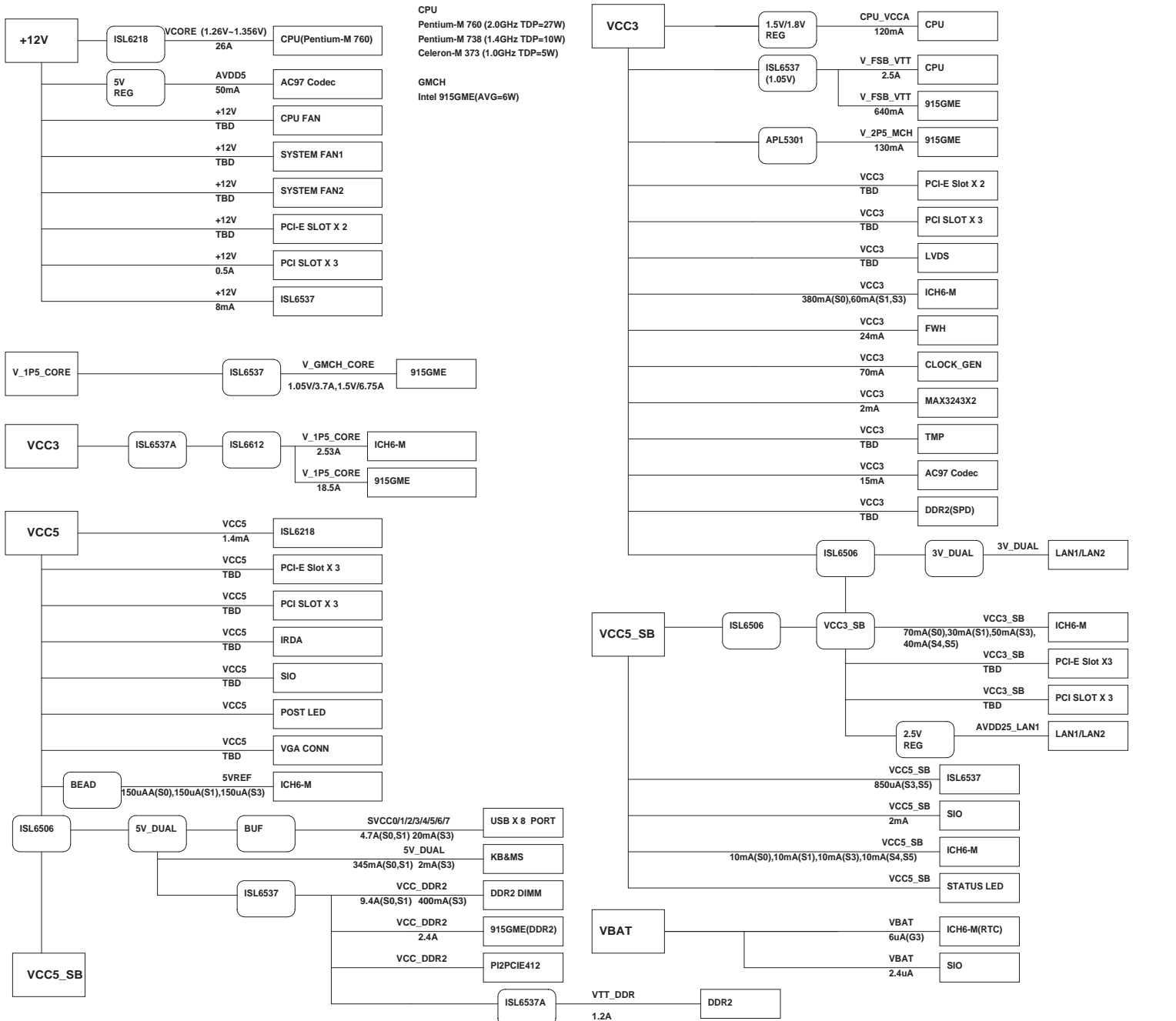


MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **System Clock Block Diagram**

Size	Document Number MS-9623	Rev 1.2
Date: Friday, August 24, 2007	Sheet 34 of 38	

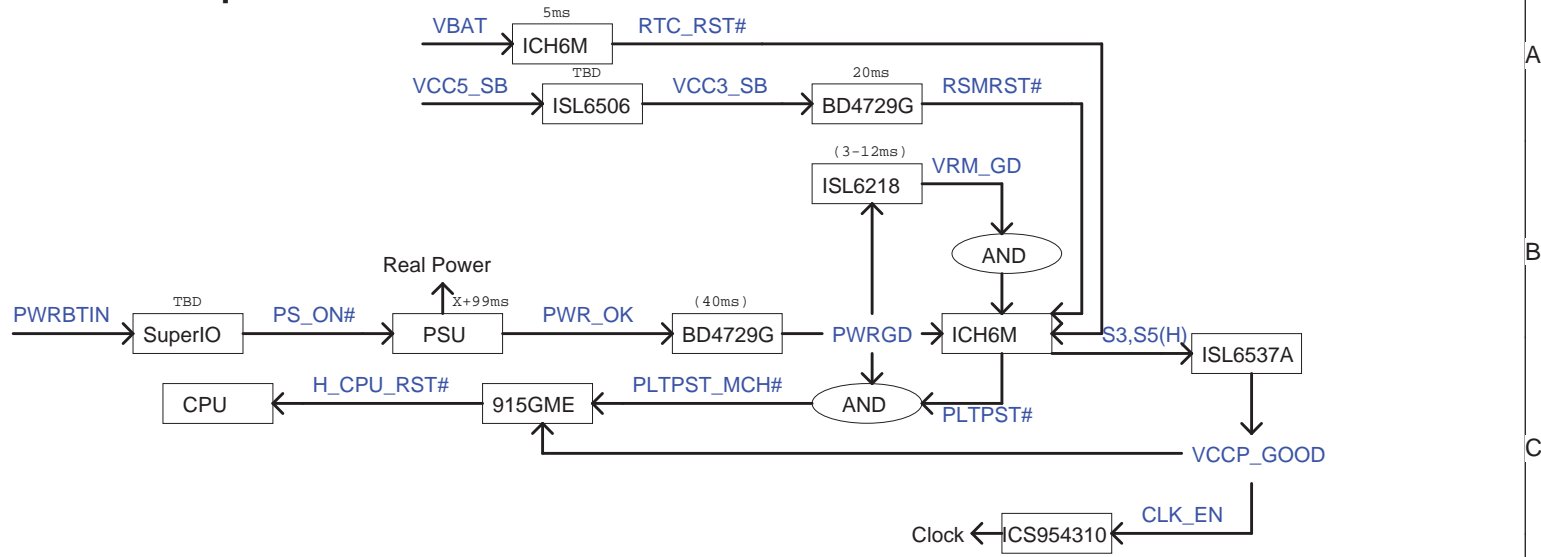
FX POWER DELIEVERY DIAGRAM



CPU
 Pentium-M 760 (2.0GHz TDP=27W)
 Pentium-M 738 (1.4GHz TDP=10W)
 Celeron-M 373 (1.0GHz TDP=5W)

GMCH
 Intel 915GME(AVG=6W)

Power on sequence



Power down sequence

